User's Manual

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RA6T2 Group

User's Manual: Hardware

32-bit MCU
Renesas Advanced (RA) Family
Renesas RA6 Series

Renesas Electronics
www.renesas.com

Rev.1.10 Dec 2021

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瑞萨电子高级(RA)系列32位MCU

Renesas RA6 Series

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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1. 防止静电放电(ESD)
   当暴露于CMOS器件时，强电场会导致栅极氧化物的破坏并最终降低器件的运行性能。脚步
   必须采取措施，尽可能停止静电的产生，并在出现时迅速消散。环境控制必须
   足够的。干燥时，应使用加湿器。建议避免使用容易产生静电的绝缘体。
   半导体器件必须在防静电容器、静电屏蔽袋或导电材料中储存和运输。所有测试和
   包括工作台和地板在内的测量工具必须接地。操作员还必须使用腕带接地。半导体
   不得赤手触摸设备。对于安装有半导体器件的印刷电路板，必须采取类似的预防措施。
2. 上电处理
   通电时产品的状态是不确定的。LSI内部电路的状态是不确定的，
   通电时寄存器设置和引脚未定义。在将复位信号施加到外部复位的成品中
   管脚，从通电到复位过程完成，管脚的状态不能保证。以类似的方式，引脚的状态
   在通过片内上电复位功能复位的产品中，从供电时间到供电达到
   指定重置的级别。
3. 断电状态下的信号输入
   请勿在设备断电时输入信号或IO上拉电源。输入此类信号或IO导致的电流注入
   上拉电源可能会导致故障，此时通过设备的异常电流可能会导致内部退化
   元素。请按照产品文档中所述的电源关闭状态下的输入信号指南进行操作。
4. 处理未使用的引脚
   按照手册中未使用引脚处理中给出的说明处理未使用的引脚。CMOS产品的输入引脚是
   一般处于高阻状态。在开路状态下使用未使用的引脚操作时，会在附近感应出额外的电磁噪声
   LSI，相关的直通电流在内部流动，并且由于将引脚状态错误识别为输入信号而发生故障
   成为可能。
5. 时钟信号
   应用复位后，只有在工作时钟信号稳定后才释放复位线。在程序中切换时钟信号时
   执行，等待目标时钟信号稳定。当时钟信号由外部谐振器或外部振荡器产生时
   在复位期间，确保只有在时钟信号完全稳定后才释放复位线。此外，当切换到时钟信号时
   在程序执行过程中由外部谐振器或外部振荡器产生，等待目标时钟信号稳定。
6. 输入引脚的电压施加波形
   由于输入噪声或反射波导致的波形失真可能会导致故障。如果CMOS器件的输入保持在VIL之间的区域
   (Max.)和VIH(Min.)由于噪音，例如，设备可能发生故障。小心，以防止颤动的噪音进入设备时，
   输入电平是固定的，并且在输入电平通过VIL(Max.)和VIH(Min.)之间的区域时的过渡期间也是如此。
7. 禁止访问保留地址
   禁止访问保留地址。保留地址是为将来可能的功能扩展提供的。不要访问这些
   不能保证LSI的正确操作。
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   在从一种产品更改为另一种产品之前，例如更改为具有不同部件号的产品，请确认更改不会导致问题。
   同一组中的微处理单元或微控制器单元产品的特性，但具有不同的部件号，其特性可能会有所不同
   内部存储器容量，布局模式和其他因素，这些因素会影响电气特性的范围，例如特性值，
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Preface

1. About this document

This manual is generally organized into an overview of the product, descriptions of the CPU, system control functions, peripheral functions, electrical characteristics, and usage notes. This manual describes the product specification of the microcontroller (MCU) superset. Depending on your product, some pins, registers, or functions might not exist. Address space that store unavailable registers are reserved.

2. Audience

This manual is written for system designers who are designing and programming applications using the Renesas Microcontroller. The user is expected to have basic knowledge of electrical circuits, logic circuits, and the MCU.

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Component	Document Type	Description
Microcontrollers	Data sheet	Features, overview, and electrical characteristics of the MCU
	User's Manual: Hardware	MCU specifications such as pin assignments, memory maps, peripheral functions, electrical characteristics, timing diagrams, and operation descriptions
	Application Notes	Technical notes, board design guidelines, and software migration information
	Technical Update (TU)	Preliminary reports on product specifications such as restriction and errata
Software	User's Manual: Software	API reference and programming information
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications
Tools & Kits, Solutions	User's Manual: Development Tools	User's manual and quick start guide for developing embedded software applications with Development Kits (DK), Starter Kits (SK), Promotion Kits (PK), Product Examples (PE), and Application Examples (AE)
	User's Manual: Software	
	Quick Start Guide	
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications

Preface

1. 关于本文档

本手册一般由产品概述、CPU说明、系统控制功能、外围功能、电气特性和使用说明组成。本手册描述了微控制器(MCU)超集的产品规格。根据您的产品，某些引脚、寄存器或功能可能不存在。保留存储不可用寄存器的地址空间。

2. Audience

本手册是为使用瑞萨微控制器设计和编程应用程序的系统设计人员编写的。要求用户具备电路、逻辑电路和MCU的基本知识。

3. Renesas Publications

瑞萨电子提供以下文件。在使用任何这些文档之前，请访问www.renesas.com以获取该文档的最新版本。

Component	文件类型	Description
Microcontrollers	数据表	MCU的特性、概述和电气特性
	User's Manual: Hardware	MCU规范，例如引脚分配、存储器映射、外设功能、电气特性、时序图和操作描述
	应用笔记	技术说明、电路板设计指南和软件迁移信息
	技术更新(TU)	限制、勘误等产品规格的初步报告
Software	User's Manual: Software	API参考和编程信息
	应用笔记	用于开发嵌入式软件应用程序的项目文件、软件编程指南和应用程序示例
工具和套件 解决方案	用户手册：开发工具	使用开发套件(DK)、入门套件(SK)、促销套件(PK)、产品示例(PE)和应用程序开发嵌入式软件应用程序的用户手册和快速入门指南
	User's Manual: Software	
	快速入门指南	Examples (AE)
	应用笔记	用于开发嵌入式软件应用程序的项目文件、软件编程指南和应用程序示例

4. Numbering Notation

The following numbering notation is used throughout this manual:

Example	Description
011b	Binary number. For example, the binary equivalent of the number 3 is 011b.
0x1F	Hexadecimal number. For example, the hexadecimal equivalent of the number 31 is described 0x1F. In some cases, a hexadecimal number is shown with the suffix "h".
1234	Decimal number. A decimal number is followed by this symbol only when the possibility of confusion exists. Decimal numbers are generally shown without a suffix.

5. Typographic Notation

The following typographic notation is used throughout this manual:

Example	Description
WDT.WDTRCR.RSTIRQS	Periods separated a function module symbol (WDT), register symbol (WDTRCR), and bit field symbol (RSTIRQS).
WDT.WDTRCR	A period separated a function module symbol (WDT) and register symbol (WDTRCR).
WDTRCR.RSTIRQS	A period separated a register symbol (WDTRCR) and bit field symbol (RSTIRQS).
CKS[3:0]	Numbers in brackets expresses a bit number. For example, CKS[3:0] occupies bits 3 to 0 of the WDT Control Register (WDTCR) register.

6. Unit and Unit Prefix

The following units and unit prefixes are sometimes misleading. Those unit prefixes are described throughout this manual with the following meaning:

Symbol	Name	Description
b	Binary Digit	Single 0 or 1
B	Byte	This unit is generally used for memory specification of the MCU and address space.
k	kilo-	1000 = 10^3. k is also used to denote 1024 (2^{10}) but this unit prefix is used to denote 1000 (10^3) throughout this manual.
K	Kilo-	1024 = 2^{10}. This unit prefix is used to denote 1024 (2^{10}) not 1000 (10^3) throughout this manual.

7. Special Terms

The following terms have special meanings.

Term	Description
NC	Not connected pin. NC means that pin is not connected to the MCU.
Hi-Z	High impedance.

4. 编号符号

本手册通篇使用以下编号符号：

Example	Description
011b	二进制数。例如，数字3的二进制等价物是011b。
0x1F	十六进制数。例如，数字31的十六进制等效项被描述为0x1F。在某些情况下，显示的十六进制数带有后缀“h”。
1234	十进制数。仅当存在混淆的可能性时，才在十进制数后面加上此符号。十进制数字通常不带后缀。

5. 排版符号

本手册通篇使用以下印刷符号：

Example	Description
WDT.WDTRCR.RSTIRQS	句点分隔功能模块符号(WDT)、寄存器符号(WDTRCR)和位域符号(RSTIRQS)。
WDT.WDTRCR	句点分隔功能模块符号(WDT)和寄存器符号(WDTRCR)。
WDTRCR.RSTIRQS	一个句点分隔寄存器符号(WDTRCR)和位域符号(RSTIRQS)。
CKS[3:0]	括号中的数字表示一个位数。例如，CKS[3:0]占用WDT的3到0位 控制寄存器(WDTCR)寄存器。

6. 单位和单位前缀

以下单位和单位前缀有时会产生误导。这些单位前缀在本手册中进行了描述，含义如下：

Symbol	Name	Description
b	二进制数字	单个0或1
B	Byte	该单元一般用于MCU的内存规范和地址空间。
k	kilo-	1000=103。k也用于表示1024(210)，但在本手册中，此单位前缀用于表示1 000(103)。
K	Kilo-	1024=210。在本手册中，该单位前缀用于表示1024(210)而不是1000(103)。

7. 特别条款

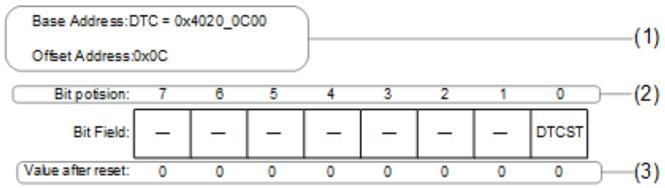
以下术语具有特殊含义。

Term	Description
NC	未连接引脚。NC表示该引脚未连接到MCU。
Hi-Z	高阻抗。

8. Register Description

Each register description includes both a register diagram that shows the bit assignments and a register bit table that describes the content of each bit. The example of symbols used in these tables are described in the sections that follow. The following is an example of a register description and associated bit field definition.

XXXX DTCST : DTC Module Start Register



(4) (5) (6)

Bit	Symbol	Function	R/W
0	DTCST	DTC Module Start 0:DTC module stop 1:DTC module start	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

(1) Function module symbol, register symbol, and address assignment

Function module symbol, register symbol, and address assignment of this register are generally expressed. Base Address and Offset Address mean DTC Module Start Register (DTCST) of Data Transfer Controller (DTC) is assigned to address 0x4020_0C00.

(2) Bit number

This number indicates the bit number. This bits are shown in order from bits 31 to 0 for 32-bit register, from bits 15 to 0 for 16-bit register, and from bits 7 to 0 for 8-bit register.

(3) Value after reset

This symbol or number indicate the value of each bit after a hard reset. The value is shown in binary unless specified otherwise.

0: Indicates that the value is 0 after a reset.

1: Indicates that the value is 1 after a reset.

x: Indicates that the value is undefined after a reset.

(4) Symbol

Symbol indicates the short name of bit field. Reserved bit is expressed with a —.

(5) Function

Function indicates the full name of the bit field and enumerated values.

(6) R/W

The R/W column indicates access type whether the bit field is readable or writable.

R/W: The bit field is readable and writable.

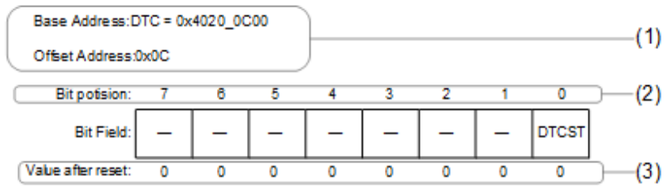
R: The bit field is readable only. Writing to this bit field has no effect.

W: The bit field is writable only. The read value is the same as after a reset unless specified otherwise.

8. 注册说明

每个寄存器描述都包括一个显示位分配的寄存器图和一个描述每个位内容的寄存器位表。这些表中使用的符号示例将在以下部分中描述。以下是寄存器描述和相关位字段定义的示例。

XXXX DTCST : DTC Module Start Register



(4) (5) (6)

Bit	Symbol	Function	R/W
0	DTCST	DTC Module Start 0:DTC module stop 1:DTC module start	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

(1)功能模块符号、寄存器符号、地址分配

一般表示该寄存器的功能模块符号、寄存器符号、地址分配。基地址和偏移地址意味着数据传输控制器(DTC)的DTC模块起始寄存器(DTCST)分配到地址0x4020_0C00。

(2)位号

该数字表示位数。对于32位寄存器，这些位按位31到0、16位寄存器从位15到0、8位寄存器从位7到0的顺序显示。

(3)复位后的值

该符号或数字表示硬复位后每个位的值。除非另有说明，否则该值以二进制显示。

0：表示复位后值为0。

1：表示复位后值为1。

x：表示复位后该值未定义。

(4) Symbol

符号表示位域的简称。保留位用—表示。

(5) Function

函数表示位域的全称和枚举值。

(6) R/W

RW列指示位字段是可读还是可写的访问类型。

RW：位域可读可写。

R：位域是只读的。写入该位域无效。

W：位域只可写。除非另有说明，否则读取的值与复位后的值相同。

9. Abbreviations

Abbreviations used in this document are shown in the following table.

Abbreviation	Description
AES	Advanced Encryption Standard
AHB	Advanced High-performance Bus
AHB-AP	AHB Access Port
APB	Advanced Peripheral Bus
ARC	Alleged RC
ATB	Advanced Trace Bus
BCD	Binary Coded Decimal
BSDL	Boundary Scan Description Language
DES	Data Encryption Standard
DSA	Digital Signature Algorithm
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell
FLL	Frequency Locked Loop
FPU	Floating Point Unit
HMI	Human Machine Interface
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NVIC	Nested Vector Interrupt Controller
PC	Program Counter
PFS	Port Function Select
PLL	Phase Locked Loop
POR	Power-on reset
PWM	Pulse Width Modulation
RSA	Rivest Shamir Adleman
SHA	Secure Hash Algorithm
S/H	Sample and Hold
SP	Stack Pointer
SWD	Serial Wire Debug
SW-DP	Serial Wire-Debug Port
TRNG	True Random Number Generator
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

9. Abbreviations

本文档中使用的缩写如下表所示。

Abbreviation	Description
AES	高级加密标准
AHB	先进的高性能总线
AHB-AP	AHB访问端口
APB	先进的外围总线
ARC	Alleged RC
ATB	高级跟踪总线
BCD	二进制编码的十进制
BSDL	边界扫描描述语言
DES	数据加密标准
DSA	数字签名算法
ETB	嵌入式跟踪缓冲区
ETM	嵌入式跟踪宏单元
FLL	锁频环
FPU	浮点单元
HMI	人机接口
IrDA	红外数据协会
LSB	最低有效位
MSB	最高有效位
NVIC	嵌套向量中断控制器
PC	程序计数器
PFS	端口功能选择
PLL	锁相环
POR	Power-on reset
PWM	脉冲宽度调制
RSA	Rivest Shamir Adleman
SHA	安全哈希算法
S/H	采样和保持
SP	堆栈指针
SWD	串口线调试
SW-DP	串行线调试端口
TRNG	真随机数发生器
UART	通用异步收发器
VCO	压控振荡器

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Contents

Contents

High-performance 240 MHz Arm Cortex-M33 core, up to 512 KB code flash memory with background operation, 16 KB Data flash memory, and 64 KB SRAM with ECC. Integrated 12-bit A/D Converter with sample-and-hold circuit for simultaneous sampling and single-end/pseudo-differential input supportive amplifier. Integrated General PWM Timer with 200 MHz operation and high resolution. Integrated Secure Cryptographic Engine with cryptography accelerators and key management support in concert with Arm TrustZone for integrated secure element functionality.

Features

■ Arm® Cortex®-M33 Core

- Armv8-M architecture with the main extension
- Maximum operating frequency: 240 MHz
- Arm Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two Systick timers: Secure and Non-secure instance
  - Driven by LOCO or system clock
- CoreSight™ ETM-M33

■ Memory

- Up to 512-KB code flash memory
- 16-KB data flash memory (125,000 program/erase (P/E) cycles)
- 64-KB SRAM

■ Connectivity

- Serial Communications Interface (SCI) × 6
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Smart card interface
  - Simple IIC
  - Simple SPI
  - Simple LIN
  - Manchester coding
- I^2C bus interface (IIC) × 2
  - Transfer at up to 3.2 Mpbs (high speed mode)
- Serial Peripheral Interface (SPI) × 2
- CAN with Flexible Data-rate (CANFD)

■ Analog

- 12-bit A/D Converter (ADC) × 2
  - Sample-and-hold circuits × 6
  - Programmable Gain Amplifier × 4
- High-Speed Analog Comparator (ACMPHS) × 4
- 12-bit D/A Converter (DAC12) × 4
- Temperature Sensor (TSN)

■ Timers

- General PWM Timer 32-bit (GPT32) with High Resolution × 4
  - 156 ps resolution in 200 MHz
- General PWM Timer 32-bit (GPT32) × 6
- Low Power Asynchronous General Purpose Timer (AGT) × 2

■ Security and Encryption

- Secure Cryptographic Engine (SCE5)
  - Symmetric algorithms: AES
  - Hash-value generation: GHASH
  - 128-bit unique ID
- Arm® TrustZone®
  - Up to three regions for the code flash
  - Up to two regions for the data flash
  - Up to three regions for the SRAM
  - Individual secure or non-secure security attribution for each peripheral
- Device lifecyle management

■ System and Power Management

- Low power modes
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- DMA Controller (DMAC) × 8
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings
- Watchdog Timer (WDT)
- Independent Watchdog Timer (IWDT)
- Key Interrupt Funciton (KINT)

■ Data Processing Accelerator

- Trigonometric Function Unit (TFU)
- IIR Filter Accelerator (IIRFA)

■ Multiple Clock Sources

- Main clock oscillator (MOSC) (8 to 24 MHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- PLL/PLL2
- Clock out support

■ General-Purpose I/O Ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Operating Voltage

- VCC: 2.7 to 3.6 V

■ Operating Temperature and Packages

- Ta = -40°C to +105°C
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 64-pin QFN (8 mm × 8 mm, 0.4 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)

高性能240MHzArmCortex-M33内核、高达512KB的后台运行代码闪存、16KB数据闪存和带ECC的64KBSRAM。集成12位AD转换器，带有用于同步采样的采样保持电路和单端伪差分输入支持放大器。具有200MHz操作和高分辨率的集成通用PWM定时器。具有加密加速器和密钥管理支持的集成安全加密引擎与ArmTrustZone相结合，可实现集成安全元件功能。

Features

■Arm®Cortex®-M33内核

●带有主扩展的Armv8-M架构●最大工作频率：240MHz●Arm内存保护单元（ArmMPU）

受保护的内存系统架构(PMSAv8) 安全MPU(MPU_S)：8个区域 非安全MPU(MPU_NS)：8个区域●SysTick计时器

嵌入两个Systick计时器：安全和非安全实例 由LOCO或系统时钟驱动●CoreSight ETM-M33

■ Memory

●高达512-KB代码闪存●16-KB数据闪存（125 000次程序擦除(PE)周期）●64-KBSRAM

■ Connectivity

●串行通信接口(SCI)×6 异步接口 8位时钟同步接口 智能卡接口 SimpleIIC SimpleSPI SimpleLIN Manchester编码●I2C总线接口(IIC)×2

传输速率高达3.2Mpbs（高速模式）●串行外设接口(SPI)×2●具有灵活数据速率的CAN(CANFD)

■ Analog

●12位模数转换器(ADC)×2 采样保持电路×6 可编程增益放大器×4●高速模拟比较器(ACMPHS)×4●12位数模转换器(DAC12)×4●温度传感器(TSN)

■ Timers

●通用PWM定时器32位(GPT32)，高分辨率×4 156ps分辨率，200MHz●通用PWM定时器32位(GPT32)×6●低功耗异步通用定时器(AGT)×2

■安全和加密

●安全加密引擎(SCE5) 对称算法：AES 哈希值生成：GHASH 128位唯一ID●Arm®TrustZone®

代码闪存最多三个区域 数据闪存最多两个区域 SRAM最多三个区域 每个外围设备的单独安全或非安全安全属性●设备生命周期管理

■系统和电源管理●低功耗模式●事件链接控制器(ELC)●数据传输控制器(DTC)●DMA控制器(DMAC)×8●上电复位●具有电压设置的低电压检测(LVD)●看门狗定时器(WDT)●独立看门狗定时器(IWDT)●按键中断功能(KINT)

■数据处理加速器

●三角函数单元(TFU)●IIR滤波器加速器(IIRFA)

■多个时钟源

●主时钟振荡器（MOSC）（8至24MHz）●高速片上振荡器（HOCO）（161820MHz）●中速片上振荡器（MOCO）（8MHz）●低速开启片上振荡器(LOCO)(32.768kHz)●IWDT专用片上振荡器(15kHz)●HOCOMOCOLOCO的时钟微调功能●PLLPLL2●时钟输出支持

■ General-Purpose I/O Ports

●5V容差、开漏、输入上拉、可切换驱动能力

■工作电压●VCC：2.7至3.6V

■工作温度和封装●Ta=-40℃to+105℃

100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
- 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
- 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
- 64-pin QFN (8 mm × 8 mm, 0.4 mm pitch)
- 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M33 core running up to 240 MHz with the following features:

- Up to 512 KB code flash memory
- 64 KB SRAM
- General PWM Timer (GPT) - Enhanced High Resolution
- Analog peripherals
- Security and safety features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M33 core	• Maximum operating frequency: up to 240 MHz • Arm Cortex-M33 core: – Armv8-M architecture with security extension – Revision: r0p4-00rel0 • Arm Memory Protection Unit (Arm MPU) – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – Embeds two Systick timers: Secure and Non-secure instance – Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK) • CoreSight™ ETM-M33

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 512 KB of code flash memory. See section 43, Flash Memory.
Data flash memory	16 KB of data flash memory. See section 43, Flash Memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 6, Option-Setting Memory.
SRAM	On-chip high-speed SRAM with Error Correction Code (ECC). See section 41, SRAM.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI boot mode See section 3, Operating Modes.
Resets	The MCU provides 14 resets. See section 5, Resets.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds. See section 7, Low Voltage Detection (LVD).

1. Overview

该MCU集成了多个基于Arm®软件兼容的32位内核，这些内核共享一组通用的瑞萨外设，以促进设计可扩展性和高效的基于平台的产品开发。

该系列中的MCU包含一个运行频率高达240MHz的高性能ArmCortex®-M33内核，具有以下特性：

●高达512KB的代码闪存
- 64 KB SRAM
●通用PWM定时器(GPT)增强型高分辨率
●模拟外设
●安全和安全功能

1.1 功能概要

Table 1.1 臂芯

Feature	功能说明
ArmCortex-M33内核	• 最大工作频率：高达240MHz • Arm Cortex-M33 core: – 带有安全扩展的Armv8-M架构 – Revision: r0p4-00rel0 • Arm内存保护单元（ArmMPU） – 受保护的内存系统架构(PMSAv8) – 安全MPU(MPU_S)：8个区域 – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – 嵌入两个Systick计时器：安全和非安全实例 – 由SysTick定时器时钟(SYSTICCLK)或系统时钟(ICLK)驱动 • CoreSight™ ETM-M33

Table 1.2 Memory

Feature	功能说明
代码闪存	最大512KB的代码闪存。 请参阅第43节，闪存。
数据闪存	16KB数据闪存。请参阅第43节 ，闪存。
Option-setting memory	选项设置存储器确定复位后MCU的状态。 请参阅第6节，选项设置内存。
SRAM	具有纠错码(ECC)的片上高速SRAM。 参见第41节，SRAM。

Table 1.3 系统(1of2)

Feature	功能说明
操作模式	两种操作模式：● • SCI开机模式 请参阅第3节，操作模式。
Resets	MCU提供14次复位。 请参阅第5节，重置。
低电压检测(LVD)	低电压检测(LVD)模块监控输入到VCC引脚的电压电平。检测等级可以通过寄存器设置来选择。LVD模块由三个独立的电压电平检测器（LVD0、LVD1、LVD2）组成。LVD0、LVD1和LVD2测量输入到VCC引脚的电压电平。LVD寄存器允许您的应用程序配置在各种电压阈值下检测VCC变化。请参见第7节，低电压检测(LVD)。

Table 1.3 System (2 of 2)

Feature	Functional description
Clocks	• Main clock oscillator (MOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • PLL/PLL2 • Clock out support See section 8, Clock Generation Circuit.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 9, Clock Frequency Accuracy Measurement Circuit (CAC).
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts. See section 12, Interrupt Controller Unit (ICU).
Key Interrupt Function (KINT)	The key interrupt function (KINT) generates the key interrupt by detecting rising or falling edge on the key interrupt input pins. See section 19, Key Interrupt Function (KINT).
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 10, Low Power Modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR). See section 11, Register Write Protection.
Memory Protection Unit (MPU)	The MCU has one Memory Protection Unit (MPU). See section 14, Memory Protection Unit (MPU).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention. See section 17, Event Link Controller (ELC).

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 16, Data Transfer Controller (DTC).
DMA Controller (DMAC)	The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 15, DMA Controller (DMAC).

Table 1.6 Timers (1 of 2)

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 10 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 21, General PWM Timer (GPT).

Table 1.3 系统(2之2)

Feature	功能说明
Clocks	• 主时钟振荡器(MOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • PLL/PLL2 • 打卡支持 请参见第8节，时钟生成电路。
时钟频率精度测量电路(CAC)	时钟频率精度测量电路(CAC)在选择作为测量基准的时钟（测量基准时钟）产生的时间内对要测量的时钟（测量目标时钟）的脉冲进行计数，并根据脉冲数在允许范围内。当测量完成或测量参考时钟产生的时间内的脉冲数不在允许范围内时，将产生中断请求。请参见第9节，时钟频率精度测量电路(CAC)。
中断控制器单元(ICU)	中断控制器单元(ICU)控制哪些事件信号链接到嵌套向量中断控制器(NVIC)、DMA控制器(DMAC)和数据传输控制器(DTC)模块。ICU还控制不可屏蔽的中断。请参阅第12节，中断控制器单元(ICU)。
按键中断功能(KINT)	按键中断功能(KINT)通过检测按键中断输入引脚的上升沿或下降沿来产生按键中断。请参见第19节，按键中断功能(KINT)。
低功耗模式	可以通过多种方式降低功耗，包括设置时钟分频器、停止模块、在正常操作中选择电源控制模式以及转换到低功耗模式。请参阅第10节，低功耗模式。
寄存器写保护	寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。要保护的寄存器由保护寄存器(PRCR)设置。请参见第11节，寄存器写保护。
内存保护单元(MPU)	MCU有一个内存保护单元(MPU)。 请参阅第14节，内存保护单元(MPU)。

Table 1.4 活动链接

Feature	功能说明
事件链接控制器(ELC)	EventLinkController(ELC)使用各种外围模块产生的事件请求作为源信号，将它们连接到不同的模块，允许模块之间直接链接，无需CPU干预。请参阅第17节，事件链接控制器(ELC)。

Table 1.5 直接内存访问

Feature	功能说明
数据传输控制器(DTC)	数据传输控制器(DTC)模块用于在被中断请求激活时传输数据。请参阅第16节，数据传输控制器(DTC)。
DMA Controller (DMAC)	MCU包括一个8通道直接内存访问控制器(DMAC)，无需CPU干预即可传输数据。当产生DMA传输请求时，DMAC将存储在传输源地址的数据传输到传输目标地址。请参见第15节，DMA控制器(DMAC)。

Table 1.6 计时器(1of2)

Feature	功能说明
通用PWM定时器(GPT)	通用PWM定时器(GPT)是一个具有GPT32×10通道的32位定时器。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。此外，可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。请参见第21节，通用PWM定时器(GPT)。

Table 1.6 Timers (2 of 2)

Feature	Functional description
PWM Delay Generation Circuit (PDG)	The PWM Delay Generation circuit (PDG) has 4 channels delay circuits that can connect to the GPT. The PDG can control the rise and fall edge timing with which the PWM output for the GPT320 through the GPT323. See section 22, PWM Delay Generation Circuit (PDG).
Port Output Enable for GPT (POEG)	The POEG issues requests to stop output from output pins of the general PWM timer (GPT). Select the method of detection for stopping the output from the list below. See section 20, Port Output Enable for GPT (POEG).
Low power Asynchronous General Purpose Timer (AGT)	The low power Asynchronous General Purpose Timer (AGT) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register. See section 23, Low Power Asynchronous General Purpose Timer (AGTW).
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt. See section 24, Watchdog Timer (WDT).
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers. See section 25, Independent Watchdog Timer (IWDT).

Table 1.7 Communication interfaces

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 6 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Simple LIN ● Smart card interface ● Manchester interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0 to 4, 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 26, Serial Communications Interface (SCI).
I^2C bus interface (IIC)	The I^2C bus interface (IIC) has 2 channels. The IIC module conform with and provide a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions. See section 27, I^2C Bus Interface (IIC).
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) has 2 channels. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 30, Serial Peripheral Interface (SPI).
CAN with Flexible Data-rate (CANFD)	The CAN with Flexible Data-rate (CANFD) module can handle classical CAN frames and CAN-FD frames complied with ISO 11898-1 standard. The module supports 4 transmit buffers and 32 receive buffer. See section 28, CAN with Flexible Data-rate (CANFD).

Table 1.6 计时器（2个中的2个）

Feature	功能说明
PWM延迟产生电路(PDG)	PWM延迟生成电路(PDG)有4个通道的延迟电路，可以连接到GPT。PDG可以控制PWM输出的上升沿和下降沿时序GPT320通过GPT323。 请参见第22节，PWM延迟生成电路(PDG)。
GPT(POEG)的端口输出使能	POEG发出请求以停止通用PWM定时器(GPT)的输出引脚的输出。从下表中选择停止输出的检测方法。 请参阅第20节，GPT(POEG)的端口输出启用。
低功耗异步通用目的定时器(AGT)	低功耗异步通用定时器(AGT)是一个32位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。该定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配到同一个地址，可以通过AGT寄存器访问。请参见第23节，低功耗异步通用定时器(AGTW)。
看门狗定时器(WDT)	看门狗定时器(WDT)是一个14位递减计数器，可用于在计数器下溢时复位MCU，因为系统已失控且无法刷新WDT。此外，WDT可用于产生不可屏蔽中断或下溢中断。请参见第24节，看门狗定时器(WDT)。
独立看门狗定时器(IWDT)	独立看门狗定时器(IWDT)包含一个14位递减计数器，必须定期对其进行服务以防止计数器下溢。IWDT提供复位MCU或生成不可屏蔽中断或下溢中断的功能。由于定时器使用独立的专用时钟源运行，因此当系统失控时，它在将MCU作为故障安全机制返回到已知状态时特别有用。IWDT可以通过复位、下溢、刷新错误或寄存器中的计数值的刷新来自动触发。请参见第25节，独立看门狗定时器(IWDT)。

Table 1.7 通讯接口

Feature	功能说明
串行通信接口(SCI)	串行通信接口(SCI)×6通道具有异步和同步串行接口：● 异步接口（UART和异步通信接口适配器(ACIA)） ● 8位时钟同步接口 ● Simple IIC (master-only) ● 简单的SPI ● 简单的LIN ● 智能卡接口 ● 曼彻斯特界面 智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。SCIn(n=0到4 9)具有FIFO缓冲区以实现连续和全双工通信，并且可以使用片上波特率发生器独立配置数据传输速度。参见第26节，串行通信接口(SCI)。
I2C总线接口(IIC)	I2C总线接口(IIC)有2个通道。IIC模块符合并提供NXPI2C（内部集成电路）总线接口功能的子集。参见第27节，I2C总线接口(IIC)。
串行外设接口(SPI)	串行外设接口(SPI)有2个通道。SPI提供与多个处理器和外围设备的高速全双工同步串行通信。请参阅第30节，串行外设接口(SPI)。
具有灵活数据速率的CAN(CANFD)	具有灵活数据速率(CANFD)模块的CAN可以处理经典CAN帧和CAN FD框架符合ISO11898-1标准。 该模块支持4个发送缓冲区和32个接收缓冲区。 请参阅第28节，具有灵活数据速率的CAN(CANFD)。

Table 1.8 Analog

Feature	Functional description
12-bit A/D Converter (ADC)	The 12-bit A/D Converter (ADC) has two units of 12-bit successive approximation A/D Converters with sample-and-hold circuits and programmable gain amplifiers (PGA) provided. The A/D converter unit 0 (ADC0) can select up to 21 channels of analog inputs. The A/D converter unit 1 (ADC1) can select up to 17 channels of analog inputs. The temperature sensor, internal reference voltage, and D/A converters can be A/D-converted by ADC0 or ADC1. See section 36, 12-Bit A/D Converter (ADC).
12-bit D/A Converter (DAC12)	A 12-bit D/A converter (DAC12) is provided. See section 37, 12-Bit D/A Converter (DAC12).
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 39, High-Speed Analog Comparator (ACMPHS).
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC for conversion and can be further used by the end application. See section 38, Temperature Sensor (TSN).

Table 1.9 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC)	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows to monitor the access to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 31, Cyclic Redundancy Check (CRC).
Data Operation Circuit (DOC)	The data operation circuit (DOC) is used to compare, add, and subtract 16 or 32-bit data. An interrupt can be generated when the following conditions apply. ● When the 16 or 32-bit compared values match the detection condition ● When the result of 16 or 32-bit data addition overflows ● When the result of 16 or 32-bit data subtraction underflows See section 40, Data Operation Circuit (DOC).

Table 1.10 Data processing accelerator

Feature	Functional description
Trigonometric function unit (TFU)	Calculation of sine, cosine, arctangent, and $\sqrt{x^2+y^2}$ ● A sine and cosine can be simultaneously calculated. ● An arctangent and $\sqrt{x^2+y^2}$ can be simultaneously calculated.
IIR Filter Accelerator (IIRFA)	● 16 channels of biquad IIR filter ● cascaded biquad filter (max.32 stages) ● Operations using single-precision floating-point numbers

Table 1.11 Security

Feature	Functional description
Securty function	● ARMv8-M TrustZone security ● Device lifecycle management ● Debug access level ● Key injection
Secure Cryptographic Engine (SCE5)	● Symmetric algorithms: AES ● Hash-value generation: GHASH ● 128-bit unique ID. See section 35, Secure Cryptographic Engine (SCE5).

Table 1.8 Analog

Feature	功能说明
12-bit A/D Converter (ADC)	12位AD转换器(ADC)有两个单元12位逐次逼近AD 提供带有采样保持电路和可编程增益放大器(PGA)的转换器。 AD转换器单元0(ADC0)最多可以选择21个模拟输入通道。AD转换器单元1(ADC1)最多可以选择17个模拟输入通道。温度传感器、内部参考电压和DA转换器可通过ADC0或ADC1进行AD转换。 请参阅第36节，12位模数转换器(ADC)。
12-bit D/A Converter (DAC12)	提供了一个12位DA转换器(DAC12)。 请参阅第37节，12位DA转换器(DAC12)。
高速模拟比较器(ACMPHS)	高速模拟比较器(ACMPHS)将测试电压与参考电压进行比较，并根据转换结果提供数字输出。测试电压和参考电压都可以从内部源（例如DAC12输出和内部参考电压）以及带有或不带有内部PGA的外部源提供给比较器。这种灵活性在需要在模拟信号之间执行go-no-go比较而不一定需要AD转换的应用中很有用。请参见第39节，高速模拟比较器(ACMPHS)。
温度传感器(TSN)	片上温度传感器(TSN)确定并监控芯片温度，以确保器件可靠运行。传感器输出与管芯温度成正比的电压，管芯温度与输出电压之间的关系相当线性。输出电压提供给ADC进行转换，并可进一步供最终应用使用。请参见第38节，温度传感器(TSN)。

Table 1.9 数据处理

Feature	功能说明
循环冗余校验(CRC)	循环冗余校验(CRC)生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外，还可以使用各种CRC生成多项式。snoop功能允许监视对特定地址的访问。此功能在需要在某些事件中自动生成CRC代码的应用中很有用，例如监视对串行发送缓冲区的写入和从串行接收缓冲区的读取。请参阅第31节，循环冗余校验(CRC)。
数据运算电路(DOC)	数据运算电路(DOC)用于对16位或32位数据进行比较、加法和减法。当以下条件适用时，可以产生中断。● 当16位或32位比较值与检测条件匹配时 ● 当16位或32位数据相加结果溢出时 ● 当16位或32位数据减法的结果下溢时 请参见第40节，数据操作电路(DOC)。

Table 1.10 数据处理加速器

Feature	功能说明
三角函数单元(TFU)	计算正弦、余弦、反正切和x2+y2 可以同时计算正弦和余弦。 可以同时计算反正切和x2+y2。
IIR滤波器加速器(IIRFA)	V16通道双二阶IIR滤波器 级联双二阶滤波器（最多32级） 使用单精度浮点数的运算

Table 1.11 Security

Feature	功能说明
安全功能	● ARMv8-M TrustZone security ● 设备生命周期管理 ● 调试访问级别 ● 密钥注入
安全加密引擎(SCE5)	● Symmetric algorithms: AES ● Hash-value generation: GHASH ●128位唯一标识。请参阅第35节，安全加密引擎(SCE5)。

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

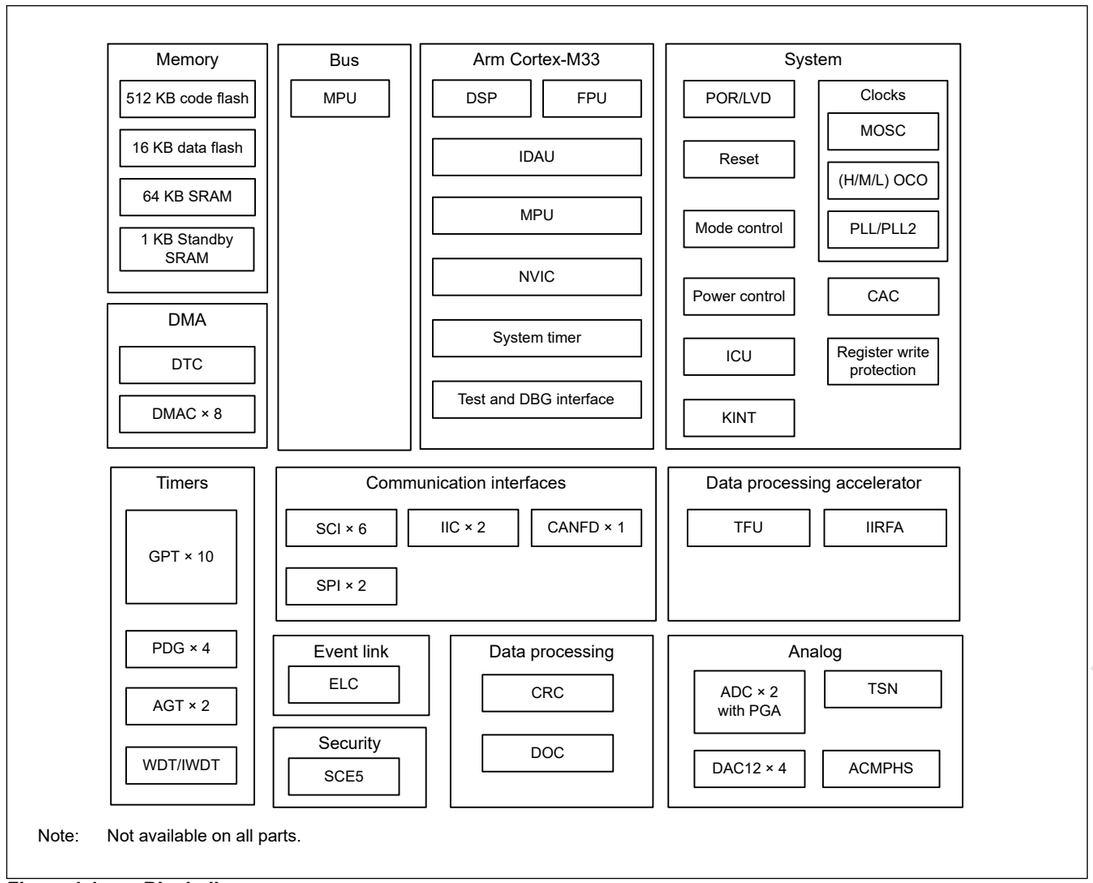


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a list of products.

1.2 框图

图1.1显示了MCU超集的框图。组内的某些单独设备具有部分功能。

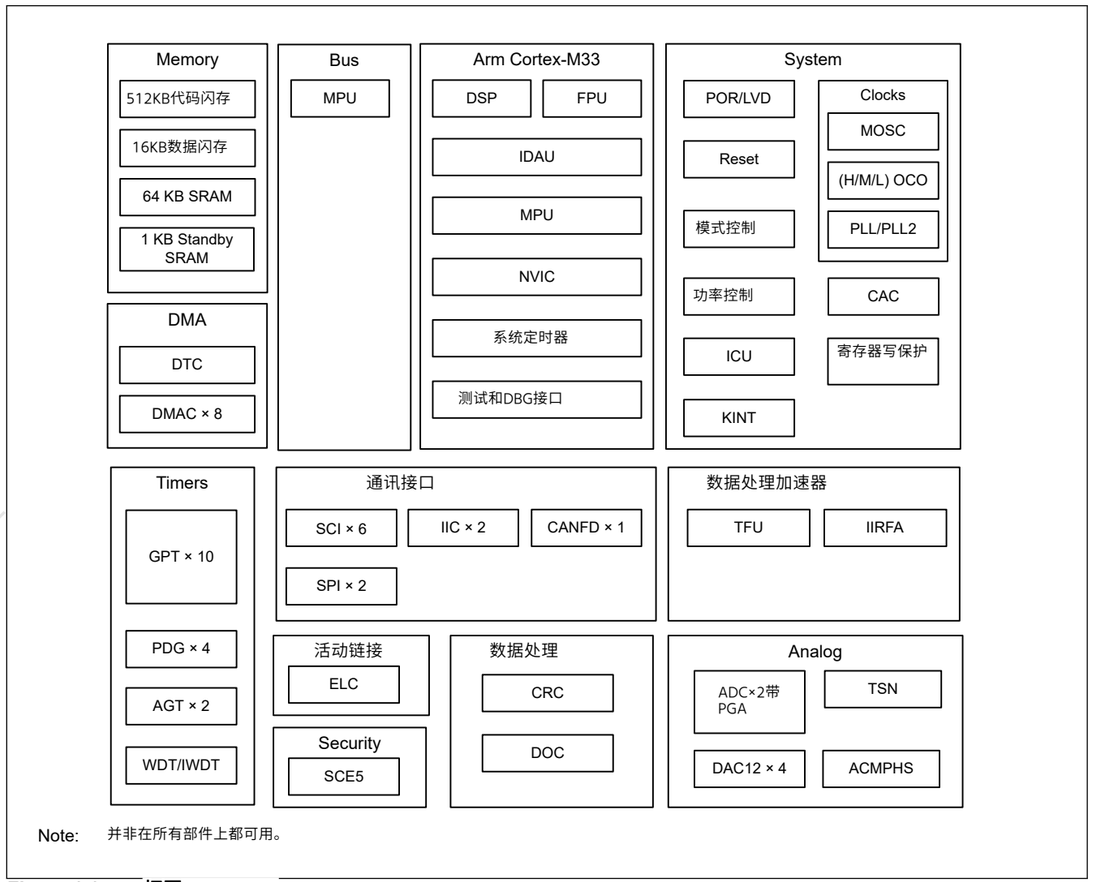


Figure 1.1 框图

1.3 零件编号

图1.2显示了产品部件号信息，包括内存容量和封装类型。表1.12显示了产品列表。

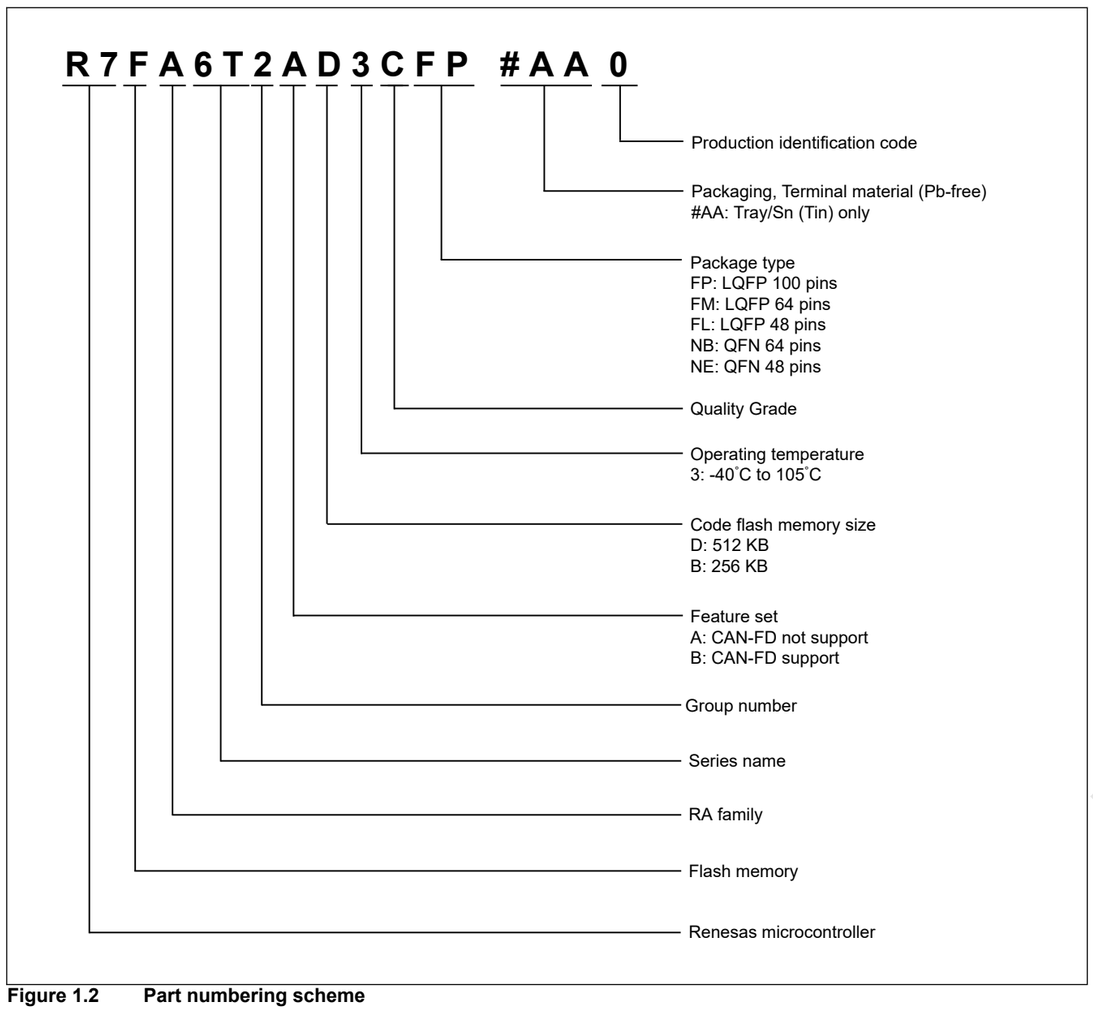


Figure 1.2 Part numbering scheme

Table 1.12 Product list (1 of 2)

Product part number	Package code	Code flash	Data flash	SRAM	CAN-FD	Operating temperature
R7FA6T2AD3CFP	PLQP0100KB-B	512 KB	16 KB	64 KB	Not support	-40 to +105°C
R7FA6T2AD3CFM	PLQP0064KB-C					
R7FA6T2AD3CFL	PLQP0048KB-B					
R7FA6T2AD3CNB	PWQN0064LA-A					
R7FA6T2AD3CNE	PWQN0048KB-A					
R7FA6T2AB3CFP	PLQP0100KB-B	256 KB				
R7FA6T2AB3CFM	PLQP0064KB-C					
R7FA6T2AB3CFL	PLQP0048KB-B					
R7FA6T2AB3CNB	PWQN0064LA-A					
R7FA6T2AB3CNE	PWQN0048KB-A					

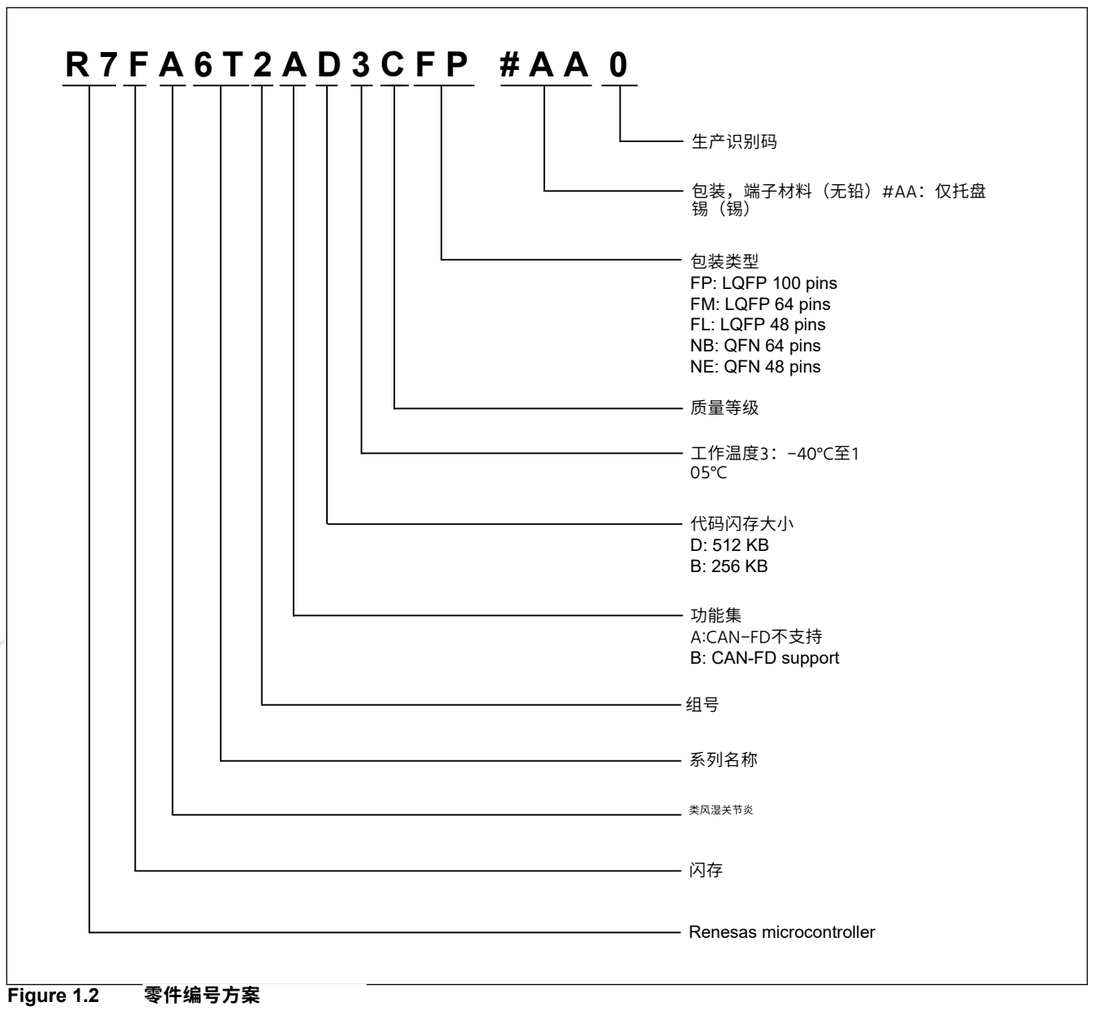


Figure 1.2 零件编号方案

Table 1.12 产品列表(1of2)

产品部件号	包装代码	代码闪存	数据闪存	SRAM	CAN-FD	工作温度
R7FA6T2AD3CFP	PLQP0100KB-B	512 KB	16 KB	64 KB	不支持	-40 to +105°C
R7FA6T2AD3CFM	PLQP0064KB-C					
R7FA6T2AD3CFL	PLQP0048KB-B					
R7FA6T2AD3CNB	PWQN0064LA-A					
R7FA6T2AD3CNE	PWQN0048KB-A					
R7FA6T2AB3CFP	PLQP0100KB-B	256 KB				
R7FA6T2AB3CFM	PLQP0064KB-C					
R7FA6T2AB3CFL	PLQP0048KB-B					
R7FA6T2AB3CNB	PWQN0064LA-A					
R7FA6T2AB3CNE	PWQN0048KB-A					

Table 1.12 Product list (2 of 2)

Product part number	Package code	Code flash	Data flash	SRAM	CAN-FD	Operating temperature
R7FA6T2BD3CFP	PLQP0100KB-B	512 KB	16 KB	64 KB	Support	-40 to +105°C
R7FA6T2BD3CFM	PLQP0064KB-C					
R7FA6T2BD3CFL	PLQP0048KB-B					
R7FA6T2BD3CNB	PWQN0064LA-A					
R7FA6T2BD3CNE	PWQN0048KB-A					
R7FA6T2BB3CFP	PLQP0100KB-B	256 KB				
R7FA6T2BB3CFM	PLQP0064KB-C					
R7FA6T2BB3CFL	PLQP0048KB-B					
R7FA6T2BB3CNB	PWQN0064LA-A					
R7FA6T2BB3CNE	PWQN0048KB-A					

Table 1.12 产品列表（2个中的2个）

产品部件号	包装代码	代码闪存	数据闪存	SRAM	CAN-FD	工作温度
R7FA6T2BD3CFP	PLQP0100KB-B	512 KB	16 KB	64 KB	Support	-40 to +105°C
R7FA6T2BD3CFM	PLQP0064KB-C					
R7FA6T2BD3CFL	PLQP0048KB-B					
R7FA6T2BD3CNB	PWQN0064LA-A					
R7FA6T2BD3CNE	PWQN0048KB-A					
R7FA6T2BB3CFP	PLQP0100KB-B	256 KB				
R7FA6T2BB3CFM	PLQP0064KB-C					
R7FA6T2BB3CFL	PLQP0048KB-B					
R7FA6T2BB3CNB	PWQN0064LA-A					
R7FA6T2BB3CNE	PWQN0048KB-A					

1.4 Function Comparison

Table 1.13 Function Comparison

Parts number		R7FA6T2XX3CFP	R7FA6T2XX3CFM	R7FA6T2XX3CFL	R7FA6T2XX3CNB	R7FA6T2XX3CNE
Pin count		100	64	48	64	48
Package		LQFP			QFN	
Code flash memory		512 KB, 256KB				
Data flash memory		16 KB				
SRAM	ECC	64 KB				
Standby SRAM	Parity	1 KB				
DMA	DTC	Yes				
	DMAC	8				
System	CPU clock	240 MHz (max.)				
	CPU clock sources	MOSC, HOCO, MOCO, LOCO, PLL				
	CAC	Yes				
	WDT/IWDT	Yes				
	KINT	Yes				
Communication	SCI	6				
	IIC	2*2				
	SPI	2				
	CANFD	1				
Timers	GPT*1	10				
	AGT*1	2				
Analog	ADC	Unit 0: 12 + 9*3, Unit 1: 8 + 9*3	Unit 0: 10, Unit 1: 8	Unit 0: 6, Unit 1: 4	Unit 0: 10, Unit 1: 8	Unit 0: 6, Unit 1: 4
	DAC12	4		2	4	2
	ACMPHS	4		2	4	2
	PGA	4		3	4	3
	TSN	Yes				
Data processing	CRC	Yes				
	DOC	Yes				
Event control	ELC	Yes				
Accelerator	TFU	Yes				
	IIRFA	Yes				
Security		SCE5, TrustZone and Lifecycle management				

Note: The product name differs depend on the memory size and CAN-FD support. see section 1.3. Part Numbering.
Note 1. Available pins depend on the Pin count, about details see section 1.7. Pin Lists.
Note 2. Fm+ and Hs-mode is only available for IIC channel IIC0.
Note 3. Shared terminal for UNIT0 and UNIT1.

1.4 功能比较

Table 1.13 功能比较

零件编号		R7FA6T2XX3CFP	R7FA6T2XX3CFM	R7FA6T2XX3CFL	R7FA6T2XX3CNB	R7FA6T2XX3CNE
针数		100	64	48	64	48
Package		LQFP			QFN	
代码闪存		512 KB, 256KB				
数据闪存		16 KB				
SRAM	ECC	64 KB				
Standby SRAM	Parity	1 KB				
DMA	DTC	Yes				
	DMAC	8				
System	中央处理器时钟	240 MHz (max.)				
	CPU时钟源	MOSC, HOCO, MOCO, LOCO, PLL				
	CAC	Yes				
	WDT/IWDT	Yes				
	KINT	Yes				
Communication	SCI	6				
	IIC	2*2				
	SPI	2				
	CANFD	1				
Timers	GPT*1	10				
	AGT*1	2				
Analog	ADC	Unit 0: 12 + 9*3, Unit 1: 8 + 9*3	Unit 0: 10, Unit 1: 8	Unit 0: 6, Unit 1: 4	Unit 0: 10, Unit 1: 8	Unit 0: 6, Unit 1: 4
	DAC12	4		2	4	2
	ACMPHS	4		2	4	2
	PGA	4		3	4	3
	TSN	Yes				
数据处理	CRC	Yes				
	DOC	Yes				
事件控制	ELC	Yes				
Accelerator	TFU	Yes				
	IIRFA	Yes				
Security		SCE5、TrustZone和生命周期管理				

Note: 产品名称因内存大小和CAN-FD支持而异。见第1.3节。零件编号。
注1.可用管脚取决于管脚数，详情见1.7节。引脚列表。
注2.Fm+和Hs模式仅适用于IIC通道IIC0。
注3.UNIT0和UNIT1共用端子。

1.5 Pin Functions

Table 1.14 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	EXTAL	Input	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	XTAL	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip emulator	TMS	Input	On-chip emulator or boundary scan pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	Output clock for synchronization with the trace data
	TDATA0 to TDATA3	Output	Trace data output
	SWO	Output	Serial wire trace output pin
	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQn	Input	Maskable interrupt request pins
	IRQn-DS	Input	Maskable interrupt request pins that can also be used in Deep Software Standby mode
KINT	KR00 to KR07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins

1.5 引脚功能

Table 1.14 引脚功能(1of3)

Function	Signal	I/O	Description
电源	VCC	Input	电源引脚。将其连接到系统电源。通过一个0.1μF电容将此引脚连接到VSS。电容应靠近引脚放置。
	VCL	I/O	通过用于稳定内部电源的平滑电容器将此引脚连接到VSS引脚。将电容器靠近引脚放置。
	VSS	Input	接地引脚。将其连接到系统电源(0V)。
Clock	EXTAL	Input	晶体谐振器的引脚。外部时钟信号可以通过EXTAL引脚输入。
	XTAL	Output	
	CLKOUT	Output	时钟输出引脚
操作模式控制	MD	Input	用于设置操作模式的引脚。在从复位状态释放的操作模式转换期间，不得更改此引脚上的信号电平。
系统控制	RES	Input	复位信号输入引脚。当该信号变低时，MCU进入复位状态。
CAC	CACREF	Input	测量参考时钟输入引脚
On-chip emulator	TMS	Input	片上仿真器或边界扫描引脚
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	用于与跟踪数据同步的输出时钟
	TDATA0 to TDATA3	Output	跟踪数据输出
	SWO	Output	串行线迹输出引脚
	SWDIO	I/O	串行线调试数据输入输出引脚
	SWCLK	Input	串行线时钟引脚
Interrupt	NMI	Input	不可屏蔽中断请求引脚
	IRQn	Input	可屏蔽中断请求引脚
	IRQn-DS	Input	可屏蔽中断请求引脚，也可用于Deep 软件待机模式
KINT	KR00 to KR07	Input	通过向按键中断输入引脚输入下降沿可以产生按键中断

Table 1.14 Pin functions (2 of 3)

Function	Signal	I/O	Description
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOCnA, GTIOCnB	I/O	Input capture, output compare, or PWM output pins
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
	GTCPPO0 to GTCPPO4, GTCPPO7	Output	Toggle output synchronized with PWM period
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEEn	Input	External event input enable signals
	AGTIOn	I/O	External event input and pulse output pins
	AGTOn	Output	Pulse output pins
	AGTOAn	Output	Output compare match A output pins
	AGTOBn	Output	Output compare match B output pins
SCI	SCKn	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	CTSn	Input	Input for the start of transmission.
	DEn	Output	Output pins for Driver Enable signal
	SCLn	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn	Input	Chip-select input pins (simple SPI mode), active-low
IIC	SCLn	I/O	Input/output pins for the clock
	SDAn	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection

Table 1.14 引脚功能（2个，共3个）

Function	Signal	I/O	Description
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	外部触发输入引脚
	GTIOCnA, GTIOCnB	I/O	输入捕捉、输出比较或PWM输出引脚
	GTADSM0, GTADSM1	Output	AD转换开始请求监视输出引脚
	GTCPPO0 to GTCPPO4, GTCPPO7	Output	与PWM周期同步的切换输出
	GTIU	Input	霍尔传感器输入引脚U
	GTIV	Input	霍尔传感器输入引脚V
	GTIW	Input	霍尔传感器输入引脚W
	GTOUUP	Output	用于BLDC电机控制的3相PWM输出（正U相）
	GTOULO	Output	用于BLDC电机控制的3相PWM输出（负U相）
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出（正V相）
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出（负V相）
	GTOWUP	Output	用于BLDC电机控制的3相PWM输出（正W相）
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出（负W相）
AGT	AGTEEn	Input	外部事件输入使能信号
	AGTIOn	I/O	外部事件输入和脉冲输出引脚
	AGTOn	Output	脉冲输出引脚
	AGTOAn	Output	输出比较匹配A输出引脚
	AGTOBn	Output	输出比较匹配B输出引脚
SCI	SCKn	I/O	时钟输入输出引脚（时钟同步模式）
	RXDn	Input	接收数据的输入引脚（异步模式时钟同步模式）
	TXDn	Output	传输数据的输出引脚（异步模式时钟同步模式）
	CTSn_RTSn	I/O	输入输出引脚用于控制发送和接收的开始（异步模式时钟同步模式），低电平有效。
	CTSn	Input	开始传输的输入。
	DEn	Output	驱动器使能信号的输出引脚
	SCLn	I/O	IIC时钟的输入输出引脚（简单IIC模式）
	SDAn	I/O	IIC数据的输入输出引脚（简单IIC模式）
	SCKn	I/O	时钟输入输出引脚（简单SPI模式）
	MISOn	I/O	用于从机传输数据的输入输出引脚（简单SPI模式）
	MOSIn	I/O	输入输出引脚用于主数据传输（简单SPI模式）
	SSn	Input	片选输入引脚（简单SPI模式），低电平有效
IIC	SCLn	I/O	时钟的输入输出引脚
	SDAn	I/O	数据输入输出引脚
SPI	RSPCKA, RSPCKB	I/O	时钟输入输出引脚
	MOSIA, MOSIB	I/O	用于从主机输出数据的输入或输出引脚
	MISOA, MISOB	I/O	从机数据输出的输入或输出引脚
	SSLA0, SSLB0	I/O	从机选择的输入或输出引脚
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	从机选择的输出引脚

Table 1.14 Pin functions (3 of 3)

Function	Signal	I/O	Description
CANFD	CRX0	Input	Receive data
	CTX0	Output	Transmit data
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH0	Input	Analog reference voltage supply pin for the ADC. Connect this pin to AVCC0 when not using the ADC.
	VREFL0	Input	Analog reference ground pin for the ADC. Connect this pin to AVSS0 when not using the ADC.
ADC	AN000 to AN028	Input	Input pins for the analog signals to be processed by the A/D converter.
	PGAIN0 to PGAIN3	Input	Pseudo-differential input pins of programmable gain amplifier (Signal source side)
	PGAVSS0 to PGAVSS3	Input	Pseudo-differential input pins of programmable gain amplifier (reference ground side)
	PGAOUT0 to PGAOUT3	Output	Monitor output pins of programmable gain amplifier
	ADTRGm	Input	Input pins for the external trigger signals that start the A/D conversion, active-low.
DAC12	DAn	Output	Output pins for the analog signals processed by the D/A converter.
ACMPHS	VCOUT	Output	Comparator output pin (OR output of all units)
	CMPOUTm	Output	Comparator output pin (m:unit number)
	CMPOUT012	Output	Comparator output pin (OR output of units 0, 1 and 2)
	IVREF0, IVREF1	Input	Reference voltage input pins for comparator
	IVCMPm0, IVCMPm2, IVCMPm3	Input	Analog voltage input pins for comparator (m:unit number)
I/O ports	P201, P212, P213, PA08 to PA15, PB03 to PB10, PB12 to PB15, PC06 to PC12, PC14, PC15, PD00 to PD15, PE00 to PE06, PE08 to PE15	I/O	General-purpose input/output pins
	P000, P001, P002, PA00 to PA07, PB00 to PB02, PC00 to PC05, PC13	Input	General-purpose input pins

Table 1.14 引脚功能（3个中的3个）

Function	Signal	I/O	Description
CANFD	CRX0	Input	接收数据
	CTX0	Output	传输数据
模拟电源	AVCC0	Input	模拟电压电源引脚。这用作各个模块的模拟电源。为该引脚提供与VCC引脚相同的电压。
	AVSS0	Input	模拟接地引脚。这用作各个模块的模拟地。为该引脚提供与VSS引脚相同的电压。
	VREFH0	Input	ADC的模拟参考电压电源引脚。将此引脚连接到不使用ADC时的AVCC0。
	VREFL0	Input	ADC的模拟参考接地引脚。将此引脚连接到不使用ADC时为AVSS0。
ADC	AN000 to AN028	Input	AD转换器要处理的模拟信号的输入引脚。
	PGAIN0 to PGAIN3	Input	可编程增益放大器的伪差分输入引脚（信号源侧）
	PGAVSS0 to PGAVSS3	Input	可编程增益放大器的伪差分输入引脚（参考地侧）
	PGAOUT0 to PGAOUT3	Output	监控可编程增益放大器的输出引脚
	ADTRGm	Input	用于启动AD转换的外部触发信号的输入引脚，低电平有效。
DAC12	DAn	Output	由数模转换器处理的模拟信号的输出引脚。
ACMPHS	VCOUT	Output	比较器输出引脚（所有单元的OR输出）
	CMPOUTm	Output	比较器输出引脚（m：单元号）
	CMPOUT012	Output	比较器输出引脚（单元0、1和2的OR输出）
	IVREF0, IVREF1	Input	比较器的参考电压输入引脚
	IVCMPm0, IVCMPm2, IVCMPm3	Input	比较器的模拟电压输入引脚（m：单元数）
I/O ports	P201, P212, P213, PA08 to PA15, PB03 to PB10, PB12 to PB15, PC06 to PC12, PC14, PC15, PD00 to PD15, PE00 to PE06, PE08 to PE15	I/O	General-purpose input/output pins
	P000, P001, P002, PA00 to PA07, PB00 to PB02, PC00 to PC05, PC13	Input	通用输入引脚

1.6 Pin Assignments

The following figures show the pin assignments from the top view.

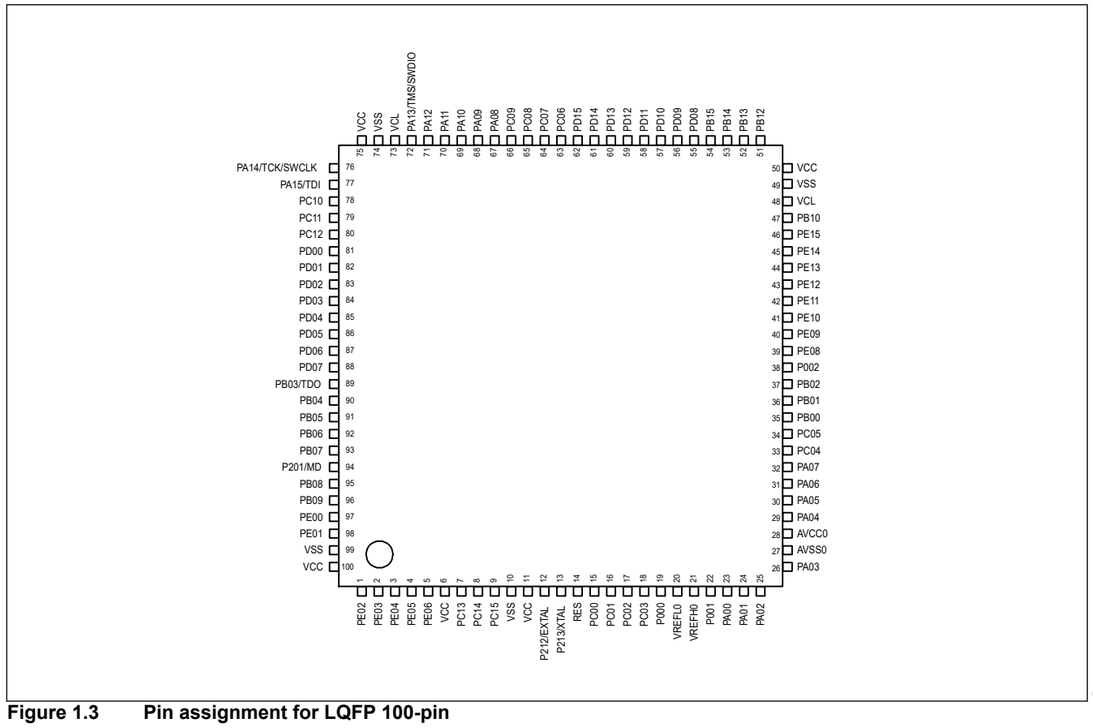


Figure 1.3 Pin assignment for LQFP 100-pin

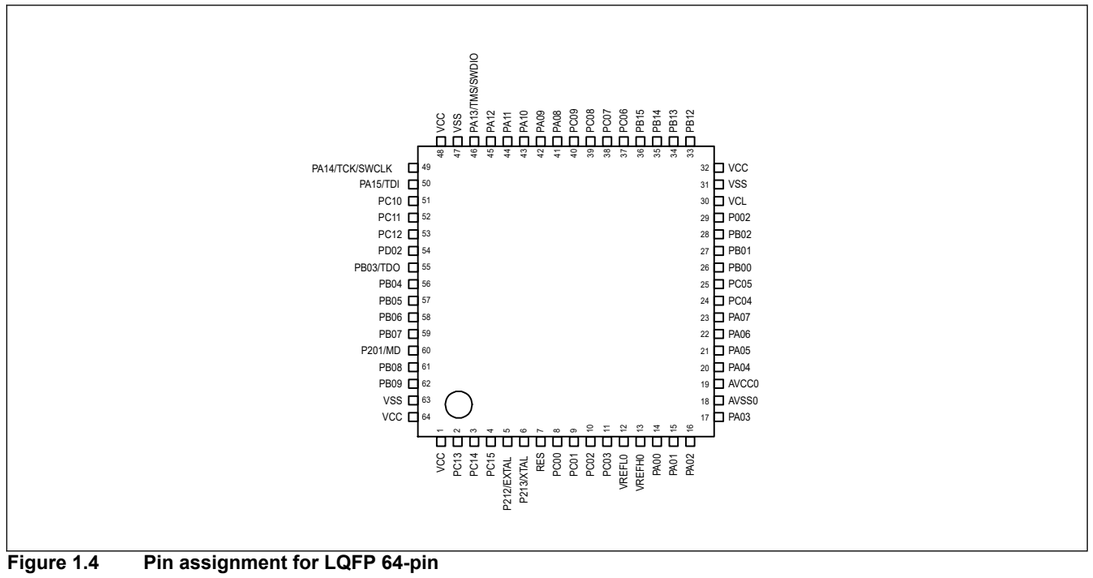


Figure 1.4 Pin assignment for LQFP 64-pin

1.6 引脚分配

下图从顶视图显示了引脚分配。

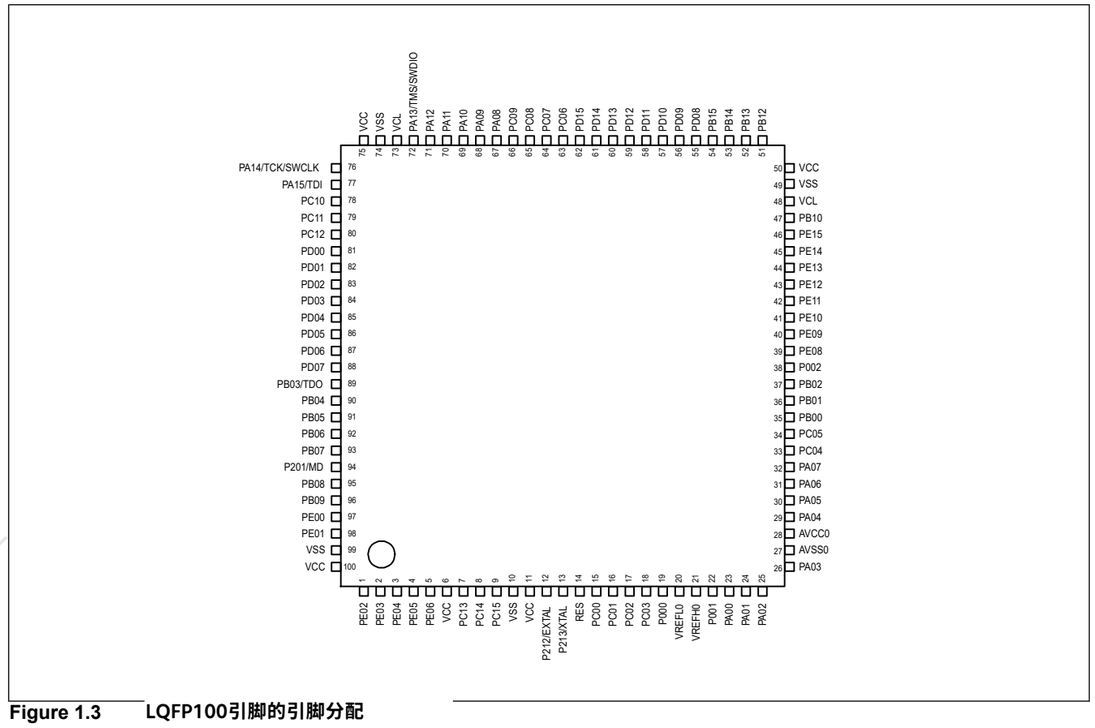


Figure 1.3 LQFP100引脚的引脚分配

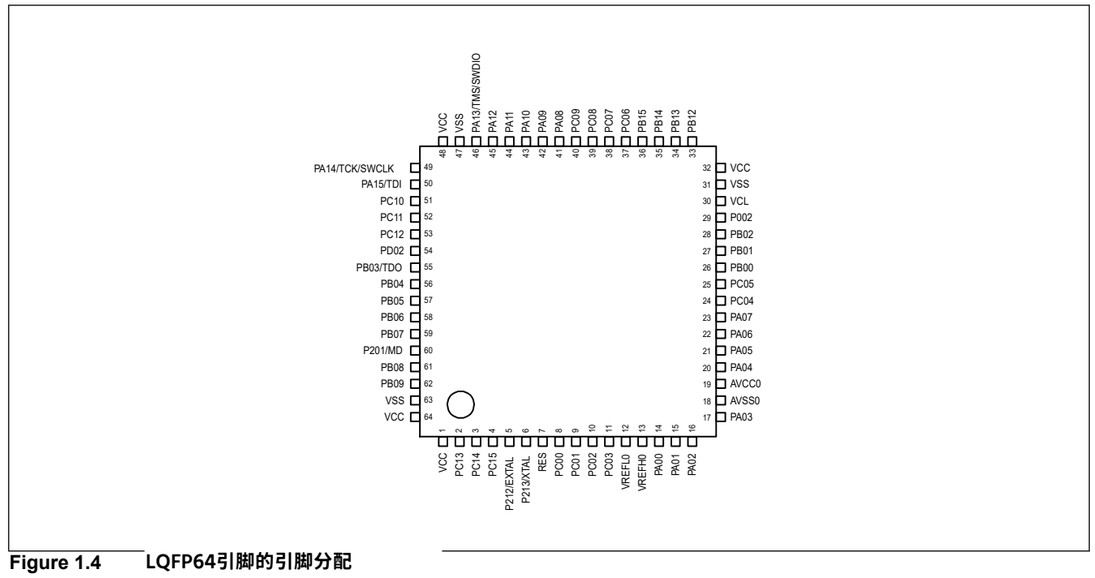


Figure 1.4 LQFP64引脚的引脚分配

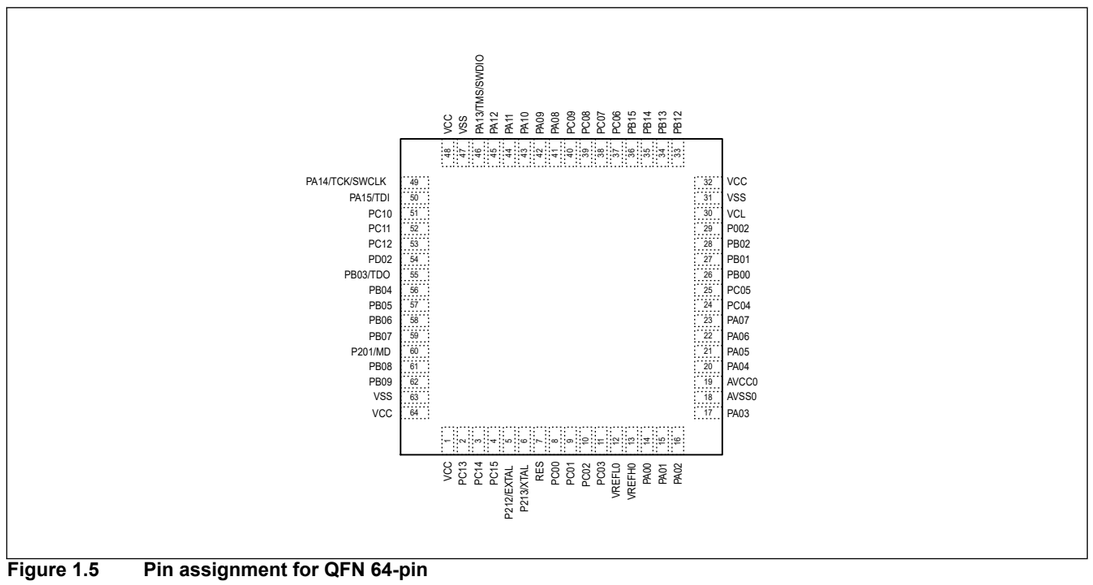


Figure 1.5 Pin assignment for QFN 64-pin

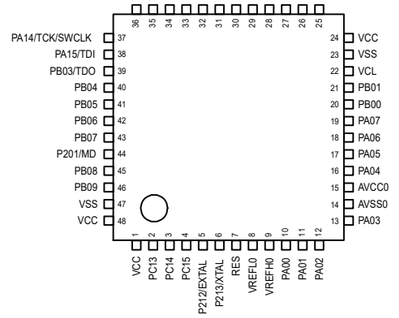


Figure 1.6 Pin assignment for LQFP 48-pin

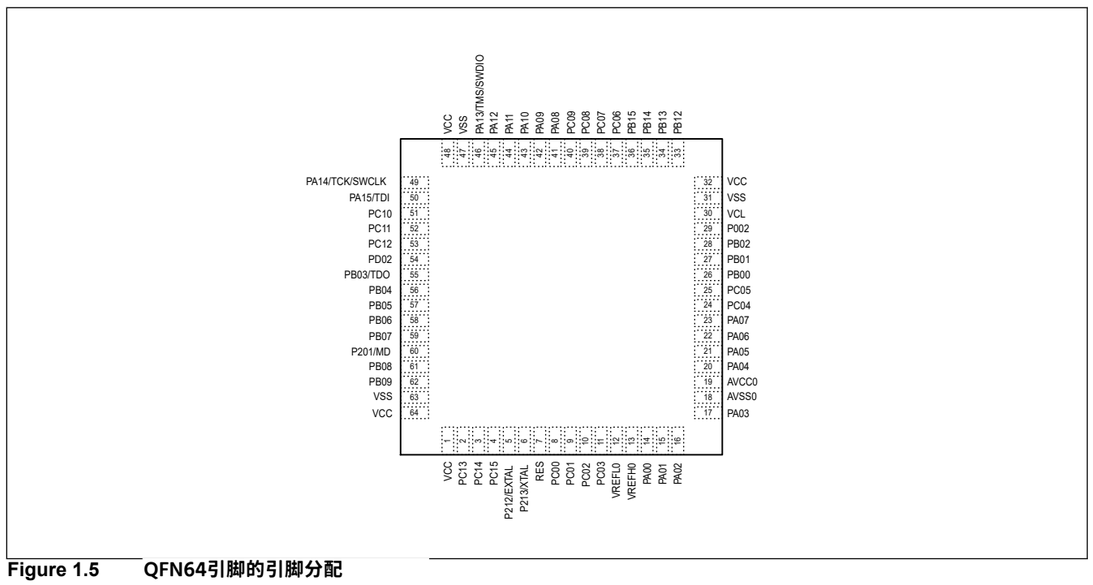


Figure 1.5 QFN64引脚的引脚分配

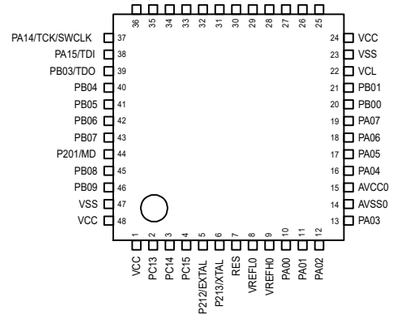


Figure 1.6 LQFP48引脚的引脚分配

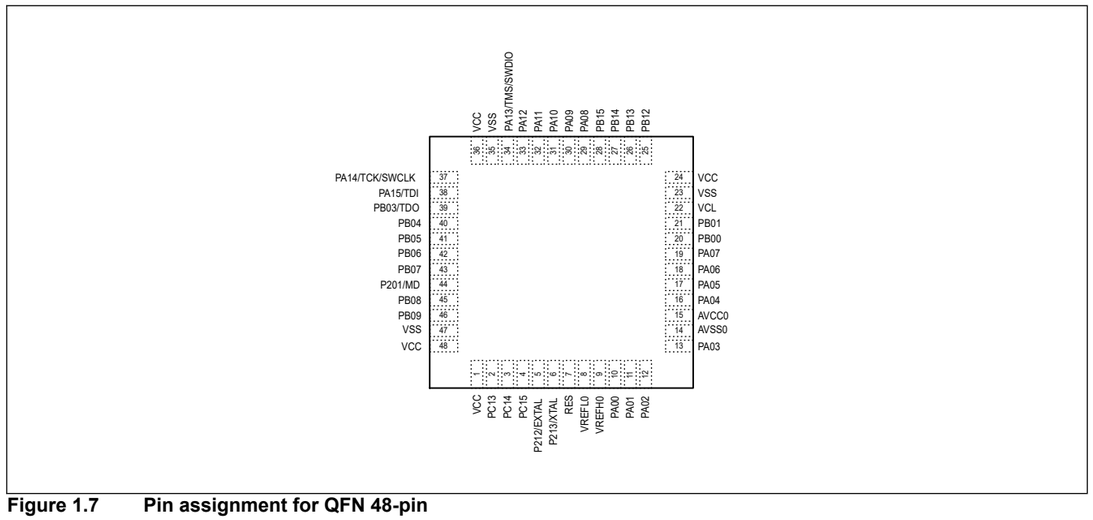


Figure 1.7 Pin assignment for QFN 48-pin

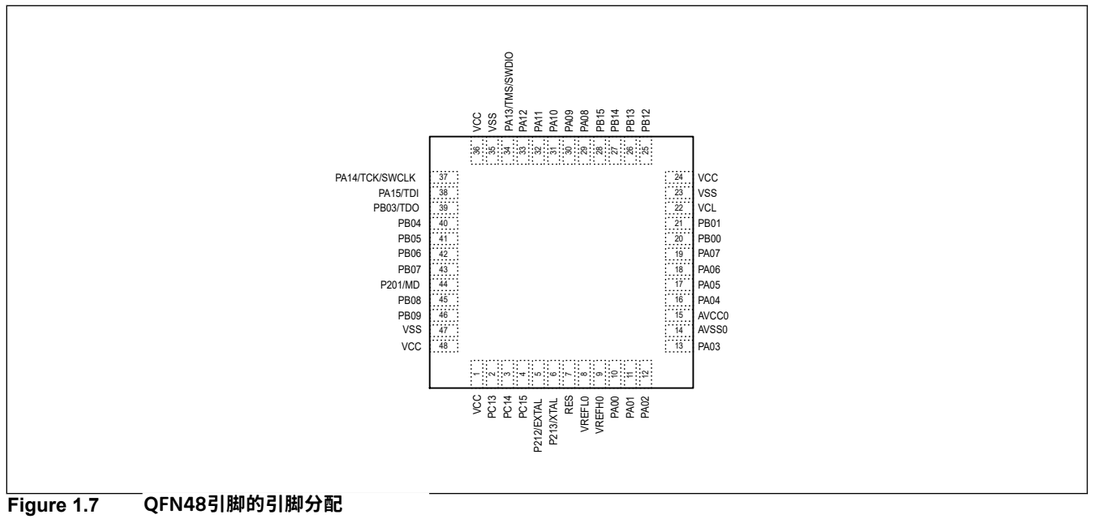


Figure 1.7 QFN48引脚的引脚分配

1.7 Pin Lists

Table 1.15 Pin list (1 of 3)

LQFP100	LQFP64, QFN64	LQFP48, QFN48	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt/KINT	SCI/IIC/SPI/CANFD	GPT/AGT	ADC/DAC12/ACMPHS
1	—	—	CLKOUT/TCLK	PE02	—	SCK0_B/DE0/SCK3_A/DE3/RSPCKB_C	GTOVLO/GTIOC7B/GTIOC8A	CMPOUT0
2	—	—	TDATA0	PE03	—	RXD0_B/MISO0_B/SCL0/CTS3_A/SSLB0_C	GTOWLO/GTIOC8A/GTIOC9A	CMPOUT1
3	—	—	TDATA1	PE04	—	TXD0_B/MOSI0_B/SDA0/CTS3_RTS3/SS3_A/DE3/ SSLB1_C	GTOUUP/GTIOC8B/GTIOC7B	CMPOUT2
4	—	—	TDATA2	PE05	—	CTS0_RTS0/SS0_B/DE0/RXD3_A/MISO3_A/SCL3/ MISOB_C	GTOVUP/GTIOC9A/GTIOC8B/ GTCPPO2	CMPOUT3
5	—	—	TDATA3	PE06	—	CTS0_B/TXD3_A/MOSI3_A/SDA3/MOSIB_C	GTOWUP/GTIOC9B/GTCPPO3	—
6	1	1	VCC	—	—	—	—	—
7	2	2	—	PC13	NMI	—	GTETRGD	—
8	3	3	—	PC14	IRQ14	—	GTETRGA/GTIOC3A/GTCPPO0/ GTADSM0/GTCPPO4/AGTIO0	ADTRG0/CMPOUT012
9	4	4	—	PC15	IRQ15	—	GTETRGB/GTIOC3B/GTCPPO1/ GTADSM1/GTCPPO7/AGTIO1	ADTRG1/CMPOUT3
10	—	—	VSS	—	—	—	—	—
11	—	—	VCC	—	—	—	—	—
12	5	5	EXTAL	P212	—	—	—	—
13	6	6	XTAL	P213	IRQ0	—	—	—
14	7	7	RES	—	—	—	—	—
15	8	—	—	PC00	IRQ11-DS	—	—	AN012/PGAOUT0/IVCMP00
16	9	—	—	PC01	IRQ12-DS	—	—	AN013/PGAOUT1/IVCMP10
17	10	—	—	PC02	IRQ13-DS	—	—	AN014/PGAOUT2/IVCMP20
18	11	—	—	PC03	IRQ14-DS	—	—	AN015/PGAOUT3/IVCMP30
19	—	—	—	P000	IRQ0	—	—	AN016/IVREF0
20	12	8	VREFL0	—	—	—	—	—
21	13	9	VREFH0	—	—	—	—	—
22	—	—	—	P001	IRQ2	—	—	AN017/IVREF1
23	14	10	—	PA00	IRQ0-DS	—	—	AN000/PGAIN0/IVCMP02/ IVCMP03
24	15	11	—	PA01	IRQ1	—	—	AN001/PGAVSS0
25	16	12	—	PA02	IRQ2	—	—	AN002/PGAIN1/IVCMP12/ IVCMP13
26	17	13	—	PA03	IRQ3	—	—	AN003/PGAVSS1
27	18	14	AVSS0	—	—	—	—	—
28	19	15	AVCC0	—	—	—	—	—
29	20	16	—	PA04	IRQ4	—	—	AN004/PGAIN2/IVCMP22/ IVCMP23
30	21	17	—	PA05	IRQ5	—	—	AN005/PGAVSS2
31	22	18	—	PA06	IRQ6	—	—	AN006/DA0
32	23	19	—	PA07	IRQ7	—	—	AN007/DA1
33	24	—	—	PC04	IRQ10	—	—	AN010/DA2
34	25	—	—	PC05	IRQ11	—	—	AN011/DA3
35	26	20	—	PB00	IRQ0	—	—	AN008/PGAOUT0/PGAOUT2
36	27	21	—	PB01	IRQ1	—	—	AN009/PGAOUT1/PGAOUT3
37	28	—	—	PB02	IRQ15-DS	—	—	AN018/PGAIN3/IVCMP32/ IVCMP33
38	29	—	—	P002	—	—	—	AN019/PGAVSS3
39	—	—	—	PE08	KR00	SSLA3_C	GTIV/GTIOC3A/GTETRGC/ GTADSM0	AN020/ADTRG0/ CMPOUT012
40	—	—	CACREF	PE09	KR01	SSLA2_C	GTIW/GTIOC3B/GTETRGD/ GTADSM1	AN021/ADTRG1/CMPOUT3
41	—	—	—	PE10	KR02	SSLA1_C	GTOULO/GTIOC2A/GTIOC4A/ GTIOC7A	AN022

1.7 引脚列表

Table 1.15 引脚列表（1个，共3个）

LQFP100	LQFP64, QFN64	LQFP48, QFN48	电源、系统、时钟、调试、CAC	I/O ports	Ex. Interrupt/KINT	SCI/IIC/SPI/CANFD	GPT/AGT	ADC/DAC12/ACMPHS
1	—	—	CLKOUT/TCLK	PE02	—	SCK0_B/DE0/SCK3_A/DE3/RSPCKB_C	GTOVLO/GTIOC7B/GTIOC8A	CMPOUT0
2	—	—	TDATA0	PE03	—	RXD0_B/MISO0_B/SCL0/CTS3_A/SSLB0_C	GTOWLO/GTIOC8A/GTIOC9A	CMPOUT1
3	—	—	TDATA1	PE04	—	TXD0_B/MOSI0_B/SDA0/CTS3_RTS3/SS3_A/DE3/ SSLB1_C	GTOUUP/GTIOC8B/GTIOC7B	CMPOUT2
4	—	—	TDATA2	PE05	—	CTS0_RTS0/SS0_B/DE0/RXD3_A/MISO3_A/SCL3/ MISOB_C	GTOVUP/GTIOC9A/GTIOC8B/ GTCPPO2	CMPOUT3
5	—	—	TDATA3	PE06	—	CTS0_B/TXD3_A/MOSI3_A/SDA3/MOSIB_C	GTOWUP/GTIOC9B/GTCPPO3	—
6	1	1	VCC	—	—	—	—	—
7	2	2	—	PC13	NMI	—	GTETRGD	—
8	3	3	—	PC14	IRQ14	—	GTETRGA/GTIOC3A/GTCPPO0/ GTADSM0/GTCPPO4/AGTIO0	ADTRG0/CMPOUT012
9	4	4	—	PC15	IRQ15	—	GTETRGB/GTIOC3B/GTCPPO1/ GTADSM1/GTCPPO7/AGTIO1	ADTRG1/CMPOUT3
10	—	—	VSS	—	—	—	—	—
11	—	—	VCC	—	—	—	—	—
12	5	5	EXTAL	P212	—	—	—	—
13	6	6	XTAL	P213	IRQ0	—	—	—
14	7	7	RES	—	—	—	—	—
15	8	—	—	PC00	IRQ11-DS	—	—	AN012/PGAOUT0/IVCMP00
16	9	—	—	PC01	IRQ12-DS	—	—	AN013/PGAOUT1/IVCMP10
17	10	—	—	PC02	IRQ13-DS	—	—	AN014/PGAOUT2/IVCMP20
18	11	—	—	PC03	IRQ14-DS	—	—	AN015/PGAOUT3/IVCMP30
19	—	—	—	P000	IRQ0	—	—	AN016/IVREF0
20	12	8	VREFL0	—	—	—	—	—
21	13	9	VREFH0	—	—	—	—	—
22	—	—	—	P001	IRQ2	—	—	AN017/IVREF1
23	14	10	—	PA00	IRQ0-DS	—	—	AN000/PGAIN0/IVCMP02/ IVCMP03
24	15	11	—	PA01	IRQ1	—	—	AN001/PGAVSS0
25	16	12	—	PA02	IRQ2	—	—	AN002/PGAIN1/IVCMP12/ IVCMP13
26	17	13	—	PA03	IRQ3	—	—	AN003/PGAVSS1
27	18	14	AVSS0	—	—	—	—	—
28	19	15	AVCC0	—	—	—	—	—
29	20	16	—	PA04	IRQ4	—	—	AN004/PGAIN2/IVCMP22/ IVCMP23
30	21	17	—	PA05	IRQ5	—	—	AN005/PGAVSS2
31	22	18	—	PA06	IRQ6	—	—	AN006/DA0
32	23	19	—	PA07	IRQ7	—	—	AN007/DA1
33	24	—	—	PC04	IRQ10	—	—	AN010/DA2
34	25	—	—	PC05	IRQ11	—	—	AN011/DA3
35	26	20	—	PB00	IRQ0	—	—	AN008/PGAOUT0/PGAOUT2
36	27	21	—	PB01	IRQ1	—	—	AN009/PGAOUT1/PGAOUT3
37	28	—	—	PB02	IRQ15-DS	—	—	AN018/PGAIN3/IVCMP32/ IVCMP33
38	29	—	—	P002	—	—	—	AN019/PGAVSS3
39	—	—	—	PE08	KR00	SSLA3_C	GTIV/GTIOC3A/GTETRGC/ GTADSM0	AN020/ADTRG0/ CMPOUT012
40	—	—	CACREF	PE09	KR01	SSLA2_C	GTIW/GTIOC3B/GTETRGD/ GTADSM1	AN021/ADTRG1/CMPOUT3
41	—	—	—	PE10	KR02	SSLA1_C	GTOULO/GTIOC2A/GTIOC4A/ GTIOC7A	AN022

Table 1.15 Pin list (2 of 3)

LQFP100	LQFP64, QFN64	LQFP48, QFN48	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt/KINT	SCI/IIC/SPI/CANFD	GPT/AGT	ADC/DAC12/ACMPHS
42	—	—	—	PE11	KR03	SSLA0_C	GTOUUP/GTIOC2B/GTIOC5A/ GTIOC8A	AN023
43	—	—	—	PE12	KR04	RSPCKA_C	GTOVLO/GTIOC1A/GTIOC6A/ GTIOC9A	AN024
44	—	—	—	PE13	KR05	MISOA_C	GTOVUP/GTIOC1B/GTIOC4B/ GTIOC7B	AN025
45	—	—	—	PE14	KR06	MOSIA_C	GTOWLO/GTIOC0A/GTIOC5B/ GTIOC8B	AN026
46	—	—	—	PE15	KR07	RXD4_A/MISO4_A/SCL4	GTOWUP/GTIOC0B/GTIOC6B/ GTIOC9B	AN027
47	—	—	CACREF/VCOUT	PB10	IRQ10-DS	TXD4_A/MOSI4_A/SDA4/CTS3_B	GTIU/GTETRGA/GTETRGB/ GTCPPO4/GTCPPO7	AN028
48	30	22	VCL	—	—	—	—	—
49	31	23	VSS	—	—	—	—	—
50	32	24	VCC	—	—	—	—	—
51	33	25	—	PB12	IRQ2	SCK4_A/DE4/RXD3_B/MISO3_B/SCL3/SSLB0_A/ CRX0	GTETRGA/GTIOC0A/GTIOC4A	ADTRG0
52	34	26	—	PB13	IRQ3	CTS4_A/TXD3_B/MOSI3_B/SDA3/RSPCKB_A/CTX0	GTOULO/GTIOC0B/GTIOC7A/ GTIOC5A	—
53	35	27	—	PB14	IRQ4	CTS4_RTS4/SS4_A/DE4/SCK3_B/DE3/SDA0_C/ MISOB_A	GTOVLO/GTIOC1A/GTIOC8A/ GTIOC6A	—
54	36	28	—	PB15	IRQ5	RXD4_A/MISO4_A/SCL4/CTS3_RTS3/SS3_B/DE3/ SCL0_C/MOSIB_A	GTOWLO/GTIOC1B/GTIOC9A/ GTIOC4B	—
55	—	—	—	PD08	KR00	CTS2_B/TXD1_A/MOSI1_A/SDA1/SSLB1_A	GTIOC2A	—
56	—	—	—	PD09	KR01	CTS2_RTS2/SS2_B/DE2/RXD1_A/MISO1_A/SCL1/ SSLB2_A	GTIOC2B	—
57	—	—	—	PD10	KR02	SCK2_C/DE2/SCK1_A/DE1/SSLB3_A	GTETRGC/GTIOC3A	—
58	—	—	—	PD11	KR03	RXD2_C/MISO2_C/SCL2/CTS1_A	GTIOC3B	—
59	—	—	—	PD12	IRQ12/KR04	TXD2_C/MOSI2_C/SDA2/CTS1_RTS1/SS1_A/DE1/ SCL1_D	GTIOC4A	—
60	—	—	—	PD13	IRQ13/KR05	SCK4_C/DE4/SCK9_C/DE9/SDA1_D	GTIOC4B	—
61	—	—	—	PD14	IRQ14/KR06	RXD4_C/MISO4_C/SCL4/RXD9_C/MISO9_C/SCL9/ SCL0_F	GTIOC5A	—
62	—	—	—	PD15	IRQ15/KR07	TXD4_C/MOSI4_C/SDA4/TXD9_C/MOSI9_C/ SDA9/DE9/SDA0_F	GTIOC5B	—
63	37	—	—	PC06	IRQ6	TXD2_B/MOSI2_B/SDA2/CTS9_RTS9/SS9_C/DE9/ SCL1_E	GTETRGD/GTIOC6A/GTIOC5B/ AGTO0	—
64	38	—	—	PC07	IRQ7	RXD2_B/MISO2_B/SCL2/CTS9_C/SDA1_E	GTETRGA/GTIOC6B/AGTEE0	—
65	39	—	CACREF	PC08	IRQ8	SCK2_B/DE2/CTS3_RTS3/SS3_C/DE3/SCL0_E/ SSLA3_B	GTIV/GTIOC7A/AGTOA0	—
66	40	—	CLKOUT	PC09	IRQ9	CTS2_RTS2/SS2_B/DE2/CTS3_C/SDA0_D/SDA0_E/ SSLA2_B	GTIW/GTIOC7B/GTIOC8A/AGTOB0	—
67	41	29	CLKOUT	PA08	IRQ8/KR00	SCK0_A/DE0/SCK1_C/DE1/SCL0_D/SSLA1_B	GTOUUP/GTIOC8A/GTIOC7B/ GTIOC2A/GTIOC9A/AGTIO0	CMPOUT2
68	42	30	—	PA09	IRQ9/KR01	TXD0_A/MOSI0_A/SDA0/SCL1_C/SSLA0_B	GTOVUP/GTIOC8B/GTIOC8B/ GTIOC2B/GTIOC7B	CMPOUT3
69	43	31	—	PA10	IRQ10/KR02	RXD0_A/MISO0_A/SCL0/SDA1_C/RSPCKA_B	GTOWUP/GTIOC9A/GTIOC9B/ GTIOC3A/GTIOC8B	CMPOUT0
70	44	32	—	PA11	IRQ11/KR03	CTS0_A/RXD1_C/MISO1_C/SCL1/MOSIA_B/CTX0	GTETRGD/GTIOC9B/GTETRGC/ GTIOC3B	CMPOUT1
71	45	33	CACREF	PA12	IRQ12/KR04	CTS0_RTS0/SS0_A/DE0/TXD1_C/MOSI1_C/SDA1/ MISOA_B/CRX0	GTETRGB/GTCPPO0/GTCPPO2/ GTADSM0/GTCPPO7	ADTRG1
72	46	34	TMS/SWDIO	PA13	—	SCK0_C/DE0/CTS1_RTS1/SS1_C/DE1	AGTO0	—
73	—	—	VCL	—	—	—	—	—
74	47	35	VSS	—	—	—	—	—
75	48	36	VCC	—	—	—	—	—
76	49	37	TCK/SWCLK	PA14	—	TXD0_C/MOSI0_C/SDA0/SCK9_B/DE9	AGTO1	—
77	50	38	TDI	PA15	IRQ1/KR02	RXD0_C/MISO0_C/SCL0/RXD9_B/MISO9_B/SCL9/ SSLA0_A	GTETRGB/GTADSM1/GTCPPO4	ADTRG0/CMPOUT012
78	51	—	—	PC10	IRQ6-DS/KR05	TXD1_B/MOSI1_B/SDA1/SCL0_B/RSPCKB_B	AGTIO1	CMPOUT0

Table 1.15 引脚列表（2个，共3个）

LQFP100	LQFP64, QFN64	LQFP48, QFN48	电源、系统、时钟、调试、CAC	I/O ports	Ex. Interrupt/KINT	SCI/IIC/SPI/CANFD	GPT/AGT	ADC/DAC12/ACMPHS
42	—	—	—	PE11	KR03	SSLA0_C	GTOUUP/GTIOC2B/GTIOC5A/ GTIOC8A	AN023
43	—	—	—	PE12	KR04	RSPCKA_C	GTOVLO/GTIOC1A/GTIOC6A/ GTIOC9A	AN024
44	—	—	—	PE13	KR05	MISOA_C	GTOVUP/GTIOC1B/GTIOC4B/ GTIOC7B	AN025
45	—	—	—	PE14	KR06	MOSIA_C	GTOWLO/GTIOC0A/GTIOC5B/ GTIOC8B	AN026
46	—	—	—	PE15	KR07	RXD4_A/MISO4_A/SCL4	GTOWUP/GTIOC0B/GTIOC6B/ GTIOC9B	AN027
47	—	—	CACREF/VCOUT	PB10	IRQ10-DS	TXD4_A/MOSI4_A/SDA4/CTS3_B	GTIU/GTETRGA/GTETRGB/ GTCPPO4/GTCPPO7	AN028
48	30	22	VCL	—	—	—	—	—
49	31	23	VSS	—	—	—	—	—
50	32	24	VCC	—	—	—	—	—
51	33	25	—	PB12	IRQ2	SCK4_A/DE4/RXD3_B/MISO3_B/SCL3/SSLB0_A/ CRX0	GTETRGA/GTIOC0A/GTIOC4A	ADTRG0
52	34	26	—	PB13	IRQ3	CTS4_A/TXD3_B/MOSI3_B/SDA3/RSPCKB_A/CTX0	GTOULO/GTIOC0B/GTIOC7A/ GTIOC5A	—
53	35	27	—	PB14	IRQ4	CTS4_RTS4/SS4_A/DE4/SCK3_B/DE3/SDA0_C/ MISOB_A	GTOVLO/GTIOC1A/GTIOC8A/ GTIOC6A	—
54	36	28	—	PB15	IRQ5	RXD4_A/MISO4_A/SCL4/CTS3_RTS3/SS3_B/DE3/ SCL0_C/MOSIB_A	GTOWLO/GTIOC1B/GTIOC9A/ GTIOC4B	—
55	—	—	—	PD08	KR00	CTS2_B/TXD1_A/MOSI1_A/SDA1/SSLB1_A	GTIOC2A	—
56	—	—	—	PD09	KR01	CTS2_RTS2/SS2_B/DE2/RXD1_A/MISO1_A/SCL1/ SSLB2_A	GTIOC2B	—
57	—	—	—	PD10	KR02	SCK2_C/DE2/SCK1_A/DE1/SSLB3_A	GTETRGC/GTIOC3A	—
58	—	—	—	PD11	KR03	RXD2_C/MISO2_C/SCL2/CTS1_A	GTIOC3B	—
59	—	—	—	PD12	IRQ12/KR04	TXD2_C/MOSI2_C/SDA2/CTS1_RTS1/SS1_A/DE1/ SCL1_D	GTIOC4A	—
60	—	—	—	PD13	IRQ13/KR05	SCK4_C/DE4/SCK9_C/DE9/SDA1_D	GTIOC4B	—
61	—	—	—	PD14	IRQ14/KR06	RXD4_C/MISO4_C/SCL4/RXD9_C/MISO9_C/SCL9/ SCL0_F	GTIOC5A	—
62	—	—	—	PD15	IRQ15/KR07	TXD4_C/MOSI4_C/SDA4/TXD9_C/MOSI9_C/ SDA9/DE9/SDA0_F	GTIOC5B	—
63	37	—	—	PC06	IRQ6	TXD2_B/MOSI2_B/SDA2/CTS9_RTS9/SS9_C/DE9/ SCL1_E	GTETRGD/GTIOC6A/GTIOC5B/ AGTO0	—
64	38	—	—	PC07	IRQ7	RXD2_B/MISO2_B/SCL2/CTS9_C/SDA1_E	GTETRGA/GTIOC6B/AGTEE0	—
65	39	—	CACREF	PC08	IRQ8	SCK2_B/DE2/CTS3_RTS3/SS3_C/DE3/SCL0_E/ SSLA3_B	GTIV/GTIOC7A/AGTOA0	—
66	40	—	CLKOUT	PC09	IRQ9	CTS2_RTS2/SS2_B/DE2/CTS3_C/SDA0_D/SDA0_E/ SSLA2_B	GTIW/GTIOC7B/GTIOC8A/AGTOB0	—
67	41	29	CLKOUT	PA08	IRQ8/KR00	SCK0_A/DE0/SCK1_C/DE1/SCL0_D/SSLA1_B	GTOUUP/GTIOC8A/GTIOC7B/ GTIOC2A/GTIOC9A/AGTIO0	CMPOUT2
68	42	30	—	PA09	IRQ9/KR01	TXD0_A/MOSI0_A/SDA0/SCL1_C/SSLA0_B	GTOVUP/GTIOC8B/GTIOC8B/ GTIOC2B/GTIOC7B	CMPOUT3
69	43	31	—	PA10	IRQ10/KR02	RXD0_A/MISO0_A/SCL0/SDA1_C/RSPCKA_B	GTOWUP/GTIOC9A/GTIOC9B/ GTIOC3A/GTIOC8B	CMPOUT0
70	44	32	—	PA11	IRQ11/KR03	CTS0_A/RXD1_C/MISO1_C/SCL1/MOSIA_B/CTX0	GTETRGD/GTIOC9B/GTETRGC/ GTIOC3B	CMPOUT1
71	45	33	CACREF	PA12	IRQ12/KR04	CTS0_RTS0/SS0_A/DE0/TXD1_C/MOSI1_C/SDA1/ MISOA_B/CRX0	GTETRGB/GTCPPO0/GTCPPO2/ GTADSM0/GTCPPO7	ADTRG1
72	46	34	TMS/SWDIO	PA13	—	SCK0_C/DE0/CTS1_RTS1/SS1_C/DE1	AGTO0	—
73	—	—	VCL	—	—	—	—	—
74	47	35	VSS	—	—	—	—	—
75	48	36	VCC	—	—	—	—	—
76	49	37	TCK/SWCLK	PA14	—	TXD0_C/MOSI0_C/SDA0/SCK9_B/DE9	AGTO1	—
77	50	38	TDI	PA15	IRQ1/KR02	RXD0_C/MISO0_C/SCL0/RXD9_B/MISO9_B/SCL9/ SSLA0_A	GTETRGB/GTADSM1/GTCPPO4	ADTRG0/CMPOUT012
78	51	—	—	PC10	IRQ6-DS/KR05	TXD1_B/MOSI1_B/SDA1/SCL0_B/RSPCKB_B	AGTIO1	CMPOUT0

Table 1.15 Pin list (3 of 3)

LQFP100	LQFP64, QFN64	LQFP48, QFN48	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt/KINT	SCI/IIC/SPI/CANFD	GPT/AGT	ADC/DAC12/ACMPHS
79	52	—	—	PC11	IRQ7-DS/KR06	RXD1_B/MISO1_B/SCL1/SDA0_B/MISOB_B	AGTOA1	CMPOUT1
80	53	—	—	PC12	IRQ8-DS/KR07	TXD4_B/MOSI4_B/SDA4/SCK1_B/DE1/MOSIB_B	AGTOB1	CMPOUT2
81	—	—	—	PD00	KR00	CTS2_A/RXD3_C/MISO3_C/SCL3/SSLB0_B/CRX0	GTADSM0/GTCPPO4	—
82	—	—	—	PD01	KR01	CTS2_RTS2/SS2_A/DE2/TXD3_C/MOSI3_C/SDA3/ SSLB1_B/CTX0	GTADSM1/GTCPPO7	—
83	54	—	CLKOUT	PD02	IRQ9-DS/KR02	RXD4_B/MISO4_B/SCL4/SCK3_C/DE3	GTCPPO0/GTCPPO2/AGTEE1	CMPOUT3
84	—	—	—	PD03	KR03	SCK4_B/DE4/CTS9_A/SSLB2_B	GTCPPO0	CMPOUT0
85	—	—	—	PD04	KR04	CTS4_RTS4/SS4_B/DE4/CTS9_RTS9/SS9_A/DE9/ SSLB3_B	GTCPPO1	CMPOUT1
86	—	—	—	PD05	KR05	TXD9_A/MOSI9_A/SDA9/SDA1_B/SSLA3_A	GTADSM0/GTCPPO3	—
87	—	—	—	PD06	KR06	RXD9_A/MISO9_A/SCL9/SCL1_B/SSLA2_A	GTCPPO4	—
88	—	—	—	PD07	KR07	SCK9_A/DE9/SSLA1_A	GTADSM1/GTCPPO7	—
89	55	39	TDO/SWO	PB03	IRQ0/KR03	TXD2_A/MOSI2_A/SDA2/TXD9_B/MOSI9_B/SDA9/ RSPCKA_A/CRX0	GTIOC4A/GTCPPO1/GTCPPO3/ AGTO1	ADTRG1/CMPOUT3
90	56	40	CACREF/VCOUT	PB04	IRQ13/KR04	RXD2_A/MISO2_A/SCL2/RXD3_D/MISO3_D/SCL3/ MISOA_A/CTX0	GTIOC4A/GTIOC5A/GTIOC0A/ AGTOA0	—
91	57	41	—	PB05	IRQ3-DS/KR05	SCK2_A/DE2/TXD3_D/MOSI3_D/SDA3/MOSIA_A/ CRX0	GTIU/GTIOC4B/GTIOC6A/GTIOC0B/ AGTOB0	—
92	58	42	—	PB06	IRQ4-DS/KR06	TXD0_D/MOSI0_D/SDA0/CTS3_RTS3/SS3_D/DE3/ SCL0_A/CTX0	GTIV/GTIOC5A/GTIOC4B/GTIOC1A/ AGTOA1	—
93	59	43	—	PB07	IRQ5-DS/KR07	RXD0_D/MISO0_D/SCL0/CTS1_RTS1/SS1_D/DE1/ SDA0_A	GTIW/GTIOC5B/GTETRGC/ GTIOC1B/AGTOB1	—
94	60	44	MD	P201	—	—	—	—
95	61	45	—	PB08	IRQ1-DS/KR00	RXD4/MISO4_C/SCL4/RXD1_D/MISO1_D/SCL1/ SCL1_A/CRX0	GTIOC6A/GTIOC5B/GTIOC2A/ AGTIO0	—
96	62	46	—	PB09	IRQ2-DS/KR01	TXD4/MOSI4_C/SDA4/TXD1_D/MOSI1_D/SDA1/ SDA1_A/CTX0	GTIOC6B/GTIOC2B/AGTIO1	—
97	—	—	CACREF	PE00	—	TXD0_E/MOSI0_E/SDA0/TXD9_D/MOSI9_D/SDA9/ SSLB3_C	GTETRGA/GTIOC4A/GTADSM0/ AGTEE0	ADTRG0
98	—	—	—	PE01	—	RXD0_E/MISO0_E/SCL0/RXD9_D/MISO9_D/SCL9/ SSLB2_C	GTOULO/GTIOC7A/GTIOC4B/ GTADSM1/AGTEE1	ADTRG1
99	63	47	VSS	—	—	—	—	—
100	64	48	VCC	—	—	—	—	—

Note: Several pin names have the added suffix of _A, _B, _C, _D, _E and _F. The suffix can be ignored when assigning functionality.

Table 1.15 引脚列表（3个中的3个）

LQFP100	LQFP64, QFN64	LQFP48, QFN48	电源、系统、时钟、调试、CAC	I/O ports	Ex. Interrupt/KINT	SCI/IIC/SPI/CANFD	GPT/AGT	ADC/DAC12/ACMPHS
79	52	—	—	PC11	IRQ7-DS/KR06	RXD1_B/MISO1_B/SCL1/SDA0_B/MISOB_B	AGTOA1	CMPOUT1
80	53	—	—	PC12	IRQ8-DS/KR07	TXD4_B/MOSI4_B/SDA4/SCK1_B/DE1/MOSIB_B	AGTOB1	CMPOUT2
81	—	—	—	PD00	KR00	CTS2_A/RXD3_C/MISO3_C/SCL3/SSLB0_B/CRX0	GTADSM0/GTCPPO4	—
82	—	—	—	PD01	KR01	CTS2_RTS2/SS2_A/DE2/TXD3_C/MOSI3_C/SDA3/ SSLB1_B/CTX0	GTADSM1/GTCPPO7	—
83	54	—	CLKOUT	PD02	IRQ9-DS/KR02	RXD4_B/MISO4_B/SCL4/SCK3_C/DE3	GTCPPO0/GTCPPO2/AGTEE1	CMPOUT3
84	—	—	—	PD03	KR03	SCK4_B/DE4/CTS9_A/SSLB2_B	GTCPPO0	CMPOUT0
85	—	—	—	PD04	KR04	CTS4_RTS4/SS4_B/DE4/CTS9_RTS9/SS9_A/DE9/ SSLB3_B	GTCPPO1	CMPOUT1
86	—	—	—	PD05	KR05	TXD9_A/MOSI9_A/SDA9/SDA1_B/SSLA3_A	GTADSM0/GTCPPO3	—
87	—	—	—	PD06	KR06	RXD9_A/MISO9_A/SCL9/SCL1_B/SSLA2_A	GTCPPO4	—
88	—	—	—	PD07	KR07	SCK9_A/DE9/SSLA1_A	GTADSM1/GTCPPO7	—
89	55	39	TDO/SWO	PB03	IRQ0/KR03	TXD2_A/MOSI2_A/SDA2/TXD9_B/MOSI9_B/SDA9/ RSPCKA_A/CRX0	GTIOC4A/GTCPPO1/GTCPPO3/ AGTO1	ADTRG1/CMPOUT3
90	56	40	CACREF/VCOUT	PB04	IRQ13/KR04	RXD2_A/MISO2_A/SCL2/RXD3_D/MISO3_D/SCL3/ MISOA_A/CTX0	GTIOC4A/GTIOC5A/GTIOC0A/ AGTOA0	—
91	57	41	—	PB05	IRQ3-DS/KR05	SCK2_A/DE2/TXD3_D/MOSI3_D/SDA3/MOSIA_A/ CRX0	GTIU/GTIOC4B/GTIOC6A/GTIOC0B/ AGTOB0	—
92	58	42	—	PB06	IRQ4-DS/KR06	TXD0_D/MOSI0_D/SDA0/CTS3_RTS3/SS3_D/DE3/ SCL0_A/CTX0	GTIV/GTIOC5A/GTIOC4B/GTIOC1A/ AGTOA1	—
93	59	43	—	PB07	IRQ5-DS/KR07	RXD0_D/MISO0_D/SCL0/CTS1_RTS1/SS1_D/DE1/ SDA0_A	GTIW/GTIOC5B/GTETRGC/ GTIOC1B/AGTOB1	—
94	60	44	MD	P201	—	—	—	—
95	61	45	—	PB08	IRQ1-DS/KR00	RXD4/MISO4_C/SCL4/RXD1_D/MISO1_D/SCL1/ SCL1_A/CRX0	GTIOC6A/GTIOC5B/GTIOC2A/ AGTIO0	—
96	62	46	—	PB09	IRQ2-DS/KR01	TXD4/MOSI4_C/SDA4/TXD1_D/MOSI1_D/SDA1/ SDA1_A/CTX0	GTIOC6B/GTIOC2B/AGTIO1	—
97	—	—	CACREF	PE00	—	TXD0_E/MOSI0_E/SDA0/TXD9_D/MOSI9_D/SDA9/ SSLB3_C	GTETRGA/GTIOC4A/GTADSM0/ AGTEE0	ADTRG0
98	—	—	—	PE01	—	RXD0_E/MISO0_E/SCL0/RXD9_D/MISO9_D/SCL9/ SSLB2_C	GTOULO/GTIOC7A/GTIOC4B/ GTADSM1/AGTEE1	ADTRG1
99	63	47	VSS	—	—	—	—	—
100	64	48	VCC	—	—	—	—	—

Note: 几个管脚名称添加了_A、_B、_C、_D、_E和_F的后缀。分配功能时可以忽略后缀。

2. CPU

The MCU is based on the Arm® Cortex®-M33 core.

2.1 Overview

2.1.1 CPU

- Arm Cortex-M33
  - Revision: r0p4-00rel1
  - Armv8-M architecture profile
  - Single Precision Floating-Point Unit compliant with the ANSI/IEEE Std 754-2008
- SAU (Security Attribution Unit): 0 region
- IDAU (Implementation Defined Attribution Unit): 8 regions
  - Code flash (secure/non-secure callable/non-secure)
  - Data Flash (secure/non-secure)
  - SRAM0 (secure/non-secure callable/non-secure)
- Memory Protection Unit (MPU)
  - Armv8 Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Two Systick timers: Secure and Non-secure instance
  - Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK)

See reference 1. and reference 2. in section 2.14. References for details.

2.1.2 Debug

- Arm® CoreSight™ ETM-M33
  - Revision: r0p2-00rel0
  - ARM ETM Architecture version 4.2
- Instrumentation Trace Macrocell (ITM)
- Data Watchpoint and Trace Unit (DWT)
  - 4 comparators for watchpoints and triggers
- Breakpoint Unit (BPU)
  - Breakpoint function is available.
    - 8 instruction comparators
    - 0 literal comparators
- Time Stamp Generator (TSG)
  - Time stamp for ETM and ITM
  - Driven by CPU clock
- Debug Register Module (DBGREG)
  - Reset control
  - Halt control
- Debug Access Port (DAP)

2. CPU

MCU基于Arm®Cortex®-M33内核。

2.1 Overview

2.1.1 CPU

- Arm Cortex-M33
  - Revision: r0p4-00rel1
    Armv8-M架构配置文件
    符合ANSIIEEEStd754-2008的单精度浮点单元
- ●SAU（安全归属单元）：0地区
- ●IDAU（实施定义的归因单元）：8个地区
    代码闪存（安全非安全可调用非安全）
    数据闪存（安全非安全）
  - SRAM0 (secure/non-secure callable/non-secure)
- ●内存保护单元（MPU）
    Armv8保护内存系统架构(PMSAv8)
    安全MPU(MPU_S)：8个区域
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
    两个Systick计时器：安全和非安全实例
    由SysTick定时器时钟(SYSTICCLK)或系统时钟(ICLK)驱动

请参阅第2.14节中的参考1.和参考2.。详情参考。

2.1.2 Debug

- Arm® CoreSight™ ETM-M33
  - Revision: r0p2-00rel0
    ARMETM架构版本4.2
- ●仪器跟踪宏单元(ITM)
- ●数据观察点和跟踪单元(DWT)
    4个用于观察点和触发器的比较器
- Breakpoint Unit (BPU)
    断点功能可用。
    - 8 instruction comparators
    - 0 literal comparators
- ●时间戳生成器(TSG)
    ETM和ITM的时间戳
    由CPU时钟驱动
- ●调试寄存器模块（DBGREG）
    重置控制
    停止控制
- ●调试访问端口(DAP)

- JTAG Debug Port (JTAG-DP)
- Serial Wire Debug Port (SW-DP)

- Cortex-M33 Trace Port Interface Unit (TPIU)
  - 4 bits TPIU formatter output
  - Serial Wire Output
- Cross Trigger Interface (CTI)
- Embedded Trace Buffer (ETB)
  - CoreSight Trace Memory Controller with ETB configuration
  - Buffer size: 2 KB

See reference 1. and reference 2. in section 2.14. References for details.

2.1.3 Operating Frequency

The operating frequencies for the MCU are as follows:

- CPU: maximum 240 MHz
- 4-bit TPIU trace interface: maximum 60 MHz
- Serial Write Output (SWO) trace interface: maximum 60 MHz
- Joint Test Action Group (JTAG) interface: maximum 25 MHz
- Serial Wire Data (SWD) interface: maximum 25 MHz

2.1.4 Block Diagram

Figure 2.1 shows a block diagram of the Cortex-M33 core.

JTAG调试端口(JTAG-DP)
串行线调试端口(SW-DP)

●Cortex-M33跟踪端口接口单元(TPIU)
4位TPIU格式化输出
串行线输出

●交叉触发接口(CTI)

●嵌入式跟踪缓冲区(ETB)
具有ETB配置的CoreSight跟踪内存控制器
- Buffer size: 2 KB

请参阅第2.14节中的参考1.和参考2.。详情参考。

2.1.3 工作频率

MCU的工作频率如下：

- CPU: maximum 240 MHz

●4位TPIU跟踪接口：最大60MHz
●串行写输出(SWO)跟踪接口：最大60MHz
●联合测试行动组(JTAG)接口：最大25MHz
●串行线数据(SWD)接口：最大25MHz

2.1.4 框图

图2.1显示了Cortex-M33内核的框图。

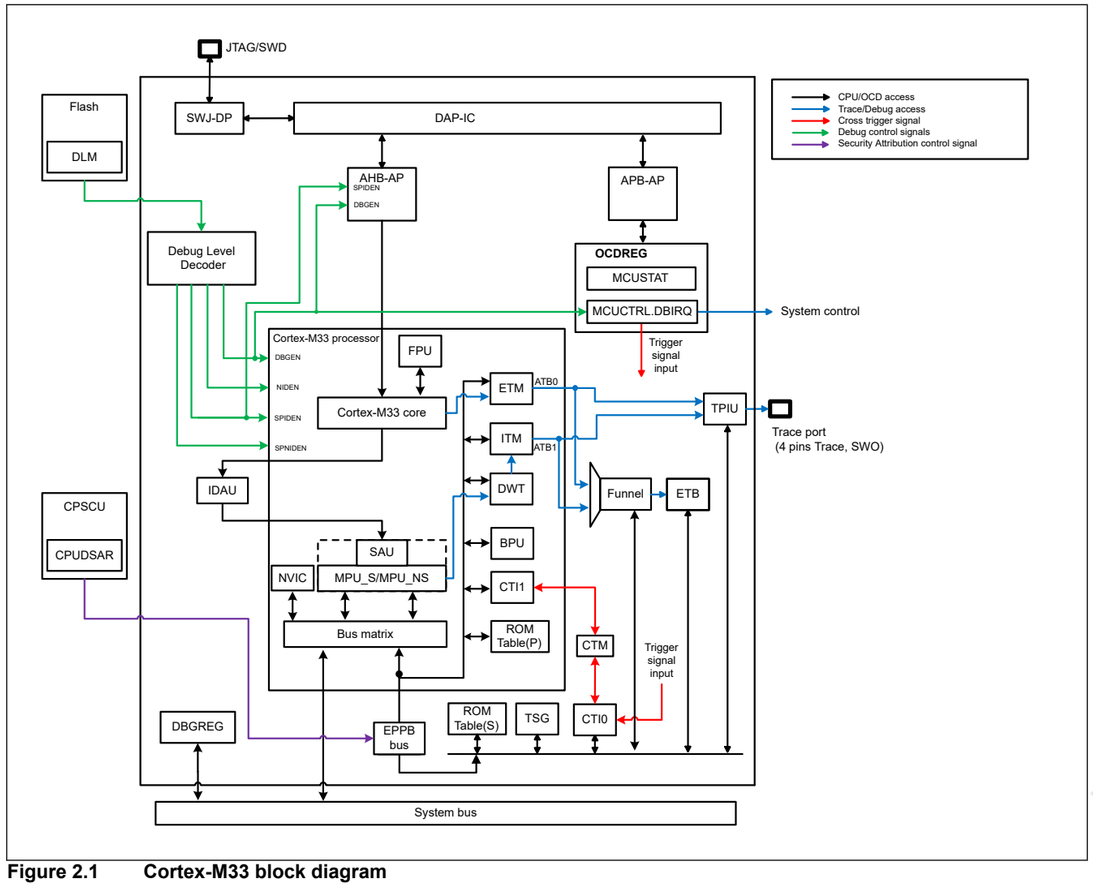


Figure 2.1 Cortex-M33 block diagram

2.2 Implementation Options

Table 2.1 shows the implementation options of the MCU.

Table 2.1 Implementation options (1 of 2)

Option	Implementation
SAU	Not included
IDAU	Included, 8 regions
MPU	Included, 8 regions for Secure and 8 regions for Non-secure
BPU	Included
Cross Trigger Interface (CTI)	Included
DWT	Included
Number of Wakeup Interrupt Controllers (WIC)	Not included ICU can wake up CPU instead of WIC. See section 12, Interrupt Controller Unit (ICU) for details.
TPIU	Included • 4 bits TPIU formatter output • Serial Wire Output
FPU	Included
DSP	Included

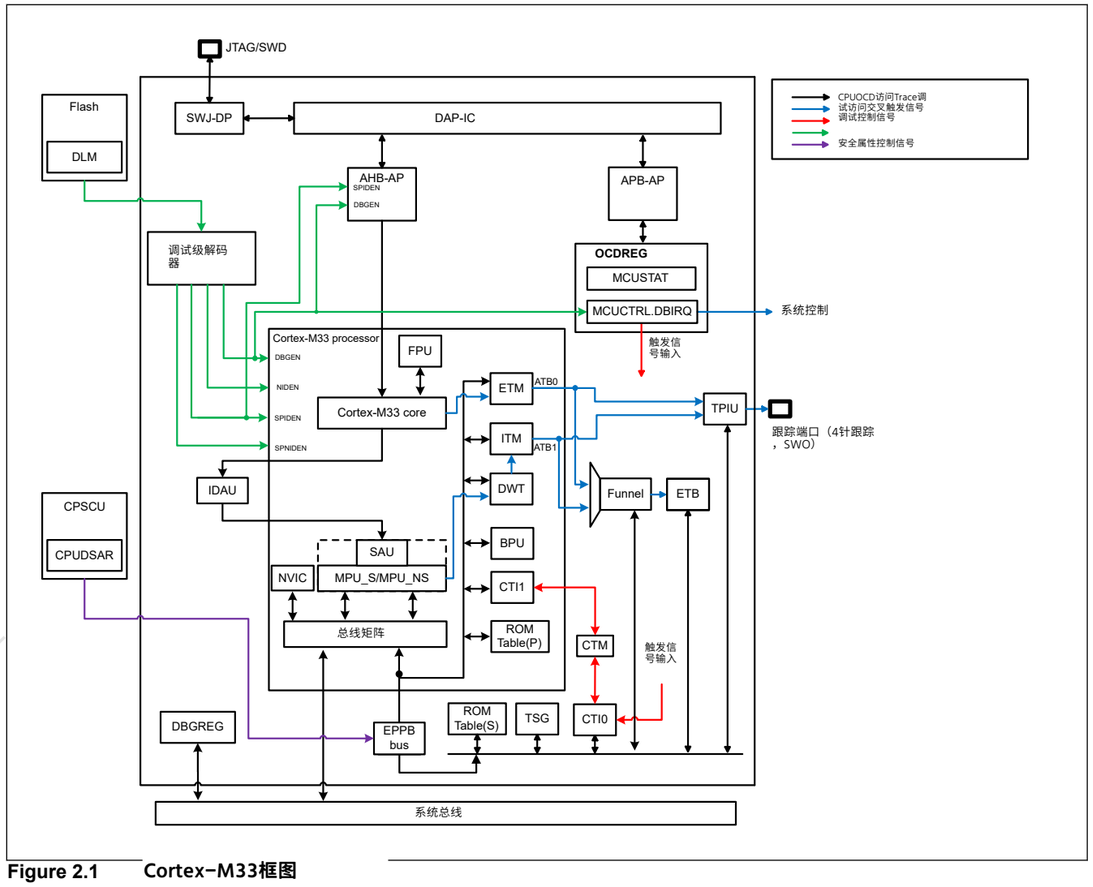


Figure 2.1 Cortex-M33框图

2.2 实施选项

表2.1显示了MCU的实现选项。

Table 2.1 实施选项（2个中的1个）

Option	Implementation
SAU	不包含
IDAU	包括，8个地区
MPU	包括，8个安全区域和8个非安全区域
BPU	Included
交叉触发接口(CTI)	Included
DWT	Included
唤醒中断控制器(WIC)的数量	不包含 ICU可以唤醒CPU而不是WIC。有关详细信息，请参见第12节，中断控制器单元(ICU)。
TPIU	Included • 4位TPIU格式化输出 • 串行线输出
FPU	Included
DSP	Included

Table 2.1 Implementation options (2 of 2)

Option	Implementation
Embedded Trace Macrocell (ETM)	Included
Sleep mode power saving	Sleep mode and other low power modes are supported. For more details, see section 10, Low Power Modes. Note: SCB.SCR.SLEEPDEEP is ignored.
Interrupts	96
Priority bits	4 bits (16 levels)
Endianness	Little-endian
Memory features	Cacheable attribute is utilized in the MCU. See section 13, Buses for the detail.
SysTick	Included
SYST_CALIB register (0x4000_0147)	Bit [31] = 0 Reference clock provided Bit [30] = 1 TENMS value is inexact Bits [29:24] = 0x00 Reserved Bits [23:0] = 0x000147 TENMS: (32768 × 10 ms) - 1/32.768 kHz = 326.66 decimal = 327 with skew = 0x000147
Event input/output	Not implemented
Global exclusive monitor	Not implemented
System reset request output	The SYSRESETREQ bit in Application Interrupt and Reset Control Register causes a CPU reset

2.3 Trace Interface

A Trace Port Interface Unit (TPIU) and Serial Wire Output (SWO) provide trace output. Table 2.2 shows the MCU pins for the function. These pins are multiplexed with other functions.

Table 2.2 Trace function pins

Name	I/O	Function	When not in use
TCLK	Output	Trace clock	Open
TDATA0	Output	Trace data output 0	Open
TDATA1	Output	Trace data output 1	Open
TDATA2	Output	Trace data output 2	Open
TDATA3	Output	Trace data output 3	Open
TDO/SWO	Output	Serial wire output multiplexed with JTAG TDO pin	Open

2.4 JTAG/SWD Interface

Table 2.3 shows the JTAG/SWD pins.

Table 2.3 JTAG/SWD pins

Name	I/O	Function	When not in use
TDI	Input	JTAG TDI pin	Pull-up
TDO/SWO	Output	JTAG TDO pin multiplexed with serial wire output	Open
TCK/SWCLK	Input	JTAG clock pin Serial wire clock pin	Pull-up
TMS/SWDIO	I/O	JTAG TMS pin Serial wire data I/O pin	Pull-up

Table 2.1 实施选项（2个中的2个）

Option	Implementation
嵌入式跟踪宏单元(ETM)	Included
睡眠模式省电	支持睡眠模式和其他低功耗模式。有关详细信息，请参阅第10节，低电源模式。 Note: SCB.SCR.SLEEPDEEP被忽略。
Interrupts	96
优先位	4 bits (16 levels)
Endianness	Little-endian
记忆功能	可缓存属性在MCU中使用。有关详细信息，请参阅第13节，总线。
SysTick	Included
SYST_CALIB register (0x4000_0147)	Bit [31] = 0 提供参考时钟 Bit [30] = 1 TENMS值不准确 Bits [29:24] = 0x00 Reserved Bits [23:0] = 0x000147 TENMS：(32768×10ms)132.768kHz=32 6.66十进制=327，偏斜=0x000147
Event input/output	未实现
全球独家监控	未实现
系统复位请求输出	应用程序中断和复位控制寄存器中的SYSRESETREQ位导致CPU复位

2.3 跟踪接口

跟踪端口接口单元(TPIU)和串行线输出(SWO)提供跟踪输出。表2.2显示了该功能的MCU引脚。这些引脚与其他功能复用。

Table 2.2 跟踪功能引脚

Name	I/O	Function	不使用时
TCLK	Output	跟踪时钟	Open
TDATA0	Output	跟踪数据输出0	Open
TDATA1	Output	跟踪数据输出1	Open
TDATA2	Output	跟踪数据输出2	Open
TDATA3	Output	跟踪数据输出3	Open
TDO/SWO	Output	串行线输出与JTAGTDO引脚复用	Open

2.4 JTAG/SWD Interface

表2.3显示了JTAGSWD引脚。

Table 2.3 JTAG/SWD pins

Name	I/O	Function	不使用时
TDI	Input	JTAG TDI pin	Pull-up
TDO/SWO	Output	JTAGTDO引脚与串行线输出复用	Open
TCK/SWCLK	Input	JTAG时钟引脚 串行线时钟引脚	Pull-up
TMS/SWDIO	I/O	JTAG TMS pin 串行线数据IO引脚	Pull-up

2.5 Security Attribution for Memory

In this MCU, SAU is not implemented and IDAU performs region definition for memory. IDAU divides the memory into 8 different areas as shown in Figure 2.2.

The code flash, the data flash, and the SRAM are divided into Secure (S), Non-secure (NS) and Non-secure callable (NSC) regions. These memory security attributions are set into the nonvolatile memory by the serial programming command when the device lifecycle is in SSD state. These memory security attributions are loaded into the IDAU and the memory controller before application execution. These memory security attributions cannot be updated by application but can read through the dedicated registers.

Note: When configuring, the memory regions should satisfy the setting condition of minimum address unit shown in Table 2.4.

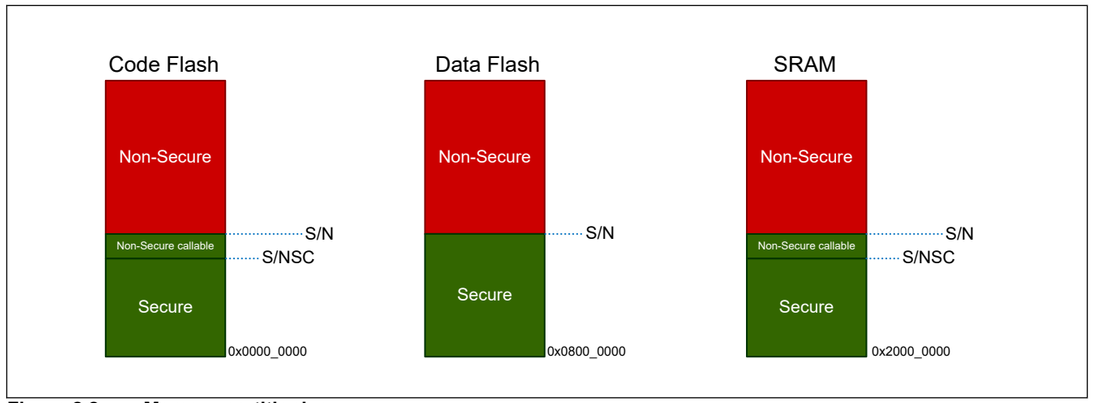


Figure 2.2 Memory partitioning

Table 2.4 S/NS and S/NSC boundary list

Boundary	Code flash	Data flash	SRAM
S/NS	32 KB	1 KB	8 KB
S/NSC	1 KB	—	1 KB

Each region has its dedicated ID as follows. For more details, see section 2.14. References.

IREGION (IDAU region number)	Description
0x0D	Non-secure SRAM
0x0E	Non-secure callable SRAM
0x0F	Secure SRAM
0x09	Non-secure data flash
0x0B	Secure data flash
0x05	Non-secure code flash
0x06	Non-secure callable code flash
0x07	Secure code flash

2.6 Debug Function

2.6.1 Debugger connectivity

In this MCU, debug function is considered in three levels, DBG0, DBG1, DBG2. At DBG0, no debug function is available. DBG1 level is defined as non-secure debug in ARMv-8 and the debugger can only access defined non-secure debug accessible regions. DBG2 level is defined as secure debug in ARMv-8 and at this level, nonsecure and secure debug function is enabled and can be accessible from the debugger.

2.5 内存安全归属

在这个MCU中，没有实现SAU，而IDAU为内存执行区域定义。IDAU将内存划分为8个不同的区域，如图2.2所示。

代码闪存、数据闪存和SRAM分为安全(S)、非安全(NS)和非安全可调用(NSC)区域。当设备生命周期处于SSD状态时，这些内存安全属性由串行编程命令设置到非易失性内存中。这些内存安全属性在应用程序执行之前被加载到IDAU和内存控制器中。这些内存安全属性不能由应用程序更新，但可以通过专用寄存器读取。

Note: 配置时，内存区域应满足表2.4所示的最小地址单元设置条件。

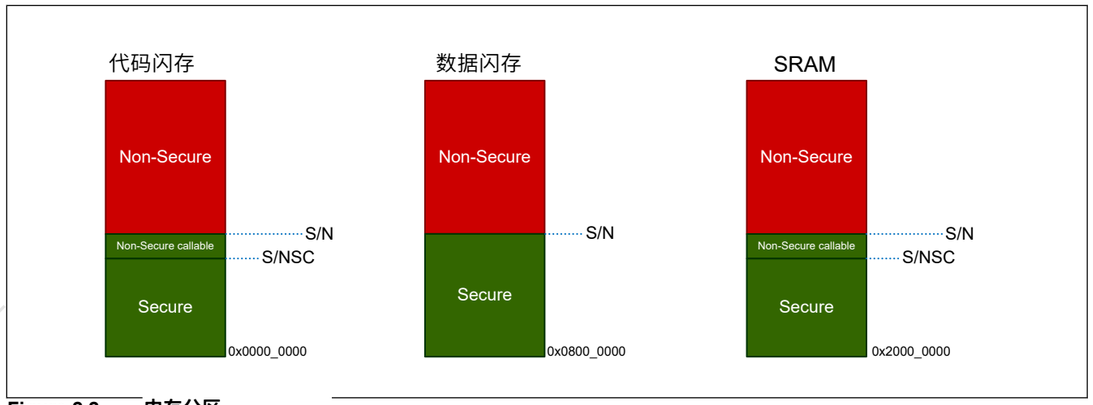


Figure 2.2 内存分区

Table 2.4 SNS和SNSC边界列表

Boundary	代码闪存	数据闪存	SRAM
S/NS	32 KB	1 KB	8 KB
S/NSC	1 KB	—	1 KB

每个区域都有其专用ID，如下所示。有关详细信息，请参阅第2.14节。参考。

IREGION (IDAU region number)	Description
0x0D	Non-secure SRAM
0x0E	Non-secure callable SRAM
0x0F	Secure SRAM
0x09	非安全数据闪存
0x0B	安全数据闪存
0x05	非安全代码闪存
0x06	非安全可调用代码闪存
0x07	安全代码闪存

2.6 调试功能

2.6.1 调试器连接

在本单片机中，调试功能分为三个层次，DBG0、DBG1、DBG2。在DBG0，没有调试功能可用。
DBG1级别在ARMv-8中定义为非安全调试，调试器只能访问已定义的非安全调试可访问区域。DBG2级别在ARMv-8中定义为安全调试，在此级别，启用了非安全和安全调试功能，并且可以从调试器访问。

Debug level is determined by the Device Lifecycle Management (DLM) state of the product.

See Figure 2.1 for debugger accessible regions.

Table 2.5 shows the CPU debug function and conditions.

Table 2.5 CPU debug function and conditions

Condition			Permitted debug function
OCD connect*1	DLM State	Debug level	Description
Connected	CM	DBG2	All debug functions are available
Connected	SSD	DBG2	All debug functions are available
Connected	NSECSD	DBG1	Only Non-secure debug function is available
Connected	DPL	DBG0	Debugger connection is not available
Connected	LCK_DBG	DBG0	Debugger connection is not available
Connected	LCK_BOOT	DBG0	Debugger connection is not available
Connected	RMA_REQ	DBG0	Debugger connection is not available
Connected	RMA_ACK	DBG2	All debug functions are available

Note 1. OCD connect is determined by the CDBGPWRUPREQ bit output in the SWJ-DP register. The bit can only be written by the OCD. However, the level of the bit can be confirmed by reading the DBGSTR.CDBGPWRUPREQ bit.

2.6.2 Emulator Connection

Renesas provides the emulator which supports both debugging using SWD or JTAG communication and serial programming using SCI communication. This emulator makes it easy to switch between debug-ging and serial programming.

Table 2.6 shows the pinout of 10 pin or 20 pin socket pinouts when using this emulator. The pinout of SWD and JTAG is ARM standard, and MD, TXD, RXD pins are added for the serial programming using SCI communication.

The serial programming interface must be used to program the TrustZone IDAU boundary register settings.

It is recommended to connect PA14/SWCLK/TCK and P201/MD pins using wired OR circuit on the board to use both debugging and serial programming.

Table 2.6 Pin assign for emulator

Pin No.	SWD	JTAG	Serial Programming using SCI
1	VCC	VCC	VCC
2	PA13/SWDIO	PA13/TMS	NC
4	PA14/SWCLK Wired OR with P201/MD	PA14/TCK Wired OR with P201/MD	P201/MD
6	PB03/SWO/TXD9	PB03/SWO/TXD9	PB03/TXD9
8	PA15/RXD9	PA15/TDI/RXD9	PA15/RXD9
9	GNDdetect	GNDdetect	GNDdetect
10	nRESET	nRESET	nRESET
12	PE02/TCLK	PE02/TCLK	NC
14	PE03/TDATA[0]	PE03/TDATA[0]	NC
16	PE04/TDATA[1]	PE04/TDATA[1]	NC
18	PE05/TDATA[2]	PE05/TDATA[2]	NC
20	PE06/TDATA[3]	PE06/TDATA[3]	NC
3, 5, 15, 17, 19	GND	GND	GND
7	NC	NC	NC
11, 13	NC	NC	NC

调试级别由产品的设备生命周期管理(DLM)状态确定。

有关调试器可访问区域，请参见图2.1。

表2.5显示了CPU调试功能和条件。

Table 2.5 CPU调试功能及条件

Condition			允许的调试功能
强迫症连接*1	DLM State	调试级别	Description
Connected	CM	DBG2	所有调试功能均可用
Connected	SSD	DBG2	所有调试功能均可用
Connected	NSECSD	DBG1	只有非安全调试功能可用
Connected	DPL	DBG0	调试器连接不可用
Connected	LCK_DBG	DBG0	调试器连接不可用
Connected	LCK_BOOT	DBG0	调试器连接不可用
Connected	RMA_REQ	DBG0	调试器连接不可用
Connected	RMA_ACK	DBG2	所有调试功能均可用

注1.OCD连接由SWJ-DP寄存器中的CDBGPWUPREQ位输出决定。该位只能由OCD写入。
但是，可以通过读取DBGSTR.CDBGPWUPREQ位来确认该位的电平。

2.6.2 仿真器连接

瑞萨电子提供的仿真器支持使用SWD或JTAG通信进行调试和使用SCI通信进行串行编程。该仿真器可以轻松地在调试和串行编程之间切换。

表2.6显示了使用该仿真器时10针或20针插座的引脚排列。SWD和JTAG的管脚是ARM标准，并增加了MD、TXD、RXD引脚用于使用SCI通信的串行编程。

必须使用串行编程接口对TrustZoneIDAU边界寄存器设置进行编程。

建议使用板上的有线或电路连接PA14SWCLKTCK和P201MD引脚，以同时使用调试和串行编程。

Table 2.6 为模拟器分配引脚

针号	SWD	JTAG	使用SCI进行串行编程
1	VCC	VCC	VCC
2	PA13/SWDIO	PA13/TMS	NC
4	PA14/SWCLK 有线或带P201MD	PA14/TCK 有线或带P201MD	P201/MD
6	PB03/SWO/TXD9	PB03/SWO/TXD9	PB03/TXD9
8	PA15/RXD9	PA15/TDI/RXD9	PA15/RXD9
9	GNDdetect	GNDdetect	GNDdetect
10	nRESET	nRESET	nRESET
12	PE02/TCLK	PE02/TCLK	NC
14	PE03/TDATA[0]	PE03/TDATA[0]	NC
16	PE04/TDATA[1]	PE04/TDATA[1]	NC
18	PE05/TDATA[2]	PE05/TDATA[2]	NC
20	PE06/TDATA[3]	PE06/TDATA[3]	NC
3, 5, 15, 17, 19	GND	GND	GND
7	NC	NC	NC
11, 13	NC	NC	NC

2.6.3 Self-Hosted Debug Function

As described in section 2.7.6. CPUDSAR : CPU Debug Security Attribution Register, at the initial setting access from the CPU in non-secure state to CoreSight debug components is protected, that is, the non-secure access to Coresight debug components from the self-hosted debugger is not allowed when the debug level is DBG2 at the initial setting. Therfore, the CPUDSAR.CPUDSA0 must be set to 1 to enable the self-hosted debug for CPU in non-secure state.

Note: There is no restriction for the self-hosted debug function while the CPU is in the secure state.

2.6.4 Effect of Debug Function

The debug function effects inside and outside of CPU.

2.6.4.1 Low power mode

All CoreSight debug components can store the register settings even when the CPU enters Software Standby, Snooze or Deep Software Standby mode. However, AHB-AP cannot respond to On-Chip Debug (OCD) access in these low power modes. The OCD must wait for cancellation of the low power mode to access the CoreSight debug components. To request low power mode cancellation, the OCD can set the DBIRQ bit in the MCUCTRL register. For details, see section 2.7.5.2. MCUCTRL : MCU Control Register.

2.6.4.2 Reset

In OCD mode, some resets depend on the CPU status and the DBGSTOPCR register setting.

Table 2.7 Reset or interrupt and mode setting

Reset or interrupt name	Control in On-Chip Debug (OCD) mode	
	OCD break mode	OCD run mode
RES pin reset	Same as user mode	
Power-on reset	Same as user mode	
Independent watchdog timer reset/interrupt	Does not occur*1	Depends on DBGSTOPCR setting
Watchdog timer reset/interrupt	Does not occur*1	Depends on DBGSTOPCR setting
Voltage monitor 0 reset	Depends on DBGSTOPCR setting	
Voltage monitor 1 reset/interrupt	Depends on DBGSTOPCR setting	
Voltage monitor 2 reset/interrupt	Depends on DBGSTOPCR setting	
SRAM parity error reset/interrupt	Depends on DBGSTOPCR setting	
SRAM ECC error reset/interrupt	Depends on DBGSTOPCR setting	
Cache parity error reset/interrupt	Depends on DBGSTOPCR setting	
Bus master MPU error reset/interrupt	Same as user mode	
Deep software standby reset	Same as user mode	
Software reset	Same as user mode	

Note: In OCD break mode, the CPU is halted. In OCD run mode, the CPU is in OCD mode and the CPU is not halted.
Note 1. The IWDT and WDT always stop in this mode.

2.7 Programmers Model

2.7.1 Address Spaces

The MCU debug system includes two CoreSight Access Ports (AP):

- AHB-AP, which is connected to the CPU bus matrix and has the same access to the system address space as the CPU
- APB-AP, which has a dedicated address space (OCD address space) and is connected to the OCDREG registers.

Figure 2.3 shows a block diagram of the AP connection and address spaces.

2.6.3 自托管调试功能

如第2.7.6节所述。CPUDSAR:CPUDebugSecurityAttributionRegister 在初始设置时从非安全状态的CPU对CoreSight调试组件的访问受到保护，即不允许从自托管调试器对Coresight调试组件的非安全访问初始设置时调试级别为DBG2。因此，必须将CPUDSAR.CPUDSA0设置为1以启用非安全状态下CPU的自托管调试。

Note: 当CPU处于安全状态时，自托管调试功能没有限制。

2.6.4 调试功能的效果

调试功能影响CPU内部和外部。

2.6.4.1 低功耗模式

即使CPU进入软件待机、贪睡或深度软件待机模式，所有CoreSight调试组件都可以存储寄存器设置。但是，AHB-AP在这些低功耗模式下无法响应片上调试(OCD)访问。OCD必须等待取消低功耗模式才能访问CoreSight调试组件。要请求取消低功耗模式，OCD可以设置MCUCTRL寄存器中的DBIRQ位。详见2.7.5.2节。MCUCTRL：MCU控制寄存器。

2.6.4.2 Reset

在OCD模式下，一些复位取决于CPU状态和DBGSTOPCR寄存器设置。

Table 2.7 复位或中断和模式设置

重置或中断名称	片上调试(OCD)模式下的控制	
	强迫症休息模式	强迫症运行模式
RES引脚复位	与用户模式相同	
Power-on reset	与用户模式相同	
独立看门狗定时器复位中断	不发生*1	取决于DBGSTOPCR设置
看门狗定时器复位中断	不发生*1	取决于DBGSTOPCR设置
电压监控器0复位	取决于DBGSTOPCR设置	
电压监视器1复位中断	取决于DBGSTOPCR设置	
电压监视器2复位中断	取决于DBGSTOPCR设置	
SRAM奇偶校验错误复位中断	取决于DBGSTOPCR设置	
SRAM ECC error reset/interrupt	取决于DBGSTOPCR设置	
缓存奇偶校验错误复位中断	取决于DBGSTOPCR设置	
总线主控MPU错误复位中断	与用户模式相同	
深度软件待机复位	与用户模式相同	
软件复位	与用户模式相同	

Note: 在OCD中断模式下，CPU停止。在OCD运行模式下，CPU处于OCD模式并且CPU不会停止。
注1.IWDT和WDT在此模式下始终停止。

2.7 程序员模型

2.7.1 地址空间

MCU调试系统包括两个CoreSight访问端口(AP)：

- AHB-AP，与CPU总线矩阵相连，与CPU具有相同的系统地址空间访问权限
- APB-AP，具有专用的地址空间（OCD地址空间）并连接到OCDREG寄存器。

图2.3显示了AP连接和地址空间的框图。

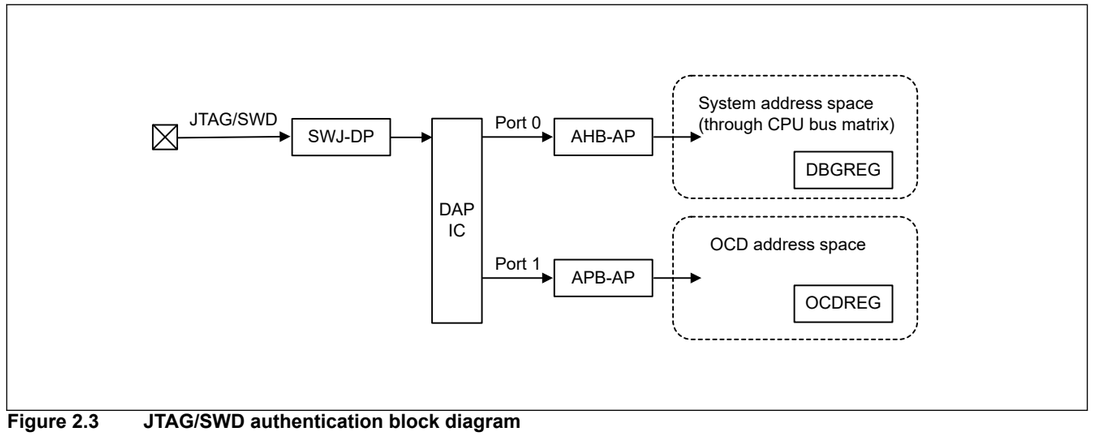


Figure 2.3 JTAG/SWD authentication block diagram

For debugging purposes, there are two register modules, DBGREG and OCDREG. DBGREG is located in the system address space and can be accessed from the OCD emulator, the CPU, and other bus masters in the MCU. OCDREG is located in the OCD address space and can only be accessed from the OCD tool. The CPU and other bus masters cannot access OCDREG.

2.7.2 Peripheral Address Map

In system address space, the Cortex-M33 core has a Private Peripheral Bus (PPB) which can be accessed only from CPU and OCD emulator. The PPB is expanded from the original implementation of the Cortex-M33 core for this MCU. Table 2.8 shows the address map of the MCU.

Table 2.8 Peripheral address map

Component name	Start address	End address	Note
ITM	0xE000_0000	0xE000_0FFF	See reference 2. in section 2.14. References
DWT	0xE000_1000	0xE000_1FFF	See reference 2. in section 2.14. References
BPU	0xE000_2000	0xE000_2FFF	See reference 2. in section 2.14. References
Secure SCS/SCS	0xE000_E000	0xE000_EFFF	See reference 1. in section 2.14. References
Non-Secure SCS	0xE002_E000	0xE002_EFFF	See reference 2. in section 2.14. References
TPIU	0xE004_0000	0xE004_0FFF	See reference 3. in section 2.14. References
ETM	0xE004_1000	0xE004_1FFF	See reference 1. in section 2.14. References
CTI1	0xE004_2000	0xE004_2FFF	See reference 2. in section 2.14. References
CTI0	0xE004_4000	0xE004_4FFF	See reference 4. in section 2.14. References
ATB Funnel	0xE004_7000	0xE004_7FFF	See section 2.9. CoreSight ATB Funnel and reference 4. in section 2.14. References
ETB	0xE004_8000	0xE004_8FFF	See reference 4. in section 2.14. References
Time Stamp Generator	0xE004_9000	0xE004_9FFF	See section 2.11. CoreSight Time Stamp Generator and reference 4. in section 2.14. References
System ROM Table	0xE00F_E000	0xE00F_EFFF	See reference 3. in section 2.14. References
Processor ROM Table	0xE00F_F000	0xE00F_FFFF	See reference 2. in section 2.14. References

2.7.3 CoreSight ROM Table

The MCU contains two CoreSight ROM Tables, the processor and system ROM Tables. The Processor ROM Table contains entries which hold a list of debug components inside the processor. The System ROM Table contains entries of Processor ROM Table and others debug components outside the processor.

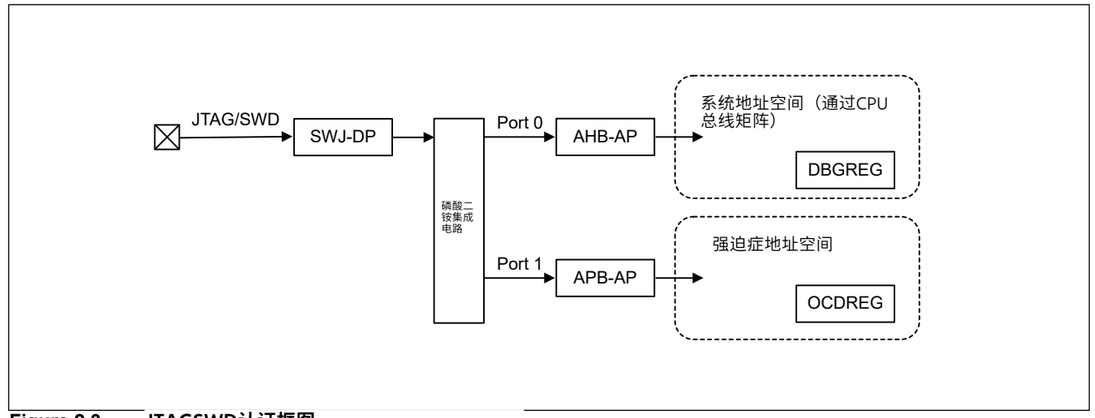


Figure 2.3 JTAGSWD认证框图

出于调试目的，有两个寄存器模块，DBGREG和OCDREG。DBGREG位于系统地址空间中，可以从OCD仿真器、CPU和MCU中的其他总线主控器访问。OCDREG位于OCD地址空间，只能从OCD工具访问。CPU和其他总线主机无法访问OCDREG。

2.7.2 外设地址映射

在系统地址空间中，Cortex-M33内核有一个专用外设总线(PPB)，只能从CPU和OCD仿真器访问。PPB是从该MCU的Cortex-M33内核的原始实现扩展而来的。表2.8显示了MCU的地址映射。

Table 2.8 外设地址图

组件名称	起始地址	结束地址	Note
ITM	0xE000_0000	0xE000_0FFF	请参阅第2.14节中的参考2。参考
DWT	0xE000_1000	0xE000_1FFF	请参阅第2.14节中的参考2。参考
BPU	0xE000_2000	0xE000_2FFF	请参阅第2.14节中的参考2。参考
Secure SCS/SCS	0xE000_E000	0xE000_EFFF	请参阅第2.14节中的参考1。参考
Non-Secure SCS	0xE002_E000	0xE002_EFFF	请参阅第2.14节中的参考2。参考
TPIU	0xE004_0000	0xE004_0FFF	请参见第2.14节中的参考3。参考
ETM	0xE004_1000	0xE004_1FFF	请参阅第2.14节中的参考1。参考
CTI1	0xE004_2000	0xE004_2FFF	请参阅第2.14节中的参考2。参考
CTI0	0xE004_4000	0xE004_4FFF	参见第2.14节中的参考4。参考
ATB Funnel	0xE004_7000	0xE004_7FFF	请参阅第2.9节。CoreSightATB漏斗和参考4.在第2.14节中。References
ETB	0xE004_8000	0xE004_8FFF	参见第2.14节中的参考4。参考
时间戳生成器	0xE004_9000	0xE004_9FFF	请参阅第2.11节。CoreSight时间戳生成器和第2.14节中的参考4。参考
系统ROM表	0xE00F_E000	0xE00F_EFFF	请参见第2.14节中的参考3。参考
处理器ROM表	0xE00F_F000	0xE00F_FFFF	请参阅第2.14节中的参考2。参考

2.7.3 CoreSightROM表

MCU包含两个CoreSightROM表，即处理器和系统ROM表。处理器ROM表包含保存处理器内部调试组件列表的条目。系统ROM表包含处理器ROM表和处理器外部的其他调试组件的条目。

2.7.3.1 ROM entries

ROM entries hold a list of components in the system. OCD emulator can use the ROM entries to determine which components are implemented in a system.

Table 2.9 and Table 2.10 show the System ROM entries and Processor ROM entries. See reference 5. in section 2.14. References for details.

Table 2.9 System ROM entries

#	Address	Access size	R/W	Value	Target module pointer
0	0xE00F_E000	32 bits	R	0xFFF46003	CTI0
1	0xE00F_E004	32 bits	R	0xFFF49003	Funnel
2	0xE00F_E008	32 bits	R	0xFFF4A003	ETB
3	0xE00F_E00C	32 bits	R	0xFFF4B003	TSG
4	0xE00F_E010	32 bits	R	0xFFF42003	TPIU
5	0xE00F_E014	32 bits	R	0x00001003	Processor ROM table
6	0xE00F_E018	32 bits	R	0x00000000	End of entries

Table 2.10 Processor ROM Entries

#	Address	Access size	R/W	Value	Target module pointer
0	0xE00F_F000	32 bits	R	0xFFF0F003	SCS
1	0xE00F_F004	32 bits	R	0xFFF02003	DWT
2	0xE00F_F008	32 bits	R	0xFFF03003	BPU
3	0xE00F_F00C	32 bits	R	0xFFF01003	ITM
4	0xE00F_F014	32 bits	R	0xFFF42003	ETM
5	0xE00F_F018	32 bits	R	0xFFF43003	CTI1
6	0xE00F_F020	32 bits	R	0x00000000	End of entries

2.7.3.2 CoreSight component registers

The CoreSight ROM Table lists the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.11 shows the registers. See reference 5. in section 2.14. References for details of each register.

Table 2.11 CoreSight component registers in the CoreSight ROM Table

Name	Address	Access size	R/W	Initial value
PID4	0xE00F_EFD0	32 bits	R	0x00000004
PID5	0xE00F_EFD4	32 bits	R	0x00000000
PID6	0xE00F_EFD8	32 bits	R	0x00000000
PID7	0xE00F_EFDC	32 bits	R	0x00000000
PID0	0xE00F_EFE0	32 bits	R	0x0000003E
PID1	0xE00F_EFE4	32 bits	R	0x00000030
PID2	0xE00F_EFE8	32 bits	R	0x0000000A
PID3	0xE00F_EFEC	32 bits	R	0x00000000
CID0	0xE00F_EFF0	32 bits	R	0x0000000D
CID1	0xE00F_EFF4	32 bits	R	0x00000010
CID2	0xE00F_EFF8	32 bits	R	0x00000005
CID3	0xE00F_EFFC	32 bits	R	0x000000B1

2.7.3.1 ROM条目

ROM条目保存系统中的组件列表。OCD仿真器可以使用ROM条目来确定系统中实现了哪些组件。

表2.9和表2.10显示了系统ROM条目和处理器ROM条目。请参阅第2.14节中的参考5。
详情参考。

Table 2.9 系统ROM条目

#	Address	访问大小	R/W	Value	目标模块指针
0	0xE00F_E000	32 bits	R	0xFFF46003	CTI0
1	0xE00F_E004	32 bits	R	0xFFF49003	Funnel
2	0xE00F_E008	32 bits	R	0xFFF4A003	ETB
3	0xE00F_E00C	32 bits	R	0xFFF4B003	TSG
4	0xE00F_E010	32 bits	R	0xFFF42003	TPIU
5	0xE00F_E014	32 bits	R	0x00001003	处理器ROM表
6	0xE00F_E018	32 bits	R	0x00000000	条目结束

Table 2.10 处理器ROM条目

#	Address	访问大小	R/W	Value	目标模块指针
0	0xE00F_F000	32 bits	R	0xFFF0F003	SCS
1	0xE00F_F004	32 bits	R	0xFFF02003	DWT
2	0xE00F_F008	32 bits	R	0xFFF03003	BPU
3	0xE00F_F00C	32 bits	R	0xFFF01003	ITM
4	0xE00F_F014	32 bits	R	0xFFF42003	ETM
5	0xE00F_F018	32 bits	R	0xFFF43003	CTI1
6	0xE00F_F020	32 bits	R	0x00000000	条目结束

2.7.3.2 CoreSight组件寄存器

CoreSightROM表列出了ArmCoreSight架构中定义的CoreSight组件寄存器。
表2.11显示了寄存器。请参阅第2.14节中的参考5。每个寄存器的详细信息参考。

Table 2.11 CoreSightROM表中的CoreSight组件寄存器

Name	Address	访问大小	R/W	初始值
PID4	0xE00F_EFD0	32 bits	R	0x00000004
PID5	0xE00F_EFD4	32 bits	R	0x00000000
PID6	0xE00F_EFD8	32 bits	R	0x00000000
PID7	0xE00F_EFDC	32 bits	R	0x00000000
PID0	0xE00F_EFE0	32 bits	R	0x0000003E
PID1	0xE00F_EFE4	32 bits	R	0x00000030
PID2	0xE00F_EFE8	32 bits	R	0x0000000A
PID3	0xE00F_EFEC	32 bits	R	0x00000000
CID0	0xE00F_EFF0	32 bits	R	0x0000000D
CID1	0xE00F_EFF4	32 bits	R	0x00000010
CID2	0xE00F_EFF8	32 bits	R	0x00000005
CID3	0xE00F_EFFC	32 bits	R	0x000000B1

2.7.4 DBGREG Module

The DBGREG module controls the debug functionalities and is implemented as a CoreSight-compliant component.

Table 2.12 shows the DBGREG registers other than the CoreSight component registers.

Table 2.12 Non-CoreSight DBGREG registers

Name		DAP port	Address	Access size	R/W
Debug Status Register	DBGSTR	Port 0	0x4001_B000	32 bits	R
Debug Stop Control Register	DBGSTOPCR	Port 0	0x4001_B010	32 bits	R/W

2.7.4.1 DBGSTR : Debug Status Register

Base address: DBG = 0x4001_B000

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
27:0	—	These bits are read as 0.	R
28	CDBGPWRUPREQ	Debug power-up request 0: OCD is not requesting debug power up 1: OCD is requesting debug power up	R
29	CDBGPWRUPACK	Debug power-up acknowledge 0: Debug power-up request is not acknowledged 1: Debug power-up request is acknowledged	R
31:30	—	These bits are read as 0.	R

The DBGSTR register is a status register which indicates the state of the debug power-up request to the MCU from the emulator.

2.7.4.2 DBGSTOPCR : Debug Stop Control Register

Base address: DBG = 0x4001_B000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DBGSTOP_CPER	—	—	—	—	—	DBGSTOP_RECCR	DBGSTOP_RPER	—	—	—	—	—	DBGSTOP_LVD2	DBGSTOP_LVD1	DBGSTOP_LVD0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

2.7.4 DBGREG Module

DBGREG模块控制调试功能并被实现为符合CoreSight的组件。

表2.12显示了除CoreSight组件寄存器之外的DBGREG寄存器。

Table 2.12 Non-CoreSight DBGREG registers

Name		端口	Address	访问大小	R/W
调试状态寄存器	DBGSTR	Port 0	0x4001_B000	32 bits	R
调试停止控制寄存器	DBGSTOPCR	Port 0	0x4001_B010	32 bits	R/W

2.7.4.1 DBGSTR：调试状态寄存器

Base address: DBG = 0x4001_B000

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
27:0	—	这些位读为0。	R
28	CDBGPWRUPREQ	调试上电请求 0：OCD不请求调试上电1：OCD请求调试上电	R
29	CDBGPWRUPACK	调试上电确认 0：未确认调试上电请求1：确认调试上电请求	R
31:30	—	这些位读为0。	R

DBGSTR寄存器是一个状态寄存器，它指示从仿真器到MCU的调试上电请求的状态。

2.7.4.2 DBGSTOPCR:调试停止控制寄存器

Base address: DBG = 0x4001_B000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DBGSTOP_CPER	—	—	—	—	—	DBGSTOP_RECCR	DBGSTOP_RPER	—	—	—	—	—	DBGSTOP_LVD2	DBGSTOP_LVD1	DBGSTOP_LVD0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	DBGSTOP_IWDT	Mask bit for IWDT reset/interrupt in the OCD run mode In the OCD break mode, the reset/interrupt is masked and IWDT counter is stopped, regardless of this bit value. 0: Enable IWDT reset/interrupt 1: Mask IWDT reset/interrupt and stop IWDT counter	R/W
1	DBGSTOP_WDT	Mask bit for WDT reset/interrupt in the OCD run mode In the OCD break mode, the reset/interrupt is masked and WDT counter is stopped, regardless of this bit value. 0: Enable WDT reset/interrupt 1: Mask WDT reset/interrupt and stop WDT counter	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
16	DBGSTOP_LVD0	Mask bit for LVD0 reset 0: Enable LVD0 reset 1: Mask LVD0 reset	R/W
17	DBGSTOP_LVD1	Mask bit for LVD1 reset/interrupt 0: Enable LVD1 reset/interrupt 1: Mask LVD1 reset/interrupt	R/W
18	DBGSTOP_LVD2	Mask bit for LVD2 reset/interrupt 0: Enable LVD2 reset/interrupt 1: Mask LVD2 reset/interrupt	R/W
23:19	—	These bits are read as 0. The write value should be 0.	R/W
24	DBGSTOP_RPER	Mask bit for SRAM parity error reset/interrupt 0: Enable SRAM parity error reset/interrupt 1: Mask SRAM parity error reset/interrupt	R/W
25	DBGSTOP_RECCR	Mask bit for SRAM ECC error reset/interrupt 0: Enable SRAM ECC error reset/interrupt 1: Mask SRAM ECC error reset/interrupt	R/W
30:26	—	These bits are read as 0. The write value should be 0.	R/W
31	DBGSTOP_CPER	Mask bit for Cache SRAM parity error reset/interrupt 0: Enable Cache SRAM parity error reset/interrupt 1: Mask Cache SRAM parity error reset/interrupt	R/W

The Debug Stop Control Register (DBGSTOPCR) specifies the functional stop in OCD mode. All bits in the register are regarded as 0 when the MCU is not in OCD mode.

2.7.4.3 DBGREG CoreSight component registers

The DBGREG module provides the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.13 shows the registers. See reference 4. in section 2.14. References for details of each register.

Table 2.13 DBGREG CoreSight component registers (1 of 2)

Name	Address	Access size	R/W	Initial value
PID4	0x4001_BFD0	32 bits	R	0x00000004
PID5	0x4001_BFD4	32 bits	R	0x00000000
PID6	0x4001_BFD8	32 bits	R	0x00000000
PID7	0x4001_BFDC	32 bits	R	0x00000000
PID0	0x4001_BFE0	32 bits	R	0x00000005
PID1	0x4001_BFE4	32 bits	R	0x00000030
PID2	0x4001_BFE8	32 bits	R	0x0000000A
PID3	0x4001_BFEC	32 bits	R	0x00000000
CID0	0x4001_BFF0	32 bits	R	0x0000000D
CID1	0x4001_BFF4	32 bits	R	0x000000F0

Bit	Symbol	Function	R/W
0	DBGSTOP_IWDT	OCD运行模式下IWDT复位中断的屏蔽位 在OCD中断模式下，复位中断被屏蔽，IWDT计数器停止，无论该位值如何。 0：使能IWDT复位中断1：屏蔽IWDT复位中断并停止IWDT计数器	R/W
1	DBGSTOP_WDT	OCD运行模式下WDT复位中断的屏蔽位 在OCD中断模式下，复位中断被屏蔽并且WDT计数器停止，无论该位值如何。 0：使能WDT复位中断1：屏蔽WDT复位中断并停止WDT计数器	R/W
15:2	—	这些位被读取为0。写入值应为0。	R/W
16	DBGSTOP_LVD0	LVD0复位屏蔽位 0：启用LVD0复位1：屏蔽LVD0复位	R/W
17	DBGSTOP_LVD1	LVD1复位中断的屏蔽位 0：使能LVD1复位中断1：屏蔽LVD1复位中断	R/W
18	DBGSTOP_LVD2	LVD2复位中断的屏蔽位 0：使能LVD2复位中断1：屏蔽LVD2复位中断	R/W
23:19	—	这些位被读取为0。写入值应为0。	R/W
24	DBGSTOP_RPER	SRAM奇偶校验错误复位中断的屏蔽位 0：使能SRAM奇偶校验错误复位中断1：屏蔽SRAM奇偶校验错误复位中断	R/W
25	DBGSTOP_RECCR	SRAMECC错误复位中断的屏蔽位 0：使能SRAMECC错误复位中断1：屏蔽SRAMECC错误复位中断	R/W
30:26	—	这些位被读取为0。写入值应为0。	R/W
31	DBGSTOP_CPER	CacheSRAM奇偶校验错误复位中断的屏蔽位 0：使能CacheSRAM奇偶校验错误复位中断1：屏蔽CacheSRAM奇偶校验错误复位中断	R/W

调试停止控制寄存器(DBGSTOPCR)指定OCD模式下的功能停止。当MCU不处于OCD模式时，寄存器中的所有位都被视为0。

2.7.4.3 DBGREGCoreSight组件寄存器

DBGREG模块提供在ArmCoreSight架构中定义的CoreSight组件寄存器。

表2.13显示了寄存器。参见第2.14节中的参考4。每个寄存器的详细信息参考。

Table 2.13 DBGREGCoreSight组件寄存器（1个，共2个）

Name	Address	访问大小	R/W	初始值
PID4	0x4001_BFD0	32 bits	R	0x00000004
PID5	0x4001_BFD4	32 bits	R	0x00000000
PID6	0x4001_BFD8	32 bits	R	0x00000000
PID7	0x4001_BFDC	32 bits	R	0x00000000
PID0	0x4001_BFE0	32 bits	R	0x00000005
PID1	0x4001_BFE4	32 bits	R	0x00000030
PID2	0x4001_BFE8	32 bits	R	0x0000000A
PID3	0x4001_BFEC	32 bits	R	0x00000000
CID0	0x4001_BFF0	32 bits	R	0x0000000D
CID1	0x4001_BFF4	32 bits	R	0x000000F0

Table 2.13 DBGREG CoreSight component registers (2 of 2)

Name	Address	Access size	R/W	Initial value
CID2	0x4001_BFF8	32 bits	R	0x00000005
CID3	0x4001_BFFC	32 bits	R	0x000000B1

2.7.5 OCDREG Module

The OCDREG module are only accessible by the On-Chip Debug (OCD) emulator. OCDREG is implemented as a CoreSight-compliant component.

Table 2.14 lists the OCDREG registers.

Table 2.14 OCDREG registers

Name		DAP port	Address	Access size	R/W
MCU Status Register	MCUSTAT	Port 1	0x8000_0400	32 bits	R
MCU Control Register	MCUCTRL	Port 1	0x8000_0410	32 bits	R/W

Note: OCDREG is located in the dedicated OCD address space. This address map is independent from the system address map.

2.7.5.1 MCUSTAT : MCU Status Register

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x400

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	SECDBG	DBGFUNCEN	BOOTMD	—	—	—	—	—	—	—	—	CPUSTOPCLK	CPUSLEEP	—
Value after reset:	0	0	1/0*1	1/0*1	1/0*1	0	0	1	0	0	0	0	0	1/0*1	1/0*1	0

Bit	Symbol	Function	R/W
0	—	These bits are read as 0.	R
1	CPUSLEEP	Sleep mode status This bit is unpredictable when the MCU is in Software Standby mode, Snooze mode, or Deep Software Standby mode. 0: CPU is not in Sleep mode 1: CPU in Sleep mode	R
2	CPUSTOPCLK	CPU clock status This bit is unpredictable when the MCU is in Deep Software Standby mode. 0: CPU clock is not stopped. 1: CPU clock is stopped.	R
7:3	—	These bits are read as 0.	R
8	—	These bits are read as 1.	R
10:9	—	These bits are read as 0.	R
11	BOOTMD	Boot mode status 0: Device is not in Boot mode 1: Device is in Boot mode	R
12	DBGFUNCEN	Debugger status 0: Debugger connection is not available 1: Debugger function is enabled	R

Table 2.13 DBGREGCoreSight组件寄存器（2个中的2个）

Name	Address	访问大小	R/W	初始值
CID2	0x4001_BFF8	32 bits	R	0x00000005
CID3	0x4001_BFFC	32 bits	R	0x000000B1

2.7.5 OCDREG Module

OCDREG模块只能由片上调试(OCD)仿真器访问。OCDREG被实现为CoreSight-compliant component.

表2.14列出了OCDREG寄存器。

Table 2.14 OCDREG registers

Name		端口	Address	访问大小	R/W
MCU状态寄存器	MCUSTAT	Port 1	0x8000_0400	32 bits	R
MCU控制寄存器	MCUCTRL	Port 1	0x8000_0410	32 bits	R/W

Note: OCDREG位于专用的OCD地址空间中。该地址映射独立于系统地址映射。

2.7.5.1 MCUSTAT：MCU状态寄存器

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x400

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	SECDBG	DBGFUNCEN	BOOTMD	—	—	—	—	—	—	—	—	CPUSTOPCLK	CPUSLEEP	—
重置后的值:	0	0	1/0*1	1/0*1	1/0*1	0	0	1	0	0	0	0	0	1/0*1	1/0*1	0

Bit	Symbol	Function	R/W
0	—	这些位读为0。	R
1	CPUSLEEP	睡眠模式状态 当MCU处于软件待机模式、贪睡模式或深度软件待机模式。 0：CPU不处于休眠模式1：CPU处于休眠模式	R
2	CPUSTOPCLK	CPU时钟状态 当MCU处于深度软件待机模式时，该位是不可预测的。 0：CPU时钟不停止。1：CPU时钟停止。	R
7:3	—	这些位读为0。	R
8	—	这些位读为1。	R
10:9	—	这些位读为0。	R
11	BOOTMD	引导模式状态 0：设备未处于引导模式1：设备处于引导模式	R
12	DBGFUNCEN	调试器状态 0：调试器连接不可用1：调试器功能启用	R

Bit	Symbol	Function	R/W
13	SECDBG	Secure Debug status 0: Secure Debug is not available 1: Secure Debug is available	R
31:14	—	These bits are read as 0.	R

Note 1. Depends on the MCU status.

2.7.5.2 MCUCTRL : MCU Control Register

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x410

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUWAIT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	These bits are read as 0. The write value should be 0.	R/W
8	DBIRQ*2	Debug Interrupt Request Writing 1 to the bit wakes up the MCU from low power mode. The condition can be cleared by writing 0 to the DBIRQ bit. 0: Debug interrupt not requested 1: Debug interrupt requested	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	CPUWAIT*2	CPU Wait Setting Write 1 to assert CPUWAIT, write 0 to dessert CPUWAIT*1. 0: Clear CPUWAIT to low 1: Set CPUWAIT to high	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. CPUWAIT is used to prevent the processor from executing code immediately after reset.
Note 2. Access (R/W) to bit is valid only when Debug Level is DBG1 or DBG2.

2.7.5.3 OCDREG CoreSight component registers

The OCDREG module provides the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.15 shows the registers. See reference 4. in section 2.14. References for details of each register.

Table 2.15 OCDREG CoreSight component registers (1 of 2)

Name	Address	Access size	R/W	Initial value
PID4	0x8000_0FD0	32 bits	R	0x00000004
PID5	0x8000_0FD4	32 bits	R	0x00000000
PID6	0x8000_0FD8	32 bits	R	0x00000000
PID7	0x8000_0FDC	32 bits	R	0x00000000
PID0	0x8000_0FE0	32 bits	R	0x00000004
PID1	0x8000_0FE4	32 bits	R	0x00000030
PID2	0x8000_0FE8	32 bits	R	0x0000000A
PID3	0x8000_0FEC	32 bits	R	0x00000000

Bit	Symbol	Function	R/W
13	SECDBG	安全调试状态 0：安全调试不可用1：安全调试可用	R
31:14	—	这些位读为0。	R

注1.取决于MCU状态。

2.7.5.2 MCUCTRL:MCU控制寄存器

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x410

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUWAIT
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	这些位被读取为0。写入值应为0。	R/W
8	DBIRQ*2	调试中断请求 向该位写入1将MCU从低功耗模式唤醒。可以通过将0写入DBIRQ位来清除该条件。 0：未请求调试中断1：请求调试中断	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
16	CPUWAIT*2	CPU等待设置 写1来断言CPUWAIT，写0到甜点CPUWAIT*1。 0：清除CPUWAIT为低1：设置CPUWAIT为高	R/W
31:17	—	这些位被读取为0。写入值应为0。	R/W

注1.CPUWAIT用于防止处理器在复位后立即执行代码。
注2.只有当DebugLevel为DBG1或DBG2时，对位的访问(RW)才有效。

2.7.5.3 OCDREGCoreSight组件寄存器

OCDREG模块提供在ArmCoreSight架构中定义的CoreSight组件寄存器。

表2.15显示了寄存器。参见第2.14节中的参考4。每个寄存器的详细信息参考。

Table 2.15 OCDREGCoreSight组件寄存器（1个，共2个）

Name	Address	访问大小	R/W	初始值
PID4	0x8000_0FD0	32 bits	R	0x00000004
PID5	0x8000_0FD4	32 bits	R	0x00000000
PID6	0x8000_0FD8	32 bits	R	0x00000000
PID7	0x8000_0FDC	32 bits	R	0x00000000
PID0	0x8000_0FE0	32 bits	R	0x00000004
PID1	0x8000_0FE4	32 bits	R	0x00000030
PID2	0x8000_0FE8	32 bits	R	0x0000000A
PID3	0x8000_0FEC	32 bits	R	0x00000000

Table 2.15 OCDREG CoreSight component registers (2 of 2)

Name	Address	Access size	R/W	Initial value
CID0	0x8000_0FF0	32 bits	R	0x0000000D
CID1	0x8000_0FF4	32 bits	R	0x000000F0
CID2	0x8000_0FF8	32 bits	R	0x00000005
CID3	0x8000_0FFC	32 bits	R	0x000000B1

2.7.6 CPUDSAR : CPU Debug Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x1B0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUDSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	CPUDSA0	CPU Debug Security Attribution 0 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and non-secure read access are allowed. Non-secure write access is denied, and no TrustZone access error is generated.

Note: This register is write-protected by PRCR register.

When Debug level of the MCU is DBG2, by guarding entire EPPB bus, the non-secure access from CPU to debug related components is completely controlled by the current value of the CPUDSA0 bit. Since this bit is modifiable only when CPU is in secure state, user must be aware of the CPUDSAR register before using Coresight debug components.

CPUDSA0 bit (CPU Debug Security Attribution 0)

Security attributes of register for accessing the debug component of the CPU.

0: Debug component can only be accessed with secure access.

1: There is no restriction on accessing the debug component.

2.7.7 Processing on Error response generated by CPU access

In addition to the specific-error detection specification of the Arm Cortex-M33 processor, this MCU also provides additional error information which is described in section 13, Buses.

This section describes how to handle the additional error information with no conflict to that of the Arm Cortex-M33 processor.

Table 2.16 shows error detection modules, which are also described in section 13, Buses. These error detection modules not only provide error information on the bus module, but also notify the processor to trigger the exception handler.

Table 2.16 (1 of 2)

	NMI/RESET request	Interrupt	Bus error status register	Error address register Error RW register
Slave TZF	NMISR.TZFST	Bus Fault*1 (Hard Fault)	BUS.BUSnERRSTAT.STERRSTAT	BUS.BTZFnERRADD BUS.BTZFnERRRW

Table 2.15 OCDREGCoreSight组件寄存器（2个中的2个）

Name	Address	访问大小	R/W	初始值
CID0	0x8000_0FF0	32 bits	R	0x0000000D
CID1	0x8000_0FF4	32 bits	R	0x000000F0
CID2	0x8000_0FF8	32 bits	R	0x00000005
CID3	0x8000_0FFC	32 bits	R	0x000000B1

2.7.6 CPUDSAR:CPU调试安全属性寄存器

Base address: CPSCU = 0x4000_8000

Offset address: 0x1B0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUDSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	CPUDSA0	CPU调试安全属性0 0: Secure 1: Non-secure	R/W
31:1	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问。拒绝非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

当MCU的Debug级别为DBG2时，通过保护整个EPPB总线，CPU对调试相关组件的非安全访问完全由CPUDSA0位的当前值控制。由于该位仅在CPU处于安全状态时才可修改，因此用户在使用Coresight调试组件之前必须了解CPUDSAR寄存器。

CPUDSA0位（CPU调试安全属性0）

用于访问CPU调试组件的寄存器的安全属性。

0：只能通过安全访问访问调试组件。

1：对调试组件的访问没有限制。

2.7.7 CPU访问产生的错误响应的处理

除了ArmCortex-M33处理器的特定错误检测规范外，该MCU还提供第13节“总线”中描述的附加错误信息。

本节介绍如何处理与ArmCortex-M33处理器不冲突的附加错误信息。

表2.16显示了错误检测模块，这些模块也在第13节“总线”中进行了描述。这些错误检测模块不仅提供总线模块上的错误信息，还通知处理器触发异常处理程序。

Table 2.16 (1 of 2)

	NMI/RESET request	Interrupt	总线错误状态寄存器	错误地址寄存器 错误RW寄存器
Slave TZF	NMISR.TZFST	总线故障*1 (Hard Fault)	BUS.BUSnERRSTAT.STERRSTAT	BUS.BTZFnERRADD BUS.BTZFnERRRW

Table 2.16 (2 of 2)

	NMI/RESET request	Interrupt	Bus error status register	Error address register Error RW register
Slave bus error	—	Bus Fault	BUS.BUSnERRSTAT.SLERRSTAT	BUS.BUSnERRADD BUS.BUSnERRRW
Illegal address access error	—	Bus Fault	BUS.BUSnERRSTAT.ILERRSTAT	BUS.BUSnERRADD BUS.BUSnERRRW

Note 1. A Bus Fault can be treated as HardFault. *ARM® Cortex®-M33 Device Generic User Guide* in the References section 2.14. References

To prevent unexpected operation, when handling the exception, additional operation should be added into exception routing.

BusFault when occurred by error detected as shown in Table 2.16:

- See section 13, Buses for the error information in the corresponding register
- Clear the data in cache for the error address
- Clear the Error Status register in the bus module
- Service exception handling with Arm-guided operation

For a Bus Fault that is not detected in the Renesas-specific error detection module (occurred inside the Arm Cortex-M33 core), see the *ARM® Cortex®-M33 Device Generic User Guide* to handle this case.

In the system bus specification, there is a specific case for Slave TrustZone Filter, that is, if an error is selected to generate an NMI, then before the processor handles the Bus Fault exception, NMI with higher priority takes the exception first. Therefore, use the BusFault handler and not NMI handler to handle this error. In other words, the NMI status should be cleared but the error status bit should not be cleared to ensure that BusFault captures all the error information.

Figure 2.4 and Figure 2.5 show the recommended flows for NMI handler and BusFault handler for the errors described in Table 2.16.

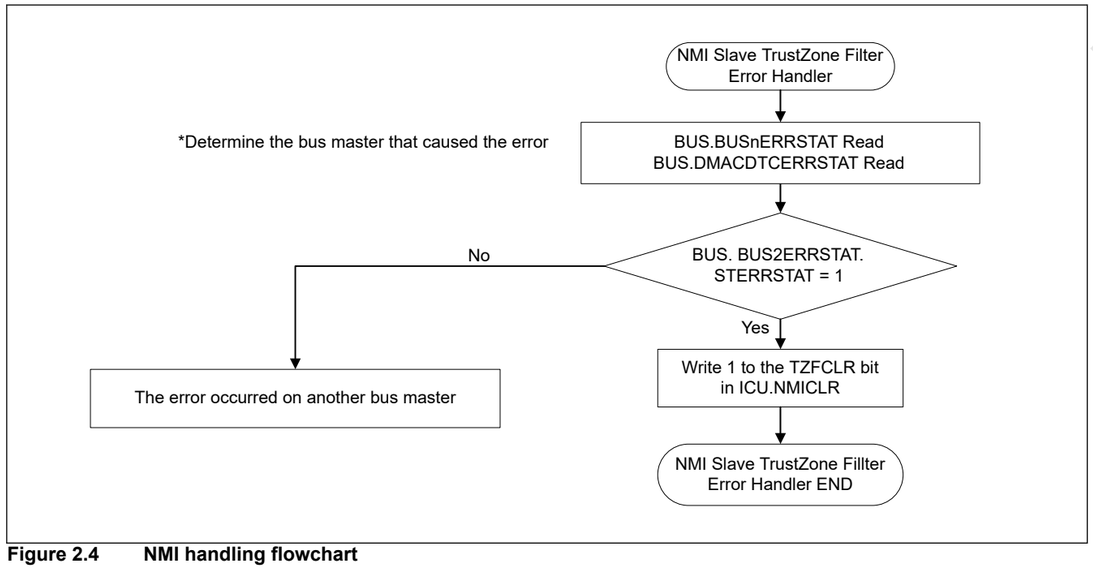


Figure 2.4 NMI handling flowchart

Table 2.16 (2 of 2)

	NMI/RESET request	Interrupt	总线错误状态寄存器	错误地址寄存器 错误RW寄存器
从站总线错误	—	总线故障	BUS.BUSnERRSTAT.SLERRSTAT	BUS.BUSnERRADD BUS.BUSnERRRW
非法地址访问错误	—	总线故障	BUS.BUSnERRSTAT.ILERRSTAT	BUS.BUSnERRADD BUS.BUSnERRRW

注1.总线故障可被视为硬故障。参考第2.14节中的ARM®Cortex®-M33设备通用用户指南。
References

为防止意外操作，在处理异常时，应在异常路由中增加额外的操作。

检测到错误发生时的BusFault，如表2.16所示：

- ●相应寄存器中的错误信息见第13节，总线
- ●清除缓存中错误地址的数据
- ●清除总线模块中的错误状态寄存器
- ●服务异常处理，手臂引导操作

对于未在Renesas特定错误检测模块中检测到的总线故障（发生在ArmCortex-M33内核中），请参阅ARM®Cortex®-M33DeviceGenericUserGuide来处理这种情况。

在系统总线规范中，SlaveTrustZoneFilter有一个具体的案例，即如果选择了错误产生NMI，那么在处理器处理BusFault异常之前，优先级较高的NMI先处理该异常。因此，使用BusFault处理程序而不是NMI处理程序来处理此错误。换言之，应清除NMI状态但不应清除错误状态位，以确保BusFault捕获所有错误信息。

图2.4和图2.5显示了NMI处理程序和BusFault处理程序的推荐流程，用于处理中描述的错误
Table 2.16.

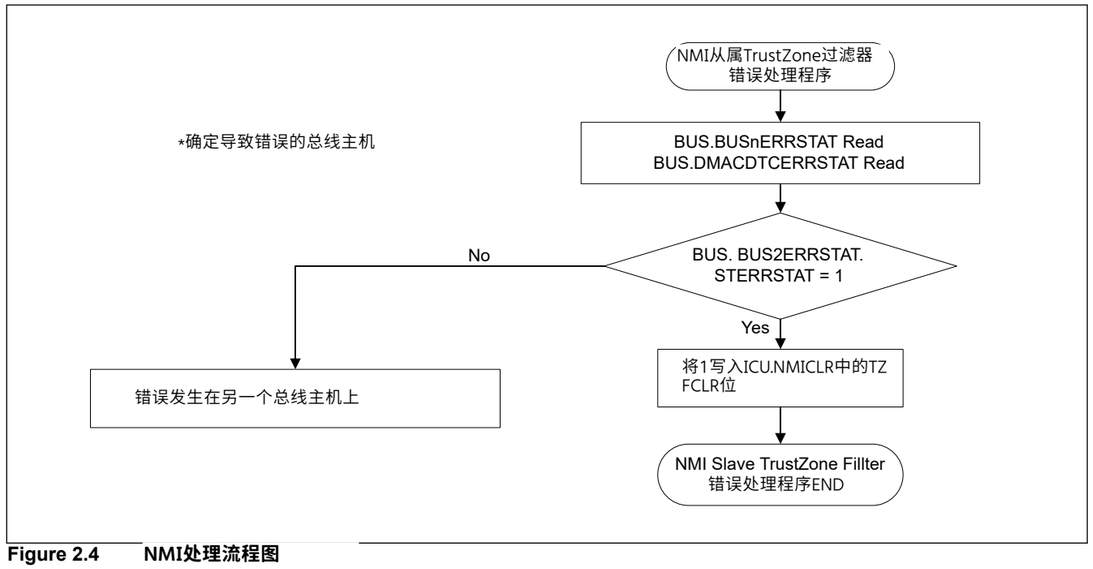


Figure 2.4 NMI处理流程图

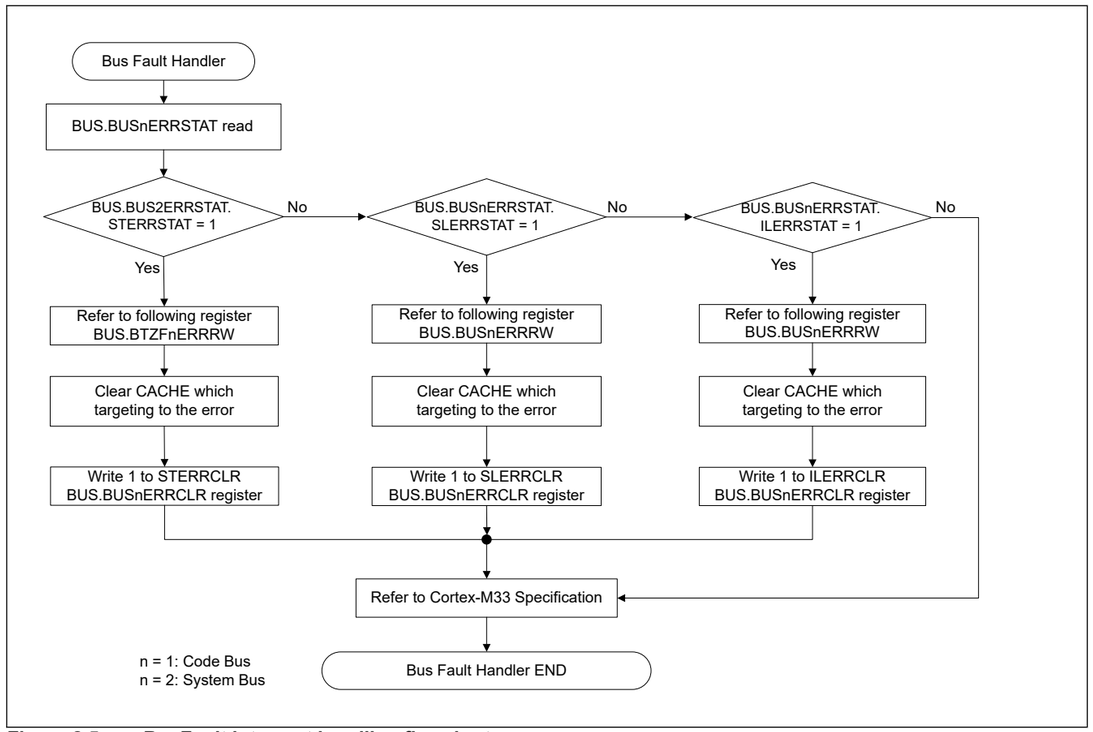


Figure 2.5 BusFault interrupt handling flowchart

2.8 CoreSight Cross Trigger Interface (CTI)

As shown in Figure 2.6, the input and output of a Cross Trigger Interface (CTI) interact with each other through four CTM channels. Input of a CTI can be used to trigger the output of another CTI using the four CTM channels.

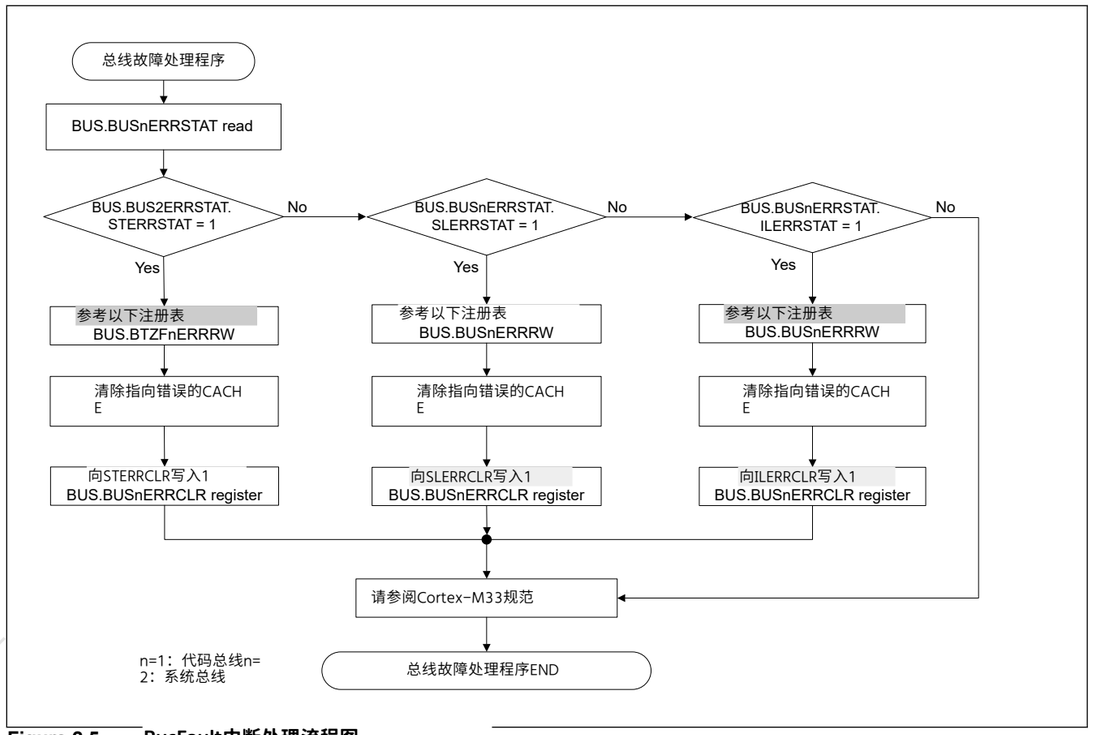


Figure 2.5 BusFault中断处理流程图

2.8 CoreSight交叉触发接口(CTI)

如图2.6所示，交叉触发接口（CTI）的输入和输出通过四个CTM通道相互交互。一个CTI的输入可用于使用四个CTM通道触发另一个CTI的输出。

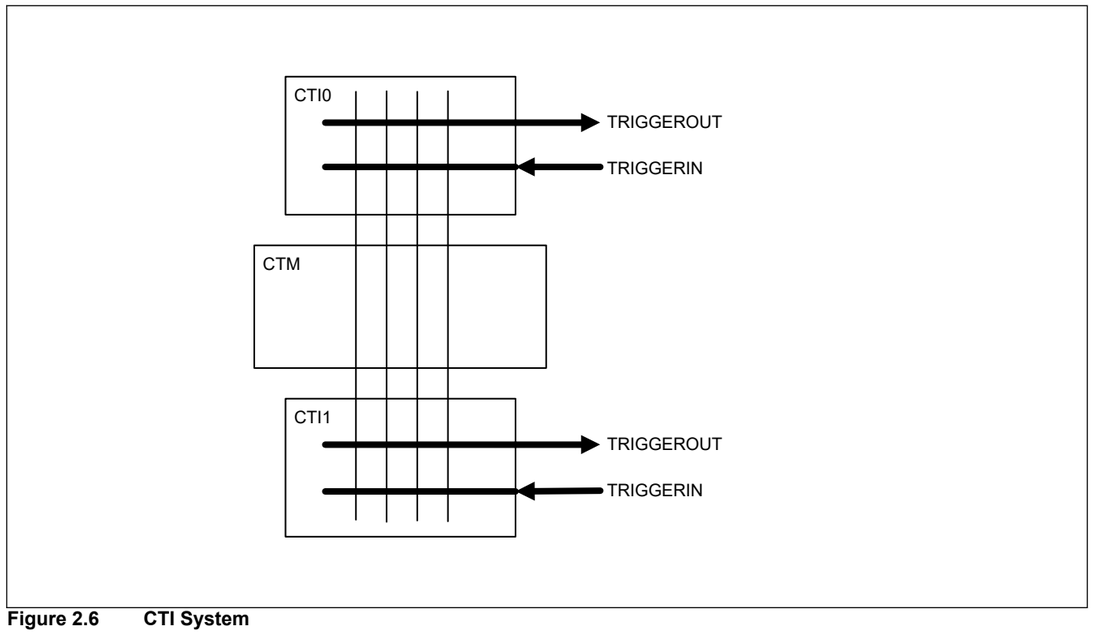


Figure 2.6 CTI System

Debug Interrupt Request (DBGIRQ) is controlled by MCUCTRL register in OCDREG module.

Table 2.17 CTI Trigger signals

Number of CTI channel	CTITRIGIN		CTITRIGOUT	
CTI0 (Debug common)	0	ACQCOMP	0	—
	1	FULL	1	—
	2	DBIRQ	2	ETB FLUSHIN
	3	—	3	ETB TRIGIN
	4	—	4	—
	5	—	5	—
	6	—	6	—
	7	—	7	—
CTI1 (CPU)	0	Processor Halted	0	Processor debug request
	1	DWT Comparator Output 0	1	Processor Restart
	2	DWT Comparator Output 1	2	CTIIRQ[0] (Connected to IRQ96)
	3	DWT Comparator Output 2	3	CTIIRQ[1] (Connected to IRQ97)
	4	ETM Event Output 0	4	ETM Event Input 0
	5	ETM Event Output 1	5	ETM Event Input 1
	6	—	6	ETM Event Input 2
	7	—	7	ETM Event Input 3

2.9 CoreSight ATB Funnel

There is one CoreSight ATB funnel in the MCU. The funnel has two ATB slaves and one ATB master, and it selects the debug trace source from ETM and ITM to ETB. Figure 2.7 shows the CoreSight ATB connection in the MCU.

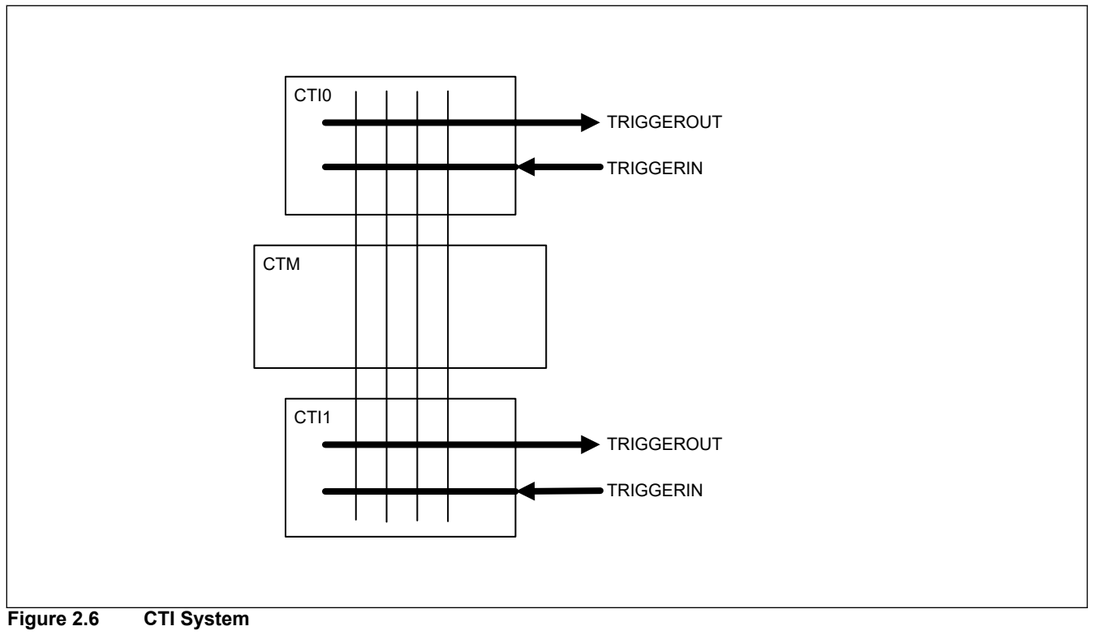


Figure 2.6 CTI System

调试中断请求(DBGIRQ)由OCDREG模块中的MCUCTRL寄存器控制。

Table 2.17 CTI触发信号

CTI通道数	CTITRIGIN		CTITRIGOUT	
CTI0 (Debug common)	0	ACQCOMP	0	—
	1	FULL	1	—
	2	DBIRQ	2	ETB FLUSHIN
	3	—	3	ETB TRIGIN
	4	—	4	—
	5	—	5	—
	6	—	6	—
	7	—	7	—
CTI1 (CPU)	0	处理器停止	0	处理器调试请求
	1	DWT比较器输出0	1	处理器重启
	2	DWT比较器输出1	2	CTIIRQ[0] (Connected to IRQ96)
	3	DWT比较器输出2	3	CTIIRQ[1] (Connected to IRQ97)
	4	ETM事件输出0	4	ETM事件输入0
	5	ETM事件输出1	5	ETM事件输入1
	6	—	6	ETM事件输入2
	7	—	7	ETM事件输入3

2.9 CoreSight ATB Funnel

MCU中有一个CoreSightATB漏斗。漏斗有两个ATB从站和一个ATB主站，它选择从ETM和ITM到ETB的调试跟踪源。图2.7显示了MCU中的CoreSightATB连接。

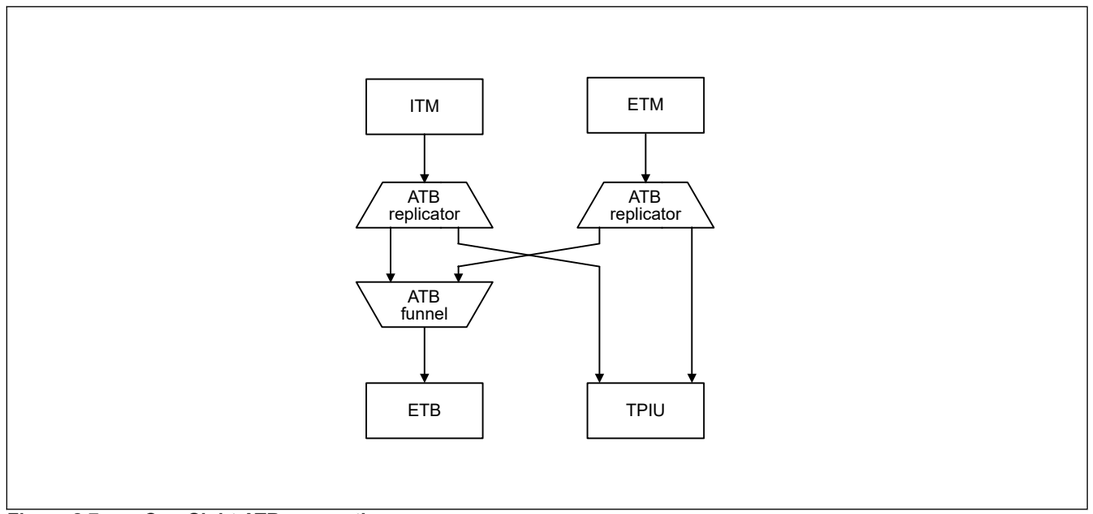


Figure 2.7 CoreSight ATB connection

Table 2.18 shows the ATB slave connection for the funnel.

Table 2.18 ATB slave connection

ATB slave number	Connected trace source
#0	ITM
#1	ETM

See reference 4. in section 2.14. References for details of the ATB and funnel.

2.10 Break Point Unit

The MCU has Break Point Unit. See BreakPoint unit chapter of reference 1. in section 2.14. References for details about register description of this module.

2.11 CoreSight Time Stamp Generator

A CoreSight Time Stamp Generator provides a CPU clock-based timestamp to ITM and ETM.The timestamp is generated by a 64-bit counter. See reference 4. in section 2.14. References for details.

2.12 SysTick Timer

The MCU has SysTick timer that provides two 24-bit down counters, non-secure and secure counters. The timer can select SysTick timer clock (SYSTICCLK) or System clock (ICLK).

See section 8, Clock Generation Circuit and reference 1. in section 2.14. References for details.

Note: SysTick timer counter operation is enabled by signal synchronized with CPU clock. Therefore, the counter might not operate correctly if the CPU clock is slower than the SysTick timer clock. In other words, clock setting must satisfy the following: CPU clock ≥ Systick clock (LOCO: 32.768 kHz).

2.13 OCD Emulator Connection

In this product, the MCU confirms the access permission for Non-secure debug and Non-secure chip resources by checking Debug level is DBG1 or higher. For full access permission for debug and chip resources, Secure debug level DBG2 is required.

Figure 2.8 shows a block diagram of SWD authentication mechanism.

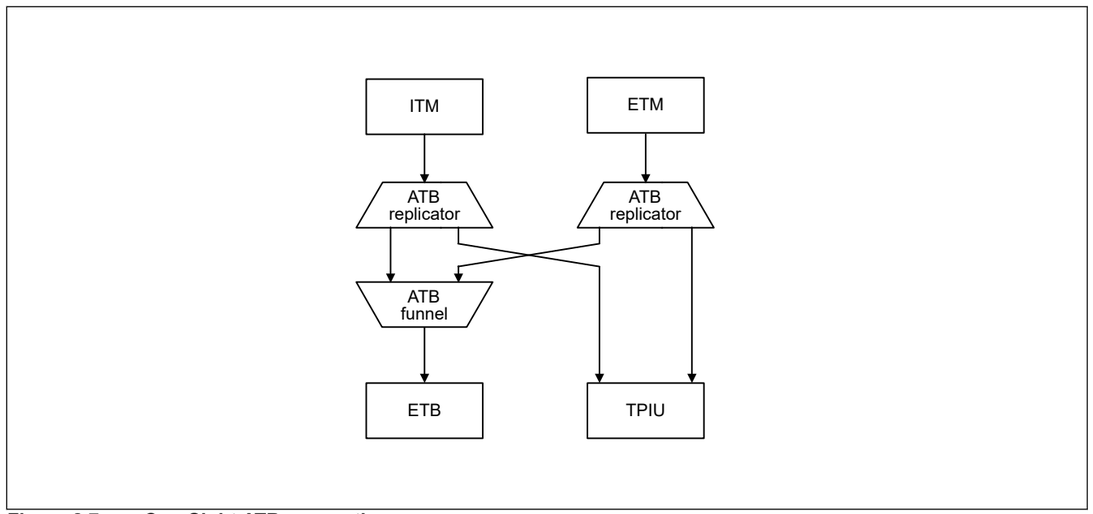


Figure 2.7 CoreSight ATB connection

表2.18显示了漏斗的ATB从属连接。

Table 2.18 ATB从机连接

ATB从机号	连接的跟踪源
#0	ITM
#1	ETM

参见第2.14节中的参考4。有关ATB和漏斗详细信息的参考资料。

2.10 断点单元

MCU有断点单元。请参阅第2.14节中参考文献1.的断点单元章节。关于该模块的寄存器描述的详细信息参考。

2.11 CoreSight时间戳生成器

CoreSight时间戳生成器为ITM和ETM提供基于CPU时钟的时间戳。时间戳由64位计数器生成。参见第2.14节中的参考4。详情参考。

2.12 SysTick Timer

MCU具有SysTick定时器，提供两个24位递减计数器、非安全计数器和安全计数器。定时器可以选择SysTick定时器时钟(SYSTICCLK)或系统时钟(ICLK)。

请参见第8节，时钟生成电路和第2.14节中的参考1。详情参考。

Note: SysTick定时器计数器操作由与CPU时钟同步的信号启用。因此，如果CPU时钟比SysTick定时器时钟慢，计数器可能无法正确运行。换言之，时钟设置必须满足以下条件：CPU时钟≥Systick时钟（LOCO：32.768kHz）。

2.13 OCD模拟器连接

本产品中，MCU通过勾选确认非安全调试和非安全芯片资源的访问权限
调试级别为DBG1或更高。对于调试和芯片资源的完全访问权限，需要安全调试级别DBG2。

图2.8显示了SWD认证机制的框图。

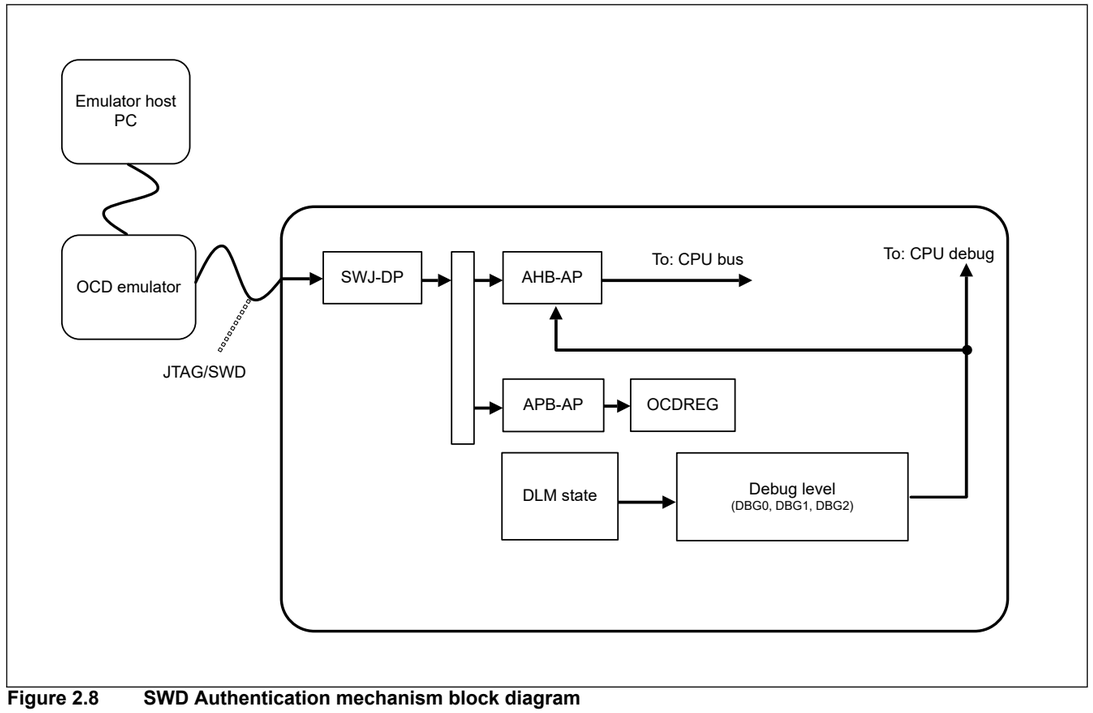


Figure 2.8 SWD Authentication mechanism block diagram

Three levels of debug capability are available, DBG0, DBG1, and DBG2, which correspond to the Device Level Management (DLM) states. When debug level is DBG0, access to debug components and system bus from OCD emulator is not permitted. When debug level is DBG1 or DBG2, the corresponding non-secure or secure debug components and system bus can be accessed from the OCD emulator. See Table 2.5 for more information about debug levels.

2.13.1 DBGEN

After the OCD emulator gets access permission, the OCD emulator must set the DBGEN bit in the System Control OCD Control Register (SYOCDCR). In addition, the OCD emulator must clear the DBGEN bit before disconnecting it. See section 10, Low Power Modes for details.

2.13.2 Restrictions on Connecting an OCD emulator

This section describes the restrictions on emulator access.

2.13.2.1 Starting connection while in low power mode

When starting a JTAG/SWD connection from an OCD emulator, the MCU must be in Normal or Sleep mode. If the MCU is in Software Standby, Snooze, or Deep Software Standby mode, the OCD emulator can cause the MCU to hang.

2.13.2.2 Changing low power mode while in OCD mode

When the MCU is in OCD mode, the low power mode can be changed. However, system bus access from AHB-AP is prohibited in Software Standby, Snooze or Deep Software Standby mode. Only SWJ-DP, APB-AP, and OCDREG can be accessed from the OCD emulator in these modes. Table 2.19 shows the restrictions.

Table 2.19 Restrictions by mode (1 of 2)

Active mode	Start OCD emulator connection	Change low power mode	Access AHB-AP and system bus	Access APB-AP and OCDREG
Normal	Yes	Yes	Yes	Yes

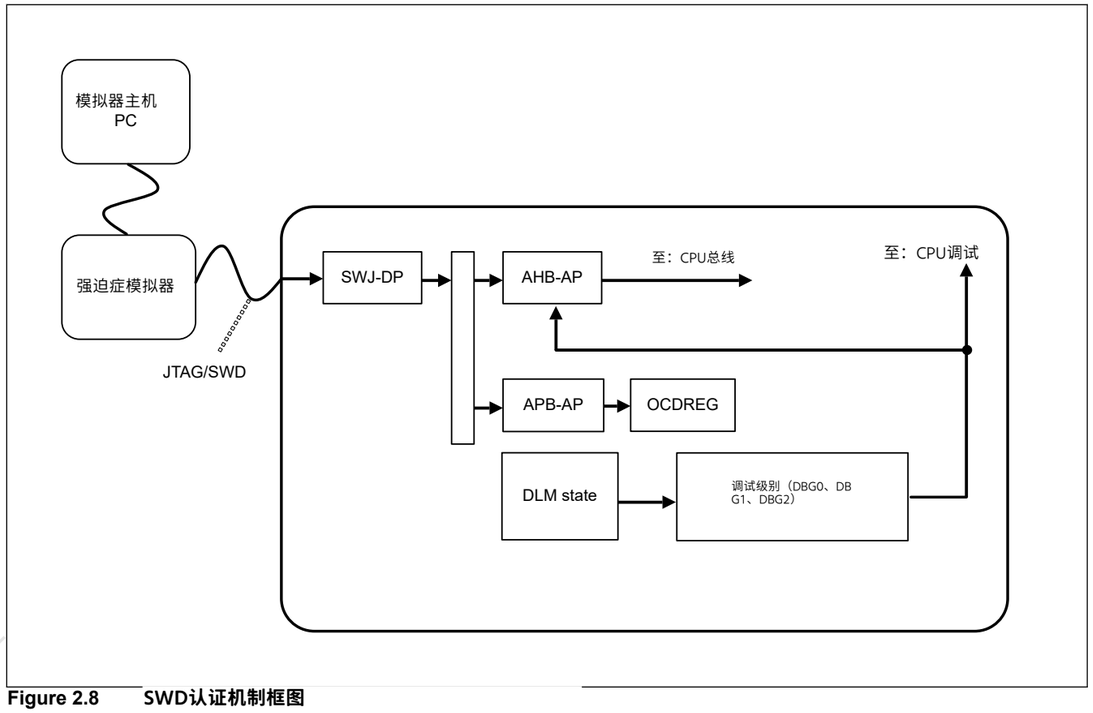


Figure 2.8 SWD认证机制框图

提供三个级别的调试能力，DBG0、DBG1和DBG2，它们对应于DeviceLevel管理(DLM)状态。当调试级别为DBG0时，不允许从OCD仿真器访问调试组件和系统总线。当调试级别为DBG1或DBG2时，可以从OCD仿真器访问相应的非安全或安全调试组件和系统总线。有关调试级别的更多信息，请参见表2.5。

2.13.1 DBGEN

OCD模拟器获得访问权限后，OCD模拟器必须设置SystemControlOCD中的DBGEN位控制寄存器(SYOCDCR)。此外，OCD仿真器必须在断开连接之前清除DBGEN位。有关详细信息，请参见第10节，低功耗模式。

2.13.2 连接强迫症模拟器的限制

本节介绍对仿真器访问的限制。

2.13.2.1 在低功耗模式下开始连接

从OCD仿真器启动JTAGSWD连接时，MCU必须处于正常或睡眠模式。如果MCU处于软件待机、贪睡或深度软件待机模式，OCD仿真器可能会导致MCU挂起。

2.13.2.2 在OCD模式下更改低功耗模式

当MCU处于OCD模式时，可以更改低功耗模式。但是，在软件待机、贪睡或深度软件待机模式下，禁止从AHB-AP访问系统总线。在这些模式下，只能从OCD仿真器访问SWJ-DP、APB-AP和OCDREG。表2.19显示了这些限制。

Table 2.19 模式限制(1of2)

主动模式	启动强迫症模拟器连接	更改低功耗模式	访问AHB-AP和系统总线	访问APB-AP和OCDREG
Normal	Yes	Yes	Yes	Yes

Table 2.19 Restrictions by mode (2 of 2)

Active mode	Start OCD emulator connection	Change low power mode	Access AHB-AP and system bus	Access APB-AP and OCDREG
Sleep	Yes	Yes	Yes	Yes
Software Standby	No	Yes	No	Yes
Snooze	No	Yes	No	Yes
Deep Software Standby	No	Yes	No	Yes

If system bus access is required in Software Standby, Snooze, or Deep Software Standby mode, set the MCUCTRL.DBIRQ bit in OCDREG to wake up the MCU from the low power modes. Simultaneously, by asserting the MCUCTRL.DBIRQ bit in OCDREG, the OCD emulator can wake up the MCU without starting CPU execution by using a CPU break.

2.13.2.3 Connecting sequence and JTAG/SWD authentication

1. Connect the OCD debugger to the MCU through the JTAG or SWD interface.
2. Set up SWJ-DP to access DAP bus.
   In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJDP.
   Control Status Register, and then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set the APB-AP to access OCDREG. This APB-AP is connected to DAP bus port 1.
4. Set MCUCTRL.CPUWAIT = 1.
5. Confirm the debug capability of device by reading MCUSTAT:
   - If Debug function is prohibited, this device is not able to debug.
   - If Debug function is enabled and secure debug is not available, only non-secure debug is available.
   - If Debug function is enabled and secure debug is available, full debug functions are available.

   If Debug function is available, set debug-related register then clear MCUCTRL.CPUWAIT = 0.
6. Set up the AHB-AP to access the system address space. The AHB-AP is connected to DAP bus port 0.
7. Set SYOCDCR.DBGEN to 1.
8. Start accessing the CPU debug resources using the AHB-AP.

Note: Debug level is determined by the current DLM state of product.

2.14 References

1. *ARM®v8-M Architecture Reference Manual* (ARM DDI 0553B.a)
2. *ARM® Cortex®-M33 Processor Technical Reference Manual* (ARM 100230)
3. *ARM® Cortex®-M33 Device Generic User Guide* (ARM 100235)
4. *ARM® CoreSight™ SoC-400 Technical Reference Manual* (ARM DDI 0480G)
5. *ARM® CoreSight™ Architecture Specification* (ARM IHI 0029E)

Table 2.19 模式限制(2of2)

主动模式	启动强迫症模拟器连接	更改低功耗模式	访问AHB-AP和系统总线	访问APB-AP和OCDREG
Sleep	Yes	Yes	Yes	Yes
软件待机	No	Yes	No	Yes
Snooze	No	Yes	No	Yes
深度软件待机	No	Yes	No	Yes

如果在软件待机、贪睡或深度软件待机模式下需要系统总线访问，则设置OCDREG中的MCUCTRL.DBIRQ位以将MCU从低功耗模式中唤醒。同时，通过置位OCDREG中的MCUCTRL.DBIRQ位，OCD仿真器可以在不使用CPU中断启动CPU执行的情况下唤醒MCU。

2.13.2.3 连接顺序和JTAGSWD认证

1.通过JTAG或SWD接口将OCD调试器连接到MCU。

2.设置SWJ-DP访问DAP总线。
在设置中，OCD仿真器必须在SWJDP中声明CDBGPWRUPREQ。
控制状态寄存器，然后等待同一寄存器中的CSDBGPWRUPACK被断言。

3.将APB-AP设置为访问OCDREG。此APB-AP连接到DAP总线端口1。

4. Set MCUCTRL.CPUWAIT = 1.

5.通过读取MCUSTAT确认设备的调试能力：
●如果Debug功能被禁止，则本设备无法调试。
●如果启用了Debug功能且没有安全调试，则只能进行非安全调试。
●如果启用了Debug功能并且可以使用安全调试，则可以使用完整的调试功能。

如果Debug功能可用，设置调试相关寄存器然后清除MCUCTRL.CPUWAIT=0。

6.设置AHB-AP访问系统地址空间。AHB-AP连接到DAP总线端口0。

7.将SOOCDCR.DBGEN设置为1。

8.开始使用AHB-AP访问CPU调试资源。

Note: 调试级别由产品的当前DLM状态决定。

2.14 References

1.ARM®v8-M架构参考手册（ARMDDI0553B.a）

2.ARM®Cortex®-M33处理器技术参考手册（ARM100230）

3.ARM®Cortex®-M33设备通用用户指南(ARM100235)

4.ARM®CoreSight SoC-400技术参考手册（ARMDDI0480G）

5.ARM®CoreSight 架构规范（ARMIHI0029E）

3. Operating Modes

3.1 Overview

Table 3.1 shows the selection of operating modes by the mode-setting pin. For details, see section 3.2. Details of Operating Modes. Operation starts with the on-chip flash memory enabled, regardless of the mode in which operation started.

Table 3.1 Selection of operating modes by the mode-setting pin

Mode-setting pin (MD)	Operating mode	On-chip Flash
1	Single-chip mode	Enable
0	SCI boot mode	Enable

3.2 Details of Operating Modes

3.2.1 Single-Chip Mode

In single-chip mode, all I/O pins are available for use as input or output port, inputs or outputs for peripheral functions, or as interrupt inputs.

When a reset is released while the MD pin is high, the MCU starts in single-chip mode and the on-chip flash is enabled.

3.2.2 SCI Boot Mode

In this mode, the on-chip flash memory programming routine (SCI boot program), stored in the boot area within the MCU, is used. The on-chip flash, including code flash memory and data flash memory, can be modified from outside the MCU by using a universal asynchronous receiver/transmitter (UART) SCI. For details, see section 43, Flash Memory. The MCU starts in SCI boot mode if the MD pin is held low on release from the reset state.

3.3 Operating Modes Transitions

3.3.1 Operating Mode Transitions as Determined by the Mode-Setting Pin

Figure 3.1 shows operating mode transitions determined by the MD pin settings.

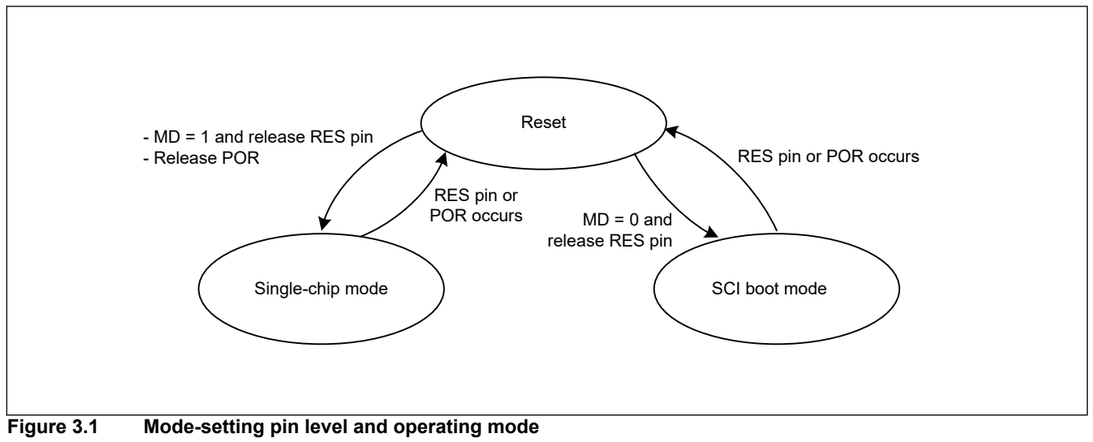


Figure 3.1 Mode-setting pin level and operating mode

3. 操作模式

3.1 Overview

表3.1显示了通过模式设置引脚选择的工作模式。有关详细信息，请参阅第3.2节。经营详情模式。无论操作以何种模式开始，操作都会从启用片上闪存开始。

Table 3.1 通过模式设置引脚选择工作模式

Mode-setting pin (MD)	操作模式	On-chip Flash
1	Single-chip mode	Enable
0	SCI开机模式	Enable

3.2 操作模式的详细信息

3.2.1 Single-Chip Mode

在单片机模式下，所有IO引脚都可用作输入或输出端口、外围功能的输入或输出，或用作中断输入。

当MD引脚为高电平时释放复位时，MCU以单芯片模式启动，并启用片上闪存。

3.2.2 SCI启动模式

在这种模式下，使用存储在MCU引导区域中的片上闪存编程例程（SCI引导程序）。片上闪存，包括代码闪存和数据闪存，可以通过使用通用异步接收发送器(UART)SCI从MCU外部进行修改。有关详细信息，请参阅第43节，闪存。如果MD引脚在从复位状态释放时保持低电平，则MCU以SCI启动模式启动。

3.3 操作模式转换

3.3.1 由模式设置引脚确定的操作模式转换

图3.1显示了由MD引脚设置确定的操作模式转换。

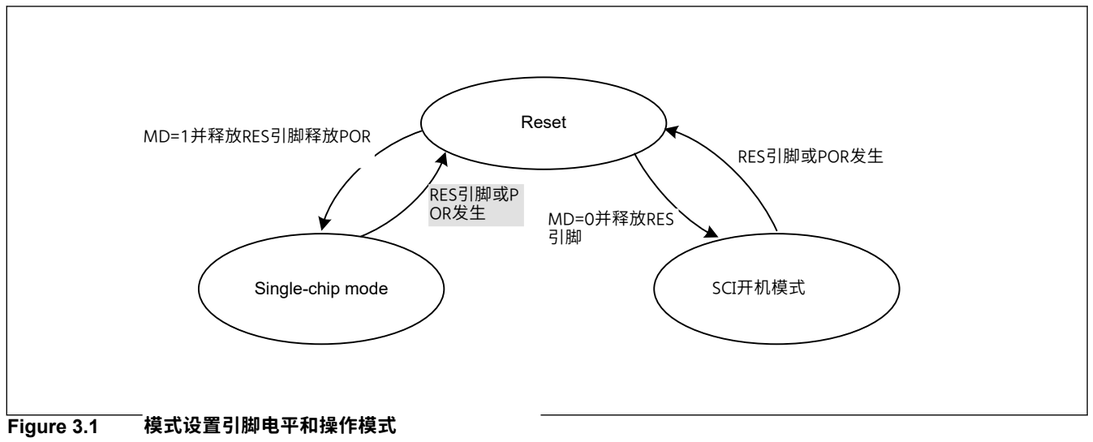
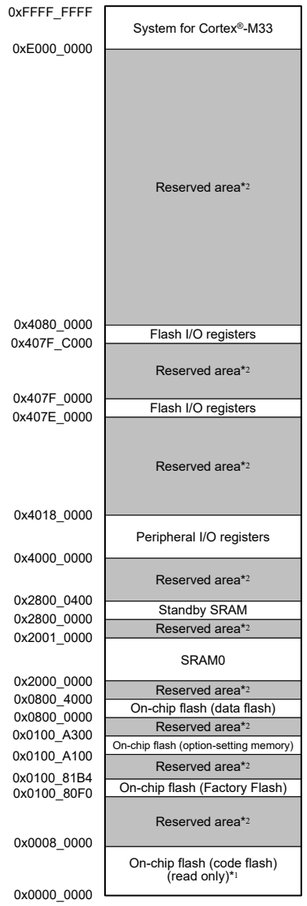


Figure 3.1 模式设置引脚电平和操作模式

4. Address Space

4.1 Address Space

The MCU supports a 4-GB linear address space ranging from 0x0000_0000 to 0xFFFF_FFFF that can contain both program and data. Figure 4.1 shows the memory map.



Note 1. See Table 4.1. The capacity of the flash differs depending on the product.
Note 2. Do not access reserved areas.

Figure 4.1 Memory map

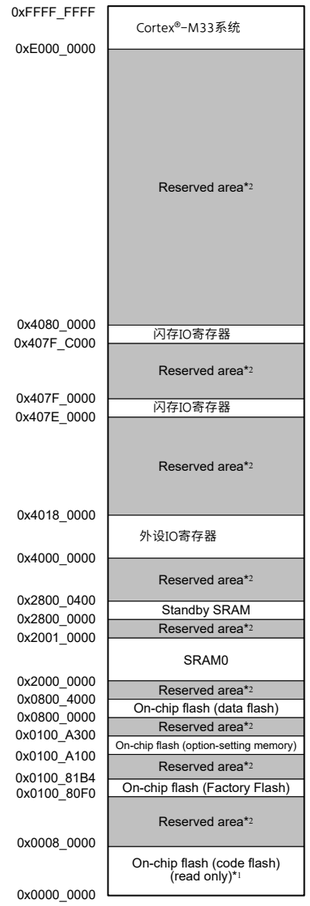
Table 4.1 Capacity of the code flash memory, data flash memory, and SRAM0

Code flash memory		Data flash memory		SRAM0	
Capacity	**Address**	**Capacity**	**Address**	**Capacity**	**Address**
512 KB	0x0000_0000 - 0x0007_FFFF	16 KB	0x0800_0000 - 0x0800_3FFF	64 KB	0x2000_0000 - 0x2000_FFFF
256 KB	0x0000_0000 - 0x0003_FFFF				

4. 地址空间

4.1 地址空间

MCU支持4-GB线性地址空间，范围从0x0000_0000到0xFFFF_FFFF，可以同时包含程序和数据。图4.1显示了内存映射。



注1.见表4.1。闪光灯的容量因产品而异。
注2.请勿进入保留区域。

Figure 4.1 内存映射

Table 4.1 代码闪存、数据闪存和SRAM0的容量

代码闪存		数据闪存		SRAM0	
Capacity	**Address**	**Capacity**	**Address**	**Capacity**	**Address**
512 KB	0x0000_0000 - 0x0007_FFFF	16 KB	0x0800_0000 - 0x0800_3FFF	64 KB	0x2000_0000 - 0x2000_FFFF
256 KB	0x0000_0000 - 0x0003_FFFF				

5. Resets

5.1 Overview

The MCU provides 14 resets.

Table 5.1 lists the reset names and sources.

Table 5.1 Reset names and sources

Reset name	Source
RES pin reset	Voltage input to the RES pin is driven low
Power-on reset	VCC rise (voltage detection V_{POR})*1
Independent watchdog timer reset	IWDT underflow or refresh error
Watchdog timer reset	WDT underflow or refresh error
Voltage monitor 0 reset	VCC fall (voltage detection V_{det0})*1
Voltage monitor 1 reset	VCC fall (voltage detection V_{det1})*1
Voltage monitor 2 reset	VCC fall (voltage detection V_{det2})*1
SRAM parity error reset	SRAM parity error detection
SRAM ECC error reset	SRAM ECC error detection
Bus master MPU error reset	Bus master MPU error detection
TrustZone error reset	TrustZone error detection
Cache Parity error reset	Cache Parity error detection
Deep software standby reset	Deep software standby mode is canceled by an interrupt
Software reset	Register setting (use the software reset bit AIRCR.SYSRESETREQ)

Note 1. For details on the voltages to be monitored (V_{POR}, V_{det0}, V_{det1}, and V_{det2}), see section 7, Low Voltage Detection (LVD) and section 46, Electrical Characteristics.

The internal state and pins are initialized by a reset. Table 5.2 and Table 5.3 list the targets initialized by resets.

Table 5.2 Reset detect flags initialized by each reset source (1 of 4)

Flag to be initialized	Reset source							
	RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Power-On Reset Detect Flag (RSTSR0.PORF)	✓	—	—	—	—	—	—	—
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	✓	✓	—	—	—	—	—	—
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	✓	✓	✓	—	—	—	—	—
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	✓	✓	✓	—	—	—	—	—
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	✓	✓	✓	—	—	—	—	—
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	✓	✓	✓	—	—	—	—	—

5. Resets

5.1 Overview

MCU提供14次复位。

表5.1列出了复位名称和来源。

Table 5.1 重置名称和来源

重设名称	Source
RES引脚复位	输入到RES引脚的电压被驱动为低电平
Power-on reset	VCC上升（电压检测VPOR）*1
独立看门狗定时器复位	IWDT下溢或刷新错误
看门狗定时器复位	WDT下溢或刷新错误
电压监控器0复位	VCC下降（电压检测Vdet0）*1
电压监视器1复位	VCC下降（电压检测Vdet1）*1
电压监视器2复位	VCC下降（电压检测Vdet2）*1
SRAM奇偶校验错误复位	SRAM奇偶校验错误检测
SRAMECC错误复位	SRAMECC错误检测
总线主控MPU错误复位	总线主控MPU错误检测
TrustZone错误重置	TrustZone错误检测
缓存奇偶校验错误重置	缓存奇偶校验错误检测
深度软件待机复位	深度软件待机模式被中断取消
软件复位	寄存器设置（使用软件复位位AIRCR.SYSRESETREQ）

注1.有关要监控的电压（VPOR、Vdet0、Vdet1和Vdet2）的详细信息，请参见第7节，低电压检测(LVD)和第46节，电气特性。

内部状态和引脚由复位初始化。表5.2和表5.3列出了由复位初始化的目标。

Table 5.2 由每个复位源初始化的复位检测标志（4个中的1个）

要初始化的标志	重置源							
	RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位	电压监视器1复位	电压监视器2复位	软件复位
上电复位检测标志(RSTSR0.PORF)	✓	—	—	—	—	—	—	—
电压监视器0复位检测标志(RSTSR0.LVD0RF)	✓	✓	—	—	—	—	—	—
Independent 看门狗定时器 复位检测标志(RSTSR1.IWDTRF)	✓	✓	✓	—	—	—	—	—
看门狗定时器 复位检测标志(RSTSR1.WDTRF)	✓	✓	✓	—	—	—	—	—
电压监视器1复位检测标志(RSTSR0.LVD1RF)	✓	✓	✓	—	—	—	—	—
电压监视器2复位检测标志(RSTSR0.LVD2RF)	✓	✓	✓	—	—	—	—	—

Table 5.2 Reset detect flags initialized by each reset source (2 of 4)

Flag to be initialized	Reset source							
	RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Software Reset Detect Flag (RSTSR1.SWRF)	✓	✓	✓	—	—	—	—	—
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	✓	✓	✓	—	—	—	—	—
SRAM ECC Error Reset Detect Flag (RSTSR1.REERF)	✓	✓	✓	—	—	—	—	—
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	✓	✓	✓	—	—	—	—	—
TrustZone Error Reset Detect Flag (RSTSR1.TZERF)	✓	✓	✓	—	—	—	—	—
Cache Parity Reset Detect Flag (RSTSR1.CPERF)	✓	✓	✓	—	—	—	—	—
Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF)	✓	✓	✓	—	—	—	—	—
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	—	✓	—	—	—	—	—	—

Table 5.2 Reset detect flags initialized by each reset source (3 of 4)

Flag to be initialized	Reset source						
	SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	TrustZone reset error	Cache Parity error reset	Deep Software Standby reset	
						DEEPCUT[0] = 0	DEEPCUT[0] = 1
Power-On Reset Detect Flag (RSTSR0.PORF)	—	—	—	—	—	—	—
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	—	—	—	—	—	—	—
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	—	—	—	—	—	✓	✓
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	—	—	—	—	—	✓	✓
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	—	—	—	—	—	—	—
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	—	—	—	—	—	—	—
Software Reset Detect Flag (RSTSR1.SWRF)	—	—	—	—	—	✓	✓
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	—	—	—	—	—	✓	✓
SRAM ECC Error Reset Detect Flag (RSTSR1.REERF)	—	—	—	—	—	✓	✓
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	—	—	—	—	—	✓	✓

Table 5.2 由每个复位源初始化的复位检测标志（4个中的2个）

要初始化的标志	重置源							
	RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位	电压监视器1复位	电压监视器2复位	软件复位
软件复位检测标志(RSTSR1.SWRF)	✓	✓	✓	—	—	—	—	—
SRAM奇偶校验错误复位检测标志（RSTSR1.RPERF）	✓	✓	✓	—	—	—	—	—
SRAMECC错误复位检测标志(RSTSR1.REERF)	✓	✓	✓	—	—	—	—	—
总线主控MPU错误复位检测标志(RSTSR1.BUSMRF)	✓	✓	✓	—	—	—	—	—
TrustZone错误重置检测标志(RSTSR1.TZERF)	✓	✓	✓	—	—	—	—	—
高速缓存奇偶校验复位检测标志(RSTSR1.CPERF)	✓	✓	✓	—	—	—	—	—
深度软件待机复位检测标志(RSTSR0.DPRSTF)	✓	✓	✓	—	—	—	—	—
冷启动热启动确定标志(RSTSR2.CWSF)	—	✓	—	—	—	—	—	—

Table 5.2 由每个复位源初始化的复位检测标志（4个中的3个）

要初始化的标志	重置源						
	SRAM奇偶校验错误复位	SRAM ECC错误复位	总线主控MPU错误复位	TrustZone重置错误	缓存奇偶校验错误重置	深度软件待机复位	
						DEEPCUT[0] = 0	DEEPCUT[0] = 1
上电复位检测标志(RSTSR0.PORF)	—	—	—	—	—	—	—
电压监控器0复位检测Flag (RSTSR0.LVD0RF)	—	—	—	—	—	—	—
独立看门狗定时器复位检测标志(RSTSR1.IWDTRF)	—	—	—	—	—	✓	✓
看门狗定时器复位检测Flag (RSTSR1.WDTRF)	—	—	—	—	—	✓	✓
电压监视器1复位检测Flag (RSTSR0.LVD1RF)	—	—	—	—	—	—	—
电压监视器2复位检测Flag (RSTSR0.LVD2RF)	—	—	—	—	—	—	—
软件复位检测标志(RSTSR1.SWRF)	—	—	—	—	—	✓	✓
SRAM奇偶校验错误复位检测Flag (RSTSR1.RPERF)	—	—	—	—	—	✓	✓
SRAMECC错误复位检测Flag (RSTSR1.REERF)	—	—	—	—	—	✓	✓
总线主控MPU错误复位检测标志(RSTSR1.BUSMRF)	—	—	—	—	—	✓	✓

Table 5.2 Reset detect flags initialized by each reset source (4 of 4)

Flag to be initialized	Reset source						
	SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	TrustZone reset error	Cache Parity error reset	Deep Software Standby reset	
						DEEPCUT[0] = 0	DEEPCUT[0] = 1
TrustZone Error Reset Detect Flag (RSTSR1.TZERF)	—	—	—	—	—	✓	✓
Cache Parity Reset Detect Flag (RSTSR1.CPERF)	—	—	—	—	—	✓	✓
Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF)	—	—	—	—	—	—	—
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	—	—	—	—	—	—	—

Note: ✓ : Initialized to 0
— : Not initialized

Table 5.3 Module-related registers initialized by each reset source (1 of 4)

Registers to be initialized		Reset source							
		RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Independent watchdog timer registers	IWDTRR, IWDTSR	✓	✓	✓	✓	✓	✓	✓	✓
Watchdog timer registers	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓	✓
Voltage monitor function 1 registers	LVD1CR0,LVD1CMPCR	✓	✓	✓	✓	✓	—	—	—
	LVD1CR1/LVD1SR	✓	✓	✓	✓	✓	—	—	—
Voltage monitor function 2 registers	LVD2CR0, LVD2CMPCR	✓	✓	✓	✓	✓	—	—	—
	LVD2CR1/LVD2SR	✓	✓	✓	✓	✓	—	—	—
LOCO registers	LOCOCR	✓	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	—	✓	✓	—	—	✓	✓	—
MOSC register	MOMCR	✓	✓	✓	✓	✓	✓	✓	✓
Bus, MPU and TrustZone error registers*2	BUS_ERROR_ADDRESS Register BUS_ERROR_STATUS Register	✓	✓	✓	✓	✓	✓	✓	✓
Pin states		✓	✓	✓	✓	✓	✓	✓	✓
Low-power function registers	DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	✓	✓	✓
	SYOCDCR	—	✓	—	—	—	—	—	—

Table 5.2 由每个复位源初始化的复位检测标志（4个中的4个）

要初始化的标志	重置源						
	SRAM奇偶校验错误复位	SRAM ECC错误复位	总线主控MPU错误复位	TrustZone重置错误	缓存奇偶校验错误重置	深度软件待机复位	
						DEEPCUT[0] = 0	DEEPCUT[0] = 1
TrustZone错误复位检测标志(RSTSR1.TZERF)	—	—	—	—	—	✓	✓
高速缓存奇偶校验复位检测标志(RSTSR1.CPERF)	—	—	—	—	—	✓	✓
深度软件待机复位检测标志(RSTSR0.DPRSTF)	—	—	—	—	—	—	—
冷启动热启动确定标志(RSTSR2.CWSF)	—	—	—	—	—	—	—

Note: :初始化为0—:未初始化

Table 5.3 由每个复位源初始化的模块相关寄存器（4个中的1个）

待初始化的寄存器		重置源							
		RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位	电压监视器1复位	电压监视器2复位	软件复位
独立的看门狗定时器寄存器	IWDTRR, IWDTSR	✓	✓	✓	✓	✓	✓	✓	✓
看门狗定时器寄存器	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓	✓
电压监控功能1个寄存器	LVD1CR0,LVD1CMPCR	✓	✓	✓	✓	✓	—	—	—
	LVD1CR1/LVD1SR	✓	✓	✓	✓	✓	—	—	—
电压监控功能2个寄存器	LVD2CR0, LVD2CMPCR	✓	✓	✓	✓	✓	—	—	—
	LVD2CR1/LVD2SR	✓	✓	✓	✓	✓	—	—	—
LOCO寄存器	LOCOCR	✓	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	—	✓	✓	—	—	✓	✓	—
MOSC register	MOMCR	✓	✓	✓	✓	✓	✓	✓	✓
总线、MPU和TrustZone错误寄存器*2	BUS_ERROR_ADDRESS寄存器BUS_ERROR_STAT 美国注册	✓	✓	✓	✓	✓	✓	✓	✓
引脚状态		✓	✓	✓	✓	✓	✓	✓	✓
低功耗功能寄存器	DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	✓	✓	✓
	SYOCDCR	—	✓	—	—	—	—	—	—

Table 5.3 Module-related registers initialized by each reset source (2 of 4)

Registers to be initialized		Reset source							
		RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Security Attribute Registers	CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, TZFSAR	✓*3	✓	✓*3	✓*3	✓*3	✓*3	✓*3	✓*3
Registers other than those shown, CPU, and internal state		✓	✓	✓	✓	✓	✓	✓	✓

Table 5.3 Module-related registers initialized by each reset source (3 of 4)

Registers to be initialized		Reset source						
		SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	TrustZone error reset	Cache Parity error reset	Deep Software Standby reset	
							DEEPCUT[0] = 0	DEEPCUT[0] = 1
Independent watchdog timer registers	IWDTRR, IWDTSR	✓	✓	✓	✓	✓	✓	✓
Watchdog timer registers	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓
Voltage monitor function 1 registers	LVD1CR0,LVD1CMPCR	—	—	—	—	—	—	—
	LVD1CR1 / LVD1SR	—	—	—	—	—	✓	✓
Voltage monitor function 2 registers	LVD2CR0, LVD2CMPCR	—	—	—	—	—	—	—
	LVD2CR1/LVD2SR	—	—	—	—	—	✓	✓
LOCO registers	LOCOCR	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	—	—	—	—	—	—	✓
MOSC register	MOMCR	✓	✓	✓	✓	✓	—	—
Bus, MPU and TrustZone error registers*2	BUS_ERROR_ADDRESS Register BUS_ERROR_STATUS Register	✓	✓	—	—	—	✓	✓
Pin states		✓	✓	✓	✓	✓	*1	*1
Low-power function registers	DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	—	—
	SYOCDCR	—	—	—	—	—	—	—

Table 5.3 由每个复位源初始化的模块相关寄存器（4个中的2个）

待初始化的寄存器		重置源							
		RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位	电压监视器1复位	电压监视器2复位	软件复位
安全属性Registers	CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, TZFSAR	✓*3	✓	✓*3	✓*3	✓*3	✓*3	✓*3	✓*3
未显示的寄存器、CPU和内部状态		✓	✓	✓	✓	✓	✓	✓	✓

Table 5.3 由每个复位源初始化的模块相关寄存器（4个中的3个）

待初始化的寄存器		重置源						
		SRAM奇偶校验错误复位	SRAMECC错误复位	总线主控MPU错误复位	TrustZone错误重置	缓存奇偶校验错误重置	深度软件待机复位	
							DEEPCUT[0] = 0	DEEPCUT[0] = 1
独立的看门狗定时器寄存器	IWDTRR, IWDTSR	✓	✓	✓	✓	✓	✓	✓
看门狗定时器寄存器	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓
电压监控功能1个寄存器	LVD1CR0,LVD1CMPCR	—	—	—	—	—	—	—
	LVD1CR1 / LVD1SR	—	—	—	—	—	✓	✓
电压监控功能2个寄存器	LVD2CR0, LVD2CMPCR	—	—	—	—	—	—	—
	LVD2CR1/LVD2SR	—	—	—	—	—	✓	✓
LOCO寄存器	LOCOCR	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	—	—	—	—	—	—	✓
MOSC register	MOMCR	✓	✓	✓	✓	✓	—	—
总线、MPU和TrustZone错误寄存器*2	BUS_ERROR_ADDRESS Register BUS_ERROR_STATUS Register	✓	✓	—	—	—	✓	✓
引脚状态		✓	✓	✓	✓	✓	*1	*1
低功耗功能寄存器	DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	—	—
	SYOCDCR	—	—	—	—	—	—	—

Table 5.3 Module-related registers initialized by each reset source (4 of 4)

Registers to be initialized		Reset source						
		SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	TrustZone error reset	Cache Parity error reset	Deep Software Standby reset	
							DEEPCU T[0] = 0	DEEPCU T[0] = 1
Security Attribute Registers	CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, TZFSAR	✓*3	✓*3	✓*3	✓*3	✓*3	✓*4	✓*4
Registers other than those shown, CPU, and internal state		✓	✓	✓	✓	✓	✓	✓

Note: ✓ : Initialized
— : Not initialized
Note 1. Depends on the setting of DPSBYCR.IOKEEP.
Note 2. Some control bits are not initialized by all types of resets. For details on the target bits, see section 13, Buses
Note 3. Reset does not occur while the debugger is connected (DBGSTR.CDBGPWRUPREQ = 1) even if On-chip debugger is disabled (SYOCDCR.DBGEN = 0).
Note 4. Reset does not occur while On-chip debugger is enabled (SYOCDCR.DBGEN = 1).

Table 5.4 shows the states of LOCO when a reset occurs.

Table 5.4 States of LOCO when a reset occurs

		Reset source	
		POR, LVD0, LVD1, LVD2, Deep Software Standby (DEEPCUT[0] = 1)	Other
LOCO	Enable or disable	Initialized to enable	
	Oscillation accuracy*1	Initialized to accuracy before trimming by power-on (accuracy: ± 10%)	Continue with the accuracy that was trimmed by LOCOUTCR

Note 1. The LOCO User Trimming Control Register (LOCOUTCR) is reset by POR, LVD0, LVD1, LVD2, and Deep Software Standby (DEEPCUT[0] = 1) resets, returning the LOCO to the default oscillation accuracy. To restore the pre-reset LOCO oscillation accuracy, reload the required trimming value into LOCOUTCR after any of these resets.

When a reset is released, reset exception handling starts.

Table 5.5 lists the pin related to the reset function.

Table 5.5 Pin related to reset

Pin name	I/O	Function
RES	Input	Reset pin

Table 5.3 由每个复位源初始化的模块相关寄存器（4个，共4个）

待初始化的寄存器		重置源						
		SRAM奇偶校验错误复位	SRAMECC错误复位	总线主控MPU错误复位	TrustZone错误重置	缓存奇偶校验错误重置	深度软件待机复位	
							DEEPCU T[0] = 0	DEEPCU T[0] = 1
安全属性Registers	CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, TZFSAR	✓*3	✓*3	✓*3	✓*3	✓*3	✓*4	✓*4
未显示的寄存器、CPU和内部状态		✓	✓	✓	✓	✓	✓	✓

Note: :已初始化—:未初始化
注1.取决于DPSBYCR.IOKEEP的设置。
注2.并非所有类型的复位都会初始化一些控制位。有关目标位的详细信息，请参阅第13节，总线
注3.连接调试器(DBGSTR.CDBGPWRUPREQ=1)时不会发生复位，即使片上调试器被禁用(SYOCDCR.DBGEN=0)。

注4.启用片上调试器(SYOCDCR.DBGEN=1)时不会发生复位。

表5.4显示了复位发生时LOCO的状态。

Table 5.4 发生复位时的LOCO状态

		重置源	
		POR、LVD0、LVD1、LVD2、深软件待机（DEEPCUT[0]=1）	Other
LOCO	启用或禁用	初始化为启用	
	振荡精度*1	上电微调前初始化为精度（精度：±10%）	继续使用被修剪的精度LOCOUTCR

注1.LOCO用户微调控制寄存器(LOCOUTCR)通过POR、LVD0、LVD1、LVD2和深度软件待机(DEEPCUT[0]=1)复位，将LOCO返回到默认振荡精度。要恢复预复位的LOCO振荡精度，请在任何这些复位后将所需的微调值重新加载到LOCOUTCR。

当一个复位被释放时，复位异常处理开始。

表5.5列出了与复位功能相关的引脚。

Table 5.5 复位相关引脚

引脚名称	I/O	Function
RES	Input	复位引脚

5.2 Register Descriptions

5.2.1 RSTSAR : Reset Security Attribution Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3C4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC2	NONSEC1	NONSEC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0	Non Secure Attribute bit 0 Target register: Reset Status Register 0 0: Secure 1: Non Secure	R/W
1	NONSEC1	Non Secure Attribute bit 1 Target register: Reset Status Register 1 0: Secure 1: Non Secure	R/W
2	NONSEC2	Non Secure Attribute bit 2 Target register: Reset Status Register 2 0: Secure 1: Non Secure	R/W
31:3	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

NONSEC0 bit (Non Secure Attribute bit 0)

This bit controls the security attribute of RSTSR0.

NONSEC1 bit (Non Secure Attribute bit 1)

This bit controls the security attribute of RSTSR1.

NONSEC2 bit (Non Secure Attribute bit 2)

This bit controls the security attribute of RSTSR2.

5.2.2 RSTSR0 : Reset Status Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x410

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSRSTF	—	—	—	LVD2RF	LVD1RF	LVD0RF	PORF
Value after reset:	x*1	0	0	0	x*1	x*1	x*1	x*1

5.2 注册说明

5.2.1 RSTSAR：重置安全属性寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x3C4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC2	NONSEC1	NONSEC0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0	非安全属性位0 目标寄存器：复位状态寄存器0 0：安全1：不安全	R/W
1	NONSEC1	非安全属性位1 目标寄存器：复位状态寄存器1 0：安全1：不安全	R/W
2	NONSEC2	非安全属性位2 目标寄存器：复位状态寄存器2 0：安全1：不安全	R/W
31:3	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

NONSEC0位（非安全属性位0）

该位控制RSTSR0的安全属性。

NONSEC1位（非安全属性位1）

该位控制RSTSR1的安全属性。

NONSEC2位（非安全属性位2）

该位控制RSTSR2的安全属性。

5.2.2 RSTSR0：复位状态寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x410

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSRSTF	—	—	—	LVD2RF	LVD1RF	LVD0RF	PORF
重置后的值：	x*1	0	0	0	x*1	x*1	x*1	x*1

Bit	Symbol	Function	R/W
0	PORF	Power-On Reset Detect Flag 0: Power-on reset not detected 1: Power-on reset detected	R/W*2
1	LVD0RF	Voltage Monitor 0 Reset Detect Flag 0: Voltage monitor 0 reset not detected 1: Voltage monitor 0 reset detected	R/W*2
2	LVD1RF	Voltage Monitor 1 Reset Detect Flag 0: Voltage monitor 1 reset not detected 1: Voltage monitor 1 reset detected	R/W*2
3	LVD2RF	Voltage Monitor 2 Reset Detect Flag 0: Voltage monitor 2 reset not detected 1: Voltage monitor 2 reset detected	R/W*2
6:4	—	These bits are read as 0. The write value should be 0.	R/W
7	DPSRSTF	Deep Software Standby Reset Flag 0: Deep software standby mode cancellation not requested by an interrupt. 1: Deep software standby mode cancellation requested by an interrupt.	R/W*2

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The value after reset depends on the reset source.
Note 2. The register is cleared when a reset source listed in Table 5.2 occurs or when 0 is written to clear a flag. Bits other than the flag that is cleared should be set to 1.

PORF flag (Power-On Reset Detect Flag)

The PORF flag indicates that a power-on reset occurred.

[Setting condition]

- When a power-on reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When PORF is read as 1 and then 0 is written to PORF

LVD0RF flag (Voltage Monitor 0 Reset Detect Flag)

The LVD0RF flag indicates that the VCC voltage fell below V_{det0}.

[Setting condition]

- When a voltage monitor 0 reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When LVD0RF is read as 1 and then 0 is written to LVD0RF.

LVD1RF flag (Voltage Monitor 1 Reset Detect Flag)

The LVD1RF flag indicates that the VCC voltage fell below V_{det1}.

[Setting condition]

- When a voltage monitor 1 reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When LVD1RF is read as 1 and then 0 is written to LVD1RF

Bit	Symbol	Function	R/W
0	PORF	上电复位检测标志 0：未检测到上电复位1：检测到上电复位	R/W*2
1	LVD0RF	电压监视器0复位检测标志 0：未检测到电压监控器0复位1：检测到电压监控器0复位	R/W*2
2	LVD1RF	电压监视器1复位检测标志 0：未检测到电压监控器1复位1：检测到电压监控器1复位	R/W*2
3	LVD2RF	电压监视器2复位检测标志 0：未检测到电压监控器2复位1：检测到电压监控器2复位	R/W*2
6:4	—	这些位被读取为0。写入值应为0。	R/W
7	DPSRSTF	深度软件待机复位标志 0：中断未请求深度软件待机模式取消。1：中断请求的深度软件待机模式取消。	R/W*2

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.复位后的值取决于复位源。
注2.当表5.2中列出的复位源发生或写入0以清除标志时，该寄存器被清除。清除标志以外的位应设置为1。

PORF标志（上电复位检测标志）

PORF标志表示发生了上电复位。

[Setting condition]

●发生上电复位时。

[Clearing conditions]

●发生表5.2中列出的复位时
●当PORF读为1，然后将0写入PORF

LVD0RF标志（电压监视器0复位检测标志）

LVD0RF标志表示VCC电压低于Vdet0。

[Setting condition]

●发生电压监视器0复位时。

[Clearing conditions]

●发生表5.2中列出的复位时
●当LVD0RF被读为1，然后0被写入LVD0RF。

LVD1RF标志（电压监视器1复位检测标志）

LVD1RF标志表示VCC电压低于Vdet1。

[Setting condition]

●发生电压监视器1复位时。

[Clearing conditions]

●发生表5.2中列出的复位时
●当LVD1RF被读为1，然后0被写入LVD1RF

LVD2RF flag (Voltage Monitor 2 Reset Detect Flag)

The LVD2RF flag indicates that the VCC voltage fell below V_{det2}.

[Setting condition]

- When a voltage monitor 2 reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When LVD2RF is read as 1 and then 0 is written to LVD2RF

DPSRSTF flag (Deep Software Standby Reset Flag)

The DPSRSTF flag indicates that deep software standby mode has been canceled by an external or internal interrupt and that an internal reset (deep software standby reset) occurred when the exception from Deep Software Standby Mode occur.

[Setting condition]

- When deep software standby mode is cancelled by an external or an internal interrupt. For details, see section 10, Low Power Modes.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs.
- When DPSRSTF is read as 1 and then 0 is written to DPSRSTF

5.2.3 RSTSR1 : Reset Status Register 1

Base address: SYSC = 0x4001_E000
Offset address: 0x0C0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPERF	—	TZERF	—	BUSMRF	—	REERF	RPERF	—	—	—	—	—	SWRF	WDTRF	IWDTRF
Value after reset:	x*1	0	x*1	0	x*1	0	x*1	x*1	0	0	0	0	0	x*1	x*1	x*1

Bit	Symbol	Function	R/W
0	IWDTRF	Independent Watchdog Timer Reset Detect Flag 0: Independent watchdog timer reset not detected 1: Independent watchdog timer reset detected	R/W*2
1	WDTRF	Watchdog Timer Reset Detect Flag 0: Watchdog timer reset not detected 1: Watchdog timer reset detected	R/W*2
2	SWRF	Software Reset Detect Flag 0: Software reset not detected 1: Software reset detected	R/W*2
7:3	—	These bits are read as 0. The write value should be 0.	R/W
8	RPERF	SRAM Parity Error Reset Detect Flag 0: SRAM parity error reset not detected 1: SRAM parity error reset detected	R/W*2
9	REERF	SRAM ECC Error Reset Detect Flag 0: SRAM ECC error reset not detected 1: SRAM ECC error reset detected	R/W*2
10	—	This bit is read as 0. The write value should be 0.	R/W
11	BUSMRF	Bus Master MPU Error Reset Detect Flag 0: Bus master MPU error reset not detected 1: Bus master MPU error reset detected	R/W*2
12	—	This bit is read as 0. The write value should be 0.	R/W

LVD2RF标志（电压监视器2复位检测标志）

LVD2RF标志表示VCC电压低于Vdet2。

[Setting condition]

●发生电压监视器2复位时。

[Clearing conditions]

●发生表5.2中列出的复位时

●当LVD2RF被读为1，然后0被写入LVD2RF

DPRSTF标志（深度软件待机复位标志）

DPSRSTF标志表示深度软件待机模式已被外部或内部中断取消，并且当深度软件待机模式发生异常时发生内部复位（深度软件待机复位）。

[Setting condition]

●当深度软件待机模式被外部或内部中断取消时。有关详细信息，请参阅第10节，低功耗模式。

[Clearing conditions]

●发生表5.2中列出的复位时。

●DPSRSTF被读为1，然后0被写入DPSRSTF

5.2.3 RSTSR1：复位状态寄存器1

Base address: SYSC = 0x4001_E000
Offset address: 0x0C0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPERF	—	TZERF	—	BUSMRF	—	REERF	RPERF	—	—	—	—	—	SWRF	WDTRF	IWDTRF
重置后的值：	x*1	0	x*1	0	x*1	0	x*1	x*1	0	0	0	0	0	x*1	x*1	x*1

Bit	Symbol	Function	R/W
0	IWDTRF	独立看门狗定时器复位检测标志 0：未检测到独立看门狗定时器复位1：检测到独立看门狗定时器复位	R/W*2
1	WDTRF	看门狗定时器复位检测标志 0：未检测到看门狗定时器复位1：检测到看门狗定时器复位	R/W*2
2	SWRF	软件复位检测标志 0：未检测到软件复位1：检测到软件复位	R/W*2
7:3	—	这些位被读取为0。写入值应为0。	R/W
8	RPERF	SRAM奇偶校验错误复位检测标志 0：未检测到SRAM奇偶校验错误复位1：检测到SRAM奇偶校验错误复位	R/W*2
9	REERF	SRAMECC错误复位检测标志 0：未检测到SRAMECC错误复位1：检测到SRAMECC错误复位	R/W*2
10	—	该位读取为0。写入值应为0。	R/W
11	BUSMRF	总线主控MPU错误复位检测标志 0：未检测到总线主控MPU错误复位1：检测到总线主控MPU错误复位	R/W*2
12	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
13	TZERF	TrustZone Error Reset Detect Flag 0: TrustZone error reset not detected. 1: TrustZone error reset detected.	R/W*2
14	—	This bit is read as 0. The write value should be 0.	R/W
15	CPERF	Cache Parity Error Reset Detect Flag 0: Cache Parity error reset not detected. 1: Cache Parity error reset detected.	R/W*2

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag. The flag must be cleared by writing 0 after 1 is read.

IWDTRF flag (Independent Watchdog Timer Reset Detect Flag)

The IWDTRF flag indicates that an independent watchdog timer reset occurs.

[Setting condition]

- When an independent watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to IWDTRF.

WDTRF flag (Watchdog Timer Reset Detect Flag)

The WDTRF flag indicates that a watchdog timer reset occurs.

[Setting condition]

- When a watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written WDTRF.

SWRF flag (Software Reset Detect Flag)

The SWRF flag indicates that a software reset occurs.

[Setting condition]

- When a software reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to SWRF.

RPERF flag (SRAM Parity Error Reset Detect Flag)

The RPERF flag indicates that an SRAM parity error reset occurs.

[Setting condition]

- When an SRAM parity error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read as 1 and then 0 is written to RPERF.

Bit	Symbol	Function	R/W
13	TZERF	TrustZone错误复位检测标志 0：未检测到TrustZone错误复位。1： 检测到TrustZone错误复位。	R/W*2
14	—	该位读取为0。写入值应为0。	R/W
15	CPERF	高速缓存奇偶校验错误复位检测标志 0：未检测到缓存奇偶校验错误复位。1： 检测到缓存奇偶校验错误复位。	R/W*2

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.复位后的值取决于复位源。
注2.只能写入0来清除标志。该标志必须在读取1后写入0来清除。

IWDTRF标志（独立看门狗定时器复位检测标志）

IWDTRF标志指示发生了独立的看门狗定时器复位。

[Setting condition]

●发生独立看门狗定时器复位时。

[Clearing conditions]

●发生表5.2中列出的复位时

●读取1，然后将0写入IWDTRF。

WDTRF标志（看门狗定时器复位检测标志）

WDTRF标志指示发生了看门狗定时器复位。

[Setting condition]

●发生看门狗定时器复位时。

[Clearing conditions]

●发生表5.2中列出的复位时

●读取1后写入0时WDTRF。

SWRF标志（软件复位检测标志）

SWRF标志表示发生了软件复位。

[Setting condition]

●发生软件复位时。

[Clearing conditions]

●发生表5.2中列出的复位时

●读取1，然后将0写入SWRF。

RPERF标志（SRAM奇偶校验错误复位检测标志）

RPERF标志表示发生SRAM奇偶校验错误复位。

[Setting condition]

●SRAM奇偶校验错误复位发生时。

[Clearing conditions]

●发生表5.2中列出的复位时

●当1被读为1，然后0被写入RPERF。

REERF flag (SRAM ECC Error Reset Detect Flag)

The REERF flag indicates that an SRAM ECC error reset occurs.

[Setting condition]

- When an SRAM ECC error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read as 1 and then 0 is written to REERF.

BUSMRF flag (Bus Master MPU Error Reset Detect Flag)

The BUSMRF flag indicates that a bus master MPU error reset occurs.

[Setting condition]

- When a bus master MPU error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to BUSMRF.

TZERF flag (TrustZone Error Reset Detect Flag)

The TZERF flag indicates that a TrustZone error reset has occurred.

[Setting condition]

- When a TrustZone error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read then and 0 is written to TZERF.

CPERF flag (Cache Parity Error Reset Detect Flag)

The CPERF flag indicates that a Cache Parity error reset has occurred.

[Setting condition]

- When a Cache Parity error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read then and 0 is written to CPERF.

5.2.4 RSTSR2 : Reset Status Register 2

Base address: SYSC = 0x4001_E000

Offset address: 0x411

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CWSF
Value after reset:	0	0	0	0	0	0	0	x*1

Bit	Symbol	Function	R/W
0	CWSF	Cold/Warm Start Determination Flag 0: Cold start 1: Warm start	R/W*2

REERF标志（SRAMECC错误复位检测标志）

REERF标志表示发生了SRAMECC错误复位。

[Setting condition]

●SRAMECC错误复位发生时。

[Clearing conditions]

●发生表5.2中列出的复位时

●当1被读为1，然后0被写入REERF。

BUSMRF标志（总线主控MPU错误复位检测标志）

BUSMRF标志指示发生总线主控MPU错误复位。

[Setting condition]

●发生总线主控MPU错误复位时。

[Clearing conditions]

●发生表5.2中列出的复位时

●读取1，然后将0写入BUSMRF。

TZERF标志（TrustZone错误复位检测标志）

TZERF标志指示发生了TrustZone错误重置。

[Setting condition]

●发生TrustZone错误重置时。

[Clearing conditions]

●发生表5.2中列出的复位时

●读取1并将0写入TZERF。

CPERF标志（高速缓存奇偶校验错误复位检测标志）

CPERF标志表示发生了缓存奇偶校验错误重置。

[Setting condition]

●发生CacheParity错误复位时。

[Clearing conditions]

●发生表5.2中列出的复位时

●读取1并将0写入CPERF。

5.2.4 RSTSR2：复位状态寄存器2

Base address: SYSC = 0x4001_E000

Offset address: 0x411

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CWSF
重置后的值：	0	0	0	0	0	0	0	x*1

Bit	Symbol	Function	R/W
0	CWSF	冷暖启动确定标志 0：冷启动1： 热启动	R/W*2

Bit	Symbol	Function	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The value after reset depends on the reset source.
Note 2. Only 1 can be written to set the flag.

RSTSR2 determines whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

CWSF flag (Cold/Warm Start Determination Flag)

The CWSF flag indicates the type of reset processing, either cold start or warm start. The determines whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start). CWSF flag is initialized by a power-on reset. It is not initialized by a reset signal generated by the RES pin.

[Setting condition]

- When 1 is written by software. Writing 0 to CWSF does not set it to 0.

[Clearing condition]

- When a reset listed in Table 5.2 occurs.

5.3 Operation

5.3.1 RES Pin Reset

The RES pin generates this reset. When the RES pin is driven low, all the processing in progress is aborted and the MCU enters a reset state. To successfully reset the MCU, the RES pin must be held low for the power supply stabilization time specified at power-on.

When the RES pin is driven high from low, the internal reset is canceled after the post-RES cancellation wait time (t_{RESWT}) elapses. The CPU then starts the reset exception handling.

For details, see section 46, Electrical Characteristics.

5.3.2 Power-On Reset

The power-on reset (POR) is an internal reset generated by the power-on reset circuit. A power-on reset is generated under the following conditions.

1. If the RES pin is in a high level state when power is supplied
2. If the RES pin is in a high level state when VCC is below V_{POR}

After VCC exceeds V_{POR} and the specified power-on reset time (t_{POR}) elapses, the CPU starts the reset exception handling. The power-on reset time is a stabilization period of the external power supply and the MCU circuit.

After a power-on reset is generated, the PORF flag in the RSTSR0 is set to 1. The PORF flag is initialized by the RES pin reset. When VCC falls below V_{POR}, a power-on reset state is occurred.

Figure 5.1 shows example of operations during a power-on reset.

Bit	Symbol	Function	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.复位后的值取决于复位源。
注2.只能写入1来设置标志。

RSTSR2判断是上电复位导致复位处理（冷启动）还是操作期间输入的复位信号导致复位处理（热启动）。

CWSF标志（冷暖启动确定标志）

CWSF标志指示复位处理的类型，冷启动或热启动。确定是上电复位导致复位处理（冷启动）还是操作期间输入的复位信号导致复位处理（热启动）。CWSF标志由上电复位初始化。它不会被RES引脚产生的复位信号初始化。

[Setting condition]

●软件写入1时。将0写入CWSF不会将其设置为0。

[Clearing condition]

●发生表5.2中列出的复位时。

5.3 Operation

5.3.1 RES引脚复位

RES引脚产生此复位。当RES引脚被驱动为低电平时，所有正在进行的处理都被中止，MCU进入复位状态。要成功复位MCU，RES引脚必须在上电时指定的电源稳定时间内保持低电平。

当RES引脚从低电平驱动为高电平时，内部复位会在RES取消后等待时间(tRESWT)过去后取消。CPU然后开始复位异常处理。

有关详细信息，请参见第46节，电气特性。

5.3.2 Power-On Reset

上电复位（POR）是由上电复位电路产生的内部复位。在以下条件下会产生上电复位。

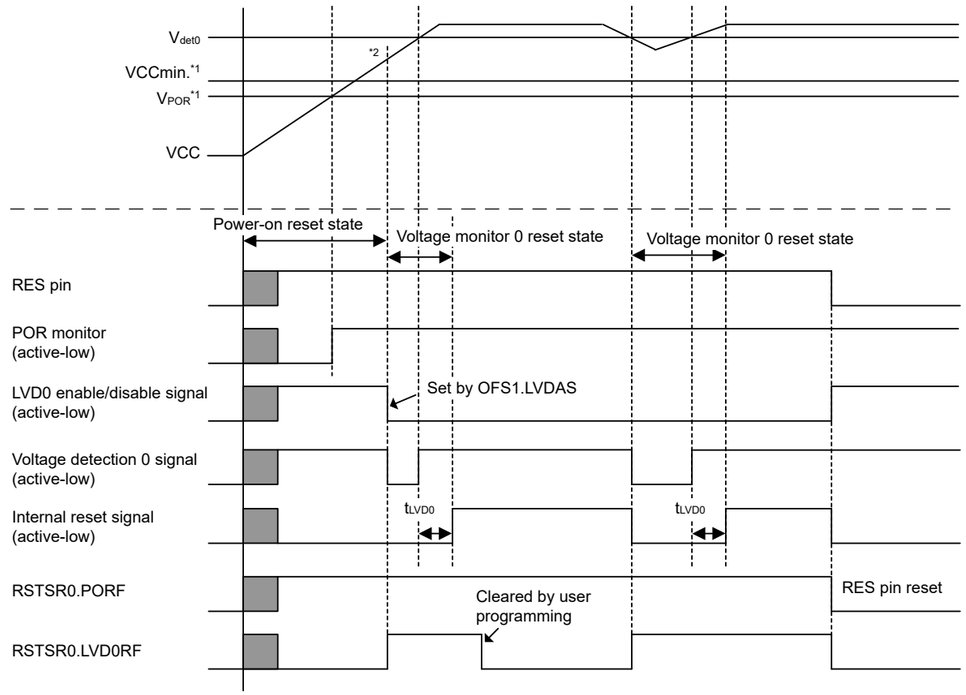
1.如果RES引脚在供电时处于高电平状态

2.如果VCC低于VPOR时RES管脚处于高电平状态

在VCC超过VPOR并且经过指定的上电复位时间(tPOR)后，CPU开始复位异常处理。
上电复位时间是外部电源和MCU电路的稳定期。

上电复位产生后，RSTSR0中的PORF标志设置为1。PORF标志由RES引脚复位初始化。当VCC低于VPOR时，会发生上电复位状态。

图5.1显示了上电复位期间的操作示例。



Note: For details on the electrical characteristics, see section 46, Electrical Characteristics.
Note 1. V_{POR} shows a power-on reset detection level, and VCCmin shows the minimum guaranteed voltage of MCU.
Note 2. At power-on, VCC should rise to the minimum guaranteed voltage before the power-on reset is released.

Figure 5.1 Example of operations during a power-on reset

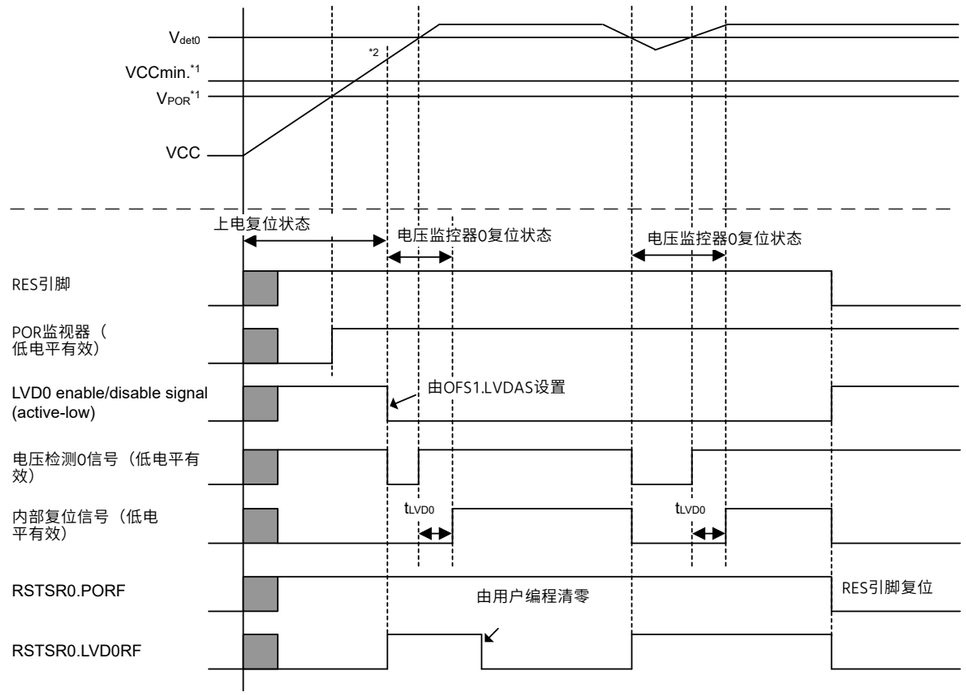
5.3.3 Voltage Monitor Reset

The voltage monitor i (i = 0, 1, 2) reset is an internal reset generated by the voltage monitor i circuit. If the Voltage Detection 0 Circuit Start (LVDAS) bit in the Option Function Select Register 1 (OFS1) is 0 (voltage monitor 0 reset is enabled after a reset) and VCC falls below V_{det0}, the RSTSR0.LVD0RF flag becomes 1 and the voltage detection circuit generates voltage monitor 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitor 0 reset is to be used. After VCC exceeds V_{det0} and the voltage monitor 0 reset time (t_{LVD0}) elapses, the internal reset is canceled and the CPU starts the reset exception handling.

When the Voltage Monitor 1 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the Voltage Monitor 1 Circuit Mode Select bit (RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0), the RSTSR0.LVD1RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 1 reset if VCC falls to or below V_{det1}.

Likewise, when the Voltage Monitor 2 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the Voltage Monitor 2 Circuit Mode Select bit (RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in Voltage Monitor 2 Circuit Control Register 0 (LVD2CR0), the RSTSR0.LVD2RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 2 reset if VCC falls to or below V_{det2}.

Similarly, timing for release from the voltage monitor 1 reset state is selectable with the Voltage Monitor 1 Reset Negate Select bit (RN) in the LVD1CR0. When the LVD1CR0.RN bit is 0 and VCC falls to or below V_{det1}, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (t_{LVD1}) elapses after VCC rises above V_{det1}. When the LVD1CR0.RN bit is 1 and VCC falls to or below V_{det1}, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (t_{LVD1}) elapses.



Note: 有关电气特性的详细信息，请参见第46节，电气特性。
注1.VPOR表示上电复位检测电平，VCCmin表示MCU的最低保证电压。
注2.上电时，VCC应上升到上电复位解除前的最低保证电压。

Figure 5.1 上电复位时的动作示例

5.3.3 电压监视器复位

电压监视器i(i=0 1 2)复位是由电压监视器i电路产生的内部复位。如果电压选项功能选择寄存器1(OFS1)中的检测0电路启动(LVDAS)位为0（复位后使能电压监视器0复位）且VCC低于Vdet0时，RSTSR0.LVD0RF标志变为1，电压检测电路生成电压监视器0复位。如果要使用电压监视器0复位，则将OFS1.LVDAS位清零。在VCC超过Vdet0并且经过电压监视器0复位时间(tLVD0)后，内部复位被取消，CPU开始复位异常处理。

当电压监控器1中断复位允许位(RIE)设置为1（允许电压检测电路产生复位或中断）并且电压监控器1电路模式选择位(RI)设置为1（选择产生电压监控器1电路控制寄存器0(LVD1CR0)中的低电压检测复位响应，RSTSR0.LVD1RF标志设置为1，如果VCC降至或低于V，电压检测电路产生电压监控器1复位det1。

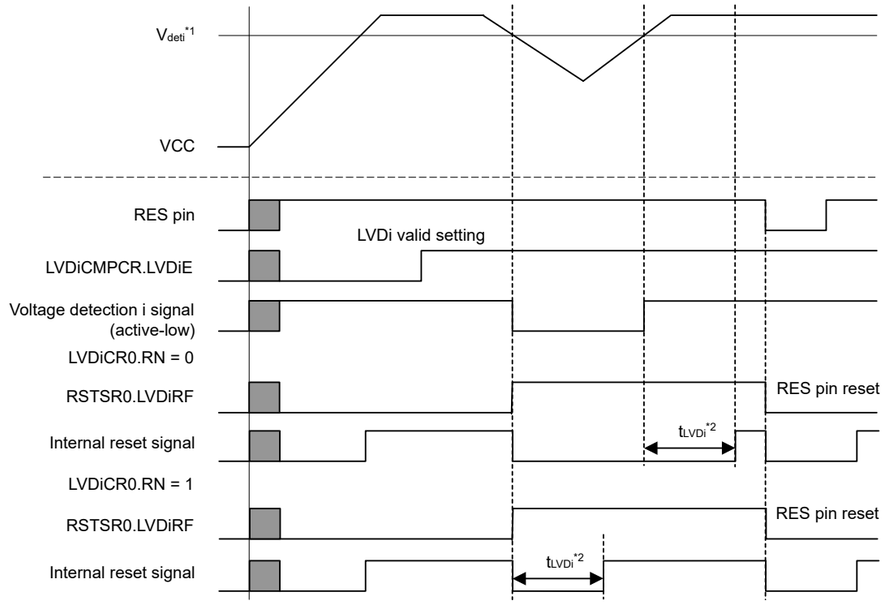
同样，当电压监视器2中断复位使能位(RIE)设置为1（允许电压检测电路产生复位或中断）并且电压监视器2电路模式选择位(RI)设置为1（选择在电压监控器2电路控制寄存器0(LVD2CR0)中响应检测到低电压产生复位），RSTSR0.LVD2RF标志设置为1，如果VCC下降到或电压检测电路产生电压监控器2复位低于Vdet2。

类似地，从电压监视器1复位状态释放的时间可通过LVD1CR0中的电压监视器1复位否定选择位(RN)来选择。当LVD1CR0.RN位为0且VCC下降到或低于Vdet1时，CPU从内部复位状态中释放并在VCC上升到Vdet1以上后经过LVD1复位时间(tLVD1)时开始复位异常处理。当LVD1CR0.RN位为1且VCC下降到或低于Vdet1时，CPU会从内部复位状态中释放，并在LVD1复位时间(tLVD1)过去后开始复位异常处理。

Likewise, timing for release from the voltage monitor 2 reset state is selectable by setting the Voltage Monitor 2 Reset Negate Select bit (RN) in the LDV2CR0 register.

Detection levels V_{det1} and V_{det2} can be changed in the Voltage Monitoring Comparator Control Register (LVD1CMPCR/ LVD2CMPCR).

Figure 5.2 shows example of operations during voltage monitor 1 and 2 resets. For details on the voltage monitor 1 reset and voltage monitor 2 reset, see section 7, Low Voltage Detection (LVD).



Note: For details on the electrical characteristics, see section 46, Electrical Characteristics.
Note 1. V_{deti} indicates the detection level of a voltage monitor 1 reset and a voltage monitor 2 reset (i = 1, 2).
Note 2. t_{LVDi} indicates the time for a voltage monitor 1 reset and a voltage monitor 2 reset (i = 1, 2).

Figure 5.2 Example of operations during voltage monitor 1 and voltage monitor 2 resets

5.3.4 Deep Software Standby Reset

This is an internal reset generated when deep software standby mode is canceled by an interrupt.

When a deep software standby mode cancelation source is generated, a deep software standby reset is generated. The deep software standby reset is canceled after t_{DSBY} (return time after deep software standby mode cancelation) has elapsed. At the same time, deep software standby mode is also canceled.

When t_{DSBYWT} (wait time after deep software standby mode cancelation) has elapsed after deep software standby mode has been canceled, the internal reset is canceled and the CPU starts the reset exception handling.

For details of the deep software standby reset, see section 10, Low Power Modes.

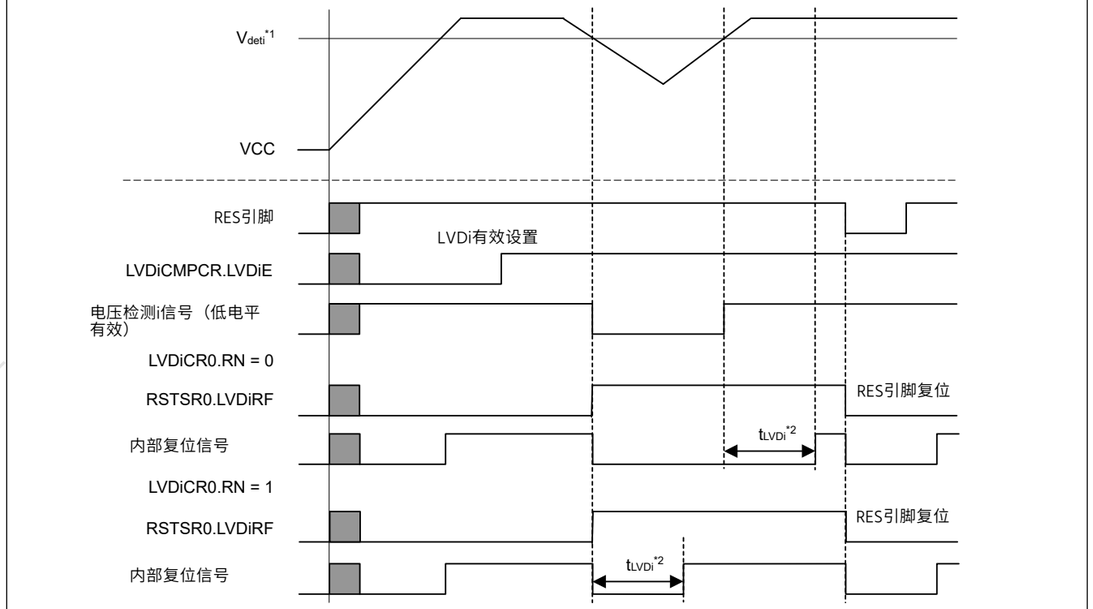
5.3.5 Independent Watchdog Timer Reset

The independent watchdog timer reset is an internal reset generated from the Independent Watchdog Timer (IWDT). Output of the reset from the IWDT can be selected in the Option Function Select Register 0 (OFS0).

同样，从电压监视器2复位状态释放的时间可通过设置电压监视器2复位来选择LDV2CR0寄存器中的取反选择位(RN)。

检测电平Vdet1和Vdet2可以在电压监控比较器控制寄存器(LVD1CMPCR LVD2CMPCR).

图5.2显示了电压监视器1和2复位期间的操作示例。有关电压监视器1复位和电压监视器2复位的详细信息，请参见第7节，低电压检测(LVD)。



Note: 有关电气特性的详细信息，请参见第46节，电气特性。
注1.Vdeti表示电压监视器1复位和电压监视器2复位(i=1 2)的检测电平。
注2.tLVDi表示电压监视器1复位和电压监视器2复位(i=1 2)的时间。

Figure 5.2 电压监控器1和电压监控器2复位期间的操作示例

5.3.4 深度软件待机复位

这是当深度软件待机模式被中断取消时产生的内部复位。

当产生深度软件待机模式取消源时，将产生深度软件待机复位。在经过tDSBY（深度软件待机模式取消后的返回时间）后，深度软件待机复位被取消。同时，深度软件待机模式也被取消。

在深度软件待机模式取消后经过tDSBYWT（深度软件待机模式取消后的等待时间）时，内部复位被取消，CPU开始复位异常处理。

有关深度软件待机复位的详细信息，请参见第10节，低功耗模式。

5.3.5 独立看门狗定时器复位

独立看门狗定时器复位是由独立看门狗定时器（IWDT）产生的内部复位。可以在选项功能选择寄存器0(OFS0)中选择IWDT的复位输出。

When output of the independent watchdog timer reset is selected, the reset is generated if the IWDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (t_{RESW2}) elapses after the independent watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the independent watchdog timer reset, see section 25, Independent Watchdog Timer (IWDT).

5.3.6 Watchdog Timer Reset

The watchdog timer reset is an internal reset generated from the Watchdog Timer (WDT). Output of the reset from the WDT can be selected in the WDT Reset Control Register (WDTRCR) or Option Function Select register 0 (OFS0).

When output of the watchdog timer reset is selected, a watchdog timer reset is generated if the WDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (t_{RESW2}) elapses after the watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the watchdog timer reset, see section 24, Watchdog Timer (WDT).

5.3.7 Software Reset

The software reset is an internal reset generated by a software setting of the SYSRESETREQ bit in the AIRCR register in the Arm core. When the SYSRESETREQ bit is set to 1, a software reset is generated. When the internal reset time (t_{RESW2}) elapses after the software reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the SYSRESETREQ bit, see the *ARM® Cortex®-M33 Technical Reference Manual*.

5.3.8 Determination of Cold/Warm Start

Read the CWSF flag in RSTSR2 to determine the cause of reset processing. This flag indicates whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

The CWSF flag is set to 0 when a power-on reset occurs (cold start), otherwise the flag is not set to 0. The flag is set to 1 when 1 is written to it through software. It is not set to 0 even on writing 0 to it.

Figure 5.3 shows an example of cold/warm start determination operation.

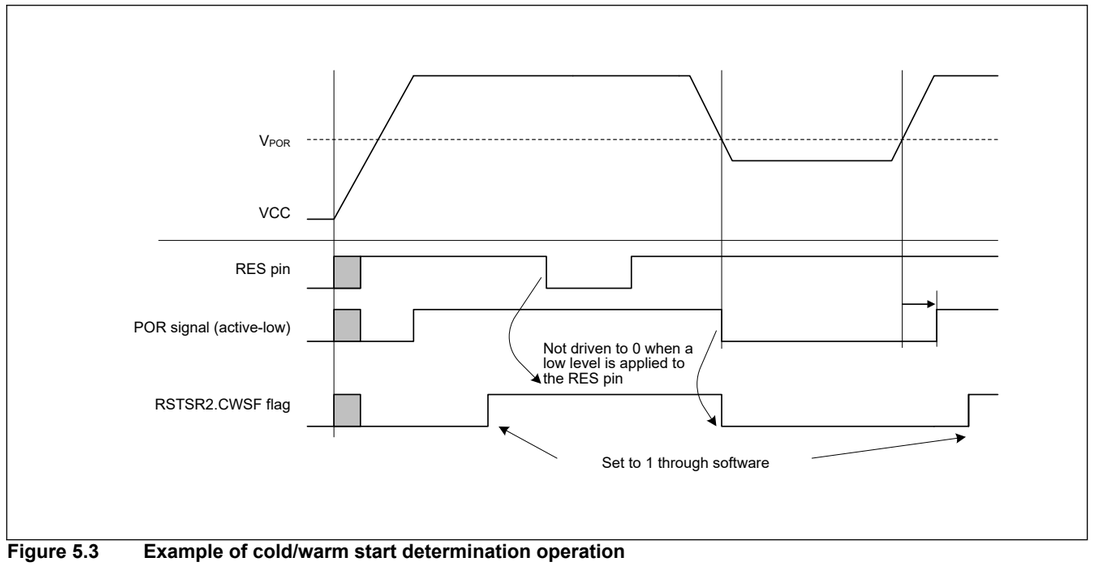


Figure 5.3 Example of cold/warm start determination operation

5.3.9 Determination of Reset Generation Source

Read RSTSR0 and RSTSR1 to determine which reset executes the reset exception handling.

Whenoutputoftheindependentwatchdogtimerresetisselected theresetisgeneratediftheIWDTunderflows orifdataiswrittenwhenrefreshoperationisdisabled.当独立看门狗定时器复位产生后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

有关独立看门狗定时器复位的详细信息，请参见第25节，独立看门狗定时器(IWDT)。

5.3.6 看门狗定时器复位

看门狗定时器复位是由看门狗定时器(WDT)产生的内部复位。WDT的复位输出可以在WDT复位控制寄存器(WDTRCR)或选项功能选择寄存器0(OFS0)中选择。

选择看门狗定时器复位输出时，如果WDT下溢，或者在禁止刷新操作时写入数据，则会产生看门狗定时器复位。在产生看门狗定时器复位后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

有关看门狗定时器复位的详细信息，请参见第24节，看门狗定时器(WDT)。

5.3.7 软件复位

软件复位是通过软件设置Arm内核的AIRCR寄存器中的SYSRESETREQ位产生的内部复位。当SYSRESETREQ位设置为1时，会产生软件复位。当软件复位产生后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

有关SYSRESETREQ位的详细信息，请参阅ARM®Cortex®-M33技术参考手册。

5.3.8 冷暖启动的测定

读取RSTSR2中的CWSF标志以确定复位处理的原因。该标志指示是上电复位导致复位处理（冷启动）还是操作期间输入的复位信号导致复位处理（热启动）。

当发生上电复位（冷启动）时，CWSF标志设置为0，否则该标志不设置为0。当通过软件向其写入1时，该标志设置为1。即使向其写入0，它也不会设置为0。

图5.3显示了冷暖启动确定操作的示例。

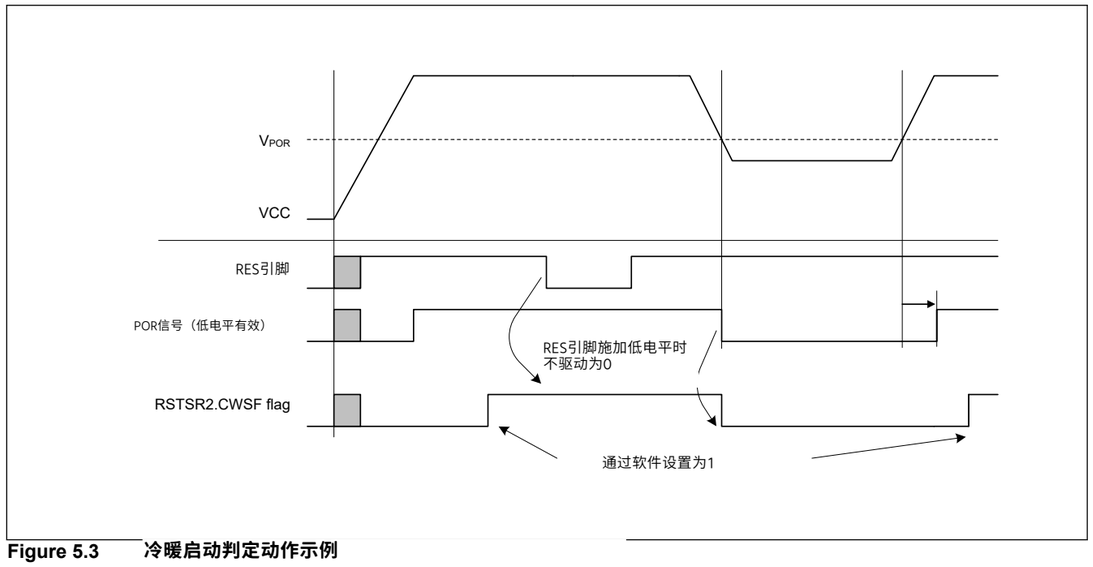
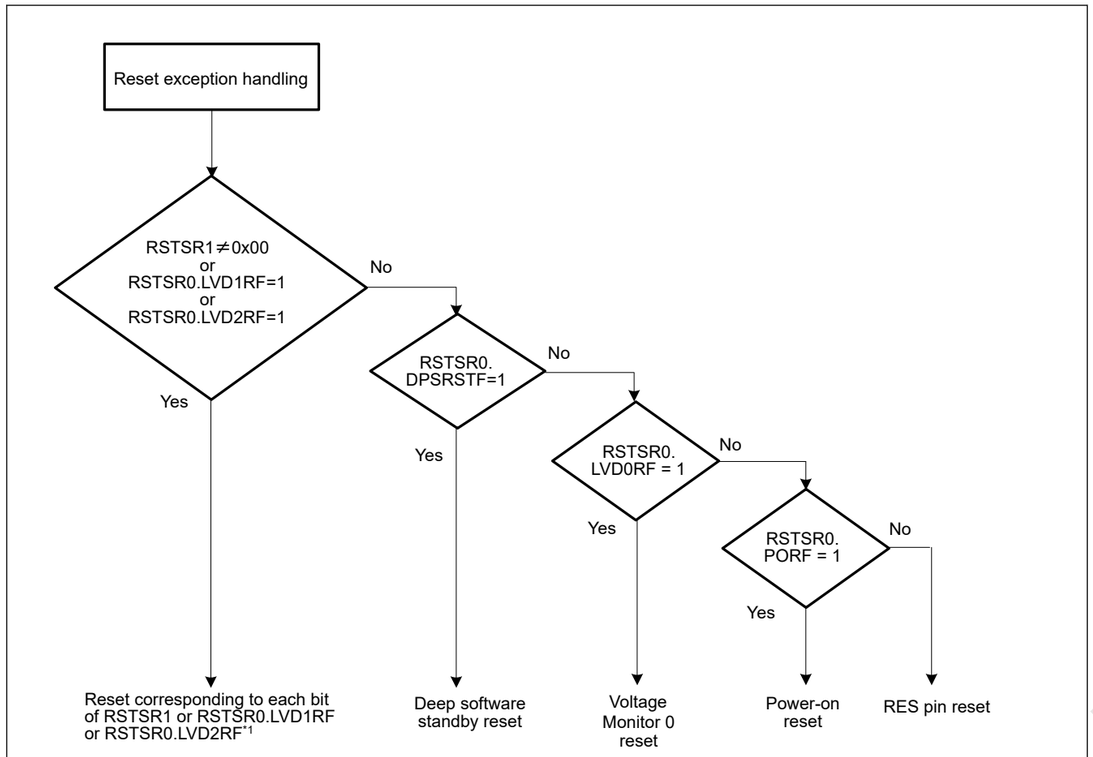


Figure 5.3 冷暖启动判定动作示例

5.3.9 复位产生源的确定

读取RSTSR0和RSTSR1以确定哪个复位执行复位异常处理。

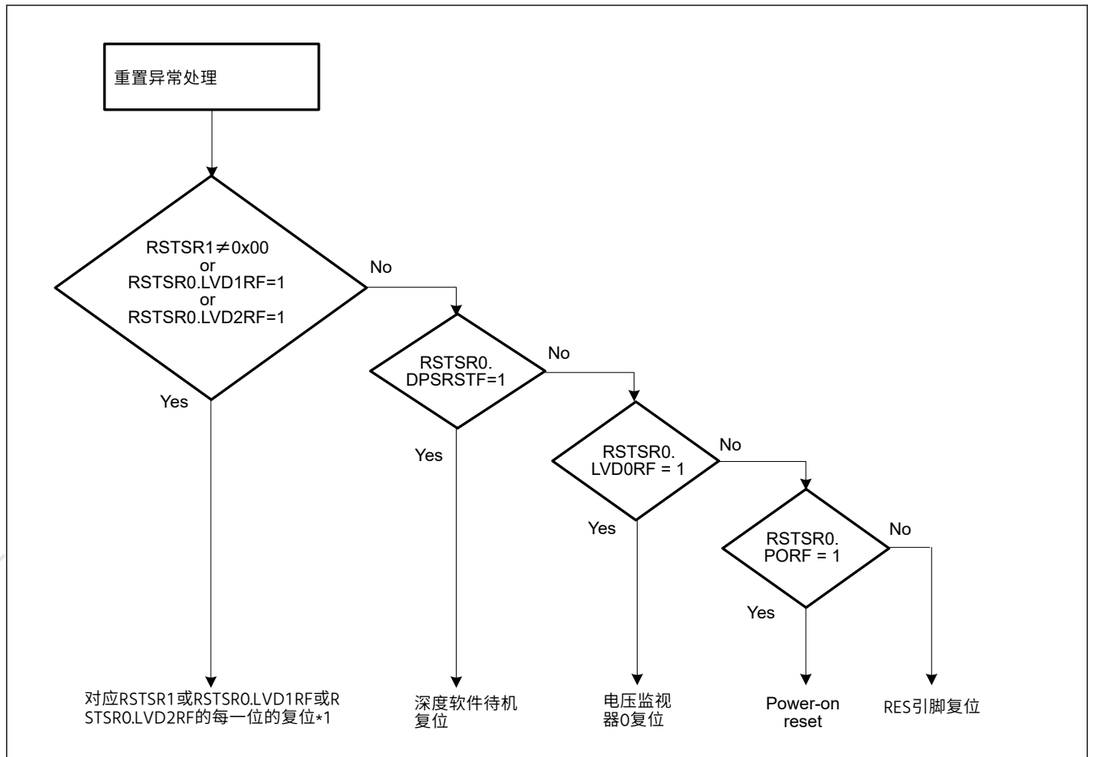
Figure 5.4 shows an example of the flow to identify a reset generation source. The reset flag must be written with 0 after it is read as 1.



Note 1. When resets are generated simultaneously by two or more sources, the two or more corresponding reset flags will be set to 1.

Figure 5.4 Example of reset generation source determination flow

图5.4显示了识别复位产生源的流程示例。复位标志读为1后必须写为0。



注1.当两个或多个源同时产生复位时，两个或多个相应的复位标志将设置为1。

Figure 5.4 复位产生源确定流程示例

6. Option-Setting Memory

6.1 Overview

The option-setting memory determines the state of the MCU after a reset. The option-setting memory is allocated to the configuration setting area of the flash memory.

Figure 6.1 shows the option-setting memory area. The option-setting memory area has secure region. Table 6.1 shows the programming condition of the option-setting memory area.

6. Option-Setting Memory

6.1 Overview

选项设置存储器确定复位后MCU的状态。选项设置内存分配给闪存的配置设置区域。

图6.1显示了选项设置存储区。选项设置内存区域具有安全区域。表6.1显示了选项设置存储区的编程条件。

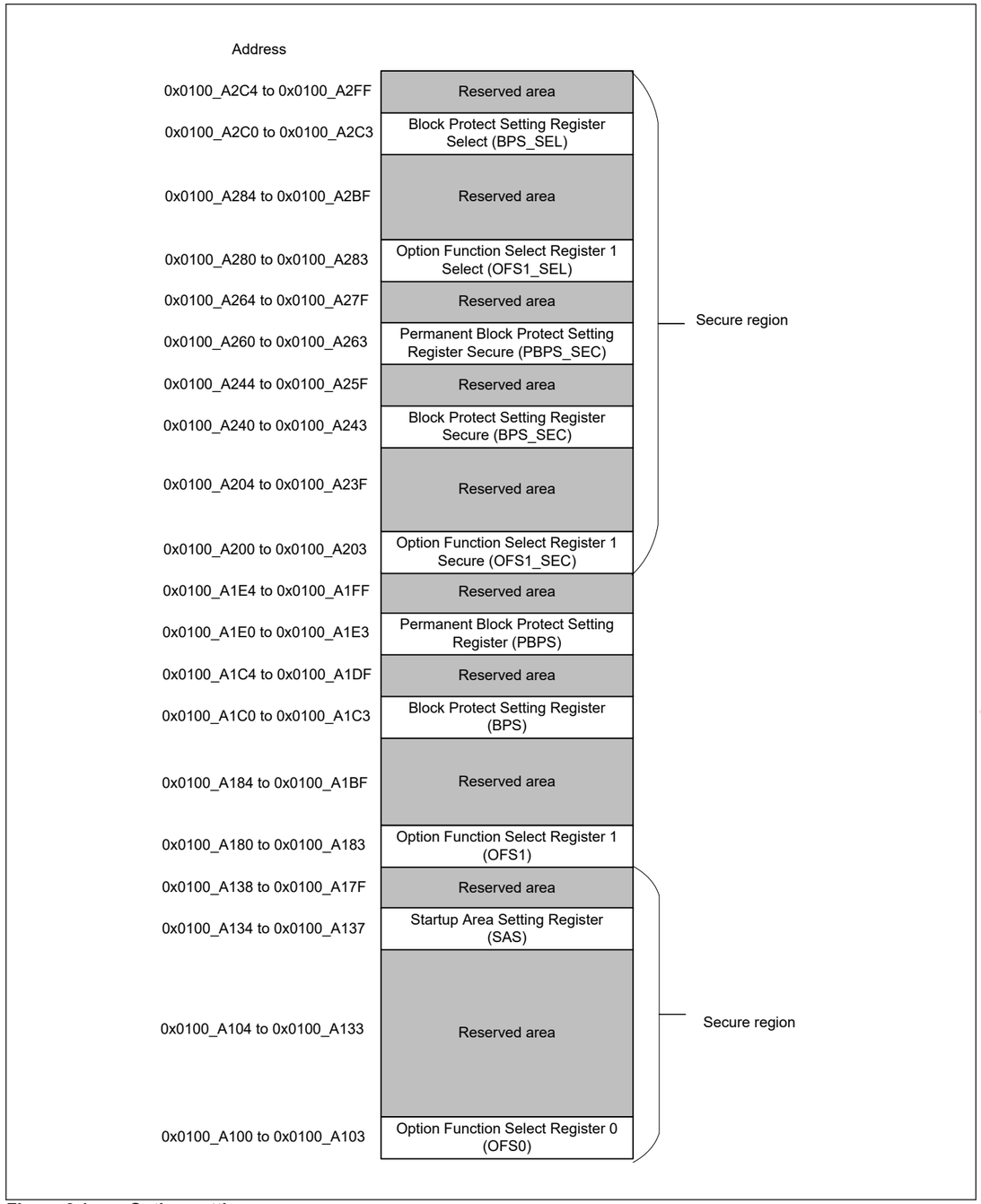


Figure 6.1 Option-setting memory area

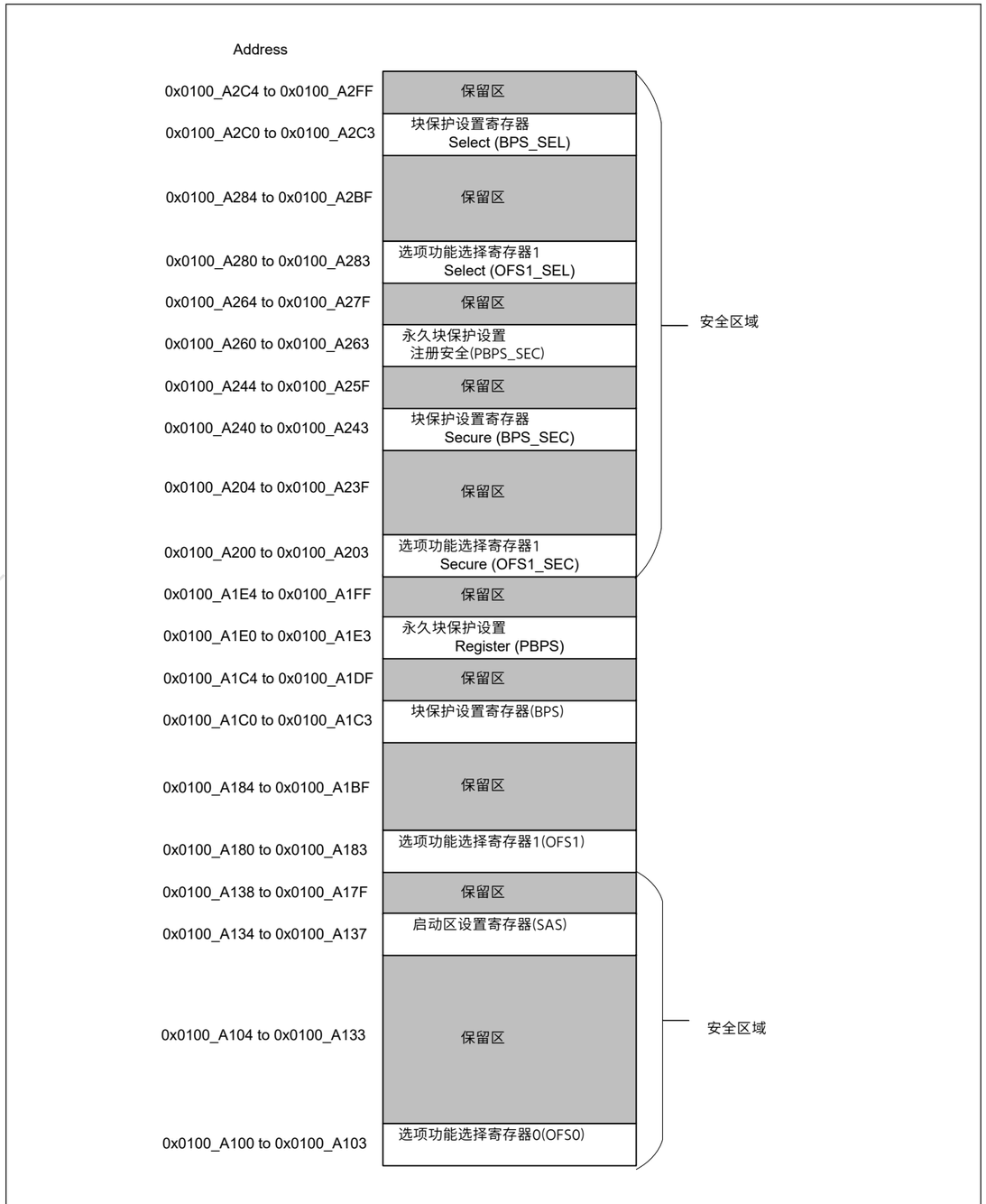


Figure 6.1 选项设置存储区

Table 6.1 The programming condition of the option-setting memory area

	Self programming	Serial programming	Programming by the on-chip debugger
Secure region	Programming commands issued by secure access.	Programming commands issued when the device life cycle is SSD.	Programming commands issued when the debug level is DBG2.
Other region	Programming commands issued by secure or non-secure access.	Programming commands issued when the devise life cycle is SSD or NSECSD.	Programming commands issued when the debug level is DBG2 or DBG1.

6.2 Register Descriptions

6.2.1 OFS0 : Option Function Select Register 0

Address: 0x0100_A100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	WDTSTPCTL	—	WDTRSTIRQS	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTSTRT	—
Value after reset:	User setting*1															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	IWDTSTPCTL	—	IWDTRSTIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTSTRT	—
Value after reset:	User setting*1															

Bit	Symbol	Function	R/W
0	—	When read, this bit returns the written value. The write value should be 1.	R
1	IWDTSTRT	IWDT Start Mode Select 0: Automatically activate IWDT after a reset (auto start mode) 1: Disable IWDT after a reset	R
3:2	IWDTTOPS[1:0]	IWDT Timeout Period Select 0 0: 128 cycles (0x007F) 0 1: 512 cycles (0x01FF) 1 0: 1024 cycles (0x03FF) 1 1: 2048 cycles (0x07FF)	R
7:4	IWDTCKS[3:0]	IWDT-Dedicated Clock Frequency Division Ratio Select 0x0: × 1 0x2: × 1/16 0x3: × 1/32 0x4: × 1/64 0xF: × 1/128 0x5: × 1/256 Others: Setting prohibited	R
9:8	IWDTRPES[1:0]	IWDT Window End Position Select 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (no window end position setting)	R
11:10	IWDTRPSS[1:0]	IWDT Window Start Position Select 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (no window start position setting)	R
12	IWDTRSTIRQS	IWDT Reset Interrupt Request Select 0: Enable non-maskable interrupt request or interrupt request 1: Enable reset	R

Table 6.1 选项设置存储区的编程条件

	自编程	串行编程	通过片上调试器进行编程
安全区域	安全访问发出的编程命令。	设备生命周期为SSD时发出的编程命令。	调试级别为DBG2时发出的编程命令。
其他地区	通过安全或非安全访问发出的编程命令。	设备生命周期为SSD或NSECSD时发出的编程命令。	调试级别为DBG2或DBG1时发出的编程命令。

6.2 注册说明

6.2.1 OFS0：选项功能选择寄存器0

Address: 0x0100_A100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	WDTSTPCTL	—	WDTRSTIRQS	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTSTRT	—
重置后的值：	用户设置*1															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	IWDTSTPCTL	—	IWDTRSTIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTSTRT	—
重置后的值：	用户设置*1															

Bit	Symbol	Function	R/W
0	—	读取时，该位返回写入的值。写入值应为1。	R
1	IWDTSTRT	IWDT启动模式选择 0：复位后自动激活IWDT（自动启动模式）1：复位后禁用IWDT	R
3:2	IWDTTOPS[1:0]	IWDT超时周期选择 0 0: 128 cycles (0x007F) 0 1: 512 cycles (0x01FF) 1 0: 1024 cycles (0x03FF) 1 1: 2048 cycles (0x07FF)	R
7:4	IWDTCKS[3:0]	IWDT-专用时钟分频比选择 0x0: × 1 0x2: × 1/16 0x3: × 1/32 0x4: × 1/64 0xF: × 1/128 0x5: × 1/256 Others: 禁止设定	R
9:8	IWDTRPES[1:0]	IWDT窗口结束位置选择 00：75%01：50%10：25%11：0%（无窗口结束位置设置）	R
11:10	IWDTRPSS[1:0]	IWDT窗口起始位置选择 00：25%01：50%10：75%11：100%（无窗口起始位置设置）	R
12	IWDTRSTIRQS	IWDT复位中断请求选择 0：使能不可屏蔽中断请求或中断请求1：使能复位	R

Bit	Symbol	Function	R/W
13	—	When read, this bit returns the written value. The write value should be 1.	R
14	IWDTSTPCTL	IWDT Stop Control 0: Continue counting 1: Stop counting when in Sleep, Snooze, or Software Standby mode	R
16:15	—	When read, these bits return the written value. The write value should be 1.	R
17	WDTSTRT	WDT Start Mode Select 0: Automatically activate WDT after a reset (auto start mode) 1: Stop WDT after a reset (register start mode)	R
19:18	WDTTOPS[1:0]	WDT Timeout Period Select 0 0: 1024 cycles (0x03FF) 0 1: 4096 cycles (0x0FFF) 1 0: 8192 cycles (0x1FFF) 1 1: 16384 cycles (0x3FFF)	R
23:20	WDTCKS[3:0]	WDT Clock Frequency Division Ratio Select 0x1: PCLKB divided by 4 0x4: PCLKB divided by 64 0xF: PCLKB divided by 128 0x6: PCLKB divided by 512 0x7: PCLKB divided by 2048 0x8: PCLKB divided by 8192 Others: Setting prohibited	R
25:24	WDTRPES[1:0]	WDT Window End Position Select 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (no window end position setting)	R
27:26	WDTRPSS[1:0]	WDT Window Start Position Select 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (no window start position setting)	R
28	WDTRSTIRQS	WDT Reset Interrupt Request Select 0: Enable non-maskable interrupt request or interrupt request 1: Reset	R
29	—	When read, these bits return the written value. The write value should be 1.	R
30	WDTSTPCTL	WDT Stop Control 0: Continue counting 1: Stop counting when entering Sleep mode	R
31	—	When read, these bits return the written value. The write value should be 1.	R

Note 1. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

IWDTSTRT bit (IWDT Start Mode Select)

The IWDTSTRT bit selects the mode in which the IWDT is activated after a reset (stopped state or activated state).

IWDTTOPS[1:0] bits (IWDT Timeout Period Select)

The IWDTTOPS[1:0] bits specify the timeout period, that is, the time it takes for the down counter to underflow, as 128, 512, 1024, or 2048 cycles of the frequency-divided clock set in the IWDTCKS[3:0] bits. The number of clock cycles that the IWDT takes to underflow after a refresh operation is determined by the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits.

For details, see section 25, Independent Watchdog Timer (IWDT).

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the prescaler for dividing the frequency of the clock for the IWDT as 1/1, 1/16, 1/32, 1/64, 1/128, and 1/256. Using this setting combined with the IWDTTOPS[1:0] bits setting, the IWDT counting period can be set from 128 to 524288 IWDT clock cycles.

For details, see section 25, Independent Watchdog Timer (IWDT).

Bit	Symbol	Function	R/W
13	—	读取时，该位返回写入的值。写入值应为1。	R
14	IWDTSTPCTL	IWDT停止控制 0：继续计数1：在休眠、贪睡或软件待机模式下停止计数	R
16:15	—	读取时，这些位返回写入的值。写入值应为1。	R
17	WDTSTRT	WDT启动模式选择 0：复位后自动激活WDT（自动启动模式）1：复位后停止WDT（寄存器启动模式）	R
19:18	WDTTOPS[1:0]	WDT超时周期选择 0 0: 1024 cycles (0x03FF) 0 1: 4096 cycles (0x0FFF) 1 0: 8192 cycles (0x1FFF) 1 1: 16384 cycles (0x3FFF)	R
23:20	WDTCKS[3:0]	WDT时钟分频比选择 0x1：PCLKB4分频0x4：PCLKB64分频0xF：PCLKB128分频 0x6：PCLKB512分频0x7：PCLKB2048分频0x8：PCLKB8192分频 Others: 禁止设定	R
25:24	WDTRPES[1:0]	WDT窗口结束位置选择 00：75%01：50%10：25%11：0%（无窗口结束位置设置）	R
27:26	WDTRPSS[1:0]	WDT窗口起始位置选择 00：25%01：50%10：75%11：100%（无窗口起始位置设置）	R
28	WDTRSTIRQS	WDT复位中断请求选择 0：使能不可屏蔽中断请求或中断请求1：复位	R
29	—	读取时，这些位返回写入的值。写入值应为1。	R
30	WDTSTPCTL	WDT停止控制 0：继续计数1：进入休眠模式时停止计数	R
31	—	读取时，这些位返回写入的值。写入值应为1。	R

注1.空白产品中的值为0xFFFFFFFF。它设置为您的应用程序写入的值。

IWDTSTRT位（IWDT启动模式选择）

IWDTSTRT位选择复位后激活IWDT的模式（停止状态或激活状态）。

IWDTTOPS[1:0]位（IWDT超时周期选择）

IWDTTOPS[1:0]位指定超时周期，即递减计数器下溢所需的时间，为IWDTCKS[3中设置的分频时钟的128、512、1024或2048个周期：0]位。刷新操作后IWDT下溢所需的时钟周期数由IWDTCKS[3:0]和IWDTTOPS[1:0]位的组合决定。

有关详细信息，请参见第25节，独立看门狗定时器(IWDT)。

IWDTCKS[3:0]位（IWDT专用时钟分频比选择）

IWDTCKS[3:0]位指定用于将IWDT的时钟频率分频为11、116、132、164、1128和1256的预分频器的分频比。将此设置与IWDTTOPS[1:0]位设置，IWDT计数周期可以设置为128到524288个IWDT时钟周期。

有关详细信息，请参见第25节，独立看门狗定时器(IWDT)。

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the position where the window for the down counter ends as 0%, 25%, 50%, or 75% of the count value. The value of the window end position must be smaller than the value of the window start position, otherwise only the value for the window start position is valid.

The counter values associated with the settings for the start and end positions of the window in the IWDTRPSS[1:0] and IWDTRPES[1:0] bits vary with the setting in the IWDTTOPS[1:0] bits.

For details, see section 25, Independent Watchdog Timer (IWDT).

IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits specify the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the window starts and ends positions becomes the period in which a refresh is possible. Refresh is not possible outside this period.

For details, see section 25, Independent Watchdog Timer (IWDT).

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit selects the operation on an underflow of the down counter or generation of a refresh error. The operation is selectable to an independent watchdog timer reset, a non-maskable interrupt request, or an interrupt request.

For details, see section 25, Independent Watchdog Timer (IWDT).

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit specifies whether to stop counting when entering Sleep mode, Snooze mode, or Software Standby mode.

For details, see section 25, Independent Watchdog Timer (IWDT).

WDTSTRT bit (WDT Start Mode Select)

The WDTSTRT bit selects the mode in which the WDT is activated after a reset (stopped state or activated in auto start mode). When WDT is activated in auto start mode, the OFS0 register setting for the WDT is valid.

WDTTOPS[1:0] bits (WDT Timeout Period Select)

The WDTTOPS[1:0] bits specify the timeout period, that is, the time it takes for the down counter to underflow as 1024, 4096, 8192, or 16384 cycles of the frequency-divided clock set in the WDTCKS[3:0] bits. The number of PCLKB cycles that takes to underflow after a refresh operation is determined by a combination of the WDTCKS[3:0] and WDTTOPS[1:0] bits.

For details, see section 24, Watchdog Timer (WDT).

WDTCKS[3:0] bits (WDT Clock Frequency Division Ratio Select)

The WDTCKS[3:0] bits specify the division ratio of the prescaler for dividing the frequency of PCLKB as 1/4, 1/64, 1/128, 1/512, 1/2048, and 1/8192. Using this setting combined with the WDTTOPS[1:0] bits setting, the WDT counting period can be set from 4096 to 134217728 PCLKB cycles.

For details, see section 24, Watchdog Timer (WDT).

WDTRPES[1:0] bits (WDT Window End Position Select)

The WDTRPES[1:0] bits specify the position where the window on the down counter ends as 0%, 25%, 50%, or 75% of the counted value. The value of the window end position must be smaller than the value of the window start position, otherwise only the value for the window start position is valid.

The counter values associated with the settings for the start and end positions of the window in the WDTRPSS[1:0] and WDTRPES[1:0] bits vary with the setting of the WDTTOPS[1:0] bits.

For details, see section 24, Watchdog Timer (WDT).

IWDTRPES[1:0]位（IWDT窗口结束位置选择）

IWDTRPES[1:0]位指定递减计数器窗口结束的位置为计数值的0%、25%、50%或75%。窗口结束位置的值必须小于窗口开始位置的值，否则只有窗口开始位置的值有效。

与IWDTRPSS[1:0]中窗口的开始和结束位置的设置相关的计数器值和
IWDTRPES[1:0]位随IWDTTOPS[1:0]位的设置而变化。

有关详细信息，请参见第25节，独立看门狗定时器(IWDT)。

IWDTRPSS[1:0]位（IWDT窗口起始位置选择）

IWDTRPSS[1:0]位指定递减计数器窗口的起始位置为计数值的25%、50%、75%或100%。计数开始点为100%，下溢发生点为0%。窗口开始位置和结束位置之间的间隔成为可以刷新的时间段。在此期间之外无法刷新。

有关详细信息，请参见第25节，独立看门狗定时器(IWDT)。

IWDTRSTIRQS位（IWDT复位中断请求选择）

IWDTRSTIRQS位选择在递减计数器下溢或产生刷新错误时的操作。该操作可选择独立看门狗定时器复位、不可屏蔽中断请求或中断请求。

有关详细信息，请参见第25节，独立看门狗定时器(IWDT)。

IWDTSTPCTL位（IWDT停止控制）

IWDTSTPCTL位指定在进入休眠模式、贪睡模式或软件待机模式时是否停止计数。

有关详细信息，请参见第25节，独立看门狗定时器(IWDT)。

WDTSTRT位（WDT启动模式选择）

WDTSTRT位选择WDT在复位后激活的模式（停止状态或在自动启动模式下激活）。当WDT在自动启动模式下激活时，WDT的OFS0寄存器设置有效。

WDTOPS[1:0]位（WDT超时周期选择）

WDTTOPS[1:0]位指定超时周期，即在WDTCKS[3:0中设置的分频时钟的1024、4096、8192或16384个周期时，递减计数器下溢所需的时间。]位。刷新操作后下溢的PCLKB周期数由WDTCKS[3:0]和WDTTOPS[1:0]位的组合决定。

有关详细信息，请参见第24节，看门狗定时器(WDT)。

WDTCKS[3:0]位（WDT时钟分频比选择）

WDTCKS[3:0]位指定用于分频PCLKB的预分频器的分频比为14、164、1128、1512、12048和18192。将此设置与WDTOPS[1:0]位设置，WDT计数周期可以设置为4096到134217728个PCLKB周期。

有关详细信息，请参见第24节，看门狗定时器(WDT)。

WDTRPES[1:0]位（WDT窗口结束位置选择）

WDTRPES[1:0]位指定递减计数器上窗口结束的位置为计数值的0%、25%、50%或75%。窗口结束位置的值必须小于窗口开始位置的值，否则只有窗口开始位置的值有效。

与WDTRPSS[1:0]中窗口的开始和结束位置设置相关的计数器值和
WDTRPES[1:0]位随WDTTOPS[1:0]位的设置而变化。

有关详细信息，请参见第24节，看门狗定时器(WDT)。

WDTRPSS[1:0] bits (WDT Window Start Position Select)

The WDTRPSS[1:0] bits specify the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the positions where the window starts and ends becomes the period in which a refresh is possible.

Refresh is not possible outside this period.

For details, see section 24, Watchdog Timer (WDT).

WDTRSTIRQS bit (WDT Reset Interrupt Request Select)

The WDTRSTIRQS bit selects the operation on an underflow of the down-counter or generation of a refresh error. The operation is selectable to a watchdog timer reset, a non-maskable interrupt request, or an interrupt request.

For details, see section 24, Watchdog Timer (WDT).

WDTSTPCTL bit (WDT Stop Control)

The WDTSTPCTL bit specifies whether to stop counting when entering Sleep mode.

For details, see section 24, Watchdog Timer (WDT).

6.2.2 SAS : Startup Area Setting Register

Address: 0x0100_A134

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BTFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	User setting															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSPR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	User setting															

Bit	Symbol	Function	R/W
14:0	—	When read, these bits return the written value. The write value should be 1.	R
15	FSPR	Protection of Startup Area Select Function This bit controls the programming of the write/erase protection for the Startup Area Select flag (SAS.BTFLG), and the temporary boot swap control. When this bit is set to 0, it cannot be changed to 1. 0: Executing the configuration setting command for programming the Startup Area Select flag (SAS.BTFLG) is invalid. 1: Executing the configuration setting command for programming the Startup Area Select flag (SAS.BTFLG) is valid.	R
30:16	—	When read, these bits return the written value. The write value should be 1.	R
31	BTFLG	Startup Area Select Flag This bit specifies whether the address of the startup area is exchanged for the boot swap function or not. 0: First 8-KB area (0x0000_0000 to 0x0000_1FFF) and second 8-KB area (0x0000_2000 to 0x0000_3FFF) are exchanged. 1: First 8-KB area (0x0000_0000 to 0x0000_1FFF) and second 8-KB area (0x0000_2000 to 0x0000_3FFF) are not exchanged.	R

WDTRPSS[1:0]位（WDT窗口起始位置选择）

WDTRPSS[1:0]位指定递减计数器窗口的起始位置为计数值的25%、50%、75%或100%。计数开始点为100%，下溢发生点为0%。窗口开始和结束位置之间的间隔成为可以刷新的时间段。

在此期间之外无法刷新。

有关详细信息，请参见第24节，看门狗定时器(WDT)。

WDTRSTIRQS位（WDT复位中断请求选择）

WDTRSTIRQS位选择在递减计数器下溢或产生刷新错误时的操作。该操作可选择看门狗定时器复位、不可屏蔽中断请求或中断请求。

有关详细信息，请参见第24节，看门狗定时器(WDT)。

WDTSTPCTL位（WDT停止控制）

WDTSTPCTL位指定进入休眠模式时是否停止计数。

有关详细信息，请参见第24节，看门狗定时器(WDT)。

6.2.2 SAS：启动区设置寄存器

Address: 0x0100_A134

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BTFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	用户设置															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSPR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	用户设置															

Bit	Symbol	Function	R/W
14:0	—	读取时，这些位返回写入的值。写入值应为1。	R
15	FSPR	保护启动区选择功能 该位控制启动区域选择标志(SAS.BTFLG)的写擦除保护的编程，以及临时引导交换控制。当该位设置为0时，不能更改为1。 0：执行用于编程启动区域选择标志（SAS.BTFLG）的配置设置命令无效。 1：执行用于编程启动区域选择标志（SAS.BTFLG）的配置设置命令有效。	R
30:16	—	读取时，这些位返回写入的值。写入值应为1。	R
31	BTFLG	启动区选择标志 该位指定是否将启动区域的地址交换为引导交换功能。 0：交换第一个8-KB区域（0x0000_0000到0x0000_1FFF）和第二个8-KB区域（0x0000_2000到0x0000_3FFF）。 1：第一个8-KB区域（0x0000_0000到0x0000_1FFF）和第二个8-KB区域（0x0000_2000到0x0000_3FFF）不交换。	R

6.2.3 OFS1, OFS1_SEC, OFS1_SEL : Option Function Select Register 1

Address: OFS1: 0x0100_A180
OFS1_SEC: 0x0100_A200
OFS1_SEL: 0x0100_A280

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	PGADEN[3:0]			
Value after reset:	The value set by the user*1															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	HOCOFRQ0[1:0]		HOCOEN	—	—	—	—	—	LVDAS	VDSEL[1:0]	
Value after reset:	The value set by the user*1															

Bit	Symbol	Function	R/W
1:0	VDSEL[1:0]	Voltage Detection 0 Level Select 0 0: Setting prohibited 0 1: Select 2.94 V 1 0: Select 2.87 V 1 1: Select 2.80 V	R
2	LVDAS	Voltage Detection 0 Circuit Start 0: Enable voltage monitor 0 reset after a reset 1: Disable voltage monitor 0 reset after a reset	R
7:3	—	When read, these bits return the written value. The write value should be 1.	R
8	HOCOEN	HOCO Oscillation Enable 0: Enable HOCO oscillation after a reset 1: Disable HOCO oscillation after a reset	R
10:9	HOCOFRQ0[1:0]	HOCO Frequency Setting 0 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz 1 1: Setting prohibited	R
15:11	—	When read, these bits return the written value. The write value should be 1.	R
19:16	PGADEN[3:0]	PGAn pseudo-differential input Enable (n = 0 to 3) If not set, the pseudo-differential input of PGAn is enabled. Set this bit to 0 when pseudo-differential input to the PGAs is not to be used. 0: After reset, PGAn pseudo-differential input disabled (single-ended input) 1: After reset, PGAn pseudo-differential input enabled	R
31:20	—	When read, these bits return the written value. The write value shoud be 1.	R

Note 1. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

Only secure developer can program OFS1_SEC and OFS1_SEL registers. OFS1_SEC register is for secure developer, and OFS1 register is for non-secure developer. The applied setting value is determined by the setting value of the corresponding bit in OFS1_SEL register. For details, see section 6.3.3. Security attribution of option-setting memory.

VDSEL[1:0] bits (Voltage Detection 0 Level Select)

The VDSEL[1:0] bits select the voltage detection level of the voltage detection 0 circuit.

LVDAS bits (Voltage Detection 0 Circuit Start)

The LVDAS bit selects whether the voltage monitor 0 reset is enabled or disabled after a reset.

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

6.2.3 OFS1、OFS1_SEC、OFS1_SEL：选项功能选择寄存器1

Address: OFS1: 0x0100_A180
OFS1_SEC: 0x0100_A200
OFS1_SEL: 0x0100_A280

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	PGADEN[3:0]			
重置后的值：	用户设置的值*1															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	HOCOFRQ0[1:0]		HOCOEN	—	—	—	—	—	LVDAS	VDSEL[1:0]	
重置后的值：	用户设置的值*1															

Bit	Symbol	Function	R/W
1:0	VDSEL[1:0]	电压检测0电平选择 00：禁止设置01：选择2.94V10：选择2.87V11：选择2.80V	R
2	LVDAS	电压检测0电路启动 0：启用电压监控0复位后复位1：禁用电压监控0复位后复位	R
7:3	—	读取时，这些位返回写入的值。写入值应为1。	R
8	HOCOEN	HOCO振荡使能 0：复位后启用HOCO振荡1：复位后禁用HOCO振荡	R
10:9	HOCOFRQ0[1:0]	HOCO频率设定0 00：16MHz01：18MHz10：20MHz11：禁止设置	R
15:11	—	读取时，这些位返回写入的值。写入值应为1。	R
19:16	PGADEN[3:0]	PGAn伪差分输入使能（n=0至3） 如果未设置，则启用PGAn的伪差分输入。 当不使用PGA的伪差分输入时，将此位设置为0。 0：复位后，PGAn伪差分输入禁止（单端输入）1：复位后，PGAn伪差分输入使能	R
31:20	—	读取时，这些位返回写入的值。写入值应为1。	R

注1.空白产品中的值为0xFFFFFFFF。它设置为您的应用程序写入的值。

只有安全的开发人员才能对OFS1_SEC和OFS1_SEL寄存器进行编程。OFS1_SEC寄存器用于安全开发者，OFS1寄存器用于非安全开发者。应用的设置值由OFS1_SEL寄存器中相应位的设置值决定。详见6.3.3节。选项设置内存的安全属性。

VDSEL[1:0]位（电压检测0电平选择）

VDSEL[1:0]位选择电压检测0电路的电压检测电平。

LVDAS位（电压检测0电路启动）

LVDAS位选择在复位后是启用还是禁用电压监视器0复位。

HOCOEN位（HOCO振荡使能）

HOCOEN位选择在复位后是启用还是禁用HOCO振荡。将此位设置为0允许在CPU开始运行之前启动HOCO振荡，减少了振荡稳定的等待时间。

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFRQ0 bit to an optimum value.

HOCOFRQ0[1:0] bits (HOCO Frequency Setting 0)

The HOCOFRQ0[1:0] bits specify the HOCO frequency after a reset as 16, 18, or 20 MHz.

PGADEN[3:0] bits (PGAn pseudo-differential input Enable)

This bit selects whether the pseudo-differential input on the PGAn pin is enabled or disabled (single-ended input) after a reset.

6.2.4 BPS, BPS_SEC, BPS_SEL : Block Protect Setting Register

address:

BPS: 0x0100_A1C0
BPS_SEC: 0x0100_A240
BPS_SEL: 0x0100_A2C0

Bit position:	31	0
Bit field:		
Value after reset:	User setting*1	

Note 1. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

Only secure developer can program BPS_SEC and BPS_SEL registers. BPS_SEC register is for secure developer, and BPS register is for non-secure developer. The applied setting value is determined by the setting value of the corresponding bit in BPS_SEL register. For details, see section 6.3.3. Security attribution of option-setting memory.

The BPS and BPS_SEC registers invalidate the programming and erasure to the code flash memory. When the bit of this register is set to 0, the programming and erasure to the corresponding block are invalid. Figure 6.2 shows the code flash block structure of each product. Figure 6.3 shows the relationship between the bit of register and the block number. Unused bits are reserved and should be set to 1.

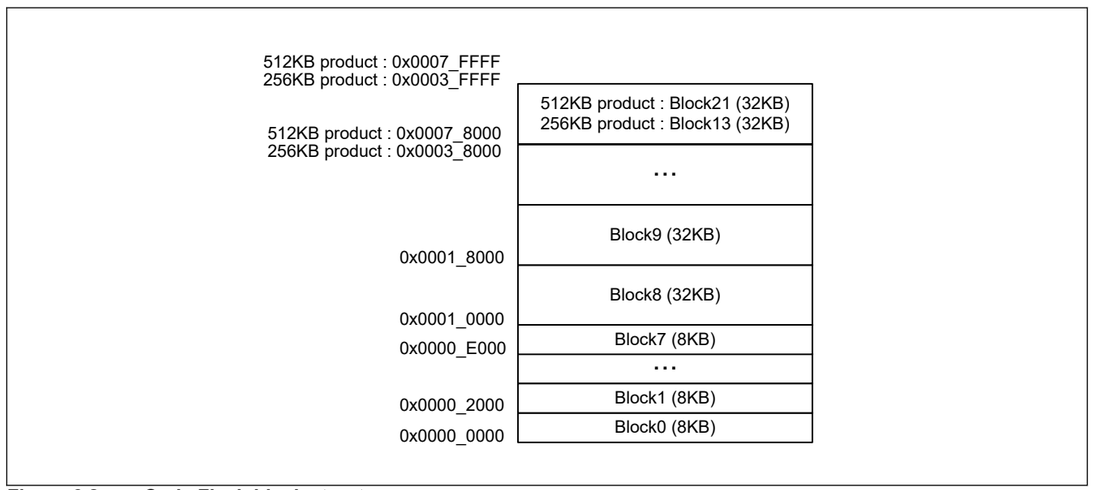


Figure 6.2 Code Flash block structure

Note: 当HOCOEN位设置为0时，系统时钟源不切换到HOCO。系统时钟源只能通过设置时钟源选择位(SCKSCR.CKSEL[2:0])切换到HOCO。要使用HOCO时钟，您必须将OFS1.HOCOFRQ0位设置为最佳值。

HOCOFRQ0[1:0]位（HOCO频率设置0）

HOCOFRQ0[1:0]位指定复位后的HOCO频率为16、18或20MHz。

PGADEN[3:0]位（PGAn伪差分输入使能）

该位选择复位后PGAn引脚上的伪差分输入是启用还是禁用（单端输入）。

6.2.4 BPS、BPS_SEC、BPS_SEL：块保护设置寄存器

address:

BPS: 0x0100_A1C0
BPS_SEC: 0x0100_A240
BPS_SEL: 0x0100_A2C0

Bit position:	31	0
Bit field:		
重置后的值：	用户设置*1	

注1.空白产品中的值为0xFFFFFFFF。它设置为您的应用程序写入的值。

只有安全的开发人员才能对BPS_SEC和BPS_SEL寄存器进行编程。BPS_SEC寄存器用于安全开发者，BPS寄存器用于非安全开发者。应用的设置值由BPS_SEL寄存器中相应位的设置值决定。详见6.3.3节。选项设置内存的安全属性。

BPS和BPS_SEC寄存器使对代码闪存的编程和擦除无效。当该寄存器的位设置为0时，对相应块的编程和擦除无效。图6.2显示了每个产品的代码闪存块结构。图6.3显示了寄存器的位和块号之间的关系。未使用的位被保留，应设置为1。

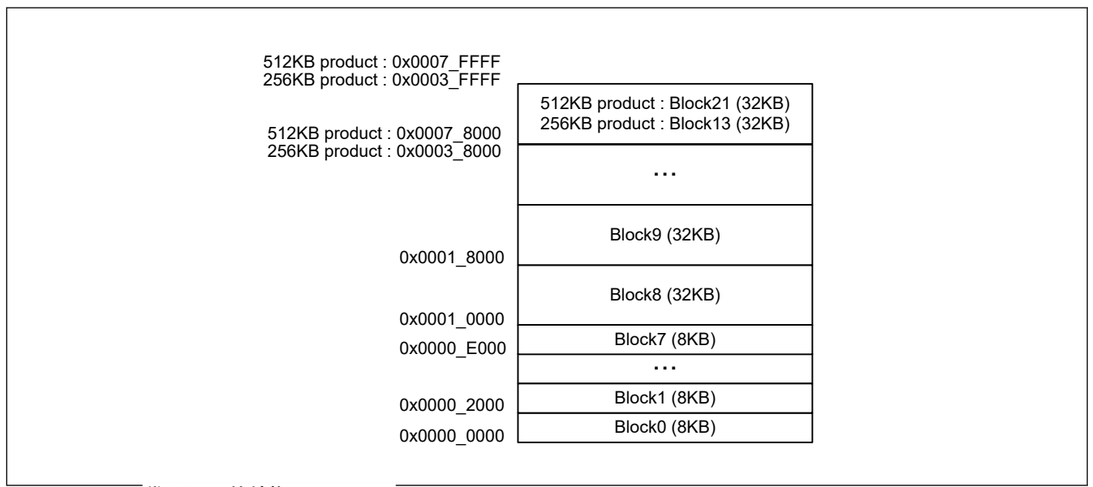


Figure 6.2 代码Flash块结构

Regiser	Address	+31	+30	+29	+28	+27	+26	+25	+24	+23	+22	+21	+20	+19	+18	+17	+16	+15	+14	+13	+12	+11	+10	+ 9	+ 8	+ 7	+ 6	+ 5	+ 4	+ 3	+ 2	+ 1	+ 0
BPS_SEL	0x0100_A2C0											21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	⋮																																
BPS_SEC	0x0100_A240											21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	⋮																																
BPS	0x0100_A1C0											21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 6.3 The relationship between the bit of register and the block number

6.2.5 PBPS, PBPS_SEC : Permanent Block Protect Setting Register

Address: PBPS: 0x0100_A1E0
PBPS_SEC: 0x0100_A260

Bit position:	31																															0
Bit field:																																
Value after reset:	User setting*1																															

Note 1. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

Only secure developer can program PBPS_SEC register. PBPS_SEC register is for secure developer, and PBPS register is for non-secure developer. The applied setting value is determined by the setting value of the corresponding bit in BPS_SEL register. For details, see section 6.3.3. Security attribution of option-setting memory. The security attribution register is same BPS_SEL register between the block protection and permanent block protection.

The PBPS and PBPS_SEC registers invalidate writes to bits of BPS and BPS_SEC. The bit of this register can be set to 0 when corresponding bit of BPS and BPS_SEC is set to 0. When the bit of this register is set to 0, writing the corresponding bit of BPS and BPS_SEC register is invalid. Once the bit of this register is set to 0, it is impossible to change the bit to 1.

Table 6.2 shows the relationship between the bit of applied PBPS and bit of applied BPS.

The relationship between the bit of this register and the block number is same as BPS and BPS_SEC registers (section 6.2.4. BPS, BPS_SEC, BPS_SEL : Block Protect Setting Register). Unused bits are reserved and should be set to 1.

Table 6.2 The relationship between the bit of PBPS, PBPS_SEC and bit of BPS, BPS_SEC

The bit of applied PBPS	The bit of applied BPS	Content
1	1	Programming and erasure to the corresponding block is valid.
1	0	Programming and erasure to the corresponding block is invalid. This protection can be canceled by FBPROT0 or FBPROT1 registers.
0	1	Can not set this condition
0	0	Programming and erasure to the corresponding block is invalid permanently

6.3 Setting Option-Setting Memory

6.3.1 Allocation of Data in Option-Setting Memory

Programming data is allocated to the addresses in the option-setting memory shown in Figure 6.1. The allocated data is used by tools such as a flash programming software or an on-chip debugger.

Note: Programming formats vary depending on the compiler. See the compiler manual for details.

6.3.2 Setting Data for Programming Option-Setting Memory

Allocating data according to the procedure described in section 6.3.1. Allocation of Data in Option-Setting Memory, alone does not actually write the data to the option-setting memory. You must also follow one of the actions described in this section.

Regiser	Address	+31	+30	+29	+28	+27	+26	+25	+24	+23	+22	+21	+20	+19	+18	+17	+16	+15	+14	+13	+12	+11	+10	+ 9	+ 8	+ 7	+ 6	+ 5	+ 4	+ 3	+ 2	+ 1	+ 0
BPS_SEL	0x0100_A2C0											21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	⋮																																
BPS_SEC	0x0100_A240											21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	⋮																																
BPS	0x0100_A1C0											21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 6.3 寄存器位与块号的关系

6.2.5 PBPS PBPS_SEC:永久块保护设置寄存器

Address: PBPS: 0x0100_A1E0
PBPS_SEC: 0x0100_A260

Bit position:	31																															0
Bit field:																																
重置后的值:	用户设置*1																															

注1.空白产品中的值为0xFFFFFFFF。它设置为您的应用程序写入的值。

只有安全的开发人员才能对PBPS_SEC寄存器进行编程。PBPS_SEC寄存器用于安全开发者，PBPS寄存器用于非安全开发者。应用的设置值由BPS_SEL寄存器中相应位的设置值决定。详见6.3.3节。选项设置内存的安全属性。安全属性寄存器与块保护和永久块保护之间的BPS_SEL寄存器相同。

PBPS和PBPS_SEC寄存器使对BPS和BPS_SEC位的写入无效。当BPS和BPS_SEC的对应位设置为0时，该寄存器的位可以设置为0。当该寄存器的位设置为0时，写入BPS和BPS_SEC寄存器的对应位无效。一旦该寄存器的位设置为0，就无法将该位更改为1。表6.2显示了应用PBPS位和应用BPS位之间的关系。

该寄存器的位与块号的关系与BPS和BPS_SEC寄存器相同（第6.2.4节）。
BPS、BPS_SEC、BPS_SEL：块保护设置寄存器）。未使用的位被保留，应设置为1。

Table 6.2 PBPS、PBPS_SEC的位与BPS、BPS_SEC的位的关系

应用PBPS的位	应用BPS的点滴	Content
1	1	对相应块的编程和擦除是有效的。
1	0	对相应块的编程和擦除无效。该保护可以通过FBPROT0或FBPROT1寄存器取消。
0	1	不能设置这个条件
0	0	对相应块的编程和擦除永久无效

6.3 设置选项设置内存

6.3.1 选项设置内存中的数据分配

编程数据被分配到图6.1所示的选项设置存储器中的地址。分配的数据由闪存编程软件或片上调试器等工具使用。

Note: 编程格式因编译器而异。有关详细信息，请参阅编译器手册。

6.3.2 编程选项设置存储器的设置数据

根据第6.3.1节中描述的程序分配数据。选项设置内存中的数据分配，单独并不实际将数据写入选项设置内存。您还必须遵循本节中描述的操作之一。

(1) Changing the option-setting memory by self-programming

Use the configuration setting command to write data to the option-setting memory in the configuration setting area.

The option-setting memory does not support background operations (BGO). When write the option-setting memory, jump to SRAM after copying writing softwere to SRAM.

For details of the configuration setting command, see section 43, Flash Memory.

(2) Debugging through an OCD or programming by a flash writer

This procedure depends on the tool in use, see the tool manual for details.

The MCU provides two setting procedures:

- Read the data allocated as described in section 6.3.1. Allocation of Data in Option-Setting Memory, from an object file or Motorola S-format file generated by the compiler, and write the data to the MCU
- Use the GUI interface of the tool to program the same data as allocated in section 6.3.1. Allocation of Data in Option-Setting Memory.

6.3.3 Security attribution of option-setting memory

Some functionality has 3 registers for non-secure (FUNC NAME), and secure (FUNC NAME_SEC), and security attribution (FUNC NAME_SEL). Only secure developer can set the registers for secure and security attribution. As shown in Figure 6.4, when the bit of security attribution register is set to 0, the corresponding bit of secure register is applied. When the bit of security attribution register is set to 1, the corresponding bit of non-secure register is applied.

For example, if the secure developer wants to configure LVD of OFS1 as secure, HOCO and PGA of OFS1 as non-secure, the secure developer needs to set OFS1_SEL as follows.

OFS1_SEL = 0xFFFF_FFF8

By this setting, LVDAS and VDSEL[1:0] values of OFS1_SEC and HOCOFRQ0[1:0], HOCOEN and PGADEN[3:0] values of OFS1 are applied to MCU. The reserved bits of the security attribution register (FUNC NAME_SEL) should be set to 1.

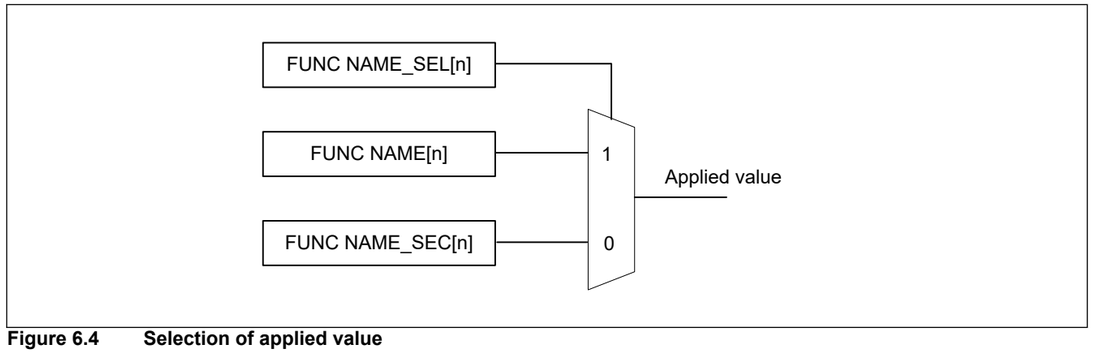


Figure 6.4 Selection of applied value

6.3.4 Timing of the Setting Value

For SAS, BPS, BPS_SEC, PBPS, and PBPS_SEC registers, the setting value of the related startup area and block protection is applied immediately after programming. For other registers, the setting value is applied after the MCU is reset.

In case the programming using the serial programming mode in customer's factory, be careful that the block protection for secure user is applied after MCU is reset. Because initial value of the security attribution registers of block protection (BPS_SEL) is 1 (non-secure), the block protection setting for secure developer (BPS_SEC/PBPS_SEC) is not applied until MCU is reset even if the corresponding bit of BPS_SEL is programmed to 0 (secure).

(1) 通过自编程更改选项设置存储器

使用配置设置命令将数据写入配置设置区的选项设置内存。

选项设置内存不支持后台操作(BGO)。写入选项设置内存时，跳转到
将写入软件复制到SRAM后的SRAM。

有关配置设置命令的详细信息，请参见第43节，闪存。

(2) 通过OCD进行调试或通过闪存写入器进行编程

此过程取决于所使用的工具，详细信息请参见工具手册。

MCU提供两种设置程序：

●读取第6.3.1节所述分配的数据。在选项设置内存中分配数据，从编译器生成的目标文件或摩托罗拉S格式文件，并将数据写入MCU

●使用工具的GUI界面对6.3.1节分配的相同数据进行编程。OptionSetting内存中的数据分配。

6.3.3 选项设置内存的安全属性

某些功能具有3个用于非安全(FUNCNAME)、安全(FUNCNAME_SEC)和安全属性(FUNCNAME_SEL)的寄存器。只有安全的开发人员才能设置安全和安全属性的寄存器。如图6.4所示，当安全属性寄存器的位设置为0时，应用安全寄存器的相应位。当安全属性寄存器的位设置为1时，应用非安全寄存器的相应位。

例如，如果安全开发者要将OFS1的LVD配置为安全，将OFS1的HOCO和PGA配置为非安全，则安全开发者需要如下设置OFS1_SEL。

OFS1_SEL = 0xFFFF_FFF8

通过此设置，OFS1_SEC的LVDAS和VDSEL[1:0]值和OFS1的HOCOFRQ0[1:0]、HOCOEN和PGADEN[3:0]值应用于MCU。安全属性寄存器(FUNCNAME_SEL)的保留位应设置为1。

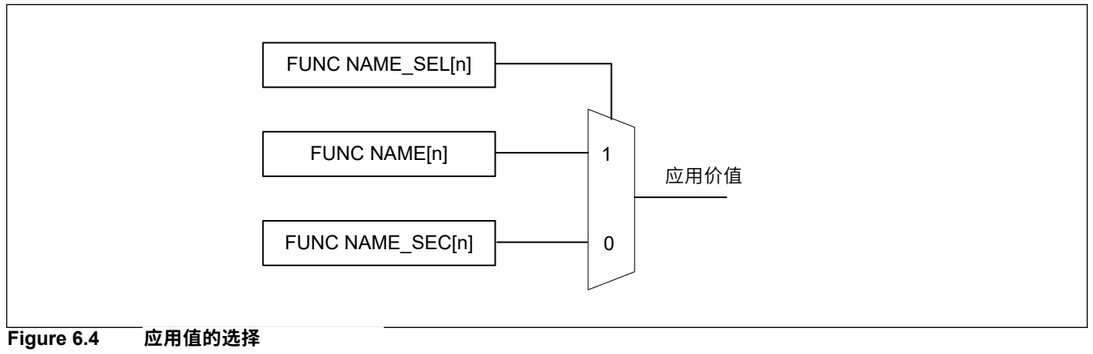


Figure 6.4 应用值的选择

6.3.4 设定值的时机

对于SAS、BPS、BPS_SEC、PBPS和PBPS_SEC寄存器，编程后立即应用相关启动区域和块保护的设置值。对于其他寄存器，设置值在MCU复位后应用。

如果在客户工厂使用串行编程模式进行编程，请注意在MCU复位后应用安全用户的块保护。由于块保护(BPS_SEL)的安全属性寄存器的初始值为1（非安全），因此即使BPS_SEL的相应位被编程为0（安全）。

6.4 Usage Notes

6.4.1 Data for Programming Reserved Areas and Reserved Bits in the Option-Setting Memory

When reserved areas and reserved bits in the option-setting memory are within the scope of programming, write 1 to all bits of reserved areas and all reserved bits. If 0 is written to these bits, normal operation cannot be guaranteed.

6.4 使用说明

6.4.1 用于编程选项设置中的保留区域和保留位的数据 Memory

当期权设置内存中的保留区域和保留位在编程范围内时，将1写入保留区域和所有保留位的所有位。如果将0写入这些位，则无法保证正常操作。

7. Low Voltage Detection (LVD)

7.1 Overview

The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.

Voltage monitor registers are used to configure the LVD to trigger an interrupt, event link output, or reset when the thresholds are crossed.

Table 7.1 lists the LVD specifications. Figure 7.1 shows a block diagram of the voltage monitor 0 reset generation circuit. Figure 7.2 shows a block diagram of the voltage monitor 1 interrupt and reset circuit, and Figure 7.3 shows a block diagram of the voltage monitor 2 interrupt and reset circuit.

Table 7.1 LVD specifications

Parameter		Voltage monitor 0	Voltage monitor 1	Voltage monitor 2
Means for setting up operation		OFS1 register	Registers	Registers
Target for monitoring		VCC pin input voltage	VCC pin input voltage	VCC pin input voltage
Monitored voltage		V_{det0}	V_{det1}	V_{det2}
Detected event		Voltage falls past V_{det0}	Voltage rises or falls past V_{det1}	Voltage rises or falls past V_{det2}
Detection voltage		Selectable from 3 different levels in the OFS1.VDSEL[1:0] bits	Selectable from 3 different levels in the LVD1CMPCR.LVD1LVL[4:0] bits	Selectable from 3 different levels in the LVD2CMPCR.LVD2LVL[2:0] bits
Monitoring flag		None	LVD1SR.MON flag: Monitors whether voltage is higher or lower than V_{det1}	LVD2SR.MON flag: Monitors whether voltage is higher or lower than V_{det2}
			LVD1SR.DET flag: V_{det1} passage detection	LVD2SR.DET flag: V_{det2} passage detection
Process on voltage detection	Reset	Voltage monitor 0 reset	Voltage monitor 1 reset	Voltage monitor 2 reset
		Reset when V_{det0} > VCC CPU restart after specified time with VCC > V_{det0}	Reset when V_{det1} > VCC CPU restart timing selectable: after specified time with VCC > V_{det1} or V_{det1} > VCC	Reset when V_{det2} > VCC CPU restart timing selectable: after specified time with either VCC > V_{det2} or V_{det2} > VCC
	Interrupt	No interrupt	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Non-maskable or maskable interrupt selectable	Non-maskable or maskable interrupt selectable
			Interrupt request issued when V_{det1} > VCC and VCC > V_{det1} or either	Interrupt request issued when V_{det2} > VCC and VCC > V_{det2} or either
Digital filter	Switching between enable and disable	No digital filter function	Available	Available
	Sampling time	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		None	Available Output of event signals on detection of V_{det1} crossings	Available Output of event signals on detection of V_{det2} crossings
TrustZone Filter		—	Security attribution can be set for each registers	

7. 低电压检测(LVD)

7.1 Overview

低电压检测(LVD)模块监控输入到VCC引脚的电压电平。检测等级可以通过寄存器设置来选择。LVD模块由三个独立的电压电平检测器（LVD0、LVD1、LVD2）组成。LVD0、LVD1和LVD2测量输入到VCC引脚的电压电平。LVD寄存器允许您的应用程序配置在各种电压阈值下检测VCC变化。

电压监控寄存器用于配置LVD，以在超过阈值时触发中断、事件链接输出或复位。

表7.1列出了LVD规格。图7.1显示了电压监视器0复位产生电路的框图。
图7.2显示了电压监视器1中断和复位电路的框图，图7.3显示了电压监视器2中断和复位电路的框图。

Table 7.1 LVD specifications

Parameter		电压监视器0	电压监视器1	电压监测器2
设置操作的方法		OFS1 register	Registers	Registers
监测目标		VCC引脚输入电压	VCC引脚输入电压	VCC引脚输入电压
监控电压		V_{det0}	V_{det1}	V_{det2}
检测到的事件		电压下降超过Vdet0	电压上升或下降超过Vdet1	电压上升或下降超过Vdet2
检测电压		可从OFS1.VDSEL[1:0]位的3个不同级别中选择	可从LVD1CMPCR.LVD1LVL[4:0]位中的3个不同级别中选择	可从LVD2CMPCR.LVD2LVL[2:0]位中的3个不同级别中选择
监控标志		None	LVD1SR.MON标志：监控电压是高于还是低于Vdet1	LVD2SR.MON标志：监控电压是高于还是低于Vdet2
			LVD1SR.DET标志：Vdet1通过检测	LVD2SR.DET标志：Vdet2通过检测
电压检测流程	Reset	电压监控器0复位	电压监视器1复位	电压监视器2复位
		当Vdet0>VCC时复位 CPU在VCC>Vdet0指定时间后重启	当Vdet1>VCC时复位 CPU重启时间可选：在VCC>Vdet1或Vdet1>VCC的指定时间后	当Vdet2>VCC时复位 CPU重启时间可选：在VCC>Vdet2或Vdet2>VCC的指定时间后
	Interrupt	无中断	电压监视器1中断	电压监视器2中断
			可选择不可屏蔽或可屏蔽中断	可选择不可屏蔽或可屏蔽中断
			当Vdet1>时发出中断请求 VCC和VCC>Vdet1或	当Vdet2>VCC和VCC>Vdet2或任一时发出中断请求
数字滤波器	在启用和禁用之间切换	无数字滤波功能	Available	Available
	采样时间	—	1nLOCO频率×2(n:2 4 8 16)	1nLOCO频率×2(n:2 4 8 16)
事件链接功能		None	Available 在检测到Vdet1交叉点时输出事件信号	Available 在检测到Vdet2交叉点时输出事件信号
TrustZone Filter		—	可以为每个寄存器设置安全属性	

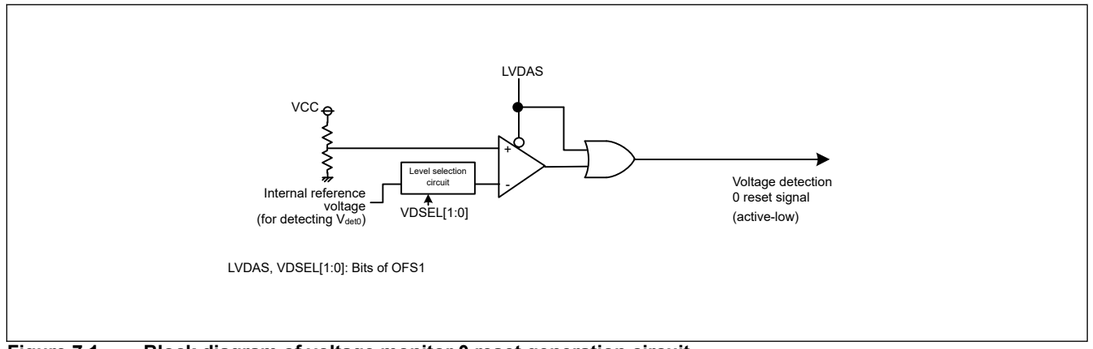


Figure 7.1 Block diagram of voltage monitor 0 reset generation circuit

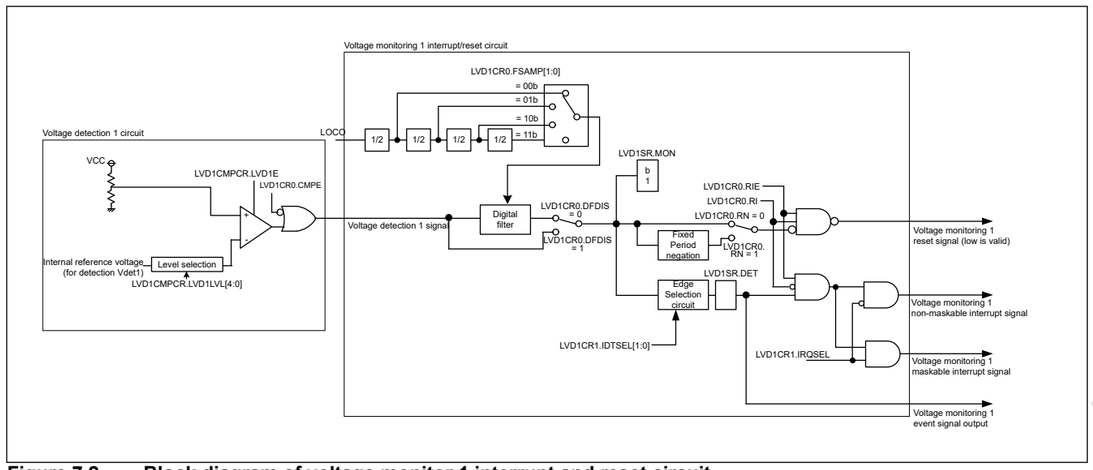


Figure 7.2 Block diagram of voltage monitor 1 interrupt and reset circuit

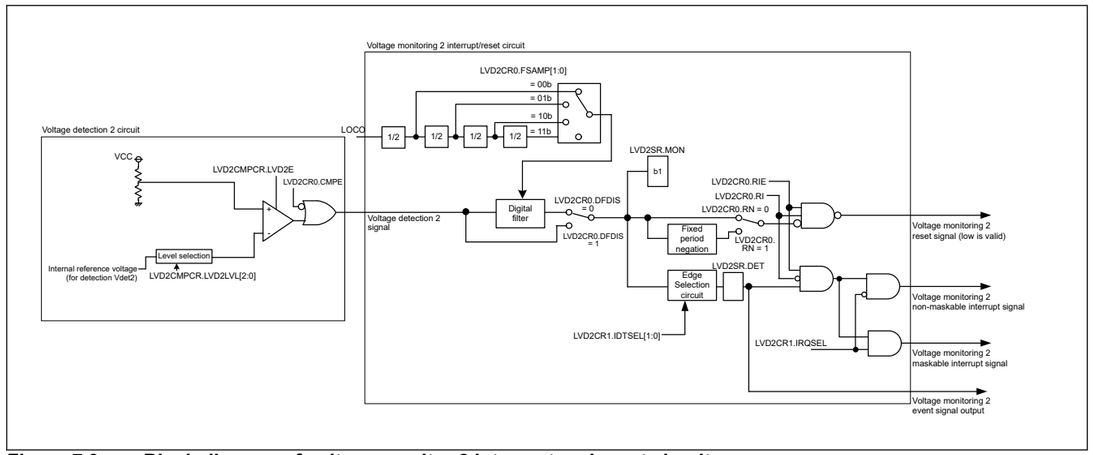


Figure 7.3 Block diagram of voltage monitor 2 interrupt and reset circuit

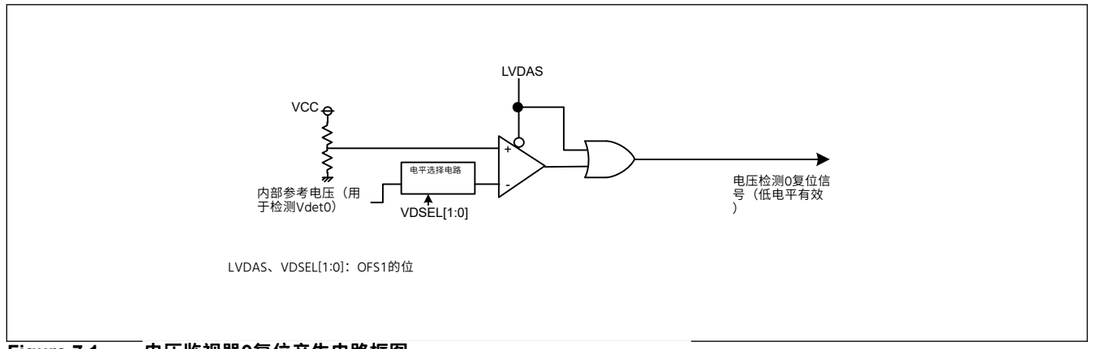


Figure 7.1 电压监视器0复位产生电路框图

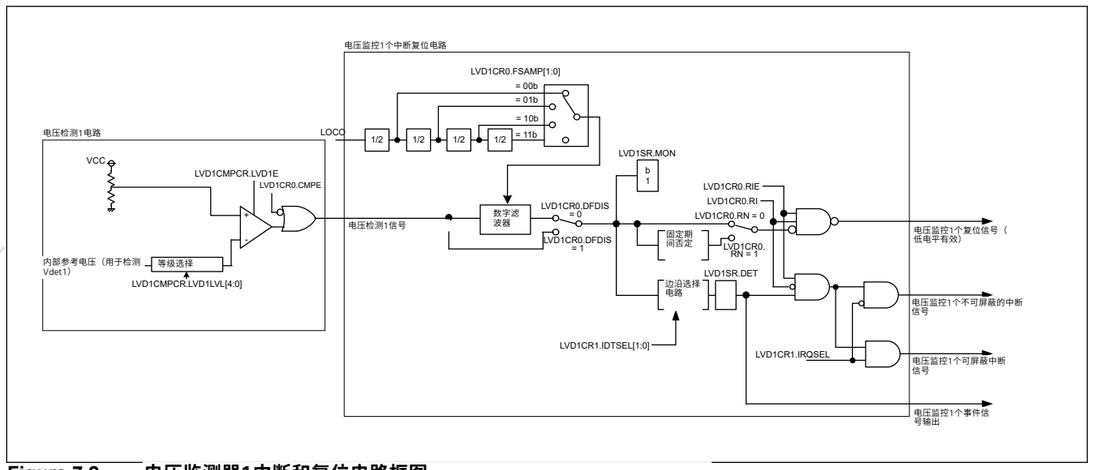


Figure 7.2 电压监测器1中断和复位电路框图

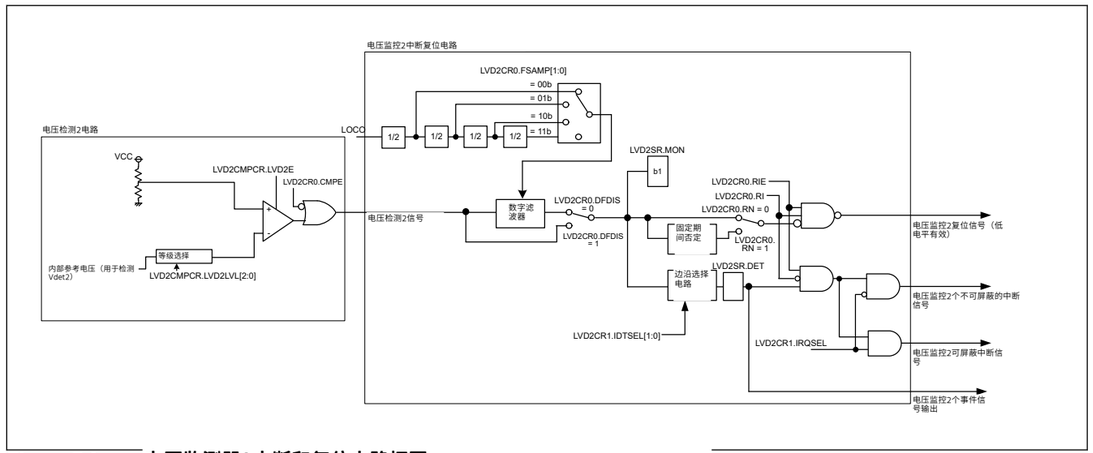


Figure 7.3 电压监测器2中断和复位电路框图

7.2 Register Descriptions

7.2.1 LVDSAR : Low Voltage Detection Security Attribution Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3CC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC1	NONSEC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0	Non Secure Attribute bit 0 Target register: registers for LVD1 0: Secure 1: Non Secure	R/W
1	NONSEC1	Non Secure Attribute bit 1 Target register: registers for LVD2 0: Secure 1: Non Secure	R/W
31:2	—	These bits are read as 1. The write value must be 1 when it is possible to write.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

The LVDSAR register controls the secure attribute of LVD registers.

NONSEC0 bit (Non Secure Attribute bit 0)

This bit controls the security attribute of LVD1CMPCR, LVD1CR0, LVD1CR1, LVD1SR.

NONSEC1 bit (Non Secure Attribute bit 1)

This bit controls the security attribute of LVD2CMPCR, LVD2CR0, LVD2CR1, LVD2SR.

7.2.2 LVD1CMPCR : Voltage Monitoring 1 Comparator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x417

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LVD1E	—	—	LVD1LVL[4:0]				
Value after reset:	0	0	0	1	0	0	1	1

Bit	Symbol	Function	R/W
4:0	LVD1LVL[4:0]	Voltage Detection 1 Level Select (Standard voltage during drop in voltage) 0x11: 2.99 V (Vdet1_11) 0x12: 2.92 V (Vdet1_12) 0x13: 2.85 V (Vdet1_13) Others: Setting prohibited	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W

7.2 注册说明

7.2.1 LVDSAR：低电压检测安全属性寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x3CC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC1	NONSEC0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0	非安全属性位0 目标寄存器：LVD1的寄存器 0：安全1：不 安全	R/W
1	NONSEC1	非安全属性位1 目标寄存器：LVD2的寄存器 0：安全1：不 安全	R/W
31:2	—	这些位被读取为1。当可以写入时，写入值必须为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

LVDSAR寄存器控制LVD寄存器的安全属性。

NONSEC0位（非安全属性位0）

该位控制LVD1CMPCR、LVD1CR0、LVD1CR1、LVD1SR的安全属性。

NONSEC1位（非安全属性位1）

该位控制LVD2CMPCR、LVD2CR0、LVD2CR1、LVD2SR的安全属性。

7.2.2 LVD1CMPCR:电压监测1比较器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x417

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LVD1E	—	—	LVD1LVL[4:0]				
重置后的值：	0	0	0	1	0	0	1	1

Bit	Symbol	Function	R/W
4:0	LVD1LVL[4:0]	电压检测1电平选择（电压下降时的标准电压） 0x11: 2.99 V (Vdet1_11) 0x12: 2.92 V (Vdet1_12) 0x13: 2.85 V (Vdet1_13) 其他：禁止设置	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
7	LVD1E	Voltage Detection 1 Enable 0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

The LVD1CMPCR.LVD1LVL can be changed only if the LVD1CMPCR.LVD1E and LVD2CMPCR.LVD2E bits are both 0. The voltage detection circuits 1 and 2 should not be set at the same voltage detection level.

Please do not change LVD1CMPCR.LVD1LVL and LVD1CMPCR.LVD1E at the same time.

LVD1E bit (Voltage Detection 1 Enable)

When using voltage detection 1 interrupt/reset or the LVD1SR.MON bit, set the LVD1E bit to 1. The voltage detection 1 circuit starts once td(E-A) passes after the LVD1E bit value is changed from 0 to 1. When using the voltage detection 1 circuit in deep software standby mode, do not set the DPSBYCR.DEEPCUT[1:0] bits to 11b.

7.2.3 LVD2CMPCR : Voltage Monitoring 2 Comparator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x418

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LVD2E	—	—	—	—	LVD2LVL[2:0]		
Value after reset:	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
2:0	LVD2LVL[2:0]	Voltage Detection 2 Level Select (Standard voltage during drop in voltage) 1 0 1: 2.99 V (Vdet2_5) 1 1 0: 2.92 V (Vdet2_6) 1 1 1: 2.85 V (Vdet2_7) Others: Setting prohibited	R/W
6:3	—	These bits are read as 0. The write value should be 0.	R/W
7	LVD2E	Voltage Detection 2 Enable 0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

The LVD2CMPCR.LVD2LVL can be changed only if the LVD1CMPCR.LVD1E and LVD2CMPCR.LVD2E bits are both 0. The voltage detection circuits 1 and 2 should not be set at the same voltage detection level.

Do not change LVD2CMPCR.LVD2LVL and LVD2CMPCR.LVD2E at the same time.

LVD2E bit (Voltage Detection 2 Enable)

When using voltage detection 2 interrupt/reset or the LVD2SR.MON bit, set the LVD2E bit to 1. The voltage detection 2 circuit starts once td(E-A) passes after the LVD2E bit value is changed from 0 to 1. When using the voltage detection 2 circuit in deep software standby mode, do not set the DPSBYCR.DEEPCUT[1:0] bits to 11b.

Bit	Symbol	Function	R/W
7	LVD1E	电压检测1使能 0：电压检测1电路无效1：电压检测1电路有效	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

LVD1CMPCR.LVD1LVL只有在LVD1CMPCR.LVD1E和LVD2CMPCR.LVD2E位均为0时才能更改。电压检测电路1和2不应设置为相同的电压检测电平。

请不要同时更改LVD1CMPCR.LVD1LVL和LVD1CMPCR.LVD1E。

LVD1E位（电压检测1使能）

使用电压检测1中断复位或LVD1SR.MON位时，将LVD1E位设置为1。LVD1E位值从0变为1后，一旦经过td(E-A)，电压检测1电路就会启动。使用电压检测时1电路处于深度软件待机模式，请勿将DPSBYCR.DEEPCUT[1:0]位设置为11b。

7.2.3 LVD2CMPCR:电压监测2比较器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x418

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LVD2E	—	—	—	—	LVD2LVL[2:0]		
重置后的值:	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
2:0	LVD2LVL[2:0]	电压检测2电平选择（电压下降时的标准电压） 1 0 1: 2.99 V (Vdet2_5) 1 1 0: 2.92 V (Vdet2_6) 1 1 1: 2.85 V (Vdet2_7) 其他：禁止设置	R/W
6:3	—	这些位被读取为0。写入值应为0。	R/W
7	LVD2E	电压检测2使能 0：电压检测2电路无效1：电压检测2电路有效	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

LVD2CMPCR.LVD2LVL只有在LVD1CMPCR.LVD1E和LVD2CMPCR.LVD2E位均为0时才能更改。电压检测电路1和2不应设置为相同的电压检测电平。

不要同时更改LVD2CMPCR.LVD2LVL和LVD2CMPCR.LVD2E。

LVD2E位（电压检测2使能）

使用电压检测2中断复位或LVD2SR.MON位时，将LVD2E位设置为1。LVD2E位值从0变为1后，一旦经过td(E-A)，电压检测2电路就会启动。使用电压检测时2电路处于深度软件待机模式，请勿将DPSBYCR.DEEPCUT[1:0]位设置为11b。

7.2.4 LVD1CR0 : Voltage Monitor 1 Circuit Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x41A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
Value after reset:	1	0	0	0	x	0	1	0

Bit	Symbol	Function	R/W
0	RIE	Voltage Monitor 1 Interrupt/Reset Enable 0: Disable 1: Enable	R/W
1	DFDIS	Voltage monitor 1 Digital Filter Disabled Mode Select 0: Enable the digital filter 1: Disable the digital filter	R/W
2	CMPE	Voltage Monitor 1 Circuit Comparison Result Output Enable 0: Disable voltage monitor 1 circuit comparison result output 1: Enable voltage monitor 1 circuit comparison result output	R/W
3	—	The read value is undefined. The write value should be 1.	R/W
5:4	FSAMP[1:0]	Sampling Clock Select 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency	R/W
6	RI	Voltage Monitor 1 Circuit Mode Select 0: Generate voltage monitor 1 interrupt on V_{det1} crossing 1: Enable voltage monitor 1 reset when the voltage falls to and below V_{det1}	R/W
7	RN	Voltage Monitor 1 Reset Negate Select 0: Negate after a stabilization time (t_{LVD1}) when VCC > V_{det1} is detected 1: Negate after a stabilization time (t_{LVD1}) on assertion of the LVD1 reset	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

RIE bit (Voltage Monitor 1 Interrupt/Reset Enable)

The RIE bit enables or disables voltage monitor 1 interrupt/reset. Ensure that neither a voltage monitor 1 interrupt nor a voltage monitor 1 reset is generated during programming or erasure of the flash memory.

DFDIS bit (Voltage monitor 1 Digital Filter Disabled Mode Select)

The DFDIS bit disables the digital filter circuit. Set the LOCOCR.LCSTP bit to 0 (the LOCO operates) when this bit is 0(enabled). Set this bit to 1 (disabled) when using the voltage monitor 1 circuit in Software Standby mode or in Deep Software Standby mode.

CMPE bit (Voltage Monitor 1 Circuit Comparison Result Output Enable)

The CMPE bit enables or disables voltage monitor 1 circuit comparison result output. Set the CMPE bit to 1 after the voltage detection 1 circuit enables and stabilization time ($t_{d(E-A)}$) elapses. When stopping the voltage detection 1 circut, disable the voltage detection 1 circuit after setting the CMPE bit is 0.

FSAMP[1:0] bits (Sampling Clock Select)

The FSAMP[1:0] bits can be rewritten only when the LVD1CR0.DFDIS bit is 1 (digital filter circuit disabled). Do not rewrite these bits if the LVD1CR0.DFDIS bit is 0 (digital filter circuit enabled).

7.2.4 LVD1CR0：电压监视器1电路控制寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x41A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
重置后的值：	1	0	0	0	x	0	1	0

Bit	Symbol	Function	R/W
0	RIE	电压监视器1中断复位使能 0：禁用1 ：启用	R/W
1	DFDIS	电压监视器1数字滤波器禁用模式选择 0：启用数字滤波器1：禁用数字滤波器	R/W
2	CMPE	电压监视器1电路比较结果输出使能 0：禁止电压监视1电路比较结果输出1：使能电压监视1电路比较结果输出	R/W
3	—	读取值未定义。写入值应为1。	R/W
5:4	FSAMP[1:0]	采样时钟选择 00:12LOCO频率01:14LOCO频率10:18LOCO频率11:116LOCO频率	R/W
6	RI	电压监视器1电路模式选择 0：在Vdet1交叉时产生电压监视器1中断1：当电压下降到或低于Vdet1时使能电压监视器1复位	R/W
7	RN	电压监视器1复位否定选择 0：在检测到VCC>Vdet1时在稳定时间(tLVD1)后取反1：在LVD1复位有效时在稳定时间(tLVD1)后取反	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

RIE位（电压监视器1中断复位使能）

RIE位启用或禁用电压监视器1中断复位。确保在对闪存进行编程或擦除期间，既不会产生电压监视器1中断，也不会产生电压监视器1复位。

DFDIS位（电压监视器1数字滤波器禁用模式选择）

DFDIS位禁用数字滤波器电路。当该位为0（启用）时，将LOCOCR.LCSTP位设置为0（LOCO运行）。在软件待机模式或深度软件待机模式下使用电压监视器1电路时，将此位设置为1（禁用）。

CMPE位（电压监视器1电路比较结果输出使能）

CMPE位启用或禁用电压监视器1电路比较结果输出。在电压检测1电路使能并经过稳定时间(td(E-A))后，将CMPE位设置为1。停止电压检测1电路时，将CMPE位设置为0后禁用电压检测1电路。

FSAMP[1:0]位（采样时钟选择）

只有当LVD1CR0.DFDIS位为1（数字滤波器电路禁用）时，FSAMP[1:0]位才能被重写。如果LVD1CR0.DFDIS位为0（启用数字滤波器电路），请勿重写这些位。

RI bit (Voltage Monitor 1 Circuit Mode Select)

When the RI bit is 1 (voltage monitor 1 reset selected), transition to Deep Software Standby mode cannot be made. In this case, transition to Software Standby mode is made. To enter Deep Software Standby mode, set the RI bit to 0 (voltage monitor 1 interrupt selected).

RN bit (Voltage Monitor 1 Reset Negate Select)

If the RN bit is set to 1 (negation follows a stabilization time on assertion of the LVD1 reset signal), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). In addition, for a transition to Software Standby or Deep Software Standby mode, the only possible value for the RN bit is 0 (negation follows stabilization time when VCC > V_{det1} is detected). Do not set the RN bit to 1 when this is the case.

7.2.5 LVD2CR0 : Voltage Monitor 2 Circuit Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x41B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
Value after reset:	1	0	0	0	x	0	1	0

Bit	Symbol	Function	R/W
0	RIE	Voltage Monitor 2 Interrupt/Reset Enable 0: Disable 1: Enable	R/W
1	DFDIS	Voltage monitor 2 Digital Filter Disabled Mode Select 0: Enable the digital filter 1: Disable the digital filter	R/W
2	CMPE	Voltage Monitor 2 Circuit Comparison Result Output Enable 0: Disable voltage monitor 2 circuit comparison result output 1: Enable voltage monitor 2 circuit comparison result output	R/W
3	—	The read value is undefined. The write value should be 1.	R/W
5:4	FSAMP[1:0]	Sampling Clock Select 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency	R/W
6	RI	Voltage Monitor 2 Circuit Mode Select 0: Generate voltage monitor 2 interrupt on V_{det2} crossing 1: Enable voltage monitor 2 reset when the voltage falls to and below V_{det2}	R/W
7	RN	Voltage Monitor 2 Reset Negate Select 0: Negate after a stabilization time (t_{LVD2}) when VCC > V_{det2} is detected 1: Negate after a stabilization time (t_{LVD2}) on assertion of the LVD2 reset	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

RIE bit (Voltage Monitor 2 Interrupt/Reset Enable)

The RIE bit enables or disables the voltage monitor 2 interrupt/reset. Ensure that neither a voltage monitor 2 interrupt nor a voltage monitor 2 reset is generated during programming or erasure of the flash memory.

RI位（电压监视器1电路模式选择）

当RI位为1（选择电压监视器1复位）时，无法转换到深度软件待机模式。在这种情况下，将转换到软件待机模式。要进入深度软件待机模式，请将RI位设置为0（选择电压监视器1中断）。

RN位（电压监视器1复位否定选择）

如果RN位设置为1（否定遵循LVD1复位信号断言的稳定时间），设置LOCOCR.LCSTP位为0（LOCO运行）。此外，为了转换到软件待机或深度软件待机模式，RN位的唯一可能值为0（当检测到VCC>Vdet1时，取反跟随稳定时间）。在这种情况下，请勿将RN位设置为1。

7.2.5 LVD2CR0：电压监视器2电路控制寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x41B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
重置后的值：	1	0	0	0	x	0	1	0

Bit	Symbol	Function	R/W
0	RIE	电压监视器2中断复位使能 0：禁用1 ：启用	R/W
1	DFDIS	电压监视器2数字滤波器禁用模式选择 0：启用数字滤波器1：禁用数字滤波器	R/W
2	CMPE	电压监视器2电路比较结果输出使能 0：禁止电压监视2电路比较结果输出1：使能电压监视2电路比较结果输出	R/W
3	—	读取值未定义。写入值应为1。	R/W
5:4	FSAMP[1:0]	采样时钟选择 00:12LOCO频率01:14LOCO频率10:18LOCO频率11:116LOCO频率	R/W
6	RI	电压监视器2电路模式选择 0：在Vdet2交叉时产生电压监视器2中断1：当电压下降到或低于Vdet2时使能电压监视器2复位	R/W
7	RN	电压监视器2复位否定选择 0：在检测到VCC>Vdet2时在稳定时间(tLVD2)后取反1：在LVD2复位有效时在稳定时间(tLVD2)后取反	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

RIE位（电压监视器2中断复位使能）

RIE位启用或禁用电压监视器2中断复位。确保在对闪存进行编程或擦除期间，既不会产生电压监视器2中断，也不会产生电压监视器2复位。

DFDIS bit (Voltage monitor 2 Digital Filter Disabled Mode Select)

The DFDIS bit disables the digital filter circuit. Set the LOCOCR.LCSTP bit to 0 (the LOCO operates) when this bit is 0 (digital filter enabled). Set this bit to 1 (digital filter disabled) when using the voltage monitor 2 circuit in Software Standby mode or in Deep Software Standby mode.

CMPE bit (Voltage Monitor 2 Circuit Comparison Result Output Enable)

The CMPE bit enables or disables voltage monitor 2 circuit comparison result output. Set the CMPE bit to 1 after the voltage detection 2 circuit enables and stabilization time ($t_{d(E-A)}$) elapses. When stopping the voltage detection 2 circut, disable the voltage detection 2 circuit after setting the CMPE bit is 0.

FSAMP[1:0] bits (Sampling Clock Select)

The FSAMP[1:0] bits can be rewritten only when the LVD2CR0.DFDIS bit is 1 (digital filter circuit disabled). Do not rewrite these bits if the LVD2CR0.DFDIS bit is 0 (digital filter circuit enabled).

RI bit (Voltage Monitor 2 Circuit Mode Select)

When the RI bit is 1 (voltage monitor 2 reset selected), transition to Deep Software Standby mode cannot be made. In this case, transition to Software Standby mode is made. To enter Deep Software Standby mode, set the RI bit to 0 (voltage monitor 2 interrupt selected).

RN bit (Voltage Monitor 2 Reset Negate Select)

If the RN bit is set to 1 (negating LVD2 reset in a specified time after its assertion), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). Additionally, for a transition to Software Standby or Deep Software Standby mode, the only possible value for the RN bit is 0 (negation follows a stabilization time when VCC > V_{det2} is detected). Do not set the RN bit to 1 (negation follows a stabilization time after assertion of the LVD2 reset signal) when this is the case.

7.2.6 LVD1CR1 : Voltage Monitor 1 Circuit Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0E0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	IDTSEL[1:0]	Voltage Monitor 1 Interrupt Generation Condition Select 0 0: When VCC ≥ V_{det1} (rise) is detected 0 1: When VCC < V_{det1} (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited	R/W
2	IRQSEL	Voltage Monitor 1 Interrupt Type Select 0: Non-maskable interrupt 1: Maskable interrupt*1	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (writing enabled) before rewriting this register.

Note 1. When enabling maskable interrupts, do not change the NMIER.LVD1EN bit value in the ICU from the reset state.

DFDIS位（电压监视器2数字滤波器禁用模式选择）

DFDIS位禁用数字滤波器电路。当该位为0（启用数字滤波器）时，将LOCOCR.LCSTP位设置为0（LOCO运行）。在软件待机模式或深度软件待机模式下使用电压监视器2电路时，将此位设置为1（禁用数字滤波器）。

CMPE位（电压监视器2电路比较结果输出使能）

CMPE位启用或禁用电压监视器2电路比较结果输出。在电压检测2电路使能且稳定时间(td(E-A))过后，将CMPE位设置为1。停止电压检测2电路时，将CMPE位设置为0后禁用电压检测2电路。

FSAMP[1:0]位（采样时钟选择）

只有当LVD2CR0.DFDIS位为1（数字滤波器电路禁用）时，FSAMP[1:0]位才能被重写。如果LVD2CR0.DFDIS位为0（启用数字滤波器电路），请勿重写这些位。

RI位（电压监视器2电路模式选择）

当RI位为1（选择电压监视器2复位）时，无法转换到深度软件待机模式。在这种情况下，将转换到软件待机模式。要进入深度软件待机模式，请将RI位设置为0（选择电压监视器2中断）。

RN位（电压监视器2复位否定选择）

如果RN位设置为1（在其断言后的指定时间内否定LVD2复位），则将LOCOCR.LCSTP位设置为0（LOCO运行）。此外，为了转换到软件待机或深度软件待机模式，RN位的唯一可能值是0（当检测到VCC>Vdet2时，取反遵循稳定时间）。在这种情况下，请勿将RN位设置为1（在LVD2复位信号置位后的稳定时间之后取反）。

7.2.6 LVD1CR1：电压监视器1电路控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0E0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	IDTSEL[1:0]	电压监视器1中断发生条件选择 00：检测到VCC≥Vdet1（上升）时01：检测到VCC<Vdet1（下降）时10：检测到下降和上升时11：禁止设置	R/W
2	IRQSEL	电压监视器1中断类型选择 0: Non-maskable interrupt 1: Maskable interrupt*1	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

注1.当使能可屏蔽中断时，不要从复位状态更改ICU中的NMIER.LVD1EN位值。

7.2.7 LVD1SR : Voltage Monitor 1 Circuit Status Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0E1

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
0	DET	Voltage Monitor 1 Voltage Variation Detection Flag 0: Not detected 1: V_{det1} crossing is detected	R/W*1
1	MON	Voltage Monitor 1 Signal Monitor Flag 0: VCC < V_{det1} 1: VCC ≥ V_{det1} or MON is disabled	R
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

Note 1. Only 0 can be written to this bit. After writing 0 to this bit, 2 system clock cycles are required for the bit to be read as 0.

DET flag (Voltage Monitor 1 Voltage Variation Detection Flag)

The DET flag is enabled when the LVD1CMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

When detecting V_{det1}, set the DET flag to 0 after setting LVD1CR0.RIE is 0 (disabled). When setting LVD1CR0.RIE bit to 1 (enabled) after setting it to 0, wait for 2 or more PCLKB cycles which have elapsed.

MON flag (Voltage Monitor 1 Signal Monitor Flag)

The MON flag is enabled when the LVD1CMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

7.2.8 LVD2CR1 : Voltage Monitor 2 Circuit Control Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x0E2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	IDTSEL[1:0]	Voltage Monitor 2 Interrupt Generation Condition Select 0 0: When VCC ≥ V_{det2} (rise) is detected 0 1: When VCC < V_{det2} (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited	R/W
2	IRQSEL	Voltage Monitor 2 Interrupt Type Select 0: Non-maskable interrupt 1: Maskable interrupt*1	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

7.2.7 LVD1SR:电压监视器1电路状态寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0E1

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MON	DET
重置后的值:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
0	DET	电压监视器1电压变化检测标志 0：未检测到1：检测到Vdet 1交叉	R/W*1
1	MON	电压监视器1信号监视器标志 0：VCC<Vdet11：VCC≥Vdet1或M ON被禁用	R
7:2	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
- 允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

注1.该位只能写入0。向该位写入0后，需要2个系统时钟周期才能将该位读为0。

DET标志（电压监视器1电压变化检测标志）

当LVD1CMPCR.LVD1E位为1（使能电压检测1电路）且
LVD1CR0.CMPE位为1（电压监视器1电路比较结果输出使能）。

检测Vdet1时，将LVD1CR0.RIE设置为0（禁用）后，将DET标志设置为0。在将LVD1CR0.RIE位设置为0后将其设置为1（启用）时，等待2个或更多PCLKB周期已过去。

MON标志（电压监控1信号监控标志）

当LVD1CMPCR.LVD1E位为1（使能电压检测1电路）且
LVD1CR0.CMPE位为1（电压监视器1电路比较结果输出使能）。

7.2.8 LVD2CR1：电压监视器2电路控制寄存器1

Base address: SYSC = 0x4001_E000

Offset address: 0x0E2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	IDTSEL[1:0]	电压监视器2中断发生条件选择 00：检测到VCC≥Vdet2（上升）时01： 检测到VCC<Vdet2（下降）时10：检测到 下降和上升时11：禁止设置	R/W
2	IRQSEL	电压监视器2中断类型选择 0: Non-maskable interrupt 1: Maskable interrupt*1	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (writing enabled) before rewriting this register.
Note 1. When enabling maskable interrupts, do not change the NMIER.LVD2EN bit value in the ICU from the reset state.

7.2.9 LVD2SR : Voltage Monitor 2 Circuit Status Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0E3

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
0	DET	Voltage Monitor 2 Voltage Variation Detection Flag 0: Not detected 1: V_{det2} crossing is detected	R/W*1
1	MON	Voltage Monitor 2 Signal Monitor Flag 0: VCC < V_{det2} 1: VCC ≥ V_{det2} or MON is disabled	R
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, 2 system clock cycles are required for the bit to be read as 0.

DET flag (Voltage Monitor 2 Voltage Variation Detection Flag)

The DET flag is enabled when the LVD2CMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.CMPE bit is 1 (voltage monitor 2 circuit comparison result output enabled).

Set the DET flag to 0 after setting LVD2CR0.RIE is 0 (disabled). When setting LVD2CR0.RIE bit to 1 (enabled) after setting it to 0, wait for 2 or more PCLKB cycles which have elapsed.

MON flag (Voltage Monitor 2 Signal Monitor Flag)

The MON flag is enabled when the LVD2CMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.CMPE bit is 1 (voltage monitor 2 circuit comparison result output enabled).

7.3 VCC Input Voltage Monitor

7.3.1 Monitoring V_{det0}

The comparison results from voltage monitor 0 are not available for reading.

7.3.2 Monitoring V_{det1}

Table 7.2 shows the procedures to set up monitoring against V_{det1}. After the settings are complete, the comparison results from voltage monitor 1 can be monitored with the LVD1SR.MON flag.

Note: 如果安全属性配置为安全：
- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：
- 允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。
注1.当启用可屏蔽中断时，不要从复位状态更改ICU中的NMIER.LVD2EN位值。

7.2.9 LVD2SR：电压监视器2电路状态寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0E3

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MON	DET
重置后的值：	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
0	DET	电压监视器2电压变化检测标志 0：未检测到1：检测到Vdet2交叉	R/W*1
1	MON	电压监视器2信号监视器标志 0：VCC<Vdet21：VCC≥Vdet2或MON被禁用	R
7:2	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：
- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：
- 允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。
注1.该位只能写入0。向该位写入0后，需要2个系统时钟周期才能将该位读为0。

DET标志（电压监视器2电压变化检测标志）

当LVD2CMPCR.LVD2E位为1（使能电压检测2电路）且LVD2CR0.CMPE位为1（电压监控器2电路比较结果输出使能）。

设置LVD2CR0.RIE为0（禁用）后，将DET标志设置为0。在将LVD2CR0.RIE位设置为0后将其设置为1（启用）时，等待2个或更多PCLKB周期已过去。

MON标志（电压监控2信号监控标志）

当LVD2CMPCR.LVD2E位为1（电压检测2电路使能）且LVD2CR0.CMPE位为1（电压监控器2电路比较结果输出使能）。

7.3 VCC输入电压监视器

7.3.1 Monitoring V_{det0}

电压监视器0的比较结果不可读取。

7.3.2 Monitoring V_{det1}

表7.2显示了针对Vdet1设置监控的程序。设置完成后，电压监视器1的比较结果可以通过LVD1SR.MON标志进行监视。

Table 7.2 Procedures to set up monitoring against V_{det1}

Step		Monitoring the comparison results from voltage monitor 1
Setting up the voltage detection 1 circuit	1	Set LVD1CMPCR.LVD1E = 0 to disable voltage detection 1 before writing to the LVD1CMPCR.LVD1LVL[4:0] bits.
	2	Select the detection voltage in the LVD1CMPCR.LVD1LVL[4:0] bits.
	3	Set LVD1CMPCR.LVD1E = 1 to enable the voltage detection 1 circuit.
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD1 operation stabilization time after LVD1 is enabled.*1
Setting the digital filter*2	5	Select the sampling clock for the digital filter in the LVD1CR0.FSAMP[1:0] bits.
	6	Set LVD1CR0.DFDIS = 0 to enable the digital filter.
	7	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.
Enabling output	8	Set LVD1CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 1.

Note 1. Steps 5 to 7 can be performed during the wait time of step 4. For details of $t_{d(E-A)}$, see section 46, Electrical Characteristics.
Note 2. Steps 5 to 7 are not required if the digital filter is not in use.

7.3.3 Monitoring V_{det2}

Table 7.3 shows the procedures to set up monitoring against V_{det2}. After the settings are complete, the comparison results from voltage monitor 2 can be monitored in the LVD2SR.MON flag.

Table 7.3 Procedures to set up monitoring against V_{det2}

Step		Monitoring the results of comparison by voltage monitor 2
Setting up the voltage detection 2 circuit	1	Set LVD2CMPCR.LVD2E = 0 to disable voltage detection 2 before writing to the LVD2CMPCR.LVD2LVL[2:0] bits.
	2	Select the detection voltage in the LVD2CMPCR.LVD2LVL[2:0] bits.
	3	Set LVD2CMPCR.LVD2E = 1 to enable the voltage detection 2 circuit.
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD2 operation stabilization time after LVD2 is enabled.*1
Setting the digital filter*2	5	Select the sampling clock for the digital filter in the LVD2CR0.FSAMP[1:0] bits.
	6	Set LVD2CR0.DFDIS = 0 to enable the digital filter.
	7	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.
Enabling output	8	Set LVD2CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 2.

Note 1. Steps 5 to 7 can be performed during the wait time of step 4. For details of $t_{d(E-A)}$, see section 46, Electrical Characteristics.
Note 2. Steps 5 to 7 are not required if the digital filter is not in use.

7.4 Reset from Voltage Monitor 0

When using the reset from voltage monitor 0, clear the OFS1.LVDAS bit to 0 to enable the voltage monitor 0 reset after a reset. However, at boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Figure 7.4 shows an example of operations for a voltage monitor 0 reset.

Table 7.2 针对Vdet1设置监控的程序

Step		从电压监视器1监视比较结果
设置电压检测1电路	1	设置LVD1CMPCR.LVD1E=0以在写入之前禁用电压检测1 LVD1CMPCR.LVD1LVL[4:0] bits.
	2	在LVD1CMPCR.LVD1LVL[4:0]位中选择检测电压。
	3	设置LVD1CMPCR.LVD1E=1以启用电压检测1电路。
	4	启用LVD1后，至少等待td(E-A)的LVD1操作稳定时间。*1
设置数字滤波器*2	5	在LVD1CR0.FSAMP[1:0]位中选择数字滤波器的采样时钟。
	6	设置LVD1CR0.DFDIS=0以启用数字滤波器。
	7	等待至少2n+3个LOCO周期，其中n=2、4、8或16，数字滤波器的采样时钟是LOCO分频的n。
启用输出	8	设置LVD1CR0.CMPE=1以使能电压监视器1的比较结果输出。

注1.可以在步骤4的等待时间内执行步骤5到7。有关td(E-A)的详细信息，请参阅第46节，电气特性。
注2.如果不使用数字滤波器，则不需要步骤5至7。

7.3.3 Monitoring V_{det2}

表7.3显示了针对Vdet2设置监控的程序。设置完成后，可以在LVD2SR.MON标志中监控电压监视器2的比较结果。

Table 7.3 针对Vdet2设置监控的程序

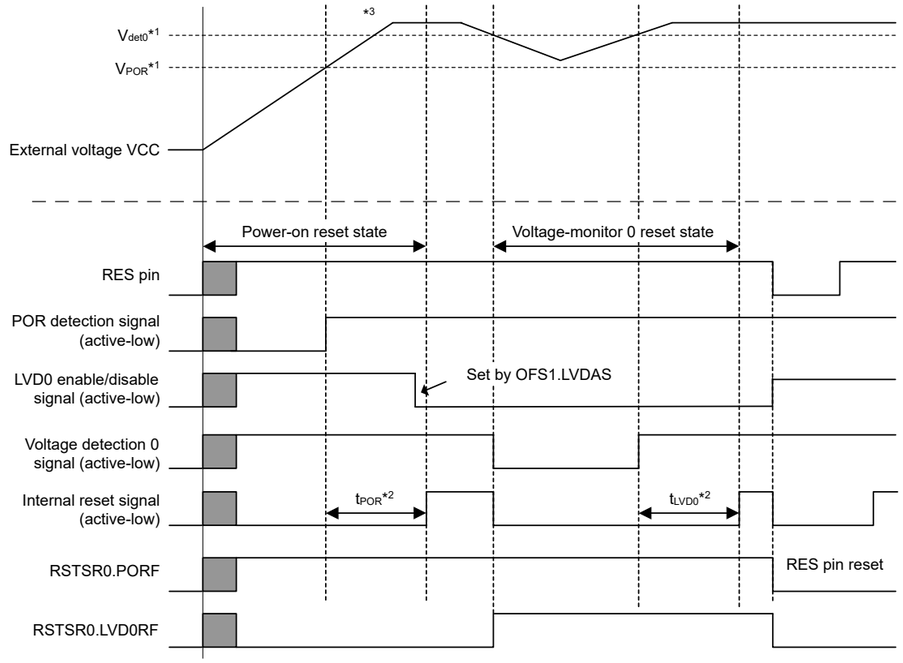
Step		通过电压监视器2监视比较结果
设置电压检测2电路	1	设置LVD2CMPCR.LVD2E=0以在写入之前禁用电压检测2 LVD2CMPCR.LVD2LVL[2:0] bits.
	2	在LVD2CMPCR.LVD2LVL[2:0]位中选择检测电压。
	3	设置LVD2CMPCR.LVD2E=1以启用电压检测2电路。
	4	启用LVD2后，至少等待td(E-A)的LVD2操作稳定时间。*1
设置数字滤波器*2	5	在LVD2CR0.FSAMP[1:0]位中选择数字滤波器的采样时钟。
	6	设置LVD2CR0.DFDIS=0以启用数字滤波器。
	7	等待至少2n+3个LOCO周期，其中n=2、4、8或16，数字滤波器的采样时钟是LOCO分频的n。
启用输出	8	设置LVD2CR0.CMPE=1以使能电压监视器2的比较结果输出。

注1.可以在步骤4的等待时间内执行步骤5到7。有关td(E-A)的详细信息，请参阅第46节，电气特性。
注2.如果不使用数字滤波器，则不需要步骤5至7。

7.4 从电压监视器复位0

使用电压监控器0复位时，将OFS1.LVDAS位清零以在复位后启用电压监控器0复位。但是，在引导模式下，无论OFS1.LVDAS位的值如何，都禁止从电压监视器0进行的复位。

图7.4显示了电压监视器0复位的操作示例。



Note: For details of the electrical characteristics, see section 46, Electrical Characteristics.
Note 1. V_{POR} indicates the detection level for a power-on reset and V_{det0} indicates the detection level for a voltage monitor 0 reset.
Note 2. t_{POR}: the period of a power-on reset.
t_{LVD0}: the period of a voltage monitor 0 reset.
Note 3. At power-on, the POR reset is released after VCC has reached the minimum guaranteed voltage.

Figure 7.4 Example of voltage monitor 0 reset operation

7.5 Interrupt and Reset from Voltage Monitor 1

An interrupt or reset can be generated in response to the comparison results from the voltage monitor 1 circuit.

Table 7.4 shows the procedures for setting bits related to the voltage monitor 1 interrupt/reset so that voltage monitoring occurs. Table 7.5 shows the procedures for setting bits related to the voltage monitor 1 interrupt/reset so that voltage monitoring stops. Figure 7.5 shows an example of operations for a voltage monitor 1 interrupt. For the operation of the voltage monitor 1 reset, see Figure 5.2 in section 5, Resets.

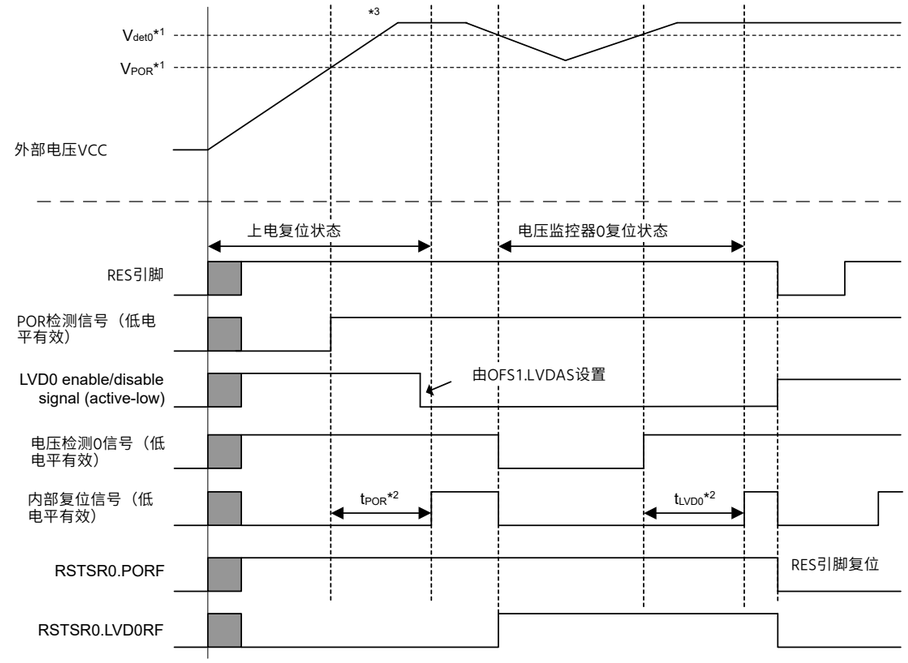
When using the voltage monitor 1 circuit in Software Standby mode or Deep Software Standby mode, set up the circuit using the procedures in this section.

(1) Setting in Software Standby mode

- Disable the digital filter (LVD1CR0.DFDIS = 1).
- When VCC > V_{det1} is detected, negate the voltage monitor 1 reset signal (LVD1CR0.RN = 0) following a stabilization time.

(2) Settings in Deep Software Standby mode

- Disable the digital filter (LVD1CR0.DFDIS = 1).



Note: 有关电气特性的详细信息，请参见第46节，电气特性。
注1.VPOR表示上电复位的检测电平，Vdet0表示电压监视器0复位的检测电平。

注2.tPOR：上电复位周期。
tLVD0:电压监视器0复位的周期。
注3.上电时，当VCC达到最低保证电压后，POR复位被释放。

Figure 7.4 电压监视器0复位操作示例

7.5 电压监视器1的中断和复位

响应电压监视器1电路的比较结果，可以产生中断或复位。

表7.4显示了设置与电压监控1中断复位相关的位以进行电压监控的过程。表7.5显示了设置与电压监控1中断复位相关的位以停止电压监控的步骤。图7.5显示了电压监视器1中断的操作示例。有关电压监视器1复位的操作，请参见第5节"复位"中的图5.2。

在软件待机模式或深度软件待机模式下使用电压监视器1电路时，请使用本节中的步骤设置电路。

(1) 在软件待机模式下设置

●禁用数字滤波器（LVD1CR0.DFDIS=1）。
●当检测到VCC>Vdet1时，在经过一段稳定时间后将电压监视器1复位信号(LVD1CR0.RN=0)取反。

(2) 深度软件待机模式中的设置

●禁用数字滤波器（LVD1CR0.DFDIS=1）。

- Enable the voltage monitor 1 interrupt (LVD1CR0.RI = 0). If the voltage monitor 1 reset is enabled (LVD1CR0.RI = 1), a transition to Deep Software Standby mode is not possible, and the operation transitions to Software Standby mode instead.
- When the DPSBYCR.DEEPCUT[1:0] bits are 11b, the voltage monitor 1 circuit stops. To use the voltage monitor 1 circuit in Deep Software Standby mode, set the DPSBYCR.DEEPCUT[1:0] bits to a value other than 11b.

Table 7.4 Procedures for setting bits related to voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring occurs

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output)	Voltage monitor 1 reset
Setting up the voltage detection 1 circuit	1	Set LVD1CMPCR.LVD1E = 0 to disable voltage detection 1 before writing to the LVD1CMPCR register.	
	2	Select the detection voltage in the LVD1CMPCR.LVD1LVL[4:0] bits.	
	3	Set LVD1CMPCR.LVD1E = 1 to enable the voltage detection 1 circuit.	
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD1 operation stabilization time after LVD1 is enabled.*1	
Setting the digital filter*3	5	Select the sampling clock for the digital filter in the LVD1CR0.FSAMP[1:0] bits.	
	6	Set LVD1CR0.DFDIS = 0 to enable the digital filter.	
	7	Wait for at least 2n + 3 LOCO cycles, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.*4	
Setting up the voltage monitor 1 interrupt or reset	8	Set LVD1CR0.RI = 0 to select the voltage monitor 1 interrupt.	• Set LVD1CR0.RI = 1 to select the voltage monitor 1 reset. • Select the type of reset negation in the LVD1CR0.RN bit.
	9	• Select the interrupt request condition in the LVD1CR1.IDTSEL[1:0] bits. • Select the interrupt type in the LVD1CR1.IRQSEL bit.	—
Enabling output	10	Set LVD1SR.DET = 0.	
	11	Set LVD1CR0.RIE = 1 to enable the voltage monitor 1 interrupt or reset.*2	
	12	Set LVD1CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 1.	

Note 1. Steps 5 to 11 can be performed during the wait time in step 4. For details on $t_{d\ (E-A)}$, see section 46, Electrical Characteristics.
Note 2. Step 11 is not required if only the ELC event signal is to be output.
Note 3. Steps 5 to 7 are not required if the digital filter is not in use.
Note 4. Steps 8 to 11 can be performed during the wait time of step 7.

Table 7.5 Procedures for setting bits related to voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring stops

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output), voltage monitor 1 reset
Stopping the enabling output	1	Set LVD1CR0.CMPE = 0 to disable output of the comparison results from voltage monitor 1.
	2	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.*2
	3	Set LVD1CR0.RIE = 0 to disable the voltage monitor 1 interrupt or reset.*1
Stopping the digital filter	4	Set LVD1CR0.DFDIS = 1 to disable the digital filter.*2 *3
Stopping the voltage detection 1 circuit	5	Set LVD1CMPCR.LVD1E = 0 to disable the voltage detection 1 circuit.

Note 1. Step 3 is not required if only the ELC event signal is to be output.
Note 2. Steps 2 and 4 are not required if the digital filter is not in use.
Note 3. To disable the digital filter from its enabled state and then re-enable it, disable it and wait for at least 2 LOCO clock cycles before re-enabling it.

If the voltage monitor 1 interrupt or reset setting is to be made again after it is used and stopped once, you can omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting the voltage detection 1 circuit is not required if the settings for the circuit do not change.
- Setting the digital filter is not required if the settings for the circuit do not change.

●启用电压监视器1中断(LVD1CR0.RI=0)。如果使能电压监视器1复位(LVD1CR0.RI=1)，则无法转换到深度软件待机模式，而是将操作转换到软件待机模式。

●当DPSBYCR.DEEPCUT[1:0]位为11b时，电压监视器1电路停止。要在深度软件待机模式下使用电压监视器1电路，请将DPSBYCR.DEEPCUT[1:0]位设置为11b以外的值。

Table 7.4 设置与电压监控器1中断和电压监控器1相关的位以进行电压监控的步骤

Step		电压监视器1中断（电压监视器1 ELC event output)	电压监视器1复位
设置电压检测1电路	1	设置LVD1CMPCR.LVD1E=0以在写入LVD1CMPCR寄存器之前禁用电压检测1。	
	2	在LVD1CMPCR.LVD1LVL[4:0]位中选择检测电压。	
	3	设置LVD1CMPCR.LVD1E=1以启用电压检测1电路。	
	4	启用LVD1后，至少等待td(E-A)的LVD1操作稳定时间。*1	
设置数字滤波器*3	5	在LVD1CR0.FSAMP[1:0]位中选择数字滤波器的采样时钟。	
	6	设置LVD1CR0.DFDIS=0以启用数字滤波器。	
	7	等待至少2n+3个LOCO周期，其中n=2、4、8或16，并且数字滤波器的采样时钟是LOCO频率除以n。*4	
设置电压监视器1中断或复位	8	设置LVD1CR0.RI=0以选择电压监视器1中断。	• 设置LVD1CR0.RI=1以选择电压监视器1复位。 • 选择复位否定的类型 LVD1CR0.RN bit.
	9	• 选择中断请求条件 LVD1CR1.IDTSEL[1:0] bits. • 选择中断类型 LVD1CR1.IRQSEL bit.	—
启用输出	10	Set LVD1SR.DET = 0.	
	11	设置LVD1CR0.RIE=1以启用电压监视器1中断或复位。*2	
	12	设置LVD1CR0.CMPE=1以使能电压监视器1的比较结果输出。	

注1.步骤5至11可以在步骤4的等待时间内执行。有关td(E-A)的详细信息，请参阅第46节，电气特性。
注2.如果只输出ELC事件信号，则不需要步骤11。
注3.如果不使用数字滤波器，则不需要步骤5至7。
注4.步骤7的等待时间内可以执行步骤8至11。

Table 7.5 设置与电压监控1中断和电压监控1相关的位以使电压监控停止的步骤

Step		电压监视器1中断（电压监视器1ELC事件输出），电压监视器1复位
停止使能输出	1	设置LVD1CR0.CMPE=0以禁用电压监视器1的比较结果输出。
	2	等待至少2n+3个LOCO周期，其中n=2、4、8或16，数字滤波器的采样时钟是LOCO分频的n。*2
	3	设置LVD1CR0.RIE=0以禁用电压监视器1中断或复位。*1
停止数字滤波器	4	设置LVD1CR0.DFDIS=1以禁用数字滤波器。*2*3
停止电压检测1电路	5	设置LVD1CMPCR.LVD1E=0以禁用电压检测1电路。

注1.如果只输出ELC事件信号，则不需要步骤3。
注2.如果不使用数字滤波器，则不需要步骤2和4。
注3.要从启用状态禁用数字滤波器然后重新启用它，请禁用它并等待至少2个LOCO时钟周期，然后再重新启用它。

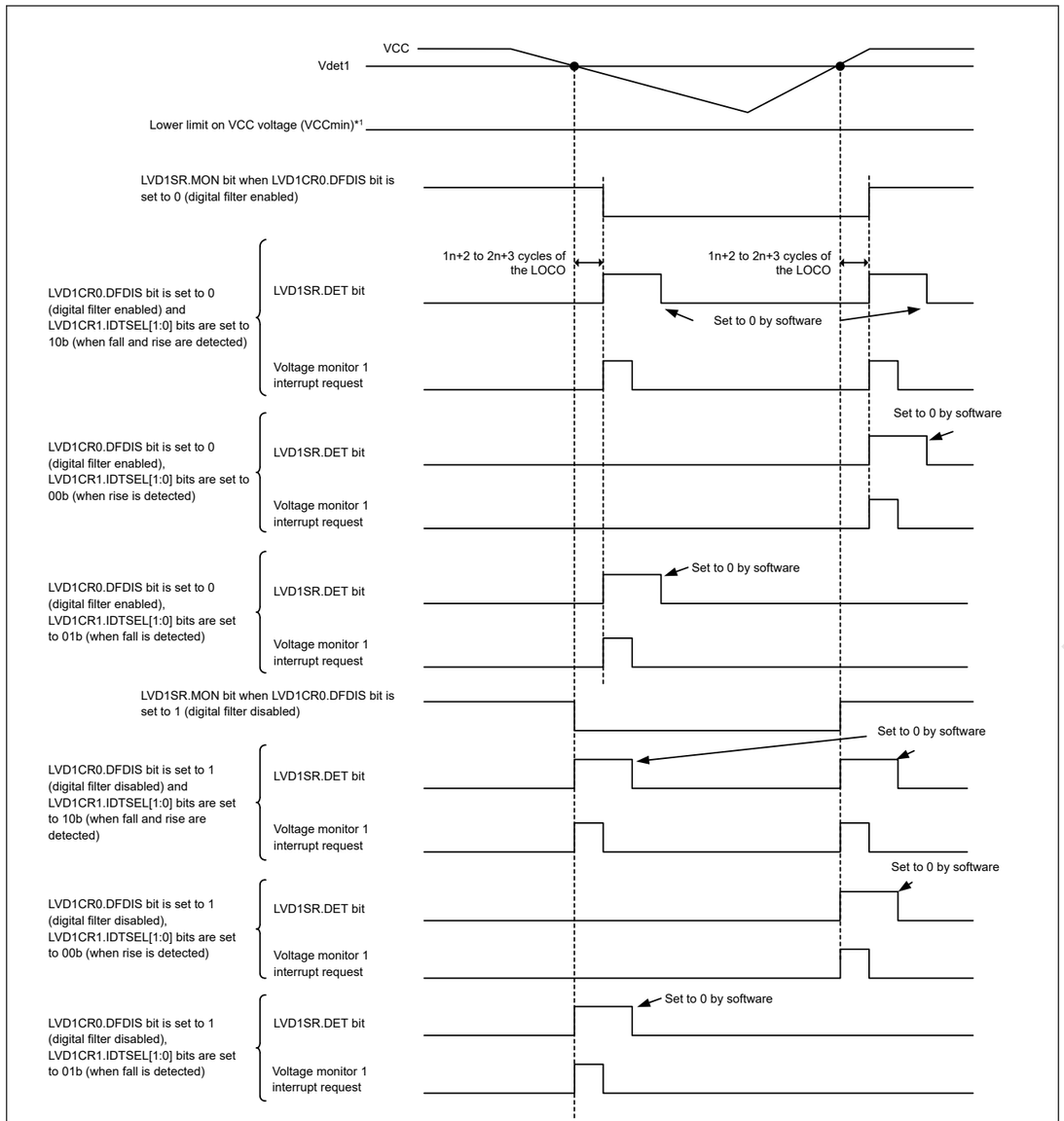
如果电压监测器1在使用和停止一次后再次进行中断或复位设置，可以根据情况省略停止和设置过程中的以下步骤：

●如果电路的设置不变，则不需要设置电压检测1电路。

●如果电路的设置不变，则不需要设置数字滤波器。

- Setting the voltage monitor 1 interrupt or reset is not required if the settings for the voltage monitor 1 interrupt or voltage monitor 1 reset do not change.

Figure 7.5 shows an example of the voltage monitor 1 interrupt operation.



Note: n: Frequency of the sampling clock for the digital filter is the LOCO frequency divided by n
Note 1. When the voltage monitor 0 reset is not in use, use at VCC ≥ VCCmin.

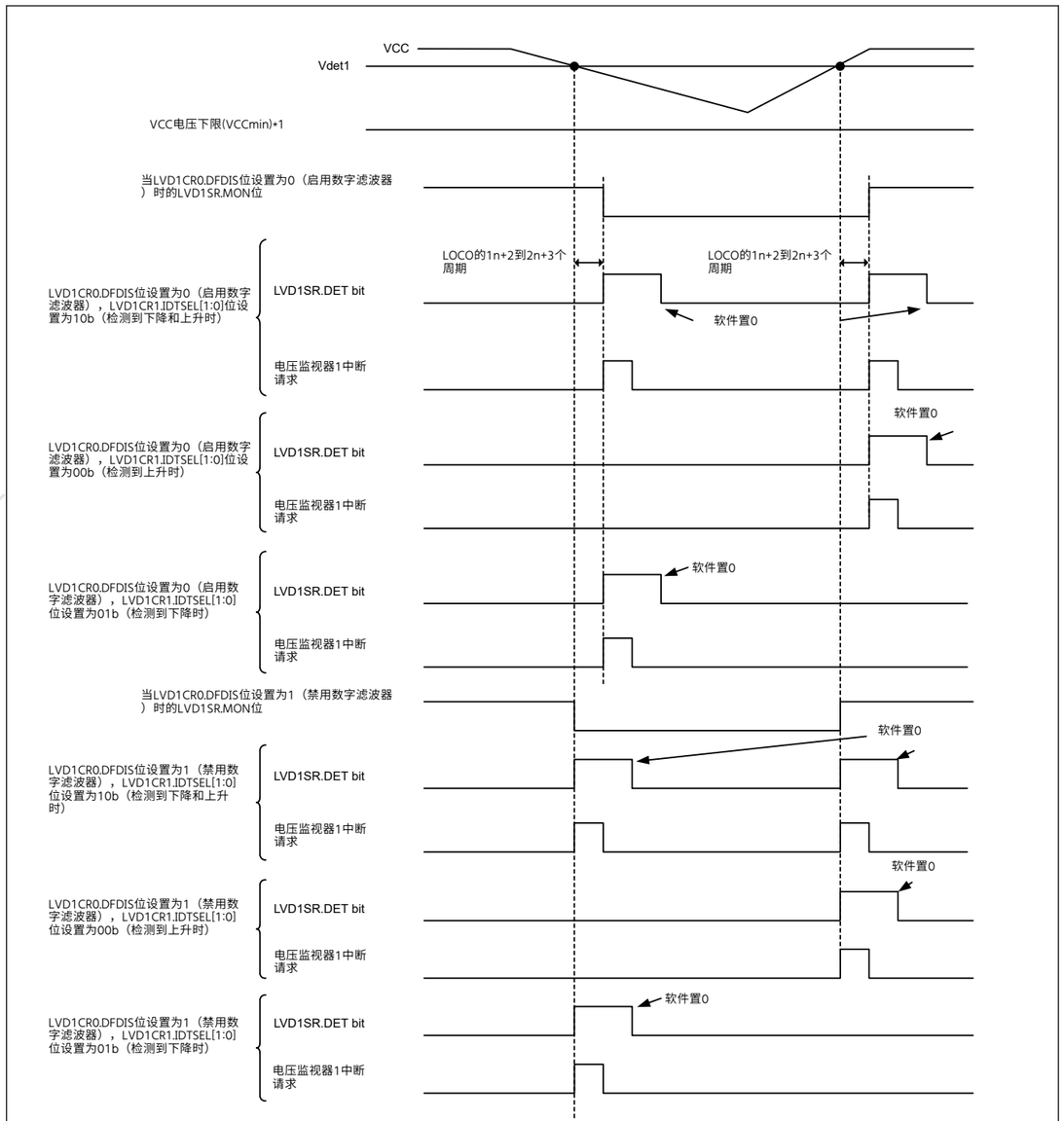
Figure 7.5 Example of voltage monitor 1 interrupt operation

7.6 Interrupt and Reset from Voltage Monitor 2

An interrupt or reset can be generated in response to the comparison results from the voltage monitor 2 circuit.

●如果电压监视器1中断或电压监视器1复位的设置没有改变，则不需要设置电压监视器1中断或复位。

图7.5显示了电压监视器1中断操作的示例。



Note: n：数字滤波器的采样时钟频率是LOCO频率除以n
注1.不使用电压监视器0复位时，请在VCC≥VCCmin时使用。

Figure 7.5 电压监视器1中断操作示例

7.6 电压监视器2的中断和复位

响应电压监视器2电路的比较结果，可以产生中断或复位。

Table 7.6 shows the procedures for setting bits related to the voltage monitor 2 interrupt/reset so that voltage monitoring occurs. Table 7.7 shows the procedures for setting bits related to the voltage monitor 2 interrupt/reset so that voltage monitoring stops. Figure 7.6 shows an example of operations for a voltage monitor 2 interrupt. For the operation of the voltage monitor 2 reset, see Figure 5.2 in section 5, Resets.

When using the voltage monitor 2 circuit in Software Standby mode or Deep Software Standby mode, set up the circuit with the following procedures.

(1) Setting in Software Standby mode

- Disable the digital filter (LVD2CR0.DFDIS = 1)
- When VCC > V_{det2} is detected, negate the voltage monitor 2 reset signal (LVD2CR0.RN = 0) following a LVD2 stabilization time.

(2) Settings in Deep Software Standby mode

- Disable the digital filter (LVD2CR0.DFDIS = 1).
- Enable the voltage monitor 2 interrupt (LVD2CR0.RI = 0). If the voltage monitor 2 reset is enabled (LVD2CR0.RI = 1), a transition to Deep Software Standby mode is not possible, and the operation transitions to Software Standby mode instead.
- When the DPSBYCR.DEEPCUT[1:0] bits are 11b, the voltage monitor 2 circuit stops. To use the voltage monitor 2 circuit in Deep Software Standby mode, set the DPSBYCR.DEEPCUT[1:0] bits to a value other than 11b.

Table 7.6 Procedures for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring occurs

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output)	Voltage monitor 2 reset
2 circuit	1	Set LVD2CMPCR.LVD2E = 0 to disable voltage detection 2 before writing to the LVD2CMPCR register.	
	2	Select the detection voltage in the LVD2CMPCR.LVD2LVL[2:0] bits.	
	3	Set LVD2CMPCR.LVD2E = 1 to enable the voltage detection 2 circuit.	
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD2 operation stabilization time after LVD2 is enabled.*1	
Setting the digital filter*3	5	Select the sampling clock for the digital filter in the LVD2CR0.FSAMP[1:0] bits.	
	6	Set LVD2CR0.DFDIS = 0 to enable the digital filter.	
	7	Wait for at least 2n + 3 LOCO cycles, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.*4	
Setting up the voltage monitor 2 interrupt or reset	8	Set LVD2CR0.RI = 0 to select the voltage monitor 2 interrupt.	• Set LVD2CR0.RI = 1 to select the voltage monitor 2 reset. • Select the type of reset negation in the LVD2CR0.RN bit.
	9	• Select the interrupt request condition in the LVD2CR1.IDTSEL[1:0] bits. • Select the interrupt type in the LVD2CR1.IRQSEL bit.	—
Enabling output	10	Set LVD2SR.DET = 0.	
	11	Set LVD2CR0.RIE = 1 to enable the voltage monitor 2 interrupt or reset.*2	
	12	Set LVD2CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 2.	

Note 1. Steps 5 to 11 can be performed during the wait time in step 4. For details on $t_{d(E-A)}$, see section 46, Electrical Characteristics.
Note 2. Step 11 is not required if only the ELC event signal is to be output.
Note 3. Steps 5 to 7 are not required if the digital filter is not in use.
Note 4. Steps 8 to 11 can be performed during the wait time of step 7.

表7.6显示了设置与电压监视器2中断复位相关的位以进行电压监视的过程。表7.7显示了设置与电压监控2中断复位相关的位以停止电压监控的步骤。图7.6显示了电压监视器2中断的操作示例。有关电压监视器2复位的操作，请参见第5节“复位”中的图5.2。

在软件待机模式或深度软件待机模式下使用电压监视器2电路时，请按照以下步骤设置电路。

(1) 在软件待机模式下设置

●禁用数字滤波器(LVD2CR0.DFDIS=1)

●当检测到VCC>Vdet2时，在LVD2稳定时间后取消电压监视器2复位信号(LVD2CR0.RN=0)。

(2) 深度软件待机模式中的设置

●禁用数字滤波器（LVD2CR0.DFDIS=1）。

●启用电压监视器2中断(LVD2CR0.RI=0)。如果启用电压监视器2复位(LVD2CR0.RI=1)，则无法转换到深度软件待机模式，而是将操作转换到软件待机模式。

●当DPSBYCR.DEEPCUT[1:0]位为11b时，电压监视器2电路停止。要在深度软件待机模式下使用电压监视器2电路，请将DPSBYCR.DEEPCUT[1:0]位设置为11b以外的值。

Table 7.6 设置与电压监控器2中断和电压监控器2相关的位以进行电压监控的步骤

Step		电压监视器2中断（电压监视器2 ELC event output)	电压监视器2复位
2 circuit	1	在写入LVD2CMPCR寄存器之前，设置LVD2CMPCR.LVD2E=0以禁用电压检测2。	
	2	在LVD2CMPCR.LVD2LVL[2:0]位中选择检测电压。	
	3	设置LVD2CMPCR.LVD2E=1以启用电压检测2电路。	
	4	启用LVD2后，至少等待td(E-A)的LVD2操作稳定时间。*1	
设置数字滤波器*3	5	在LVD2CR0.FSAMP[1:0]位中选择数字滤波器的采样时钟。	
	6	设置LVD2CR0.DFDIS=0以启用数字滤波器。	
	7	等待至少2n+3个LOCO周期，其中n=2、4、8或16，并且数字滤波器的采样时钟是LOCO频率除以n。*4	
设置电压监视器2中断或复位	8	设置LVD2CR0.RI=0以选择电压监视器2中断。	• 设置LVD2CR0.RI=1以选择电压监视器2复位。 • 选择复位否定的类型 LVD2CR0.RN bit.
	9	• 选择中断请求条件 LVD2CR1.IDTSEL[1:0] bits. • 选择中断类型 LVD2CR1.IRQSEL bit.	—
启用输出	10	Set LVD2SR.DET = 0.	
	11	设置LVD2CR0.RIE=1以启用电压监视器2中断或复位。*2	
	12	设置LVD2CR0.CMPE=1以使能电压监视器2的比较结果输出。	

注1.步骤5至11可以在步骤4的等待时间内执行。有关td(E-A)的详细信息，请参阅第46节，电气特性。
注2.如果只输出ELC事件信号，则不需要步骤11。
注3.如果不使用数字滤波器，则不需要步骤5至7。
注4.步骤7的等待时间内可以执行步骤8至11。

Table 7.7 Procedures for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring stops

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output), voltage monitor 2 reset
Settings to stop enabling output	1	Set LVD2CR0.CMPE = 0 to disable output of the comparison results from voltage monitor 2.
	2	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.*2
	3	Set LVD2CR0.RIE = 0 to disable the voltage monitor 2 interrupt or reset.*1
Stopping the digital filter	4	Set LVD2CR0.DFDIS = 1 to disable the digital filter. *2 *3
Stopping the voltage detection 2 circuit	5	Set LVD2CMPCR.LVD2E = 0 to disable the voltage detection 2 circuit.

Note 1. Step 3 is not required if only the ELC event signal is to be output.
Note 2. Steps 2 and 4 are not required if the digital filter is not in use.
Note 3. To disable the digital filter from its enabled state and then re-enable it, disable it and wait for at least 2 LOCO clock cycles before re-enabling it.

If the voltage monitor 2 interrupt or reset setting is to be made again after it is used and stopped once, you can omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting the voltage detection 2 is not required if the settings for the circuit do not change.
- Setting the digital filter is not required if the settings for the circuit do not change.
- Setting the voltage monitor 2 interrupt or reset is not required if the settings for the voltage monitor 2 interrupt or voltage monitor 2 reset do not change.

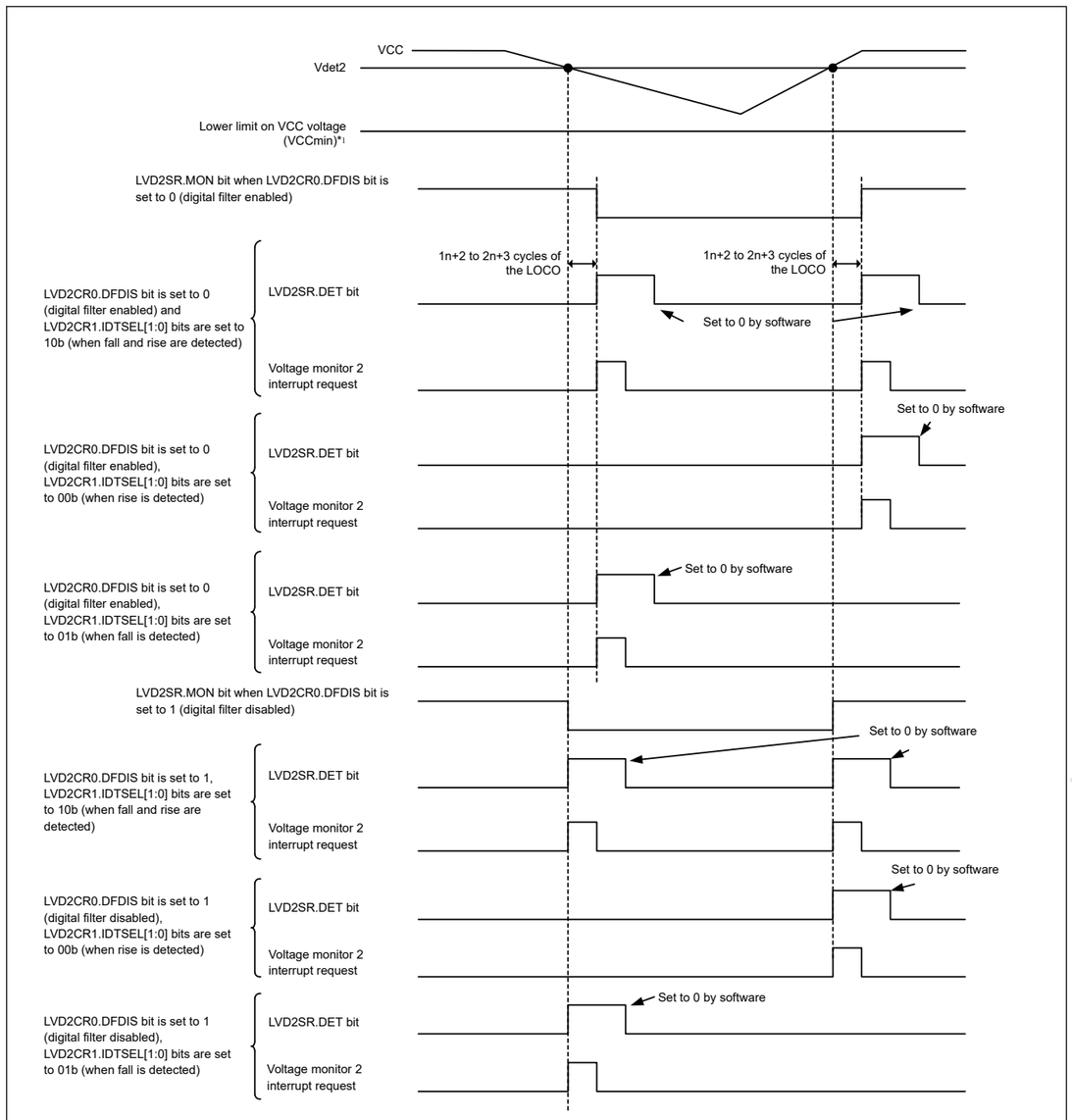
Table 7.7 设置与电压监控器2中断和电压监控器2相关的位以使电压监控器停止的步骤

Step		电压监控器2中断（电压监控器2ELC事件输出），电压监控器2复位
停止启用输出的设置	1	设置LVD2CR0.CMPE=0以禁用电压监视器2的比较结果输出。
	2	等待至少2n+3个LOCO周期，其中n=2、4、8或16，数字滤波器的采样时钟是LOCO分频的n。*2
	3	设置LVD2CR0.RIE=0以禁用电压监视器2中断或复位。*1
停止数字滤波器	4	设置LVD2CR0.DFDIS=1以禁用数字滤波器。*2*3
停止电压检测2电路	5	设置LVD2CMPCR.LVD2E=0以禁用电压检测2电路。

注1.如果只输出ELC事件信号，则不需要步骤3。
注2.如果不使用数字滤波器，则不需要步骤2和4。
注3.要从启用状态禁用数字滤波器然后重新启用它，请禁用它并等待至少2个LOCO时钟周期，然后再重新启用它。

如果电压监测器2的中断或复位设置在使用和停止一次后再次进行，可以根据情况省略停止和设置过程中的以下步骤：

- ●如果电路的设置不变，则不需要设置电压检测2。
- ●如果电路的设置不变，则不需要设置数字滤波器。
- ●如果电压监视器2中断或电压监视器2复位的设置没有改变，则不需要设置电压监视器2中断或复位。



Note: n: Frequency of the sampling clock for the digital filter is the LOCO frequency divided by n
Note 1. When the voltage monitor 0 reset is not in use, use at VCC ≥ VCCmin.

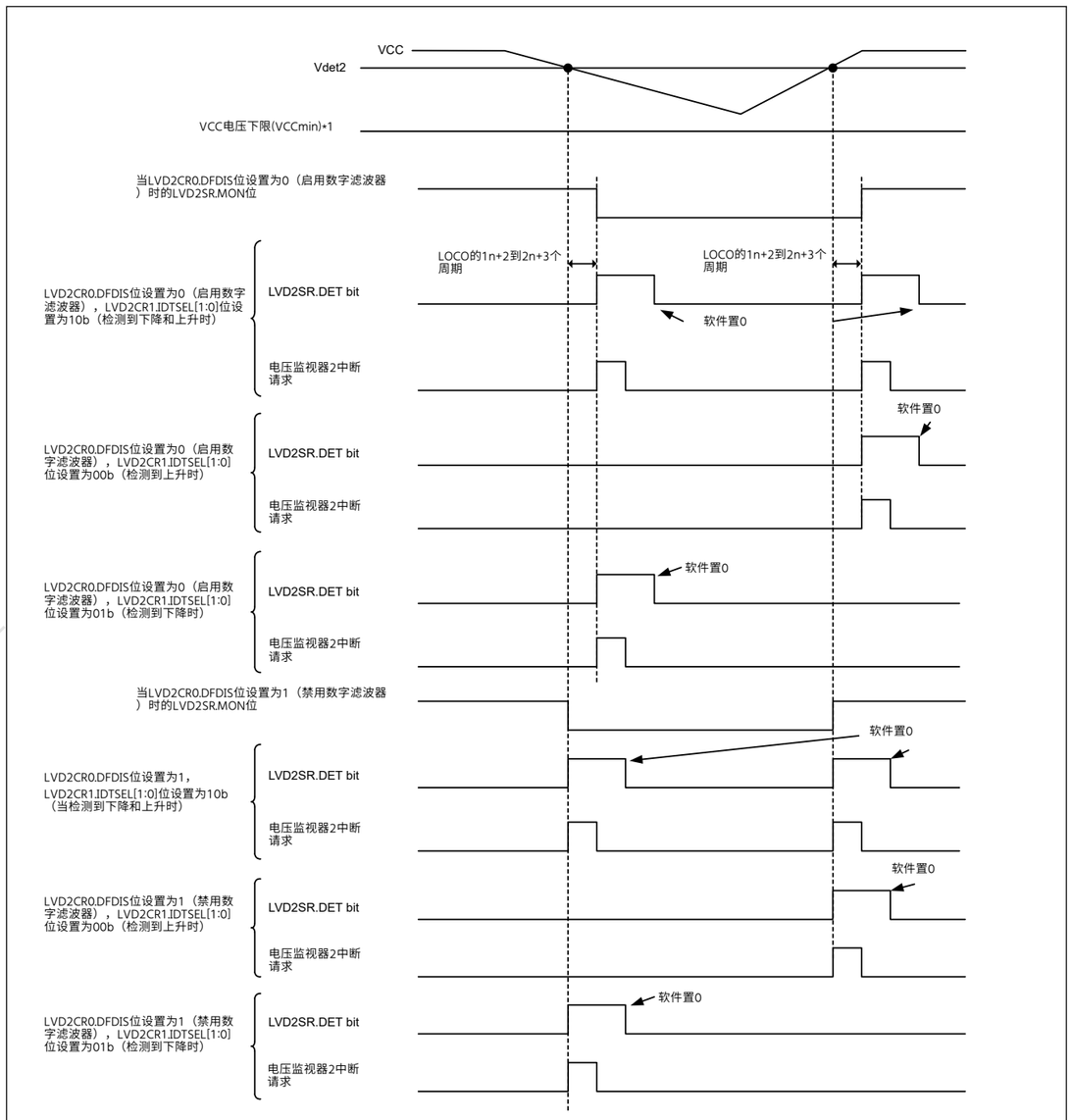
Figure 7.6 Example of voltage monitor 2 interrupt operation

7.7 Event Link Controller (ELC) Output

The LVD can output the event signals to the Event Link Controller (ELC).

(1) V_{det1} Crossing Detection Event

The LVD outputs the event signal when it detects that the voltage has passed the V_{det1} voltage while both the voltage detection 1 circuit and the voltage monitor 1 circuit comparison result output are enabled.



Note: n：数字滤波器的采样时钟频率是LOCO频率除以n
注1.不使用电压监视器0复位时，请在VCC≥VCCmin时使用。

Figure 7.6 电压监视器2中断操作示例

7.7 事件链接控制器(ELC)输出

LVD可以将事件信号输出到事件链接控制器(ELC)。

(1) Vdet1交叉检测事件

当电压检测1电路和电压监视器1电路比较结果输出都启用时，LVD检测到电压已超过Vdet1电压时输出事件信号。

(2) V_{det2} Crossing Detection Event

The LVD outputs the event signal when it detects that the voltage has passed the V_{det2} voltage while both the voltage detection 2 circuit and the voltage monitor 2 circuit comparison result output are enabled.

When enabling the event link output function of the LVD, you must enable the LVD before enabling the LVD event link function of the ELC. To stop the event link output function of the LVD, you must stop the LVD before disabling the LVD event link function of the ELC.

7.7.1 Interrupt Handling and Event Linking

The LVD provides bits to separately enable or disable the voltage monitor 1 and 2 interrupts. When an interrupt source is generated and the interrupt is enabled by the interrupt enable bit, the interrupt signal is output to the CPU.

In contrast, as soon as an interrupt source is generated, an event link signal is output as the event signal to the other module through the ELC, regardless of the state of the interrupt enable bit.

It is possible to output voltage monitor 1 and 2 interrupts in Software Standby and Deep Software Standby modes. The event signals for the ELC in Software Standby and Deep Software Standby modes are output as follows:

- When a V_{det1} or V_{det2} passage events is detected in Software Standby mode, event signals are not generated for the ELC because the clock is not supplied in Software Standby mode. Because the V_{det1} and V_{det2} passage detection flags are saved, when the clock supply resumes after returning from Software Standby mode, the event signals for the ELC are output based on the state of the V_{det1} and V_{det2} detection flags.
- When a Vdet1 or Vdet2 passage events are detected in Deep Software Standby mode, event signals are not generated for the ELC.

(2) Vdet2交叉检测事件

当电压检测2电路和电压监测器2电路比较结果输出都启用时，LVD检测到电压已超过Vdet2电压时输出事件信号。

使能LVD的事件链接输出功能时，必须先使能LVD，再使能ELC的LVD事件链接功能。要停止LVD的事件链接输出功能，必须先停止LVD，然后再禁用ELC的LVD事件链接功能。

7.7.1 中断处理和事件链接

LVD提供位来分别启用或禁用电压监视器1和2中断。当产生中断源并通过中断使能位使能中断时，将中断信号输出到CPU。

相反，一旦产生中断源，无论中断使能位的状态如何，都会通过ELC将事件链接信号作为事件信号输出到其他模块。

在软件待机和深度软件待机模式下，可以输出电压监视器1和2中断。软件待机和深度软件待机模式下ELC的事件信号输出如下：

- 当在软件待机模式下检测到Vdet1或Vdet2通过事件时，不会为ELC，因为在软件待机模式下不提供时钟。因为保存了Vdet1和Vdet2通过检测标志，所以当从软件待机模式恢复后时钟供应恢复时，ELC的事件信号将根据Vdet1和Vdet2检测标志的状态输出。
- 当在深度软件待机模式下检测到Vdet1或Vdet2通过事件时，不会为ELC生成事件信号。

8. Clock Generation Circuit

8.1 Overview

The MCU provides a clock generation circuit. Table 8.1 and Table 8.2 list the clock generation circuit specifications. Figure 8.1 show a block diagram, and Table 8.3 lists the I/O pins.

Table 8.1 Clock generation circuit specifications for the clock sources

Clock source	Description	Specification
Main clock oscillator (MOSC)	Resonator frequency	8 MHz to 24 MHz
	External clock input frequency	Up to 24 MHz
	External resonator or additional circuit	ceramic resonator, crystal
	Connection pins	EXTAL, XTAL
	Drive capability switching	Available
	Oscillation stop detection function	Available
PLL circuit	Input clock source	MOSC, HOCO
	Input pulse frequency division ratio	Selectable from 1, 2, and 3
	Input frequency	8 MHz to 24 MHz
	Frequency multiplication ratio	Selectable from 10 to 30 (0.5 steps)
	Output pulse frequency division ratio	Unavailable
	PLL Output frequency	120 MHz to 240 MHz
PLL2 circuit	Input clock source	MOSC, HOCO
	Input pulse frequency division ratio	Selectable from 1, 2, and 3
	Input frequency	8 MHz to 24 MHz
	Frequency multiplication ratio	Selectable from 10 to 30 (0.5 steps)
	Output pulse frequency division ratio	Unavailable
	PLL Output frequency	120 MHz to 240 MHz
	PLL2-LDO stop function	Unavailable
High-speed on-chip oscillator (HOCO)	Oscillation frequency	16/18/20 MHz
	FLL function	Unavailable
	User trimming	Available
Middle-speed on-chip oscillator (MOCO)	Oscillation frequency	8 MHz
	User trimming	Available
Low-speed on-chip oscillator (LOCO)	Oscillation frequency	32.768 kHz
	User trimming	Available
IWDT-dedicated on-chip oscillator (IWDTLOCO)	Oscillation frequency	15 kHz
	User trimming	Unavailable
External clock input for JTAG (TCK)	Input clock frequency	Up to 25 MHz
External clock input for SWD (SWCLK)	Input clock frequency	Up to 25 MHz

Table 8.2 Clock generation circuit specifications for the internal clocks (1 of 2)

Item	Clock source	Clock supply	Specification
System clock (ICLK)	MOSC/HOCO/MOCO/ LOCO/PLL	CPU, DTC, DMAC, Flash, RAM, I/O ports, TFU, IIRFA	Up to 240 MHz Division ratios: 1/2/4/8/16/32/64

8. 时钟产生电路

8.1 Overview

MCU提供时钟生成电路。表8.1和表8.2列出了时钟生成电路规格。图8.1显示了框图，表8.3列出了IO引脚。

Table 8.1 时钟源的时钟生成电路规格

时钟源	Description	Specification
主时钟振荡器(MOSC)	谐振器频率	8 MHz to 24 MHz
	外部时钟输入频率	高达24MHz
	外部谐振器或附加电路	陶瓷谐振器，晶体
	连接引脚	EXTAL, XTAL
	驱动能力切换	Available
	振荡停止检测功能	Available
PLL circuit	输入时钟源	MOSC, HOCO
	输入脉冲分频比	可从1、2和3中选择
	输入频率	8 MHz to 24 MHz
	倍频比	可选择10至30（0.5步）
	输出脉冲分频比	Unavailable
	锁相环输出频率	120 MHz to 240 MHz
PLL2 circuit	输入时钟源	MOSC, HOCO
	输入脉冲分频比	可从1、2和3中选择
	输入频率	8 MHz to 24 MHz
	倍频比	可选择10至30（0.5步）
	输出脉冲分频比	Unavailable
	锁相环输出频率	120 MHz to 240 MHz
	PLL2-LDO停止功能	Unavailable
High-speed on-chip oscillator (HOCO)	振荡频率	16/18/20 MHz
	FLL function	Unavailable
	用户修剪	Available
Middle-speed on-chip oscillator (MOCO)	振荡频率	8 MHz
	用户修剪	Available
Low-speed on-chip oscillator (LOCO)	振荡频率	32.768 kHz
	用户修剪	Available
IWDT-dedicated on-chip oscillator (IWDTLOCO)	振荡频率	15 kHz
	用户修剪	Unavailable
JTAG(TCK)的外部时钟输入	输入时钟频率	高达25MHz
SWD的外部时钟输入(SWCLK)	输入时钟频率	高达25MHz

Table 8.2 内部时钟的时钟生成电路规格（1of2）

Item	时钟源	时钟电源	Specification
系统时钟(ICLK)	MOSC/HOCO/MOCO/ LOCO/PLL	CPU、DTC、DMAC、闪存、RAM、IO端口、TFU、IIRFA	高达240兆赫 Division ratios: 1/2/4/8/16/32/64

Table 8.2 Clock generation circuit specifications for the internal clocks (2 of 2)

Item	Clock source	Clock supply	Specification
Peripheral module clock A (PCLKA)	MOSC/HOCO/MOCO/ LOCO/PLL	Peripheral modules (SCI, CANFD-RAM, CNECC, SPI, CRC, DOC, ADC, DAC12, SCE5, GPT bus clock, PDG, IIC)	Up to 120 MHz Division ratio: 1/2/4/8/16/32/64
Peripheral module clock B (PCLKB)	MOSC/HOCO/MOCO/ LOCO/PLL	Peripheral modules (CAC, ELC, POEG, WDT, IWDT, AGT, CANFD, TSN, Standby SRAM, KINT ACMPHS)	Up to 60 MHz Division ratio: 1/2/4/8/16/32/64
Peripheral module clock C (PCLKC)	MOSC/HOCO/MOCO/ LOCO/PLL	Peripheral module (ADC)	Up to 60 MHz Division ratio: 1/2/4/8/16/32/64
Peripheral module clock D (PCLKD)	MOSC/HOCO/MOCO/ LOCO/PLL	Peripheral module (GPT)	Up to 120 MHz Division ratio: 1/2/4/8/16/32/64
FlashIF clock (FCLK)	MOSC/HOCO/MOCO/ LOCO/PLL	FlashIF	4 MHz to 60 MHz(P/E) Up to 60 MHz(read) Division ratio: 1/2/4/8/16/32/64
CANFD clock (CANFDCLK)	PLL/PLL2	CANFD	Up to 40 MHz Division ratio: 1/2/4/6/8
CAN clock (CANMCLK)	MOSC	CANFD	8 MHz to 24 MHz
Peripheral module asynchronous clock for GPT (GPTCLK)	MOSC/HOCO/MOCO/ LOCO/PLL/PLL2	GPT	Up to 200 MHz Division ratio: 1/2/4/6/8
Peripheral module asynchronous clock for IIC (IICCLK)	MOSC/HOCO/MOCO/ LOCO/PLL/PLL2	IIC	Up to 200 MHz Division ratio: 1/2/4/6/8
Peripheral module asynchronous clock for SCI/SPI (SCISPICLK)	MOSC/HOCO/MOCO/ LOCO/PLL/PLL2	SCI, SPI	Up to 120 MHz Division ratio: 1/2/4/6/8
AGT clock (AGTLCLK)	LOCO	AGT	32.768 kHz
CAC Main clock (CACMCLK)	MOSC	CAC	Up to 24 MHz
CAC LOCO clock (CACLCLK)	LOCO	CAC	32.768 kHz
CAC MOCO clock (CACMOCLK)	MOCO	CAC	8 MHz
CAC HOCO clock (CACHCLK)	HOCO	CAC	16/18/20 MHz
CAC IWDTLOCO clock (CACILCLK)	IWDTLOCO	CAC	15 kHz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick timer clock (SYSTICCLK)	LOCO	SysTick timer	32.768 kHz
JTAG clock (JTAGTCK)	TCK	JTAG	Up to 25 MHz
Serial wire clock (SWCLK)	SWCLK	OCD	Up to 25 MHz
Trace clock (TRCLK)	MOSC/HOCO/MOCO/ LOCO/PLL	CPU-OCD	Up to 120 MHz Division ratio: 1/2/4
TCLK pin output (TCLK)	1/2 TRCLK	TCLK pin	Up to 60 MHz
Clock/buzzer output (CLKOUT)	MOSC/LOCO/MOCO/HOCO	CLKOUT pin	Up to 24 MHz Division ratios: 1/2/4/8/16/32/64/128

Note: Restrictions on setting clock frequency: ICLK ≥ PCLKA ≥ PCLKB, PCLKD ≥ PCLKA ≥ PCLKB, GPTCLK ≥ PCLKA
ICLK ≥ FCLK
Restrictions on clock frequency ratio: (N: integer, and up to 64)
ICLK:FCLK = N:1, ICLK:PCLKA = N:1, ICLK:PCLKB = N:1, ICLK:PCLKC = N:1 or 1:N , ICLK:PCLKD= N:1 or 1:N, ICLK:TRCLK= N:1 or 1:N
If the CANFD is used, clock frequency ratio is constrained to be PCLKA:PCLKB = 2:1.

Note: Restrictions on the minimum FCLK frequency 4MHz when P/E.

Table 8.2 内部时钟的时钟生成电路规格(2of2)

Item	时钟源	时钟电源	Specification
外设模块时钟A(PCLKA)	MOSC/HOCO/MOCO/ LOCO/PLL	外围模块（SCI、CANFD RAM、CNECC、SPI、CRC、DOC、ADC、DAC12、SCE5、GPT总线时钟、PDG、IIC）	高达120MHz Division ratio: 1/2/4/8/16/32/64
外设模块时钟B(PCLKB)	MOSC/HOCO/MOCO/ LOCO/PLL	外围模块（CAC、ELC、POEG, WDT, IWDT, AGT, CANFD, TSN, Standby SRAM, KINT ACMPHS)	高达60MHz Division ratio: 1/2/4/8/16/32/64
外设模块时钟C(PCLKC)	MOSC/HOCO/MOCO/ LOCO/PLL	外围模块(ADC)	高达60MHz Division ratio: 1/2/4/8/16/32/64
外设模块时钟D(PCLKD)	MOSC/HOCO/MOCO/ LOCO/PLL	外围模块(GPT)	高达120MHz Division ratio: 1/2/4/8/16/32/64
FlashIF clock (FCLK)	MOSC/HOCO/MOCO/ LOCO/PLL	FlashIF	4MHz至60MHz(PE)高达60MHz（读取） Division ratio: 1/2/4/8/16/32/64
CANFD clock (CANFDCLK)	PLL/PLL2	CANFD	高达40MHz Division ratio: 1/2/4/6/8
CAN时钟(CANMCLK)	MOSC	CANFD	8 MHz to 24 MHz
GPT外设模块异步时钟(GPTCLK)	MOSC/HOCO/MOCO/ LOCO/PLL/PLL2	GPT	高达200兆赫兹 Division ratio: 1/2/4/6/8
IIC外设模块异步时钟(IICCLK)	MOSC/HOCO/MOCO/ LOCO/PLL/PLL2	IIC	高达200兆赫兹 Division ratio: 1/2/4/6/8
用于SCISPI(SCISPICLK)的外设模块异步时钟	MOSC/HOCO/MOCO/ LOCO/PLL/PLL2	SCI、SPI	高达120MHz Division ratio: 1/2/4/6/8
AGT clock (AGTLCLK)	LOCO	AGT	32.768 kHz
CAC主时钟(CACMCLK)	MOSC	CAC	高达24MHz
CACLOCO时钟(CACLCLK)	LOCO	CAC	32.768 kHz
CACMOCO时钟(CACMOCLK)	MOCO	CAC	8 MHz
CACHOCO时钟(CACHCLK)	HOCO	CAC	16/18/20 MHz
CACIWDTLOCO时钟(CACILCLK)	IWDTLOCO	CAC	15 kHz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick定时器时钟(SYSTICCLK)	LOCO	SysTick timer	32.768 kHz
JTAG clock (JTAGTCK)	TCK	JTAG	高达25MHz
串行线时钟(SWCLK)	SWCLK	OCD	高达25MHz
跟踪时钟(TRCLK)	MOSC/HOCO/MOCO/ LOCO/PLL	CPU-OCD	高达120MHz Division ratio: 1/2/4
TCLK引脚输出(TCLK)	1/2 TRCLK	TCLK pin	高达60MHz
Clock/buzzer output (CLKOUT)	MOSC/LOCO/MOCO/HOCO	CLKOUT pin	高达24MHz Division ratios: 1/2/4/8/16/32/64/128

Note: 设置时钟频率的限制：ICLK≥PCLKA≥PCLKB，PCLKD≥PCLKA≥PCLKB，GPTCLK≥PCLKA
ICLK ≥ FCLK
时钟频率比的限制：（N：整数，最大为64）
ICLK:FCLK = N:1, ICLK:PCLKA = N:1, ICLK:PCLKB = N:1, ICLK:PCLKC = N:1 or 1:N , ICLK:PCLKD= N:1 or 1:N, ICLK:TRCLK= N:1 or 1:N
如果使用CANFD，时钟频率比被限制为PCLKA:PCLKB=2:1。

Note: PE时对最小FCLK频率4MHz的限制。

Note: The multiplication of PLL and PLL2 should be set to be within the output frequency range of PLL and PLL2, taking the frequency of HOCO into consideration. The division of PLL and PLL2 input also should be set to be within the input frequency range of PLL and PLL2, taking the frequency of HOCO into consideration.

Note: Clocks have a permissible frequency range (See Table 8.2).
Flash memory also have a permissible operating frequency range in each wait cycle setting. (See section 43, Flash Memory)
Those clock frequency ranges must be satisfied even if the HOCO has its maximum or minimum frequency. (See section 46, Electrical Characteristics).

Note: PLL和PLL2的倍频应设置在PLL和PLL2的输出频率范围内，同时考虑HOCO的频率。PLL和PLL2输入的分频也应设置在PLL的输入频率范围内，并且
PLL2，考虑到HOCO的频率。

Note: 时钟有一个允许的频率范围（见表8.2）。
闪存在每个等待周期设置中也有一个允许的工作频率范围。（参见第43节，闪存）即使HOCO具有其最大或最小频率，也必须满足这些时钟频率范围。（见第46节，
电气特性）。

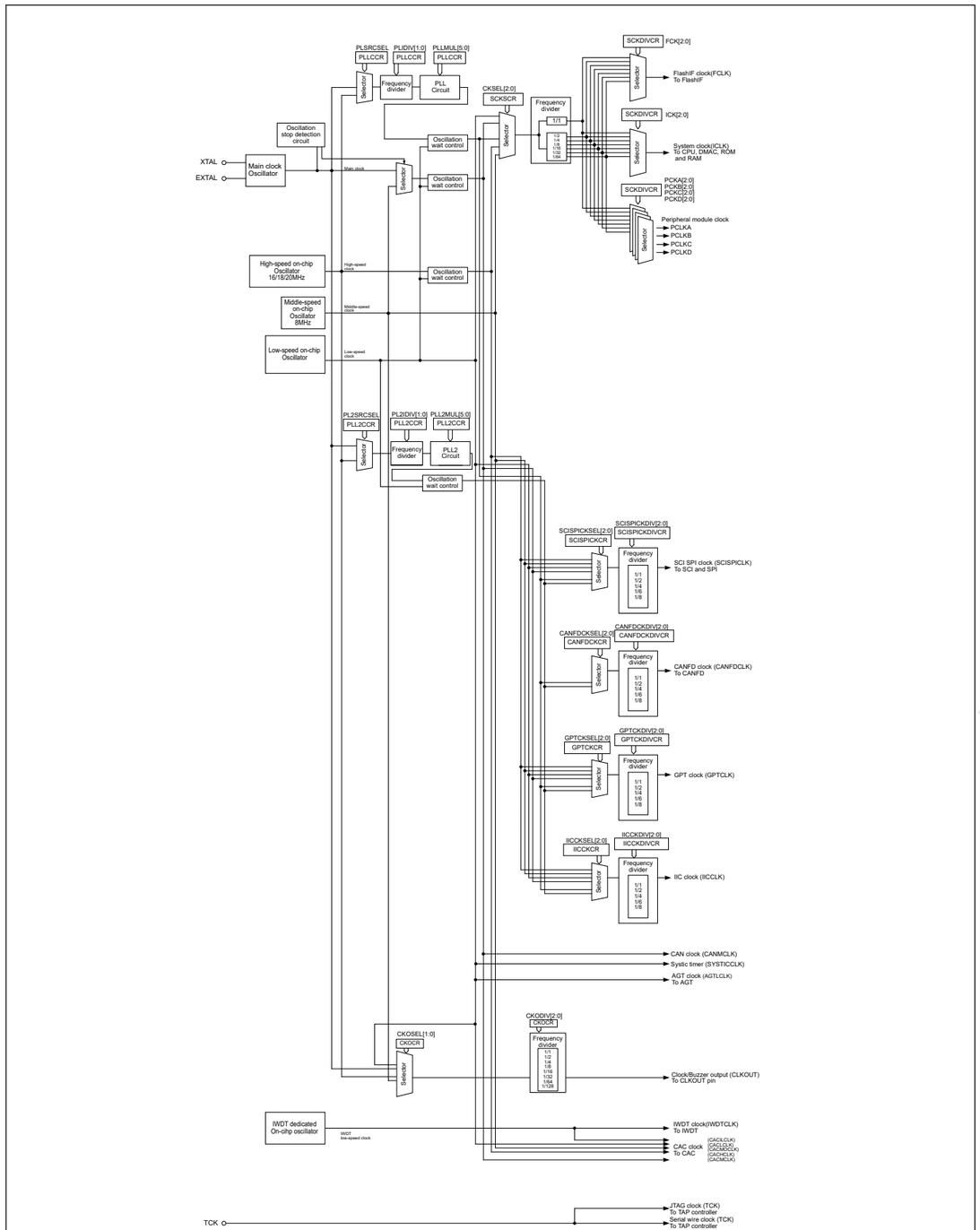


Figure 8.1 Clock generation circuit block diagram

Table 8.3 lists the input/output pins of the clock generation circuit.

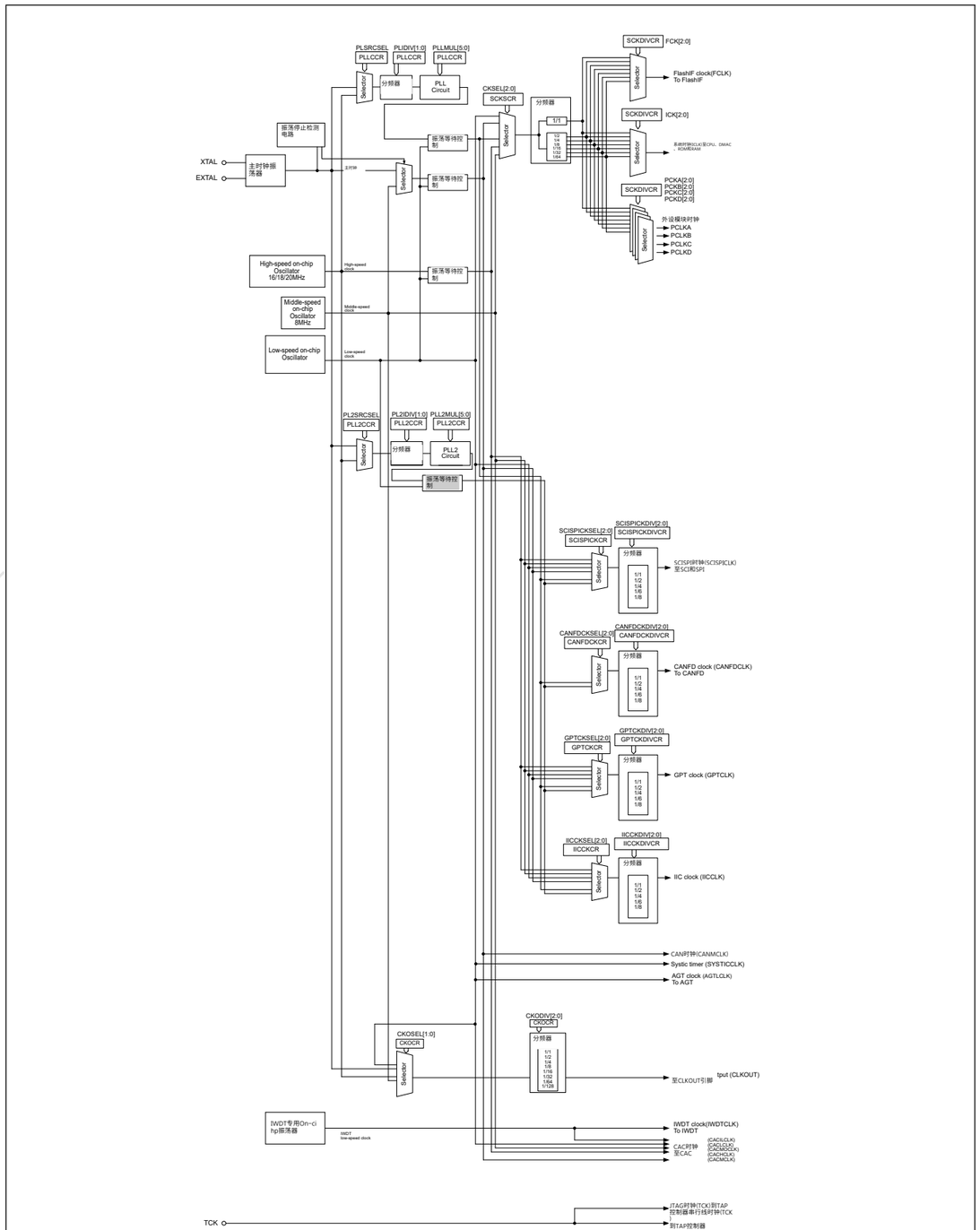


Figure 8.1 时钟产生电路框图

表8.3列出了时钟生成电路的输入输出引脚。

Table 8.3 Input/Output Pins of Clock Generation Circuit

Pin name	I/O	Description
XTAL	Output	These pins are used to connect a ceramic resonator or crystal resonator. The EXTAL pin can also be used to input an external clock. For details, see section 8.3.2. External Clock Input.
EXTAL	Input	
TCK/SWCLK	Input	This pin is used to input the clock for the JTAG/SWD
CLKOUT	Output	This pin is used to output the CLKOUT/BUZZER clock

8.2 Register Descriptions

8.2.1 CGFSAR : Clock Generation Function Security Attribute Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3C0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	NONSEC20	NONSEC19	NONSEC18	NONSEC17	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	NONSEC11	—	NONSEC09	NONSEC08	—	NONSEC06	NONSEC05	NONSEC04	NONSEC03	NONSEC02	—	NONSEC00
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC00*1	Non Secure Attribute bit 00 Target register: SCKDIVCR, SCKSCR Target factor: system clock control 0: Secure 1: Non Secure	R/W
1	—	This bit is read as 1. The write value should be 1.	R/W
2	NONSEC02*1	Non Secure Attribute bit 02 Target register: HOCOCR, HOCOUTCR Target factor: HOCO 0: Secure 1: Non Secure	R/W
3	NONSEC03*1	Non Secure Attribute bit 03 Target register: MOCOCR, MOCOUTCR Target factor: MOCO 0: Secure 1: Non Secure	R/W
4	NONSEC04	Non Secure Attribute bit 04 Target register: LOCOCR, LOCOUTCR Target factor: LOCO 0: Secure 1: Non Secure	R/W
5	NONSEC05	Non Secure Attribute bit 05 Target register: MOSCCR, MOSCWTCR, MOMCR Target factor: MOSC 0: Secure 1: Non Secure	R/W
6	NONSEC06	Non Secure Attribute bit 06 Target register: OSTDCR, OSTDSR Target factor: oscillation stop detection control 0: Secure 1: Non Secure	R/W

Table 8.3 时钟产生电路的输入输出引脚

引脚名称	I/O	Description
XTAL	Output	这些引脚用于连接陶瓷谐振器或晶体谐振器。EXTAL引脚也可用于输入外部时钟。详见8.3.2节。外部时钟输入。
EXTAL	Input	
TCK/SWCLK	Input	该引脚用于输入JTAGSWD的时钟
CLKOUT	Output	该引脚用于输出CLKOUTBUZZER时钟

8.2 注册说明

8.2.1 CGFSAR:时钟生成功能安全属性寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x3C0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	NONSEC20	NONSEC19	NONSEC18	NONSEC17	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	NONSEC11	—	NONSEC09	NONSEC08	—	NONSEC06	NONSEC05	NONSEC04	NONSEC03	NONSEC02	—	NONSEC00
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC00*1	非安全属性位00 Target register: SCKDIVCR, SCKSCR 目标因素：系统时钟控制 0：安全1：不安全	R/W
1	—	该位读取为1。写入值应为1。	R/W
2	NONSEC02*1	非安全属性位02 Target register: HOCOCR, HOCOUTCR Target factor: HOCO 0：安全1：不安全	R/W
3	NONSEC03*1	非安全属性位03 Target register: MOCOCR, MOCOUTCR Target factor: MOCO 0：安全1：不安全	R/W
4	NONSEC04	非安全属性位04 Target register: LOCOCR, LOCOUTCR 目标因素：LOCO 0：安全1：不安全	R/W
5	NONSEC05	非安全属性位05 Target register: MOSCCR, MOSCWTCR, MOMCR Target factor: MOSC 0：安全1：不安全	R/W
6	NONSEC06	非安全属性位06 Target register: OSTDCR, OSTDSR 目标因素：振荡停止检测控制 0：安全1：不安全	R/W

Bit	Symbol	Function	R/W
7	—	This bit is read as 1. The write value should be 1.	R/W
8	NONSEC08*1	Non Secure Attribute bit 08 Target register: PLLCCR, PLLCR Target factor: PLL 0: Secure 1: Non Secure	R/W
9	NONSEC09	Non Secure Attribute bit 09 Target register: PLL2CCR, PLL2CR Target factor: PLL2 0: Secure 1: Non Secure	R/W
10	—	This bit is read as 1. The write value should be 1.	R/W
11	NONSEC11	Non Secure Attribute bit 11 Target register: CKOCR Target factor: CLKOUT control 0: Secure 1: Non Secure	R/W
16:12	—	These bits are read as 1. The write value should be 1.	R/W
17	NONSEC17	Non Secure Attribute bit 17 Target register: SCISPICKDIVCR, SCISPICKCR Target factor: SCISPICLK 0: Secure 1: Non Secure	R/W
18	NONSEC18	Non Secure Attribute bit 18 Target register: CANFDCKDIVCR, CANFDCKCR Target factor: CANFDCLK 0: Secure 1: Non Secure	R/W
19	NONSEC19	Non Secure Attribute bit 19 Target register: GPTCKDIVCR, GPTCKCR Target factor: GPTCLK 0: Secure 1: Non Secure	R/W
20	NONSEC20	Non Secure Attribute bit 20 Target register: IICCKDIVCR, IICCKCR Target factor: IICCLK 0: Secure 1: Non Secure	R/W
31:21	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.
Note 1. It is recommended that these bits are configured as Non Secure when the device life cycle is NSECSD (DLMMON.DLMMON[3:0] = 0011b). See section 45.6.1. Restrictions on setting the security attribution for the details.

CGFSAR register controls the secure attribute of Clock Generation Function registers.

NONSEC00 bit (Non Secure Attribute bit 00)

This bit controls the security attribute of SCKDIVCR, SCKSCR.

NONSEC02 bit (Non Secure Attribute bit 02)

This bit controls the security attribute of HOCOCR, HOCOUTCR.

NONSEC03 bit (Non Secure Attribute bit 03)

This bit controls the security attribute of MOCOCR, MOCOUTCR.

NONSEC04 bit (Non Secure Attribute bit 04)

This bit controls the security attribute of LOCOCR, LOCOUTCR.

Bit	Symbol	Function	R/W
7	—	该位读取为1。写入值应为1。	R/W
8	NONSEC08*1	非安全属性位08 Target register: PLLCCR, PLLCR Target factor: PLL 0：安全1：不安全	R/W
9	NONSEC09	非安全属性位09 Target register: PLL2CCR, PLL2CR Target factor: PLL2 0：安全1：不安全	R/W
10	—	该位读取为1。写入值应为1。	R/W
11	NONSEC11	非安全属性位11 Target register: CKOCR 目标因素：CLKOUT控制 0：安全1：不安全	R/W
16:12	—	这些位被读取为1。写入值应为1。	R/W
17	NONSEC17	非安全属性位17 Target register: SCISPICKDIVCR, SCISPICKCR Target factor: SCISPICLK 0：安全1：不安全	R/W
18	NONSEC18	非安全属性位18目标寄存器：CANFDCKDIVCR、CANFDCKCR Target factor: CANFDCLK 0：安全1：不安全	R/W
19	NONSEC19	非安全属性位19 Target register: GPTCKDIVCR, GPTCKCR Target factor: GPTCLK 0：安全1：不安全	R/W
20	NONSEC20	非安全属性位20 Target register: IICCKDIVCR, IICCKCR Target factor: IICCLK 0：安全1：不安全	R/W
31:21	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。
注1.当器件生命周期为NSECSD(DLMMON.DLMMON[3:0]=0011b)时，建议将这些位配置为非安全。请参见第45.6.1节。设置详细信息的安全属性的限制。

CGFSAR寄存器控制时钟生成功能寄存器的安全属性。

NONSEC00位（非安全属性位00）

该位控制SCKDIVCR、SCKSCR的安全属性。

NONSEC02位（非安全属性位02）

该位控制HOCOCR、HOCOUTCR的安全属性。

NONSEC03位（非安全属性位03）

该位控制MOCOCR、MOCOUTCR的安全属性。

NONSEC04位（非安全属性位04）

该位控制LOCOCR、LOCOUTCR的安全属性。

NONSEC05 bit (Non Secure Attribute bit 05)

This bit controls the security attribute of MOSCCR, MOSCWTCR, MOMCR.

NONSEC06 bit (Non Secure Attribute bit 06)

This bit controls the security attribute of OSTDCR, OSTDSR.

NONSEC08 bit (Non Secure Attribute bit 08)

This bit controls the security attribute of PLLCCR, PLLCR.

NONSEC09 bit (Non Secure Attribute bit 09)

This bit controls the security attribute of PLL2CCR, PLL2CR.

NONSEC11 bit (Non Secure Attribute bit 11)

This bit controls the security attribute of CKOCR.

NONSEC17 bit (Non Secure Attribute bit 17)

This bit controls the security attribute of SCISPICKDIVCR, SCISPICKCR.

NONSEC18 bit (Non Secure Attribute bit 18)

This bit controls the security attribute of CANFDCKDIVCR, CANFDCKCR.

NONSEC19 bit (Non Secure Attribute bit 19)

This bit controls the security attribute of GPTCKDIVCR, GPTCKCR.

NONSEC20 bit (Non Secure Attribute bit 20)

This bit controls the security attribute of IICCKDIVCR, IICCKCR.

8.2.2 SCKDIVCR : System Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	FCK[2:0]			—	ICK[2:0]			—	—	—	—	—	RSV		
Value after reset:	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	PCKA[2:0]			—	PCKB[2:0]			—	PCKC[2:0]			—	PCKD[2:0]		
Value after reset:	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0

Bit	Symbol	Function	R/W
2:0	PCKD[2:0]*3	Peripheral Module Clock D (PCLKD) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W

NONSEC05位（非安全属性位05）

该位控制MOSCCR、MOSCWTCR、MOMCR的安全属性。

NONSEC06位（非安全属性位06）

该位控制OSTDCR、OSTDSR的安全属性。

NONSEC08位（非安全属性位08）

该位控制PLLCCR、PLLCR的安全属性。

NONSEC09位（非安全属性位09）

该位控制PLL2CCR、PLL2CR的安全属性。

NONSEC11位（非安全属性位11）

该位控制CKOCR的安全属性。

NONSEC17位（非安全属性位17）

该位控制SCISPICKDIVCR、SCISPICKCR的安全属性。

NONSEC18位（非安全属性位18）

该位控制CANFDCKDIVCR、CANFDCKCR的安全属性。

NONSEC19位（非安全属性位19）

该位控制GPTCKDIVCR、GPTCKCR的安全属性。

NONSEC20位（非安全属性位20）

该位控制IICCKDIVCR、IICCKCR的安全属性。

8.2.2 SCKDIVCR:系统时钟分频控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	FCK[2:0]			—	ICK[2:0]			—	—	—	—	—	RSV		
重置后的值：	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	PCKA[2:0]			—	PCKB[2:0]			—	PCKC[2:0]			—	PCKD[2:0]		
重置后的值：	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0

Bit	Symbol	Function	R/W
2:0	PCKD[2:0]*3	外设模块时钟D(PCLKD)选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置。	R/W
3	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
6:4	PCKC[2:0]*3	Peripheral Module Clock C (PCLKC) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
10:8	PCKB[2:0]*2	Peripheral Module Clock B (PCLKB) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
14:12	PCKA[2:0]*2	Peripheral Module Clock A (PCLKA) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
15	—	This bit is read as 0. The write value should be 0.	R/W
18:16	RSV	Reserved. Set these bits to the same value as PCKB[2:0]. 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Settings prohibited	R/W
23:19	—	These bits are read as 0. The write value should be 0.	R/W
26:24	ICK[2:0]*1*2*3*4	System Clock (ICLK) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
27	—	This bit is read as 0. The write value should be 0.	R/W
30:28	FCK[2:0]*1	FlashIF Clock (FCLK) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
6:4	PCKC[2:0]*3	外设模块时钟C(PCLKC)选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置。	R/W
7	—	该位读取为0。写入值应为0。	R/W
10:8	PCKB[2:0]*2	外设模块时钟B(PCLKB)选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置。	R/W
11	—	该位读取为0。写入值应为0。	R/W
14:12	PCKA[2:0]*2	外设模块时钟A(PCLKA)选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置。	R/W
15	—	该位读取为0。写入值应为0。	R/W
18:16	RSV	预订的。将这些位设置为与PCKB[2:0]相同的值。 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置	R/W
23:19	—	这些位被读取为0。写入值应为0。	R/W
26:24	ICK[2:0]*1*2*3*4	系统时钟(ICLK)选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置。	R/W
27	—	该位读取为0。写入值应为0。	R/W
30:28	FCK[2:0]*1	FlashIF时钟(FCLK)选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置。	R/W
31	—	该位读取为0。写入值应为0。	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. The following relation is required between the frequencies of the system clock (ICLK) and the FlashIF clock (FCLK).
ICLK:FCLK=N:1 (N: integer)
Note 2. The following relation is required between the frequencies of the system clock (ICLK) and the peripheral module clocks (PCLKA, PCLKB)
ICLK:PCLKA = N:1, ICLK:PCLKB = N:1 (N: integer)
Note 3. The following relation is required between the frequencies of the system clock (ICLK) and the peripheral module clocks (PCLKC, PCLKD):
ICLK:PCLKC,PCLKD = N:1or1:N (N: integer)
Note 4. The frequency of the system clock (ICLK) is limited to the flash wait cycle register (FLWT). See section 43, Flash Memory.

SCKDIVCR selects the frequencies of the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), FlashIF clock (FCLK).

When the PLL is selected as the clock source, you must enter the following modules in module-stop state before changing the value of this register: ADC, SCE5.

In addition, when changing any value in SCKDIVCR from a lower division ratio to a higher division ratio, wait at least 750 ns before the changing the value and change as follows according to the ICLK frequency before the change.

- When the ICLK frequency before change is more than 120 MHz:
  At first, wait 5 µs after setting ICLK frequency division ratio to 1/2, then wait 5 µs after setting SCKDIVCR.
- When the ICLK frequency before change is 120 MHz or less:
  Wait 5 µs after setting SCKDIVCR.

When changing any value from a higher division ratio to a lower division ratio, change as follows according to the changed ICLK frequency, before starting the subsequent processing.

- When the ICLK frequency after change is more than 120 MHz:
  At first, wait 1 µs after setting ICLK frequency division ratio to 1/2, then wait 1 µs after setting SCKDIVCR.
- When the ICLK frequency after change is 120 MHz or less:
  Wait 1 µs after setting SCKDIVCR.

The recommended method to measure the wait time is through software.

Be sure to consider the worst-case conditions to ensure that the required wait time elapses.

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
注1.系统时钟(ICLK)和FlashIF时钟(FCLK)的频率之间需要以下关系。
ICLK:FCLK=N:1 (N: integer)
注2.系统时钟(ICLK)和外围模块时钟(PCLKA
PCLKB)
ICLK:PCLKA = N:1, ICLK:PCLKB = N:1 (N: integer)
注3.系统时钟(ICLK)和外围模块时钟(PCLKC
PCLKD):
ICLK:PCLKC,PCLKD = N:1or1:N (N: integer)
注4.系统时钟(ICLK)的频率仅限于闪存等待周期寄存器(FLWT)。请参阅第43节，闪存。

SCKDIVCR选择系统时钟（ICLK）、外围模块时钟（PCLKA、PCLKB、PCLKC、PCLKD), FlashIF clock (FCLK).

WhenthePLLisselectedastheclocksource youmustenterthefollowingmodulesinmodule-stopstatebeforechanging thevalueofthisregister:ADC SCE5.

此外，当将SCKDIVCR中的任何值从较低的分频比更改为较高的分频比时，在更改该值之前至少等待750ns，并根据更改前的ICLK频率进行如下更改。

●变更前的ICLK频率大于120MHz时：
首先，将ICLK分频比设置为12后等待5µs，然后在设置SCKDIVCR后等待5µs。

●变更前的ICLK频率为120MHz以下时：设置SCKDIVCR后等待5µs。

将任何值从较高的分频比更改为较低的分频比时，根据更改后的值进行如下更改ICLK频率，在开始后续处理之前。

●当改变后的ICLK频率大于120MHz时：
首先，将ICLK分频比设置为12后等待1µs，然后在设置SCKDIVCR后等待1µs。

●变更后的ICLK频率为120MHz以下时：设置SCKDIVCR后等待1µs。

测量等待时间的推荐方法是通过软件。

请务必考虑最坏情况，以确保经过所需的等待时间。

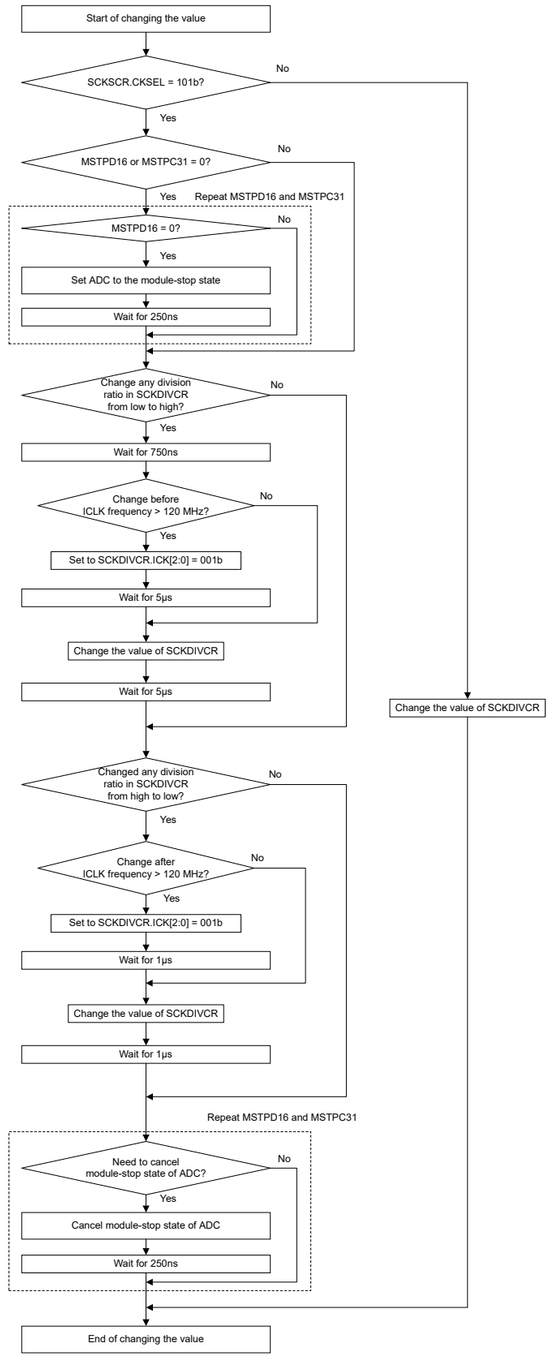


Figure 8.2 Example flow for changing the value of SCKDIVCR

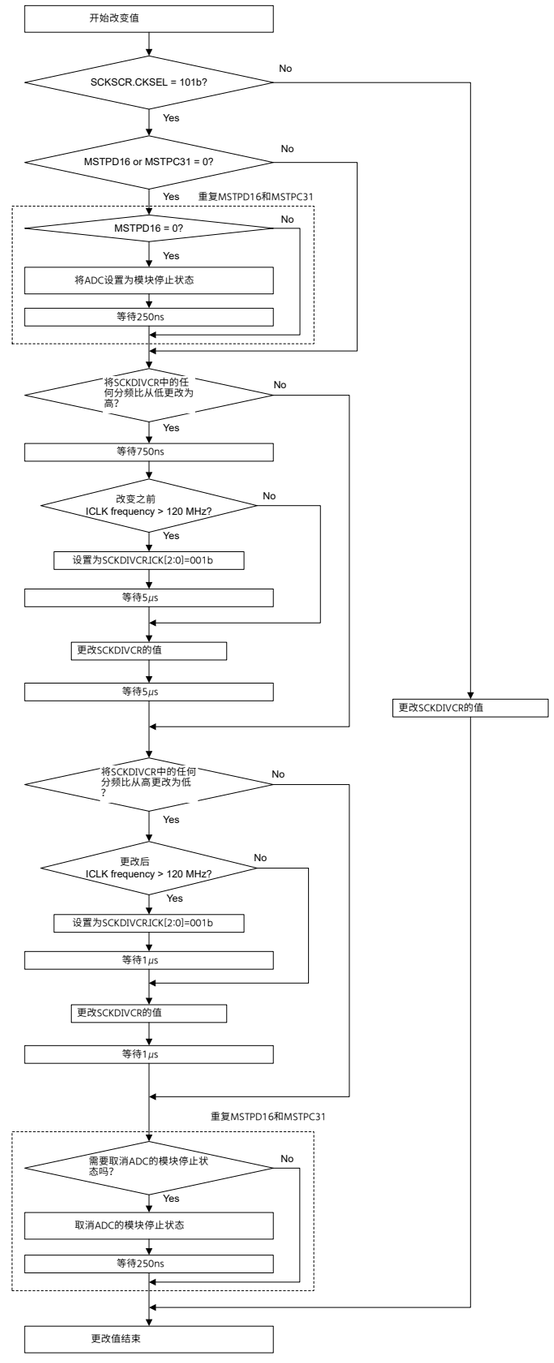


Figure 8.2 更改SCKDIVCR值的示例流程

8.2.3 SCKSCR : System Clock Source Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x026

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CKSEL[2:0]	Clock Source Select 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: Main clock oscillator (MOSC) 1 0 0: Setting prohibited 1 0 1: PLL 1 1 0: Setting prohibited 1 1 1: Setting prohibited	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The SCKSCR register selects the clock source for the system clock.

When changing the value of SCKSCR to either select or diselect the PLL, set the following modules to the module-stop state before changing the SCKSCR value: ADC, SCE5.

In addition, when changing the value of SCKSCR from the PLL to a different clock source, wait at least 750 ns before the changing the value and change as follows according to the ICLK frequency before the change.

- When the ICLK frequency before change is more than 120 MHz:
  At first, wait 5 µs after setting ICLK frequency division ratio to 1/2, then wait 5 µs after setting SCKSCR.
- When the ICLK frequency before change is 120 MHz or less:
  Wait 5 µs after setting SCKSCR.

When changing the value from a non-PLL clock source to the PLL, change as follows according to the changed ICLK frequency, before starting the subsequent processing.

- When the ICLK frequency after change is more than 120 MHz:
  At first, wait 1 µs after setting ICLK frequency division ratio to 1/2, then wait 1 µs after setting SCKSCR.
- When the ICLK frequency after change is 120 MHz or less:
  Wait 1 µs after setting SCKSCR.

The recommended method to measure the wait time is through software. Be sure to consider the worst-case conditions to ensure that the required wait time elapses.

8.2.3 SCKSCR:系统时钟源控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x026

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CKSEL[2:0]		
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CKSEL[2:0]	时钟源选择 000：HOCO001：MOCO010：LOCO011：主时钟振荡器（MOSC）100：禁止设置101：PLL110：禁止设置111：禁止设置	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

SCKSCR寄存器选择系统时钟的时钟源。

当更改SCKSCR的值以选择或取消选择PLL时，在更改SCKSCR值之前将以下模块设置为模块停止状态：ADC、SCE5。

此外，当将SCKSCR的值从PLL更改为不同的时钟源时，在更改值之前至少等待750ns，并根据更改前的ICLK频率进行如下更改。

●变更前的ICLK频率大于120MHz时：
首先，将ICLK分频比设置为12后等待5µs，然后在设置SCKSCR后等待5µs。

●更改前的ICLK频率为120MHz以下时：设置SCKSCR后等待5µs。

将值从非PLL时钟源更改为PLL时，根据更改后的ICLK频率进行如下更改，然后再开始后续处理。

●当改变后的ICLK频率大于120MHz时：
首先，将ICLK分频比设置为12后等待1µs，然后在设置SCKSCR后等待1µs。

●变更后的ICLK频率为120MHz以下时：设置SCKSCR后等待1µs。

测量等待时间的推荐方法是通过软件。请务必考虑最坏情况，以确保经过所需的等待时间。

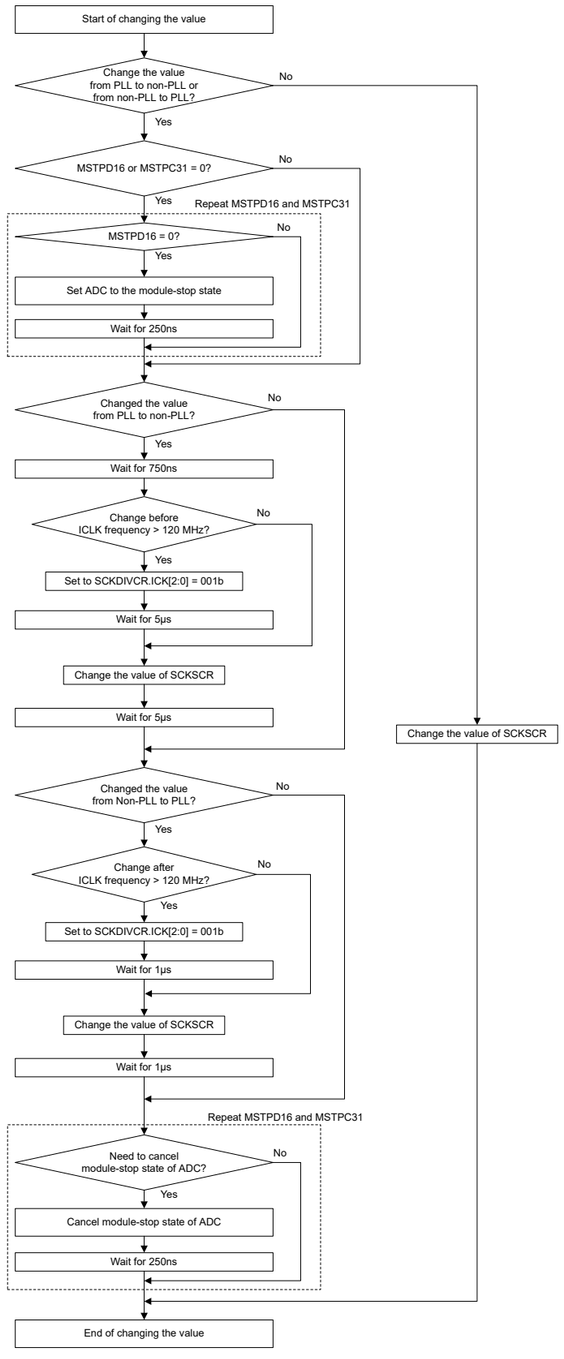


Figure 8.3 Example flow for changing the value of SCKSCR

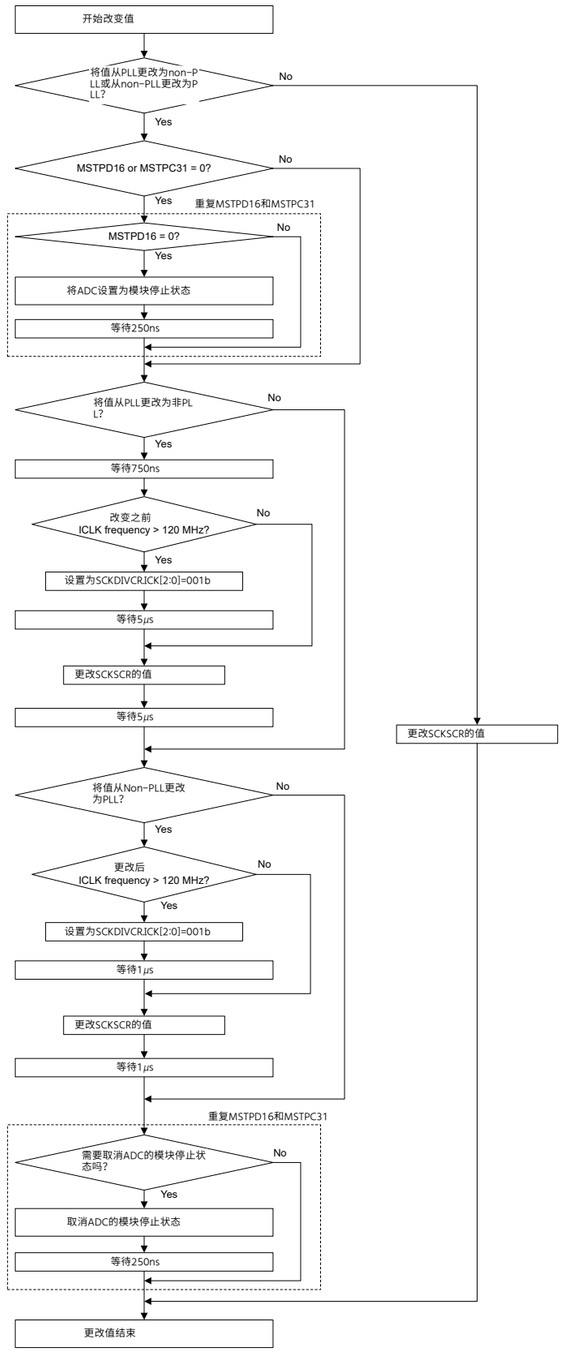


Figure 8.3 更改SCKSCR值的示例流程

CKSEL[2:0] bits (Clock Source Select)

The CKSEL[2:0] bits select the source for the following modules:

- System clock (ICLK)
- Peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD)
- FlashIF clock (FCLK)

The bits select from one of the following sources:

- Low-speed on-chip oscillator (LOCO)
- Middle-speed on-chip oscillator (MOCO)
- High-speed on-chip oscillator (HOCO)
- Main clock oscillator (MOSC)
- PLL

The operating state of each clock source is controlled not only by the clock oscillation enable settings but also by the operating modes of the product. Some clock sources might be forcibly stopped depending on the product operating mode being used.

Check the operation state of clock sources in each product operating mode, and do not select the clock source to be stopped in SCKSCR. The clock sources should be switched when there are no occurring internal asynchronous interrupt. For details, see section 10, Low Power Modes.

8.2.4 PLLCCR : PLL Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x028

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PLLMUL[5:0]						—	—	—	PLSRCSEL	—	—	PLIDIV[1:0]	
Value after reset:	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PLIDIV[1:0]*1	PLL Input Frequency Division Ratio Select 0 0: /1 0 1: /2 1 0: /3 Others: Setting prohibited.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	PLSRCSEL	PLL Clock Source Select 0: Main clock oscillator 1: HOCO	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
13:8	PLLMUL[5:0]*2	PLL Frequency Multiplication Factor Select 0x13: × 10.0 (value after reset) 0x14: × 10.5 0x15: × 11.0 ⋮ 0x1C: × 14.5 0x1D: × 15.0 0x1E: × 15.5 ⋮ 0x3A: × 29.5 0x3B: × 30.0 Others: Setting prohibited.	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

CKSEL[2:0]位（时钟源选择）

CKSEL[2:0]位选择以下模块的源：

●系统时钟（ICLK）

●外设模块时钟（PCLKA、PCLKB、PCLKC和PCLKD）

- FlashIF clock (FCLK)

这些位从以下来源之一中选择：

- Low-speed on-chip oscillator (LOCO)
- Middle-speed on-chip oscillator (MOCO)
- High-speed on-chip oscillator (HOCO)

●主时钟振荡器（MOSC）

- PLL

每个时钟源的工作状态不仅由时钟振荡使能设置控制，还由产品的工作模式控制。根据所使用的产品操作模式，某些时钟源可能会被强制停止。

检查各产品工作模式下时钟源的运行状态，不要在SCKSCR中选择要停止的时钟源。当没有发生内部异步中断时，应切换时钟源。有关详细信息，请参阅第10节，低功耗模式。

8.2.4 PLLCCR:PLL时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x028

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PLLMUL[5:0]						—	—	—	PLSRCSEL	—	—	PLIDIV[1:0]	
重置后的值：	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PLIDIV[1:0]*1	PLL输入分频比选择 0 0: /1 0 1: /2 1 0: /3 其他：禁止设置。	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	PLSRCSEL	PLL时钟源选择 0：主时钟振荡器1：H OCO	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
13:8	PLLMUL[5:0]*2	PLL倍频因子选择 0x13: × 10.0 (value after reset) 0x14: × 10.5 0x15: × 11.0 ⋮ 0x1C: × 14.5 0x1D: × 15.0 0x1E: × 15.5 ⋮ 0x3A: × 29.5 0x3B: × 30.0 其他：禁止设置。	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. PLIDIV[1:0] should be set so that the frequency of PLL input signal is within the range of section 8.1. Overview.
Note 2. PLLMUL[5:0] should be set so that the frequency of PLL output signal is within the range of section 8.1. Overview.

The PLLCCR register sets the operation of the PLL circuit.

Writing to the PLLCCR is prohibited when the PLLCR.PLLSTP bit is 0 (the PLL operates).

PLIDIV[1:0] bits (PLL Input Frequency Division Ratio Select)

These bits select the frequency division ratio of the PLL clock source.

PLSRCSEL bit (PLL Clock Source Select)

This bit selects the clock source for the PLL.

PLLMUL[5:0] bits (PLL Frequency Multiplication Factor Select)

These bits select the frequency multiplication factor of the PLL circuit.

8.2.5 PLLCR : PLL Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x02A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	PLLSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	PLLSTP	PLL Stop Control 0: PLL is operating 1: PLL is stopped.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The PLLCR register controls the operation of the PLL circuit.

PLLSTP bit (PLL Stop Control)

This bit runs or stops the PLL circuit.

If the main clock oscillator is to be selected as the clock source for the PLL by the PLLCCR.PLSRCSEL bit, the Main Clock Oscillator Wait Control Register (MOSCWTCR) must be set.

After the PLLSTP bit setting is changed to run the PLL, only use the PLL clock after confirming that the OSCSF.PLLSF bit is set to 1. That is, a fixed time for stabilization is required after starting the PLL operation. A fixed time is also required for oscillation to stop after stopping the PLL operation. Additionally, apply the following limitations when starting and stopping the PLL operation by the PLLSTP bit:

- After stopping the PLL, confirm that the OSCSF.PLLSF bit is 0 before restarting the PLL.
- Confirm that the PLL is operating and that the OSCSF.PLLSF bit is 1 before stopping the PLL.
- Regardless of whether the PLL clock is selected as the system clock, confirm that the OSCSF.PLLSF is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode after operating the PLL.

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
注1.应设置PLIDIV[1:0]，使PLL输入信号的频率在8.1节的范围内。概述。
注2.PLLMUL[5:0]应设置为使PLL输出信号的频率在8.1节的范围内。概述。

PLLCCR寄存器设置PLL电路的操作。

当PLLCR.PLLSTP位为0（PLL工作）时，禁止写入PLLCCR。

PLIDIV[1:0]位（PLL输入分频比选择）

这些位选择PLL时钟源的分频比。

PLSRCSEL位（PLL时钟源选择）

该位选择PLL的时钟源。

PLLMUL[5:0]位（PLL倍频因子选择）

这些位选择PLL电路的倍频因子。

8.2.5 PLLCR:PLL控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x02A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	PLLSTP
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	PLLSTP	PLL停止控制 0：PLL正在运行1： PLL停止。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

PLLCR寄存器控制PLL电路的操作。

PLLSTP位（PLL停止控制）

该位运行或停止PLL电路。

如果要通过PLLCCR.PLSRCSEL位选择主时钟振荡器作为PLL的时钟源，则Main
必须设置时钟振荡器等待控制寄存器(MOSCWTCR)。

更改PLLSTP位设置以运行PLL后，只有在确认OSCSF.PLLSF位设置为1后才能使用PLL时钟。即，启动PLL操作后需要固定的稳定时间。在停止PLL操作后，振荡停止也需要一段固定的时间。此外，在通过PLLSTP位启动和停止PLL操作时应用以下限制：

●停止PLL后，请确认OSCSF.PLLSF位为0，然后再重新启动PLL。

●在停止PLL之前，确认PLL正在运行并且OSCSF.PLLSF位为1。

●无论是否选择PLL时钟作为系统时钟，在执行WFI指令之前确认OSCSF.PLLSF设置为1，以便在操作PLL后将MCU置于软件待机或深度软件待机模式。

- When transitioning to Software Standby or Deep Software Standby mode after stopping the PLL, confirm that the OSCSF.PLLSF bit is cleared to 0 before executing a WFI instruction.

Writing 1 to the PLLSTP bit is prohibited when SCKSCR.CKSEL[2:0] = 101 (system clock source = PLL).

Confirm the following conditions before writing 0 to PLLSTP:

- When PLL source clock = MOSC: MOSCCR.MOSTP = 0 (MOSC is enabled)
- When PLL source clock = HOCO: HOCOCR.HCSTP = 0 (HOCO is enabled).

8.2.6 PLL2CCR : PLL2 Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x048

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PLL2MUL[5:0]						—	—	—	PL2SRCSEL	—	—	PL2IDIV[1:0]	
Value after reset:	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PL2IDIV[1:0]*1	PLL2 Input Frequency Division Ratio Select 0 0: /1 (value after reset) 0 1: /2 1 0: /3 Others: Setting prohibited.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	PL2SRCSEL	PLL2 Clock Source Select 0: Main clock oscillator 1: HOCO	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
13:8	PLL2MUL[5:0]*2	PLL2 Frequency Multiplication Factor Select 0x13: × 10.0 (value after reset) 0x14: × 10.5 0x15: × 11.0 ⋮ 0x1C: × 14.5 0x1D: × 15.0 0x1E: × 15.5 ⋮ 0x3A: × 29.5 0x3B: × 30.0 Others: Setting prohibited.	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. PL2IDIV[1:0] should be set so that the frequency of PLL2 input signal is within the range of section 8.1. Overview.

Note 2. PLL2MUL[5:0] should be set so that the frequency of PLL2 output signal is within the range of section 8.1. Overview.

The PLL2CCR register sets the operation of the PLL2 circuit.

Writing to the PLL2CCR register is prohibited when the PLL2CR.PLL2STP bit is 0 (the PLL2 operates).

PL2IDIV[1:0] bits (PLL2 Input Frequency Division Ratio Select)

These bits select the frequency division ratio of the PLL2 clock source.

●在停止PLL后转换到软件待机或深度软件待机模式时，请确认OSCSF.PLLSF位在执行WFI指令之前被清除为0。

当SCKSCR.CKSEL[2:0]=101（系统时钟源=PLL）时，禁止向PLLSTP位写入1。

在将0写入PLLSTP之前，请确认以下条件：

●当PLL源时钟=MOSC时：MOSCCR.MOSTP=0（启用MOSC）

●当PLL源时钟=HOCO时：HOCOCR.HCSTP=0（启用HOCO）。

8.2.6 PLL2CCR:PLL2时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x048

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PLL2MUL[5:0]						—	—	—	PL2SRCSEL	—	—	PL2IDIV[1:0]	
重置后的值：	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PL2IDIV[1:0]*1	PLL2输入分频比选择 0 0: /1 (value after reset) 0 1: /2 1 0: /3 其他：禁止设置。	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	PL2SRCSEL	PLL2时钟源选择 0：主时钟振荡器1：HOCO	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
13:8	PLL2MUL[5:0]*2	PLL2倍频因子选择 0x13: × 10.0 (value after reset) 0x14: × 10.5 0x15: × 11.0 ⋮ 0x1C: × 14.5 0x1D: × 15.0 0x1E: × 15.5 ⋮ 0x3A: × 29.5 0x3B: × 30.0 其他：禁止设置。	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
- 允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

注1.应设置PL2IDIV[1:0]，使PLL2输入信号的频率在8.1节的范围内。概述。

注2.PLL2MUL[5:0]应设置为使PLL2输出信号的频率在8.1节的范围内。概述。

PLL2CCR寄存器设置PLL2电路的操作。

当PLL2CR.PLL2STP位为0（PLL2工作）时，禁止写入PLL2CCR寄存器。

PL2IDIV[1:0]位（PLL2输入分频比选择）

这些位选择PLL2时钟源的分频比。

PL2SRCSEL bit (PLL2 Clock Source Select)

This bit selects the clock source for the PLL2.

PLL2MUL[5:0] bits (PLL2 Frequency Multiplication Factor Select)

These bits select the frequency multiplication factor of the PLL2 circuit.

8.2.7 PLL2CR : PLL2 Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x04A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	PLL2STP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	PLL2STP	PLL2 Stop Control 0: PLL2 is operating 1: PLL2 is stopped.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The PLL2CR register controls the operation of the PLL2 circuit.

PLL2STP bit (PLL2 Stop Control)

This bit runs or stops the PLL2 circuit.

If the main clock oscillator is to be selected as the clock source for the PLL2 by the PLL2CCR.PL2SRCSEL bit, the Main Clock Oscillator Wait Control Register (MOSCWTCR) must be set.

After the PLL2STP bit setting is changed to run the PLL2, only use the PLL2 clock after confirming that the OSCSF.PLL2SF bit is set to 1. That is, a fixed time for stabilization is required after starting the PLL2 operation. A fixed time is also required for oscillation to stop after stopping the PLL2 operation. Additionally, apply the following limitations when starting and stopping the PLL2 operation by the PLL2STP bit:

- After stopping the PLL2, confirm that the OSCSF.PLL2SF bit is 0 before restarting the PLL2.
- Confirm that the PLL2 is operating and that the OSCSF.PLL2SF bit is 1 before stopping the PLL2.
- Confirm that the OSCSF.PLL2SF bit is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode after operating the PLL2.
- When transitioning to Software Standby or Deep Software Standby mode after stopping the PLL2, confirm that the OSCSF.PLL2SF bit is cleared to 0 before executing a WFI instruction.

Confirm the following conditions before writing 0 to PLL2STP:

- When the PLL2 source clock = MOSC: MOSCCR.MOSTP = 0 (MOSC is enabled)
- When the PLL2 source clock = HOCO: HOCOCR.HCSTP = 0 (HOCO is enabled).

PL2SRCSEL位（PLL2时钟源选择）

该位选择PLL2的时钟源。

PLL2MUL[5:0]位（PLL2倍频因子选择）

这些位选择PLL2电路的倍频因子。

8.2.7 PLL2CR：PLL2控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x04A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	PLL2STP
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	PLL2STP	PLL2停止控制 0：PLL2正在运行1： PLL2停止。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

PLL2CR寄存器控制PLL2电路的操作。

PLL2STP位（PLL2停止控制）

该位运行或停止PLL2电路。

如果要通过PLL2CCR.PL2SRCSEL位选择主时钟振荡器作为PLL2的时钟源，则Main
必须设置时钟振荡器等待控制寄存器(MOSCWTCR)。

更改PLL2STP位设置运行PLL2后，确认
OSCSF.PLL2SF位设置为1。也就是说，在启动PLL2操作后需要一个固定的稳定时间。在停止PLL2操作后，振荡停止也需要一个固定的时间。此外，在通过PLL2STP位启动和停止PLL2操作时应用以下限制：

●停止PLL2后，确认OSCSF.PLL2SF位为0，再重启PLL2。

●在停止PLL2之前，确认PLL2正在运行并且OSCSF.PLL2SF位为1。

●在操作PLL2后，在执行WFI指令以将MCU置于软件待机或深度软件待机模式之前，确认OSCSF.PLL2SF位设置为1。

●在停止PLL2后转换到软件待机或深度软件待机模式时，请确认OSCSF.PLL2SF位在执行WFI指令之前被清除为0。

在将0写入PLL2STP之前，请确认以下条件：

●当PLL2源时钟=MOSC时：MOSCCR.MOSTP=0（启用MOSC）

●当PLL2源时钟=HOCO时：HOCOCR.HCSTP=0（启用HOCO）。

8.2.8 MOSCCR : Main Clock Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x032

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MOSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	MOSTP	Main Clock Oscillator Stop 0: Operate the main clock oscillator*1 1: Stop the main clock oscillator	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. MOMCR register must be set before setting MOSTP to 0.

The MOSCCR register controls the main clock oscillator.

MOSTP bit (Main Clock Oscillator Stop)

The MOSTP bit starts or stops the main clock oscillator.

When changing the value of the MOSTP bit, execute subsequent instructions only after reading the bit to check that the value is updated.

When using the main clock, the Main Clock Oscillator Mode Oscillation Control Register (MOMCR) and the Main Clock Oscillator Wait Control Register (MOSCWTCR) must be set before setting MOSTP to 0. After setting the MOSTP bit to 0, confirm that the OSCSF.MOSCSF bit is set to 1 before using the main clock oscillator.

A fixed stabilization wait time is required after setting the main clock oscillator to start operation. A fixed wait time is also required for oscillation to stop after stopping the main clock oscillator.

The following restrictions apply when starting and stopping operation:

- After stopping the main clock oscillator, confirm that the OSCSF.MOSCSF bit is 0 before restarting the main clock oscillator
- Confirm that the main clock oscillator operates and that the OSCSF.MOSCSF bit is 1 before stopping the main clock oscillator
- Regardless of whether the main clock oscillator is selected as the system clock, confirm that the OSCSF.MOSCSF bit is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode.
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the main clock oscillator, confirm that the OSCSF.MOSCSF bit is set to 0 before executing the WFI instruction.

Writing 1 to MOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC).
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL)
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and PLLCR.PLLSTP = 0 (PLL is operating)
- PLL2CCR.PL2SRCSEL = 0 (PLL2 source clock = MOSC) and PLL2CR.PLL2STP = 0 (PLL2 is operating)

8.2.8 MOSCCR:主时钟振荡器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x032

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MOSTP
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	MOSTP	主时钟振荡器停止 0:运行主时钟振荡器*1 1：停止主时钟振荡器	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.在将MOSTP设置为0之前，必须设置MOMCR寄存器。

MOSCCR寄存器控制主时钟振荡器。

MOSTP位（主时钟振荡器停止）

MOSTP位启动或停止主时钟振荡器。

更改MOSTP位的值时，仅在读取该位后执行后续指令以检查该值是否已更新。

使用主时钟时，必须先设置主时钟振荡器模式振荡控制寄存器(MOMCR)和主时钟振荡器等待控制寄存器(MOSCWTCR)，然后再将MOSTP设置为0。将MOSTP位设置为0后，确认OSCSF。MOSCSF位在使用主时钟振荡器之前设置为1。

设置主时钟振荡器开始工作后，需要一个固定的稳定等待时间。停止主时钟振荡器后，振荡停止也需要一个固定的等待时间。

启动和停止操作时适用以下限制：

●停止主时钟振荡器后，请确认OSCSF.MOSCSF位为0，然后再重新启动主时钟振荡器

●在停止主时钟振荡器之前，确认主时钟振荡器工作并且OSCSF.MOSCSF位为1

●无论是否选择主时钟振荡器作为系统时钟，在执行WFI指令之前确认OSCSF.MOSCSF位设置为1，将MCU置于软件待机或深度软件待机模式。

●当转换到软件待机或深度软件待机模式是按照设置停止主时钟振荡器时，在执行WFI指令之前确认OSCSF.MOSCSF位设置为0。

在以下情况下禁止向MOSTP写入1：

●SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）。

●PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）和SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）

●PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）和PLLCR.PLLSTP=0（PLL正在运行）

●PLL2CCR.PL2SRCSEL=0（PLL2源时钟=MOSC）和PLL2CR.PLL2STP=0（PLL2正在运行）

8.2.9 LOCOCR : Low-Speed On-Chip Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x490

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	LCSTP	LOCO Stop 0: Operate the LOCO clock 1: Stop the LOCO clock	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The LOCOCR register controls the LOCO clock.

LCSTP bit (LOCO Stop)

The LCSTP bit starts or stops the LOCO clock.

After setting the LCSTP bit to 0 to start the LOCO clock, only use the clock after the LOCO clock-oscillation stabilization wait time (t_{LOCOWT}) elapses. A fixed stabilization wait time is required after setting the LOCO clock to start operation. A fixed wait time is also required after setting the LOCO clock to stop.

The following restrictions apply when starting and stopping operation:

- After stopping the LOCO clock, allow a stop interval of at least 5 LOCO clock cycles before restarting it
- Confirm that LOCO oscillation is stable before stopping the LOCO clock
- Regardless of whether the LOCO is selected as the system clock, confirm that LOCO oscillation is stable before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the LOCO clock, wait for at least 3 LOCO cycles before executing the WFI instruction.

Writing 1 to LCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 010b (system clock source = LOCO).

Because the LOCO clock measures the wait time for other oscillators, it continues to oscillate while measuring this time, regardless of the setting in LOCOCR.LCSTP. As a result, the LOCO clock might be unintentionally supplied even when the LCSTP is set to stop.

8.2.10 HOCOCR : High-Speed On-Chip Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x036

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	HCSTP
Value after reset:	0	0	0	0	0	0	0	0/1*1

8.2.9 LOCOCR：低速片上振荡器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x490

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LCSTP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	LCSTP	机车站 0：运行LOCO时钟1：停止LOCO时钟	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

LOCOCR寄存器控制LOCO时钟。

LCSTP bit (LOCO Stop)

LCSTP位启动或停止LOCO时钟。

将LCSTP位设置为0以启动LOCO时钟后，仅在LOCO时钟振荡稳定等待时间(tLOCOWT)过去后使用时钟。设置LOCO时钟开始运行后，需要一个固定的稳定等待时间。将LOCO时钟设置为停止后，还需要一个固定的等待时间。

启动和停止操作时适用以下限制：

●停止LOCO时钟后，在重新启动之前允许至少5个LOCO时钟周期的停止间隔

●在停止LOCO时钟之前确认LOCO振荡稳定

●无论是否选择LOCO作为系统时钟，在执行WFI指令将MCU置于软件待机或深度软件待机模式之前，请确认LOCO振荡稳定

●当转换到软件待机或深度软件待机模式是按照设置停止LOCO时钟时，在执行WFI指令之前至少等待3个LOCO周期。

在以下情况下禁止向LCSTP写入1：

●SCKSCR.CKSEL[2:0]=010b（系统时钟源=LOCO）。

因为LOCO时钟测量其他振荡器的等待时间，所以无论LOCOCR.LCSTP中的设置如何，它都会在测量该时间时继续振荡。因此，即使LCSTP设置为停止，也可能会无意中提供LOCO时钟。

8.2.10 HOCOCR:高速片上振荡器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x036

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	HCSTP
重置后的值：	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Function	R/W
0	HCSTP	HOCO Stop 0: Operate the HOCO clock *2 1: Stop the HOCO clock	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.
Note 2. If you are using the HOCO (HCSTP = 0), set the OFS1.HOCOFRQ0[1:0] bit to an optimum value.

The HOCOCR register controls the HOCO clock.

HCSTP bit (HOCO Stop)

The HCSTP bit starts or stops the HOCO clock.

After setting the HCSTP bit to 0 to start the HOCO clock, confirm that the OSCSF.HOCOSF is set to 1 before using the clock. When OFS1.HOCOEN is set to 0, confirm that OSCSF.HOCOSF is also set to 1 before using the HOCO clock. A fixed stabilization wait time is required after setting the HOCO clock to start operation. A fixed wait time is also required after setting the HOCO clock to stop.

The following limitations apply when starting and stopping operation:

- After stopping the HOCO clock, confirm that the OSCSF.HOCOSF is 0 before restarting the HOCO clock.
- Confirm that the HOCO clock operates and that the OSCSF.HOCOSF is 1 before stopping the HOCO clock.
- Regardless of whether the HOCO clock is selected as the system clock, confirm that the OSCSF.HOCOSF is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode after setting HOCO operation with the HCSTP bit.
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting of the HOCO clock to stop, confirm that the OSCSF.HOCOSF is set to 0 after setting the HOCO clock and before executing the WFI instruction.

Writing 1 to HCSTP is prohibited under the following conditions:

- SCKSCR.CKSEL[2:0] = 000b (system clock source = HOCO).
- PLLCCR.PLSRCSEL = 1 (PLL source clock = HOCO) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL)
- PLLCCR.PLSRCSEL = 1 (PLL source clock = HOCO) and PLLCR.PLLSTP = 0 (PLL is operating)
- PLL2CCR.PL2SRCSEL = 1 (PLL2 source clock = HOCO) and PLL2CR.PLL2STP = 0 (PLL2 is operating)

8.2.11 MOCOCR : Middle-Speed On-Chip Oscillator Control Register

Base address: SYSC = 0x4001_E000
Offset address: 0x038

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MCSTP	MOCO Stop 0: MOCO clock is operating 1: MOCO clock is stopped	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
0	HCSTP	HOCO Stop 0：运行HOCO时钟*2 1：停止HOCO时钟	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.OFS1.HOCOEN位为0时复位后的HCSTP位值为0。OFS1.HOCOEN位为1时为1。
注2.如果您使用HOCO(HCSTP=0)，请将OFS1.HOCOFRQ0[1:0]位设置为最佳值。

HOCOCR寄存器控制HOCO时钟。

HCSTP bit (HOCO Stop)

HCSTP位启动或停止HOCO时钟。

将HCSTP位设置为0以启动HOCO时钟后，在使用时钟之前确认OSCSF.HOCOSF设置为1。当OFS1.HOCOEN设置为0时，请在使用HOCO时钟之前确认OSCSF.HOCOSF也设置为1。设置HOCO时钟开始运行后，需要一个固定的稳定等待时间。将HOCO时钟设置为停止后，还需要一个固定的等待时间。

启动和停止操作时适用以下限制：

●停止HOCO时钟后，确认OSCSF.HOCOSF为0，再重新启动HOCO时钟。

●在停止HOCO时钟之前，请确认HOCO时钟运行并且OSCSF.HOCOSF为1。

●无论是否选择HOCO时钟作为系统时钟，确认OSCSF.HOCOSF设置为1
在使用HCSTP位设置HOCO操作后，执行WFI指令以将MCU置于软件待机或深度软件待机模式之前。

●当转换到软件待机或深度软件待机模式是跟随HOCO时钟的设置停止时，在设置HOCO时钟之后和执行WFI指令之前确认OSCSF.HOCOSF设置为0。

在以下情况下禁止向HCSTP写入1：

●SCKSCR.CKSEL[2:0]=000b（系统时钟源=HOCO）。

●PLLCCR.PLSRCSEL=1（PLL源时钟=HOCO）和SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）

●PLLCCR.PLSRCSEL=1（PLL源时钟=HOCO）和PLLCR.PLLSTP=0（PLL正在运行）

●PLL2CCR.PL2SRCSEL=1（PLL2源时钟=HOCO）和PLL2CR.PLL2STP=0（PLL2正在运行）

8.2.11 MOCOCR:中速片上振荡器控制寄存器

Base address: SYSC = 0x4001_E000
Offset address: 0x038

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MCSTP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MCSTP	MOCO Stop 0：MOCO时钟运行1：MOCO时钟停止	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The MOCOCR register controls the MOCO clock.

MCSTP bit (MOCO Stop)

The MCSTP bit starts or stops the MOCO clock.

After setting MCSTP to 0, use the MOCO clock only after the MOCO clock oscillation stabilization time (t_{MOCOWT}) elapses. A fixed stabilization wait time is required after setting the MOCO clock to start operation. A fixed wait time is also required for oscillation to stop after setting the MOCO clock to stop operation.

The following restrictions apply when starting and stopping the oscillator:

- After stopping the MOCO clock, allow a stop interval of at least 5 MOCO clock cycles before restarting it
- Confirm that MOCO clock oscillation is stable before stopping the MOCO clock
- Regardless of whether the MOCO clock is selected as the system clock, confirm that MOCO clock oscillation is stable before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the MOCO clock, wait for at least 3 MOCO clock cycles before executing the WFI instruction.

Writing 1 to MCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 001b (system clock source = MOCO).

Writing 1 to the MCSTP bit (stopping the MOCO) is prohibited if oscillation stop detection is enabled in the Oscillation Stop Detection Control Register (OSTDCR.OSTDE).

8.2.12 OSCSF : Oscillation Stabilization Flag Register

Base address: SYSC = 0x4001_E000

Offset address: 0x03C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	PLL2SF	PLLSF	—	MOSCSF	—	—	HOCOSF
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Function	R/W
0	HOCOSF	HOCO Clock Oscillation Stabilization Flag 0: The HOCO clock is stopped or is not yet stable 1: The HOCO clock is stable, so is available for use as the system clock	R
2:1	—	These bits are read as 0.	R
3	MOSCSF	Main Clock Oscillation Stabilization Flag 0: The main clock oscillator is stopped (MOSTP = 1) or is not yet stable*2 1: The main clock oscillator is stable, so is available for use as the system clock	R
4	—	This bit is read as 0.	R
5	PLLSF	PLL Clock Oscillation Stabilization Flag 0: The PLL clock is stopped, or oscillation of the PLL clock is not stable yet 1: The PLL clock is stable, so is available for use as the system clock	R
6	PLL2SF	PLL2 Clock Oscillation Stabilization Flag 0: The PLL2 clock is stopped, or oscillation of the PLL2 clock is not stable yet 1: The PLL2 clock is stable	R
7	—	These bits are read as 0.	R

Note 1. The value after reset depends on the OFS1.HOCOEN setting.

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
● 忽略非安全写入访问，不会生成TrustZone访问错误。
如果安全属性配置为非安全：●
允许安全和非安全访问。

MOCOCR寄存器控制MOCO时钟。

MCSTP bit (MOCO Stop)

MCSTP位启动或停止MOCO时钟。

将MCSTP设置为0后，仅在MOCO时钟振荡稳定时间(tMOCOWT)过去后使用MOCO时钟。设置MOCO时钟开始运行后，需要一个固定的稳定等待时间。在将MOCO时钟设置为停止操作后，振荡停止也需要一个固定的等待时间。

启动和停止振荡器时适用以下限制：

●停止MOCO时钟后，在重新启动之前允许至少5个MOCO时钟周期的停止间隔

●确认MOCO时钟振荡稳定后再停止MOCO时钟

●无论是否选择MOCO时钟作为系统时钟，在执行WFI指令将MCU置于软件待机或深度软件待机模式之前，请确认MOCO时钟振荡稳定

●当按照设置转换到软件待机或深度软件待机模式以停止MOCO时钟时，请等待至少3个MOCO时钟周期，然后再执行WFI指令。

在以下情况下禁止向MCSTP写入1：

●SCKSCR.CKSEL[2:0]=001b（系统时钟源=MOCO）。

如果在Oscillation中使能了振荡停止检测，则禁止向MCSTP位写入1（停止MOCO）
停止检测控制寄存器(OSTDCR.OSTDE)。

8.2.12 OSCSF:振荡稳定标志寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x03C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	PLL2SF	PLLSF	—	MOSCSF	—	—	HOCOSF
重置后的值：	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Function	R/W
0	HOCOSF	HOCO时钟振荡稳定标志 0：HOCO时钟停止或尚未稳定1：HOCO时钟稳定，可用作系统时钟	R
2:1	—	这些位读为0。	R
3	MOSCSF	主时钟振荡稳定标志 0：主时钟振荡器停止（MOSTP=1）或尚未稳定*2 1：主时钟振荡器稳定，可作为系统时钟使用	R
4	—	该位读为0。	R
5	PLLSF	PLL时钟振荡稳定标志 0：PLL时钟停止，或PLL时钟振荡尚未稳定1：PLL时钟稳定，可用作系统时钟	R
6	PLL2SF	PLL2时钟振荡稳定标志 0：PLL2时钟停止，或PLL2时钟振荡尚未稳定1：PLL2时钟稳定	R
7	—	这些位读为0。	R

注1.复位后的值取决于OFS1.HOCOEN的设置。

When OFS1.HOCOEN = 1 (disable HOCO), the value after reset of HOCOSF is 0.
When OFS1.HOCOEN = 0 (enable HOCO), the HOCOSF value is set to 0 immediately after reset is released, and the HOCOSF value is set to 1 after the HOCO oscillation stabilization wait time elapses.

Note 2. This is true when an appropriate value is set in the Wait Control register for the main clock oscillator. If the wait time value is not sufficient, the oscillation stabilization flag is set to 1 and supply of the clock signal to the internal circuits starts before oscillation is stable.

This register is not controlled by CGFSAR register.

The OSCSF register contains flags to indicate the operating status of the counters in the oscillation stabilization wait circuits for the individual oscillators. After oscillation starts, these counters measure the wait time until each oscillator output clock is supplied to the internal circuits. An overflow of a counter indicates that the clock supply is stable and available for the associated circuit.

HOCOSF flag (HOCO Clock Oscillation Stabilization Flag)

The HOCOSF flag indicates the operating status of the counter that measures the wait time for the high-speed clock oscillator (HOCO). When OFS1.HOCOEN is set to 0, confirm that OSCSF.HOCOSF is set to 1 before using the HOCO clock.

[Setting condition]

- When the HOCO clock is stopped and the HOCOCR.HCSTP bit is set to 0, and then the HOCO oscillation stabilization time is counted by the LOCO clock and supply of the HOCO clock within the MCU is started. For the HOCO oscillation stabilization time, see section 46, Electrical Characteristics.

[Clearing condition]

- When the HOCO clock is operating and then is deactivated because the HOCOCR.HCSTP bit is set to 1.

MOSCSF flag (Main Clock Oscillation Stabilization Flag)

The MOSCSF flag indicates the operating status of the counter that measures the wait time for the main clock oscillator.

[Setting condition]

- When the main clock oscillator is stopped and the MOSCCR.MOSTP bit is set to 0, and then the number of LOCO clock cycles corresponding to the setting of the MOSCWTCR register is counted and supply of the main clock within the MCU is started.

[Clearing condition]

- When the main clock oscillator is operating and then is deactivated because the MOSCCR.MOSTP bit is set to 1.

PLLSF flag (PLL Clock Oscillation Stabilization Flag)

The PLLSF flag indicates the operating state of the counter that measures the wait time of the PLL.

[Setting condition]

- When the PLL is stopped and the PLLCR.PLLSTP bit is set to 0, and then the PLL oscillation stabilization time is counted by the LOCO clock and supply of the PLL clock within the MCU is started. If oscillation by the PLL clock source is not stable when the PLLCR.PLLSTP bit is set to 0, counting of the LOCO cycles continues even after the PLL clock source oscillation is stabilized. For the PLL oscillation stabilization time, see section 46, Electrical Characteristics.

[Clearing condition]

- When the PLL is operating and then is deactivated because the PLLCR.PLLSTP bit is set to 1.

PLL2SF flag (PLL2 Clock Oscillation Stabilization Flag)

The PLL2SF flag indicates the operating state of the counter that measures the wait time of the PLL2.

[Setting condition]

- When the PLL2 is stopped and the PLL2CR.PLL2STP bit is set to 0, and then the PLL2 oscillation stabilization time is counted by the LOCO clock and supply of the PLL2 clock within the MCU is started. If oscillation by the PLL2 clock source is not stable when the PLL2CR.PLL2STP bit is set to 0, counting of the LOCO cycles continues even after the PLL2 clock source oscillation is stabilized. For the PLL2 oscillation stabilization time, see section 46, Electrical Characteristics.

当OFS1.HOCOEN=1（禁用HOCO）时，HOCOSF复位后的值为0。
当OFS1.HOCOEN=0（启用HOCO）时，释放复位后立即将HOCOSF值设置为0，并在经过HOCO振荡稳定等待时间后将HOCOSF值设置为1。

注2.当主时钟振荡器的等待控制寄存器中设置了适当的值时，这是正确的。如果等待时间值不够，则将振荡稳定标志设置为1，并在振荡稳定之前开始向内部电路提供时钟信号。

该寄存器不受CGFSAR寄存器控制。

OSCSF寄存器包含用于指示各个振荡器的振荡稳定等待电路中的计数器的操作状态的标志。振荡开始后，这些计数器测量等待时间，直到每个振荡器输出时钟被提供给内部电路。计数器溢出表明时钟供应稳定并可用于相关电路。

HOCOSF标志（HOCO时钟振荡稳定标志）

HOCOSF标志指示测量高速时钟振荡器(HOCO)等待时间的计数器的操作状态。当OFS1.HOCOEN设置为0时，请在使用HOCO时钟之前确认OSCSF.HOCOSF设置为1。

[Setting condition]

●当HOCO时钟停止并且HOCOCR.HCSTP位设置为0时，然后通过LOCO时钟计算HOCO振荡稳定时间并开始提供MCU内的HOCO时钟。关于HOCO振荡稳定时间，请参见第46节，电气特性。

[Clearing condition]

●HOCO时钟正在运行，然后由于HOCOCR.HCSTP位设置为1而被停用。

MOSCSF标志（主时钟振荡稳定标志）

MOSCSF标志指示测量主时钟振荡器等待时间的计数器的操作状态。

[Setting condition]

●当主时钟振荡器停止并且MOSCCR.MOSTP位设置为0，然后LOCO的个数
与MOSCWTCR寄存器的设置相对应的时钟周期被计数，并开始提供MCU内的主时钟。

[Clearing condition]

●当主时钟振荡器正在运行，然后因为MOSCCR.MOSTP位被设置为1而被禁用时。

PLLSF标志（PLL时钟振荡稳定标志）

PLLSF标志指示测量PLL等待时间的计数器的操作状态。

[Setting condition]

●当PLL停止并且PLLCR.PLLSTP位设置为0时，然后PLL振荡稳定时间由LOCO时钟计数并开始提供MCU内的PLL时钟。如果当PLLCR.PLLSTP位设置为0时PLL时钟源的振荡不稳定，即使PLL时钟源振荡稳定后，LOCO周期的计数也会继续。关于PLL振荡稳定时间，请参见第46节，电气特性。

[Clearing condition]

●当PLL正在运行然后因为PLLCR.PLLSTP位设置为1而被停用时。

PLL2SF标志（PLL2时钟振荡稳定标志）

PLL2SF标志指示测量PLL2等待时间的计数器的操作状态。

[Setting condition]

●当PLL2停止并且PLL2CR.PLL2STP位设置为0时，然后PLL2振荡稳定时间由LOCO时钟计数并开始提供MCU内的PLL2时钟。如果当PLL2CR.PLL2STP位设置为0时PLL2时钟源的振荡不稳定，即使在PLL2时钟源振荡稳定后，LOCO周期的计数也会继续。有关PLL2振荡稳定时间，请参见第46节，电气

Characteristics.

[Clearing condition]

- When the PLL2 is operating and then is deactivated because the PLL2CR.PLL2STP bit is set to 1.

8.2.13 OSTDCR : Oscillation Stop Detection Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x040

Bit position:	7	6	5	4	3	2	1	0
Bit field:	OSTDE	—	—	—	—	—	—	OSTDIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OSTDIE	Oscillation Stop Detection Interrupt Enable 0: Disable oscillation stop detection interrupt (do not notify the POEG) 1: Enable oscillation stop detection interrupt (notify the POEG)	R/W
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	OSTDE	Oscillation Stop Detection Function Enable 0: Disable oscillation stop detection function 1: Enable oscillation stop detection function	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The OSTDCR register controls the oscillation stop detection function.

OSTDIE bit (Oscillation Stop Detection Interrupt Enable)

The OSTDIE bit enables the oscillation stop detection function interrupt. It also controls whether oscillation stop detection is reported to the POEG.

If the Oscillation Stop Detection flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) requires clearing, set the OSTDIE bit to 0 before clearing OSTDF. Wait for at least 2 PCLKB cycles before setting the OSTDIE bit to 1. By reading the I/O register whose access cycle number is defined by PCLKB, it is possible to secure waiting time of 2 or more cycles of PCLKB.

OSTDE bit (Oscillation Stop Detection Function Enable)

The OSTDE bit enables the oscillation stop detection function.

When the OSTDE bit is 1 (enabled), the MOCO stop bit (MOCOCR.MCSTP) is set to 0 and the MOCO operation starts. The MOCO clock cannot be stopped while the oscillation stop detection function is enabled. Writing 1 to the MOCOCR.MCSTP bit (MOCO stopped) is invalid.

When the Oscillation Stop Detection flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) is 1 (main clock oscillation stop detected), writing 0 to the OSTDE bit is invalid.

The OSTDE bit must be set to 0 before transitioning to Software Standby or Deep Software Standby mode. To transition to Software Standby or Deep Software Standby mode, first set the OSTDE bit to 0, then execute the WFI instruction.

The following restrictions apply when using the oscillation stop detection function:
In low-speed mode, selecting division by 1, 2, 4, 8 for ICLK, FCLK, PCLKA, PCLKB, PCLKC, and PCLKD is prohibited.

[Clearing condition]

●当PLL2正在运行，然后因为PLL2CR.PLL2STP位设置为1而被停用时。

8.2.13 OSTDCR:振荡停止检测控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x040

Bit position:	7	6	5	4	3	2	1	0
Bit field:	OSTDE	—	—	—	—	—	—	OSTDIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OSTDIE	振荡停止检测中断使能 0：禁止振荡停止检测中断（不通知POEG）1：使能振荡停止检测中断（通知POEG）	R/W
6:1	—	这些位被读取为0。写入值应为0。	R/W
7	OSTDE	振荡停止检测功能启用 0：禁用振荡停止检测功能1：启用振荡停止检测功能	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

OSTDCR寄存器控制振荡停止检测功能。

OSTDIE位（振荡停止检测中断使能）

OSTDIE位使能振荡停止检测功能中断。它还控制是否将振荡停止检测报告给POEG。

如果振荡停止检测状态寄存器(OSTDSR.OSTDF)中的振荡停止检测标志需要清零，则在清零OSTDF之前将OSTDIE位设置为0。在将OSTDIE位设置为1之前等待至少2个PCLKB周期。通过读取访问周期数由PCLKB定义的IO寄存器，可以确保2个或更多PCLKB周期的等待时间。

OSTDE位（振荡停止检测功能使能）

OSTDE位使能振荡停止检测功能。

当OSTDE位为1（使能）时，MOCO停止位（MOCOCR.MCSTP）设置为0，MOCO操作开始。
MOCO时钟在振荡停止检测功能启用时不能停止。将1写入
MOCOCR.MCSTP位（MOCO停止）无效。

当振荡停止检测状态寄存器(OSTDSR.OSTDF)中的振荡停止检测标志为1（检测到主时钟振荡停止）时，向OSTDE位写入0无效。

在转换到软件待机或深度软件待机模式之前，必须将OSTDE位设置为0。过渡到
软件待机或深度软件待机模式，首先将OSTDE位设置为0，然后执行WFI指令。

使用振荡停止检测功能时有以下限制：
在低速模式下，禁止为ICLK、FCLK、PCLKA、PCLKB、PCLKC和PCLKD选择1、2、4、8分频。

8.2.14 OSTDSR : Oscillation Stop Detection Status Register

Base address: SYSC = 0x4001_E000

Offset address: 0x041

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OSTDF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OSTDF	Oscillation Stop Detection Flag 0: Main clock oscillation stop not detected 1: Main clock oscillation stop detected	R/W*1
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. This bit can only be set to 0. This bit is cleared to 0 by writing 0 after reading it as 1.

The OSTDSR register indicates the stop detection status of the main clock oscillator.

OSTDF flag (Oscillation Stop Detection Flag)

The OSTDF flag indicates the main clock oscillator status. When this flag is 1, it indicates that the main clock oscillation stop was detected. After this stop is detected, the OSTDF flag is not set to 0 even when the main clock oscillation is restarted. The OSTDF bit is cleared to 0 by writing 0 after reading it as 1.

At least 3 ICLK cycles of wait time are required between writing 0 to OSTDF and reading it as 0. If the OSTDF flag is set to 0 when the main clock oscillation is stopped, the OSTDF flag becomes 0 then returns to 1.

The OSTDF flag cannot be set to 0 under the following conditions:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC).
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (System clock source = PLL)

The OSTDF flag must be set to 0 after switching the clock source to sources other than the main clock oscillator and PLL.

[Setting condition]

- The main clock oscillator is stopped when OSTDCR.OSTDE = 1 (oscillation stop detection function enabled).

[Clearing condition]

- 1 is read and then 0 is written when the SCKSCR.CKSEL[2:0] bits are neither 011b (system clock is MOSC) nor 101b (system clock is PLL) and PLLCCR.PLSRCSEL bit is not 0 (PLL source clock is MOSC).

8.2.15 MOSCWTCR : Main Clock Oscillator Wait Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0A2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	MSTS[3:0]			
Value after reset:	0	0	0	0	0	1	0	1

8.2.14 OSTDSR：振荡停止检测状态寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x041

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OSTDF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OSTDF	振荡停止检测标志 0：未检测到主时钟振荡停止1：检测到主时钟振荡停止	R/W*1
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.该位只能设置为0。读为1后写入0清除该位为0。

OSTDSR寄存器指示主时钟振荡器的停止检测状态。

OSTDF标志（振荡停止检测标志）

OSTDF标志指示主时钟振荡器状态。该标志为1时，表示检测到主时钟振荡停止。检测到此停止后，即使重新启动主时钟振荡，OSTDF标志也不会设置为0。OSTDF位在读为1后写入0清零。

从向OSTDF写入0到将其读取为0之间至少需要3个ICLK周期的等待时间。如果在主时钟振荡停止时将OSTDF标志设置为0，则OSTDF标志变为0然后返回1。

在以下情况下，OSTDF标志不能设置为0：

●SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）。

●PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）和SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）

将时钟源切换到主时钟振荡器和PLL以外的源后，必须将OSTDF标志设置为0。

[Setting condition]

●当OSTDCR.OSTDE=1（振荡停止检测功能使能）时，主时钟振荡器停止。

[Clearing condition]

●当SCKSCR.CKSEL[2:0]位既不是011b（系统时钟为MOSC）也不是101b（系统时钟为PLL）且PLLCCR.PLSRCSEL位不为0（PLL源时钟为MOSC）。

8.2.15 MOSCWTCR:主时钟振荡器等待控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0A2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	MSTS[3:0]			
重置后的值：	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
3:0	MSTS[3:0]	Main Clock Oscillator Wait Time Setting 0x0: Wait time = 3 cycles (11.4 µs) 0x1: Wait time = 35 cycles (133.5 µs) 0x2: Wait time = 67 cycles (255.6 µs) 0x3: Wait time = 131 cycles (499.7 µs) 0x4: Wait time = 259 cycles (988.0 µs) 0x5: Wait time = 547 cycles (2086.6 µs) 0x6: Wait time = 1059 cycles (4039.8 µs) 0x7: Wait time = 2147 cycles (8190.2 µs) 0x8: Wait time = 4291 cycles (16368.9 µs) 0x9: Wait time = 8163 cycles (31139.4 µs) Others: Setting prohibited	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

MSTS[3:0] bits (Main Clock Oscillator Wait Time Setting)

The MSTS[3:0] bits specify the oscillation stabilization wait time for the main clock oscillator.

Set the main clock oscillation stabilization time to a period longer than or equal to the stabilization time recommended by the oscillator manufacturer. When the main clock is input externally, set these bits to 0x0 because the oscillation stabilization time is not required.

The wait time set in these bits is counted using: 1 cycle (µs) = 1/(fLOCO[MHz] × 8) = 1/(0.032768 × 8) = 3.81 (µs) (min.)
The LOCO clock automatically oscillates when necessary, regardless of the value of the LOCO.LCSTP bit. After the specified wait time elapses, supply of the main clock starts internally in the MCU, and the OSCSF.MOSCSF flag is set to 1. If the specified wait time is short, supply of the main clock starts before oscillation of the clock becomes stable.

Only rewrite the MOSCWTCR register when the MOSCCR.MOSTP bit is 1 and the OSCSF.MOSCSF flag is 0. Do not rewrite this register under any other conditions.

8.2.16 MOMCR : Main Clock Oscillator Mode Oscillation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x413

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	MOSEL	MODRV[1:0]		—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
5:4	MODRV[1:0]	Main Clock Oscillator Drive Capability 0 Switching 0 0: 20 MHz to 24 MHz 0 1: 16 MHz to 20 MHz 1 0: 8 MHz to 16 MHz 1 1: 8 MHz	R/W
6	MOSEL	Main Clock Oscillator Switching 0: Resonator 1: External clock input	R/W
7	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

Bit	Symbol	Function	R/W
3:0	MSTS[3:0]	主时钟振荡器等待时间设置 0x0：等待时间=3个周期(11.4µs)0x1：等待时间=35个周期(133.5µs)0x2：等待时间=67个周期(255.6µs)0x3：等待时间=131个周期(499.7µs)0x4：等待时间=259周期(988.0µs)0x5：等待时间=547个周期(2086.6µs)0x6：等待时间=1059个周期(4039.8µs)0x7：等待时间=2147个周期(8190.2µs)0x8：等待时间=4291个周期(16368.9µs)0x9:等待时间=8163个周期(31139.4µs) 其他：禁止设置	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

MSTS[3:0]位（主时钟振荡器等待时间设置）

MSTS[3:0]位指定主时钟振荡器的振荡稳定等待时间。

将主时钟振荡稳定时间设置为大于或等于振荡器制造商推荐的稳定时间。当主时钟从外部输入时，将这些位设置为0x0，因为不需要振荡稳定时间。

这些位中设置的等待时间使用以下公式计算：1个周期(µs)=1(fLOCO[MHz]×8)=1(0.032768×8)=3.81(µs)(min.)
无论LOCO.LCSTP位的值如何，LOCO时钟都会在必要时自动振荡。经过指定的等待时间后，MCU内部开始提供主时钟，并将OSCSF.MOSCSF标志设置为1。如果指定的等待时间短，则在时钟振荡稳定之前开始提供主时钟.

仅当MOSCCR.MOSTP位为1且OSCSF.MOSCSF标志为0时才重写MOSCWTCR寄存器。在任何其他情况下请勿重写此寄存器。

8.2.16 MOMCR：主时钟振荡器模式振荡控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x413

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	MOSEL	MODRV[1:0]		—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	这些位被读取为0。写入值应为0。	R/W
5:4	MODRV[1:0]	主时钟振荡器驱动能力0开关 0 0: 20 MHz to 24 MHz 0 1: 16 MHz to 20 MHz 1 0: 8 MHz to 16 MHz 1 1: 8 MHz	R/W
6	MOSEL	主时钟振荡器切换 0：谐振器1：外部时钟输入	R/W
7	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：

- Secure and Non-secure access are allowed.

Note: The EXTAL/XTAL pins are also used as ports. In the initial state, the pin is set as a port.
Note: The MOSTP bit must be 1 (MOSC is stopped) before changing this register.
Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

MODRV[1:0] bit (Main Clock Oscillator Drive Capability 0 Switching)

The MODRV[1:0] bit switches the drive capability of the main clock oscillator.

MOSEL bit (Main Clock Oscillator Switching)

The MOSEL bit switches the source for the main clock oscillator.

8.2.17 CKOCR : Clock Out Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x03E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CKOEN	CKODIV[2:0]			—	CKOSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CKOSEL[2:0]	Clock Out Source Select 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: MOSC 1 0 0: Setting prohibited 1 0 1: Setting prohibited Others: Setting prohibited	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	CKODIV[2:0]	Clock Output Frequency Division Ratio 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 1 1 1: × 1/128	R/W
7	CKOEN	Clock Out Enable 0: Disable clock out 1: Enable clock out	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

CKOSEL[2:0] bits (Clock Out Source Select)

The CKOSEL[2:0] bits select the source of the clock to be output from the CLKOUT pin. When changing the clock source, set the CKOEN bit to 0.

CKODIV[2:0] bits (Clock Output Frequency Division Ratio)

The CKODIV[2:0] bits specify the clock division ratio. Set the CKOEN bit to 0 when changing the division ratio.

CKOEN bit (Clock Out Enable)

The CKOEN bit enables output from the CLKOUT pin.

- 允许安全和非安全访问。

Note: EXTALXTAL引脚也用作端口。在初始状态下，该引脚被设置为一个端口。
Note: 在更改此寄存器之前，MOSTP位必须为1（MOSC停止）。
Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

MODRV[1:0]位（主时钟振荡器驱动能力0切换）

MODRV[1:0]位切换主时钟振荡器的驱动能力。

MOSEL位（主时钟振荡器切换）

MOSEL位切换主时钟振荡器的源。

8.2.17 CKOCR：时钟输出控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x03E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CKOEN	CKODIV[2:0]			—	CKOSEL[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CKOSEL[2:0]	时钟输出源选择 000：HOCO001：MOC O010：LOCO011：MOS C100：禁止设置101： 禁止设置 其他：禁止设置	R/W
3	—	该位读取为0。写入值应为0。	R/W
6:4	CKODIV[2:0]	时钟输出分频比 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 1 1 1: × 1/128	R/W
7	CKOEN	时钟输出使能 0：禁用时钟输出1 ：启用时钟输出	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

CKOSEL[2:0]位（时钟输出源选择）

CKOSEL[2:0]位选择从CLKOUT引脚输出的时钟源。更改时钟源时，将CKOEN位设置为0。

CKODIV[2:0]位（时钟输出分频比）

CKODIV[2:0]位指定时钟分频比。更改分频比时将CKOEN位设置为0。

CKOEN位（时钟输出使能）

CKOEN位使能CLKOUT引脚的输出。

When this bit is set to 1, the selected clock is output. When this bit is set to 0, low is output. When changing this bit, confirm that the clock out source clock selected in the CKOSEL[2:0] bits is stable. Otherwise, a glitch might be generated in the output.

Clear this bit before entering Software Standby or Deep Software Standby mode if the selecting clock out source clock is stopped in that mode.

8.2.18 LOCOUTCR : LOCO User Trimming Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x492

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	LOCOUTRM[7:0]	LOCO User Trimming 0x80: -128 0x81: -127 ⋮ 0xFF: -1 0x00: Center Code 0x01: +1 ⋮ 0x7E: +126 0x7F: +127	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The LOCOUTCR register is added to the original LOCO trimming data.

MCU operation is not guaranteed when LOCOUTCR is set to a value that causes the LOCO frequency to be outside of the specification range. When LOCOUTCR is modified, the frequency stabilization time corresponds to the frequency stabilization time at the start of MCU operation. When the ratio of the LOCO frequency and the other oscillation frequency is an integer value, changing the LOCOUTCR value is prohibited.

8.2.19 MOCOUTCR : MOCO User Trimming Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x061

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

当该位设置为1时，输出选定的时钟。当该位设置为0时，输出低电平。更改此位时，请确认CKOSEL[2:0]位中选择的时钟输出源时钟稳定。否则，可能会在输出中产生故障。

如果选择时钟输出源时钟在该模式下停止，则在进入软件待机或深度软件待机模式之前清零该位。

8.2.18 LOCOUTCR:LOCO用户微调控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x492

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LOCOUTRM[7:0]							
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	LOCOUTRM[7:0]	LOCO用户修整 0x80：-1280x81： -127 0xFF：-10x00 ：中心代码0x01：+ 1 0x7E：+1260x7F ：+127	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

LOCOUTCR寄存器被添加到原始LOCO修整数据中。

当LOCOUTCR设置为导致LOCO频率超出规范范围的值时，MCU操作无法保证。修改LOCOUTCR时，频率稳定时间对应于MCU工作开始时的频率稳定时间。当LOCO频率与其他振荡频率之比为整数值时，禁止更改LOCOUTCR值。

8.2.19 MOCOUTCR:MOCO用户微调控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x061

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MOCOUTRM[7:0]							
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	MOCOUTRM[7:0]	MOCO User Trimming 0x80: -128 0x81: -127 ⋮ 0xFF: -1 0x00: Center Code 0x01: +1 ⋮ 0x7E: +126 0x7F: +127	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The MOCOUTCR register is added to the original MOCO trimming data.

MCU operation is not guaranteed when MOCOUTCR is set to a value that causes the MOCO frequency to be outside of the specification range. When MOCOUTCR is modified, the frequency stabilization wait time corresponds to the frequency stabilization wait time at the start of the MCU operation. When the ratio of the MOCO frequency and the other oscillation frequency is an integer value, changing the MOCOUTCR value is prohibited.

8.2.20 HOCOUTCR : HOCO User Trimming Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x062

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	HOCOUTRM[7:0]	HOCO User Trimming 0x80: -128 0x81: -127 ⋮ 0xFF: -1 0x00: Center Code 0x01: +1 ⋮ 0x7E: +126 0x7F: +127	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The HOCOUTCR register is added to the original HOCO trimming data.

MCU operation is not guaranteed when HOCOUTCR is set to a value that causes the HOCO frequency to be outside of the specification range. When HOCOUTCR is modified, the frequency stabilization wait time corresponds to the frequency stabilization wait time at the start of the MCU operation.

Bit	Symbol	Function	R/W
7:0	MOCOUTRM[7:0]	MOCO用户修整 0x80：-1280x81： -127 0xFF：-10x00 ：中心代码0x01：+ 1 0x7E：+1260x7F ：+127	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

MOCOUTCR寄存器被添加到原始MOCO修整数据中。

当MOCOUTCR设置为导致MOCO频率超出规格范围的值时，无法保证MCU操作。修改MOCOUTCR时，稳频等待时间对应MCU运行开始时的稳频等待时间。当MOCO频率与其他振荡频率之比为整数值时，禁止更改MOCOUTCR值。

8.2.20 HOCOUTCR:HOCO用户微调控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x062

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOCOUTRM[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	HOCOUTRM[7:0]	HOCO用户修整 0x80：-1280x81： -127 0xFF：-10x00 ：中心代码0x01：+ 1 0x7E：+1260x7F ：+127	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

HOCOUTCR寄存器被添加到原始HOCO修整数据中。

当HOCOUTCR设置为导致HOCO频率超出规范范围的值时，MCU操作无法保证。修改HOCOUTCR时，稳频等待时间对应MCU运行开始时的稳频等待时间。

8.2.21 SCISPICKDIVCR : SCI SPI Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x06D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SCISPICKDIV[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SCISPICKDIV[2:0]	SCI SPI Clock (SCISPICLK) Division Select 0 0 0: /1 (value after reset) 0 0 1: /2 0 1 0: /4 0 1 1: /6 1 0 0: /8 Others: Setting prohibited.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

SCISPICKDIVCR controls the SCI SPI clock (SCISPICLK).

SCISPICKDIV[2:0] bits (SCI SPI Clock (SCISPICLK) Division Select)

These bits select the frequency of the SCI SPI clock (SCISPICLK) and must be modified when SCISPICKCR.SCISPICKSRDY = 1.

8.2.22 CANFDCKDIVCR : CANFD Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x06E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CANFDCKDIV[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CANFDCKDIV[2:0]	CANFD clock (CANFDCLK) Division Select 0 0 0: 1 0 0 1: 2 0 1 0: 4 0 1 1: 6 1 0 0: 8 Settings other than above are prohibited.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

8.2.21 SCISPICKDIVCR:SCISPI时钟分频控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x06D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SCISPICKDIV[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SCISPICKDIV[2:0]	SCISPI时钟(SCISPICLK)分频选择 0 0 0: /1 (value after reset) 0 0 1: /2 0 1 0: /4 0 1 1: /6 1 0 0: /8 其他：禁止设置。	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

SCISPICKDIVCR控制SCISPI时钟(SCISPICLK)。

SCISPICKDIV[2:0]位（SCISPI时钟(SCISPICLK)分频选择）

这些位选择SCISPI时钟(SCISPICLK)的频率，并且必须在SCISPICKCR.SCISPICKSRDY = 1.

8.2.22 CANFDCKDIVCR:CANFD时钟分频控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x06E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CANFDCKDIV[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CANFDCKDIV[2:0]	CANFD时钟(CANFDCLK)分频选择 0 0 0: 1 0 0 1: 2 0 1 0: 4 0 1 1: 6 1 0 0: 8 禁止上述以外的设置。	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

CANFDCKDIVCR controls the CANFD clock (CANFDCLK).

CANFDCKDIV[2:0] bit (CANFD clock (CANFDCLK) Division Select)

These bits select the frequency of the CANFD clock (CANFDCLK).

These bits must change when CANFDCKCR.CANFDCKSRDY = 1.

8.2.23 GPTCKDIVCR : GPT Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x06F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	GPTCKDIV[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	GPTCKDIV[2:0]	GPT clock (GPTCLK) Division Select 0 0 0: /1 (value after reset) 0 0 1: /2 0 1 0: /4 0 1 1: /6 1 0 0: /8 Settings other than above are prohibited.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

GPTCKDIVCR controls the GPT clock (GPTCLK).

GPTCKDIV[2:0] bit (GPT clock (GPTCLK) Division Select)

These bits select the frequency of the GPT clock (GPTCLK).

These bits must change when GPTCKCR.GPTCKCRSRDY = 1.

8.2.24 IICCKDIVCR : IIC Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x070

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IICCKDIV[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

CANFDCKDIVCR控制CANFD时钟(CANFDCLK)。

CANFDCKDIV[2:0]位（CANFD时钟(CANFDCLK)分频选择）

这些位选择CANFD时钟(CANFDCLK)的频率。

当CANFDCKCR.CANFDCKSRDY=1时，这些位必须改变。

8.2.23 GPTCKDIVCR:GPT时钟分频控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x06F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	GPTCKDIV[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	GPTCKDIV[2:0]	GPT时钟(GPTCLK)分频选择 0 0 0: /1 (value after reset) 0 0 1: /2 0 1 0: /4 0 1 1: /6 1 0 0: /8 禁止上述以外的设置。	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

GPTCKDIVCR控制GPT时钟(GPTCLK)。

GPTCKDIV[2:0]位（GPT时钟(GPTCLK)分频选择）

这些位选择GPT时钟(GPTCLK)的频率。

当GPTCKCR.GPTCKCRSRDY=1时，这些位必须改变。

8.2.24 IICCKDIVCR:IIC时钟分频控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x070

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IICCKDIV[2:0]		
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	IICCKDIV[2:0]	IIC clock (IICCLK) Division Select 0 0 0: /1 (value after reset) 0 0 1: /2 0 1 0: /4 0 1 1: /6 1 0 0: /8 Settings other than above are prohibited.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
IICCKDIVCR controls the IIC clock (IICCLK).

IICCKDIV[2:0] bit (IIC clock (IICCLK) Division Select)

These bits select the frequency of the IIC clock (IICCLK).

These bits must change when IICCKCR.IICCKSRDY = 1.

8.2.25 SCISPICKCR : SCI SPI Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x075

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SCISPICKSRDY	SCISPICKSREQ	—	—	—	SCISPICKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	SCISPICKSEL[2:0]	SCI SPI Clock (SCISPICLK) Source Select 0 0 0: HOCO 0 0 1: MOCO (value after reset) 0 1 0: LOCO 0 1 1: Main clock oscillator 1 0 1: PLL 1 1 0: PLL2 Others: Setting prohibited.	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	SCISPICKSREQ	SCI SPI Clock (SCISPICLK) Switching Request 0: No request 1: Request switching.	R/W
7	SCISPICKSRDY	SCI SPI Clock (SCISPICLK) Switching Ready state flag 0: Switching not possible 1: Switching possible.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The SCISPICKCR register controls the SCI SPI clock (SCISPICLK).

Bit	Symbol	Function	R/W
2:0	IICCKDIV[2:0]	IIC时钟(IICCLK)分频选择 0 0 0: /1 (value after reset) 0 0 1: /2 0 1 0: /4 0 1 1: /6 1 0 0: /8 禁止上述以外的设置。	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
IICCKDIVCR控制IIC时钟(IICCLK)。

IICCKDIV[2:0]位（IIC时钟（IICCLK）分频选择）

这些位选择IIC时钟(IICCLK)的频率。

当IICCKCR.IICCKSRDY=1时，这些位必须改变。

8.2.25 SCISPICKCR:SCISPI时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x075

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SCISPICKSRDY	SCISPICKSREQ	—	—	—	SCISPICKSEL[2:0]		
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	SCISPICKSEL[2:0]	SCISPI时钟(SCISPICLK)源选择 000：HOCO001：MOCO（复位后的值）010：LOCO011：主时钟振荡器101：PLL110：PLL2 其他：禁止设置。	R/W
5:3	—	这些位被读取为0。写入值应为0。	R/W
6	SCISPICKSREQ	SCISPI时钟(SCISPICLK)切换请求 0：无请求1：请求切换。	R/W
7	SCISPICKSRDY	SCISPI时钟(SCISPICLK)切换就绪状态标志 0：不能切换1：可以切换。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

SCISPICKCR寄存器控制SCISPI时钟(SCISPICLK)。

When switching the clock source, ensure that the clock before the switch and the clock after the switch generate stable output.

To change the set value of SCISPICKDIVCR.SCISPICKDIV[2:0] and SCISPICKSEL[2:0], use the following procedure:

1. Write 1 to SCISPICKSREQ.
2. Poll until SCISPICKSRDY is read as 1. While SCISPICKSRDY = 1, no clock is output to SCISPICLK.
3. Write to SCISPICKDIVCR.SCISPICKDIV[2:0] and SCISPICKSEL[2:0].
4. Write 0 to SCISPICKSREQ.
5. Poll until SCISPICKSRDY is read as 0.
6. When SCISPICKSRDY becomes 0, SCISPICLK starts to output. Clock switching is complete.

When transitioning to Software Standby or Deep Software Standby mode, do not execute the WFI instruction while performing clock switching. That is, do not execute the WFI instruction when SCISPICKSREQ = 1 and SCISPICKSRDY = 0, or when SCISPICKSREQ = 0 and SCISPICKSRDY = 1.

SCISPICKSEL[2:0] bits (SCI SPI Clock (SCISPICLK) Source Select)

These bits select the clock source of the SCI SPI clock (SCISPICLK) and must be modified when SCISPICKCR.SCISPICKSRDY = 1.

SCISPICKSREQ bit (SCI SPI Clock (SCISPICLK) Switching Request)

This bit selects the SCISPICLK switching request.

SCISPICKSRDY flag (SCI SPI Clock (SCISPICLK) Switching Ready state flag)

This flag indicates the state of switching ready for the SCISPICLK. When SCISPICKSRDY = 1, no clock is output to SCISPICLK.

8.2.26 CANFDCKCR : CANFD Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x076

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CANFDCKSRDY	CANFDCKSREQ	—	—	—	CANFDCKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CANFDCKSEL[2:0]	CANFD clock (CANFDCLK) Source Select 1 0 1: PLL 1 1 0: PLL2 Settings other than above are prohibited.	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	CANFDCKSREQ	CANFD clock (CANFDCLK) Switching Request 0: No request 1: Request switching	R/W
7	CANFDCKSRDY	CANFD clock (CANFDCLK) Switching Ready state flag 0: Impossible to Switch 1: Possible to Switch	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

切换时钟源时，确保切换前的时钟和切换后的时钟产生稳定的输出。

要更改SCISPICKDIVCR.SCISPICKDIV[2:0]和SCISPICKSEL[2:0]的设置值，请使用以下过程：

1.向SCISPICKSREQ写入1。

2.轮询直到SCISPICKSRDY被读取为1。当SCISPICKSRDY=1时，没有时钟输出到SCISPICLK。

3.写入SCISPICKDIVCR.SCISPICKDIV[2:0]和SCISPICKSEL[2:0]。

4.将0写入SCISPICKSREQ。

5.轮询直到SCISPICKSRDY被读取为0。

6.当SCISPICKSRDY变为0时，SCISPICLK开始输出。时钟切换完成。

当转换到软件待机或深度软件待机模式时，不要在执行时钟切换时执行WFI指令。也就是说，当SCISPICKSREQ=1和SCISPICKSRDY=0时，或者当SCISPICKSREQ=0和SCISPICKSRDY=1时，不执行WFI指令。

SCISPICKSEL[2:0]位（SCISPI时钟(SCISPICLK)源选择）

这些位选择SCISPI时钟(SCISPICLK)的时钟源，并且必须在SCISPICKCR.SCISPICKSRDY = 1.

SCISPICKSREQ位（SCISPI时钟(SCISPICLK)切换请求）

该位选择SCISPICLK切换请求。

SCISPICKSRDY标志（SCISPI时钟(SCISPICLK)切换就绪状态标志）

该标志指示SCISPICLK的切换就绪状态。当SCISPICKSRDY=1时，没有时钟输出到SCISPICLK.

8.2.26 CANFDCKCR:CANFD时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x076

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CANFDCKSRDY	CANFDCKSREQ	—	—	—	CANFDCKSEL[2:0]		
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CANFDCKSEL[2:0]	CANFD时钟(CANFDCLK)源选择 1 0 1: PLL 1 1 0: PLL2 禁止上述以外的设置。	R/W
5:3	—	这些位被读取为0。写入值应为0。	R/W
6	CANFDCKSREQ	CANFD时钟(CANFDCLK)切换请求 0：无请求1：请求切换	R/W
7	CANFDCKSRDY	CANFD时钟(CANFDCLK)切换就绪状态标志 0：不能切换1：可以切换	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The CANFDCKCR register controls the CANFD clock (CANFDCLK).

When switching the clock source, ensure that the clock before the switch and the clock after the switch generate stable output. To change the set value of CANFDCKDIVCR.CANFDCKDIV[2:0] and CANFDCKSEL[2:0], use the following procedure:

1. Write 1 to CANFDCKSREQ.
2. Poll until CANFDCKSRDY is read as 1. While CANFDCKSRDY = 1, no clock is output to CANFDCLK.
3. Write to CANFDCKDIVCR.CANFDCKDIV[2:0] and CANFDCKSEL[2:0].
4. Write 0 to CANFDCKSREQ.
5. Poll until CANFDCKSRDY is read as 0.
6. When CANFDCKSRDY becomes 0, CANFDCLK starts to output. Clock switching is complete.

When transitioning to Software Standby or Deep Software Standby mode, do not execute the WFI instruction while performing clock switching. That is, do not execute the WFI instruction when CANFDCKSREQ = 1 and CANFDCKSRDY = 0, or when CANFDCKSREQ = 0 and CANFDCKSRDY = 1.

CANFDCKSEL[2:0] bits (CANFD clock (CANFDCLK) Source Select)

These bits select the clock source of the CANFD clock (CANFDCLK) and must be modified when CANFDCKCR.CANFDCKSRDY = 1.

CANFDCKSREQ bit (CANFD clock (CANFDCLK) Switching Request)

This bit selects the CANFDCLK switching request.

CANFDCKSRDY flag (CANFD clock (CANFDCLK) Switching Ready state flag)

This flag indicates the state of switching ready for the CANFDCLK. When CANFDCKSRDY = 1, no clock is output to CANFDCLK.

8.2.27 GPTCKCR : GPT Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x077

Bit position:	7	6	5	4	3	2	1	0
Bit field:	GPTCKSRDY	GPTCKSREQ	—	—	—	GPTCKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	GPTCKSEL[2:0]	GPT clock (GPTCLK) Source Select 0 0 0: HOCO 0 0 1: MOCO (value after reset) 0 1 0: LOCO 0 1 1: Main clock oscillator 1 0 1: PLL 1 1 0: PLL2 Settings other than above are prohibited.	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	GPTCKSREQ	GPT clock (GPTCLK) Switching Request 0: No request 1: Request switching	R/W
7	GPTCKSRDY	GPT clock (GPTCLK) Switching Ready state flag 0: Impossible to Switch 1: Possible to Switch	R

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

CANFDCKCR寄存器控制CANFD时钟(CANFDCLK)。

切换时钟源时，确保切换前的时钟和切换后的时钟产生稳定的输出。要更改CANFDCKDIVCR.CANFDCKDIV[2:0]和CANFDCKSEL[2:0]的设置值，请使用以下过程：

1.将1写入CANFDCKSREQ。

2.轮询直到CANFDCKSRDY被读取为1。当CANFDCKSRDY=1时，没有时钟输出到CANFDCLK。

3.写入CANFDCKDIVCR.CANFDCKDIV[2:0]和CANFDCKSEL[2:0]。

4.将0写入CANFDCKSREQ。

5.轮询直到CANFDCKSRDY被读取为0。

6.当CANFDCKSRDY变为0时，CANFDCLK开始输出。时钟切换完成。

当转换到软件待机或深度软件待机模式时，不要在执行时钟切换时执行WFI指令。即CANFDCKSREQ=1且CANFDCKSRDY=0时，或CANFDCKSREQ=0且CANFDCKSRDY=1时不执行WFI指令。

CANFDCKSEL[2:0]位（CANFD时钟(CANFDCLK)源选择）

这些位选择CANFD时钟(CANFDCLK)的时钟源，并且必须在CANFDCKCR.CANFDCKSRDY = 1.

CANFDCKSREQ位（CANFD时钟(CANFDCLK)切换请求）

该位选择CANFDCLK切换请求。

CANFDCKSRDY标志（CANFD时钟(CANFDCLK)切换就绪状态标志）

该标志指示CANFDCLK的切换就绪状态。当CANFDCKSRDY=1时，没有时钟输出到CANFDCLK.

8.2.27 GPTCKCR:GPT时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x077

Bit position:	7	6	5	4	3	2	1	0
Bit field:	GPTCKSRDY	GPTCKSREQ	—	—	—	GPTCKSEL[2:0]		
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	GPTCKSEL[2:0]	GPT时钟(GPTCLK)源选择 000：HOCO001：MOCO（复位后的值）010：LOCO011：主时钟振荡器101：PLL110：PLL2 禁止上述以外的设置。	R/W
5:3	—	这些位被读取为0。写入值应为0。	R/W
6	GPTCKSREQ	GPT时钟(GPTCLK)切换请求 0：无请求1：请求切换	R/W
7	GPTCKSRDY	GPT时钟(GPTCLK)切换就绪状态标志 0：不能切换1：可以切换	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The GPTCKCR register controls the GPT clock (GPTCLK).

When switching the clock source, ensure that the clock before the switch and the clock after the switch generate stable output. To change the set value of GPTCKDIVCR.GPTCKDIV[2:0] and GPTCKSEL[2:0], use the following procedure:

1. Write 1 to GPTCKSREQ.
2. Poll until GPTCKSRDY is read as 1. While GPTCKSRDY = 1, no clock is output to GPTCLK.
3. Write to GPTCKDIVCR.GPTCKDIV[2:0] and GPTCKSEL[2:0].
4. Write 0 to GPTCKSREQ.
5. Poll until GPTCKSRDY is read as 0.
6. When GPTCKSRDY becomes 0, GPTCLK starts to output. Clock switching is complete.

When transitioning to Software Standby or Deep Software Standby mode, do not execute the WFI instruction while performing clock switching. That is, do not execute the WFI instruction when GPTCKSREQ = 1 and GPTCKSRDY = 0, or when GPTCKSREQ = 0 and GPTCKSRDY = 1.

GPTCKSEL[2:0] bits (GPT clock (GPTCLK) Source Select)

These bits select the clock source of the GPT clock (GPTCLK) and must be modified when GPTCKCR.GPTCKSRDY = 1.

GPTCKSREQ bit (GPT clock (GPTCLK) Switching Request)

This bit selects the GPTCLK switching request.

GPTCKSRDY flag (GPT clock (GPTCLK) Switching Ready state flag)

This flag indicates the state of switching ready for the GPTCLK. When GPTCKSRDY = 1, no clock is output to GPTCLK.

8.2.28 IICCKCR : IIC Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x078

Bit position:	7	6	5	4	3	2	1	0
Bit field:	IICCK SRDY	IICCK SREQ	—	—	—	IICCKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	IICCKSEL[2:0]	IIC clock (IICCLK) Source Select 0 0 0: HOCO 0 0 1: MOCO (value after reset) 0 1 0: LOCO 0 1 1: Main clock oscillator 1 0 1: PLL 1 1 0: PLL2 Settings other than above are prohibited.	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	IICCKSREQ	IIC clock (IICCLK) Switching Request 0: No request 1: Request switching	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

GPTCKCR寄存器控制GPT时钟(GPTCLK)。

切换时钟源时，确保切换前的时钟和切换后的时钟产生稳定的输出。要更改GPTCKDIVCR.GPTCKDIV[2:0]和GPTCKSEL[2:0]的设置值，请使用以下过程：

1.将1写入GPTCKSREQ。

2.轮询直到GPTCKSRDY被读取为1。当GPTCKSRDY=1时，没有时钟输出到GPTCLK。

3.写入GPTCKDIVCR.GPTCKDIV[2:0]和GPTCKSEL[2:0]。

4.将0写入GPTCKSREQ。

5.轮询直到GPTCKSRDY被读取为0。

6.当GPTCKSRDY变为0时，GPTCLK开始输出。时钟切换完成。

当转换到软件待机或深度软件待机模式时，不要在执行时钟切换时执行WFI指令。即，当GPTCKSREQ=1且GPTCKSRDY=0时，或GPTCKSREQ=0且GPTCKSRDY=1时，不执行WFI指令。

GPTCKSEL[2:0]位（GPT时钟(GPTCLK)源选择）

这些位选择GPT时钟(GPTCLK)的时钟源，并且必须在GPTCKCR.GPTCKSRDY=1时进行修改。

GPTCKSREQ位（GPT时钟(GPTCLK)切换请求）

该位选择GPTCLK切换请求。

GPTCKSRDY标志（GPT时钟(GPTCLK)切换就绪状态标志）

该标志指示GPTCLK的切换就绪状态。当GPTCKSRDY=1时，没有时钟输出到GPTCLK。

8.2.28 IICCKCR:IIC时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x078

Bit position:	7	6	5	4	3	2	1	0
Bit field:	IICCK SRDY	IICCK SREQ	—	—	—	IICCKSEL[2:0]		
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	IICCKSEL[2:0]	IIC时钟(IICCLK)源选择 000：HOCO001：MOCO（复位后的值）010：LOCO011：主时钟振荡器101：PLL110：PLL2 禁止上述以外的设置。	R/W
5:3	—	这些位被读取为0。写入值应为0。	R/W
6	IICCKSREQ	IIC时钟(IICCLK)切换请求 0：无请求1：请求切换	R/W

Bit	Symbol	Function	R/W
7	IICCKSRDY	IIC clock (IICCLK) Switching Ready state flag 0: Impossible to Switch 1: Possible to Switch	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The IICCKCR register controls the IIC clock (IICCLK).

When switching the clock source, ensure that the clock before the switch and the clock after the switch generate stable output. To change the set value of IICCKDIVCR.IICCKDIV[2:0] and IICCKSEL[2:0], use the following procedure:

1. Write 1 to IICCKSREQ.
2. Poll until IICCKSRDY is read as 1. While IICCKSRDY = 1, no clock is output to IICCLK.
3. Write to IICCKDIVCR.IICCKDIV[2:0] and IICCKSEL[2:0].
4. Write 0 to IICCKSREQ.
5. Poll until IICCKSRDY is read as 0.
6. When IICCKSRDY becomes 0, IICCLK starts to output. Clock switching is complete.

When transitioning to Software Standby or Deep Software Standby mode, do not execute the WFI instruction while performing clock switching. That is, do not execute the WFI instruction when IICCKSREQ = 1 and IICCKSRDY = 0, or when IICCKSREQ = 0 and IICCKSRDY = 1.

IICCKSEL[2:0] bits (IIC clock (IICCLK) Source Select)

These bits select the clock source of the IIC clock (IICCLK) and must be modified when IICCKCR.IICCKSRDY = 1.

IICCKSREQ bit (IIC clock (IICCLK) Switching Request)

This bit selects the IICCLK switching request.

IICCKSRDY flag (IIC clock (IICCLK) Switching Ready state flag)

This flag indicates the state of switching ready for the IICCLK. When IICCKSRDY = 1, no clock is output to IICCLK.

8.2.29 TRCKCR : Trace Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x03F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TRCKEN	—	—	—	TRCK[3:0]			
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
3:0	TRCK[3:0]	Trace Clock operating frequency select 0x0: /1 0x1: /2 (value after reset) 0x2: /4 Others: Setting prohibited	R/W
6:4	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
7	IICCKSRDY	IIC时钟(IICCLK)切换就绪状态标志 0：不能切换1：可以切换	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

IICCKCR寄存器控制IIC时钟（IICCLK）。

切换时钟源时，确保切换前的时钟和切换后的时钟产生稳定的输出。要更改IICCKDIVCR.IICCKDIV[2:0]和IICCKSEL[2:0]的设置值，请使用以下过程：

1.将1写入IICCKSREQ。

2.轮询直到IICCKSRDY被读取为1。当IICCKSRDY=1时，没有时钟输出到IICCLK。

3.写入IICCKDIVCR.IICCKDIV[2:0]和IICCKSEL[2:0]。

4.将0写入IICCKSREQ。

5.轮询直到IICCKSRDY被读取为0。

6.当IICCKSRDY变为0时，IICCLK开始输出。时钟切换完成。

当转换到软件待机或深度软件待机模式时，不要在执行时钟切换时执行WFI指令。即，当IICCKSREQ=1且IICCKSRDY=0或IICCKSREQ=0且IICCKSRDY=1时不执行WFI指令。

IICCKSEL[2:0]位（IIC时钟（IICCLK）源选择）

这些位选择IIC时钟(IICCLK)的时钟源，并且必须在IICCKCR.IICCKSRDY=1时进行修改。

IICCKSREQ位（IIC时钟(IICCLK)切换请求）

该位选择IICCLK切换请求。

IICCKSRDY标志（IIC时钟(IICCLK)切换就绪状态标志）

该标志指示IICCLK的切换就绪状态。当IICCKSRDY=1时，没有时钟输出到IICCLK。

8.2.29 TRCKCR：跟踪时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x03F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TRCKEN	—	—	—	TRCK[3:0]			
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
3:0	TRCK[3:0]	跟踪时钟工作频率选择 0x0: /1 0x1: /2 (value after reset) 0x2: /4 其他：禁止设置	R/W
6:4	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
7	TRCKEN	Trace Clock operating Enable 0: Stop 1: Operation enable	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Trace Clock Control Register controls switching the trace clock.

TRCKCR can be written only when the debugger is connected (DBGSTR.CDBGPWRUPREQ = 1).

Change the TRCLK frequency in the state of TRCKEN = 0.

Factor of the initialization of TRCKCR register is all resets.

8.3 Main Clock Oscillator

To supply the clock signal to the main clock oscillator, use one of the following ways:

- Connect an oscillator
- Connect the input of an external clock signal.

8.3.1 Connecting a Crystal Resonator

Figure 8.4 shows an example of connecting a crystal resonator. A damping resistor (Rd) can be added, if required.

Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the manufacturer recommends using an external feedback resistor (Rf), insert an Rf between EXTAL and XTAL by following the instructions.

When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the main clock oscillator as described in Table 8.1.

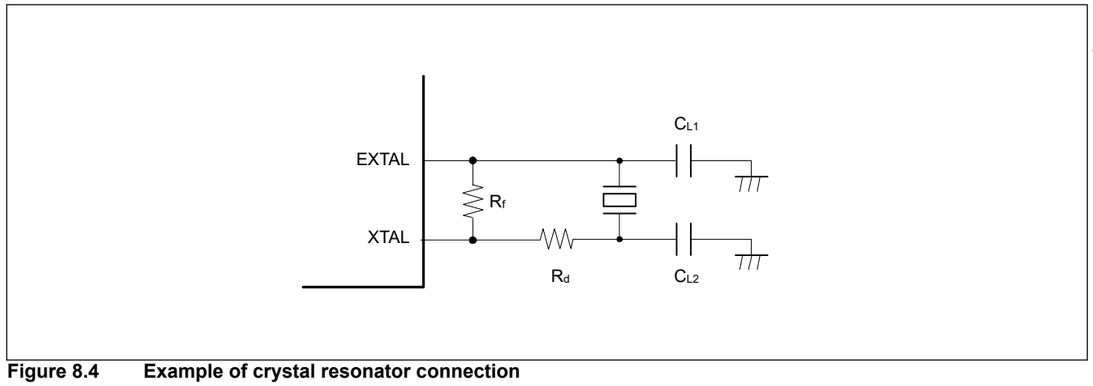


Figure 8.4 Example of crystal resonator connection

Figure 8.5 shows an equivalent circuit of the crystal resonator.

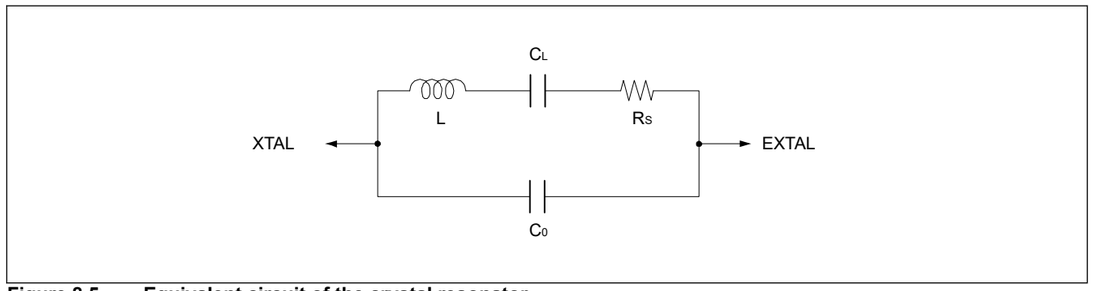


Figure 8.5 Equivalent circuit of the crystal resonator

Bit	Symbol	Function	R/W
7	TRCKEN	跟踪时钟操作使能 0：停止1：运行使能	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

跟踪时钟控制寄存器控制跟踪时钟的切换。

TRCKCR只能在调试器连接时写入(DBGSTR.CDBGPWRUPREQ=1)。

在TRCKEN=0的状态下改变TRCLK频率。

TRCKCR寄存器初始化的因素是所有的复位。

8.3 主时钟振荡器

要将时钟信号提供给主时钟振荡器，请使用以下方法之一：

●连接振荡器

●连接外部时钟信号的输入。

8.3.1 连接晶体谐振器

图8.4显示了连接晶体谐振器的示例。如果需要，可以添加一个阻尼电阻器(Rd)。

由于电阻值因谐振器和振荡驱动能力而异，请使用谐振器制造商推荐的值。如果制造商建议使用外部反馈电阻器(Rf)，请按照说明在EXTAL和XTAL之间插入一个Rf。

连接谐振器以提供时钟时，谐振器的频率必须在表8.1中所述的主时钟振荡器的谐振器频率范围内。

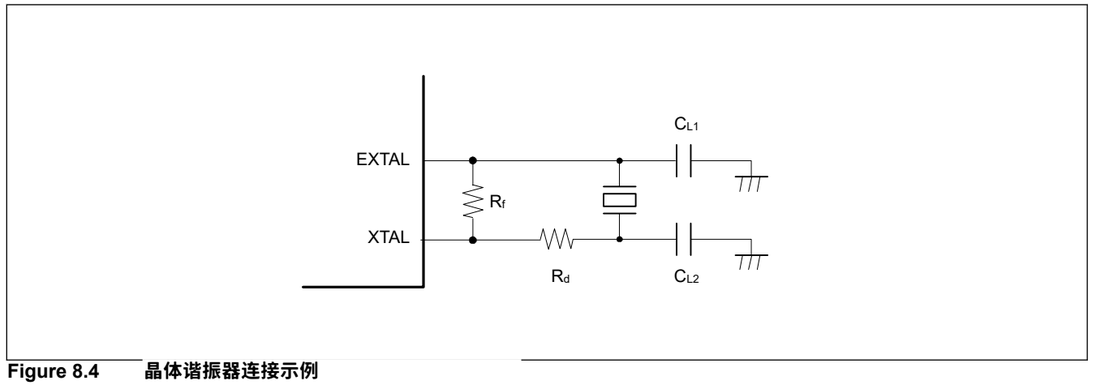


Figure 8.4 晶体谐振器连接示例

图8.5显示了晶体谐振器的等效电路。

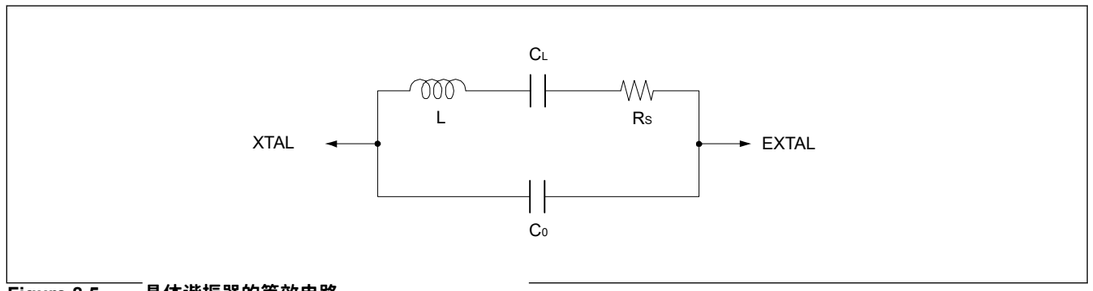


Figure 8.5 晶体谐振器的等效电路

8.3.2 External Clock Input

Figure 8.6 shows an example of connecting an external clock input. To operate the oscillator with an external clock signal, set the MOMCR.MOSEL bit to 1. The XTAL pin becomes high impedance.

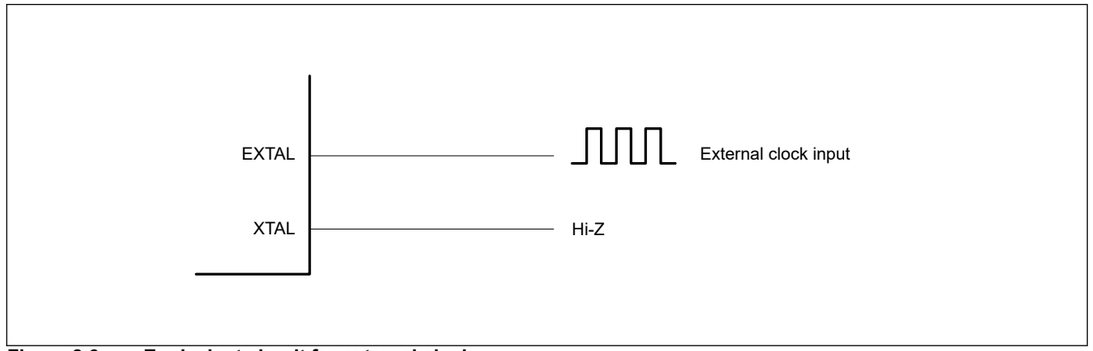


Figure 8.6 Equivalent circuit for external clock

8.3.3 Notes on External Clock Input

The frequency of the external clock input can only be changed when the main clock oscillator is stopped. Do not change the frequency of the external clock input when the setting of the Main Clock Oscillator Stop bit (MOSCCR.MOSTP) is 0.

8.4 Oscillation Stop Detection Function

8.4.1 Oscillation Stop Detection and Operation after Detection

The oscillation stop detection function detects the main clock oscillator stop. When oscillation stop is detected, the system clock switches as follows:

- If an oscillation stop is detected with SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC), the system clock source switches to the MOCO clock.
- If an oscillation stop is detected with PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL), PLL clock remains the system clock source. However, the frequency becomes a free-running oscillation frequency.

An oscillation stop detection interrupt request can be generated when an oscillation stop is detected. In addition, the General PWM Timer (GPT) output can be forced to a high-impedance state on detection.

The main clock oscillation stop is detected when the input clock remains at 0 or 1 for a certain period, for example, when a malfunction occurs in the main clock oscillator. See section 46, Electrical Characteristics.

Switching between the main clock oscillator and the MOCO clock or between the PLL clock and PLL free-running clock is controlled by the Oscillation Stop Detection Flag (OSTDSR.OSTDF).

OSTDF controls the switched clock as follows:

- When SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC):
  - When OSTDF changes from 0 to 1, the clock source switches to the MOCO clock.
  - When OSTDF changes from 1 to 0, the clock source switches back to MOSC.
- When PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (System clock source = PLL):
  - When OSTDF changes 0 to 1, the clock source switches to the PLL free-running oscillation clock.
  - When OSTDF changes 1 to 0, the clock source switches back to PLL.

8.3.2 外部时钟输入

图8.6显示了连接外部时钟输入的示例。要使用外部时钟信号操作振荡器，请将MOMCR.MOSEL位设置为1。XTAL引脚变为高阻抗。

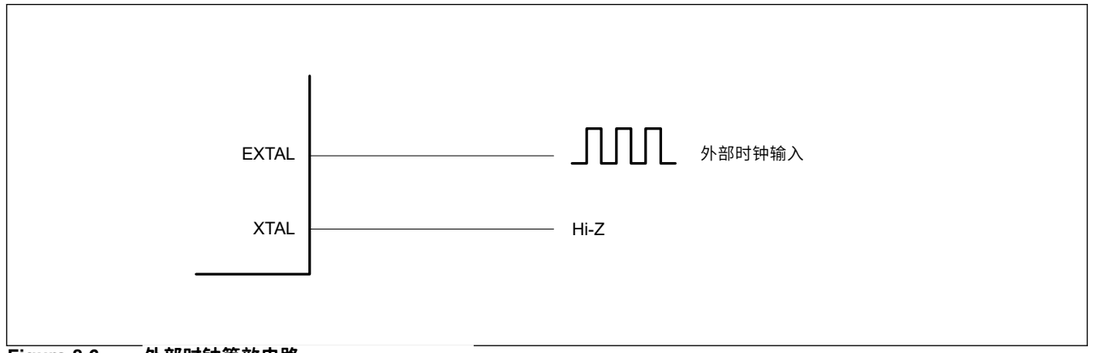


Figure 8.6 外部时钟等效电路

8.3.3 外部时钟输入注意事项

外部时钟输入的频率只有在主时钟振荡器停止时才能改变。当主时钟振荡器停止位(MOSCCR.MOSTP)设置为0时，请勿更改外部时钟输入的频率。

8.4 振荡停止检测功能

8.4.1 振荡停止检测和检测后操作

振荡停止检测功能检测主时钟振荡器停止。当检测到振荡停止时，系统时钟切换如下：

●如果通过SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）检测到振荡停止，则系统时钟源切换到MOCO时钟。

●如果在PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）的情况下检测到振荡停止并且SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL），PLL时钟仍然是系统时钟源。然而，该频率变为自由运行的振荡频率。

当检测到振荡停止时，可以产生一个振荡停止检测中断请求。此外，一般PWM定时器(GPT)输出可在检测时强制为高阻抗状态。

当输入时钟保持在0或1一段时间，例如，当主时钟振荡器发生故障时，检测到主时钟振荡停止。参见第46节，电气特性。

主时钟振荡器和MOCO时钟之间或PLL时钟和PLL自由运行时钟之间的切换由振荡停止检测标志(OSTDSR.OSTDF)控制。

OSTDF控制切换时钟如下：

●当SCKSCR.CKSEL[2:0]=011b时（系统时钟源=MOSC）：

当OSTDF从0变为1时，时钟源切换到MOCO时钟。

当OSTDF从1变为0时，时钟源切换回MOSC。

●当PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）且SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）时：

当OSTDF由0变为1时，时钟源切换到PLL自由运行振荡时钟。

当OSTDF由1变为0时，时钟源切换回PLL。

To switch the clock source to the main clock or PLL clock again after the oscillation stop detection, set the CKSEL[2:0] bits to a clock source other than the main clock or PLL clock and clear the OSTDF flag to 0. Also, check that the OSTDF flag is not 1, then set the CKSEL[2:0] bits to the main clock or PLL clock after the specified oscillation stabilization time elapses.

After a reset release, the main clock oscillator is stopped and the oscillation stop detection function is disabled. To enable the oscillation stop detection function, activate the main clock oscillator and write 1 to the oscillation stop detection function enable bit (OSTDCR.OSTDE) after a specified oscillation stabilization time elapses.

The oscillation stop detection function detects when the main clock is stopped by an external cause. Therefore, the oscillation stop detection function must be disabled before the main clock oscillator is stopped by software or a transition is made to Software Standby or Deep Software Standby mode.

The oscillation stop detection function switches all clocks that can be selected as the MOSC clock except CLKOUT to the MOCO (when system clock is MOSC) or PLL free-running (when system clock is PLL).

The system clock (ICLK) frequency during the MOCO(when system clock is MOSC) or PLL free-running (when system clock is PLL) operation is specified by the MOCO oscillation frequency and the division ratio set by the system clock select bits (SCKDIVCR.ICK[2:0])

要在检测到振荡停止后再次将时钟源切换为主时钟或PLL时钟，请将CKSEL[2:0]位设置为主时钟或PLL时钟以外的时钟源，并将OSTDF标志清零。此外，检查OSTDF标志不为1，然后在指定的振荡稳定时间过去后将CKSEL[2:0]位设置为主时钟或PLL时钟。

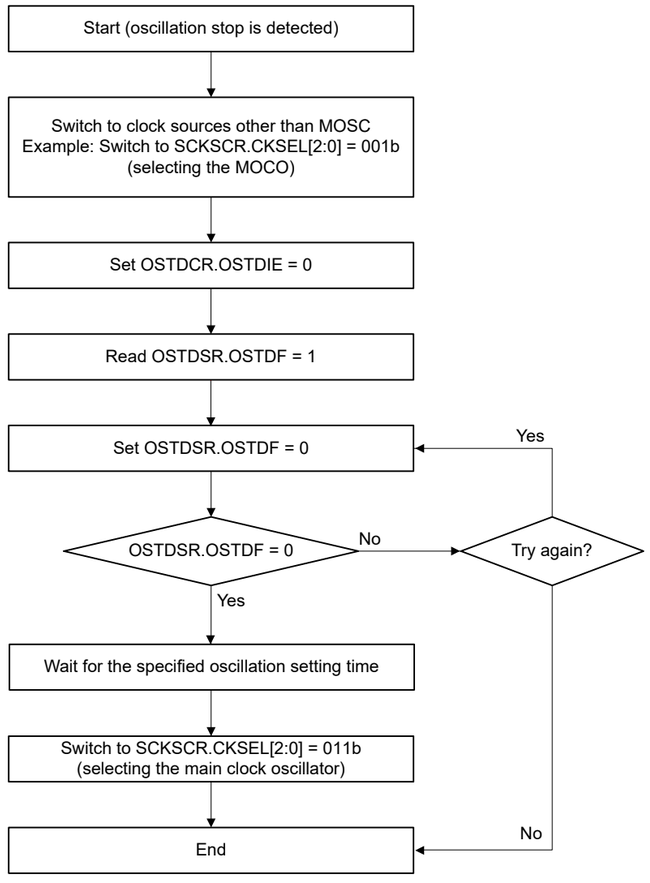
复位释放后，主时钟振荡器停止，振荡停止检测功能被禁用。要启用振荡停止检测功能，激活主时钟振荡器并在经过指定的振荡稳定时间后将1写入振荡停止检测功能使能位(OSTDCR.OSTDE)。

振荡停止检测功能检测主时钟何时因外部原因停止。因此，必须在软件停止主时钟振荡器或转换到软件待机或深度软件待机模式之前禁用振荡停止检测功能。

振荡停止检测功能将除CLKOUT之外的所有可选择作为MOSC时钟的时钟切换到
MOCO（系统时钟为MOSC时）或PLL自由运行（系统时钟为PLL时）。

MOCO（系统时钟为MOSC时）或PLL自由运行（系统时钟为PLL时）操作期间的系统时钟（ICLK）频率由MOCO振荡频率和系统时钟选择位（SCKDIVCR）设置的分频比指定.ICK[2:0])

Example of returning when CKSEL[2:0] = 011b (selecting the main clock oscillator) after an oscillation stop is detected



Note: On return from the oscillation-stopped state, the factor responsible for stopping the main clock oscillation circuit must be removed from the system to allow oscillation to resume.

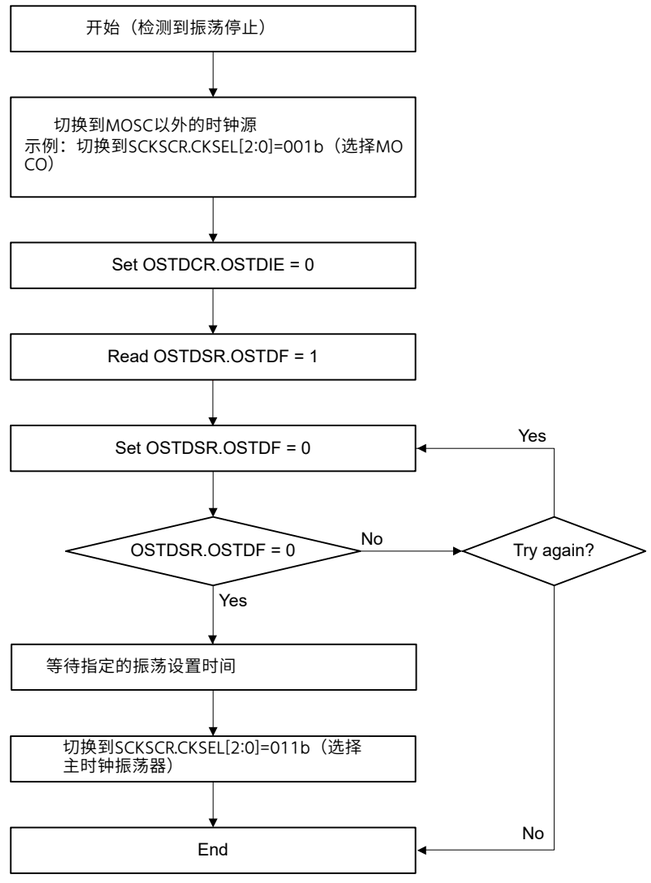
Figure 8.7 Flow of recovery on detection of oscillator stop

8.4.2 Oscillation Stop Detection Interrupts

An oscillation stop detection interrupt (MOSC_STOP) is generated when the Oscillation Stop Detection Flag (OSTDSR.OSTDF) is 1 and the Oscillation Stop Detection Interrupt Enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE) is 1 (enabled). The Port Output Enable for GPT (POEG) is notified of the main clock oscillator stop. On receiving the notification, the POEG sets the Oscillation Stop Detection Flag in the POEG Group n Setting Register (POEGGn.OSTPF) to 1 (n = A, B, C, D).

After the oscillation stop is detected, wait at least 10 PCLKB clock cycles before writing to the POEGGn.OSTPF flag. When the OSTDSR.OSTDF flag requires clearing, do so after clearing the Oscillation Stop Detection Interrupt Enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE). Wait at least 2 PCLKB clock cycles before setting the OSTDCR.OSTDIE bit to 1 again. A longer PCLKB wait time might be required, depending on the number of cycles required to read a given I/O register.

检测到振荡停止后CKSEL[2:0]=011b（选择主时钟振荡器）时返回的示例



Note: 在从振荡停止状态返回时，必须从系统中移除负责停止主时钟振荡电路的因素以允许振荡恢复。

Figure 8.7 检测到振荡器停止时的恢复流程

8.4.2 振荡停止检测中断

当振荡停止检测标志(OSTDSR.OSTDF)为1且振荡停止检测控制寄存器(OSTDCR.OSTDIE)中的振荡停止检测中断使能位为1（使能）时，将产生一个振荡停止检测中断(MOSC_STOP)。GPT端口输出使能(POEG)被通知主时钟振荡器停止。收到通知后，POEG将POEG组n设置寄存器(POEGGn.OSTPF)中的振荡停止检测标志设置为1(n=A B C D)。

检测到振荡停止后，至少等待10个PCLKB时钟周期，然后再写入POEGGn.OSTPF标志。
当需要清除OSTDSR.OSTDF标志时，请在清除振荡停止检测控制寄存器(OSTDCR.OSTDIE)中的振荡停止检测中断使能位后执行此操作。至少等待2个PCLKB时钟周期，然后再将OSTDCR.OSTDIE位设置为1。可能需要更长的PCLKB等待时间，具体取决于读取给定IO寄存器所需的周期数。

The oscillation stop detection interrupt is a non-maskable interrupt. Because non-maskable interrupts are disabled in the initial state after a reset release, enable non-maskable interrupts through software before using oscillation stop detection interrupts. For details, see section 12, Interrupt Controller Unit (ICU).

8.5 PLL Circuit

The PLL circuit has a function to multiply the frequency from the oscillator.

8.6 Internal Clock

Clock sources for the internal clock signals include:

- Main clock
- HOCO clock
- MOCO clock
- LOCO clock
- PLL clock
- PLL2 clock
- IWDT-dedicated clock
- JTAG clock

The following internal clocks are produced from these sources.

- Operating clock of the CPU, DMAC, DTC, Flash, I/O ports, TFU, IIRFA and RAM: System clock (ICLK)
- Operating clocks of peripheral modules: Peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD)
- Operating clock of the FlashIF: FlashIF clock (FCLK)
- Operating clock for the GPT : GPT clock (GPTCLK)
- Operating clock for the SCI and SPI: SCI SPI clock (SCISPICLK)
- Operating clock for the CANFD: CANFD clock (CANFDCLK)
- Operating clock for the CANFD: CAN clock (CANMCLK)
- Operating clocks for the IIC: IIC clock (IICCLK)
- Operating clocks for the CAC: CAC clock (CACCLK)
- Operating clock for the IWDT: IWDT-dedicated clock (IWDTCLK)
- Operating clock for the AGT: AGT-dedicated LOCO clock (AGTLCLK)
- Operating clock for the Systick Timer: Systick Timer-dedicated clock (SYSTICCLK)
- Clock for external pin output: Clock/Buzzer output clock(CLKOUT)
- Operating clock for the JTAG: JTAG clock (JTAGTCK)

For details on the registers used to set the frequencies of the internal clocks, see section 8.6.1. System Clock (ICLK) to section 8.6.14. JTAG Clock (JTAGTCK)

If the value of any of these bits is changed, subsequent operation is at the frequency determined by the new value.

8.6.1 System Clock (ICLK)

The system clock (ICLK) is the operating clock of the CPU, DMAC, DTC, Flash, and SRAM.

The ICLK frequency is specified by the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, the PLLMUL[5:0], and PLIDIV[1:0] bits in PLLCCR, and the HOCOFRQ0[1:0] bits in OFS1.

When the ICLK clock source is switched, the duration of the ICLK clock cycle becomes longer during the clock source transition period. See Figure 8.8 and Figure 8.9.

振荡停止检测中断是一个不可屏蔽的中断。由于不可屏蔽中断在复位释放后的初始状态下被禁用，因此在使用振荡停止检测中断之前，请通过软件启用不可屏蔽中断。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

8.5 PLL Circuit

PLL电路具有倍增振荡器频率的功能。

8.6 内部时钟

内部时钟信号的时钟源包括：

●主时钟

- HOCO clock
- MOCO clock

●LOCO时钟

- PLL clock
- PLL2 clock
- IWDT-dedicated clock
- JTAG clock

以下内部时钟由这些源产生。

●CPU、DMAC、DTC、Flash、IO口、TFU、IIRFA、RAM的工作时钟：系统时钟（ICLK）
●外设模块工作时钟：外设模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）
●FlashIF的工作时钟：FlashIF时钟（FCLK）
●GPT的工作时钟：GPT时钟(GPTCLK)
●SCI和SPI的工作时钟：SCISPI时钟(SCISPICLK)
●CANFD的工作时钟：CANFD时钟(CANFDCLK)
●CANFD的工作时钟：CAN时钟(CANMCLK)
●IIC的工作时钟：IIC时钟（IICCLK）
●CAC的工作时钟：CAC时钟(CACCLK)
●IWDT的工作时钟：IWDT专用时钟（IWDTCLK）
●AGT的工作时钟：AGT专用的LOCO时钟(AGTLCLK)
●SystickTimer的工作时钟：SystickTimer专用时钟(SYSTICCLK)
●外部引脚输出时钟：时钟蜂鸣器输出时钟（CLKOUT）
●JTAG的工作时钟：JTAG时钟（JTAGTCK）

有关用于设置内部时钟频率的寄存器的详细信息，请参见第8.6.1节。系统时钟(ICLK)参见第8.6.14节。JTAG时钟(JTAGTCK)

如果这些位中的任何一个的值发生变化，则后续操作将以新值确定的频率进行。

8.6.1 系统时钟(ICLK)

系统时钟(ICLK)是CPU、DMAC、DTC、Flash和SRAM的工作时钟。

ICLK频率由SCKDIVCR中的ICK[2:0]位、SCKSCR中的CKSEL[2:0]位、PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位以及HOCOFRQ0指定OFS1中的[1:0]位。

当ICLK时钟源切换时，ICLK时钟周期的持续时间在时钟源转换期间变长。请参见图8.8和图8.9。

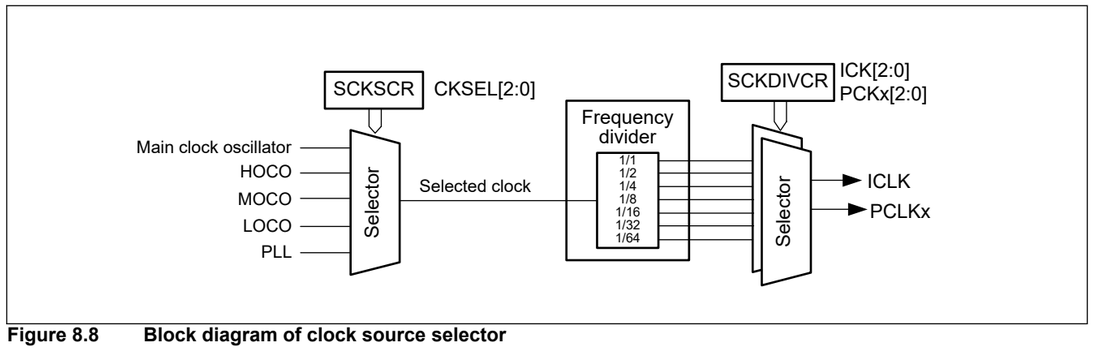


Figure 8.8 Block diagram of clock source selector

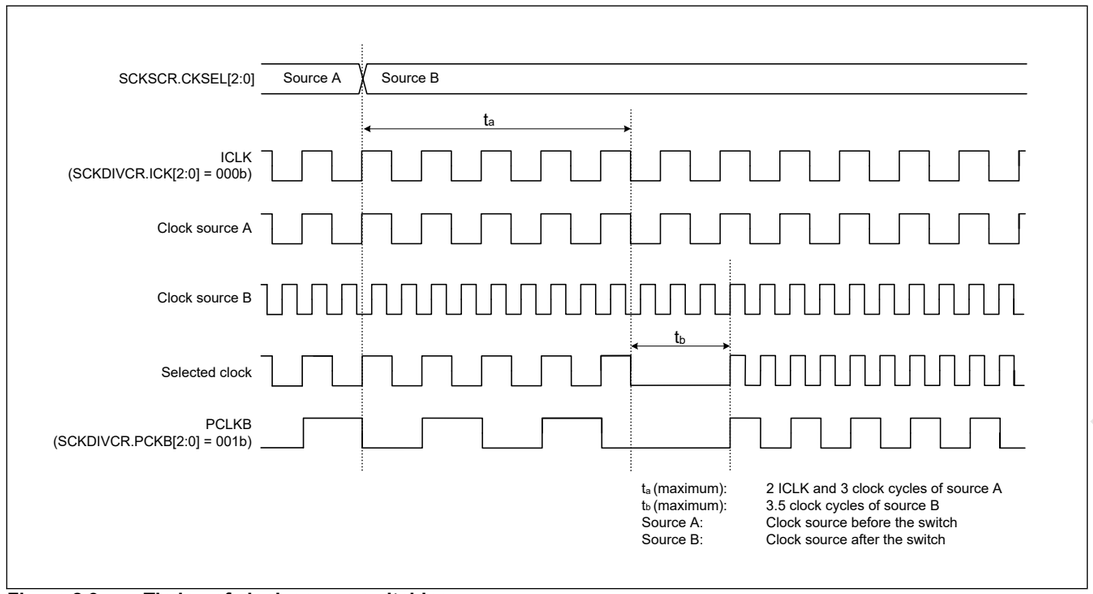


Figure 8.9 Timing of clock source switching

8.6.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

The peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD) are the operating clocks for the peripheral modules.

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0], PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

When the clock source of the peripheral module clock is switched, the duration of the peripheral module clock cycle becomes longer during the clock source transition period. See Figure 8.8 and Figure 8.9.

8.6.3 FlashIF Clock (FCLK)

The flash interface clock (FCLK) is the operating clock for the flash memory interface. In addition to reading from the data flash, FCLK is used for the programming and erasure of the code flash and data flash.

The FCLK frequency is specified in the following bits:

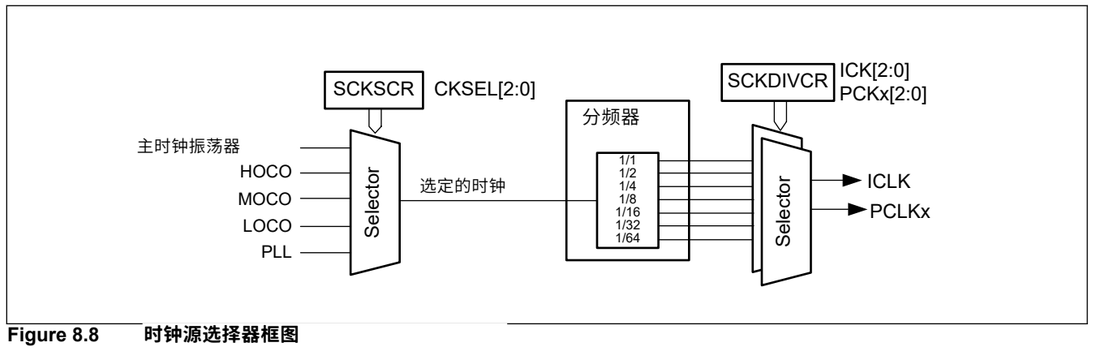


Figure 8.8 时钟源选择器框图

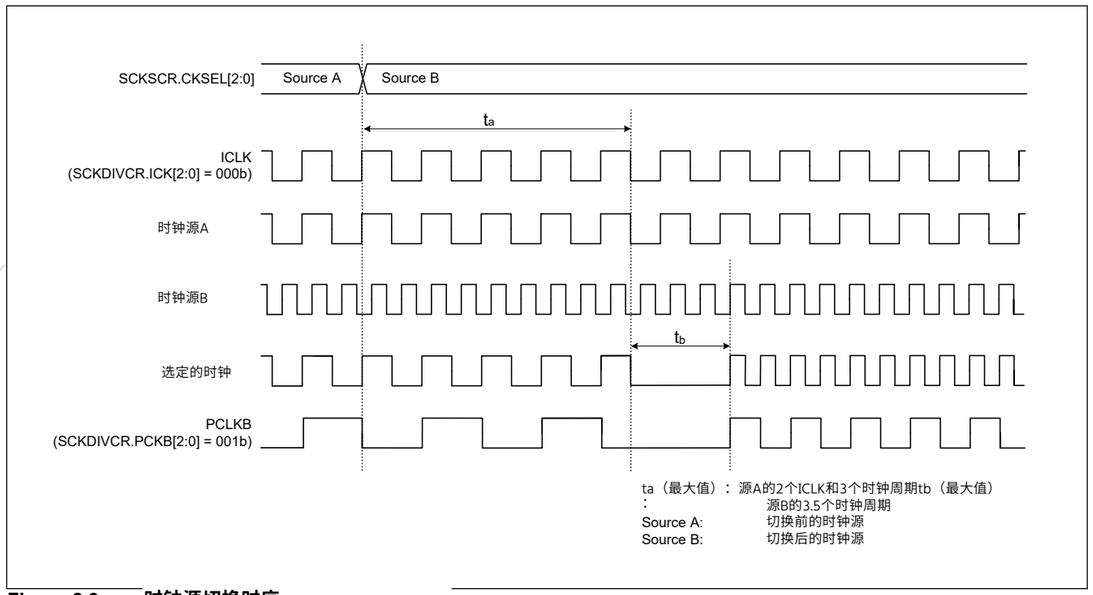


Figure 8.9 时钟源切换时序

8.6.2 外设模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）

外围模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）是外围模块的工作时钟。

给定时钟的频率在以下位中指定：

- SCKDIVCR中的PCKA[2:0]、PCKB[2:0]、PCKC[2:0]、PCKD[2:0]位
- SCKSCR中的CKSEL[2:0]位
- PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位
- OFS1中的HOCOFRQ0[1:0]位。

当外围模块时钟的时钟源切换时，外围模块时钟周期的持续时间在时钟源转换期间会变长。请参见图8.8和图8.9。

8.6.3 FlashIF Clock (FCLK)

闪存接口时钟(FCLK)是闪存接口的工作时钟。除了从数据闪存读取外，FCLK还用于代码闪存和数据闪存的编程和擦除。

FCLK频率在以下位中指定：

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

8.6.4 GPT Clock (GPTCLK)

The GPT clock (GPTCLK) is the operating clock for the GPT module.

The GPTCLK frequency is specified in the following bits:

- GPTCKSEL[2:0] bits in GPTCKCR
- GPTCKDIV[2:0] bits in GPTCKDIVCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- PLL2MUL[5:0] and PL2IDIV[1:0] bits in PLL2CCR
- HOCOFRQ0[1:0] bits in OFS1.

8.6.5 SCI SPI clock (SCISPICLK)

The SCI SPI clock (SCISPICLK) is the operating clock for the SCI and SPI module.

The SCISPICLK frequency is specified in the following bits:

- SCISPICKSEL[2:0] bits in SCISPICKCR
- SCISPICKDIV[2:0] bits in SCISPICKDIVCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- PLL2MUL[5:0] and PL2IDIV[1:0] bits in PLL2CCR
- HOCOFRQ0[1:0] bits in OFS1.

8.6.6 CAN Clock (CANMCLK)

The CAN clock, CANMCLK, is the operating clock for the CANFD module. CANMCLK is generated by the main clock oscillator.

8.6.7 CANFD clock (CANFDCLK)

The CANFD clock (CANFDCLK) is the operating clock for the CANFD module.

The CANFDCLK frequency is specified in the following bits:

- CANFDCKSEL[2:0] bits in CANFDCKCR
- CANFDCKDIV[2:0] bits in CANFDCKDIVCR
- PLLMUL[5:0], and PLIDIV[1:0] bits in PLLCCR
- PLL2MUL[5:0], and PL2IDIV[1:0] bits in PLL2CCR.

8.6.8 CAC Clock (CACCLK)

The CAC clock, CACCLK, is the operating clock for the CAC. CACCLK is generated by the following oscillators:

- Main clock oscillator
- High-speed clock oscillator (HOCO)
- Middle-speed clock oscillator (MOCO)
- Low-speed on-chip oscillator (LOCO)
- IWDT-dedicated on-chip oscillator. (IWDTLOCO)

●SCKDIVCR中的FCK[2:0]位
●SCKSCR中的CKSEL[2:0]位
●PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位
●OFS1中的HOCOFRQ0[1:0]位。

8.6.4 GPT Clock (GPTCLK)

GPT时钟(GPTCLK)是GPT模块的工作时钟。

GPTCLK频率在以下位中指定：

●GPTCKCR中的GPTCKSEL[2:0]位
●GPTCKDIVCR中的GPTCKDIV[2:0]位
●PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位
●PLL2CCR中的PLL2MUL[5:0]和PL2IDIV[1:0]位
●OFS1中的HOCOFRQ0[1:0]位。

8.6.5 SCISPI时钟(SCISPICLK)

SCISPI时钟(SCISPICLK)是SCI和SPI模块的工作时钟。

SCISPICLK频率在以下位中指定：

●SCISPICKCR中的SCISPICKSEL[2:0]位
●SCISPICKDIVCR中的SCISPICKDIV[2:0]位
●PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位
●PLL2CCR中的PLL2MUL[5:0]和PL2IDIV[1:0]位
●OFS1中的HOCOFRQ0[1:0]位。

8.6.6 CAN时钟(CANMCLK)

CAN时钟CANMCLK是CANFD模块的工作时钟。CANMCLK由主时钟振荡器产生。

8.6.7 CANFD clock (CANFDCLK)

CANFD时钟(CANFDCLK)是CANFD模块的工作时钟。

CANFDCLK频率在以下位中指定：

●CANFDCKCR中的CANFDCKSEL[2:0]位
●CANFDCKDIVCR中的CANFDCKDIV[2:0]位
●PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位
●PLL2CCR中的PLL2MUL[5:0]和PL2IDIV[1:0]位。

8.6.8 CAC时钟(CACCLK)

CAC时钟CACCLK是CAC的工作时钟。CACCLK由以下振荡器产生：

●主时钟振荡器
●高速时钟振荡器（HOCO）
●中速时钟振荡器（MOCO）

- Low-speed on-chip oscillator (LOCO)
- IWDT-dedicated on-chip oscillator. (IWDTLOCO)

8.6.9 IIC clock (IICCLK)

The IIC clock (IICCLK) is the operating clock for the IIC module.

The IICCLK frequency is specified in the following bits:

- IICCKSEL[2:0] bits in IICCKCR
- IICCKDIV[2:0] bits in IICCKDIVCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- PLL2MUL[5:0] and PL2IDIV[1:0] bits in PLL2CCR
- HOCOFRQ0[1:0] bits in OFS1.

8.6.10 IWDT-Dedicated Clock (IWDTCLK)

The IWDT-dedicated clock (IWDTCLK) is the operating clock for the IWDT. IWDTCLK is internally generated by the IWDT-dedicated on-chip oscillator.

8.6.11 AGT-Dedicated LOCO Clock (AGTLCLK)

The AGT-dedicated LOCO clock (AGTLCLK) is the operating clock for the AGT. AGTLCLK is generated by the LOCO clock.

8.6.12 SysTick Timer-Dedicated Clock (SYSTICCLK)

The SysTick timer-dedicated clock, SYSTICCLK, is the operating clock for the SysTick timer. SYSTICCLK is generated by the LOCO clock.

8.6.13 External Pin Output Clock (CLKOUT)

The CLKOUT is output externally from the CLKOUT pin for the clock or buzzer output. CLKOUT is output to the CLKOUT pin when CKOCR.CKOEN is set to 1. Only change the value in the CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR when the CKOCR.CKOEN bit is 0.

The CLKOUT clock frequency is specified in the following bits:

- CKODIV[2:0] or CKOSEL[2:0] in CKOCR
- HOCOFRQ0[1:0] bit in OFS1

8.6.14 JTAG Clock (JTAGTCK)

The JTAG clock (JTAGTCK) is the clock for the JTAG.

JTAGTCK is generated by the JTAG external clock (TCK).

8.7 Usage Notes

8.7.1 Notes on Clock Generation Circuit

The frequency of the following clocks supplied to each module changes according to the setting of the SCKDIVCR register:

- System clock (ICLK)
- Peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD)
- FlashIF clock (FCLK)

Each frequency must meet the following conditions:

- Each frequency must be selected within the operation-guaranteed range of the operating frequency (f) specified in the AC characteristics. See section 46, Electrical Characteristics.
- The system clock, peripheral module clock must be set according to Table 8.2.

8.6.9 IIC clock (IICCLK)

IIC时钟(IICCLK)是IIC模块的工作时钟。

IICCLK频率在以下位中指定：

●IICCKCR中的IICCKSEL[2:0]位

●IICCKDIVCR中的IICCKDIV[2:0]位

●PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位

●PLL2CCR中的PLL2MUL[5:0]和PL2IDIV[1:0]位

●OFS1中的HOCOFRQ0[1:0]位。

8.6.10 IWDT-Dedicated Clock (IWDTCLK)

IWDT专用时钟(IWDTCLK)是IWDT的工作时钟。IWDTCLK由内部产生
IWDT-dedicated on-chip oscillator.

8.6.11 AGT专用LOCO时钟(AGTLCLK)

AGT专用的LOCO时钟(AGTLCLK)是AGT的工作时钟。AGTLCLK由LOCO时钟产生。

8.6.12 SysTick Timer-Dedicated Clock (SYSTICCLK)

SysTick定时器专用时钟SYSTICCLK是SysTick定时器的工作时钟。SYSTICCLK由LOCO时钟生成。

8.6.13 外部引脚输出时钟(CLKOUT)

CLKOUT从CLKOUT引脚外部输出，用于时钟或蜂鸣器输出。CLKOUT被输出到
CKOCR.CKOEN设置为1时的CLKOUT引脚。仅更改CKODIV[2:0]或CKOSEL[2:0]位中的值
CKOCR.CKOEN位为0时的CKOCR。

CLKOUT时钟频率在以下位中指定：

●CKOCR中的CKODIV[2:0]或CKOSEL[2:0]

●OFS1中的HOCOFRQ0[1:0]位

8.6.14 JTAG Clock (JTAGTCK)

JTAG时钟(JTAGTCK)是JTAG的时钟。

JTAGTCK由JTAG外部时钟(TCK)生成。

8.7 使用说明

8.7.1 时钟产生电路注意事项

提供给每个模块的以下时钟的频率根据SCKDIVCR寄存器的设置而变化：

●系统时钟（ICLK）

●外设模块时钟（PCLKA、PCLKB、PCLKC和PCLKD）

- FlashIF clock (FCLK)

每个频率必须满足以下条件：

●各频率必须在交流特性规定的工作频率(f)的工作保证范围内选择。参见第46节，电气特性。

●系统时钟、外围模块时钟必须按照表8.2设置。

To ensure correct processing after the clock frequency changes, first write to the relevant Clock Control register to change the frequency, then read the value from the register, and finally perform the subsequent processing.

8.7.2 Notes on Board Design

When using a crystal resonator, place the resonator and its load capacitors as close to the XTAL and EXTAL pins as possible. Other signal lines should be routed away from the oscillation circuit as shown in Figure 8.10 to prevent electromagnetic induction from interfering with correct oscillation. Figure 8.10 shows the case which the main clock oscillator is used.

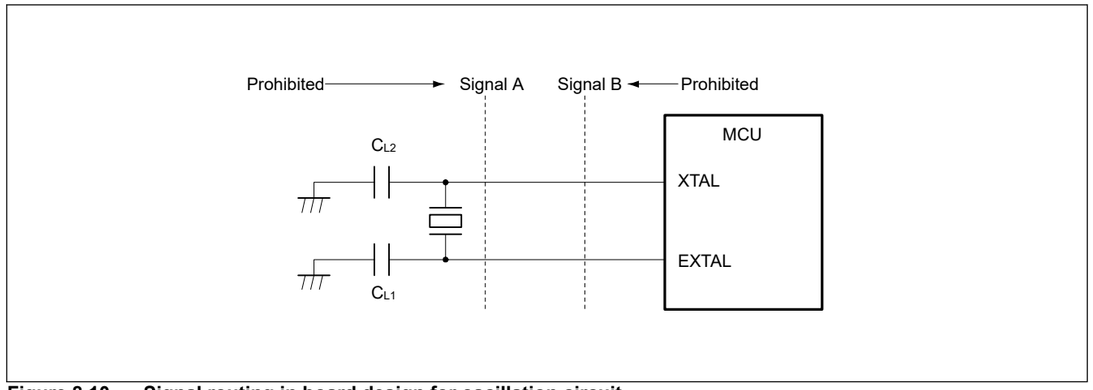


Figure 8.10 Signal routing in board design for oscillation circuit

8.7.3 Notes on Resonator Connect Pin

When the main clock is not used, the EXTAL and XTAL pins can be used as general ports. When these pins are used as general ports, the main clock must be stopped (MOSCCR.MOSTP bit should be set to 1).

为保证时钟频率改变后的正确处理，首先写入相关的ClockControl寄存器改变频率，然后从该寄存器中读取值，最后进行后续处理。

8.7.2 电路板设计注意事项

使用晶体谐振器时，将谐振器及其负载电容尽可能靠近XTAL和EXTAL引脚。其他信号线应远离振荡电路，如图8.10所示，以防止电磁感应干扰正确的振荡。图8.10显示了使用主时钟振荡器的情况。

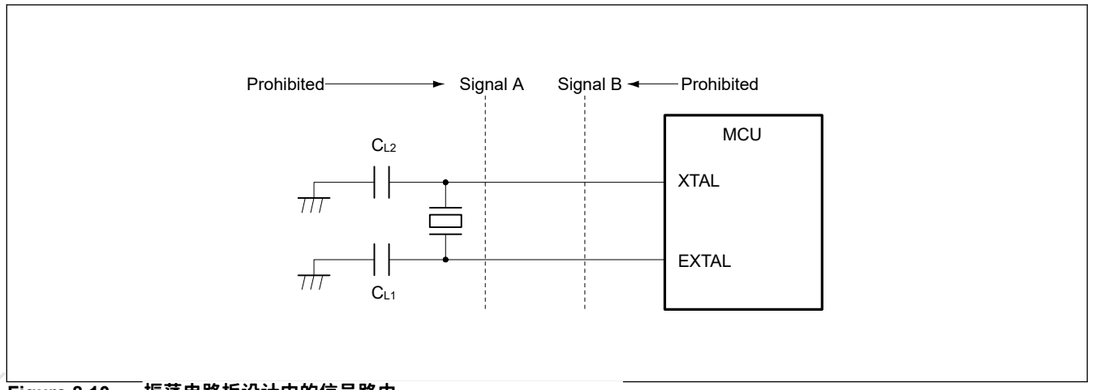


Figure 8.10 振荡电路板设计中的信号路由

8.7.3 谐振器连接引脚注意事项

当不使用主时钟时，EXTAL和XTAL引脚可用作通用端口。当这些引脚用作通用端口时，必须停止主时钟（MOSCCR.MOSTP位应设置为1）。

9. Clock Frequency Accuracy Measurement Circuit (CAC)

9.1 Overview

The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.

Table 9.1 lists the CAC specifications, Figure 9.1 shows the CAC block diagram, and Table 9.2 lists the CAC I/O pin.

Table 9.1 CAC specifications

Parameter	Specifications
Measurement target clocks	Frequency can be measured for: • Main clock oscillator • HOCO clock • MOCO clock • LOCO clock • Peripheral module clock B (PCLKB) • IWDT-dedicated clock
Measurement reference clocks	Frequency can be referenced to: • External clock input to the CACREF pin • Main clock oscillator • HOCO clock • MOCO clock • LOCO clock • Peripheral module clock B (PCLKB) • IWDT-dedicated clock
Selectable function	Digital filter
Interrupt sources	• Measurement end • Frequency error • Overflow
Module-stop function	Module-stop state can be set to reduce power consumption
TrustZone Filter	Security attribution can be set

9. 时钟频率精度测量电路(CAC)

9.1 Overview

时钟频率精度测量电路(CAC)在选择作为测量基准的时钟（测量基准时钟）产生的时间内对要测量的时钟（测量目标时钟）的脉冲进行计数，并根据脉冲数在允许范围内。当测量完成或测量参考时钟产生的时间内的脉冲数不在允许范围内时，将产生中断请求。

表9.1列出了CAC规格，图9.1显示了CAC框图，表9.2列出了CACIO引脚。

Table 9.1 CAC规格

Parameter	Specifications
测量目标时钟	可以测量频率：● 主时钟振荡器 • HOCO clock • MOCO clock • 机车时钟 • 外设模块时钟B(PCLKB) • IWDT-dedicated clock
测量参考时钟	频率可参考：● CACREF引脚的外部时钟输入 • 主时钟振荡器 • HOCO clock • MOCO clock • 机车时钟 • 外设模块时钟B(PCLKB) • IWDT-dedicated clock
可选择的功能	数字滤波器
中断源	• 测量结束 • 频率误差 • Overflow
Module-stop function	可设置模块停止状态以降低功耗
TrustZone Filter	可设置安全属性

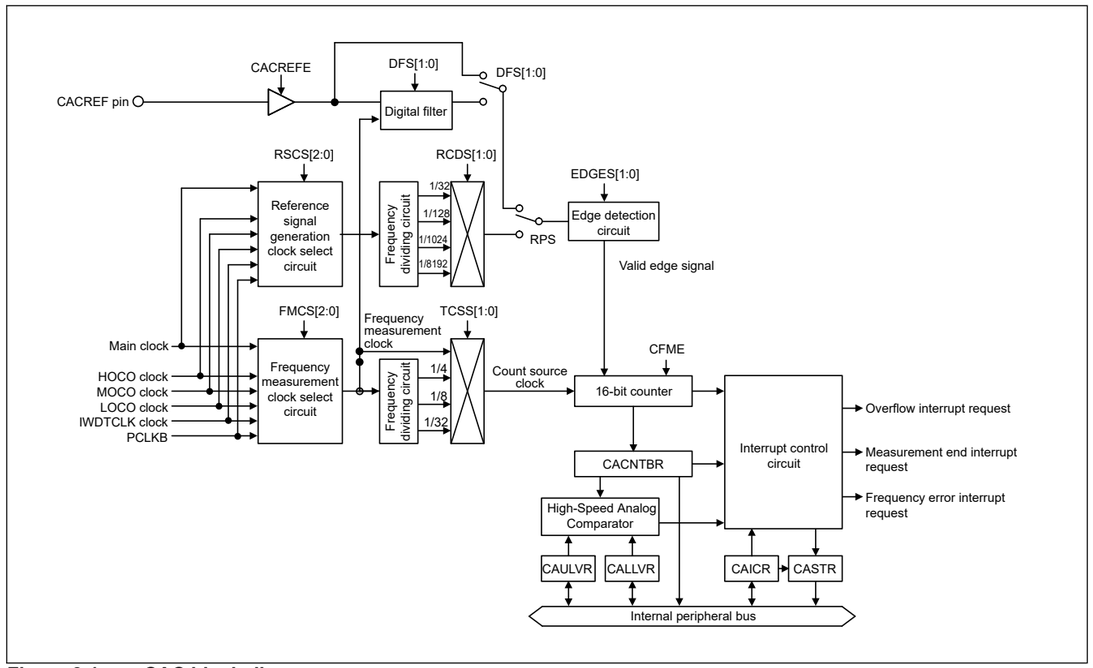


Figure 9.1 CAC block diagram

Table 9.2 CAC I/O pin

Function	Pin name	I/O	Description
CAC	CACREF	Input	Measurement reference clock input pin

9.2 Register Descriptions

9.2.1 CACR0 : CAC Control Register 0

Base address: CAC = 0x4008_3600

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFME
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFME	Clock Frequency Measurement Enable 0: Disable 1: Enable	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

CFME bit (Clock Frequency Measurement Enable)

The CFME bit enables clock frequency measurement. Changes made to this bit are not immediately reflected to the internal circuit. Read the bit to confirm that the change has been reflected.

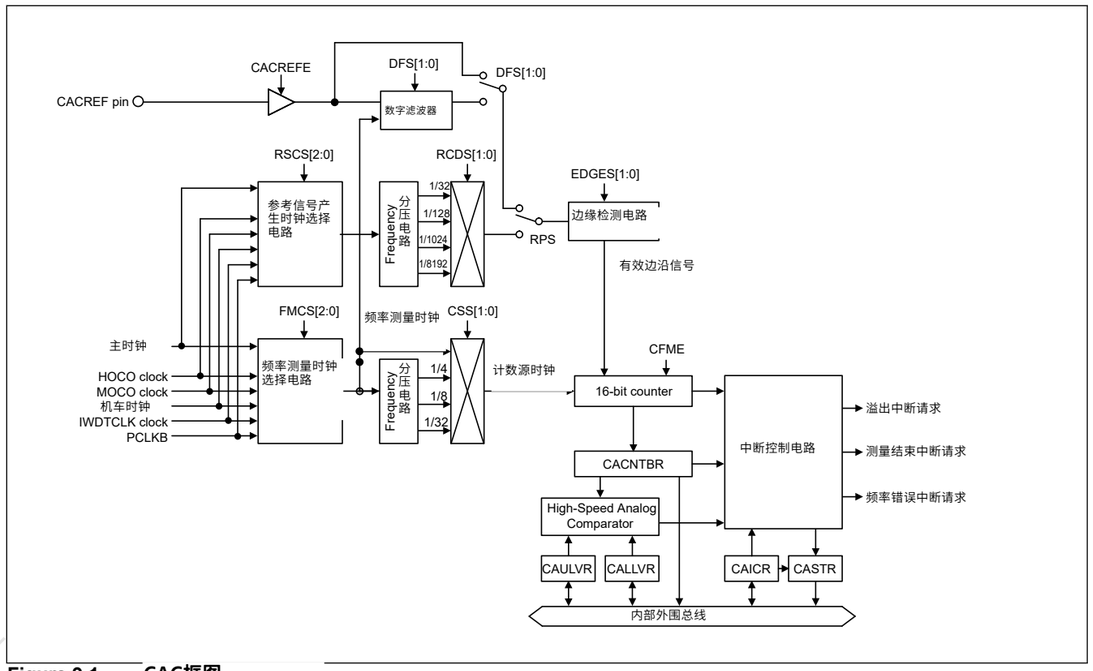


Figure 9.1 CAC框图

Table 9.2 CACIO引脚

Function	引脚名称	I/O	Description
CAC	CACREF	Input	测量参考时钟输入引脚

9.2 注册说明

9.2.1 CACR0:CAC控制寄存器0

Base address: CAC = 0x4008_3600

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFME
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFME	时钟频率测量启用 0：禁用1 ：启用	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

CFME位（时钟频率测量使能）

CFME位使能时钟频率测量。对该位所做的更改不会立即反映到内部电路。读取该位以确认更改已反映。

9.2.2 CACR1 : CAC Control Register 1

Base address: CAC = 0x4008_3600

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	EDGES[1:0]		TCSS[1:0]		FMCS[2:0]			CACREFE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CACREFE	CACREF Pin Input Enable 0: Disable 1: Enable	R/W
3:1	FMCS[2:0]	Measurement Target Clock Select 0 0 0: Main clock oscillator 0 0 1: Setting prohibited 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: IWDT-dedicated clock 1 1 1: Setting prohibited	R/W
5:4	TCSS[1:0]	Timer Count Clock Source Select 0 0: No division 0 1: × 1/4 clock 1 0: × 1/8 clock 1 1: × 1/32 clock	R/W
7:6	EDGES[1:0]	Valid Edge Select 0 0: Rising edge 0 1: Falling edge 1 0: Both rising and falling edges 1 1: Setting prohibited	R/W

Note: Set the CACR1 register when the CACR0.CFME bit is 0.

CACREFE bit (CACREF Pin Input Enable)

The CACREFE bit enables the CACREF pin input.

FMCS[2:0] bits (Measurement Target Clock Select)

The FMCS[2:0] bits select the measurement target clock whose frequency is to be measured.

TCSS[1:0] bits (Timer Count Clock Source Select)

The TCSS[1:0] bits select the division ratio of the measurement target clock.

EDGES[1:0] bits (Valid Edge Select)

The EDGES[1:0] bits select the valid edge for the reference signal.

9.2.3 CACR2 : CAC Control Register 2

Base address: CAC = 0x4008_3600

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DFS[1:0]		RCDS[1:0]		RSCS[2:0]			RPS
Value after reset:	0	0	0	0	0	0	0	0

9.2.2 CACR1：CAC控制寄存器1

Base address: CAC = 0x4008_3600

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	EDGES[1:0]		TCSS[1:0]		FMCS[2:0]			CACREFE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CACREFE	CACREF引脚输入使能 0：禁用1 ：启用	R/W
3:1	FMCS[2:0]	测量目标时钟选择 000：主时钟振荡器001：禁止设置010：HOCO时钟011：MOCO时钟100：LOCO时钟101：外围模块时钟B(PCLKB)110：IWDT专用时钟111：禁止设定	R/W
5:4	TCSS[1:0]	定时器计数时钟源选择 00：不分频01：×14个时钟10：×18个时钟11：×132个时钟	R/W
7:6	EDGES[1:0]	有效边选择 00：上升沿01：下降沿10：上升沿和下降沿11：禁止设置	R/W

Note: 当CACR0.CFME位为0时设置CACR1寄存器。

CACREFE位（CACREF引脚输入使能）

CACREFE位使能CACREF引脚输入。

FMCS[2:0]位（测量目标时钟选择）

FMCS[2:0]位选择要测量其频率的测量目标时钟。

TCSS[1:0]位（定时器计数时钟源选择）

TCSS[1:0]位选择测量目标时钟的分频比。

EDGES[1:0]位（有效边沿选择）

EDGES[1:0]位选择参考信号的有效边沿。

9.2.3 CACR2：CAC控制寄存器2

Base address: CAC = 0x4008_3600

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DFS[1:0]		RCDS[1:0]		RSCS[2:0]			RPS
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPS	Reference Signal Select 0: CACREF pin input 1: Internal clock (internally generated signal)	R/W
3:1	RSCS[2:0]	Measurement Reference Clock Select 0 0 0: Main clock oscillator 0 0 1: Setting prohibited 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: IWDT-dedicated clock 1 1 1: Setting prohibited	R/W
5:4	RCDS[1:0]	Measurement Reference Clock Frequency Division Ratio Select 0 0: × 1/32 clock 0 1: × 1/128 clock 1 0: × 1/1024 clock 1 1: × 1/8192 clock	R/W
7:6	DFS[1:0]	Digital Filter Select 0 0: Disable digital filtering 0 1: Use sampling clock for the digital filter as the frequency measuring clock 1 0: Use sampling clock for the digital filter as the frequency measuring clock divided by 4 1 1: Use sampling clock for the digital filter as the frequency measuring clock divided by 16.	R/W

Note: Set the CACR2 register when the CACR0.CFME bit is 0.

RPS bit (Reference Signal Select)

The RPS bit selects whether to use the CACREF pin input or an internal clock (internally generated signal) as the reference signal.

RSCS[2:0] bits (Measurement Reference Clock Select)

The RSCS[2:0] bits select the reference clock for measurement.

RCDS[1:0] bits (Measurement Reference Clock Frequency Division Ratio Select)

The RCDS[1:0] bits select the frequency-divisor of the reference clock for measurement when an internal reference clock is selected. When RPS = 0 (CACREF pin is used as the reference clock source), the reference clock is not divided.

DFS[1:0] bits (Digital Filter Select)

The DFS[1:0] bits enable or disable the digital filter and selects its sampling clock.

9.2.4 CAICR : CAC Interrupt Control Register

Base address: CAC = 0x4008_3600

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FERRIE	Frequency Error Interrupt Request Enable 0: Disable 1: Enable	R/W
1	MENDIE	Measurement End Interrupt Request Enable 0: Disable 1: Enable	R/W

Bit	Symbol	Function	R/W
0	RPS	参考信号选择 0：CACREF引脚输入1：内部时钟（内部产生的信号）	R/W
3:1	RSCS[2:0]	测量参考时钟选择 000：主时钟振荡器001：禁止设置010：HOCO时钟011：MOCO时钟100：LOCO时钟101：外围模块时钟B(PCLKB)110：IWDT专用时钟111：禁止设定	R/W
5:4	RCDS[1:0]	测量参考时钟分频比选择 0 0: × 1/32 clock 0 1: × 1/128 clock 1 0: × 1/1024 clock 1 1: × 1/8192 clock	R/W
7:6	DFS[1:0]	数字滤波器选择 00：关闭数字滤波01：使用数字滤波器的采样时钟作为测频时钟10：使用数字滤波器的采样时钟作为测频时钟的4分频 11：使用数字滤波器的采样时钟作为频率测量时钟除以16。	R/W

Note: 当CACR0.CFME位为0时设置CACR2寄存器。

RPS位（参考信号选择）

RPS位选择是使用CACREF引脚输入还是使用内部时钟（内部产生的信号）作为参考信号。

RSCS[2:0]位（测量参考时钟选择）

RSCS[2:0]位选择用于测量的参考时钟。

RCDS[1:0]位（测量参考时钟分频比选择）

TheRCDS[1:0]bitsselectthefrequency-divisorofthereferececlockformeasurementwhenaninternalreferenceclockisselected.当RPS=0（CACREF引脚用作参考时钟源）时，参考时钟不分频。

DFS[1:0]位（数字滤波器选择）

DFS[1:0]位启用或禁用数字滤波器并选择其采样时钟。

9.2.4 CAICR:CAC中断控制寄存器

Base address: CAC = 0x4008_3600

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FERRIE	频率错误中断请求使能 0：禁用1 ：启用	R/W
1	MENDIE	测量结束中断请求使能 0：禁用1 ：启用	R/W

Bit	Symbol	Function	R/W
2	OVFIE	Overflow Interrupt Request Enable 0: Disable 1: Enable	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	FERRFCL	FERRF Clear 0: No effect 1: The CASTR.FERRF flag is cleared	W
5	MENDFCL	MENDF Clear 0: No effect 1: The CASTR.MENDF flag is cleared	W
6	OVFFCL	OVFF Clear 0: No effect 1: The CASTR.OVFF flag is cleared.	W
7	—	This bit is read as 0. The write value should be 0.	R/W

FERRIE bit (Frequency Error Interrupt Request Enable)

The FERRIE bit enables or disables the frequency error interrupt request.

MENDIE bit (Measurement End Interrupt Request Enable)

The MENDIE bit enables or disables the measurement end interrupt request.

OVFIE bit (Overflow Interrupt Request Enable)

The OVFIE bit enables or disables the overflow interrupt request.

FERRFCL bit (FERRF Clear)

Setting the FERRFCL bit to 1 clears the CASTR.FERRF flag.

MENDFCL bit (MENDF Clear)

Setting the MENDFCL bit to 1 clears the CASTR.MENDF flag.

OVFFCL bit (OVFF Clear)

Setting the OVFFCL bit to 1 clears the CASTR.OVFF flag.

9.2.5 CASTR : CAC Status Register

Base address: CAC = 0x4008_3600

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	OVFF	MENDF	FERRF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FERRF	Frequency Error Flag 0: Clock frequency is within the allowable range 1: Clock frequency has deviated beyond the allowable range (frequency error).	R
1	MENDF	Measurement End Flag 0: Measurement is in progress 1: Measurement ended	R
2	OVFF	Overflow Flag 0: Counter has not overflowed 1: Counter overflowed	R
7:3	—	These bits are read as 0.	R

Bit	Symbol	Function	R/W
2	OVFIE	溢出中断请求使能 0：禁用1 ：启用	R/W
3	—	该位读取为0。写入值应为0。	R/W
4	FERRFCL	FERRF Clear 0：无效1：清除CASTR.FERRF标志	W
5	MENDFCL	MENDF Clear 0：无效1：清除CASTR.MENDF标志	W
6	OVFFCL	OVFF Clear 0：无效1：清除CASTR.OVFF标志。	W
7	—	该位读取为0。写入值应为0。	R/W

FERRIE位（频率错误中断请求使能）

FERRIE位启用或禁用频率错误中断请求。

MENDIE位（测量结束中断请求使能）

MENDIE位启用或禁用测量结束中断请求。

OVFIE位（溢出中断请求使能）

OVFIE位启用或禁用溢出中断请求。

FERRFCL bit (FERRF Clear)

将FERRFCL位设置为1会清除CASTR.FERRF标志。

MENDFCL bit (MENDF Clear)

将MENDFCL位设置为1会清除CASTR.MENDF标志。

OVFFCL bit (OVFF Clear)

将OVFFCL位设置为1会清除CASTR.OVFF标志。

9.2.5 CASTR:CAC状态寄存器

Base address: CAC = 0x4008_3600

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	OVFF	MENDF	FERRF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FERRF	频率错误标志 0：时钟频率在允许范围内1：时钟频率偏离允许范围（频率误差）。	R
1	MENDF	测量结束标志 0：测量中1：测量结束	R
2	OVFF	溢出标志 0：计数器未溢出1：计数器溢出	R
7:3	—	这些位读为0。	R

FERRF flag (Frequency Error Flag)

The FERRF flag indicates a deviation of the clock frequency from the set value (frequency error).

[Setting condition]

- The clock frequency is outside the allowable range defined in the CAULVR and CALLVR registers.

[Clearing condition]

- 1 is written to the FERRFCL bit.

MENDF flag (Measurement End Flag)

The MENDF flag indicates the end of measurement.

[Setting condition]

- Measurement ends.

[Clearing condition]

- 1 is written to the MENDFCL bit.

OVFF flag (Overflow Flag)

The OVFF flag indicates that the counter overflowed.

[Setting condition]

- The counter overflows.

[Clearing condition]

- 1 is written to the CAICR.OVFFCL bit.

9.2.6 CAULVR : CAC Upper-Limit Value Setting Register

Base address: CAC = 0x4008_3600

Offset address: 0x06

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	The Upper Value of the Allowable Range The CAULVR register is a 16-bit read/write register that specifies the upper value of the allowable range. When the counter value exceeds the value specified in this register, a frequency error is detected. Write to this register when the CACR0.CFME bit is 0. The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit, and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.	R/W

9.2.7 CALLVR : CAC Lower-Limit Value Setting Register

Base address: CAC = 0x4008_3600

Offset address: 0x08

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FERRF标志（频率错误标志）

FERRF标志表示时钟频率与设定值的偏差（频率误差）。

[Setting condition]

●时钟频率超出CAULVR和CALLVR寄存器中定义的允许范围。

[Clearing condition]

●1写入FERRFCL位。

MENDF标志（测量结束标志）

MENDF标志表示测量结束。

[Setting condition]

●测量结束。

[Clearing condition]

●1写入MENDFCL位。

OVFF flag (Overflow Flag)

OVFF标志表示计数器溢出。

[Setting condition]

●计数器溢出。

[Clearing condition]

●1写入CAICR.OVFFCL位。

9.2.6 CAULVR:CAC上限值设置寄存器

Base address: CAC = 0x4008_3600

Offset address: 0x06

Bit position:	15															0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	允许范围的上限值 CAULVR寄存器是一个16位读写寄存器，用于指定允许范围的上限值。当计数器值超过此寄存器中指定的值时，检测到频率错误。当CACR0.CFME位为0时写入该寄存器。存储在CACNTBR中的计数器值会根据数字滤波器和边沿检测电路的相位差以及CACREF引脚上的信号而变化。确保此设置允许有足够的余量。	R/W

9.2.7 CALLVR:CAC下限值设置寄存器

Base address: CAC = 0x4008_3600

Offset address: 0x08

Bit position:	15															0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	The Lower Value of the Allowable Range The CALLVR register is a 16-bit read/write register that specifies the lower value of the allowable range. When the counter value falls below the value specified in this register, a frequency error is detected. Write to this register when the CACR0.CFME bit is 0. The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit, and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.	R/W

9.2.8 CACNTBR : CAC Counter Buffer Register

Base address: CAC = 0x4008_3600

Offset address: 0x0A

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	The Measurement Result The CACNTBR register is a 16-bit read-only register that stores the measurement result.	R

9.3 Operation

9.3.1 Measuring Clock Frequency

The CAC measures the clock frequency using the CACREF pin input or an internal clock as a reference. Figure 9.2 shows an operating example of the CAC.

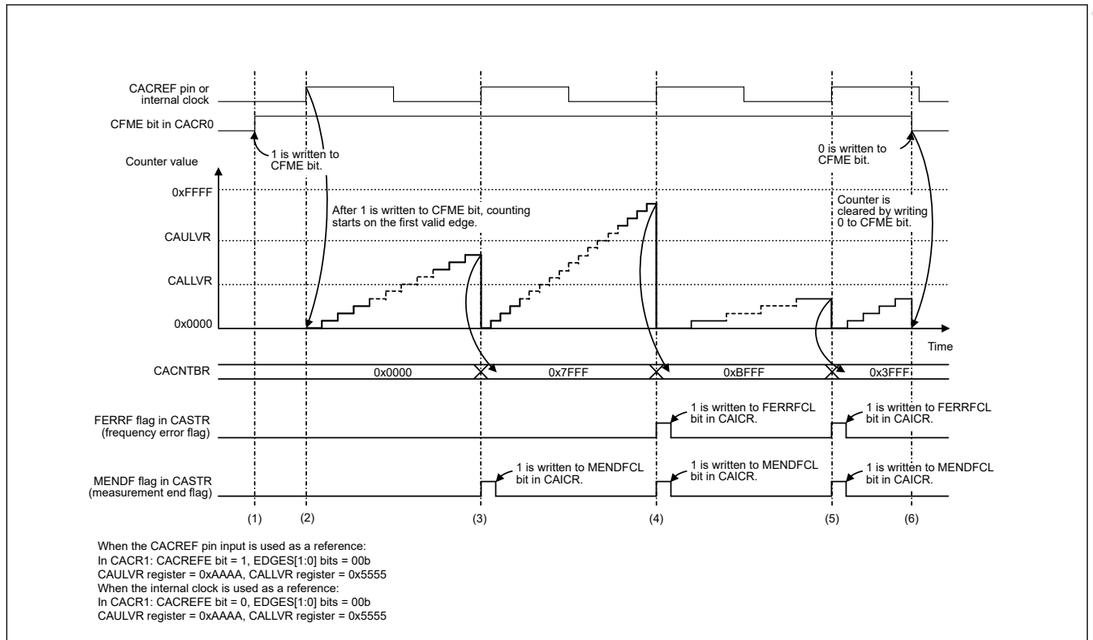


Figure 9.2 CAC operating example

Bit	Symbol	Function	R/W
15:0	n/a	允许范围的下限值 CALLVR寄存器是一个16位读写寄存器，用于指定允许范围的下限值。当计数器值低于此寄存器中指定的值时，检测到频率错误。当CACR0.CFME位为0时写入该寄存器。存储在CACNTBR中的计数器值会根据数字滤波器和边沿检测电路的相位差以及CACREF引脚上的信号而变化。确保此设置允许有足够的余量。	R/W

9.2.8 CACNTBR:CAC计数器缓冲寄存器

Base address: CAC = 0x4008_3600

Offset address: 0x0A

Bit position:	15															0
Bit field:																
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	测量结果 CACNTBR寄存器是一个16位只读寄存器，用于存储测量结果。	R

9.3 Operation

9.3.1 测量时钟频率

CAC使用CACREF引脚输入或内部时钟作为参考来测量时钟频率。图9.2显示了CAC的操作示例。

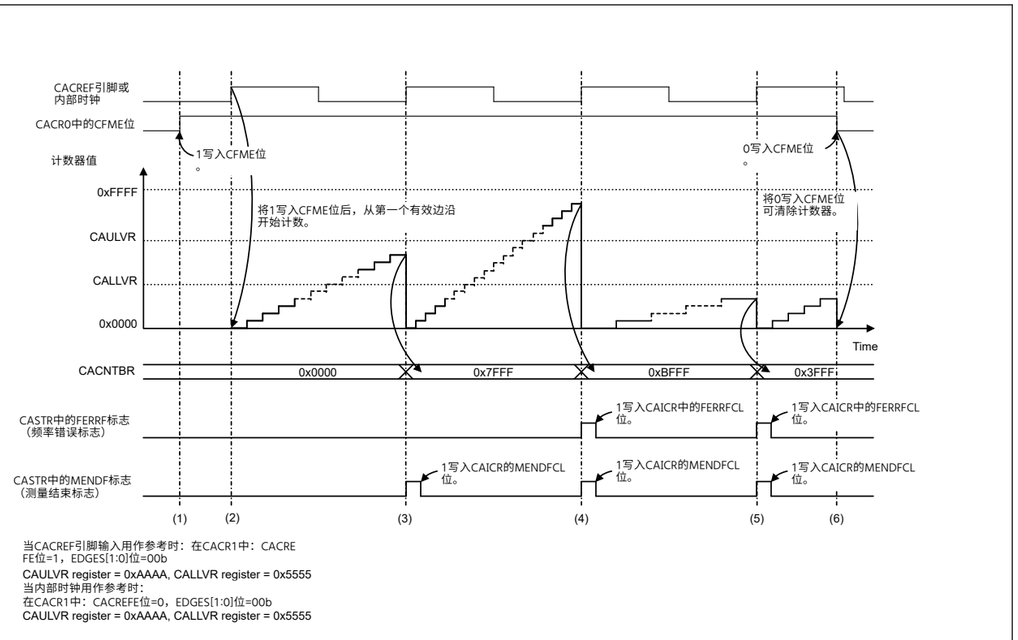


Figure 9.2 CAC操作示例

The events in Figure 9.2 are:

1. When the CACREF pin input is used as reference (CACR1.CACREFE = 1), frequency measurement is enabled by writing 1 to the CACR0.CFME bit while the CACR2.RPS bit is set to 0 and the CACR1.CACREFE bit is set to 1. When the internal clock is used as reference (CACR1.CACREFE = 0), frequency measurement is enabled by writing 1 to the CACR0.CFME bit while the CACR2.RPS bit is set to 1.
2. When the CACREF pin input is used as reference, after 1 is written to the CFME bit, the timer starts up-counting if the valid edge selected by the CACR1.EDGES[1:0] bits (rising edge (CACR1.EDGES[1:0] = 00b) in Figure 9.2) is input from the CACREF pin. When the internal clock is used as reference, after 1 is written to the CFME bit, the timer starts up-counting if the valid edge selected by the CACR1.EDGES[1:0] bits (rising edge (CACR1.EDGES[1:0] = 00b) in Figure 9.2) is input based on the clock source selected by the CACR2.RSCS[2:0] bits.
3. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If both CACNTBR ≤ CAULVR and CACNTBR ≥ CALLVR are true, only the MENDF flag in CASTR is set to 1, because the clock frequency is correct. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
4. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If CACNTBR > CAULVR, the FERRF flag in CASTR is set to 1, because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
5. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If CACNTBR < CALLVR, the FERRF flag in CASTR is set to 1, because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
6. When the CFME bit in CACR0 is 1, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR every time a valid edge is input. Writing 0 to the CFME bit in CACR0 clears the counter and stops up-counting.

9.3.2 Digital Filtering of Signals on CACREF Pin

The CACREF pin has a digital filter, and levels on the CACREF pin are transmitted to the internal circuitry after three consecutive matches in the selected sampling interval. The same level continues to be transmitted internally until the level on the pin has three consecutive matches again. Enabling or disabling of the digital filter and its sampling clock are selectable.

The counter value transferred to CACNTBR might be in error by up to 1 cycle of the sampling clock because of the difference between the phases of the digital filter and the signal input to the CACREF pin. When a frequency dividing clock is selected as a count source clock, the counter value error is obtained using the following formula:

Counter value error = (1 cycle of the count source clock)/ (1 cycle of the sampling clock)

9.4 Interrupt Requests

The CAC generates three types of interrupt requests:

- Frequency error interrupt
- Measurement end interrupt
- Overflow interrupt

When an interrupt source is generated, the associated status flag is set to 1. Table 9.3 provides information on the CAC interrupt requests.

Table 9.3 CAC interrupt requests (1 of 2)

Interrupt request	Interrupt enable bit	Status flag	Interrupt sources
Frequency error interrupt	CAICR.FERRIE	CASTR.FERRF	The result of comparing CACNTBR with CAULVR and CALLVR is either CACNTBR > CAULVR or CACNTBR < CALLVR

图9.2中的事件是：

1.当CACREF引脚输入用作参考时（CACR1.CACREFE=1），频率测量通过以下方式启用
将1写入CACR0.CFME位，同时将CACR2.RPS位设置为0，并将CACR1.CACREFE位设置为1。当内部时钟用作参考时(CACR1.CACREFE=0)，频率测量通过以下方式启用将1写入CACR0.CFME位，同时CACR2.RPS位设置为1。

2.当CACREF引脚输入用作参考时，向CFME位写入1后，如果CACR1.EDGES[1:0]位选择的有效沿（上升沿（CACR1.EDGES图9.2中的[1:0]=00b))从CACREF引脚输入。当内部时钟用作参考时，CFME位写入1后，如果CACR1.EDGES[1:0]位选择的有效沿（上升沿（CACR1.EDGES[1:图9.2中的0]=00b))根据CACR2.RSCS[2:0]位选择的时钟源输入。

3.当输入下一个有效边沿时，计数器值被传送到CACNTBR并与中的值进行比较
CAULVR和CALLVR。如果CACNTBR≤CAULVR和CACNTBR≥CALLVR都为真，则只有MENDF标志CASTR设置为1，因为时钟频率正确。如果CAICR中的MENDIE位为1，则产生测量结束中断。

4.当输入下一个有效边沿时，计数器值被传送到CACNTBR并与中的值进行比较
CAULVR和CALLVR。如果CACNTBR>CAULVR，则CASTR中的FERRF标志设置为1，因为时钟频率错误。如果CAICR中的FERRIE位为1，则产生频率错误中断。CASTR中的MENDF标志在测量结束时设置为1。如果CAICR中的MENDIE位为1，则产生测量结束中断。

5.当输入下一个有效边沿时，计数器值被传送到CACNTBR并与中的值进行比较
CAULVR和CALLVR。如果CACNTBR<CALLVR，则CASTR中的FERRF标志设置为1，因为时钟频率错误。如果CAICR中的FERRIE位为1，则产生频率错误中断。CASTR中的MENDF标志在测量结束时设置为1。如果CAICR中的MENDIE位为1，则产生测量结束中断。

6.当CACR0中的CFME位为1时，每次输入有效边沿时，计数器值被传送到CACNTBR并与CAULVR和CALLVR中的值进行比较。向CACR0中的CFME位写入0将清除计数器并停止向上计数。

9.3.2 CACREF引脚上的信号数字滤波

CACREF引脚有一个数字滤波器，CACREF引脚上的电平在选定的采样间隔内连续三个匹配后传输到内部电路。同一电平继续在内部传输，直到引脚上的电平再次连续匹配三个。可选择启用或禁用数字滤波器及其采样时钟。

由于数字滤波器的相位和输入到CACREF引脚的信号之间的差异，传输到CACNTBR的计数器值可能会出现最多1个采样时钟周期的错误。Whenafrequencydividingclockisselectedasacountsourceclock thecountervalueerrorisobtainedusingthefollowingformula:

计数器值误差=（计数源时钟的1个周期）（采样时钟的1个周期）

9.4 中断请求

CAC产生三种类型的中断请求：

●频率错误中断
●测量结束中断
●溢出中断

产生中断源时，相关状态标志设置为1。表9.3提供了有关CAC中断请求的信息。

Table 9.3 CAC中断请求(1of2)

中断请求	中断使能位	状态标志	中断源
频率错误中断	CAICR.FERRIE	CASTR.FERRF	CACNTBR与CAULVR和CALLVR比较的结果是CACNTBR>CAULVR或CACNTBR<CALLVR

Table 9.3 CAC interrupt requests (2 of 2)

Interrupt request	Interrupt enable bit	Status flag	Interrupt sources
Measurement end interrupt	CAICR.MENDIE	CASTR.MENDF	• Valid edge is input from the CACREF pin or internal clock • Measurement end interrupt does not occur at the first valid edge after writing 1 to the CACR0.CFME bit
Overflow interrupt	CAICR.OVFIE	CASTR.OVFF	Counter overflows

9.5 Usage Notes

9.5.1 Settings for the Module-Stop Function

The Module Stop Control Register C (MSTPCRC) can enable or disable CAC operation. The CAC module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

Table 9.3 CAC中断请求（2个中的2个）

中断请求	中断使能位	状态标志	中断源
测量结束中断	CAICR.MENDIE	CASTR.MENDF	• 有效边沿从CACREF引脚或内部时钟输入 • 将1写入CACR0.CFME位后，在第一个有效边沿不发生测量结束中断
溢出中断	CAICR.OVFIE	CASTR.OVFF	计数器溢出

9.5 使用说明

9.5.1 模块停止功能的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用CAC操作。CAC模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

10. Low Power Modes

10.1 Overview

The MCU has several functions for reducing power consumption, such as setting clock dividers, stopping modules, selecting power control mode in Normal mode, and transitioning to low power modes.

Table 10.1 lists the specifications of the low power mode functions. Table 10.2 lists the conditions to transition to low power modes, the states of the CPU and peripheral modules, and the method for canceling each mode. After a reset, the MCU enters the program execution state, but only the DTC, DMAC and SRAM operate.

Table 10.1 Specifications of the low power mode functions

Item	Specification
Reducing power consumption by switching clock signals	The frequency division ratio can be selected independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), and flash interface clock (FCLK). *1
Module stop	Functions can be stopped independently for each peripheral module
Low-power modes	• Sleep mode • Software Standby mode • Snooze mode • Deep Software Standby mode
Power control modes	• Power consumption can be reduced in Normal and Sleep modes by selecting an appropriate operating power control mode according to the operating frequency. • Three operating power control modes are available: High-speed mode Low-speed mode
TrustZone Filter	Security attribution can be set for each registers

Note 1. For details, see section 8, Clock Generation Circuit

Table 10.2 Operating conditions of each low power mode (1 of 2)

Item	Sleep mode	Software Standby mode	Snooze mode	Deep Software Standby mode
Transition condition	WFI instruction while SBYCR.SSBY = 0	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 0	Snooze request trigger in Software Standby mode. SNZCR.SNZE=1.	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 1
Canceling method	All interrupts. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.
State after cancellation by an interrupt	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Reset state
State after cancellation by a reset	Reset state	Reset state	Reset state	Reset state
Main clock oscillator	Selectable	Stop	Selectable*4	Stop
High-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Middle-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Low-speed on-chip oscillator	Selectable	Selectable	Selectable	Selectable*7
IWDT-dedicated on-chip oscillator	Selectable*1	Selectable*1	Selectable*1	Stop
PLL	Selectable	Stop	Selectable*4	Stop
PLL2	Selectable	Stop	Selectable*4	Stop
Oscillation stop detection function	Selectable	Operation prohibited	Operation prohibited	Operation prohibited
Clock/buzzer output function	Selectable	Selectable*2	Selectable	Stop (Undefined)
CPU	Stop (Retained)	Stop (Retained)	Stop (Retained)	Stop (Undefined)
SRAMn (n = 0)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Standby SRAM	Selectable	Stop (Retained)	Selectable	Stop (Retained/Undefined)*8
Flash memory	Operating	Stop (Retained)	Stop (Retained)	Stop (Retained)

10. 低功耗模式

10.1 Overview

MCU具有多种降低功耗的功能，例如设置时钟分频器、停止模块、在正常模式下选择电源控制模式以及转换到低功耗模式。

表10.1列出了低功耗模式功能的规格。表10.2列出了转换到低功耗模式的条件、CPU和外围模块的状态以及取消每种模式的方法。复位后，MCU进入程序执行状态，但只有DTC、DMAC和SRAM运行。

Table 10.1 低功耗模式功能的规格

Item	Specification
通过切换时钟信号降低功耗	分频比可以为系统时钟（ICLK）、外围模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）和闪存接口时钟（FCLK）独立选择。*1
模块停止	每个外围模块可以独立停止功能
Low-power modes	• 睡眠模式 • 软件待机模式 • 贪睡模式 • 深度软件待机模式
电源控制模式	• 根据工作频率选择合适的工作功率控制模式，可以降低正常和睡眠模式下的功耗。 • 提供三种工作功率控制模式： High-speed mode Low-speed mode
TrustZone Filter	可以为每个寄存器设置安全属性

注1.详见第8节，时钟产生电路

Table 10.2 每种低功耗模式的运行条件（2个中的1个）

Item	睡眠模式	软件待机模式	贪睡模式	深度软件待机模式
过渡条件	WFI指令同时 SBYCR.SSBY = 0	WFI指令同时 SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 0	软件待机模式下的贪睡请求触发。 SNZCR.SNZE=1.	WFI指令同时 SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 1
取消方法	所有中断。 该模式下可用的任何复位。	中断如表10.3所示。该模式下可用的任何复位。	中断如表10.3所示。该模式下可用的任何复位。	中断如表10.3所示。该模式下可用的任何复位。
中断取消后的状态	程序执行状态（中断处理）	程序执行状态（中断处理）	程序执行状态（中断处理）	重置状态
通过复位取消后的状态	重置状态	重置状态	重置状态	重置状态
主时钟振荡器	Selectable	Stop	Selectable*4	Stop
High-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Middle-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Low-speed on-chip oscillator	Selectable	Selectable	Selectable	Selectable*7
IWDT-dedicated on-chip oscillator	Selectable*1	Selectable*1	Selectable*1	Stop
PLL	Selectable	Stop	Selectable*4	Stop
PLL2	Selectable	Stop	Selectable*4	Stop
振荡停止检测功能	Selectable	禁止操作	禁止操作	禁止操作
时钟蜂鸣器输出功能	Selectable	Selectable*2	Selectable	Stop (Undefined)
CPU	Stop (Retained)	Stop (Retained)	Stop (Retained)	Stop (Undefined)
SRAMn (n = 0)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Standby SRAM	Selectable	Stop (Retained)	Selectable	Stop (Retained/Undefined)*8
闪存	Operating	Stop (Retained)	Stop (Retained)	Stop (Retained)

Table 10.2 Operating conditions of each low power mode (2 of 2)

Item	Sleep mode	Software Standby mode	Snooze mode	Deep Software Standby mode
DMA Controller (DMAC)	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
Data Transfer Controller (DTC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Watchdog Timer (WDT)	Selectable*1	Stop (Retained)	Stop (Retained)	Stop (Undefined)
Independent Watchdog Timer (IWDT)	Selectable*1	Selectable*1	Selectable*1	Stop (Undefined)
Asynchronous General Purpose Timer (AGTn (n = 0, 1))	Selectable	Selectable*12	Selectable*12	Stop (Undefined)
12-Bit A/D Converter (ADC)	Selectable	Stop (Retained)	Selectable*13	Stop (Undefined)
Programmable Gain Amplifiers (PGAs)	Selectable*14	Stop (Retained)	Selectable*14	Stop (Undefined)
12-Bit D/A Converter (DAC12)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Data Operation Circuit (DOC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Serial Communications Interface (SCI0)	Selectable	Stop (Retained)	Selectable (RXD0 falling edge is available, to enter snooze mode) (only in asynchronous mode).*5	Stop (Undefined)
Serial Communications Interface (SCIn (n = 1 to 4, 9))	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
I2C Bus Interface (IIC0)	Selectable	Selectable*3	Selectable*3 Only wakeup interrupt is available.	Stop (Undefined)
I2C Bus Interface (IIC1)	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
Event Link Controller (ELC)	Selectable	Stop (Retained)	Selectable*6	Stop (Undefined)
High-Speed Analog Comparator (ACMPHSn, n = 0 to 3)	Selectable	Stop (Retained)	Selectable VCOUT function only.*9	Stop (Undefined)
IRQn (n = 0 to 15) pin interrupt	Selectable	Selectable	Selectable	Stop (Undefined)
NMI, IRQn-DS (n = 0 to 15) pin interrupt	Selectable	Selectable	Selectable	Selectable
Key Interrupt Function (KINT)	Selectable	Selectable	Selectable	Stop (Undefined)
Low voltage detection (LVD)	Selectable	Selectable	Selectable	Selectable*10
Power-on reset circuit	Operating	Operating	Operating	Operating*11
Other peripheral modules	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
I/O Ports	Operating	Retained	Operating	Retained

Note: Selectable means that operating or not operating can be selected by the control registers.
Stop (Retained) means that the contents of the internal registers are retained but the operations are suspended.
Operation prohibited means that the function must be stopped before entering Software Standby mode.
Stop (Undefined) means that the contents of the internal registers are undefined and power to the internal circuit is cut off.
All modules whose module-stop bits are 0 start as soon as PCLKs are supplied after entering Snooze mode. In order to avoid increase in power consumption in Snooze mode, module-stop bit of modules which are unnecessary in Snooze mode must be set to 1 before entering Software Standby mode.

Note 1. In IWDT-dedicated on-chip oscillator and IWDT, operating or stopping is selected by setting the IWDT Stop Control bit (IWDTSTPCTL) in Option Function Select register 0 (OFS0) in IWDT auto start mode. In WDT, operating or stopping is selected by setting the WDT Stop Control bit (WDTSTPCTL) in Option Function Select Register 0 (OFS0) in WDT auto start mode.Power consumption can be reduced in Normal and Sleep modes by selecting an appropriate operating power control mode according to the operating frequency.

Note 2. Stopped when the clock output source select bits (CKOCR.CKOSEL[2:0]) are set to a value other than 010b (LOCO).

Note 3. IIC0 wakeup interrupt is available.

Note 4. When using SCI0 in Snooze mode, MOSCCR.MOSTP and PLLCR.PLLSTP and PLL2CR.PLL2STP bits must be 1.

Note 5. Serial communication modes of SCI0 is only in asynchronous mode.

Note 6. Event lists the restrictions described in section 10.10.13. ELC Events in Snooze Mode.

Note 7. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, the oscillator status is the same as before entering Deep Software Standby mode. When the DPSBYCR.DEEPCUT[1:0] bits are not 00b, the oscillator stops when the MCU enters Deep Software Standby mode.

Note 8. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, data in the Standby SRAM is retained in Deep Software Standby mode. When the DPSBYCR.DEEPCUT[1:0] bits are not 00b, data in the Standby SRAM is undefined in Deep Software Standby mode.

Table 10.2 每种低功耗模式的操作条件（2个中的2个）

Item	睡眠模式	软件待机模式	贪睡模式	深度软件待机模式
DMA Controller (DMAC)	Selectable	Stop (Retained)	禁止操作	Stop (Undefined)
数据传输控制器(DTC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
看门狗定时器(WDT)	Selectable*1	Stop (Retained)	Stop (Retained)	Stop (Undefined)
独立看门狗 Timer (IWDT)	Selectable*1	Selectable*1	Selectable*1	Stop (Undefined)
异步通用 Timer (AGTn (n = 0, 1))	Selectable	Selectable*12	Selectable*12	Stop (Undefined)
12-Bit A/D Converter (ADC)	Selectable	Stop (Retained)	Selectable*13	Stop (Undefined)
可编程增益放大器(PGA)	Selectable*14	Stop (Retained)	Selectable*14	Stop (Undefined)
12-Bit D/A Converter (DAC12)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
数据运算电路(DOC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
串行通信接口(SCI0)	Selectable	Stop (Retained)	可选（RXD0下降沿可用，进入贪睡模式）（仅在异步模式下）。*5	Stop (Undefined)
串行通信接口(SCIn(n=1to4 9))	Selectable	Stop (Retained)	禁止操作	Stop (Undefined)
I2C总线接口(IIC0)	Selectable	Selectable*3	Selectable*3 只有唤醒中断可用。	Stop (Undefined)
I2C总线接口(IIC1)	Selectable	Stop (Retained)	禁止操作	Stop (Undefined)
事件链接控制器(ELC)	Selectable	Stop (Retained)	Selectable*6	Stop (Undefined)
高速模拟比较器（ACMPHSn，n =0至3）	Selectable	Stop (Retained)	Selectable 仅VCOUT功能。*9	Stop (Undefined)
IRQn(n=0to15)引脚中断	Selectable	Selectable	Selectable	Stop (Undefined)
NMI IRQn-DS(n=0to15)引脚中断	Selectable	Selectable	Selectable	Selectable
按键中断功能(KINT)	Selectable	Selectable	Selectable	Stop (Undefined)
低电压检测(LVD)	Selectable	Selectable	Selectable	Selectable*10
上电复位电路	Operating	Operating	Operating	Operating*11
其他外围模块	Selectable	Stop (Retained)	禁止操作	Stop (Undefined)
I/O Ports	Operating	Retained	Operating	Retained

Note: 可选择的意思是可以通过控制寄存器来选择操作或不操作。
停止（Retained）表示内部寄存器的内容被保留但操作被暂停。
禁止操作意味着在进入软件待机模式之前必须停止该功能。
停止（未定义）表示内部寄存器的内容未定义，内部电路的电源被切断。
进入贪睡模式后，一旦提供PCLK，所有模块停止位为0的模块都会启动。为了避免贪睡模式下的功耗增加，在进入软件待机模式之前，必须将在贪睡模式下不需要的模块的模块停止位设置为1。

注1.在IWDT专用内部振荡器和IWDT中，通过设置IWDT停止控制位来选择操作或停止
(IWDTSTPCTL)在IWDT自动启动模式下选项功能选择寄存器0(OFS0)。在WDT中，通过在WDT自动启动模式下设置选项功能选择寄存器0(OFS0)中的WDT停止控制位(WDTSTPCTL)来选择操作或停止。通过选择适当的操作功率控制，可以在正常和睡眠模式下降低功耗模式根据工作频率。

注2.当时钟输出源选择位(CKOCR.CKOSEL[2:0])设置为010b(LOCO)以外的值时停止。
注3.IIC0唤醒中断可用。
注4.在贪睡模式下使用SCI0时，MOSCCR.MOSTP和PLLCR.PLLSTP和PLL2CR.PLL2STP位必须为1。
注5.SCI0的串行通信模式仅在异步模式下。
注6.事件列出了10.10.13节中描述的限制。贪睡模式下的ELC事件。
注7.如果DPSBYCR.DEEPCUT[1:0]位为00b，则振荡器状态与进入深度软件待机模式前相同。
当DPSBYCR.DEEPCUT[1:0]位不为00b时，当MCU进入深度软件待机模式时振荡器停止。
注8.如果DPSBYCR.DEEPCUT[1:0]位为00b，则待机SRAM中的数据在深度软件待机模式下保留。当。。。的时候
DPSBYCR.DEEPCUT[1:0]位不是00b，在深度软件待机模式下，待机SRAM中的数据未定义。

Note 9. Only VCOUT function is permitted. The VCOUT pin operates when ACMPHS uses no digital filter. For details on digital filter, see section 39, High-Speed Analog Comparator (ACMPHS).
Note 10. When using LVD in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] bits must be 00b or 01b before entering Deep Software Standby mode.
Note 11. When the MCU enters Deep Software Standby mode with the DPSBYCR.DEEPCUT[1:0] bits set to 11b, the LVD circuit stops and the low-power function of the power-on reset circuit is enabled.
Note 12. AGT0 operation is possible when 100b (AGTLCLK) is selected by the AGT0.AGTMR1.TCK[2:0] bits. AGT1 operation is possible when 100b (AGTLCLK) or 101 (Underflow event signal from AGT0) is selected by the AGT1.AGTMR1.TCK[2:0] bits.
Note 13. When using the 12-bit A/D Converter in Snooze mode, the ADCMPENR.CMPENn bits must be 1. (The precautions for using the 12-Bit A/D Converter in snooze mode are determined after evaluation.)
Note 14. When using the Programmable Gain Amplifiers, MSTPD16 must be set to 0. For details, see section 36.3.13. Programmable Gain Amplifier. (The precautions for using the PGAs are determined after evaluation.)

Table 10.3 Interrupt Source for canceling Snooze, Software Standby and Deep Software Standby Modes

Interrupt source	Name	Software Standby Mode	Snooze Mode	Deep Software Standby Mode
NMI		Yes	Yes	Yes
Port	PORT_IRQn (n = 0 to 15)	Yes	Yes	Yes*3
LVD	LVD_LVD1	Yes	Yes	Yes
	LVD_LVD2	Yes	Yes	Yes
IWDT	IWDT_NMIUNDF	Yes	Yes	No
KINT	KEY_INTKR	Yes	Yes	No
AGT1	AGT1_AGTI	Yes	Yes*2	No
	AGT1_AGTCMAI	Yes	Yes	No
	AGT1_AGTCMBI	Yes	Yes	No
IIC0	IIC0_WU	Yes	Yes	No
ADC	ADC_CCMPM0	No	Yes with SELSR0*1 *2	No
	ADC_CCMPM1	No	Yes with SELSR0*1 *2	No
SCI0	SCI0_AM	No	Yes with SELSR0*1	No
DTC	DTC_COMPLETE	No	Yes with SELSR0*1 *2	No
DOC	DOC_DOPCI	No	Yes with SELSR0 *1	No

Note 1. To use the interrupt request as a trigger for exiting the Snooze mode, the request must be selected in SELSR0 . See section 12, Interrupt Controller Unit (ICU) for the setting of SELSR0. When a trigger selected in SELSR0 occurs after executing WFI instruction and during the transition from Normal mode to Software Standby mode, the request might or might not be accepted, depending on the timing of the occurrence.
Note 2. The event which is enabled by the SNZEDCR0 must not be used.
Note 3. IRQn-DS pin interrupt is available. IRQn pin interrupt is not available.

注9.仅允许使用VCOUT功能。当ACMPHS不使用数字滤波器时，VCOUT引脚工作。有关数字滤波器的详细信息，请参阅第39节，高速模拟比较器(ACMPHS)。
注10.在深度软件待机模式下使用LVD时，DPSBYCR.DEEPCUT[1:0]位在进入深度之前必须为00b或01b软件待机模式。
注11.当MCU进入深度软件待机模式且DPSBYCR.DEEPCUT[1:0]位设置为11b时，LVD电路停止并启用上电复位电路的低功耗功能。

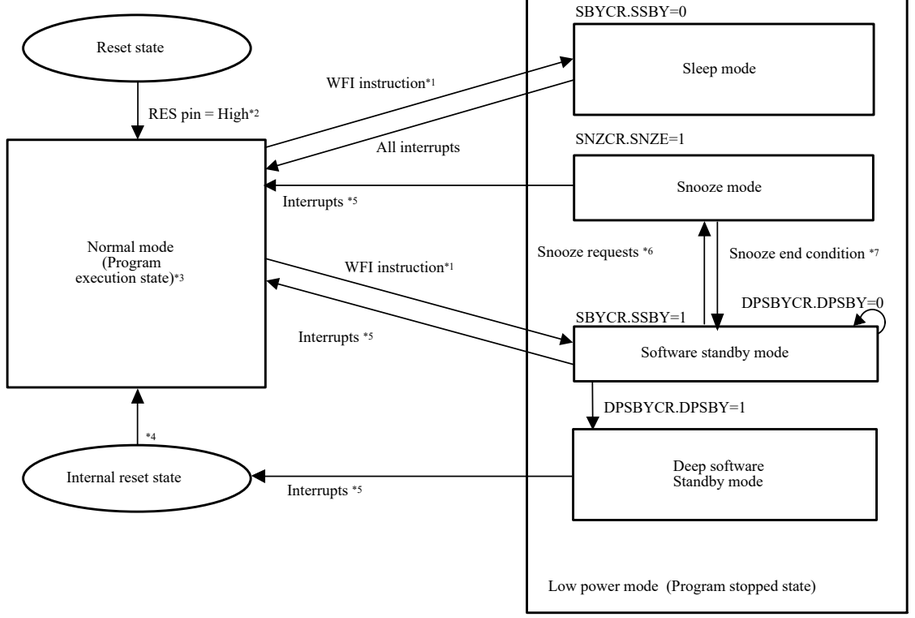
注12.当AGT0.AGTMR1.TCK[2:0]位选择100b(AGTLCLK)时，可以进行AGT0操作。当AGT1.AGTMR1.TCK[2:0]位选择100b（AGTLCLK）或101（来自AGT0的下溢事件信号）时，可以进行AGT1操作。
注13.在贪睡模式下使用12位AD转换器时，ADCMPENR.CMPENn位必须为1。（使用12位AD转换器的注意事项打盹模式下的位AD转换器在评估后确定。）
注14.使用可编程增益放大器时，MSTPD16必须设置为0。有关详细信息，请参阅第36.3.13节。可编程增益放大器。（使用PGA的注意事项在评估后确定。）

Table 10.3 用于取消贪睡、软件待机和深度软件待机模式的中断源

中断源	Name	软件待机模式	贪睡模式	深度软件待机模式
NMI		Yes	Yes	Yes
Port	PORT_IRQn (n = 0 to 15)	Yes	Yes	Yes*3
LVD	LVD_LVD1	Yes	Yes	Yes
	LVD_LVD2	Yes	Yes	Yes
IWDT	IWDT_NMIUNDF	Yes	Yes	No
KINT	KEY_INTKR	Yes	Yes	No
AGT1	AGT1_AGTI	Yes	Yes*2	No
	AGT1_AGTCMAI	Yes	Yes	No
	AGT1_AGTCMBI	Yes	Yes	No
IIC0	IIC0_WU	Yes	Yes	No
ADC	ADC_CCMPM0	No	是SELSR0*1*2	No
	ADC_CCMPM1	No	是SELSR0*1*2	No
SCI0	SCI0_AM	No	是SELSR0*1	No
DTC	DTC_COMPLETE	No	是SELSR0*1*2	No
DOC	DOC_DOPCI	No	是SELSR0*1	No

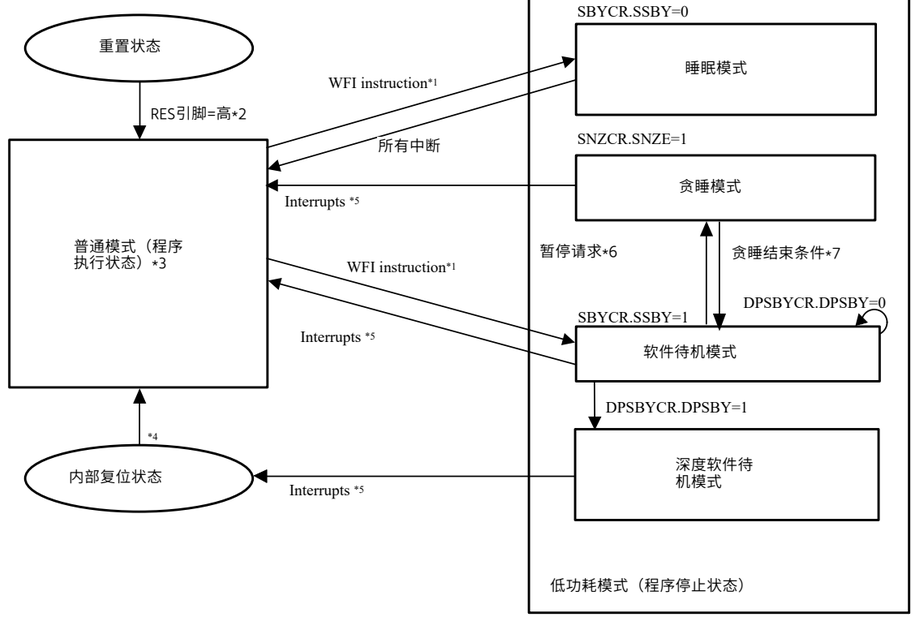
注1.要将中断请求用作退出贪睡模式的触发器，必须在SELSR0中选择该请求。见第12节，用于设置SELSR0的中断控制器单元(ICU)。当SELSR0中选择的触发发生在执行WFI指令之后以及从正常模式到软件待机模式的转换期间，请求可能会或可能不会被接受，具体取决于发生的时间。

注2.不得使用由SNZEDCR0启用的事件。
注3.IRQn-DS引脚中断可用。IRQn引脚中断不可用。



Note 1. When an interrupt that acts as a trigger for cancel is received during a transition to the program-stopped state after the execution of a WFI instruction, the MCU executes interrupt exception handling instead of transitioning to low power mode.
Note 2. The MOCO clock is the source of the operating clock following a transition from the reset state to Normal mode.
Note 3. The transition to Normal mode is made because of an interrupt from Sleep mode, Snooze mode, or Software Standby mode. The clock source is the same as before entering the low power mode.
Note 4. When an available interrupt request is generated, an internal reset (Deep Software Standby reset) is generated over a fixed period. Canceling of Deep Software Standby mode accompanies release from the internal reset state, and then the MCU transitions to Normal mode and executes reset exception processing with the MOCO clock as the source of the operating clock.
Note 5. See Table 10.3
Note 6. See Table 10.7
Note 7. See Table 10.9

Figure 10.1 Mode Transitions



注1.在WFI指令执行后转换到程序停止状态期间，如果接收到用作取消触发的中断，MCU将执行中断异常处理，而不是转换到低功耗模式。

注2.MOCO时钟是从复位状态转换到正常模式后的工作时钟源。
注3.由于休眠模式、贪睡模式或软件待机模式的中断，会转换到正常模式。时钟源与进入低功耗模式前相同。

注4.当产生可用中断请求时，会在固定周期内产生内部复位（深度软件待机复位）。深度软件待机模式的取消伴随着内部复位状态的释放，然后MCU转换到正常模式并以MOCO时钟作为工作时钟源执行复位异常处理。

注5.见表10.3注6.见表10
.7注7.见表10.9

Figure 10.1 模式转换

10.2 Register Descriptions

10.2.1 LPMSAR : Low Power Mode Security Attribution Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3C8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	NONSEC9	NONSEC8	—	—	—	NONSEC4	—	NONSEC2	—	NONSEC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0*1	Non Secure Attribute bit 0 Target register: OPCCR 0: Secure 1: Non Secure	R/W
1	—	This bit is read as 1. The write value should be 1.	R/W
2	NONSEC2	Non Secure Attribute bit 2 Target register: SBYCR 0: Secure 1: Non Secure	R/W
3	—	This bit is read as 1. The write value should be 1.	R/W
4	NONSEC4	Non Secure Attribute bit 4 Target register: SNZCR, SNZEDCR0, SNZREQCR0 0: Secure 1: Non Secure	R/W
7:5	—	These bits are read as 1. The write value should be 1.	R/W
8	NONSEC8	Non Secure Attribute bit 8 Target register: DPSBYCR 0: Secure 1: Non Secure	R/W
9	NONSEC9	Non Secure Attribute bit 9 Target register: DPSWCR 0: Secure 1: Non Secure	R/W
31:10	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

Note 1. It is recommended that these bits are configured as Non Secure when the device life cycle is NSECSD (DLMMON.DLMMON[3:0]=0011b). See section 45.6.1. Restrictions on setting the security attribution for the details.

The LPMSAR register controls the secure attribute of Low Power Mode registers.

NONSEC0 bit (Non Secure Attribute bit 0)

This bit controls the security attribute of OPCCR.

NONSEC2 bit (Non Secure Attribute bit 2)

This bit controls the security attribute of SBYCR.

NONSEC4 bit (Non Secure Attribute bit 4)

This bit controls the security attribute of SNZCR, SNZEDCR0, SNZREQCR0

10.2 注册说明

10.2.1 LPMSAR：低功耗模式安全属性寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x3C8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	NONSEC9	NONSEC8	—	—	—	NONSEC4	—	NONSEC2	—	NONSEC0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0*1	非安全属性位0 Target register: OPCCR 0：安全1：不安全	R/W
1	—	该位读取为1。写入值应为1。	R/W
2	NONSEC2	非安全属性位2 Target register: SBYCR 0：安全1：不安全	R/W
3	—	该位读取为1。写入值应为1。	R/W
4	NONSEC4	非安全属性位4 Target register: SNZCR, SNZEDCR0, SNZREQCR0 0：安全1：不安全	R/W
7:5	—	这些位被读取为1。写入值应为1。	R/W
8	NONSEC8	非安全属性位8目标寄存器：DPSBYCR 0：安全1：不安全	R/W
9	NONSEC9	非安全属性位9目标寄存器：DPSWCR 0：安全1：不安全	R/W
31:10	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

注1.当设备生命周期为NSECSD时，建议将这些位配置为非安全(DLMMON.DLMMON[3:0]=0011b)。请参见第45.6.1节。设置详细信息的安全属性的限制。

LPMSAR寄存器控制低功耗模式寄存器的安全属性。

NONSEC0位（非安全属性位0）

该位控制OPCCR的安全属性。

NONSEC2位（非安全属性位2）

该位控制SBYCR的安全属性。

NONSEC4位（非安全属性位4）

该位控制SNZCR、SNZEDCR0、SNZREQCR0的安全属性

NONSEC8 bit (Non Secure Attribute bit 8)

This bit controls the security attribute of DPSBYCR.

NONSEC9 bit (Non Secure Attribute bit 9)

This bit controls the security attribute of DPSWCR.

10.2.2 DPFSAR : Deep Standby Interrupt Factor Security Attribution Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3E0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DPFSA20	—	—	DPFSA17	DPFSA16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DPFSA15	DPFSA14	DPFSA13	DPFSA12	DPFSA11	DPFSA10	DPFSA9	DPFSA8	DPFSA7	DPFSA6	DPFSA5	DPFSA4	DPFSA3	DPFSA2	DPFSA1	DPFSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	DPFSA0 to DPFSA7	Deep Standby Interrupt Factor Security Attribute bit n (n = 0 to 7) Target register: DPSIER0.bn, DPSIFR0.bn, DPSIEGR0.bn (n = 0 to 7) Target factor : IRQn-DS Pin (n = 0 to 7) 0: Secure 1: Non Secure	R/W
15:8	DPFSA8 to DPFSA15	Deep Standby Interrupt Factor Security Attribute bit n (n = 8 to 15) Target register: DPSIER1.bn, DPSIFR1.bn, DPSIEGR1.bn (n = 0 to 7) Target factor : IRQn-DS Pin (n = 8 to 15) 0: Secure 1: Non Secure	R/W
16	DPFSA16	Deep Standby Interrupt Factor Security Attribute bit 16 Target register: DPSIER2.b0, DPSIFR2.b0, DPSIEGR2.b0 Target factor : LVD1 0: Secure 1: Non Secure	R/W
17	DPFSA17	Deep Standby Interrupt Factor Security Attribute bit 17 Target register: DPSIER2.b1, DPSIFR2.b1, DPSIEGR2.b1 Target factor : LVD2 0: Secure 1: Non Secure	R/W
19:18	—	These bits are read as 1. The write value should be 1.	R/W
20	DPFSA20	Deep Standby Interrupt Factor Security Attribute bit 20 Target register: DPSIER2.b4, DPSIFR2.b4, DPSIEGR2.b4 Target factor : NMI Pin 0: Secure 1: Non Secure	R/W
31:21	—	These bits are read as 1. The write value should be 1.	R/W

The DPFSAR register controls the secure attribute of Deep Standby Interrupt Factor control registers.

DPFSA bit (Deep Standby Interrupt Factor Security Attribute bit n (n = 0 to 7))

This bit controls the security attribute of DPSIER0.bn, DPSIFR0.bn, DPSIEGR0.bn (n = 0 to 7) .

Target factor is IRQn-DS Pin (n = 0 to 7).

DPFSA bit (Deep Standby Interrupt Factor Security Attribute bit n (n = 8 to 15))

This bit controls the security attribute of DPSIER1.bn, DPSIFR1.bn, DPSIEGR1.bn (n = 0 to 7) .

NONSEC8位（非安全属性位8）

该位控制DPSBYCR的安全属性。

NONSEC9位（非安全属性位9）

该位控制DPSWCR的安全属性。

10.2.2 DPFSAR：深度待机中断因素安全属性寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x3E0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DPFSA20	—	—	DPFSA17	DPFSA16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DPFSA15	DPFSA14	DPFSA13	DPFSA12	DPFSA11	DPFSA10	DPFSA9	DPFSA8	DPFSA7	DPFSA6	DPFSA5	DPFSA4	DPFSA3	DPFSA2	DPFSA1	DPFSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	DPFSA0 to DPFSA7	深度待机中断因素安全属性位n（n=0到7） 目标寄存器：DPSIER0.bn、DPSIFR0.bn、DPSIEGR0.bn（n=0到7） 目标因素：IRQn-DS引脚（n=0至7） 0：安全1：不安全	R/W
15:8	DPFSA8 to DPFSA15	深度待机中断因素安全属性位n（n=8到15） 目标寄存器：DPSIER1.bn、DPSIFR1.bn、DPSIEGR1.bn（n=0到7） 目标因素：IRQn-DS引脚（n=8至15） 0：安全1：不安全	R/W
16	DPFSA16	深度待机中断因素安全属性位16 Target register: DPSIER2.b0, DPSIFR2.b0, DPSIEGR2.b0 目标因素：LVD1 0：安全1：不安全	R/W
17	DPFSA17	深度待机中断因素安全属性位17 Target register: DPSIER2.b1, DPSIFR2.b1, DPSIEGR2.b1 目标因素：LVD2 0：安全1：不安全	R/W
19:18	—	这些位被读取为1。写入值应为1。	R/W
20	DPFSA20	深度待机中断因素安全属性位20 Target register: DPSIER2.b4, DPSIFR2.b4, DPSIEGR2.b4 目标因素:NMIPin 0：安全1：不安全	R/W
31:21	—	这些位被读取为1。写入值应为1。	R/W

DPFSAR寄存器控制深度待机中断因子控制寄存器的安全属性。

DPFSA位（深度待机中断因素安全属性位n（n=0至7））

该位控制DPSIER0.bn DPSIFR0.bn DPSIEGR0.bn(n=0to7)的安全属性。

目标因子是IRQn-DS引脚（n=0到7）。

DPFSA位（深度待机中断因素安全属性位n（n=8至15））

该位控制DPSIER1.bn DPSIFR1.bn DPSIEGR1.bn(n=0to7)的安全属性。

Target factor is IRQn-DS Pin (n = 8 to 15)

DPFSA16 bit (Deep Standby Interrupt Factor Security Attribute bit 16)

This bit controls the security attribute of DPSIER2.b0, DPSIFR2.b0, DPSIEGR2.b0 .

Target factor is LVD1.

DPFSA17 bits (Deep Standby Interrupt Factor Security Attribute bit 17)

This bit controls the security attribute of DPSIER2.b1, DPSIFR2.b1, DPSIEGR2.b1.

Target factor is LVD2.

DPFSA20 bit (Deep Standby Interrupt Factor Security Attribute bit 20)

This bit controls the security attribute of DPSIER2.b4, DPSIFR2.b4, DPSIEGR2.b4.

Target factor is NMI Pin.

10.2.3 SBYCR : Standby Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x00C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSBY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	These bits are read as reset value.The write value should be reset value	R/W
15	SSBY	Software Standby Mode Select 0: Sleep mode 1: Software Standby mode.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

SSBY bit (Software Standby Mode Select)

The SSBY bit specifies the transition destination after a WFI instruction is executed.

When the SSBY bit is set to 1, the MCU enters Software Standby mode after execution of a WFI instruction. When the MCU returns to Normal mode from Software Standby mode by an interrupt, the SSBY bit remains 1. The SSBY bit can be cleared by writing 0 to it.

While the OSTDCR.OSTDE bit is 1, setting of the SSBY bit is ignored. Even if SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.

While the FENTRYR.FENTRYC bit is 1 setting of the SSBY bit is ignored. Even if SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.

While the FENTRYR.FENTRYD bit is 1 setting of the SSBY bit is ignored. Even if SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.

目标因子是IRQn-DS引脚（n=8到15）

DPFSA16位（深度待机中断因素安全属性位16）

该位控制DPSIER2.b0、DPSIFR2.b0、DPSIEGR2.b0的安全属性。

目标因子是LVD1。

DPFSA17位（深度待机中断因素安全属性位17）

该位控制DPSIER2.b1、DPSIFR2.b1、DPSIEGR2.b1的安全属性。

目标因子是LVD2。

DPFSA20位（深度待机中断因素安全属性位20）

该位控制DPSIER2.b4、DPSIFR2.b4、DPSIEGR2.b4的安全属性。

目标因素是NMI引脚。

10.2.3 SBYCR：待机控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x00C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSBY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	这些位被读取为复位值。写入值应为复位值	R/W
15	SSBY	软件待机模式选择 0：休眠模式1：软件待机模式。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

SSBY位（软件待机模式选择）

SSBY位指定执行WFI指令后的转移目标。

当SSBY位设置为1时，MCU在执行WFI指令后进入软件待机模式。当。。。的时候
MCU通过中断从软件待机模式返回到正常模式，SSBY位保持为1。SSBY位可以通过向其写入0来清除。

当OSTDCR.OSTDE位为1时，忽略SSBY位的设置。即使SSBY位为1，MCU也会在执行WFI指令时进入休眠模式。

当FENTRYR.FENTRYC位为1时，SSBY位的设置被忽略。即使SSBY位为1，MCU也会在执行WFI指令时进入休眠模式。

当FENTRYR.FENTRYD位为1时，SSBY位的设置被忽略。即使SSBY位为1，MCU也会在执行WFI指令时进入休眠模式。

10.2.4 MSTPCRA : Module Stop Control Register A

Base address: MSTP = 0x4008_4000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	MSTPA22	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	MSTPA7	—	—	—	—	—	—	MSTPA0
Value after reset:	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	MSTPA0	SRAM0 Module Stop Target module: SRAM0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
6:1	—	These bits are read as 1. The write value should be 1.	R/W
7	MSTPA7	Standby SRAM Module Stop Target module: Standby SRAM 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
21:8	—	These bits are read as 1. The write value should be 1.	R/W
22	MSTPA22	DMA Controller/Data Transfer Controller Module Stop*1 Target module: DTC, DMAC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
31:23	—	These bits are read as 1. The write value should be 1.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. When rewriting the MSTPA22 bit from 0 to 1, disable the DMAC and DTC before setting the MSTPA22 bit.

10.2.5 MSTPCRB : Module Stop Control Register B

Base address: MSTP = 0x4008_4000

Offset address: 0x004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPB31	MSTPB30	MSTPB29	MSTPB28	MSTPB27	—	—	—	—	MSTPB22	—	—	MSTPB19	MSTPB18	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MSTPB9	MSTPB8	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	—	This bit is read as 1. The write value should be 1.	R/W

10.2.4 MSTPCRA:模块停止控制寄存器A

Base address: MSTP = 0x4008_4000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	MSTPA22	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	MSTPA7	—	—	—	—	—	—	MSTPA0
重置后的值:	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	MSTPA0	SRAM0模块停止 Target module: SRAM0 0：取消模块停止状态1：进入模块停止状态	R/W
6:1	—	这些位被读取为1。写入值应为1。	R/W
7	MSTPA7	待机SRAM模块停止 目标模块：备用SRAM 0：取消模块停止状态1：进入模块停止状态	R/W
21:8	—	这些位被读取为1。写入值应为1。	R/W
22	MSTPA22	DMA控制器数据传输控制器模块停止*1 Target module: DTC, DMAC 0：取消模块停止状态1：进入模块停止状态	R/W
31:23	—	这些位被读取为1。写入值应为1。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.将MSTPA22位从0改写为1时，在设置MSTPA22位之前禁用DMAC和DTC。

10.2.5 MSTPCRB:模块停止控制寄存器B

Base address: MSTP = 0x4008_4000

Offset address: 0x004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPB31	MSTPB30	MSTPB29	MSTPB28	MSTPB27	—	—	—	—	MSTPB22	—	—	MSTPB19	MSTPB18	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MSTPB9	MSTPB8	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	—	该位读取为1。写入值应为1。	R/W

Bit	Symbol	Function	R/W
8	MSTPB8	I²C Bus Interface 1 Module Stop*1 Target module: IIC1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
9	MSTPB9	I²C Bus Interface 0 Module Stop*1 Target module: IIC0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
17:10	—	These bits are read as 1. The write value should be 1.	R/W
18	MSTPB18	Serial Peripheral Interface 1 Module Stop*2 Target module: SPI1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
19	MSTPB19	Serial Peripheral Interface 0 Module Stop*2 Target module: SPI0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
21:20	—	These bits are read as 1. The write value should be 1.	R/W
22	MSTPB22	Serial Communication Interface 9 Module Stop*2 Target module: SCI9 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
26:23	—	These bits are read as 1. The write value should be 1.	R/W
27	MSTPB27	Serial Communication Interface 4 Module Stop*2 Target module: SCI4 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
28	MSTPB28	Serial Communication Interface 3 Module Stop*2 Target module: SCI3 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
29	MSTPB29	Serial Communication Interface 2 Module Stop*2 Target module: SCI2 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
30	MSTPB30	Serial Communication Interface 1 Module Stop*2 Target module: SCI1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
31	MSTPB31	Serial Communication Interface 0 Module Stop*2 Target module: SCI0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The MSTPBi bit must be written while the oscillation of the clock controlled by this bit is stabilized. For entering Software Standby mode after writing the MSTPBi bit, wait for two IICCLK cycles after writing, and then execute a WFI instruction (i = 8, 9).

Note 2. The MSTPBi bit must be written while the oscillation of the clock controlled by this bit is stabilized. For entering Software Standby mode after writing the MSTPBi bit, wait for two SCISPICLK cycles after writing, and then execute a WFI instruction (i = 18, 19, 22, and 27 to 31).

Bit	Symbol	Function	R/W
8	MSTPB8	I2C总线接口1模块停止*1 Target module: IIC1 0：取消模块停止状态1：进入模块停止状态	R/W
9	MSTPB9	I2C总线接口0模块停止*1 Target module: IIC0 0：取消模块停止状态1：进入模块停止状态	R/W
17:10	—	这些位被读取为1。写入值应为1。	R/W
18	MSTPB18	串行外设接口1模块停止*2 Target module: SPI1 0：取消模块停止状态1：进入模块停止状态	R/W
19	MSTPB19	串行外设接口0模块停止*2 Target module: SPI0 0：取消模块停止状态1：进入模块停止状态	R/W
21:20	—	这些位被读取为1。写入值应为1。	R/W
22	MSTPB22	串行通讯接口9模块停止*2 Target module: SCI9 0：取消模块停止状态1：进入模块停止状态	R/W
26:23	—	这些位被读取为1。写入值应为1。	R/W
27	MSTPB27	串行通讯接口4模块停止*2 Target module: SCI4 0：取消模块停止状态1：进入模块停止状态	R/W
28	MSTPB28	串行通讯接口3模块停止*2 Target module: SCI3 0：取消模块停止状态1：进入模块停止状态	R/W
29	MSTPB29	串行通讯接口2模块停止*2 Target module: SCI2 0：取消模块停止状态1：进入模块停止状态	R/W
30	MSTPB30	串行通讯接口1模块停止*2 Target module: SCI1 0：取消模块停止状态1：进入模块停止状态	R/W
31	MSTPB31	串行通讯接口0模块停止*2 Target module: SCI0 0：取消模块停止状态1：进入模块停止状态	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.MSTPBi位必须在由该位控制的时钟振荡稳定时写入。要在写入MSTPBi位后进入软件待机模式，写入后等待两个IICCLK周期，然后执行WFI指令（i=8 9）。

注2.MSTPBi位必须在由该位控制的时钟振荡稳定时写入。要在写入MSTPBi位后进入软件待机模式，写入后等待两个SCISPICLK周期，然后执行WFI指令（i=18、19、22和27到31）。

10.2.6 MSTPCRC : Module Stop Control Register C

Base address: MSTP = 0x4008_4000

Offset address: 0x008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPC31	—	—	—	MSTPC27	—	—	—	—	—	MSTPC21	MSTPC20	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MSTPC14	MSTPC13	—	—	—	—	—	—	—	—	—	—	—	MSTPC1	MSTPC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MSTPC0	Clock Frequency Accuracy Measurement Circuit Module Stop*1 Target module: CAC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
1	MSTPC1	Cyclic Redundancy Check Module Stop Target module: CRC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
12:2	—	These bits are read as 1. The write value should be 1.	R/W
13	MSTPC13	Data Operation Circuit Module Stop Target module: DOC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
14	MSTPC14	Event Link Controller Module Stop Target module: ELC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
19:15	—	These bits are read as 1. The write value should be 1.	R/W
20	MSTPC20	Trigonometric Function Unit Module Stop Target module: TFU 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
21	MSTPC21	IIR Filter Accelerator Module Stop Target module: IIRFA 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
26:22	—	These bits are read as 1. The write value should be 1.	R/W
27	MSTPC27	CANFD Module Stop*2 Target module: CANFD 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
30:28	—	These bits are read as 1. The write value should be 1.	R/W
31	MSTPC31	Secure Cryptographic Engine Module Stop Target module: SCE5 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

10.2.6 MSTPCRC:模块停止控制寄存器C

Base address: MSTP = 0x4008_4000

Offset address: 0x008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPC31	—	—	—	MSTPC27	—	—	—	—	—	MSTPC21	MSTPC20	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MSTPC14	MSTPC13	—	—	—	—	—	—	—	—	—	—	—	MSTPC1	MSTPC0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MSTPC0	时钟频率精度测量电路模块停止*1 目标模块：CAC 0：取消模块停止状态1：进入模块停止状态	R/W
1	MSTPC1	循环冗余校验模块停止 Target module: CRC 0：取消模块停止状态1：进入模块停止状态	R/W
12:2	—	这些位被读取为1。写入值应为1。	R/W
13	MSTPC13	数据运算电路模块停止 目标模块：DOC 0：取消模块停止状态1：进入模块停止状态	R/W
14	MSTPC14	事件链接控制器模块停止 Target module: ELC 0：取消模块停止状态1：进入模块停止状态	R/W
19:15	—	这些位被读取为1。写入值应为1。	R/W
20	MSTPC20	三角函数单元模块停止 Target module: TFU 0：取消模块停止状态1：进入模块停止状态	R/W
21	MSTPC21	IIR滤波器加速器模块停止 Target module: IIRFA 0：取消模块停止状态1：进入模块停止状态	R/W
26:22	—	这些位被读取为1。写入值应为1。	R/W
27	MSTPC27	CANFD模块停止*2 Target module: CANFD 0：取消模块停止状态1：进入模块停止状态	R/W
30:28	—	这些位被读取为1。写入值应为1。	R/W
31	MSTPC31	安全加密引擎模块停止 Target module: SCE5 0：取消模块停止状态1：进入模块停止状态	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note 1. The MSTPC0 bit must be written while the oscillation of the clock to be controlled by this bit is stable. To enter Software Standby mode after writing this bit, wait for 2 cycles of the slowest clock from the clocks output by the oscillators, then execute a WFI instruction.
Note 2. The MSTPC27 bit must be written while the oscillation of the clock controlled by this bit is stabilized. For entering Software Standby mode after writing the MSTPC27 bit, wait for two CANFD clock (CANFDCLK) cycles after writing, and then execute a WFI instruction.

10.2.7 MSTPCRD : Module Stop Control Register D

Base address: MSTP = 0x4008_4000

Offset address: 0x00C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	MSTPD28	MSTPD27	MSTPD26	MSTPD25	—	—	MSTPD22	—	MSTPD20	MSTPD19	—	—	MSTPD16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MSTPD14	MSTPD13	MSTPD12	MSTPD11	—	—	—	—	—	—	—	MSTPD3	MSTPD2	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 1. The write value should be 1.	R/W
2	MSTPD2	Low Power Asynchronous General Purpose Timer 1 Module Stop*1 Target module: AGT1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
3	MSTPD3	Low Power Asynchronous General Purpose Timer 0 Module Stop*2 Target module: AGT0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
10:4	—	These bits are read as 1. The write value should be 1.	R/W
11	MSTPD11	Port Output Enable for GPT 3 Module Stop Target module: POEG3 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
12	MSTPD12	Port Output Enable for GPT 2 Module Stop Target module: POEG2 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
13	MSTPD13	Port Output Enable for GPT 1 Module Stop Target module: POEG1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
14	MSTPD14	Port Output Enable for GPT 0 Module Stop Target module: POEG0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
15	—	This bit is read as 1. The write value should be 1.	R/W
16	MSTPD16	12-bit A/D Converter Module Stop Target module: ADC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
18:17	—	These bits are read as 1. The write value should be 1.	R/W

注1.MSTPC0位必须在该位控制的时钟振荡稳定时写入。要在写入该位后进入软件待机模式，请等待振荡器输出时钟中最慢时钟的2个周期，然后执行WFI指令。

注2.MSTPC27位必须在由该位控制的时钟振荡稳定时写入。写入MSTPC27位后进入软件待机模式，写入后等待两个CANFD时钟（CANFDCLK）周期，然后执行WFI指令。

10.2.7 MSTPCRD:模块停止控制寄存器D

Base address: MSTP = 0x4008_4000

Offset address: 0x00C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	MSTPD28	MSTPD27	MSTPD26	MSTPD25	—	—	MSTPD22	—	MSTPD20	MSTPD19	—	—	MSTPD16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MSTPD14	MSTPD13	MSTPD12	MSTPD11	—	—	—	—	—	—	—	MSTPD3	MSTPD2	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
1:0	—	这些位被读取为1。写入值应为1。	R/W
2	MSTPD2	低功耗异步通用定时器1模块停止*1 Target module: AGT1 0：取消模块停止状态1：进入模块停止状态	R/W
3	MSTPD3	低功耗异步通用定时器0模块停止*2 Target module: AGT0 0：取消模块停止状态1：进入模块停止状态	R/W
10:4	—	这些位被读取为1。写入值应为1。	R/W
11	MSTPD11	GPT3模块停止的端口输出启用 Target module: POEG3 0：取消模块停止状态1：进入模块停止状态	R/W
12	MSTPD12	GPT2模块停止的端口输出启用 Target module: POEG2 0：取消模块停止状态1：进入模块停止状态	R/W
13	MSTPD13	GPT1模块停止的端口输出使能 Target module: POEG1 0：取消模块停止状态1：进入模块停止状态	R/W
14	MSTPD14	GPT0模块停止的端口输出使能 Target module: POEG0 0：取消模块停止状态1：进入模块停止状态	R/W
15	—	该位读取为1。写入值应为1。	R/W
16	MSTPD16	12位模数转换器模块停止目标模块：ADC 0：取消模块停止状态1：进入模块停止状态	R/W
18:17	—	这些位被读取为1。写入值应为1。	R/W

Bit	Symbol	Function	R/W
19	MSTPD19	12-bit D/A Converter 1 Module Stop Target module: DAC121 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
20	MSTPD20	12-bit D/A Converter 0 Module Stop Target module: DAC120 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
21	—	This bit is read as 1. The write value should be 1.	R/W
22	MSTPD22	Temperature Sensor Module Stop Target module: TSN 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
24:23	—	These bits are read as 1. The write value should be 1.	R/W
25	MSTPD25	High-Speed Analog Comparator 3 Module Stop Target module: ACMPHS3 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
26	MSTPD26	High-Speed Analog Comparator 2 Module Stop Target module: ACMPHS2 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
27	MSTPD27	High-Speed Analog Comparator 1 Module Stop Target module: ACMPHS1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
28	MSTPD28	High-Speed Analog Comparator 0 Module Stop Target module: ACMPHS0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
31:29	—	These bits are read as 1. The write value should be 1.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. When the count source is LOCO, AGT1 counting does not stop even if MSTPD2 is set to 1. If the count source is LOCO, this bit must be set to 1 except when accessing the AGT1 registers.

Note 2. When the count source is LOCO, AGT0 counting does not stop even if MSTPD3 is set to 1. If the count source is LOCO, this bit must be set to 1 except when accessing the AGT0 registers.

10.2.8 MSTPCRE : Module Stop Control Register E

Base address: MSTP = 0x4008_4000

Offset address: 0x010

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPE31	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	MSTPE4	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
19	MSTPD19	12位DA转换器1模块停止目标模块 ：DAC121 0：取消模块停止状态1：进入模块停止状态	R/W
20	MSTPD20	12位DA转换器0模块停止目标模块 ：DAC120 0：取消模块停止状态1：进入模块停止状态	R/W
21	—	该位读取为1。写入值应为1。	R/W
22	MSTPD22	温度传感器模块停止 Target module: TSN 0：取消模块停止状态1：进入模块停止状态	R/W
24:23	—	这些位被读取为1。写入值应为1。	R/W
25	MSTPD25	高速模拟比较器3模块停止 Target module: ACMPHS3 0：取消模块停止状态1：进入模块停止状态	R/W
26	MSTPD26	高速模拟比较器2模块停止 Target module: ACMPHS2 0：取消模块停止状态1：进入模块停止状态	R/W
27	MSTPD27	高速模拟比较器1模块停止 Target module: ACMPHS1 0：取消模块停止状态1：进入模块停止状态	R/W
28	MSTPD28	高速模拟比较器0模块停止 Target module: ACMPHS0 0：取消模块停止状态1：进入模块停止状态	R/W
31:29	—	这些位被读取为1。写入值应为1。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.当计数源为LOCO时，即使MSTPD2设置为1，AGT1计数也不会停止。如果计数源为LOCO，则该位必须设置为1，除非访问AGT1寄存器。

注2.当计数源为LOCO时，即使MSTPD3设置为1，AGT0计数也不会停止。如果计数源为LOCO，该位必须设置为1，除非访问AGT0寄存器。

10.2.8 MSPCRE:模块停止控制寄存器E

Base address: MSTP = 0x4008_4000

Offset address: 0x010

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPE31	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	MSTPE4	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 1. The write value should be 1.	R/W
4	MSTPE4	Key Interrupt Function Module Stop Target module: KINT 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
30:5	—	These bits are read as 1. The write value should be 1.	R/W
31	MSTPE31	General PWM Timer and PWM Delay Generation Circuit Module Stop*1 Target module: GPT, PDG 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The MSTPE31 bit must be written while the oscillation of the clock controlled by this bit is stabilized. For entering Software Standby mode after writing the MSTPE31 bit, wait for two GPTCLK cycles after writing, and then execute a WFI instruction.

10.2.9 OPCCR : Operating Power Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0A0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	OPCMTSF	—	—	OPCM[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	OPCM[1:0]	Operating Power Control Mode Select 0 0: High-speed mode 0 1: Setting prohibited 1 0: Setting prohibited 1 1: Low-speed mode	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	OPCMTSF	Operating Power Control Mode Transition Status Flag 0: Transition completed 1: During transition	R
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The OPCCR register is used to reduce power consumption in Normal and Sleep modes by specifying a lower operating frequency. For the procedure to change the operating power control modes, see section 10.5. Function for Lower Operating Power Consumption.

When transitioning from Software Standby mode to Normal or Snooze mode, the settings in the OPCCR.OPCM[1:0] bits are as follows, regardless of their settings before entering Software Standby mode:

- OPCCR.OPCM[1:0] = 00b (High-speed mode)

If Software Standby mode is canceled before the transition to Software Standby completes, the OPCCR.OPCM[1:0] bits retain their settings from before the WFI instruction is executed. If this causes any problem, set the MCU to High-speed mode during the exception handling procedure when canceling Software Standby mode.

Bit	Symbol	Function	R/W
3:0	—	这些位被读取为1。写入值应为1。	R/W
4	MSTPE4	按键中断功能模块停止 Target module: KINT 0：取消模块停止状态1：进入模块停止状态	R/W
30:5	—	这些位被读取为1。写入值应为1。	R/W
31	MSTPE31	通用PWM定时器和PWM延迟发生电路模块停止*1 Target module: GPT, PDG 0：取消模块停止状态1：进入模块停止状态	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.MSTPE31位必须在由该位控制的时钟振荡稳定时写入。要在写入MSTPE31位后进入软件待机模式，写入后等待两个GPTCLK周期，然后执行WFI指令。

10.2.9 OPCCR:工作电源控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0A0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	OPCMTSF	—	—	OPCM[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	OPCM[1:0]	工作电源控制模式选择 00：高速模式01：禁止设定10：禁止设定1 1：低速模式	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	OPCMTSF	工作电源控制模式转换状态标志 0：转换完成1：转换中	R
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

OPCCR寄存器用于通过指定较低的工作频率来降低 正常和休眠模式下的功耗。有关更改运行功率控制模式的步骤，请参阅第10.5节。降低运行功耗的功能。

从软件待机模式转换到正常或贪睡模式时，OPCCR.OPCM[1:0]位的设置如下，无论它们在进入软件待机模式之前的设置如何：

- OPCCR.OPCM[1:0] = 00b (High-speed mode)

如果在转换到软件待机完成之前取消软件待机模式，则OPCCR.OPCM[1:0]位将保留其在执行WFI指令之前的设置。如果这导致任何问题，请在取消软件待机模式时的异常处理过程中将MCU设置为高速模式。

OPCM[1:0] bits (Operating Power Control Mode Select)

The OPCM[1:0] bits select the operating power control mode in Normal and Sleep modes. Table 10.4 shows the relationship between the operating power control modes and the OPCM[1:0] settings.

OPCMTSF flag (Operating Power Control Mode Transition Status Flag)

The OPCMTSF flag indicates the switching control state when the operating power control mode is switched. This flag becomes 1 when the OPCM bit is written, and 0 when mode transition completes. Read this flag and confirm that it is 0 before proceeding.

Table 10.4 Operating power control mode

Operating power control mode	OPCM[1:0] bits	Power consumption
High-speed mode	00b	High
Low-speed mode	11b	Low

For details about the operating frequency range, see section 46, Electrical Characteristics.

Each operating power control mode is described below.

- High-speed mode
  After a reset cancellation, the MCU is activated in this mode.
- Low-speed mode
  The following constraints apply in low-speed mode:
  - Programming and erasure operations for the flash memory are prohibited
  - Using the PLL or PLL2 is prohibited. See section 10.10.1. Register Access

  In this mode, lower power consumption is possible than in High-speed mode when the same operation is performed under the same conditions, such as operating frequency.

10.2.10 SNZCR : Snooze Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x092

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SNZE	—	—	—	—	—	SNZDTCEN	RXDREQEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RXDREQEN	RXD0 Snooze Request Enable 0: Ignore RXD0 falling edge in Software Standby mode 1: Detect RXD0 falling edge in Software Standby mode	R/W
1	SNZDTCEN	DTC Enable in Snooze mode 0: Disable DTC operation 1: Enable DTC operation	R/W
6:2	—	These bits are read as 0. The write value should be 0.	R/W
7	SNZE	Snooze mode Enable 0: Disable Snooze mode 1: Enable Snooze mode	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

OPCM[1:0]位（工作电源控制模式选择）

OPCM[1:0]位选择正常和休眠模式下的工作功率控制模式。表10.4显示了工作功率控制模式和OPCM[1:0]设置之间的关系。

OPCMTSF标志（工作电源控制模式转换状态标志）

OPCMTSF标志指示切换操作功率控制模式时的切换控制状态。该标志在OPCM位被写入时变为1，在模式转换完成时变为0。阅读此标志并确认其为0，然后再继续。

Table 10.4 工作功率控制方式

工作功率控制方式	OPCM[1:0] bits	能量消耗
High-speed mode	00b	High
Low-speed mode	11b	Low

有关工作频率范围的详细信息，请参见第46节，电气特性。

下面描述每种操作功率控制模式。

- High-speed mode
  复位取消后，MCU在此模式下激活。
- Low-speed mode
  以下约束适用于低速模式：

  禁止对闪存进行编程和擦除操作

  禁止使用PLL或PLL2。请参阅第10.10.1节。注册访问

  在这种模式下，如果在相同的条件下（例如工作频率）执行相同的操作，则可能比高速模式下的功耗更低。

10.2.10 SNZCR:贪睡控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x092

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SNZE	—	—	—	—	—	SNZDTCEN	RXDREQEN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RXDREQEN	RXD0贪睡请求启用 0：在软件待机模式下忽略RXD0下降沿1：在软件待机模式下检测RXD0下降沿	R/W
1	SNZDTCEN	在贪睡模式下启用DTC 0：禁用DTC操作1：启用DTC操作	R/W
6:2	—	这些位被读取为0。写入值应为0。	R/W
7	SNZE	贪睡模式启用 0：禁用贪睡模式1：启用贪睡模式	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

RXDREQEN bit (RXD0 Snooze Request Enable)

The RXDREQEN bit specifies whether to detect a falling edge of the RXD0 pin in Software Standby mode. This bit can be used only when SCI0 is operating in asynchronous mode. To detect a falling edge of the RXD0 pin, set this bit before entering Software Standby mode. When this bit is set to 1, a falling edge of the RXD0 pin in Software Standby mode causes the MCU to enter Snooze mode.

SNZDTCEN bit (DTC Enable in Snooze mode)

The SNZDTCEN bit specifies whether to use the DTC and SRAM in Snooze mode. To use the DTC and SRAM in Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, the DTC can be activated by setting IELSRn register.

SNZE bit (Snooze mode Enable)

The SNZE bit specifies whether to enable a transition from Software Standby mode to Snooze mode. To use Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, a trigger as shown in Table 10.7 in Software Standby mode causes the MCU to enter Snooze mode. After the MCU transitions from Software Standby mode or Snooze mode to Normal mode, set 0 to the SNZE bit once then set it before re-entering Software Standby mode. For details, see section 10.8. Snooze Mode.

10.2.11 SNZEDCR0 : Snooze End Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x094

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SCI0UMTED	—	AD1MATED	—	AD0MATED	DTCNZRED	DTCZRED	AGTUNFED
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AGTUNFED	AGT1 Underflow Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
1	DTCZRED	Last DTC Transmission Completion Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
2	DTCNZRED	Not Last DTC Transmission Completion Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
3	AD0MATED	ADC Compare Match 0 Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
4	—	This bit is read as 0. The write value should be 0.	R/W
5	AD1MATED	ADC Compare Match 1 Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	SCI0UMTED	SCI0 Address Mismatch Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

RXDREQEN位（RXD0贪睡请求使能）

RXDREQEN位指定在软件待机模式下是否检测RXD0引脚的下降沿。该位只能在SCI0工作在异步模式时使用。要检测RXD0引脚的下降沿，请在进入软件待机模式之前设置该位。当该位设置为1时，软件待机模式下RXD0引脚的下降沿会导致MCU进入贪睡模式。

SNZDTCEN位（在贪睡模式下启用DTC）

SNZDTCEN位指定是否在贪睡模式下使用DTC和SRAM。要在贪睡模式下使用DTC和SRAM，请在进入软件待机模式之前将此位设置为1。当该位设置为1时，可以通过设置IELSRn寄存器来激活DTC。

SNZE位（贪睡模式启用）

SNZE位指定是否启用从软件待机模式到贪睡模式的转换。要使用贪睡模式，请在进入软件待机模式之前将此位设置为1。当该位设置为1时，软件待机模式下如表10.7所示的触发会导致MCU进入贪睡模式。在MCU从软件待机模式或贪睡模式转换到正常模式后，将SNZE位设置为0一次，然后在重新进入软件待机模式之前将其设置。有关详细信息，请参阅第10.8节。贪睡模式。

10.2.11 SNZEDCR0：贪睡结束控制寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x094

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SCI0UMTED	—	AD1MATED	—	AD0MATED	DTCNZRED	DTCZRED	AGTUNFED
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AGTUNFED	AGT1下溢贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
1	DTCZRED	上次DTC传输完成贪睡结束启用 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
2	DTCNZRED	不是最后一个DTC传输完成贪睡结束启用 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
3	AD0MATED	ADC比较匹配0贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
4	—	该位读取为0。写入值应为0。	R/W
5	AD1MATED	ADC比较匹配1贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	SCI0UMTED	SCI0地址不匹配贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

The SNZEDCR0 register controls the condition of switching from Snooze mode to Software Standby mode. In order to use a trigger shown in Table 10.8 as a condition to switch from Snooze mode to Software Standby mode, the corresponding bitin the SNZEDCR0 register must be set to 1.

The event that is used to return from snooze mode to normal mode as shown in Table 10.3 must not be enabled in the SNZEDCR0 register.

AGTUNFED bit (AGT1 Underflow Snooze End Enable)

The AGTUNFED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AGT1 underflow. For details on the trigger conditions, see section 23, Low Power Asynchronous General Purpose Timer (AGTW).

DTCZRED bit (Last DTC Transmission Completion Snooze End Enable)

The DTCZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on completion of the last DTC transmission, that is, when CRA or CRB registers in the DTC is 0. For details on the trigger conditions, see section 16, Data Transfer Controller (DTC).

DTCNZRED bit (Not Last DTC Transmission Completion Snooze End Enable)

The DTCNZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on completion of each DTC transmission, that is, when CRA or CRB registers in the DTC is not 0. For details on the trigger conditions, see section 16, Data Transfer Controller (DTC).

AD0MATED bit (ADC Compare Match 0 Snooze End Enable)

The AD0MATED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an ADC event when a conversion result matches the expected data. For details on the trigger conditions, see section 36, 12-Bit A/D Converter (ADC).

AD1MATED bit (ADC Compare Match 1 Snooze End Enable)

The AD1MATED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an ADC event when a conversion result matches the expected data. For details on the trigger conditions, see section 36, 12-Bit A/D Converter (ADC).

SCI0UMTED bit (SCI0 Address Mismatch Snooze End Enable)

The SCI0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an SCI0 event when an address received in Software Standby mode does not match the expected data. For details on the trigger conditions, see section 26, Serial Communications Interface (SCI). Only set this bit to 1 when SCI0 operates in asynchronous mode.

10.2.12 SNZREQCR0 : Snooze Request Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x098

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	SNZREQEN30	SNZREQEN29	SNZREQEN28	—	—	—	—	—	—	—	—	—	—	SNZREQEN17	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SNZREQEN15	SNZREQEN14	SNZREQEN13	SNZREQEN12	SNZREQEN11	SNZREQEN10	SNZREQEN9	SNZREQEN8	SNZREQEN7	SNZREQEN6	SNZREQEN5	SNZREQEN4	SNZREQEN3	SNZREQEN2	SNZREQEN1	SNZREQEN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SNZREQEN0	Enable IRQ0 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W

SNZEDCR0寄存器控制从贪睡模式切换到软件待机模式的条件。为了使用表10.8中所示的触发作为从贪睡模式切换到软件待机模式的条件，必须将SNZEDCR0寄存器中的相应位设置为1。

如表10.3所示用于从贪睡模式返回正常模式的事件不得在
SNZEDCR0 register.

AGTUNFED位（AGT1下溢贪睡结束使能）

AGTUNFED位指定是否在AGT1下溢时启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参见第23节，低功耗异步通用定时器(AGTW)。

DTCZRED位（最后一个DTC传输完成贪睡结束使能）

DTCZRED位指定是否在最后一次DTC传输完成时，即当DTC中的CRA或CRB寄存器为0时启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参见第16节，数据传输控制器(DTC)。

DTCNZRED位（非最后一个DTC传输完成贪睡结束使能）

DTCNZRED位指定是否在每次DTC传输完成时启用从贪睡模式到软件待机模式的转换，即当DTC中的CRA或CRB寄存器不为0时。有关触发条件的详细信息，请参见第16节，数据传输控制器(DTC)。

AD0MATED位（ADC比较匹配0贪睡结束使能）

AD0MATED位指定当转换结果与预期数据匹配时，是否在ADC事件上启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参阅第36节，12位AD转换器(ADC)。

AD1MATED位（ADC比较匹配1暂停结束使能）

AD1MATED位指定当转换结果与预期数据匹配时，是否在ADC事件上启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参阅第36节，12位AD转换器(ADC)。

SCI0UMTED位（SCI0地址不匹配贪睡结束使能）

SCI0UMTED位指定当在软件待机模式下接收到的地址与预期数据不匹配时，是否在发生SCI0事件时启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参阅第26节，串行通信接口(SCI)。仅当SCI0在异步模式下工作时将该位设置为1。

10.2.12 SNZREQCR0:贪睡请求控制寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x098

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	SNZREQEN30	SNZREQEN29	SNZREQEN28	—	—	—	—	—	—	—	—	—	—	SNZREQEN17	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SNZREQEN15	SNZREQEN14	SNZREQEN13	SNZREQEN12	SNZREQEN11	SNZREQEN10	SNZREQEN9	SNZREQEN8	SNZREQEN7	SNZREQEN6	SNZREQEN5	SNZREQEN4	SNZREQEN3	SNZREQEN2	SNZREQEN1	SNZREQEN0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SNZREQEN0	启用IRQ0引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W

Bit	Symbol	Function	R/W
1	SNZREQEN1	Enable IRQ1 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
2	SNZREQEN2	Enable IRQ2 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
3	SNZREQEN3	Enable IRQ3 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
4	SNZREQEN4	Enable IRQ4 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
5	SNZREQEN5	Enable IRQ5 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
6	SNZREQEN6	Enable IRQ6 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
7	SNZREQEN7	Enable IRQ7 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
8	SNZREQEN8	Enable IRQ8 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
9	SNZREQEN9	Enable IRQ9 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
10	SNZREQEN10	Enable IRQ10 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
11	SNZREQEN11	Enable IRQ11 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
12	SNZREQEN12	Enable IRQ12 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
13	SNZREQEN13	Enable IRQ13 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
14	SNZREQEN14	Enable IRQ14 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
15	SNZREQEN15	Enable IRQ15 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
16	—	This bit is read as 0. The write value should be 0.	R/W
17	SNZREQEN17	Enable Key Interrupt snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
27:18	—	These bits are read as 0. The write value should be 0.	R/W
28	SNZREQEN28	Enable AGT1 underflow snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W

Bit	Symbol	Function	R/W
1	SNZREQEN1	启用IRQ1引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
2	SNZREQEN2	启用IRQ2引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
3	SNZREQEN3	启用IRQ3引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
4	SNZREQEN4	启用IRQ4引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
5	SNZREQEN5	启用IRQ5引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
6	SNZREQEN6	启用IRQ6引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
7	SNZREQEN7	启用IRQ7引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
8	SNZREQEN8	启用IRQ8引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
9	SNZREQEN9	启用IRQ9引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
10	SNZREQEN10	启用IRQ10引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
11	SNZREQEN11	启用IRQ11引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
12	SNZREQEN12	启用IRQ12引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
13	SNZREQEN13	启用IRQ13引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
14	SNZREQEN14	启用IRQ14引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
15	SNZREQEN15	启用IRQ15引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
16	—	该位读取为0。写入值应为0。	R/W
17	SNZREQEN17	启用按键中断贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
27:18	—	这些位被读取为0。写入值应为0。	R/W
28	SNZREQEN28	启用AGT1下溢暂停请求 0：禁用贪睡请求1：启用贪睡请求	R/W

Bit	Symbol	Function	R/W
29	SNZREQEN29	Enable AGT1 compare match A snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
30	SNZREQEN30	Enable AGT1 compare match B snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The SNZREQCR0 register controls which trigger causes the MCU to switch from Software Standby mode to Snooze mode. If a trigger is selected as a request to cancel Software Standby mode by setting the WUPENn register, see section 12, Interrupt Controller Unit (ICU), the MCU enters Normal mode when the trigger is generated while the associated bit of the SNZREQCR0 is 1. The setting of the WUPENn register always has higher priority than the setting of the SNZREQCR0 register. For details, see section 10.8. Snooze Mode and section 12, Interrupt Controller Unit (ICU).

10.2.13 DPSBYCR : Deep Standby Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x400

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSBY	IOKEEP	—	—	—	—	DEEPCUT[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	DEEPCUT[1:0]	Power-Supply Control 0 0: Power to the standby RAM and Low-speed on-chip oscillator is supplied in Deep Software Standby mode. 0 1: Power to the standby RAM and Low-speed on-chip oscillator is not supplied in Deep Software Standby mode. 1 0: Setting prohibited 1 1: Power to the standby RAM and Low-speed on-chip oscillator is not supplied in Deep Software Standby mode. In addition, LVD is disabled and the low power function in a power-on reset circuit is enabled.	R/W
5:2	—	These bits are read as 0. The write value should be 0.	R/W
6	IOKEEP	I/O Port Rentention 0: When the Deep Software Standby mode is canceled, the I/O ports are in the reset state. 1: When the Deep Software Standby mode is canceled, the I/O ports are in the same state as in the Deep Software Standby mode.	R/W
7	DPSBY	Deep Software Standby 0: Sleep mode (SBYCR.SSBY=0) / Software Standby mode (SBYCR.SSBY=1) 1: Sleep mode (SBYCR.SSBY=0) / Deep Software Standby mode (SBYCR.SSBY=1)	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The DPSBYCR register controls the Deep Software Standby mode.

Bit	Symbol	Function	R/W
29	SNZREQEN29	启用AGT1比较匹配贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
30	SNZREQEN30	启用AGT1比较匹配B贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
31	—	该位读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

SNZREQCR0寄存器控制哪个触发器导致MCU从软件待机模式切换到贪睡模式。如果通过设置WUPENn寄存器选择触发作为取消软件待机模式的请求，请参见第12节，
中断控制器单元（ICU），当触发产生时MCU进入正常模式，而相关位
SNZREQCR0为1。WUPENn寄存器的设置总是比SNZREQCR0寄存器的设置具有更高的优先级。有关详细信息，请参阅第10.8节。贪睡模式和第12节，中断控制器单元(ICU)。

10.2.13 DPSBYCR：深度待机控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x400

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSBY	IOKEEP	—	—	—	—	DEEPCUT[1:0]	
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	DEEPCUT[1:0]	Power-Supply Control 00：在深度软件待机模式下为待机RAM和低速片上振荡器供电。 01：在深度软件待机模式下不为待机RAM和低速片上振荡器供电。 10：禁止设置11：在深度软件待机模式下不为待机RAM和低速片上振荡器供电。此外，LVD被禁用，上电复位电路中的低功耗功能被启用。	R/W
5:2	—	这些位被读取为0。写入值应为0。	R/W
6	IOKEEP	I/O Port Rentention 0：取消深度软件待机模式时，IO口处于复位状态。 1：当深度软件待机模式取消时，IO端口处于与深度软件待机模式相同的状态。	R/W
7	DPSBY	深度软件待机 0：休眠模式（SBYCR.SSBY=0）软件待机模式(SBYCR.SSBY=1) 1：休眠模式（SBYCR.SSBY=0）深度软件待机模式(SBYCR.SSBY=1)	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DPSBYCR寄存器控制深度软件待机模式。

DPSBYCR is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode. For details, see section 5, Resets.

DEEPCUT[1:0] bit (Power-Supply Control)

The DEEPCUT[1:0] bits control the internal power supply to the standby RAM and Low-speed on-chip oscillator in Deep Software Standby mode. In addition, these bits control the state of LVD and power-on reset circuit in Deep Software Standby mode.

When an LVD interrupt is used in Deep Software Standby mode, the DEEPCUT[1:0] bits must be set to 00b or 01b.

For lower power consumption, set the DEEPCUT[1:0] bits to 11b so that the LVD is stopped and the low power consumption function of the power-on reset circuit is enabled.

Regardless of the DEEPCUT [1: 0] bit setting, during deep software standby mode, internal power supply to SRAM other than standby SRAM is stopped.

When a deep standby mode is used, set DPSWCR.WTSTS bits depending on the value of DEEPCUT[1] before entering Deep Software Standby mode.

IOKEEP bit (I/O Port Rentention)

In Deep Software Standby mode, I/O ports keep the same states as in the Software Standby mode. The IOKEEP bit specifies whether to reset the state of the I/O ports or not when the Deep Software Standby mode is canceled.

DPSBY bit (Deep Software Standby)

The DPSBY bit controls transitions to Deep Software Standby mode.

When the WFI instruction is executed while SBYCR.SSBY bit and DPSBYCR.DPSBY bit are both 1, the MCU enters Deep Software Standby mode through Software Standby mode.

The DPSBY bit remains 1 when Deep Software Standby mode is canceled by certain pins which are sources of external pin interrupts (NMI, IRQn-DS (n = 0 to 15) or a peripheral interrupt (voltage monitor 1, or voltage monitor 2). Write 0 to this bit to clear it.

The DPSBY bit setting is invalid when OFS0.IWDTSTPCTL bit is 0 (counting continues) regardless of the setting in OFS0.IWDTSTRT bit. In that case, even when SBYCR.SSBY bit is 1 and the DPSBY bit is 1, the transition after the execution of a WFI instruction is to Software Standby mode.

The setting of the DPSBY bit is invalid when voltage monitor 1 reset is enabled (LVD1CR0.RI = 1) or when a voltage monitor 2 reset is enabled (LVD2CR0.RI = 1). In this case, even when the SBYCR.SSBY bit is 1 and the DPSBY bit is 1, the transition after the execution of a WFI instruction is to Software Standby mode.

10.2.14 DPSWCR : Deep Standby Wait Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x401

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	WTSTS[5:0]					
Value after reset:	0	0	0	1	1	0	0	1

Bit	Symbol	Function	R/W
5:0	WTSTS[5:0]	Deep Software Wait Standby Time Setting Bit 0x0E: Wait cycle for fast recovery 0x19: Wait cycle for slow recovery Others: Setting prohibited	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSBYCR不会由作为取消深度软件待机模式的源的内部复位信号初始化。有关详细信息，请参阅第5节，重置
。

DEEPCUT[1:0] bit (Power-Supply Control)

DEEPCUT[1:0]位控制对备用RAM和Deep中低速片上振荡器的内部电源
软件待机模式。此外，这些位控制LVD的状态和DeepSoftware中的上电复位电路
待机模式。

在深度软件待机模式下使用LVD中断时，DEEPCUT[1:0]位必须设置为00b或01b。

为降低功耗，将DEEPCUT[1:0]位设置为11b，使LVD停止并启用上电复位电路的低功耗功能。

无论DEEPCUT[1:0]位设置如何，在深度软件待机模式下，除待机SRAM之外的SRAM内部电源都会停止。

当使用深度待机模式时，在进入之前根据DEEPCUT[1]的值设置DPSWCR.WTSTS位
深度软件待机模式。

IOKEEP位（IO端口保留）

在深度软件待机模式下，IO端口保持与软件待机模式相同的状态。IOKEEP位指定当深度软件待机模式被取消时是否复位IO端口的状态。

DPSBY位（深度软件待机）

DPSBY位控制向深度软件待机模式的转换。

当SBYCR.SSBY位和DPSBYCR.DPSBY位均为1时执行WFI指令，MCU进入
深度软件待机模式到软件待机模式。

当某些引脚取消深度软件待机模式时，DPSBY位保持为1，这些引脚是外部引脚中断（NMI、IRQn-DS（n=0至15）或外设中断（电压监视器1或电压监视器2）的源）。向该位写入0以清除它。

无论OFS0.IWDTSTRT位的设置如何，当OFS0.IWDTSTPCL位为0（继续计数）时，DPSBY位设置无效。在这种情况下，即使SBYCR.SSBY位为1且DPSBY位为1，在执行WFI指令后转换为软件待机模式。

当使能电压监视器1复位(LVD1CR0.RI=1)或使能电压监视器2复位(LVD2CR0.RI=1)时，DPSBY位的设置无效。在这种情况下，即使SBYCR.SSBY位为1且DPSBY位为1，在执行WFI指令后转换为软件待机模式。

10.2.14 DPSWCR：深度待机等待控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x401

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	WTSTS[5:0]					
重置后的值：	0	0	0	1	1	0	0	1

Bit	Symbol	Function	R/W
5:0	WTSTS[5:0]	深度软件等待待机时间设置位 0x0E：快速恢复的等待周期0x19： 慢速恢复的等待周期 其他：禁止设置	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

The DPSWCR register sets the wait stabilization time when a Deep Software Standby mode is canceled by certain pins that are the sources of external pin interrupts or a peripheral interrupt.

During a wait stabilization period set in this register, a Deep Software Standby reset occurs, and the MCU is initialized.

The DPSWCR register is not initialized with the internal reset signal by the cancellation of the Deep Software Standby mode. For details, see section 5, Resets.

When a deep standby mode is used, set DPSWCR.WTSTS bits according to the value of DPSBYCR.DEEPCUT[1] before entering Deep Software Standby mode.

When DPSBYCR.DEEPCUT[1]=0, you can set DPSWCR.WTSTS to the wait cycle for fast recovery.

When DPSBYCR.DEEPCUT[1]=1, you must set DPSWCR.WTSTS to the wait cycle for slow recovery.

10.2.15 DPSIER0 : Deep Standby Interrupt Enable Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x402

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7E	DIRQ6E	DIRQ5E	DIRQ4E	DIRQ3E	DIRQ2E	DIRQ1E	DIRQ0E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0E	IRQ0-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
1	DIRQ1E	IRQ1-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
2	DIRQ2E	IRQ2-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
3	DIRQ3E	IRQ3-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
4	DIRQ4E	IRQ4-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
5	DIRQ5E	IRQ5-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
6	DIRQ6E	IRQ6-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
7	DIRQ7E	IRQ7-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIER0 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

After the setting of DPSIER0 is modified, an edge may be internally generated depending on the state of the pin, resulting in DPSIFR0 being set to 1. Therefore, DPSIFR0 should be cleared to 0 before entering Deep Software Standby mode.

当某个作为外部引脚中断或外设中断源的引脚取消深度软件待机模式时，DPSWCR寄存器设置等待稳定时间。

在此寄存器中设置的等待稳定期间，会发生深度软件待机复位，并且初始化MCU。

通过取消深度软件待机模式，DPSWCR寄存器不会使用内部复位信号进行初始化。有关详细信息，请参阅第5节，重置。

当使用深度待机模式时，在进入深度软件待机模式之前，根据DPSBYCR.DEEPCUT[1]的值设置DPSWCR.WTSTS位。

当DPSBYCR.DEEPCUT[1]=0时，可以设置DPSWCR.WTSTS为等待周期，以便快速恢复。

当DPSBYCR.DEEPCUT[1]=1时，必须将DPSWCR.WTSTS设置为等待周期，以便缓慢恢复。

10.2.15 DPSIER0：深度待机中断使能寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x402

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7E	DIRQ6E	DIRQ5E	DIRQ4E	DIRQ3E	DIRQ2E	DIRQ1E	DIRQ0E
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0E	IRQ0-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
1	DIRQ1E	IRQ1-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
2	DIRQ2E	IRQ2-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
3	DIRQ3E	IRQ3-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
4	DIRQ4E	IRQ4-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
5	DIRQ5E	IRQ5-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
6	DIRQ6E	IRQ6-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
7	DIRQ7E	IRQ7-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DPSIER0未被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

修改DPSIER0的设置后，可能会在内部产生一个边沿，具体取决于引脚的状态，导致DPSIFR0被设置为1。因此，在进入深度软件待机模式之前，应将DPSIFR0清零。

10.2.16 DPSIER1 : Deep Standby Interrupt Enable Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x403

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ15E	DIRQ14E	DIRQ13E	DIRQ12E	DIRQ11E	DIRQ10E	DIRQ9E	DIRQ8E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ8E	IRQ8-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
1	DIRQ9E	IRQ9-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
2	DIRQ10E	IRQ10-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
3	DIRQ11E	IRQ11-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
4	DIRQ12E	IRQ12-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
5	DIRQ13E	IRQ13-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
6	DIRQ14E	IRQ14-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
7	DIRQ15E	IRQ15-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIER1 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

After the setting of DPSIER1 is modified, an edge may be internally generated depending on the state of the pin, resulting in DPSIFR1 being set to 1. Therefore, DPSIFR1 should be cleared to 0 before entering Deep Software Standby mode.

10.2.17 DPSIER2 : Deep Standby Interrupt Enable Register 2

Base address: SYSC = 0x4001_E000

Offset address: 0x404

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIE	—	—	DLVD2IE	DLVD1IE
Value after reset:	0	0	0	0	0	0	0	0

10.2.16 DPSIER1：深度待机中断使能寄存器1

Base address: SYSC = 0x4001_E000

Offset address: 0x403

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ15E	DIRQ14E	DIRQ13E	DIRQ12E	DIRQ11E	DIRQ10E	DIRQ9E	DIRQ8E
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ8E	IRQ8-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
1	DIRQ9E	IRQ9-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
2	DIRQ10E	IRQ10-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
3	DIRQ11E	IRQ11-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
4	DIRQ12E	IRQ12-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
5	DIRQ13E	IRQ13-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
6	DIRQ14E	IRQ14-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
7	DIRQ15E	IRQ15-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DPSIER1未被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

修改DPSIER1的设置后，可能会在内部产生一个边沿，具体取决于引脚的状态，导致DPSIFR1被设置为1。因此，在进入深度软件待机模式之前，应将DPSIFR1清零。

10.2.17 DPSIER2：深度待机中断使能寄存器2

Base address: SYSC = 0x4001_E000

Offset address: 0x404

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIE	—	—	DLVD2IE	DLVD1IE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLVD1IE	LVD1 Deep Standby Cancel Signal Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
1	DLVD2IE	LVD2 Deep Standby Cancel Signal Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	DNMIE	NMI Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W*1
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.
Note 1. 1 can be written only once. Once 1 is written to this bit, subsequent write accesses are disabled.

DPSIER2 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

After the setting of DPSIER2 is modified, an edge may be internally generated depending on the state of the pin, resulting in DPSIFR2 being set to 1. Therefore, DPSIFR2 should be cleared to 0 before entering Deep Software Standby mode.

10.2.18 DPSIFR0 : Deep Standby Interrupt Flag Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x406

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7F	DIRQ6F	DIRQ5F	DIRQ4F	DIRQ3F	DIRQ2F	DIRQ1F	DIRQ0F
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0F	IRQ0-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
1	DIRQ1F	IRQ1-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
2	DIRQ2F	IRQ2-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
3	DIRQ3F	IRQ3-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
4	DIRQ4F	IRQ4-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
5	DIRQ5F	IRQ5-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
6	DIRQ6F	IRQ6-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W

Bit	Symbol	Function	R/W
0	DLVD1IE	LVD1深度待机取消信号使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
1	DLVD2IE	LVD2深度待机取消信号使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	DNMIE	NMI引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W*1
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。
注1.1只能写一次。一旦向该位写入1，随后的写访问将被禁用。

DPSIER2未被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

修改DPSIER2的设置后，可能会根据引脚的状态在内部产生一个边沿，从而导致DPSIFR2被设置为1。因此，在进入深度软件待机模式之前，应将DPSIFR2清除为0。

10.2.18 DPSIFR0：深度待机中断标志寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x406

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7F	DIRQ6F	DIRQ5F	DIRQ4F	DIRQ3F	DIRQ2F	DIRQ1F	DIRQ0F
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0F	IRQ0-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
1	DIRQ1F	IRQ1-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
2	DIRQ2F	IRQ2-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
3	DIRQ3F	IRQ3-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
4	DIRQ4F	IRQ4-DS引脚深度待机取消标志 0：不产生取消请求 1：生成取消请求	R/W
5	DIRQ5F	IRQ5-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
6	DIRQ6F	IRQ6-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W

Bit	Symbol	Function	R/W
7	DIRQ7F	IRQ7-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Writing 0 clears the flag. Writing 1 is ignored.
Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Each flag is set to 1 when a cancel request specified by DPSIEGR0 is generated.

Each flag may be set to 1 when a cancel request is generated in any mode (not only in Deep Software Standby mode) or when the setting of DPSIER0 is modified. Therefore, a transition to Deep Software Standby mode should be made after DPSIFR0 is cleared to 0x00.

To clear DPSIFR0 to 0x00 after modifying DPSIER0, wait for at least 6 PCLKB cycles, read DPSIFR0, and then write 0 to DPSIFR0. Six or more PCLKB cycles can be secured, for example, by reading DPSIER0.

DPSIFR0 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. To clear DPSIFR0 to 0x00 after modifying DPSIER0, wait for at least 6 PCLKB cycles, read DPSIFR0, and then write 0 to DPSIFR0. Six or more PCLKB cycles can be secured, for example, by reading DPSIER0. For details, see section 5, Resets.

DIRQnF flag (IRQn-DS Pin Deep Standby Cancel Flag) (n = 0 to 7)

The DIRQnF flag indicates that a cancel request by the IRQn-DS pin has been generated.

[Setting condition]

A cancel request by the IRQn-DS pin specified by DPSIEGR0 is generated.

[Clearing condition]

Writing 0 to each flag after 1 is read.

10.2.19 DPSIFR1 : Deep Standby Interrupt Flag Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x407

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ15F	DIRQ14F	DIRQ13F	DIRQ12F	DIRQ11F	DIRQ10F	DIRQ9F	DIRQ8F
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ8F	IRQ8-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
1	DIRQ9F	IRQ9-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
2	DIRQ10F	IRQ10-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
3	DIRQ11F	IRQ11-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
4	DIRQ12F	IRQ12-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W

Bit	Symbol	Function	R/W
7	DIRQ7F	IRQ7-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 写入0清除标志。写入1被忽略。
Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

当生成由DPSIEGR0指定的取消请求时，每个标志都设置为1。

当在任何模式下（不仅在深度软件待机模式下）生成取消请求或修改DPSIER0的设置时，每个标志都可以设置为1。因此，应在DPSIFR0清零后转换到深度软件待机模式。

要在修改DPSIER0后将DPSIFR0清为0x00，请等待至少6个PCLKB周期，读取DPSIFR0，然后将0写入DPSIFR0。例如，可以通过读取DPSIER0来确保六个或更多PCLKB周期。

DPSIFR0不被用作深度软件待机模式取消源的内部复位信号初始化。清除修改DPSIER0后DPSIFR0到0x00，等待至少6个PCLKB周期，读取DPSIFR0，然后写入0到DPSIFR0。例如，可以通过读取DPSIER0来确保六个或更多PCLKB周期。有关详细信息，请参阅第5节，重置。

DIRQnF标志（IRQn-DS引脚深度待机取消标志）（n=0至7）

DIRQnF标志表示已生成IRQn-DS引脚的取消请求。

[Setting condition]

由DPSIEGR0指定的IRQn-DS引脚产生一个取消请求。

[Clearing condition]

读取1后将0写入每个标志。

10.2.19 DPSIFR1：深度待机中断标志寄存器1

Base address: SYSC = 0x4001_E000

Offset address: 0x407

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ15F	DIRQ14F	DIRQ13F	DIRQ12F	DIRQ11F	DIRQ10F	DIRQ9F	DIRQ8F
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ8F	IRQ8-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
1	DIRQ9F	IRQ9-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
2	DIRQ10F	IRQ10-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
3	DIRQ11F	IRQ11-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
4	DIRQ12F	IRQ12-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W

Bit	Symbol	Function	R/W
5	DIRQ13F	IRQ13-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
6	DIRQ14F	IRQ14-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
7	DIRQ15F	IRQ15-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Writing 0 clears the flag. Writing 1 is ignored.
Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Each flag is set to 1 when a cancel request specified by DPSIEGR1 is generated.

Each flag may be set to 1 when a cancel request is generated in any mode (not only in Deep Software Standby mode) or when the setting of DPSIER1 is modified. Therefore, a transition to Deep Software Standby mode should be made after DPSIFR1 is cleared to 0x00.

To clear DPSIFR1 to 0x00 after modifying DPSIER1, wait for at least 6 PCLKB cycles, read DPSIFR1, and then write 0 to DPSIFR1. Six or more PCLKB cycles can be secured, for example, by reading DPSIER1.

DPSIFR1 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

DIRQnF flag (IRQn-DS Pin Deep Standby Cancel Flag) (n = 8 to 15)

The DIRQnF flag indicates that a cancel request by the IRQn-DS pin has been generated.

[Setting condition]

A cancel request by the IRQn-DS pin specified by DPSIEGR1 is generated.

[Clearing condition]

Writing 0 to each flag after 1 is read.

10.2.20 DPSIFR2 : Deep Standby Interrupt Flag Register 2

Base address: SYSC = 0x4001_E000

Offset address: 0x408

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIF	—	—	DLVD2IF	DLVD1IF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLVD1IF	LVD1 Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
1	DLVD2IF	LVD2 Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	DNMIF	NMI Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W

Bit	Symbol	Function	R/W
5	DIRQ13F	IRQ13-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
6	DIRQ14F	IRQ14-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
7	DIRQ15F	IRQ15-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 写入0清除标志。写入1被忽略。
Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

当生成由DPSIEGR1指定的取消请求时，每个标志都设置为1。

当在任何模式下（不仅在深度软件待机模式下）生成取消请求或修改DPSIER1的设置时，每个标志都可以设置为1。因此，应在DPSIFR1被清除为0x00后转换到深度软件待机模式。

修改DPSIER1后要清除DPSIFR1为0x00，至少等待6个PCLKB周期，读取DPSIFR1，然后将0写入DPSIFR1。例如，可以通过读取DPSIER1来确保六个或更多PCLKB周期。

DPSIFR1未被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

DIRQnF标志（IRQn-DS引脚深度待机取消标志）（n=8到15）

DIRQnF标志表示已生成IRQn-DS引脚的取消请求。

[Setting condition]

由DPSIEGR1指定的IRQn-DS引脚产生取消请求。

[Clearing condition]

读取1后将0写入每个标志。

10.2.20 DPSIFR2：深度待机中断标志寄存器2

Base address: SYSC = 0x4001_E000

Offset address: 0x408

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIF	—	—	DLVD2IF	DLVD1IF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLVD1IF	LVD1深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
1	DLVD2IF	LVD2深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	DNMIF	NMI引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W

Bit	Symbol	Function	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Writing 0 clears the flag. Writing 1 is ignored.
Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Each flag is set to 1 when a cancel request specified by DPSIEGR2 is generated.

Each flag may be set to 1 when a cancel request is generated in any mode (not only in Deep Software Standby mode) or when the setting of DPSIER2 is modified. Therefore, a transition to Deep Software Standby mode should be made after DPSIFR2 is cleared to 0x00.

To clear DPSIFR2 to 0x00 after modifying DPSIER2, wait for at least 6 PCLKB cycles, read DPSIFR2, and then write 0 to DPSIFR2. Six or more PCLKB cycles can be secured, for example, by reading DPSIER2.

DPSIFR2 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

DLVDmIF flag (LVDm Deep Standby Cancel Flag) (m = 1 to 2)

The DLVDmIF flag indicates that a cancel request by the voltage monitor m signal has been generated.

[Setting condition]

A cancel request is generated by the voltage monitor m signal that is selected in DPSIEGR2.

[Clearing condition]

Writing 0 to each flag after 1 is read.

DNMIF flag (NMI Pin Deep Standby Cancel Flag)

This flag indicates that a cancel request by the NMI pin has been generated.

[Setting condition]

A cancel request by the NMI pin specified by DPSIEGR2 is generated

[Clearing condition]

Writing 0 to each flag after 1 is read.

10.2.21 DPSIEGR0 : Deep Standby Interrupt Edge Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x40A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7EG	DIRQ6EG	DIRQ5EG	DIRQ4EG	DIRQ3EG	DIRQ2EG	DIRQ1EG	DIRQ0EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0EG	IRQ0-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
1	DIRQ1EG	IRQ1-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
2	DIRQ2EG	IRQ2-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W

Bit	Symbol	Function	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 写入0清除标志。写入1被忽略。
Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

当生成由DPSIEGR2指定的取消请求时，每个标志都设置为1。

当在任何模式下（不仅在深度软件待机模式下）生成取消请求或修改DPSIER2的设置时，每个标志都可以设置为1。因此，应在DPSIFR2清零为0x00后转换到深度软件待机模式。

要在修改DPSIER2后将DPSIFR2清为0x00，请等待至少6个PCLKB周期，读取DPSIFR2，然后将0写入DPSIFR2。例如，可以通过读取DPSIER2来确保六个或更多PCLKB周期。

DPSIFR2未被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

DLVDmIF标志（LVDm深度待机取消标志）（m=1到2）

DLVDmIF标志表示电压监视器m信号的取消请求已经产生。

[Setting condition]

取消请求由DPSIEGR2中选择的电压监视器m信号生成。

[Clearing condition]

读取1后将0写入每个标志。

DNMIF标志（NMI引脚深度待机取消标志）

该标志表示已生成NMI引脚的取消请求。

[Setting condition]

由DPSIEGR2指定的NMI引脚生成取消请求

[Clearing condition]

读取1后将0写入每个标志。

10.2.21 DPSIEGR0：深度待机中断边沿寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x40A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7EG	DIRQ6EG	DIRQ5EG	DIRQ4EG	DIRQ3EG	DIRQ2EG	DIRQ1EG	DIRQ0EG
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0EG	IRQ0-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W
1	DIRQ1EG	IRQ1-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W
2	DIRQ2EG	IRQ2-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W

Bit	Symbol	Function	R/W
3	DIRQ3EG	IRQ3-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
4	DIRQ4EG	IRQ4-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
5	DIRQ5EG	IRQ5-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
6	DIRQ6EG	IRQ6-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
7	DIRQ7EG	IRQ7-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIEGR0 is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode. For details, see section 5, Resets.

10.2.22 DPSIEGR1 : Deep Standby Interrupt Edge Register 1

Base address: SYSC = 0x4001 E000

Offset address: 0x40B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ15EG	DIRQ14EG	DIRQ13EG	DIRQ12EG	DIRQ11EG	DIRQ10EG	DIRQ9EG	DIRQ8EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ8EG	IRQ8-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
1	DIRQ9EG	IRQ9-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
2	DIRQ10EG	IRQ10-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge	R/W
3	DIRQ11EG	IRQ11-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
4	DIRQ12EG	IRQ12-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
5	DIRQ13EG	IRQ13-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
6	DIRQ14EG	IRQ14-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W

Bit	Symbol	Function	R/W
3	DIRQ3EG	IRQ3-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W
4	DIRQ4EG	IRQ4-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W
5	DIRQ5EG	IRQ5-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W
6	DIRQ6EG	IRQ6-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W
7	DIRQ7EG	IRQ7-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DPSIEGR0不会被作为取消深度软件待机模式的源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

10.2.22 DPSIEGR1：深度待机中断边沿寄存器1

Base address: SYSC = 0x4001 E000

Offset address: 0x40B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ15EG	DIRQ14EG	DIRQ13EG	DIRQ12EG	DIRQ11EG	DIRQ10EG	DIRQ9EG	DIRQ8EG
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ8EG	IRQ8-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求。	R/W
1	DIRQ9EG	IRQ9-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求。	R/W
2	DIRQ10EG	IRQ10-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求	R/W
3	DIRQ11EG	IRQ11-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求。	R/W
4	DIRQ12EG	IRQ12-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求。	R/W
5	DIRQ13EG	IRQ13-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求。	R/W
6	DIRQ14EG	IRQ14-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求。	R/W

Bit	Symbol	Function	R/W
7	DIRQ15EG	IRQ15-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIEGR1 is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode. For details, see section 5, Resets.

10.2.23 DPSIEGR2 : Deep Standby Interrupt Edge Register 2

Base address: SYSC = 0x4001_E000

Offset address: 0x40C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIEG	—	—	DLVD2EG	DLVD1EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLVD1EG	LVD1 Edge Select 0: A cancel request is generated when VCC < V_{det1} (fall) is detected 1: A cancel request is generated when VCC ≥ V_{det1} (rise) is detected	R/W
1	DLVD2EG	LVD2 Edge Select 0: A cancel request is generated when VCC < V_{det2} (fall) is detected 1: A cancel request is generated when VCC ≥ V_{det2} (rise) is detected	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	DNMIEG	NMI Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIEGR2 is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode. For details, see section 5, Resets.

10.2.24 SYOCDCR : System Control OCD Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x040E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DBGEN	—	—	—	—	—	—	DOCDF
Value after reset:	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
7	DIRQ15EG	IRQ15-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DPSIEGR1不会被作为取消深度软件待机模式的源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

10.2.23 DPSIEGR2：深度待机中断边沿寄存器2

Base address: SYSC = 0x4001_E000

Offset address: 0x40C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIEG	—	—	DLVD2EG	DLVD1EG
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLVD1EG	LVD1边沿选择 0：检测到VCC<Vdet1（下降）时产生取消请求1：检测到VCC≥Vdet1（上升）时产生取消请求	R/W
1	DLVD2EG	LVD2边沿选择 0：检测到VCC<Vdet2（下降）时产生取消请求1：检测到VCC≥Vdet2（上升）时产生取消请求	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	DNMIEG	NMI引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DPSIEGR2不会由作为取消深度软件待机模式的源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

10.2.24 SOOCDCR:系统控制OCD控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x040E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DBGEN	—	—	—	—	—	—	DOCDF
重置后的值：	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	DOCDF	Deep Software Standby OCD flag 0: DBIRQ is not generated 1: DBIRQ is generated	R/W*1
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	DBGEN	Debugger Enable bit Set to 1 first in on-chip debug mode. 0: On-chip debugger is disabled 1: On-chip debugger is enabled	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.
Note 1. Writing 0 clears the flag. Writing 1 is ignored

This register is not controlled by any security attribute register (eg. LPMSAR, DPFSAR).

SYOCDCR can be written when DBGSTR.CDBGPWRUPREQ = 1 (the debugger is connected).

SYOCDCR is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode.

DOCDF flag (Deep Software Standby OCD flag)

DOCDF flag indicates that a cancel request of Deep Software Standby mode by the MCUCTRL.DBIRQ bit has been generated. DOCDF flag is set to 1 when a cancel request is generated. This flag may be set to 1 when a cancel request is generated in any mode (not only in Deep Software Standby mode). Therefore, a transition to Deep Software Standby mode must be made after DOCDF flag is cleared to 0.

[Setting condition]

- A cancel request by the MCUCTRL.DBIRQ is generated

[Clearing condition]

- Writing 0 to the flag after reading the bit as 1
- When DBGEN bit is 0

DBGEN bit (Debugger Enable bit)

The DBGEN bit enables the on-chip debug mode. This bit must be set to 1 first in the on-chip debugger mode.

[Setting condition]

- Writing 1 to the bit when the debugger is connected.

[Clearing condition]

- Power-on reset is generated
- Writing 0 to the bit.

Note: Certain restrictions apply in terms of the MCU states in which the DBGEN bit can be set to 1. For details, see section 2.13.2. Restrictions on Connecting an OCD emulator.

10.3 Reducing Power Consumption by Switching Clock Signals

The clock frequency changes when the SCKDIVCR register is set.

For information on module and clock associations, see section 8.2.2. SCKDIVCR : System Clock Division Control Register.

10.4 Module-Stop Function

The module stop function can stop the clock supply set for each peripheral module.

When the MSTPmi bit (m = A to E, i = 31 to 0) in MSTPCRn (n = A to E) is set to 1, the specified module stops operating and enters the module-stop state, but the CPU continues to operate independently. Setting the MSTPmi bit to 0 cancels the module-stop state, allowing the module to resume operation at the end of the bus cycle.

Bit	Symbol	Function	R/W
0	DOCDF	深度软件待机OCD标志 0：不产生DBIRQ1：产生D BIRQ	R/W*1
6:1	—	这些位被读取为0。写入值应为0。	R/W
7	DBGEN	调试器使能位 在片上调试模式下首先设置为1。 0：禁用片上调试器1：启用片上 调试器	R/W

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。
注1.写入0清除标志。写1被忽略

该寄存器不受任何安全属性寄存器（例如LPMSAR、DPFSAR）的控制。

当DBGSTR.CDBGPWRUPREQ=1（调试器已连接）时，可以写入SOOCDCR。

SOOCDCR不会由作为取消深度软件待机模式的源的内部复位信号初始化。

DOCDF标志（深度软件待机OCD标志）

DOCDF标志指示已通过MCUCTRL.DBIRQ位生成了深度软件待机模式的取消请求。生成取消请求时，DOCDF标志设置为1。当在任何模式下（不仅在深度软件待机模式下）生成取消请求时，此标志可能设置为1。因此，必须在DOCDF标志清零后转换到深度软件待机模式。

[Setting condition]

●MCUCTRL.DBIRQ产生取消请求

[Clearing condition]

●读取位为1后向标志位写入0

●DBGEN位为0时

DBGEN位（调试器启用位）

DBGEN位使能片上调试模式。在片上调试器模式下，该位必须首先设置为1。

[Setting condition]

●连接调试器时向该位写入1。

[Clearing condition]

●产生上电复位

●向该位写入0。

Note: 某些限制适用于可以将DBGEN位设置为1的MCU状态。有关详细信息，请参阅第2.13.2节。连接强迫症模拟器的限制。

10.3 通过切换时钟信号降低功耗

设置SCKDIVCR寄存器时，时钟频率会发生变化。

有关模块和时钟关联的信息，请参见第8.2.2节。SCKDIVCR:系统时钟分频控制Register.

10.4 Module-Stop Function

模块停止功能可以停止为每个外围模块设置的时钟供应。

当MSTPCRn(n=AtoE)中的MSTPmi位(m=AtoE i=31to0)设置为1时，指定模块停止运行并进入module-stop状态，但CPU继续运行独立。将MSTPmi位设置为0可取消模块停止状态，允许模块在总线周期结束时恢复运行。

After a reset is canceled, all modules other than the DMAC, DTC and SRAMn modules are placed in the module-stop state. Do not access the module while the corresponding MSTPmi bit is 1. Additionally, do not set 1 to the MSTPmi bit while the corresponding module is accessed.

When the PLL is selected as the clock source, MSTPmi bits must be changed only one bit at a time. In this case, wait at least 250 ns after changing each MSTPmi bit before starting subsequent processing if you change any of the following bits:

MSTPD16 (ADC), MSTPC31 (SCE5).

The recommended method to measure the wait time is through software. Be sure to consider the worst-case conditions to ensure that the required wait time elapses.

10.5 Function for Lower Operating Power Consumption

By selecting an appropriate operating power consumption control mode according to the operating frequency, power consumption can be reduced in Normal mode, Sleep mode, and Snooze mode.

10.5.1 Setting Operating Power Control Mode

Ensure the operating condition such as the frequency range is always within the specified range before and after switching the operating power control modes.

This section provides example procedures for switching operating power control modes.

Table 10.5 Available oscillators in each mode

Mode	Oscillator					
	PLL, PLL2	High-speed on-chip oscillator	Middle-speed on-chip oscillator	Low-speed on-chip oscillator	Main clock oscillator	IWDT-dedicated on-chip oscillator
High-speed	Available	Available	Available	Available	Available	Available
Low-speed	N/A	Available	Available	Available	Available	Available

(1) Switching from a higher power mode to a lower power mode

Example 1: From High-speed mode to Low-speed mode:

(Operation begins in High-speed mode)

1. Change the oscillator to what is used in Low-speed mode. Set the frequency of each clock lower than the maximum operating frequency in Low-speed mode.
2. Turn off the oscillator that is not required in Low-speed mode.
3. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
4. Set the OPCCR.OPCM[1:0] bits to 11b (Low-speed mode).
5. Confirm that OPCCR.OPCMTSF flag is 0 (indicates transition completed).

(Operation is now in Low-speed mode)

(2) Switching from a lower power mode to a higher power mode

Example 1: From Low-speed mode to High-speed mode

(Operation begins in Low-speed mode)

1. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
2. Set the OPCCR.OPCM[1:0] bits to 00b (High-speed mode).
3. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
4. Turn on any required oscillator in High-speed mode.
5. Set the frequency of each clock lower than the maximum operating frequency for High-speed mode.

取消复位后，除DMAC、DTC和SRAMn模块之外的所有模块都置于模块停止状态。相应的MSTPmi位为1时不要访问模块。另外，访问相应的模块时不要将MSTPmi位设置为1。

WhenthePLLisselectedastheclocksource MSTPmibitsmustbechangedonlyonebitatatime.在这种情况下，如果更改以下任何位，请在更改每个MSTPmi位后至少等待250ns，然后再开始后续处理：

MSTPD16 (ADC), MSTPC31 (SCE5).

测量等待时间的推荐方法是通过软件。请务必考虑最坏情况，以确保经过所需的等待时间。

10.5 降低运行功耗的功能

通过根据工作频率选择合适的工作功耗控制模式，可以在正常模式、睡眠模式和贪睡模式下降低功耗。

10.5.1 设置工作电源控制模式

确保在切换工作功率控制模式前后，频率范围等工作条件始终在规定范围内。

本节提供切换操作电源控制模式的示例程序。

Table 10.5 每种模式下可用的振荡器

Mode	Oscillator					
	PLL, PLL2	High-speed on-chip oscillator	Middle-speed on-chip oscillator	Low-speed on-chip oscillator	主时钟振荡器	IWDT-dedicated on-chip oscillator
High-speed	Available	Available	Available	Available	Available	Available
Low-speed	N/A	Available	Available	Available	Available	Available

(1) 从高功率模式切换到低功率模式

示例1：从高速模式到低速模式：

（以高速模式开始运行）

1.将振荡器更改为低速模式下使用的振荡器。将每个时钟的频率设置为低于低速模式下的最大工作频率。

2.关闭低速模式下不需要的振荡器。

3.确认OPCCR.OPCMTSF标志为0（表示转换完成） 。

4.将OPCCR.OPCM[1:0]位设置为11b（低速模式）。

5.确认OPCCR.OPCMTSF标志为0（表示转换完成） 。

（操作现在处于低速模式）

(2) 从低功耗模式切换到高功耗模式

示例1：从低速模式到高速模式

（以低速模式开始运行）

1.确认OPCCR.OPCMTSF标志为0（表示转换完成） 。

2.将OPCCR.OPCM[1:0]位设置为00b（高速模式）。

3.确认OPCCR.OPCMTSF标志为0（表示转换完成） 。

4.在高速模式下打开任何需要的振荡器。

5.将每个时钟的频率设置为低于高速模式的最大工作频率。

(Operation is now in High-speed mode)

10.6 Sleep Mode

10.6.1 Transitioning to Sleep Mode

When a WFI instruction is executed while SBYCR.SSBY bit is 0, the MCU enters Sleep mode. In this mode, the CPU stops operating but the contents of its internal registers are retained. Other peripheral functions do not stop. Available resets or interrupts in Sleep mode cause the MCU to cancel Sleep mode. All interrupt sources are available. If using an interrupt to cancel Sleep mode, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 12, Interrupt Controller Unit (ICU).

Counting by IWDT stops when the MCU enters Sleep mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep mode, Software Standby mode, or Snooze mode).

Counting by IWDT continues when the MCU enters Sleep mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep mode, Software Standby mode, or Snooze mode).

Counting by WDT stops when the MCU enters Sleep mode while the WDT is in auto start mode and the OFS0.WDTSTPCTL bit is 1 (WDT stops in Sleep mode). Similarly, counting by WDT stops when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit is 1 (WDT stops in Sleep mode).

Counting by WDT continues when the MCU enters Sleep mode while the WDT is in auto start mode and the OFS0.WDTSTPCTL bit is 0 (WDT does not stop in Sleep mode). Similarly, counting by WDT continues when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit is 0 (WDT does not stop in Sleep mode).

10.6.2 Canceling Sleep Mode

Sleep mode is canceled by:

- An interrupt
- A RES pin reset
- A power-on reset
- A voltage monitor reset
- An SRAM parity error reset
- An SRAM ECC error reset
- A bus master MPU error reset
- A TrustZone error reset
- A reset caused by an IWDT or a WDT underflow

The operations are as follows:

1. Canceling by an interrupt
   When an available interrupt request is generated, Sleep mode is canceled and the MCU starts the interrupt handling.
2. Canceling by RES pin reset
   When the RES pin is driven low, the MCU enters the reset state. Be sure to keep the RES pin low for the time period specified in section 46, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts the reset exception handling.
3. Canceling by IWDT reset
   - Sleep mode is canceled by an internal reset generated by an IWDT underflow and the MCU starts the reset exception handling. However, IWDT stops in Sleep mode and an internal reset for canceling Sleep mode is not generated in the following conditions:
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.
4. Canceling by WDT reset

（操作现在处于高速模式）

10.6 睡眠模式

10.6.1 转换到睡眠模式

当SBYCR.SSBY位为0时执行WFI指令，MCU进入休眠模式。在这种模式下，CPU停止运行，但其内部寄存器的内容被保留。其他外围功能不会停止。休眠模式下可用的复位或中断会导致MCU取消休眠模式。所有中断源均可用。如果使用中断取消休眠模式，则必须在执行WFI指令之前设置相关的IELSRn寄存器。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

当MCU进入休眠模式且IWDT处于自动启动模式且OFS0.IWDTSTPCTL位为1（IWDT在休眠模式、软件待机模式或贪睡模式下停止）。

当MCU进入休眠模式且IWDT处于自动启动模式且OFS0.IWDTSTPCTL位为0（IWDT在休眠模式、软件待机模式或贪睡模式下不停止）时，IWDT继续计数。

当MCU进入休眠模式且WDT处于自动启动模式且OFS0.WDTSTPCTL位为1（WDT在休眠模式下停止）。同样，当MCU进入休眠模式且WDT处于寄存器启动模式且WDTCSTPR.SLCSTP位为1（WDT在休眠模式下停止）时，WDT停止计数。

当MCU进入休眠模式且WDT处于自动启动模式且OFS0.WDTSTPCTL位为0（WDT在休眠模式下不停止）。同样，当MCU进入休眠模式且WDT处于寄存器启动模式且WDTCSTPR.SLCSTP位为0（休眠模式下WDT不会停止）时，WDT继续计数。

10.6.2 取消睡眠模式

睡眠模式通过以下方式取消：

●中断

●ARES引脚复位

- A power-on reset

●电压监视器复位

●SRAM奇偶校验错误复位

●SRAMECC错误复位

●总线主控MPU错误复位

●TrustZone错误重置

●IWDT或WDT下溢引起的复位

操作如下：

1.中断取消
当产生可用的中断请求时，休眠模式被取消，MCU开始中断处理。

2.通过RES引脚复位取消
当RES引脚驱动为低电平时，MCU进入复位状态。请务必在第46节“电气特性”中指定的时间段内保持RES引脚为低电平。当RES引脚在指定时间后被驱动为高电平时，CPU开始复位异常处理。

3.IWDT复位取消

●休眠模式由IWDT下溢产生的内部复位取消，MCU开始复位
异常处理。但是，IWDT在休眠模式下停止，并且在以下情况下不会产生用于取消休眠模式的内部复位：

- OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.

4.WDT复位取消

Sleep mode is canceled by an internal reset generated by a WDT underflow and the MCU starts the reset exception handling. However, WDT stops in Sleep mode even when counting in Normal mode and an internal reset for canceling Sleep mode is not generated in the following conditions:

- OFS0.WDTSTRT = 0 (auto start mode) and OFS0.WDTSTPCTL = 1
- OFS0.WDTSTRT = 1 (register start mode) and WDTCSTPR.SLCSTP = 1.

5. Canceling by other resets available in Sleep mode
Sleep mode is canceled by other resets and the MCU starts the reset exception handling.

Note: For details on proper setting of the interrupts, see section 12, Interrupt Controller Unit (ICU).

10.7 Software Standby Mode

10.7.1 Transitioning to Software Standby Mode

When a WFI instruction is executed while SBYCR.SSBY bit is 1 and DPSBYCR.DPSBY bit is 0, the MCU enters Software Standby mode. In this mode, the CPU, most of the on-chip peripheral functions and the oscillators stop. However, the contents of the CPU internal registers and SRAM data, the states of on-chip peripheral functions and the I/O ports are retained. Software Standby mode allows significant reduction in power consumption because most of the oscillators stops in this mode. Table 10.2 shows the status of each on-chip peripheral functions and oscillators. Available resets or interrupts in Software Standby mode make the MCU to cancel Software Standby mode. See Table 10.3 for available interrupt sources and section 12.2.17. WUPEN0 : Wake Up Interrupt Enable Register 0 for information on waking up the MCU from Software Standby mode. If using an interrupt to cancel an interrupt, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 12, Interrupt Controller Unit (ICU).

Clear DMAST.DMST bit and DTCST.DTCST bit to 0 before executing WFI instruction except when using DTC in Snooze mode. If DTC is required in Snooze mode, set DTCST.DTCST bit to 1 before executing a WFI instruction.

Counting by the IWDT stops if the MCU enters Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep, Software Standby or Snooze mode).

Counting by the IWDT continues if the MCU enters Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep, Software Standby or Snooze mode).

WDT stops counting when the MCU enters Software Standby mode because the PCLKB stops.

Do not enter Software Standby mode while OSTDCR.OSTDE = 1 (oscillation stop detection function is enabled). To enter Software Standby mode, execute a WFI instruction after disabling the oscillation stop detection function (OSTDCR.OSTDE = 0). In case of executing WFI instruction while OSTDCR.OSTDE = 1, the MCU enters Sleep mode even if SBYCR.SSBY = 1.

Do not enter Software Standby mode while the flash memory is programming or erasing. To enter Software Standby mode, execute a WFI instruction after programming or erasing procedure completes.

When the PLL is selected as the clock source, set the following modules to the module-stop state before executing a WFI instruction:

ADC, SCE5.

In this case, wait for least 750 ns and if the ICLK frequency before executing the WFI instruction exceeds 120 MHz, it is necessary to set the ICLK frequency division ratio to 1/2 and wait 5 µs. The recommended method to measure the wait time is through software. Be sure to consider the worst-case conditions to ensure that the required wait time elapses.

睡眠模式由WDT下溢产生的内部复位取消，MCU启动复位异常处理。但是，即使在正常模式下计数，WDT也会在休眠模式下停止，并且在以下情况下不会产生用于取消休眠模式的内部复位：

●OFS0.WDTSTRT=0（自动启动模式）和OFS0.WDTSTPCTL=1

●OFS0.WDTSTRT=1（寄存器启动模式）和WDTCSTPR.SLCSTP=1。

5.通过睡眠模式下可用的其他复位取消
休眠模式被其他复位取消，MCU开始复位异常处理。

Note: 有关正确设置中断的详细信息，请参阅第12节，中断控制器单元(ICU)。

10.7 软件待机模式

10.7.1 过渡到软件待机模式

当SBYCR.SSBY位为1且DPSBYCR.DPSBY位为0时执行WFI指令，MCU进入软件待机模式。在这种模式下，CPU、大部分片上外围功能和振荡器停止。但是，CPU内部寄存器和SRAM数据的内容、片上外围功能的状态和IO端口的状态会被保留。软件待机模式可显着降低功耗，因为大多数振荡器在此模式下停止。表10.2显示了每个片上外围功能和振荡器的状态。软件待机模式下可用的复位或中断使MCU取消软件待机模式。有关可用的中断源，请参见表10.3和第12.2.17节。WUPEN0：唤醒中断使能寄存器0用于将MCU从软件待机模式唤醒的信息。如果使用中断取消中断，则必须在执行WFI指令之前设置相关的IELSRn寄存器。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

在执行WFI指令之前将DMAST.DMST位和DTCST.DTCST位清除为0，除非在贪睡模式下使用DTC。如果在贪睡模式下需要DTC，请在执行WFI指令之前将DTCST.DTCST位设置为1。

如果MCU进入软件待机模式，而IWDT处于自动启动模式并且OFS0.IWDTSTPCTL位为1（IWDT在休眠、软件待机或贪睡模式下停止）。

如果MCU进入软件待机模式，而IWDT处于自动启动模式并且OFS0.IWDTSTPCTL位为0（IWDT在休眠、软件待机或贪睡模式下不停止）。

当MCU进入软件待机模式时，WDT停止计数，因为PCLKB停止。

OSTDCR.OSTDE=1时不要进入软件待机模式（振荡停止检测功能启用）。要进入软件待机模式，请在禁用振荡停止检测功能(OSTDCR.OSTDE=0)后执行WFI指令。如果在OSTDCR.OSTDE=1时执行WFI指令，即使SBYCR.SSBY=1，MCU也会进入休眠模式。

闪存正在编程或擦除时，请勿进入软件待机模式。要进入软件待机模式，请在编程或擦除过程完成后执行WFI指令。

WhenthePLLisselectedastheclocksource setthefollowingmodulestothemodule−stopstatebeforeexecutingaWFIinstruction:

ADC, SCE5.

在这种情况下，至少等待750ns，如果执行WFI指令前的ICLK频率超过120MHz，则需要将ICLK分频比设置为12并等待5µs。测量等待时间的推荐方法是通过软件。请务必考虑最坏情况，以确保经过所需的等待时间。

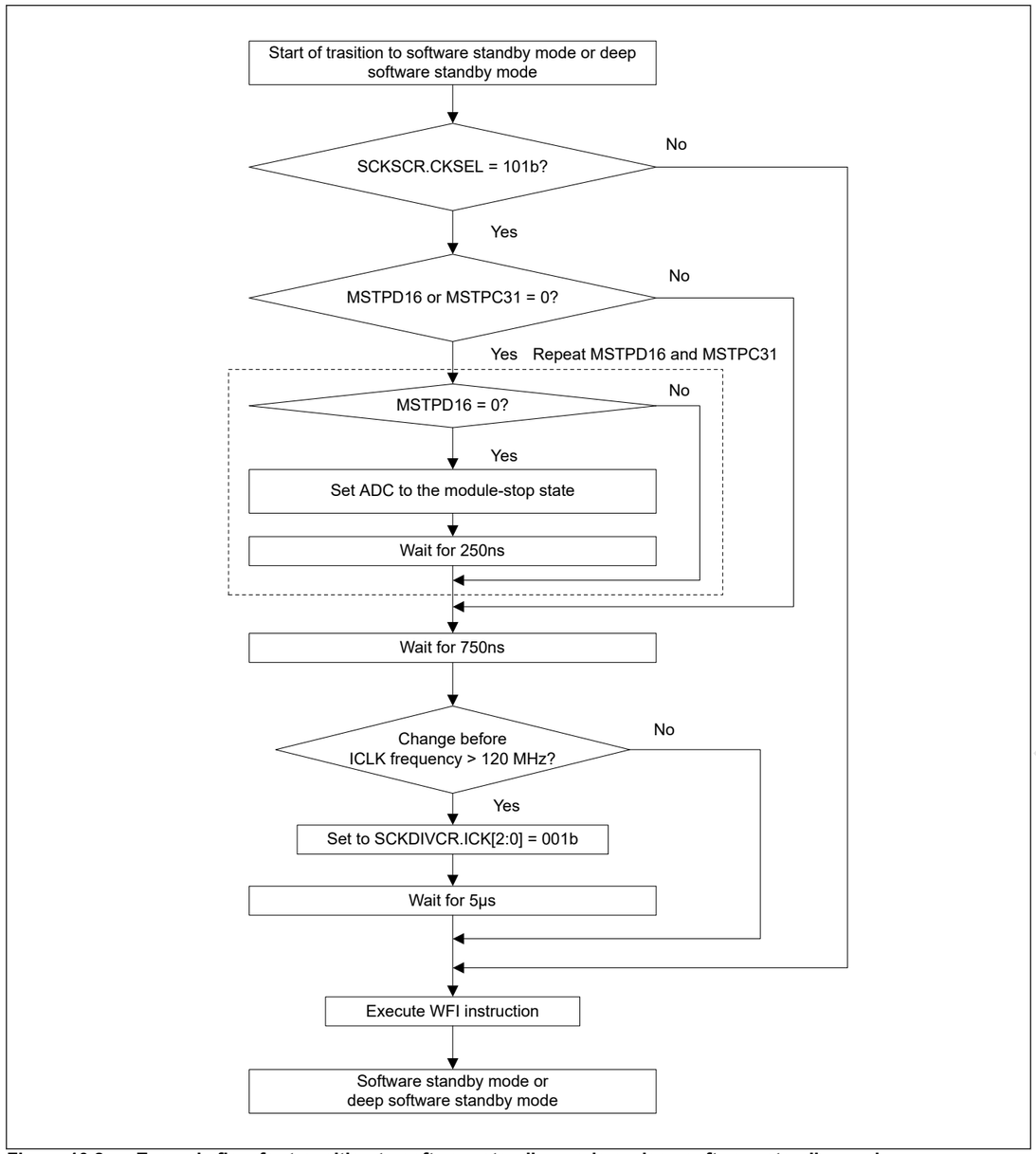


Figure 10.2 Example flow for transition to software standby mode or deep software standby mode

Table 10.6 shows the setting of the related control bits and the modes to enter after executing WFI instruction.

Table 10.6 Bit settings that affect modes when executing a WFI instruction (1 of 2)

		SBYCR.SSBY and PSBYCR.DPSBY bit settings			
		SSBY = 0, DPSBY = 0	SSBY = 0, DPSBY = 1	SSBY = 1, DPSBY = 0	SSBY = 1, DPSBY = 1
OSTDCR.OSTDE	0	Sleep	Sleep	Software Standby	Deep Software Standby
	1			Sleep	Sleep

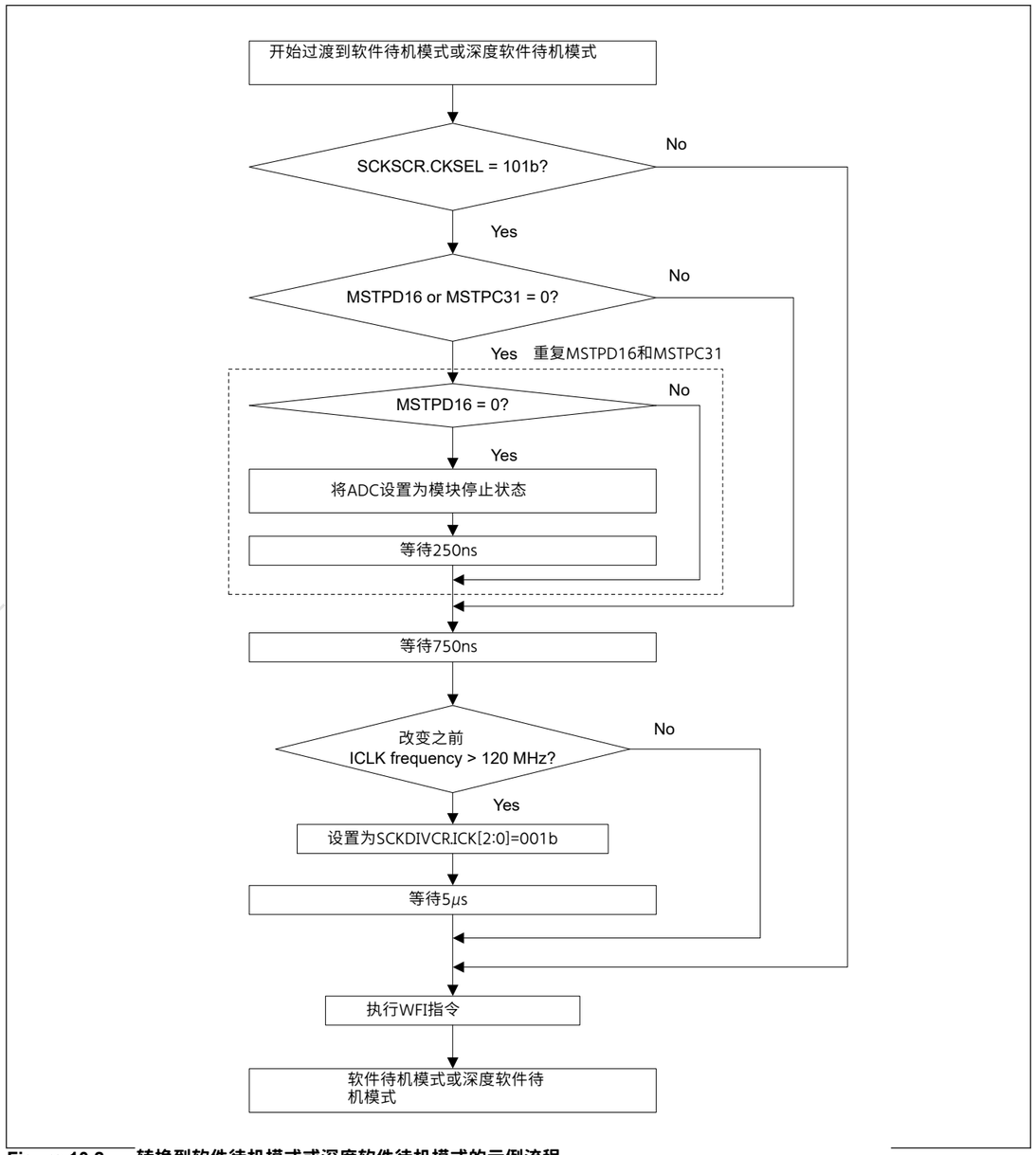


Figure 10.2 转换到软件待机模式或深度软件待机模式的示例流程

表10.6显示了相关控制位的设置以及执行WFI指令后进入的模式。

Table 10.6 执行WFI指令时影响模式的位设置(1of2)

		SBYCR.SSBY和PSBYCR.DPSBY位设置			
		SSBY = 0, DPSBY = 0	SSBY = 0, DPSBY = 1	SSBY = 1, DPSBY = 0	SSBY = 1, DPSBY = 1
OSTDCR.OSTDE	0	Sleep	Sleep	软件待机	深度软件待机
	1			Sleep	Sleep

Table 10.6 Bit settings that affect modes when executing a WFI instruction (2 of 2)

		SBYCR.SSBY and PSBYCR.DPSBY bit settings			
		SSBY = 0, DPSBY = 0	SSBY = 0, DPSBY = 1	SSBY = 1, DPSBY = 0	SSBY = 1, DPSBY = 1
FENTRYR.FENTRYC FENTRYR.FENTRYD	0	Sleep	Sleep	Software Standby	Deep Software Standby
	1			Sleep	Sleep
OFS0.IWDTSTPCTL	0	Sleep	Sleep	Software Standby	Software Standby
	1				Deep Software Standby
LVD1CR0.RI	0	Sleep	Sleep	Software Standby	Deep Software Standby
	1				Software Standby
LVD2CR0.RI	0	Sleep	Sleep	Software Standby	Deep Software Standby
	1				Software Standby

10.7.2 Canceling Software Standby Mode

Software Standby mode is canceled by:

- An available interrupt shown in Table 10.3
- A RES pin reset
- A power-on reset
- A voltage monitor reset
- A reset caused by an IWDT underflow.

On exiting Software Standby mode, the oscillators that operate before the transition to the mode restart. After all the oscillators are stabilized, the MCU returns to Normal mode from Software Standby mode. See section 12.2.17. WUPEN0 : Wake Up Interrupt Enable Register 0 for information on how to wake up the MCU from Software Standby mode.

You can cancel Software Standby mode in any of the following ways:

1. Canceling by an interrupt
   When an available interrupt request (see Table 10.3) is generated, an oscillator that operates before the transition to Software Standby mode restarts. After all the oscillators are stabilized, the MCU returns to Normal mode from Software Standby mode and starts the interrupt handling.
   When the PLL is selected as the clock source, you must insert a wait time of at least 250 ns at the beginning of the interrupt handling. The recommended method to measure the wait time is through software.
   Be sure to consider the worst-case conditions to ensure that the required wait time elapses.

Table 10.6 执行WFI指令时影响模式的位设置(2of2)

		SBYCR.SSBY和PSBYCR.DPSBY位设置			
		SSBY = 0, DPSBY = 0	SSBY = 0, DPSBY = 1	SSBY = 1, DPSBY = 0	SSBY = 1, DPSBY = 1
FENTRYR.FENTRYC FENTRYR.FENTRYD	0	Sleep	Sleep	软件待机	深度软件待机
	1			Sleep	Sleep
OFS0.IWDTSTPCTL	0	Sleep	Sleep	软件待机	软件待机
	1				深度软件待机
LVD1CR0.RI	0	Sleep	Sleep	软件待机	深度软件待机
	1				软件待机
LVD2CR0.RI	0	Sleep	Sleep	软件待机	深度软件待机
	1				软件待机

10.7.2 取消软件待机模式

软件待机模式通过以下方式取消：

●可用中断如表10.3所示

●ARES引脚复位

- A power-on reset

●电压监视器复位

●IWDT下溢引起的复位。

在退出软件待机模式时，在转换到模式之前工作的振荡器会重新启动。在所有振荡器稳定后，MCU从软件待机模式返回到正常模式。请参阅第12.2.17节。WUPEN0：唤醒中断使能寄存器0，了解如何将MCU从软件待机模式唤醒。

您可以通过以下任一方式取消软件待机模式：

1.中断取消
   当一个可用的中断请求（见表10.3）产生时，一个振荡器在转换到
   软件待机模式重新启动。在所有振荡器稳定后，MCU从软件返回到正常模式
   待机模式并启动中断处理。
   WhenthePLLisselectedastheclocksource youmustinsertawaittimeofatleast250nsatthebeginningoftheint errupthandling.测量等待时间的推荐方法是通过软件。请务必考虑最坏情况，以确保经过所需的等待时间。

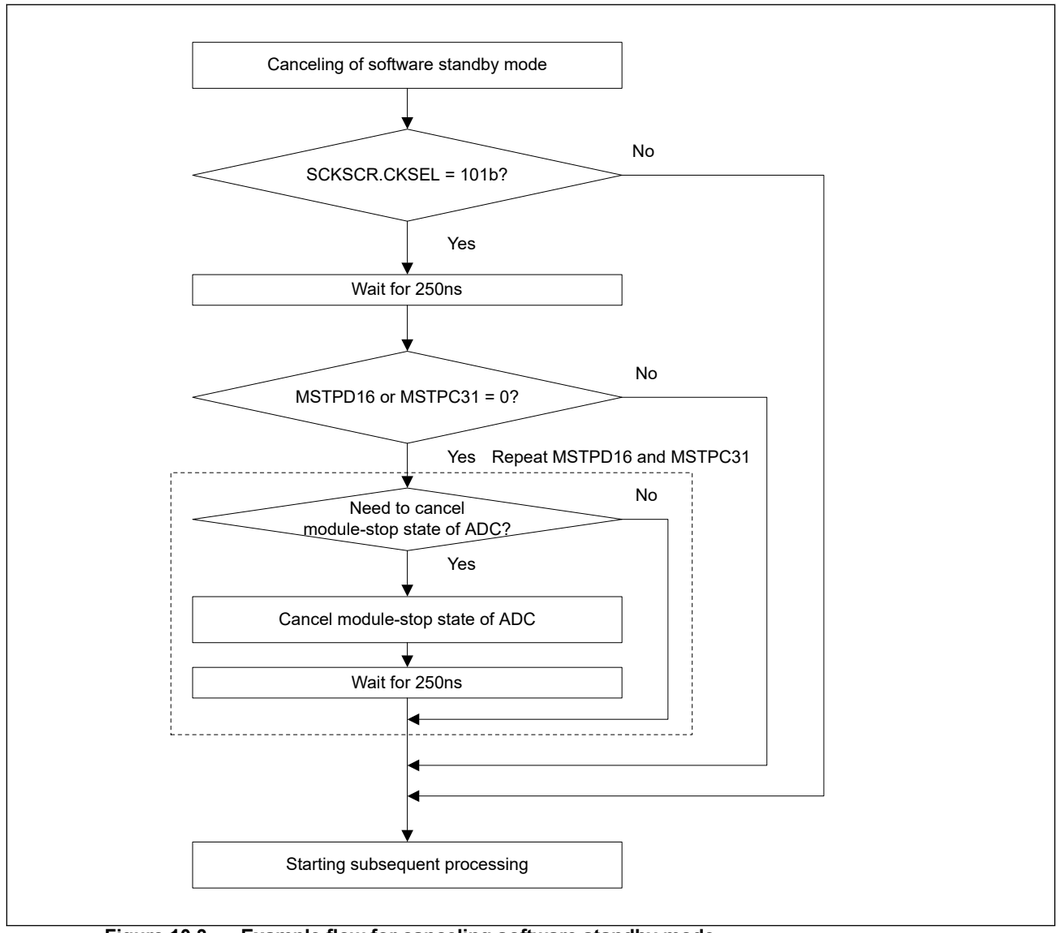


Figure 10.3 Example flow for canceling software standby mode

2. Canceling by a RES pin reset
   When the RES pin is driven low, the MCU enters the reset state, and the oscillators whose default status is operating, start the oscillation. Be sure to keep the RES pin low for the time period specified in section 46, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts the reset exception handling.
3. Canceling by a power-on reset
   Software Standby mode is canceled by a power-on reset and the MCU starts the reset exception handling.
4. Canceling by a voltage monitor reset
   Software Standby mode is canceled by a voltage monitor reset from the voltage detection circuit and the MCU starts the reset exception handling.
5. Canceling by IWDT reset
   Software Standby mode is canceled by an internal reset generated by an IWDT underflow and the MCU starts the reset exception handling. However, IWDT stops in Software Standby mode and an internal reset for canceling Software Standby mode is not generated in the following condition:
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.

10.7.3 Example of Software Standby Mode Application

Figure 10.4 shows an example of entry to Software Standby mode on detection of a falling edge of the IRQn pin, and exit from Software Standby mode by a rising edge of the IRQn pin.

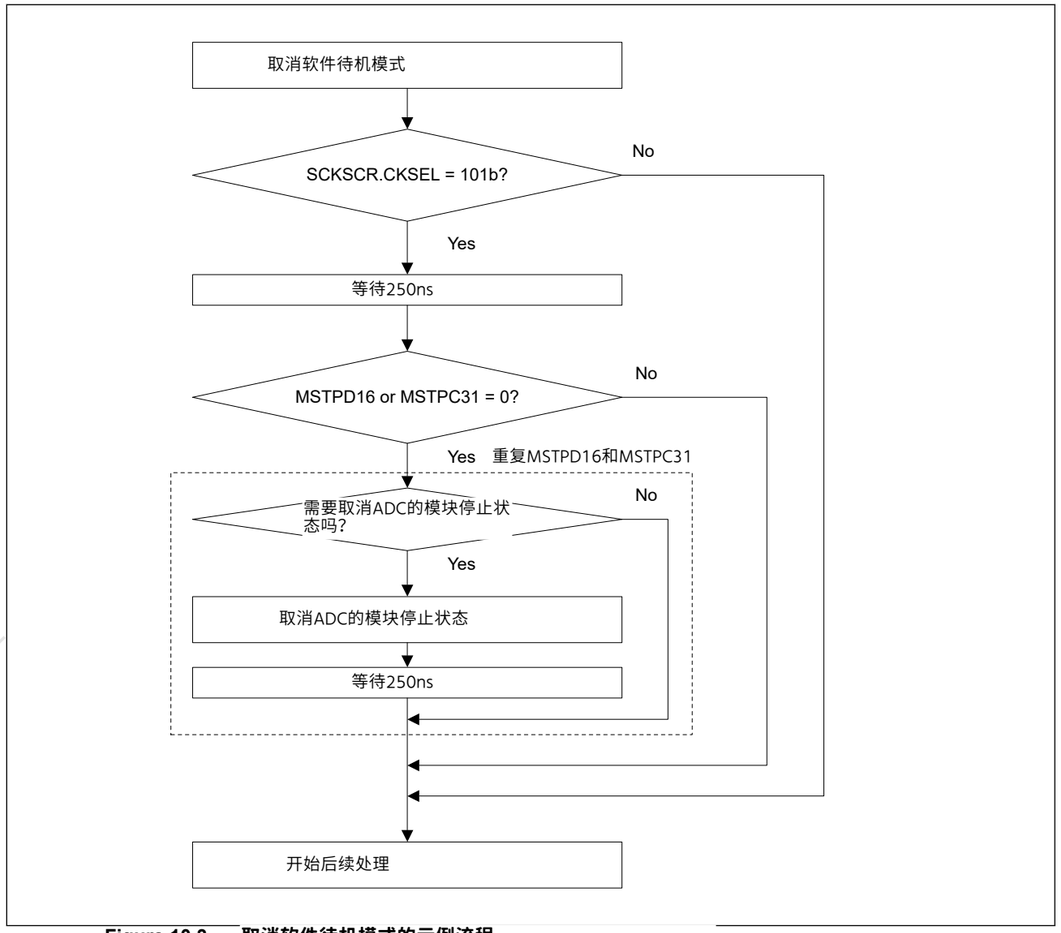


Figure 10.3 取消软件待机模式的示例流程

2.通过RES引脚复位取消
当RES引脚驱动为低电平时，MCU进入复位状态，默认状态为工作的振荡器开始振荡。请务必在第46节“电气特性”中指定的时间段内保持RES引脚为低电平。当RES引脚在指定时间后被驱动为高电平时，CPU开始复位异常处理。

3.上电复位取消
软件待机模式通过上电复位取消，MCU启动复位异常处理。

4.通过电压监视器复位取消
软件待机模式通过电压检测电路的电压监视器复位取消，MCU开始复位异常处理。

5.IWDT复位取消
软件待机模式由IWDT下溢产生的内部复位取消，MCU开始复位异常处理。但是，IWDT在软件待机模式下停止，并且在以下情况下不会产生用于取消软件待机模式的内部复位：

- OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.

10.7.3 软件待机模式应用示例

图10.4显示了在检测到IRQn引脚的下降沿进入软件待机模式并在IRQn引脚的上升沿退出软件待机模式的示例。

In this example, an IRQn pin interrupt is accepted with the IRQCRi.IRQMD[1:0] bits of the ICU set to 00b (falling edge) in Normal mode, and the IRQCRi.IRQMD[1:0] bits are set to 01b (rising edge). After that, the SBYCR.SSBY bit is set to 1 and a WFI instruction is executed. As a result, entry to Software Standby mode completes and exit from Software Standby mode is initiated by a rising edge of the IRQn pin.

Setting the ICU is also required to exit Software Standby mode. For details, see section 12, Interrupt Controller Unit (ICU). The oscillation stabilization time in Figure 10.4 is specified in section 46, Electrical Characteristics.

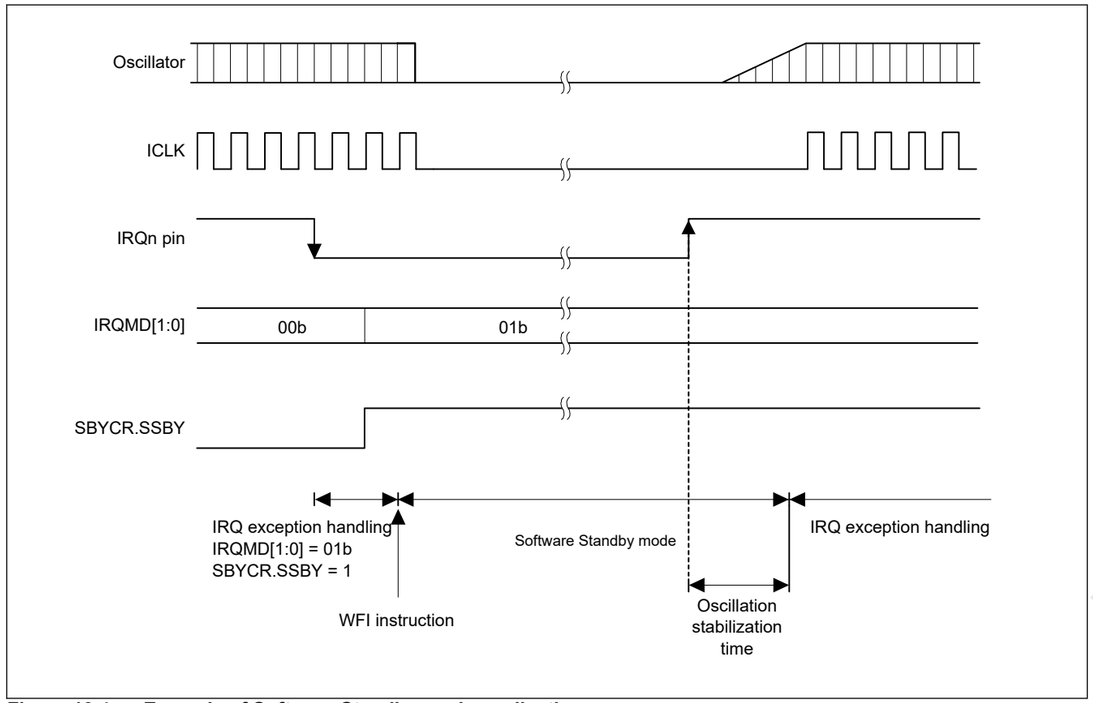


Figure 10.4 Example of Software Standby mode application

10.8 Snooze Mode

10.8.1 Transition to Snooze Mode

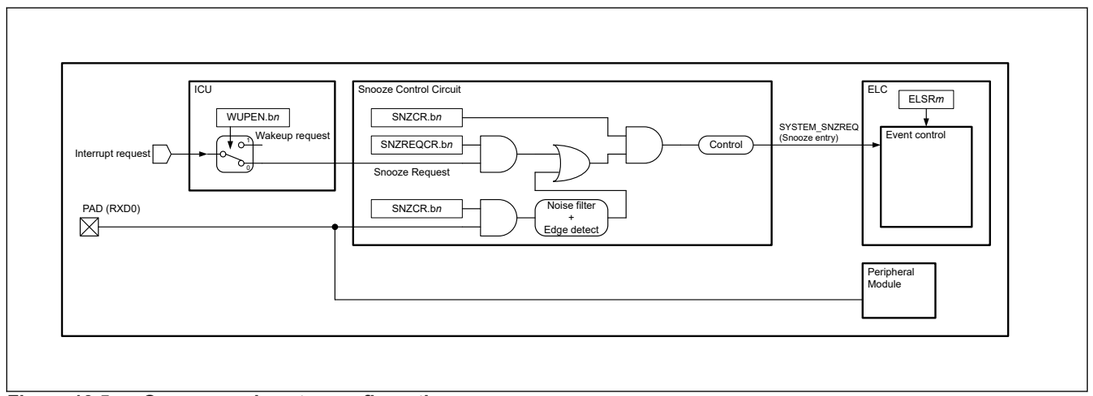


Figure 10.5 Snooze mode entry configuration

在此示例中，接受IRQn引脚中断，同时ICU的IRQCRi.IRQMD[1:0]位设置为00b（下降沿）正常模式，并且IRQCRi.IRQMD[1:0]位设置为01b（上升沿）。之后，SBYCR.SSBY位设置为1并执行WFI指令。因此，软件待机模式的进入完成，软件待机模式的退出由IRQn引脚的上升沿启动。

退出软件待机模式也需要设置ICU。有关详细信息，请参阅第12节，中断控制器单元(ICU)。图10.4中的振荡稳定时间在第46节"电气特性"中指定。

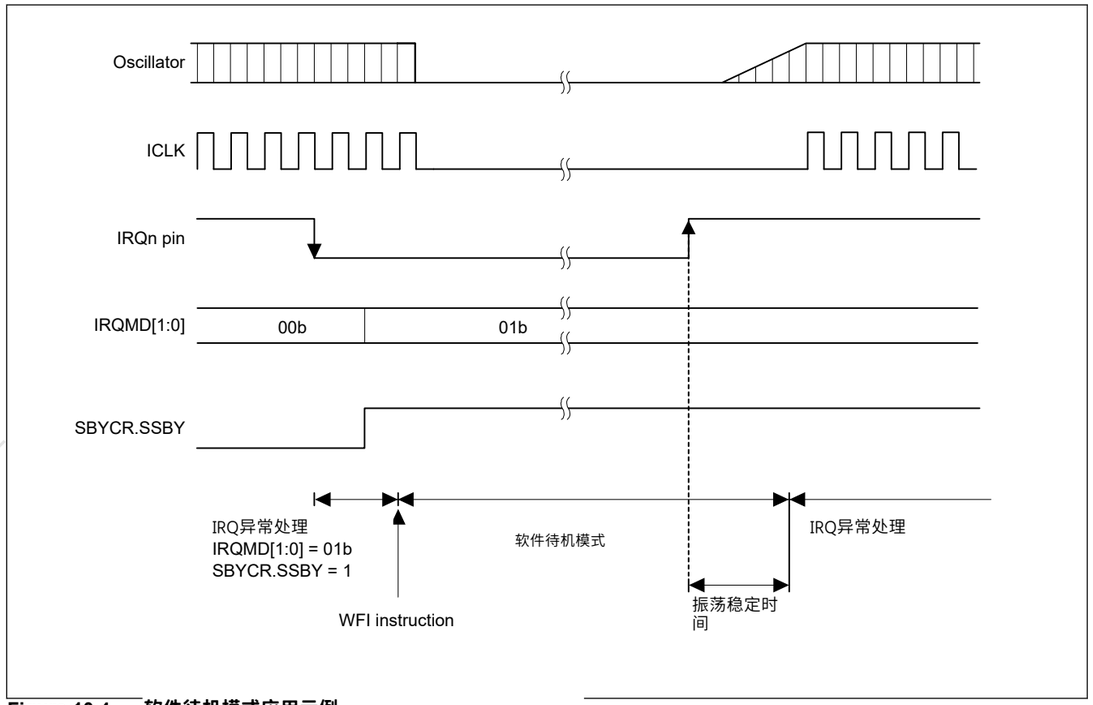


Figure 10.4 软件待机模式应用示例

10.8 贪睡模式

10.8.1 过渡到贪睡模式

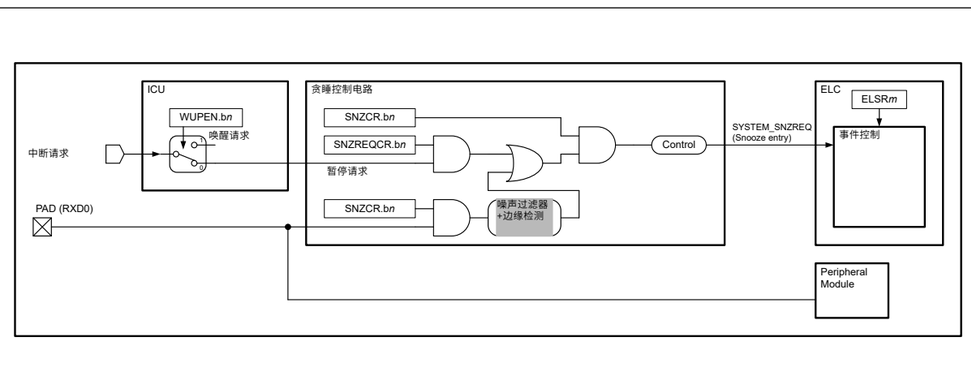


Figure 10.5 贪睡模式进入配置

When the snooze control circuit accepts an available snooze request in Software Standby mode, the MCU transfers to Snooze mode. In this mode, some peripheral modules operates without waking the CPU. The peripheral modules that can operate in Snooze mode are shown in Table 10.2. Also, DTC operation in Snooze mode can be selected by the setting of SNZCR.SNZDTCEN bit.

Table 10.7 shows the Snooze requests that switch the MCU from Software Standby mode to Snooze mode. To use the listed Snooze requests as a trigger to switch to Snooze mode, the corresponding SNZREQENn bit of the SNZREQCR0 register or RXDREQEN bit of SNZCR register must be set before entering Software Standby mode.

Table 10.7 Available snooze requests to switch to Snooze mode

Snooze request	Control Register	
	Register	Bit*1
PORT_IRQn (n = 0 to 15)	SNZREQCR0	SNZREQENn (n = 0 to 15)
KEY_INTKR	SNZREQCR0	SNZREQEN17
AGT1_AGTI	SNZREQCR0	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR0	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR0	SNZREQEN30
RXD0 falling edge	SNZCR	RXDREQEN*2

Note 1. Do not enable multiple snooze requests at the same time.
Note 2. Do not set the RXDREQEN bit to 1 except in asynchronous mode.

Clear the DMAST.DMST and DTCST.DTCST bits to 0 before executing a WFI instruction, except when using the DTC in Snooze mode. If the DTC is required in Snooze mode, set the DTCST.DTCST bit to 1 before executing a WFI instruction.

10.8.2 Canceling Snooze Mode

Snooze mode is canceled by an interrupt request that is available in Software Standby mode or a reset. Table 10.3 shows the requests that can be used to exit each mode. After canceling the Snooze mode, the MCU enters Normal mode and proceeds with exception processing for the given interrupt or reset. The action triggered by the interrupt requests, selected in SELSR0, cancels Snooze mode. Interrupt canceling Snooze mode must be selected in IELSRn to link to the NVIC for the corresponding interrupt handling. See section 12, Interrupt Controller Unit (ICU) for information on SELSR0 and IELSRn registers.

当贪睡控制电路在软件待机模式下接受一个可用的贪睡请求时，MCU转移到贪睡模式。在这种模式下，一些外围模块在不唤醒CPU的情况下运行。可在贪睡模式下运行的外围模块如表10.2所示。此外，可以通过设置SNZCR.SNZDTCEN位来选择贪睡模式下的DTC操作。

表10.7显示了将MCU从软件待机模式切换到贪睡模式的贪睡请求。要使用列出的贪睡请求作为切换到贪睡模式的触发器，SNZREQCR0寄存器的相应SNZREQENn位或
在进入软件待机模式之前，必须设置SNZCR寄存器的RXDREQEN位。

Table 10.7 可用的贪睡请求以切换到贪睡模式

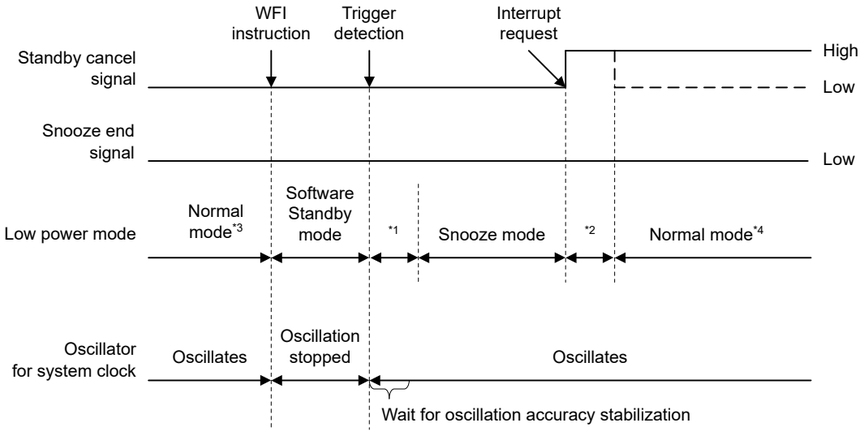
暂停请求	控制寄存器	
	Register	Bit*1
PORT_IRQn (n = 0 to 15)	SNZREQCR0	SNZREQENn (n = 0 to 15)
KEY_INTKR	SNZREQCR0	SNZREQEN17
AGT1_AGTI	SNZREQCR0	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR0	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR0	SNZREQEN30
RXD0下降沿	SNZCR	RXDREQEN*2

注意1.不要同时启用多个贪睡请求。
注2.除异步模式外，请勿将RXDREQEN位设置为1。

在执行WFI指令之前将DMAST.DMST和DTCST.DTCST位清零，除非在贪睡模式下使用DTC。如果在贪睡模式下需要DTC，请在执行WFI指令之前将DTCST.DTCST位设置为1。

10.8.2 取消贪睡模式

贪睡模式由软件待机模式下可用的中断请求或复位取消。表10.3显示了可用于退出每种模式的请求。取消贪睡模式后，MCU进入正常模式并继续对给定中断或复位进行异常处理。在SELSR0中选择的中断请求触发的动作取消贪睡模式。必须在IELSRn中选择中断取消贪睡模式以链接到NVIC以进行相应的中断处理。有关SELSR0和IELSRn寄存器的信息，请参见第12节，中断控制器单元(ICU)。



Note 1. Transition time from Software Standby mode to Snooze mode.
Note 2. Transition time from Snooze mode to Normal mode.
Note 3. Enable Snooze mode (SNZCR.SNZE = 1) immediately before switching to Software Standby mode.
Note 4. Disable Snooze mode (SNZCR.SNZE = 0) immediately after returning to Normal mode.

Figure 10.6 Canceling of Snooze mode when an interrupt request signal is generated

10.8.3 Returning from Snooze Mode to Software Standby Mode

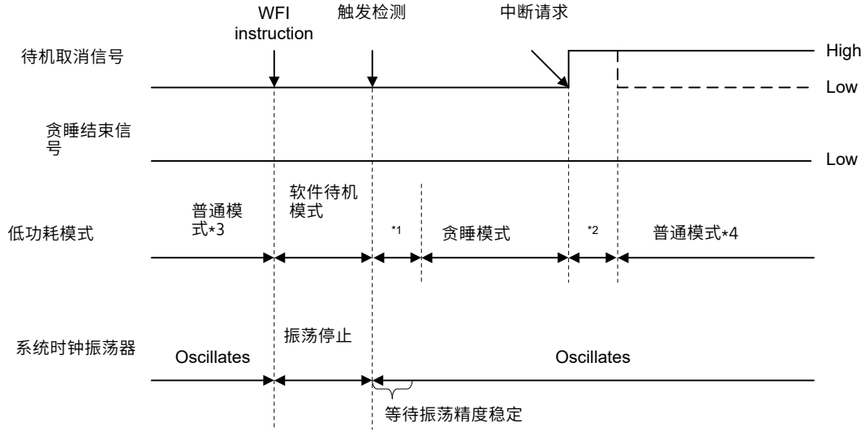
Table 10.8 shows the snooze end request that can be used as triggers to return to Software Standby mode. The snooze end requests are available only in Snooze mode. If the requests are generated when the MCU is not in Snooze mode, they are ignored. When multiple requests are selected, each of the requests invokes transition to Software Standby mode from Snooze mode.

Table 10.9 shows the snooze end conditions that consist of the snooze end requests and the conditions of the peripheral modules. The SCI0, ADC, and DTC modules can keep the MCU in Snooze mode until they complete the operation. However, an AGTn (n = 1) underflow as a trigger to return to Software Standby mode cancels Snooze mode without waiting for the completion of SCI0 operation.

Figure 10.7 shows the timing diagram for the transition from Snooze mode to Software Standby mode. This mode transition occurs according to which snooze end requests are set in the SNZEDCR0 register. A snooze request is cleared automatically after returning to Software Standby mode.

Table 10.8 Available snooze end requests (triggers to return to Software Standby mode)

Peripheral Module	Snooze end request	Enable/Disable Control	
		Register	Symbol
AGT1	AGT1 underflow (AGT1_AGTI)	SNZEDCR0	AGTUNFED
DTC	Last DTC transmission completion (DTC_COMPLETE)	SNZEDCR0	DTCZRED
DTC	Not Last DTC Transmission Completion (DTC_TRANSFER)	SNZEDCR0	DTCNZRED
ADC	Composite compare match 0 (ADC_CCMPM0)	SNZEDCR0	AD0MATED
ADC	Composite compare match 1 (ADC_CCMPM1)	SNZEDCR0	AD1MATED
SCI0	SCI0 address mismatch (SCI0_DCUF)	SNZEDCR0	SCI0UMTED



注1.从软件待机模式到贪睡模式的转换时间。
注2.从贪睡模式到正常模式的转换时间。
注3.在切换到软件待机模式之前立即启用贪睡模式(SNZCR.SNZE=1)。
注4.返回正常模式后立即禁用贪睡模式(SNZCR.SNZE=0)。

Figure 10.6 产生中断请求信号时取消贪睡模式

10.8.3 从贪睡模式返回到软件待机模式

表10.8显示了可用作返回到软件待机模式的触发器的贪睡结束请求。贪睡结束请求仅在贪睡模式下可用。如果请求是在MCU未处于贪睡模式时生成的，则它们将被忽略。选择多个请求时，每个请求都会从贪睡模式转移到软件待机模式。

表10.9显示了贪睡结束条件，包括贪睡结束请求和外围模块的条件。SCI0、ADC和DTC模块可以使MCU保持在贪睡模式，直到它们完成操作。然而，作为返回软件待机模式的触发的AGTn(n=1)下溢会取消贪睡模式，而无需等待SCI0操作完成。

图10.7显示了从贪睡模式转换到软件待机模式的时序图。该模式转换根据SNZEDCR0寄存器中设置的贪睡结束请求发生。返回软件待机模式后，贪睡请求会自动清除。

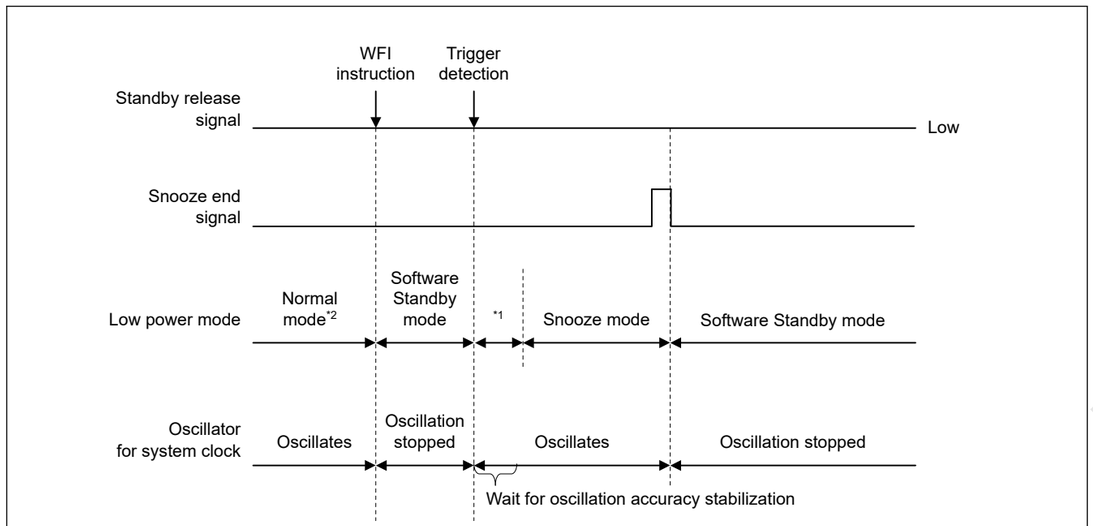
Table 10.8 可用的暂停结束请求（触发返回到软件待机模式）

Peripheral Module	暂停结束请求	Enable/Disable Control	
		Register	Symbol
AGT1	AGT1 underflow (AGT1_AGTI)	SNZEDCR0	AGTUNFED
DTC	上次DTC传输完成(DTC_COMPLETE)	SNZEDCR0	DTCZRED
DTC	不是最后一个DTC传输完成(DTC_TRANSFER)	SNZEDCR0	DTCNZRED
ADC	复合比较匹配0(ADC_CCMPM0)	SNZEDCR0	AD0MATED
ADC	复合比较匹配1(ADC_CCMPM1)	SNZEDCR0	AD1MATED
SCI0	SCI0地址不匹配(SCI0_DCUF)	SNZEDCR0	SCI0UMTED

Table 10.9 Snooze end conditions

Operating module when a snooze end request occurs	Snooze end request	
	AGT1 underflow	Other than AGT1 underflow
DTC	The MCU transfers to the Software Standby mode after all of the modules listed in this table complete operation.	The MCU transfers to the Software Standby mode after all of the modules listed to the left of this column complete the operation.
ADC		
SCI0	The MCU transfers to the Software Standby mode immediately after the snooze end request is generated.	
Other than specified	The MCU transfers to the Software Standby mode immediately after a snooze end request is generated.	

Note: If the DTC is used to activate the ADC, or SCI, the MCU transitions to Software Standby mode immediately after a snooze end request is generated.



Note 1. Transition time from Software Standby mode to Snooze mode.
Note 2. Enable Snooze mode (SNZCR.SNZE = 1) immediately before switching to Software Standby mode.

Figure 10.7 Canceling of Snooze mode when an interrupt request signal is not generated

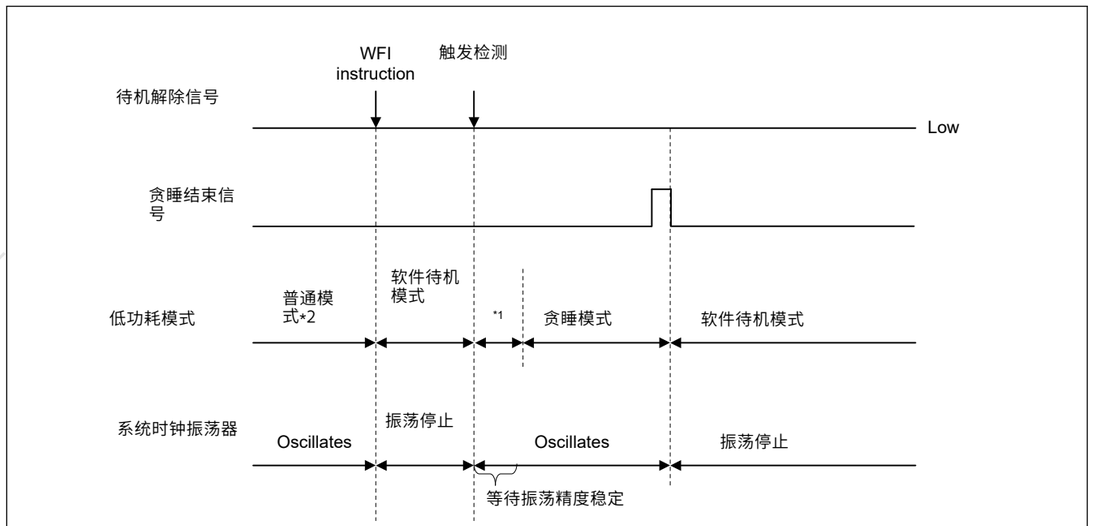
10.8.4 Snooze Operation Example

Figure 10.8 shows an example setting for using ELC in Snooze mode.

Table 10.9 暂停结束条件

发生贪睡结束请求时的操作模块	暂停结束请求	
	AGT1 underflow	除了AGT1下溢
DTC	在此表中列出的所有模块完成操作后，MCU将进入软件待机模式。	在此列左侧列出的所有模块完成操作后，MCU将进入软件待机模式。
ADC		
SCI0	产生贪睡结束请求后，MCU立即进入软件待机模式。	
指定以外的	产生贪睡结束请求后，MCU立即转入软件待机模式。	

Note: 如果DTC用于激活ADC或SCI，则MCU在产生贪睡结束请求后立即转换到软件待机模式。

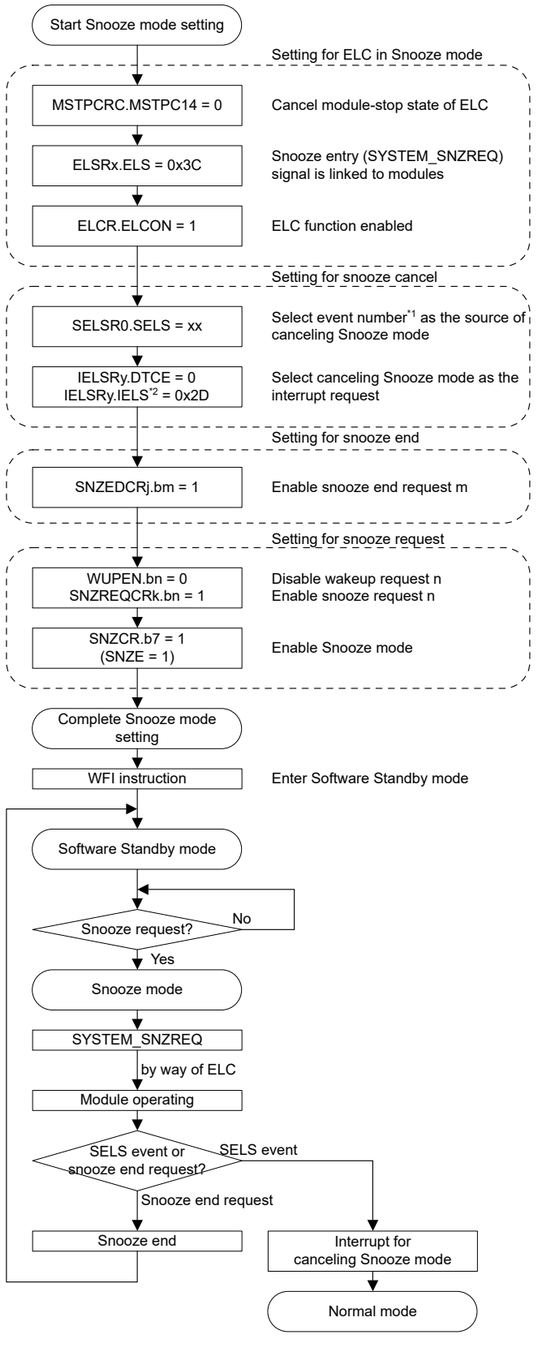


注1.从软件待机模式到贪睡模式的转换时间。
注2.在切换到软件待机模式之前立即启用贪睡模式(SNZCR.SNZE=1)。

Figure 10.7 未产生中断请求信号时取消贪睡模式

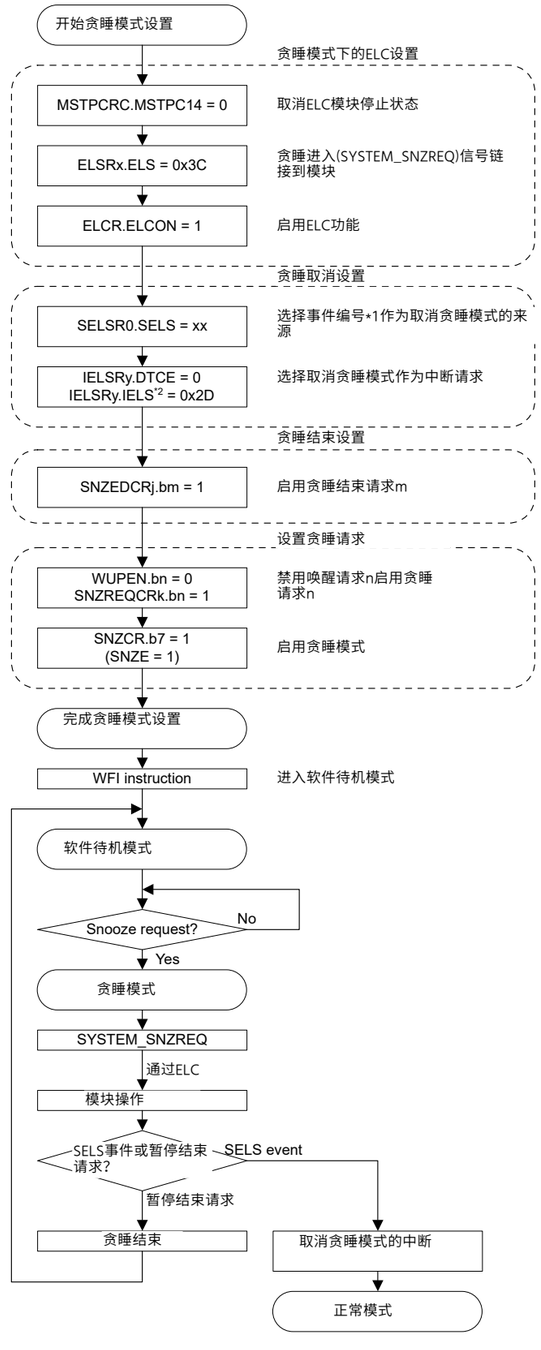
10.8.4 贪睡操作示例

图10.8显示了在贪睡模式下使用ELC的示例设置。



Note 1. See Table 12.4

Figure 10.8 Setting example of using ELC in Snooze mode



注1.见表12.4

Figure 10.8 在贪睡模式下使用ELC的设置示例

The MCU can transmit and receive data in SCI0 asynchronous mode without CPU intervention. When using the SCI0 in Snooze mode, use either High-speed mode or Low-speed mode.

Table 10.10 shows the maximum transfer rate of SCI0 in Snooze mode.

Table 10.10 HOCO: ± 1.4% (Ta = -20° to 105°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and TRCLK	HOCO frequency					
	LOCO is not operating			LOCO is operating		
	16 MHz	18 MHz	20 MHz	16 MHz	18 MHz	20 MHz
1	2400			4800		
2						
4						
8						
16						
32	1200			2400		
64						

When using SCI0 in Snooze mode, use the following setting: BGDM = 0, ABCS = 0, ABCSE = 0. See section 26, Serial Communications Interface (SCI) for information on these bits.

Figure 10.9 shows a setting example for using SCI0 in Snooze mode entry.

MCU可以在SCI0异步模式下发送和接收数据，无需CPU干预。在使用SCI0时贪睡模式，使用高速模式或低速模式。

表10.10显示了Snooze模式下SCI0的最大传输速率。

Table 10.10 HOCO: ± 1.4% (Ta = -20° to 105°C) (Unit: bps)

ICLK、PCLKA、PCLKB、PCLKC的最大分频比，PCLKD, FCLK, and TRCLK	HOCO frequency					
	LOCO没有运行			LOCO正在运营		
	16 MHz	18 MHz	20 MHz	16 MHz	18 MHz	20 MHz
1	2400			4800		
2						
4						
8						
16						
32	1200			2400		
64						

在贪睡模式下使用SCI0时，使用以下设置：BGDM=0，ABCS=0，ABCSE=0。参见第26节，串行通信接口(SCI)以获取有关这些位的信息。

图10.9显示了在贪睡模式进入中使用SCI0的设置示例。

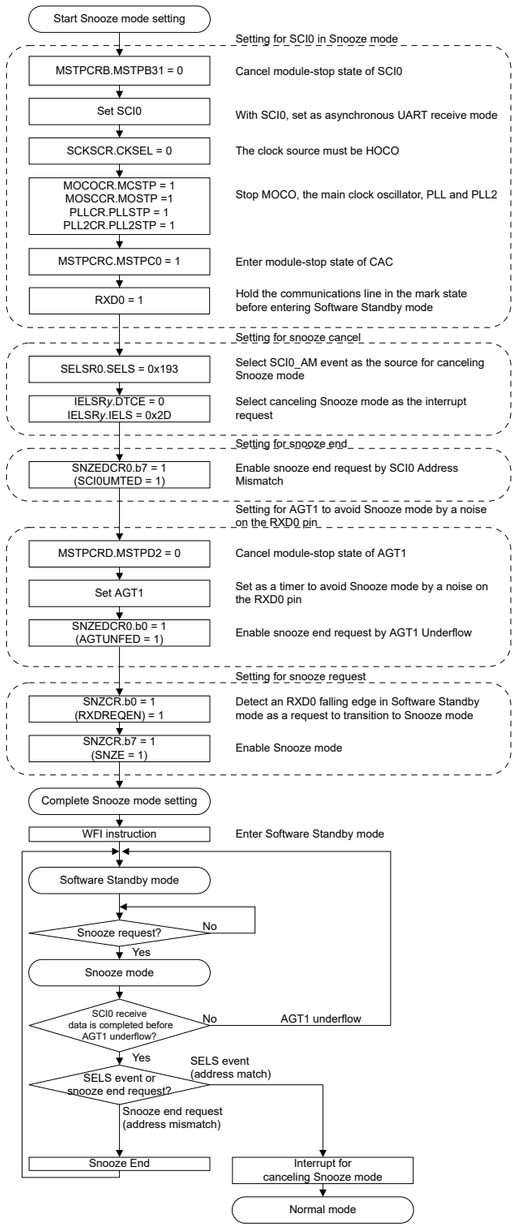


Figure 10.9 Setting example of using SCI0 in Snooze mode entry

10.9 Deep Software Standby Mode

10.9.1 Transitioning to Deep Software Standby Mode

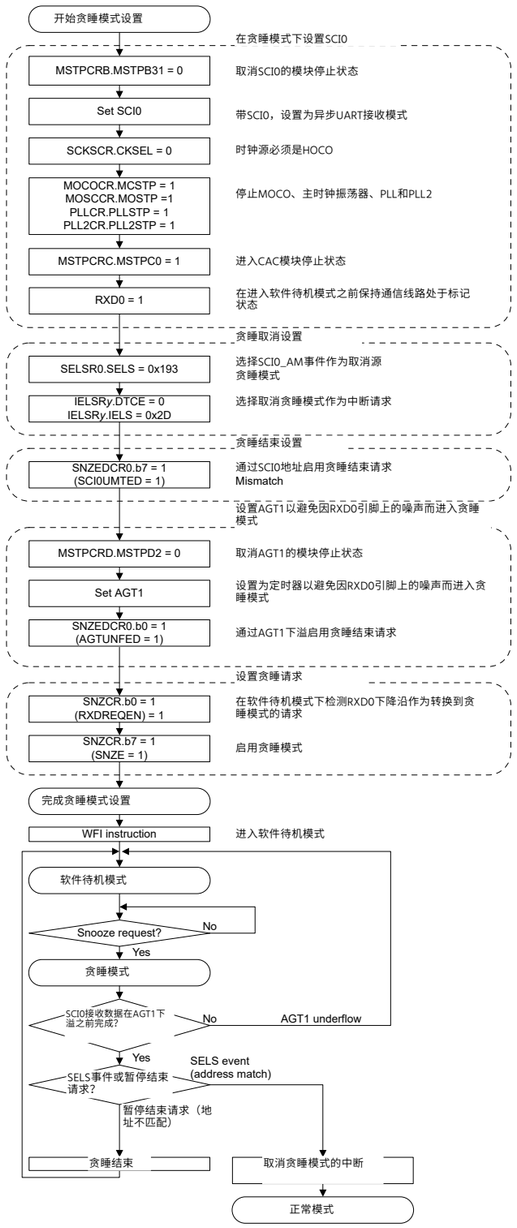


Figure 10.9 在Snooze模式进入使用SCI0的设置示例

10.9 深度软件待机模式

10.9.1 过渡到深度软件待机模式

When a WFI instruction is executed with the SBYCR.SSBY and DPSBYCR.DPSBY bits set to 1, the MCU enters Deep Software Standby mode. See Table 10.6 for the setting of the related control bits. In this mode, the CPU, on-chip peripheral functions, SRAM (except for standby RAM), and all oscillators (except for Low-speed on-chip oscillator) are stopped. Also because the internal power supply to these modules is stopped, power consumption is remarkably reduced. The contents of all CPU registers and internal peripheral modules become undefined.

Data in the standby SRAM are preserved if the setting of the DEEPCUT[1:0] bits are 00b. If the setting of the DEEPCUT[1:0] bits are 01b, the internal power supply to the standby SRAM is cut off, reducing power consumption. Data in the standby SRAM becomes undefined at this time. If the setting of the DEEPCUT[1:0] bits are 11b, the internal power supply to the standby SRAM is cut off, the LVD is stopped, and the low-power-consumption function of the power-on reset circuit is enabled, so power consumption is further reduced. For details, see section 46, Electrical Characteristics.

When the MCU enters Deep Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1, power supply to the IWDT-dedicated clock and the IWDT is cut off, and counting by the IWDT stops.

When OFS0.IWDTSTPCTL bit is 0, the MCU enters Software Standby mode instead of Deep Software Standby mode, regardless of the setting of OFS0.IWDTSTRT bit or DPSBYCR.DPSBY bit. If OFS0.IWDTSTPCTL bit is 0 while OFS0.IWDTSTRT bit is 0 (auto start mode), IWDT-dedicated clock and IWDT continues the operation.

When LVD1CR0.RI = 1 (voltage monitor 1 reset selected) or LVD2CR0.RI = 1 (voltage monitor 2 reset selected), the MCU enters Software Standby mode instead of Deep Software Standby mode. The I/O port states are the same as in Software Standby mode.

When the PLL is selected as the clock source, set the following modules to the module-stop state before executing a WFI instruction:

ADC, SCE5.

In this case, wait for least 750 ns and if the ICLK frequency before executing the WFI instruction exceeds 120 MHz, it is necessary to set the ICLK frequency division ratio to 1/2 and wait 5 µs. Measurement of the waiting time, it is recommended the measurement by the software. If you use the timer, regardless of the use conditions, ensure that the waiting time has elapsed.

See Figure 10.2 for Example flow for transition to software standby mode or deep software standby mode.

Note: Conditions on the DTC, DMAC, and IWDT for transitioning to Software Standby mode should be met before the WFI instruction is executed. For details, see section 10.7. Software Standby Mode.

10.9.2 Cancelling Deep Software Standby Mode

Deep Software Standby mode is canceled by:

- An interrupt shown in Table 10.3
- A RES pin reset
- A power-on reset
- A voltage monitor 0 reset.

(1) Cancelling by an interrupt

Cancelling by interrupts is controlled by DPSIERn (n = 0 to 2) and DPSIFRn (n = 0 to 2). When a Deep Software Standby Cancelling interrupt is generated, the corresponding flag in DPSIFRn is set to 1. If the interrupt is enabled in DPSIERn, Deep Software Standby mode is canceled. Rising edge or falling edge can be selected by DPSIEGRn (n = 0 to 2). The interrupts for which an edge can be selected are the NMI, IRQn-DS (n = 0 to 15), voltage monitor 1, and voltage monitor 2 interrupts. When a Deep Software Standby mode canceling request occurs, the internal power is supplied and MOCO starts oscillating, and an internal reset (Deep Software Standby reset) is generated for the entire MCU.

The stable MOCO clock is supplied to the entire MCU and Deep Software Standby reset is canceled. The MCU starts reset exception handling.

When Deep Software Standby mode is canceled by an external interrupt pin or internal interrupt signal, the RSTSR0.DPSRSTF flag is set to 1.

当在SBYCR.SSBY和DPSBYCR.DPSBY位设置为1的情况下执行WFI指令时，MCU进入Deep
软件待机模式。相关控制位的设置见表10.6。在此模式下，CPU、片上外围功能、SRAM（除了待机RAM）和所有振荡器（除了低速片上振荡器）都停止。此外，由于这些模块的内部电源停止，功耗显着降低。所有CPU寄存器和内部外围模块的内容变为未定义。

如果DEEPCUT[1:0]位的设置为00b，则保留备用SRAM中的数据。如果设置
DEEPCUT[1:0]位为01b，内部对待机SRAM的供电被切断，降低了功耗。此时备用SRAM中的数据变为未定义。如果DEEPCUT[1:0]位设置为11b，则内部对备用SRAM的供电被切断，LVD停止，上电复位电路的低功耗功能被使能，因此功耗进一步降低。有关详细信息，请参见第46节，电气特性。

当MCU在IWDT处于自动启动模式且OFS0.IWDTSTPCTL位为1时进入深度软件待机模式时，IWDT专用时钟和IWDT的电源被切断，IWDT的计数停止。

当OFS0.IWDTSTPCTL位为0时，MCU进入软件待机模式而不是深度软件待机模式，无论OFS0.IWDTSTRT位或DPSBYCR.DPSBY位如何设置。如果OFS0.IWDTSTPCL位为0而OFS0.IWDTSTRT位为0（自动启动模式），IWDT专用时钟和IWDT继续运行。

当LVD1CR0.RI=1（选择电压监视器1复位）或LVD2CR0.RI=1（选择电压监视器2复位）时，MCU进入软件待机模式而不是深度软件待机模式。IO端口状态与软件待机模式相同。

WhenthePLLisselectedastheclocksource setthefollowingmodulestothemodule-stopstatebeforeexecutingaWFIinstruction:

ADC, SCE5.

在这种情况下，至少等待750ns，如果执行WFI指令前的ICLK频率超过120MHz，则需要将ICLK分频比设置为12并等待5µs。等待时间的测量，建议通过软件测量。如果您使用定时器，无论使用条件如何，请确保等待时间已过。

有关转换到软件待机模式或深度软件待机模式的示例流程，请参见图10.2。

Note: 在执行WFI指令之前，应满足DTC、DMAC和IWDT转换到软件待机模式的条件。有关详细信息，请参阅第10.7节。软件待机模式。

10.9.2 取消深度软件待机模式

深度软件待机模式通过以下方式取消：

●表10.3所示的中断

●ARES引脚复位

- A power-on reset

●电压监视器0复位。

(1) 通过中断取消

中断取消由DPSIERn(n=0到2)和DPSIFRn(n=0到2)控制。深度软件待机时
产生取消中断时，DPSIFRn中的相应标志置1。如果在DPSIERN中使能中断，
深度软件待机模式被取消。上升沿或下降沿可以通过DPSIEGRn(n=0到2)选择。可以选择边沿的中断是NMI、IRQn-DS（n=0到15）、电压监视器1和电压监视器2中断。当产生深度软件待机模式取消请求时，内部电源被提供，MOCO开始振荡，并为整个MCU产生内部复位（深度软件待机复位）。

为整个MCU提供稳定的MOCO时钟，并取消深度软件待机复位。MCU开始复位异常处理。

当深度软件待机模式被外部中断引脚或内部中断信号取消时，
RSTSR0.DPSRSTF标志设置为1。

(2) Cancelling by RES pin reset

When the RES pin is driven low, the MCU cancels Deep Software Standby mode and enters the reset state. Keep the RES pin low for the time specified in section 46, Electrical Characteristics. When RES pin is driven high after the specified time period, the CPU starts the reset exception handling.

(3) Cancelling by a power-on reset

Deep Software Standby mode is canceled by a power-on reset and the MCU starts the reset exception handling.

(4) Cancelling by a voltage monitor 0 reset

Deep Software Standby mode is canceled by a voltage monitor 0 reset from the voltage detection circuit and the MCU starts the reset exception handling.

10.9.3 Pin States when Deep Software Standby mode is Canceled

In Deep Software Standby mode, the I/O ports retain the same states from Software Standby mode. The MCU is initialized by an internal reset generated when Deep Software Standby mode is canceled, and reset exception handling starts immediately. The DPSBYCR.IOKEEP bit setting determines whether to initialize the I/O ports or to retain the I/O ports states for Software Standby mode. The following is the state of the I/O ports for each bit setting:

- When the DPSBYCR.IOKEEP bit = 0
  I/O ports are initialized by an internal reset generated when Deep Software Standby mode is canceled.
- When the DPSBYCR.IOKEEP bit = 1
  Although the MCU is initialized by an internal reset generated when Deep Software Standby mode is canceled, the I/O ports retain their states from Software Standby mode regardless of the MCU internal state. The I/O ports states remain unchanged from Software Standby mode even when settings are made to the I/O ports or peripheral modules. The retained I/O ports states are released by clearing the DPSBYCR.IOKEEP bit to 0, and the MCU operates according to the internal state. The DPSBYCR.IOKEEP bit is not initialized by any internal reset generated when Deep Software Standby mode is canceled.

10.9.4 Example of Deep Software Standby Mode Application

(1) Entering and exiting Deep Software Standby mode

Figure 10.10 shows an example where a transition to Deep Software Standby mode is made at the falling edge of the IRQn-DS pin, and exiting Deep Software Standby mode is made at the rising edge of the IRQn-DS pin. In this example, an IRQn interrupt is accepted with the IRQCRi.IRQMD[1:0] bits of the ICU set to 00b (falling edge). After the DPSIEGRy.DIRQnEG (y = 0 or 1, n = 0 to 15) bit is set to 1 (rising edge) and the SBYCR.SSBY bit and DPSBYCR.DPSBY bit are both set to 1, the WFI instruction is executed. As a result, the MCU transitions to Deep Software Standby mode. Deep Software Standby mode is then canceled on the rising edge of the IRQn-DS pin.

(2) 通过RES引脚复位取消

当RES引脚驱动为低电平时，MCU取消深度软件待机模式并进入复位状态。在第46节“电气特性”中指定的时间内保持RES引脚为低电平。当RES引脚在指定时间段后被驱动为高电平时，CPU开始复位异常处理。

(3) 通过上电复位取消

深度软件待机模式通过上电复位取消，MCU启动复位异常处理。

(4) 通过电压监视器取消0复位

深度软件待机模式通过电压检测电路的电压监视器0复位取消，MCU开始复位异常处理。

10.9.3 取消深度软件待机模式时的引脚状态

在深度软件待机模式下，IO端口保持与软件待机模式相同的状态。MCU通过取消深度软件待机模式时产生的内部复位进行初始化，并立即开始复位异常处理。DPSBYCR.IOKEEP位设置确定是初始化IO端口还是保留软件待机模式下的IO端口状态。以下是每个位设置的IO端口状态：

- 当DPSBYCR.IOKEEP位=0时
  IO端口由取消深度软件待机模式时产生的内部复位进行初始化。
- 当DPSBYCR.IOKEEP位=1时
  虽然MCU由取消深度软件待机模式时产生的内部复位来初始化，但无论MCU内部状态如何，IO端口仍保持软件待机模式下的状态。即使对IO端口或外围模块进行了设置，IO端口状态在软件待机模式下也保持不变。通过将DPSBYCR.IOKEEP位清0来释放保留的IO端口状态，MCU根据内部状态运行。DPSBYCR.IOKEEP位不会被取消深度软件待机模式时产生的任何内部复位初始化。

10.9.4 深度软件待机模式应用示例

(1) 进入和退出深度软件待机模式

图10.10显示了一个示例，其中在IRQnDS引脚的下降沿转换到深度软件待机模式，在IRQn-DS引脚的上升沿退出深度软件待机模式。在此示例中，接受IRQn中断，同时ICU的IRQCRi.IRQMD[1:0]位设置为00b（下降沿）。在DPSIEGRy.DIRQnEG（y=0或1，n=0到15）位设置为1（上升沿）并且SBYCR.SSBY位和

DPSBYCR.DPSBY位都设置为1，执行WFI指令。因此，MCU过渡到DeepSoftware待机模式。然后在IRQn-DS引脚的上升沿取消深度软件待机模式。

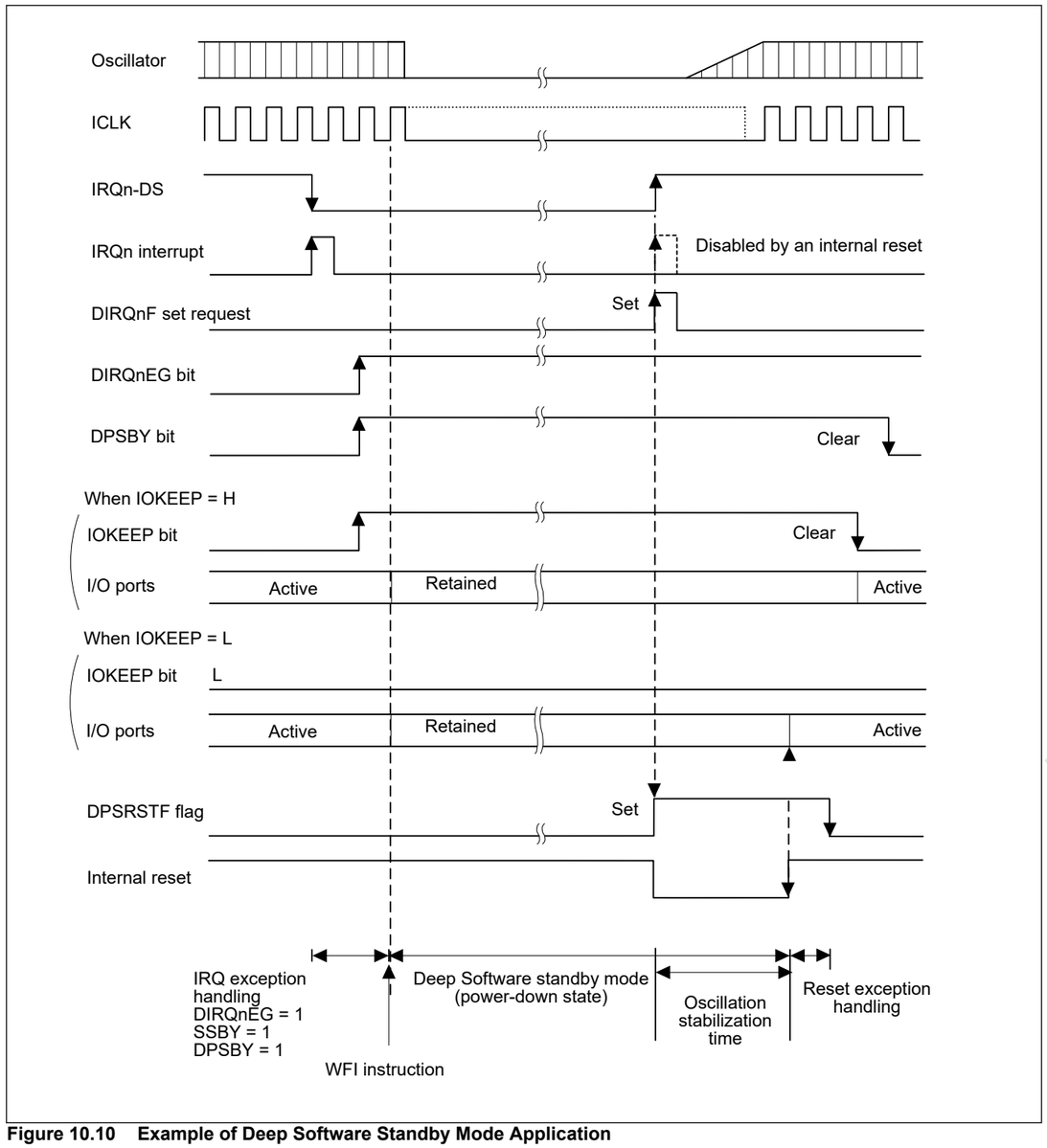


Figure 10.10 Example of Deep Software Standby Mode Application

10.9.5 Usage Flow for Deep Software Standby Mode

Figure 10.11 shows an example flow for using Deep Software Standby mode.

In this example, the RSTSR0.DPSRSTF flag of the reset function is read after the reset exception handling to determine whether a reset was generated by the RES pin or by the cancellation of Deep Software Standby mode.

For a reset by the RES pin, the MCU transitions to Deep Software Standby mode after the required register settings are made.

For a reset by cancellation of Deep Software Standby mode, the DPSBYCR.IOKEEP bit is cleared to 0 after the I/O port settings are made.

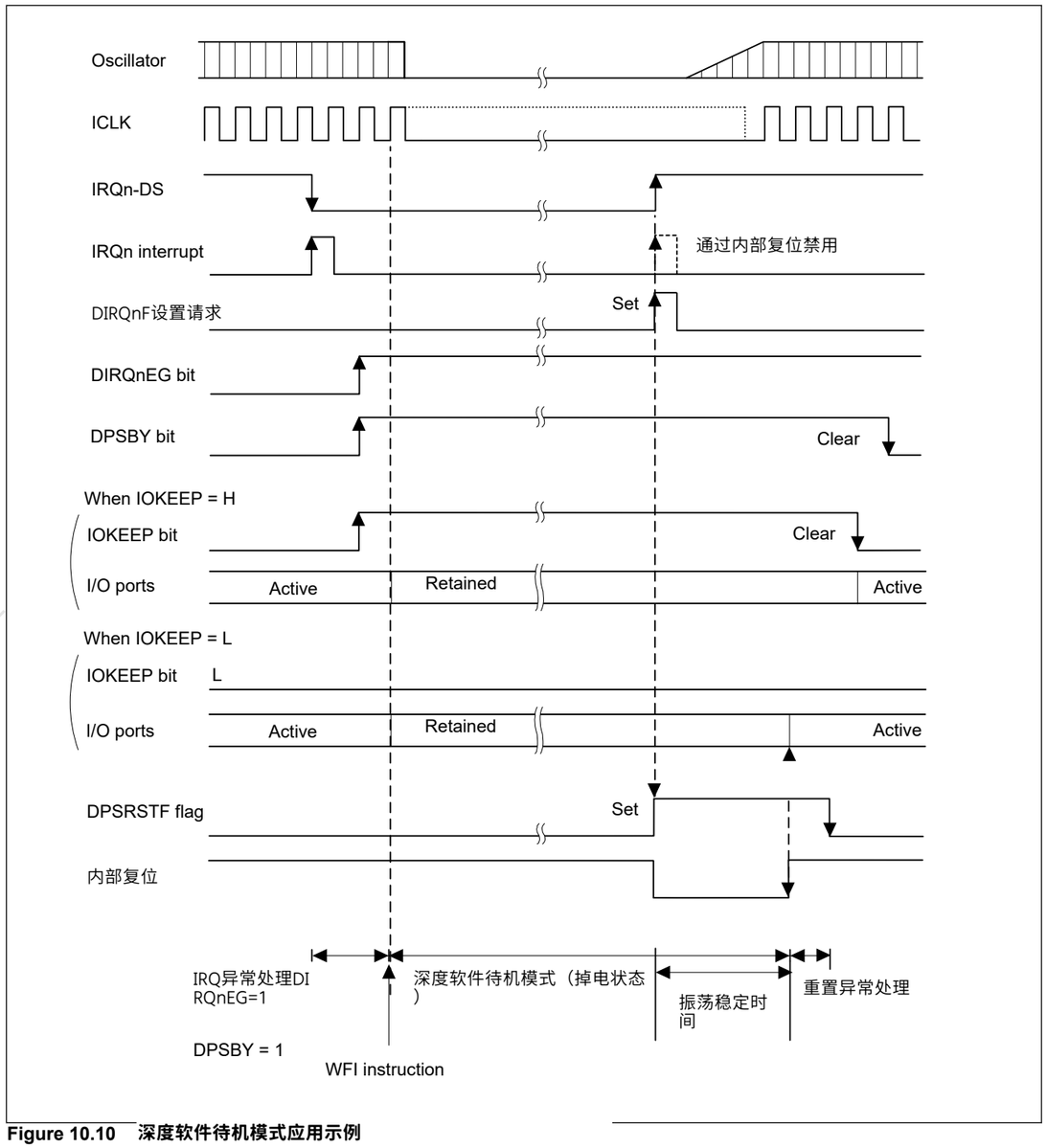


Figure 10.10 深度软件待机模式应用示例

10.9.5 深度软件待机模式的使用流程

图10.11显示了使用深度软件待机模式的示例流程。

在本例中，复位功能的RSTSR0.DPRSTF标志在复位异常处理后被读取，以确定复位是由RES引脚产生还是由深度软件待机模式的取消产生。

对于通过RES引脚进行的复位，在进行所需的寄存器设置后，MCU会转换到深度软件待机模式。

对于通过取消深度软件待机模式进行的复位，在IO端口设置完成后DPSBYCR.IOKEEP位被清零。

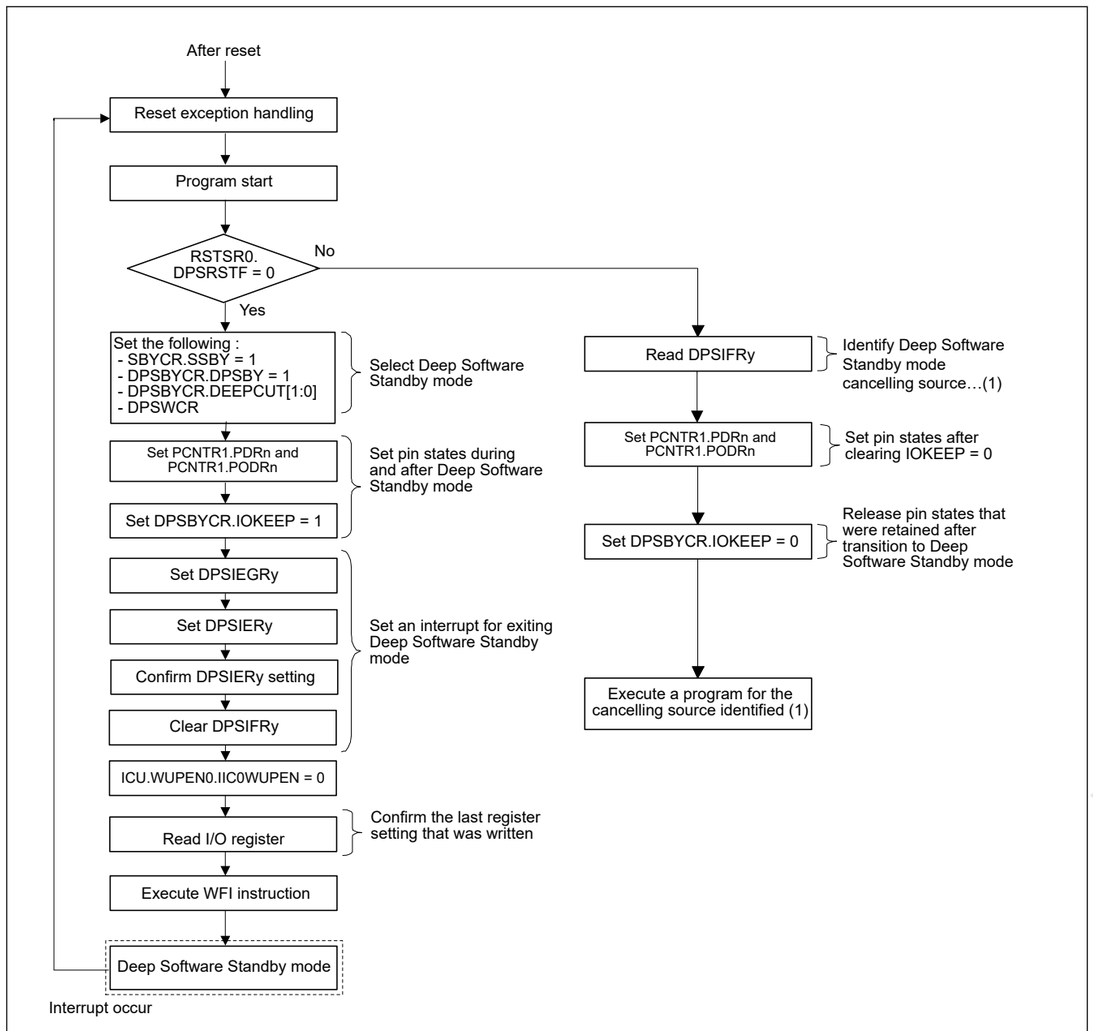


Figure 10.11 Example flow for using Deep Software Standby mode

10.10 Usage Notes

10.10.1 Register Access

(1) Invalid register write accesses during specific modes or transitions

Do not write to registers under any of the conditions listed in this section.

[Registers]

- All registers with a peripheral name of SYSTEM.

[Conditions]

- OPCCR.OPCMTSF = 1 (during transition of the operating power control mode)
- During the time period from executing a WFI instruction to returning to Normal mode
- FENTRYR.FENTRYC = 1 or FENTRYR.FENTRYD = 1 (flash P/E mode, data flash P/E mode)

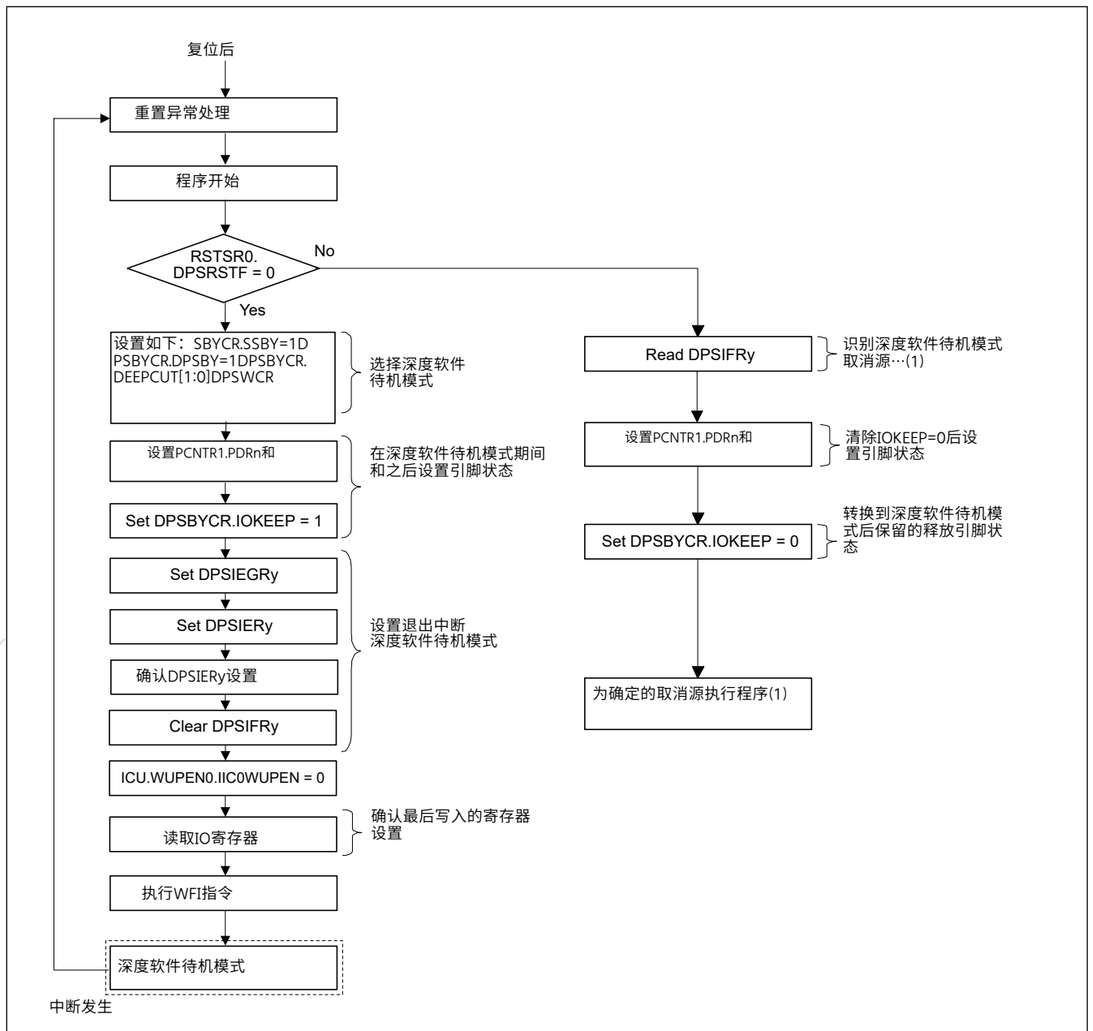


Figure 10.11 使用深度软件待机模式的示例流程

10.10 使用说明

10.10.1 注册访问

(1) 特定模式或转换期间的无效寄存器写访问

不要在本节列出的任何条件下写入寄存器。

[Registers]

●外设名称为SYSTEM的所有寄存器。

[Conditions]

●OPCCR.OPCMTSF=1（在工作功率控制模式转换期间）

●从执行WFI指令到返回Normal模式的时间段内

●FENTRYR.FENTRYC=1或FENTRYR.FENTRYD=1（闪存PE模式，数据闪存PE模式）

(2) Valid setting for the clock-related registers

Table 10.11 and Table 10.12 show the valid settings of the clock-related registers in each operating power control mode. Do not write any value other than the valid setting. Each register has certain prohibited settings under conditions other than those related to the operating power control modes. See section 8, Clock Generation Circuit for another condition of each register.

Table 10.11 Valid settings for the clock-related registers (1)

Mode	Valid settings							
	SCKSCR.CKSEL[2:0] CKOCR.CKOSEL[2:0]	SCKDIVCR.FCK[2:0] ICK[2:0]	PLLCR.PLLSTP	PLL2CR.PLL2STP	HOCOCR.HCSTP	MOCOCR.MCSTP	LOCOCR.LCSTP	MOSCCR.MOSTP
High-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 101b (PLL) *1	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
Low-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock)		1 (stop)	1 (stop)				

Note 1. SCKSCR.CKSEL[2:0] only

Table 10.12 Valid settings for the clock-related registers (2)

Operating oscillator	Valid settings
	OPCCR.OPCM[1:0]
PLL, PLL2	00b
High-speed on-chip oscillator	00b, 11b
Middle-speed on-chip oscillator	
Main clock oscillator	
Low-speed on-chip oscillator	
IWDT-dedicated on-chip oscillator	

(3) Invalid register write accesses by the DTC or DMAC

Do not write to registers listed in this section by the DTC or DMAC.

[Registers]

- MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, MSTPCRE

(4) Invalid register write accesses in Snooze mode

Do not write to registers listed in this section in Snooze mode. They must be set before entering Software Standby mode.

[Registers]

- SNZCR, SNZEDCR0, SNZREQCR0.

(5) Invalid write access when PRCR.PRC1 is 0

Do not write to registers listed in this section when the PRCR.PRC1 bit is 0.

[Registers]

- SBYCR, SNZCR, SNZEDCR0, SNZREQCR0, OPCCR, DPSBYCR, DPSWCR, DPSIERn, DPSIFRn, DPSIEGRn, SYOCDCR

(6) Invalid write access when when PRCR.PRC4 bit is 0

Do not write to registers listed in this section when the PRCR.PRC4 bit is 0.

[Registers]

(2) 时钟相关寄存器的有效设置

表10.11和表10.12显示了每种工作电源控制模式下时钟相关寄存器的有效设置。请勿写入有效设置以外的任何值。每个寄存器在与工作功率控制模式相关的条件下都有某些禁止设置。有关每个寄存器的另一个条件，请参见第8节，时钟生成电路。

Table 10.11 时钟相关寄存器的有效设置(1)

Mode	有效设置							
	SCKSCR.CKSEL[2:0] CKOCR.CKOSEL[2:0]	SCKDIVCR.FCK[2:0] ICK[2:0]	PLLCR.PLLSTP	PLL2CR.PLL2STP	HOCOCR.HCSTP	MOCOCR.MCSTP	LOCOCR.LCSTP	MOSCCR.MOSTP
High-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 101b (PLL) *1	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
Low-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock)		1 (stop)	1 (stop)				

注1.仅SCKSCR.CKSEL[2:0]

Table 10.12 时钟相关寄存器的有效设置(2)

操作振荡器	有效设置
	OPCCR.OPCM[1:0]
PLL, PLL2	00b
High-speed on-chip oscillator	00b, 11b
Middle-speed on-chip oscillator	
主时钟振荡器	
Low-speed on-chip oscillator	
IWDT-dedicated on-chip oscillator	

(3) DTC或DMAC的无效寄存器写访问

不要写入DTC或DMAC在本节中列出的寄存器。

[Registers]

- MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, MSTPCRE

(4) 贪睡模式下的无效寄存器写访问

不要在贪睡模式下写入本节中列出的寄存器。必须在进入软件待机模式之前设置它们。

[Registers]

- SNZCR, SNZEDCR0, SNZREQCR0.

(5) 当PRCR.PRC1为0时，写入访问无效

当PRCR.PRC1位为0时，不要写入本节中列出的寄存器。

[Registers]

- SBYCR, SNZCR, SNZEDCR0, SNZREQCR0, OPCCR, DPSBYCR, DPSWCR, DPSIERn, DPSIFRn, DPSIEGRn, SYOCDCR

(6) 当PRCR.PRC4位为0时，写访问无效

当PRCR.PRC4位为0时，不要写入本节中列出的寄存器。

[Registers]

- LPMSAR, DPFSAR

10.10.2 I/O Port pin states

The I/O port pin states in Software Standby mode, Deep Software Standby and Snooze mode, unless modifying in Snooze mode, are the same before entering the modes. Therefore, power consumption is not reduced while the output signals are held high.

10.10.3 Module-Stop State of DTC, DMAC

Before writing 1 to MSTPCRA.MSTPA22, clear the DMAST.DMST bit of the DMAC and the DTCST.DTCST bit of the DTC to 0. For details, see section 15, DMA Controller (DMAC) and section 16, Data Transfer Controller (DTC).

10.10.4 Internal Interrupt Sources

Interrupts do not operate in the module-stop state. If setting the module-stop bit while an interrupt request is generated, a CPU interrupt source or a DTC or DMAC startup source cannot be cleared. Always disable the associated interrupts before setting the module-stop bits.

10.10.5 Input Buffer Control by DIRQnE Bit

Setting the DPSIERy.DIRQnE (y = 0 or 1, n = 0 to 15) bit to 1 enables the associated input buffer of the IRQn-DS (n = 0 to 15) pins. Although inputs to these pins are sent to the DPSIFRy.DIRQnF (y = 0 or 1, n = 0 to 15) bits, they are not sent to the interrupt controller (ICU), peripheral modules, and I/O ports.

10.10.6 Transitioning to Low Power Modes

Because the MCU does not support wakeup by events, do not enter the low power modes such as Sleep mode, Software Standby mode or Deep Software Standby Mode by executing a WFE instruction. Also, do not set the SLEEPDEEP bit of the System Control Register in the Cortex-M33 core because the MCU does not support low power modes by SLEEPDEEP.

10.10.7 Timing of WFI Instruction

It is possible for the WFI instruction to be executed before I/O register write is completed, in which case operation might not be as intended. This can happen if the WFI is placed immediately after a write to an I/O register. To avoid this problem, read back the register that was written to confirm that the write completed.

10.10.8 Writing to the WDT/IWDT Registers by DTC or DMAC in Sleep Mode or Snooze Mode

Do not write to the WDT or IWDT registers by the DTC or DMAC while WDT or IWDT is stopped after entering Sleep mode or Snooze mode.

10.10.9 Oscillators in Snooze Mode

Oscillators that stop on entering Software Standby mode automatically restart when a trigger for switching to Snooze mode is generated. The MCU does not enter Snooze mode until all the oscillators stabilize. If in Snooze mode, you must disable oscillators that are not required in Snooze mode before entering Software Standby mode. Otherwise, the transition from Software Standby mode to Snooze mode takes longer.

10.10.10 Snooze Mode Entry by RXD0 Falling Edge

When the SNZCR.RXDREQEN bit is 1, the falling edge of RXD0 pin is used to switch MCU from Software Standby mode to Snooze mode when using UART of SCI0 in Snooze mode. In this case an interrupt such as SCI0_AM or an address mismatch event is used as the source for canceling Snooze mode. However noise on the RXD0 pin might cause the MCU to transfer from Software Standby mode to Snooze mode unexpectedly. In this case if the MCU does not receive RXD0 data after the noise, an interrupt such as SCI0_AM, or an address mismatch event is not generated and the MCU stays in Snooze mode. This can be avoided by using AGTn (n = 1) underflow interrupt to return to Software Standby mode or Normal mode unless otherwise UART receive data is completed before AGTn (n = 1) underflow. However, do not use the AGTn (n = 1) underflow as a source to return to Software Standby mode during an UART communication. This causes the UART to stop the operation in a half-finished state.

- LPMSAR, DPFSAR

10.10.2 IO端口引脚状态

软件待机模式、深度软件待机和贪睡模式下的IO端口引脚状态，除非在贪睡模式下进行修改，否则在进入这些模式之前是相同的。因此，当输出信号保持为高时，功耗不会降低。

10.10.3 DTC、DMAC的模块停止状态

在将1写入MSTPCRA.MSTPA22之前，清除DMAC的DMAST.DMST位和DTCST.DTCST位
DTC为0。有关详细信息，请参阅第15节，DMA控制器(DMAC)和第16节，数据传输控制器(DTC)。

10.10.4 内部中断源

中断不会在模块停止状态下运行。如果在产生中断请求时设置模块停止位，则
无法清除CPU中断源或DTC或DMAC启动源。在设置模块停止位之前，始终禁用相关的中断。

10.10.5 通过DIRQnE位控制输入缓冲器

将DPSIERy.DIRQnE（y=0或1，n=0至15）位设置为1可启用IRQn-DS（n=0至15）引脚的相关输入缓冲器。尽管这些引脚的输入被发送到DPSIFRy.DIRQnF（y=0或1，n=0到15）位，但它们不会被发送到中断控制器(ICU)、外设模块和IO端口。

10.10.6 过渡到低功耗模式

由于MCU不支持事件唤醒，请勿进入睡眠模式、软件等低功耗模式
待机模式或深度软件待机模式通过执行WFE指令。此外，不要设置Cortex-M33内核中系统控制寄存器的SLEEPDEEP位，因为MCU不支持SLEEPDEEP的低功耗模式。

10.10.7 WFI指令的时间安排

WFI指令可能在IO寄存器写入完成之前执行，在这种情况下操作可能不会按预期进行。如果在写入IO寄存器后立即放置WFI，则会发生这种情况。为避免此问题，请回读已写入的寄存器以确认写入已完成。

10.10.8 在睡眠模式或贪睡模式下通过DTC或DMAC写入WDTIWDT寄存器 Mode

当WDT或IWDT在进入休眠模式或贪睡模式后停止时，请勿通过DTC或DMAC写入WDT或IWDT寄存器。

10.10.9 贪睡模式下的振荡器

进入软件待机模式时停止的振荡器会在生成切换到贪睡模式的触发器时自动重新启动。在所有振荡器稳定之前，MCU不会进入贪睡模式。如果处于贪睡模式，您必须在进入软件待机模式之前禁用贪睡模式中不需要的振荡器。否则，从软件待机模式到贪睡模式的转换需要更长的时间。

10.10.10 通过RXD0下降沿进入贪睡模式

当SNZCR.RXDREQEN位为1时，在贪睡模式下使用SCI0的UART时，RXD0引脚的下降沿用于将MCU从软件待机模式切换到贪睡模式。在这种情况下，中断如SCI0_AM或地址不匹配事件被用作取消贪睡模式的源。然而，RXD0引脚上的噪声可能会导致MCU意外地从软件待机模式转换到贪睡模式。在这种情况下，如果MCU在噪声后没有接收到RXD0数据，则不会产生SCI0_AM等中断或地址不匹配事件，并且MCU保持在贪睡模式。这可以通过使用AGTn(n=1)下溢中断返回到软件待机模式或正常模式来避免，除非在AGTn(n=1)下溢之前完成UART接收数据。但是，不要使用AGTn(n=1)下溢作为UART通信期间返回软件待机模式的源。这会导致UART在半完成状态下停止操作。

10.10.11 Using UART of SCI0 in Snooze Mode

When using UART in Snooze mode, ensure that the snooze request (RXD0 falling edge) does not conflict with the wakeup requests set by the WUPEN register, otherwise UART cannot be guaranteed.

When using UART in Snooze mode, the following conditions must be satisfied:

- The clock source must be HOCO
- MOCO, PLL, PLL2, and the main clock oscillator must be stopped before entering Software Standby mode
- The RXD0 pin must be kept high before entering Software Standby mode
- A transition to Software Standby mode must not occur during an SCI0 communication
- The MSTPCRC.MSTPC0 bit must be 1 before entering Software Standby mode.

10.10.12 Conditions of A/D Conversion Start in Snooze Mode

ADC can only be triggered by the ELC in Snooze mode. Do not use software trigger or ADTRGn (n = 0, 1) pin.

10.10.13 ELC Events in Snooze Mode

This section lists available ELC events in Snooze mode. Do not use any other events. If starting peripheral modules for the first time after entering Snooze mode, the Event Link Setting Register (ELSRn) must set a Snooze mode entry event (SYSTEM_SNZREQ) as the trigger.

- Snooze mode entry (SYSTEM_SNZREQ)
- DTC transfer end (DTC_DTCEND)
- ADC Composite compare match 0 (ADC_CCMPM0)
- ADC Composite compare match 1 (ADC_CCMPM1)
- Data operation circuit interrupt (DOC_DOPCI).

10.10.14 Module-Stop Bit Write Timing

It is possible that access to I/O register may be executed before the corresponding module-stop bit write completed. In this case, access to I/O register may not proceed as intended. To avoid this issue, before accessing I/O register, read back the module-stop bit that was written to confirm that the write completed.

10.10.11 在贪睡模式下使用SCI0的UART

在Snooze模式下使用UART时，确保Snooze请求（RXD0下降沿）与WUPEN寄存器设置的唤醒请求不冲突，否则无法保证UART。

在Snooze模式下使用UART时，必须满足以下条件：

●时钟源必须是HOCO

●MOCO、PLL、PLL2和主时钟振荡器必须在进入软件待机模式之前停止

●进入软件待机模式前，RXD0引脚必须保持高电平

●在SCI0通信期间不得转换到软件待机模式

●MSTPCRC.MSTPC0位必须为1才能进入软件待机模式。

10.10.12 贪睡模式下AD转换开始的条件

ADC只能由ELC在贪睡模式下触发。不要使用软件触发或ADTRGn(n=0 1)引脚。

10.10.13 贪睡模式下的ELC事件

本节列出了贪睡模式下可用的ELC事件。不要使用任何其他事件。如果进入贪睡模式后第一次启动外围模块，事件链接设置寄存器（ELSRn）必须设置贪睡模式进入事件（SYSTEM_SNZREQ）作为触发器。

●贪睡模式条目(SYSTEM_SNZREQ)

●DTC传输结束（DTC_DTCEND）

●ADC复合比较匹配0(ADC_CCMPM0)

●ADC复合比较匹配1(ADC_CCMPM1)

●数据操作电路中断（DOC_DOPCI）。

10.10.14 模块停止位写时序

在相应的模块停止位写入完成之前，可能会执行对IO寄存器的访问。在这种情况下，对IO寄存器的访问可能不会按预期进行。为避免此问题，在访问IO寄存器之前，请回读已写入的模块停止位以确认写入已完成。

11. Register Write Protection

11.1 Overview

The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).

Table 11.1 lists the association between the bits in the PRCR register and the registers to be protected.

Table 11.1 Association between the bits in the PRCR register and registers to be protected

PRCR bit	Register to be protected
PRC0	• Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, MOCOUTCR, HOCOUTCR, SCISPICKDIVCR, CANFDCKDIVCR, GPTCKDIVCR, IICCKDIVCR, SCISPICKCR, CANFDCKCR, GPTCKCR, IICCKCR, MOSCWTCR, MOMCR, LOCOCR, LOCOUTCR
PRC1	• Registers related to the low power modes: SBYCR, SNZCR, SNZEDCR0, SNZREQCR0, OPCCR, DPSBYCR, DPSWCR, DPSIER0-2, DPSIFR0-2, DPSIEGR0-2, SYOCDCR
PRC3	• Registers related to the LVD: LVD1CR1, LVD1SR, LVD2CR1, LVD2SR, LVD1CMPCR, LVD2CMPCR, LVD1CR0, LVD2CR0
PRC4	• Registers related to the security function: CGFSAR, RSTSAR, LPMSAR, LVDSAR, DPFSAR, CSAR, SRAMSAR, STBRAMSAR, DTCSAR, DMACSAR, ICUSARx, BUSSARx, MMPUSARx, TZFSAR, CPUDSAR, FSAR, PSARx, MSSAR, PmSAR, ELCSARx

11.2 Register Descriptions

11.2.1 PRCR : Protect Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3FE

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	PRC4	PRC3	—	PRC1	PRC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PRC0	Enable writing to the registers related to the clock generation circuit 0: Disable writes 1: Enable writes	R/W
1	PRC1	Enable writing to the registers related to the low power modes 0: Disable writes 1: Enable writes	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	PRC3	Enable writing to the registers related to the LVD 0: Disable writes 1: Enable writes	R/W
4	PRC4	Enables writing to the registers related to the security function 0: Disable writes 1: Enable writes	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
15:8	PRKEY[7:0]	PRC Key Code These bits control the write access to the PRCR register. To modify the PRCR register, write 0xA5 to the upper 8 bits and the target value to the lower 8 bits as a 16-bit unit.	W

11. 寄存器写保护

11.1 Overview

寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。要保护的寄存器由保护寄存器(PRCR)设置。

表11.1列出了PRCR寄存器中的位与要保护的寄存器之间的关联。

Table 11.1 PRCR寄存器中的位与要保护的寄存器之间的关联

PRCR bit	注册受保护
PRC0	• 与时钟产生电路相关的寄存器： SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, MOCOUTCR, HOCOUTCR, SCISPICKDIVCR, CANFDCKDIVCR, GPTCKDIVCR, IICCKDIVCR, SCISPICKCR, CANFDCKCR, GPTCKCR, IICCKCR, MOSCWTCR, MOMCR, LOCOCR, LOCOUTCR
PRC1	• 与低功耗模式相关的寄存器： SBYCR, SNZCR, SNZEDCR0, SNZREQCR0, OPCCR, DPSBYCR, DPSWCR, DPSIER0-2, DPSIFR0-2, DPSIEGR0-2, SYOCDCR
PRC3	• 与LVD相关的寄存器： LVD1CR1, LVD1SR, LVD2CR1, LVD2SR, LVD1CMPCR, LVD2CMPCR, LVD1CR0, LVD2CR0
PRC4	• 与安全功能相关的寄存器： CGFSAR, RSTSAR, LPMSAR, LVDSAR, DPFSAR, CSAR, SRAMSAR, STBRAMSAR, DTCSAR, DMACSAR, ICUSARx, BUSSARx, MMPUSARx, TZFSAR, CPUDSAR, FSAR, PSARx, MSSAR, PmSAR, ELCSARx

11.2 注册说明

11.2.1 PRCR:保护寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x3FE

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	PRC4	PRC3	—	PRC1	PRC0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PRC0	允许写入与时钟生成电路相关的寄存器 0：禁用写入1： 启用写入	R/W
1	PRC1	允许写入与低功耗模式相关的寄存器 0：禁用写入1： 启用写入	R/W
2	—	该位读取为0。写入值应为0。	R/W
3	PRC3	允许写入与LVD相关的寄存器 0：禁用写入1： 启用写入	R/W
4	PRC4	允许写入与安全功能相关的寄存器 0：禁用写入1： 启用写入	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
15:8	PRKEY[7:0]	中华人民共和国密钥代码 这些位控制对PRCR寄存器的写访问。修改PRCR寄存器，将0xA5写入高8位，将目标值写入低8位，以16位为单位。	W

PRCn bits (Protect bit n) (n = 0, 1, 3, 4)

The PRCn bits enable or disable writing to the protected registers listed in Table 11.1. Setting the PRCn bits to 1 or 0 enables or disables writing, respectively.

The register controlled by PRC4 may not reflect the PRC4 change when PRCR and its controlled registers are continuously written access. Avoid continuous write access or read the PRCR after PRC4 change, and then write access the PRC4-controlled register.

PRCn位（保护位n）（n=0、1、3、4）

PRCn位启用或禁用对表11.1中列出的受保护寄存器的写入。将PRCn位设置为1或0分别启用或禁用写入。

当PRCR及其受控寄存器连续写入访问时，PRC4控制的寄存器可能无法反映PRC4的变化。避免连续写访问或在PRC4更改后读取PRCR，然后再写访问PRC4控制的寄存器。

12. Interrupt Controller Unit (ICU)

12.1 Overview

The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.

Table 12.1 lists the ICU specifications, Figure 12.1 shows a block diagram, and Table 12.2 lists the I/O pins.

Table 12.1 ICU specifications

Parameter		Description
Maskable interrupts	Peripheral function interrupts	• Interrupts from peripheral modules Number of sources: 265 (select factor within event list numbers 17 to 511)
	External pin interrupts	• Interrupt detection on low level*4, falling edge, rising edge, rising and falling edges. One of these detection methods can be set for each source • Digital filter function supported • 16 sources, with interrupts from IRQi (i = 0 to 15) pins.
	Interrupt requests to CPU (NVIC)	• 96 interrupt requests are output to NVIC.
	DMAC control	• The DMAC can be activated using interrupt sources*1 • The target interrupt source can be selected individually for every DMAC channels.
	DTC control	• The DTC can be activated using interrupt sources*1 • The method for selecting an interrupt source is the same as that of the interrupt request to NVIC.
Non-maskable interrupts*2	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection on falling edge or rising edge • Digital filter function supported
	WDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	IWDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	Low voltage detection 1*3	Voltage monitor 1 interrupt of the voltage monitor 1 circuit (LVD_LVD1)
	Low voltage detection 2*3	Voltage monitor 2 interrupt of the voltage monitor 2 circuit (LVD_LVD2)
	RPEST*5	Interrupt on SRAM parity error
	RECCST*5	Interrupt on SRAM ECC error
	TZFST*5	TrustZone Filter error.
	CPEST*5	Cache RAM Parity error.
	Oscillation stop detection interrupt*3	Interrupt on detecting that the main oscillation has stopped
	Bus master MPU error*5	Interrupt on MPU bus master error
Low power modes		• Sleep mode: return is initiated by non-maskable interrupts or any other interrupt source • Software Standby mode: return is initiated by non-maskable interrupts. Interrupt can be selected in the WUPEN register. • Snooze mode: return is initiated by non-maskable interrupts. Interrupt can be selected in the SELSR0 and WUPEN registers. See section 12.2.16. SELSR0 : SYS Event Link Setting Register and section 12.2.17. WUPEN0 : Wake Up Interrupt Enable Register 0.
TrustZone Filter		Available

Note 1. For the DMAC and DTC activation sources, see Table 12.4.
Note 2. Non-maskable interrupts can be enabled only once after a reset release.
Note 3. These non-maskable interrupts can also be used as maskable interrupts. When used as maskable interrupts, do not change the value of the NMIER register from the reset state. To enable voltage monitor 1 and voltage monitor 2 interrupts, set the LVD1CR1.IRQSEL and LVD2CR1.IRQSEL bits to 1.
Note 4. Low level: interrupt detection is not canceled if you do not clear it after a detection.
Note 5. These non-maskable interrupt sources cannot be recovered if the request source clock is stopped during low power mode.

12. 中断控制器单元(ICU)

12.1 Overview

中断控制器单元(ICU)控制哪些事件信号链接到嵌套向量中断控制器(NVIC)、DMA控制器(DMAC)和数据传输控制器(DTC)模块。ICU还控制不可屏蔽的中断。

表12.1列出了ICU规格，图12.1显示了框图，表12.2列出了IO引脚。

Table 12.1 ICU规格

Parameter		Description
Maskable interrupts	外设功能中断	• 来自外围模块的中断 源数：265（在事件列表编号17到511中选择因子）
	外部引脚中断	• 低电平中断检测*4、下降沿、上升沿、上升沿和下降沿。可以为每个来源设置其中一种检测方法 • 支持数字滤波功能 • 16个源，来自IRQi（i=0到15）引脚的中断。
	对CPU的中断请求(NVIC)	• 96个中断请求输出到NVIC。
	DMAC control	• 可以使用中断源激活DMAC*1 • 可以为每个DMAC通道单独选择目标中断源。
	DTC control	• 可以使用中断源激活DTC*1 • 中断源的选择方法与中断请求相同 NVIC.
Non-maskable interrupts*2	NMI引脚中断	• 来自NMI引脚的中断 • 下降沿或上升沿中断检测 • 支持数字滤波功能
	WDT underflow/refresh error*3	递减计数器下溢或发生刷新错误时中断
	IWDT underflow/refresh error*3	递减计数器下溢或发生刷新错误时中断
	低电压检测1*3	电压监视器1电路的电压监视器1中断(LVD_LVD1)
	低电压检测2*3	电压监视器2电路的电压监视器2中断(LVD_LVD2)
	RPEST*5	SRAM奇偶校验错误中断
	RECCST*5	SRAMECC错误中断
	TZFST*5	TrustZone过滤器错误。
	CPEST*5	高速缓存RAM奇偶校验错误。
	振荡停止检测中断*3	检测到主振荡停止时中断
	总线主控MPU错误*5	MPU总线主机错误中断
低功耗模式		• 睡眠模式：返回由不可屏蔽中断或任何其他中断源启动 • 软件待机模式：返回由不可屏蔽的中断启动。可以在WUPEN寄存器中选择中断。 • 贪睡模式：返回由不可屏蔽的中断发起。中断可以在SELSR0和WUPEN寄存器。 请参阅第12.2.16节。SELSR0：SYS事件链接设置寄存器和第12.2.17节。乌彭0：唤醒中断使能寄存器0。
TrustZone Filter		Available

注1.对于DMAC和DTC激活源，请参见表12.4。
注2.不可屏蔽中断只能在复位释放后启用一次。
注3：这些不可屏蔽中断也可以用作可屏蔽中断。当用作可屏蔽中断时，不要从复位状态更改NMIER寄存器的值。要启用电压监视器1和电压监视器2中断，请将LVD1CR1.IRQSEL和LVD2CR1.IRQSEL位设置为1。

注4.低电平：检测后不清除中断检测不取消。
注5.如果请求源时钟在低功耗模式下停止，这些不可屏蔽的中断源将无法恢复。

Figure 12.1 shows the ICU block diagram.

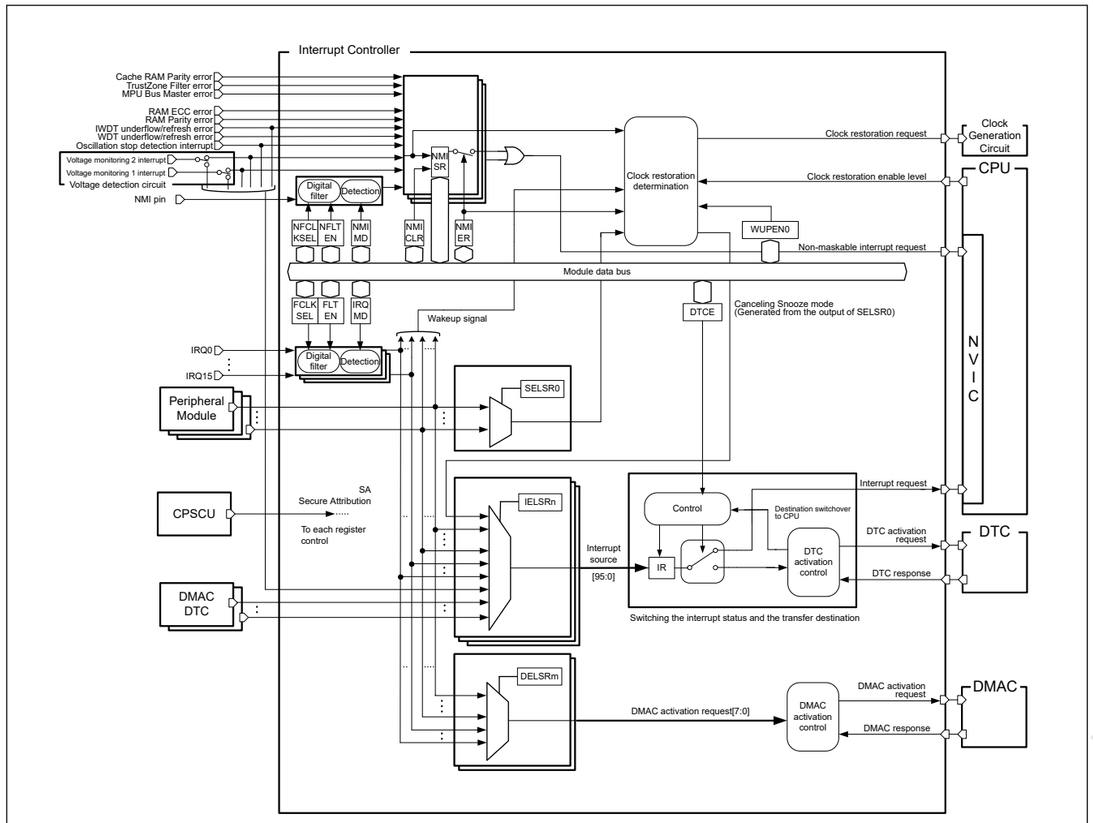


Figure 12.1 ICU block diagram

Table 12.2 lists the ICU input/output pins.

Table 12.2 ICU I/O pins

Pin name	I/O	Description
NMI	Input	Non-maskable interrupt request pin
IRQi (i = 0 to 15)	Input	External interrupt request pins

12.2 Register Descriptions

This chapter does not describe the Arm® NVIC internal registers. For information about these registers, see ARM Limited., ARM® Cortex®-M33 Processor Technical Reference Manual (ARM 100230).

图12.1显示了ICU框图。

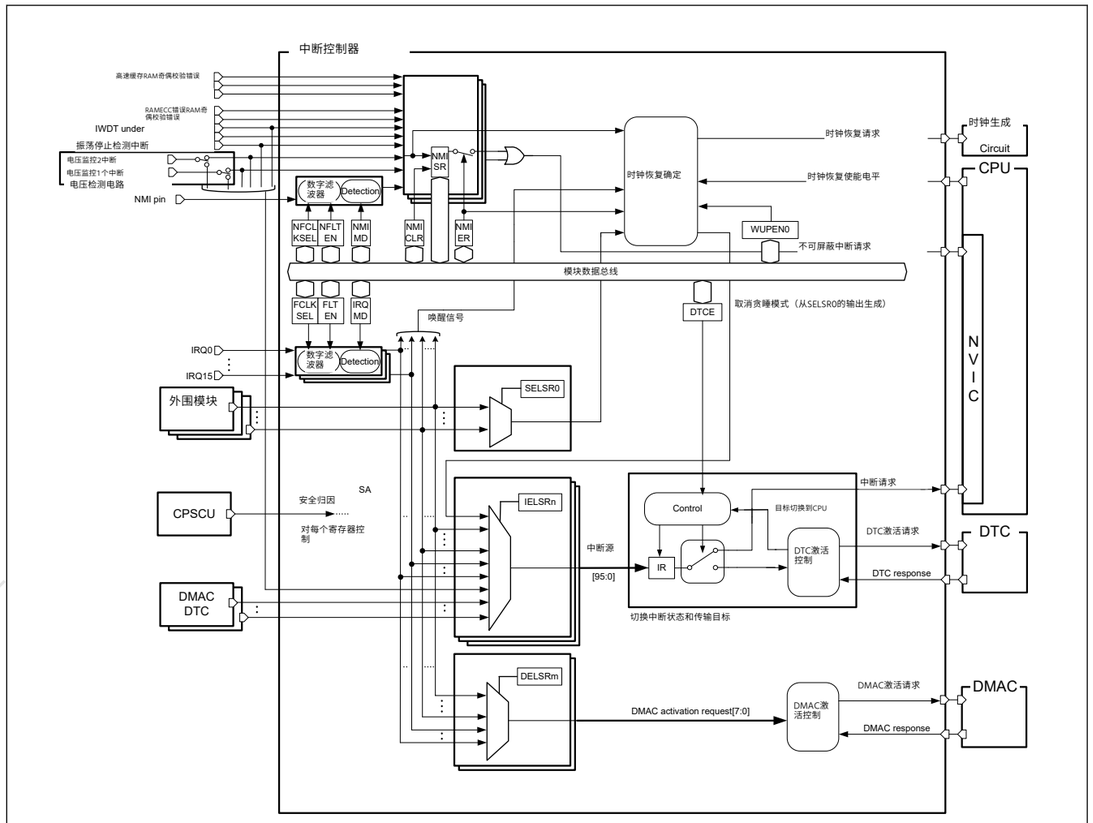


Figure 12.1 ICU框图

表12.2列出了ICU输入输出引脚。

Table 12.2 ICUIO引脚

引脚名称	I/O	Description
NMI	Input	不可屏蔽中断请求引脚
IRQi (i = 0 to 15)	Input	外部中断请求引脚

12.2 注册说明

本章不介绍Arm®NVIC内部寄存器。有关这些寄存器的信息，请参阅ARMLimited。
ARM®Cortex®-M33处理器技术参考手册(ARM100230)。

12.2.1 ICUSARA : Interrupt Controller Unit Security Attribution Register A

Base address: CPSCU = 0x4000_8000

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIRQCR15	SAIRQCR14	SAIRQCR13	SAIRQCR12	SAIRQCR11	SAIRQCR10	SAIRQCR9	SAIRQCR8	SAIRQCR7	SAIRQCR6	SAIRQCR5	SAIRQCR4	SAIRQCR3	SAIRQCR2	SAIRQCR1	SAIRQCR0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	SAIRQCR15 to SAIRQCR0	Security attributes of registers for the IRQCRn register 0: Secure 1: Non-secure	R/W
31:16	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SAIRQCRn bits (Security attributes of registers for the IRQCRn register)

The target registers are as follows:

- IRQCR0 to IRQCR15 registers
- WUPEN0.IRQWUPEN[15:0] bits

12.2.2 ICUSARB : Interrupt Controller Unit Security Attribution Register B

Base address: CPSCU = 0x4000_8000

Offset address: 0x44

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SANMI
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SANMI	Security attributes of registers for nonmaskable interrupt 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SANMI bit (Security attributes of registers for nonmaskable interrupt)

Security attributes of registers for non-maskable interrupt. The target registers are as follows:

- NMIER

12.2.1 ICUSARA:中断控制器单元安全属性寄存器A

Base address: CPSCU = 0x4000_8000

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIRQCR15	SAIRQCR14	SAIRQCR13	SAIRQCR12	SAIRQCR11	SAIRQCR10	SAIRQCR9	SAIRQCR8	SAIRQCR7	SAIRQCR6	SAIRQCR5	SAIRQCR4	SAIRQCR3	SAIRQCR2	SAIRQCR1	SAIRQCR0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	SAIRQCR15 to SAIRQCR0	IRQCRn寄存器的寄存器安全属性 0: Secure 1: Non-secure	R/W
31:16	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

SAIRQCRn位（IRQCRn寄存器的寄存器安全属性）

目标寄存器如下：

- IRQCR0到IRQCR15寄存器
- WUPEN0.IRQWUPEN[15:0] bits

12.2.2 ICUSARB:中断控制器单元安全属性寄存器B

Base address: CPSCU = 0x4000_8000

Offset address: 0x44

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SANMI
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SANMI	不可屏蔽中断寄存器的安全属性 0: Secure 1: Non-secure	R/W
31:1	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

SANMI位（不可屏蔽中断的寄存器的安全属性）

不可屏蔽中断的寄存器的安全属性。目标寄存器如下：

- NMIER

- NMICLR
- NMICR

The value of AIRCR.BFHFNMINS bit [13] in Application Interrupt and Reset Control Register of ARM CPU should be the same as the value of security attribution. The initial values of AIRCR.BFHFNMINS and the SANMI bits are different. AIRCR.BFHFNMINS is secure and SANMI is non-secure. Polarity has the same meaning so program these to match.

Note: Only one of Secure and Non-Secure can set security attribution for non-maskable interrupt-related registers. If you program the Secure attribute as secure, it always goes to the Secure interrupt handler. To release any of the non-maskable interrupt sources to the non-secure user, write a function to execute a nonsecure program from the interrupt handler for Secure.

12.2.3 ICUSARC : Interrupt Controller Unit Security Attribution Register C

Base address: CPSCU = 0x4000_8000

Offset address: 0x48

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SADMAC7	SADMAC6	SADMAC5	SADMAC4	SADMAC3	SADMAC2	SADMAC1	SADMAC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	SADMAC7 to SADMAC0	Security attributes of registers for DMAC channel 0: Secure 1: Non-secure	R/W
31:8	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SADMACn bits (Security attributes of registers for DMAC channel)

Security attributes of registers for DMAC channel. This register is referred to as the security attribute of the ICU and DMAC registers.

The controlled ICU register is:

- DELSRn

The controlled DMAC registers are:

- DMACn.DMSAR
- DMACn.DMSRR
- DMACn.DMDAR
- DMACn.DMDRR
- DMACn.DMCRA
- DMACn.DMCRB
- DMACn.DMTMD
- DMACn.DMINT
- DMACn.DMAMD
- DMACn.DMOFR

- NMICLR
- NMICR

ARMCPU的应用中断和复位控制寄存器AIRCR.BFHFNMINSbit[13]的值应与安全属性的值相同。AIRCR.BFHFNMINS和SANMI位的初始值不同。AIRCR.BFHFNMINS是安全的，而SANMI是不安全的。极性具有相同的含义，因此请对它们进行编程以匹配。

Note: 只有Secure和Non-Secure之一可以为不可屏蔽的中断相关寄存器设置安全属性。如果您将Secure属性编程为安全，则它始终会转到Secure中断处理程序。要将任何不可屏蔽的中断源释放给非安全用户，请编写一个函数以从Secure的中断处理程序执行非安全程序。

12.2.3 ICUSARC:中断控制器单元安全属性寄存器C

Base address: CPSCU = 0x4000_8000

Offset address: 0x48

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SADMAC7	SADMAC6	SADMAC5	SADMAC4	SADMAC3	SADMAC2	SADMAC1	SADMAC0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	SADMAC7 to SADMAC0	DMAC通道寄存器的安全属性 0: Secure 1: Non-secure	R/W
31:8	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

SADMACn位（DMAC通道寄存器的安全属性）

DMAC通道寄存器的安全属性。该寄存器被称为ICU的安全属性和
DMAC registers.

受控ICU寄存器为：

- DELSRn

受控的DMAC寄存器是：

- DMACn.DMSAR
- DMACn.DMSRR
- DMACn.DMDAR
- DMACn.DMDRR
- DMACn.DMCRA
- DMACn.DMCRB
- DMACn.DMTMD
- DMACn.DMINT
- DMACn.DMAMD
- DMACn.DMOFR

- DMACn.DMCNT
- DMACn.DMREQ
- DMACn.DMSTS
- DMACn.DMSBS
- DMACn.DMDBS

For details on DMAC registers, see section 15, DMA Controller (DMAC).

12.2.4 ICUSARD : Interrupt Controller Unit Security Attribution Register D

Base address: CPSCU = 0x4000_8000

Offset address: 0x4C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SASELSR0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SASELSR0	Security attributes of registers for SELSR0 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

12.2.5 ICUSARE : Interrupt Controller Unit Security Attribution Register E

Base address: CPSCU = 0x4000_8000

Offset address: 0x50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIIC0WUP	SAAGT1CBWUP	SAAGT1CAWUP	SAAGT1UDWUP	—	—	—	—	—	—	—	—	SALVD2WUP	SALVD1WUP	SAKEYWUP	SAIWDTWUP
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 1. The write value should be 1.	R/W
16	SAIWDTWUP	Security attributes of registers for WUPEN0.b16 0: Secure 1: Non-secure	R/W
17	SAKEYWUP	Security attributes of registers for WUPEN0.b17 0: Secure 1: Non-secure	R/W

- DMACn.DMCNT
- DMACn.DMREQ
- DMACn.DMSTS
- DMACn.DMSBS
- DMACn.DMDBS

有关DMAC寄存器的详细信息，请参见第15节，DMA控制器(DMAC)。

12.2.4 ICUSARD:中断控制器单元安全属性寄存器D

Base address: CPSCU = 0x4000_8000

Offset address: 0x4C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SASELSR0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SASELSR0	SELSR0寄存器的安全属性 0: Secure 1: Non-secure	R/W
31:1	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

12.2.5 ICUSARE:中断控制器单元安全属性寄存器E

Base address: CPSCU = 0x4000_8000

Offset address: 0x50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIIC0WUP	SAAGT1CBWUP	SAAGT1CAWUP	SAAGT1UDWUP	—	—	—	—	—	—	—	—	SALVD2WUP	SALVD1WUP	SAKEYWUP	SAIWDTWUP
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	—	这些位被读取为1。写入值应为1。	R/W
16	SAIWDTWUP	WUPEN0.b16寄存器的安全属性 0: Secure 1: Non-secure	R/W
17	SAKEYWUP	WUPEN0.b17寄存器的安全属性 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
18	SALVD1WUP	Security attributes of registers for WUPEN0.b18 0: Secure 1: Non-secure	R/W
19	SALVD2WUP	Security attributes of registers for WUPEN0.b19 0: Secure 1: Non-secure	R/W
27:20	—	These bits are read as 1. The write value should be 1.	R/W
28	SAAGT1UDWUP	Security attributes of registers for WUPEN0.b28 0: Secure 1: Non-secure	R/W
29	SAAGT1CAWUP	Security attributes of registers for WUPEN0.b29 0: Secure 1: Non-secure	R/W
30	SAAGT1CBWUP	Security attributes of registers for WUPEN0.b30 0: Secure 1: Non-secure	R/W
31	SAIIC0WUP	Security attributes of registers for WUPEN0.b31 0: Secure 1: Non-secure	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

12.2.6 ICUSARG : Interrupt Controller Unit Security Attribution Register G

Base address: CPSCU = 0x4000_8000
Offset address: 0x70

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIEL SR31	SAIEL SR30	SAIEL SR29	SAIEL SR28	SAIEL SR27	SAIEL SR26	SAIEL SR25	SAIEL SR24	SAIEL SR23	SAIEL SR22	SAIEL SR21	SAIEL SR20	SAIEL SR19	SAIEL SR18	SAIEL SR17	SAIEL SR16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIEL SR15	SAIEL SR14	SAIEL SR13	SAIEL SR12	SAIEL SR11	SAIEL SR10	SAIEL SR9	SAIEL SR8	SAIEL SR7	SAIEL SR6	SAIEL SR5	SAIEL SR4	SAIEL SR3	SAIEL SR2	SAIEL SR1	SAIEL SR0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR31 to SAIELSR0	Security attributes of registers for IELSR31 to IELSR0 0: Secure 1: Non-secure	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

SAIELSRn bits (Security attributes of registers for IELSR31 to IELSR0)

The Secure Attribute managed within the Arm CPU NVIC must match the security attribution of IELSEn (n = 0 to 31).
NVIC internal registers are in NVIC_ITNS0[31:0]. The initial values of NVIC_ITNS0 and ICUSARG are different.
NVIC_ITNS0 is secure and ICUSARG is non-secure. Polarity has the same meaning so program these to match.

Bit	Symbol	Function	R/W
18	SALVD1WUP	WUPEN0.b18寄存器的安全属性 0: Secure 1: Non-secure	R/W
19	SALVD2WUP	WUPEN0.b19寄存器的安全属性 0: Secure 1: Non-secure	R/W
27:20	—	这些位被读取为1。写入值应为1。	R/W
28	SAAGT1UDWUP	WUPEN0.b28寄存器的安全属性 0: Secure 1: Non-secure	R/W
29	SAAGT1CAWUP	WUPEN0.b29寄存器的安全属性 0: Secure 1: Non-secure	R/W
30	SAAGT1CBWUP	WUPEN0.b30寄存器的安全属性 0: Secure 1: Non-secure	R/W
31	SAIIC0WUP	WUPEN0.b31寄存器的安全属性 0: Secure 1: Non-secure	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

12.2.6 ICUSARG:中断控制器单元安全属性寄存器G

Base address: CPSCU = 0x4000_8000
Offset address: 0x70

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIEL SR31	SAIEL SR30	SAIEL SR29	SAIEL SR28	SAIEL SR27	SAIEL SR26	SAIEL SR25	SAIEL SR24	SAIEL SR23	SAIEL SR22	SAIEL SR21	SAIEL SR20	SAIEL SR19	SAIEL SR18	SAIEL SR17	SAIEL SR16
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIEL SR15	SAIEL SR14	SAIEL SR13	SAIEL SR12	SAIEL SR11	SAIEL SR10	SAIEL SR9	SAIEL SR8	SAIEL SR7	SAIEL SR6	SAIEL SR5	SAIEL SR4	SAIEL SR3	SAIEL SR2	SAIEL SR1	SAIEL SR0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR31 to SAIELSR0	IELSR31到IELSR0寄存器的安全属性 0: Secure 1: Non-secure	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

SAIELSRn位（IELSR31至IELSR0寄存器的安全属性）

ArmCPUNVIC中管理的安全属性必须与IELSEn的安全属性匹配（n=0到31）。
NVIC内部寄存器位于NVIC_ITNS0[31:0]。NVIC_ITNS0和ICUSARG的初始值不同。
NVIC_ITNS0是安全的，而ICUSARG是不安全的。极性具有相同的含义，因此请对它们进行编程以匹配。

12.2.7 ICUSARH : Interrupt Controller Unit Security Attribution Register H

Base address: CPSCU = 0x4000_8000

Offset address: 0x74

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIELSR63	SAIELSR62	SAIELSR61	SAIELSR60	SAIELSR59	SAIELSR58	SAIELSR57	SAIELSR56	SAIELSR55	SAIELSR54	SAIELSR53	SAIELSR52	SAIELSR51	SAIELSR50	SAIELSR49	SAIELSR48
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIELSR47	SAIELSR46	SAIELSR45	SAIELSR44	SAIELSR43	SAIELSR42	SAIELSR41	SAIELSR40	SAIELSR39	SAIELSR38	SAIELSR37	SAIELSR36	SAIELSR35	SAIELSR34	SAIELSR33	SAIELSR32
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR63 to SAIELSR32	Security attributes of registers for IELSR63 to IELSR32 0: Secure 1: Non-secure	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SAIELSRn bits (Security attributes of registers for IELSR63 to IELSR32)

The Secure Attribute managed within the ARM CPU NVIC must match the security attribution of IELSEn (n = 32 to 63).
NVIC internal registers are in NVIC_ITNS1[31:0]. The initial values of NVIC_ITNS1 and ICUSARH are different.
NVIC_ITNS1 is secure and ICUSARH is non-secure. Polarity has the same meaning so program these to match.

12.2.8 ICUSARI : Interrupt Controller Unit Security Attribution Register I

Base address: CPSCU = 0x4000_8000

Offset address: 0x78

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIELSR95	SAIELSR94	SAIELSR93	SAIELSR92	SAIELSR91	SAIELSR90	SAIELSR89	SAIELSR88	SAIELSR87	SAIELSR86	SAIELSR85	SAIELSR84	SAIELSR83	SAIELSR82	SAIELSR81	SAIELSR80
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIELSR79	SAIELSR78	SAIELSR77	SAIELSR76	SAIELSR75	SAIELSR74	SAIELSR73	SAIELSR72	SAIELSR71	SAIELSR70	SAIELSR69	SAIELSR68	SAIELSR67	SAIELSR66	SAIELSR65	SAIELSR64
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR95 to SAIELSR64	Security attributes of registers for IELSR95 to IELSR64 0: Secure 1: Non-secure	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SAIELSRn bits (Security attributes of registers for IELSR95 to IELSR64)

The Secure Attribute managed within the ARM CPU NVIC must match the security attribution of IELSEn (n = 64 to 95).
NVIC internal registers are in NVIC_ITNS2[31:0]. The initial values of NVIC_ITNS2 and ICUSARI are different.
NVIC_ITNS2 is secure and ICUSARI is non-secure. Polarity has the same meaning so program these to match.

12.2.7 ICUSARH：中断控制器单元安全属性寄存器H

Base address: CPSCU = 0x4000_8000

Offset address: 0x74

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIELSR63	SAIELSR62	SAIELSR61	SAIELSR60	SAIELSR59	SAIELSR58	SAIELSR57	SAIELSR56	SAIELSR55	SAIELSR54	SAIELSR53	SAIELSR52	SAIELSR51	SAIELSR50	SAIELSR49	SAIELSR48
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIELSR47	SAIELSR46	SAIELSR45	SAIELSR44	SAIELSR43	SAIELSR42	SAIELSR41	SAIELSR40	SAIELSR39	SAIELSR38	SAIELSR37	SAIELSR36	SAIELSR35	SAIELSR34	SAIELSR33	SAIELSR32
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR63 to SAIELSR32	IELSR63到IELSR32寄存器的安全属性 0: Secure 1: Non-secure	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

SAIELSRn位（IELSR63至IELSR32寄存器的安全属性）

在ARMCPUNVIC中管理的安全属性必须与IELSEn的安全属性匹配（n=32到63）。
NVIC内部寄存器位于NVIC_ITNS1[31:0]中。NVIC_ITNS1和ICUSARH的初始值不同。
NVIC_ITNS1是安全的，而ICUSARH是不安全的。极性具有相同的含义，因此请对它们进行编程以匹配。

12.2.8 ICUSARI:中断控制器单元安全属性寄存器I

Base address: CPSCU = 0x4000_8000

Offset address: 0x78

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIELSR95	SAIELSR94	SAIELSR93	SAIELSR92	SAIELSR91	SAIELSR90	SAIELSR89	SAIELSR88	SAIELSR87	SAIELSR86	SAIELSR85	SAIELSR84	SAIELSR83	SAIELSR82	SAIELSR81	SAIELSR80
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIELSR79	SAIELSR78	SAIELSR77	SAIELSR76	SAIELSR75	SAIELSR74	SAIELSR73	SAIELSR72	SAIELSR71	SAIELSR70	SAIELSR69	SAIELSR68	SAIELSR67	SAIELSR66	SAIELSR65	SAIELSR64
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR95 to SAIELSR64	IELSR95到IELSR64寄存器的安全属性 0: Secure 1: Non-secure	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

SAIELSRn位（IELSR95至IELSR64寄存器的安全属性）

ARMCPUNVIC中管理的安全属性必须与IELSEn的安全属性相匹配（n=64到95）。
NVIC内部寄存器位于NVIC_ITNS2[31:0]中。NVIC_ITNS2和ICUSARI的初始值不同。
NVIC_ITNS2是安全的，而ICUSARI是不安全的。极性具有相同的含义，因此请对它们进行编程以匹配。

12.2.9 IRQCRi : IRQ Control Register (i = 0 to 15)

Base address: ICU = 0x4000_6000

Offset address: 0x000 + 0x1 × i

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FLTEN	—	FCLKSEL[1:0]		—	—	IRQMD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	IRQMD[1:0]	IRQi Detection Sense Select 0 0: Falling edge 0 1: Rising edge 1 0: Rising and falling edges 1 1: Low level	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
5:4	FCLKSEL[1:0]	IRQi Digital Filter Sampling Clock Select 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	FLTEN	IRQi Digital Filter Enable 0: Digital filter is disabled 1: Digital filter is enabled.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

IRQCRi register changes must satisfy the following conditions:

- For a CPU interrupt or DTC trigger:
  Change the IRQCRi register value before setting the target IELSRn register (n = 0 to 95).
  The register value should be changed only when the value of the target IELSRn register is 0x0000.
- For a DMAC trigger:
  Change the IRQCRi register value before setting the target DELSRn register (n = 0 to 7).
  The register value should be changed only when the value of the target DELSRn register is 0x0000.
- For a wakeup enable signal:
  Change the IRQCRi register setting before setting the target WUPEN0.IRQWUPEN[n] (n = 0 to 15). The register value should be changed when the target WUPEN0.IRQWUPEN[n] is 0.

IRQMD[1:0] bits (IRQi Detection Sense Select)

The IRQMD[1:0] bits set the detection sensing method for the IRQi external pin interrupt sources. For more information about the settings, see section 12.5.6. External Pin Interrupts.

FCLKSEL[1:0] bits (IRQi Digital Filter Sampling Clock Select)

The FCLKSEL[1:0] bits select the digital filter sampling clock for the IRQi external pin interrupt request pins, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles)

For details of the digital filter, see section 12.5.5. Digital Filter.

12.2.9 IRQCRi:IRQ控制寄存器(i=0to15)

Base address: ICU = 0x4000_6000

Offset address: 0x000 + 0x1 × i

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FLTEN	—	FCLKSEL[1:0]		—	—	IRQMD[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	IRQMD[1:0]	IRQi检测检测选择 00：下降沿01：上升沿10： 上升沿和下降沿11：低电平	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
5:4	FCLKSEL[1:0]	IRQi数字滤波器采样时钟选择 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	FLTEN	IRQi数字滤波器启用 0：禁用数字滤波器1：启 用数字滤波器。	R/W

Note: 如果安全属性配置为安全：●
- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

IRQCRi寄存器变更必须满足以下条件：

●对于CPU中断或DTC触发：
在设置目标IELSRn寄存器（n=0到95）之前更改IRQCRi寄存器值。
仅当目标IELSRn寄存器的值为0x0000时才应更改寄存器值。

- For a DMAC trigger:
  在设置目标DELSRn寄存器（n=0到7）之前更改IRQCRi寄存器值。
  仅当目标DELSRn寄存器的值为0x0000时，才应更改寄存器值。

●对于唤醒使能信号：
在设置目标WUPEN0.IRQWUPEN[n]（n=0到15）之前更改IRQCRi寄存器设置。当目标WUPEN0.IRQWUPEN[n]为0时，应更改寄存器值。

IRQMD[1:0]位（IRQi检测检测选择）

IRQMD[1:0]位设置IRQi外部引脚中断源的检测检测方法。有关设置的更多信息，请参阅第12.5.6节。外部引脚中断。

FCLKSEL[1:0]位（IRQi数字滤波器采样时钟选择）

FCLKSEL[1:0]位选择IRQi外部引脚中断请求引脚的数字滤波器采样时钟，可选择：

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles)

有关数字滤波器的详细信息，请参阅12.5.5节。数字滤波器。

FLTEN bit (IRQi Digital Filter Enable)

The FLTEN bit enables the digital filter used for the IRQi external pin interrupt sources. The digital filter is enabled when the IRQCRi.FLTEN bit is 1 and disabled when the IRQCRi.FLTEN bit is 0. The IRQi pin level is sampled at the clock cycle specified in the IRQCRi.FCLKSEL[1:0] bits. When the sampled level matches three times, the output level from the digital filter changes. For details of the digital filter, see section 12.5.5. Digital Filter.

12.2.10 NMISR : Non-Maskable Interrupt Status Register

Base address: ICU = 0x4000_6000

Offset address: 0x140

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPEST	—	TZFST	—	BUSMST	—	RECCST	RPEST	NMIST	OSTST	—	—	LVD2ST	LVD1ST	WDTST	IWDTST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTST	IWDT Underflow/Refresh Error Status Flag 0: Interrupt not requested 1: Interrupt requested	R
1	WDTST	WDT Underflow/Refresh Error Status Flag 0: Interrupt not requested 1: Interrupt requested	R
2	LVD1ST	Voltage Monitor 1 Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
3	LVD2ST	Voltage Monitor 2 Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
5:4	—	These bits are read as 0.	R
6	OSTST	Oscillation Stop Detection Interrupt Status Flag 0: Interrupt not requested for main oscillation stop 1: Interrupt requested for main oscillation stop	R
7	NMIST	NMI Status Flag 0: Interrupt not requested 1: Interrupt requested	R
8	RPEST	SRAM Parity Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
9	RECCST	SRAM ECC Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
10	—	This bit is read as 0.	R
11	BUSMST	MPU Bus Master Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
12	—	This bit is read as 0.	R
13	TZFST	TrustZone Filter Error Status Flag 0: Interrupt not requested 1: Interrupt requested	R
14	—	This bit is read as 0.	R
15	CPEST	Cache RAM Parity Error Status Flag 0: Interrupt not requested 1: Interrupt requested	R

FLTEN位（IRQi数字滤波器使能）

FLTEN位使能用于IRQi外部引脚中断源的数字滤波器。数字滤波器在IRQCRi.FLTEN位为1时启用，在IRQCRi.FLTEN位为0时禁用。IRQi引脚电平在IRQCRi.FCLKSEL[1:0]位指定的时钟周期内采样。当采样电平匹配3次时，数字滤波器的输出电平会发生变化。有关数字滤波器的详细信息，请参阅12.5.5节。数字滤波器。

12.2.10 NMISR：不可屏蔽中断状态寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x140

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPEST	—	TZFST	—	BUSMST	—	RECCST	RPEST	NMIST	OSTST	—	—	LVD2ST	LVD1ST	WDTST	IWDTST
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTST	IWDT下溢刷新错误状态标志 0：未请求中断1：请求中断	R
1	WDTST	WDT下溢刷新错误状态标志 0：未请求中断1：请求中断	R
2	LVD1ST	电压监视器1中断状态标志 0：未请求中断1：请求中断	R
3	LVD2ST	电压监视器2中断状态标志 0：未请求中断1：请求中断	R
5:4	—	这些位读为0。	R
6	OSTST	振荡停止检测中断状态标志 0：主振荡停止时不请求中断1：主振荡停止时请求中断	R
7	NMIST	NMI状态标志 0：未请求中断1：请求中断	R
8	RPEST	SRAM奇偶校验错误中断状态标志 0：未请求中断1：请求中断	R
9	RECCST	SRAMECC错误中断状态标志 0：未请求中断1：请求中断	R
10	—	该位读为0。	R
11	BUSMST	MPU总线主机错误中断状态标志 0：未请求中断1：请求中断	R
12	—	该位读为0。	R
13	TZFST	TrustZone过滤器错误状态标志 0：未请求中断1：请求中断	R
14	—	该位读为0。	R
15	CPEST	高速缓存RAM奇偶校验错误状态标志 0：未请求中断1：请求中断	R

The NMISR register monitors the status of non-maskable interrupt sources. Writes to the NMISR register are ignored. The setting in the Non-Maskable Interrupt Enable Register (NMIER) does not affect the status flags in this register. Before the end of the non-maskable interrupt handler, check that all of the bits in this register are set to 0 to confirm that no other NMI requests are generated during handler processing.

IWDTST flag (IWDT Underflow/Refresh Error Status Flag)

The IWDTST flag indicates an IWDT underflow/refresh error interrupt request. It is read-only and cleared by the NMICLR.IWDTCLR bit.

[Setting condition]

When the IWDT underflow/refresh error interrupt is generated and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.IWDTCLR bit.

WDTST flag (WDT Underflow/Refresh Error Status Flag)

The WDTST flag indicates a WDT underflow/refresh error interrupt request. It is read-only and cleared by the NMICLR.WDTCLR bit.

[Setting condition]

When the WDT underflow/refresh error interrupt is generated.

[Clearing condition]

When 1 is written to the NMICLR.WDTCLR bit.

LVD1ST flag (Voltage Monitor 1 Interrupt Status Flag)

The LVD1ST flag indicates a request for voltage monitor 1 interrupt. It is read-only and cleared by the NMICLR.LVD1CLR bit.

[Setting condition]

When the voltage monitor 1 interrupt is generated and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.LVD1CLR bit.

LVD2ST flag (Voltage Monitor 2 Interrupt Status Flag)

The LVD2ST flag indicates a request for voltage monitor 2 interrupt. It is read-only and cleared by the NMICLR.LVD2CLR bit.

[Setting condition]

When the voltage monitor 2 interrupt is generated and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.LVD2CLR bit.

OSTST flag (Oscillation Stop Detection Interrupt Status Flag)

The OSTST flag indicates an oscillation stop detection interrupt request. It is read-only and cleared by the NMICLR.OSTCLR bit.

[Setting condition]

When the main oscillation stop detection interrupt is generated.

[Clearing condition]

When 1 is written to the NMICLR.OSTCLR bit.

NMIST flag (NMI Status Flag)

The NMIST flag indicates an NMI pin interrupt request. It is read-only and cleared by the NMICLR.NMICLR bit.

[Setting condition]

When an edge specified by the NMICR.NMIMD bit is input to the NMI pin.

NMISR寄存器监视不可屏蔽中断源的状态。忽略对NMISR寄存器的写入。不可屏蔽中断使能寄存器(NMIER)中的设置不会影响该寄存器中的状态标志。在不可屏蔽中断处理程序结束之前，检查该寄存器中的所有位是否都设置为0，以确认在处理程序处理期间没有产生其他NMI请求。

IWDTST标志（IWDT下溢刷新错误状态标志）

IWDTST标志指示IWDT下溢刷新错误中断 请求。它是只读的并由NMICLR.IWDTCLR bit.

[Setting condition]

当IWDT下溢刷新错误中断 产生并且该中断源被使能时。

[Clearing condition]

当1写入NMICLR.IWDTCLR位时。

WDTST标志（WDT下溢刷新错误状态标志）

WDTST标志指示WDT下溢刷新错误中断 请求。它是只读的并由NMICLR.WDTCLR bit.

[Setting condition]

当产生WDT下溢刷新错误中断 时。

[Clearing condition]

当1写入NMICLR.WDTCLR位时。

LVD1ST标志（电压监视器1中断状态标志）

LVD1ST标志指示电压监视器1中断请求。它是只读的，由NMICLR.LVD1CLR位清零。

[Setting condition]

当电压监视器1中断产生并且该中断源被使能时。

[Clearing condition]

当1写入NMICLR.LVD1CLR位时。

LVD2ST标志（电压监视器2中断状态标志）

LVD2ST标志指示电压监视器2中断请求。它是只读的，由NMICLR.LVD2CLR位清零。

[Setting condition]

当电压监视器2中断产生并且该中断源被使能时。

[Clearing condition]

当1写入NMICLR.LVD2CLR位时。

OSTST标志（振荡停止检测中断状态标志）

OSTST标志表示振荡停止检测中断请求。它是只读的并由NMICLR.OSTCLR bit.

[Setting condition]

当产生主振荡停止检测中断时。

[Clearing condition]

当1写入NMICLR.OSTCLR位时。

NMIST标志（NMI状态标志）

NMIST标志指示NMI引脚中断请求。它是只读的，由NMICLR.NMICLR位清零。

[Setting condition]

当NMICR.NMIMD位指定的边沿输入到NMI引脚时。

[Clearing condition]

When 1 is written to the NMICLR.NMICLR bit.

RPEST flag (SRAM Parity Error Interrupt Status Flag)

The RPEST flag indicates an SRAM parity error interrupt request.

[Setting condition]

When an interrupt is generated in response to an SRAM parity error.

[Clearing condition]

When 1 is written to the NMICLR.RPECLR bit.

RECCST flag (SRAM ECC Error Interrupt Status Flag)

The RECCST flag indicates an SRAM ECC error interrupt request.

[Setting condition]

When an interrupt is generated in response to an SRAM ECC error.

[Clearing condition]

When 1 is written to the NMICLR.RECCCLR bit.

BUSMST flag (MPU Bus Master Error Interrupt Status Flag)

The BUSMST flag indicates a bus master error interrupt request.

[Setting condition]

When an interrupt is generated in response to a bus master error.

[Clearing condition]

When 1 is written to the NMICLR.BUSMCLR bit.

TZFST flag (TrustZone Filter Error Status Flag)

This flag indicates the TrustZone Filter error interrupt request.

[Setting condition]

When an interrupt is generated in response to a TrustZone Filter error

[Clearing condition]

When 1 is written to the NMICLR.TZFCLR bit

CPEST flag (Cache RAM Parity Error Status Flag)

This flag indicates the Cache RAM Parity error interrupt request.

[Setting condition]

When an interrupt is generated in response to an Cache RAM Parity error

[Clearing condition]

When 1 is written to the NMICLR.CPECLR bit

12.2.11 NMIER : Non-Maskable Interrupt Enable Register

Base address: ICU = 0x4000_6000

Offset address: 0x120

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPEEN	—	TZFEN	—	BUSMEN	—	RECCEN	RPEEN	NMIEN	OSTEN	—	—	LVD2EN	LVD1EN	WDTEN	IWDTEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Clearing condition]

当1写入NMICLR.NMICLR位时。

RPEST标志（SRAM奇偶校验错误中断状态标志）

RPEST标志指示SRAM奇偶校验错误中断请求。

[Setting condition]

当响应SRAM奇偶校验错误而产生中断时。

[Clearing condition]

当1写入NMICLR.RPECLR位时。

RECCST标志（SRAMECC错误中断状态标志）

RECCST标志指示SRAMECC错误中断请求。

[Setting condition]

当响应SRAMECC错误而产生中断时。

[Clearing condition]

当1写入NMICLR.RECCCLR位时。

BUSMST标志（MPU总线主机错误中断状态标志）

BUSMST标志指示总线主机错误中断请求。

[Setting condition]

当响应总线主机错误而产生中断时。

[Clearing condition]

当1写入NMICLR.BUSMCLR位时。

TZFST标志（TrustZone过滤器错误状态标志）

该标志指示TrustZoneFilter错误中断请求。

[Setting condition]

当响应TrustZone过滤器错误而生成中断时

[Clearing condition]

当1写入NMICLR.TZFCLR位时

CPEST标志（高速缓存RAM奇偶校验错误状态标志）

该标志指示缓存RAM奇偶校验错误中断请求。

[Setting condition]

当响应高速缓存RAM奇偶校验错误而产生中断时

[Clearing condition]

当1写入NMICLR.CPECLR位时

12.2.11 NMIER:不可屏蔽中断使能寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x120

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPEEN	—	TZFEN	—	BUSMEN	—	RECCEN	RPEEN	NMIEN	OSTEN	—	—	LVD2EN	LVD1EN	WDTEN	IWDTEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTEN	IWDT Underflow/Refresh Error Interrupt Enable 0: Disabled 1: Enabled.	R/W*1 *2
1	WDTEN	WDT Underflow/Refresh Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
2	LVD1EN	Voltage monitor 1 Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
3	LVD2EN	Voltage monitor 2 Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	OSTEN	Oscillation Stop Detection Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
7	NMIEN	NMI Pin Interrupt Enable 0: Disabled 1: Enabled	R/W*1
8	RPEEN	SRAM Parity Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1
9	RECCEN	SRAM ECC Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1
10	—	This bit is read as 0. The write value should be 0.	R/W
11	BUSMEN	MPU Bus Master Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1
12	—	This bit is read as 0. The write value should be 0.	R/W
13	TZFEN	TrustZone Filter Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1
14	—	This bit is read as 0. The write value should be 0.	R/W
15	CPEEN	Cache RAM Parity Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. You can write 1 to this bit only once after reset. Subsequent write accesses are invalid. Writing 0 to this bit is invalid.
Note 2. Do not write 1 to this bit when the source is used as an event signal.

IWDTEN bit (IWDT Underflow/Refresh Error Interrupt Enable)

The IWDTEN bit enables IWDT underflow/refresh error interrupt as an NMI trigger.

WDTEN bit (WDT Underflow/Refresh Error Interrupt Enable)

The WDTEN bit enables WDT underflow/refresh error interrupt as an NMI trigger.

LVD1EN bit (Voltage monitor 1 Interrupt Enable)

The LVD1EN bit enables voltage monitor 1 interrupt as an NMI trigger.

LVD2EN bit (Voltage monitor 2 Interrupt Enable)

The LVD2EN bit enables voltage monitor 2 interrupt as an NMI trigger.

Bit	Symbol	Function	R/W
0	IWDTEN	IWDT下溢刷新错误中断 使能 0：禁用1： 启用。	R/W*1 *2
1	WDTEN	WDT下溢刷新错误中断 使能 0：禁用1： 启用	R/W*1 *2
2	LVD1EN	电压监视器1中断使能 0：禁用1： 启用	R/W*1 *2
3	LVD2EN	电压监视器2中断使能 0：禁用1： 启用	R/W*1 *2
5:4	—	这些位被读取为0。写入值应为0。	R/W
6	OSTEN	振荡停止检测中断使能 0：禁用1： 启用	R/W*1 *2
7	NMIEN	NMI引脚中断使能 0：禁用1： 启用	R/W*1
8	RPEEN	SRAM奇偶校验错误中断使能 0：禁用1： 启用	R/W*1
9	RECCEN	SRAMECC错误中断使能 0：禁用1： 启用	R/W*1
10	—	该位读取为0。写入值应为0。	R/W
11	BUSMEN	MPU总线主机错误中断使能 0：禁用1： 启用	R/W*1
12	—	该位读取为0。写入值应为0。	R/W
13	TZFEN	TrustZone过滤器错误中断启用 0：禁用1： 启用	R/W*1
14	—	该位读取为0。写入值应为0。	R/W
15	CPEEN	高速缓存RAM奇偶校验错误中断使能 0：禁用1： 启用	R/W*1

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.复位后您只能向该位写入1一次。随后的写访问无效。向该位写入0无效。
注2.当源用作事件信号时，请勿向该位写入1。

IWDTEN位（IWDT下溢刷新错误中断 允许）

IWDTEN位使能IWDT下溢刷新错误中断 作为NMI触发。

WDTEN位（WDT下溢刷新错误中断 允许）

WDTEN位使能WDT下溢刷新错误中断 作为NMI触发。

LVD1EN位（电压监视器1中断允许）

LVD1EN位使能电压监视器1中断作为NMI触发。

LVD2EN位（电压监视器2中断允许）

LVD2EN位使能电压监视器2中断作为NMI触发。

OSTEN bit (Oscillation Stop Detection Interrupt Enable)

The OSTEN bit enables main oscillation stop detection interrupt as an NMI trigger.

NMIEN bit (NMI Pin Interrupt Enable)

The NMIEN bit enables NMI pin interrupt as an NMI trigger.

RPEEN bit (SRAM Parity Error Interrupt Enable)

The RPEEN bit enables SRAM parity error interrupt as an NMI trigger.

RECCEN bit (SRAM ECC Error Interrupt Enable)

The RECCEN bit enables SRAM ECC error interrupt as an NMI trigger.

BUSMEN bit (MPU Bus Master Error Interrupt Enable)

The BUSMEN bit enables bus master error interrupt as an NMI trigger.

TZFEN bit (TrustZone Filter Error Interrupt Enable)

TZFEN bit enables the TrustZone Filter error interrupt as an NMI trigger.

CPEEN bit (Cache RAM Parity Error Interrupt Enable)

CPEEN bit enables the Cache RAM Parity error interrupt as an NMI trigger.

12.2.12 NMICLR : Non-Maskable Interrupt Status Clear Register

Base address: ICU = 0x4000_6000

Offset address: 0x130

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPECLR	—	TZFCLR	—	BUSMCLR	—	RECCCLR	RPECLR	NMICLR	OSTCLR	—	—	LVD2CLR	LVD1CLR	WDTCLR	IWDTCLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTCLR	IWDT Underflow/Refresh Error Status Flag Clear 0: No effect 1: Clear the NMISR.IWDTST flag	R/W*1
1	WDTCLR	WDT Underflow/Refresh Error Status Flag Clear 0: No effect 1: Clear the NMISR.WDTST flag	R/W*1
2	LVD1CLR	Voltage Monitor 1 Interrupt Status Flag Clear 0: No effect 1: Clear the NMISR.LVD1ST flag	R/W*1
3	LVD2CLR	Voltage Monitor 2 Interrupt Status Flag Clear 0: No effect 1: Clear the NMISR.LVD2ST flag.	R/W*1
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	OSTCLR	Oscillation Stop Detection Interrupt Status Flag Clear 0: No effect 1: Clear the NMISR.OSTST flag	R/W*1
7	NMICLR	NMI Status Flag Clear 0: No effect 1: Clear the NMISR.NMIST flag	R/W*1
8	RPECLR	SRAM Parity Error Clear 0: No effect 1: Clear the NMISR.RPEST flag	R/W*1

OSTEN位（振荡停止检测中断使能）

OSTEN位使能主振荡停止检测中断作为NMI触发。

NMIEN位（NMI引脚中断允许）

NMIEN位使能NMI引脚中断作为NMI触发器。

RPEEN位（SRAM奇偶校验错误中断使能）

RPEEN位启用SRAM奇偶校验错误中断作为NMI触发器。

RECCEN位（SRAMECC错误中断允许）

RECCEN位启用SRAMECC错误中断作为NMI触发器。

BUSMEN位（MPU总线主机错误中断允许）

BUSMEN位使能总线主机错误中断作为NMI触发器。

TZFEN位（TrustZone过滤器错误中断使能）

TZFEN位启用TrustZone过滤器错误中断作为NMI触发器。

CPEEN位（高速缓存RAM奇偶校验错误中断使能）

CPEEN位启用缓存RAM奇偶校验错误中断作为NMI触发器。

12.2.12 NMICLR:不可屏蔽中断状态清除寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x130

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPECLR	—	TZFCLR	—	BUSMCLR	—	RECCCLR	RPECLR	NMICLR	OSTCLR	—	—	LVD2CLR	LVD1CLR	WDTCLR	IWDTCLR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTCLR	IWDT下溢刷新错误状态标志清除 0：无效1：清除NMISR.IWDTST标志	R/W*1
1	WDTCLR	WDT下溢刷新错误状态标志清除 0：无效1：清除NMISR.WDTST标志	R/W*1
2	LVD1CLR	电压监视器1中断状态标志清除 0：无效1：清除NMISR.LVD1ST标志	R/W*1
3	LVD2CLR	电压监视器2中断状态标志清除 0：无效1：清除NMISR.LVD2ST标志。	R/W*1
5:4	—	这些位被读取为0。写入值应为0。	R/W
6	OSTCLR	振荡停止检测中断状态标志清零 0：无效1：清除NMISR.OSTST标志	R/W*1
7	NMICLR	NMI状态标志清除 0：无效1：清除NMISR.NMIST标志	R/W*1
8	RPECLR	SRAM奇偶校验错误清除 0：无效1：清除NMISR.RPEST标志	R/W*1

Bit	Symbol	Function	R/W
9	RECCCLR	SRAM ECC Error Clear 0: No effect 1: Clear the NMISR.RECCST flag	R/W*1
10	—	This bit is read as 0. The write value should be 0.	R/W
11	BUSMCLR	Bus Master Error Clear 0: No effect 1: Clear the NMISR.BUSMST flag	R/W*1
12	—	This bit is read as 0. The write value should be 0.	R/W
13	TZFCLR	TrustZone Filter Error Clear 0: No effect 1: Clear the NMISR.TZFCLR flag	R/W*1
14	—	This bit is read as 0. The write value should be 0.	R/W
15	CPECLR	Cache RAM Parity Error Clear 0: No effect 1: Clear the NMISR.CPECLR flag	R/W*1

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Only write 1 to this bit.

IWDTCLR bit (IWDT Underflow/Refresh Error Status Flag Clear)

Writing 1 to the IWDTCLR bit clears the NMISR.IWDTST flag. This bit is read as 0.

WDTCLR bit (WDT Underflow/Refresh Error Status Flag Clear)

Writing 1 to the WDTCLR bit clears the NMISR.WDTST flag. This bit is read as 0.

LVD1CLR bit (Voltage Monitor 1 Interrupt Status Flag Clear)

Writing 1 to the LVD1CLR bit clears the NMISR.LVD1ST flag. This bit is read as 0.

LVD2CLR bit (Voltage Monitor 2 Interrupt Status Flag Clear)

Writing 1 to the LVD2CLR bit clears the NMISR.LVD2ST flag. This bit is read as 0.

OSTCLR bit (Oscillation Stop Detection Interrupt Status Flag Clear)

Writing 1 to the OSTCLR bit clears the NMISR.OSTST flag. This bit is read as 0.

NMICLR bit (NMI Status Flag Clear)

Writing 1 to the NMICLR bit clears the NMISR.NMIST flag. This bit is read as 0.

RPECLR bit (SRAM Parity Error Clear)

Writing 1 to the RPECLR bit clears the NMISR.RPEST flag. This bit is read as 0.

RECCCLR bit (SRAM ECC Error Clear)

Writing 1 to the RECCCLR bit clears the NMISR.RECCST flag. This bit is read as 0.

BUSMCLR bit (Bus Master Error Clear)

Writing 1 to the BUSMCLR bit clears the NMISR.BUSMST flag. This bit is read as 0.

TZFCLR bit (TrustZone Filter Error Clear)

Writing 1 to the TZFCLR bit clears the NMISR.TZFST flag. This bit is read as 0.

CPECLR bit (Cache RAM Parity Error Clear)

Writing 1 to the CPECLR bit clears the NMISR.CPEST flag. This bit is read as 0.

Bit	Symbol	Function	R/W
9	RECCCLR	SRAMECC错误清除 0：无效1：清除NMISR.RECCST标志	R/W*1
10	—	该位读取为0。写入值应为0。	R/W
11	BUSMCLR	总线主机错误清除 0：无效1：清除NMISR.BUSMST标志	R/W*1
12	—	该位读取为0。写入值应为0。	R/W
13	TZFCLR	TrustZone过滤器错误清除 0：无效1：清除NMISR.TZFCLR标志	R/W*1
14	—	该位读取为0。写入值应为0。	R/W
15	CPECLR	高速缓存RAM奇偶校验错误清除 0：无效1：清除NMISR.CPECLR标志	R/W*1

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.仅向该位写入1。

IWDTCLR位（IWDT下溢刷新错误状态标志清除）

将1写入IWDTCLR位会清除NMISR.IWDTST标志。该位读为0。

WDTCLR位（WDT下溢刷新错误状态标志清除）

将1写入WDTCLR位会清除NMISR.WDTST标志。该位读为0。

LVD1CLR位（电压监视器1中断状态标志清除）

将1写入LVD1CLR位会清除NMISR.LVD1ST标志。该位读为0。

LVD2CLR位（电压监视器2中断状态标志清除）

将1写入LVD2CLR位会清除NMISR.LVD2ST标志。该位读为0。

OSTCLR位（振荡停止检测中断状态标志清除）

将1写入OSTCLR位会清除NMISR.OSTST标志。该位读为0。

NMICLR位（NMI状态标志清除）

将1写入NMICLR位会清除NMISR.NMIST标志。该位读为0。

RPECLR位（SRAM奇偶校验错误清除）

将1写入RPECLR位会清除NMISR.RPEST标志。该位读为0。

RECCCLR位（SRAMECC错误清除）

将1写入RECCCLR位会清除NMISR.RECCST标志。该位读为0。

BUSMCLR位（总线主机错误清除）

将1写入BUSMCLR位会清除NMISR.BUSMST标志。该位读为0。

TZFCLR位（TrustZone过滤器错误清除）

将1写入TZFCLR位会清除NMISR.TZFST标志。该位读为0。

CPECLR位（高速缓存RAM奇偶校验错误清除）

将1写入CPECLR位会清除NMISR.CPEST标志。该位读为0。

12.2.13 NMICR : NMI Pin Interrupt Control Register

Base address: ICU = 0x4000_6000

Offset address: 0x100

Bit position:	7	6	5	4	3	2	1	0
Bit field:	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	NMIMD	NMI Detection Set 0: Falling edge 1: Rising edge	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
5:4	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock Select 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	NFLTEN	NMI Digital Filter Enable 0: Disabled 1: Enabled	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Change the NMICR register settings before enabling NMI pin interrupts, that is, before setting NMIER.NMIEN to 1.

NMIMD bit (NMI Detection Set)

The NMIMD bit selects the detection sensing method for the NMI pin interrupts.

NFCLKSEL[1:0] bits (NMI Digital Filter Sampling Clock Select)

The NFCLKSEL[1:0] bits select the digital filter sampling clock for the NMI pin interrupts, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles)

For details of the digital filter, see section 12.5.5. Digital Filter.

NFLTEN bit (NMI Digital Filter Enable)

The NFLTEN bit enables the digital filter used for NMI pin interrupts. The filter is enabled when NFLTEN is 1, and disabled when NFLTEN is 0. The NMI pin level is sampled at the clock cycle specified in NFCLKSEL[1:0]. When the sampled level matches three times, the output level from the digital filter changes. For details of the digital filter, see section 12.5.5. Digital Filter.

12.2.13 NMICR:NMI引脚中断控制寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x100

Bit position:	7	6	5	4	3	2	1	0
Bit field:	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	NMIMD	NMI检测集 0：下降沿1： 上升沿	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
5:4	NFCLKSEL[1:0]	NMI数字滤波器采样时钟选择 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	NFLTEN	NMI数字滤波器启用 0：禁用1： 启用	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在启用NMI引脚中断之前更改NMICR寄存器设置，即将NMIER.NMIEN设置为1。

NMIMD位（NMI检测集）

NMIMD位选择NMI引脚中断的检测检测方法。

NFCLKSEL[1:0]位（NMI数字滤波器采样时钟选择）

NFCLKSEL[1:0]位选择用于NMI引脚中断的数字滤波器采样时钟，可选择：

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles)

有关数字滤波器的详细信息，请参阅12.5.5节。数字滤波器。

NFLTEN位（NMI数字滤波器使能）

NFLTEN位使能用于NMI引脚中断的数字滤波器。滤波器在NFLTEN为1时启用，在NFLTEN为0时禁用。NMI引脚电平在NFCLKSEL[1:0]中指定的时钟周期进行采样。当采样电平匹配3次时，数字滤波器的输出电平会发生变化。有关数字滤波器的详细信息，请参阅12.5.5节。数字滤波器。

12.2.14 IELSRn : ICU Event Link Setting Register n (n = 0 to 95)

Base address: ICU = 0x4000_6000

Offset address: 0x300 + 0x4 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	DTCE	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	IELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	IELS[8:0]	ICU Event Link Select 0x00: Disable interrupts to the associated NVIC or DTC module Others: Event signal number to be linked. For details, see section 12.3.2. Event Number.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	IR	Interrupt Status Flag 0: No interrupt request generated. 1: An interrupt request is generated.	R/W*1
23:17	—	These bits are read as 0. The write value should be 0.	R/W
24	DTCE	DTC Activation Enable 0: DTC activation is disabled. 1: DTC activation is enabled.	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: This register requires halfword or word access.

Note 1. Writing 1 to the IR flag is prohibited.

The IELSRn register selects the IRQi source used by the NVIC. For details, see Table 12.3. IELSRn corresponds to the NVIC IRQ input source number, where n = 0 to 95.

IELS[8:0] bits (ICU Event Link Select)

The IELS[8:0] bits link an event signal to the associated NVIC or DTC module. Event options are classified into 8 groups (groups 0 to 7). For details, see Table 12.3 and Table 12.4.

IR flag (Interrupt Status Flag)

The IR status flag indicates an individual interrupt request from the event specified in IELS[8:0].

[Setting condition]

When an interrupt request is received from the associated peripheral module or IRQi pin.

[Clearing condition]

- The IR flag is cleared to 0 by writing 0.
- In the case of DTC.DISEL = 0. At the time other than the final transfer end in DTC transfer during DTCE = 1, IR flag repeat set and cleared by Hardware.
- In the case of DTC.DISEL = 1. For DTC transfers during DTCE = 1, the hardware does not clear the IR flag. Should be cleared by the CPU writing 0.

When DTC transfer except last transfer is completed (DTCE bit is changed from 1 to 0).

During DTCE = 1, write 0 to IR register is prohibited.

12.2.14 IELSRn:ICU事件链接设置寄存器n(n=0到95)

Base address: ICU = 0x4000_6000

Offset address: 0x300 + 0x4 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	DTCE	—	—	—	—	—	—	—	IR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	IELS[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	IELS[8:0]	ICU事件链接选择 0x00：禁用相关NVIC或DTC模块的中断 其他：要链接的事件信号编号。详见12.3.2节。事件编号。	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
16	IR	中断状态标志 0：不产生中断请求。1：产生中断请求。	R/W*1
23:17	—	这些位被读取为0。写入值应为0。	R/W
24	DTCE	DTC激活启用 0：禁用DTC激活。1：启用DTC激活。	R/W
31:25	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 该寄存器需要半字或字访问。

注1.禁止向IR标志写入1。

IELSRn寄存器选择NVIC使用的IRQi源。详见表12.3。IELSRn对应于NVICIRQ输入源编号，其中n=0到95。

IELS[8:0]位（ICU事件链接选择）

IELS[8:0]位将事件信号链接到相关的NVIC或DTC模块。事件选项分为8组（组0到7）。详见表12.3和表12.4。

IR标志（中断状态标志）

IR状态标志指示来自IELS[8:0]中指定事件的单个中断请求。

[Setting condition]

当从相关外设模块或IRQi引脚接收到中断请求时。

[Clearing condition]

●IR标志通过写入0清除为0。

●在DTC.DISEL=0的情况下。在DTCE=1期间DTC传输的最后传输结束以外的时间，IR标志重复由硬件设置和清除。

●在DTC.DISEL=1的情况下。对于DTCE=1期间的DTC传输，硬件不会清除IR标志。应由CPU写入0清除。

完成最后一次传输以外的DTC传输时（DTCE位从1变为0）。

在DTCE=1期间，禁止向IR寄存器写入0。

In the case of level detection, clear of the IR flag should follow the steps below.

1. Negate the input interrupt signal.
2. Read access the peripheral once and wait for 2 clock cycles of the target module clock.
3. Clear the IR flag by writing 0.

DTCE bit (DTC Activation Enable)

When the DTCE bit is set to 1, the associated event is selected as the source for DTC activation.

[Setting condition]

- When 1 is written to the DTCE bit.

[Clearing condition]

- When the specified number of transfers is complete. For chain transfers, when the specified number of transfers for the last chain transfer is complete.
- When 0 is written to the DTCE bit.

Note: Error during DTC transfer

If an error response occurs during DTC transfer, the DTC notifies the ICU that an error has occurred. ICU clears all bits of the target IELSRn (n = 0 to 95). IELSRn that is not the target is not cleared.

Note: DTC transfer error in snooze mode

When an error occurs in DTC transfer in Snooze mode, ICU issues a wakeup request. However, interrupt requests are not issued automatically. See section 16, Data Transfer Controller (DTC) for how to set the interrupt when a DTC error occurs.

12.2.15 DELSRn : DMAC Event Link Setting Register n (n = 0 to 7)

Base address: ICU = 0x4000_6000

Offset address: 0x280 + 0x4 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DELS[8:0]	DMAC Event Link Select 0x00: Disable interrupts to the associated DMAC module Others: Event signal number to be linked. For details, see Table 12.4.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	IR	DMAC Activation Request Status flag 0: No DMAC activation request occurred 1: DMAC activation request occurred.	R/W*1
31:17	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Writing 1 to the IR flag is prohibited.

在电平检测的情况下，清除IR标志应遵循以下步骤。

1.取反输入中断信号。

2.对外设进行一次读取访问，并等待目标模块时钟的2个时钟周期。

3.写0清除IR标志。

DTCE位（DTC激活使能）

当DTCE位设置为1时，相关事件被选为DTC激活源。

[Setting condition]

●当1写入DTCE位时。

[Clearing condition]

●当指定数量的传输完成时。对于链式转移，当最后一次链式转移的指定转移次数完成时。

●当0写入DTCE位时。

Note: DTC传输期间出错

如果在DTC传输期间发生错误响应，则DTC会通知ICU发生了错误。ICU清除目标IELSRn(n=0到95)的所有位。不是目标的IELSRn不会被清除。

Note: 贪睡模式下的DTC传输错误

当贪睡模式下的DTC传输发生错误时，ICU会发出唤醒请求。但是，不会自动发出中断请求。有关如何在发生DTC错误时设置中断，请参见第16节，数据传输控制器(DTC)。

12.2.15 DELSRn：DMAC事件链接设置寄存器n（n=0到7）

Base address: ICU = 0x4000_6000

Offset address: 0x280 + 0x4 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DELS[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DELS[8:0]	DMAC事件链接选择 0x00：禁用相关DMAC模块的中断 其他：要链接的事件信号编号。详见表12.4。	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
16	IR	DMAC激活请求状态标志 0：未发生DMAC激活请求1：发生DMAC激活请求。	R/W*1
31:17	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.禁止向IR标志写入1。

DELS[8:0] bit (DMAC Event Link Select)

The DELS[8:0] bits link an event signal to the associated DMAC module. Do not set the same event number in multiple DELSRn registers.

IR flag (DMAC Activation Request Status flag)

The IR flag is the status flag of a DMAC activation request. This flag is associated with the DELS[8:0] bits of this register.

[Setting condition]

- The flag is set to 1 when a DMAC activation request is generated from the associated peripheral module or IRQi pin.

[Clearing conditions]

- When 0 is written to the flag
- At the start of a DMA transfer after the DMAC activation request is issued.

Note: The IR flag is automatically cleared after completion of DMA transfer, so do not write 0 unless an abort occurs. DMA transfer operation when 0 is written cannot be guaranteed.

Note: Error during DMAC transfer

If an error response occurs during DMAC transfer, the DMAC notifies the ICU that an error has occurred.

The ICU clears all bits of the target channel of DELSRn (n = 0 to 7). DELSRn that is not the target channel is not cleared.

12.2.16 SELSR0 : SYS Event Link Setting Register

Base address: ICU = 0x4000_6000

Offset address: 0x200

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SELS[8:0]	SYS Event Link Select 0x00: Disable event output to the associated low-power mode module Others: Event signal number to be linked. For details, see Table 12.4.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The SELSR0 register selects the events that wake up the CPU from Snooze mode. You can use only the events listed in Table 12.4 checked as “Canceling Snooze mode using SELSR0”. Events specified in this register are defined as ICU_SNZCANCEL in Table 12.4. When ICU_SNZCANCEL is selected in the IELSRn.IELS[8:0] bits, the SELSR0 event interrupt occurs.

Caution: For security attribution added to parts related to a series of actions, make sure to match all security attribution so that security holes cannot be created.

About security attribution to be matched

- **Event source to be set to SELSR0.**
- **SELSR0**
- **IELSRn (n = 0 to 95) to receive event No. 45 (ICU_SNZCANCEL).**
- **NVIC internal registers in the CPU of the interrupt specified in the previous item.**
- **Interrupt Handler.**

DELS[8:0]位（DMAC事件链接选择）

DELS[8:0]位将事件信号链接到相关的DMAC模块。不要在多个中设置相同的事件编号
DELSRn registers.

IR标志（DMAC激活请求状态标志）

IR标志是DMAC激活请求的状态标志。该标志与该寄存器的DELS[8:0]位相关联。

[Setting condition]

●当相关外设模块或IRQi引脚产生DMAC激活请求时，该标志设置为1。

[Clearing conditions]

●标志写入0时

●在发出DMAC激活请求后开始DMA传输。

Note: IR标志在DMA传输完成后自动清除，因此除非发生中止，否则不要写0。无法保证写入0时的DMA传输操作。

Note: DMAC传输期间出错

如果在DMAC传输期间发生错误响应，则DMAC会通知ICU发生了错误。

ICU清除DELSRn（n=0到7）的目标通道的所有位。不是目标通道的DELSRn不会被清除。

12.2.16 SELSR0：SYS事件链接设置寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x200

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SELS[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SELS[8:0]	SYS事件链接选择 0x00：禁用到相关低功耗模式模块的事件输出 其他：要链接的事件信号编号。详见表12.4。	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

SELSR0寄存器选择将CPU从贪睡模式唤醒的事件。您只能使用中列出的事件
表12.4选中“使用SELSR0取消贪睡模式”。该寄存器中指定的事件定义为
ICU_SNZCANCEL在表12.4中。在IELSRn.IELS[8:0]位中选择ICU_SNZCANCEL时，将发生SELSR0事件中断。

Caution: 对于添加到与一系列动作相关的部分的安全属性，请确保匹配所有的安全属性，以免造成安全漏洞。

关于要匹配的安全属性●
事件源设置为SELSR0。

- **SELSR0**
- **IELSRn(n=0到95)接收事件编号45(ICU_SNZCANCEL)。**
- **上项指定的中断的CPU中的NVIC内部寄存器。**
- **中断处理程序。**

12.2.17 WUPEN0 : Wake Up Interrupt Enable Register 0

Base address: ICU = 0x4000_6000

Offset address: 0x1A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	IIC0WUPEN	AGT1CBWUPEN	AGT1CAWUPEN	AGT1UDWUPEN	—	—	—	—	—	—	—	—	LVD2WUPEN	LVD1WUPEN	KEYWUPEN	IWDTWUPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	IRQWUPEN[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	IRQWUPEN[15:0]	IRQn Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by IRQn interrupt is disabled 1: Software Standby/Snooze Mode returns by IRQn interrupt is enabled*1	R/W
16	IWDTWUPEN	IWDT Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by IWDT interrupt is disabled 1: Software Standby/Snooze Mode returns by IWDT interrupt is enabled	R/W
17	KEYWUPEN	Key interrupt S/W standby returns enable bit 0: S/W standby returns by KEY interrupt is disabled 1: S/W standby returns by KEY interrupt is enabled	R/W
18	LVD1WUPEN	LVD1 Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by LVD1 interrupt is disabled 1: Software Standby/Snooze Mode returns by LVD1 interrupt is enabled	R/W
19	LVD2WUPEN	LVD2 Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by LVD2 interrupt is disabled 1: Software Standby/Snooze Mode returns by LVD2 interrupt is enabled	R/W
27:20	—	These bits are read as 0. The write value should be 0.	R/W
28	AGT1UDWUPEN	AGT1 Underflow Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by AGT1 underflow interrupt is disabled 1: Software Standby/Snooze Mode returns by AGT1 underflow interrupt is enabled	R/W
29	AGT1CAWUPEN	AGT1 Compare Match A Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by AGT1 compare match A interrupt is disabled 1: Software Standby/Snooze Mode returns by AGT1 compare match A interrupt is enabled	R/W
30	AGT1CBWUPEN	AGT1 Compare Match B Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by AGT1 compare match B interrupt is disabled 1: Software Standby/Snooze Mode returns by AGT1 compare match B interrupt is enabled	R/W
31	IIC0WUPEN	IIC0 Address Match Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by IIC0 address match interrupt is disabled 1: Software Standby/Snooze Mode returns by IIC0 address match interrupt is enabled	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Description is a description of each bit.

12.2.17 WUPEN0:唤醒中断使能寄存器0

Base address: ICU = 0x4000_6000

Offset address: 0x1A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	IIC0WUPEN	AGT1CBWUPEN	AGT1CAWUPEN	AGT1UDWUPEN	—	—	—	—	—	—	—	—	LVD2WUPEN	LVD1WUPEN	KEYWUPEN	IWDTWUPEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	IRQWUPEN[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	IRQWUPEN[15:0]	IRQn中断软件待机贪睡模式返回使能位 0：禁用IRQn中断返回软件待机贪睡模式1：启用IRQn中断返回软件待机贪睡模式*1	R/W
16	IWDTWUPEN	IWDT中断软件待机贪睡模式返回使能位 0：禁止通过IWDT中断返回软件待机贪睡模式1：使能通过IWDT中断返回软件待机贪睡模式	R/W
17	KEYWUPEN	按键中断SW待机返回使能位 0：禁止通过KEY中断返回SW待机1：使能通过KEY中断返回SW待机	R/W
18	LVD1WUPEN	LVD1中断软件待机贪睡模式返回使能位 0：禁用LVD1中断返回软件待机贪睡模式1：启用LVD1中断返回软件待机贪睡模式	R/W
19	LVD2WUPEN	LVD2中断软件待机贪睡模式返回使能位 0：禁用LVD2中断返回软件待机贪睡模式1：启用LVD2中断返回软件待机贪睡模式	R/W
27:20	—	这些位被读取为0。写入值应为0。	R/W
28	AGT1UDWUPEN	AGT1下溢中断软件待机贪睡模式返回使能位 0：禁用AGT1下溢中断返回软件待机贪睡模式1：启用AGT1下溢中断返回软件待机贪睡模式	R/W
29	AGT1CAWUPEN	AGT1比较匹配中断软件待机贪睡模式返回使能位 0：软件待机贪睡模式由AGT1比较匹配返回A中断被禁用 1：软件待机贪睡模式由AGT1比较匹配返回启用中断	R/W
30	AGT1CBWUPEN	AGT1比较匹配B中断软件待机贪睡模式返回使能位 0：软件待机贪睡模式由AGT1比较匹配B中断被禁用返回 1：软件待机贪睡模式由AGT1比较匹配B中断启用	R/W
31	IIC0WUPEN	IIC0地址匹配中断软件待机贪睡模式返回使能位 0：软件待机贪睡模式由IIC0地址匹配中断返回被禁用 1：软件待机贪睡模式由IIC0地址匹配中断返回使能	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.描述是对每个位的描述。

IRQWUPEN[15:0] bits (IRQn Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the IRQn pin as a Software standby return factor.

n = 0 to 15

IWDTWUPEN bit (IWDT Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the IWDT interrupt as an Software standby return factor.

KEYWUPEN bit (Key interrupt S/W standby returns enable bit)

This bit is the enable bit to control the use of the KEY interrupt as an Software standby return factor.

LVD1WUPEN bit (LVD1 Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the LVD1 interrupt as an Software standby return factor.

LVD2WUPEN bit (LVD2 Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the LVD2 interrupt as an Software standby return factor.

AGT1UDWUPEN bit (AGT1 Underflow Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the AGT1 underflow interrupt as an Software standby return factor.

AGT1CAWUPEN bit (AGT1 Compare Match A Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the AGT1 compare match A interrupt as an Software standby return factor.

AGT1CBWUPEN bit (AGT1 Compare Match B Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the AGT1 compare match B interrupt as an Software standby return factor.

IIC0WUPEN bit (IIC0 Address Match Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the IIC0 interrupt as an Software standby return factor.

Note: The security attribution of this register is set for each wakeup event.
To avoid the occurrence of a security hole, the target event of a wakeup and the security attribution added to this bit must match.

12.3 Vector Table

The ICU detects maskable and non-maskable interrupts. Interrupt priorities are set up in the Arm NVIC. For information about these registers, see section 12.9. Reference.

12.3.1 Interrupt Vector Table

Table 12.3 describes the interrupt vector table. The interrupt vector addresses conform to the NVIC specifications.

Table 12.3 Interrupt vector table (1 of 4)

Exception number	IRQ number	Vector offset	Source	Description
0	—	0x000	Arm	Initial stack pointer
1	—	0x004	Arm	Initial program counter (reset vector)
2	—	0x008	Arm	Non-Maskable Interrupt (NMI)
3	—	0x00C	Arm	Hard Fault
4	—	0x010	Arm	MemManage fault
5	—	0x014	Arm	BusFault
6	—	0x018	Arm	UsageFault
7	—	0x01C	Arm	SecureFault

IRQWUPEN[15:0]位（IRQn中断软件待机贪睡模式返回使能位）

该位是控制使用IRQn引脚作为软件待机返回因子的使能位。

n = 0 to 15

IWDTWUPEN位（IWDT中断软件待机贪睡模式返回使能位）

该位是控制使用IWDT中断作为软件待机返回因素的使能位。

KEYWUPEN位（按键中断SW待机返回使能位）

该位是控制使用KEY中断作为软件待机返回因素的使能位。

LVD1WUPEN位（LVD1中断软件待机贪睡模式返回使能位）

该位是控制使用LVD1中断作为软件待机返回因素的使能位。

LVD2WUPEN位（LVD2中断软件待机贪睡模式返回使能位）

该位是控制使用LVD2中断作为软件待机返回因素的使能位。

AGT1UDWUPEN位（AGT1下溢中断软件待机贪睡模式返回使能位）

该位是控制使用AGT1下溢中断作为软件待机返回因素的使能位。

AGT1CAWUPEN位（AGT1比较匹配A中断软件待机贪睡模式返回使能位）

该位是控制使用AGT1比较匹配A中断作为软件待机返回因素的使能位。

AGT1CBWUPEN位（AGT1比较匹配B中断软件待机贪睡模式返回使能位）

该位是控制使用AGT1比较匹配B中断作为软件待机返回因素的使能位。

IIC0WUPEN位（IIC0地址匹配中断软件待机贪睡模式返回使能位）

该位是控制使用IIC0中断作为软件待机返回因素的使能位。

Note: 该寄存器的安全属性为每个唤醒事件设置。
为了避免安全漏洞的发生，唤醒的目标事件和添加到该位的安全属性必须匹配。

12.3 向量表

ICU检测可屏蔽和不可屏蔽中断。中断优先级在ArmNVIC中设置。有关这些寄存器的信息，请参阅第12.9节。参考。

12.3.1 中断向量表

表12.3描述了中断向量表。中断向量地址符合NVIC规范。

Table 12.3 中断向量表(1of4)

异常编号	IRQ number	矢量偏移	Source	Description
0	—	0x000	Arm	初始堆栈指针
1	—	0x004	Arm	初始程序计数器（复位向量）
2	—	0x008	Arm	Non-Maskable Interrupt (NMI)
3	—	0x00C	Arm	硬故障
4	—	0x010	Arm	MemManage fault
5	—	0x014	Arm	BusFault
6	—	0x018	Arm	UsageFault
7	—	0x01C	Arm	SecureFault

Table 12.3 Interrupt vector table (2 of 4)

Exception number	IRQ number	Vector offset	Source	Description
8	—	0x020	Arm	Reserved
9	—	0x024	Arm	Reserved
10	—	0x028	Arm	Reserved
11	—	0x02C	Arm	Supervisor Call (SVCall)
12	—	0x030	Arm	DebugMonitor
13	—	0x034	Arm	Reserved
14	—	0x038	Arm	Pendable request for system service (PendableSrvReq)
15	—	0x03C	Arm	System Tick Timer (SysTick)
16	0	0x040	ICU.IELSR0	Event selected in the ICU.IELSR0 register
17	1	0x044	ICU.IELSR1	Event selected in the ICU.IELSR1 register
18	2	0x048	ICU.IELSR2	Event selected in the ICU.IELSR2 register
19	3	0x04C	ICU.IELSR3	Event selected in the ICU.IELSR3 register
20	4	0x050	ICU.IELSR4	Event selected in the ICU.IELSR4 register
21	5	0x054	ICU.IELSR5	Event selected in the ICU.IELSR5 register
22	6	0x058	ICU.IELSR6	Event selected in the ICU.IELSR6 register
23	7	0x05C	ICU.IELSR7	Event selected in the ICU.IELSR7 register
24	8	0x060	ICU.IELSR8	Event selected in the ICU.IELSR8 register
25	9	0x064	ICU.IELSR9	Event selected in the ICU.IELSR9 register
26	10	0x068	ICU.IELSR10	Event selected in the ICU.IELSR10 register
27	11	0x06C	ICU.IELSR11	Event selected in the ICU.IELSR11 register
28	12	0x070	ICU.IELSR12	Event selected in the ICU.IELSR12 register
29	13	0x074	ICU.IELSR13	Event selected in the ICU.IELSR13 register
30	14	0x078	ICU.IELSR14	Event selected in the ICU.IELSR14 register
31	15	0x07C	ICU.IELSR15	Event selected in the ICU.IELSR15 register
32	16	0x080	ICU.IELSR16	Event selected in the ICU.IELSR16 register
33	17	0x084	ICU.IELSR17	Event selected in the ICU.IELSR17 register
34	18	0x088	ICU.IELSR18	Event selected in the ICU.IELSR18 register
35	19	0x08C	ICU.IELSR19	Event selected in the ICU.IELSR19 register
36	20	0x090	ICU.IELSR20	Event selected in the ICU.IELSR20 register
37	21	0x094	ICU.IELSR21	Event selected in the ICU.IELSR21 register
38	22	0x098	ICU.IELSR22	Event selected in the ICU.IELSR22 register
39	23	0x09C	ICU.IELSR23	Event selected in the ICU.IELSR23 register
40	24	0x0A0	ICU.IELSR24	Event selected in the ICU.IELSR24 register
41	25	0x0A4	ICU.IELSR25	Event selected in the ICU.IELSR25 register
42	26	0x0A8	ICU.IELSR26	Event selected in the ICU.IELSR26 register
43	27	0x0AC	ICU.IELSR27	Event selected in the ICU.IELSR27 register
44	28	0x0B0	ICU.IELSR28	Event selected in the ICU.IELSR28 register
45	29	0x0B4	ICU.IELSR29	Event selected in the ICU.IELSR29 register
46	30	0x0B8	ICU.IELSR30	Event selected in the ICU.IELSR30 register
47	31	0x0BC	ICU.IELSR31	Event selected in the ICU.IELSR31 register
48	32	0x0C0	ICU.IELSR32	Event selected in the ICU.IELSR32 register

Table 12.3 中断向量表(2of4)

异常编号	IRQ number	矢量偏移	Source	Description
8	—	0x020	Arm	Reserved
9	—	0x024	Arm	Reserved
10	—	0x028	Arm	Reserved
11	—	0x02C	Arm	主管呼叫(SVCall)
12	—	0x030	Arm	DebugMonitor
13	—	0x034	Arm	Reserved
14	—	0x038	Arm	系统服务的挂起请求(PendableSrvReq)
15	—	0x03C	Arm	系统滴答计时器(SysTick)
16	0	0x040	ICU.IELSR0	在ICU.IELSR0寄存器中选择的事件
17	1	0x044	ICU.IELSR1	在ICU.IELSR1寄存器中选择的事件
18	2	0x048	ICU.IELSR2	在ICU.IELSR2寄存器中选择的事件
19	3	0x04C	ICU.IELSR3	在ICU.IELSR3寄存器中选择的事件
20	4	0x050	ICU.IELSR4	在ICU.IELSR4寄存器中选择的事件
21	5	0x054	ICU.IELSR5	在ICU.IELSR5寄存器中选择的事件
22	6	0x058	ICU.IELSR6	在ICU.IELSR6寄存器中选择的事件
23	7	0x05C	ICU.IELSR7	在ICU.IELSR7寄存器中选择的事件
24	8	0x060	ICU.IELSR8	在ICU.IELSR8寄存器中选择的事件
25	9	0x064	ICU.IELSR9	在ICU.IELSR9寄存器中选择的事件
26	10	0x068	ICU.IELSR10	在ICU.IELSR10寄存器中选择的事件
27	11	0x06C	ICU.IELSR11	在ICU.IELSR11寄存器中选择的事件
28	12	0x070	ICU.IELSR12	在ICU.IELSR12寄存器中选择的事件
29	13	0x074	ICU.IELSR13	在ICU.IELSR13寄存器中选择的事件
30	14	0x078	ICU.IELSR14	在ICU.IELSR14寄存器中选择的事件
31	15	0x07C	ICU.IELSR15	在ICU.IELSR15寄存器中选择的事件
32	16	0x080	ICU.IELSR16	在ICU.IELSR16寄存器中选择的事件
33	17	0x084	ICU.IELSR17	在ICU.IELSR17寄存器中选择的事件
34	18	0x088	ICU.IELSR18	在ICU.IELSR18寄存器中选择的事件
35	19	0x08C	ICU.IELSR19	在ICU.IELSR19寄存器中选择的事件
36	20	0x090	ICU.IELSR20	在ICU.IELSR20寄存器中选择的事件
37	21	0x094	ICU.IELSR21	在ICU.IELSR21寄存器中选择的事件
38	22	0x098	ICU.IELSR22	在ICU.IELSR22寄存器中选择的事件
39	23	0x09C	ICU.IELSR23	在ICU.IELSR23寄存器中选择的事件
40	24	0x0A0	ICU.IELSR24	在ICU.IELSR24寄存器中选择的事件
41	25	0x0A4	ICU.IELSR25	在ICU.IELSR25寄存器中选择的事件
42	26	0x0A8	ICU.IELSR26	在ICU.IELSR26寄存器中选择的事件
43	27	0x0AC	ICU.IELSR27	在ICU.IELSR27寄存器中选择的事件
44	28	0x0B0	ICU.IELSR28	在ICU.IELSR28寄存器中选择的事件
45	29	0x0B4	ICU.IELSR29	在ICU.IELSR29寄存器中选择的事件
46	30	0x0B8	ICU.IELSR30	在ICU.IELSR30寄存器中选择的事件
47	31	0x0BC	ICU.IELSR31	在ICU.IELSR31寄存器中选择的事件
48	32	0x0C0	ICU.IELSR32	在ICU.IELSR32寄存器中选择的事件

Table 12.3 Interrupt vector table (3 of 4)

Exception number	IRQ number	Vector offset	Source	Description
49	33	0x0C4	ICU.IELSR33	Event selected in the ICU.IELSR33 register
50	34	0x0C8	ICU.IELSR34	Event selected in the ICU.IELSR34 register
51	35	0x0CC	ICU.IELSR35	Event selected in the ICU.IELSR35 register
52	36	0x0D0	ICU.IELSR36	Event selected in the ICU.IELSR36 register
53	37	0x0D4	ICU.IELSR37	Event selected in the ICU.IELSR37 register
54	38	0x0D8	ICU.IELSR38	Event selected in the ICU.IELSR38 register
55	39	0x0DC	ICU.IELSR39	Event selected in the ICU.IELSR39 register
56	40	0x0E0	ICU.IELSR40	Event selected in the ICU.IELSR40 register
57	41	0x0E4	ICU.IELSR41	Event selected in the ICU.IELSR41 register
58	42	0x0E8	ICU.IELSR42	Event selected in the ICU.IELSR42 register
59	43	0x0EC	ICU.IELSR43	Event selected in the ICU.IELSR43 register
60	44	0x0F0	ICU.IELSR44	Event selected in the ICU.IELSR44 register
61	45	0x0F4	ICU.IELSR45	Event selected in the ICU.IELSR45 register
62	46	0x0F8	ICU.IELSR46	Event selected in the ICU.IELSR46 register
63	47	0x0FC	ICU.IELSR47	Event selected in the ICU.IELSR47 register
64	48	0x100	ICU.IELSR48	Event selected in the ICU.IELSR48 register
65	49	0x104	ICU.IELSR49	Event selected in the ICU.IELSR49 register
66	50	0x108	ICU.IELSR50	Event selected in the ICU.IELSR50 register
67	51	0x10C	ICU.IELSR51	Event selected in the ICU.IELSR51 register
68	52	0x110	ICU.IELSR52	Event selected in the ICU.IELSR52 register
69	53	0x114	ICU.IELSR53	Event selected in the ICU.IELSR53 register
70	54	0x118	ICU.IELSR54	Event selected in the ICU.IELSR54 register
71	55	0x11C	ICU.IELSR55	Event selected in the ICU.IELSR55 register
72	56	0x120	ICU.IELSR56	Event selected in the ICU.IELSR56 register
73	57	0x124	ICU.IELSR57	Event selected in the ICU.IELSR57 register
74	58	0x128	ICU.IELSR58	Event selected in the ICU.IELSR58 register
75	59	0x12C	ICU.IELSR59	Event selected in the ICU.IELSR59 register
76	60	0x130	ICU.IELSR60	Event selected in the ICU.IELSR60 register
77	61	0x134	ICU.IELSR61	Event selected in the ICU.IELSR61 register
78	62	0x138	ICU.IELSR62	Event selected in the ICU.IELSR62 register
79	63	0x13C	ICU.IELSR63	Event selected in the ICU.IELSR63 register
80	64	0x140	ICU.IELSR64	Event selected in the ICU.IELSR64 register
81	65	0x144	ICU.IELSR65	Event selected in the ICU.IELSR65 register
82	66	0x148	ICU.IELSR66	Event selected in the ICU.IELSR66 register
83	67	0x14C	ICU.IELSR67	Event selected in the ICU.IELSR67 register
84	68	0x150	ICU.IELSR68	Event selected in the ICU.IELSR68 register
85	69	0x154	ICU.IELSR69	Event selected in the ICU.IELSR69 register
86	70	0x158	ICU.IELSR70	Event selected in the ICU.IELSR70 register
87	71	0x15C	ICU.IELSR71	Event selected in the ICU.IELSR71 register
88	72	0x160	ICU.IELSR72	Event selected in the ICU.IELSR72 register
89	73	0x164	ICU.IELSR73	Event selected in the ICU.IELSR73 register

Table 12.3 中断向量表(3of4)

异常编号	IRQ number	矢量偏移	Source	Description
49	33	0x0C4	ICU.IELSR33	在ICU.IELSR33寄存器中选择的事件
50	34	0x0C8	ICU.IELSR34	在ICU.IELSR34寄存器中选择的事件
51	35	0x0CC	ICU.IELSR35	在ICU.IELSR35寄存器中选择的事件
52	36	0x0D0	ICU.IELSR36	在ICU.IELSR36寄存器中选择的事件
53	37	0x0D4	ICU.IELSR37	在ICU.IELSR37寄存器中选择的事件
54	38	0x0D8	ICU.IELSR38	在ICU.IELSR38寄存器中选择的事件
55	39	0x0DC	ICU.IELSR39	在ICU.IELSR39寄存器中选择的事件
56	40	0x0E0	ICU.IELSR40	在ICU.IELSR40寄存器中选择的事件
57	41	0x0E4	ICU.IELSR41	在ICU.IELSR41寄存器中选择的事件
58	42	0x0E8	ICU.IELSR42	在ICU.IELSR42寄存器中选择的事件
59	43	0x0EC	ICU.IELSR43	在ICU.IELSR43寄存器中选择的事件
60	44	0x0F0	ICU.IELSR44	在ICU.IELSR44寄存器中选择的事件
61	45	0x0F4	ICU.IELSR45	在ICU.IELSR45寄存器中选择的事件
62	46	0x0F8	ICU.IELSR46	在ICU.IELSR46寄存器中选择的事件
63	47	0x0FC	ICU.IELSR47	在ICU.IELSR47寄存器中选择的事件
64	48	0x100	ICU.IELSR48	在ICU.IELSR48寄存器中选择的事件
65	49	0x104	ICU.IELSR49	在ICU.IELSR49寄存器中选择的事件
66	50	0x108	ICU.IELSR50	在ICU.IELSR50寄存器中选择的事件
67	51	0x10C	ICU.IELSR51	在ICU.IELSR51寄存器中选择的事件
68	52	0x110	ICU.IELSR52	在ICU.IELSR52寄存器中选择的事件
69	53	0x114	ICU.IELSR53	在ICU.IELSR53寄存器中选择的事件
70	54	0x118	ICU.IELSR54	在ICU.IELSR54寄存器中选择的事件
71	55	0x11C	ICU.IELSR55	在ICU.IELSR55寄存器中选择的事件
72	56	0x120	ICU.IELSR56	在ICU.IELSR56寄存器中选择的事件
73	57	0x124	ICU.IELSR57	在ICU.IELSR57寄存器中选择的事件
74	58	0x128	ICU.IELSR58	在ICU.IELSR58寄存器中选择的事件
75	59	0x12C	ICU.IELSR59	在ICU.IELSR59寄存器中选择的事件
76	60	0x130	ICU.IELSR60	在ICU.IELSR60寄存器中选择的事件
77	61	0x134	ICU.IELSR61	在ICU.IELSR61寄存器中选择的事件
78	62	0x138	ICU.IELSR62	在ICU.IELSR62寄存器中选择的事件
79	63	0x13C	ICU.IELSR63	在ICU.IELSR63寄存器中选择的事件
80	64	0x140	ICU.IELSR64	在ICU.IELSR64寄存器中选择的事件
81	65	0x144	ICU.IELSR65	在ICU.IELSR65寄存器中选择的事件
82	66	0x148	ICU.IELSR66	在ICU.IELSR66寄存器中选择的事件
83	67	0x14C	ICU.IELSR67	在ICU.IELSR67寄存器中选择的事件
84	68	0x150	ICU.IELSR68	在ICU.IELSR68寄存器中选择的事件
85	69	0x154	ICU.IELSR69	在ICU.IELSR69寄存器中选择的事件
86	70	0x158	ICU.IELSR70	在ICU.IELSR70寄存器中选择的事件
87	71	0x15C	ICU.IELSR71	在ICU.IELSR71寄存器中选择的事件
88	72	0x160	ICU.IELSR72	在ICU.IELSR72寄存器中选择的事件
89	73	0x164	ICU.IELSR73	在ICU.IELSR73寄存器中选择的事件

Table 12.3 Interrupt vector table (4 of 4)

Exception number	IRQ number	Vector offset	Source	Description
90	74	0x168	ICU.IELSR74	Event selected in the ICU.IELSR74 register
91	75	0x16C	ICU.IELSR75	Event selected in the ICU.IELSR75 register
92	76	0x170	ICU.IELSR76	Event selected in the ICU.IELSR76 register
93	77	0x174	ICU.IELSR77	Event selected in the ICU.IELSR77 register
94	78	0x178	ICU.IELSR78	Event selected in the ICU.IELSR78 register
95	79	0x17C	ICU.IELSR79	Event selected in the ICU.IELSR79 register
96	80	0x180	ICU.IELSR80	Event selected in the ICU.IELSR80 register
97	81	0x184	ICU.IELSR81	Event selected in the ICU.IELSR81 register
98	82	0x188	ICU.IELSR82	Event selected in the ICU.IELSR82 register
99	83	0x18C	ICU.IELSR83	Event selected in the ICU.IELSR83 register
100	84	0x190	ICU.IELSR84	Event selected in the ICU.IELSR84 register
101	85	0x194	ICU.IELSR85	Event selected in the ICU.IELSR85 register
102	86	0x198	ICU.IELSR86	Event selected in the ICU.IELSR86 register
103	87	0x19C	ICU.IELSR87	Event selected in the ICU.IELSR87 register
104	88	0x1A0	ICU.IELSR88	Event selected in the ICU.IELSR88 register
105	89	0x1A4	ICU.IELSR89	Event selected in the ICU.IELSR89 register
106	90	0x1A8	ICU.IELSR90	Event selected in the ICU.IELSR90 register
107	91	0x1AC	ICU.IELSR91	Event selected in the ICU.IELSR91 register
108	92	0x1B0	ICU.IELSR92	Event selected in the ICU.IELSR92 register
109	93	0x1B4	ICU.IELSR93	Event selected in the ICU.IELSR93 register
110	94	0x1B8	ICU.IELSR94	Event selected in the ICU.IELSR94 register
111	95	0x1BC	ICU.IELSR95	Event selected in the ICU.IELSR95 register

12.3.2 Event Number

The following table lists heading details for Table 12.4, which describes each event number.

Heading	Description
Interrupt request source	Name of the source generating the interrupt request
Name	Name of the interrupt
Connect to NVIC	“ ✓” indicates the interrupt can be used as a CPU interrupt
Invoke DTC	“ ✓” indicates the interrupt can be used to request DTC activation
Invoke DMAC	“✓” indicates the interrupt can be used to request DMAC activation
Canceling Snooze	“ ✓” indicates the interrupt can be used to request a return from Snooze mode
Canceling Software Standby	“ ✓” indicates the interrupt can be used to request a return from Software Standby mode
Canceling Deep Software Standby	“✓” indicates the interrupt can be used to request a return from Deep Software Standby mode

Table 12.3 中断向量表(4of4)

异常编号	IRQ number	矢量偏移	Source	Description
90	74	0x168	ICU.IELSR74	在ICU.IELSR74寄存器中选择的事件
91	75	0x16C	ICU.IELSR75	在ICU.IELSR75寄存器中选择的事件
92	76	0x170	ICU.IELSR76	在ICU.IELSR76寄存器中选择的事件
93	77	0x174	ICU.IELSR77	在ICU.IELSR77寄存器中选择的事件
94	78	0x178	ICU.IELSR78	在ICU.IELSR78寄存器中选择的事件
95	79	0x17C	ICU.IELSR79	在ICU.IELSR79寄存器中选择的事件
96	80	0x180	ICU.IELSR80	在ICU.IELSR80寄存器中选择的事件
97	81	0x184	ICU.IELSR81	在ICU.IELSR81寄存器中选择的事件
98	82	0x188	ICU.IELSR82	在ICU.IELSR82寄存器中选择的事件
99	83	0x18C	ICU.IELSR83	在ICU.IELSR83寄存器中选择的事件
100	84	0x190	ICU.IELSR84	在ICU.IELSR84寄存器中选择的事件
101	85	0x194	ICU.IELSR85	在ICU.IELSR85寄存器中选择的事件
102	86	0x198	ICU.IELSR86	在ICU.IELSR86寄存器中选择的事件
103	87	0x19C	ICU.IELSR87	在ICU.IELSR87寄存器中选择的事件
104	88	0x1A0	ICU.IELSR88	在ICU.IELSR88寄存器中选择的事件
105	89	0x1A4	ICU.IELSR89	在ICU.IELSR89寄存器中选择的事件
106	90	0x1A8	ICU.IELSR90	在ICU.IELSR90寄存器中选择的事件
107	91	0x1AC	ICU.IELSR91	在ICU.IELSR91寄存器中选择的事件
108	92	0x1B0	ICU.IELSR92	在ICU.IELSR92寄存器中选择的事件
109	93	0x1B4	ICU.IELSR93	在ICU.IELSR93寄存器中选择的事件
110	94	0x1B8	ICU.IELSR94	在ICU.IELSR94寄存器中选择的事件
111	95	0x1BC	ICU.IELSR95	在ICU.IELSR95寄存器中选择的事件

12.3.2 事件编号

下表列出了表12.4的标题详细信息，其中描述了每个事件编号。

Heading	Description
中断请求源	产生中断请求的源名称
Name	中断名称
连接到NVIC	“ ”表示该中断可以作为CPU中断使用
Invoke DTC	“ ”表示该中断可用于请求DTC激活
Invoke DMAC	“ ”表示该中断可用于请求DMAC激活
取消贪睡	“ ”表示该中断可用于请求从贪睡模式返回
取消软件待机	“ ”表示该中断可用于请求从软件待机模式返回
取消深度软件待机	“ ”表示该中断可用于请求从深度软件待机模式返回

Table 12.4 Event table (1 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x001	Port	PORT_IRQ0	✓	✓	✓	✓	✓	✓
0x002		PORT_IRQ1	✓	✓	✓	✓	✓	✓
0x003		PORT_IRQ2	✓	✓	✓	✓	✓	✓
0x004		PORT_IRQ3	✓	✓	✓	✓	✓	✓
0x005		PORT_IRQ4	✓	✓	✓	✓	✓	✓
0x006		PORT_IRQ5	✓	✓	✓	✓	✓	✓
0x007		PORT_IRQ6	✓	✓	✓	✓	✓	✓
0x008		PORT_IRQ7	✓	✓	✓	✓	✓	✓
0x009		PORT_IRQ8	✓	✓	✓	✓	✓	✓
0x00A		PORT_IRQ9	✓	✓	✓	✓	✓	✓
0x00B		PORT_IRQ10	✓	✓	✓	✓	✓	✓
0x00C		PORT_IRQ11	✓	✓	✓	✓	✓	✓
0x00D		PORT_IRQ12	✓	✓	✓	✓	✓	✓
0x00E		PORT_IRQ13	✓	✓	✓	✓	✓	✓
0x00F		PORT_IRQ14	✓	✓	✓	✓	✓	✓
0x010		PORT_IRQ15	✓	✓	✓	✓	✓	✓
0x011	IIRFA	IIRFA_ORDY0	✓	—	—	—	—	—
0x012		IIRFA_CPRCF0	✓	—	—	—	—	—
0x013		IIRFA_ORDY1	✓	—	—	—	—	—
0x014		IIRFA_CPRCF1	✓	—	—	—	—	—
0x015		IIRFA_ORDY2	✓	—	—	—	—	—
0x016		IIRFA_CPRCF2	✓	—	—	—	—	—
0x017		IIRFA_ORDY3	✓	—	—	—	—	—
0x018		IIRFA_CPRCF3	✓	—	—	—	—	—
0x019		IIRFA_ERR	✓	—	—	—	—	—
0x020	DMAC0	DMAC0_INT	✓	✓	—	—	—	—
0x021	DMAC1	DMAC1_INT	✓	✓	—	—	—	—
0x022	DMAC2	DMAC2_INT	✓	✓	—	—	—	—
0x023	DMAC3	DMAC3_INT	✓	✓	—	—	—	—
0x024	DMAC4	DMAC4_INT	✓	✓	—	—	—	—
0x025	DMAC5	DMAC5_INT	✓	✓	—	—	—	—
0x026	DMAC6	DMAC6_INT	✓	✓	—	—	—	—
0x027	DMAC7	DMAC7_INT	✓	✓	—	—	—	—
0x029	DTC	DTC_COMPLETE	✓	—	—	✓*1	—	—
0x02B	DMAC/DTC	DMA_TRANSERR	✓	—	—	✓	—	—
0x02D	ICU	ICU_SNZCANCEL	✓	—	—	✓	—	—
0x030	FCU	FCU_FIFERR	✓	—	—	—	—	—
0x031		FCU_FRDYI	✓	—	—	—	—	—
0x038	LVD	LVD_LVD1	✓	—	—	✓	✓	✓
0x039		LVD_LVD2	✓	—	—	✓	✓	✓

Table 12.4 事件表（1个，共8个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至 NVIC	Invoke DTC	Invoke DMAC			
0x001	Port	PORT_IRQ0	✓	✓	✓	✓	✓	✓
0x002		PORT_IRQ1	✓	✓	✓	✓	✓	✓
0x003		PORT_IRQ2	✓	✓	✓	✓	✓	✓
0x004		PORT_IRQ3	✓	✓	✓	✓	✓	✓
0x005		PORT_IRQ4	✓	✓	✓	✓	✓	✓
0x006		PORT_IRQ5	✓	✓	✓	✓	✓	✓
0x007		PORT_IRQ6	✓	✓	✓	✓	✓	✓
0x008		PORT_IRQ7	✓	✓	✓	✓	✓	✓
0x009		PORT_IRQ8	✓	✓	✓	✓	✓	✓
0x00A		PORT_IRQ9	✓	✓	✓	✓	✓	✓
0x00B		PORT_IRQ10	✓	✓	✓	✓	✓	✓
0x00C		PORT_IRQ11	✓	✓	✓	✓	✓	✓
0x00D		PORT_IRQ12	✓	✓	✓	✓	✓	✓
0x00E		PORT_IRQ13	✓	✓	✓	✓	✓	✓
0x00F		PORT_IRQ14	✓	✓	✓	✓	✓	✓
0x010		PORT_IRQ15	✓	✓	✓	✓	✓	✓
0x011	IIRFA	IIRFA_ORDY0	✓	—	—	—	—	—
0x012		IIRFA_CPRCF0	✓	—	—	—	—	—
0x013		IIRFA_ORDY1	✓	—	—	—	—	—
0x014		IIRFA_CPRCF1	✓	—	—	—	—	—
0x015		IIRFA_ORDY2	✓	—	—	—	—	—
0x016		IIRFA_CPRCF2	✓	—	—	—	—	—
0x017		IIRFA_ORDY3	✓	—	—	—	—	—
0x018		IIRFA_CPRCF3	✓	—	—	—	—	—
0x019		IIRFA_ERR	✓	—	—	—	—	—
0x020	DMAC0	DMAC0_INT	✓	✓	—	—	—	—
0x021	DMAC1	DMAC1_INT	✓	✓	—	—	—	—
0x022	DMAC2	DMAC2_INT	✓	✓	—	—	—	—
0x023	DMAC3	DMAC3_INT	✓	✓	—	—	—	—
0x024	DMAC4	DMAC4_INT	✓	✓	—	—	—	—
0x025	DMAC5	DMAC5_INT	✓	✓	—	—	—	—
0x026	DMAC6	DMAC6_INT	✓	✓	—	—	—	—
0x027	DMAC7	DMAC7_INT	✓	✓	—	—	—	—
0x029	DTC	DTC_COMPLETE	✓	—	—	✓*1	—	—
0x02B	DMAC/DTC	DMA_TRANSERR	✓	—	—	✓	—	—
0x02D	ICU	ICU_SNZCANCEL	✓	—	—	✓	—	—
0x030	FCU	FCU_FIFERR	✓	—	—	—	—	—
0x031		FCU_FRDYI	✓	—	—	—	—	—
0x038	LVD	LVD_LVD1	✓	—	—	✓	✓	✓
0x039		LVD_LVD2	✓	—	—	✓	✓	✓

Table 12.4 Event table (2 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x03B	MOSC	MOSC_STOP	✓	—	—	—	—	—
0x03C	LPW	SYSTEM_SNZREQ	—	✓	—	—	—	—
0x040	AGT0	AGT0_AGTI	✓	✓	✓	—	—	—
0x041		AGT0_AGTCMAI	✓	✓	✓	—	—	—
0x042		AGT0_AGTCMBI	✓	✓	✓	—	—	—
0x043	AGT1	AGT1_AGTI	✓	✓	✓	✓	✓	—
0x044		AGT1_AGTCMAI	✓	✓	✓	✓	✓	—
0x045		AGT1_AGTCMBI	✓	✓	✓	✓	✓	—
0x052	IWDT	IWDT_NMIUNDF	✓	—	—	✓	✓	—
0x053	WDT	WDT_NMIUNDF	✓	—	—	—	—	—
0x059	CANFD	CAN_RXF	✓	—	—	—	—	—
0x05A		CAN_GLERR	✓	—	—	—	—	—
0x05B		CAN_RF_DMAREQ0	✓	✓	✓	—	—	—
0x05C		CAN_RF_DMAREQ1	✓	✓	✓	—	—	—
0x063		CAN0_TX	✓	—	—	—	—	—
0x064		CAN0_CHERR	✓	—	—	—	—	—
0x065		CAN0_COMFRX	✓	—	—	—	—	—
0x066		CAN0_CF_DMAREQ	✓	✓	✓	—	—	—
0x067		CAN0_RXMB	✓	—	—	—	—	—
0x08F	ACMPHS	ACMP_HS0	✓	—	—	—	—	—
0x090		ACMP_HS1	✓	—	—	—	—	—
0x091		ACMP_HS2	✓	—	—	—	—	—
0x092		ACMP_HS3	✓	—	—	—	—	—
0x09D	KINT	KEY_INTKR	✓	—	—	✓*2	✓*2	—
0x09E	CAC	CAC_FEERI	✓	—	—	—	—	—
0x09F		CAC_MENDI	✓	—	—	—	—	—
0x0A0		CAC_OVFI	✓	—	—	—	—	—
0x0B1	PORT	IOPORT_GROUPB	✓	✓*3	✓*3	—	—	—
0x0B2		IOPORT_GROUPC	✓	✓*3	✓*3	—	—	—
0x0B3		IOPORT_GROUPD	✓	✓*3	✓*3	—	—	—
0x0B4		IOPORT_GROUPE	✓	✓*3	✓*3	—	—	—
0x0B5	ELC	ELC_SWEVT0	✓*4	✓	—	—	—	—
0x0B6		ELC_SWEVT1	✓*4	✓	—	—	—	—
0x0B7	POEG	POEG_GROUPA	✓	—	—	—	—	—
0x0B8		POEG_GROUPB	✓	—	—	—	—	—
0x0B9		POEG_GROUPC	✓	—	—	—	—	—
0x0BA		POEG_GROUPD	✓	—	—	—	—	—

Table 12.4 事件表（2个，共8个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至 NVIC	Invoke DTC	Invoke DMAC			
0x03B	MOSC	MOSC_STOP	✓	—	—	—	—	—
0x03C	LPW	SYSTEM_SNZREQ	—	✓	—	—	—	—
0x040	AGT0	AGT0_AGTI	✓	✓	✓	—	—	—
0x041		AGT0_AGTCMAI	✓	✓	✓	—	—	—
0x042		AGT0_AGTCMBI	✓	✓	✓	—	—	—
0x043	AGT1	AGT1_AGTI	✓	✓	✓	✓	✓	—
0x044		AGT1_AGTCMAI	✓	✓	✓	✓	✓	—
0x045		AGT1_AGTCMBI	✓	✓	✓	✓	✓	—
0x052	IWDT	IWDT_NMIUNDF	✓	—	—	✓	✓	—
0x053	WDT	WDT_NMIUNDF	✓	—	—	—	—	—
0x059	CANFD	CAN_RXF	✓	—	—	—	—	—
0x05A		CAN_GLERR	✓	—	—	—	—	—
0x05B		CAN_RF_DMAREQ0	✓	✓	✓	—	—	—
0x05C		CAN_RF_DMAREQ1	✓	✓	✓	—	—	—
0x063		CAN0_TX	✓	—	—	—	—	—
0x064		CAN0_CHERR	✓	—	—	—	—	—
0x065		CAN0_COMFRX	✓	—	—	—	—	—
0x066		CAN0_CF_DMAREQ	✓	✓	✓	—	—	—
0x067		CAN0_RXMB	✓	—	—	—	—	—
0x08F	ACMPHS	ACMP_HS0	✓	—	—	—	—	—
0x090		ACMP_HS1	✓	—	—	—	—	—
0x091		ACMP_HS2	✓	—	—	—	—	—
0x092		ACMP_HS3	✓	—	—	—	—	—
0x09D	KINT	KEY_INTKR	✓	—	—	✓*2	✓*2	—
0x09E	CAC	CAC_FEERI	✓	—	—	—	—	—
0x09F		CAC_MENDI	✓	—	—	—	—	—
0x0A0		CAC_OVFI	✓	—	—	—	—	—
0x0B1	PORT	IOPORT_GROUPB	✓	✓*3	✓*3	—	—	—
0x0B2		IOPORT_GROUPC	✓	✓*3	✓*3	—	—	—
0x0B3		IOPORT_GROUPD	✓	✓*3	✓*3	—	—	—
0x0B4		IOPORT_GROUPE	✓	✓*3	✓*3	—	—	—
0x0B5	ELC	ELC_SWEVT0	✓*4	✓	—	—	—	—
0x0B6		ELC_SWEVT1	✓*4	✓	—	—	—	—
0x0B7	POEG	POEG_GROUPA	✓	—	—	—	—	—
0x0B8		POEG_GROUPB	✓	—	—	—	—	—
0x0B9		POEG_GROUPC	✓	—	—	—	—	—
0x0BA		POEG_GROUPD	✓	—	—	—	—	—

Table 12.4 Event table (3 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x0C0	GPT0	GPT0_CCMPA	✓	✓	✓	—	—	—
0x0C1		GPT0_CCMPB	✓	✓	✓	—	—	—
0x0C2		GPT0_CMPC	✓	✓	✓	—	—	—
0x0C3		GPT0_CMPD	✓	✓	✓	—	—	—
0x0C4		GPT0_CMPE	✓	✓	✓	—	—	—
0x0C5		GPT0_CMPF	✓	✓	✓	—	—	—
0x0C6		GPT0_OVF	✓	✓	✓	—	—	—
0x0C7		GPT0_UDF	✓	✓	✓	—	—	—
0x0C8		GPT0_PC	✓	✓	✓	—	—	—
0x0CA		GPT0_ADTRGA	✓	✓	✓	—	—	—
0x0CB		GPT0_ADTRGB	✓	✓	✓	—	—	—
0x0CC	GPT1	GPT1_CCMPA	✓	✓	✓	—	—	—
0x0CD		GPT1_CCMPB	✓	✓	✓	—	—	—
0x0CE		GPT1_CMPC	✓	✓	✓	—	—	—
0x0CF		GPT1_CMPD	✓	✓	✓	—	—	—
0x0D0		GPT1_CMPE	✓	✓	✓	—	—	—
0x0D1		GPT1_CMPF	✓	✓	✓	—	—	—
0x0D2		GPT1_OVF	✓	✓	✓	—	—	—
0x0D3		GPT1_UDF	✓	✓	✓	—	—	—
0x0D4		GPT1_PC	✓	✓	✓	—	—	—
0x0D6		GPT1_ADTRGA	✓	✓	✓	—	—	—
0x0D7		GPT1_ADTRGB	✓	✓	✓	—	—	—
0x0D8	GPT2	GPT2_CCMPA	✓	✓	✓	—	—	—
0x0D9		GPT2_CCMPB	✓	✓	✓	—	—	—
0x0DA		GPT2_CMPC	✓	✓	✓	—	—	—
0x0DB		GPT2_CMPD	✓	✓	✓	—	—	—
0x0DC		GPT2_CMPE	✓	✓	✓	—	—	—
0x0DD		GPT2_CMPF	✓	✓	✓	—	—	—
0x0DE		GPT2_OVF	✓	✓	✓	—	—	—
0x0DF		GPT2_UDF	✓	✓	✓	—	—	—
0x0E0		GPT2_PC	✓	✓	✓	—	—	—
0x0E2		GPT2_ADTRGA	✓	✓	✓	—	—	—
0x0E3		GPT2_ADTRGB	✓	✓	✓	—	—	—

Table 12.4 事件表（3个，共8个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至 NVIC	Invoke DTC	Invoke DMAC			
0x0C0	GPT0	GPT0_CCMPA	✓	✓	✓	—	—	—
0x0C1		GPT0_CCMPB	✓	✓	✓	—	—	—
0x0C2		GPT0_CMPC	✓	✓	✓	—	—	—
0x0C3		GPT0_CMPD	✓	✓	✓	—	—	—
0x0C4		GPT0_CMPE	✓	✓	✓	—	—	—
0x0C5		GPT0_CMPF	✓	✓	✓	—	—	—
0x0C6		GPT0_OVF	✓	✓	✓	—	—	—
0x0C7		GPT0_UDF	✓	✓	✓	—	—	—
0x0C8		GPT0_PC	✓	✓	✓	—	—	—
0x0CA		GPT0_ADTRGA	✓	✓	✓	—	—	—
0x0CB		GPT0_ADTRGB	✓	✓	✓	—	—	—
0x0CC	GPT1	GPT1_CCMPA	✓	✓	✓	—	—	—
0x0CD		GPT1_CCMPB	✓	✓	✓	—	—	—
0x0CE		GPT1_CMPC	✓	✓	✓	—	—	—
0x0CF		GPT1_CMPD	✓	✓	✓	—	—	—
0x0D0		GPT1_CMPE	✓	✓	✓	—	—	—
0x0D1		GPT1_CMPF	✓	✓	✓	—	—	—
0x0D2		GPT1_OVF	✓	✓	✓	—	—	—
0x0D3		GPT1_UDF	✓	✓	✓	—	—	—
0x0D4		GPT1_PC	✓	✓	✓	—	—	—
0x0D6		GPT1_ADTRGA	✓	✓	✓	—	—	—
0x0D7		GPT1_ADTRGB	✓	✓	✓	—	—	—
0x0D8	GPT2	GPT2_CCMPA	✓	✓	✓	—	—	—
0x0D9		GPT2_CCMPB	✓	✓	✓	—	—	—
0x0DA		GPT2_CMPC	✓	✓	✓	—	—	—
0x0DB		GPT2_CMPD	✓	✓	✓	—	—	—
0x0DC		GPT2_CMPE	✓	✓	✓	—	—	—
0x0DD		GPT2_CMPF	✓	✓	✓	—	—	—
0x0DE		GPT2_OVF	✓	✓	✓	—	—	—
0x0DF		GPT2_UDF	✓	✓	✓	—	—	—
0x0E0		GPT2_PC	✓	✓	✓	—	—	—
0x0E2		GPT2_ADTRGA	✓	✓	✓	—	—	—
0x0E3		GPT2_ADTRGB	✓	✓	✓	—	—	—

Table 12.4 Event table (4 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x0E4	GPT3	GPT3_CCMPA	✓	✓	✓	—	—	—
0x0E5		GPT3_CCMPB	✓	✓	✓	—	—	—
0x0E6		GPT3_CMPC	✓	✓	✓	—	—	—
0x0E7		GPT3_CMPD	✓	✓	✓	—	—	—
0x0E8		GPT3_CMPE	✓	✓	✓	—	—	—
0x0E9		GPT3_CMPF	✓	✓	✓	—	—	—
0x0EA		GPT3_OVF	✓	✓	✓	—	—	—
0x0EB		GPT3_UDF	✓	✓	✓	—	—	—
0x0EC		GPT3_PC	✓	✓	✓	—	—	—
0x0EE		GPT3_ADTRGA	✓	✓	✓	—	—	—
0x0EF		GPT3_ADTRGB	✓	✓	✓	—	—	—
0x0F0	GPT4	GPT4_CCMPA	✓	✓	✓	—	—	—
0x0F1		GPT4_CCMPB	✓	✓	✓	—	—	—
0x0F2		GPT4_CMPC	✓	✓	✓	—	—	—
0x0F3		GPT4_CMPD	✓	✓	✓	—	—	—
0x0F4		GPT4_CMPE	✓	✓	✓	—	—	—
0x0F5		GPT4_CMPF	✓	✓	✓	—	—	—
0x0F6		GPT4_OVF	✓	✓	✓	—	—	—
0x0F7		GPT4_UDF	✓	✓	✓	—	—	—
0x0FA		GPT4_ADTRGA	✓	✓	✓	—	—	—
0x0FB		GPT4_ADTRGB	✓	✓	✓	—	—	—
0x0FC	GPT5	GPT5_CCMPA	✓	✓	✓	—	—	—
0x0FD		GPT5_CCMPB	✓	✓	✓	—	—	—
0x0FE		GPT5_CMPC	✓	✓	✓	—	—	—
0x0FF		GPT5_CMPD	✓	✓	✓	—	—	—
0x100		GPT5_CMPE	✓	✓	✓	—	—	—
0x101		GPT5_CMPF	✓	✓	✓	—	—	—
0x102		GPT5_OVF	✓	✓	✓	—	—	—
0x103		GPT5_UDF	✓	✓	✓	—	—	—
0x106		GPT5_ADTRGA	✓	✓	✓	—	—	—
0x107		GPT5_ADTRGB	✓	✓	✓	—	—	—

Table 12.4 事件表（4个，共8个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至 NVIC	Invoke DTC	Invoke DMAC			
0x0E4	GPT3	GPT3_CCMPA	✓	✓	✓	—	—	—
0x0E5		GPT3_CCMPB	✓	✓	✓	—	—	—
0x0E6		GPT3_CMPC	✓	✓	✓	—	—	—
0x0E7		GPT3_CMPD	✓	✓	✓	—	—	—
0x0E8		GPT3_CMPE	✓	✓	✓	—	—	—
0x0E9		GPT3_CMPF	✓	✓	✓	—	—	—
0x0EA		GPT3_OVF	✓	✓	✓	—	—	—
0x0EB		GPT3_UDF	✓	✓	✓	—	—	—
0x0EC		GPT3_PC	✓	✓	✓	—	—	—
0x0EE		GPT3_ADTRGA	✓	✓	✓	—	—	—
0x0EF		GPT3_ADTRGB	✓	✓	✓	—	—	—
0x0F0	GPT4	GPT4_CCMPA	✓	✓	✓	—	—	—
0x0F1		GPT4_CCMPB	✓	✓	✓	—	—	—
0x0F2		GPT4_CMPC	✓	✓	✓	—	—	—
0x0F3		GPT4_CMPD	✓	✓	✓	—	—	—
0x0F4		GPT4_CMPE	✓	✓	✓	—	—	—
0x0F5		GPT4_CMPF	✓	✓	✓	—	—	—
0x0F6		GPT4_OVF	✓	✓	✓	—	—	—
0x0F7		GPT4_UDF	✓	✓	✓	—	—	—
0x0FA		GPT4_ADTRGA	✓	✓	✓	—	—	—
0x0FB		GPT4_ADTRGB	✓	✓	✓	—	—	—
0x0FC	GPT5	GPT5_CCMPA	✓	✓	✓	—	—	—
0x0FD		GPT5_CCMPB	✓	✓	✓	—	—	—
0x0FE		GPT5_CMPC	✓	✓	✓	—	—	—
0x0FF		GPT5_CMPD	✓	✓	✓	—	—	—
0x100		GPT5_CMPE	✓	✓	✓	—	—	—
0x101		GPT5_CMPF	✓	✓	✓	—	—	—
0x102		GPT5_OVF	✓	✓	✓	—	—	—
0x103		GPT5_UDF	✓	✓	✓	—	—	—
0x106		GPT5_ADTRGA	✓	✓	✓	—	—	—
0x107		GPT5_ADTRGB	✓	✓	✓	—	—	—

Table 12.4 Event table (5 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x108	GPT6	GPT6_CCMPA	✓	✓	✓	—	—	—
0x109		GPT6_CCMPB	✓	✓	✓	—	—	—
0x10A		GPT6_CMPC	✓	✓	✓	—	—	—
0x10B		GPT6_CMPD	✓	✓	✓	—	—	—
0x10C		GPT6_CMPE	✓	✓	✓	—	—	—
0x10D		GPT6_CMPF	✓	✓	✓	—	—	—
0x10E		GPT6_OVF	✓	✓	✓	—	—	—
0x10F		GPT6_UDF	✓	✓	✓	—	—	—
0x112		GPT6_ADTRGA	✓	✓	✓	—	—	—
0x113		GPT6_ADTRGB	✓	✓	✓	—	—	—
0x114	GPT7	GPT7_CCMPA	✓	✓	✓	—	—	—
0x115		GPT7_CCMPB	✓	✓	✓	—	—	—
0x116		GPT7_CMPC	✓	✓	✓	—	—	—
0x117		GPT7_CMPD	✓	✓	✓	—	—	—
0x118		GPT7_CMPE	✓	✓	✓	—	—	—
0x119		GPT7_CMPF	✓	✓	✓	—	—	—
0x11A		GPT7_OVF	✓	✓	✓	—	—	—
0x11B		GPT7_UDF	✓	✓	✓	—	—	—
0x11E		GPT7_ADTRGA	✓	✓	✓	—	—	—
0x11F		GPT7_ADTRGB	✓	✓	✓	—	—	—
0x120	GPT8	GPT8_CCMPA	✓	✓	✓	—	—	—
0x121		GPT8_CCMPB	✓	✓	✓	—	—	—
0x122		GPT8_CMPC	✓	✓	✓	—	—	—
0x123		GPT8_CMPD	✓	✓	✓	—	—	—
0x124		GPT8_CMPE	✓	✓	✓	—	—	—
0x125		GPT8_CMPF	✓	✓	✓	—	—	—
0x126		GPT8_OVF	✓	✓	✓	—	—	—
0x127		GPT8_UDF	✓	✓	✓	—	—	—
0x12A		GPT8_ADTRGA	✓	✓	✓	—	—	—
0x12B		GPT8_ADTRGB	✓	✓	✓	—	—	—
0x12C	GPT9	GPT9_CCMPA	✓	✓	✓	—	—	—
0x12D		GPT9_CCMPB	✓	✓	✓	—	—	—
0x12E		GPT9_CMPC	✓	✓	✓	—	—	—
0x12F		GPT9_CMPD	✓	✓	✓	—	—	—
0x130		GPT9_CMPE	✓	✓	✓	—	—	—
0x131		GPT9_CMPF	✓	✓	✓	—	—	—
0x132		GPT9_OVF	✓	✓	✓	—	—	—
0x133		GPT9_UDF	✓	✓	✓	—	—	—
0x136		GPT9_ADTRGA	✓	✓	✓	—	—	—
0x137		GPT9_ADTRGB	✓	✓	✓	—	—	—

Table 12.4 事件表（5个，共8个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至 NVIC	Invoke DTC	Invoke DMAC			
0x108	GPT6	GPT6_CCMPA	✓	✓	✓	—	—	—
0x109		GPT6_CCMPB	✓	✓	✓	—	—	—
0x10A		GPT6_CMPC	✓	✓	✓	—	—	—
0x10B		GPT6_CMPD	✓	✓	✓	—	—	—
0x10C		GPT6_CMPE	✓	✓	✓	—	—	—
0x10D		GPT6_CMPF	✓	✓	✓	—	—	—
0x10E		GPT6_OVF	✓	✓	✓	—	—	—
0x10F		GPT6_UDF	✓	✓	✓	—	—	—
0x112		GPT6_ADTRGA	✓	✓	✓	—	—	—
0x113		GPT6_ADTRGB	✓	✓	✓	—	—	—
0x114	GPT7	GPT7_CCMPA	✓	✓	✓	—	—	—
0x115		GPT7_CCMPB	✓	✓	✓	—	—	—
0x116		GPT7_CMPC	✓	✓	✓	—	—	—
0x117		GPT7_CMPD	✓	✓	✓	—	—	—
0x118		GPT7_CMPE	✓	✓	✓	—	—	—
0x119		GPT7_CMPF	✓	✓	✓	—	—	—
0x11A		GPT7_OVF	✓	✓	✓	—	—	—
0x11B		GPT7_UDF	✓	✓	✓	—	—	—
0x11E		GPT7_ADTRGA	✓	✓	✓	—	—	—
0x11F		GPT7_ADTRGB	✓	✓	✓	—	—	—
0x120	GPT8	GPT8_CCMPA	✓	✓	✓	—	—	—
0x121		GPT8_CCMPB	✓	✓	✓	—	—	—
0x122		GPT8_CMPC	✓	✓	✓	—	—	—
0x123		GPT8_CMPD	✓	✓	✓	—	—	—
0x124		GPT8_CMPE	✓	✓	✓	—	—	—
0x125		GPT8_CMPF	✓	✓	✓	—	—	—
0x126		GPT8_OVF	✓	✓	✓	—	—	—
0x127		GPT8_UDF	✓	✓	✓	—	—	—
0x12A		GPT8_ADTRGA	✓	✓	✓	—	—	—
0x12B		GPT8_ADTRGB	✓	✓	✓	—	—	—
0x12C	GPT9	GPT9_CCMPA	✓	✓	✓	—	—	—
0x12D		GPT9_CCMPB	✓	✓	✓	—	—	—
0x12E		GPT9_CMPC	✓	✓	✓	—	—	—
0x12F		GPT9_CMPD	✓	✓	✓	—	—	—
0x130		GPT9_CMPE	✓	✓	✓	—	—	—
0x131		GPT9_CMPF	✓	✓	✓	—	—	—
0x132		GPT9_OVF	✓	✓	✓	—	—	—
0x133		GPT9_UDF	✓	✓	✓	—	—	—
0x136		GPT9_ADTRGA	✓	✓	✓	—	—	—
0x137		GPT9_ADTRGB	✓	✓	✓	—	—	—

Table 12.4 Event table (6 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x138	GPT	GPT_UVWEDGE	✓	—	—	—	—	—
0x140	IIC0	IIC0_RX	✓	✓	✓	—	—	—
0x141		IIC0_TX	✓	✓	✓	—	—	—
0x142		IIC0_TEND	✓	—	—	—	—	—
0x143		IIC0_EEI	✓	—	—	—	—	—
0x144		IIC0_WU	✓	—	—	✓	✓	—
0x146	IIC1	IIC1_RX	✓	✓	✓	—	—	—
0x147		IIC1_TX	✓	✓	✓	—	—	—
0x148		IIC1_TEND	✓	—	—	—	—	—
0x149		IIC1_EEI	✓	—	—	—	—	—
0x157	ADC	ADC_LIMCLPI	✓	—	—	—	—	—
0x158		ADC_FIFOOVF	✓	—	—	—	—	—
0x159		ADC_ADI0	✓	✓	✓	—	—	—
0x15A		ADC_ADI1	✓	✓	✓	—	—	—
0x15B		ADC_ADI2	✓	✓	✓	—	—	—
0x15C		ADC_CMPI0	✓	—	—	—	—	—
0x15D		ADC_CMPI1	✓	—	—	—	—	—
0x15E		ADC_CCMPM0	✓	✓	✓	✓*1	—	—
0x160		ADC_ERR0	✓	—	—	—	—	—
0x161		ADC_RESOVF0	✓	—	—	—	—	—
0x163		ADC_CALEND0	✓	—	—	—	—	—
0x164		ADC_FIFOREQ0	✓	✓	✓	—	—	—
0x165		ADC_FIFOREQ1	✓	✓	✓	—	—	—
0x166		ADC_FIFOREQ2	✓	✓	✓	—	—	—
0x167		ADC_ADI3	✓	✓	✓	—	—	—
0x168		ADC_ADI4	✓	✓	✓	—	—	—
0x169		ADC_ADI5678	✓	✓	✓	—	—	—
0x16A		ADC_CMPI2	✓	—	—	—	—	—
0x16B		ADC_CMPI3	✓	—	—	—	—	—
0x16C		ADC_CCMPM1	✓	✓	✓	✓*1	—	—
0x16E		ADC_ERR1	✓	—	—	—	—	—
0x16F		ADC_RESOVF1	✓	—	—	—	—	—
0x171		ADC_CALEND1	✓	—	—	—	—	—
0x172		ADC_FIFOREQ3	✓	✓	✓	—	—	—
0x173		ADC_FIFOREQ4	✓	✓	✓	—	—	—
0x174		ADC_FIFOREQ5678	✓	✓	✓	—	—	—

Table 12.4 事件表（6个，共8个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至 NVIC	Invoke DTC	Invoke DMAC			
0x138	GPT	GPT_UVWEDGE	✓	—	—	—	—	—
0x140	IIC0	IIC0_RX	✓	✓	✓	—	—	—
0x141		IIC0_TX	✓	✓	✓	—	—	—
0x142		IIC0_TEND	✓	—	—	—	—	—
0x143		IIC0_EEI	✓	—	—	—	—	—
0x144		IIC0_WU	✓	—	—	✓	✓	—
0x146	IIC1	IIC1_RX	✓	✓	✓	—	—	—
0x147		IIC1_TX	✓	✓	✓	—	—	—
0x148		IIC1_TEND	✓	—	—	—	—	—
0x149		IIC1_EEI	✓	—	—	—	—	—
0x157	ADC	ADC_LIMCLPI	✓	—	—	—	—	—
0x158		ADC_FIFOOVF	✓	—	—	—	—	—
0x159		ADC_ADI0	✓	✓	✓	—	—	—
0x15A		ADC_ADI1	✓	✓	✓	—	—	—
0x15B		ADC_ADI2	✓	✓	✓	—	—	—
0x15C		ADC_CMPI0	✓	—	—	—	—	—
0x15D		ADC_CMPI1	✓	—	—	—	—	—
0x15E		ADC_CCMPM0	✓	✓	✓	✓*1	—	—
0x160		ADC_ERR0	✓	—	—	—	—	—
0x161		ADC_RESOVF0	✓	—	—	—	—	—
0x163		ADC_CALEND0	✓	—	—	—	—	—
0x164		ADC_FIFOREQ0	✓	✓	✓	—	—	—
0x165		ADC_FIFOREQ1	✓	✓	✓	—	—	—
0x166		ADC_FIFOREQ2	✓	✓	✓	—	—	—
0x167		ADC_ADI3	✓	✓	✓	—	—	—
0x168		ADC_ADI4	✓	✓	✓	—	—	—
0x169		ADC_ADI5678	✓	✓	✓	—	—	—
0x16A		ADC_CMPI2	✓	—	—	—	—	—
0x16B		ADC_CMPI3	✓	—	—	—	—	—
0x16C		ADC_CCMPM1	✓	✓	✓	✓*1	—	—
0x16E		ADC_ERR1	✓	—	—	—	—	—
0x16F		ADC_RESOVF1	✓	—	—	—	—	—
0x171		ADC_CALEND1	✓	—	—	—	—	—
0x172		ADC_FIFOREQ3	✓	✓	✓	—	—	—
0x173		ADC_FIFOREQ4	✓	✓	✓	—	—	—
0x174		ADC_FIFOREQ5678	✓	✓	✓	—	—	—

Table 12.4 Event table (7 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x18D	SCI0	SCI0_RXI	✓	✓	✓	—	—	—
0x18E		SCI0_TXI	✓	✓	✓	—	—	—
0x18F		SCI0_TEI	✓	—	—	—	—	—
0x190		SCI0_ERI	✓	—	—	—	—	—
0x191		SCI0_AED	✓	—	—	—	—	—
0x192		SCI0_BFD	✓	—	—	—	—	—
0x193		SCI0_AM	✓	—	—	✓*1	—	—
0x195	SCI1	SCI1_RXI	✓	✓	✓	—	—	—
0x196		SCI1_TXI	✓	✓	✓	—	—	—
0x197		SCI1_TEI	✓	—	—	—	—	—
0x198		SCI1_ERI	✓	—	—	—	—	—
0x199		SCI1_AED	✓	—	—	—	—	—
0x19A		SCI1_BFD	✓	—	—	—	—	—
0x19B		SCI1_AM	✓	—	—	—	—	—
0x19C	SCI2	SCI2_RXI	✓	✓	✓	—	—	—
0x19D		SCI2_TXI	✓	✓	✓	—	—	—
0x19E		SCI2_TEI	✓	—	—	—	—	—
0x19F		SCI2_ERI	✓	—	—	—	—	—
0x1A0		SCI2_AED	✓	—	—	—	—	—
0x1A1		SCI2_BFD	✓	—	—	—	—	—
0x1A2		SCI2_AM	✓	—	—	—	—	—
0x1A3	SCI3	SCI3_RXI	✓	✓	✓	—	—	—
0x1A4		SCI3_TXI	✓	✓	✓	—	—	—
0x1A5		SCI3_TEI	✓	—	—	—	—	—
0x1A6		SCI3_ERI	✓	—	—	—	—	—
0x1A7		SCI3_AED	✓	—	—	—	—	—
0x1A8		SCI3_BFD	✓	—	—	—	—	—
0x1A9		SCI3_AM	✓	—	—	—	—	—
0x1AA	SCI4	SCI4_RXI	✓	✓	✓	—	—	—
0x1AB		SCI4_TXI	✓	✓	✓	—	—	—
0x1AC		SCI4_TEI	✓	—	—	—	—	—
0x1AD		SCI4_ERI	✓	—	—	—	—	—
0x1AE		SCI4_AED	✓	—	—	—	—	—
0x1AF		SCI4_BFD	✓	—	—	—	—	—
0x1B0		SCI4_AM	✓	—	—	—	—	—

Table 12.4 事件表（8个中的7个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至 NVIC	Invoke DTC	Invoke DMAC			
0x18D	SCI0	SCI0_RXI	✓	✓	✓	—	—	—
0x18E		SCI0_TXI	✓	✓	✓	—	—	—
0x18F		SCI0_TEI	✓	—	—	—	—	—
0x190		SCI0_ERI	✓	—	—	—	—	—
0x191		SCI0_AED	✓	—	—	—	—	—
0x192		SCI0_BFD	✓	—	—	—	—	—
0x193		SCI0_AM	✓	—	—	✓*1	—	—
0x195	SCI1	SCI1_RXI	✓	✓	✓	—	—	—
0x196		SCI1_TXI	✓	✓	✓	—	—	—
0x197		SCI1_TEI	✓	—	—	—	—	—
0x198		SCI1_ERI	✓	—	—	—	—	—
0x199		SCI1_AED	✓	—	—	—	—	—
0x19A		SCI1_BFD	✓	—	—	—	—	—
0x19B		SCI1_AM	✓	—	—	—	—	—
0x19C	SCI2	SCI2_RXI	✓	✓	✓	—	—	—
0x19D		SCI2_TXI	✓	✓	✓	—	—	—
0x19E		SCI2_TEI	✓	—	—	—	—	—
0x19F		SCI2_ERI	✓	—	—	—	—	—
0x1A0		SCI2_AED	✓	—	—	—	—	—
0x1A1		SCI2_BFD	✓	—	—	—	—	—
0x1A2		SCI2_AM	✓	—	—	—	—	—
0x1A3	SCI3	SCI3_RXI	✓	✓	✓	—	—	—
0x1A4		SCI3_TXI	✓	✓	✓	—	—	—
0x1A5		SCI3_TEI	✓	—	—	—	—	—
0x1A6		SCI3_ERI	✓	—	—	—	—	—
0x1A7		SCI3_AED	✓	—	—	—	—	—
0x1A8		SCI3_BFD	✓	—	—	—	—	—
0x1A9		SCI3_AM	✓	—	—	—	—	—
0x1AA	SCI4	SCI4_RXI	✓	✓	✓	—	—	—
0x1AB		SCI4_TXI	✓	✓	✓	—	—	—
0x1AC		SCI4_TEI	✓	—	—	—	—	—
0x1AD		SCI4_ERI	✓	—	—	—	—	—
0x1AE		SCI4_AED	✓	—	—	—	—	—
0x1AF		SCI4_BFD	✓	—	—	—	—	—
0x1B0		SCI4_AM	✓	—	—	—	—	—

Table 12.4 Event table (8 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x1B1	SCI9	SCI9_RXI	✓	✓	✓	—	—	—
0x1B2		SCI9_TXI	✓	✓	✓	—	—	—
0x1B3		SCI9_TEI	✓	—	—	—	—	—
0x1B4		SCI9_ERI	✓	—	—	—	—	—
0x1B5		SCI9_AED	✓	—	—	—	—	—
0x1B6		SCI9_BFD	✓	—	—	—	—	—
0x1B7		SCI9_AM	✓	—	—	—	—	—
0x1C4	SPI0	SPI0_SPRI	✓	✓	✓	—	—	—
0x1C5		SPI0_SPTI	✓	✓	✓	—	—	—
0x1C6		SPI0_SPII	✓	—	—	—	—	—
0x1C7		SPI0_SPEI	✓	—	—	—	—	—
0x1C8		SPI0_SPCEND	✓	—	—	—	—	—
0x1C9	SPI1	SPI1_SPRI	✓	✓	✓	—	—	—
0x1CA		SPI1_SPTI	✓	✓	✓	—	—	—
0x1CB		SPI1_SPII	✓	—	—	—	—	—
0x1CC		SPI1_SPEI	✓	—	—	—	—	—
0x1CD		SPI1_SPCEND	✓	—	—	—	—	—
0x1D0	CANFD ECC	CAN_MRAM_ERI	✓	—	—	—	—	—
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*1	—	—

Note 1. Using SELSR0.
Note 2. Only supported when KRCTL.KRMD = 1.
Note 3. Only the first edge detection is valid.
Note 4. Only interrupts after DTC transfer are supported.

12.4 Interrupt Operation

The ICU performs the following functions:

- Detecting interrupts
- Enabling and disabling interrupts
- Selecting interrupt request destinations such as CPU interrupt, DTC activation, and DMAC activation.

12.4.1 Detecting Interrupts

The ICU selects an event source input from a peripheral function interrupt or an external pin interrupt with IELSRn.IELS [8:0].

The accepted interrupt source sets the IELSRn.IR to 1 and sends an interrupt request to the NVIC.

External pin interrupt requests are detected by either:

- Edges (falling edge, rising edge, or rising and falling edges)
- Level (low level) of the interrupt signal.

Set the IRQCRi.IRQMD[1:0] bits to select the detection mode for the IRQi pins. For interrupt sources associated with peripheral modules, see Table 12.3 and Table 12.4. Events must be accepted by the NVIC before an interrupt occurs and is accepted by the CPU.

Table 12.4 事件表（8个中的8个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至NVIC	Invoke DTC	Invoke DMAC			
0x1B1	SCI9	SCI9_RXI	✓	✓	✓	—	—	—
0x1B2		SCI9_TXI	✓	✓	✓	—	—	—
0x1B3		SCI9_TEI	✓	—	—	—	—	—
0x1B4		SCI9_ERI	✓	—	—	—	—	—
0x1B5		SCI9_AED	✓	—	—	—	—	—
0x1B6		SCI9_BFD	✓	—	—	—	—	—
0x1B7		SCI9_AM	✓	—	—	—	—	—
0x1C4	SPI0	SPI0_SPRI	✓	✓	✓	—	—	—
0x1C5		SPI0_SPTI	✓	✓	✓	—	—	—
0x1C6		SPI0_SPII	✓	—	—	—	—	—
0x1C7		SPI0_SPEI	✓	—	—	—	—	—
0x1C8		SPI0_SPCEND	✓	—	—	—	—	—
0x1C9	SPI1	SPI1_SPRI	✓	✓	✓	—	—	—
0x1CA		SPI1_SPTI	✓	✓	✓	—	—	—
0x1CB		SPI1_SPII	✓	—	—	—	—	—
0x1CC		SPI1_SPEI	✓	—	—	—	—	—
0x1CD		SPI1_SPCEND	✓	—	—	—	—	—
0x1D0	CANFD ECC	CAN_MRAM_ERI	✓	—	—	—	—	—
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*1	—	—

注1.使用SELSR0。
注2.仅当KRCTL.KRMD=1时支持。
注3.只有第一个边缘检测有效。
注4.仅支持DTC传输后的中断。

12.4 中断操作

ICU执行以下功能：

●检测中断
●启用和禁用中断
●选择中断请求目标，例如CPU中断、DTC激活和DMAC激活。

12.4.1 检测中断

ICU通过IELSRn.IELS[8:0]从外围功能中断或外部引脚中断选择事件源输入。

接受的中断源将IELSRn.IR设置为1，并向NVIC发送中断请求。

外部引脚中断请求通过以下任一方式检测：

●边沿（下降沿、上升沿或上升沿和下降沿）
●中断信号的电平（低电平）。

设置IRQCRi.IRQMD[1:0]位以选择IRQi引脚的检测模式。对于与外围模块相关的中断源，请参见表12.3和表12.4。事件必须在中断发生之前被NVIC接受并被CPU接受。

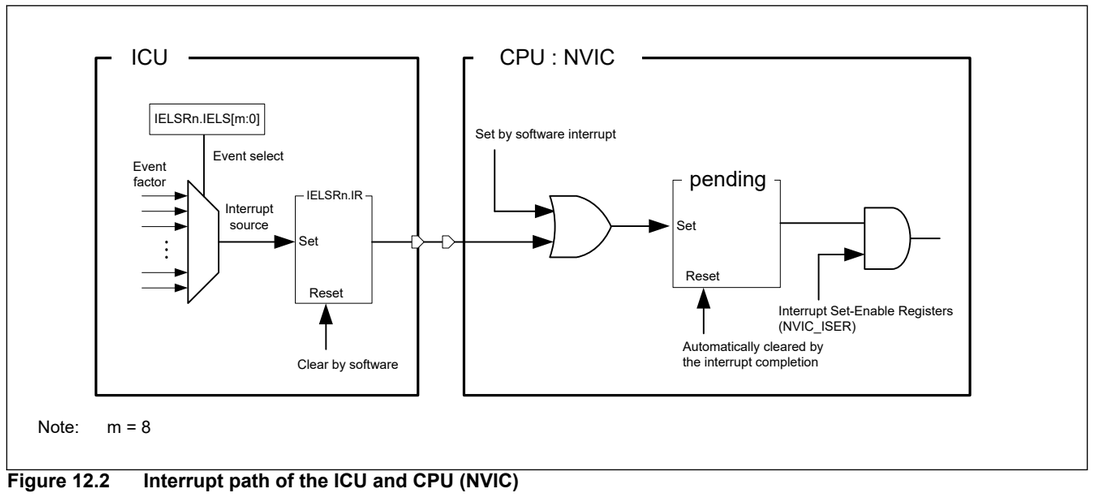


Figure 12.2 Interrupt path of the ICU and CPU (NVIC)

12.5 Interrupt setting procedure

12.5.1 Enabling Interrupt Requests

The procedure for enabling an interrupt request is as follows:

1. Set the Interrupt Set-Enable register (NVIC_ISER).
2. Set the IELSRn.IELS[8:0] bits as the interrupt source.
3. Specify the operation settings for the event source, such as DMAC activation (DELSRn.DELS[8:0]), snooze mode cancellation (SELSR0.SELS[8:0]), software standby mode cancellation (WUPEN register setting).

12.5.2 Disabling Interrupt Requests

The procedure to disable the interrupt request is as follows:

1. Disable the operation settings for the event source, such as DMAC activation (DELSRn.DELS[8:0]), snooze mode cancellation (SELSR0.SELS[8:0]), software standby mode cancellation (WUPEN register setting).
2. Clear the interrupt source setting (IELSRn.IELS[8:0] = 0x00).
3. Clear the interrupt status flag (IELSRn.IR = 0).
4. Clear the interrupt Clear-Enable register (NVIC_ICER) and interrupt Clear-Pending register (NVIC_ICPR).

12.5.3 Polling for interrupts

The procedure for polling for interrupt requests is as follows:

1. Set the Interrupt Clear-Enable register (NVIC_ICER).
2. Set the IELSRn.IELS[8:0] bits as the interrupt source.
3. Specify the operation settings for the event source, such as DMAC activation (DELSRn.DELS[8:0]), snooze mode cancellation (SELSR0.SELS[8:0]), software standby mode cancellation (WUPEN register setting).
4. Poll the interrupt Set-Pending register (NVIC_ISPR).

12.5.4 Selecting Interrupt Request Destinations

The available destinations are fixed for each interrupt, as described in Table 12.3, Table 12.4.

The interrupt output destination, CPU, DMAC, or DTC can be independently selected for each interrupt source.

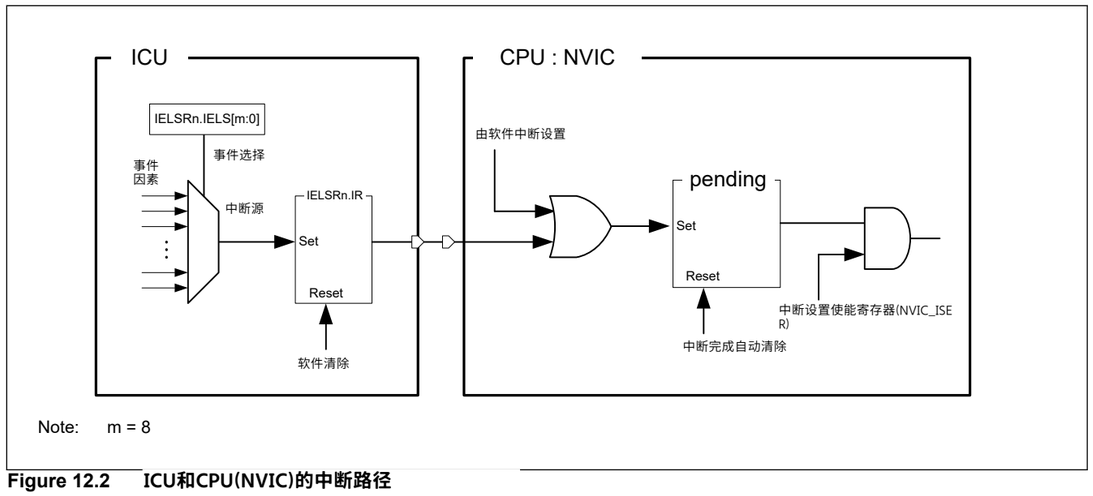


Figure 12.2 ICU和CPU(NVIC)的中断路径

12.5 中断设置程序

12.5.1 启用中断请求

使能中断请求的过程如下：

1.设置中断设置使能寄存器(NVIC_ISER)。

2.将IELSRn.IELS[8:0]位设置为中断源。

3.指定事件源的操作设置，例如DMAC激活（DELSRn.DELS[8:0]）、贪睡模式取消（SELSR0.SELS[8:0]）、软件待机模式取消（WUPEN寄存器设置）。

12.5.2 禁用中断请求

禁用中断请求的过程如下：

1.禁用事件源的操作设置，例如DMAC激活（DELSRn.DELS[8:0]）、贪睡模式取消（SELSR0.SELS[8:0]）、软件待机模式取消（WUPEN寄存器设置）。

2.清除中断源设置（IELSRn.IELS[8:0]=0x00）。

3.清除中断状态标志（IELSRn.IR=0）。

4.清除中断清除启用寄存器（NVIC_ICER）和中断清除挂起寄存器（NVIC_ICPR）。

12.5.3 轮询中断

轮询中断请求的过程如下：

1.设置中断清除启用寄存器(NVIC_ICER)。

2.将IELSRn.IELS[8:0]位设置为中断源。

3.指定事件源的操作设置，例如DMAC激活（DELSRn.DELS[8:0]）、贪睡模式取消（SELSR0.SELS[8:0]）、软件待机模式取消（WUPEN寄存器设置）。

4.轮询中断设置挂起寄存器(NVIC_ISPR)。

12.5.4 选择中断请求目标

每个中断的可用目的地都是固定的，如表12.3和表12.4中所述。

可以为每个中断源独立选择中断输出目标、CPU、DMAC或DTC。

Use an interrupt request destination setting that is indicated by a "✓" in the event list (see section 12.3.2. Event Number).

Note: Setting the same interrupt source for IELSRn and DELSRn is prohibited.

If the DMAC or DTC is selected as the destination for requests from an IRQi pin, you must set the IRQCRi.IRQMD[1:0] bits for that interrupt to select edge detection.

12.5.4.1 CPU interrupt request

When IELSRn.DTCE = 0, the event specified in the IELSRn register is output to the NVIC. Set the IELSRn.IELS[8:0] bits to the target event and set the IELSRn.DTCE bit to 0.

12.5.4.2 DTC activation

When IELSRn.DTCE = 1, the event specified in the IELSRn register is output to the DTC. Use the following procedure:

1. Set the IELSRn.IELS[8:0] bits to the target event and set the IELSRn.DTCE bit to 1.
2. Set the DTC Module Start bit (DTCST.DTCST) to 1.

Table 12.5 shows operation when the DTC is the interrupt request destination.

Table 12.5 Operation when DTC becomes interrupt request destination

Interrupt request destination	DISEL*1	Remaining transfer operations	Operation per request	IR*2	Interrupt request destination after transfer
DTC*3	1	≠ 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	CPU (IELSRn.DTCE bit is automatically cleared)
	0	≠ 0	DTC transfer	Cleared at the start of DTC data transfer after reading DTC transfer data	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	CPU (IELSRn.DTCE bit is automatically cleared)

Note 1. DTC.MRB.DISEL bit controles the interrupt generates timing from DTC to CPU.
Note 2. When the IELSRn.IR flag is 1, an interrupt request (DTC activation request) that occurs again is ignored.
Note 3. For chain transfers, DTC transfer continues until the last chain transfer ends. The DISEL bit state and the remaining transfer count determine whether a CPU interrupt occurs, the IELSRn.IR flag clear timing, and the interrupt request destination after transfer. See Table 16.2 in section 16, Data Transfer Controller (DTC).

Note: Error during DTC transfer

If an error response occurs during DTC transfer, the DTC notifies the ICU that an error has occurred. ICU clears all bits of the target IELSRn (n = 0 to 95). IELSRn that is not the target is not cleared.

Note: DTC transfer error in snooze mode

When an error occurs in DTC transfer in Snooze mode, ICU issues a Wake Up request. However, interrupt requests are not issued automatically. See section 16, Data Transfer Controller (DTC) chapter for information on how to set the interrupt when a DTC error occurs.

12.5.4.3 DMAC Activation

Events specified in the DELSRn registers are output to the DMAC.

To set the interrupt source for DMAC, use the following procedure:

1. Set the DELSRn.DELS[8:0] bits to the event to activate the DMAC.
2. When using interrupts to CPU, set the IELSRn.IELS bit to factor of DMAC interrupt and IELSRn.DTCE bit to 0.
3. Set the activation source for the target DMAC channel (DMACm.DMTMD.DCTG[1:0]) to 01b (interrupt module detection).
4. Set the DMAC transfer enable bit for the target DMAC channel (DMACm.DMCNT.DTE) to 1.

使用事件列表中由"✓"指示的中断请求目标设置（参见第12.3.2节。事件编号）。

Note: 禁止为IELSRn和DELSRn设置相同的中断源。

如果选择DMAC或DTC作为来自IRQi引脚的请求的目标，则必须设置IRQCRi.IRQMD[1:0]位以使该中断选择边沿检测。

12.5.4.1 CPU中断请求

当IELSRn.DTCE=0时，将IELSRn寄存器中指定的事件输出到NVIC。将IELSRn.IELS[8:0]位设置为目标事件，并将IELSRn.DTCE位设置为0。

12.5.4.2 DTC activation

当IELSRn.DTCE=1时，将IELSRn寄存器中指定的事件输出到DTC。使用以下过程：

1.将IELSRn.IELS[8:0]位设置为目标事件，并将IELSRn.DTCE位设置为1。

2.将DTC模块起始位(DTCST.DTCST)设置为1。

表12.5显示了DTC为中断请求目标时的操作。

Table 12.5 DTC成为中断请求目标时的操作

中断请求目的地	DISEL*1	剩余的转移操作	按请求操作	IR*2	传输后的中断请求目的地
DTC*3	1	≠ 0	DTC传输→CPU中断	CPU接受中断时清零	DTC
		= 0	DTC传输→CPU中断	CPU接受中断时清零	CPU（IELSRn.DTCE位自动清零）
	0	≠ 0	DTC transfer	读取DTC传输数据后，在DTC数据传输开始时清零	DTC
		= 0	DTC传输→CPU中断	CPU接受中断时清零	CPU（IELSRn.DTCE位自动清零）

注1.DTC.MRB.DISEL位控制从DTC到CPU的中断产生时序。
注2.IELSRn.IR标志为1时，忽略再次发生的中断请求（DTC激活请求）。
注3.对于链式传输，DTC传输将持续到最后一个链式传输结束。DISEL位状态和剩余传输计数决定是否发生CPU中断、IELSRn.IR标志清除时序以及传输后的中断请求目的地。请参见第16节"数据传输控制器(DTC)"中的表16.2。

Note: DTC传输期间出错

如果在DTC传输期间发生错误响应，则DTC会通知ICU发生了错误。ICU清除目标IELSRn(n=0到95)的所有位。不是目标的IELSRn不会被清除。

Note: 贪睡模式下的DTC传输错误

当贪睡模式下的DTC传输发生错误时，ICU会发出唤醒请求。但是，不会自动发出中断请求。有关如何在发生DTC错误时设置中断的信息，请参见第16节，数据传输控制器(DTC)章节。

12.5.4.3 DMAC Activation

在DELSRn寄存器中指定的事件被输出到DMAC。

要为DMAC设置中断源，请使用以下过程：

1.将DELSRn.DELS[8:0]位设置为事件以激活DMAC。

2.当对CPU使用中断时，将IELSRn.IELS位设置为DMAC中断因素，并将IELSRn.DTCE位设置为0。

3.将目标DMAC通道（DMACm.DMTMD.DCTG[1:0]）的激活源设置为01b（中断模块检测）。

4.将目标DMAC通道(DMACm.DMCNT.DTE)的DMAC传输使能位设置为1。

5. Set the DMAC operation enable bit (DMAST.DMST) to 1.

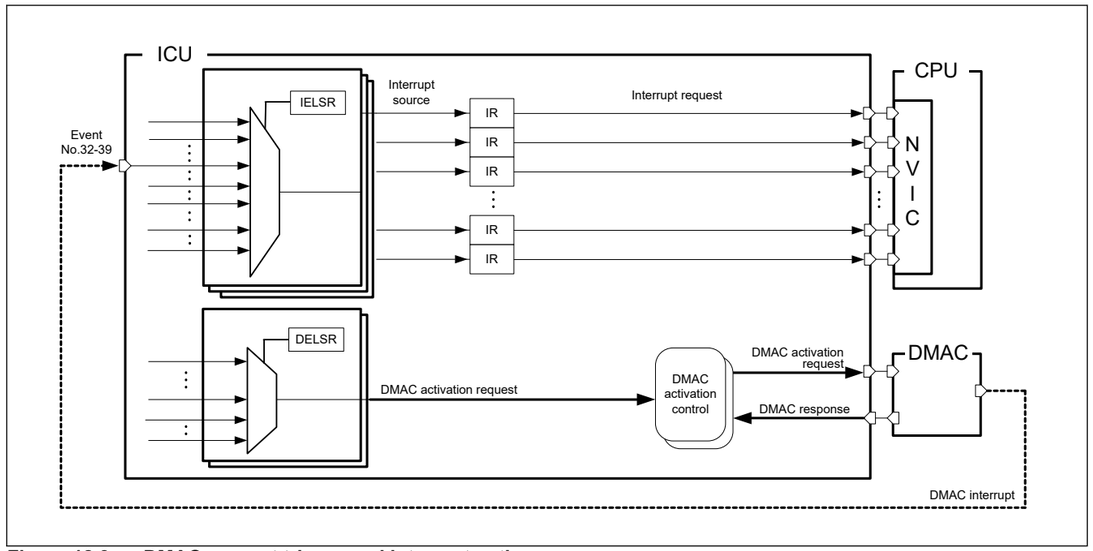


Figure 12.3 DMAC request trigger and interrupt path

Note: Error during DMAC transfer

If an error response occurs during DMAC transfer, the DMAC notifies the ICU that an error has occurred. The ICU clears all bits of the target channel of DELSRn (n = 0 to 7). DELSRn that is not the target channel is not cleared.

12.5.5 Digital Filter

A digital filter function is provided for the external interrupt request pins IRQi, (i = 0 to 15) and the NMI pin interrupt. It samples input signals on the filter PCLKB sampling clock, and removes any signal with a pulse width less than 3 sampling cycles.

To use the digital filter for an IRQi pin:

1. Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 in the IRQCRi.FCLKSEL[1:0] bits (i = 0 to 15).
2. Set the IRQCRi.FLTEN bit (i = 0 to 15) to 1 (digital filter enabled).

To use the digital filter for an NMI pin:

1. Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 in the NMICR.NFCLKSEL[1:0] bits.
2. Set the NMICR.NFLTEN bit to 1 (digital filter enabled).

Figure 12.4 shows an example of digital filter operation.

5.将DMAC操作使能位(DMAST.DMST)设置为1。

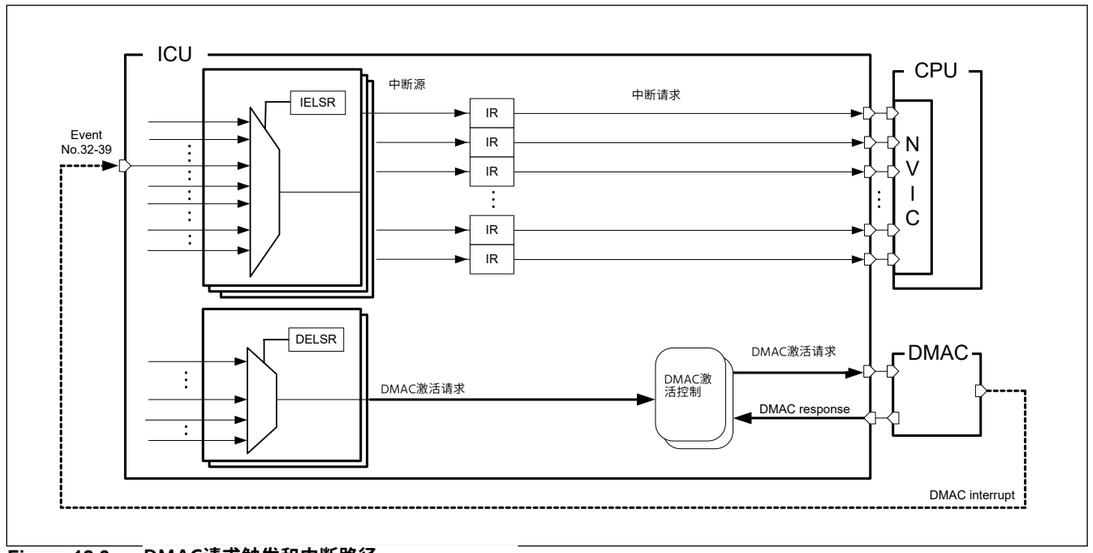


Figure 12.3 DMAC请求触发和中断路径

Note: DMAC传输期间出错

如果在DMAC传输期间发生错误响应，则DMAC会通知ICU发生了错误。ICU清除DELSRn（n=0到7）的目标通道的所有位。不是目标通道的DELSRn不会被清除。

12.5.5 数字滤波器

为外部中断请求引脚IRQi（i=0到15）和NMI引脚中断提供了数字过滤功能。它在滤波器PCLKB采样时钟上对输入信号进行采样，并去除脉冲宽度小于3个采样周期的任何信号。

为IRQi引脚使用数字滤波器：

1.在IRQCRi.FCLKSEL[1:0]位（i=0到15）中将采样时钟周期设置为PCLKB、PCLKB8、PCLKB32或PCLKB64。

2.将IRQCRi.FLTEN位（i=0到15）设置为1（启用数字滤波器）。

要将数字滤波器用于NMI引脚：

1.在NMICR.NFCLKSEL[1:0]位中将采样时钟周期设置为PCLKB、PCLKB8、PCLKB32或PCLKB64。

2.将NMICR.NFLTEN位设置为1（启用数字滤波器）。

图12.4显示了数字滤波器操作的示例。

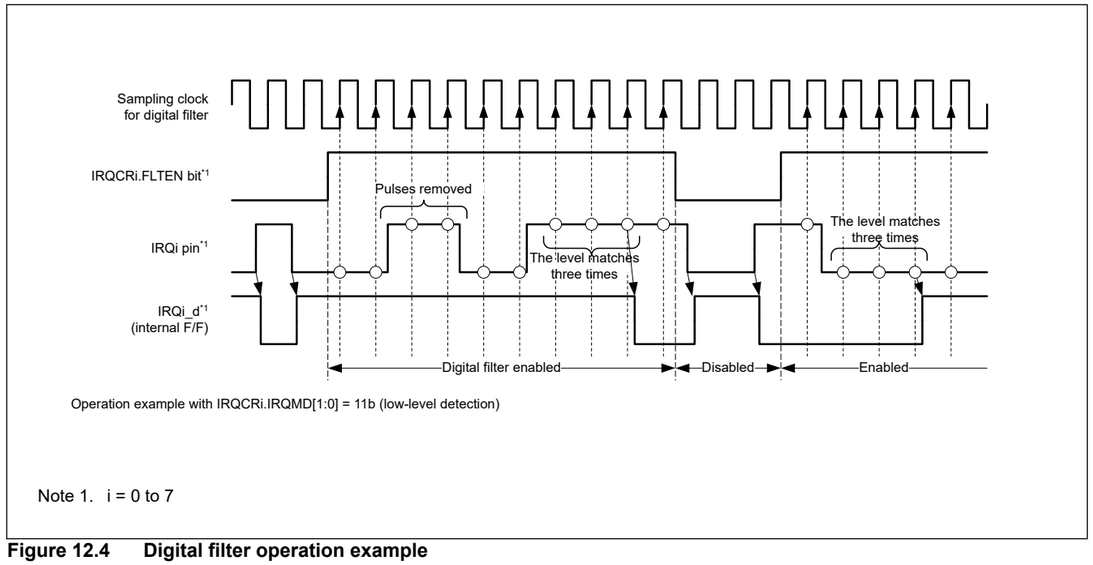


Figure 12.4 Digital filter operation example

Before entering Software Standby mode, disable the digital filters by clearing the IRQCRi.FLTEN and NMICR.NFLTEN bits. The ICU clock stops in Software Standby mode.

On exiting Software Standby, the circuit detects the edge by comparing the state before standby to the state after standby release. If the input changes during Software Standby, an incorrect edge might be detected. The digital filters can be enabled again after exiting Software Standby mode.

12.5.6 External Pin Interrupts

To use external pin interrupts:

1. Configure I/O ports settings
2. Clear the IRQCRi.FLTEN bit (i = 0 to 15) to 0 (digital filter disabled).
3. Set the IRQMD[1:0] bits of the given IRQCRi register (i = 0 to 15) to select the senses of detection.
4. Set the FCLKSEL[1:0] bits, and the FLTEN bit of the IRQCRi register.
5. Select the IRQ pin as follows:
   - If the IRQ pin is to be used for CPU interrupt requests, set the IELSRn.IELS[8:0] bits and the IELSRn.DTCE bit to 0.
   - If the IRQ pin is to be used for DTC activation, set the IELSRn.IELS[8:0] bits and the IELSRn.DTCE bit to 1.
   - If the IRQ pin is to be used for DMAC activation, set the DELSRn.DELS[8:0] bits.

12.6 Non-Maskable Interrupt Operation

The following sources can trigger a non-maskable interrupt:

- NMI pin interrupt
- Oscillation stop detection interrupt
- WDT underflow/refresh error interrupt
- IWDT underflow/refresh error interrupt
- Voltage monitor 1 interrupt
- Voltage monitor 2 interrupt
- SRAM parity error interrupt
- SRAM ECC error interrupt

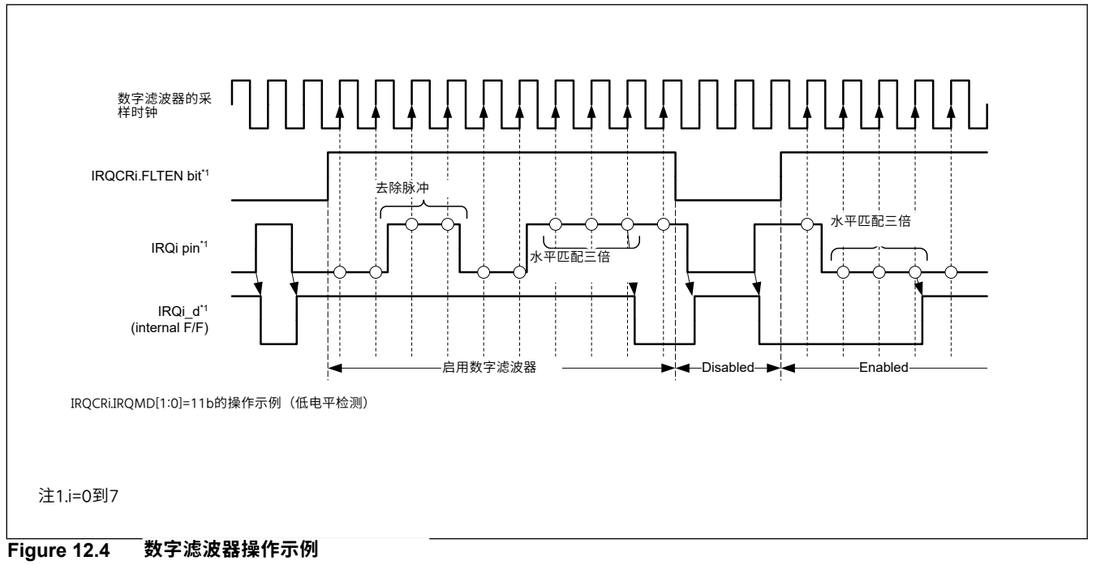


Figure 12.4 数字滤波器操作示例

在进入软件待机模式之前，通过清除IRQCRi.FLTEN和NMICR.NFLTEN位来禁用数字滤波器。ICU时钟在软件待机模式下停止。

在退出软件待机时，电路通过将待机前的状态与待机释放后的状态进行比较来检测边沿。如果在软件待机期间输入发生变化，则可能会检测到不正确的边沿。退出软件待机模式后，可以再次启用数字滤波器。

12.5.6 外部引脚中断

要使用外部引脚中断：

1.配置IO端口设置

2.将IRQCRi.FLTEN位（i=0到15）清零（禁用数字滤波器）。

3.设置给定IRQCRi寄存器（i=0到15）的IRQMD[1:0]位以选择检测的意义。

4.设置FCLKSEL[1:0]位和IRQCRi寄存器的FLTEN位。

5.选择IRQ引脚如下：

- ●如果IRQ引脚用于CPU中断请求，请将IELSRn.IELS[8:0]位和IELSRn.DTCE位设置为0。
- ●如果IRQ引脚用于DTC激活，请将IELSRn.IELS[8:0]位和IELSRn.DTCE位设置为1。
- ●如果IRQ引脚用于激活DMAC，设置DELSRn.DELS[8:0]位。

12.6 不可屏蔽中断操作

以下源可以触发不可屏蔽中断：

- ●NMI引脚中断
- ●振荡停止检测中断
- ●WDT下溢刷新错误中断
- ●IWDT下溢刷新错误中断
- ●电压监控器1中断
- ●电压监测器2中断
- ●SRAM奇偶校验错误中断
- ●SRAMECC错误中断

- MPU bus master error interrupt
- TrustZone filter error interrupt
- Cache RAM parity error interrupt.

Non-maskable interrupts can only be used with the CPU, not to activate the DTC or DMAC. Non-maskable interrupts take precedence over all other interrupts. The non-maskable interrupt states can be verified in the Non-Maskable Interrupt Status Register (NMISR). Confirm that all bits in the NMISR are 0 before returning from the NMI handler.

Non-maskable interrupts are disabled by default. To use non-maskable interrupts:

1. Clear the NMICR.NFLTEN bit to 0 (digital filter disabled).
2. Set the NMIMD bit, NFCLKSEL[1:0] bits, and NFLTEN bit of NMICR register.
3. Write 1 to the NMICLR.NMICLR bit to clear the NMISR.NMIST flag to 0.
4. Enable the non-maskable interrupt by writing 1 to the associated bit in the Non-Maskable Interrupt Enable Register (NMIER).

After 1 is written to the NMIER register, subsequent write access to the NMIEN bit in NMIER is ignored. An NMI interrupt cannot be disabled when enabled, except by a reset.

The secure attribution managed within the Application Interrupt and Reset Control Register (AIRCR) of the Arm CPU must match the security attribution of NMI.

The NMI secure of the CPU is changed by AIRCR.BFHFNMINS. It is managed by software developers who manage Secure program.

12.6.1 Correspondence to TrustZone-M by NMI

The NMI security is set by AIRCR.BFHFNMINS.

Although there is only one NMI as a CPU, multiple factors can be set.

This section describes the procedure for mixing secure and non-secure factors of NMI.

When mixing secure and non-secure, NMI related registers in the CPU should be set to Secure.

NMI-related registers:

- NMIER
- NMICLR
- NMICR

Figure 12.5 shows the flow.

●MPU总线主机错误中断

●TrustZone过滤器错误中断

●CacheRAM奇偶校验错误中断。

不可屏蔽中断只能用于CPU，不能激活DTC或DMAC。不可屏蔽中断优先于所有其他中断。不可屏蔽中断状态可以在不可屏蔽中断状态寄存器(NMISR)中验证。在从NMI处理程序返回之前，确认NMISR中的所有位都为0。

默认情况下禁用不可屏蔽中断。要使用不可屏蔽的中断：

1.将NMICR.NFLTEN位清为0（禁用数字滤波器）。

2.设置NMICR寄存器的NMIMD位、NFCLKSEL[1:0]位和NFLTEN位。

3.将1写入NMICLR.NMICLR位以将NMISR.NMIST标志清零。

4.通过将1写入不可屏蔽中断使能寄存器(NMIER)中的相关位来启用不可屏蔽中断。

将1写入NMIER寄存器后，随后对NMIER中的NMIEN位的写访问将被忽略。启用时不能禁用NMI中断，除非通过复位。

在ArmCPU的应用程序中断和复位控制寄存器(AIRCR)中管理的安全属性必须与NMI的安全属性相匹配。

CPU的NMI安全由AIRCR.BFHFNMINS更改。它由管理的软件开发人员管理
安全程序。

12.6.1 NMI与TrustZone-M的通信

NMI安全性由AIRCR.BFHFNMINS设置。

虽然只有一个NMI作为CPU，但可以设置多个因素。

本节介绍混合NMI的安全和非安全因素的过程。

混合安全和非安全时，CPU中的NMI相关寄存器应设置为Secure。

NMI-related registers:

- NMIER
- NMICLR
- NMICR

图12.5显示了流程。

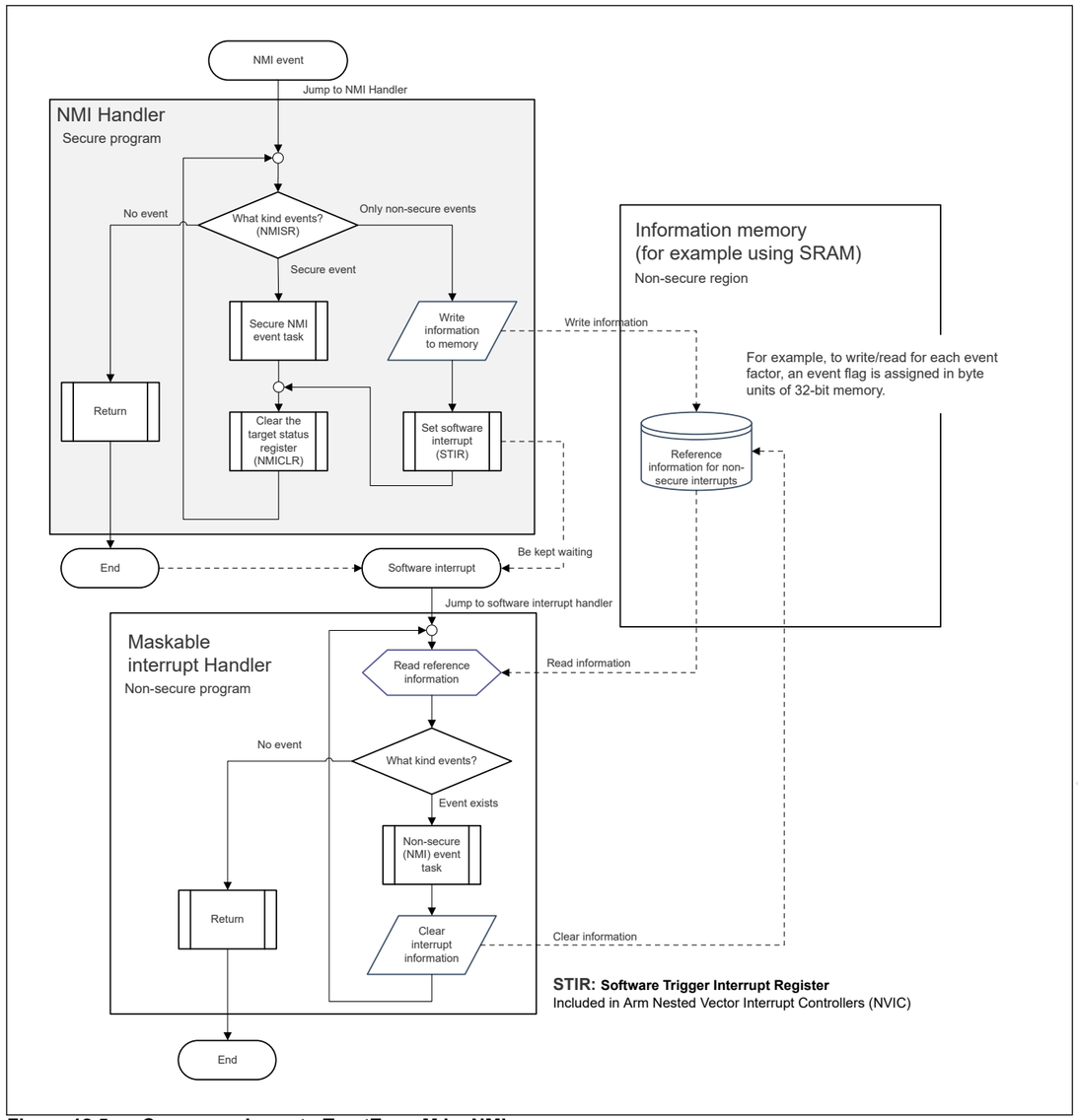


Figure 12.5 Correspondence to TrustZone-M by NMI

See the Arm documentation for details on how to move between secure and non-secure programs.

12.7 Return from Low Power Modes

Table 12.4 lists the interrupt sources that can be used to exit Sleep, Snooze, or Software Standby mode. For more information, see section 10, Low Power Modes.

12.7.1 Return from Sleep Mode

To return from Sleep mode in response to an interrupt:

non-maskable interrupt

- Use the NMIER register to enable the target interrupt request.

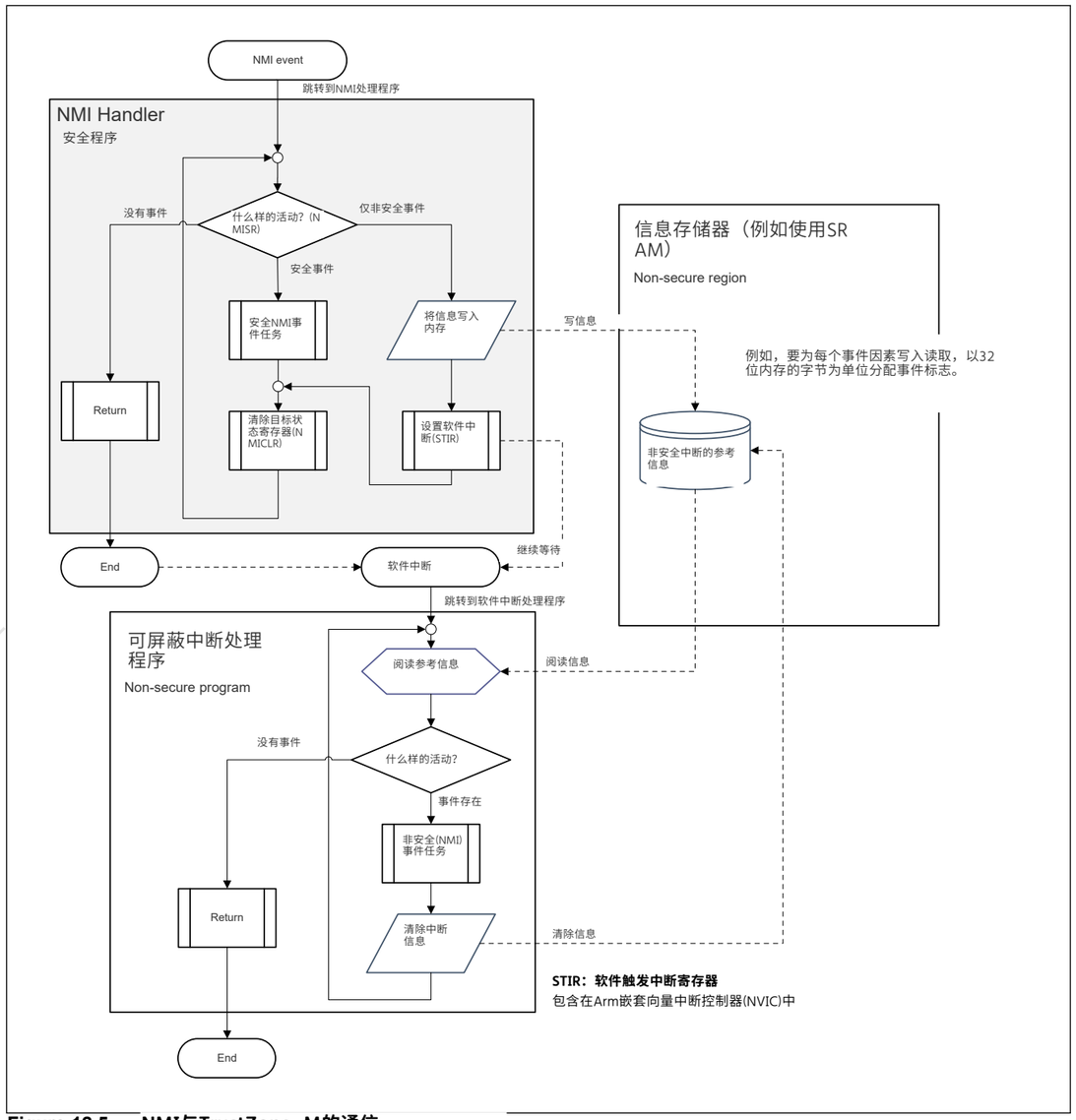


Figure 12.5 NMI与TrustZone-M的通信

有关如何在安全程序和非安全程序之间移动的详细信息，请参阅Arm文档。

12.7 从低功耗模式返回

表12.4列出了可用于退出休眠、贪睡或软件待机模式的中断源。有关详细信息，请参阅第10节，低功耗模式。

12.7.1 从睡眠模式返回

从睡眠模式返回以响应中断：

non-maskable interrupt

●使用NMIER寄存器启用目标中断请求。

maskable interrupt

- Select the CPU as the interrupt request destination.
- Enable the interrupt in the NVIC.

12.7.2 Return from Software Standby Mode

The ICU returns from Software Standby mode using a non-maskable interrupt or a maskable interrupt. For maskable interrupt of canceling source, see Table 12.4.

To return from Software Standby mode:

1. Select the interrupt source that enables return from Software Standby:
   - For non-maskable interrupts, use the NMIER register to enable the target interrupt request
   - For maskable interrupts, use the WUPEN register to enable the target interrupt request.
2. Select the CPU as the interrupt request destination
3. Enable the interrupt in the NVIC.

Interrupt requests through the IRQn pins that do not satisfy these conditions are not detected while the clock is stopped in Software Standby mode.

Similarly, request for a non-maskable interrupt from a request source whose clock is stopped in Software Standby mode cannot be detected.

Transition to/from Software Standby mode

1. Before Software Standby mode is entered, disable the digital filter for the interrupt source as a return target (IRQCRi.FLTEN = 0, NMICR.NFLTEN = 0).
2. To use the digital filter again after returning from Software Standby mode, enable the digital filter (IRQCRi.FLTEN = 1, NMICR.NFLTEN = 1).

12.7.3 Return from Snooze Mode

The ICU can return to Normal mode from Snooze mode using the interrupts provided for this mode.

To return to Normal mode from Snooze mode:

1. Set the number of the required interrupt request in SELSR0.SELS[8:0]
2. Set the value 0x02D (ICU_SNZCANCEL) in IELSRn.IELS[8:0] (n = 0 to 95).
3. Select the CPU as the interrupt request destination.
4. Enable the interrupt in the NVIC.

Interrupt requests through the non-maskable that do not satisfy the above conditions are not detected while the clock is stopped in snooze mode.

Note: In Snooze mode, a clock is supplied to the ICU. If an event selected in IELSRn is detected, the CPU acknowledges the interrupt after returning to Normal mode from Software Standby mode. If an event selected in DELSRn is detected, the DMAC can acknowledge the interrupt after returning to Normal mode from Software Standby mode.

12.8 Using the WFI Instruction with Non-Maskable Interrupts

Whenever a WFI instruction is executed, confirm that all status flags in the NMISR register are 0.

12.9 Reference

- ARM Limited., ARM® Cortex®-M33 Processor Technical Reference Manual (ARM 100230)

maskable interrupt

●选择CPU作为中断请求目标。

●在NVIC中启用中断。

12.7.2 从软件待机模式返回

ICU使用不可屏蔽中断或可屏蔽中断从软件待机模式返回。取消源的可屏蔽中断见表12.4。

从软件待机模式返回：

1.选择允许从软件待机返回的中断源：

●对于不可屏蔽的中断，使用NMIER寄存器使能目标中断请求

●对于可屏蔽中断，使用WUPEN寄存器启用目标中断请求。

2.选择CPU作为中断请求目的地

3.在NVIC中启用中断。

不满足这些条件的通过IRQn引脚的中断请求在时钟停止时不会被检测到
软件待机模式。

同样，无法检测到来自时钟在软件待机模式下停止的请求源的不可屏蔽中断请求。

从软件待机模式转换

1.在进入软件待机模式之前，禁用作为返回目标的中断源的数字滤波器（IRQCRi.FLTEN=0，NMICR.NFLTEN=0）。

2.要在从软件待机模式返回后再次使用数字滤波器，请启用数字滤波器（IRQCRi.FLTEN=1，NMICR.NFLTEN=1）。

12.7.3 从贪睡模式返回

ICU可以使用为该模式提供的中断从贪睡模式返回到正常模式。

要从贪睡模式返回正常模式：

1.在SELSR0.SELS[8:0]中设置所需中断请求的数量

2.在IELSRn.IELS[8:0]（n=0到95）中设置值0x02D(ICU_SNZCANCEL)。

3.选择CPU作为中断请求目标。

4.在NVIC中启用中断。

当时钟在贪睡模式下停止时，不会检测到通过不可屏蔽的不满足上述条件的中断请求。

Note: 在贪睡模式下，向ICU提供时钟。如果检测到在IELSRn中选择的事件，CPU在从软件待机模式返回到正常模式后确认中断。如果检测到在DELSRn中选择的事件，则DMAC可以在从软件待机模式返回正常模式后确认中断。

12.8 将WFI指令与不可屏蔽中断一起使用

每当执行WFI指令时，请确认NMISR寄存器中的所有状态标志为0。

12.9 Reference

●ARMLimited. ARM®Cortex®-M33处理器技术参考手册(ARM100230)

13. Buses

13.1 Overview

The buses consists of 32 bits AHB bus matrix. Table 13.1 lists the bus masters and bus slaves and Figure 13.1 shows the bus configuration.

Table 13.1 Bus Specifications

Classification	Bus Master/Slave name	Bus I/F Max Freq	Sync Clock	Specifications
Bus Masters	Code bus (Cortex-M33)	240 MHz	ICLK	Connected to the CPU Instruction Cache for instructions and operands
	System bus (Cortex-M33)	240 MHz	ICLK	Connected to the CPU Data Cache for system
	DMAC / DTC	240 MHz	ICLK	Connected to the DMAC/DTC
Bus Slaves	FHBIU	240 MHz	ICLK	Connected to Code Flash memory and Configuration area
	FLBIU	60 MHz	FCLK	Connected to Data Flash memory, FACI
	S0BIU	240 MHz	ICLK	Connected to SRAM0 (Standby RAM)
	PSBIU	240 MHz	ICLK	• Connected to peripheral system modules (DTC, DMAC, ICU, Flash, MPU, SRAM, Debug/Trace module, System controller and BUS controller) • Connected to peripheral modules (IIRFA, TFU, and IO ports)
	PLBIU	60 MHz	PCLKB	Connected to peripheral modules (CAC, ELC, POEG, WDT, IWDT, AGT, CANFD, TSN, ACMPHS, and KINT)
	PHBIU	120 MHz	PCLKA	Connected to peripheral modules (GPT, SCI, SPI, CRC, DOC, ADC, DAC12, CNECC, IIC, SCE5, and PDG)

Note: FHBIU: Flash High speed Bus Interface Unit.
FLBIU: Flash Low speed Bus Interface Unit.
S0BIU: SRAM0 Bus Interface Unit.
PSBIU: Peripheral System Bus Interface Unit.
PLBIU: Peripheral Low speed Bus Interface Unit.
PHBIU: Peripheral High speed Bus Interface Unit.

13. Buses

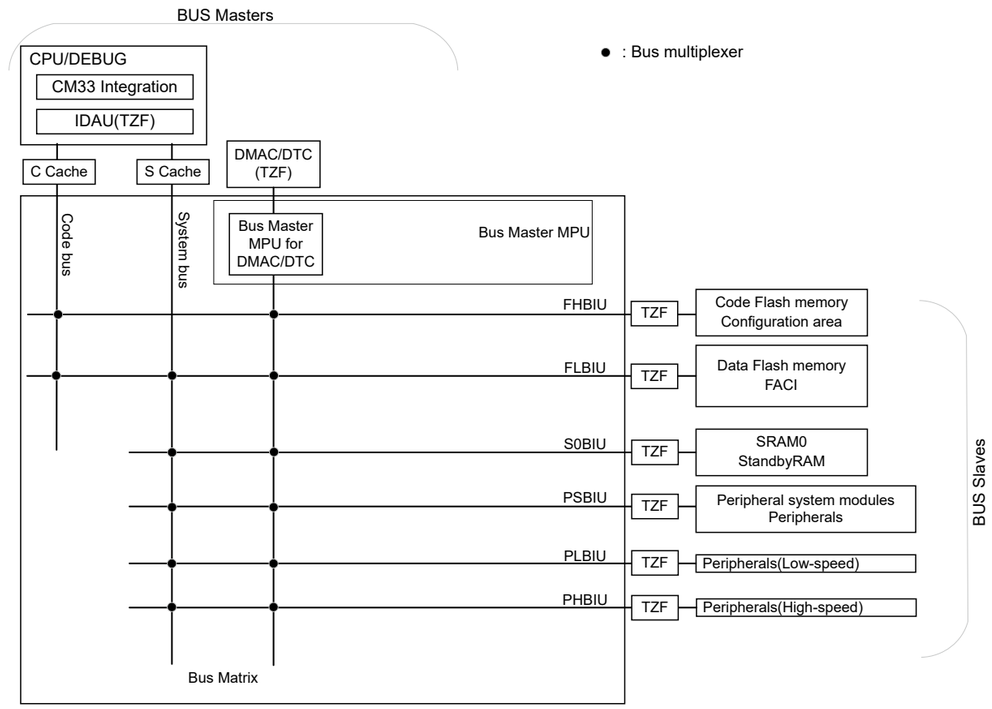
13.1 Overview

总线由32位AHB总线矩阵组成。表13.1列出了总线主机和总线从机，图13.1显示了总线配置。

Table 13.1 总线规格

Classification	总线主从名称	Bus I/F 最大频率	同步时钟	Specifications
巴士大师	代码总线(Cortex-M33)	240 MHz	ICLK	连接到CPU指令缓存以获取指令和操作数
	系统总线(Cortex-M33)	240 MHz	ICLK	连接到系统的CPU数据缓存
	DMAC / DTC	240 MHz	ICLK	连接到DMACDTC
总线从站	FHBIU	240 MHz	ICLK	连接到代码闪存和配置区
	FLBIU	60 MHz	FCLK	连接到数据闪存，FACI
	S0BIU	240 MHz	ICLK	连接到SRAM0（备用RAM）
	PSBIU	240 MHz	ICLK	• 连接外围系统模块（DTC、DMAC、ICU、Flash、MPU、SRAM、调试跟踪模块、系统控制器和总线控制器） • 连接到外围模块（IIRFA、TFU和IO端口）
	PLBIU	60 MHz	PCLKB	连接外围模块（CAC、ELC、POEG、WDT、IWDT, AGT, CANFD, TSN, ACMPHS, and KINT)
	PHBIU	120 MHz	PCLKA	连接到外围模块（GPT、SCI、SPI、CRC、DOC、ADC, DAC12, CNECC, IIC, SCE5, and PDG)

Note: FHBIU：闪存高速总线接口单元。FLBIU：闪存低速总线接口单元。
S0BIU：SRAM0总线接口单元。
PSBIU：外围系统总线接口单元。
PLBIU：外围低速总线接口单元。PHBIU：外围高速总线接口单元。



Note: TZF is TrustZone Filter. C cache is instruction cache. S cache is data cache.
For FLBIU, the code bus accesses the data flash memory and configuration areas (code region) through FLBIU. The system bus accesses FACI (peripheral region) through FLBIU.

Figure 13.1 Bus Connection

13.2 Description of Buses

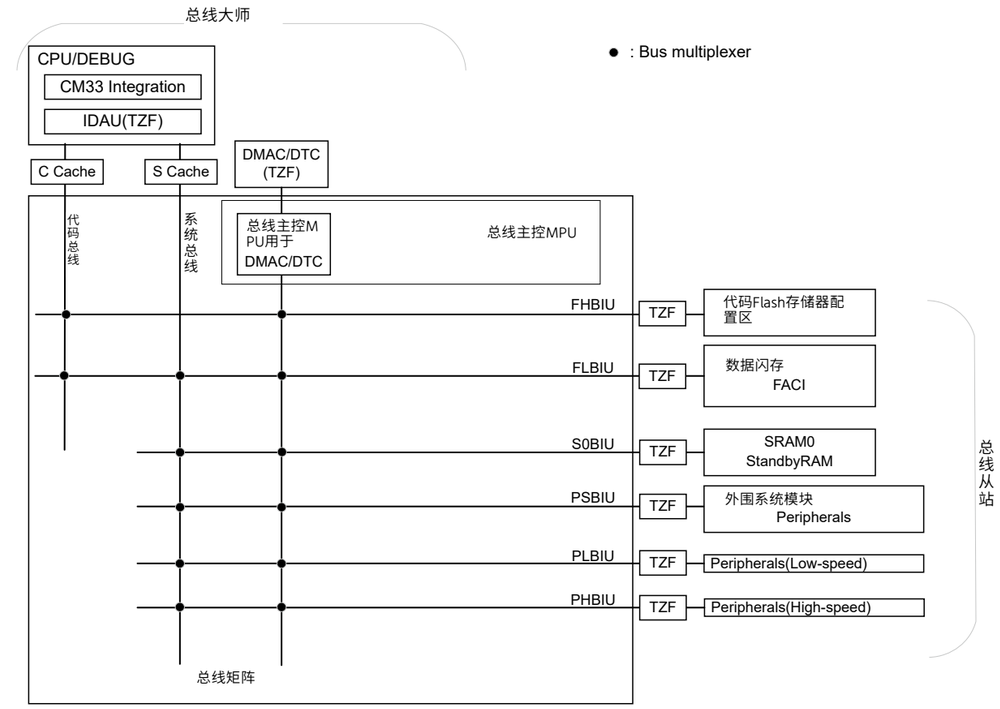
13.2.1 Arbitration

For arbitration between masters in each slave, fixed-priority and round-robin methods can be selected for each master. For details, see section 13.3.3. BUSSCNT<slave> : Slave Bus Control Register (<slave> = FHBIU, FLBIU, S0BIU), section 13.3.4. BUSSCNT<slave> : Slave Bus Control Register (<slave> = PSBIU, PLBIU, PHBIU).

13.2.2 Parallel Operation

Parallel operation is possible when different bus-master modules are requesting access to different slave modules. For example, if the CPU is fetching an instruction from Code Flash and an operand from SRAM0, the DMAC can handle transfer between a peripheral module at the same time.

Figure 13.2 shows an example of parallel operations. In this example, the CPU uses code bus and system bus for simultaneous access to FHBIU and S0BIU, respectively. Furthermore, the DMAC/DTC simultaneously accesses the peripheral bus during access to FHBIU and S0BIU by the CPU.



Note: TZF是TrustZone过滤器。C缓存是指令缓存。S缓存是数据缓存。
对于FLBIU，代码总线通过FLBIU访问数据闪存和配置区域（代码区域）。系统总线通过FLBIU访问FACI（外围区域）。

Figure 13.1 巴士连接

13.2 巴士的描述

13.2.1 Arbitration

对于每个从属设备中的主设备之间的仲裁，可以为每个主设备选择固定优先级和循环方法。详见13.3.3节。BUSSCNT<slave>：从总线控制寄存器(<slave>=FHBIU FLBIU S0BIU)，第13.3.4节。BUSSCNT<slave>:从总线控制寄存器(<slave>=PSBIU PLBIU PHBIU)。

13.2.2 并联运行

当不同的总线主模块请求访问不同的从模块时，并行操作是可能的。例如，如果CPU从CodeFlash中获取指令并从SRAM0中获取操作数，则DMAC可以同时处理外设模块之间的传输。

图13.2显示了并行操作的示例。在本例中，CPU使用代码总线和系统总线分别同时访问FHBIU和S0BIU。此外，在CPU访问FHBIU和S0BIU期间，DMACDTC同时访问外围总线。

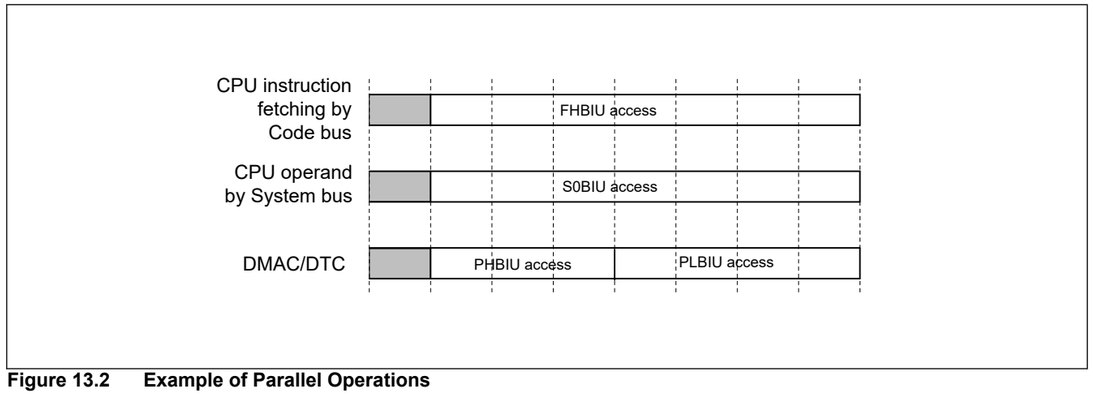


Figure 13.2 Example of Parallel Operations

13.2.3 Restrictions

(1) Restriction on Endian

Memory space must be little-endian in order to execute Cortex code.

(2) Bufferable write access

When CPU perform Bufferable Write access to PLBIU or PHBIU, if an STZF error occurs then the error response is invalidated. So there is no error flag will be set and no NMI / RESET request is generated.

When CPU perform Bufferable Write access to PHBIU, if a Slave BUS error occurs then the error response will become invalid and the error flag will not be set.

If error response is required, set the bus master to non-bufferable access.

(3) Access to reserved area of FLBIU and S0BIU

Access to the reserved area of FLBIU and S0BIU is prohibited. Operation is not guaranteed if accessed.

(4) Clock setting

The clock division ratio prohibits setting changes during slave bus access to FLBIU, PLBIU, and PHBIU.

13.3 Register Descriptions

13.3.1 BUSSARA : BUS Security Attribution Register A

Base address: CPSCU = 0x4000_8000

Offset address: 0x0100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUSSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

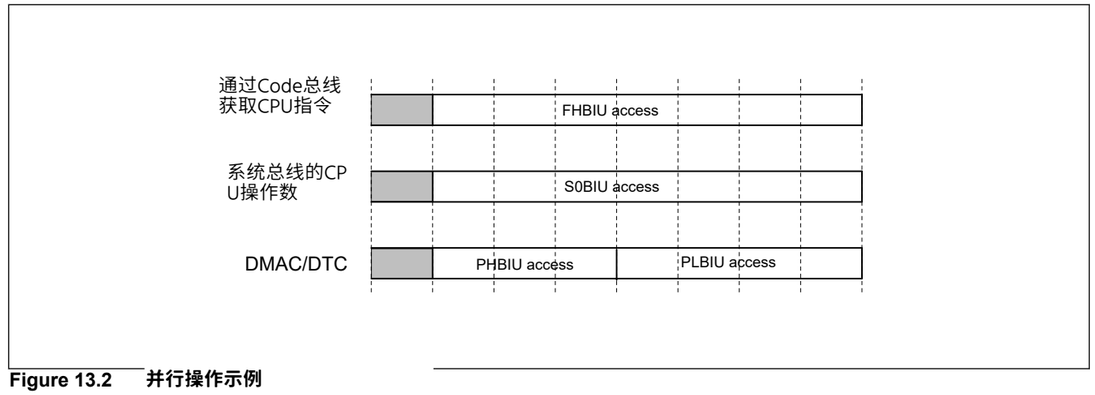


Figure 13.2 并行操作示例

13.2.3 Restrictions

(1) 对字节序的限制

为了执行Cortex代码，内存空间必须是little-endian。

(2) 可缓冲的写访问

当CPU对PLBIU或PHBIU执行BufferableWrite访问时，如果发生STZF错误，则错误响应无效。因此不会设置错误标志，也不会生成NMIRESET请求。

当CPU对PHBIU执行BufferableWrite访问时，如果发生SlaveBUS错误，则错误响应将变为无效且错误标志不会被设置。

如果需要错误响应，请将总线主机设置为非缓冲访问。

(3) 访问FLBIU和S0BIU的保留区

禁止访问FLBIU和S0BIU的保留区域。如果访问，则无法保证操作。

(4) 时钟设置

时钟分频比禁止在从总线访问FLBIU、PLBIU和PHBIU期间更改设置。

13.3 注册说明

13.3.1 BUSSARA:BUS安全属性寄存器A

Base address: CPSCU = 0x4000_8000

Offset address: 0x0100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUSSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	BUSSA0	BUS Security Attribution A0 0: Secure 1: Non-Secure	R/W
31:1	—	These bits are read as 1.	R

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

BUSSA0 bit (BUS Security Attribution A0)

The correspondence between register and BIU name is as follows

Connection (BUSSCNT<slave> = FHBIU/FLBIU/S0BIU/PSBIU/PLBIU/PHBIU)

Please see to Figure 13.1 for connection between BIU and BUS

- BUSSCNTFHBIU
- BUSSCNTFLBIU
- BUSSCNTS0BIU
- BUSSCNTPSBIU
- BUSSCNTPLBIU
- BUSSCNTPHBIU

13.3.2 BUSSARB : BUS Security Attribution Register B

Base address: CPSCU = 0x4000_8000
Offset address: 0x0104

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUSSB0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	BUSSB0	BUS Security Attribution B0 0: Secure 1: Non-Secure	R/W
31:1	—	These bits are read as 1.	R

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

BUSSB0 bit (BUS Security Attribution B0)

The BUSSB0 bit specifies the security attributes of registers for Bus Error Clear registers and DMAC/DTC Error Clear register.

BUS1ERRCLR: Code bus

BUS2ERRCLR: System bus

BUS3ERRCLR: DMAC/DTC

DMACDTCERRCLR: DMAC/DTC (Master-TZF)

See Figure 13.1 for connection of each BUS.

Bit	Symbol	Function	R/W
0	BUSSA0	BUS安全属性A0 0: Secure 1: Non-Secure	R/W
31:1	—	这些位读为1。	R

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

BUSSA0位（BUS安全属性A0）

寄存器和BIU名称的对应关系如下

Connection (BUSSCNT<slave> = FHBIU/FLBIU/S0BIU/PSBIU/PLBIU/PHBIU)

BIU和BUS的连接见图13.1

- BUSSCNTFHBIU
- BUSSCNTFLBIU
- BUSSCNTS0BIU
- BUSSCNTPSBIU
- BUSSCNTPLBIU
- BUSSCNTPHBIU

13.3.2 BUSSARB:BUS安全属性寄存器B

Base address: CPSCU = 0x4000_8000
Offset address: 0x0104

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUSSB0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	BUSSB0	BUS安全属性B0 0: Secure 1: Non-Secure	R/W
31:1	—	这些位读为1。	R

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

BUSSB0位（BUS安全属性B0）

BUSSB0位指定总线错误清除寄存器和DMACDTC错误清除寄存器的安全属性。

BUS1ERRCLR：代码总线

BUS2ERRCLR：系统总线

BUS3ERRCLR: DMAC/DTC

DMACDTCERRCLR: DMAC/DTC (Master-TZF)

每个BUS的连接请参见图13.1。

13.3.3 BUSSCNT<slave> : Slave Bus Control Register (<slave> = FHBIU, FLBIU, S0BIU)

Base address: BUS = 0x4000_3000

Offset address: 0x1100 (BUSSCNTFHBIU)
0x1104 (BUSSCNTFLBIU)
0x1110 (BUSSCNTS0BIU)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARBS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ARBS[1:0]	Arbitration Select for two masters Specify the priority between bus master. > : Fixed Priority ↔: Round-Robin 0 0: DMAC/DTC > CPU 0 1: DMAC/DTC ↔ CPU 1 0: Setting prohibited 1 1: Setting prohibited	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note:
- BUSSCNT<slave> : <slave> is bus interface unit name for Slave
- The change is prohibited from initial value (0) to reserved bit. Operation when changing is not guaranteed.

ARBS[1:0] bits (Arbitration Select for two masters)

The ARBS bits sets the arbitration method of each master.

13.3.4 BUSSCNT<slave> : Slave Bus Control Register (<slave> = PSBIU, PLBIU, PHBIU)

Base address: BUS = 0x4000_3000

Offset address: 0x1120 (BUSSCNTPSBIU)
0x1130 (BUSSCNTPLBIU)
0x1134 (BUSSCNTPHBIU)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARBS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ARBS	Arbitration Select for two masters Specify the priority between bus master. > : Fixed Priority ↔: Round-Robin 0: DMAC/DTC > CPU 1: DMAC/DTC ↔ CPU	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note:
- BUSSCNT<slave> : <slave> is bus interface unit name for Slave
- The change is prohibited from initial value (0) to reserved bit. Operation when changing is not guaranteed.

13.3.3 BUSSCNT<slave>:从总线控制寄存器(<slave>=FHBIU FLBIU S0BIU)

Base address: BUS = 0x4000_3000

Offset address: 0x1100 (BUSSCNTFHBIU)
0x1104 (BUSSCNTFLBIU)
0x1110 (BUSSCNTS0BIU)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARBS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ARBS[1:0]	两个主机的仲裁选择 指定总线主机之间的优先级。>:固定优 先级↔:循环 00：DMACDTC>CPU01 ：DMACDTC↔CPU10： 禁止设置11：禁止设置	R/W
15:2	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note:
- BUSSCNT<slave>:<slave>是Slave的总线接口单元名称
- 禁止从初始值(0)更改为保留位。不保证更换时的操作。

ARBS[1:0]位（两个主机的仲裁选择）

ARBS位设置每个主机的仲裁方法。

13.3.4 BUSSCNT<slave>:从总线控制寄存器(<slave>=PSBIU PLBIU PHBIU)

Base address: BUS = 0x4000_3000

Offset address: 0x1120 (BUSSCNTPSBIU)
0x1130 (BUSSCNTPLBIU)
0x1134 (BUSSCNTPHBIU)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARBS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ARBS	两个主机的仲裁选择 指定总线主机之间的优先级。>:固定优 先级↔:循环 0: DMAC/DTC > CPU 1: DMAC/DTC ↔ CPU	R/W
15:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note:
- BUSSCNT<slave>:<slave>是Slave的总线接口单元名称
- 禁止从初始值(0)更改为保留位。不保证更换时的操作。

ARBS bit (Arbitration Select for two masters)

The ARBS bits sets the arbitration method of each master.

13.3.5 BUSnERRADD : BUS Error Address Register (n = 1 to 3)

Base address: BUS = 0x4000_3000

Offset address: 0x1800 + 0x10 × (n - 1)

Bit position:	31																													0
Bit field:	BERAD[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	BERAD[31:0]	Bus Error Address When a bus error occurs, these bits store the error address	R

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU- and TZF-related resets, see section 5, Resets, section 14, Memory Protection Unit (MPU) and section 45.2. Arm TrustZone Security .

The following bus errors correspond to the master bus:

BUS1ERRADD : Code bus

BUS2ERRADD : System bus

BUS3ERRADD : DMAC/DTC

BERAD[31:0] bits (Bus Error Address)

The BERAD[31:0] bits indicate the address when an error occurs on the associated bus. For detail of error that occurs by bus, see section 13.3.9. BUSnERRSTAT : BUS Error Status Register n (n = 1 to 3) and section 13.4. Bus Error Monitoring Section.

When an error occurs on the bus, the corresponding bit of ILERRSTAT, MMERRSTAT, SLERRSTAT in BUSnERRSTAT (n = 1 to 3) is set to 1, at the same time, the BERAD[31:0] bits store the address of the bus error access.

BERAD[31:0] bits are only valid when ILERRSTAT, MMERRSTAT, and SLERRSTAT in BUSnERRSTAT (n = 1 to 3) are set to 1.

13.3.6 BUSnERRRW : BUS Error Read Write Register (n = 1 to 3)

Base address: BUS = 0x4000_3000

Offset address: 0x1804 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	RWSTAT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RWSTAT	Error Access Read/Write Status The status at the time of the error 0: Read access 1: Write access	R
7:1	—	These bits are read as 0. The write value should be 0.	R/W

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

ARBS位（两个主机的仲裁选择）

ARBS位设置每个主机的仲裁方法。

13.3.5 BUSnERRADD：总线错误地址寄存器（n=1到3）

Base address: BUS = 0x4000_3000

Offset address: 0x1800 + 0x10 × (n - 1)

Bit position:	31																													0
Bit field:	BERAD[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	BERAD[31:0]	总线错误地址 当发生总线错误时，这些位存储错误地址	R

该寄存器由除MPU和TZF相关的复位之外的复位清除，这些复位是总线主控MPU错误复位和TrustZone过滤器错误重置。

有关MPU和TZF相关复位的详细信息，请参阅第5节，复位，第14节，内存保护单元(MPU)和第45.2节。ArmTrustZone安全。

以下总线错误对应于主总线：

BUS1ERRADD:代码总线

BUS2ERRADD:系统总线

BUS3ERRADD : DMAC/DTC

BERAD[31:0]位（总线错误地址）

BERAD[31:0]位指示相关总线上发生错误时的地址。有关总线发生错误的详细信息，请参阅第13.3.9节。BUSnERRSTAT：总线错误状态寄存器n（n=1到3）和第13.4节。总线错误监控部分。

当总线发生错误时，BUSnERRSTAT（n=1～3）中ILERRSTAT、MMERRSTAT、SLERRSTAT的对应位置1，同时BERAD[31:0]位存储总线地址错误访问。

BERAD[31:0]位仅在BUSnERRSTAT（n=1至3）中的ILERRSTAT、MMERRSTAT和SLERRSTAT设置为1时有效。

13.3.6 BUSnERRRW：总线错误读写寄存器（n=1到3）

Base address: BUS = 0x4000_3000

Offset address: 0x1804 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	RWSTAT
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RWSTAT	错误访问读写状态 出错时的状态 0：读访问1：写访问	R
7:1	—	这些位被读取为0。写入值应为0。	R/W

该寄存器由除MPU和TZF相关的复位之外的复位清除，这些复位是总线主控MPU错误复位和TrustZone过滤器错误重置。

For detail of MPU related reset, see section 5, Resets and section 14, Memory Protection Unit (MPU).

The following bus errors correspond to the master bus:

BUS1ERRRW : Code bus

BUS2ERRRW : System bus

BUS3ERRRW : DMAC/DTC

RWSTAT bit (Error Access Read/Write Status)

The RWSTAT bit indicates the access status, (write access or read access) when an error occurs on the associated bus. For detail of error that occurs by bus, see section 13.3.9. BUSnERRSTAT : BUS Error Status Register n (n = 1 to 3) and section 13.4. Bus Error Monitoring Section.

When an error occurs on the bus, the corresponding bit of ILERRSTAT, MMERRSTAT, SLERRSTAT in BUSnERRSTAT (n = 1 to 3) is set to 1, at the same time, the RWSTAT bits store the read/write status of the bus error access.

RWSTAT bit is only valid when ILERRSTAT, MMERRSTAT, and SLERRSTAT in BUSnERRSTAT (n = 1 to 3) are set to 1.

13.3.7 BTZFnERRADD : BUS TZF Error Address Register (n = 1 to 3)

Base address: BUS = 0x4000_3000

Offset address: 0x1900 + 0x10 × (n - 1)

Bit position:	31																													0
Bit field:	BTZFERAD[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	BTZFERAD[31:0]	Bus TrustZone Filter Error Address When a bus error occurs, these bits store the error address	R

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU- and TZF-related resets, see section 5, Resets, section 14, Memory Protection Unit (MPU) and section 45.2. Arm TrustZone Security .

The following bus errors correspond to the master bus:

BTZF1ERRADD : Code bus

BTZF2ERRADD : System bus

BTZF3ERRADD : DMAC/DTC

See Figure 13.1 for connection of each BUS.

BTZFERAD[31:0] bits (Bus TrustZone Filter Error Address)

The BTZFERAD[31:0] bits indicate the address, when an error occurs on the associated bus. For detail of error that occurs by bus, see section 13.3.9. BUSnERRSTAT : BUS Error Status Register n (n = 1 to 3) and section 13.4. Bus Error Monitoring Section.

When an error occurs on the bus, the corresponding bit of STERRSTAT in BUSnERRSTAT (n = 1 to 3) is set to 1, at the same time, the BTZFERAD[31:0] bits store the address of the bus error access.

BTZFERAD[31:0] bits are only valid when STERRSTAT in BUSnERRSTAT (n = 1 to 3) is set to 1.

有关MPU相关复位的详细信息，请参阅第5节，复位和第14节，内存保护单元(MPU)。

以下总线错误对应于主总线：

BUS1ERRRW:代码总线

BUS2ERRRW:系统总线

BUS3ERRRW : DMAC/DTC

RWSTAT位（错误访问读写状态）

RWSTAT位指示相关总线上发生错误时的访问状态（写访问或读访问）。有关总线发生错误的详细信息，请参阅第13.3.9节。BUSnERRSTAT：总线错误状态寄存器n（n=1到3）和第13.4节。总线错误监控部分。

当总线发生错误时，BUSnERRSTAT（n=1～3）中ILERRSTAT、MMERRSTAT、SLERRSTAT的相应位设置为1，同时RWSTAT位存储总线错误访问的读写状态。

RWSTAT位仅在BUSnERRSTAT（n=1至3）中的ILERRSTAT、MMERRSTAT和SLERRSTAT设置为1时有效。

13.3.7 BTZFnERRADD:BUSTZF错误地址寄存器(n=1to3)

Base address: BUS = 0x4000_3000

Offset address: 0x1900 + 0x10 × (n - 1)

Bit position:	31																													0
Bit field:	BTZFERAD[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	BTZFERAD[31:0]	总线TrustZone过滤器错误地址 当发生总线错误时，这些位存储错误地址	R

该寄存器由除MPU和TZF相关的复位之外的复位清除，这些复位是总线主控MPU错误复位和TrustZone过滤器错误重置。

有关MPU和TZF相关复位的详细信息，请参阅第5节，复位，第14节，内存保护单元(MPU)和第45.2节。ArmTrustZone安全。

以下总线错误对应于主总线：

BTZF1ERRADD:代码总线

BTZF2ERRADD:系统总线

BTZF3ERRADD : DMAC/DTC

每个BUS的连接请参见图13.1。

BTZFERAD[31:0]位（总线TrustZone过滤器错误地址）

当相关总线上发生错误时，BTZFERAD[31:0]位指示地址。有关总线发生错误的详细信息，请参阅第13.3.9节。BUSnERRSTAT：总线错误状态寄存器n（n=1到3）和第13.4节。总线错误监控部分。

当总线发生错误时，BUSnERRSTAT(n=1到3)中的STERRSTAT对应位设置为1，同时BTZFERAD[31:0]位存储总线错误访问的地址。

BTZFERAD[31:0]位仅在BUSnERRSTAT（n=1至3）中的STERRSTAT设置为1时有效。

13.3.8 BTZFnERRRW : BUS TZF Error Read Write Register (n = 1 to 3)

Base address: BUS = 0x4000_3000

Offset address: 0x1904 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TRWSTAT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TRWSTAT	TrustZone filter error access Read/Write Status The status at the time of the error 0: Read access 1: Write access	R
7:1	—	These bits are read as 0. The write value should be 0.	R/W

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU- and TZF-related resets, see section 5, Resets, section 14, Memory Protection Unit (MPU) and section 45.2. Arm TrustZone Security .

The following bus errors correspond to the master bus:

BTZF1ERRRW : Code bus

BTZF2ERRRW : System bus

BTZF3ERRRW : DMAC/DTC

See Figure 13.1 for connection of each BUS.

TRWSTAT bit (TrustZone filter error access Read/Write Status)

The TRWSTAT bit indicates the access status, (write access or read access), when an error occurs on the associated bus. For detail of error that occurs by bus, see section 13.3.9. BUSnERRSTAT : BUS Error Status Register n (n = 1 to 3) and section 13.4. Bus Error Monitoring Section.

When an error occurs on the bus, the corresponding bit of STERRSTAT in BUSnERRSTAT (n = 1 to 3) is set to 1, at the same time, the TRWSTAT bits store the read/write status of the bus error access. The TRWSTAT bit is only valid when STERRSTAT in BUSnERRSTAT (n = 1 to 3) is set to 1.

13.3.9 BUSnERRSTAT : BUS Error Status Register n (n = 1 to 3)

Base address: BUS = 0x4000_3000

Offset address: 0x1A00 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	ILERRSTAT	MMERRSTAT	—	STERRSTAT	SLERRSTAT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SLERRSTAT	Slave bus Error Status 0: No error occurred 1: Error occurred	R
1	STERRSTAT	Slave TrustZone filter Error Status 0: No error occurred 1: Error occurred	R
2	—	This bit is read as 0.	R

13.3.8 BTZFnERRRW：BUSTZF错误读写寄存器（n=1到3）

Base address: BUS = 0x4000_3000

Offset address: 0x1904 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TRWSTAT
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TRWSTAT	TrustZone过滤器错误访问读写状态 出错时的状态 0：读访问1：写访问	R
7:1	—	这些位被读取为0。写入值应为0。	R/W

该寄存器由除MPU和TZF相关的复位之外的复位清除，这些复位是总线主控MPU错误复位和TrustZone过滤器错误重置。

有关MPU和TZF相关复位的详细信息，请参阅第5节，复位，第14节，内存保护单元(MPU)和第45.2节。ArmTrustZone安全。

以下总线错误对应于主总线：

BTZF1ERRRW:代码总线

BTZF2ERRRW:系统总线

BTZF3ERRRW : DMAC/DTC

每个BUS的连接请参见图13.1。

TRWSTAT位（TrustZone过滤器错误访问读写状态）

当相关总线上发生错误时，TRWSTAT位指示访问状态（写访问或读访问）。有关总线发生错误的详细信息，请参阅第13.3.9节。BUSnERRSTAT：总线错误状态寄存器n（n=1到3）和第13.4节。总线错误监控部分。

当总线发生错误时，BUSnERRSTAT（n=1～3）中STERRSTAT的对应位被置1，同时TRWSTAT位存储总线错误访问的读写状态。TRWSTAT位仅在BUSnERRSTAT（n=1至3）中的STERRSTAT设置为1时有效。

13.3.9 BUSnERRSTAT:BUS错误状态寄存器n(n=1到3)

Base address: BUS = 0x4000_3000

Offset address: 0x1A00 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	ILERRSTAT	MMERRSTAT	—	STERRSTAT	SLERRSTAT
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SLERRSTAT	从站总线错误状态 0：未发生错误1：发生错误	R
1	STERRSTAT	从站TrustZone过滤器错误状态 0：未发生错误1：发生错误	R
2	—	该位读为0。	R

Bit	Symbol	Function	R/W
3	MMERRSTAT	Master MPU Error Status 0: No error occurred 1: Error occurred	R
4	ILERRSTAT	Illegal address access Error Status 0: No error occurred 1: Error occurred	R
7:5	—	These bits are read as 0.	R

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU- and TZF-related resets, see section 5, Resets, section 14, Memory Protection Unit (MPU) and section 45.2. Arm TrustZone Security .

The following bus errors correspond to the master bus:

BUS1ERRSTAT : Code bus

BUS2ERRSTAT : System bus

BUS3ERRSTAT : DMAC/DTC

See Figure 13.1 for connection of each BUS

When an illegal access error, master MPU error, and slave bus error all occurred at the same time, the STAT bit is only valid in the following order of priority. The left side has higher priority.

Master MPU Error > Illegal access error, slave bus error

Note: Illegal access error and slave bus error do not occur at the same time.

If one of ILERRSTAT, MMERRSTAT or SLERRSTAT is set, these bits are not renewed until it is cleared.

SLERRSTAT bit (Slave bus Error Status)

When slave error occurs by bus, BUSnERRSTAT.SLERRSTAT (n = 1 to 3) is set to 1. Clear condition is reset or set BUSnERRCLR.SLERRCLR (n = 1 to 3) to 1. Slave error is an error that occurs on a slave such as a timeout. For detail of slave error that occurs by bus, see section 13.4. Bus Error Monitoring Section.

STERRSTAT bit (Slave TrustZone filter Error Status)

When slave TrustZone filter error occurs by bus, BUSnERRSTAT.STERRSTAT (n = 1 to 3) is set to 1. Clear condition is reset or set BUSnERRCLR.STERRCLR (n = 1 to 3) to 1. The STERRSTAT bit is not set when the debugger accesses the security area. For detail of slave TrustZone filter error that occurs by bus, see section 45, Security Features .

MMERRSTAT bit (Master MPU Error Status)

When master MPU error occurs by bus, BUSnERRSTAT.MMERRSTAT (n = 1 to 3) is set to 1. Clear condition is reset or set BUSnERRCLR.MMERRCLR (n = 1 to 3) to 1. For detail of master MPU error that occurs by bus, see section 14, Memory Protection Unit (MPU).

Note: At master MPU error is occur in DMAC or DTC access, if error address value is not as master MPU area, Illegal address access error or slave error is occurring before DMAC or DTC access. Decide the what error was happened by referring the error address value.

ILERRSTAT bit (Illegal address access Error Status)

When illegal address access error occurs by bus, BUSnERRSTAT.ILERRSTAT (n = 1 to 3) is set to 1. Clear condition is reset or set BUSnERRCLR.ILERRCLR (n = 1 to 3) to 1. For detail of illegal address access error that occurs by bus, see section 13.4. Bus Error Monitoring Section.

Bit	Symbol	Function	R/W
3	MMERRSTAT	主控MPU错误状态 0：未发生错误1：发生错误	R
4	ILERRSTAT	非法地址访问错误状态 0：未发生错误1：发生错误	R
7:5	—	这些位读为0。	R

该寄存器由除MPU和TZF相关的复位之外的复位清除，这些复位是总线主控MPU错误复位和TrustZone过滤器错误重置。

有关MPU和TZF相关复位的详细信息，请参阅第5节，复位，第14节，内存保护单元(MPU)和第45.2节。ArmTrustZone安全。

以下总线错误对应于主总线：

BUS1ERRSTAT:代码总线

BUS2ERRSTAT:系统总线

BUS3ERRSTAT : DMAC/DTC

每个BUS的连接见图13.1

当非法访问错误、主MPU错误和从总线错误同时发生时，STAT位仅按以下优先级顺序有效。左侧优先级更高。

MasterMPUError>Illegalaccesserror slavebuserror

Note: 非法访问错误和从总线错误不会同时发生。

如果ILERRSTAT、MMERRSTAT或SLERRSTAT之一被设置，则这些位在被清除之前不会更新。

SLERRSTAT位（从总线错误状态）

当总线发生从机错误时，BUSnERRSTAT.SLERRSTAT(n=1to3)设置为1。清除条件被复位或设置BUSnERRCLR.SLERRCLR(n=1to3)to1。从站错误是发生在从站上的错误，例如超时。关于总线发生的从站错误的详细信息，请参阅13.4节。总线错误监控部分。

STERRSTAT位（从属TrustZone过滤器错误状态）

当总线发生从机TrustZone过滤器错误时，BUSnERRSTAT.STERRSTAT（n=1至3）设置为1。清除条件复位或设置BUSnERRCLR.STERRCLR（n=1至3）为1。STERRSTAT位不设置时调试器访问安全区域。有关总线发生的从属TrustZone过滤器错误的详细信息，请参阅第45节，安全功能。

MMERRSTAT位（主MPU错误状态）

当总线发生主MPU错误时，BUSnERRSTAT.MMERRSTAT(n=1到3)设置为1。清除条件复位或设置BUSnERRCLR.MMERRCLR(n=1到3)为1。有关发生的主MPU错误的详细信息通过总线，请参阅第14节，内存保护单元(MPU)。

Note: 在访问DMAC或DTC时发生主MPU错误，如果错误地址值不是主MPU区域，则在访问DMAC或DTC之前发生非法地址访问错误或从站错误。通过参考错误地址值来确定发生了什么错误。

ILERRSTAT位（非法地址访问错误状态）

当总线发生非法地址访问错误时，BUSnERRSTAT.ILERRSTAT(n=1至3)设置为1。清除条件复位或设置BUSnERRCLR.ILERRCLR(n=1至3)为1。有关非　　法地址访问错误的详细信息由公共汽车发生，请参阅第13.4节。总线错误监控部分。

13.3.10 DMACDTCERRSTAT : DMAC/DTC Error Status Register

Base address: BUS = 0x4000_3000

Offset address: 0x1A24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MTERRSTAT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MTERRSTAT	Master TrustZone Filter Error Status 0: No error occurred 1: Error occurred	R
7:1	—	These bits are read as 0.	R

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU- and TZF-related resets, see section 5, Resets, section 14, Memory Protection Unit (MPU) and section 45.2. Arm TrustZone Security .

MTERRSTAT bit (Master TrustZone Filter Error Status)

When a master TrustZone filter error occurs by DMAC or DTC, DMACDTCERRSTAT.MTERRSTAT is set to 1. Clear condition is reset or set DMACDTCERRCLR.MTERRCLR to 1.

For detail of master TrustZone filter error that occurs by DMAC or DTC, see section 15, DMA Controller (DMAC) and section 16, Data Transfer Controller (DTC)

13.3.11 BUSnERRCLR : BUS Error Clear Register n (n = 1 to 3)

Base address: BUS = 0x4000_3000

Offset address: 0x1A08 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	ILERRCLR	MMERRCLR	—	STERRCLR	SLERRCLR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SLERRCLR	Slave bus Error Clear Writing 1 to the SLERRCLR bit clears the BUSnERRSTAT.SLERRSTAT (n = 1 to 3)	R/W*1
1	STERRCLR	Slave TrustZone filter Error Clear Writing 1 to the STERRCLR bit clears the BUSnERRSTAT.STERRSTAT (n = 1 to 3)	R/W*1
2	—	This bit is read as 0. The write value should be 0.	R/W
3	MMERRCLR	Master MPU Error Clear Writing 1 to the MMERRCLR bit clears the BUSnERRSTAT.MMERRSTAT (n = 1 to 3)	R/W*1
4	ILERRCLR	Illegal Address Access Error Clear Writing 1 to the ILERRCLR bit clears the BUSnERRSTAT.ILERRSTAT (n = 1 to 3)	R/W*1
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Only 1 can be written to this bit. This bit is read as 0. Writing 0 to this bit has no effect.

The following bus errors correspond to the master bus:

13.3.10 DMACDTCERRSTAT：DMACDTC错误状态寄存器

Base address: BUS = 0x4000_3000

Offset address: 0x1A24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MTERRSTAT
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MTERRSTAT	主TrustZone过滤器错误状态 0：未发生错误1：发生错误	R
7:1	—	这些位读为0。	R

该寄存器由除MPU和TZF相关的复位之外的复位清除，这些复位是总线主控MPU错误复位和TrustZone过滤器错误重置。

有关MPU和TZF相关复位的详细信息，请参阅第5节，复位，第14节，内存保护单元(MPU)和第45.2节。ArmTrustZone安全。

MTERRSTAT位（主TrustZone过滤器错误状态）

当DMAC或DTC发生主TrustZone过滤器错误时，DMACDTCERRSTAT.MTERRSTAT设置为1。清除条件复位或将DMACDTCERRCLR.MTERRCLR设置为1。

有关DMAC或DTC发生的主TrustZone过滤器错误的详细信息，请参阅第15节，DMA控制器(DMAC)和第16节，数据传输控制器(DTC)

13.3.11 BUSnERRCLR：总线错误清除寄存器n（n=1到3）

Base address: BUS = 0x4000_3000

Offset address: 0x1A08 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	ILERRCLR	MMERRCLR	—	STERRCLR	SLERRCLR
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SLERRCLR	从总线错误清除 将1写入SLERRCLR位会清除BUSnERRSTAT.SLERRSTAT（n=1到3）	R/W*1
1	STERRCLR	从站TrustZone过滤器错误清除 将1写入STERRCLR位会清除BUSnERRSTAT.STERRSTAT（n=1至3）	R/W*1
2	—	该位读取为0。写入值应为0。	R/W
3	MMERRCLR	主MPU错误清除 将1写入MMERRCLR位会清除BUSnERRSTAT.MMERRSTAT（n=1到3）	R/W*1
4	ILERRCLR	非法地址访问错误清除 将1写入ILERRCLR位会清除BUSnERRSTAT.ILERRSTAT（n=1到3）	R/W*1
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.该位只能写入1。该位被读取为0。向该位写入0无效。

以下总线错误对应于主总线：

BUS1ERRCLR : Code bus

BUS2ERRCLR : System bus

BUS3ERRCLR : DMAC/DTC

When writing 1 to BUSnERRCLR (n = 1 to 3), stop the bus access that causes an error in the corresponding bus master.

13.3.12 DMACDTCERRCLR : DMAC/DTC Error Clear Register

Base address: BUS = 0x4000_3000

Offset address: 0x1A2C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MTERRCLR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MTERRCLR	Master TrustZone filter Error Clear Writing 1 to this bit clears the DMACDTCERRSTAT.MTERRSTAT flag.	R/W*1
7:1	—	This bit is read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Only 1 can be written to this bit. This bit is read as 0. Writing 0 to this bit has no effect.

When writing 1 to DMACDTCERRCLR, stop the bus access that causes an error in DMAC/DTC.

13.4 Bus Error Monitoring Section

The bus error monitoring system monitors each individual area, and when an error is detected, an error is returned to the requesting master IP using the AHB-Lite error response protocol.

13.4.1 Bus Error Types

The following types of errors can occur on each bus:

- Illegal address access
- Bus master MPU error
- TrustZone Filter error
- Bus error transmitted from each slave IP

Table 13.2 lists the address ranges where access leads to illegal address access errors. The reserved area in the slave does not trigger an illegal address access error. For more information on the bus master MPU, see section 14, Memory Protection Unit (MPU).

13.4.2 Operations When a Bus Error Occurs

When a bus error occurs, operation is not guaranteed and the error is returned to the requesting master IP.

Figure 13.3 shows operation from each error detection to user notification on the bus.

BUS1ERRCLR:代码总线

BUS2ERRCLR:系统总线

BUS3ERRCLR : DMAC/DTC

将1写入BUSnERRCLR（n=1至3）时，停止导致相应总线主机出错的总线访问。

13.3.12 DMACDTCERRCLR:DMACDTC错误清除寄存器

Base address: BUS = 0x4000_3000

Offset address: 0x1A2C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MTERRCLR
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MTERRCLR	主TrustZone过滤器错误清除 向该位写入1会清除DMACDTCERRSTAT.MTERRSTAT标志。	R/W*1
7:1	—	该位读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.该位只能写入1。该位被读取为0。向该位写入0无效。

向DMACDTCERRCLR写入1时，停止导致DMACDTC错误的总线访问。

13.4 总线错误监控部分

总线错误监控系统监控每个单独的区域，当检测到错误时，使用AHB-Lite错误响应协议将错误返回给请求的主IP。

13.4.1 总线错误类型

每条总线上都可能发生以下类型的错误：

●非法地址访问

●总线主控MPU错误

●TrustZone过滤器错误

●从每个从IP传输的总线错误

表13.2列出了访问导致非法地址访问错误的地址范围。从机中的保留区域不会触发非法地址访问错误。有关总线主控MPU的更多信息，请参阅第14节，内存保护单元(MPU)。

13.4.2 发生总线错误时的操作

当发生总线错误时，无法保证操作，错误会返回到请求的主IP。

图13.3显示了从每个错误检测到总线上的用户通知的操作。

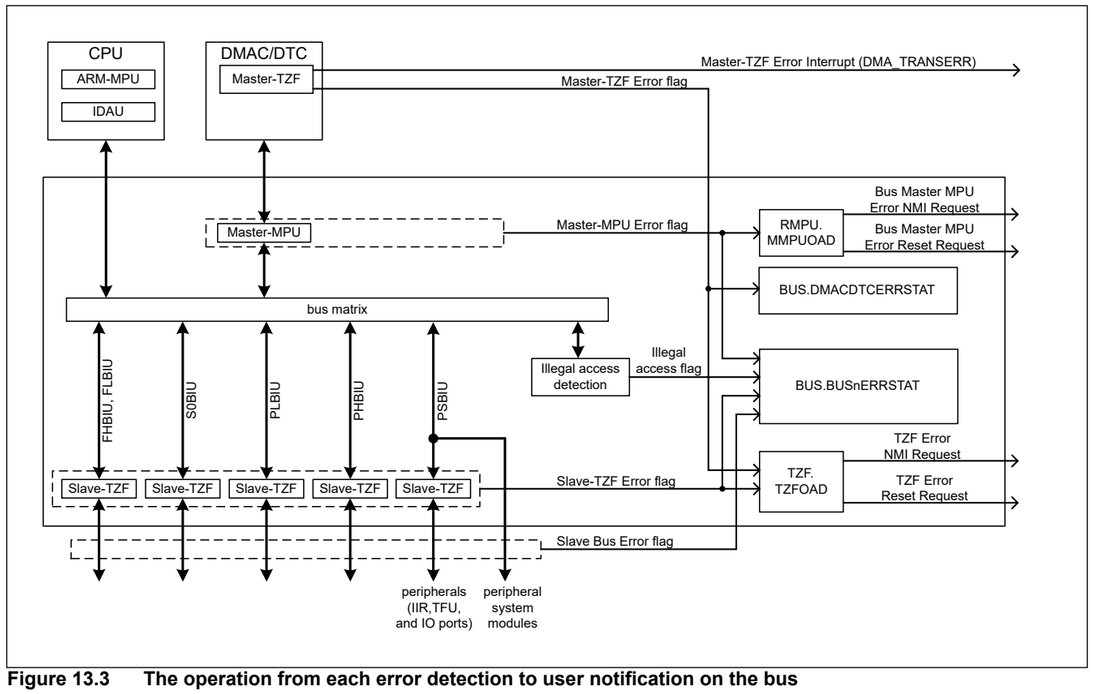


Figure 13.3 The operation from each error detection to user notification on the bus

(1) Bus Master MPU Error

The bus master of DMAC/DTC has a master MPU for access control of the set address area. The CPU does not have a master MPU because it has an Arm MPU. When a bus master MPU error is detected, an Error response is returned to the master. At the same time, perform the following steps:

1. Store the address of the error in BUSnERRADD (n = 3).
2. Store the read/write information of the error in BUSnERRRW (n = 3).
3. Set 1 to MMERRSTAT bit of BUSnERRSTAT (n = 3).

An NMI request or a reset request is generated according to the MMPUOAD.OAD setting (see section 14, Memory Protection Unit (MPU)). Since BUSnERRADD (n = 3), BUSnERRRW (n = 3), and BUSnERRSTAT (n = 3) are held until reset other than MPU- and TZF-related resets or cleared by BUSnERRCLR (n = 3), they can be verified in the NMI handler or after reset.

An NMI request is generated only on the first bus master MPU error after a reset or clearing of BUSnERRSTAT.MMERRSTAT (n = 3) bit by BUSnERRCLR (n = 3).

(2) Illegal Access Error

section 13.4.3. Conditions Leading to Illegal Address Access Errors, describes illegal access errors. When an illegal access error is detected, an Error response is returned to the master. At the same time, perform the following steps:

1. Store the address of the error in BUSnERRADD (n = 1 to 3).
2. Store the read/write information of the error in BUSnERRRW (n = 1 to 3).
3. Set 1 to ILERRSTAT bit of BUSnERRSTAT (n = 1 to 3).

NMI request and reset request are not generated. Since BUSnERRADD (n = 1 to 3), BUSnERRRW (n = 1 to 3), BUSnERRSTAT (n = 1 to 3) are held until reset other than MPU- and TZF-related resets or cleared by BUSnERRCLR (n = 1 to 3), they can be confirmed in the Bus Fault handler or the interrupt handler.

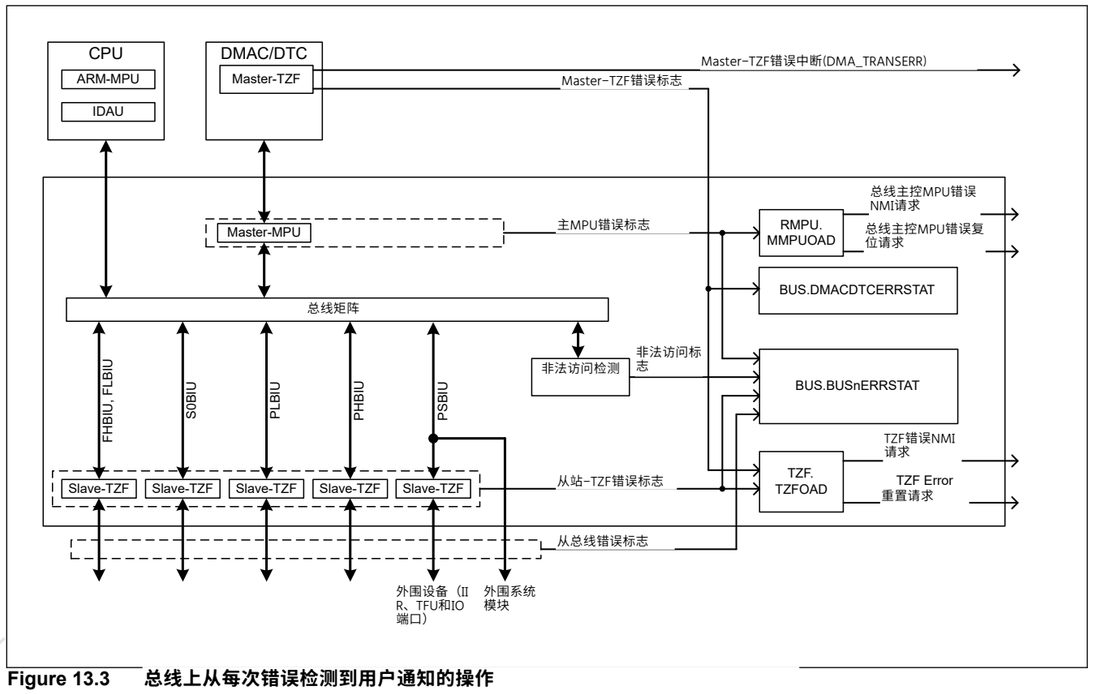


Figure 13.3 总线上从每次错误检测到用户通知的操作

(1) 总线主控MPU错误

DMACDTC的总线主控器有一个主控MPU，用于对设置的地址区域进行访问控制。CPU没有主MPU，因为它有一个ArmMPU。当检测到总线主控MPU错误时，会向主控返回错误响应。同时，执行以下步骤：

1.将错误地址存储在BUSnERRADD(n=3)中。

2.将错误的读写信息存入BUSnERRRW(n=3)。

3.将BUSnERRSTAT的MMERRSTAT位设置为1(n=3)。

根据MMPUOAD.OAD设置生成NMI请求或复位请求（参见第14节，内存保护单元（MPU））。由于BUSnERRADD(n=3)、BUSnERRRW(n=3)和BUSnERRSTAT(n=3)一直保持到除MPU和TZF相关复位之外的复位或被BUSnERRCLR(n=3)清除之前，它们可以在NMI中进行验证处理程序或重置后。

NMI请求仅在复位或清除后第一个总线主MPU错误时生成BUSnERRSTAT.MMERRSTAT(n=3)位由BUSnERRCLR(n=3)。

(2) 非法访问错误

第13.4.3节。导致非法地址访问错误的条件，描述非法访问错误。当检测到非法访问错误时，向主站返回错误响应。同时，执行以下步骤：

1.将错误地址存储在BUSnERRADD（n=1到3）中。

2.将错误的读写信息存入BUSnERRRW(n=1to3)。

3.将BUSnERRSTAT的ILERRSTAT位设置为1（n=1到3）。

不生成NMI请求和复位请求。由于BUSnERRADD（n=1到3）、BUSnERRRW（n=1到3），BUSnERRSTAT(n=1到3)一直保持到除MPU和TZF相关的复位或被BUSnERRCLR(n=1到3)清除之前，它们可以在总线故障处理程序或中断处理程序中确认。

(3) Master-TZF Error

As described in section 45, Security Features , DMAC/DTC has Master-TZF errors. When a Master-TZF error is detected, 1 is set to MTERRSTAT bit of DMACDTCERRSTAT, and because the DMAC/DTC does not perform bus access, no bus error information is stored in BTZF3ERRADD and BTZF3ERRRW.

An NMI request or reset request is generated according to the setting of TZFOAD.OAD. See section 15, DMA Controller (DMAC), section 16, Data Transfer Controller (DTC) for details on Master-TZF errors. Because DMACDTCERRSTAT is held until reset other than MPU- and TZF-related resets or cleared by DMACDTCERRCLR, they can be verified in the NMI handler or after reset.

An NMI request is generated only on the first Master-TZF error after reset or clearing of the DMACDTCERRSTAT.MTERRSTAT bit by DMACDTCERRCLR.

(4) Slave-TZF Error

As described in section 45, Security Features , FHBIU (code flash), FLBIU (data flash), S0BIU (SRAM), peripheral modules of PSBIU (IIRFA, TFU, IO ports), PHBIU and PLBIU have Slave-TZF errors. When a Slave-TZF error is detected, perform the following steps:

1. Store the address of the error in BTZFnERRADD (n = 1 to 3).
2. Store the read/write information of the error in BTZFnERRRW (n = 1 to 3).
3. Set 1 to STERRSTAT bit of BUSnERRSTAT (n = 1 to 3).

NMI request or reset request is generated according to the setting in TZFOAD.OAD. Since BTZFnERRADD (n = 1 to 3), BTZFnERRRW (n = 1 to 3), and BUSnERRSTAT (n = 1 to 3) are held until reset other than MPU- and TZF-related resets or cleared by BUSnERRCLR (n = 1 to 3), they can be verified in the NMI handler or after reset.

An NMI request is generated only on the first Slave-TZF error after a reset or clearing of the BUSnERRSTAT.STERRSTAT (n = 1 to 3) bit by BUSnERRCLR (n = 1 to 3).

(5) Slave Bus Error

Slave Bus Error occurs in the slave. When Slave Bus Error is detected, an Error response is returned to the master. At the same time, perform the following steps:

1. Store the address of the error in BUSnERRADD (n = 1 to 3)
2. Store the read/write information of the error in BUSnERRRW (n = 1 to 3)
3. Set 1 to SLERRSTAT bit of BUSnERRSTAT (n = 1 to 3).

An NMI request and reset request are not generated. Since BUSnERRADD (n = 1 to 3), BUSnERRRW (n = 1 to 3), and BUSnERRSTAT (n = 1 to 3) are held until reset other than MPU- and TZF-related resets or cleared by BUSnERRCLR (n = 1 to 3), they can be verified in the Bus Fault handler or interrupt handler.

13.4.3 Conditions Leading to Illegal Address Access Errors

Table 13.2 lists the address spaces for each bus that trigger illegal address access errors.

Table 13.2 Conditions leading to illegal address access errors (1 of 2)

Address	Slave bus	Master bus		
		CPU		DMA
		Code	System	
0x0000_0000 to 0x01FF_FFFF	FHBIU	—		—
0x0200_0000 to 0x07FF_FFFF	Reserved	E		E
0x0800_0000 to 0x0803_FFFF	FLBIU	—		—
0x0804_0000 to 0x0FFF_FFFF	Reserved	E		E
0x1000_0000 to 0x100F_FFFF	Reserved	—		E
0x1010_0000 to 0x1FFF_FFFF	Reserved	E		E

(3) Master-TZF Error

如第45节“安全功能”中所述，DMACDTC存在Master-TZF错误。当检测到Master-TZF错误时，将DMACDTCERRSTAT的MTERRSTAT位设置为1，并且由于DMACDTC不执行总线访问，因此BTZF3ERRADD和BTZF3ERRRW中不存储总线错误信息。

根据TZFOAD.OAD的设置生成NMI请求或复位请求。有关Master-TZF错误的详细信息，请参见第15节，DMA控制器(DMAC)，第16节，数据传输控制器(DTC)。因为除了MPU和TZF相关的复位或由DMACDTCERRCLR清除之外，DMACDTCERRSTAT一直保持到复位，所以可以在NMI处理程序中或在复位后对其进行验证。

NMI请求仅在复位或清除后第一个Master-TZF错误时生成DMACDTCERRCLR的DMACDTCERRSTAT.MTERRSTAT位。

(4) Slave-TZF Error

如第45节“安全特性”所述，FHBIU（代码闪存）、FLBIU（数据闪存）、S0BIU（SRAM）、PSBIU的外围模块（IIRFA、TFU、IO端口）、PHBIU和PLBIU存在Slave-TZF错误。当检测到Slave-TZF错误时，执行以下步骤：

1.将错误地址存储在BTZFnERRADD(n=1to3)中。

2.将错误的读写信息存入BTZFnERRRW(n=1to3)。

3.将BUSnERRSTAT的STERRSTAT位设置为1（n=1至3）。

根据TZFOAD.OAD中的设置生成NMI请求或复位请求。由于BTZFnERRADD(n=1到3)、BTZFnERRRW(n=1到3)和BUSnERRSTAT(n=1到3)被保持到除MPU和TZF相关的复位或被BUSnERRCLR(n=1到3)清除之前，它们可以在NMI处理程序中或在重置后进行验证。

NMI请求仅在BUSnERRCLR（n=1至3）复位或清除BUSnERRSTAT.STERRSTAT（n=1至3）位后的第一个Slave-TZF错误时生成。

(5) 从总线错误

从站总线错误发生在从站。当检测到从站总线错误时，将向主站返回错误响应。同时，执行以下步骤：

1.将错误的地址存储在BUSnERRADD(n=1to3)

2.将错误的读写信息存入BUSnERRRW(n=1to3)

3.将BUSnERRSTAT的SLERRSTAT位设置为1（n=1至3）。

不会生成NMI请求和复位请求。由于BUSnERRADD(n=1到3)、BUSnERRRW(n=1到3)和BUSnERRSTAT(n=1到3)一直保持到除MPU和TZF相关复位之外的复位或被BUSnERRCLR(n=1到3)清除之前，它们可以在总线故障处理程序或中断处理程序中进行验证。

13.4.3 导致非法地址访问错误的条件

表13.2列出了触发非法地址访问错误的每条总线的地址空间。

Table 13.2 导致非法地址访问错误的条件(1of2)

Address	从总线	主总线		
		CPU		DMA
		Code	System	
0x0000_0000 to 0x01FF_FFFF	FHBIU	—		—
0x0200_0000 to 0x07FF_FFFF	Reserved	E		E
0x0800_0000 to 0x0803_FFFF	FLBIU	—		—
0x0804_0000 to 0x0FFF_FFFF	Reserved	E		E
0x1000_0000 to 0x100F_FFFF	Reserved	—		E
0x1010_0000 to 0x1FFF_FFFF	Reserved	E		E

Table 13.2 Conditions leading to illegal address access errors (2 of 2)

Address	Slave bus	Master bus		
		CPU		DMA
		Code	System	
0x2000_0000 to 0x2800_FFFF	S0BIU		—	—
0x2801_0000 to 0x3FFF_FFFF	Reserved		E	E
0x4000_0000 to 0x4007_FFFF	PSBIU		—	—
0x4008_0000 to 0x400F_FFFF	PLBIU		—	—
0x4010_0000 to 0x4017_FFFF	PHBIU		—	—
0x4018_0000 to 0x407D_FFFF	Reserved		E	E
0x407E_0000 to 0x407F_FFFF	FLBIU		—	—
0x4080_0000 to 0x5FFF_FFFF	Reserved		E	E
0x6000_0000 to 0xDFFF_FFFF	Reserved		E	E
0xE000_0000 to 0xFFFF_FFFF	System for Cortex®-M33			E

Note: "E" : A bus error occurs.
" " : Transfer does not occur.
"—" : A bus error has not occurred. Even if there has reserved area, a bus error has not occurred.
Do not access reserved area in FLBIU and S0BIU. If accessed, a slave TZF error might occur.

13.4.4 Time-out

For some peripheral modules, a timeout error occurs with the module-stop function. When there is no response from the slave for a certain period of time, a timeout error is detected. A timeout error is returned to the requesting master IP using the AHB-Lite error response protocol.

13.5 References

1. ARM Limited, ARM v8-M Architecture Reference Manual (ARM DDI0553B.g)
2. ARM Limited, ARM Cortex-M33 Processor Technical Reference Manual Revision:r0p4 (ARM 100230_0004_00_en)
3. ARM Limited, ARM AMBA 5 AHB Protocol Specification AHB5, AHB-Lite (ARM IHI 0033B.b)
4. ARM Limited, ARM AMBA AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, ACE and ACE-Lite (ARM IHI 0022D)
5. ARM Limited, ARM AMBA APB Protocol Specification Version: 2.0 (ARM IHI 0024C)

13.6 Cache

13.6.1 Overview

There are two types of caches:
- C-cache on code bus
- S-cache on system bus.

Table 13.3 lists the specifications of the cache, Figure 13.4 shows a block diagram of the cache, and Figure 13.5 shows the cache structure in details.

Table 13.3 Cache specifications (1 of 2)

Parameter	C-cache	S-cache
Capacity	4 KB	4 KB
Way	4-way set associative	4-way set associative
Line size	32/64 bytes	32/64 bytes
Number of entry	32/16 entry/way	32/16 entry/way

Table 13.2 导致非法地址访问错误的条件(2of2)

Address	从总线	主总线		
		CPU		DMA
		Code	System	
0x2000_0000 to 0x2800_FFFF	S0BIU		—	—
0x2801_0000 to 0x3FFF_FFFF	Reserved		E	E
0x4000_0000 to 0x4007_FFFF	PSBIU		—	—
0x4008_0000 to 0x400F_FFFF	PLBIU		—	—
0x4010_0000 to 0x4017_FFFF	PHBIU		—	—
0x4018_0000 to 0x407D_FFFF	Reserved		E	E
0x407E_0000 to 0x407F_FFFF	FLBIU		—	—
0x4080_0000 to 0x5FFF_FFFF	Reserved		E	E
0x6000_0000 to 0xDFFF_FFFF	Reserved		E	E
0xE000_0000 to 0xFFFF_FFFF	Cortex®-M33系统			E

Note: "E": 发生总线错误。"": 不发生传输。"—": 未发生总线错误。即使有保留区域，也没有发生总线错误。不要访问FLBIU和S0BIU中的保留区域。如果访问，可能会发生从属TZF错误。

13.4.4 Time-out

对于某些外围模块，模块停止功能会发生超时错误。当从机在一段时间内没有响应时，检测到超时错误。使用AHB-Lite错误响应协议将超时错误返回给请求的主IP。

13.5 References

1.ARMLimited，ARMv8-M架构参考手册（ARMDDI0553B.g）
2.ARMLimited，ARMCortex-M33处理器技术参考手册修订版：r0p4(ARM100230_0004_00_en)
3.ARMLimited、ARMAMBA5AHB协议规范AHB5、AHB-Lite(ARMIHI0033B.b)
4.ARMLimited、ARMAMBAAXI和ACE协议规范AXI3、AXI4和AXI4-Lite、ACE和ACE-Lite(ARMIHI0022D)
5.ARMLimited，ARMAMBAAPB协议规范版本：2.0（ARMIHI0024C）

13.6 Cache

13.6.1 Overview

缓存有两种类型：●代码总线上的C-cache●系统总线上的S-cache。

表13.3列出了缓存的规格，图13.4显示了缓存的框图，图13.5显示了详细的缓存结构。

Table 13.3 缓存规范(1of2)

Parameter	C-cache	S-cache
Capacity	4 KB	4 KB
Way	4路组关联	4路组关联
线条尺寸	32/64 bytes	32/64 bytes
入境次数	32/16 entry/way	32/16 entry/way

Table 13.3 Cache specifications (2 of 2)

Parameter	C-cache	S-cache
Write way	No write	Write-through, non-write allocate
Replace way	4-way: Full LRU (least recently used)	4-way: Full LRU (least recently used)
Cache support area	0x0000_0000 to 0x1FFF_FFFF	0x2000_0000 – 0xDFFF_FFFF*1 except Standby SRAM area (0x2800_0000 to 0x2FFF_FFFF)

Note 1. Peripheral area 0x4000_0000 to 0x5FFF_FFFF must not have the cacheable attribution in the Arm MPU.

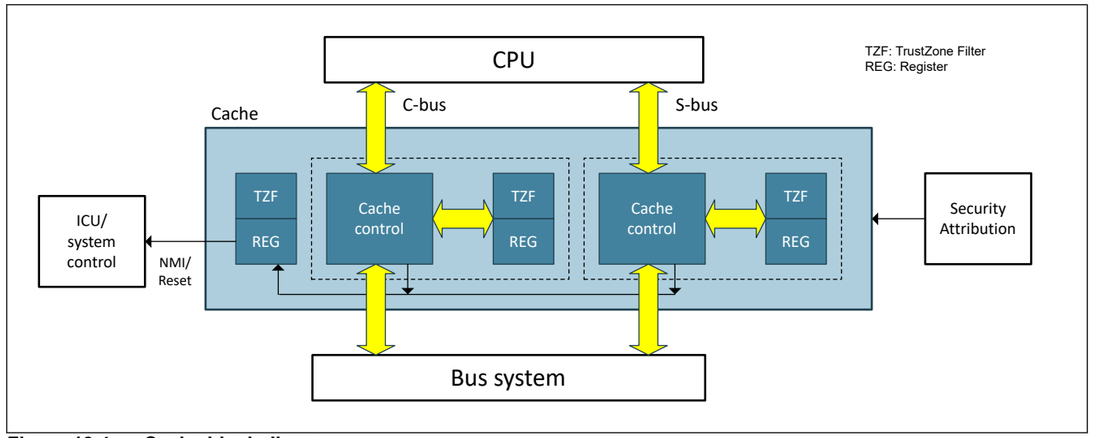


Figure 13.4 Cache block diagram

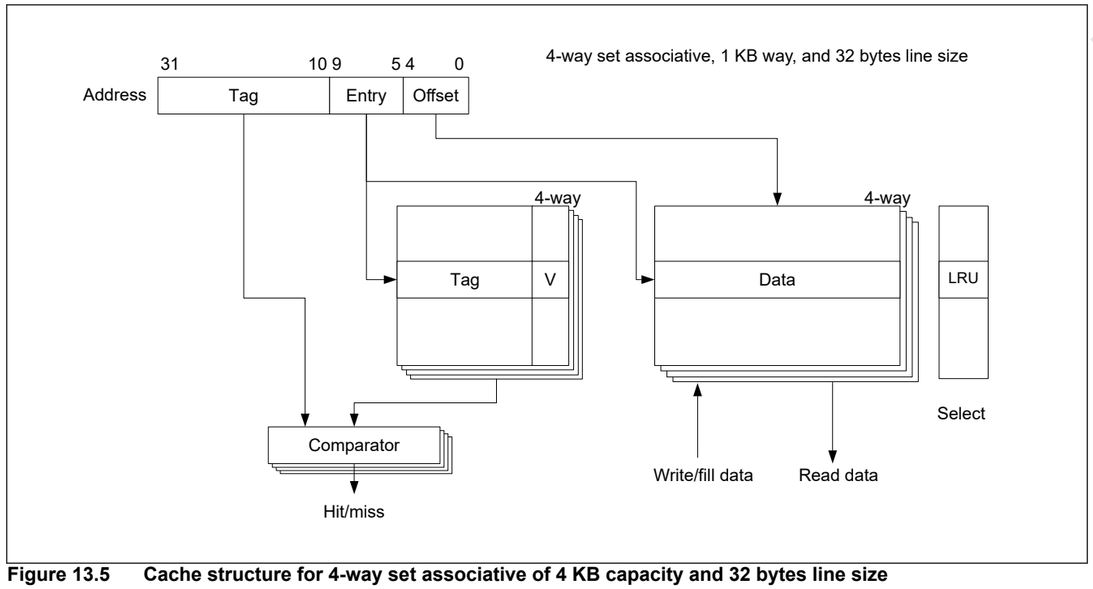


Figure 13.5 Cache structure for 4-way set associative of 4 KB capacity and 32 bytes line size

Table 13.3 缓存规范（2个中的2个）

Parameter	C-cache	S-cache
写法	不写	Write-through, non-write allocate
更换方式	4路：全LRU（最近最少使用）	4路：全LRU（最近最少使用）
缓存支持区	0x0000_0000 to 0x1FFF_FFFF	0x2000_0000 0xDFFF_FFFF*1备用SRAM区域除外（0x2800_0000至0x2FFF_FFFF）

注1.外设区域0x4000_0000到0x5FFF_FFFF在ArmMPU中不得具有可缓存属性。

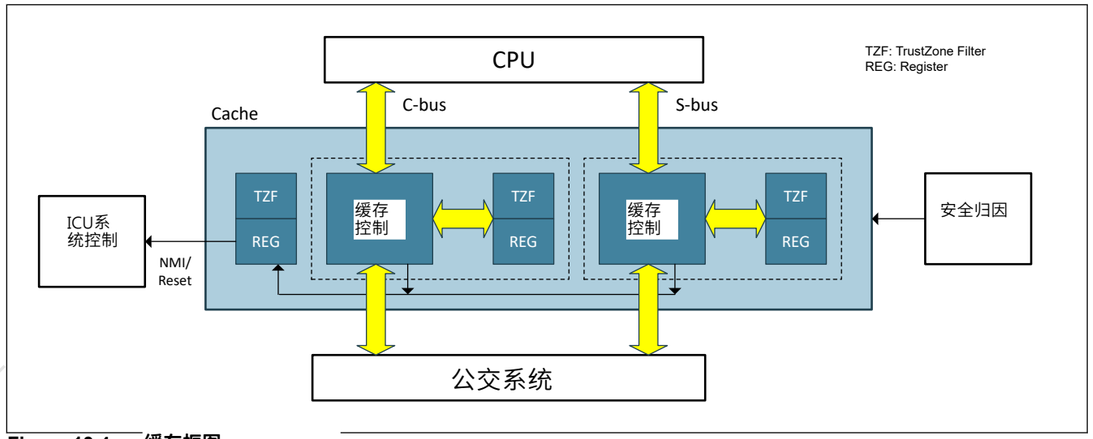


Figure 13.4 缓存框图

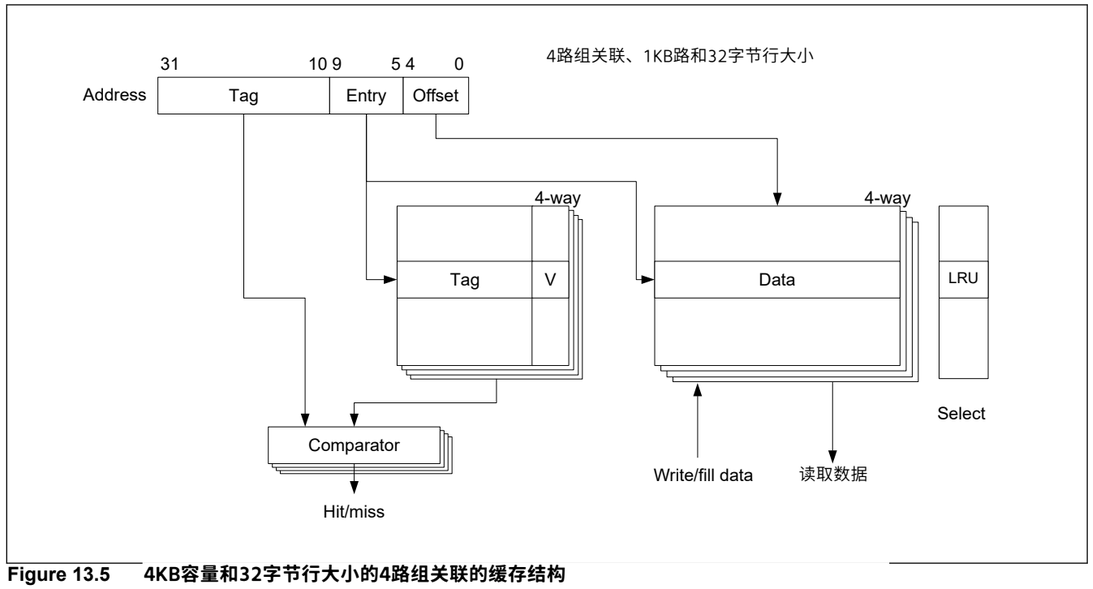


Figure 13.5 4KB容量和32字节行大小的4路组关联的缓存结构

13.6.2 Register Description

13.6.2.1 CSAR : Cache Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	CACHEESA	CACHELSA	CACHESA
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	CACHESA	Security Attributes of Registers for Cache Control 0: Secure 1: Non-secure	R/W
1	CACHELSA	Security Attributes of Registers for Cache Line Configuration 0: Secure 1: Non-secure	R/W
2	CACHEESA	Security Attributes of Registers for Cache Error 0: Secure 1: Non-secure	R/W
31:3	—	These bits are read as 1.	R

Note: This register is write-protected by PRCR register.

Note: When CACHESA = 0 (secure), cache maintenance operation cannot be performed after updated the program. Therefore, when debugging, software breakpoints cannot be used for the cache target area.

CACHESA bit (Security Attributes of Registers for Cache Control)

The CACHESA bit indicates the security attributes of registers for cache control. The target registers are:

- CCACTL
- CCAFCT
- SCACTL
- SCAFCT.

CACHELSA bit (Security Attributes of Registers for Cache Line Configuration)

The CACHELSA bit indicates the security attributes of registers for cache line configuration. The target registers are:

- CCALCF
- SCALCF.

CACHEESA bit (Security Attributes of Registers for Cache Error)

The CACHEESA bit indicates the security attributes of registers for cache error.

- CAPOAD
- CAPRCR.

13.6.2 注册说明

13.6.2.1 CSAR:缓存安全属性寄存器

Base address: CPSCU = 0x4000_8000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	CACHEESA	CACHELSA	CACHESA
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	CACHESA	缓存控制寄存器的安全属性 0: Secure 1: Non-secure	R/W
1	CACHELSA	缓存行配置寄存器的安全属性 0: Secure 1: Non-secure	R/W
2	CACHEESA	缓存错误寄存器的安全属性 0: Secure 1: Non-secure	R/W
31:3	—	这些位读为1。	R

Note: 该寄存器由PRCR寄存器写保护。

Note: CACHESA=0（安全）时，更新程序后无法进行缓存维护操作。因此，在调试时，软件断点不能用于缓存目标区域。

CACHESA位（缓存控制寄存器的安全属性）

CACHESA位指示用于缓存控制的寄存器的安全属性。目标寄存器是：●CCACTL●CCAFCT●SCACTL●SCAFCT。

CACHELSA位（缓存线配置寄存器的安全属性）

CACHELSA位指示用于高速缓存行配置的寄存器的安全属性。目标寄存器是：●CCALCF●SCALCF。

CACHEESA位（缓存错误寄存器的安全属性）

CACHEESA位指示缓存错误寄存器的安全属性。●CAPOAD●CAPRCR。

13.6.2.2 CCACTL : C-Cache Control Register

Base address: CACHE = 0x4000_7000

Offset address: 0x000

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ENC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENC	C-Cache Enable Set the C-cache enable: 0: Disable C-cache 1: Enable C-cache	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

ENC bit (C-Cache Enable)

The ENC bit controls the cache enable of C-cache. When the ENC bit changes from 0 to 1, the Valid bit of C-cache is cleared.

13.6.2.3 CCAFCT : C-Cache Flush Control Register

Base address: CACHE = 0x4000_7000

Offset address: 0x004

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FC	C-Cache Flush Set the C-cache line flush: 0: No action 1: C-cache line flush (all lines invalidated)	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

FC bit (C-Cache Flush)

The FC bit controls the cache flush of C-cache.

[Setting condition]

- When writing 1 to this bit.
- When setting CCACTL.ENC bit from "0" to "1".

[Clearing condition]

- This bit is cleared automatically when cache flush is performed.

13.6.2.2 CCACTL:C-Cache控制寄存器

Base address: CACHE = 0x4000_7000

Offset address: 0x000

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ENC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENC	C-Cache Enable 设置C缓存启用： 0：禁用C-cache1 ：启用C-cache	R/W
31:1	—	这些位被读取为0。写入值应为0。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ENC bit (C-Cache Enable)

ENC位控制C-cache的缓存使能。当ENC位从0变为1时，C-cache的Valid位被清除。

13.6.2.3 CCAFCT:C-Cache刷新控制寄存器

Base address: CACHE = 0x4000_7000

Offset address: 0x004

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FC	C-Cache Flush 设置C-cache行刷新： 0：无操作1：C-cache行刷新（所有行无效）	R/W
31:1	—	这些位被读取为0。写入值应为0。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

FC bit (C-Cache Flush)

FC位控制C-cache的缓存刷新。

[Setting condition]

●向该位写入1时。

●将CCACTL.ENC位从“0”设置为“1”时。

[Clearing condition]

●执行缓存刷新时，该位自动清零。

13.6.2.4 CCALCF : C-Cache Line Configuration Register

Base address: CACHE = 0x4000_7000

Offset address: 0x008

Bit position:	31																													1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	CC[1:0]	C-Cache Line Size Set the C-cache line size: 0 0: Prohibited 0 1: Cache line size 32 bytes 1 0: Cache line size 64 bytes 1 1: Prohibited	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

CC[1:0] bits (C-Cache Line Size)

The CC[1:0] bits control the cache line size of C-cache. This bit can be written when the CCACTL.ENC bit is 0. Otherwise, this bit cannot be written.

13.6.2.5 SCACTL : S-Cache Control Register

Base address: CACHE = 0x4000_7000

Offset address: 0x040

Bit position:	31																														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ENS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENS	S-Cache Enable Set the S-cache enable: 0: Disable S-cache 1: Enable S-cache	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

ENS bit (S-Cache Enable)

The ENS bit controls the cache enable of S-cache. When the ENS bit changes from 0 to 1, the Valid bit of S-cache is cleared.

13.6.2.4 CCALCF:C-Cache行配置寄存器

Base address: CACHE = 0x4000_7000

Offset address: 0x008

Bit position:	31																													1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	CC[1:0]	C-Cache行大小 设置C-cache行大小： 00：禁止01：缓存线大小32字节10：缓存线大小64字节1 1：禁止	R/W
31:2	—	这些位被读取为0。写入值应为0。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

CC[1:0]位（C-CacheLineSize）

CC[1:0]位控制C-cache的高速缓存行大小。当CCACTL.ENC位为0时可以写入该位。否则，无法写入该位。

13.6.2.5 SCACTL:S-Cache控制寄存器

Base address: CACHE = 0x4000_7000

Offset address: 0x040

Bit position:	31																														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ENS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENS	S-Cache Enable 设置S-cache启用： 0：禁用S-cache1 ：启用S-cache	R/W
31:1	—	这些位被读取为0。写入值应为0。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ENS位（S-Cache启用）

ENS位控制S-cache的缓存使能。当ENS位从0变为1时，S-cache的Valid位被清除。

13.6.2.6 SCAFCT : S-Cache Flush Control Register

Base address: CACHE = 0x4000_7000

Offset address: 0x044

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FS	S-Cache Flush Set the S-cache line flush: 0: No action 1: S-cache line flush (all lines invalidated)	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

FS bit (S-Cache Flush)

The FS bit controls the cache flush of S-cache.

[Setting condition]

When writing 1 to this bit.

When setting SCACTL.ENS bit from "0" to "1".

[Clearing condition]

This bit is cleared automatically when cache flush is performed.

13.6.2.7 SCALCF : S-Cache Line Configuration Register

Base address: CACHE = 0x4000_7000

Offset address: 0x048

Bit position:	31																												1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	CS[1:0]	S-Cache Line Size Set the S-cache line size: 0 0: Prohibited 0 1: Cache line size 32 bytes 1 0: Cache line size 64 bytes 1 1: Prohibited	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

13.6.2.6 SCAFCT:S-Cache刷新控制寄存器

Base address: CACHE = 0x4000_7000

Offset address: 0x044

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FS	S-Cache Flush 设置S-cache行刷新： 0：无操作1：S-cache行刷新（所有行无效）	R/W
31:1	—	这些位被读取为0。写入值应为0。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

FS bit (S-Cache Flush)

FS位控制S-cache的缓存刷新。

[Setting condition]

向该位写入1时。

将SCACTL.ENS位从"0"设置为"1"时。

[Clearing condition]

执行缓存刷新时，该位会自动清除。

13.6.2.7 SCALCF:S-Cache行配置寄存器

Base address: CACHE = 0x4000_7000

Offset address: 0x048

Bit position:	31																												1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	CS[1:0]	S-Cache行大小 设置S-cache行大小： 00：禁止01：缓存线大小32字节10：缓存线大小64字节1 1：禁止	R/W
31:2	—	这些位被读取为0。写入值应为0。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

CS[1:0] bits (S-Cache Line Size)

The CS[1:0] bits control the cache line size of S-cache. This bit can be written when the SCACTL.ENS bit is 0. Otherwise, this bit cannot be written.

[Setting condition]

This bit can be written when the CACTL.ENS bit is 0. Otherwise, this bit cannot be written.

13.6.2.8 CAPOAD : Cache Parity Error Operation After Detection Register

Base address: CACHE = 0x4000_7000

Offset address: 0x200

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation after Detection Select the operation after detection: 0: Non-maskable interrupt 1: Reset	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

OAD bit (Operation after Detection)

The OAD bit generates either a reset or a non-maskable interrupt when parity error is detected.

The protection register (CAPRCR) protects this register against writes. Modify the valid bit in the protection register (CAPRCR) to enable before writing to this bit. Do not write to CAPOAD while access to cache is in progress.

13.6.2.9 CAPRCR : Cache Protection Register

Base address: CACHE = 0x4000_7000

Offset address: 0x204

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	KW[6:0]							PRCR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PRCR	Register Write Control Set the register write control: 0: Disable writes to protected registers 1: Enable writes to protected registers	R/W
7:1	KW[6:0]	Write key code These bits enable or disable writes to the PRCR bit.	R/W

CS[1:0]位（S-Cache行大小）

CS[1:0]位控制S-cache的缓存线大小。当SCACTL.ENS位为0时可以写入该位。否则，无法写入该位。

[Setting condition]

当CACTL.ENS位为0时可以写入该位。否则，无法写入该位。

13.6.2.8 CAPOAD：检测寄存器后缓存奇偶校验错误操作

Base address: CACHE = 0x4000_7000

Offset address: 0x200

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	OAD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	检测后的操作 检测后选择操作： 0：不可屏蔽中断1：复位	R/W
31:1	—	这些位被读取为0。写入值应为0。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

OAD位（检测后的操作）

当检测到奇偶校验错误时，OAD位会产生复位或不可屏蔽中断。

保护寄存器(CAPRCR)保护该寄存器不被写入。在写入该位之前修改保护寄存器(CAPRCR)中的有效位以使能。在访问缓存的过程中不要写入CAPOAD。

13.6.2.9 CAPRCR:缓存保护寄存器

Base address: CACHE = 0x4000_7000

Offset address: 0x204

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	KW[6:0]							PRCR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PRCR	寄存器写控制 设置寄存器写控制： 0：禁止写入受保护寄存器1：允许写入受保护寄存器	R/W
7:1	KW[6:0]	编写关键代码 这些位启用或禁用对PRCR位的写入。	R/W

Bit	Symbol	Function	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

PRCR bit (Register Write Control)

The PRCR bit controls the write mode of the CAPOAD register. When this bit is set to 1, writing to the CAPOAD register is enabled. When writing to this bit, write 0x78 to the KW[6:0] bits simultaneously.

KW[6:0] bits (Write key code)

The KW[6:0] bits enable or disable writes to the PRCR bit. When writing to the PRCR bit, write 0x78 to the KW[6:0] bits simultaneously. When a value other than 0x78 is written to KW[6:0] bits, the PRCR bit is not updated. The KW[6:0] bits are always read as 0x00.

13.6.3 Operation

13.6.3.1 S-Cache

Figure 13.6 shows the access flow from CPU to S-cache.

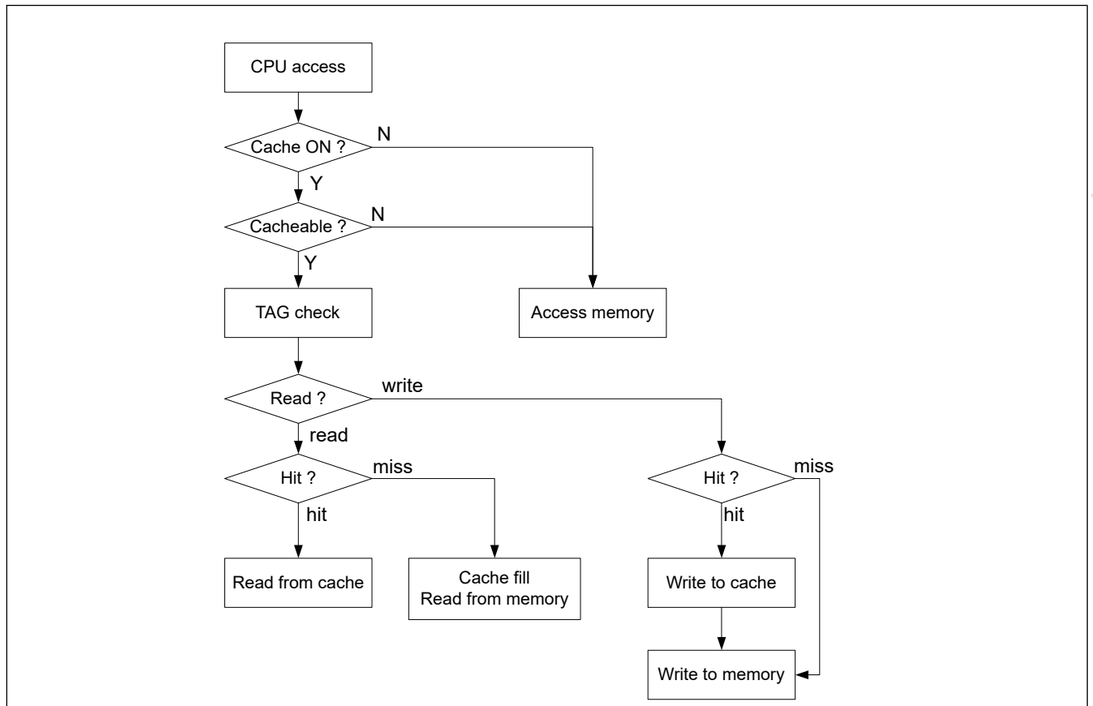


Figure 13.6 Access flow from CPU to S-cache

The cache function works when cache is enabled (CACTL.ENS = 1) and cacheable access is from CPU. The cache checks the address of CPU access request and request in cache tag, then determines whether the CPU access is a hit or a miss-hit.

Bit	Symbol	Function	R/W
31:8	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

PRCR位（寄存器写控制）

PRCR位控制CAPOAD寄存器的写模式。当该位设置为1时，允许写入CAPOAD寄存器。写入该位时，同时将0x78写入KW[6:0]位。

KW[6:0]位（写键码）

KW[6:0]位启用或禁用对PRCR位的写入。写入PRCR位时，同时将0x78写入KW[6:0]位。当将0x78以外的值写入KW[6:0]位时，PRCR位不会更新。KW[6:0]位总是被读取为0x00。

13.6.3 Operation

13.6.3.1 S-Cache

图13.6显示了从CPU到S-cache的访问流程。

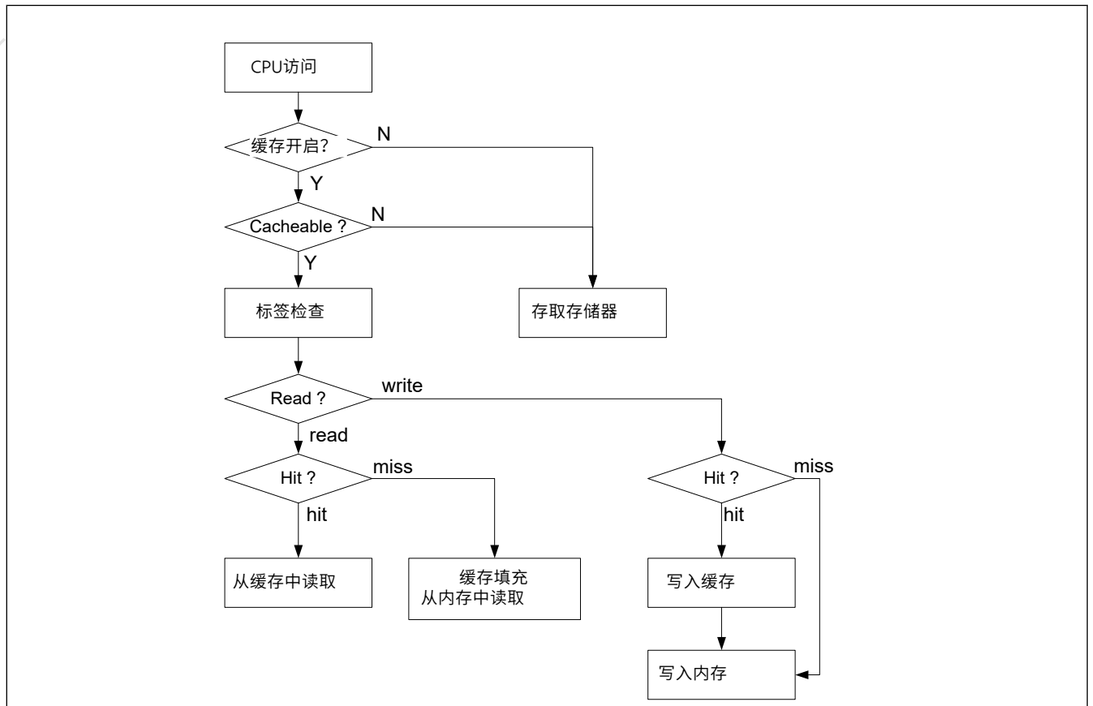


Figure 13.6 从CPU到S-cache的访问流程

缓存功能在启用缓存(CACTL.ENS=1)且可缓存访问来自CPU时起作用。缓存检查CPU访问请求的地址和缓存标签中的请求，然后确定CPU访问是命中还是未命中。

Read miss

The cache reads one cache line data from memory and stores it into the cache data. The cache then returns the required data to CPU.

Read hit

The cache reads required data from the cache data and returns it to CPU. Access cycle then determines it is a hit because of the 0 wait cycle.

Write miss

The cache processes only a write cycle to memory. No affect to cache data.

Write hit

The cache processes both a write cycle to cache data and a write cycle to memory.

13.6.3.2 C-Cache

Figure 13.7 shows the access flow from CPU to C-cache.

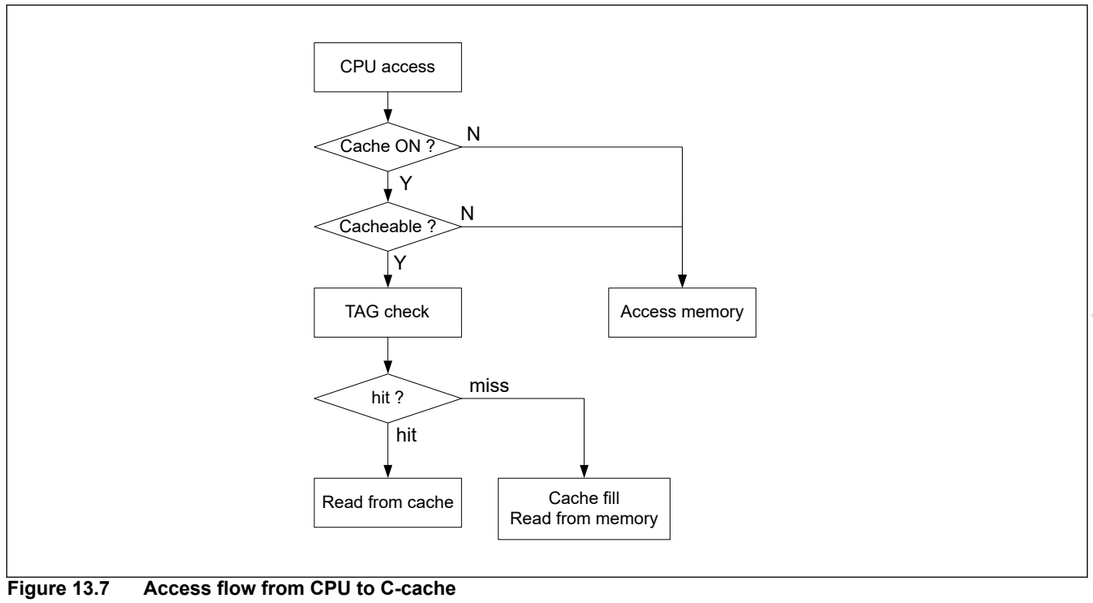


Figure 13.7 Access flow from CPU to C-cache

The cache function works when cache is enabled (CACTL.ENC = 1) and cacheable access is from CPU. The cache checks the address of CPU access request and request in cache tag, then determines whether the CPU access is a hit or a miss-hit.

Read miss

The cache reads one cache line data from memory and stores it into the cache data. The cache then returns the required data to CPU.

Read hit

The cache reads required data from the cache data and returns it to CPU. Access cycle then determines it is a hit because of the 0 wait cycle.

Because C-cache does not function in the ROM area of C-cache, therefore it operates in read-only access.

13.6.3.3 Cache Flush

The Valid bit is cleared with the CAFCT register. However, tag and cache data are not affected by the CAFCT register.

读未读

高速缓存从内存中读取一个高速缓存行数据并将其存储到高速缓存数据中。然后缓存将所需的数据返回给CPU。

阅读命中

缓存从缓存数据中读取需要的数据并返回给CPU。然后访问周期确定它是命中，因为等待周期为0。

写小姐

高速缓存仅处理对内存的写周期。不影响缓存数据。

写命中

高速缓存处理缓存数据的写周期和存储器的写周期。

13.6.3.2 C-Cache

图13.7显示了从CPU到C-cache的访问流程。

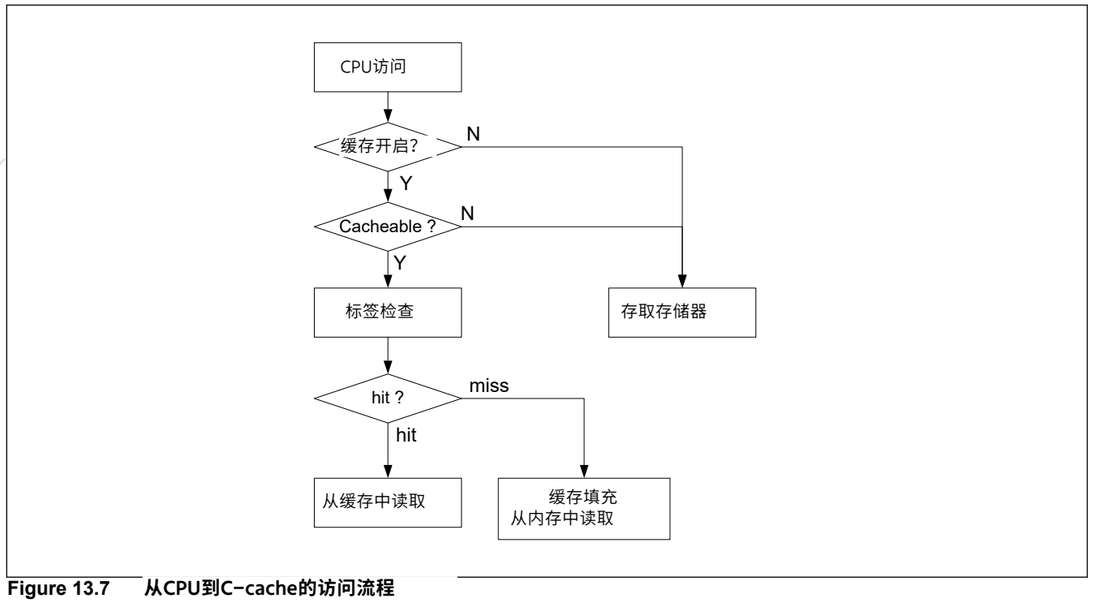


Figure 13.7 从CPU到C-cache的访问流程

缓存功能在启用缓存(CACTL.ENC=1)且可缓存访问来自CPU时起作用。缓存检查CPU访问请求的地址和缓存标签中的请求，然后确定CPU访问是命中还是未命中。

读未读

高速缓存从内存中读取一个高速缓存行数据并将其存储到高速缓存数据中。然后缓存将所需的数据返回给CPU。

阅读命中

缓存从缓存数据中读取需要的数据并返回给CPU。然后访问周期确定它是命中，因为等待周期为0。

由于C-cache在C-cache的ROM区域中不起作用，因此它以只读访问方式运行。

13.6.3.3 缓存刷新

有效位通过CAFCT寄存器清零。但是，标签和缓存数据不受 CAFCT寄存器的影响。

The valid bit is also cleared when CACTL is set from 0 to 1.

Note: After changing the cacheable attribute by the Arm MPU, clear the valid bit using the CAFCT register.

13.6.3.4 LRU and Replace

The cache uses LRU (Least Recently Used) mechanism as the cache replacement algorithm. If a CPU access is determined as a hit or a miss-hit, the cache replaces cache data that is not the last restored. Additionally, the cache is tagged as the latest data in LRU of the cache data. Therefore even when the cache line in cache ways are full, the cache can replace cache data using LRU which shows older data.

The algorithm for a 4-way Full-LRU shows the order each way, for example way 0 to way 3.

13.6.3.5 Parity Check

The cache has a parity check function for cache RAM that is stored as cache fill data. The cache has 4-bit parities for 32-bit data, that is when data is read, a parity bit is added to every 8-bit data of 32-bit data width. When the cache reads data with a hit status, it checks for parity errors. When a parity error occurs, a parity error notification is generated.

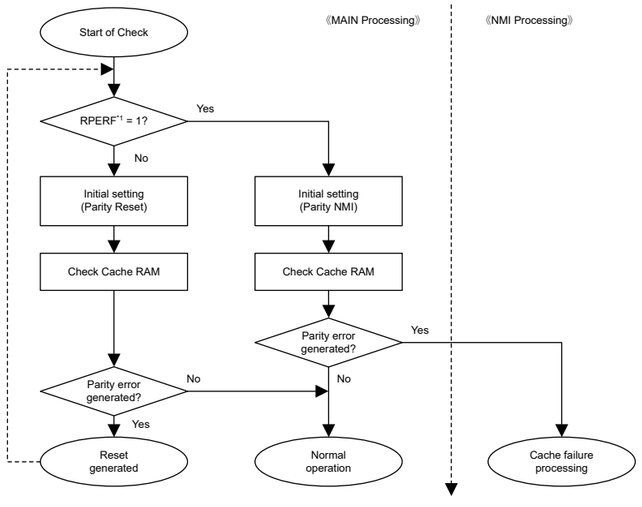
The cache reads 32-bit data even when the CPU requests a byte read or half-word read.

Note: A parity error might occur even though it is caused by a non validated-data byte of which the CPU does not request.

Parity error notification can be specified as a non-maskable interrupt or a reset request in the CAPOAD register. However, if the debug mode requests to suppress the parity error notification, then notification is not generated.

When a parity error occurs, the cache does not perform a cache flush and does not respond to the CPU with a bus error.

Parity errors often occur due to noise. To confirm whether the cause of the parity error is noise or corruption, see the flows for cache parity check in Figure 13.8 and Figure 13.9.



Note 1. RPERF: Cache Parity Error Reset Detect Flag (RSTSR1.RPERF)

Figure 13.8 Flow of cache parity check when parity reset is enabled

当CACTL从0设置为1时，有效位也会被清除。

Note: 通过ArmMPU更改可缓存属性后，使用CAFCT寄存器清除有效位。

13.6.3.4 LRU和替换

缓存使用LRU（最近最少使用）机制作为缓存替换算法。如果CPU访问被确定为命中或未命中，则缓存替换不是最后恢复的缓存数据。另外，缓存被标记为缓存数据的LRU中的最新数据。因此，即使缓存路中的缓存行已满，缓存也可以使用显示较旧数据的LRU替换缓存数据。

4路Full-LRU的算法显示了每种路的顺序，例如路0到路3。

13.6.3.5 奇偶校验

高速缓存具有用于存储为高速缓存填充数据的高速缓存RAM的奇偶校验功能。高速缓存对于32位数据有4位奇偶校验，即在读取数据时，每32位数据宽度的8位数据添加一个奇偶校验位。当缓存读取具有命中状态的数据时，它会检查奇偶校验错误。当发生奇偶校验错误时，会生成奇偶校验错误通知。

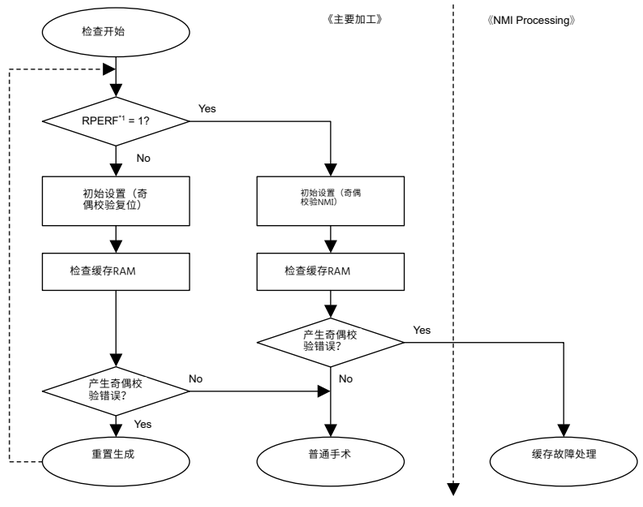
即使CPU请求字节读取或半字读取，缓存也会读取32位数据。

Note: 即使奇偶校验错误是由CPU未请求的未经验证的数据字节引起的，也可能发生奇偶校验错误。

奇偶校验错误通知可以指定为不可屏蔽中断或CAPOAD寄存器中的复位请求。但是，如果调试模式请求抑制奇偶校验错误通知，则不会生成通知。

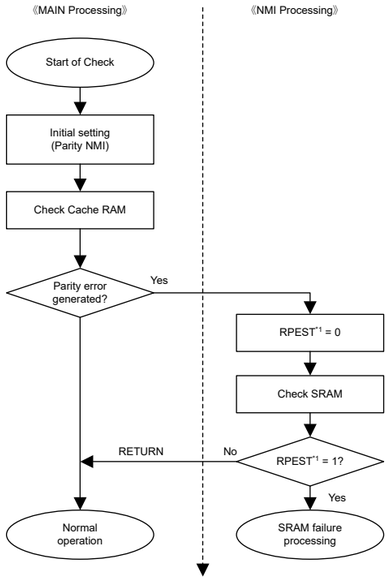
当发生奇偶校验错误时，缓存不会执行缓存刷新，也不会以总线错误响应CPU。

奇偶校验错误经常由于噪声而发生。要确认奇偶校验错误的原因是噪声还是损坏，请参见图13.8和图13.9中的缓存奇偶校验流程。



注1.RPERF：高速缓存奇偶校验错误复位检测标志(RSTSR1.RPERF)

Figure 13.8 启用奇偶校验时的缓存奇偶校验流程



Note 1. RPEST: Cache Parity Error Interrupt Detect Flag (NMISR.RPEST)

Figure 13.9 Flow of cache parity check when parity interrupt is enabled

13.6.3.5.1 Cache RAM Check

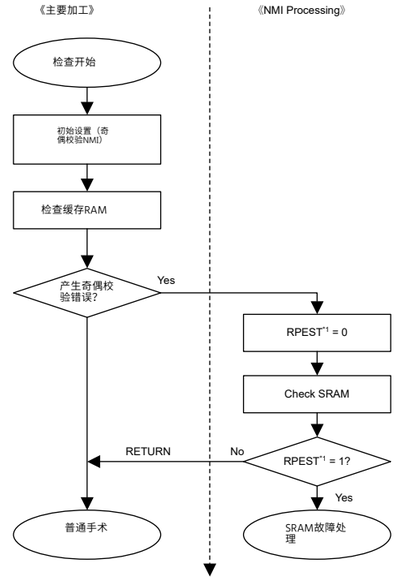
Parity error of cache RAM occurs at a read access by CPU with a cache status of read-hit. With a read-hit status, some conditions are required before performing a cache RAM check. For S-cache check, execute the check program in flash memory. For C-cache check, execute the check program in SRAM.

(1) Cache RAM check flow

1. Flush all valid bits in cache to clear the cache enable bit.
2. Reserve a 4-KB work memory such as SRAM for S-cache. Because each cache in the MCU is a 4-way set associative with 1 KB RAM per way, a total of 4 KB is required for S-cache. The target address should not be used as reserved area.
3. Set the cache enable to 1.
4. Read data from the target word address of 4 KB using the CPU. The status of cache should be a read-miss with the result stored as cache fill data.
5. Read data in another cache way whose address is calculated by adding the address in step 4. with 1 KB address. The status of cache should be a read-miss with the result stored as cache fill data in another way.
6. Read data in another cache way whose address is calculated by adding the address in step 5. with 1 KB address. The status of cache should be a read-miss with the result stored as cache fill data in another way.
7. Read data in another cache way whose address is calculated by adding the address in step 6. with 1 KB address. The status of cache should be a read-miss with the result stored as cache fill data in another way. Cache RAM check for a write/read-hit status is now complete.
8. Write test data to the target word address in steps 4., 5., 6., and 7.. The status of cache in steps 4., 5., 6., and 7. should be a write-hit with the results written to the cache RAM.
9. Read from the target word address in steps 4., 5., 6., and 7. again. The status of cache in steps 4., 5., 6., and 7. should be a read-hit. Parity check for a word data is now complete.
10. Go to step 1. to continue parity check for different target addresses.

13.6.3.6 Bus Error

The association from a bus slave to a bus error is described in the sections that follow.



注1.RPEST：高速缓存奇偶校验错误中断检测标志(NMISR.RPEST)

Figure 13.9 启用奇偶校验中断时的缓存奇偶校验流程

13.6.3.5.1 缓存RAM检查

高速缓存RAM的奇偶校验错误发生在CPU读取访问时，高速缓存状态为read-hit。对于读取命中状态，在执行高速缓存RAM检查之前需要一些条件。对于S-cache检查，执行闪存中的检查程序。对于C-cache检查，执行SRAM中的检查程序。

(1) 缓存RAM检查流程

1.刷新缓存中的所有有效位以清除缓存启用位。2.为S-cache预留一个4KB的工作存储器，例如SRAM。因为MCU中的每个缓存都是4-waysetassociative

每路1KBRAM，S-cache总共需要4KB。目标地址不应用作保留区。3.将缓存使能设置为1。4.使用CPU从4KB的目标字地址读取数据。缓存的状态应该是读未命中，结果存储为缓存填充数据。5.以另一种缓存方式读取数据，其地址是通过将步骤4中的地址与1KB地址相加计算出来的。缓存的状态应该是读未命中，结果以另一种方式存储为缓存填充数据。6.以另一种缓存方式读取数据，其地址是通过将步骤5中的地址与1KB地址相加计算得出的。缓存的状态应该是读未命中，结果以另一种方式存储为缓存填充数据。7.以另一种缓存方式读取数据，其地址是通过将步骤6中的地址与1KB地址相加计算出来的。缓存的状态应该是读未命中，结果以另一种方式存储为缓存填充数据。写读命中状态的高速缓存RAM检查现已完成。8.在步骤4.、5.、6.和7.中将测试数据写入目标字地址。步骤4.、5.、6.和7.中的缓存状态应该是write-hitwith将结果写入缓存RAM。9.再次从步骤4.、5.、6.和7.中的目标字地址读取。步骤4.、5.、6.和7.中的缓存状态应该是读取命中。单词数据的奇偶校验现已完成。10.转到步骤1.继续对不同的目标地址进行奇偶校验。

13.6.3.6 总线错误

从总线从站到总线错误的关联将在后面的部分中描述。

In cache off

The cache returns a bus error to the CPU.

For non-cacheable access

The cache returns a bus error to the CPU.

During read accesses for cache fill

For the first data that corresponds to a CPU access request, the cache returns a bus error to the CPU. For other read data while filling the cache line, the cache cannot return a bus error to the CPU except for read data with early forwarding. The cache enable bit clears the cache line if the cache accepts a bus error response from the slave.

For write-hit status

The cache cannot return a bus error to the CPU because the cache enable bit does not clear the cache line.

For write-miss status

The cache cannot return a bus error to the CPU.

13.6.3.7 Early Forwarding Function

While filling data in the cache, if the address of the CPU read request and the address of the cache fill request are the same, the cache returns the data to CPU. Table 13.4 shows an example.

Table 13.4 Example of early forwarding

Operation	Access sequence								
Address of CPU read request	0x04	0x08	0x0C	0x14	→	0x10	→	→	→
Address of cache fill	0x04	0x08	0x0C	0x10	0x14	0x18	0x1C	0x00	—
CPU access status	Read (0x04)	Read (0x08)	Read (0x0C)	—	Read (0x14)	—	—	—	Read (0x10)

When the CPU requests read accesses and the addresses are 0x04, 0x08, 0x0C, 0x14 and 0x10 sequentially, the first read access to address 0x04 is of a miss-hit status and the cache starts to fill data into cache. The early forwarding function allows a return of read data to CPU when accesses are to addresses 0x08, 0x0C and 0x14 while the cache is filling the cache line. On the other hand, access to address 0x10 must wait for the completion of filling the cache line. The cache then returns data for address 0x10 when it finished filling the cache line.

13.6.4 Usage Notes

13.6.4.1 Cache Line Configuration Register

Writes to the Cache Line Configuration Register are allowed when the status is cache off (CACTL.ENS = 0 for S-cache, CACTL.ENC = 0 for C-cache).

13.6.4.2 Coherency

The coherency between the cache and the internal SRAM must be guaranteed by software.

When allocating shared memory between the CPU and a bus master such as DMAC in the cache support area, invalidate the cache data as necessary.

在缓存关闭

高速缓存将总线错误返回给CPU。

对于不可缓存的访问

高速缓存将总线错误返回给CPU。

在缓存填充的读取访问期间

对于与CPU访问请求对应的第一个数据，缓存将总线错误返回给CPU。对于填充缓存行的其他读取数据，缓存不能向CPU返回总线错误，除了提前转发的读取数据。如果缓存接受来自从设备的总线错误响应，缓存使能位清除缓存行。

对于写命中状态

高速缓存无法向CPU返回总线错误，因为高速缓存启用位不会清除高速缓存行。

对于写未命中状态

高速缓存不能将总线错误返回给CPU。

13.6.3.7 提前转发功能

在缓存中填充数据时，如果CPU读取请求的地址和缓存填充请求的地址相同，则缓存将数据返回给CPU。表13.4显示了一个示例。

Table 13.4 提前转发示例

Operation	访问顺序								
CPU读请求地址	0x04	0x08	0x0C	0x14	→	0x10	→	→	→
缓存填充地址	0x04	0x08	0x0C	0x10	0x14	0x18	0x1C	0x00	—
CPU访问状态	Read (0x04)	Read (0x08)	Read (0x0C)	—	Read (0x14)	—	—	—	Read (0x10)

当CPU请求读访问，地址依次为0x04、0x08、0x0C、0x14和0x10时，对地址0x04的第一次读访问为未命中状态，缓存开始将数据填充到缓存中。早期转发功能允许在高速缓存填充高速缓存行时访问地址0x08、0x0C和0x14时将读取数据返回到CPU。另一方面，对地址0x10的访问必须等待缓存行的填充完成。然后，缓存在完成填充缓存行后返回地址0x10的数据。

13.6.4 使用说明

13.6.4.1 高速缓存行配置寄存器

当状态为高速缓存关闭时，允许写入高速缓存行配置寄存器（对于S-cache，CACTL.ENS=0，CACTL.ENC = 0 for C-cache).

13.6.4.2 Coherency

高速缓存和内部SRAM之间的一致性必须由软件来保证。

在高速缓存支持区域中，在CPU和DMAC等总线主控器之间分配共享内存时，根据需要使高速缓存数据无效。

14. Memory Protection Unit (MPU)

14.1 Overview

The MCU has one Memory Protection Unit (MPU).

Table 14.1 lists the MPU specifications, and Table 14.2 shows the behavior on detection of each MPU error.

Table 14.1 MPU specifications

Classification	Module/Function	Specifications
Illegal memory access	Arm® Cortex®-M33 CPU	• Arm CPU has a default memory map. If the CPU makes an illegal access, an exception interrupt occurs • The MPU can change a default memory map.
Memory protection	Arm MPU	Memory protection function for the CPU: • (8+8) region MPU with sub regions and background region for secure and non-secure.
	Bus master MPU	Memory protection function for each bus master except for the CPU: • DMAC/DTC: 8 regions

Table 14.2 Behavior on MPU error detection

MPU type	Notification type	Error Response by HRESP signal of AHB I/F	Bus Access on error detection	Storing of error access information
Arm MPU	• Hard fault	Not supported	• Does not correctly write access • Does not correctly read access	Stored in the Cortex-M33 processor
Bus Master MPU	• Reset or Non-maskable interrupts • Hard fault	Supported	• Write access ignore • Read access is read as 0	Stored

For information on error access for the Arm MPU, see section 14.4. References. For information on error access for other MPUs, see section 13.3. Register Descriptions and section 13.4. Bus Error Monitoring Section in section 13, Buses.

14.2 Arm MPU

The Arm MPU monitors the addresses accessed by the CPU across the entire address space (0x0000_0000 to 0xFFFF_FFFF) and provides support for:

- (8 + 8) protected regions
- When memory regions overlap, the processor generates a fault if a core access hits the overlapping regions
- Setting access permissions to protected region (Read, Write, Execution)
- Export of memory attributes to the system.

Arm MPU mismatches and permission violations invoke the programmable-priority MemManage fault (Hard Fault) handler. For details, see section 14.4. References.

14.3 Bus Master MPU

The bus master MPU monitors the addresses accessed by the bus masters in the entire address space (0x0000_0000 to 0xFFFF_FFFF). Access-control information can be set up to 8 regions in DMAC/DTC and monitor for access to each region is in accord with this information.

If access to a protected region is detected, the bus master MPU generates an internal reset or a non-maskable interrupt. For information on error access, see section 13.3. Register Descriptions and section 13.4. Bus Error Monitoring Section in section 13, Buses.

The access control information for each area consists of protected/not-protected to read or write.

Table 14.3 lists the specifications of the bus master MPU.

14. 内存保护单元(MPU)

14.1 Overview

MCU有一个内存保护单元(MPU)。

表14.1列出了MPU规格，表14.2显示了检测每个MPU错误时的行为。

Table 14.1 MPU specifications

Classification	Module/Function	Specifications
非法内存访问	Arm®皮质®-M33 CPU	• ArmCPU有一个默认的内存映射。如果CPU进行非法访问，则会发生异常中断 • MPU可以更改默认内存映射。
内存保护	Arm MPU	CPU的内存保护功能：● (8+8)带有子区域和背景区域的区域MPU，用于安全和非安全。
	总线主控MPU	除CPU外的每个总线主控的内存保护功能：●

Table 14.2 MPU错误检测的行为

MPU type	通知类型	错误响应 AHB的HRESP信号 I/F	错误检测总线访问	存储错误访问信息
Arm MPU	• 硬故障	不支持	• 没有正确的写访问 • 未正确读取访问权限	存储在Cortex中 M33 processor
总线主控MPU	• 复位或不可屏蔽中断 • 硬故障	Supported	• 写访问忽略 • 读权限读为0	Stored

有关ArmMPU错误访问的信息，请参阅第14.4节。参考。有关其他错误访问的信息
MPU，见第13.3节。寄存器说明和第13.4节。第13节，总线中的总线错误监控部分。

14.2 Arm MPU

ArmMPU监控整个地址空间（0x0000_0000到0xFFFF_FFFF）中CPU访问的地址，并支持：

●(8+8)个保护区
●当内存区域重叠时，如果核心访问命中重叠区域，处理器将产生故障
●设置对受保护区域的访问权限（读、写、执行）
●将内存属性导出到系统。

ArmMPU不匹配和权限违规调用可编程优先级MemManage故障（硬故障）处理程序。有关详细信息，请参阅第14.4节。参考。

14.3 总线主控MPU

总线主控MPU监控整个地址空间（0x0000_0000到0xFFFF_FFFF）中总线主控访问的地址。DMACDTC中最多可以设置8个区域的访问控制信息，每个区域的访问监控是否与该信息一致。

如果检测到对受保护区域的访问，总线主控MPU会产生内部复位或不可屏蔽中断。有关错误访问的信息，请参阅第13.3节。寄存器说明和第13.4节。第13节，总线中的总线错误监控部分。

每个区域的访问控制信息由受保护的不受保护的读或写组成。

表14.3列出了总线主控MPU的规格。

Table 14.3 Bus master MPU specifications

Parameter	Description
Protected master groups	• DMAC, DTC
Protected regions	0x0000_0000 to 0xFFFF_FFFF
Number of regions	• DMAC/DTC: 8 regions
Address specification for individual regions	• Specifying start and end address for individual regions
Enable or disable setting for memory protection in individual regions	• Enabling or disabling setting for the associated region
Access-control settings for individual regions	• Permission for read and write
Operation on error detection	• Reset or non-maskable interrupts
Register protection	• Protecting registers from illegal writes
TrustZone Filter	• DMAC: Security attribution can be set for each regions

14.3.1 Register Descriptions

Bus access must be stopped before writing to MPU registers.

14.3.1.1 MMPUSARA : Master Memory Protection Unit Security Attribution Register A

Base address: CPSCU = 0x4000_8000

Offset address: 0x130

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	MMPUASA7	MMPUASA6	MMPUASA5	MMPUASA4	MMPUASA3	MMPUASA2	MMPUASA1	MMPUASA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	MMPUASAn	MMPUA Security Attribution (n = 0 to 7) 0: Secure 1: Non-Secure	R/W
31:8	—	These bits are read as 1.	R*1

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.
Note 1. This bit is read only.

MMPUASAn bits (MMPUA Security Attribution (n = 0 to 7))

The MMPUASAn bits specify the security attributes of registers for the Bus Master MPU Region Setting register. The target registers are:

- MMPUSDMACn (n = 0 to 7)
- MMPUEDMACn (n = 0 to 7)
- MMPUACDMACn (n = 0 to 7)

Table 14.3 总线主控MPU规格

Parameter	Description
受保护的主组	• DMAC, DTC
保护区	0x0000_0000 to 0xFFFF_FFFF
地区数量	• DMAC/DTC: 8 regions
个别地区的地址规范	• 指定各个区域的开始和结束地址
在各个区域启用或禁用内存保护设置	• 启用或禁用关联区域的设置
各个区域的访问控制设置	• 读写权限
错误检测操作	• 复位或不可屏蔽中断
注册保护	• 保护寄存器免受非法写入
TrustZone Filter	• DMAC：可以为每个区域设置安全属性

14.3.1 注册说明

在写入MPU寄存器之前必须停止总线访问。

14.3.1.1 MMPUSARA:主内存保护单元安全属性寄存器A

Base address: CPSCU = 0x4000_8000

Offset address: 0x130

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	MMPUASA7	MMPUASA6	MMPUASA5	MMPUASA4	MMPUASA3	MMPUASA2	MMPUASA1	MMPUASA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	MMPUASAn	MMPUA安全属性（n=0到7） 0: Secure 1: Non-Secure	R/W
31:8	—	这些位读为1。	R*1

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。
注1.该位是只读的。

MMPUASan位（MMPUA安全属性（n=0到7））

MMPUASan位指定总线主控MPU区域设置寄存器的寄存器的安全属性。目标寄存器是：

- MMPUSDMACn (n = 0 to 7)
- MMPUEDMACn (n = 0 to 7)
- MMPUACDMACn (n = 0 to 7)

14.3.1.2 MMPUSARB : Master Memory Protection Unit Security Attribution Register B

Base address: CPSCU = 0x4000_8000

Offset address: 0x134

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MMPUBSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MMPUBSA0	MMPUB Security Attribution 0: Secure 1: Non-Secure	R/W
31:1	—	These bits are read as 1.	R*1

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

Note 1. This bit is read-only.

MMPUBSA0 bit (MMPUB Security Attribution)

The MMPUBSA0 bit specifies the security attributes of registers for the Bus Master MPU Region Setting register, Protect register, and OAD register. The target registers are:

- MMPUENDMAC
- MMPUENPTDMAC
- MMPURPTDMAC
- MMPURPTDMAC_SEC
- MMPUOAD
- MMPUOADPT

The Secure user provides a Secure API to Non-secure user for the modification of the MMPURPTDMAC value when MMPUBSA0 bit is set to 0 (Secure).

14.3.1.3 MMPUSDMACn : MMPU Start Address Register for DMAC (n = 0 to 7)

Base address: RMPU = 0x4000_0000

Offset address: 0x0204 + 0x010 × n

Bit position:	31	5	0
Bit field:	MMPUS[31:5]	—	—	—	—	—
Value after reset:	x x x x x x x x x x x x x x x x x x x x x x x x x x x	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	—	These bits are read as 0. The write value should be 0.	R/W
31:5	MMPUS[31:5]	Region start address register Address where the region starts, for use in region determination	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

14.3.1.2 MMPUSARB:主存储器保护单元安全属性寄存器B

Base address: CPSCU = 0x4000_8000

Offset address: 0x134

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MMPUBSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MMPUBSA0	MMPUB安全归因 0: Secure 1: Non-Secure	R/W
31:1	—	这些位读为1。	R*1

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

注1.该位是只读的。

MMPUBSA0位（MMPUB安全属性）

MMPUBSA0位指定总线主控MPU区域设置寄存器、保护寄存器和OAD寄存器的寄存器的安全属性。目标寄存器是：

- MMPUENDMAC
- MMPUENPTDMAC
- MMPURPTDMAC
- MMPURPTDMAC_SEC
- MMPUOAD
- MMPUOADPT

安全用户向非安全用户提供一个安全API，用于在以下情况下修改MMPURPTDMAC值
MMPUBSA0位设置为0（安全）。

14.3.1.3 MMPUSDMACn：DMAC的MMPU起始地址寄存器（n=0到7）

Base address: RMPU = 0x4000_0000

Offset address: 0x0204 + 0x010 × n

Bit position:	31	5	0
Bit field:	MMPUS[31:5]	—	—	—	—	—
重置后的值:	x x x x x x x x x x x x x x x x x x x x x x x x x x x	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	—	这些位被读取为0。写入值应为0。	R/W
31:5	MMPUS[31:5]	区域起始地址寄存器 区域起始地址，用于区域确定	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The MMPUSDMACn (n = 0 to 7) register specifies the start address where the region starts.

This register requires word access. Byte access and half word access is prohibited. When byte access and half word access is executed, operation is not guaranteed.

Regions set by MMPUSDMACn (n = 0 to 7), MMPUEDMACn (n = 0 to 7) and MMPUACDMACn (n = 0 to 7) registers, can be set for a secure access or a non-secure access with the MMPUSARA register. If the corresponding MMPUSARA.MMPUASAn (n = 0 to 7) bit is set to 1, only non-secure access is permitted for that region. On the other hand, if the corresponding MMPUSARA.MMPUASAn (n = 0 to 7) bit is set to 0, only secure access is permitted for that region.

14.3.1.4 MMPUEDMACn : MMPU End Address Register for DMAC (n = 0 to 7)

Base address: RMPU = 0x4000_0000

Offset address: 0x0208 + 0x010 × n

Bit position:	31																									5					0
Bit field:	MMPUE[31:5]																									—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	—	These bits are read as 1. The write value should be 1.	R/W
31:5	MMPUE[31:5]	Region end address register Address where the region end, for use in region determination	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The MMPUEDMAC (n = 0 to 7) register specifies the end address where the region ends.

This register requires word access. Byte access and half word access is prohibited. When byte access and half word access is executed, operation is not guaranteed.

14.3.1.5 MMPUACDMACn : MMPU Access Control Register for DMAC (n = 0 to 7)

Base address: RMPU = 0x4000_0000

Offset address: 0x0200 + 0x010 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	Region enable 0: DMAC Region n unit is disabled 1: DMAC Region n unit is enabled	R/W
1	RP	Read protection 0: Read permission 1: Read protection	R/W
2	WP	Write protection 0: Write permission 1: Write protection	R/W
15:3	—	These bits are read as 0. The write value should be 0.	R/W

如果安全属性配置为非安全：●
允许安全和非安全访问。

MMPUSDMACn（n=0到7）寄存器指定区域开始的起始地址。

该寄存器需要字访问。禁止字节访问和半字访问。当执行字节访问和半字访问时，不能保证操作。

由MMPUSDMACn（n=0到7）、MMPUEDMACn（n=0到7）和MMPUACDMACn（n=0到7）寄存器设置的区域可以通过MMPUSARA寄存器设置为安全访问或非安全访问。如果相应的MMPUSARA.MMPUASAn（n=0到7）位设置为1，则该区域仅允许非安全访问。另一方面，如果相应的MMPUSARA.MMPUASAn(n=0到7)位设置为0，则仅允许对该区域进行安全访问。

14.3.1.4 MMPUEDMACn：DMAC的MMPU结束地址寄存器（n=0到7）

Base address: RMPU = 0x4000_0000

Offset address: 0x0208 + 0x010 × n

Bit position:	31																									5					0
Bit field:	MMPUE[31:5]																									—	—	—	—	—
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	—	这些位被读取为1。写入值应为1。	R/W
31:5	MMPUE[31:5]	区域结束地址寄存器 区域结束的地址，用于区域确定	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
● 忽略非安全写入访问，不会生成TrustZone访问错误。
如果安全属性配置为非安全：●
允许安全和非安全访问。

MMPUEDMAC（n=0到7）寄存器指定区域结束的结束地址。

该寄存器需要字访问。禁止字节访问和半字访问。当执行字节访问和半字访问时，不能保证操作。

14.3.1.5 MMPUACDMACn：用于DMAC的MMPU访问控制寄存器（n=0到7）

Base address: RMPU = 0x4000_0000

Offset address: 0x0200 + 0x010 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	区域启用 0：禁用DMAC区域n单元1：启用DMAC区域n单元	R/W
1	RP	读保护 0：读取权限1：读取保护	R/W
2	WP	写保护 0：写权限1：写保护	R/W
15:3	—	这些位被读取为0。写入值应为0。	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Region n unit sets the ENABLE bit, the RP bit, and the WP bit each.

ENABLE bit (Region enable)

The ENABLE bit controls the enable or disable of DMAC/DTC region n (n = 0 to 7) unit.

When the ENABLE bit is set to 1, the RP bit and the WP bit control access permission for read and write protection to MMPUSDMACn (n = 0 to 7) and MMPUEDMACn (n = 0 to 7).

When the ENABLE bit is set to 0, access to DMAC region n (n = 0 to 7) is the outside region.

RP bit (Read protection)

The RP bit enables or disables read protection of DMAC/DTC region n (n = 0 to 7).

When the ENABLE bit is set to 1, the RP bit is available.

WP bit (Write protection)

The WP bit enables or disables write protection of DMAC/DTC region n (n = 0 to 7).

When the ENABLE bit is set to 1, the WP bit is available.

Table 14.4 Function of Region Control Circuit for DMAC

MMPUACDMACn (n = 0 to 7)			Access	Region	Output of DMAC Region n unit (n = 0 to 7)
ENABLE	RP	WP			
0	—	—	Read	—	Outside region
			Write		Outside region
1	0	0	Read	Inside	Permitted region
				Outside	Outside region
			Write	Inside	Permitted region
				Outside	Outside region
	0	1	Read	Inside	Permitted region
				Outside	Outside region
			Write	Inside	Protection region
				Outside	Outside region
	1	0	Read	Inside	Protection region
				Outside	Outside region
			Write	Inside	Permitted region
				Outside	Outside region
	1	1	Read	Inside	Protection region
				Outside	Outside region
			Write	Inside	Protection region
				Outside	Outside region

Note: Each regions of DMAC / DTC are set for secure access and non-secure access by MMPUSARA register. In this case, Non-Secure regions in secure access and secure regions in Non-Secure access are outside regions.

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

区域n单元分别设置ENABLE位、RP位和WP位。

ENABLE位（区域使能）

ENABLE位控制DMACDTC区域n（n=0到7）单元的启用或禁用。

当ENABLE位设置为1时，RP位和WP位控制读写保护的访问权限MMPUSDMACn（n=0到7）和MMPUEDMACn（n=0到7）。

当ENABLE位设置为0时，访问DMAC区域n（n=0到7）是外部区域。

RP bit (Read protection)

RP位启用或禁用DMACDTC区域n（n=0到7）的读保护。

当ENABLE位设置为1时，RP位可用。

WP bit (Write protection)

WP位启用或禁用DMACDTC区域n（n=0到7）的写保护。

当ENABLE位设置为1时，WP位可用。

Table 14.4 DMAC区域控制电路的功能

MMPUACDMACn (n = 0 to 7)			Access	Region	DMAC区域n单元的输出（n=0到7）
ENABLE	RP	WP			
0	—	—	Read	—	区域外
			Write		区域外
1	0	0	Read	Inside	许可区域
				Outside	区域外
			Write	Inside	许可区域
				Outside	区域外
	0	1	Read	Inside	许可区域
				Outside	区域外
			Write	Inside	保护区
				Outside	区域外
	1	0	Read	Inside	保护区
				Outside	区域外
			Write	Inside	许可区域
				Outside	区域外
	1	1	Read	Inside	保护区
				Outside	区域外
			Write	Inside	保护区
				Outside	区域外

Note: DMACDTC的每个区域都通过MMPUSARA寄存器设置为安全访问和非安全访问。在这种情况下，安全访问中的非安全区域和非安全访问中的安全区域是外部区域。

Table 14.5 Function of Master Control Circuit for DMAC

MMPUENDMAC ENABLE	Output of DMAC Region 0 unit	Output of DMAC Region 1 unit	Output of DMAC Region 2-7 unit	Function of DMAC
1	Protected region	Don't care	Don't care	Generate error
	Don't care	Protected region	Don't care	Generate error
	Don't care	Don't care	Protected region	Generate error
	Outside region	Outside region	Outside region	Generate error
Other cases				No error

A master MPU error occurs on the following conditions:

1. MMPUENDMAC.ENABLE = 1, and output of one or more Region n unit is protected region.
2. MMPUENDMAC.ENABLE = 1, and output of all Region n unit are outside region.

Other cases are handled as permitted region.

14.3.1.6 MMPUENDMAC : MMPU Enable Register for DMAC

Base address: RMPU = 0x4000_0000

Offset address: 0x0100

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	Bus Master MPU of DMAC enable 0: Bus Master MPU of DMAC is disabled. 1: Bus Master MPU of DMAC is enabled.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the ENABLE bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

ENABLE bit (Bus Master MPU of DMAC enable)

The ENABLE bit controls enable or disable of the bus master MPU function of each master group.

When the ENABLE bit is set to 1, MMPUACDMACn (n = 0 to 7) is valid. When the ENABLE bit is set to 0, MMPUACDMACn (n = 0 to 7) is invalid for all regions. The bus master MPU function sets the ENABLE bit of each master group. When the ENABLE bit is set, write 0xA5 in KEY[7:0] at the same time.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writing to the ENABLE bit. When writing to the ENABLE bit, write 0xA5 in KEY[7:0] bits at the same time. When values other than 0xA5 are written to KEY[7:0] bits, the ENABLE bit is not updated. The KEY[7:0] bits are always read as 0x00.

Table 14.5 DMAC主控电路的功能

MMPUENDMAC ENABLE	DMAC区域0单元的输出	DMAC区域1单元的输出	DMAC区域2-7单元的输出	DMAC的功能
1	保护区	Don't care	Don't care	产生错误
	Don't care	保护区	Don't care	产生错误
	Don't care	Don't care	保护区	产生错误
	区域外	区域外	区域外	产生错误
其他案例				没有错误

主控MPU错误发生在以下情况：

1.MMPUENDMAC.ENABLE=1，一个或多个Regionn单元的输出为受保护区域。

2.MMPUENDMAC.ENABLE=1，所有Regionn单元的输出都在Region外。

其他情况按许可区域处理。

14.3.1.6 MMPUENDMAC:DMAC的MMPU使能寄存器

Base address: RMPU = 0x4000_0000

Offset address: 0x0100

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	ENABLE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	DMAC的总线主控MPU使能 0：DMAC的总线主控MPU禁用。1：DMAC的总线主控MPU使能。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对ENABLE位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

ENABLE位（DMAC的总线主控MPU使能）

ENABLE位控制每个主机组的总线主机MPU功能的启用或禁用。

当ENABLE位设置为1时，MMPUACDMACn（n=0至7）有效。当ENABLE位设置为0时，MMPUACDMACn(n=0to7)对所有地区都无效。总线主控MPU功能设置每个主控组的ENABLE位。当ENABLE位置位时，同时在KEY[7:0]中写入0xA5。

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对ENABLE位的写入。写入ENABLE位时，将0xA5写入KEY[7:0]位。当0xA5以外的值写入KEY[7:0]位时，ENABLE位不会更新。
KEY[7:0]位总是读为0x00。

14.3.1.7 MMPUENPTDMAC : MMPU Enable Protect Register for DMAC

Base address: RMPU = 0x4000_0000

Offset address: 0x0104

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: MMPUENDMAC register writes are possible. 1: MMPUENDMAC register writes are protected. Read is possible.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the PROTECT bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the MMPUENDMAC register.

When writing to the PROTECT bit, write 0xA5 in KEY[7:0] at the same time.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, write 0xA5 in KEY[7:0] at the same time. When values other than 0xA5 are written in KEY[7:0] bits, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 0x00.

14.3.1.8 MMPURPTDMAC : MMPU Regions Protect Register for DMAC

Base address: RMPU = 0x4000_0000

Offset address: 0x0108

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: Bus Master MPU register for DMAC writing is possible. 1: Bus Master MPU register for DMAC writing is protected. Read is possible.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the PROTECT bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

14.3.1.7 MMPUENPTDMAC:MMPU启用DMAC的保护寄存器

Base address: RMPU = 0x4000_0000

Offset address: 0x0104

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	保护
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	注册保护 0：可以写入MMPUENDMAC寄存器。1：MMPUENDMAC寄存器写受保护。读取是可能的。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对PROTECT位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

PROTECT位（寄存器保护）

PROTECT位启用或禁用对MMPUENDMAC寄存器的写入。

写入PROTECT位时，同时向KEY[7:0]写入0xA5。

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对PROTECT位的写入。写入PROTECT位时，将0xA5写入KEY[7:0]同时进行。当KEY[7:0]位中写入0xA5以外的值时，PROTECT位不会更新。KEY[7:0]位总是读为0x00。

14.3.1.8 MMPURPTDMAC:DMAC的MMPU区域保护寄存器

Base address: RMPU = 0x4000_0000

Offset address: 0x0108

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	保护
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	注册保护 0：可以进行DMAC写入的总线主控MPU寄存器。1：用于DMAC写入的总线主控MPU寄存器受保护。读取是可能的。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对PROTECT位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：

- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected.

MMPURPTDMAC.PROTECT controls the following registers:

- MMPUSDMACn (n = 0 to 7) of Non-Secure program
- MMPUEDMACn (n = 0 to 7) of Non-Secure program
- MMPUACDMACn (n = 0 to 7) of Non-Secure program

When writing to the PROTECT bit, write 0xA5 simultaneously to the KEY[7:0] bits, using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, write 0xA5 simultaneously to the KEY[7:0] bits. When other values are written, the PROTECT bit is not updated.

The KEY[7:0] bits always read as 0x00.

14.3.1.9 MMPURPTDMAC_SEC : MMPU Regions Protect register for DMAC Secure

Base address: RMPU = 0x4000_0000

Offset address: 0x010C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: Bus master MPU register for DMAC secure writes are possible. 1: Bus master MPU register for DMAC secure writes are protected. Read is possible.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the PROTECT bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected.

MMPURPTDMAC_SEC.PROTECT controls the following registers:

- MMPUSDMACn (n = 0 to 7) of Secure program
- MMPUEDMACn (n = 0 to 7) of Secure program
- MMPUACDMACn (n = 0 to 7) of Secure program

When writing to the PROTECT bit, write 0xA5 simultaneously to the KEY[7:0] bits, using halfword access.

- 允许安全和非安全访问。

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

PROTECT位（寄存器保护）

PROTECT位启用或禁用对要保护的相关寄存器的写入。

MMPURPTDMAC.PROTECT控制以下寄存器：

- ●非安全程序的MMPUSDMACn(n=0到7)
- ●非安全程序的MMPUEDMACn(n=0到7)
- ●非安全程序的MMPUACDMACn(n=0to7)

写入PROTECT位时，使用半字访问同时将0xA5写入KEY[7:0]位。

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对PROTECT位的写入。写入PROTECT位时，同时将0xA5写入KEY[7:0]位。写入其他值时，PROTECT位不会更新。

KEY[7:0]位总是读为0x00。

14.3.1.9 MMPURPTDMAC_SEC：用于DMACSecure的MMPU区域保护寄存器

Base address: RMPU = 0x4000_0000

Offset address: 0x010C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	保护
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	注册保护 0：可以进行DMAC安全写入的总线主控MPU寄存器。1：用于DMAC安全写入的总线主控MPU寄存器受到保护。读取是可能的。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对PROTECT位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

PROTECT位（寄存器保护）

PROTECT位启用或禁用对要保护的相关寄存器的写入。

MMPURPTDMAC_SEC.PROTECT控制以下寄存器：

- ●Secure程序的MMPUSDMACn(n=0to7)
- ●安全程序的MMPUEDMACn(n=0到7)
- ●安全程序的MMPUACDMACn(n=0to7)

写入PROTECT位时，使用半字访问同时将0xA5写入KEY[7:0]位。

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, write 0xA5 simultaneously to the KEY[7:0] bits. When other values are written, the PROTECT bit is not updated.

The KEY[7:0] bits are always read as 0x00.

14.3.1.10 MMPUOAD : MMPU Operation After Detection Register

Base address: RMPU = 0x4000_0000

Offset address: 0x0000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation after detection 0: Non-maskable interrupt 1: Reset	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code This bit enables or disables writes to the OAD bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

OAD bit (Operation after detection)

The OAD bit is specified to generate either reset or non-maskable interrupt when the access to the protect region is detected by the BUS Master MPU.

When writing to the OAD bit, write 0xA5 simultaneously to the KEY[7:0] bits using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writing to the OAD bit. When writing to the OAD bit, write 0xA5 simultaneously to the KEY[7:0] bits. When other values are written, the OAD bit is not updated.

The KEY[7:0] bits always read as 0x00.

14.3.1.11 MMPUOADPT : MMPU Operation After Detection Protect Register

Base address: RMPU = 0x4000_0000

Offset address: 0x0004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: MMPUOAD register writes are possible. 1: MMPUOAD register writes are protected. Read is possible.	R/W

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对PROTECT位的写入。写入PROTECT位时，同时将0xA5写入KEY[7:0]位。写入其他值时，PROTECT位不会更新。

KEY[7:0]位总是读为0x00。

14.3.1.10 MMPUOAD:检测后的MMPU操作寄存器

Base address: RMPU = 0x4000_0000

Offset address: 0x0000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	OAD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	检测后操作 0：不可屏蔽中断1：复位	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 该位启用或禁用对OAD位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

OAD位（检测后的操作）

当总线主控MPU检测到对保护区域的访问时，OAD位被指定为产生复位或不可屏蔽中断。

写入OAD位时，使用半字访问同时将0xA5写入KEY[7:0]位。

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用写入OAD位。写入OAD位时，同时将0xA5写入KEY[7:0]位。写入其他值时，不会更新OAD位。

KEY[7:0]位总是读为0x00。

14.3.1.11 MMPUOADPT:检测保护寄存器后的MMPU操作

Base address: RMPU = 0x4000_0000

Offset address: 0x0004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	保护
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	注册保护 0：MMPUOAD寄存器写入是可能的。1：MMPUOAD寄存器写受保护。读取是可能的。	R/W

Bit	Symbol	Function	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key code These bits enable or disable writes to the PROTECT bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected.

MMPUOADPT.PROTECT controls the following register:

- MMPUOAD

When the PROTECT bit is set simultaneously, write 0xA5 to the KEY[7:0] bits using half word access.

KEY[7:0] bits (Key code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit simultaneously, write 0xA5 to the KEY[7:0] bits. When other values are written to the KEY[7:0] bits, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 0x00.

14.3.2 Operation

14.3.2.1 Memory protection

The bus master MPU monitors memory access using control settings made individually for the access control regions. If access to a protected region is detected, the bus master MPU generates a memory protection error.

Bus Master MPU can be set for up to 8 protection regions. It is protection region when set up of permission region and protection region overlaps. It is protection region when set up of two protection region overlaps.

Bus Master MPU has master groups of DMAC/DTC.

Memory protection checks the address of the bus which the master group unified. Therefore, all the access of a master group is detected by memory protection.

The region setting registers of the Bus Master MPU for DMAC/DTC can be set for secure access and Non-Secure access using the MMPUSARA register. Make secure access and Non-Secure access settings the same for each DMAC/DTC channel and the corresponding region setting registers of the Bus Master MPU.

Bus Master MPU is permission of all regions after reset. All region is protected by setting MMPUENDMAC.ENABLE = 1.

Each region sets up a permission region on the protection region. If access to the protected region is detected, Bus Master MPU will generate an error.

Figure 14.1 shows the use case of a bus master MPU.

Bit	Symbol	Function	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对PROTECT位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

PROTECT位（寄存器保护）

PROTECT位启用或禁用对要保护的相关寄存器的写入。

MMPUOADPT.PROTECT控制以下寄存器：

- MMPUOAD

当PROTECT位同时置位时，使用半字访问将0xA5写入KEY[7:0]位。

KEY[7:0] bits (Key code)

KEY[7:0]位启用或禁用对PROTECT位的写入。同时写入PROTECT位时，将0xA5写入KEY[7:0]位。当其他值写入KEY[7:0]位时，PROTECT位不会更新。KEY[7:0]位总是读为0x00。

14.3.2 Operation

14.3.2.1 内存保护

总线主控MPU使用为访问控制区域单独进行的控制设置来监视内存访问。如果检测到对受保护区域的访问，则总线主控MPU会产生内存保护错误。

总线主控MPU最多可设置8个保护区域。许可区域与保护区域的设置重叠时为保护区域。两个保护区域重叠设置时为保护区域。

总线主控MPU具有DMACDTC主控组。

内存保护检查主组统一的总线地址。因此，一个主组的所有访问都被内存保护检测到。

可以使用MMPUSARA寄存器为DMACDTC的总线主控MPU的区域设置寄存器设置安全访问和非安全访问。使每个DMACDTC通道和总线主控MPU的相应区域设置寄存器的安全访问和非安全访问设置相同。

BusMasterMPU是复位后所有区域的权限。通过设置MMPUENDMAC.ENABLE=1来保护所有区域。

每个区域在保护区域上设置一个权限区域。如果检测到对受保护区域的访问，则总线主控MPU会产生错误。

图14.1显示了总线主控MPU的用例。

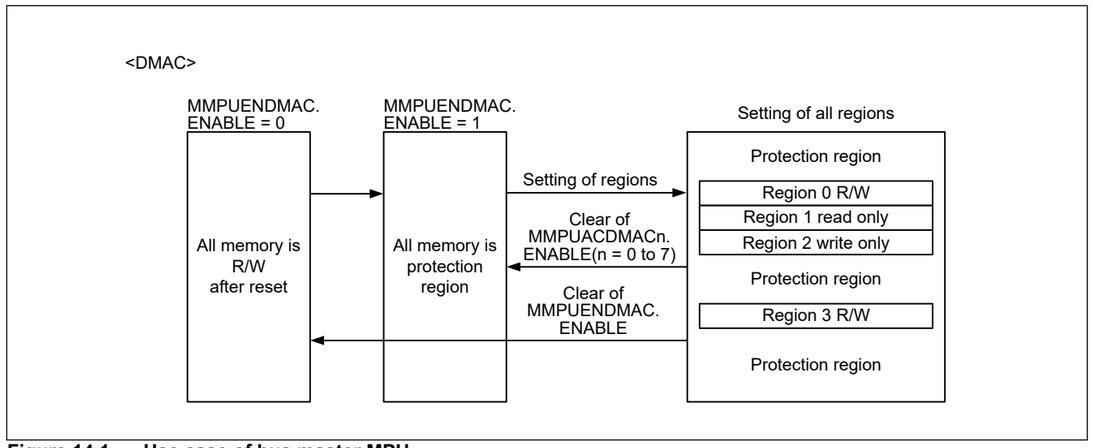


Figure 14.1 Use case of bus master MPU

Figure 14.2 shows the access permission or protection by the overlapping bus master MPU regions.

Access control for the overlapping regions is as follows:

- The region is handled as a protected region when output of one or more region units is a protected region
- The region is handled as a protected region when output of all region units is outside of the regions
- Other cases are handled as permitted regions.

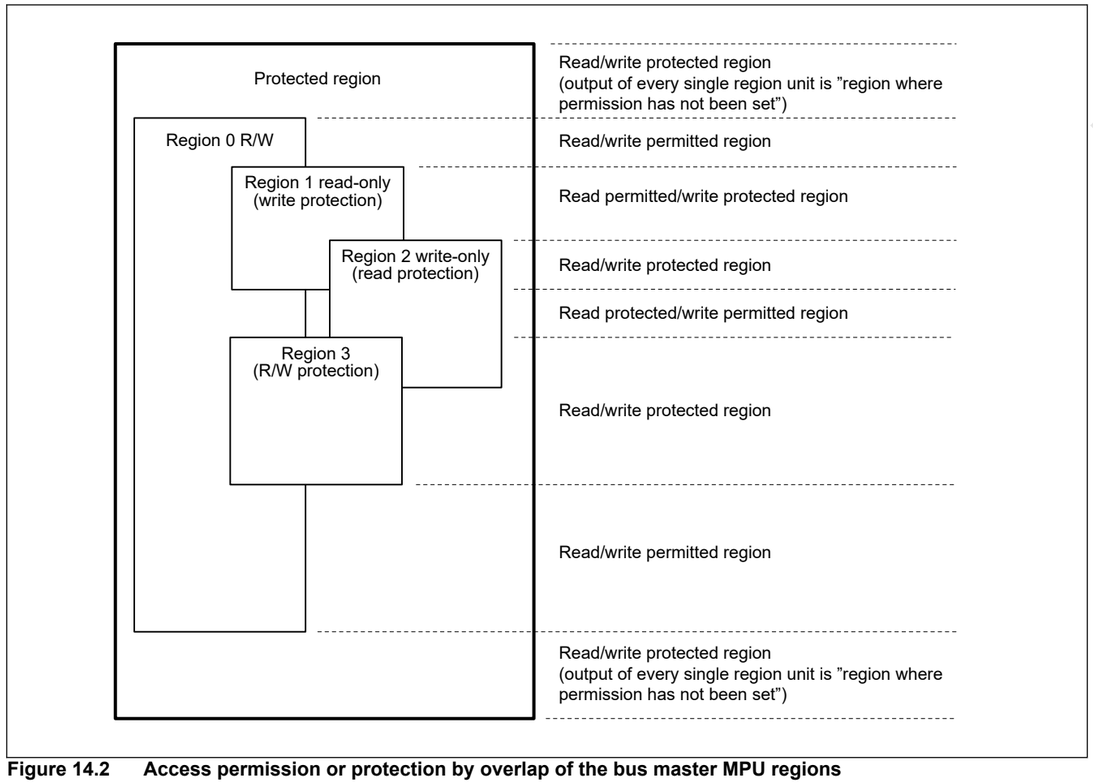


Figure 14.2 Access permission or protection by overlap of the bus master MPU regions

Figure 14.3 shows the register setting flow after reset. During this register setting, stop all bus masters except the CPU.

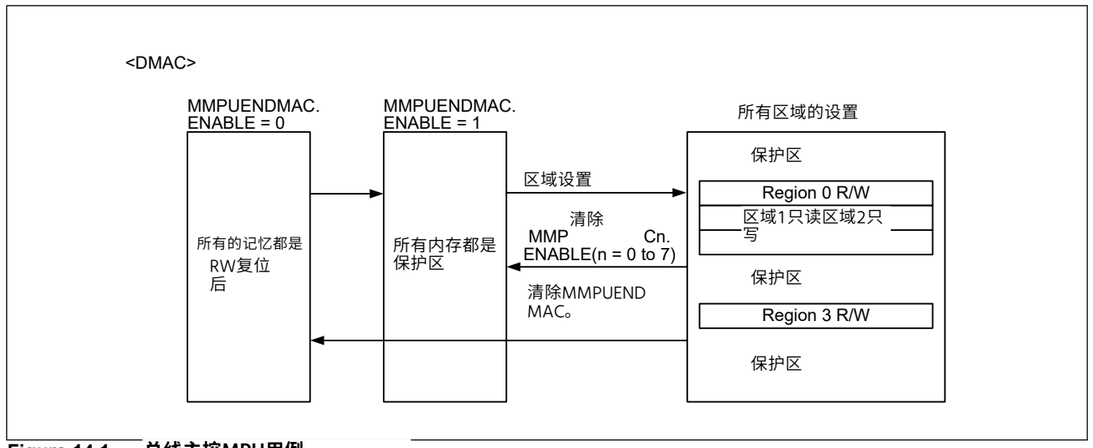


Figure 14.1 总线主控MPU用例

图14.2显示了重叠总线主控MPU区域的访问许可或保护。

重叠区域的访问控制如下：

- ●当一个或多个区域单元的输出为受保护区域时，该区域被视为受保护区域
- ●当所有区域单元的输出都在区域之外时，该区域被视为受保护区域
- ●其他情况按许可区域处理。

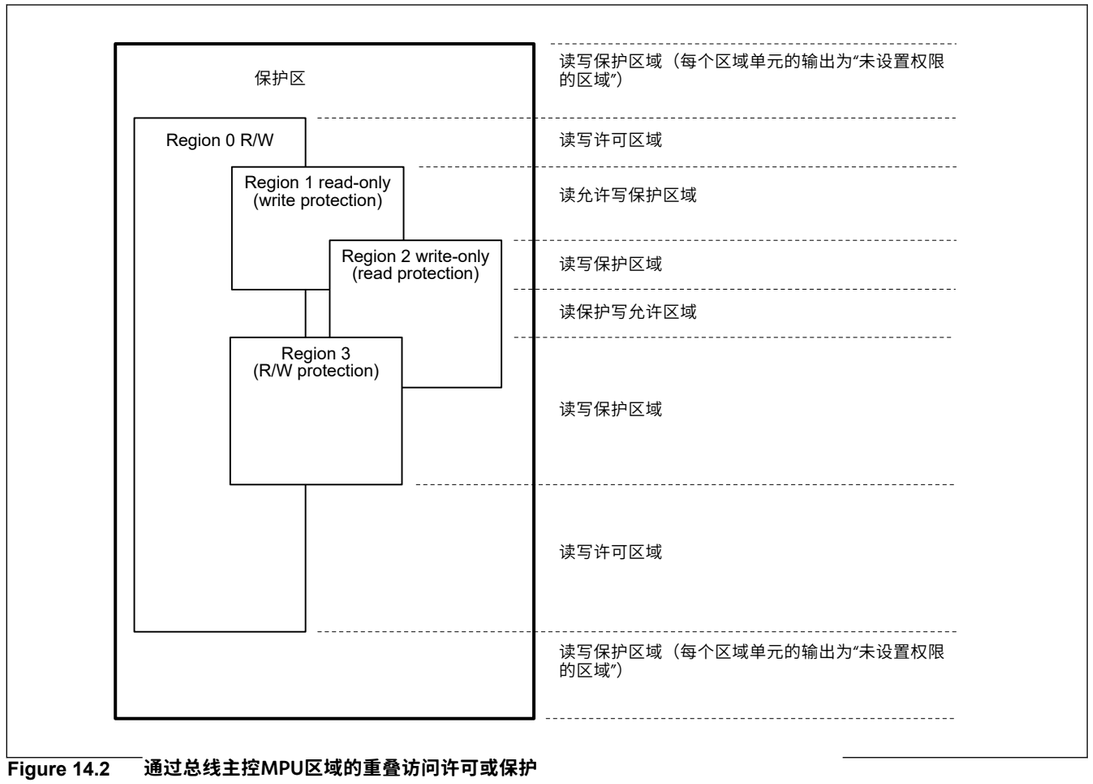


Figure 14.2 通过总线主控MPU区域的重叠访问许可或保护

图14.3显示了复位后的寄存器设置流程。在此寄存器设置期间，停止除CPU之外的所有总线主机。

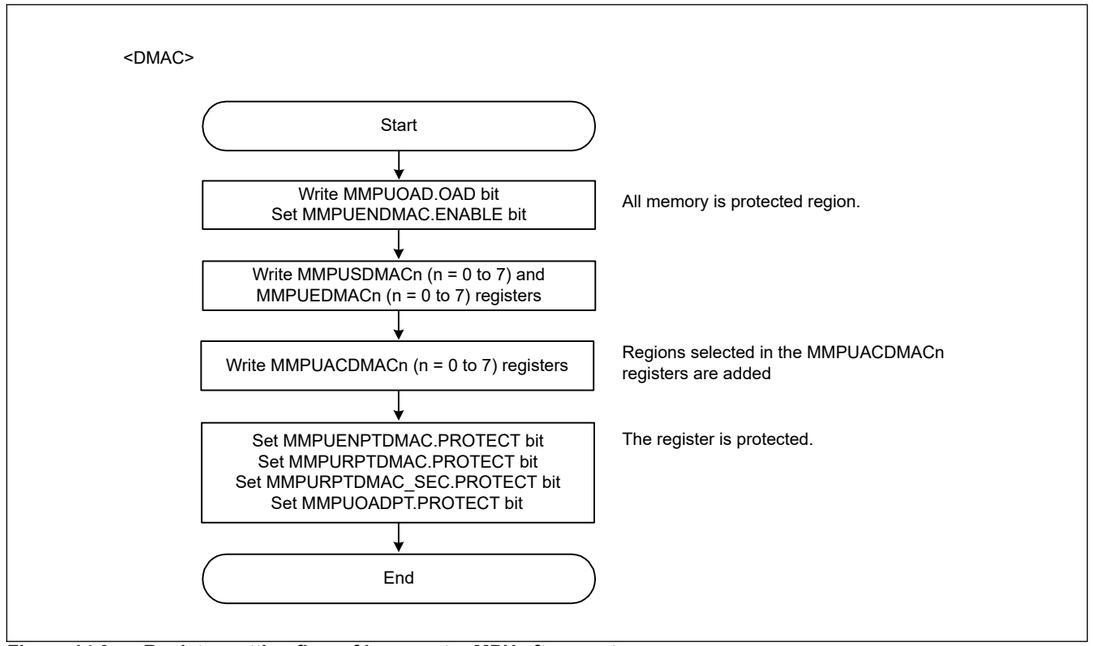


Figure 14.3 Register setting flow of bus master MPU after reset

Figure 14.4 shows the register setting flow for adding regions. During this register setting, stop all masters except the CPU.

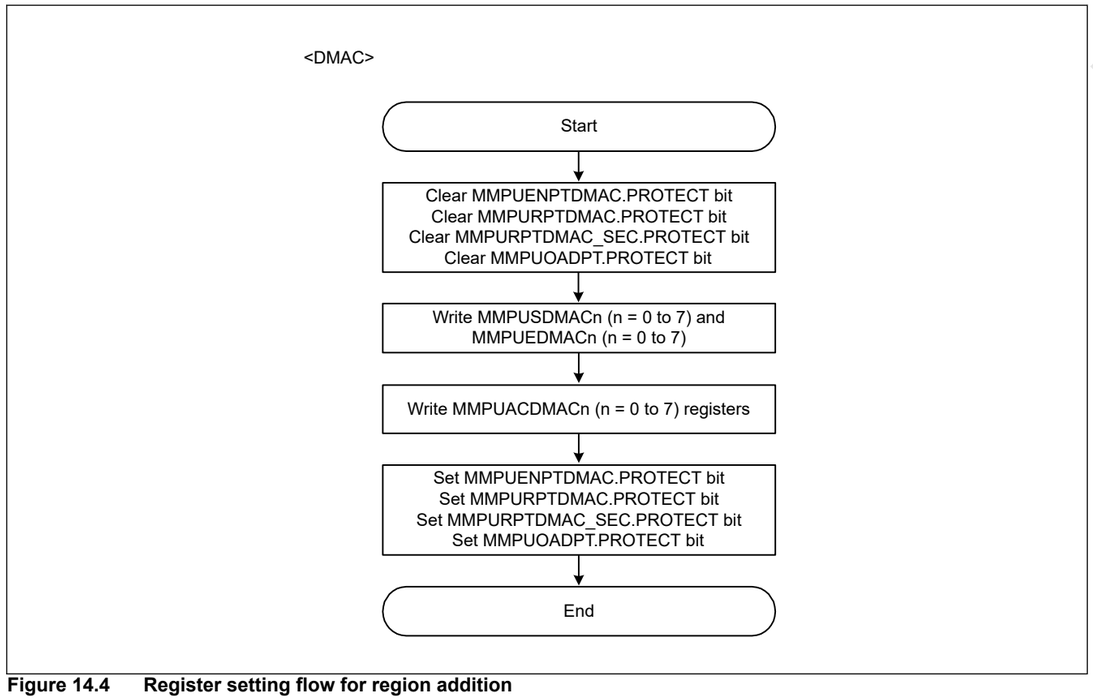


Figure 14.4 Register setting flow for region addition

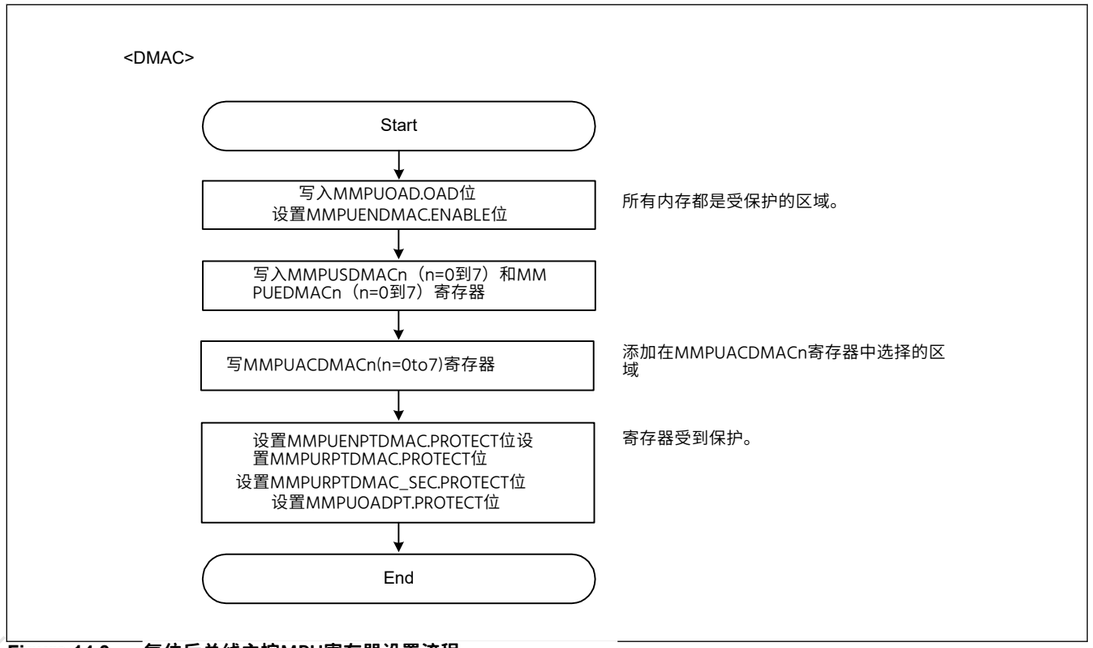


Figure 14.3 复位后总线主控MPU寄存器设置流程

图14.4显示了添加区域的寄存器设置流程。在此寄存器设置期间，停止除CPU之外的所有主机。

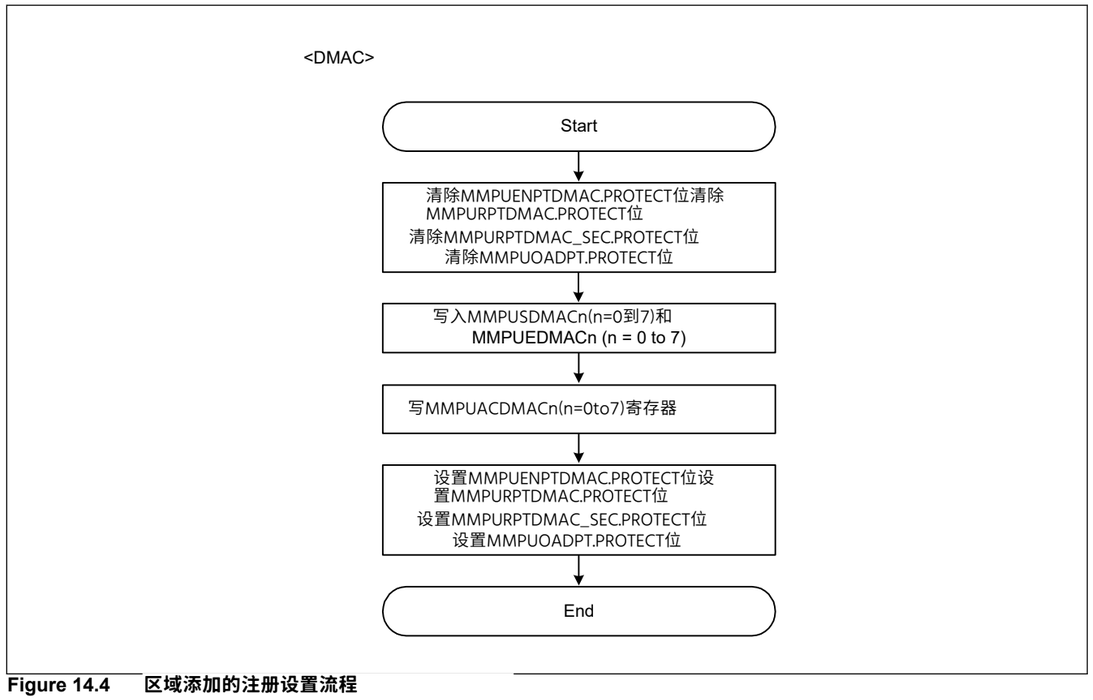


Figure 14.4 区域添加的注册设置流程

14.3.2.2 Protecting the registers

Registers related to the Bus Master MPU can be protected with the PROTECT bit in the MMPUENPTDMAC, MMPURPTDMAC, MMPURPTDMAC_SEC, and MMPUOADPT registers.

Table 14.6 PROTECT bit and Protected target registers

PROTECT bit	Protect target registers
MMPUENPTDMAC.PROTECT	MMPUENDMAC
MMPURPTDMAC.PROTECT	The following registers set to Non-Secure by MMPUSARA.MMPUASAn (n = 0 to 7). MMPUSDMACn (n = 0 to 7) MMPUEDMACn (n = 0 to 7) MMPUACDMACn (n = 0 to 7)
MMPURPTDMAC_SEC.PROTECT	The following registers set to Secure by MMPUSARA.MMPUASAn (n = 0 to 7). MMPUSDMACn (n = 0 to 7) MMPUEDMACn (n = 0 to 7) MMPUACDMACn (n = 0 to 7)
MMPUOADPT.PROTECT	MMPUOAD

14.3.2.3 Memory protection error

If access to a protected region is detected, the bus master MPU generates an error. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or a reset.

The non-maskable interrupt status is indicated in ICU.NMISR.BUSMST. For details, see section 12, Interrupt Controller Unit (ICU). The reset status is indicated in SYSTEM.RSTSR1.BUSMRF. For details, see section 5, Resets.

14.4 References

1. *Arm®v8-M Architecture Reference Manual* (ARM DDI0553B.g)
2. *Arm® Cortex®-M33 Processor Technical Reference Manual* (ARM 100230_0004_00_en)

14.3.2.2 保护寄存器

与总线主控MPU相关的寄存器可以通过MMPUENPTDMAC中的PROTECT位进行保护，MMPURPTDMAC、MMPURPTDMAC_SEC和MMPUOADPT寄存器。

Table 14.6 PROTECT位和受保护的目标寄存器

保护位	保护目标寄存器
MMPUENPTDMAC.PROTECT	MMPUENDMAC
MMPURPTDMAC.PROTECT	以下寄存器设置为非安全由 MMPUSARA.MMPUASAn (n = 0 to 7). MMPUSDMACn (n = 0 to 7) MMPUEDMACn (n = 0 to 7) MMPUACDMACn (n = 0 to 7)
MMPURPTDMAC_SEC.PROTECT	以下寄存器由MMPUSARA.MMPUASAn（n=0到7）设置为Secure。 MMPUSDMACn（n=0到7）MMPUEDMACn（n=0到7） MMPUACDMACn (n = 0 to 7)
MMPUOADPT.PROTECT	MMPUOAD

14.3.2.3 内存保护错误

如果检测到对受保护区域的访问，则总线主控MPU会产生错误。设置OAD位以选择将错误报告为不可屏蔽中断还是复位。

不可屏蔽中断状态在ICU.NMISR.BUSMST中指示。有关详细信息，请参见第12节，中断控制器单位（ICU）。复位状态在SYSTEM.RSTSR1.BUSMRF中指示。有关详细信息，请参阅第5节，重置。

14.4 References

1.Arm®v8-M架构参考手册（ARMDDI0553B.g）
2.Arm®Cortex®-M33处理器技术参考手册（ARM100230_0004_00_en）

15. DMA Controller (DMAC)

15.1 Overview

The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

Table 15.1 lists the DMAC specifications, and Figure 15.1 shows a block diagram of the DMAC.

Table 15.1 DMAC specifications (1 of 2)

Item		Description
Number of channels		8 channels (DMACn (n = 0 to 7))
Transfer space		4 GB (0x00000000 to 0xFFFFFFFF excluding reserved areas)
Maximum transfer volume		64 M data (Maximum number of transfers in block transfer mode: 1,024 data × 65,536 blocks)
DMAC activation source		Selectable for each channel: ● Software trigger ● Interrupt requests from peripheral modules or trigger from external interrupt input pins.*1
Channel priority		Channel 0 > Channel 1 > Channel 2 > Channel 3… > Channel 7 (Channel 0: Highest)
Transfer data	Single data	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1,024
Transfer mode	Normal transfer mode	● One data transfer by one DMA transfer request ● Free running function (setting in which total number of data transfers is not specified) settable
	Repeat transfer mode	● One data transfer by one DMA transfer request ● Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. ● Maximum settable repeat size: 1,024 ● Selectable free running function
	Repeat-block transfer mode	● One block data transfer by one DMA transfer request ● Maximum settable block size: 1,024 ● Block transfer can be repeated ● Maximum settable repeat size: 64K ● Selectable free running function
	Block transfer mode	● One block data transfer by one DMA transfer request ● Maximum settable block size: 1,024 data ● Selectable free running function
Selective functions	Extended repeat area function	● Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed ● Area of 2 bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination
Processing on DMAC transfer error		● When the DMAC transfer error occurs, it is stop the transfer that caused the error channel ● Request to clear the register for activation request of DMAC error channel to ICU
Interrupt (DMACn_INT)	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.
	Transfer escape end interrupt	● Generated when the repeat size of data transfer is completed. ● Generated when the source address extended repeat area overflows. ● Generated when the destination address extended repeat area overflows.
Interrupt (DMA_TRANSERR)	Error response detection interrupt	● Generated when the DMAC transfer error occurs
Event link activation (DMACn_INT)		An event link request is generated after each data transfer (for block transfer, after each block is transferred).

15. DMA Controller (DMAC)

15.1 Overview

MCU包括一个8通道直接内存访问控制器(DMAC)，无需CPU干预即可传输数据。当产生DMA传输请求时，DMAC将存储在传输源地址的数据传输到传输目标地址。

表15.1列出了DMAC规范，图15.1显示了DMAC的框图。

Table 15.1 DMAC规格(1of2)

Item		Description
通道数		8个通道（DMACn（n=0到7））
转移空间		4GB（0x00000000到0xFFFFFFFF不包括保留区域）
最大传输量		64M数据（块传输模式下的最大传输数：1 024数据×65 536块）
DMAC激活源		每个通道可选择：● 软件触发 ● 来自外围模块的中断请求或来自外部中断输入引脚的触发。*1
通道优先级		Channel 0 > Channel 1 > Channel 2 > Channel 3… > Channel 7 (Channel 0: Highest)
传输数据	单一数据	位长：8、16、32位
	块大小	数据数量：1至1 024
传输模式	正常传输模式	● 1个DMA传输请求1个数据传输 ● 自由运行功能（不指定数据传输总数的设置）可设置
	重复传输模式	● 1个DMA传输请求1个数据传输 ● 为传输源或目标指定的重复数据传输大小完成后，程序返回传输起始地址。 ● 最大可设置重复大小：1 024 ● 可选择的自由运行功能
	重复块传输模式	● 1个DMA传输请求的1个块数据传输 ● 最大可设置块大小：1 024 ● 块传输可以重复 ● 最大可设置重复大小：64K ● 可选择的自由运行功能
	块传输模式	● 1个DMA传输请求的1个块数据传输 ● 最大可设置块大小：1 024个数据 ● 可选择的自由运行功能
选择性功能	扩展重复区域功能	● 可以通过重复指定范围内的地址值来传输数据的功能，其中传输地址寄存器中的高位值是固定的 ● 2字节至128兆字节的区域可单独设置为传输源和目标的扩展重复区域
处理DMAC传输错误		● 当发生DMAC传输错误时，是停止传输导致错误通道 ● 请求清除寄存器以激活对ICU的DMAC错误通道的请求
Interrupt (DMACn_INT)	传输结束中断	在传输计数器指定的传输数据量完成时生成。
	传输转义结束中断	● 数据传输的重复大小完成时生成。 ● 当源地址扩展重复区溢出时产生。 ● 当目标地址扩展重复区溢出时产生。
Interrupt (DMA_TRANSERR)	错误响应检测中断	● 发生DMAC传输错误时生成
事件链接激活(DMACn_INT)		每次数据传输后都会生成一个事件链接请求（对于块传输，在每个块传输后）。

Table 15.1 DMAC specifications (2 of 2)

Item	Description
Master TrustZone Filter	TrustZone violation area of Flash and SRAM is detected before a non-secure channel access the bus.
Power consumption reduction function	Module-stop state can be set.
TrustZone Filter	Security attribution can be set for each channels

Note: Security attribution Register of DMAC channel is described in ICU.ICUSARC
Note 1. For details on DMAC activation sources, see Table 12.4 in section 12, Interrupt Controller Unit (ICU).

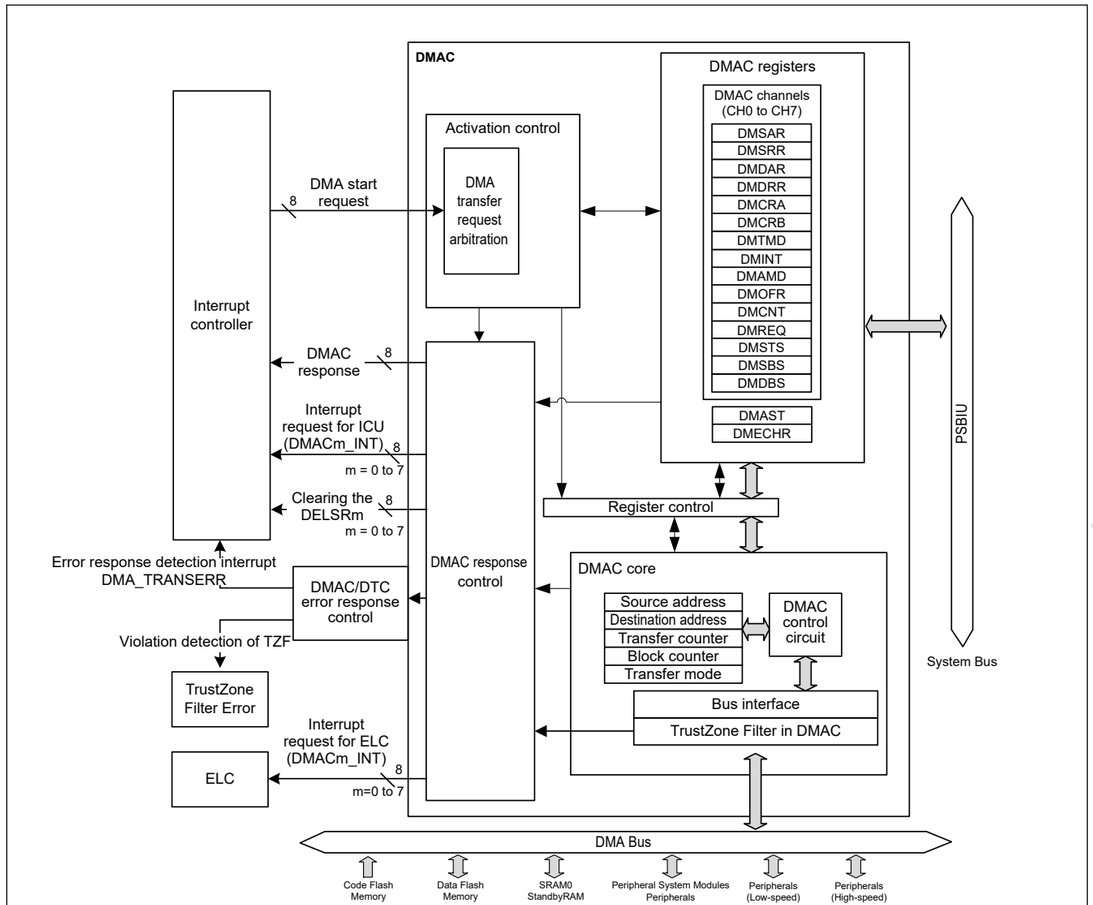


Figure 15.1 Block Diagram of DMAC

Table 15.1 DMAC规范（2个中的2个）

Item	Description
主信任区过滤器	在非安全通道访问总线之前检测到Flash和SRAM的TrustZone违规区域。
功耗降低功能	可设置模块停止状态。
TrustZone Filter	可以为每个通道设置安全属性

Note: ICU.ICUSARC中描述了DMAC通道的安全属性寄存器
注1.有关DMAC激活源的详细信息，请参阅第12节“中断控制器单元(ICU)”中的表12.4。

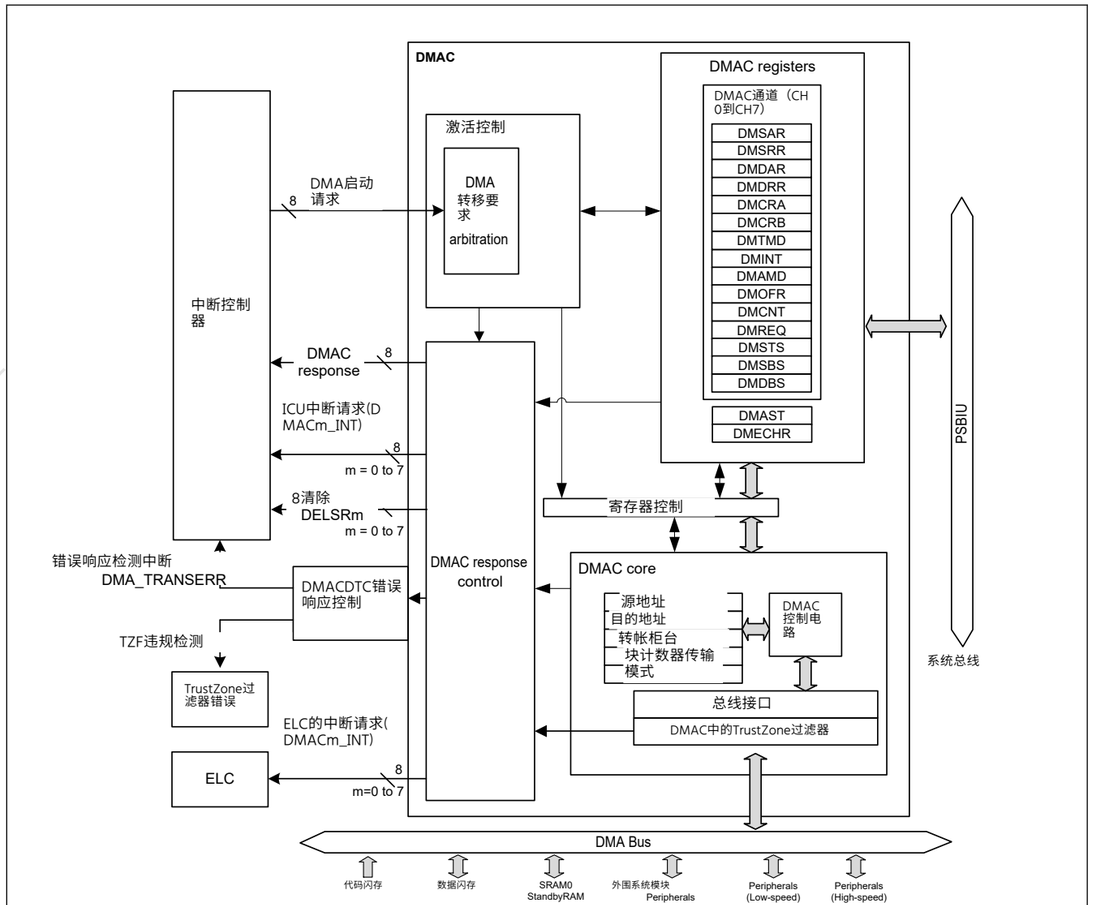


Figure 15.1 DMAC框图

15.2 Register Descriptions

15.2.1 DMACSAR : DMAC Controller Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMASTSA
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	DMASTSA	DMAST Security Attribution 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

For DMAC, security attribution is set for each channel. However, this register only sets the DMAST register security attribute. The security attribution setting of each channel is described in the section 12.2.3. ICUSARC : Interrupt Controller Unit Security Attribution Register C.

DMASTSA bit (DMAST Security Attribution)

Security attributes of registers for DMAST. Do not write to DMASTSA bit while DMA transfer is enabled or a bus master is writing to the DMA registers.

15.2.2 DMSAR : DMA Source Address Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x00

Bit position:	31	0
Bit field:		
Value after reset:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bit	Symbol	Function	R/W
31:0	n/a	Specifies the transfer source start address Setting range is 0x00000000 to 0xFFFFFFFF (4 Gbytes).	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set DMSAR while DMAC activation is disabled (the DMAST.DMST bit = 0) or DMA transfer is disabled (the DMCNT.DTE bit = 0).

Note: Address alignment in this register must match the Transfer Data Size value selected in the DMTMD.SZ bit.

15.2 注册说明

15.2.1 DMACSAR:DMAC控制器安全属性寄存器

Base address: CPSCU = 0x4000_8000

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMASTSA
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	DMASTSA	DMAST安全归因 0: Secure 1: Non-secure	R/W
31:1	—	这些位读为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

对于DMAC，为每个通道设置安全属性。但是，该寄存器仅设置DMAST寄存器安全属性。每个通道的安全属性设置在12.2.3小节中描述。ICUSARC：中断控制器单元安全属性寄存器C。

DMASTSA位（DMAST安全属性）

DMAST寄存器的安全属性。在启用DMA传输或总线主机正在写入DMA寄存器时，不要写入DMASTSA位。

15.2.2 DMSAR：DMA源地址寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x00

Bit position:	31	0
Bit field:		
重置后的值:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bit	Symbol	Function	R/W
31:0	n/a	指定传输源起始地址 设置范围是0x00000000到0xFFFFFFFF（4GB）。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在禁用DMAC激活（DMAST.DMST位=0）或禁用DMA传输（
DMCNT.DTE bit = 0).

Note: 该寄存器中的地址对齐必须与在DMTMD.SZ位中选择的传输数据大小值相匹配。

15.2.3 DMSRR : DMA Source Reload Address Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x20

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Specifies the transfer source reload address 0x0000 0000 to 0xFFFF FFFF (4 Gbytes)	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set DMSRR while DMAC activation is disabled (DMAST.DMST = 0) or DMA transfer is disabled (DMCNT.DTE = 0).

DMSRR is initial value of DMSAR. In repeat-block transfer mode, DMSAR reloads value of DMSRR after specified transfer finished.

In normal transfer mode, repeat transfer mode and block transfer mode, DMSRR is not used. The setting is invalid.

Note: Address alignment in this register must match the Transfer Data Size value selected in the DMTMD.SZ bit.

15.2.4 DMDAR : DMA Destination Address Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x04

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Specifies the transfer destination start address setting range is 0x00000000 to 0xFFFFFFFF (4 Gbytes).	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set DMDAR while DMAC activation is disabled (the DMAST.DMST bit = 0) or DMA transfer is disabled (the DMCNT.DTE bit = 0).

Note: Address alignment in this register must match the Transfer Data Size value selected in the DMTMD.SZ bit.

15.2.3 DMSRR:DMA源重载地址寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x20

Bit position:	31																													0
Bit field:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	指定传输源重载地址0x00000000到0xFFFFF FFF(4GB)	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在禁用DMAC激活(DMAST.DMST=0)或禁用DMA传输(DMCNT.DTE=0)时设置DMSRR。

DMSRR是DMSAR的初始值。在重复块传输模式下，DMSAR在指定传输完成后重新加载DMSRR的值。

在正常传输模式、重复传输模式和块传输模式下，不使用DMSRR。设置无效。

Note: 该寄存器中的地址对齐必须与在DMTMD.SZ位中选择的传输数据大小值相匹配。

15.2.4 DMDAR:DMA目标地址寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x04

Bit position:	31																													0
Bit field:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	指定传输目标起始地址设置范围为0x00000000到0xFFFF FFFF(4GB)。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在禁用DMAC激活（DMAST.DMST位=0）或禁用DMA传输（
DMCNT.DTE bit = 0).

Note: 该寄存器中的地址对齐必须与在DMTMD.SZ位中选择的传输数据大小值相匹配。

15.2.5 DMDRR : DMA Destination Reload Address Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x24

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Specifies the transfer destination reload address 0000 0000h to FFFF FFFFh (4 Gbytes)	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set DMDRR while DMAC activation is disabled (the DMAST.DMST bit = 0) or DMA transfer is disabled (the DMCNT.DTE bit = 0).

DMDRR is initial value of DMDAR. In repeat-block transfer mode, DMDAR reloads value of DMDRR after specified transfer finished.

In normal transfer mode, repeat transfer mode and block transfer mode, DMDRR is not used. The setting is invalid.

Note: Address alignment in this register must match the Transfer Data Size value selected in the DMTMD.SZ bit.

15.2.6 DMCRA : DMA Transfer Count Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	DMCRAH[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMCRAL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMCRAL[15:0]	Lower bits of transfer count Specifies the number of transfer operations.	R/W
25:16	DMCRAH[9:0]	Upper bits of transfer count Specifies the number of transfer operations.	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set the same value for DMCRAH and DMCRAL in repeat transfer mode, block transfer mode, and repeat-block transfer mode. Bits 15 to 10 are fixed to 0 in repeat transfer mode, block transfer mode, and repeat-block transfer mode.

15.2.5 DMDRR:DMA目标重载地址寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x24

Bit position:	31																													0
Bit field:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	指定传输目标重载地址00000000h至FFFFFFFFh(4GB)	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在禁用DMAC激活（DMAST.DMST位=0）或禁用DMA传输（
DMCNT.DTE bit = 0).

DMDRR是DMDAR的初始值。在重复块传输模式下，DMDAR在指定传输完成后重新加载DMDRR的值。

在正常传输模式、重复传输模式和块传输模式下，不使用DMDRR。设置无效。

Note: 该寄存器中的地址对齐必须与在DMTMD.SZ位中选择的传输数据大小值相匹配。

15.2.6 DMCRA:DMA传输计数寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	DMCRAH[9:0]									
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMCRAL[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMCRAL[15:0]	传输计数的低位 指定传输操作的数量。	R/W
25:16	DMCRAH[9:0]	传输计数的高位 指定传输操作的数量。	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在重复传输模式、块传输模式和重复块传输模式下，为DMCRAH和DMCRAL设置相同的值。在重复传输模式、块传输模式和重复块传输模式中，位15至10固定为0。

(1) Normal Transfer Mode (DMTMD.MD[1:0] = 00b)

DMCRAL functions as a 16-bit transfer counter.

The number of transfer operations is one when the setting is 0x0001, and 65,535 when it is 0xFFFF. The value is decremented by one each time data is transferred.

When the setting is 0x0000, no specific number of transfer operations is set; data transfer is performed with the transfer counter stopped (free running function).

Free running function is not selected by DMTMD.TKP bit in normal transfer mode.

DMCRAH is not used in normal transfer mode. Write 0x0000 to DMCRAH.

(2) Repeat Transfer Mode (DMTMD.MD[1:0] = 01b)

DMCRAH specifies the repeat size and DMCRAL functions as a 10-bit transfer counter.

The number of transfer operations is one when the setting is 0x001, 1,023 when it is 0x3FF, and 1,024 when it is 0x000. In repeat transfer mode, a value in the range of 0x000 to 0x3FF (1 to 1,024) can be set for DMCRAH and DMCRAL.

Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits.

The value in DMCRAL is decremented by one each time data is transferred until it reaches 0x000, at which the value in DMCRAH is loaded into DMCRAL.

(3) Block Transfer Mode (DMTMD.MD[1:0] = 10b)

DMCRAH specifies the block size and DMCRAL functions as a 10-bit block size counter.

The block size is one when the setting is 0x001, 1,023 when it is 0x3FF, and 1,024 when it is 0x000. In block transfer mode, a value in the range of 0x000 to 0x3FF can be set for DMCRAH and DMCRAL.

Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits.

The value in DMCRAL is decremented by one each time data is transferred until it reaches 0x000, at which the value in DMCRAH is loaded into DMCRAL.

(4) Repeat-Block Transfer Mode (DMTMD.MD[1:0] = 11b)

DMCRAH specifies the block size and DMCRAL functions as a 10-bit block size counter.

The block size is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h. In repeat-block transfer mode, a value in the range of 000h to 3FFh can be set for DMCRAH and DMCRAL.

Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits.

The value in DMCRAL is decremented by one each time data is transferred until it reaches 000h, at which the value in DMCRAH is loaded into DMCRAL.

15.2.7 DMCRB : DMA Block Transfer Count Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMCRBH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMCRBL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) 正常传输模式（DMTMD.MD[1:0]=00b）

DMCRAL用作16位传输计数器。

设置为0x0001时传输操作数为1，设置为0xFFFF时为65 535。每次传输数据时，该值减一。

设置为0x0000时，不设置具体的传输操作次数；在传输计数器停止的情况下执行数据传输（自由运行功能）。

在正常传输模式下，DMMTD.TKP位不选择自由运行功能。

DMCRAH不用于正常传输模式。将0x0000写入DMCRAH。

(2) 重复传输模式(DMTMD.MD[1:0]=01b)

DMCRAH指定重复大小，DMCRAL用作10位传输计数器。

设置为0x001时传输操作数为1，设置为0x3FF时为1 023，设置为0x000时为1 024。在重复传输模式下，可以为DMCRAH和DMCRAL设置0x000到0x3FF（1到1 024）范围内的值。

在DMCRAL中设置位15至10无效。将0写入这些位。

每次传输数据时，DMCRAL中的值减1，直到到达0x000，此时DMCRAL中的值DMCRAH被加载到DMCRAL中。

(3) 块传输模式（DMTMD.MD[1:0]=10b）

DMCRAH指定块大小，DMCRAL用作10位块大小计数器。

设置为0x001时块大小为1，设置为0x3FF时为1 023，设置为0x000时为1 024。在块传输模式下，可以为DMCRAH和DMCRAL设置0x000到0x3FF范围内的值。

在DMCRAL中设置位15至10无效。将0写入这些位。

每次传输数据时，DMCRAL中的值减1，直到到达0x000，此时DMCRAL中的值DMCRAH被加载到DMCRAL中。

(4) 重复块传输模式(DMTMD.MD[1:0]=11b)

DMCRAH指定块大小，DMCRAL用作10位块大小计数器。

设置为001h时块大小为1，设置为3FFh时为1023，设置为000h时为1024。在重复块传输模式下，可以为DMCRAH和DMCRAL设置000h到3FFh范围内的值。

在DMCRAL中设置位15至10无效。将0写入这些位。

每次传输数据时，DMCRAL中的值减1，直到达到000h，此时DMCRAL中的值DMCRAH被加载到DMCRAL中。

15.2.7 DMCRB:DMA块传输计数寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMCRBH[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMCRBL[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMCRBL[15:0]	Functions as a number of block, repeat or repeat-block transfer counter. 0001h to FFFFh (1 to 65,535) 0000h (65,536)	R/W
31:16	DMCRBH[15:0]	Specifies the number of block, repeat or repeat-block transfer operations. 0001h to FFFFh (1 to 65,535) 0000h (65,536)	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set the same value for DMCRBH and DMCRBL in repeat transfer mode, block transfer mode and repeat-block transfer mode.

DMCRBH specifies the number of block, repeat and repeat-block transfer operations, and DMCRBL functions as a 16-bit the number of block counter in block, repeat, repeat-block transfer mode, respectively.

The number of transfer operations is one when the setting is 0001h, 65,535 when it is FFFFh, and 65,536 when it is 0000h.

In repeat transfer mode, the value is decremented by one when the final data of one repeat size is transferred.

In block transfer mode and repeat-block transfer mode, the value is decremented by one when the final data of one block size is transferred.

In normal transfer mode, DMCRB is not used. The setting is invalid.

When DMTMD.TKP is 1 and final data of one repeat size or one block size is transferred, DMCRBL reloads value of DMCRBH automatically.

15.2.8 DMTMD : DMA Transfer Mode Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MD[1:0]		DTS[1:0]		—	TKP	SZ[1:0]		—	—	—	—	—	—	DCTG[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	DCTG[1:0]	Transfer Request Source Select 0 0: Software request 0 1: Hardware request*1 1 0: Setting prohibited 1 1: Setting prohibited	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
9:8	SZ[1:0]	Transfer Data Size Select 0 0: 8 bits 0 1: 16 bits 1 0: 32 bits 1 1: Setting prohibited	R/W
10	TKP	Transfer Keeping 0: Transfer is stopped by completion of specified total number of transfer operations. 1: Transfer is not stopped by completion of specified total number of transfer operations. (free-running)	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
15:0	DMCRBL[15:0]	用作多个块、重复或重复块传输计数器。0001h至FFFFh(1至65 535)000 0h(65 536)	R/W
31:16	DMCRBH[15:0]	指定块、重复或重复块传输操作的数量。0001h至FFFFh(1至65 535)0000 h(65 536)	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在重复传输模式、块传输模式和重复块传输模式中，将DMCRBH和DMCRBL设置为相同的值。

DMCRBH指定块、重复和重复块传输操作的数量，DMCRBL分别用作块、重复、重复块传输模式下的16位块数计数器。

设置为0001h时传输操作数为1，设置为FFFFh时为65 535，设置为0000h时为65 536。

在重复传输模式下，当传输一个重复大小的最终数据时，该值减一。

在块传输模式和重复块传输模式中，当传输一个块大小的最终数据时，该值减一。

在正常传输模式下，不使用DMCRB。设置无效。

当DMTMD.TKP为1并且传输一个重复大小或一个块大小的最终数据时，DMCRBL重新加载值DMCRBH automatically.

15.2.8 DMTMD:DMA传输模式寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MD[1:0]		DTS[1:0]		—	TKP	SZ[1:0]		—	—	—	—	—	—	DCTG[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	DCTG[1:0]	传输请求源选择 00：软件请求01：硬件请求*1 10：禁止设置11：禁止设置	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
9:8	SZ[1:0]	传输数据大小选择 00：8位01：16位10：32位11：禁止设置	R/W
10	TKP	转让保管 0：完成指定的传输操作总数后停止传输。1：完成指定的传输操作总数后传输不会停止。（自由奔跑）	R/W
11	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
13:12	DTS[1:0]	Repeat Area Select 0 0: The destination is specified as the repeat area or block area 0 1: The source is specified as the repeat area or block area 1 0: The repeat area or block area is not specified 1 1: Setting prohibited	R/W
15:14	MD[1:0]	Transfer Mode Select 0 0: Normal transfer 0 1: Repeat transfer 1 0: Block transfer 1 1: Repeat-block transfer	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. To select the DMAC activation source, use the DELSRn registers of the ICU. For details on DMAC activation sources, see Table 12.4 in section 12, Interrupt Controller Unit (ICU).

DTS[1:0] bits (Repeat Area Select)

DTS[1:0] select either the source or destination as the repeat area in repeat or block transfer mode. In normal or repeat-block transfer mode, setting these bits is invalid.

TKP bits (Transfer Keeping)

TKP selects either stopping transfer or keeping transfer by completion of specified total number of transfer operations in repeat, block or repeat-block transfer mode. In normal transfer mode, setting these bits is invalid.

15.2.9 DMINT : DMA Interrupt Setting Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DTIE	ESIE	RPTIE	SARIE	DARIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DARIE	Destination Address Extended Repeat Area Overflow Interrupt Enable 0: Disables an interrupt request for an extended repeat area overflow on the destination address 1: Enables an interrupt request for an extended repeat area overflow on the destination address	R/W
1	SARIE	Source Address Extended Repeat Area Overflow Interrupt Enable 0: Disables an interrupt request for an extended repeat area overflow on the source address 1: Enables an interrupt request for an extended repeat area overflow on the source address	R/W
2	RPTIE	Repeat Size End Interrupt Enable 0: Disables the repeat size end interrupt request 1: Enables the repeat size end interrupt request	R/W
3	ESIE	Transfer Escape End Interrupt Enable 0: Disables the transfer escape end interrupt request 1: Enables the transfer escape end interrupt request	R/W
4	DTIE	Transfer End Interrupt Enable 0: Disables the transfer end interrupt request 1: Enables the transfer end interrupt request	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:

Bit	Symbol	Function	R/W
13:12	DTS[1:0]	重复区域选择 00：目标指定为重复区域或块区域01：源指定为重复区域或块区域10：不指定重复区域或块区域11：设置禁止	R/W
15:14	MD[1:0]	传输模式选择 00：正常传输01：重复传输10：块传输11：重复块传输	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.要选择DMAC激活源，请使用ICU的DELSRn寄存器。有关DMAC激活源的详细信息，请参见第12节“中断控制器单元(ICU)”中的表12.4。

DTS[1:0]位（重复区域选择）

DTS[1:0]在重复或块传输模式中选择源或目标作为重复区域。在正常或重复块传输模式下，设置这些位无效。

TKP bits (Transfer Keeping)

TKP通过在重复、块或重复块传输模式下完成指定的传输操作总数来选择停止传输或保持传输。在正常传输模式下，设置这些位无效。

15.2.9 DMINT:DMA中断设置寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DTIE	ESIE	RPTIE	SARIE	DARIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DARIE	目标地址扩展重复区溢出中断使能 0：禁用目标地址上扩展重复区域溢出的中断请求 1：使能目标地址上扩展重复区域溢出的中断请求	R/W
1	SARIE	源地址扩展重复区溢出中断使能 0：禁用源地址上扩展重复区域溢出的中断请求 1：使能源地址上扩展重复区域溢出的中断请求	R/W
2	RPTIE	重复大小结束中断使能 0：禁用重复大小结束中断请求1：启用重复大小结束中断请求	R/W
3	ESIE	传输转义结束中断使能 0：禁用传输转义结束中断请求1：启用传输转义结束中断请求	R/W
4	DTIE	传输结束中断使能 0：禁止传输结束中断请求1：允许传输结束中断请求	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

DARIE bit (Destination Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow on the destination address occurs while DARIE bit is set to 1, the DMCNT.DTE bit is cleared to 0. At the same time, the DMSTS.ESIF flag is set to 1 to indicate that an interrupt by an extended repeat area overflow on the destination address is requested.

When block transfer mode is used with the extended repeat area function, an interrupt is requested after completion of a 1-block size transfer. When setting 1 in the DMCNT.DTE bit of the channel for which a transfer has been stopped, the transfer is resumed from the state when the transfer is stopped.

When the extended repeat area is not specified for the destination address, this bit is ignored.

When set to repeat-block transfer mode, do not use this bit.

SARIE bit (Source Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow on the source address occurs while SARIE bit is set to 1, the DMCNT.DTE bit is cleared to 0. At the same time, the DMSTS.ESIF flag is set to 1 to indicate that an interrupt by an extended repeat area overflow on the source address is requested.

When block transfer mode is used with the extended repeat area function, an interrupt is requested after completion of a 1-block size transfer. When setting 1 in the DMCNT.DTE bit of the channel for which a transfer has been stopped, the transfer is resumed from the state when the transfer is stopped.

When the extended repeat area is not specified for the source address, this bit is ignored.

When set to repeat-block transfer mode, do not use this bit.

RPTIE bit (Repeat Size End Interrupt Enable)

When RPTIE bit is set to 1 in repeat transfer mode, the DMCNT.DTE bit is cleared to 0 after completion of a 1-repeat size data transfer. At the same time, the DMSTS.ESIF flag is set to 1 to indicate that the repeat size end interrupt request has been generated. The repeat size end interrupt request can be generated even when the DMTMD.DTS[1:0] bits are 10b (= repeat area or block area is not specified).

When this bit is set to 1 in block transfer mode, the DMCNT.DTE bit is cleared to 0 after completion of a 1-block data transfer in the same way as repeat transfer mode. At the same time, the DMSTS.ESIF flag is set to 1 to indicate that the repeat size end interrupt request has been generated. The repeat size end interrupt request can be generated even when the DMTMD.DTS[1:0] bits are 10b (= repeat area or block area is not specified).

When set to repeat-block transfer mode, do not use this bit.

ESIE bit (Transfer Escape End Interrupt Enable)

ESIE bit enables or disables the transfer escape end interrupt requests (repeat size end interrupt request and extended repeat area overflow interrupt request) that are generated during DMA transfer.

The transfer escape end interrupt is generated when the DMSTS.ESIF flag is set to 1 with this bit set to 1. The transfer escape end interrupt is cleared by clearing this bit or the DMSTS.ESIF flag to 0.

DTIE bit (Transfer End Interrupt Enable)

DTIE bit enables or disables the transfer end interrupt request to be generated on completion of a specified number of data transfers.

The transfer end interrupt is generated when the DMSTS.DTIF flag is set to 1 with this bit set to 1. The transfer end interrupt is cleared by clearing this bit or the DMSTS.DTIF flag to 0.

- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●

允许安全和非安全访问。

DARIE位（目标地址扩展重复区域溢出中断允许）

当DARIE位设置为1时，当目标地址发生扩展重复区域溢出时，DMCNT.DTE位清零。同时，DMSTS.ESIF标志位设置为1，表示由请求目标地址上的扩展重复区域溢出。

当块传输模式与扩展重复区域功能一起使用时，在完成1块大小的传输后请求中断。将停止传输的通道的DMCNT.DTE位设置为1时，将从停止传输时的状态恢复传输。

当没有为目标地址指定扩展重复区域时，该位被忽略。

当设置为重复块传输模式时，不要使用该位。

SARIE位（源地址扩展重复区溢出中断使能）

当SARIE位被设置为1时，当源地址发生扩展重复区域溢出时，DMCNT.DTE位被清除为0。同时，DMSTS.ESIF标志被设置为1，表示由请求源地址上的扩展重复区域溢出。

当块传输模式与扩展重复区域功能一起使用时，在完成1块大小的传输后请求中断。将停止传输的通道的DMCNT.DTE位设置为1时，将从停止传输时的状态恢复传输。

当源地址没有指定扩展重复区域时，该位被忽略。

当设置为重复块传输模式时，不要使用该位。

RPTIE位（重复大小结束中断允许）

当RPTIE位在重复传输模式下设置为1时，DMCNT.DTE位在完成1次重复大小的数据传输后被清除为0。同时，将DMSTS.ESIF标志设置为1，表示已产生重复大小结束中断请求。即使DMTMD.DTS[1:0]位为10b（=未指定重复区域或块区域），也可以生成重复大小结束中断请求。

当该位在块传输模式下设置为1时，DMCNT.DTE位在完成1块数据传输后清零，方法与重复传输模式相同。同时，将DMSTS.ESIF标志设置为1，表示已产生重复大小结束中断请求。即使DMTMD.DTS[1:0]位为10b（=未指定重复区域或块区域），也可以生成重复大小结束中断请求。

当设置为重复块传输模式时，不要使用该位。

ESIE位（传输转义结束中断使能）

ESIE位启用或禁用在DMA传输期间产生的传输转义结束中断请求（重复大小结束中断请求和扩展重复区域溢出中断请求）。

当DMSTS.ESIF标志设置为1且该位设置为1时，将产生传输转义结束中断。通过清除该位或DMSTS.ESIF标志为0来清除传输转义结束中断。

DTIE位（传输结束中断允许）

DTIE位启用或禁用在完成指定数量的数据传输时生成的传输结束中断请求。

当DMSTS.DTIF标志设置为1且该位设置为1时，将产生传输结束中断。通过清除该位或DMSTS.DTIF标志为0来清除传输结束中断。

15.2.10 DMAMD : DMA Address Mode Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SM[1:0]		SADR	SARA[4:0]					DM[1:0]		DADR	DARA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DARA[4:0]	Destination Address Extended Repeat Area Specifies the extended repeat area on the destination address. For details on the settings, see Table 15.2.	R/W
5	DADR	Destination Address Update Select After Reload 0: Only reloading 1: Add index after reloading	R/W
7:6	DM[1:0]	Destination Address Update Mode 0 0: Destination address is fixed 0 1: Offset addition 1 0: Destination address is incremented 1 1: Destination address is decremented	R/W
12:8	SARA[4:0]	Source Address Extended Repeat Area Specifies the extended repeat area on the source address. For details on the settings, see Table 15.2.	R/W
13	SADR	Source Address Update Select After Reload 0: Only reloading 1: Add index after reloading	R/W
15:14	SM[1:0]	Source Address Update Mode 0 0: Source address is fixed 0 1: Offset addition 1 0: Source address is incremented 1 1: Source address is decremented	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

DARA[4:0] bits (Destination Address Extended Repeat Area)

DARA[4:0] bits specify the extended repeat area on the destination address. The extended repeat area function is realized by updating the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of two between 2 bytes and 128 Mbytes.

When the lower address overflows the extended repeat area by address increment, the start address of the extended repeat area is set. Similarly, when the lower address underflows the extended repeat area by address decrement, the end address of the extended repeat area is set.

When the repeat area or block area is specified as a transfer destination, do not specify the extended repeat area on the destination address. When repeat transfer or block transfer is selected, and when DMTMD.DTS[1:0] = 00b (the transfer destination is specified as the repeat area or block area), write 00000b in the DARA[4:0] bits.

In repeat-block transfer mode, write 00000b in the DARA[4:0] bits.

An interrupt can be requested when an overflow or underflow occurs in the extended repeat area with the DMINT.DARIE bit set to 1. Table 15.2 lists the settings and the corresponding extended repeat areas.

DADR bits (Destination Address Update Select After Reload)

In repeat-block transfer mode, this bit specifies the behavior of DMDAR after reloading DMDRR.

When this bit is set to 1, an index value ((DMDBSH-DMDBSL) × DataSize) is added to DMDAR after reloading DMDRR.

15.2.10 DMAMD:DMA地址模式寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SM[1:0]		SADR	SARA[4:0]					DM[1:0]		DADR	DARA[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DARA[4:0]	目标地址扩展重复区域 指定目标地址上的扩展重复区域。有关设置的详细信息，请参见表15.2。	R/W
5	DADR	重新加载后目标地址更新选择 0：仅重新加载1：重新加载 后添加索引	R/W
7:6	DM[1:0]	目的地址更新模式 00：目标地址固定01：偏移量加法10： 目标地址递增11：目标地址递减	R/W
12:8	SARA[4:0]	源地址扩展重复区 指定源地址上的扩展重复区域。有关设置的详细信息，请参阅 Table 15.2.	R/W
13	SADR	重新加载后源地址更新选择 0：仅重新加载1：重新加载 后添加索引	R/W
15:14	SM[1:0]	源地址更新模式 00：源地址固定01：偏移量加法10： 源地址递增11：源地址递减	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

DARA[4:0]位（目标地址扩展重复区）

DARA[4:0]位指定目标地址上的扩展重复区域。扩展重复区功能是通过更新指定的低地址位来实现的，剩余的高地址位是固定的。扩展重复区域的大小可以是2字节到128MB之间的任意2次幂。

当低位地址以地址增量溢出扩展重复区域时，设置扩展重复区域的起始地址。类似地，当低位地址通过地址减量使扩展重复区域下溢时，设置扩展重复区域的结束地址。

将重复区域或块区域指定为传输目标时，请勿在目标地址上指定扩展重复区域。选择重复传输或块传输时，并且当DMTMD.DTS[1:0]=00b（传输目标指定为重复区域或块区域）时，将00000b写入DARA[4:0]位。

在重复块传输模式下，将00000b写入DARA[4:0]位。

当DMINT.DARIE位设置为1的扩展重复区域发生上溢或下溢时，可以请求中断。表15.2列出了设置和相应的扩展重复区域。

DADR位（重载后目标地址更新选择）

在重复块传输模式下，该位指定重新加载DMDRR后DMDAR的行为。

当该位设置为1时，在重新加载DMDRR后将索引值((DMDBSH-DMDBSL)×DataSize)添加到DMDAR。

When this bit is set to 0, DMDAR only reloads DMDRR. This behavior is described in Table 15.13.

In normal, repeat or block transfer mode, this bit is ignored.

DM[1:0] bits (Destination Address Update Mode)

DM[1:0] bits select the mode of updating the destination address.

When increment is selected and the DMTMD.SZ[1:0] bits are set to 00b, 01b, and 10b, the destination address is incremented by 1, 2, and 4, respectively.

When decrement is selected and the DMTMD.SZ[1:0] bits are set to 00b, 01b, and 10b, the destination address is decremented by 1, 2, and 4, respectively.

When offset addition is selected, the offset specified by the DMOFR register is added to the address.

SARA[4:0] bits (Source Address Extended Repeat Area)

SARA[4:0] bits specify the extended repeat area on the source address. The extended repeat area function is realized by updating the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of two between 2 bytes and 128 Mbytes.

When the lower address overflows the extended repeat area by address increment, the start address of the extended repeat area is set. Similarly, when the lower address underflows the extended repeat area by address decrement, the end address of the extended repeat area is set.

When the repeat area or block area is specified as a transfer source, do not specify the extended repeat area on the source address. When repeat transfer or block transfer is selected, and when DMTMD.DTS[1:0] = 01b (the transfer source is specified as the repeat area or block area), write 00000b in the SARA[4:0] bits.

In repeat-block transfer mode, write 00000b in the SARA[4:0] bits.

An interrupt can be requested when an overflow or underflow occurs in the extended repeat area with the DMINT.SARIE bit set to 1. Table 15.2 lists the settings and the corresponding extended repeat areas.

SADR bits (Source Address Update Select After Reload)

In repeat-block transfer mode, this bit specifies the behavior of DMSAR after reloading DMSRR.

When this bit is set to 1, an index value ((DMSBSH-DMSBSL) × DataSize) is added to DMSAR after reloading DMSRR.

When this bit is set to 0, DMSAR only reloads DMSRR. This behavior is described in Table 15.12.

In normal, repeat or block transfer mode, this bit is ignored.

SM[1:0] bits (Source Address Update Mode)

SM[1:0] bits select the mode of updating the source address.

When increment is selected and the DMTMD.SZ[1:0] bits are set to 00b, 01b, and 10b, the source address is incremented by 1, 2, and 4, respectively.

When decrement is selected and the DMTMD.SZ[1:0] bits are set to 00b, 01b, and 10b, the source address is decremented by 1, 2, and 4, respectively.

When offset addition is selected, the offset specified by the DMOFR register is added to the address.

Table 15.2 SARA[4:0] or DARA[4:0] Settings and Corresponding Repeat Areas (1 of 2)

SARA[4:0] or DARA[4:0] Settings and Corresponding Repeat Areas	Extended Repeat Area
00000b	Not specified
00001b	2 bytes specified as extended repeat area by the lower 1 bit of the address
00010b	4 bytes specified as extended repeat area by the lower 2 bits of the address
00011b	8 bytes specified as extended repeat area by the lower 3 bits of the address
00100b	16 bytes specified as extended repeat area by the lower 4 bits of the address
00101b	32 bytes specified as extended repeat area by the lower 5 bits of the address
00110b	64 bytes specified as extended repeat area by the lower 6 bits of the address

当该位设置为0时，DMDAR仅重新加载DMDRR。这种行为在表15.13中描述。

在正常、重复或块传输模式下，该位被忽略。

DM[1:0]位（目标地址更新模式）

DM[1:0]位选择更新目标地址的模式。

Whenincrementisselectedandthe DMTMD.SZ[1:0]bitsaresetto00b 01b and10b thedestinationaddressis incrementedby1 2 and4 respectively.

WhendecrementisselectedandtheDMTMD.SZ[1:0]bitsaresetto00b 01b and10b thedestinationaddressis decrementedby1 2 and4 respectively.

选择偏移添加后，将DMOFR寄存器指定的偏移添加到地址中。

SARA[4:0]位（源地址扩展重复区）

SARA[4:0]位指定源地址上的扩展重复区域。扩展重复区功能是通过更新指定的低地址位来实现的，剩余的高地址位是固定的。扩展重复区域的大小可以是2字节到128MB之间的任意2次幂。

当低位地址以地址增量溢出扩展重复区域时，设置扩展重复区域的起始地址。类似地，当低位地址通过地址减量使扩展重复区域下溢时，设置扩展重复区域的结束地址。

当重复区域或块区域被指定为传输源时，不要在源地址上指定扩展重复区域。Whenrepeattransferorblocktransferisselected andwhenDMTMD.DTS[1:0]=01b(thetransfersourceisspecifiedastherepeatareaorblockarea) write 00000bintheSARA[4:0]bits.

在重复块传输模式下，将00000b写入SARA[4:0]位。

当DMINT.SARIE位设置为1的扩展重复区域发生上溢或下溢时，可以请求中断。表15.2列出了设置和相应的扩展重复区域。

SADR位（重载后源地址更新选择）

在重复块传输模式下，该位指定重新加载DMSRR后DMSAR的行为。

当该位设置为1时，在重新加载DMSRR后将索引值((DMSBSH−DMSBSL)×DataSize)添加到DMSAR。

当该位设置为0时，DMSAR仅重新加载DMSRR。这种行为在表15.12中描述。

在正常、重复或块传输模式下，该位被忽略。

SM[1:0]位（源地址更新模式）

SM[1:0]位选择更新源地址的模式。

WhenincrementisselectedandtheDMTMD.SZ[1:0]bitsaresetto00b 01b and10b thesourceaddressisincrementedby 1 2 and4 respectively.

WhendecrementisselectedandtheDMTMD.SZ[1:0]bitsaresetto00b 01b and10b thesourceaddressisdecremente dby1 2 and4 respectively.

选择偏移添加后，将DMOFR寄存器指定的偏移添加到地址中。

Table 15.2 SARA[4:0]或DARA[4:0]设置和对应的重复区域(1of2)

SARA[4:0]或DARA[4:0]设置和对应的重复区域	扩展重复区域
00000b	未指定
00001b	由地址的低1位指定为扩展重复区域的2个字节
00010b	由地址的低2位指定为扩展重复区域的4个字节
00011b	由地址的低3位指定为扩展重复区域的8个字节
00100b	由地址的低4位指定为扩展重复区域的16个字节
00101b	由地址的低5位指定为扩展重复区域的32个字节
00110b	由地址的低6位指定为扩展重复区域的64个字节

Table 15.2 SARA[4:0] or DARA[4:0] Settings and Corresponding Repeat Areas (2 of 2)

SARA[4:0] or DARA[4:0] Settings and Corresponding Repeat Areas	Extended Repeat Area
00111b	128 bytes specified as extended repeat area by the lower 7 bits of the address
01000b	256 bytes specified as extended repeat area by the lower 8 bits of the address
01001b	512 bytes specified as extended repeat area by the lower 9 bits of the address
01010b	1 Kbyte specified as extended repeat area by the lower 10 bits of the address
01011b	2 Kbytes specified as extended repeat area by the lower 11 bits of the address
01100b	4 Kbytes specified as extended repeat area by the lower 12 bits of the address
01101b	8 Kbytes specified as extended repeat area by the lower 13 bits of the address
01110b	16 Kbytes specified as extended repeat area by the lower 14 bits of the address
01111b	32 Kbytes specified as extended repeat area by the lower 15 bits of the address
10000b	64 Kbytes specified as extended repeat area by the lower 16 bits of the address
10001b	128 Kbytes specified as extended repeat area by the lower 17 bits of the address
10010b	256 Kbytes specified as extended repeat area by the lower 18 bits of the address
10011b	512 Kbytes specified as extended repeat area by the lower 19 bits of the address
10100b	1 Mbyte specified as extended repeat area by the lower 20 bits of the address
10101b	2 Mbytes specified as extended repeat area by the lower 21 bits of the address
10110b	4 Mbytes specified as extended repeat area by the lower 22 bits of the address
10111b	8 Mbytes specified as extended repeat area by the lower 23 bits of the address
11000b	16 Mbytes specified as extended repeat area by the lower 24 bits of the address
11001b	32 Mbytes specified as extended repeat area by the lower 25 bits of the address
11010b	64 Mbytes specified as extended repeat area by the lower 26 bits of the address
11011b	128 Mbytes specified as extended repeat area by the lower 27 bits of the address
11100b to 11111b	Setting prohibited.

15.2.11 DMOFR : DMA Offset Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x18

Bit position: 31 ... 0

Bit field:

Value after reset: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
31:0	n/a	Specifies the offset when offset addition is selected as the address update mode for transfer source or destination 0x00000000 to 0x00FFFFFF (0 bytes to (16 M – 1) bytes) 0xFF000000 to 0xFFFFFFFF (–16 Mbytes to –1 byte)	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Write to this register while the DMAC operation is stopped or DMA transfer is disabled (not during data transfer).

Setting bits 31 to 25 is invalid; a value of bit 24 is extended to bits 31 to 25. Reading DMOFR returns the extended value.

In repeat-block transfer mode, the offset is not specified by DMOFR when offset addition is selected, write 0 to DMOFR.

Table 15.2 SARA[4:0]或DARA[4:0]设置和对应的重复区域(2of2)

SARA[4:0]或DARA[4:0]设置和对应的重复区域	扩展重复区域
00111b	由地址的低7位指定为扩展重复区域的128个字节
01000b	由地址的低8位指定为扩展重复区域的256个字节
01001b	由地址的低9位指定为扩展重复区域的512个字节
01010b	1KB由地址的低10位指定为扩展重复区域
01011b	2KB由地址的低11位指定为扩展重复区域
01100b	由地址的低12位指定为扩展重复区域的4KB
01101b	8KB由地址的低13位指定为扩展重复区域
01110b	16KB由地址的低14位指定为扩展重复区域
01111b	32KB由地址的低15位指定为扩展重复区域
10000b	64KB由地址的低16位指定为扩展重复区域
10001b	128KB由地址的低17位指定为扩展重复区域
10010b	256KB由地址的低18位指定为扩展重复区域
10011b	512KB由地址的低19位指定为扩展重复区域
10100b	1MB由地址的低20位指定为扩展重复区域
10101b	2MB由地址的低21位指定为扩展重复区域
10110b	4MB由地址的低22位指定为扩展重复区域
10111b	8MB由地址的低23位指定为扩展重复区域
11000b	16MB由地址的低24位指定为扩展重复区域
11001b	32MB由地址的低25位指定为扩展重复区域
11010b	64MB由地址的低26位指定为扩展重复区域
11011b	128MB由地址的低27位指定为扩展重复区域
11100b to 11111b	禁止设置。

15.2.11 DMOFR:DMA偏移寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x18

Bit position: 31 ... 0

Bit field:

重置后的值: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
31:0	n/a	Specifiestheoffsetwhenoffsetadditionisselectedastheaddressupdatemodefortransfersource ordestination0x00000000to0x00FFFFFF(0bytesto(16M 1)bytes)0xFF000000to0xFFFFFFFF(16Mbytesto 1byte)	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在DMAC操作停止或禁用DMA传输时（不是在数据传输期间）写入该寄存器。

设置位31到25无效；位24的值扩展到位31到25。读取DMOFR将返回扩展值。

Inrepeat-blocktransfermode theoffsetisnotspecifiedbyDMOFRwhenoffsetadditionisselected write0toDMOFR.

15.2.12 DMCNT : DMA Transfer Enable Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DTE	DMA Transfer Enable 0: Disables DMA transfer 1: Enables DMA transfer	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

DTE bit (DMA Transfer Enable)

When the DMAST.DMST bit is set to 1 (DMAC activation is enabled) and this bit is set to 1 (DMA transfer is enabled), DMA transfer can be started for the corresponding channel.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

- When 0 is written to this bit.
- When the specified total volume of data transfer is completed.
- When DMA transfer is stopped by the repeat size end interrupt.
- When DMA transfer is stopped by the extended repeat area overflow interrupt.
- When DMA transfer is stopped by the access error occurs. Refer to section 15.5. Processing on DMA Transfer Error.

15.2.13 DMREQ : DMA Software Start Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	CLRS	—	—	—	SWREQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SWREQ	DMA Software Start 0: DMA transfer is not requested 1: DMA transfer is requested	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	CLRS	DMA Software Start Bit Auto Clear Select 0: SWREQ bit is cleared after DMA transfer is started by software 1: SWREQ bit is not cleared after DMA transfer is started by software	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:

15.2.12 DMCNT：DMA传输使能寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DTE	DMA传输使能 0：禁用DMA传输1：启用DMA传输	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

DTE位（DMA传输使能）

当DMAST.DMST位设置为1（启用DMAC激活）并且该位设置为1（启用DMA传输）时，可以为相应的通道启动DMA传输。

[Setting condition]

●向该位写入1时。

[Clearing conditions]

●当0写入该位时。
●当指定的总数据传输量完成时。
●当DMA传输因重复大小结束中断而停止时。
●当DMA传输因扩展重复区域溢出中断而停止时。
●DMA传输因访问错误而停止时。请参阅第15.5节。处理DMA传输错误。

15.2.13 DMREQ:DMA软件启动寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	CLRS	—	—	—	SWREQ
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SWREQ	DMA软件启动 0：不请求DMA传输1：请求DMA传输	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
4	CLRS	DMA软件起始位自动清除选择 0：软件启动DMA传输后SWREQ位清零1：软件启动DMA传输后SWREQ位不清零	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

SWREQ bit (DMA Software Start)

When 1 is written to SWREQ bit, a DMA transfer request is generated. After DMA transfer is started in response to the request, this bit is cleared to 0 if the CLRS bit is set to 0. This bit is not cleared to 0 while the CLRS bit is set to 1. In this case, a DMA transfer request can be issued again after completion of a transfer.

Note that, however, setting this bit is valid and DMA transfer by software is enabled only when the DMTMD.DCTG[1:0] bits are set to 00b (DMAC activation source is software).

Setting this bit is invalid when the DMTMD.DCTG[1:0] bits are set to a value other than 00b.

To start DMA transfer by software with the CLRS bit being 0, ensure that the SWREQ bit is 0, and then write 1 to the SWREQ bit.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

- When a DMA transfer request by software is accepted and DMA transfer is started while the CLRS bit is set to 0 (the SWREQ bit is cleared after DMA transfer is started by software).
- When 0 is written to this bit.

CLRS bit (DMA Software Start Bit Auto Clear Select)

CLRS bit specifies whether to clear the SWREQ bit to 0 after DMA transfer is started in response to the DMA transfer request generated by setting the SWREQ bit to 1. With this bit set to 0, the SWREQ bit is cleared to 0 after DMA transfer is started. With this bit set to 1, the SWREQ bit is not cleared to 0. In this case, a DMA transfer request can be issued again after completion of a transfer.

15.2.14 DMSTS : DMA Status Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ACT	—	—	DTIF	—	—	—	ESIF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESIF	Transfer Escape End Interrupt Flag 0: A transfer escape end interrupt has not been generated 1: A transfer escape end interrupt has been generated	R/W*1
3:1	—	These bits are read as 0. The write value should be 0.	R
4	DTIF	Transfer End Interrupt Flag 0: A transfer end interrupt has not been generated 1: A transfer end interrupt has been generated	R/W*1
6:5	—	These bits are read as 0. The write value should be 0.	R
7	ACT	DMAC Active Flag 0: DMAC is in the idle state 1: DMAC is operating	R

Note: If the security attribution is configured as secure:

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●

允许安全和非安全访问。

SWREQ位（DMA软件启动）

当SWREQ位写入1时，会产生DMA传输请求。响应请求启动DMA传输后，如果CLRS位设置为0，则该位清零。当CLRS位设置为1时，该位不清零。在这种情况下，DMA传输请求转让完成后可再次发行。

但是请注意，设置该位有效，并且仅当DMTMD.DCTG[1:0]位设置为00b（DMAC激活源为软件）时，才启用软件进行的DMA传输。

当DMTMD.DCTG[1:0]位设置为00b以外的值时，设置该位无效。

软件启动DMA传输时CLRS位为0，确保SWREQ位为0，然后将1写入
SWREQ bit.

[Setting condition]

●向该位写入1时。

[Clearing conditions]

●当CLRS位设置为0（软件启动DMA传输后SWREQ位清零）时，接受软件的DMA传输请求并启动DMA传输。

●当0写入该位时。

CLRS位（DMA软件起始位自动清除选择）

CLRS位指定在DMA传输开始后是否将SWREQ位清除为0，以响应通过将SWREQ位设置为1产生的DMA传输请求。当该位设置为0时，在DMA传输完成后SWREQ位被清除为0开始了。该位设置为1时，SWREQ位不会被清除为0。在这种情况下，可以在传输完成后再次发出DMA传输请求。

15.2.14 DMSTS:DMA状态寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ACT	—	—	DTIF	—	—	—	ESIF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESIF	传输转义结束中断标志 0：未产生传输转义结束中断1：已产生传输转义结束中断	R/W*1
3:1	—	这些位被读取为0。写入值应为0。	R
4	DTIF	传输结束中断标志 0：未产生传输结束中断1：已产生传输结束中断	R/W*1
6:5	—	这些位被读取为0。写入值应为0。	R
7	ACT	DMAC活动标志 0：DMAC处于空闲状态1： DMAC正在运行	R

Note: 如果安全属性配置为安全：●

允许安全访问和非安全读取访问

- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●

允许安全和非安全访问。

Note 1. Only 0 can be written to clear the flag.

ESIF flag (Transfer Escape End Interrupt Flag)

This flag indicates that the transfer escape end interrupt has been generated.

[Setting conditions]

- When 1-repeat size data transfer is completed in repeat transfer mode with the DMINT.RPTIE bit set to 1.
- When 1-block data transfer is completed in block transfer mode with the DMINT.RPTIE bit set to 1.
- When an extended repeat area overflow on the source address occurs while the DMINT.SARIE bit is set to 1 and the DMAMD.SARA[4:0] bits are set to a value other than 00000b (extended repeat area is specified on the transfer source address)
- When an extended repeat area overflow on the destination address occurs while the DMINT.DARIE bit is set to 1 and the DMAMD.DARA[4:0] bits are set to a value other than 00000b (extended repeat area is specified on the transfer destination address)

[Clearing conditions]

- When 0 is written to this bit.
- When 1 is written to the DMCNT.DTE bit.

DTIF flag (Transfer End Interrupt Flag)

This flag indicates that the transfer end interrupt has been generated.

[Setting conditions]

- When the specified number of unit-transfers are completed in normal transfer mode (the value of DMCRAL becoming 0 on completion of transfer)
- When the specified number of repeat transfer operations are completed in repeat transfer mode (the value of DMCRBL becoming 0 on completion of transfer with DMTMD.TKP = 0 or the value of DMCRBL reloading DMCRBH with DMTMD.TKP = 1)
- When the specified number of blocks have been transferred in block transfer mode and repeat-block transfer mode (the value of DMCRBL becoming 0 on completion of transfer with DMTMD.TKP = 0 or the value of DMCRBL reloading DMCRBH with DMTMD.TKP = 1)

[Clearing conditions]

- When 0 is written to this bit
- When 1 is written to the DMCNT.DTE bit

ACT flag (DMAC Active Flag)

This flag indicates whether the DMAC is in the idle or active state.

[Setting condition]

- When the DMAC starts data transfer operation

[Clearing condition]

- When data transfer in response to one transfer request is completed

注1.只能写入0来清除标志。

ESIF标志（传输转义结束中断标志）

该标志表明传输转义结束中断已经产生。

[Setting conditions]

●当DMINT.RPTIE位设置为1在重复传输模式下完成1次重复大小的数据传输时。

●当DMINT.RPTIE位设置为1在块传输模式下完成1块数据传输时。

●当DMINT.SARIE位设置为1且DMAMD.SARA[4:0]位设置为00000b以外的值时，当源地址发生扩展重复区域溢出时（扩展重复区域在传输时指定源地址）

●当DMINT.DARIE位设置为1且DMAMD.DARA[4:0]位设置为00000b以外的值时，当目标地址发生扩展重复区域溢出时（扩展重复区域在传输时指定目的地址）

[Clearing conditions]

●当0写入该位时。

●当1写入DMCNT.DTE位时。

DTIF标志（传输结束中断标志）

该标志表示已产生传输结束中断。

[Setting conditions]

●在正常传输模式下完成指定数量的unit-transfer时（传输完成时DMCRAL的值变为0）

●当在重复传输模式下完成指定次数的重复传输操作时（DMCRBL的值在DMTMD.TKP=0的传输完成时变为0或DMCRBL的值在DMTMD.TKP=1时重新加载DMCRBH）

●当在块传输模式和重复块传输模式下传输了指定数量的块时（DMCRBL的值在传输完成时变为0且DMTMD.TKP=0或DMCRBL的值在DMTMD.TKP=1时重新加载DMCRBH）

[Clearing conditions]

●当0写入该位时

●当1写入DMCNT.DTE位时

ACT标志（DMAC活动标志）

该标志指示DMAC是处于空闲状态还是活动状态。

[Setting condition]

●DMAC开始数据传输操作时

[Clearing condition]

●当响应一个传输请求的数据传输完成时

15.2.15 DMSBS : DMA Source Buffer Size Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMSBSH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMSBSL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMSBSL[15:0]	Functions as data transfer counter in repeat-block transfer mode See Table 15.3 for available settings.	R/W
31:16	DMSBSH[15:0]	Specifies the repeat-area size in repeat-block transfer mode See Table 15.3 for available settings.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Table 15.3 Available setting for DMSBS register in repeat-block transfer mode

Source Address Update Mode (DMAMD.SM)	Transfer Data Size (DMTMD.SZ)	Available Setting for DMSBSH and DMSBSL bits
Source address is fixed (SM = 00b)	Don't care	0x0000 (DMSBS is not used)
Offset addition (SM = 01b)	8 bits (SZ = 00b)	0x0001 to 0xFFFF (1 to 65535)
	16 bits (SZ = 01b)	0x0001 to 0x7FFF (1 to 32767)
	32 bits (SZ = 10b)	0x0001 to 0x3FFF (1 to 16383)
Source address is incremented or decremented (SM = 1xb)	Don't care	0x0000 (infinite) 0x0001 to 0xFFFF (1 to 65535)

Set the same value for DMSBSH and DMSBSL in repeat-block transfer mode. Write 00000000h to DMSBS in normal, repeat and block transfer mode.

DMSBSH specifies buffer size and DMSBSL functions as a 16-bit buffer size counter in repeat-block transfer mode. In repeat-block transfer mode, source repeat area is specified by DMSBSH.

When address update mode is incremented address or decremented address, this register means the numbers of data of whole buffer. When address update mode is offset addition, this register means the numbers of data of an individual buffer. In offset addition, setting DMSBSH and DMSBSL to 0x0000 is prohibited. When final data of one buffer size is transferred, DMSBSL reloads value of DMSBSH. When address update mode is fixed address, this register is ignored. Table 15.3 shows the setting values of DMA Source Buffer Size Register corresponding to Transfer Data Size in Source Address Update Mode.

In normal, repeat and block transfer mode, DMSBS is not used. The setting is invalid.

15.2.15 DMSBS:DMA源缓冲区大小寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMSBSH[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMSBSL[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMSBSL[15:0]	在重复块传输模式中用作数据传输计数器 有关可用设置，请参见表15.3。	R/W
31:16	DMSBSH[15:0]	指定重复块传输模式下的重复区域大小 有关可用设置，请参见表15.3。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Table 15.3 重复块传输模式下DMSBS寄存器的可用设置

源地址更新模式(DMAMD.SM)	传输数据大小(DMTMD.SZ)	DMSBSH的可用设置和 DMSBSL bits
源地址是固定的（SM=00b）	不在乎	0x0000（未使用DMSBS）
偏移量加法(SM=01b)	8 bits (SZ = 00b)	0x0001 to 0xFFFF (1 to 65535)
	16 bits (SZ = 01b)	0x0001 to 0x7FFF (1 to 32767)
	32 bits (SZ = 10b)	0x0001 to 0x3FFF (1 to 16383)
源地址递增或递减(SM=1xb)	不在乎	0x0000 (infinite) 0x0001 to 0xFFFF (1 to 65535)

在重复块传输模式下为DMSBSH和DMSBSL设置相同的值。在正常、重复和块传输模式下将00000000h写入DMSBS。

DMSBSH指定缓冲区大小，DMSBSL用作重复块传输模式下的16位缓冲区大小计数器。在重复块传输模式下，源重复区域由DMSBSH指定。

当地址更新模式为递增地址或递减地址时，该寄存器表示整个缓冲区的数据个数。当地址更新模式为偏移加法时，该寄存器表示单个缓冲区的数据个数。此外，禁止将DMSBSH和DMSBSL设置为0x0000。当传输一个缓冲区大小的最终数据时，DMSBSL重新加载DMSBSH的值。当地址更新模式为固定地址时，该寄存器被忽略。表15.3显示了与源地址更新模式下的传输数据大小相对应的DMA源缓冲区大小寄存器的设置值。

在正常、重复和块传输模式下，不使用DMSBS。设置无效。

15.2.16 DMDBS : DMA Destination Buffer Size Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMDBSH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMDBSL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMDBSL[15:0]	Functions as data transfer counter in repeat-block transfer mode See Table 15.4 for available settings.	R/W
31:16	DMDBSH[15:0]	Specifies the repeat-area size in repeat-block transfer mode See Table 15.4 for available settings.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Table 15.4 Available setting for DMDBS register in repeat-block transfer mode

Destination Address Update Mode (DMAMD.SM)	Transfer Data Size (DMTMD.SZ)	Available Setting for DMDBSH and DMDBSL bits
Destination address is fixed (SM = 00b)	Don't care	0x0000 (DMDBS is not used)
Offset addition (SM = 01b)	8 bits (SZ = 00b)	0x0001 to 0xFFFF (1 to 65535)
	16 bits (SZ = 01b)	0x0001 to 0x7FFF (1 to 32767)
	32 bits (SZ = 10b)	0x0001 to 0x3FFF (1 to 16383)
Destination address is incremented or decremented (SM = 1xb)	Don't care	0x0000 (infinite) 0x0001 to 0xFFFF (1 to 65535)

Set the same value for DMDBSH and DMDBSL in repeat-block transfer mode. Write 00000000h to DMDBS in normal, repeat and block transfer mode.

DMDBSH specifies buffer size and DMDBSL functions as a 16-bit buffer size counter in repeat-block transfer mode. In repeat-block transfer mode, destination repeat area is specified by DMDBSH.

When address update mode is incremented address or decremented address, this register means the numbers of data of whole buffer. When address update mode is offset addition, this register means the numbers of data of an individual buffer. In offset addition, setting DMDBSH and DMDBSL to 0x0000 is prohibited. When final data of one buffer size is transferred, DMDBSL reloads value of DMDBSH. When address update mode is fixed address, this register is ignored. Table 15.4 shows the setting values of Destination Buffer Size Register corresponding to Transfer Data Size in Destination Address Update Mode.

In normal, repeat and block transfer mode, DMDBS is not used. The setting is invalid.

15.2.16 DMDBS:DMA目标缓冲区大小寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMDBSH[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMDBSL[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMDBSL[15:0]	在重复块传输模式中用作数据传输计数器 有关可用设置，请参见表15.4。	R/W
31:16	DMDBSH[15:0]	指定重复块传输模式下的重复区域大小 有关可用设置，请参见表15.4。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Table 15.4 重复块传输模式下DMDBS寄存器的可用设置

目标地址更新模式(DMAMD.SM)	传输数据大小(DMTMD.SZ)	DMDBSH的可用设置和 DMDBSL bits
目标地址是固定的（SM=00b）	不在乎	0x0000（未使用DMDBS）
偏移量加法(SM=01b)	8 bits (SZ = 00b)	0x0001 to 0xFFFF (1 to 65535)
	16 bits (SZ = 01b)	0x0001 to 0x7FFF (1 to 32767)
	32 bits (SZ = 10b)	0x0001 to 0x3FFF (1 to 16383)
目标地址递增或递减(SM=1xb)	不在乎	0x0000 (infinite) 0x0001 to 0xFFFF (1 to 65535)

在重复块传输模式下为DMDBSH和DMDBSL设置相同的值。在正常、重复和块传输模式下将00000000h写入DMDBS。

DMDBSH指定缓冲区大小，DMDBSL用作重复块传输模式下的16位缓冲区大小计数器。在重复块传输模式中，目标重复区域由DMDBSH指定。

当地址更新模式为递增地址或递减地址时，该寄存器表示整个缓冲区的数据个数。当地址更新模式为偏移加法时，该寄存器表示单个缓冲区的数据个数。此外，禁止将DMDBSH和DMDBSL设置为0x0000。当传输一个缓冲区大小的最终数据时，DMDBSL重新加载DMDBSH的值。当地址更新模式为固定地址时，该寄存器被忽略。表15.4显示了与Destination中的TransferDataSize对应的DestinationBufferSizeRegister的设置值

地址更新模式。

在正常、重复和块传输模式下，不使用DMDBS。设置无效。

15.2.17 DMAST : DMA Module Activation Register

Base address: DMA = 0x4000_5200

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DMST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DMST	DMAC Operation Enable 0: DMAC activation is disabled 1: DMAC activation is enabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

DMST bit (DMAC Operation Enable)

Setting the DMAST.DMST to 1 enables DMAC activation for all channels. When the DMST bit is set to 1 (DMAC activation is enabled), and 1 is written to the DMCNT.DTE bit (DMA transfer is enabled) for multiple channels, all of the associated channels can be placed in the transfer request ready state at the same time.

When the DMST bit clears to 0 during DMA transfer, DMA transfer is suspended after the current data transfer associated with a single transfer request completes. To resume DMA transfer, set the DMST bit to 1 again.

[Setting condition]

- When 1 is written to this bit

[Clearing condition]

- When 0 is written to this bit

15.2.18 DMECHR : DMAC Error Channel Register

Base address: DMA = 0x4000_5200

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMESTA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DMECHSAM	—	—	—	—	—	DMECH		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	DMECH	DMAC Error channel Indicates the channel number causing the error 0 0 0: Error occurred on Channel 0 0 0 1: Error occurred on Channel 1 0 1 0: Error occurred on Channel 2 ⋮ ⋮ 1 1 1: Error occurred on Channel 7	R

15.2.17 DMAST:DMA模块激活寄存器

Base address: DMA = 0x4000_5200

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DMST
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DMST	DMAC操作使能 0：禁用DMAC激活1：启用DMAC激活	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

DMST位（DMAC操作使能）

将DMAST.DMST设置为1会启用所有通道的DMAC激活。当DMST位设置为1（启用DMAC激活），并将1写入多个通道的DMCNT.DTE位（启用DMA传输）时，所有相关联的通道都可以置于传输请求就绪状态同时。

当DMA传输期间DMST位清除为0时，在与单个传输请求相关的当前数据传输完成后，DMA传输将暂停。要恢复DMA传输，请将DMST位再次设置为1。

[Setting condition]

●向该位写入1时

[Clearing condition]

●当0写入该位时

15.2.18 DMECHR:DMAC错误通道寄存器

Base address: DMA = 0x4000_5200

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMESTA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DMECHSAM	—	—	—	—	—	DMECH		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	DMECH	DMAC错误通道 指示导致错误的通道号 000：通道0发生错误001：通道1发生错误010：通道2发生错误 ⋮ ⋮ 111：通道7发生错误	R

Bit	Symbol	Function	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R
8	DMECHSAM	DMAC Error channel Security Attribution Monitor Indicates the security attribution of a channel causing the error 0: secure channel 1: non-secure channel	R
15:9	—	These bits are read as 0. The write value should be 0.	R
16	DMESTA	DMAC Error Status 0: No DMA transfer error occurred 1: DMA transfer error occurred	R/W*1
31:17	—	These bits are read as 0. The write value should be 0.	R

Note 1. Writing to DMESTA depends on the value of DMECHSAM

DMECH[2:0] bit (DMAC Error channel)

When a transfer error due to DMA transfer occurs, it stores the channel of DMAC that was violated.

When reset was selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, Since this register is also reset. Please select NMI when you want to debug the program.

[Set condition]

- When the DMAC transfer error occurs and DMESTA = 0.

[Clearing condition]

- When 1 is written to DMESTA.

DMECHSAM bit (DMAC Error channel Security Attribution Monitor)

When a transfer error due to DMA transfer occurs, it indicates the security attribution of the violating DMAC channel.

When reset was selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, Since this register is also reset. Please select NMI when you want to debug the program.

[Set condition]

- When the DMAC transfer error occurs and DMESTA = 0.

[Clearing condition]

- When 1 is written to DMESTA.

DMESTA bit (DMAC Error Status)

Indicates whether or not a DMA transfer error occurred.

DMECH, DMECHSAM, DMESTA are cleared by writing 1 to DMESTA. Writing 0 to DMESTA is ignored.

When reset was selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, Since this register is also reset. Please select NMI when you want to debug the program.

[Set condition]

- When the DMAC transfer error occurs.

[Clearing condition]

- When 1 is written to DMESTA.

Note: When DMECHSAM = 1, it can be cleared in the secure state and non-secure state. DMECHSAM = 0, it can not be cleared in the non-secure state.

Bit	Symbol	Function	R/W
7:3	—	这些位被读取为0。写入值应为0。	R
8	DMECHSAM	DMAC错误通道安全归因监视器 指示导致错误的通道的安全属性 0：安全通道1：非安全通道	R
15:9	—	这些位被读取为0。写入值应为0。	R
16	DMESTA	DMAC错误状态 0：未发生DMA传输错误1：发生DMA传输错误	R/W*1
31:17	—	这些位被读取为0。写入值应为0。	R

注1.写入DMESTA取决于DMECHSAM的值

DMECH[2:0]位（DMAC错误通道）

当由于DMA传输而发生传输错误时，它会存储违反的DMAC通道。

当在MPU.MMPUOAD.OAD和TZF.TZFOAD.OAD中选择了复位时，由于该寄存器也被复位。请选择NMI当你想调试程序时。

[Set condition]

●发生DMAC传输错误且DMESTA=0时。

[Clearing condition]

●当1被写入DMESTA时。

DMECHSAM位（DMAC错误通道安全属性监视器）

当由于DMA传输而发生传输错误时，表明违规DMAC通道的安全属性。

当在MPU.MMPUOAD.OAD和TZF.TZFOAD.OAD中选择了复位时，由于该寄存器也被复位。请选择NMI当你想调试程序时。

[Set condition]

●发生DMAC传输错误且DMESTA=0时。

[Clearing condition]

●当1被写入DMESTA时。

DMESTA位（DMAC错误状态）

指示是否发生DMA传输错误。

DMECH、DMECHSAM、DMESTA通过向DMESTA写入1清零。将0写入DMESTA将被忽略。

当在MPU.MMPUOAD.OAD和TZF.TZFOAD.OAD中选择了复位时，由于该寄存器也被复位。请选择NMI当你想调试程序时。

[Set condition]

●发生DMAC传输错误时。

[Clearing condition]

●当1被写入DMESTA时。

Note: 当DMECHSAM=1时，可以在安全状态和非安全状态下清零。DMECHSAM=0，在非安全状态下不能清零。

15.3 Operation

15.3.1 Transfer Mode

15.3.1.1 Normal Transfer Mode

In normal transfer mode, one data is transferred by one transfer request. A maximum of 65535 can be set as the number of transfer operations using the DMCRAL register. When these bits are set to 0x0000, no specific number of transfer operations is set; data transfer is performed with the transfer counter stopped (free running function). Setting DMCRB register is invalid in normal transfer mode. Except in free running function, a transfer end interrupt request can be generated after completion of the specified number of transfer operations.

Table 15.5 summarizes the register update operation in normal transfer mode, and Figure 15.2 shows the operation in normal transfer mode.

Table 15.5 Register Update Operation in Normal Transfer Mode

Register	Function	Update Operation after Completion of a Transfer by One Transfer Request
DMSAR	Transfer source address	Increment/decrement/fixed/offset addition
DMDAR	Transfer destination address	Increment/decrement/fixed/offset addition
DMCRAL	Transfer count	Decremented by one/not updated (in free running function)
DMCRAH	—	Not updated (Not used in normal transfer mode)
DMCRB	—	Not updated (Not used in normal transfer mode)

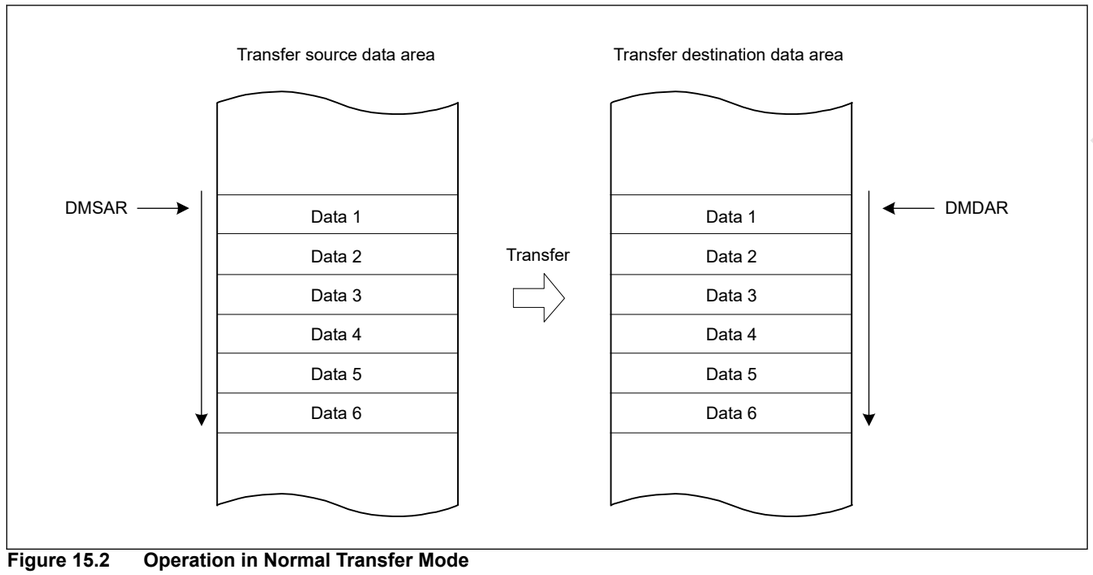


Figure 15.2 Operation in Normal Transfer Mode

15.3.1.2 Repeat Transfer Mode

In repeat transfer mode, one data is transferred by one transfer request.

A maximum of 1K data can be set as a total repeat transfer size using DMCRA register.

A maximum of 64K can be set as the number of repeat transfer operations using DMCRB register; therefore, a maximum of 64M data (1K data × 64K counts of repeat transfer operations) can be set as a total data transfer size.

Either the transfer source or transfer destination can be specified as a repeat area. When transfer of the repeat size data is completed, the address of the specified repeat area (DMSAR or DMDAR) returns to the transfer start address. When data of the specified repeat size has all been transferred in repeat transfer mode, DMA transfer can be stopped and the repeat size

15.3 Operation

15.3.1 传输模式

15.3.1.1 正常传输模式

在正常传输模式下，一个数据由一个传输请求传输。使用DMCRAL寄存器最多可以设置65535个传输操作数。当这些位设置为0x0000时，没有设置具体的传输操作数；在传输计数器停止的情况下执行数据传输（自由运行功能）。在正常传输模式下设置DMCRB寄存器无效。除自由运行功能外，在完成指定次数的传输操作后可以产生传输结束中断请求。

表15.5总结了正常传输模式下的寄存器更新操作，图15.2显示了正常传输模式下的操作。

Table 15.5 正常传输模式下的寄存器更新操作

Register	Function	一次转账完成后更新操作 Request
DMSAR	传输源地址	Increment/decrement/fixed/offset addition
DMDAR	转移目的地地址	Increment/decrement/fixed/offset addition
DMCRAL	转移计数	减一未更新（在自由运行功能中）
DMCRAH	—	未更新（ 未在正常传输模式下使用）
DMCRB	—	未更新（ 未在正常传输模式下使用）

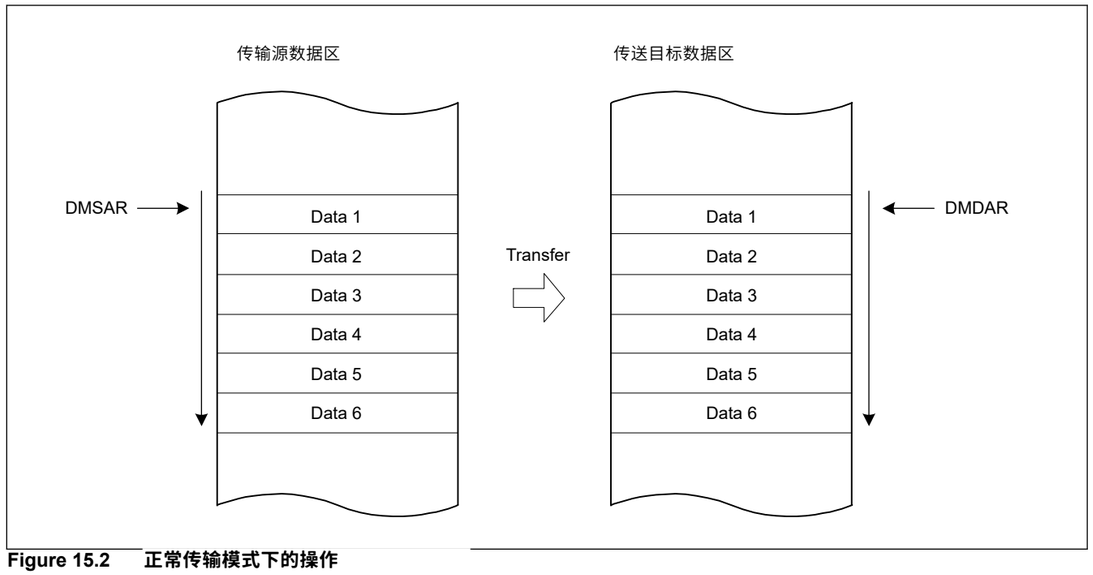


Figure 15.2 正常传输模式下的操作

15.3.1.2 重复传输模式

在重复传输模式下，一个数据由一个传输请求传输。

使用DMCRA寄存器最多可以将1K数据设置为总重复传输大小。

使用DMCRB寄存器最多可以设置64K作为重复传输操作的次数；因此，最多可以将64M数据（1K数据×64K重复传输操作计数）设置为总数据传输大小。

可以将传输源或传输目标指定为重复区域。当重复大小数据的传输完成时，指定的重复区域（DMSAR或DMDAR）的地址返回到传输起始地址。在重复传输模式下，当指定重复大小的数据全部传输完毕后，可以停止DMA传输，重复大小

end interrupt can be requested. DMA transfer can be resumed by writing 1 to the DMCNT.DTE bit in the repeat size end interrupt handling.

A transfer end interrupt request can be generated after completion of the specified number of repeat transfer operations.

Table 15.6 summarizes the register update operation in repeat transfer mode, and Figure 15.3 shows the operation in repeat transfer mode.

Table 15.6 Register Update Operation in Repeat Transfer Mode

Register	Function	Update Operation after Completion of a Transfer by One Transfer Request	
		When DMCRAL register is not 1	When DMCRAL register is 1 (Transfer of the Last Data in Repeat Size)
DMSAR	Transfer source address	Increment/decrement/fixed/offset addition	• DMTMD.DTS[1:0] = 00b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 01b Initial value of DMSAR • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMDAR	Transfer destination address	Increment/decrement/fixed/offset addition	• DMTMD.DTS[1:0] = 00b Initial value of DMDAR • DMTMD.DTS[1:0] = 01b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMCRAH	Repeat size	Not updated	Not updated
DMCRAL	Transfer count	Decremented by one	DMCRAH
DMCRBH	Number of repeat transfer operations	Not updated	Not updated
DMCRBL	Count of repeat transfer operations	Not updated	Decremented by one

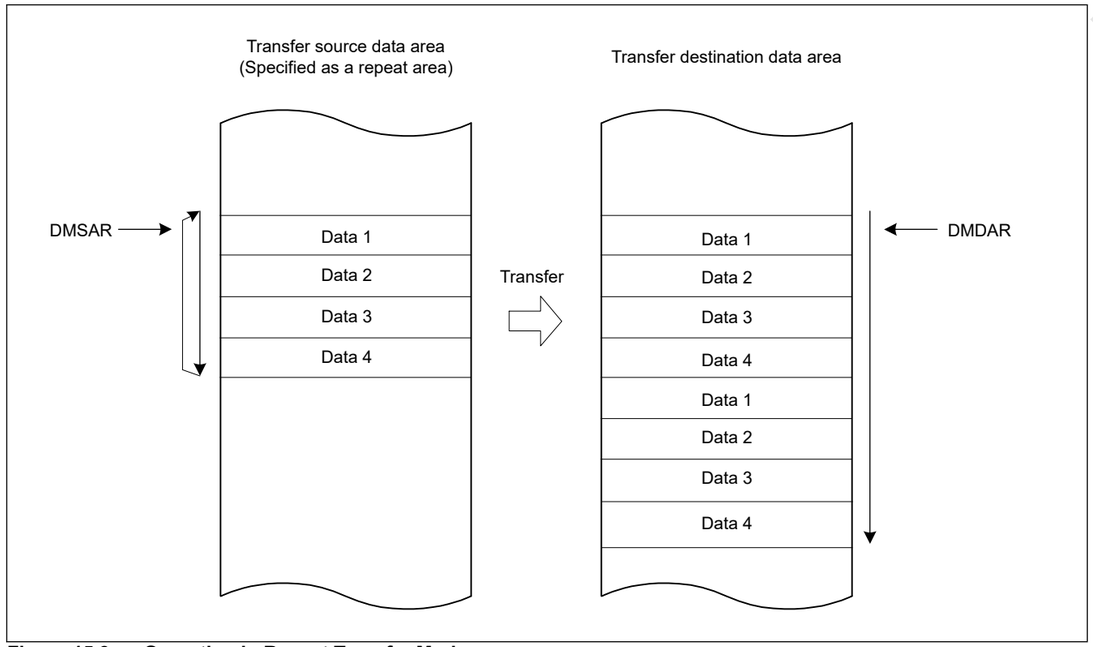


Figure 15.3 Operation in Repeat Transfer Mode

可以请求结束中断。DMA传输可以通过在重复大小结束中断处理中向DMCNT.DTE位写入1来恢复。

完成指定次数的重复传输操作后，可以产生传输结束中断请求。

表15.6总结了重复传输模式下的寄存器更新操作，图15.3显示了重复传输模式下的操作。

Table 15.6 重复传输模式下的寄存器更新操作

Register	Function	通过一个传输请求完成传输后更新操作	
		当DMCRAL寄存器不为1时	当DMCRAL寄存器为1时（传输重复大小的最后一个数据）
DMSAR	传输源地址	Increment/decrement/fixed/offset addition	• DMTMD.DTS[1:0] = 00b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 01b DMSAR初始值 • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMDAR	转移目的地地址	Increment/decrement/fixed/offset addition	• DMTMD.DTS[1:0] = 00b DMDAR的初始值 • DMTMD.DTS[1:0] = 01b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMCRAH	重复大小	未更新	未更新
DMCRAL	转移计数	减一	DMCRAH
DMCRBH	重复传输操作数	未更新	未更新
DMCRBL	重复传输操作的计数	未更新	减一

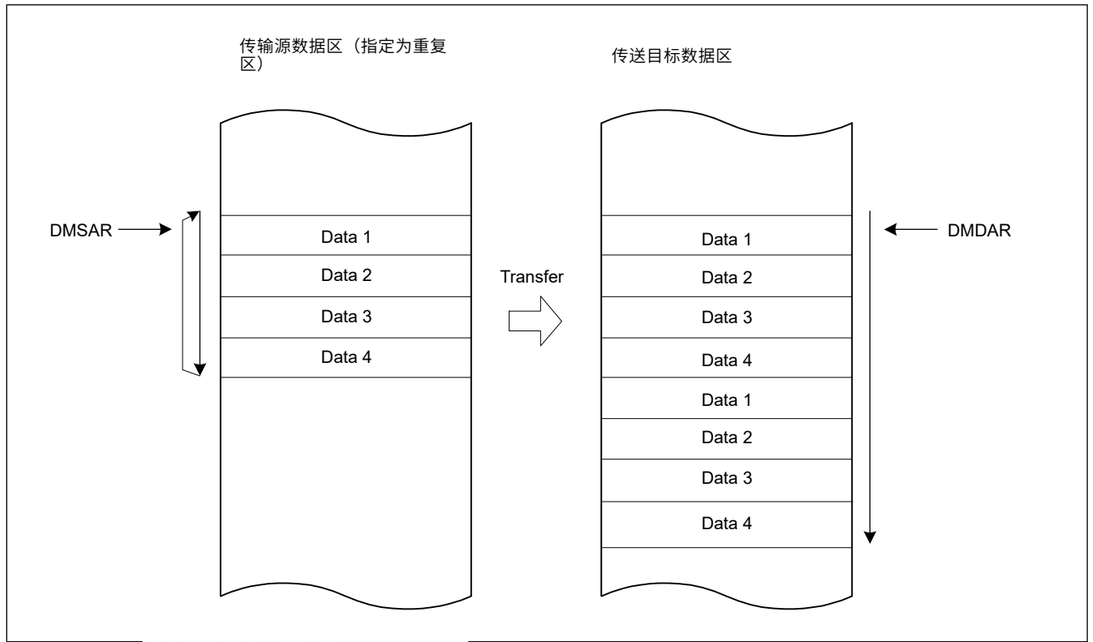


Figure 15.3 重复传输模式下的操作

15.3.1.3 Block Transfer Mode

In block transfer mode, a single block data is transferred by one transfer request.

A maximum of 1K data can be set as a total block transfer size using DMCRA register.

A maximum of 64K can be set as the number of block transfer operations using DMCRB register; therefore, a maximum of 64M data (1K data × 64K counts of block transfer operations) can be set as a total data transfer size.

Either the transfer source or transfer destination can be specified as a block area. When transfer of a single block data is completed, the address of the specified block area (DMSAR or DMDAR) returns to the transfer start address. When a single block data has all been transferred in block transfer mode, DMA transfer can be stopped and the repeat size end interrupt can be requested. DMA transfer can be resumed by writing 1 to the DMCNT.DTE bit in the repeat size end interrupt handling.

Transfer end interrupt request can be generated after completion of the specified number of block transfer operations.

Table 15.7 summarizes the register update operation in block transfer mode, and Figure 15.4 shows the operation in block transfer mode.

Table 15.7 Register Update Operation in Block Transfer Mode

Register	Function	Update Operation after Completion of Single-Block Transfer by One Transfer Request
DMSAR	Transfer source address	• DMTMD.DTS[1:0] = 00b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 01b Initial value of DMSAR • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMDAR	Transfer destination address	• DMTMD.DTS[1:0] = 00b Initial value of DMDAR • DMTMD.DTS[1:0] = 01b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMCRAH	Block size	Not updated
DMCRAL	Transfer count	DMCRAH
DMCRBH	Number of block transfer operations	Not updated
DMCRBL	Count of block transfer operations	Decremented by one

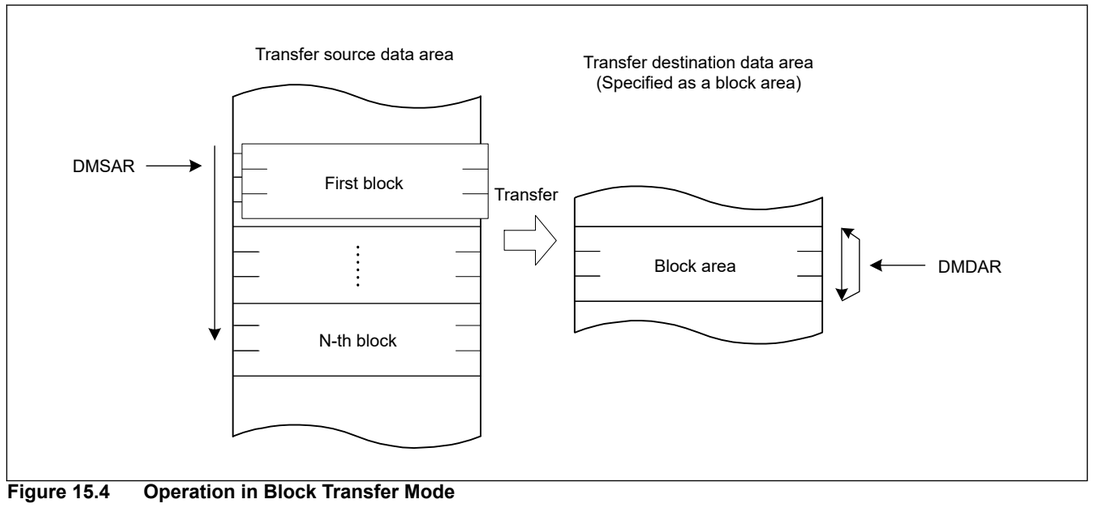


Figure 15.4 Operation in Block Transfer Mode

15.3.1.3 块传输模式

在块传输模式下，单个块数据由一个传输请求传输。

使用DMCRA寄存器最多可以将1K数据设置为总块传输大小。

使用DMCRB寄存器最多可以设置64K作为块传输操作的数量；因此，最多可以将64M数据（1K数据×64K块传输操作计数）设置为总数据传输大小。

可以将传输源或传输目标指定为块区域。当单个块数据的传输完成时，指定块区域（DMSAR或DMDAR）的地址返回到传输起始地址。在块传输模式下，当单个块数据已全部传输完毕后，可以停止DMA传输并请求重复大小结束中断。DMA传输可以通过在重复大小结束中断处理中向DMCNT.DTE位写入1来恢复。

在完成指定数量的块传输操作后，可以产生传输结束中断请求。

表15.7总结了块传输模式下的寄存器更新操作，图15.4显示了块传输模式下的操作。

Table 15.7 块传输模式下的寄存器更新操作

Register	Function	一次传输完成单块传输后的更新操作 Request
DMSAR	传输源地址	• DMTMD.DTS[1:0] = 00b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 01b DMSAR初始值 • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMDAR	转移目的地地址	• DMTMD.DTS[1:0] = 00b DMDAR的初始值 • DMTMD.DTS[1:0] = 01b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMCRAH	块大小	未更新
DMCRAL	转移计数	DMCRAH
DMCRBH	块传输操作数	未更新
DMCRBL	块传输操作的计数	减一

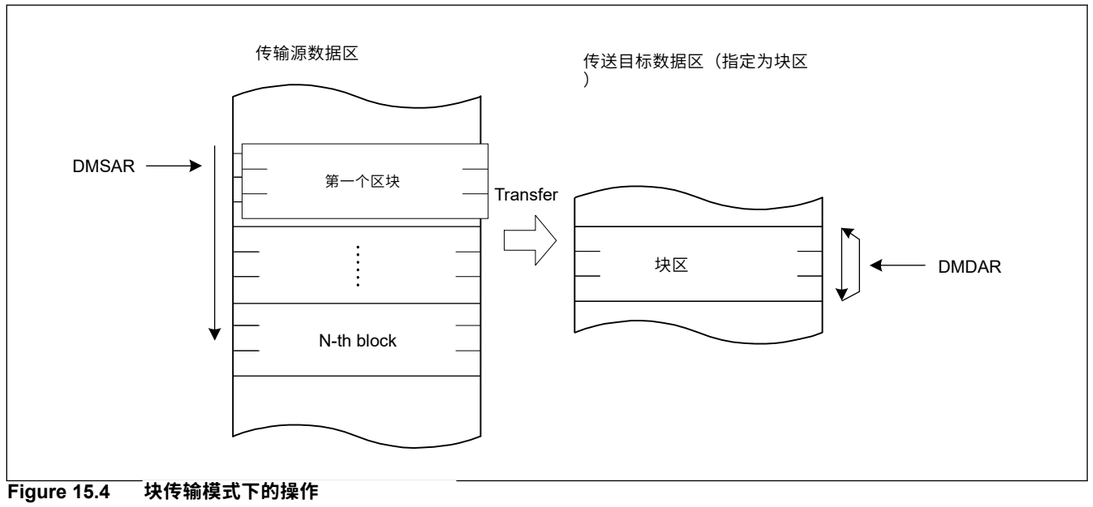


Figure 15.4 块传输模式下的操作

15.3.1.4 Repeat-Block Transfer Mode

Repeat-block transfer is the operation mode with the following functions added to the block transfer function.

Repeat function: Added function (ring buffer) to repeat specified address area.

Offset function: Multiple areas with offset can be specified within one block transfer.

The repeat function and the offset function can be used for both the transfer source and the transfer destination of repeat-block transfer.

Figure 15.5 shows an example of adding a repeat function to the transfer destination.

Figure 15.6 shows repeat-block transfer with an offset to the transfer destination.

In repeat-block transfer mode, a single block data is transferred by one transfer request.

A maximum of 1K data can be set as a total block transfer size using DMCRA of the DMACn.

A maximum of 64K can be set as the number of block transfer operations using DMCRB of the DMACn; therefore, a maximum of 64M data (1K data × 64K counts of block transfer operations) can be set as a total data transfer size.

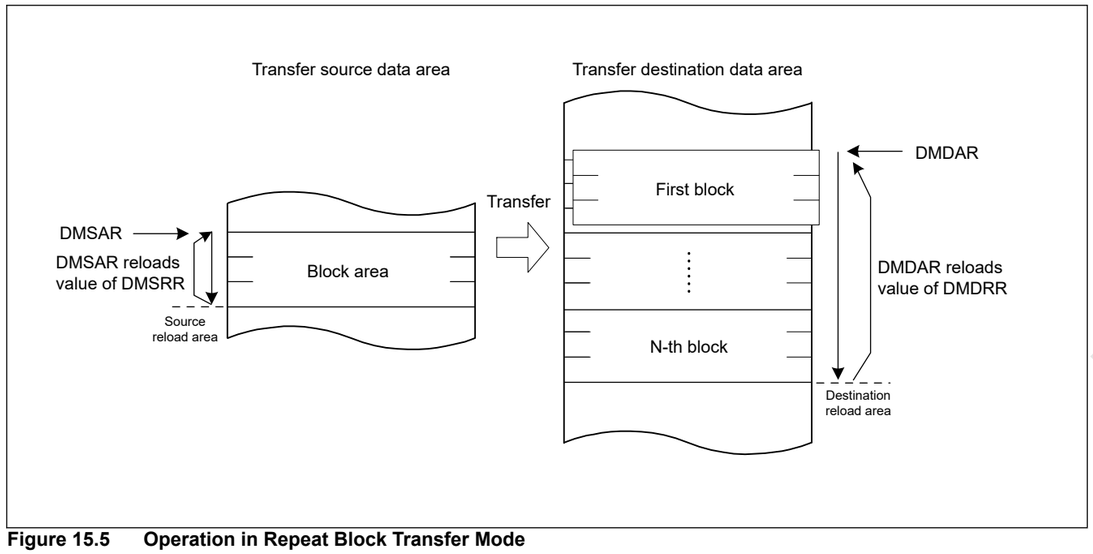


Figure 15.5 Operation in Repeat Block Transfer Mode

15.3.1.4 重复块传输模式

重复块传输是在块传输功能中添加了以下功能的操作模式。

重复功能：增加了重复指定地址区域的功能（环形缓冲区）。

偏移功能：在一次块传输中可以指定多个带偏移的区域。

重复块传输的传输源和传输目标都可以使用重复函数和偏移函数。

图15.5显示了向传输目的地添加重复功能的示例。

图15.6显示了到传输目标的偏移量的重复块传输。

在重复块传输模式中，单个块数据由一个传输请求传输。

使用DMACn的DMCRA可以将最大1K数据设置为总块传输大小。

使用DMACn的DMCRB最多可以设置64K作为块传输操作的数量；因此，最多可以将64M数据（1K数据×64K块传输操作计数）设置为总数据传输大小。

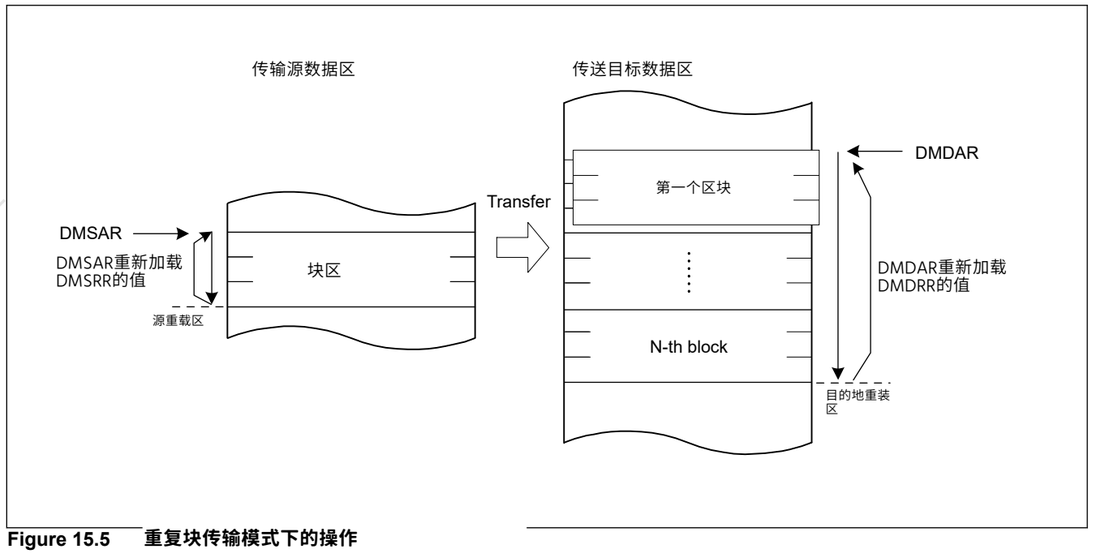


Figure 15.5 重复块传输模式下的操作

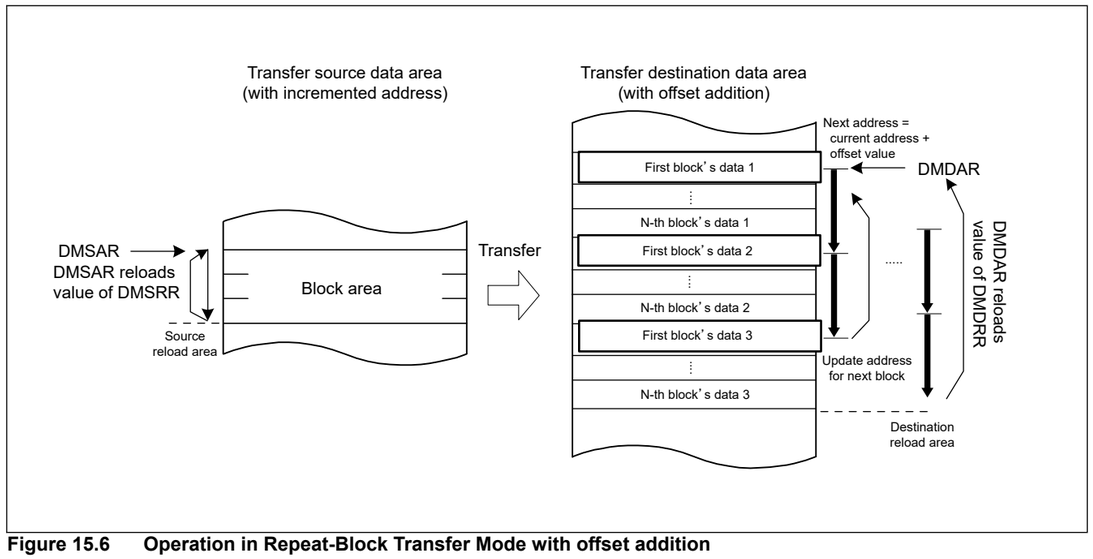


Figure 15.6 Operation in Repeat-Block Transfer Mode with offset addition

Table 15.8 to Table 15.13 summarize the register update operations in repeat-block transfer mode.

Table 15.8 Register Update Operation associated with source area in Repeat-Block Transfer Mode (Fixed address DMAMD.SM[1:0] = 00b)

Register	Function	Update operation after single data is transferred		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMSRR	Transfer source reload address	Not updated	Not updated	Not updated
DMSAR	Transfer source address	Not updated	Not updated	Not updated
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]

Table 15.9 Register Update Operation associated with destination area in Repeat-Block Transfer Mode (Fixed address DMAMD.DM[1:0] = 00b) (1 of 2)

Register	Function	Update operation after single data is transferred		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMDRR	Transfer destination reload address	Not updated	Not updated	Not updated
DMDAR	Transfer destination address	Not updated	Not updated	Not updated
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]

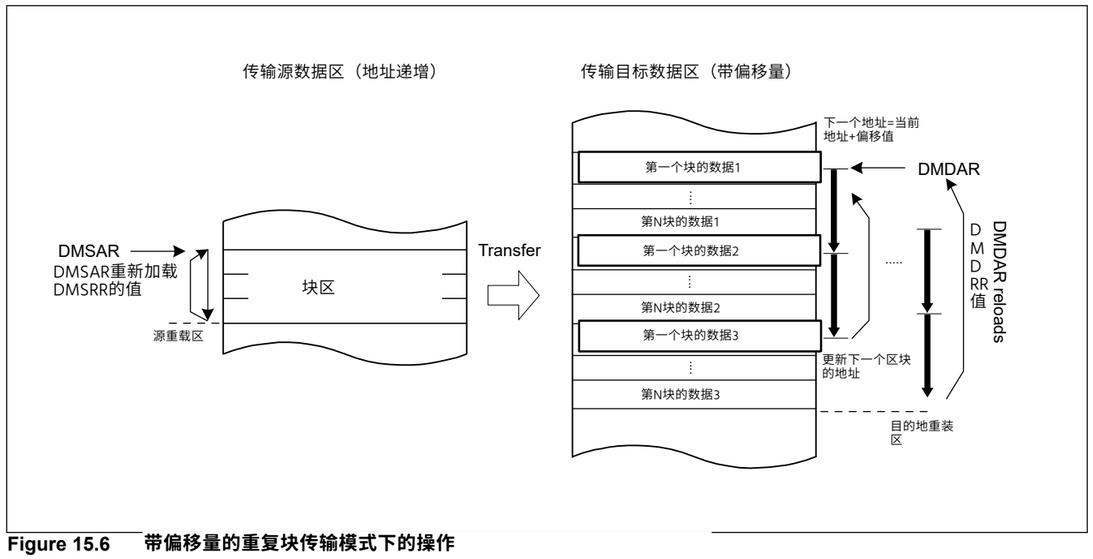


Figure 15.6 带偏移量的重复块传输模式下的操作

表15.8至表15.13总结了重复块传输模式下的寄存器更新操作。

Table 15.8 重复块传输模式下与源区域相关的寄存器更新操作（固定地址DMAMD.SM[1:0] = 00b）

Register	Function	单条数据传输后的更新操作		
		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMSRR	传输源重载地址	未更新	未更新	未更新
DMSAR	传输源地址	未更新	未更新	未更新
DMCRAH[9:0]	块大小	未更新	未更新	未更新
DMCRAL[15:0]	块大小计数	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMCRBH[15:0]	块传输操作数	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD.TKP=0时的块传输操作计数	未更新	Decremented by 1	0
	DMTMD.TKP=1时的块传输操作计数			DMCRBH[15:0]

Table 15.9 与重复块传输模式中的目标区域相关的寄存器更新操作（固定地址DMAMD.DM[1:0]=00b）（1of2）

Register	Function	单条数据传输后的更新操作		
		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMDRR	传输目的地重载地址	未更新	未更新	未更新
DMDAR	转移目的地地址	未更新	未更新	未更新
DMCRAH[9:0]	块大小	未更新	未更新	未更新
DMCRAL[15:0]	块大小计数	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]

Table 15.9 Register Update Operation associated with destination area in Repeat-Block Transfer Mode (Fixed address DMAMD.DM[1:0] = 00b) (2 of 2)

Register	Function	Update operation after single data is transferred		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]

Table 15.10 Register Update Operation associated with source area in Repeat-Block Transfer Mode (Incremented or Decre-mented address DMAMD.SM[1:0] = 10b or 11b) (1 of 2)

Register	Function	Update operation after single data is transferred					
		DMSBSL[15:0] is not 1			DMSBSL[15:0] is 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1		DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMSRR	Transfer source reload address	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMSAR	Transfer source address when DMTMD.SM[1:0] = 10b	Incremented by Data Size			DMSRR		
	Transfer source address when DMTMD.SM[1:0] = 11b	Decremented by Data Size			DMSRR		
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMSBSH[15:0]	Source buffer size (Repeat-size)	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMSBSL[15:0]	Count of transfer data in source buffer	Decremented by 1	Decremented by 1	Decremented by 1	DMSBSH	DMSBSH	DMSBSH
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated

Table 15.9 重复块传输模式中与目标区域相关的寄存器更新操作（固定地址DMAMD.DM[1:0]=00b）（2of2）

Register	Function	单条数据传输后的更新操作		
		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMCRBH[15:0]	块传输操作数	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD.TKP=0时的块传输操作计数	未更新	Decremented by 1	0
	DMTMD.TKP=1时的块传输操作计数			DMCRBH[15:0]

Table 15.10 与重复块传输模式中的源区域相关的寄存器更新操作（递增或递减地址DMAMD.SM[1:0]=10b或11b）（1of2）

Register	Function	单条数据传输后的更新操作					
		DMSBSL[15:0]不是1			DMSBSL[15:0] is 1		
		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1		DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMSRR	传输源重载地址	未更新	未更新	未更新	未更新	未更新	未更新
DMSAR	DMTMD.SM[1:0]=10b时传输源地址	按数据大小递增			DMSRR		
	DMTMD.SM[1:0]=11b时传输源地址	按数据大小递减			DMSRR		
DMCRAH[9:0]	块大小	未更新	未更新	未更新	未更新	未更新	未更新
DMCRAL[15:0]	块大小计数	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMSBSH[15:0]	源缓冲区大小（重复大小）	未更新	未更新	未更新	未更新	未更新	未更新
DMSBSL[15:0]	源缓冲区中的传输数据计数	Decremented by 1	Decremented by 1	Decremented by 1	DMSBSH	DMSBSH	DMSBSH
DMCRBH[15:0]	块传输操作数	未更新	未更新	未更新	未更新	未更新	未更新

Table 15.10 Register Update Operation associated with source area in Repeat-Block Transfer Mode (Incremented or Decre-mented address DMAMD.SM[1:0] = 10b or 11b) (2 of 2)

Register	Function	Update operation after single data is transferred					
		DMSBSL[15:0] is not 1			DMSBSL[15:0] is 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1		DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0	Not updated	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]			DMCRBH[15:0]

Table 15.11 Register Update Operation associated with destination area in Repeat-Block Transfer Mode (Incremented or Decremented address DMAMD.DM[1:0] = 10b or 11b) (1 of 2)

Register	Function	Update operation after single data is transferred					
		DMDBSL[15:0] is not 1			DMDBSL[15:0] is 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1		DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMDRR	Transfer destination reload address	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMDAR	Transfer destination address when DMTMD.DM[1:0] = 10b	Incremented by Data Size			DMDRR		
	Transfer destination address when DMTMD.DM[1:0] = 11b	Decremented by Data Size			DMDRR		
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMDBSH[15:0]	Destina-tion buffer size (Repeat-size)	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMDBSL[15:0]	Count of transfer data in destination buffer	Decremented by 1	Decremented by 1	Decremented by 1	DMDBSH	DMDBSH	DMDBSH
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated

Table 15.10 重复块传输模式中与源区域相关的寄存器更新操作（递增或递减地址DMAMD.SM[1:0]=10b或11b）（2of2）

Register	Function	单条数据传输后的更新操作					
		DMSBSL[15:0]不是1			DMSBSL[15:0] is 1		
		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1		DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMCRBL[15:0]	DMTMD.TKP=0时的块传输操作计数	未更新	Decremented by 1	0	未更新	Decremented by 1	0
	DMTMD.TKP=1时的块传输操作计数			DMCRBH[15:0]			DMCRBH[15:0]

Table 15.11 与重复块传输模式中的目标区域相关的寄存器更新操作（递增或递减地址DMAMD.DM[1:0]=10b或11b）（1of2）

Register	Function	单条数据传输后的更新操作					
		DMDBSL[15:0]不是1			DMDBSL[15:0] is 1		
		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1		DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMDRR	传输目的地重载地址	未更新	未更新	未更新	未更新	未更新	未更新
DMDAR	DMTMD.DM[1:0]=10b时传输目标地址	按数据大小递增			DMDRR		
	DMTMD.DM[1:0]=11b时传输目标地址	按数据大小递减			DMDRR		
DMCRAH[9:0]	块大小	未更新	未更新	未更新	未更新	未更新	未更新
DMCRAL[15:0]	块大小计数	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMDBSH[15:0]	目标缓冲区大小（Repeat-size）	未更新	未更新	未更新	未更新	未更新	未更新
DMDBSL[15:0]	目标缓冲区中的传输数据计数	Decremented by 1	Decremented by 1	Decremented by 1	DMDBSH	DMDBSH	DMDBSH
DMCRBH[15:0]	块传输操作数	未更新	未更新	未更新	未更新	未更新	未更新

Table 15.11 Register Update Operation associated with destination area in Repeat-Block Transfer Mode (Incremented or Decremented address DMAMD.DM[1:0] = 10b or 11b) (2 of 2)

Register	Function	Update operation after single data is transferred					
		DMDBSL[15:0] is not 1			DMDBSL[15:0] is 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1		DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0	Not updated	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]			DMCRBH[15:0]

Table 15.12 Register Update Operation associated with source area in Repeat-Block Transfer Mode (Offset addition DMAMD.SM[1:0] = 01b)

Register	Function	DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)			
			DMSBSL[15:0] is not 1		DMSBSL[15:0] is 1	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1	DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMSRR	Transfer source reload address	Not updated	Not updated	Not updated	Not updated	Not updated
DMSAR	Transfer source address when DMAMD.SADR = 0	Offset addition by DMSBSH	DMSRR		DMSRR	
	Transfer source address when DMAMD.SADR = 1		DMSRR + (DMS-BSH - DMSBSL) × DataSize			
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]
DMSBSH[15:0]	Source buffer size (Repeat-size)	Not updated	Not updated	Not updated	Not updated	Not updated
DMSBSL[15:0]	Count of transfer data in source buffer	Not updated	Decremented by 1	Decremented by 1	DMSBSH	DMSBSH
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]		DMCRBH[15:0]

Table 15.11 与重复块传输模式中的目标区域相关的寄存器更新操作（递增或递减地址DMAMD.DM[1:0]=10b或11b）（2of2）

Register	Function	单条数据传输后的更新操作					
		DMDBSL[15:0]不是1			DMDBSL[15:0] is 1		
		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1		DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMCRBL[15:0]	DMTMD.TKP=0时的块传输操作计数	未更新	Decremented by 1	0	未更新	Decremented by 1	0
	DMTMD.TKP=1时的块传输操作计数			DMCRBH[15:0]			DMCRBH[15:0]

Table 15.12 重复块传输模式下与源区域相关的寄存器更新操作（偏移量加法DMAMD.SM[1:0]=01b）

Register	Function	DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）			
			DMSBSL[15:0]不是1		DMSBSL[15:0] is 1	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1	DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMSRR	传输源重载地址	未更新	未更新	未更新	未更新	未更新
DMSAR	DMAMD.SADR=时传输源地址0	偏移量加法DMSBSH	DMSRR		DMSRR	
	DMAMD.SADR=时传输源地址1		DMSRR + (DMS-BSH - DMSBSL) × DataSize			
DMCRAH[9:0]	块大小	未更新	未更新	未更新	未更新	未更新
DMCRAL[15:0]	块大小计数	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]
DMSBSH[15:0]	源缓冲区大小（重复大小）	未更新	未更新	未更新	未更新	未更新
DMSBSL[15:0]	源缓冲区中的传输数据计数	未更新	Decremented by 1	Decremented by 1	DMSBSH	DMSBSH
DMCRBH[15:0]	块传输操作数	未更新	未更新	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD.TKP=0时的块传输操作计数	未更新	Decremented by 1	0	Decremented by 1	0
	DMTMD.TKP=1时的块传输操作计数			DMCRBH[15:0]		DMCRBH[15:0]

Table 15.13 Register Update Operation associated with destination area in Repeat-Block Transfer Mode (Offset addition DMAMD.DM[1:0] = 01b)

Register	Function	DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)			
			DMDBSL[15:0] is not 1		DMDBSL[15:0] is 1	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1	DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMDRR	Transfer destination reload address	Not updated	Not updated	Not updated	Not updated	Not updated
DMSAR	Transfer destination address when DMAMD.DADR = 0	Offset addition by DMDBSH	DMDRR		DMDRR	
	Transfer destination address when DMAMD.DADR = 1		DMDRR + (DMDBSH - DMDBSL) × DataSize			
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]
DMDBSH[15:0]	Destina-tion buffer size (Repeat-size)	Not updated	Not updated	Not updated	Not updated	Not updated
DMDBSL[15:0]	Count of transfer data in destination buffer	Not updated	Decremented by 1	Decremented by 1	DMDBSH	DMDBSH
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]		DMCRBH[15:0]

15.3.2 Extended Repeat Area Function

The DMAC supports a function to specify the extended repeat areas on the transfer source and destination addresses. With the extended repeat areas set, the address registers repeatedly indicate the addresses of the specified extended repeat areas.

The extended repeat areas can be specified separately to the transfer source address register (DMSAR) and transfer destination address register (DMDAR).

The extended repeat area on the source address is specified by the DMAMD.SARA[4:0] bits. The extended repeat area on the destination address is specified by the DMAMD.DARA[4:0] bits. The size can be specified separately for the source and destination sides.

However, the area (of transfer source or transfer destination) which is specified as the repeat area or block area should not be specified as the extended repeat area.

When the address register value reaches the end address of the extended repeat area and the extended repeat area overflows, DMA transfer is stopped and an interrupt by an extended repeat area overflow can be requested. When an overflow occurs in the extended repeat area on the transfer source while the DMINT.SARIE bit is set to 1, the DMSTS.ESIF flag is set to 1 and the DMCNT.DTE bit is cleared to 0 to stop DMA transfer. At this time, if the DMINT.ESIE bit is set to 1, an interrupt by an extended repeat area overflow is requested. When the DMINT.DARIE bit is set to 1, the destination address register

Table 15.13 重复块传输模式下与目标区域相关的寄存器更新操作（偏移量加法DMAMD.DM[1:0]=01b）

Register	Function	DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）			
			DMDBSL[15:0]不是1		DMDBSL[15:0] is 1	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1	DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMDRR	传输目的地重载地址	未更新	未更新	未更新	未更新	未更新
DMSAR	当DMAMD.DADR =时传输目标地址 0	偏移量加法 DMDBSH	DMDRR		DMDRR	
	当DMAMD.DADR =时传输目标地址 1		DMDRR + (DMDBSH - DMDBSL) × DataSize			
DMCRAH[9:0]	块大小	未更新	未更新	未更新	未更新	未更新
DMCRAL[15:0]	块大小计数	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]
DMDBSH[15:0]	目标缓冲区大小（Repeat-size）	未更新	未更新	未更新	未更新	未更新
DMDBSL[15:0]	目标缓冲区中的传输数据计数	未更新	Decremented by 1	Decremented by 1	DMDBSH	DMDBSH
DMCRBH[15:0]	块传输操作数	未更新	未更新	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD.TKP=0时的块传输操作计数	未更新	Decremented by 1	0	Decremented by 1	0
	DMTMD.TKP=1时的块传输操作计数			DMCRBH[15:0]		DMCRBH[15:0]

15.3.2 扩展重复区域功能

DMAC支持在传输源地址和目标地址上指定扩展重复区域的功能。通过设置扩展重复区域，地址寄存器重复指示指定扩展重复区域的地址。

扩展重复区域可以分别指定到传输源地址寄存器(DMSAR)和传输目标地址寄存器(DMDAR)。

源地址上的扩展重复区域由DMAMD.SARA[4:0]位指定。目标地址上的扩展重复区域由DMAMD.DARA[4:0]位指定。可以为源端和目标端分别指定大小。

但是，指定为重复区域或块区域的区域（传送源或传送目的地）不应指定为扩展重复区域。

当地址寄存器值到达扩展重复区的结束地址且扩展重复区溢出时，
DMA传输停止并且可以请求由扩展重复区域溢出引起的中断。当DMINT.SARIE位设置为1时传输源上的扩展重复区域发生溢出时，DMSTS.ESIF标志设置为1并且DMCNT.DTE位清零以停止DMA传输。此时，如果DMINT.ESIE位设置为1，则请求由扩展重复区域溢出引起的中断。当DMINT.DARIE位设置为1时，目标地址寄存器

becomes a target to apply the function. DMA transfer can be resumed by writing 1 to the DMCNT.DTE bit in the interrupt handling.

Figure 15.7 shows an example of the extended repeat area operation.

Eight bytes are specified as an extended repeat area by the lower three bits of DMSAR (DMAMD.SARA[4:0] bits = 00011b). The data size is eight bits (DMTMD.SZ[1:0] = 00b).

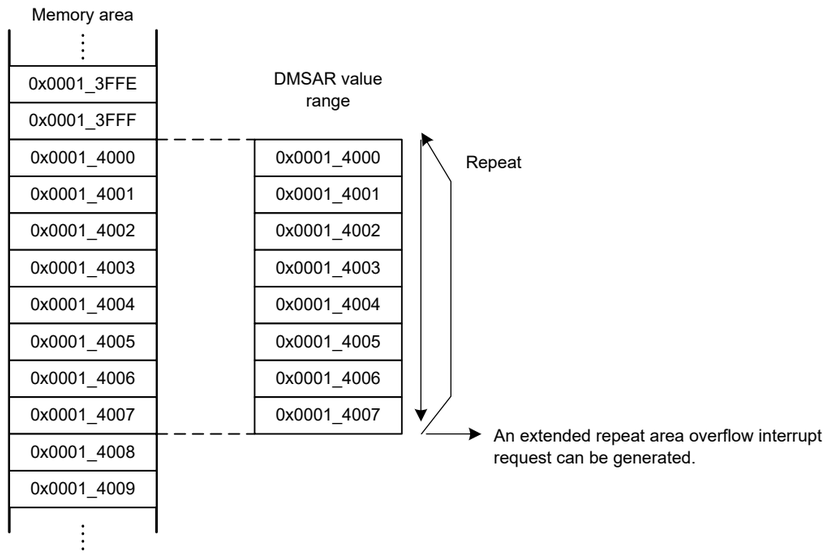


Figure 15.7 Example of Extended Repeat Area Operation

When an interrupt by an extended repeat area overflow is used in block transfer mode, the following should be taken into consideration.

When a transfer is stopped by an interrupt by an extended repeat area overflow, the address register must be set so that the block size is a power of 2 or the block size boundary is aligned with the extended repeat area boundary. When an overflow on the extended repeat area occurs during a transfer of one block, the interrupt by the overflow is suspended until transfer of the block is completed, and the transfer overruns.

Figure 15.8 shows an example when the extended repeat area function is used in block transfer mode.

成为应用该功能的目标。可以通过在中断处理中向DMCNT.DTE位写入1来恢复DMA传输。

图15.7显示了扩展重复区域操作的示例。

八个字节由DMSAR的低三位指定为扩展重复区域（DMAMD.SARA[4:0]位=00011b）。数据大小为8位(DMTMD.SZ[1:0]=00b)。

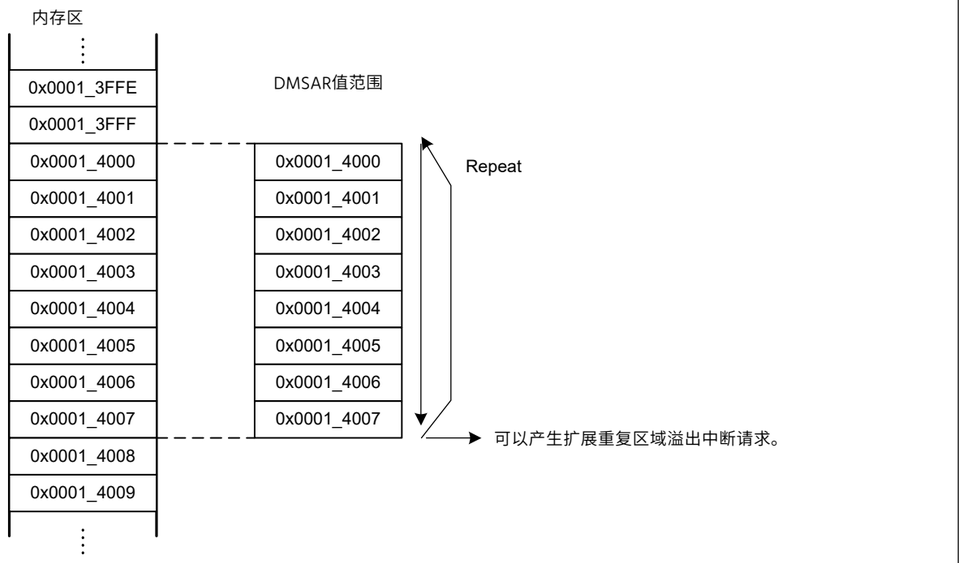


Figure 15.7 扩展重复区域操作示例

在块传输模式下使用扩展重复区域溢出中断时，应考虑以下事项。

当传输因扩展重复区域溢出中断而停止时，地址寄存器必须设置为块大小为2的幂或块大小边界与扩展重复区域边界对齐。当一个块的传输过程中扩展重复区域发生溢出时，溢出的中断被暂停，直到块的传输完成，传输溢出。

图15.8显示了在块传输模式下使用扩展重复区域功能的示例。

Eight bytes are specified as an extended repeat area by the lower three bits of DMSAR (DMAMD.SARA[4:0] bits = 00011b), block transfer mode with block size 5 is set (DMCRA = 0x0005_0005), and transfer source address is not specified as a block area. Data size is eight bits (DMTMD.SZ[1:0] bits = 00b).

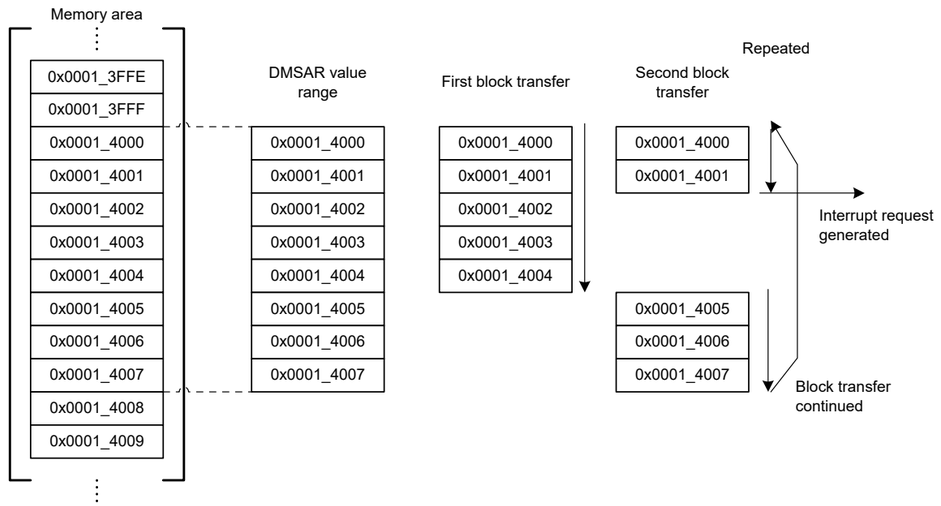


Figure 15.8 Example of Extended Repeat Area Function in Block Transfer Mode

15.3.3 Free-running Function

The DMAC supports free-running function. This function allows to transfer repeatedly without reconfiguring in interrupt handler.

15.3.3.1 In Normal Transfer Mode

In normal transfer mode, when DMCRA.DMCRAL bits are set to 0000h, no specific number of transfer operations is set; data transfer is performed with the transfer counter stopped.

For more information, see section 15.3.1.1. Normal Transfer Mode.

15.3.3.2 In Other Transfer Mode

In repeat, block and repeat-block transfer mode, the DMAC supports free-running function using the DMTMD.TKP bit. If the DMTMD.TKP bit is to be set to 1, the transfer is not stopped by completion of specified total number of transfer operations and reloads DMCRBH repeatedly.

Figure 15.9 show an example of block transfer operation without free-running function.

8个字节被DMSAR的低三位指定为扩展重复区域（DMAMD.SARA[4:0]bits=00011b），设置块大小为5的块传输模式（DMCRA=0x0005_0005），传输源地址为未指定为块区域。数据大小为8位（DMTMD.SZ[1:0]位=00b）。

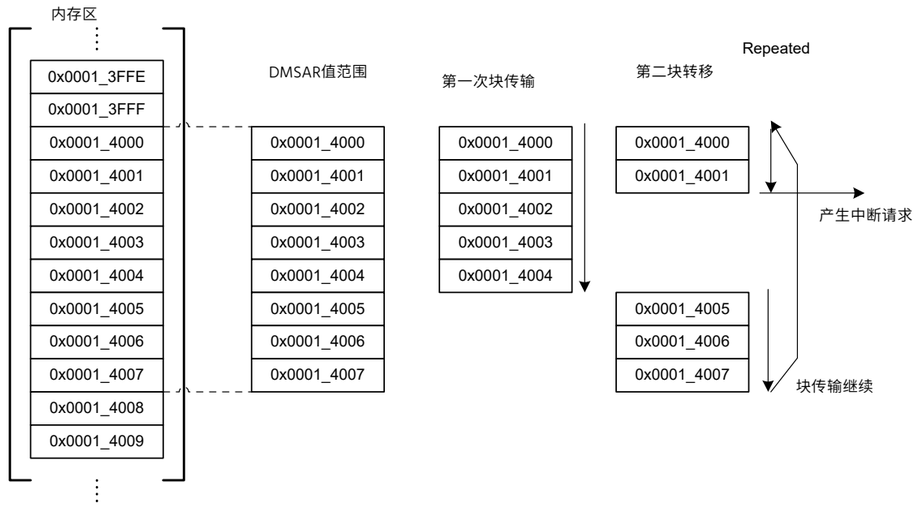


Figure 15.8 块传输模式下的扩展重复区域功能示例

15.3.3 Free-running Function

DMAC支持自由运行功能。此功能允许重复传输而无需在中断处理程序中重新配置。

15.3.3.1 在正常传输模式下

在正常传输模式下，当DMCRA.DMCRAL位设置为0000h时，不设置具体的传输操作数；在传输计数器停止的情况下执行数据传输。

有关详细信息，请参阅第15.3.1.1节。正常传输模式。

15.3.3.2 在其他传输模式下

在重复、块和重复块传输模式下，DMAC使用DMTMD.TKP位支持自由运行功能。如果要设置DMTMD.TKP位为1，则在完成指定的传输操作总数时不会停止传输并重复重新加载DMCRBH。

图15.9显示了一个没有自由运行功能的块传输操作示例。

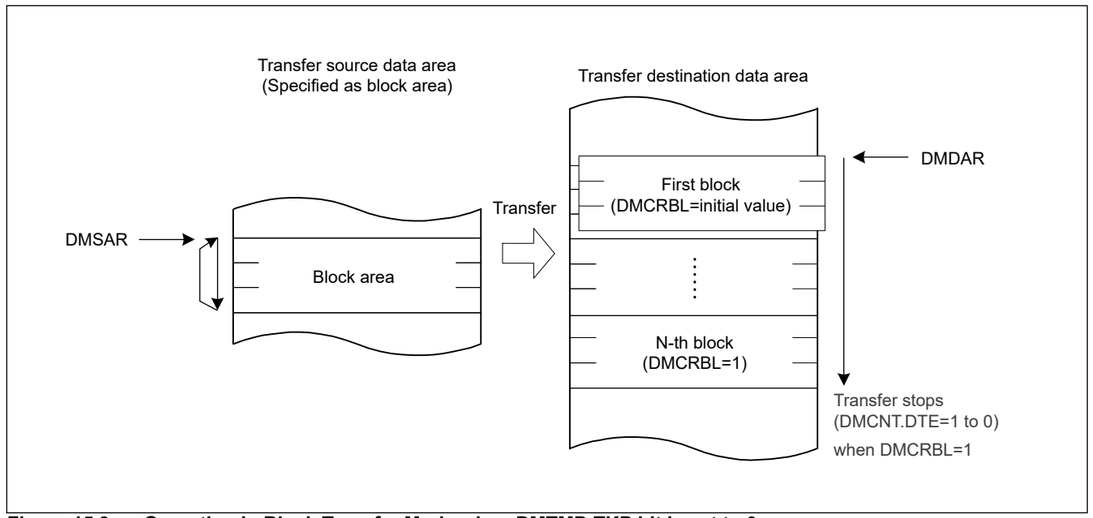


Figure 15.9 Operation in Block Transfer Mode when DMTMD.TKP bit is set to 0

Figure 15.10 show an example of block transfer operation with free-running function.

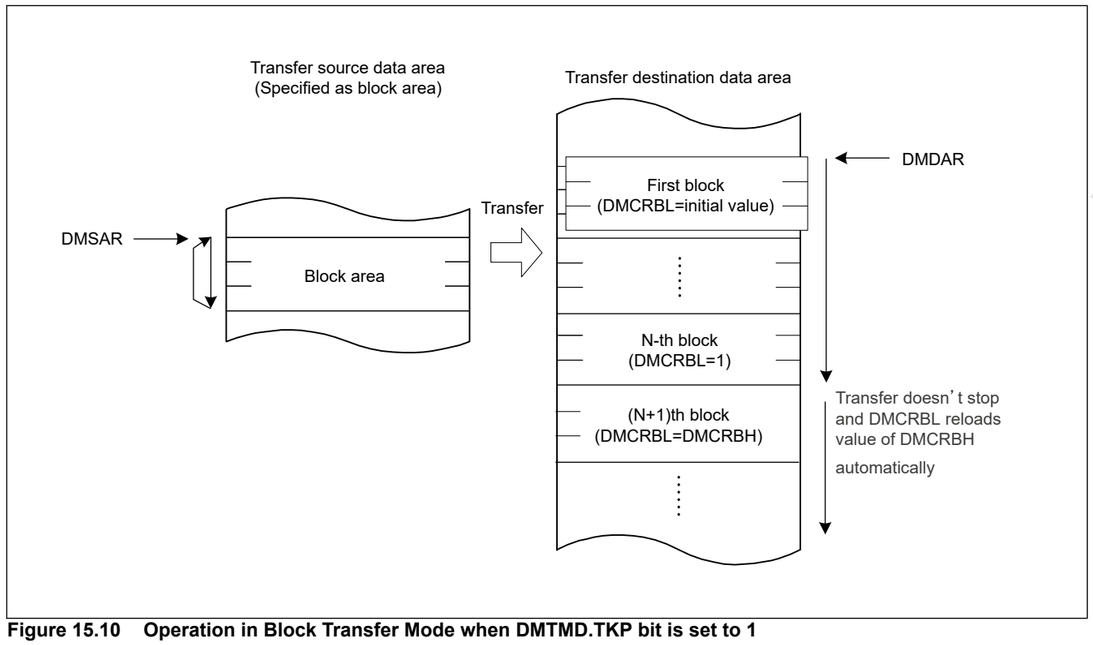


Figure 15.10 Operation in Block Transfer Mode when DMTMD.TKP bit is set to 1

15.3.4 Address Update Function using Offset

The source and destination addresses can be updated by fixing, increment, decrement, or offset addition. In normal, repeat and block transfer mode, when the offset addition is selected, the offset specified by the DMA offset register (DMOFR) is added to the address every time the DMAC performs one data transfer. This function realizes a data transfer where addresses are allocated to separated areas.

Offset subtraction can also be realized by setting a negative value in DMOFR. In this case, the negative value must be 2's complement.

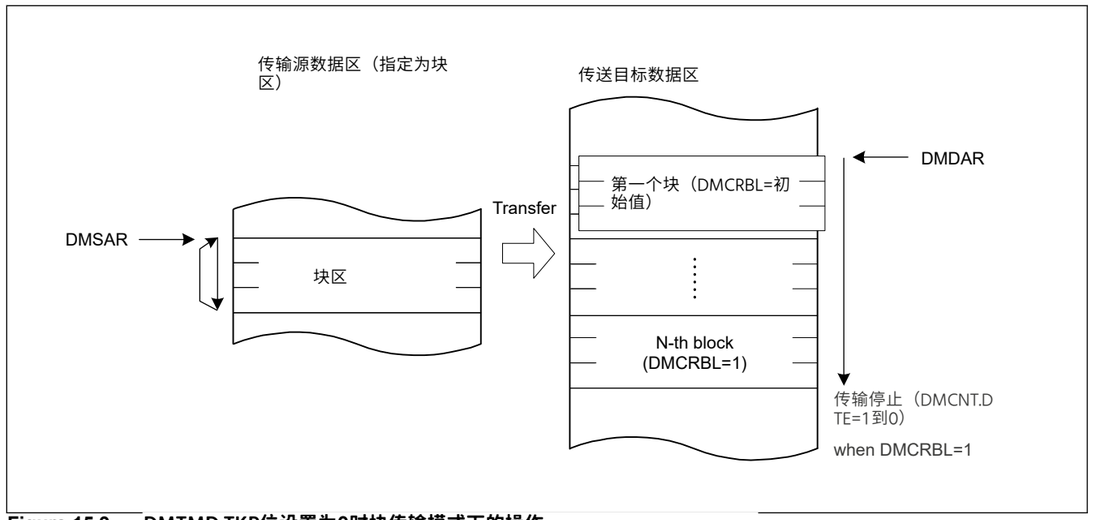


Figure 15.9 DMTMD.TKP位设置为0时块传输模式下的操作

图15.10显示了具有自由运行功能的块传输操作示例。

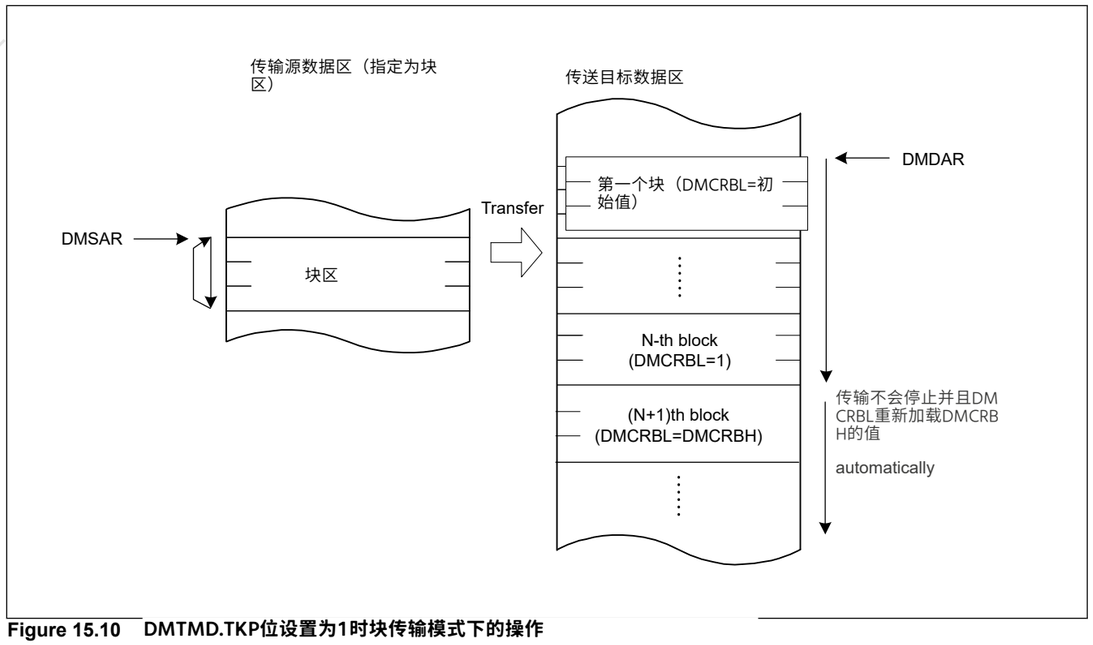


Figure 15.10 DMTMD.TKP位设置为1时块传输模式下的操作

15.3.4 使用偏移的地址更新功能

可以通过固定、递增、递减或偏移添加来更新源地址和目标地址。在正常的重复和块传输模式下，选择偏移添加时，每次DMAC执行一个数据传输时，DMA偏移寄存器（DMOFR）指定的偏移量都会添加到地址。该功能实现了将地址分配到不同区域的数据传输。

偏移量减法也可以通过在DMOFR中设置一个负值来实现。在这种情况下，负值必须是2的补码。

DMSBS or DMDBS are used instead of DMOFR in repeat-block transfer mode. For more information section 15.3.1.4. Repeat-Block Transfer Mode

Table 15.14 shows the address update method in each address update mode.

Table 15.14 Address Update Method in Each Address Update Mode

Address Update Mode	Settings of DMAMD.SM[1:0] and DMAMD.DM[1:0] for Address Update Modes	Address Update Method (for Different SZ[1:0] Settings in DMTMD)		
		SZ[1:0] = 00b	SZ[1:0] = 01b	SZ[1:0] = 10b
Address fixed	00b	Fixed		
Offset addition	01b	+DMOFR*1		
Increment	10b	+1	+2	+4
Decrement	11b	–1	–2	–4

Note 1. When setting a negative value in the DMA Offset Register, the value must be in two's complement, obtained by the following formula:
two's complement of a negative offset value = ~ (offset) + 1 (~ = bit inversion)

15.3.4.1 Basic Transfer Using Offset Addition

Figure 15.11 shows an example of address updating using offset addition.

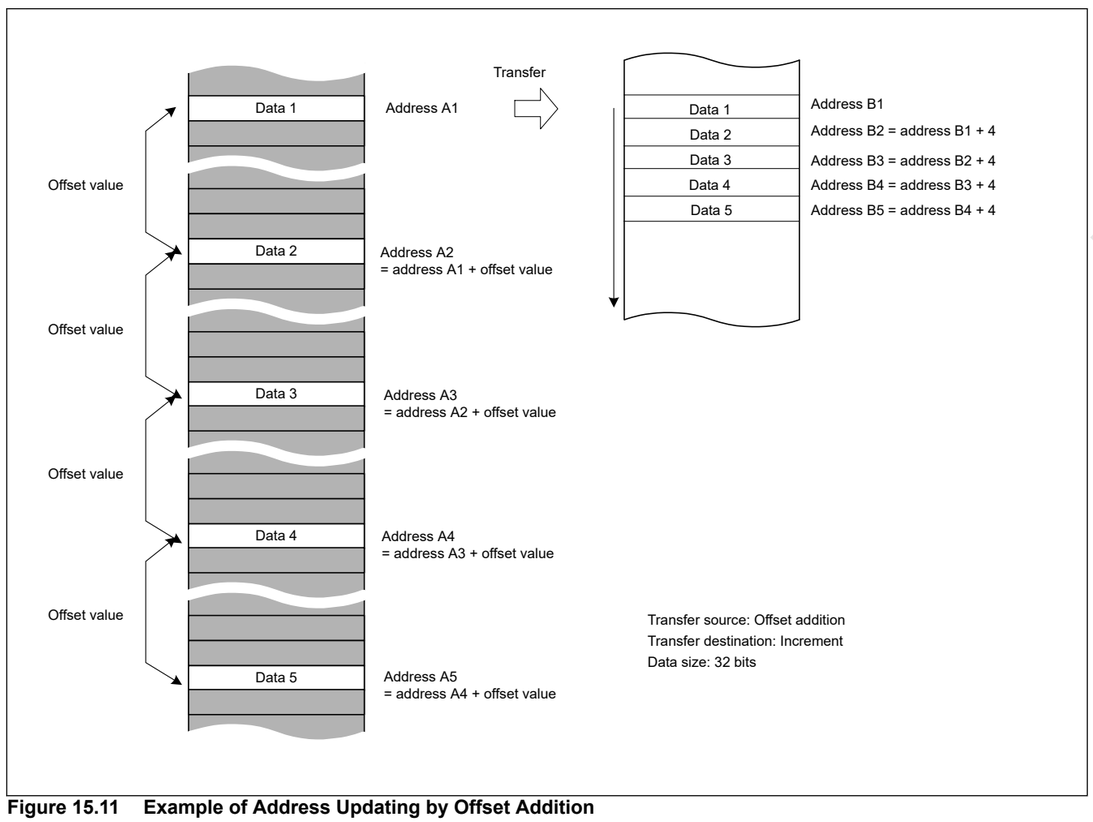


Figure 15.11 Example of Address Updating by Offset Addition

Figure 15.11 shows the setting of the following.

- The transfer data is 32 bits long
- Offset addition is set as the transfer source address update

在重复块传输模式中使用DMSBS或DMDBS代替DMOFR。有关详细信息，请参阅第15.3.1.4节。
重复块传输模式

表15.14显示了每种地址更新模式下的地址更新方法。

Table 15.14 各地址更新模式下的地址更新方法

地址更新模式	DMAMD.SM[1:0]的设置和DMAMD.DM[1:0]用于地址更新Modes	地址更新方法（针对DMTMD中的不同SZ[1:0]设置）		
		SZ[1:0] = 00b	SZ[1:0] = 01b	SZ[1:0] = 10b
地址固定	00b	Fixed		
偏移量加法	01b	+DMOFR*1		
Increment	10b	+1	+2	+4
Decrement	11b	–1	–2	–4

注1.在DMA偏移寄存器中设置负值时，该值必须是二进制补码，由以下公式获得：负偏移值的二进制补码=~(offset)+1(~=bitinversion)

15.3.4.1 使用偏移加法的基本传输

图15.11显示了使用偏移量加法的地址更新示例。

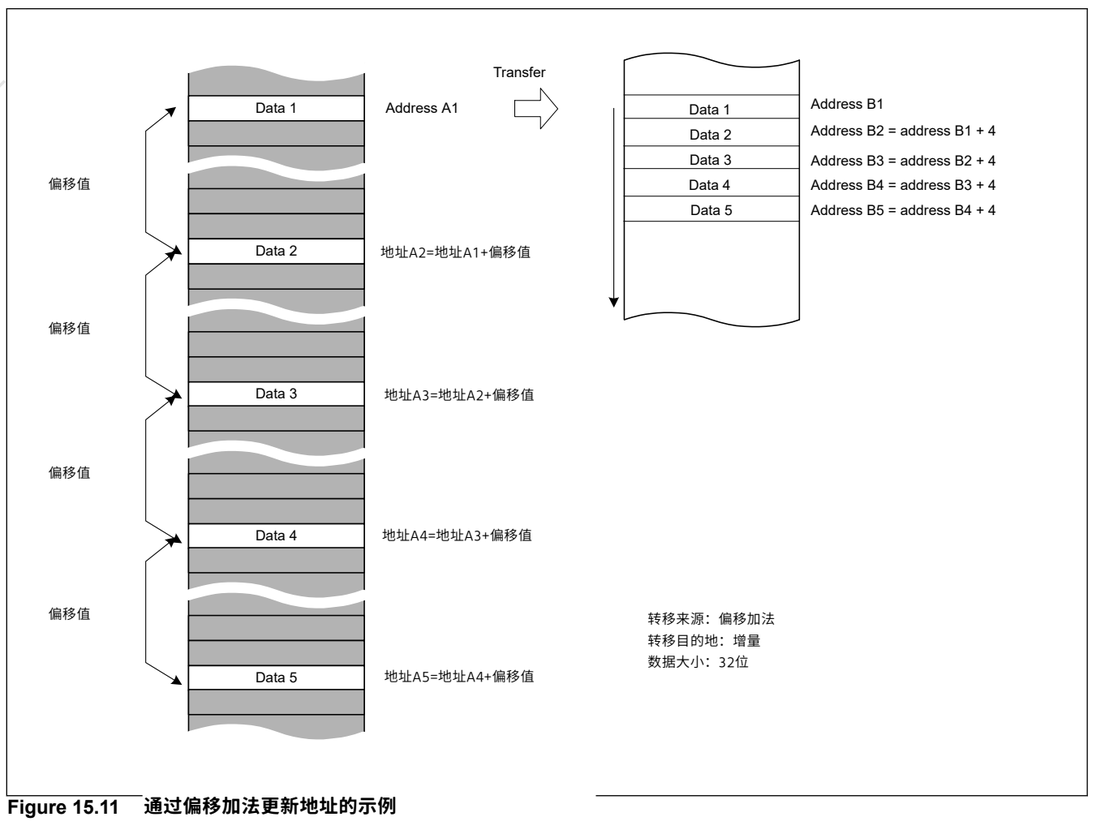


Figure 15.11 通过偏移加法更新地址的示例

图15.11显示了以下设置。

●传输数据为32位长

●偏移量加法设置为传输源地址更新

- Increment is set as the transfer destination address update mode

The second and subsequent data is each read from the transfer source address obtained by adding the offset value to the previous address. The data read from the addresses at the specified intervals is written to the continuous locations on the destination.

15.3.4.2 Example of XY Conversion Using Offset Addition

Figure 15.12 shows the XY conversion using offset addition in repeat transfer mode.

Settings are as follows:

- DMAMD.SM — Transfer source address update mode: Offset addition
- DMAMD.DM — Transfer destination address update mode: Destination address is incremented.
- DMTMD.SZ — Transfer data size select: 32 bits
- DMTMD.MD — Transfer mode select: Repeat transfer
- DMTMD.DTS — Repeat area select: The source is specified as the repeat area.
- DMOFR — Offset address: 0x10
- DMCRA — Repeat size: 0x4
- DMINT.RPTIE — The repeat size end interrupt is enabled.

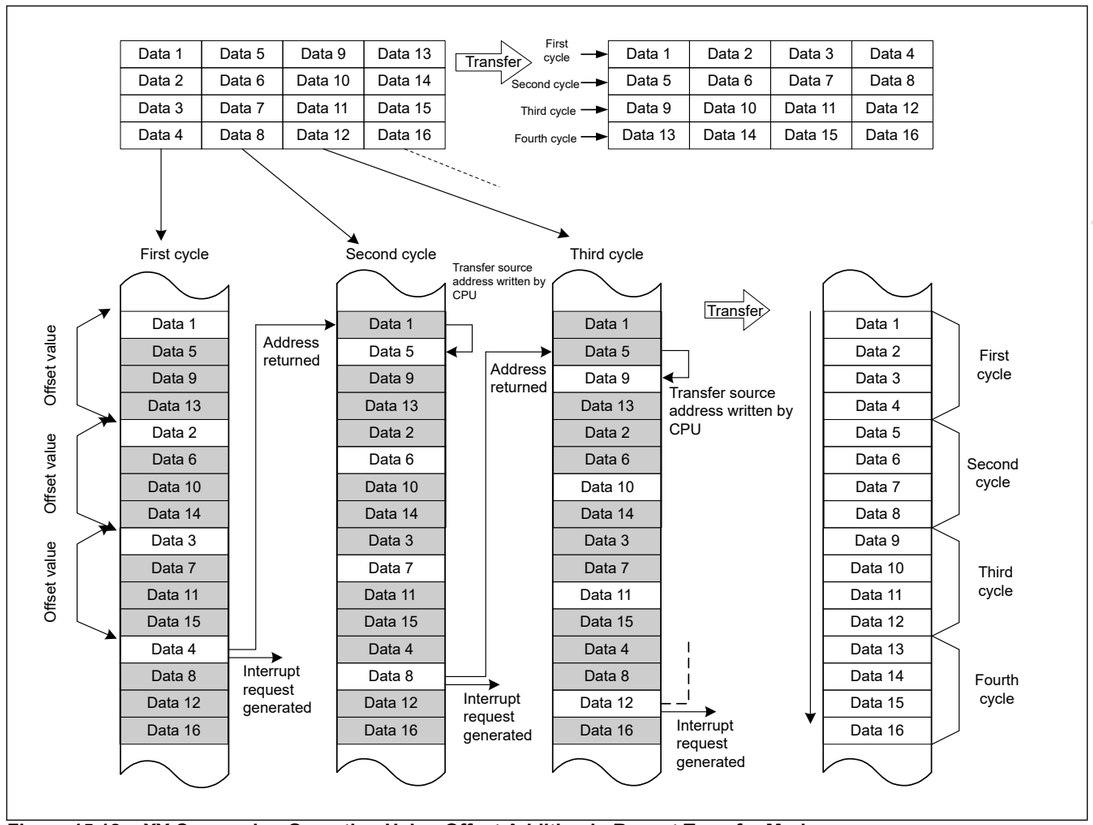


Figure 15.12 XY Conversion Operation Using Offset Addition in Repeat Transfer Mode

When a transfer starts, the offset value is added to the transfer source address every time data is transferred. The transfer data is written to continuous transfer destination addresses. When data 4 is transferred:

- The repeat size of data transfer is complete.

●增量设置为传输目标地址更新模式

第二个和随后的数据分别从通过将偏移值与前一个地址相加而获得的传输源地址读取。以指定间隔从地址读取的数据被写入目标上的连续位置。

15.3.4.2 使用偏移加法的XY转换示例

图15.12显示了在重复传输模式下使用偏移添加的XY转换。

设置如下：

●DMAMD.SM—传输源地址更新模式：偏移量加法

●DMAMD.DM—传输目标地址更新模式：目标地址递增。

●DMTMD.SZ—传输数据大小选择：32位

●DMTMD.MD—传输模式选择：重复传输

●DMTMD.DTS—重复区域选择：源被指定为重复区域。

- DMOFR — Offset address: 0x10
- DMCRA — Repeat size: 0x4

●DMINT.RPTIE—启用重复大小结束中断。

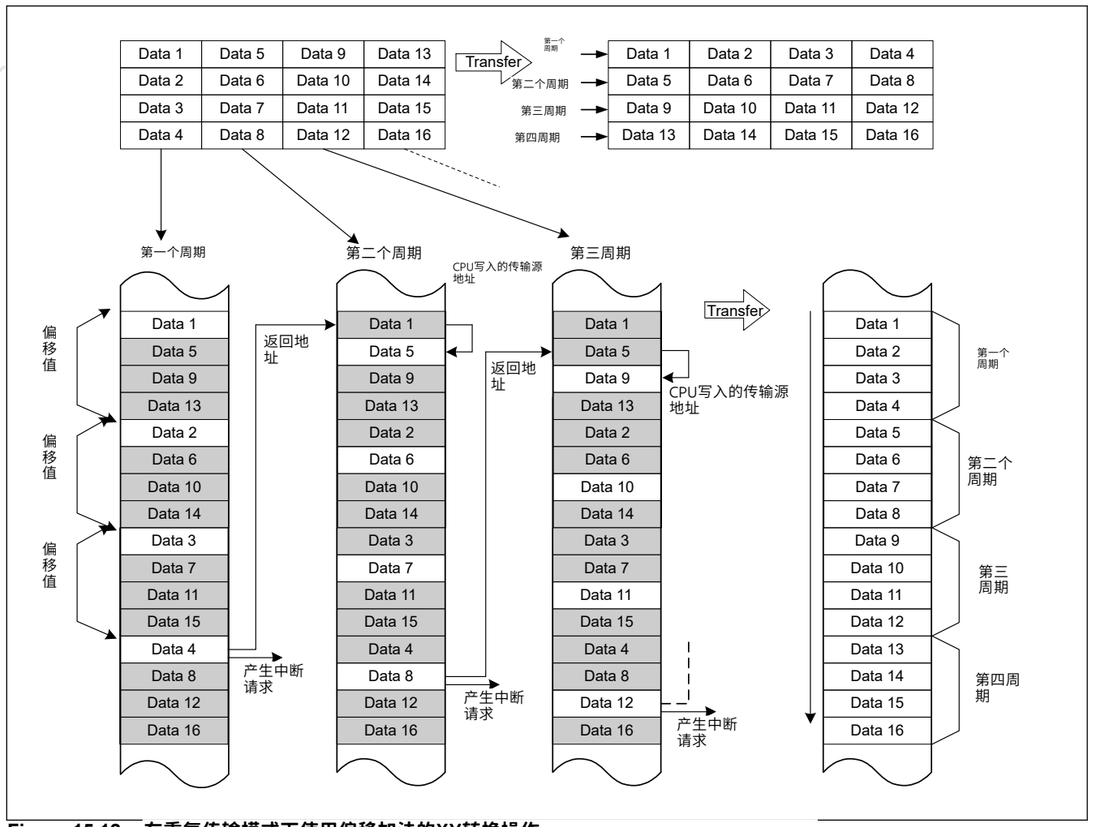


Figure 15.12 在重复传输模式下使用偏移加法的XY转换操作

传输开始时，每次传输数据时，都会将偏移值添加到传输源地址。传输数据被写入连续的传输目标地址。传输数据4时：

●数据传输的重复大小已完成。

- The transfer source address returns to the transfer start address (the address of data 1 on the transfer source).
- A repeat size end interrupt is requested.

During the time this interrupt pauses the transfer, the following operations are performed.

- DMSAR — Rewrite the DMA transfer source address to the address of data 5 (with the above example, the data 1 address + 4).
- DMCNT — Set the DTE bit to 1.

The DMA transfer is resumed from the state when the DMA transfer is stopped. After that, the operations described above are repeated until the transfer source data is transposed to the destination area (XY conversion).

Figure 15.13 shows a flowchart of the XY conversion.

●传输源地址返回传输起始地址（传输源上数据1的地址）。

●请求重复大小结束中断。

在此中断暂停传输期间，将执行以下操作。

●DMSAR—将DMA传输源地址重写为数据5的地址（在上面的示例中，数据1地址+4）。

●DMCNT—将DTE位设置为1。

DMA传输从DMA传输停止时的状态恢复。之后，重复上述操作，直到将传送源数据转置到目的地区域（XY转换）。

图15.13显示了XY转换的流程图。

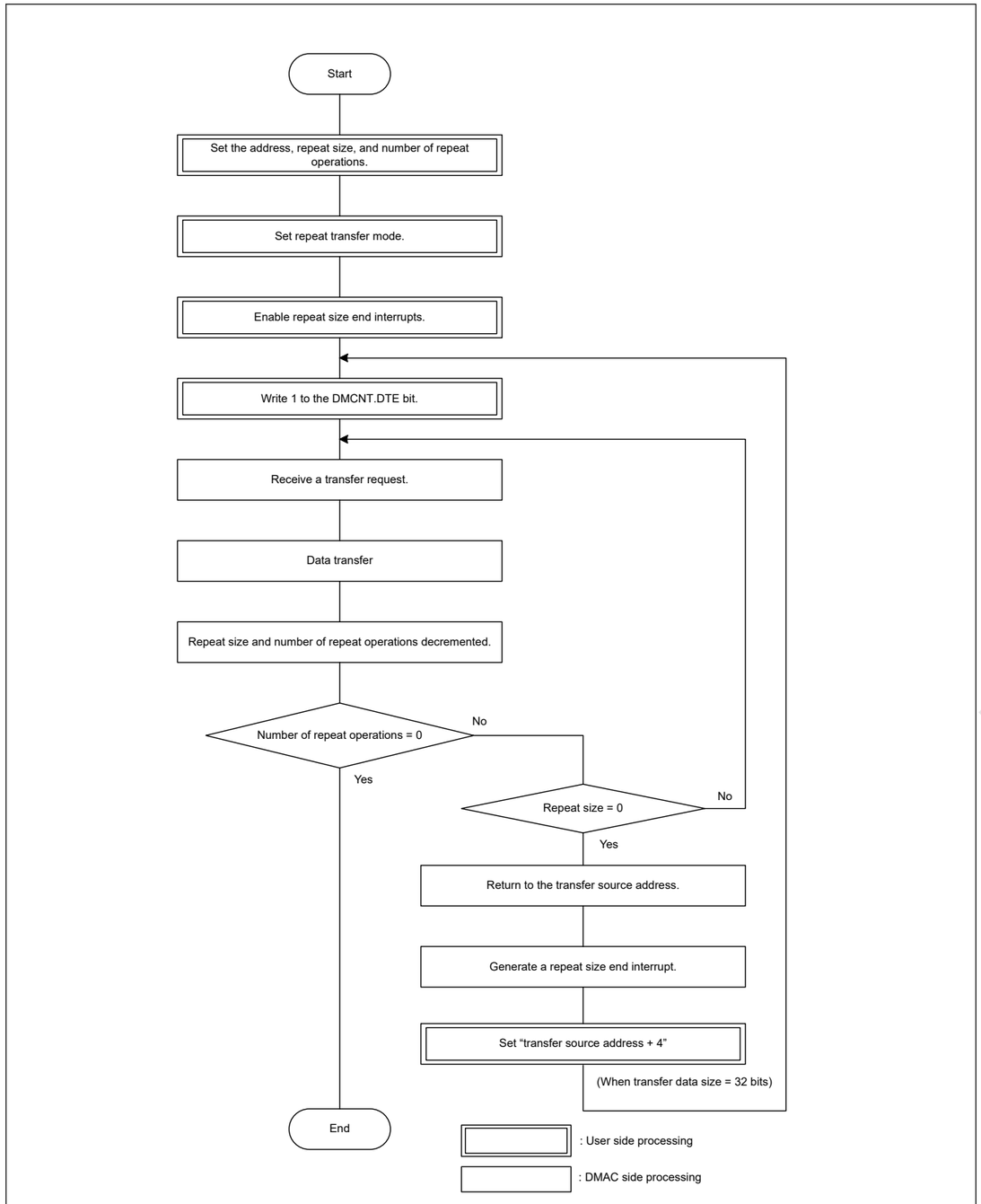


Figure 15.13 XY Conversion Flowchart Using Offset Addition in Repeat Transfer Mode

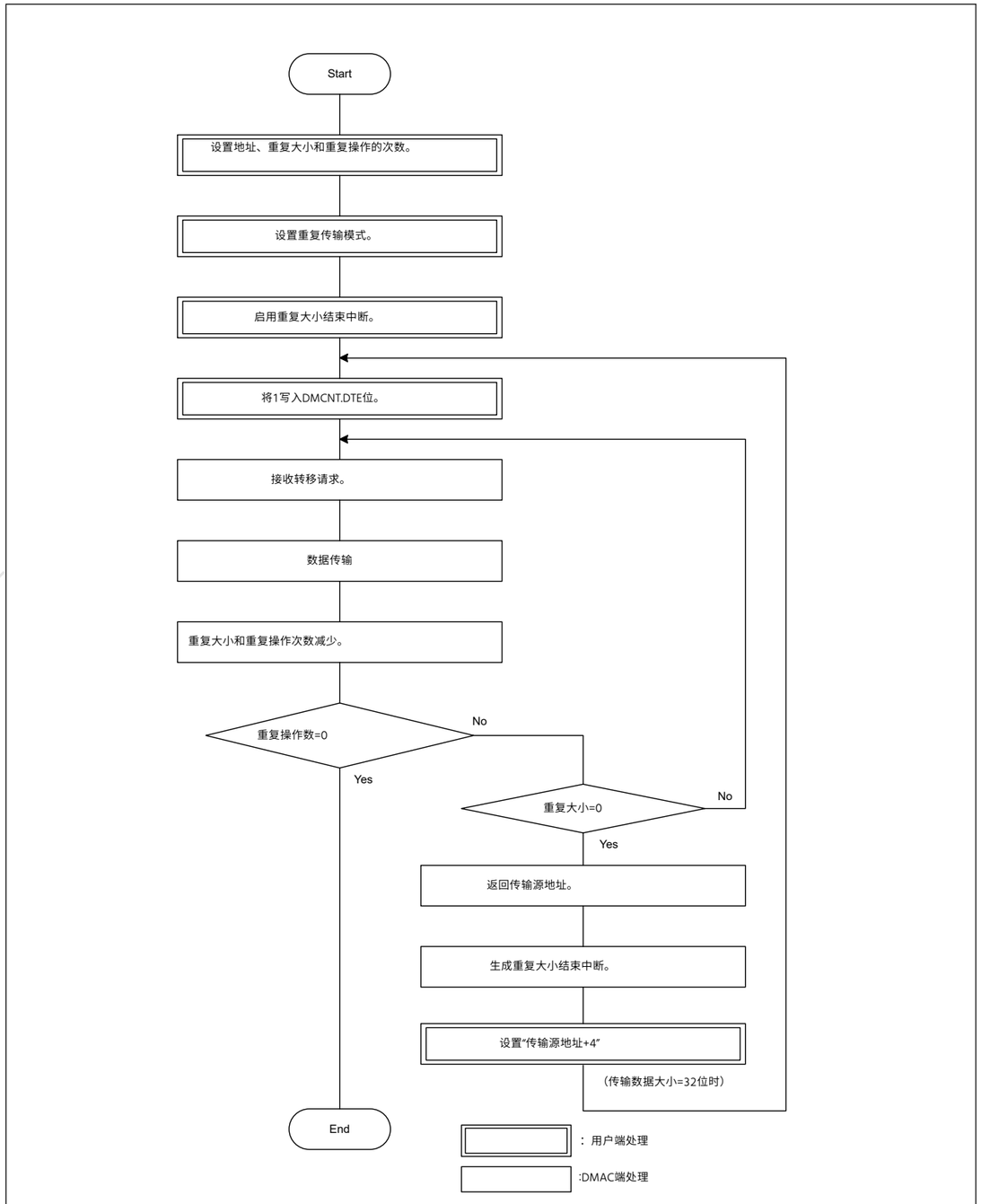


Figure 15.13 重复传输模式下使用偏移加法的XY转换流程图

15.3.5 Address Update Function in Repeat-Block Transfer Mode

Repeat-block transfer mode is an extension of repeat transfer mode and block transfer mode. However, the detailed behavior of the address update is different from these two modes. Here are the details of the address update function in repeat-block transfer mode.

15.3.5.1 Fixed Address Mode

When DMAMD.SM[1:0] is set to 00b, the address update mode of the source is fixed address. And when DMAMD.DM[1:0] is set to 00b, the address update mode of the destination is fixed address.

In fixed address, the address is not updated from the initial value of DMSAR and DMDAR. If the block size (DMCRA) is larger than 1, the same data will be transferred multiple times for one request.

Figure 15.14 shows address update in fixed address.

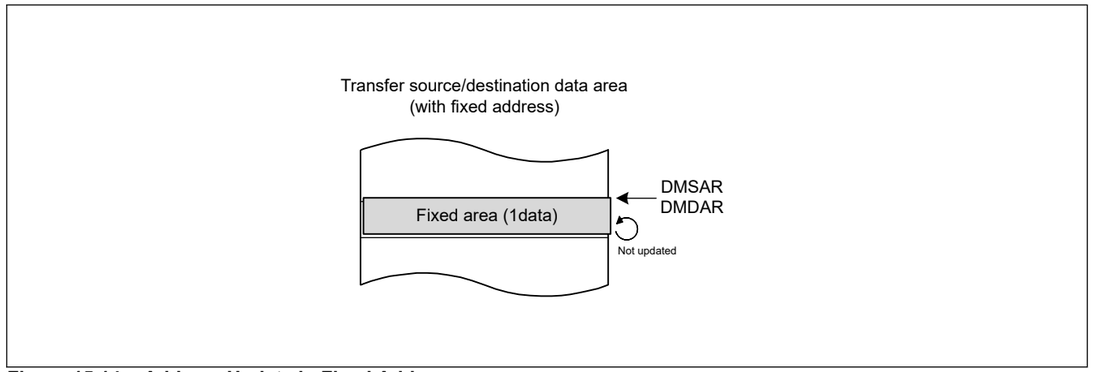


Figure 15.14 Address Update in Fixed Address

15.3.5.2 Incremental and Decremental Address mode

When DMAMD.SM[1:0] is set to 10b, the address update mode of the source is incremental address. And when DMAMD.DM[1:0] is set to 10b, the address update mode of the destination is incremental address. When DMAMD.SM[1:0] is set to 11b, the address update mode of the source is decremental address. And when DMAMD.DM[1:0] is set to 11b, the address update mode of the destination is decremental address.

In these update modes, the address is incremented or decremented according to the setting of DMTMD.SZ[1:0].

In these update modes DMSBS and DMDBS indicates a reload area. The unit of DMSBS and DMDBS is "number of data". At the start of transfer, DMSBSL and DMDBSL, which is the lower 16 bits of DMSBS and DMDBS, operates as a down counter and decrements each time one data transfer is performed. When the value becomes 1, DMSAR and DMDAR reloads the value of DMSRR and DMDRR.

Figure 15.15 shows address update in incremental address.

15.3.5 重复块传输模式中的地址更新功能

重复块传输模式是重 复传输模式和块传输模式的扩展。但是，地址更新的详细行为与这两种模式不同。以下是重复块传输模式下地址更新功能的详细信息。

15.3.5.1 固定地址模式

当DMAMD.SM[1:0]设置为00b时，源的地址更新方式为固定地址。什么时候DMAMD.DM[1:0]设置为00b，目的地址更新方式为固定地址。

在固定地址中，地址不会从DMSAR和DMDAR的初始值更新。如果块大小（DMCRA）大于1，则一个请求将多次传输相同的数据。

图15.14显示了固定地址中的地址更新。

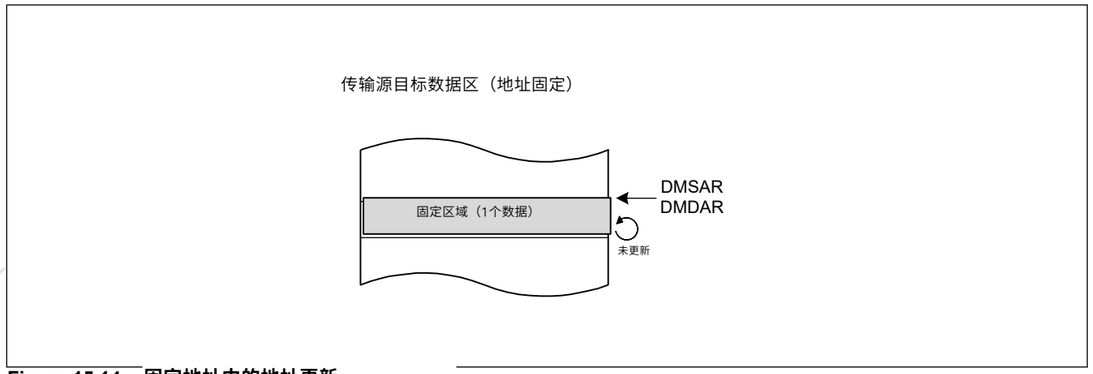


Figure 15.14 固定地址中的地址更新

15.3.5.2 递增和递减地址模式

当DMAMD.SM[1:0]设置为10b时，源地址更新方式为增量地址。什么时候DMAMD.DM[1:0]设置为10b，目的地址更新方式为增量地址。当DMAMD.SM[1:0]设置为11b时，源地址更新方式为递减地址。什么时候

DMAMD.DM[1:0]设置为11b，目的地址更新方式为递减地址。

在这些更新模式中，地址根据DMTMD.SZ[1:0]的设置递增或递减。

在这些更新模式中，DMBSS和DMDBS表示重新加载区域。DMSBS和DMDBS的单位是"数据数"。在传输开始时，作为DMSBS和DMDBS的低16位的DMSBSL和DMDBSL作为递减计数器运行，并在每次执行数据传输时递减。当值变为1时，DMSAR和DMDAR重新加载DMSRR和DMDRR的值。

图15.15显示了增量地址中的地址更新。

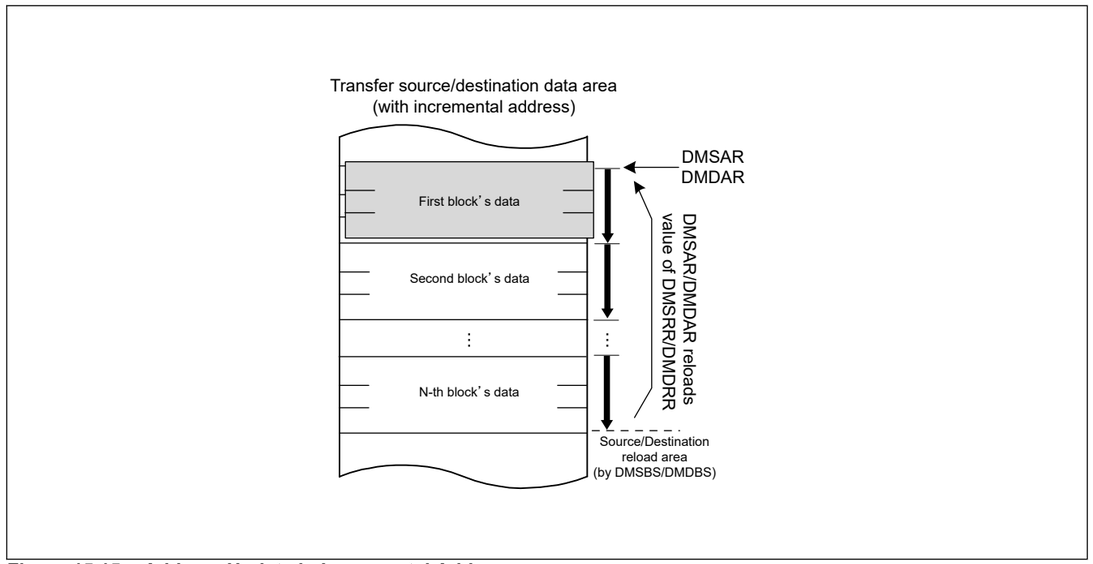


Figure 15.15 Address Update in Incremental Address

15.3.5.3 Offset Addition Mode

When DMAMD.SM[1:0] is set to 01b, the address update mode of the source is offset addition. And when DMAMD.DM[1:0] is set to 01b, the address update mode of the destination is offset addition.

In offset addition, DMSBS and DMDBS indicates reload area and also works as an access offset value. Unlike other transfer modes, DMOFR register is not used in repeat-block transfer mode. In offset addition, the unit of DMSBS and DMDBS is the number of blocks. When the transfer starts, DMCRAL operates as a down counter, DMSAR and DMDAR reloads the value of DMSRR and DMDRR every time one block is transferred. In addition, DMSBSL and DMDBSL, which is the lower 16 bits of DMSBS and DMDBS, also operates as a down counter and decrements every time one block is transferred. When the DMSBS and DMDBS value becomes 1, DMSAR and DMDAR reloads the value of DMSRR and DMDRR.

When DMAMD.SADR and DMAMD.DADR is set to 0, offset addition operation of the same area is repeated. DMDAR only reloads DMDRR. section 15.3.5.3. Offset Addition Mode shows address update in offset addition with DMAMD.SADR and DMAMD.DADR=0.

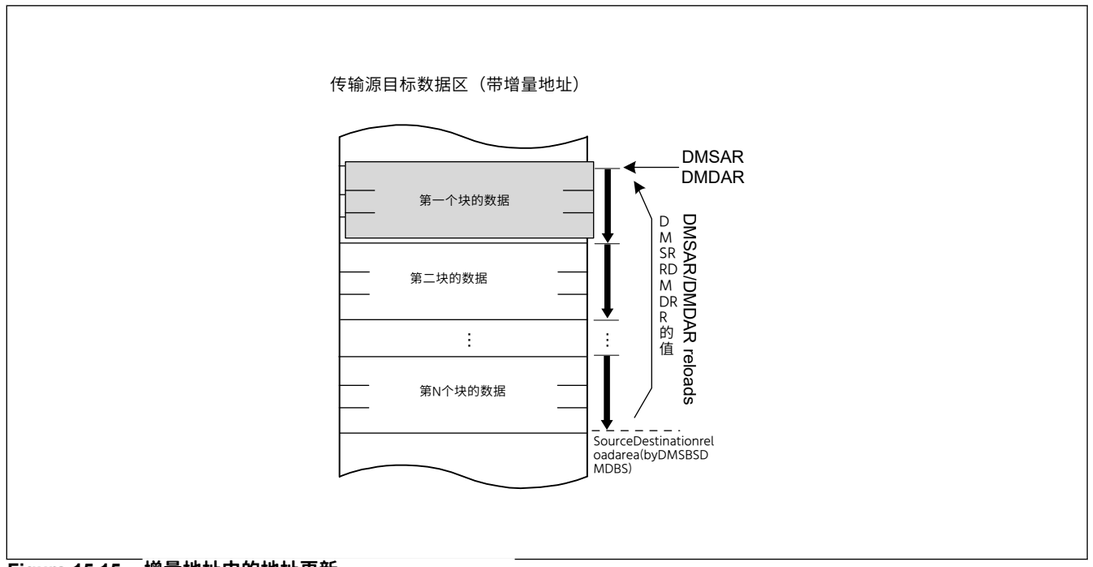


Figure 15.15 增量地址中的地址更新

15.3.5.3 偏移加法模式

当DMAMD.SM[1:0]设置为01b时，源地址更新方式为偏移加法。什么时候DMAMD.DM[1:0]设置为01b，目的地址更新方式为偏移加法。

除了偏移量之外，DMBSS和DMDBS表示重载区域，也用作访问偏移量值。与其他传输模式不同，DMOFR寄存器不用于重复块传输模式。除了偏移量之外，DMSBS和DMDBS的单位是块数。当传输开始时，DMCRAL作为一个递减计数器运行，DMSAR和DMDAR在每次传输一个块时重新加载DMSRR和DMDRR的值。此外，作为DMSBS和DMDBS的低16位的DMSBSL和DMDBSL也用作递减计数器，并且每传输一个块就递减。当DMSBS和DMDBS的值变为1时，DMSAR和DMDAR重新加载DMSRR和DMDRR的值。

当DMAMD.SADR和DMAMD.DADR设置为0时，重复相同区域的偏移添加操作。DMDAR仅重新加载DMDRR。第15.3.5.3节。偏移加法模式显示偏移加法中的地址更新，其中DMAMD.SADR和DMAMD.DADR=0。

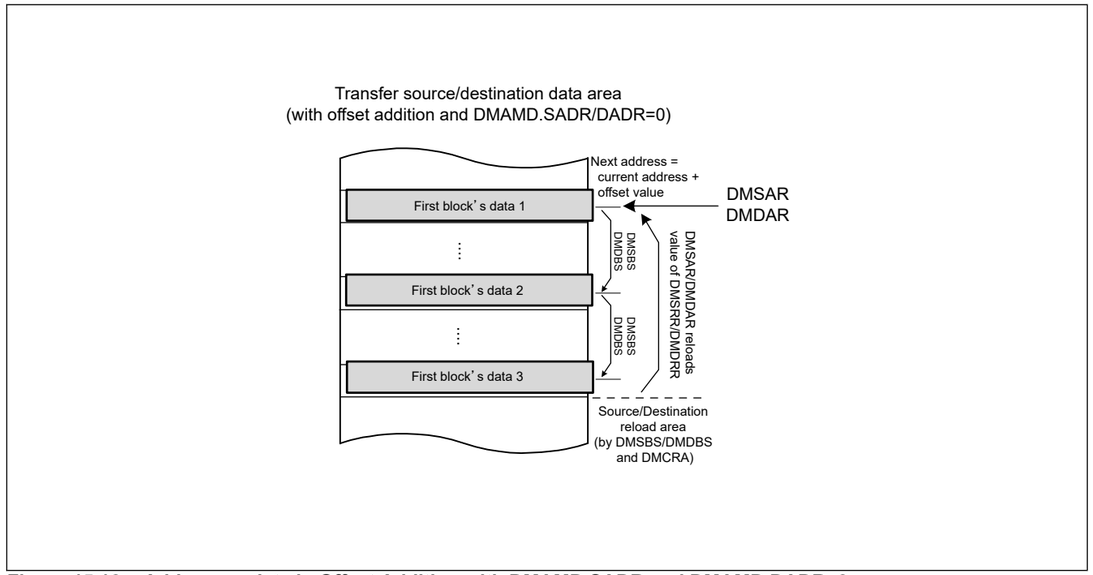


Figure 15.16 Address update in Offset Addition with DMAMD.SADR and DMAMD.DADR=0

When DMAMD.SADR and DMAMD.DADR is set to 1, the address is incremented by one data unit after DMSRR and DMDRR is reloaded by DMCRAL=1. In other words, an index value ((DMDBSH-DMDBSL) × DataSize) is added to DMDAR after DMDRR is reloaded. This behavior is used to implement multiple ring buffers. Figure 15.17 shows address update in offset addition with DMAMD.SADR and DMAMD.DADR=1.

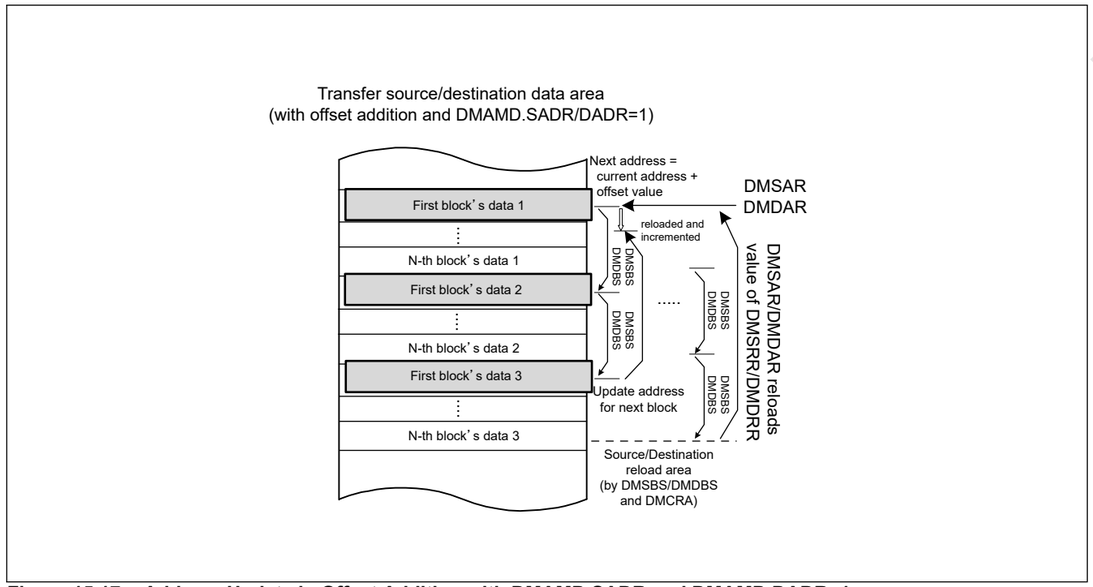


Figure 15.17 Address Update in Offset Addition with DMAMD.SADR and DMAMD.DADR=1

15.3.6 Example of Using Repeat-Block Transfer Mode

In repeat-block transfer mode, it is possible to realize repeated access to interval data and single or multiple ring buffers by combining the above address update modes. Following sections shows some usage examples.

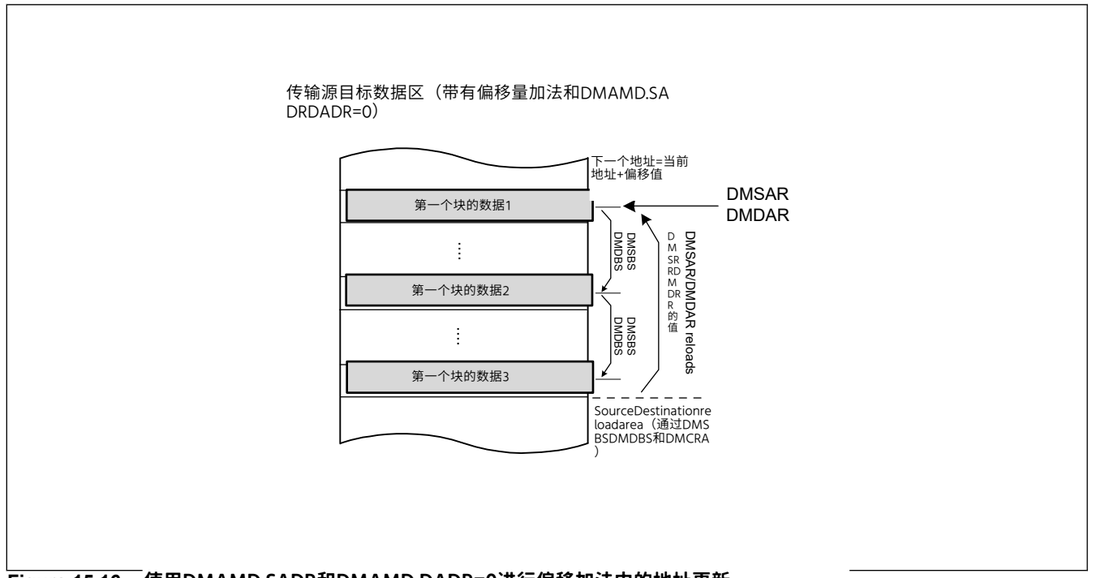


Figure 15.16 使用DMAMD.SADR和DMAMD.DADR=0进行偏移加法中的地址更新

当DMAMD.SADR和DMAMD.DADR设置为1时，在DMSRR和DMCRAL=1重新加载DMDRR后，地址增加一个数据单元。换句话说，一个索引值((DMDBSH-DMDBSL)×DataSize)被添加到
重新加载DMDRR后的DMDAR。此行为用于实现多个环形缓冲区。图15.17显示了DMAMD.SADR和DMAMD.DADR=1的偏移加法中的地址更新。

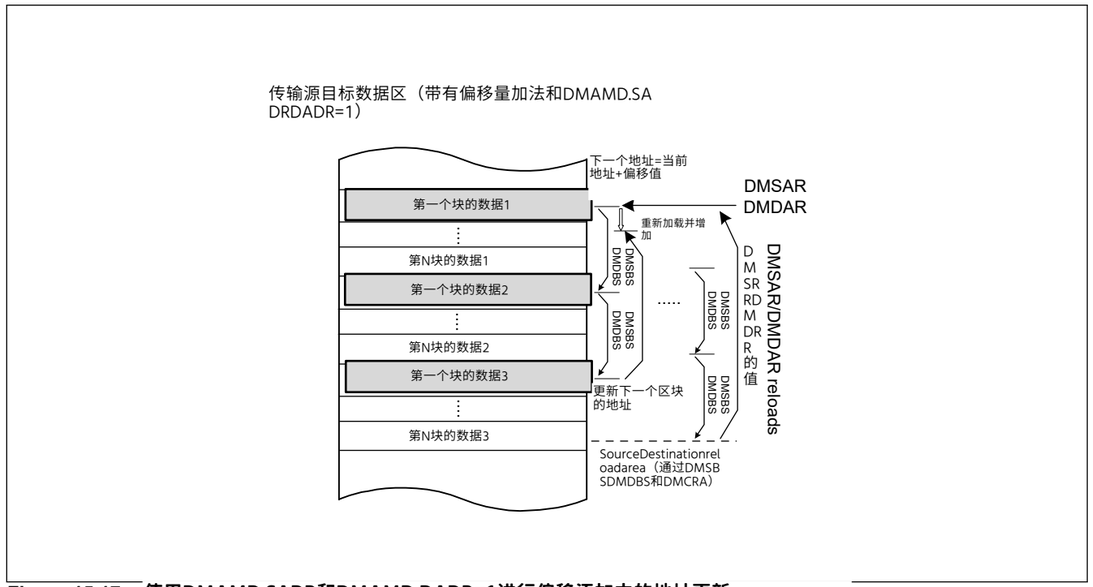


Figure 15.17 使用DMAMD.SADR和DMAMD.DADR=1进行偏移添加中的地址更新

15.3.6 使用重复块传输模式的示例

在重复块传输模式下，结合上述地址更新模式，可以实现对区间数据和单个或多个环形缓冲区的重复访问。以下部分显示了一些使用示例。

15.3.6.1 Interval Address to Single Ring Buffer

Figure 15.18 shows an example of reading interval ADDRn registers (data register) of ADC module and storing it in single ring buffer. It transfers 2 data every 4 words per 1 request. DMSAR is incremented by one data every one request. This can be achieved by setting the transfer source to offset addition and DMAMD.SADR=1, the block size (DMCRA) to 2, and the transfer source offset (DMSBS) to 4. Table 15.15 shows setting of this example.

Table 15.15 Setting of use case: from interval address to single ring buffer

Register	Value	Description
DMSAR, DMSRR	0x4017_1000	Initial source address
DMDAR, DMDRR	0x2000_0000	Initial destination address
DMTMD.SZ[1:0]	10b	Data size is word
DMAMD.SADR	1	Incremental source address after reloading
DMAMD.SM[1:0]	01b	Source update mode is offset addition
DMAMD.DM[1:0]	10b	Destination update mode is incremental address
DMCRAH, DMCRAL	2	Transfer block size
DMSBSH, DMSBSL	4	Source whole buffer size (unit is 'blocks') and Source access offset (unit is 'data')
DMDBSH, DMDBSL	N × 2(DMCRA)	Destination buffer size (unit is 'data')

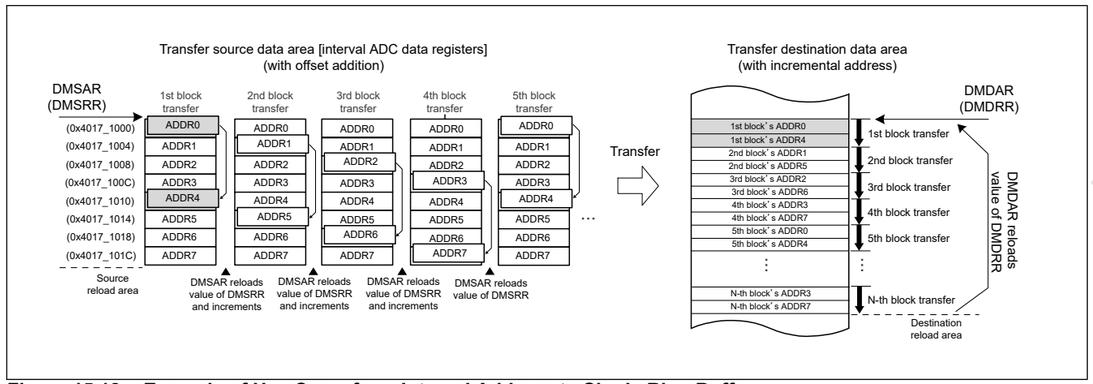


Figure 15.18 Example of Use Case: from Interval Address to Single Ring Buffer

15.3.6.2 Single Block to Multi Ring Buffer

Figure 15.19 shows an example of storing the continuous ADDRn registers (data register) of ADC module individually in multiple ring buffers. In this example, a ring buffer in which only the first element (ADDR0) in a single block is arranged in transfer order is created at the destination. Also, in the next area, create a ring buffer in which only the second element (ADDR1) is arranged in transfer order. In the following case, create a ring buffer of length N, which is defined by DMDBS. And the number of data elements in the block is 3, which is defined by DMCRA. Table 15.16 shows setting of this example.

Table 15.16 Setting of use case: from single block to multi ring buffer (1 of 2)

Register	Value	Description
DMSAR, DMSRR	0x4017_1000	Initial source address
DMDAR, DMDRR	0x2000_0000	Initial destination address
DMTMD.SZ[1:0]	10b	Data size is word
DMAMD.SADR	0	Only reloading
DMAMD.DADR	1	Incremental destination address after reloading

15.3.6.1 单个环形缓冲区的间隔地址

图15.18显示了读取ADC模块的间隔ADDRn寄存器（数据寄存器）并将其存储在单个环形缓冲区中的示例。它每1个请求每4个字传输2个数据。DMSAR每请求一个数据就增加一个数据。这可以通过将传输源设置为偏移加法和DMAMD.SADR=1，将块大小(DMCRA)设置为2，将传输源偏移量(DMSBS)设置为4来实现。表15.15显示了此示例的设置。

Table 15.15 用例设置：从区间地址到单环缓冲区

Register	Value	Description
DMSAR, DMSRR	0x4017_1000	初始源地址
DMDAR, DMDRR	0x2000_0000	初始目标地址
DMTMD.SZ[1:0]	10b	数据大小为字
DMAMD.SADR	1	重载后增量源地址
DMAMD.SM[1:0]	01b	源更新方式为偏移量加法
DMAMD.DM[1:0]	10b	目标更新方式为增量地址
DMCRAH, DMCRAL	2	传输块大小
DMSBSH, DMSBSL	4	源整个缓冲区大小（单位是"块"）和源访问偏移量（单位是"数据"）
DMDBSH, DMDBSL	N × 2(DMCRA)	目标缓冲区大小（单位是"数据"）

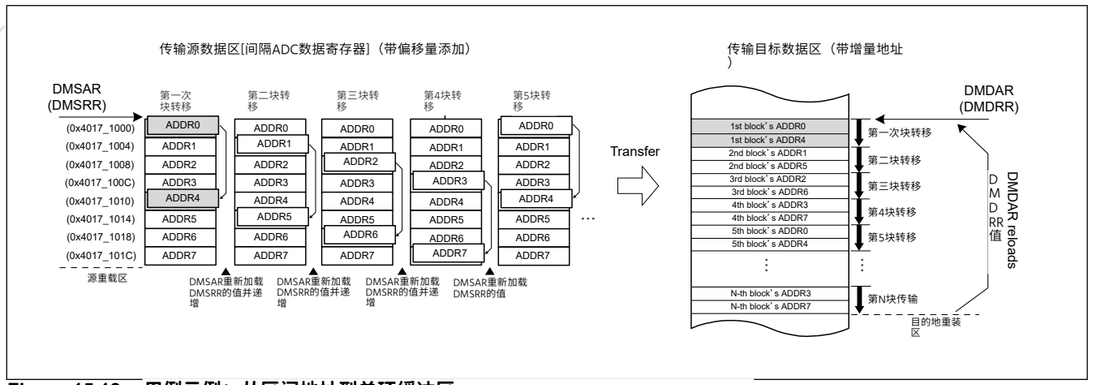


Figure 15.18 用例示例：从区间地址到单环缓冲区

15.3.6.2 单块到多环缓冲区

图15.19显示了将ADC模块的连续ADDRn寄存器（数据寄存器）单独存储在多个环形缓冲区中的示例。在此示例中，在目的地创建了一个环形缓冲区，其中仅单个块中的第一个元素（ADDR0）按传输顺序排列。此外，在下一个区域中，创建一个环形缓冲区，其中只有第二个元素(ADDR1)按传输顺序排列。在以下情况下，创建一个长度为N的环形缓冲区，由DMDBS定义。块中的数据元素个数为3，由DMCRA定义。表15.16显示了此示例的设置。

Table 15.16 用例设置：从单块到多环缓冲区（1of2）

Register	Value	Description
DMSAR, DMSRR	0x4017_1000	初始源地址
DMDAR, DMDRR	0x2000_0000	初始目标地址
DMTMD.SZ[1:0]	10b	数据大小为字
DMAMD.SADR	0	只重装
DMAMD.DADR	1	重新加载后的增量目标地址

Table 15.16 Setting of use case: from single block to multi ring buffer (2 of 2)

Register	Value	Description
DMAMD.SM[1:0]	10b	Source update mode is incremental address
DMAMD.DM[1:0]	01b	Destination update mode is offset addition
DMCRAH, DMCRAL	3	Transfer block size
DMSBSH, DMSBSL	3	Source buffer size (unit is 'data')
DMDBSH, DMDBSL	N	Destination whole buffer size (unit is 'blocks') and Destination access offset (unit is 'data')

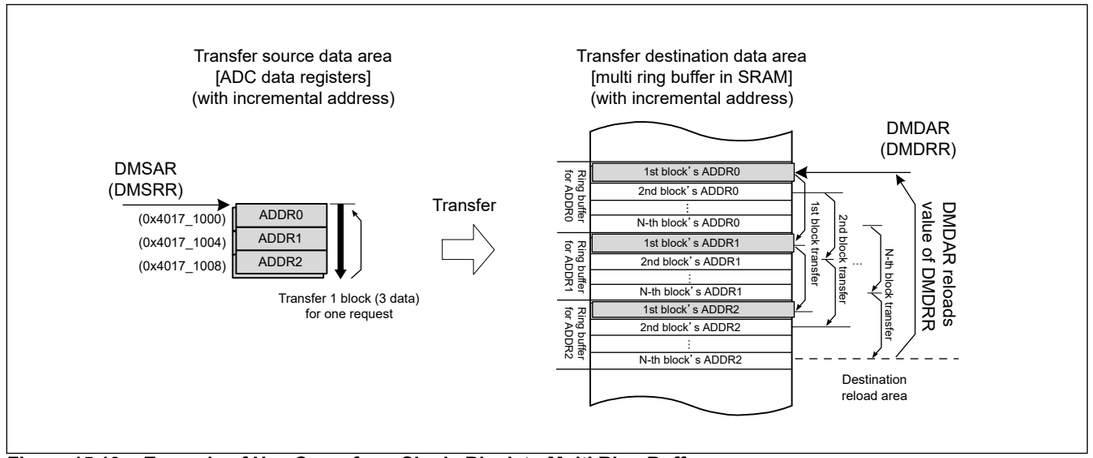


Figure 15.19 Example of Use Case: from Single Block to Multi Ring Buffer

15.3.7 Activation Sources

Software, interrupt requests from the peripheral modules, and external interrupt requests can all be specified as DMAC activation sources. Set the DMTMD.DCTG[1:0] bits to select the activation source.

15.3.7.1 DMAC Activation by Software

When start DMA transfer by software, follow below procedure.

1. Set the DMTMD.DCTG[1:0] bits to 00b
2. Set the DMCNT.DTE bit to 1 (DMA transfer is enabled)
3. Set the DMAST.DMST bit set to 1 (DMAC activation enabled)
4. Set the DMREQ.SWREQ bit to 1 (DMA requested)

When the DMAC is activated by software while the DMREQ.CLRS bit is 0, the DMREQ.SWREQ bit is cleared to 0 after data transfer is started in response to a DMA transfer request.

When the DMAC is activated by software while the CLRS bit is 1, the SWREQ bit is not cleared to 0 after data transfer is started. In this case, a DMA transfer request is issued again after completion of a transfer.

15.3.7.2 DMAC Activation through Interrupt Requests from On-Chip Peripheral Modules or External Interrupt Requests

You can specify interrupt requests from on-chip peripheral modules and external interrupt requests as DMAC activation sources. The activation sources can be selected individually for each channel in ICU.DELSRn.DELS[8:0] (n = 0 to 7).

To start DMA transfer through an interrupt request from an on-chip peripheral module or an external interrupt request, follow the procedures as indicated below.

1. Set ICU.DELSRn.DELS[8:0] (n = 0 to 7) to the event number (select the DMAC event link).

Table 15.16 用例设置：从单块到多环缓冲区（2of2）

Register	Value	Description
DMAMD.SM[1:0]	10b	源更新方式为增量地址
DMAMD.DM[1:0]	01b	目的地更新方式为偏移量加法
DMCRAH, DMCRAL	3	传输块大小
DMSBSH, DMSBSL	3	源缓冲区大小（单位是"数据"）
DMDBSH, DMDBSL	N	目标整个缓冲区大小（单位是"块"）和目标访问偏移量（单位是"数据"）

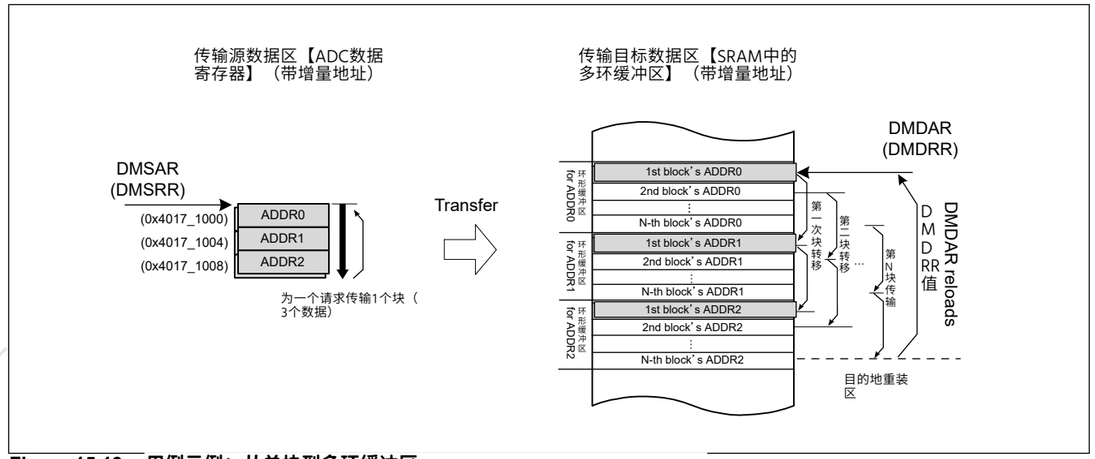


Figure 15.19 用例示例：从单块到多环缓冲区

15.3.7 激活源

软件、外设模块的中断请求和外部中断请求都可以指定为DMAC激活源。设置DMTMD.DCTG[1:0]位以选择激活源。

15.3.7.1 软件激活DMAC

当通过软件启动DMA传输时，请遵循以下步骤。

1.将DMTMD.DCTG[1:0]位设置为00b

2.将DMCNT.DTE位设置为1（启用DMA传输）

3.将DMAST.DMST位设置为1（启用DMAC激活）

4.将DMREQ.SWREQ位设置为1（请求DMA）

当DMREQ.CLRS位为0时由软件激活DMAC时，在响应DMA传输请求开始数据传输后，DMREQ.SWREQ位清零。

当CLRS位为1时由软件激活DMAC时，数据传输开始后SWREQ位不会被清零。在这种情况下，在传输完成后再次发出DMA传输请求。

15.3.7.2 通过来自片上外围模块或外部中断请求的中断请求激活DMAC

您可以将来自片上外围模块的中断请求和外部中断请求指定为DMAC激活源。可以为ICU.DELSRn.DELS[8:0]（n=0到7）中的每个通道单独选择激活源。

要通过来自片上外围模块的中断请求或外部中断请求启动DMA传输，请按照以下步骤操作。

1.将ICU.DELSRn.DELS[8:0]（n=0到7）设置为事件编号（选择DMAC事件链接）。

2. Set the DMTMD.DCTG[1:0] bits to 01b (interrupts from the peripheral modules and the external interrupt pins).
3. Set the DMCNT.DTE bit to 1 (enable DMA transfer).
4. Set the DMAST.DMST bit set to 1 (DMAC activation enabled)

For interrupt requests specified as DMAC activation sources, see Table 12.3, in section 12, Interrupt Controller Unit (ICU).

15.3.8 Operation Timing

The following timing charts have indicated the number of execution cycles of the minimum.

Figure 15.20 and Figure 15.21 show DMAC operation timing examples.

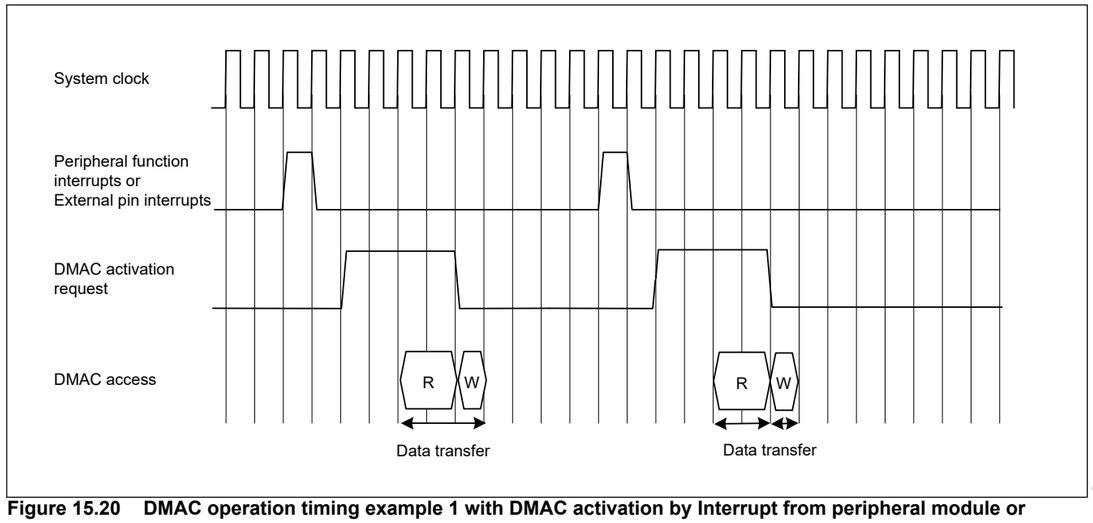


Figure 15.20 DMAC operation timing example 1 with DMAC activation by Interrupt from peripheral module or external interrupt input pin, in normal transfer mode or repeat transfer mode

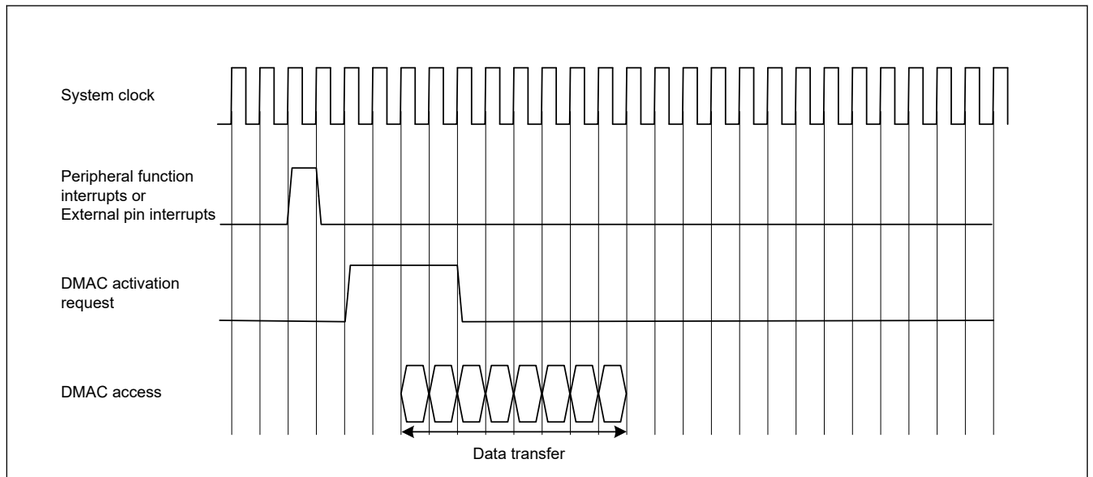


Figure 15.21 DMAC operation timing example 2 with DMAC activation by interrupt from peripheral module or external interrupt input pin, in block transfer mode with block size = 4

2.将DMTMD.DCTG[1:0]位设置为01b（来自外围模块和外部中断引脚的中断）。
3.将DMCNT.DTE位设置为1（启用DMA传输）。
4.将DMAST.DMST位设置为1（启用DMAC激活）

对于指定为DMAC激活源的中断请求，请参见第12节“中断控制器单元(ICU)”中的表12.3。

15.3.8 操作时间

下面的时序图已经表明了最小的执行周期数。

图15.20和图15.21显示了DMAC操作时序示例。

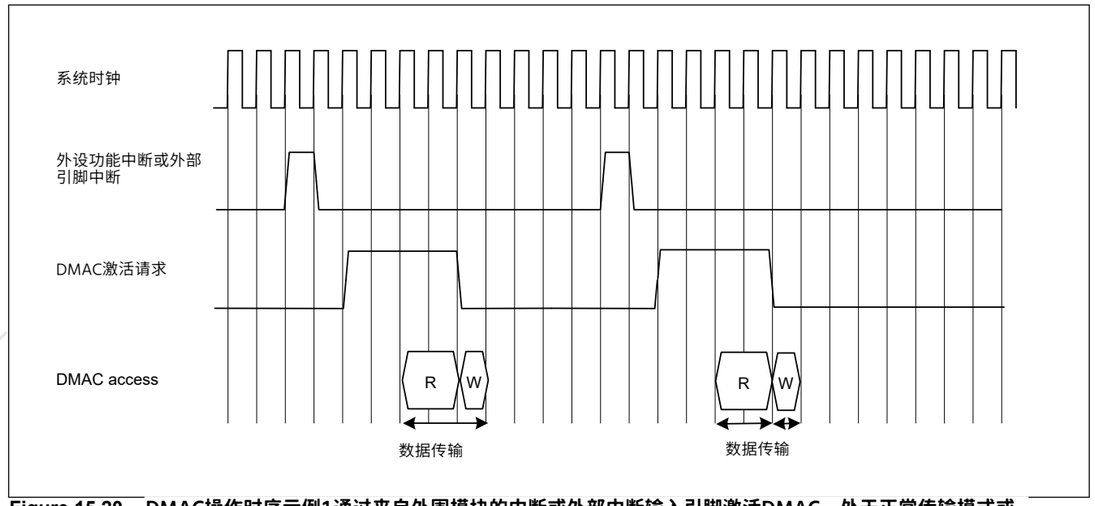


Figure 15.20 DMAC操作时序示例1通过来自外围模块的中断或外部中断输入引脚激活DMAC，处于正常传输模式或重复传输模式

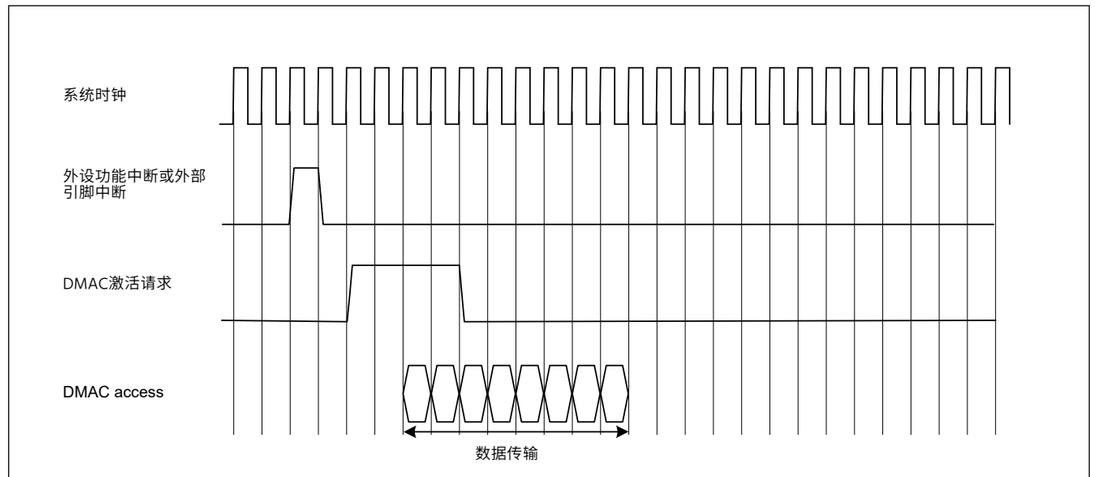


Figure 15.21 DMAC操作时序示例2，通过来自外围模块或外部中断输入引脚的中断激活DMAC，在块大小=4的块传输模式下

15.3.9 DMAC Execution Cycles

Table 15.17 lists execution cycles in one DMAC data transfer operation.

Table 15.17 DMAC Execution Cycles

Transfer Mode	Data Transfer (Read)	Data Transfer (Write)
Normal	Cr+1	Cw
Repeat	Cr+1	Cw
Block*1	P × Cr	P × Cw

Note: P: Block size (DMCRAH register setting)
Cr: Data read destination access cycle
Cw: Data write destination access cycle
Note 1. This is the case when the block size is 2 or more. When the block size is 1, normal transfer cycle is applied.

Cr and Cw depend on the access destination. For the number of cycles for each access destination, see section 41, SRAM, section 43, Flash Memory, section 13, Buses. The frequency ratio of the system clock and the peripheral clock is also taken into consideration.

The unit for +1 in "Data Transfer (Read)" column is one system clock cycle (ICLK). For the operation example, see section 15.3.8. Operation Timing.

15.3.10 Activating the DMAC

Table 15.18 shows the register setting procedure of normal, repeat and block transfer mode and Table 15.19 shows register setting procedure of repeat-block transfer mode.

Table 15.18 Register Setting Procedure of Normal Transfer Mode, Repeat Transfer Mode and Block Transfer Mode (1 of 2)

No.	Step Name	Description
1	Disable the peripheral function as the DMACn request source.	To use peripheral function interrupts as DMAC activation sources. Disable the control register for the peripheral function.
2	Disable the IRQn pin as the DMACn request source.	To use external pin interrupts as DMAC activation sources.
3	Set the DMACn Event Link select (ICU.DELSRn.DELS[8:0]) to 0x00	Disable the DMACn request.
4	Clear the DMCNT.DTE bit to 0	Disable DMA transfer.
5	Set the interrupt request as a DMACn request source in the DMAC Event Link Setting Register (ICU.DELSRn) by using the ICU.	To use internal peripheral interrupts or external pin interrupts as DMAC activation sources. Enable the interrupt bit for the activation source. Set the DMACn activation source.
6	Set the peripheral module as a DMACn request source	To use peripheral function interrupt as a DMAC activation source. Set the control register for the peripheral function without starting it.
7	Set the IRQn pin function by using the ICU.	To use external pin interrupt as a DMAC activation source. Set the IRQn pin function by using the Interrupt Controller Unit.
8	Set the DMAMD.DM[1:0] bits Set the DMAMD.SM[1:0] bits Set the DMAMD.DARA[4:0] bits Set the DMAMD.SARA[4:0] bits	Set the Transfer destination address update mode bits Set the Transfer source address update mode bits Set the Transfer destination address extended repeat area bits Set the Transfer source address extended repeat area bits
9	Set the DMTMD.DCTG[1:0] bits Set the DMTMD.SZ[1:0] bits Set the DMTMD.DTS[1:0] bits Set the DMTMD.MD[1:0] bits Set the DMTMD.TKP bit	Set the Transfer request select bits Set the Data transfer size bits Set the Repeat area select bits Set the Transfer mode select bits Set the transfer keeping select bit
10	Set the DMSAR register Set the DMDAR register Set the DMCRA register	Set the transfer source start address. Set the transfer destination start address. Set the number of transfer operations.
11	Set the DMCRB register	To use block transfer mode or repeat transfer mode. Set the number of block transfer operations.

15.3.9 DMAC执行周期

表15.17列出了一个DMAC数据传输操作中的执行周期。

Table 15.17 DMAC执行周期

传输模式	数据传输（读取）	数据传输（写入）
Normal	Cr+1	Cw
Repeat	Cr+1	Cw
Block*1	P × Cr	P × Cw

Note: P：块大小（DMCRAH寄存器设置）Cr：数据读取目标访问周期Cw：数据写入目标访问周期
注1.这是块大小为2或更大的情况。当块大小为1时，应用正常传输周期。

Cr和Cw取决于访问目的地。关于每个访问目标的周期数，请参阅第41节，SRAM，第43节，闪存，第13节，总线。系统时钟和外设时钟的频率比也被考虑在内。

"数据传输（读取）"列中+1的单位是一个系统时钟周期（ICLK）。操作示例见15.3.8节。操作时间。

15.3.10 激活DMAC

表15.18显示了正常、重复和块传输模式的寄存器设置过程，表15.19显示了重复块传输模式的寄存器设置过程。

Table 15.18 正常传输模式、重复传输模式和块传输的寄存器设置过程
模式（2个中的1个）

No.	步骤名称	Description
1	禁用外设功能作为DMACn请求源。	使用外设功能中断作为DMAC激活源。禁用外围功能的控制寄存器。
2	禁用IRQn引脚作为DMACn请求源。	使用外部引脚中断作为DMAC激活源。
3	将DMACn事件链接选择(ICU.DELSRn.DELS[8:0])设置为0x00	禁用DMACn请求。
4	将DMCNT.DTE位清0	禁用DMA传输。
5	将中断请求设置为DMACn请求源 DMAC事件链接设置寄存器(ICU.DELSRn)通过使用 ICU.	使用内部外设中断或外部引脚中断作为DMAC激活源。 启用激活源的中断位。设置DMACn激活源。
6	将外设模块设置为DMACn请求源	使用外设功能中断作为DMAC激活源。设置外围功能的控制寄存器而不启动它。
7	使用ICU设置IRQn引脚功能。	使用外部引脚中断作为DMAC激活源。 使用中断控制器单元设置IRQn引脚功能。
8	设置DMAMD.DM[1:0]位设置 DMAMD.SM[1:0]位 设置DMAMD.DARA[4:0]位设置 DMAMD.SARA[4:0]位	设置传输目标地址更新模式位 设置传输源地址更新模式位 设置传输目标地址扩展重复区域位 设置传输源地址扩展重复区域位
9	设置DMTMD.DCTG[1:0]位 设置DMTMD.SZ[1:0]位设置D MTMD.DTS[1:0]位设置DMTM D.MD[1:0]位 设置DMTMD.TKP位	设置传输请求选择位 设置数据传输大小位设置重复 区域选择位 设置传输模式选择位设置传输保 持选择位
10	设置DMSAR寄存器设置 DMDAR寄存器设置DMC RA寄存器	设置传输源起始地址。设置传送目的地起 始地址。 设置传输操作的次数。
11	设置DMCRB寄存器	使用块传输模式或重复传输模式。 设置块传输操作的数量。

Table 15.18 Register Setting Procedure of Normal Transfer Mode, Repeat Transfer Mode and Block Transfer Mode (2 of 2)

No.	Step Name	Description
12	Set the DMOFR register	To use the address update function with offset. Set the offset value.
13	Set the DMINT.DTIE bit to 1	To use the DMA transfer end interrupts. Enable DMACn transfer end interrupts.
14	Set the DMINT.RPTIE bit Set the DMINT.SARIE bit Set the DMINT.DARIE bit Set the DMINT.ESIE bit to 1	To use the DMA transfer escape end interrupts Set the repeat size end interrupt. Set the transfer source address extended repeat area overflow interrupt. Set the transfer destination address extended repeat area overflow interrupt. Enable the DMA transfer escape end interrupt.
15	Set the DMCNT.DTE bit to 1	Enable DMA transfer.
16	Set the DMAST.DMST bit to 1	Enable DMAC operation. *1 Common settings for DMAC
17	Start the peripheral function as a DMACn request source	To use peripheral function interrupt as a DMAC activation source
18	Enable the IRQn pin as a DMACn request source	To use external pin interrupt as a DMAC activation source
19	End of initial settings	For activation by software On completion of the initial settings, writing 1 to the DMA software start bit (DMREQ.SWREQ) starts DMA transfer.

Note: n: DMAC channel (n = 0 to 7)
Note 1. The DMAST.DMST bit setting does not necessarily have to follow the settings for the individual activation sources.

Table 15.19 Register Setting Procedure of Repeat-Block Transfer Mode (1 of 2)

No.	Step Name	Description
1	Disable the peripheral function as the DMACn request source.	To use peripheral function interrupts as DMA activation sources. Disable the control register for the peripheral function.
2	Disable the IRQ pin as the DMACn request source.	To use external pin interrupts as DMA activation sources.
3	Set the DMACn Event Link select (ICU.DELSRn.DELS[8:0]) to 00h	Disable the DMACn request.
4	Clear the DMCNT.DTE bit to 0	Disable DMACn transfer.
5	Set the interrupt request as a DMACn request source in the DMACn Event Link Setting Register (ICU.DELSRn) by using the ICU.	To use internal peripheral interrupts or external pin interrupts as DMA activation sources. Enable the interrupt bit for the activation source. Set the DMACn activation source.
6	Set the peripheral module as a DMACn request source	To use peripheral function interrupt as a DMA activation source. Set the control register for the peripheral function without starting it.
7	Set the IRQ pin function by using the Interrupt Controller Unit.	To use external pin interrupt as a DMA activation source. Set the IRQ pin function by using the Interrupt Controller Unit.
8	Set the DMAMD.DM[1:0] bits Set the DMAMD.SM[1:0] bits Set the DMAMD.DADR bit Set the DMAMD.SADR bit	Set the Transfer destination address update mode bits Set the Transfer source address update mode bits Set the Transfer destination address update select after reload Set the Transfer source address update select after reload
9	Set the DMTMD.DCTG[1:0] bits Set the DMTMD.SZ[1:0] bits Set the DMTMD.MD[1:0] bits Set the DMTMD.TKP bit	Set the Transfer request select bits Set the Data transfer size bits Set the Transfer mode to repeat-block transfer mode Set the transfer keeping select bit
10	Set the DMSAR register Set the DMDAR register Set the DMSRR register Set the DMDRR register Set the DMCRA register Set the DMCRB register	Set the transfer source start address Set the transfer destination start address Set the initial value of source start address Set the initial value of destination start address Set the number of transfer operations Set the number of block transfer operations

Table 15.18 正常传输模式、重复传输模式和块传输的寄存器设置过程 模式（2之2）

No.	步骤名称	Description
12	设置DMOFR寄存器	使用带偏移量的地址更新功能。 设置偏移值。
13	将DMINT.DTIE位设置为1	使用DMA传输结束中断。启用DMACn 传输结束中断。
14	设置DMINT.RPTIE位设置 DMINT.SARIE位设置DMI NT.DARIE位 将DMINT.ESIE位设置为1	使用DMA传输转义结束中断 设置重复尺寸结束中断。 设置传输源地址扩展重复区溢出中断。设置传送目标地址扩展 重复区域溢出中断。启用DMA传输转义结束中断。
15	将DMCNT.DTE位设置为1	启用DMA传输。
16	将DMAST.DMST位设置为1	启用DMAC操作。*1 DMAC的常用设置
17	作为DMACn请求源启动外设功能	使用外设功能中断作为DMAC激活源
18	启用IRQn引脚作为DMACn请求源	使用外部引脚中断作为DMAC激活源
19	初始设置结束	通过软件激活 初始设置完成后，将1写入DMA软件启动位(DMREQ.SWR EQ)开始DMA传输。

Note: n：DMAC通道（n=0到7）
注1.DMAST.DMST位设置不一定要遵循各个激活源的设置。

Table 15.19 重复块传输模式的寄存器设置过程（1of2）

No.	步骤名称	Description
1	禁用外设功能作为DMACn请求源。	使用外设功能中断作为DMA激活源。 禁用外围功能的控制寄存器。
2	禁用IRQ引脚作为DMACn请求源。	使用外部引脚中断作为DMA激活源。
3	将DMACn事件链接选择(ICU.DELSRn.DELS[8:0])设置为00h	禁用DMACn请求。
4	将DMCNT.DTE位清0	禁用DMACn传输。
5	将中断请求设置为DMACn请求源 DMACn事件链接设置寄存器(ICU.DELSRn)通过使用 ICU.	使用内部外设中断或外部引脚中断作为 DMA激活源。 启用激活源的中断位。 设置DMACn激活源。
6	将外设模块设置为DMACn请求源	使用外设功能中断作为DMA激活源。设置外围功能的控制寄存器 而不启动它。
7	使用中断控制器单元设置IRQ引脚功能。	使用外部引脚中断作为DMA激活源。 使用中断控制器单元设置IRQ引脚功能。
8	设置DMAMD.DM[1:0]位设置 DMAMD.SM[1:0]位 设置DMAMD.DADR位设置 DMAMD.SADR位	设置传输目标地址更新模式位 设置传输源地址更新模式位 重新加载后设置传输目标地址更新选择 重新加载后设置传输源地址更新选择
9	设置DMTMD.DCTG[1:0]位 设置DMTMD.SZ[1:0]位设置D MTMD.MD[1:0]位 设置DMTMD.TKP位	设置传输请求选择位 设置数据传输大小位 将传输模式设置为重复块传输模式 设置传输保持选择位
10	设置DMSAR寄存器设置 DMDAR寄存器设置DMS RR寄存器设置DMDRR寄 存器设置DMCRA寄存器 设置DMCRB寄存器	设置传输源起始地址 设置传输目标起始地址 设置源起始地址的初始值 设置目的起始地址的初始值 设置传输操作的次数 设置块传输操作的数量

Table 15.19 Register Setting Procedure of Repeat-Block Transfer Mode (2 of 2)

No.	Step Name	Description
11	Set the DMSBS register Set the DMDBS register	To use the address update function with incremental, decremental or offset Set the source buffer size and access offset Set the destination buffer size and access offset
12	Set the DMINT.DTIE bit to 1	To use DMA transfer end interrupts. Enable DMACn transfer end interrupts.
13	Set the DMCNT.DTE bit to 1	Enable DMACn transfer
14	Set the DMAST.DMST bit to 1	Enable DMAC operation.*1
15	Start the peripheral function as a DMACn request source	To use peripheral function interrupt as a DMA activation source
16	Enable the IRQ pin as a DMACn request source	To use external pin interrupt as a DMA activation source
17	End of initial settings	For activation by software On completion of the initial settings, writing 1 to the DMA software start bit (DMREQ.SWREQ) starts DMA transfer.

Note: m: DELSRn.DELS bit number (m = 0 to 8)
n: DMAC channel (n = 0 to 7)
Note 1. The DMAST.DMST bit setting does not necessarily have to follow the settings for the individual activation sources.

15.3.11 Starting DMA Transfer

To enable the DMA transfer, set the DMCNT.DTE bit to 1 (enable the DMA transfer), and then set the DMAST.DMST bit to 1 (enable the DMAC activation).

New activation requests are not accepted during the transfer of another DMAC channel or DTC. When the preceding transfer is complete, channel arbitration selects the DMA transfer request of the highest priority channel, and the DMA transfer of that channel starts. When the DMA transfer starts, the DMSTS.ACT flag is set to 1 (the DMAC is in the active state).

15.3.12 Registers during DMA Transfer

The DMAC registers are updated by a DMA transfer. The value to be updated differs according to the other settings and the transfer state. The registers to be updated are DMSAR, DMDAR, DMCRA, DMCRB, DMSBS, DMDBS, DMCNT, and DMSTS.

DMA Source Address Register (DMSAR)

When data has been transferred in response to one transfer request, the contents of DMSAR are updated to the address to be accessed by the next transfer request.

For details on register update operation in each transfer mode, see Table 15.5 to Table 15.13.

DMA Destination Address Register (DMDAR)

When data has been transferred in response to one transfer request, the contents of DMDAR are updated to the address to be accessed by the next transfer request.

For details on register update operation in each transfer mode, see Table 15.5 to Table 15.13.

DMA Transfer Count Register (DMCRA)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.

For details on register update operation in each transfer mode, see Table 15.5 to Table 15.13.

DMA Block Transfer Count Register (DMCRB)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.

For details on register update operation in each transfer mode, see Table 15.5 to Table 15.13.

Table 15.19 重复块传输模式的寄存器设置过程(2of2)

No.	步骤名称	Description
11	设置DMSBS寄存器设置 DMDBS寄存器	使用增量、减量或偏移的地址更新功能设置源缓冲区大小和访问偏移量 设置目标缓冲区大小和访问偏移量
12	将DMINT.DTIE位设置为1	使用DMA传输结束中断。 启用DMACn传输结束中断。
13	将DMCNT.DTE位设置为1	启用DMACn传输
14	将DMAST.DMST位设置为1	启用DMAC操作。*1
15	作为DMACn请求源启动外设功能	使用外设功能中断作为DMA激活源
16	启用IRQ引脚作为DMACn请求源	使用外部引脚中断作为DMA激活源
17	初始设置结束	通过软件激活 初始设置完成后，将1写入DMA软件启动位(DMREQ.SWREQ)开始DMA传输。

Note: m：DELSRn.DELS位号（m=0到8）n：DMAC通道（n=0到7）
注1.DMAST.DMST位设置不一定要遵循各个激活源的设置。

15.3.11 启动DMA传输

要启用DMA传输，请将DMCNT.DTE位设置为1（启用DMA传输），然后将DMAST.DMST位设置为1（启用DMAC激活）。

在传输另一个DMAC通道或DTC期间不接受新的激活请求。当前面的传输完成后，通道仲裁选择最高优先级通道的DMA传输请求，该通道的DMA传输开始。当DMA传输开始时，DMSTS.ACT标志设置为1（DMAC处于活动状态）。

15.3.12 DMA传输期间的寄存器

DMAC寄存器由DMA传输更新。要更新的值根据其他设置和传输状态而有所不同。要更新的寄存器是DMSAR、DMDAR、DMCRA、DMRCB、DMSBS、DMDBS、DMCNT和DMSTS。

DMA源地址寄存器(DMSAR)

当响应一个传输请求而传输了数据时，DMSAR的内容将更新为下一个传输请求要访问的地址。

每种传输模式下寄存器更新操作的详细信息，请参见表15.5至表15.13。

DMA目标地址寄存器(DMDAR)

当响应一个传输请求传输了数据时，DMDAR的内容被更新为下一个传输请求要访问的地址。

每种传输模式下寄存器更新操作的详细信息，请参见表15.5至表15.13。

DMA传输计数寄存器(DMCRA)

当响应一个传输请求传输数据时，更新计数值。更新操作取决于选择的传输模式。

每种传输模式下寄存器更新操作的详细信息，请参见表15.5至表15.13。

DMA块传输计数寄存器(DMCRB)

当响应一个传输请求传输数据时，更新计数值。更新操作取决于选择的传输模式。

每种传输模式下寄存器更新操作的详细信息，请参见表15.5至表15.13。

DMA Source Buffer Size Register (DMSBS)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.

For details on register update operation in each transfer mode, refer to Table 15.8 to Table 15.13.

DMA Destination Buffer Size Register (DMDBS)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.

For details on register update operation in each transfer mode, refer to Table 15.8 to Table 15.13.

DMA Transfer Enable Bit (DMCNT.DTE)

Although the DMCNT.DTE bit enables or disables data transfer by the register write access, it is automatically cleared to 0 by the DMAC according to the DMA transfer state.

The conditions for clearing this bit by the DMAC are as follows:

- When the specified total volume of data transfer is completed
- When DMA transfer is stopped by the repeat size end interrupt
- When DMA transfer is stopped by the extended repeat area overflow interrupt
- When DMA transfer error occurs

Writing to the registers for the channels when the corresponding DMCNT.DTE bit is set to 1 is prohibited (except for DMCNT). In this case, writing must be performed after the bit is cleared to 0.

DMAC Active Flag (DMSTS.ACT)

The DMSTS.ACT flag indicates whether the DMACn is in the idle or active state.

This flag is set to 1 when the DMAC starts data transfer, and is cleared to 0 when data transfer in response to one transfer request is completed.

Even when DMA transfer is stopped by writing 0 to the DMCNT.DTE bit during DMA transfer, this flag remains 1 until DMA transfer is completed.

Transfer End Interrupt Flag (DMSTS.DTIF)

The DMSTS.DTIF flag is set to 1 after DMA transfer of the total transfer size of data is completed.

When both this flag and the DMINT.DTIE bit are set to 1, a transfer end interrupt is requested.

This flag is set to 1 when the DMA transfer bus cycle is completed and the DMSTS.ACT flag is cleared to 0 indicating the DMA transfer end.

This flag is automatically cleared to 0 when the DMCNT.DTE bit is set to 1 during the interrupt handling.

Transfer Escape End Interrupt Flag (DMSTS.ESIF)

The DMSTS.ESIF flag is set to 1 when a repeat size end interrupt or extended repeat area overflow interrupt is requested. When this bit and the DMINT.ESIE bit are set to 1, a transfer escape end interrupt is requested.

This flag is set to 1 when the bus cycle of the DMA transfer having caused the interrupt request is completed and the DMSTS.ACT flag is cleared to 0 indicating the DMA transfer end.

This flag is automatically cleared to 0 when the DMCNT.DTE bit is set to 1 during an interrupt handling.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set.

For details, see section 12, Interrupt Controller Unit (ICU).

15.3.13 Channel Priority

When multiple DMA transfer requests are present, the DMAC determines the priority of channels that have DMA transfer requests.

- The channel priority is fixed as follows: Channel 0 > Channel 1 > Channel 2 > Channel 3… > Channel 7 (Channel 0: Highest).

DMA源缓冲区大小寄存器(DMSBS)

当响应一个传输请求传输数据时，更新计数值。更新操作取决于选择的传输模式。

有关各传输模式下的寄存器更新操作的详细信息，请参阅表15.8至表15.13。

DMA目标缓冲区大小寄存器(DMDBS)

当响应一个传输请求传输数据时，更新计数值。更新操作取决于选择的传输模式。

有关各传输模式下的寄存器更新操作的详细信息，请参阅表15.8至表15.13。

DMA传输使能位(DMCNT.DTE)

虽然DMCNT.DTE位通过寄存器写访问启用或禁用数据传输，但它会根据DMA传输状态由DMAC自动清零。

DMAC清除该位的条件如下：

- ●当指定的总数据传输量完成时
- ●当DMA传输因重复大小结束中断而停止时
- ●当DMA传输因扩展重复区域溢出中断而停止时
- ●发生DMA传输错误时

当相应的DMCNT.DTE位设置为1时，禁止写入通道的寄存器（除了DMCNT）。在这种情况下，必须在该位清0后进行写入。

DMAC活动标志(DMSTS.ACT)

DMSTS.ACT标志指示DMACn是处于空闲状态还是活动状态。

该标志在DMAC开始数据传输时设置为1，并在响应一个传输请求的数据传输完成时清除为0。

即使在DMA传输期间通过向DMCNT.DTE位写入0来停止DMA传输，该标志仍 保持为1，直到DMA传输完成。

传输结束中断标志(DMSTS.DTIF)

在数据的总传输大小的DMA传输完成后，DMSTS.DTIF标志设置为1。

当该标志和DMINT.DTIE位都设置为1时，请求传输结束中断。

当DMA传输总线周期完成并且DMSTS.ACT标志被清除为0时，该标志设置为1，表示DMA传输结束。

在中断处理期间，当DMCNT.DTE位设置为1时，该标志自动清零。

传输转义结束中断标志(DMSTS.ESIF)

当请求重复大小结束中断或扩展重复区域溢出中断时，DMSTS.ESIF标志设置为1。
当该位和DMINT.ESIE位设置为1时，请求传输转义结束中断。

当导致中断请求的DMA传输的总线周期完成并且DMSTS.ACT标志清零，表示DMA传输结束。

在中断处理期间，当DMCNT.DTE位设置为1时，该标志自动清零。

在从DMAC向CPU或DTC发送中断请求之前，必须设置中断控制寄存器。

有关详细信息，请参阅第12节，中断控制器单元(ICU)。

15.3.13 频道优先级

当存在多个DMA传输请求时，DMAC确定具有DMA传输请求的通道的优先级。

●通道优先级固定如下：通道0>通道1>通道2>通道3...>通道7（通道0：最高）。

When a DMA transfer request is generated during data transfer, channel arbitration is started after the final data has been transferred, and DMA transfer of the higher-priority channel starts.

15.3.14 Channel Security

The security attribute of transfer access of DMACn, security attribute of access to register of DMACn, security attribute of access to the ICU.DELSRn register are controlled by ICUSARC.SADMACn bit. For details on the ICUSARC register, see section 12, Interrupt Controller Unit (ICU).

When the ICUSARC.SADMACn bit is 0, transfer of DMACn is secure access for both read and write. At the same time, the registers of channel n and the DELSRn register are protected from a non-secure access.

When the ICUSARC.SADMACn bit is 1, transfer of DMACn is non-secure access for both read and write. At the same time, the registers of channel n and the DELSRn register are non-secure attributes.

Do not write to the ICUSARC.SADMACn bit while DMA transfer of same channel is enabled or a bus master is writing to the DMA registers of same channel.

Figure 15.22 shows security attribute about each DMAC channels.

如果在数据传输过程中产生DMA传输请求，则在传输完最终数据后启动通道仲裁，并开始高优先级通道的DMA传输。

15.3.14 渠道安全

DMACn的传输访问的安全属性、DMACn的寄存器访问的安全属性、ICU.DELSRn寄存器的访问的安全属性由ICUSARC.SADMACn位控制。有关ICUUSARC寄存器的详细信息，请参见第12节，中断控制器单元(ICU)。

当ICUSARC.SADMACn位为0时，DMACn的传输对于读和写都是安全访问。同时，通道n的寄存器和DELSRn寄存器受到保护，不会被非安全访问。

当ICUSARC.SADMACn位为1时，DMACn的传输对于读和写都是非安全访问。同时，通道n的寄存器和DELSRn寄存器是非安全属性。

当启用同一通道的DMA传输或总线主机正在写入同一通道的DMA寄存器时，请勿写入ICUSARC.SADMACn位。

图15.22显示了每个DMAC通道的安全属性。

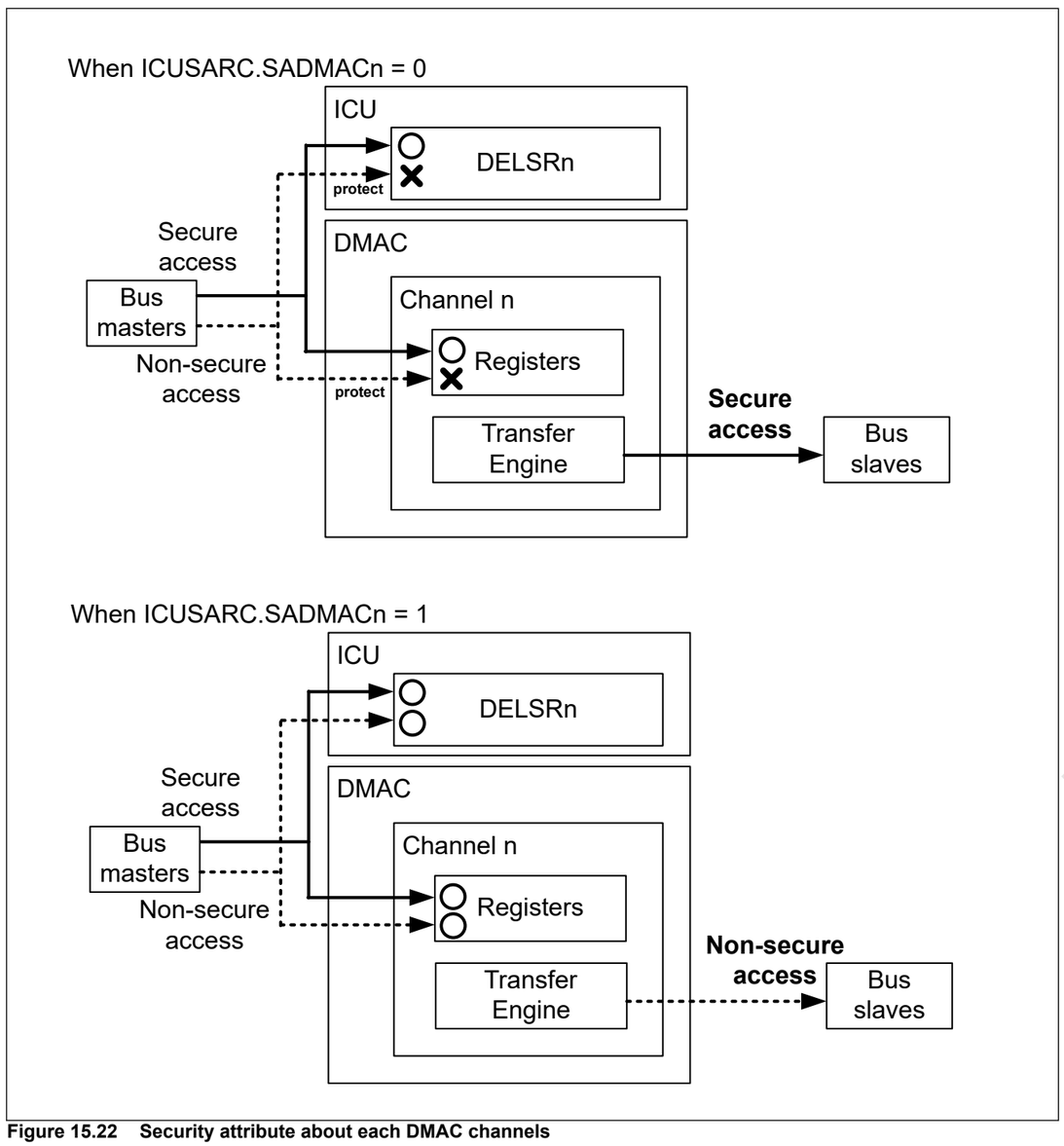


Figure 15.22 Security attribute about each DMAC channels

15.3.15 Master TrustZone Filter in DMAC

DMAC has the Master TrustZone Filter. The MasterTrustZone Filter in DMAC can detect the security areas of Flash area(code Flash and data Flash) and SRAM area defined by IDAU. When set No-secure channel accesses those addresses, it detects the security violation. Access of violation address is not performed. Detected the error is handled as the Master TrustZone Filter error.

15.4 Ending DMA Transfer

The operation for ending DMA transfer depends on the transfer end conditions. When DMA transfer ends, the DMCNT.DTE bit and the DMSTS.ACT flag are changed from 1 to 0, indicating that DMA transfer has ended.

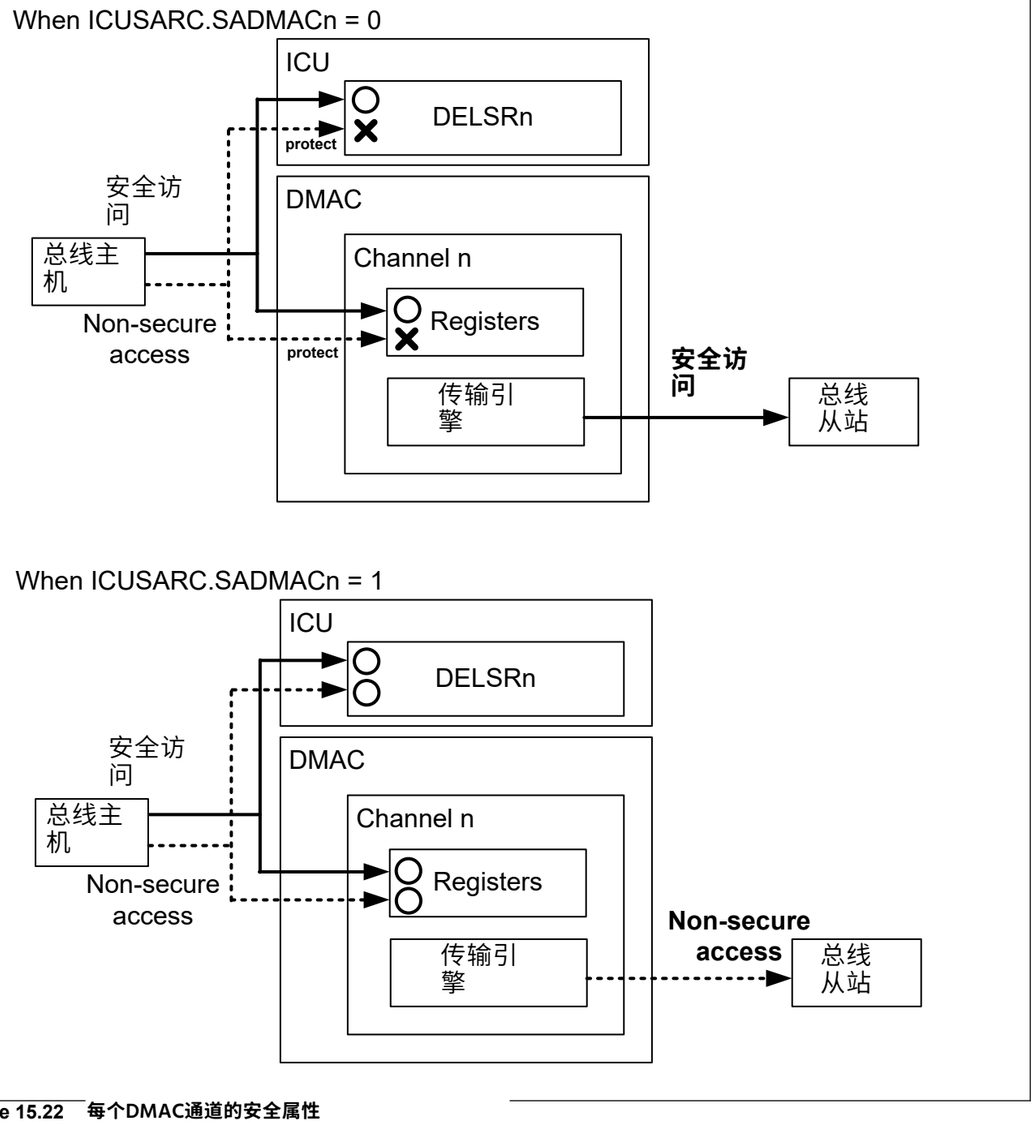


Figure 15.22 每个DMAC通道的安全属性

15.3.15 DMAC中的主TrustZone过滤器

DMAC具有MasterTrustZone过滤器。DMAC中的MasterTrustZoneFilter可以检测IDAU定义的Flash区域（代码Flash和数据Flash）和SRAM区域的安全区域。当设置无安全通道访问这些地址时，它会检测到安全违规。不执行违规地址的访问。检测到的错误作为MasterTrustZoneFilter错误处理。

15.4 结束DMA传输

结束DMA传输的操作取决于传输结束条件。当DMA传输结束时，DMCNT.DTE位和DMSTS.ACT标志由1变为0，表示DMA传输已经结束。

15.4.1 Transfer End by Completion of Specified Total Number of Transfer Operations

(1) In Normal Transfer Mode (DMTMD.MD[1:0] = 00b)

When the value of DMCRAL changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DMCNT.DTE bit is cleared to 0 and the DMSTS.DTIF flag is set to 1 at the same time. If the DMINT.DTIE bitT is 1 at this time, a transfer end interrupt request is issued to the CPU or the DTC.

(2) In Repeat Transfer Mode (DMTMD.MD[1:0] = 01b)

When the value of DMCRBL changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DMCNT.DTE bit is cleared to 0 and the DMSTS.DTIF flag is set to 1 at the same time. If the DMINT.DTIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC.

If the DMTMD.TKP bit is 1 (in free-running function), the DMSTS.DTIF bit is set to 1, but the DMCNT.DTE bit is not cleared to 0.

(3) In Block Transfer Mode (DMTMD.MD[1:0] = 10b)

When the value of DMCRBL changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DMCNT.DTE bit is cleared to 0 and the DMSTS.DTIF flag is set to 1 at the same time. If the DMINT.DTIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set.

For details, see section 12, Interrupt Controller Unit (ICU).

If the DMTMD.TKP bit is 1 (in free-running function),the DMSTS.DTIF bit is set to 1, but the DMCNT.DTE bit is not cleared to 0.

(4) In Repeat-Block Transfer Mode (DMTMD.MD[1:0] = 11b)

When the value of DMCRBL changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DMCNT.DTE bit is cleared to 0 and the DMSTS.DTIF flag is set to 1 at the same time. If the DMINT.DTIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 12, Interrupt Controller Unit (ICU).

If the DMTMD.TKP bit is 1 (in free-running function),the DMSTS.DTIF bit is set to 1, but the DMCNT.DTE bit is not cleared to 0.

15.4.2 Transfer End by Repeat Size End Interrupt

In repeat transfer mode, a repeat size end interrupt is requested when transfer of a 1-repeat size of data is completed while the DMINT.RPTIE bit is set to 1. When the interrupt is requested to complete DMA transfer, the DMCNT.DTE bit is cleared to 0 and the DMSTS.ESIF flag is set to 1 even if the DMTMD.TKP bit is 1 (in free-running function). If the DMINT.ESIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC. Here, the transfer can be resumed by writing 1 to the DMCNT.DTE bit.

A repeat size end interrupt can be requested also in block transfer mode. In block transfer mode, the interrupt is requested in the same way as in repeat transfer mode when transfer of a 1-block size data is completed.

Repeat size end interrupt cannot be requested in repeat-block transfer mode.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 12, Interrupt Controller Unit (ICU).

15.4.3 Transfer End by Interrupt on Extended Repeat Area Overflow

When an overflow on the extended repeat area occurs while the extended repeat area is specified and the DMINT.SARIE or DMINT.DARIE bit is set to 1 even if the DMTMD.TKP bit is 1 (in free-running function), an interrupt by an extended repeat area overflow is requested. When the interrupt is requested, the DMA transfer is terminated, the DMCNT.DTE bit is cleared to 0, and the ESIF flag in DMSTS is set to 1. If the DMINT.ESIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC.

15.4.1 完成指定的转移操作总数后转移结束

(1) 在正常传输模式下（DMTMD.MD[1:0]=00b）

当DMCRAL的值由1变为0时，相应通道上的DMA传输结束，同时DMCNT.DTE位清0，同时DMSTS.DTIF标志置1。如果此时DMINT.DTIEbitT为1，则向CPU或DTC发出传输结束中断请求。

(2) 在重复传输模式下(DMTMD.MD[1:0]=01b)

当DMCRBL的值从1变为0时，相应通道上的DMA传输结束，同时DMCNT.DTE位清0，同时DMSTS.DTIF标志置1。如果此时DMINT.DTIE位为1，则向CPU或DTC发出中断请求。

如果DMTMD.TKP位为1（在自由运行功能中），则DMSTS.DTIF位设置为1，但DMCNT.DTE位不清除为0。

(3) 在块传输模式下(DMTMD.MD[1:0]=10b)

当DMCRBL的值从1变为0时，相应通道上的DMA传输结束，同时DMCNT.DTE位清0，同时DMSTS.DTIF标志置1。如果此时DMINT.DTIE位为1，则向CPU或DTC发出中断请求。

在从DMAC向CPU或DTC发送中断请求之前，必须设置中断控制寄存器。

有关详细信息，请参阅第12节，中断控制器单元(ICU)。

如果DMTMD.TKP位为1（在自由运行功能中），则DMSTS.DTIF位设置为1，但DMCNT.DTE位不清除为0。

(4) 在重复块传输模式下(DMTMD.MD[1:0]=11b)

当DMCRBL的值从1变为0时，相应通道上的DMA传输结束，同时DMCNT.DTE位清0，同时DMSTS.DTIF标志置1。如果此时DMINT.DTIE位为1，则向CPU或DTC发出中断请求。

在从DMAC向CPU或DTC发送中断请求之前，必须设置中断控制寄存器。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

如果DMTMD.TKP位为1（在自由运行功能中），则DMSTS.DTIF位设置为1，但DMCNT.DTE位不清除为0。

15.4.2 按重复大小结束传输结束中断

在重复传输模式下，当DMINT.RPTIE位设置为1时完成1次重复大小的数据传输时，请求重复大小结束中断。当请求中断以完成DMA传输时，DMCNT.DTE位即使DMTMD.TKP位为1（在自由运行功能中），清除为0并且DMSTS.ESIF标志设置为1。如果此时DMINT.ESIE位为1，则向CPU或DTC发出中断请求。在这里，可以通过将1写入DMCNT.DTE位来恢复传输。

在块传输模式下也可以请求重复大小结束中断。在块传输模式中，当1块大小的数据传输完成时，以与重复传输模式相同的方式请求中断。

在重复块传输模式下不能请求重复大小结束中断。

在从DMAC向CPU或DTC发送中断请求之前，必须设置中断控制寄存器。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

15.4.3 扩展重复区溢出中断传输结束

如果在指定扩展重复区域时扩展重复区域发生溢出，并且即使DMTMD.TKP位为1（在自由运行功能中），DMINT.SARIE或DMINT.DARIE位也设置为1（在自由运行功能中），中断由请求扩展重复区域溢出。请求中断时，终止DMA传输，DMCNT.DTE位清0，DMSTS中的ESIF标志置1。如果此时DMINT.ESIE位为1，则发出中断请求到CPU或DTC。

Even if an interrupt by an extended repeat area overflow is requested during a read cycle, the following write cycle is performed.

In block transfer mode, even if an interrupt by an extended repeat area overflow is requested during a 1-block transfer, the remaining data in the block is transferred; transfer is terminated after a block transfer.

An interrupt by an extended repeat area overflow cannot be requested in repeat-block transfer mode.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 12, Interrupt Controller Unit (ICU).

15.5 Processing on DMA Transfer Error

DMA transfer error occurs with the Master TrustZone Filter error in DMAC, the Slave TrustZone Filter error, the Master MPU error, the Slave Bus Error or the Illegal Access Error. If the access error occurs during the DMA transfer, the DMAC immediately stops the transfer of error occurred channel. At this time, the ICU setting of the corresponding channel is also cleared. If there is a request other than the channel which caused the error, it will be re-arbitration as it is.

When the transfer error occurs, DMCNT.DTE of the error causing channel is set to 0. Also, the error response is informed to the ICU.DELSRn of the corresponding channel is cleared. Write back to each register is not performed. Furthermore, it generates the error response detection interrupt request (DMA_TRANSERR) to notify that an error has occurred by DMAC/DTC transfer.

When the Master TrustZone Filter error occurs, the Slave TrustZone error occurs or the Master MPU error occurs, it is possible to confirm the error information of DMAC by selecting NMI. The DMAC error channel register is cleared by selecting reset. Under the conditions where NMI is generated due to transfer error in DMAC, two interrupts(NMI and DMA_TRANSERR) are generated. In this case, NMI always responds first.

The error response detection interrupt request (DMA_TRANSERR) occurs when the Slave Bus error or the Illegal Access error occurs. Furthermore, it occurs after NMI when the error response detection interrupt request (DMA_TRANSERR) is not cleared in NMI handler.

section 15.5.1. Processing on NMI handler describes how to confirm the error information of the DMAC in the NMI handler.

section 15.5.2. Processing on Error response detection interrupt request (DMA_TRANSERR) handler describes how to confirm the error information of the DMAC in the DMA_TRANSERR handler.

Interrupts and the error information generated due to transfer errors are shown in section 15.6.2. Transfer Error Interrupt.

15.5.1 Processing on NMI handler

The cause of NMI due to the DMA transfer error is the Master TrustZone Filter error, the Slave TrustZone Filter error or the Master MPU error. When NMI occurs due to the DMAC transfer error, the error response detection interrupt request (DMA_TRANSERR) will occur after the end of NMI handler. It is possible to confirm the cause of the error and the DMAC channel in which the error occurred. When NMI occurs, perform the necessary processing according to the flow described in the ICU chapter.

Figure 15.23 shows the flow for confirm the channel that caused the Master TrustZone Filter Error in DMAC

Figure 15.24 shows the flow for confirm the channel that caused the Slave TrustZone Filter Error in DMAC

Figure 15.25 shows the flow for confirm the channel and Security Attribute that caused the Master MPU error in DMAC.

If completing all processing in NMI handler, it is possible to clear the error response detection interrupt request (DMA_TRANSERR) that occurs subsequently.

即使在读取周期期间请求由扩展重复区域溢出引起的中断，也会执行下一个写入周期。

在块传输模式下，即使在1块传输期间请求扩展重复区域溢出中断，也会传输块中剩余的数据；块传输后终止传输。

在重复块传输模式下不能请求由扩展重复区域溢出引起的中断。

在从DMAC向CPU或DTC发送中断请求之前，必须设置中断控制寄存器。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

15.5 DMA传输错误处理

DMA传输错误发生在DMAC中的MasterTrustZoneFilter错误、SlaveTrustZoneFilter错误、Master MPU错误、从总线错误或非法访问错误。如果在DMA传输过程中发生访问错误，DMAC立即停止发生错误通道的传输。此时相应通道的ICU设置也被清除。如果存在引起错误的通道以外的请求，将按原样重新仲裁。

当发生传输错误时，错误引起通道的DMCNT.DTE设置为0。同时，错误响应被通知给ICU。相应通道的DELSRn被清除。不执行回写到每个寄存器。此外，它会生成错误响应检测中断请求(DMA_TRANSERR)，以通知DMACDTC传输发生错误。

当MasterTrustZoneFilter发生错误、SlaveTrustZone错误或MasterMPU错误时，可以通过选择NMI来确认DMAC的错误信息。通过选择复位来清除DMAC错误通道寄存器。在由于DMAC中的传输错误而产生NMI的情况下，会产生两个中断（NMI和DMA_TRANSERR）。在这种情况下，NMI总是首先响应。

当发生SlaveBus错误或IllegalAccess错误时，会发生错误响应检测中断请求(DMA_TRANSERR)。此外，当NMI处理程序中未清除错误响应检测中断请求(DMA_TRANSERR)时，它会在NMI之后发生。

第15.5.1节。NMIhandler上的处理描述了如何在NMIhandler中确认DMAC的错误信息。

第15.5.2节。错误响应检测中断请求（DMA_TRANSERR）处理程序的处理描述了如何在DMA_TRANSERR处理程序中确认DMAC的错误信息。

因传输错误而产生的中断和错误信息见15.6.2节。传输错误中断。

15.5.1 在NMI处理程序上处理

由于DMA传输错误导致NMI的原因是MasterTrustZoneFilter错误、SlaveTrustZoneFilter错误或MasterMPU错误。当由于DMAC传输错误而发生NMI时，错误响应检测中断请求(DMA_TRANSERR)将在NMI处理程序结束后发生。可以确认错误的原因和发生错误的DMAC通道。当发生NMI时，按照ICU章节中描述的流程进行必要的处理。

图15.23显示了在DMAC中确认导致MasterTrustZoneFilterError的通道的流程

图15.24显示了在DMAC中确认导致SlaveTrustZoneFilterError的通道的流程

图15.25显示了在DMAC中确认导致MasterMPU错误的通道和安全属性的流程。

如果完成NMI处理程序中的所有处理，则可以清除随后发生的错误响应检测中断请求(DMA_TRANSERR)。

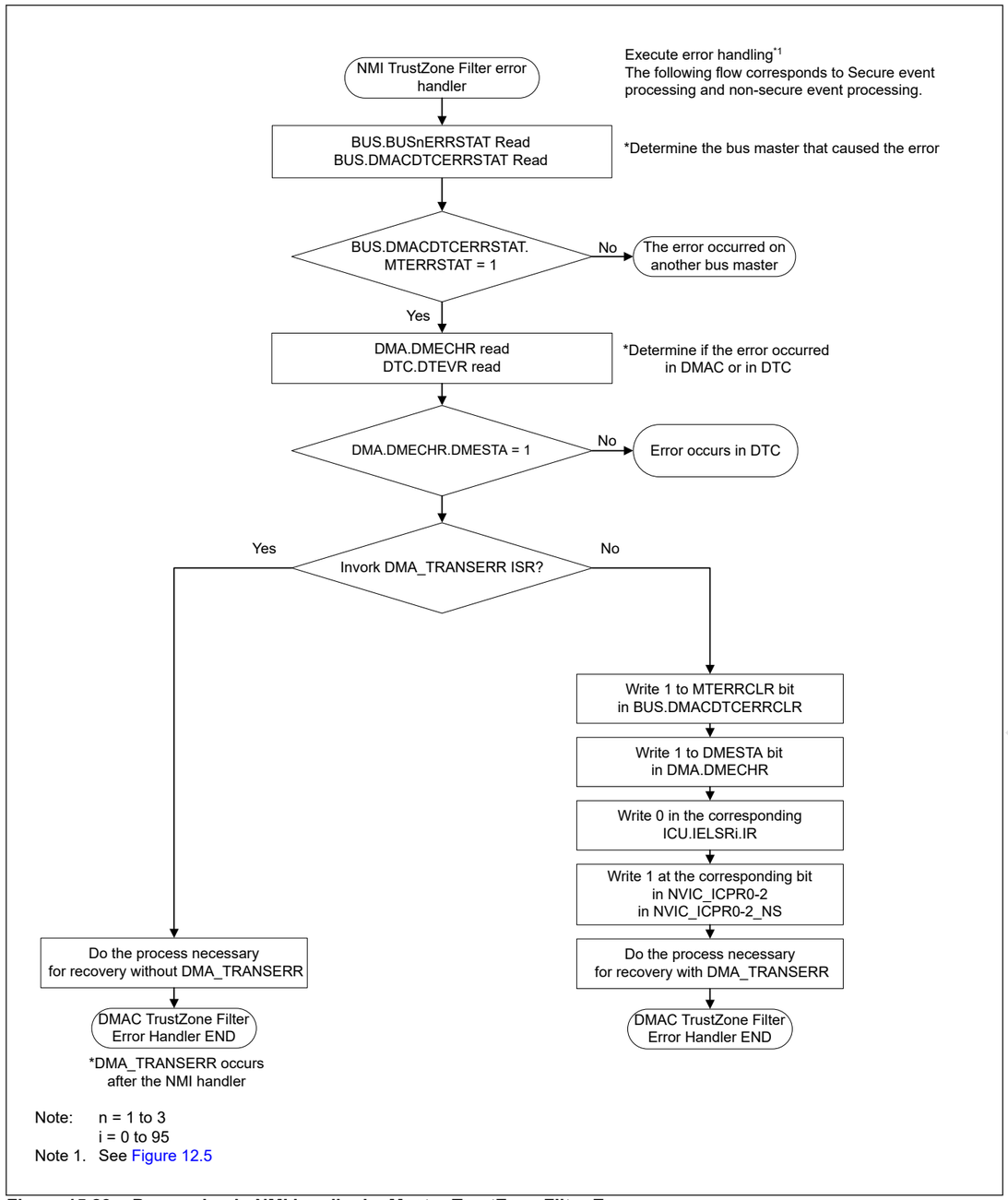


Figure 15.23 Processing in NMI handler by Master TrustZone Filter Error

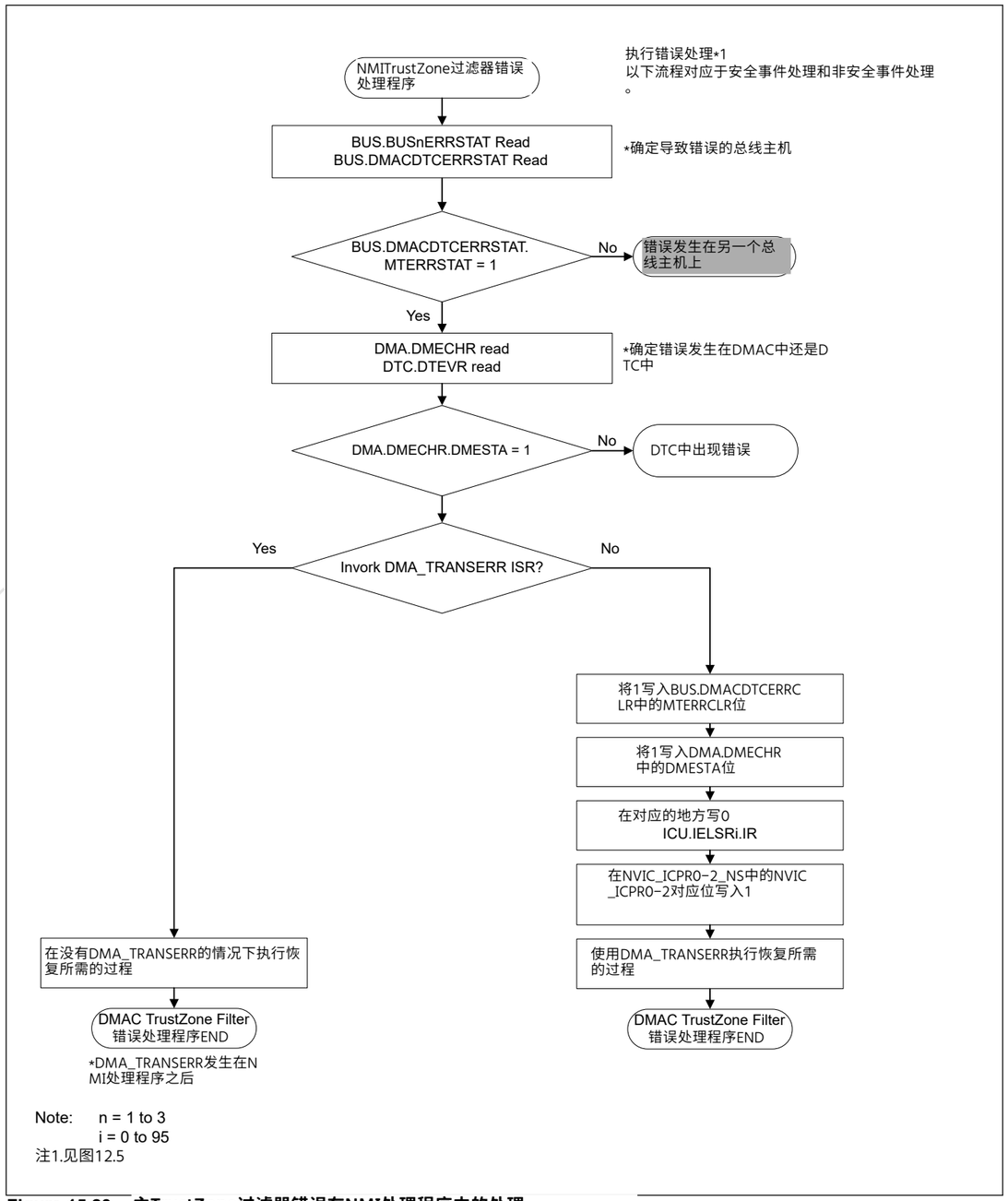


Figure 15.23 主TrustZone过滤器错误在NMI处理程序中的处理

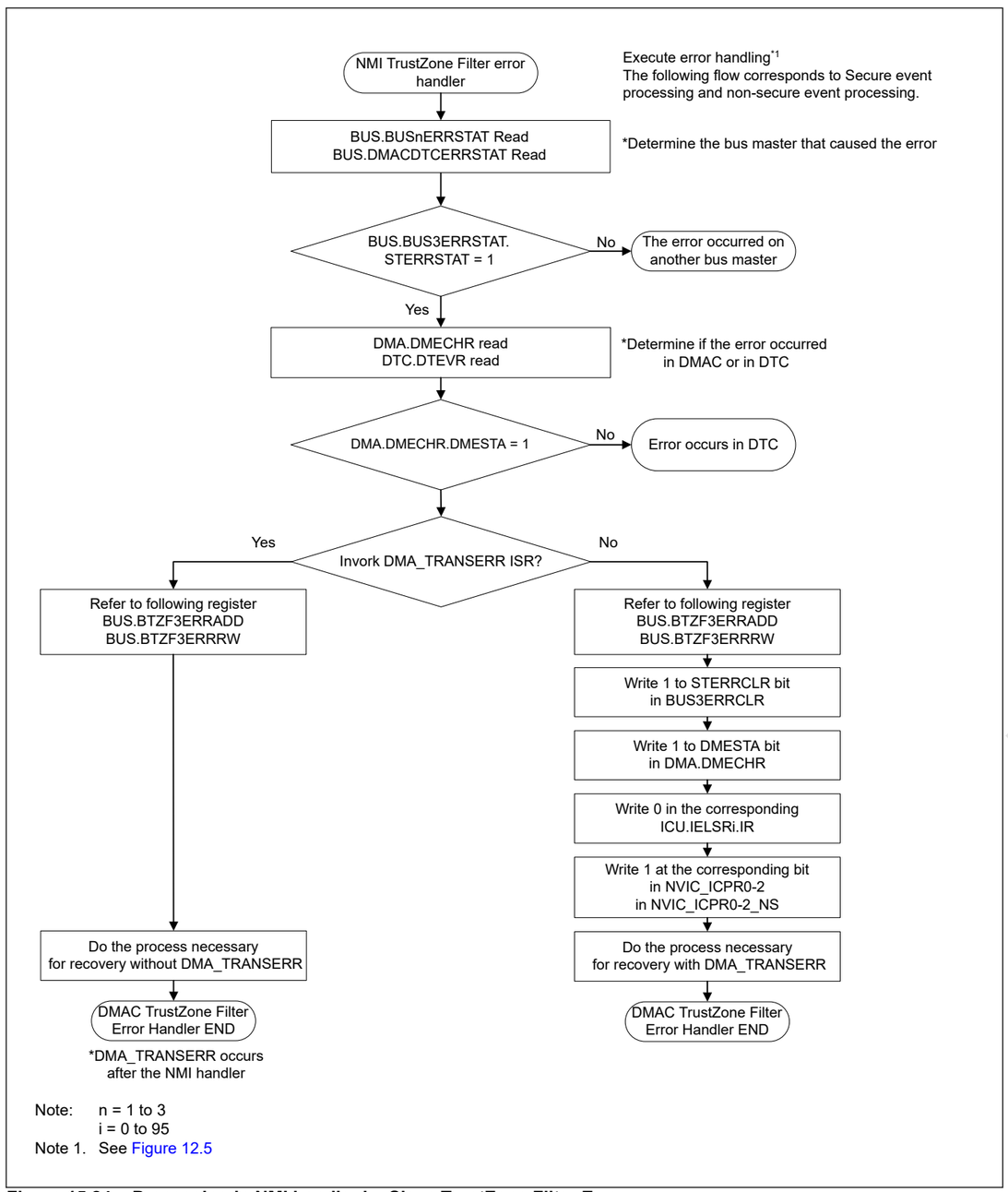


Figure 15.24 Processing in NMI handler by Slave TrustZone Filter Error

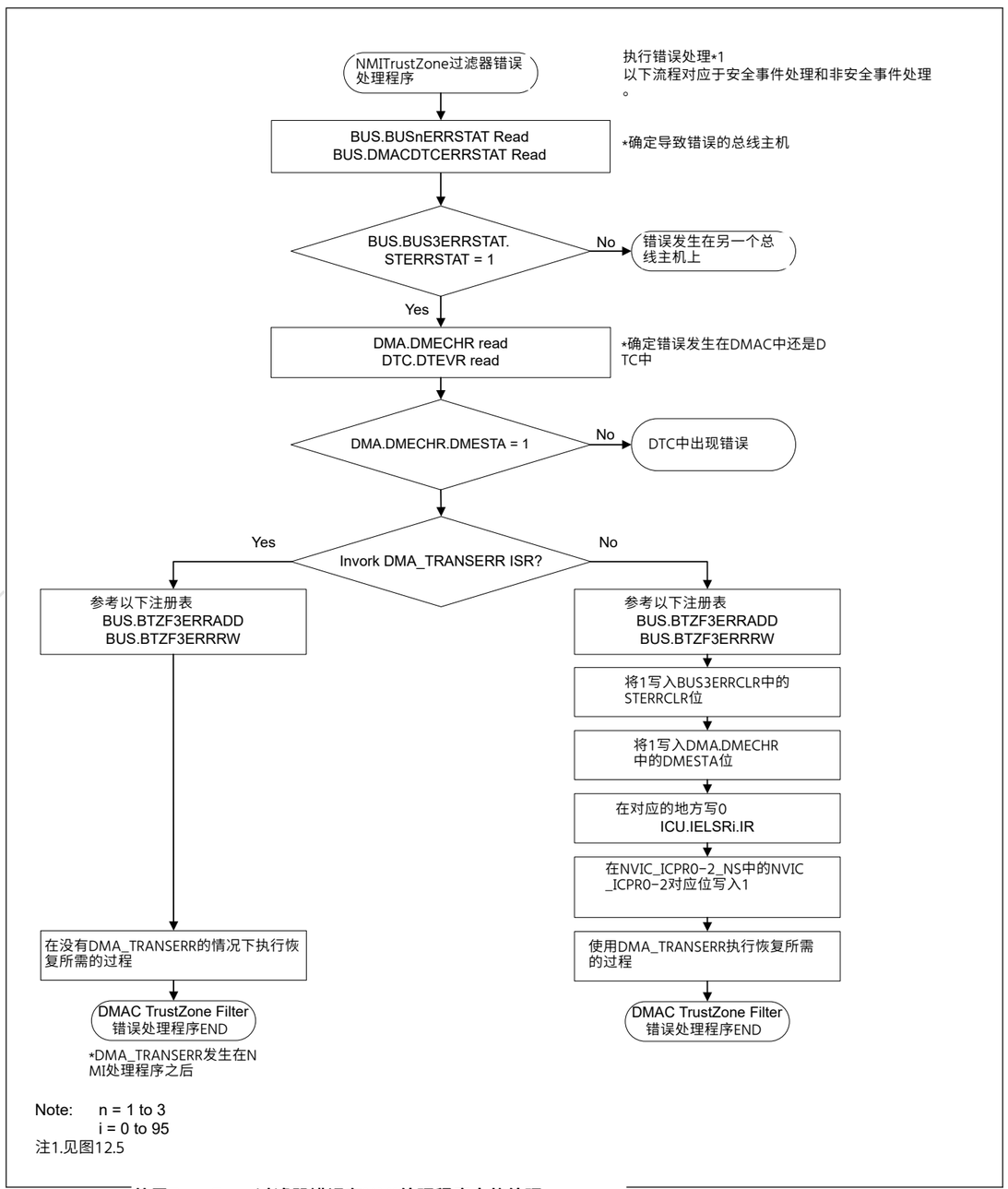


Figure 15.24 从属TrustZone过滤器错误在NMI处理程序中的处理

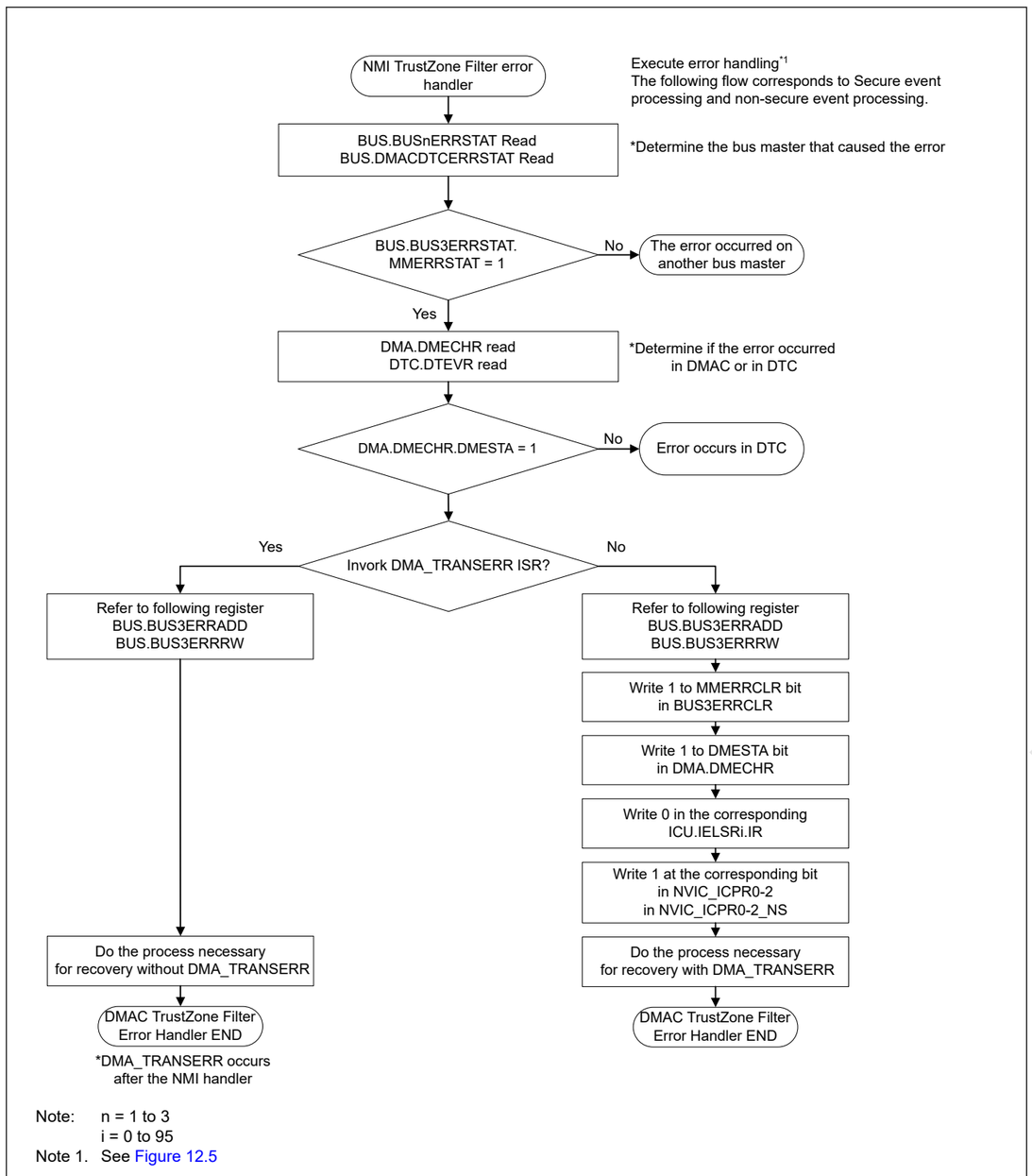


Figure 15.25 Processing in NMI handler by Master MPU Error

15.5.2 Processing on Error response detection interrupt request (DMA_TRANSERR) handler

The cause of error response detection interrupt request (DMA_TRANSERR) due to DMA transfer error is the Slave Bus Error or Illegal Access Error. Also, it occurs after the NMI handler error response detection interrupt request (DMA_TRANSERR) is not cleared by the NMI handler.

It is possible to confirm the cause of the error and the DMAC channel in which the error occurred.

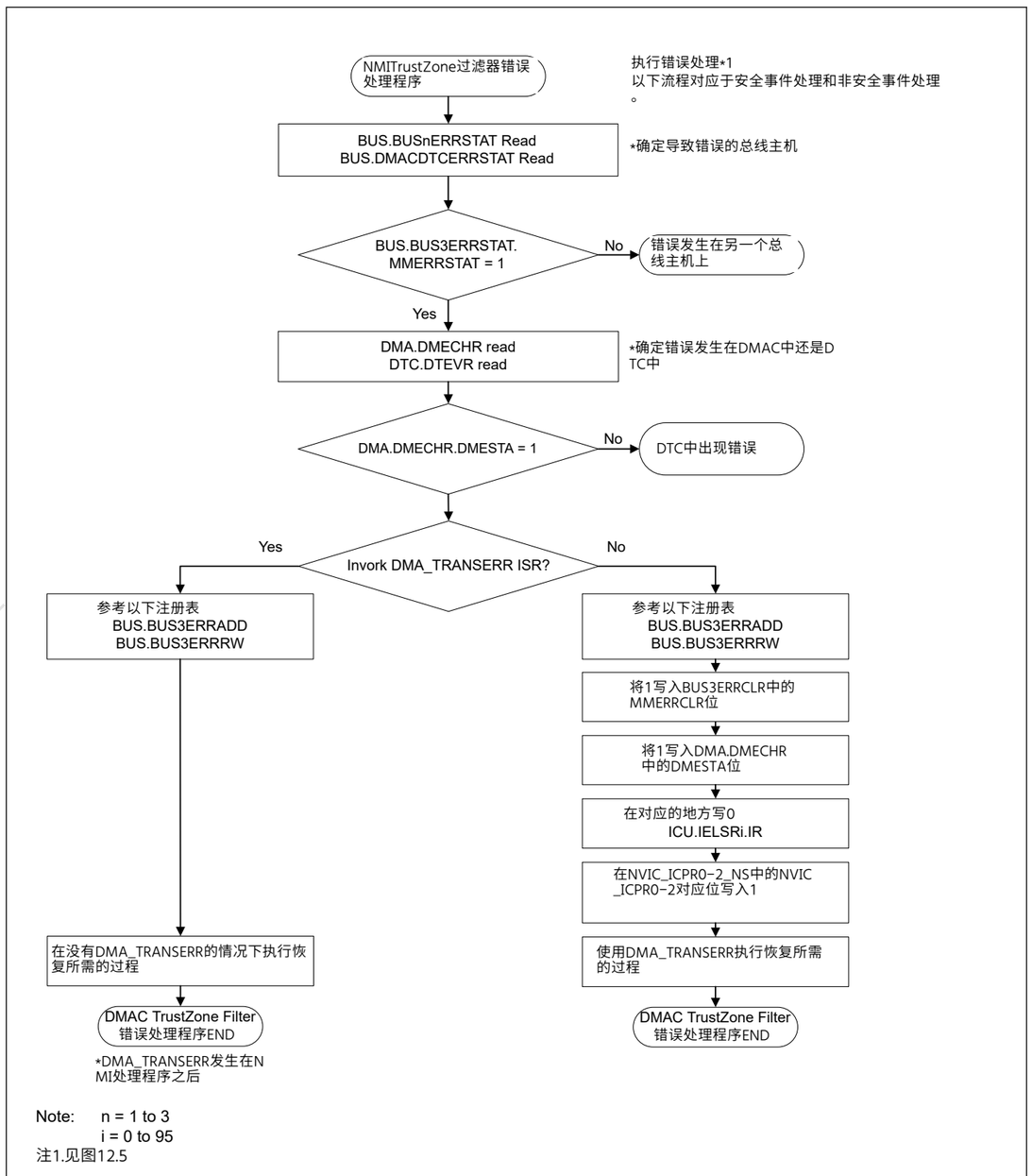


Figure 15.25 主MPU错误在NMI处理程序中的处理

15.5.2 错误响应检测中断请求(DMA_TRANSERR)处理程序的处理

由于DMA传输错误导致错误响应检测中断请求(DMA_TRANSERR)的原因是从总线错误或非法访问错误。此外，它发生在NMI处理程序错误响应检测中断请求(DMA_TRANSERR)未被NMI处理程序清除之后。

可以确认错误的原因和发生错误的DMAC通道。

Error cause confirmation procedure is shown Figure 15.26.

Figure 15.27 shows the flow for confirm the channel that caused the Master TrustZone Filter Error in DMAC

Figure 15.28 shows the flow for confirm the channel that caused the Slave TrustZone Filter Error in DMAC

Figure 15.29 shows the flow for confirm the channel and Security Attribute that caused the Master MPU Error in DMAC

Figure 15.30 shows the flow for confirm the channel and Security Attribute that caused the Slave Bus Error in DMAC

Figure 15.31 shows the flow for confirm the channel and Security Attribute that caused the Illegal Access Error in DMAC

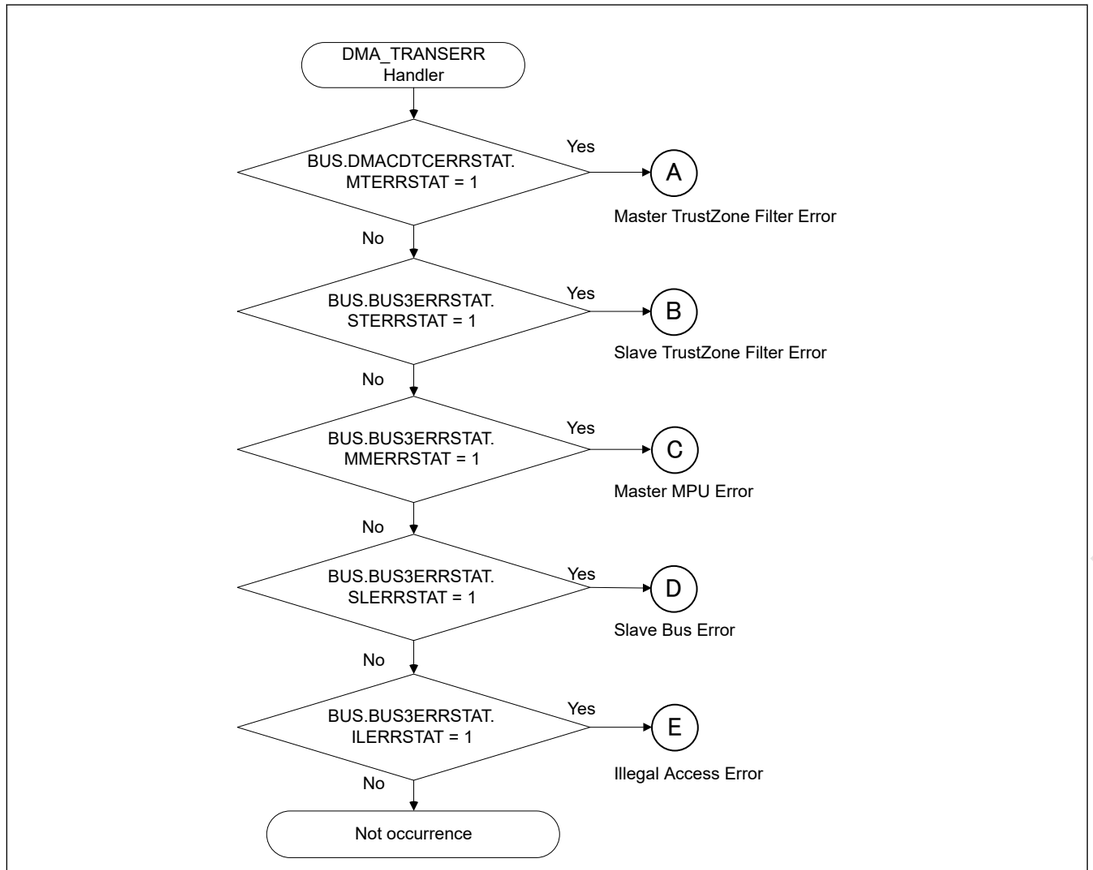


Figure 15.26 Transfer error factor judgment when the error response detection interrupt (DMA_TRANSERR) occurs

错误原因确认流程如图15.26所示。

图15.27显示了在DMAC中确认导致MasterTrustZoneFilterError的通道的流程

图15.28显示了在DMAC中确认导致SlaveTrustZoneFilterError的通道的流程

图15.29显示了在DMAC中确认导致MasterMPU错误的通道和安全属性的流程

图15.30显示了确认导致DMAC中从总线错误的通道和安全属性的流程

图15.31显示了在DMAC中确认导致非法访问错误的通道和安全属性的流程

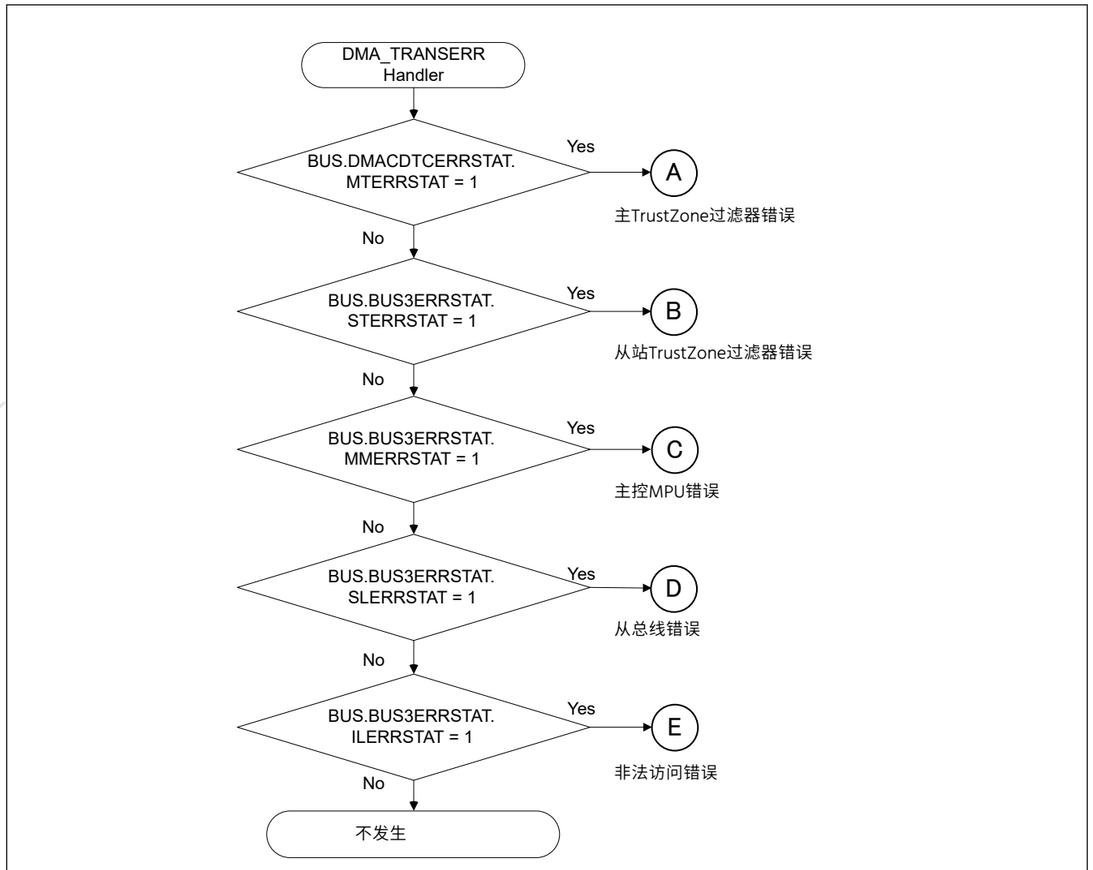


Figure 15.26 发生错误响应检测中断（DMA_TRANSERR）时的传输错误因素判断

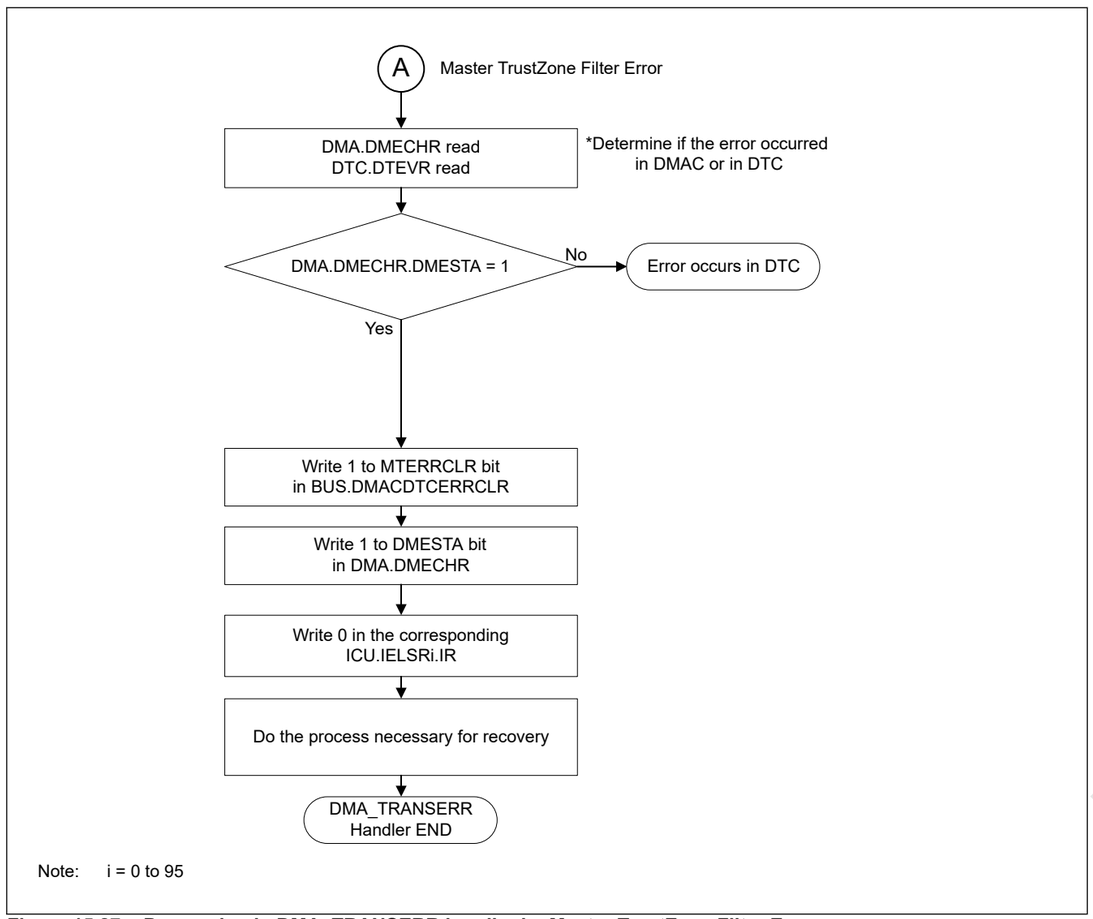


Figure 15.27 Processing in DMA_TRANSERR handler by Master TrustZone Filter Error

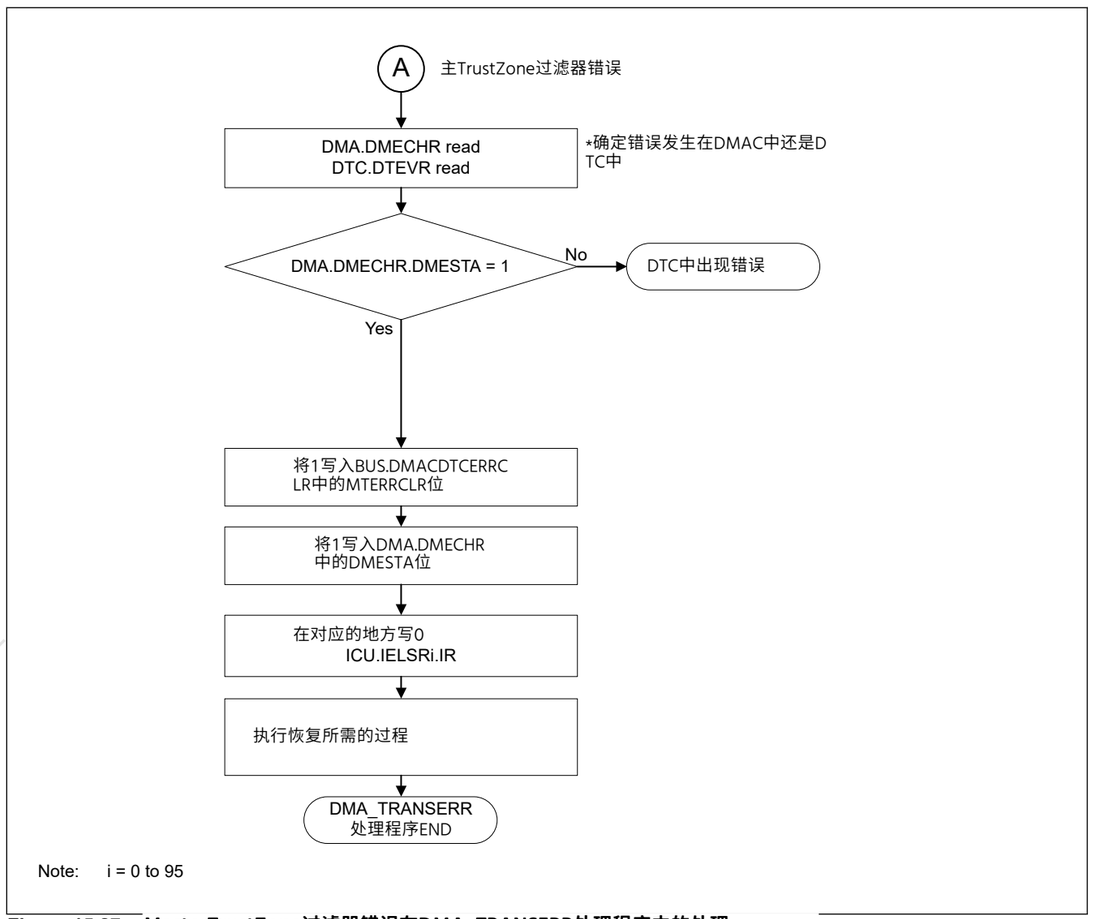


Figure 15.27 MasterTrustZone过滤器错误在DMA_TRANSERR处理程序中的处理

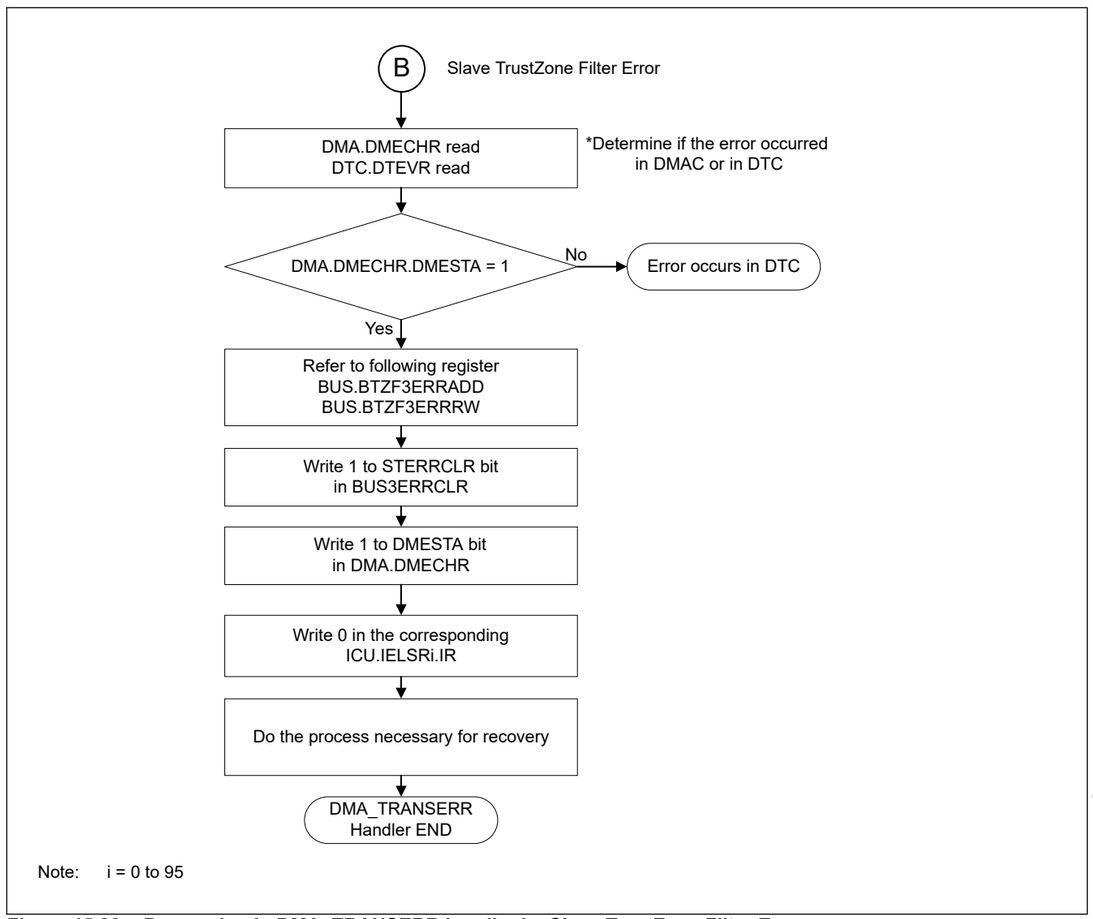


Figure 15.28 Processing in DMA_TRANSERR handler by Slave TrustZone Filter Error

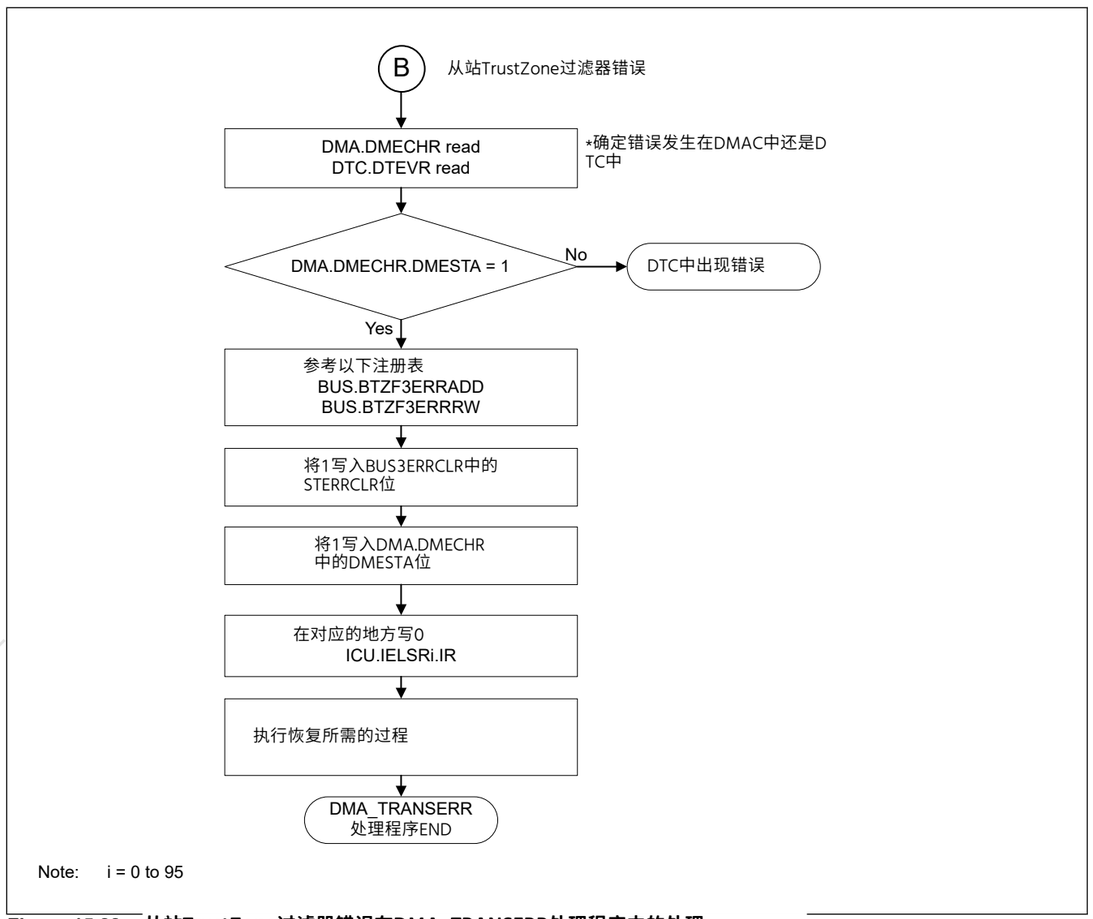


Figure 15.28 从站TrustZone过滤器错误在DMA_TRANSERR处理程序中的处理

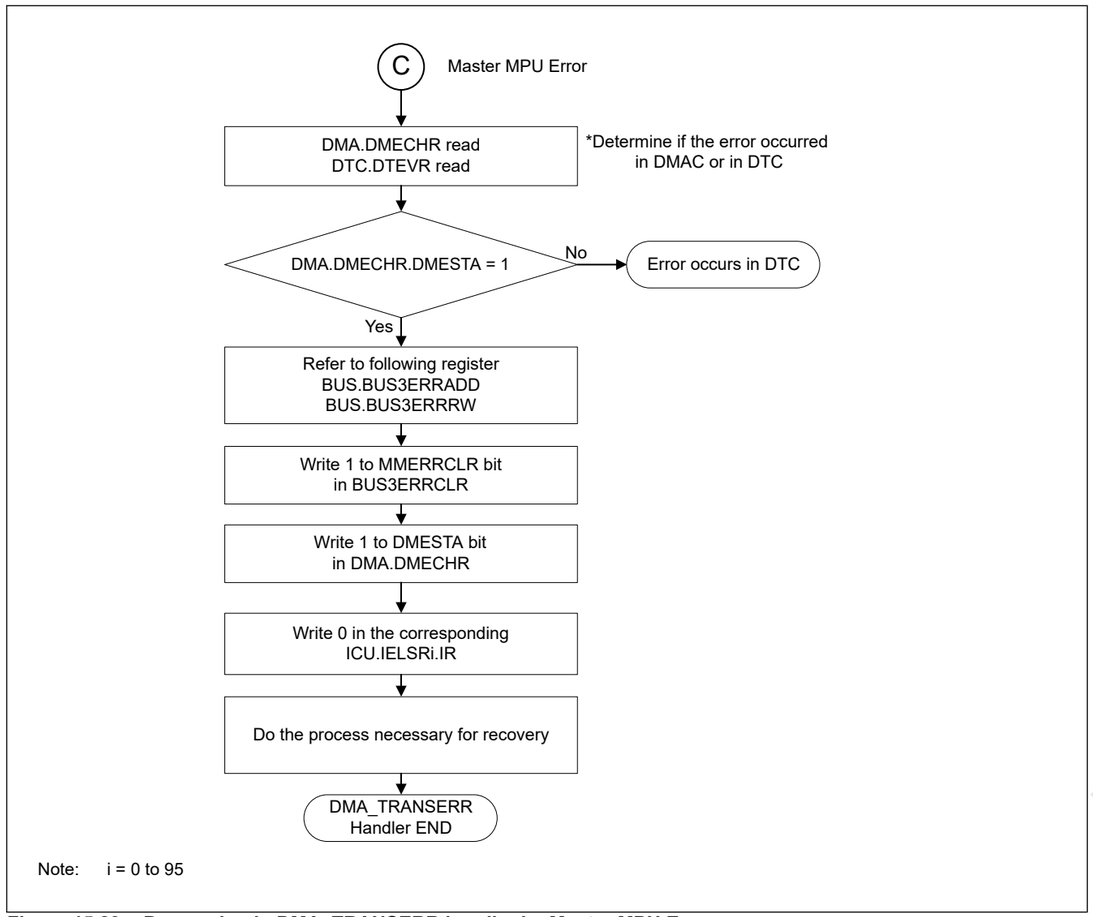


Figure 15.29 Processing in DMA_TRANSERR handler by Master MPU Error

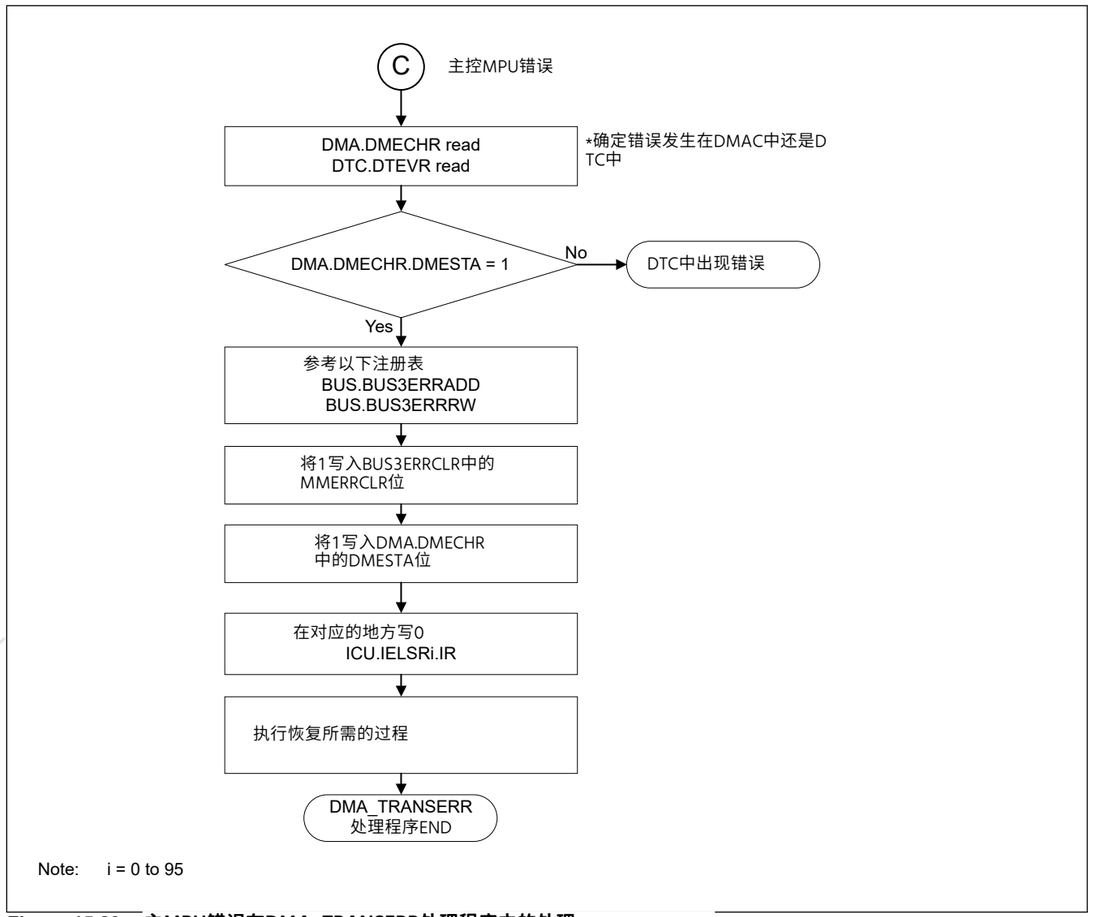


Figure 15.29 主MPU错误在DMA_TRANSERR处理程序中的处理

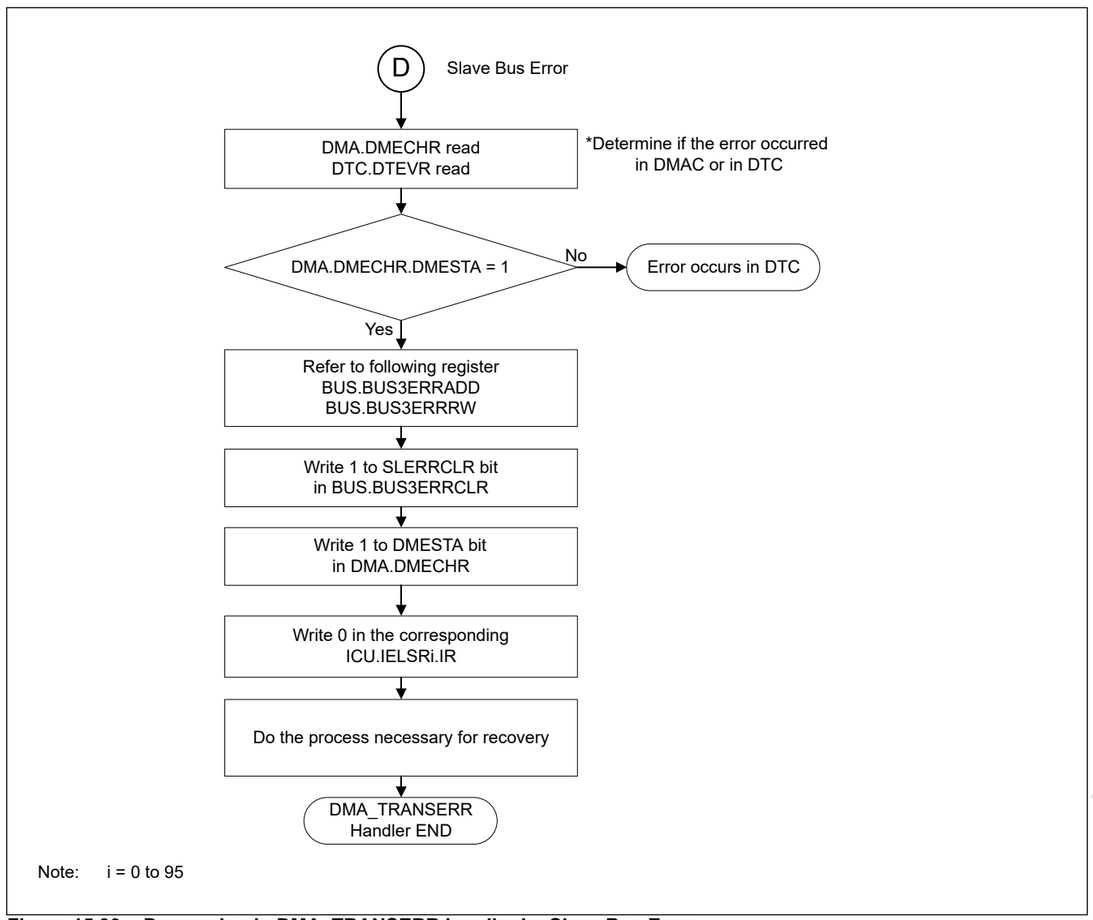


Figure 15.30 Processing in DMA_TRANSERR handler by Slave Bus Error

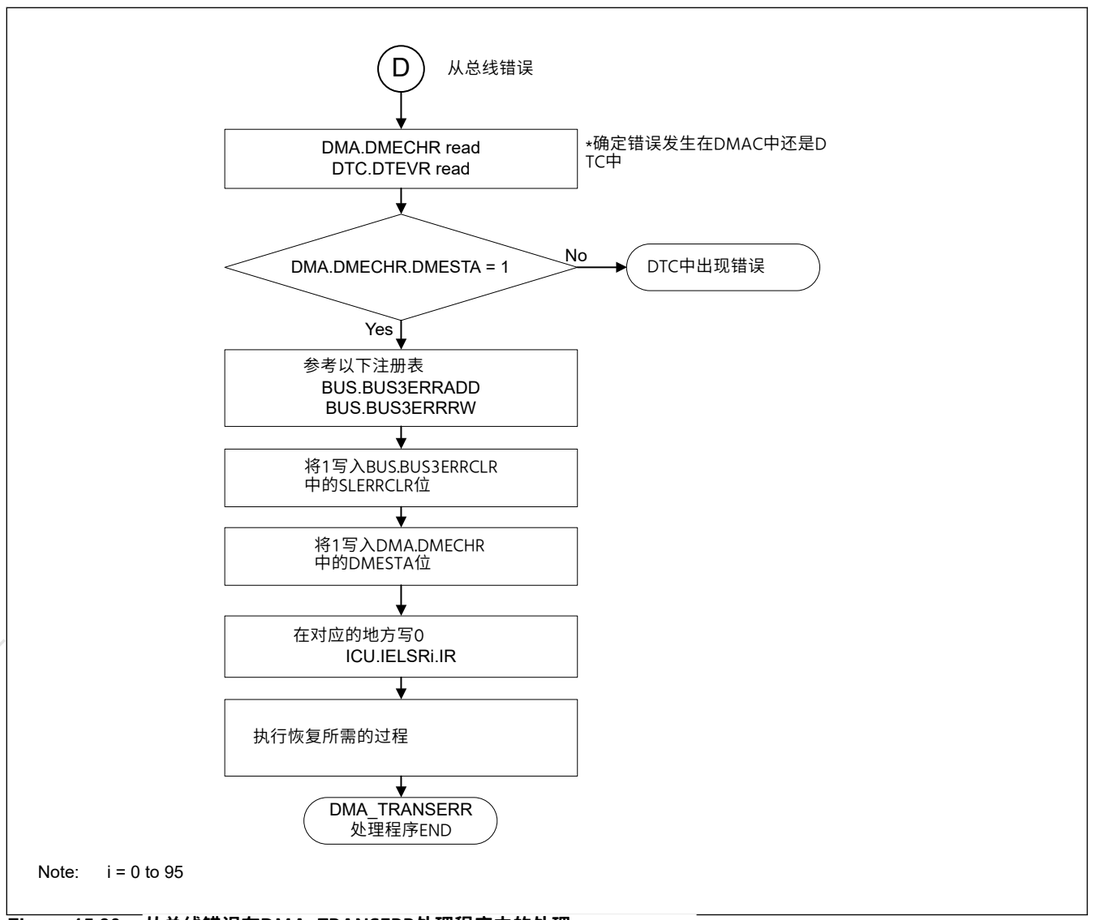


Figure 15.30 从总线错误在DMA_TRANSERR处理程序中的处理

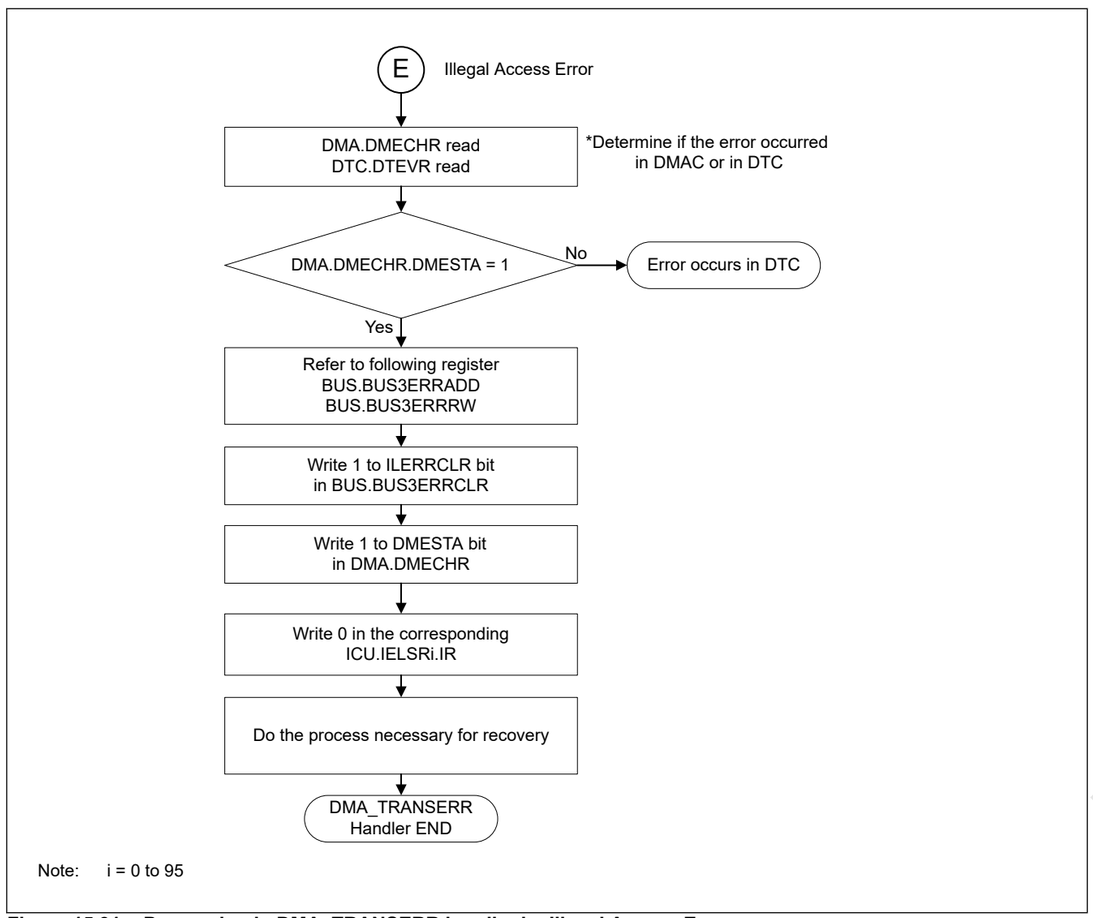


Figure 15.31 Processing in DMA_TRANSERR handler by Illegal Access Error

15.6 Interrupts

15.6.1 Transfer End Interrupt

Each DMAC channel can output an interrupt request (DMACn_INT) to the CPU or the DTC after transfer in response to one request is completed.

In repeat-block transfer mode, do not enable escape transfer end interrupt.

Table 15.20 lists the relation among the interrupt sources, the interrupt status flags, and the interrupt enable bits. Figure 15.32 shows the schematic logic diagram of interrupt outputs (DMACn (n = 0 to 7)). Figure 15.33 shows the DMAC interrupt handling routine to resume/terminate DMA transfer.

Table 15.20 Relation among Interrupt Sources, Interrupt Status Flags, and Interrupt Enable Bits (1 of 2)

Interrupt Sources	Interrupt Enable Bits	Interrupt Status Flags	Request Output Enable Bits
Transfer end	—	DMSTS.DTIF	DMINT.DTIE

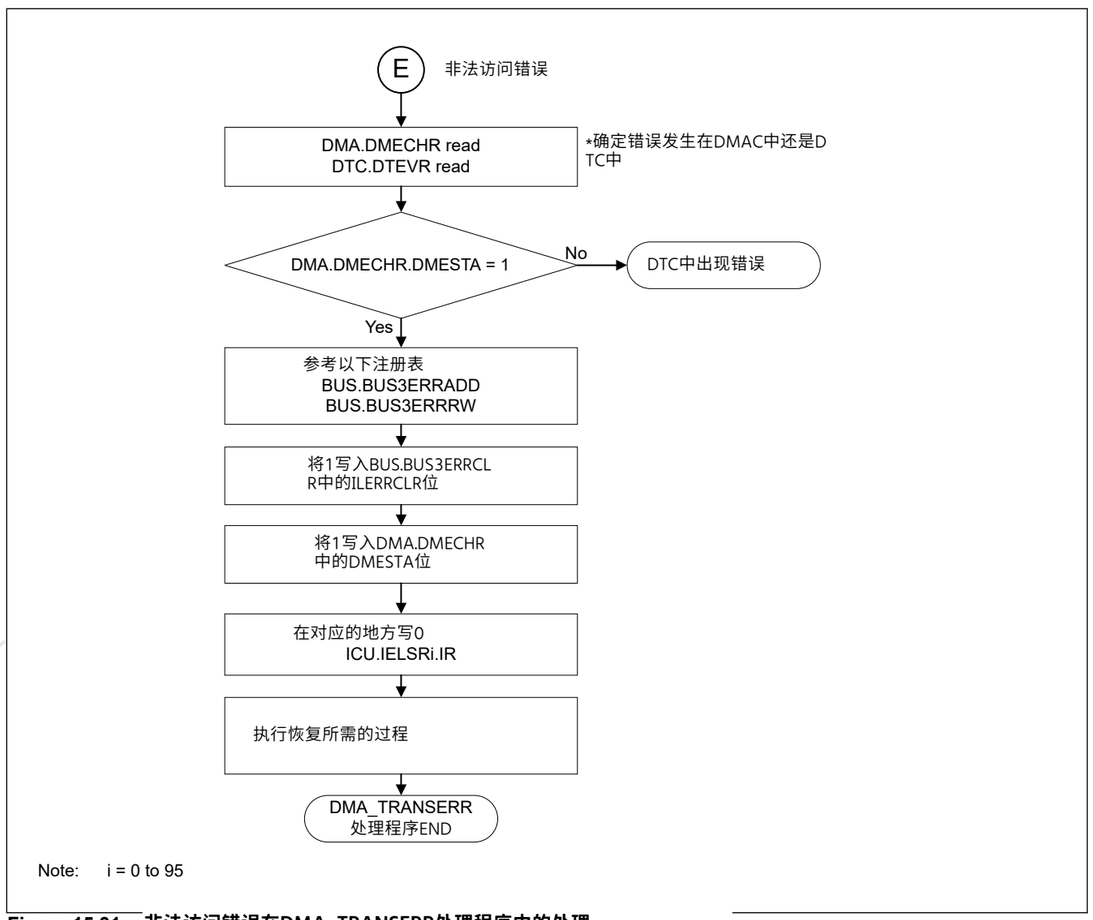


Figure 15.31 非法访问错误在DMA_TRANSERR处理程序中的处理

15.6 Interrupts

15.6.1 传输结束中断

每个DMAC通道可以在响应一个请求的传输完成后向CPU或DTC输出一个中断请求（DMACn_INT）。

在重复块传输模式下，不要启用转义传输结束中断。

表15.20列出了中断源、中断状态标志和中断使能位之间的关系。图15.32显示了中断输出(DMACn(n=0to7))的逻辑示意图。图15.33显示了用于恢复终止DMA传输的DMAC中断处理程序。

Table 15.20 中断源、中断状态标志和中断允许位之间的关系（1of2）

中断源	中断使能位	中断状态标志	请求输出使能 Bits
转账结束	—	DMSTS.DTIF	DMINT.DTIE

Table 15.20 Relation among Interrupt Sources, Interrupt Status Flags, and Interrupt Enable Bits (2 of 2)

Interrupt Sources		Interrupt Enable Bits	Interrupt Status Flags	Request Output Enable Bits
Escape transfer end	Repeat size end	DMINT.RPTIE	DMSTS.ESIF	DMINT.ESIE
	Source address extended repeat area overflow	DMINT.SARIE		
	Destination address extended repeat area overflow	DMINT.DARIE		

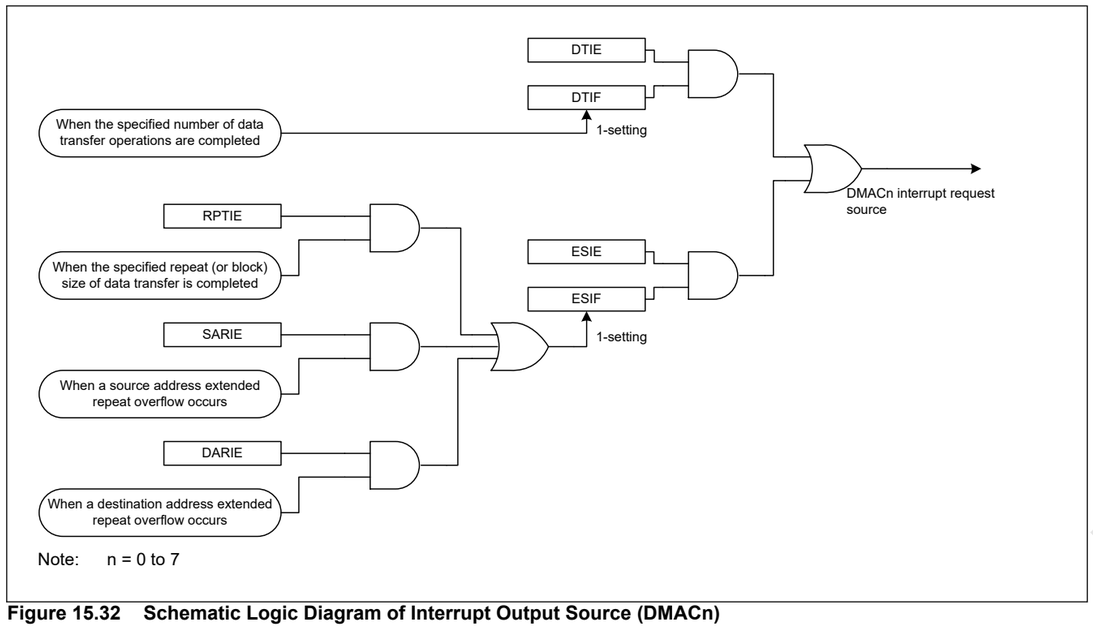


Figure 15.32 Schematic Logic Diagram of Interrupt Output Source (DMACn)

Specifically, the different procedures are used for canceling an interrupt to restart DMA transfer in the following two cases:

- When terminating a DMA transfer
- When continuing a DMA transfer

15.6.1.1 When Terminating a DMA Transfer

Write 0 to the DMSTS.DTIF flag to clear a transfer end interrupt, and to the DMSTS.ESIF flag to clear a repeat size interrupt and an extended repeat area overflow interrupt. The DMACn remains in the stop state. When starting another DMA transfer after that, set the appropriate registers, and set the DMCNT.DTE bit to 1 (DMA transfer enabled).

15.6.1.2 When Continuing a DMA Transfer

Write 1 to the DMCNT.DTE bit. The DMSTS.ESIF flag is automatically cleared to 0 (interrupt source cleared), and DMA transfer is resumed.

Table 15.20 中断源、中断状态标志和中断允许位之间的关系(2of2)

中断源		中断使能位	中断状态标志	请求输出使能 Bits
逃生转移结束	重复大小结束	DMINT.RPTIE	DMSTS.ESIF	DMINT.ESIE
	源地址扩展重复区溢出	DMINT.SARIE		
	目的地址扩展重复区溢出	DMINT.DARIE		

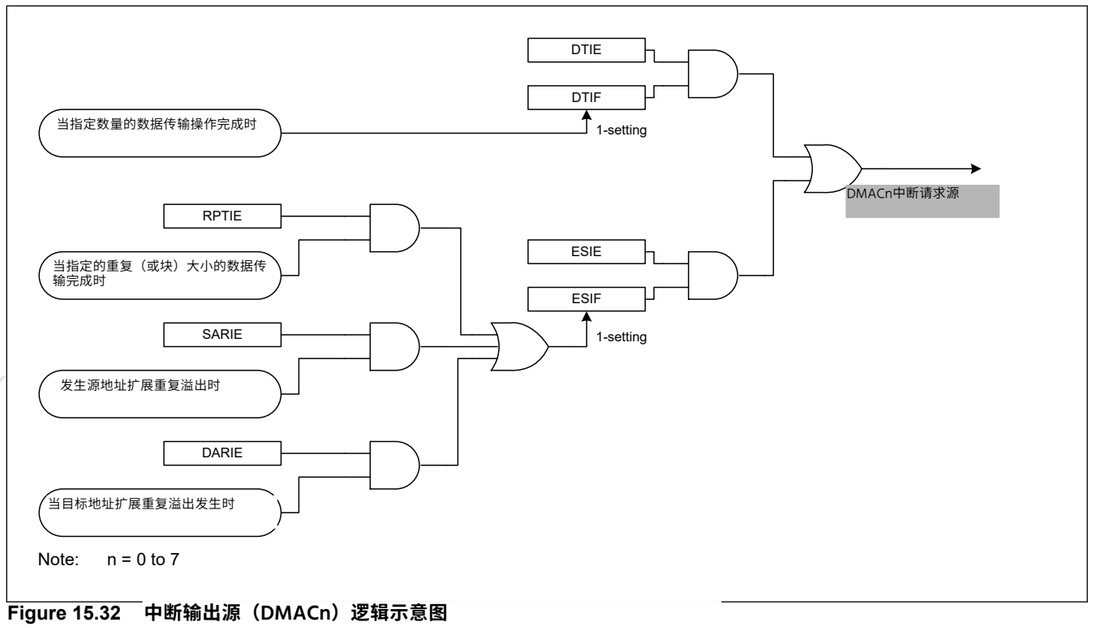


Figure 15.32 中断输出源（DMACn）逻辑示意图

具体来说，在以下两种情况下，不同的程序用于取消中断以重新启动DMA传输：

- ●终止DMA传输时
- ●继续DMA传输时

15.6.1.1 终止DMA传输时

将0写入DMSTS.DTIF标志以清除传输结束中断，写入DMSTS.ESIF标志以清除重复大小中断和扩展重复区域溢出中断。DMACn保持在停止状态。之后开始另一个DMA传输时，设置适当的寄存器，并将DMCNT.DTE位设置为1（启用DMA传输）。

15.6.1.2 继续DMA传输时

将1写入DMCNT.DTE位。DMSTS.ESIF标志自动清零（中断源清零），DMA传输恢复。

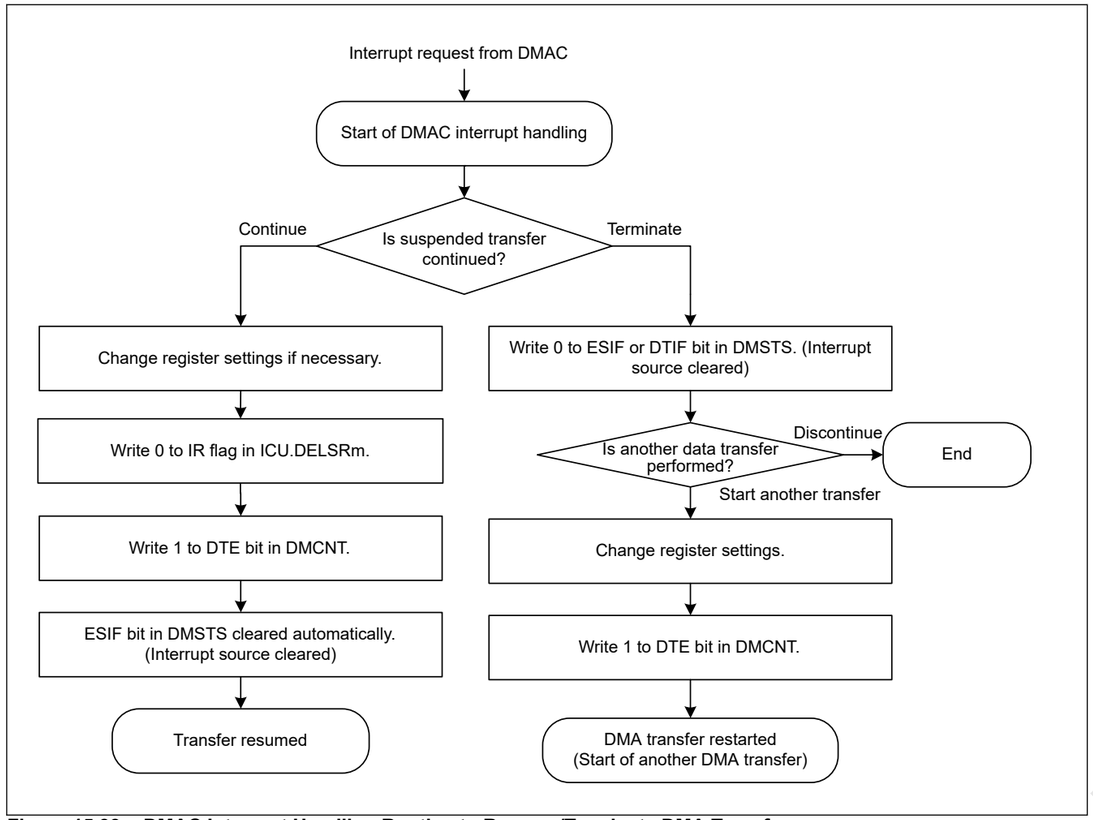


Figure 15.33 DMAC Interrupt Handling Routine to Resume/Terminate DMA Transfer

15.6.2 Transfer Error Interrupt

Error response detection interrupt request (DMA_TRANSERR) is generated from the DMAC/DTC when the transfer error is detected during DMAC transfer. The types of interrupts that occur when a DMAC transfer error occurs are listed in the Table 15.21. The Table 15.21 also shows error information stored when a transfer error occurs.

Table 15.21 Interrupt and error information due to DMAC transfer error cause

Transfer error factor	NMI/RESET*1 Request	Interrupt Request	Bus Error Status	Error Address Error R/W	Error Channel Information
Master TrustZone Filter (in DMAC/DTC)	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.DMACDTCERRSTAT.MTERRSTAT*1	—	DMA.DMECHR
Slave TrustZone Filter	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.BUS3ERRSTAT.STERRSTAT*1	BUS.BTZF3ERRADD BUS.BTZF3ERRRW	DMA.DMECHR
Master MPU	ICU.NMISR.BUSMST	DMA_TRANSERR	BUS.BUS3ERRSTAT.MMERRSTAT	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMA.DMECHR
Slave Bus Error	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.SLERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMA.DMECHR
Illegal Access Error	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.ILERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMA.DMECHR

Note 1. Interrupt generated, when NMI request selected as the operation after detection of the Master MPU error and the TrustZone Filter error. By confirming BUS.BUS3ERRSTAT and BUS.DMACDTCERRSTAT, judge whether it is the Master or the Slave.
Note 2. If the error response detection interrupt (DMA_TRANSERR) occurs and NMI of the Master MPU or NMI of the TrustZone Filter has not occurred, treat it as the Illegal address access error or the Slave Bus Error. It can be judged also by BUS.BUS3ERRSTAT and BUS. DMACDTCERRSTAT.

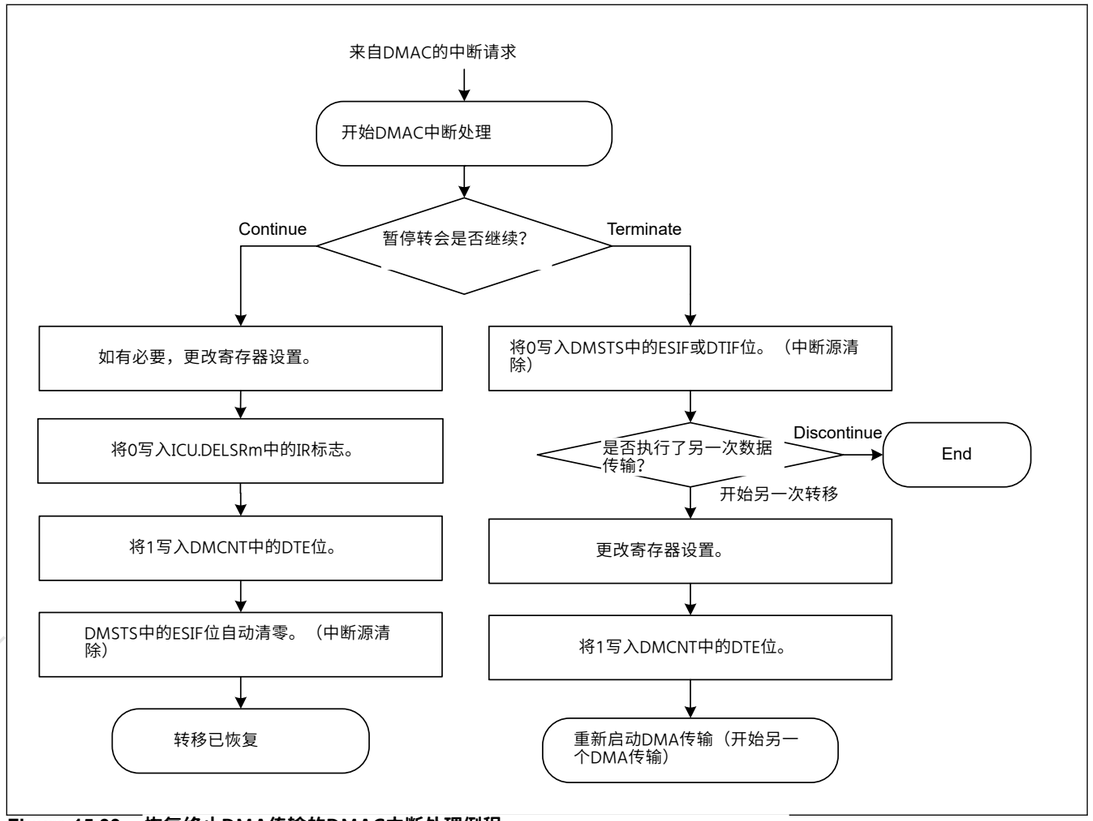


Figure 15.33 恢复终止DMA传输的DMAC中断处理例程

15.6.2 传输错误中断

在DMAC传输期间检测到传输错误时，从DMACDTC生成错误响应检测中断请求(DMA_TRANSERR)。发生DMAC传输错误时发生的中断类型在表15.21中列出。表15.21还显示了发生传输错误时存储的错误信息。

Table 15.21 由于DMAC传输错误原因导致的中断和错误信息

传递误差因子	NMI/RESET*1 Request	中断请求	总线错误状态	错误地址 Error R/W	错误通道 Information
Master TrustZone Filter (in DMAC/DTC)	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.DMACDTCERRSTAT.MTERRSTAT*1	—	DMA.DMECHR
Slave TrustZone Filter	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.BUS3ERRSTAT.STERRSTAT*1	BUS.BTZF3ERRADD BUS.BTZF3ERRRW	DMA.DMECHR
Master MPU	ICU.NMISR.BUSMST	DMA_TRANSERR	BUS.BUS3ERRSTAT.MMERRSTAT	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMA.DMECHR
从总线错误	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.SLERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMA.DMECHR
非法访问错误	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.ILERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMA.DMECHR

注意1.中断，当NMI请求在检测主MPU错误和Trustzone滤波器错误后选择为操作时中断。通过确认BUS.BUS3ERRSTAT和BUS.DMACDTCERRSTAT，判断是Master还是Slave。
注2.如果错误响应检测中断(DMA_TRANSERR)发生且MasterMPU的NMI或TrustZoneFilter的NMI未发生，则将其视为Illegaladdressaccesserror或SlaveBusError。也可以通过BUS.BUS3ERRSTAT和BUS来判断。DMACDTCERRSTAT。

Note that if the bus error occurs when writing the last data of transfer, the transfer end event and the error response detection interrupt (DMA_TRANSERR) occurs.

15.7 Event Link

Each DMAC channel outputs an event link request signal (DMACn_INT) every time it completes a data transfer, or a block transfer in block transfer mode.

For details, see section 17, Event Link Controller (ELC).

If a bus error occurs when writing the last data of transfer, a transfer end event and error response detection interrupt (DMA_TRANSERR) occurs.

15.8 Low-Power Consumption Function

Before entering the module-stop state or Software Standby mode, or Deep Software Standby mode, you must first set the DMAST.DMST bit to 0 (the DMAC module suspended), and use the settings in the sections that follow.

(1) Module-stop function

Writing 1 to the MSTPCRA.MSTPA22 bit enables the module-stop function of the DMAC. If a DMA transfer is in progress when 1 is written to the MSTPA22 bit, the transition to the module-stop state proceeds after the DMA transfer ends. Access to the DMAC registers is prohibited while the MSTPA22 bit is 1. Writing 0 to the MSTPA22 bit releases the DMAC from the module-stop state.

(2) Software Standby mode and Deep Software Standby mode

Use the settings described in section 10.7.1. Transitioning to Software Standby Mode, or in section 10.9.1. Transitioning to Deep Software Standby Mode .

If DMA transfer operations are in progress when the WFI instruction is executed, the DMA transfer completes before the transition to Software Standby mode or Deep Software Standby mode.

(3) Notes on low power consumption function

For information on the WFI instruction and register settings, see section 10.10.7. Timing of WFI Instruction.

To perform a DMA transfer after returning from a low power consumption mode, set the DMAST.DMST bit to 1 again. To use a request that is generated in Software Standby mode as an interrupt request to the CPU but not as a DMAC startup request, specify the CPU as the interrupt request destination, as described in section 12.4.1. Detecting Interrupts, and then execute the WFI instruction.

15.9 Usage Notes

15.9.1 Access to the Registers during DMA Transfer

Do not write to the following registers while the DMSTS.ACT flag of the same channel is set to 1 (DMAC active state) or the DMCNT.DTE bit of the same channel is set to 1 (DMA transfer enabled):

- DMSAR
- DMDAR
- DMCRA
- DMCRB
- DMTMD
- DMINT
- DMAMD
- DMOFR
- DMSBS
- DMDBS
- DMSRR

请注意，如果在写入传输的最后一个数据时发生总线错误，则会发生传输结束事件和错误响应检测中断（DMA_TRANSERR）。

15.7 活动链接

每个DMAC通道在每次完成数据传输或块传输模式下的块传输时都会输出一个事件链接请求信号(DMACn_INT)。

有关详细信息，请参阅第17节，事件链接控制器(ELC)。

如果在写入传输的最后一个数据时发生总线错误，则会发生传输结束事件和错误响应检测中断(DMA_TRANSERR)。

15.8 低功耗功能

在进入模块停止状态或软件待机模式或深度软件待机模式之前，您必须先设置DMAST.DMST位为0（DMAC模块挂起），并使用以下部分中的设置。

(1) Module-stop function

向MSTPCRA.MSTPA22位写入1可启用DMAC的模块停止功能。如果在向MSTPA22位写入1时正在进行DMA传输，则在DMA传输结束后继续转换到模块停止状态。当MSTPA22位为1时，禁止访问DMAC寄存器。将0写入MSTPA22位可将DMAC从模块停止状态释放。

(2) 软件待机模式和深度软件待机模式

使用第10.7.1节中描述的设置。转换到软件待机模式，或在第10.9.1节中。过渡到深度软件待机模式。

如果在执行WFI指令时DMA传输操作正在进行，则DMA传输在转换到软件待机模式或深度软件待机模式之前完成。

(3) 低功耗功能注意事项

有关WFI指令和寄存器设置的信息，请参阅第10.10.7节。WFI指令的时间安排。

要在从低功耗模式返回后执行DMA传输，请将DMAST.DMST位再次设置为1。要将在软件待机模式下生成的请求用作对CPU的中断请求但不用作DMAC启动请求，请将CPU指定为中断请求目标，如第12.4.1节所述。检测中断，然后执行WFI指令。

15.9 使用说明

15.9.1 在DMA传输期间访问寄存器

当同一通道的DMSTS.ACT标志设置为1（DMAC活动状态）或同一通道的DMCNT.DTE位设置为1（启用DMA传输）时，请勿写入以下寄存器：

- DMSAR
- DMDAR
- DMCRA
- DMCRB
- DMTMD
- DMINT
- DMAMD
- DMOFR
- DMSBS
- DMDBS
- DMSRR

- DMDRR
- ICUSARC
- DMACSAR

15.9.2 DMA Transfer to Reserved Areas

DMA transfer to the reserved areas is prohibited. If such an access is made, transfer results are not guaranteed. For details on the reserved areas, see section 4, Address Space.

15.9.3 Setting of DMAC Event Link Setting Register of the Interrupt Controller Unit (ICU.DELSRn n = 0 to 7)

The DMAC event link setting register (ICU.DELSRn) should be set while the DMA transfer enable bit (DMCNT.DTE) is cleared to 0 (DMA transfer is disabled). Moreover, the DTC activation enable register (ICU.IELSRn.DTCE (n = 0 to 95)) that corresponds to the same event number that has been set by the ICU.DELSRn register should not be set to 1. For details on the ICU.IELSRn.DTCE and ICU.DELSRn, see section 12, Interrupt Controller Unit (ICU).

15.9.4 Suspending or Restarting DMAC Activation

To suspend a DMAC activation request, write 0x00 to the DMAC Event Link select bits (ICU.DELSRn.DELS[8:0]). To restart the DMA transfer, write the event number to the ICU.DELSRn.DELS[8:0] bits following the settings shown in section 15.3.10. Activating the DMAC.

15.9.5 Precautions for Resuming DMA Transfer

A DMAC activation request might occur in the next request after a DMA transfer completes. If this happens, the DMA transfer starts and the DMAC activation request is held in the DMAC. To prevent this, stop the DMAC activation requests by setting the DELSRn.DELS[8:0] bits in the ICU to 0.

When a DMAC activation request occurs after the last round of the DMA transfer is generated, clear the DMAC activation request with either of the following approaches.

- Clear the DMAC activation request with a DMA dummy transfer.
- Set the DMCNT.DTE bit to 0 and then set the ICU.DELSRn.IR flag to 0.

See Figure 15.34.

- DMDRR
- ICUSARC
- DMACSAR

15.9.2 DMA传输到保留区域

禁止对保留区域进行DMA传输。如果进行此类访问，则无法保证传输结果。有关保留区域的详细信息，请参阅第4节，地址空间。

15.9.3 中断控制器单元的DMAC事件链接设置寄存器的设置(ICU.DELSRnn=0到7)

DMAC事件链接设置寄存器(ICU.DELSRn)应在DMA传输启用位(DMCNT.DTE)清除为0（禁用DMA传输）时设置。此外，与ICU.DELSRn寄存器设置的相同事件编号对应的DTC激活使能寄存器(ICU.IELSRn.DTCE(n=0至95))不应设置为1。有关ICU的详细信息.IELSRn.DTCE和ICU.DELSRn，请参见第12节，中断控制器单元(ICU)。

15.9.4 暂停或重新启动DMAC激活

要暂停DMAC激活请求，请将0x00写入DMAC事件链接选择位(ICU.DELSRn.DELS[8:0])。要重新启动DMA传输，请按照第15.3.10节中所示的设置将事件编号写入ICU.DELSRn.DELS[8:0]位。激活DMAC。

15.9.5 恢复DMA传输的注意事项

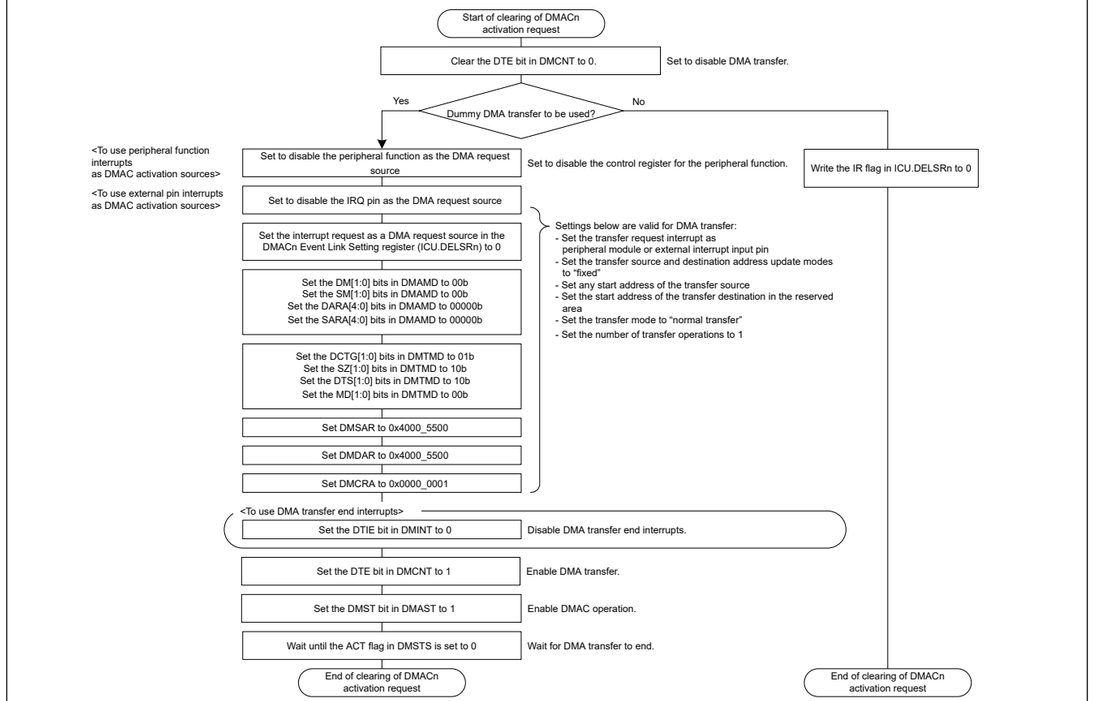
DMA传输完成后的下一个请求中可能会出现DMAC激活请求。如果发生这种情况，DMA传输开始并且DMAC激活请求被保存在DMAC中。为防止这种情况，请通过将ICU中的DELSRn.DELS[8:0]位设置为0来停止DMAC激活请求。

当最后一轮DMA传输生成后出现DMAC激活请求时，可通过以下任一方法清除DMAC激活请求。

●使用DMA虚拟传输清除DMAC激活请求。

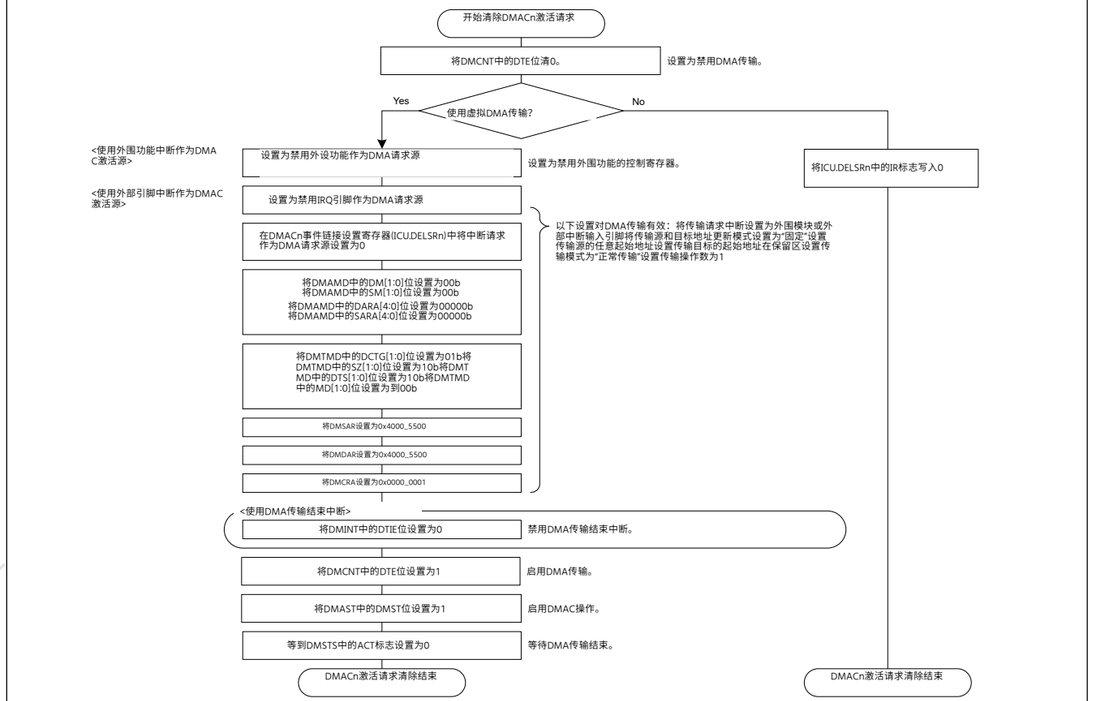
●将DMCNT.DTE位设置为0，然后将ICU.DELSRn.IR标志设置为0。

请参见图15.34。



Note: n: 0 to 7

Figure 15.34 Example of register setting procedure to clear the DMAC activation interrupt



Note: n: 0 to 7

Figure 15.34 清除DMAC激活中断的寄存器设置过程示例

16. Data Transfer Controller (DTC)

16.1 Overview

A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 16.1 lists the DTC specifications and Figure 16.1 shows DTC block diagram.

Table 16.1 DTC specifications

Parameter	Description
Transfer modes	● Normal transfer mode A single activation leads to a single data transfer. ● Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the start address after the number of data transfers reaches the specified repeat size. The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits (1024 bytes) ● Block transfer mode A single activation leads to a transfer of a single block. The maximum block size is 256 × 32 bits = 1024 bytes.
Transfer channel	● Channel transfer can be associated with the interrupt source (transferred by a DTC activation request from the ICU) ● Multiple data units can be transferred on a single activation source (chain transfer) ● Chain transfers are selectable to either execute when the counter is 0, or always execute.
Transfer space	● 4 GB area from 0x0000_0000 to 0xFFFF_FFFF, excluding reserved areas
Data transfer units	● Single data unit: 1 byte (8 bits), 1 halfword (16 bits), 1 word (32 bits) ● Single block size: 1 to 256 data units.
CPU interrupt source	● An interrupt request can be generated to the CPU on a DTC activation interrupt ● An interrupt request can be generated to the CPU after a single data transfer ● An interrupt request can be generated to the CPU after a data transfer of a specified volume.
Processing on DTC transfer error	● When the DTC transfer error occurs, it stops the transfer that caused the error ● Request to clear the register for activation request of DTC error number to ICU
Error response detection interrupt	Generated when the DTC transfer error occurs
Event link function	An event link request is generated after one data transfer (for block, after one block transfer)
Read skip	Read of transfer information can be skipped
Write-back skip	When the transfer source or destination address is specified as fixed, a write-back of transfer information can be skipped
TrustZone	TrustZone violation area of Flash and SRAM is detected in advance before access the bus.
Module-stop function	Module-stop state can be set to reduce power consumption
TrustZone Filter	Security attribution can be set for each activation source

Note: Security attribution Regiser of DTC is described in ICU.ICUSARG, ICU.ICUSARH and ICU.ICUSARI

16. 数据传输控制器(DTC)

16.1 Overview

数据传输控制器(DTC)模块用于在被中断请求激活时传输数据。

表16.1列出了DTC规范，图16.1显示了DTC框图。

Table 16.1 DTC specifications

Parameter	Description
传输模式	● 正常传输模式 单次激活导致单次数据传输。 ● 重复传输模式 单次激活导致单次数据传输。 数据传输次数达到指定的重复大小后，传输地址返回起始地址。最大重复传输次数为256，最大数据传输大小为256×32位（1024字节） ● 块传输模式 单个激活导致单个块的传输。最大块大小为256×32位=1024字节。
传输通道	● 通道传输可以与中断源相关联（由来自ICU的DTC激活请求传输） ● 可以在单个激活源上传输多个数据单元（链式传输） ● 链式传输可选择在计数器为0时执行或始终执行。
转移空间	● 4GB区域，从0x0000_0000到0xFFFF_FFFF，不包括保留区域
数据传输单元	● 单个数据单元：1个字节（8位）、1个半字（16位）、1个字（32位） ● 单块大小：1到256个数据单元。
CPU中断源	● 可以在DTC激活中断时向CPU生成中断请求 ● 单次数据传输后可向CPU产生中断请求 ● 在指定卷的数据传输后，可以向CPU产生中断请求。
DTC传输错误的处理	● 当发生DTC传输错误时，它会停止导致错误的传输 ● 向ICU请求清除DTC错误号激活请求的寄存器
错误响应检测中断	发生DTC传输错误时生成
事件链接功能	一次数据传输后产生事件链接请求（对于块，在一次块传输后）
阅读跳过	可以跳过读取传输信息
Write-back skip	当传输源或目标地址指定为固定时，可以跳过传输信息的回写
TrustZone	在访问总线之前，预先检测到Flash和SRAM的TrustZone违规区域。
Module-stop function	可设置模块停止状态以降低功耗
TrustZone Filter	可以为每个激活源设置安全属性

Note: ICU.ICUSARG、ICU.ICUSARH和ICU.ICUSARI中描述了DTC的安全属性注册器

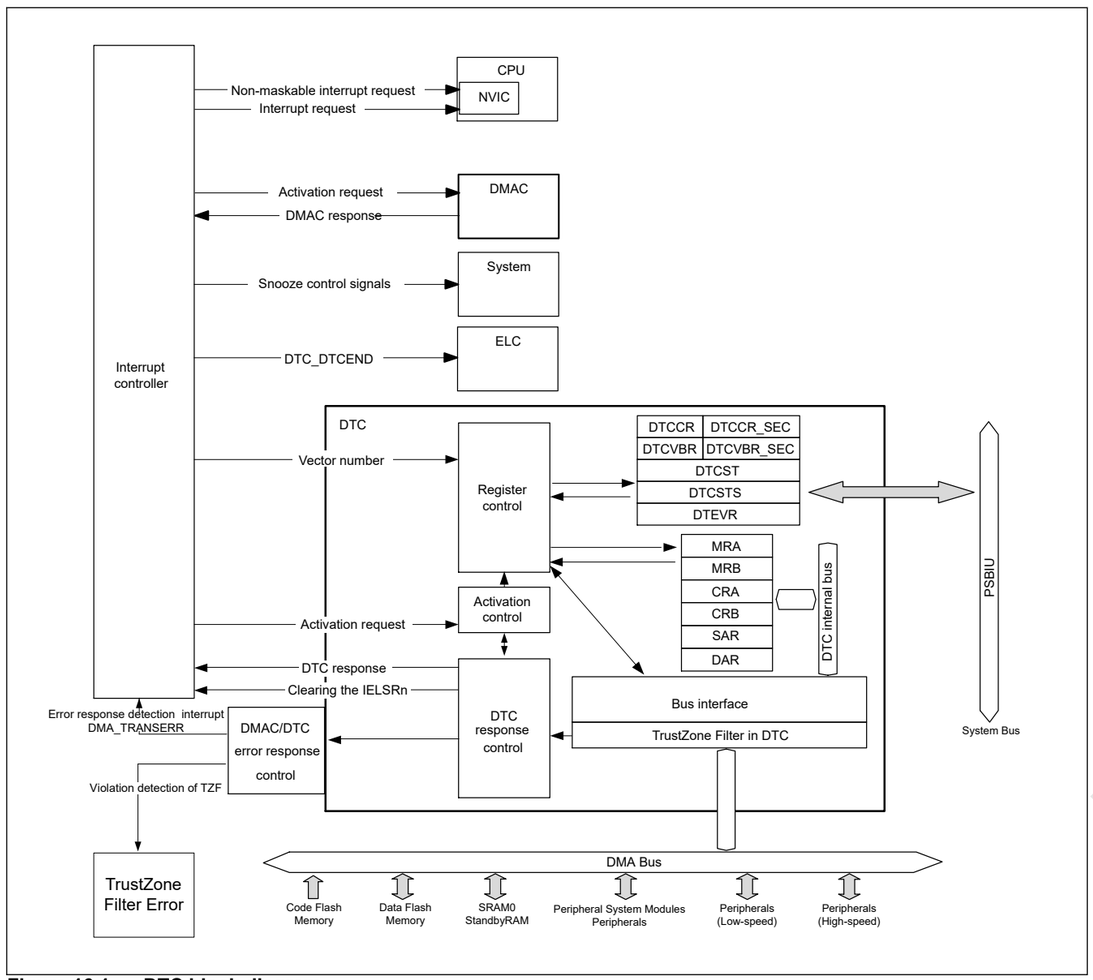


Figure 16.1 DTC block diagram

See section 12.1. Overview in section 12, Interrupt Controller Unit (ICU) for the connections between the DTC and NVIC in the CPU.

16.2 Register Descriptions

MRA, MRB, SAR, DAR, CRA, and CRB are all DTC internal registers that cannot be directly accessed from the CPU. Values to be set in these DTC internal registers are placed in the SRAM area as transfer information. When an activation request is generated, the DTC reads the transfer information from the SRAM area and sets it in its internal registers. After the data transfer ends, the internal register contents are written back to the SRAM area as transfer information.

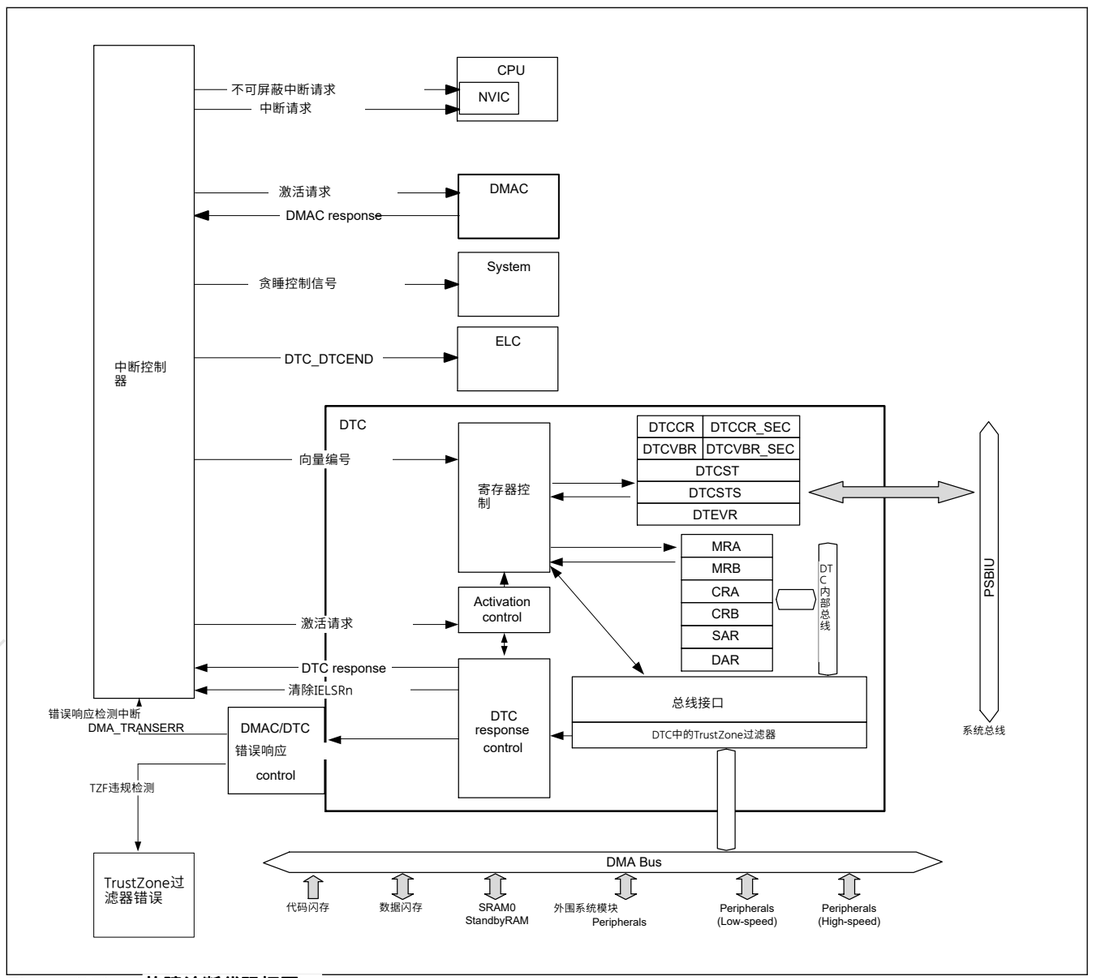


Figure 16.1 故障诊断代码框图

请参阅第12.1节。第12节，中断控制器单元(ICU)中的概述，用于CPU中DTC和NVIC之间的连接。

16.2 注册说明

MRA、MRB、SAR、DAR、CRA、CRB都是DTC内部寄存器，不能直接从CPU访问。在这些DTC内部寄存器中设置的值作为传输信息放置在SRAM区域中。当产生激活请求时，DTC从SRAM区域读取传输信息并将其设置在其内部寄存器中。数据传输结束后，内部寄存器内容作为传输信息回写到SRAM区域。

16.2.1 DTCSAR : DTC Controller Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DTCSTSA
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	DTCSTSA	DTC Security Attribution 0: Secure. 1: Non-Secure.	R/W
31:1	—	This bit is read as 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

This register only sets the DTCST security attribute.

DTCSTSA bit (DTC Security Attribution)

Security attributes of registers for DTCST.

Do not write to the DTCSTSA bit while DTC transfer is enabled or a bus master is writing to the DTC registers.

16.2.2 MRA : DTC Mode Register A

Base address: DTCVBR

Offset address: 0x03 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 16.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	—	The read values are undefined. The write value should be 0.	—
3:2	SM[1:0]	Transfer Source Address Addressing Mode 0 0: Address in the SAR register is fixed (write-back to SAR is skipped.) 0 1: Address in the SAR register is fixed (write-back to SAR is skipped.) 1 0: SAR value is incremented after data transfer: +1 when SZ[1:0] = 00b +2 when SZ[1:0] = 01b +4 when SZ[1:0] = 10b 1 1: SAR value is decremented after data transfer: -1 when SZ[1:0] = 00b -2 when SZ[1:0] = 01b -4 when SZ[1:0] = 10b	—

16.2.1 DTCSAR：DTC控制器安全属性寄存器

Base address: CPSCU = 0x4000_8000

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DTCSTSA
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	DTCSTSA	DTC安全归因 0: Secure. 1: Non-Secure.	R/W
31:1	—	该位读为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

该寄存器仅设置DTCST安全属性。

DTCSTSA位（DTC安全属性）

DTCST寄存器的安全属性。

当DTC传输启用或总线主机正在写入DTC寄存器时，请勿写入DTCSTSA位。

16.2.2 MRA:DTC模式寄存器A

Base address: DTCVBR

Offset address: 0x03+0x4×向量编号（无法直接从CPU访问。请参阅第16.3.1节。分配传输信息和DTC向量表）

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	—	读取的值未定义。写入值应为0。	—
3:2	SM[1:0]	传输源地址寻址方式 00：固定SAR寄存器中的地址（跳过对SAR的回写。）01：固定SAR寄存器中的地址（跳过对SAR的回写。）10：数据传输后SAR值递增:+1当SZ[1:0]=00b时+2当SZ[1:0]=01b时+4当SZ[1:0]=10b时 11：数据传输后SAR值递减：-1当SZ[1:0]=00b-2当SZ[1:0]=01b-4当SZ[1:0]=10b	—

Bit	Symbol	Function	R/W
5:4	SZ[1:0]	DTC Data Transfer Size 0 0: Byte (8-bit) transfer 0 1: Halfword (16-bit) transfer 1 0: Word (32-bit) transfer 1 1: Setting prohibited	—
7:6	MD[1:0]	DTC Transfer Mode Select 0 0: Normal transfer mode 0 1: Repeat transfer mode 1 0: Block transfer mode 1 1: Setting prohibited	—

The MRA register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 0x03) and DTC transfers it automatically to and from the MRA register. See section 16.3.1. Allocating Transfer Information and DTC Vector Table.

16.2.3 MRB : DTC Mode Register B

Base address: DTCVBR

Offset address: 0x02 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 16.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	—	The read values are undefined. The write value should be 0.	—
3:2	DM[1:0]	Transfer Destination Address Addressing Mode 0 0: Address in the DAR register is fixed (write-back to DAR is skipped) 0 1: Address in the DAR register is fixed (write-back to DAR is skipped) 1 0: DAR value is incremented after data transfer: +1 when MRA.SZ[1:0] = 00b +2 when SZ[1:0] = 01b +4 when SZ[1:0] = 10b 1 1: DAR value is decremented after data transfer: -1 when MRA.SZ[1:0] = 00b -2 when SZ[1:0] = 01b -4 when SZ[1:0] = 10b	—
4	DTS	DTC Transfer Mode Select 0: Select transfer destination as repeat or block area 1: Select transfer source as repeat or block area	—
5	DISEL	DTC Interrupt Select 0: Generate an interrupt request to the CPU when specified data transfer is complete 1: Generate an interrupt request to the CPU each time DTC data transfer is performed	—
6	CHNS	DTC Chain Transfer Select 0: Chain transfer is continuous 1: Chain transfer occurs only when the transfer counter changes from 1 to 0 or 1 to CRAH	—
7	CHNE	DTC Chain Transfer Enable 0: Chain transfer is disabled 1: Chain transfer is enabled	—

The MRB register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 0x02) and DTC transfers it automatically to and from the MRB register. See section 16.3.1. Allocating Transfer Information and DTC Vector Table.

Bit	Symbol	Function	R/W
5:4	SZ[1:0]	DTC数据传输大小 00：字节（8位）传送01：半字（16位）传送10：字（32位）传送11：禁止设置	—
7:6	MD[1:0]	DTC传输模式选择 00：正常传输模式01：重复传输模式10：块传输模式11：禁止设置	—

MRA寄存器不能直接从CPU访问，但是CPU可以访问SRAM区域（传输信息(n)起始地址+0x03）并且DTC会自动将其传输到MRA寄存器或从MRA寄存器传输。请参阅第16.3.1节。分配传输信息和DTC向量表。

16.2.3 MRB:DTC模式寄存器B

Base address: DTCVBR

Offset address: 0x02+0x4×向量编号（无法直接从CPU访问。请参阅第16.3.1节。分配传输信息和DTC向量表）

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	—	读取的值未定义。写入值应为0。	—
3:2	DM[1:0]	传输目标地址寻址模式 00：DAR寄存器中的地址固定（跳过DAR的回写）01：DAR寄存器中的地址固定（跳过DAR的回写）10：数据传输后DAR值递增：+1当MRA.SZ[1:0]=00b+2当SZ[1:0]=01b+4当SZ[1:0]=10b 11：数据传输后DAR值递减：-1当MRA.SZ[1:0]=00b-2当SZ[1:0]=01b-4当SZ[1:0]=10b	—
4	DTS	DTC传输模式选择 0：选择传输目标为重复区域或块区域1：选择传输源为重复区域或块区域	—
5	DISEL	DTC中断选择 0：指定数据传输完成时向CPU产生中断请求1：每次执行DTC数据传输时向CPU产生中断请求	—
6	CHNS	DTC链转移选择 0：链转移连续1：链转移仅在转移计数器从1变为0或1变为CRAH时发生	—
7	CHNE	DTC链转移启用 0：禁止链式传输1：启动链式传输	—

MRB寄存器不能直接从CPU访问，但是CPU可以访问SRAM区域（传输信息(n)起始地址+0x02）并且DTC自动将其传输到MRB寄存器和从MRB寄存器传输。请参阅第16.3.1节。分配传输信息和DTC向量表。

DM[1:0] bits (Transfer Destination Address Addressing Mode)

The DM[1:0] bits is to fix the address of the DAR register or specify increment / decrement of the DAR register after transfer.

DTS bit (DTC Transfer Mode Select)

The DTS bit specifies whether the transfer source or destination is the repeat or block area in repeat or block transfer mode.

DISEL bit (DTC Interrupt Select)

The DISEL bit specifies the condition for generating an interrupt request to the CPU.

CHNS bit (DTC Chain Transfer Select)

The CHNS bit selects the chain transfer condition. When CHNE is 0, the CHNS setting is ignored. For details on the conditions for chain transfer, see Table 16.3.

When the next transfer is chain transfer, completion of the specified number of transfers is not determined, the activation source flag is not cleared, and an interrupt request to the CPU is not generated.

CHNE bit (DTC Chain Transfer Enable)

The CHNE bit enables chain transfer. The chain transfer condition is selected by the CHNS bit. For details on chain transfer, see section 16.4.6. Chain Transfer.

16.2.4 SAR : DTC Transfer Source Register

Base address: DTCVBR

Offset address: 0x04 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 16.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	31																												0
Bit field:																													
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The SAR sets the transfer source start address and cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x04) and DTC transfers it automatically to and from the SAR register. See section 16.3.1. Allocating Transfer Information and DTC Vector Table.

Misalignment is prohibited for DTC transfers. Bit[0] must be 0 when MRA.SZ[1:0] = 01b, and bit[1] and bit[0] must be 0 when MRA.SZ[1:0] = 10b.

16.2.5 DAR : DTC Transfer Destination Register

Base address: DTCVBR

Offset address: 0x08 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 16.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	31																												0
Bit field:																													
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The DAR sets the transfer destination start address and cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x08) and DTC transfers it automatically to and from the DAR register. See section 16.3.1. Allocating Transfer Information and DTC Vector Table.

Misalignment is prohibited for DTC transfers. Bit[0] must be 0 when MRA.SZ[1:0] = 01b, and bit[1] and bit[0] must be 0 when MRA.SZ[1:0] = 10b.

DM[1:0]位（传输目标地址寻址模式）

DM[1:0]位用于固定DAR寄存器的地址或指定DAR寄存器在传输后递增递减。

DTS位（DTC传输模式选择）

DTS位指定传输源或目标是否是重复或块传输模式下的重复或块区域。

DISEL位（DTC中断选择）

DISEL位指定向CPU产生中断请求的条件。

CHNS位（DTC链传输选择）

CHNS位选择链传输条件。当CHNE为0时，忽略CHNS设置。链转移条件详见表16.3。

下一次传输为链式传输时，指定的传输次数未确定，激活源标志未清零，也不向CPU发出中断请求。

CHNE位（DTC链传输使能）

CHNE位启用链式传输。链传输条件由CHNS位选择。有关链式转移的详细信息，请参见第16.4.6节。链转移。

16.2.4 SAR：DTC传输源寄存器

Base address: DTCVBR

Offset address: 0x04+0x4×向量编号（无法直接从CPU访问。请参阅第16.3.1节。分配传输信息和DTC向量表）

Bit position:	31																												0
Bit field:																													
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

SAR设置传输源起始地址，不能直接从CPU访问。但是，CPU可以访问SRAM区域（传输信息(n)起始地址+0x04），并且DTC会自动将其传输到SAR寄存器或从SAR寄存器传输。请参阅第16.3.1节。分配传输信息和DTC向量表。

DTC传输禁止错位。当MRA.SZ[1:0]=01b时Bit[0]必须为0，当MRA.SZ[1:0]=10b时bit[1]和bit[0]必须为0。

16.2.5 DAR:DTC传输目的地寄存器

Base address: DTCVBR

Offset address: 0x08+0x4×向量编号（无法直接从CPU访问。请参阅第16.3.1节。分配传输信息和DTC向量表）

Bit position:	31																												0
Bit field:																													
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

DAR设置传输目标起始地址，不能直接从CPU访问。但是，CPU可以访问SRAM区域（传输信息(n)起始地址+0x08）并且DTC会自动将其传输到DAR寄存器或从DAR寄存器传输。请参阅第16.3.1节。分配传输信息和DTC向量表。

DTC传输禁止错位。当MRA.SZ[1:0]=01b时Bit[0]必须为0，当MRA.SZ[1:0]=10b时bit[1]和bit[0]必须为0。

16.2.6 CRA : DTC Transfer Count Register A

Base address: DTCVBR

Offset address: 0x0E + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 16.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	CRAL	Transfer Counter A Lower Register Specify the transfer count.	—
15:8	CRAH	Transfer Counter A Upper Register Specify the transfer count.	—

Note: The function depends on the transfer mode.
Note: Set CRAH and CRAL to the same value in repeat transfer mode and block transfer mode.

The CRA register consists of 16 bits. CRAL is the lower 8 bits and CRAH is the upper 8 bits. CRA is used in normal mode.

CRAL and CRAH are used in repeat transfer mode and block transfer mode.

The CRA register cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x0E) and DTC transfers it automatically to and from the CRA register. See section 16.3.1. Allocating Transfer Information and DTC Vector Table.

(1) Normal transfer mode (MRA.MD[1:0] = 00b)

In normal transfer mode, CRA functions as a 16-bit transfer counter. The transfer count is 1, 65535, and 65536 when the set value is 0x0001, 0xFFFF, and 0x0000, respectively. The CRA value is decremented (-1) on each data transfer.

(2) Repeat transfer mode (MRA.MD[1:0] = 01b)

In repeat transfer mode, the CRAH register holds the transfer count and the CRAL register functions as an 8-bit transfer counter. The transfer count is 1, 255, and 256 when the set value is 0x01, 0xFF, and 0x00, respectively. The CRAL value is decremented (-1) on each data transfer. When it reaches 0x00, the CRAH value is transferred to CRAL.

(3) Block transfer mode (MRA.MD[1:0] = 10b)

In block transfer mode, the CRAH register holds the block size and the CRAL register functions as an 8-bit block size counter. The transfer count is 1, 255, and 256 when the set value is 0x01, 0xFF, and 0x00, respectively. The CRAL value is decremented (-1) on each data transfer. When it reaches 0x00, the CRAH value is transferred to CRAL.

16.2.7 CRB : DTC Transfer Count Register B

Base address: DTCVBR

Offset address: 0x0C + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 16.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The CRB sets the block transfer count for block transfer mode. The transfer count is 1, 65535, and 65536 when the set value is 0x0001, 0xFFFF, and 0x0000, respectively. The CRB value is decremented (-1) when the final data of a single block size is transferred. When normal transfer mode or repeat transfer mode is selected, this register is not used and the set value is ignored.

16.2.6 CRA:DTC传输计数寄存器A

Base address: DTCVBR

Offset address: 0x0E+0x4×向量编号（无法直接从CPU访问。请参阅第16.3.1节。分配传输信息和DTC向量表）

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	CRAL	传送计数器A低位寄存器 指定传输计数。	—
15:8	CRAH	传送计数器A高位寄存器 指定传输计数。	—

Note: 该功能取决于传输模式。
Note: 在重复传输模式和块传输模式下，将CRAH和CRAL设置为相同的值。

CRA寄存器由16位组成。CRAL是低8位，CRAH是高8位。CRA在正常模式下使用。

CRAL和CRAH用于重复传输模式和块传输模式。

CRA寄存器不能直接从CPU访问。但是，CPU可以访问SRAM区域（传输信息(n)起始地址+0x0E），DTC会自动将其传输到CRA寄存器或从CRA寄存器传输。请参阅第16.3.1节。分配传输信息和DTC向量表。

(1) 正常传输模式（MRA.MD[1:0]=00b）

在正常传输模式下，CRA用作16位传输计数器。当设置值为0x0001、0xFFFF和0x0000时，传输计数分别为1、65535和65536。CRA值在每次数据传输时递减(-1)。

(2) 重复传输模式(MRA.MD[1:0]=01b)

在重复传输模式下，CRAH寄存器保存传输计数，CRAL寄存器用作8位传输计数器。当设置值为0x01、0xFF和0x00时，传输计数分别为1、255和256。CRAL值在每次数据传输时递减(-1)。当它达到0x00时，CRAH值被传送到CRAL。

(3) 块传输模式（MRA.MD[1:0]=10b）

在块传输模式下，CRAH寄存器保存块大小，CRAL寄存器用作8位块大小计数器。当设置值为0x01、0xFF和0x00时，传输计数分别为1、255和256。CRAL值在每次数据传输时递减(-1)。当它达到0x00时，CRAH值被传送到CRAL。

16.2.7 CRB:DTC传输计数寄存器B

Base address: DTCVBR

Offset address: 0x0C+0x4×向量编号（无法直接从CPU访问。请参阅第16.3.1节。分配传输信息和DTC向量表）

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

CRB设置块传输模式的块传输计数。当设置值为0x0001、0xFFFF和0x0000时，传输计数分别为1、65535和65536。当传输单个块大小的最终数据时，CRB值递减(-1)。Whennormaltransfermodeorrepeattransfermodeisselected thisregisterisnotusedandthesetvalueisignored.

The CRB cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x0C) and DTC transfers it automatically to and from the CRB register. See section 16.3.1. Allocating Transfer Information and DTC Vector Table.

16.2.8 DTCCR : DTC Control Register

Base address: DTC = 0x4000_5400

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RRS	—	—	—	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
3	—	This bit is read as 1. The write value should be 1.	R/W
4	RRS	DTC Transfer Information Read Skip Enable 0: Transfer information read is not skipped 1: Transfer information read is skipped when vector numbers match	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

RRS bit (DTC Transfer Information Read Skip Enable)

The RRS bit enables skipping of transfer information reads when vector numbers match. The DTC vector number is compared with the vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, DTC data transfer is performed without reading the transfer information. However, when the previous transfer is a chain transfer, the transfer information is read regardless of the RRS bit.

When the transfer counter (CRA register) becomes 0 during the previous normal transfer and when the transfer counter (CRB register) becomes 0 during the previous block transfer, the transfer information is read regardless of the RRS bit value.

16.2.9 DTCCR_SEC : DTC Control Register for secure Region

Base address: DTC = 0x4000_5400

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RRS	—	—	—	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
3	—	This bit is read as 1. The write value should be 1.	R/W
4	RRS	DTC Transfer Information Read Skip Enable for Secure 0: Transfer information read is not skipped. 1: Transfer information read is skipped when vector numbers match.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: Secure access is allowed. Non-secure access is read-only.

RRS bit (DTC Transfer Information Read Skip Enable for Secure)

The RRS bit enables skipping of transfer information reads when vector numbers match. The DTC vector number is compared with the vector number in the previous activation process. When these vector numbers match and the RRS bit is

不能直接从CPU访问CRB。但是，CPU可以访问SRAM区域（传输信息(n)起始地址+0x0C），并且DTC会自动将其传输到CRB寄存器或从CRB寄存器传输。请参阅第16.3.1节。分配传输信息和DTC向量表。

16.2.8 DTCCR:DTC控制寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RRS	—	—	—	—
重置后的值：	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	这些位被读取为0。写入值应为0。	R/W
3	—	该位读取为1。写入值应为1。	R/W
4	RRS	DTC传输信息读取跳过启用 0：不跳过传输信息读取1：当向量编号匹配时，跳过传输信息读取	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

RRS位（DTC传输信息读取跳过使能）

当向量编号匹配时，RRS位允许跳过传输信息读取。将DTC向量编号与之前激活过程中的向量编号进行比较。当这些向量编号匹配并且RRS位设置为1时，执行DTC数据传输而不读取传输信息。但是，当前一次传输是链式传输时，无论RRS位如何，都会读取传输信息。

如果在前一次正常传输期间传输计数器（CRA寄存器）变为0，并且在前一次块传输期间传输计数器（CRB寄存器）变为0，则无论RRS位值如何，都将读取传输信息。

16.2.9 DTCCR_SEC：安全区域的DTC控制寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RRS	—	—	—	—
重置后的值：	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	这些位被读取为0。写入值应为0。	R/W
3	—	该位读取为1。写入值应为1。	R/W
4	RRS	DTC传输信息读取跳过启用安全 0：不跳过读取的传输信息。1：当向量号匹配时跳过传输信息读取。	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 允许安全访问。非安全访问是只读的。

RRS位（用于安全的DTC传输信息读取跳过启用）

当向量编号匹配时，RRS位允许跳过传输信息读取。将DTC向量编号与之前激活过程中的向量编号进行比较。当这些向量编号匹配且RRS位为

set to 1, DTC data transfer is performed without reading the transfer information. However, when the previous transfer is a chain transfer, the transfer information is read regardless of the RRS bit.

When the transfer counter (CRA register) becomes 0 during the previous normal transfer and when the transfer counter (CRB register) becomes 0 during the previous block transfer, the transfer information is read regardless of the RRS bit value.

16.2.10 DTCVBR : DTC Vector Base Register

Base address: DTC = 0x4000_5400

Offset address: 0x04

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	DTC Vector Base Address Set the DTC vector base address. The lower 10 bits should be 0.	R/W

The DTCVBR sets the base address for calculating the DTC vector table address, which can be set in the range of 0x0000_0000 to 0xFFFF_FFFF (4 GB) in 1-KB units.

16.2.11 DTCVBR_SEC : DTC Vector Base Register for secure Region

Base address: DTC = 0x4000_5400

Offset address: 0x14

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	DTC Vector Base Address for secure region Set DTC Vector Base Address for secure region. The lower 10 bits should be 0.	R/W

Note: Secure access is allowed. Non-secure access is read-only.

The DTCVBR_SEC sets the base address for calculating the DTC vector table address, which can be set in the range of 0x0000_0000 to 0xFFFF_FFFF (4 GB) in 1-KB units.

16.2.12 DTCST : DTC Module Start Register

Base address: DTC = 0x4000_5400

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DTCST	DTC Module Start 0: DTC module stopped 1: DTC module started	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

设置为1，执行DTC数据传输而不读取传输信息。但是，当前一次传输是链式传输时，无论RRS位如何，都会读取传输信息。

如果在前一次正常传输期间传输计数器（CRA寄存器）变为0，并且在前一次块传输期间传输计数器（CRB寄存器）变为0，则无论RRS位值如何，都将读取传输信息。

16.2.10 DTCVBR:DTC向量基址寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x04

Bit position:	31																													0
Bit field:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	DTC向量基地址 设置DTC向量基地址。低10位应为0。	R/W

DTCVBR设置计算DTC向量表地址的基地址，可以设置在0x0000_0000到0xFFFF_FFFF(4GB)的范围内，以1KB为单位。

16.2.11 DTCVBR_SEC：安全区域的DTC向量基址寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x14

Bit position:	31																													0
Bit field:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	安全区域的DTC向量基地址 为安全区域设置DTC向量基地址。低10位应为0。	R/W

Note: 允许安全访问。非安全访问是只读的。

DTCVBR_SEC设置计算DTC向量表地址的基地址，可以设置在0x0000_0000到0xFFFF_FFFF(4GB)的范围内，以1-KB为单位。

16.2.12 DTCST:DTC模块启动寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTCST
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DTCST	DTC模块启动 0：DTC模块停止1：DTC模块启动	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

DTCST bit (DTC Module Start)

Set the DTCST bit to 1 to enable the DTC to accept transfer requests. When this bit is set to 0, transfer requests are no longer accepted. If this bit is set to 0 during a data transfer, the accepted transfer request is active until processing completes.

DTCST must be set to 0 before transitioning to one of the following state or mode:

- Module-stop state
- Software Standby mode without Snooze mode transition
- Deep Software standby mode

For details on these transitions, see section 16.10. Low Power Consumption Function and section 10, Low Power Modes.

16.2.13 DTCSTS : DTC Status Register

Base address: DTC = 0x4000_5400

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ACT	—	—	—	—	—	—	—	VECN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	VECN[7:0]	DTC-Activating Vector Number Monitoring These bits indicate the vector number for the activation source when a DTC transfer is in progress. The value is only valid if a DTC transfer is in progress (ACT flag is 1).	R
14:8	—	These bits are read as 0.	R
15	ACT	DTC Active Flag 0: DTC transfer operation is not in progress 1: DTC transfer operation is in progress	R

VECN[7:0] bits (DTC-Activating Vector Number Monitoring)

While transfer by the DTC is in progress, the VECN[7:0] bits indicate the vector number associated with the activation source for the transfer. The value read from the VECN[7:0] bits is valid if the ACT flag is 1, indicating a DTC transfer in progress, and invalid if the ACT flag is 0, indicating no DTC transfer is in progress.

ACT flag (DTC Active Flag)

The ACT flag indicates the state of the DTC transfer operation.

[Setting condition]

- When the DTC is activated by a transfer request.

[Clearing condition]

- When transfer by the DTC, in response to a transfer request, is complete.

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

DTCST位（DTC模块启动）

将DTCST位设置为1以使DTC接受传输请求。当该位设置为0时，不再接受传输请求。如果在数据传输期间该位设置为0，则接受的传输请求将处于活动状态，直到处理完成。

在转换到以下状态或模式之一之前，必须将DTCST设置为0：

- Module-stop state
- ●没有贪睡模式转换的软件待机模式
- ●深度软件待机模式

有关这些转换的详细信息，请参阅第16.10节。低功耗功能和第10节，低功耗模式。

16.2.13 DTCSTS:DTC状态寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ACT	—	—	—	—	—	—	—	VECN[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	VECN[7:0]	DTC-激活向量数量监测 当DTC传输正在进行时，这些位指示激活源的向量编号。该值仅在DTC传输正在进行（ACT标志为1）时有效。	R
14:8	—	这些位读为0。	R
15	ACT	DTC活动标志 0：未进行DTC传输操作1：正在进行DTC传输操作	R

VECN[7:0]位（DTC-激活向量编号监控）

当DTC进行传输时，VECN[7:0]位指示与传输激活源相关的向量编号。如果ACT标志为1，则从VECN[7:0]位读取的值有效，表示正在进行DTC传输，如果ACT标志为0，则表示无效，表示没有DTC传输正在进行。

ACT标志（DTC活动标志）

ACT标志指示DTC传输操作的状态。

[Setting condition]

●当DTC被传输请求激活时。

[Clearing condition]

●当DTC传输完成时，响应传输请求。

16.2.14 DTEVR : DTC Error Vector Register

Base address: DTC = 0x4000_5400

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DTESTA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTEVSAM	DTEV[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DTEV[7:0]	DTC Error Vector Number These bits represent error vector of the DTC.	R
8	DTEVSAM	DTC Error Vector Number SA Monitor Indicates the SA of vector number causing the error. 0: Secure vector number 1: Non-Secure vector number	R
15:9	—	These bits are read as 0. The write value should be 0.	R
16	DTESTA	DTC Error Status Flag 0: No DTC transfer error occurred 1: DTC transfer error occurred	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R

Note: Writing to DTESTA depends on the value of DTEVSAM

DTEV[7:0] bit (DTC Error Vector Number)

When a transfer error due to DTC transfer occurs, it stores the channel of DTC that was violated.

When reset was selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, Since this register is also reset. Please select NMI when you want to debug the program.

[Set condition]

- When the DTC transfer error occurs and DTESTA = 0.

[Clearing condition]

- When 1 is written to DTEVR.DTESTA.

DTEVSAM bit (DTC Error Vector Number SA Monitor)

When a transfer error due to DTC transfer occurs, it indicates the SA of the violating DTC vector number.

When reset was selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, Since this register is also reset. Please select NMI when you want to debug the program.

[Set condition]

- When the DTC transfer error occurs and DTESTA = 0.

[Clearing condition].

- When 1 is written to DTEVR.DTESTA.

DTESTA bit (DTC Error Status Flag)

Indicates whether or not a DTC transfer error occurred.

DTEV, DTEVSAM, DTESTA are cleared by writing 1 to DTESTA.

Writing 0 to DTESTA is ignored.

16.2.14 DTEVR:DTC错误向量寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DTESTA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTEVSAM	DTEV[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DTEV[7:0]	DTC错误向量编号 这些位代表DTC的误差向量。	R
8	DTEVSAM	DTC错误向量编号SA监视器 指示导致错误的向量号的SA。 0：安全向量编号1：非安全向量编号	R
15:9	—	这些位被读取为0。写入值应为0。	R
16	DTESTA	DTC错误状态标志 0：未发生DTC传输错误1：发生DTC传输错误	R/W
31:17	—	这些位被读取为0。写入值应为0。	R

Note: 写入DTESTA取决于DTEVSAM的值

DTEV[7:0]位（DTC错误向量编号）

当由于DTC传输而发生传输错误时，它会存储违反的DTC通道。

当在MPU.MMPUOAD.OAD和TZF.TZFOAD.OAD中选择了复位时，由于该寄存器也被复位。请选择NMI当你想调试程序时。

[Set condition]

●发生DTC传输错误且DTESTA=0时。

[Clearing condition]

●当1写入DTEVR.DTESTA时。

DTEVSAM位（DTC错误向量编号SA监视器）

当由于DTC传输而发生传输错误时，它指示违规DTC向量号的SA。

当在MPU.MMPUOAD.OAD和TZF.TZFOAD.OAD中选择了复位时，由于该寄存器也被复位。请选择NMI当你想调试程序时。

[Set condition]

●发生DTC传输错误且DTESTA=0时。

[Clearing condition].

●当1写入DTEVR.DTESTA时。

DTESTA位（DTC错误状态标志）

指示是否发生DTC传输错误。

DTEV、DTEVSAM、DTESTA通过向DTESTA写入1清零。

将0写入DTESTA将被忽略。

When reset was selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, Since this register is also reset. Please select NMI when you want to debug the program.

[Set condition]

- When the DMAC transfer error occurs.

[Clearing condition]

- When 1 is written to DTEVR.DTESTA.

Note: When DTEVSAM = 1, it can be cleared in the secure state and non-secure state. DTEVSAM = 0, it cannot be cleared in the non-secure state.

16.3 Activation Sources

The DTC is activated by an interrupt request. Setting the ICU.IELSRn.DTCE bit to 1 enables activation of the DTC by the associated interrupt. The selector output *n* number set in ICU.IELSRn is defined as the interrupt vector number, where n = 0 to 95. For an enabled interrupt, the specific DTC interrupt source associated with each interrupt vector number *n* is selected in ICU.IELSRn.IELS[8:0] where n = 0 to 95, as listed in section 12.3.2. Event Number in section 12, Interrupt Controller Unit (ICU). For activation by software, see section 17.2.2. ELSEGRn : Event Link Software Event Generation Register n (n = 0, 1).

The interrupt vector number is equivalent to the DTC vector table number. After the DTC accepted an activation request, it does not accept another activation request until transfer for that single request is complete, regardless of the priority of the requests. When multiple activation requests are generated during a DTC transfer, a highest priority request is accepted on completion of the transfer. When multiple activation requests are generated while the DTC Module Start bit (DTCST.DTCST) is 0, the DTC accepts the highest priority request when DTCST.DTCST is subsequently set to 1. The smaller interrupt vector number has higher priority.

The DTC performs the following operations at the start of a single data transfer or for a chain transfer, after the last of the consecutive transfers:

- On completion of a specified round of data transfer, the ICU.IELSRn.DTCE bit is set to 0, and an interrupt request is sent to the CPU
- If the MRB.DISEL bit is 1, an interrupt request is sent to the CPU on completion of a data transfer
- For other transfers, the ICU.IELSRn.IR flag of the activation source is set to 0 at the start of the data transfer.

16.3.1 Allocating Transfer Information and DTC Vector Table

The DTC reads the start address of the transfer information associated with each activation source from the vector table and reads the transfer information starting at that address.

DTC has two vector tables, non-secure side or secure side. Because the interrupt vector number that serves as a trigger for DTC is divided into non-secure or secure. Place the vector table of the interrupt vector number of SA = 1 in DTCVBR which is the non-secure side. Place the vector table of interrupt number SA = 0 in DTCVBR_SEC which is the secure side.

The vector table must be located so that the lower 10 bits of the base address (start address) are 0. Use the DTC Vector Base Register (DTCVBR) to set the base address of the DTC vector table. Transfer information is allocated in the SRAM area. In the SRAM area, the start address of the transfer information *n* with vector number *n* must be 4n added to the base address in the vector table.

Figure 16.2 shows the relationship between the DTC vector table and transfer information. Figure 16.3 shows the allocation of transfer information in the SRAM area.

当在MPU.MMPUOAD.OAD和TZF.TZFOAD.OAD中选择了复位时，由于该寄存器也被复位。请选择NMI当你想调试程序时。

[Set condition]

●发生DMAC传输错误时。

[Clearing condition]

●当1写入DTEVR.DTESTA时。

Note: 当DTEVSAM=1时，可以在安全状态和非安全状态下清零。DTEVSAM=0，在非安全状态下不能清零。

16.3 激活源

DTC由中断请求激活。将ICU.IELSRn.DTCE位设置为1可以通过相关中断激活DTC。ICU.IELSRn中设置的选择器输出n号定义为中断向量号，其中n=0到95。对于启用的中断，在ICU.IELSRn.IELS中选择与每个中断向量号n关联的特定DTC中断源[8:0]其中n=0到95，如第12.3.2节中所列。第12节，中断控制器单元(ICU)中的事件编号。关于通过软件激活，请参见第17.2.2节。ELSEGRn：事件链接软件事件生成寄存器n(n=0 1)。

中断向量编号相当于DTC向量表编号。在DTC接受激活请求后，它不会接受另一个激活请求，直到该单个请求的传输完成，无论请求的优先级如何。如果在DTC传输期间生成多个激活请求，则在传输完成时接受最高优先级的请求。当DTC模块起始位(DTCST.DTCST)为0时产生多个激活请求时，当DTCST.DTCST随后设置为1时，DTC接受最高优先级请求。较小的中断向量编号具有较高的优先级。

DTC在单次数据传输开始时执行以下操作，或者对于链式传输，在最后一次连续传输之后执行以下操作：

●完成指定轮次的数据传输后，ICU.IELSRn.DTCE位设置为0，并向CPU发送中断请求

●如果MRB.DISEL位为1，则在数据传输完成时向CPU发送中断请求

●对于其他传输，激活源的ICU.IELSRn.IR标志在数据传输开始时设置为0。

16.3.1 分配传输信息和DTC向量表

DTC从向量表中读取与每个激活源相关联的传输信息的起始地址，并读取从该地址开始的传输信息。

DTC有两个向量表，非安全端或安全端。因为作为DTC触发的中断向量号分为非安全和安全。将SA=1的中断向量号的向量表放在非安全端DTCVBR中。将中断号SA=0的向量表放在安全侧DTCVBR_SEC中。

向量表的定位必须使基地址（起始地址）的低10位为0。使用DTC向量基址寄存器(DTCVBR)设置DTC向量表的基地址。传输信息分配在SRAM区域中。在SRAM区域中，向量编号为n的传输信息n的起始地址必须与向量表中的基地址相加4n。

图16.2显示了DTC向量表和传输信息之间的关系。图16.3显示了SRAM区域中传输信息的分配。

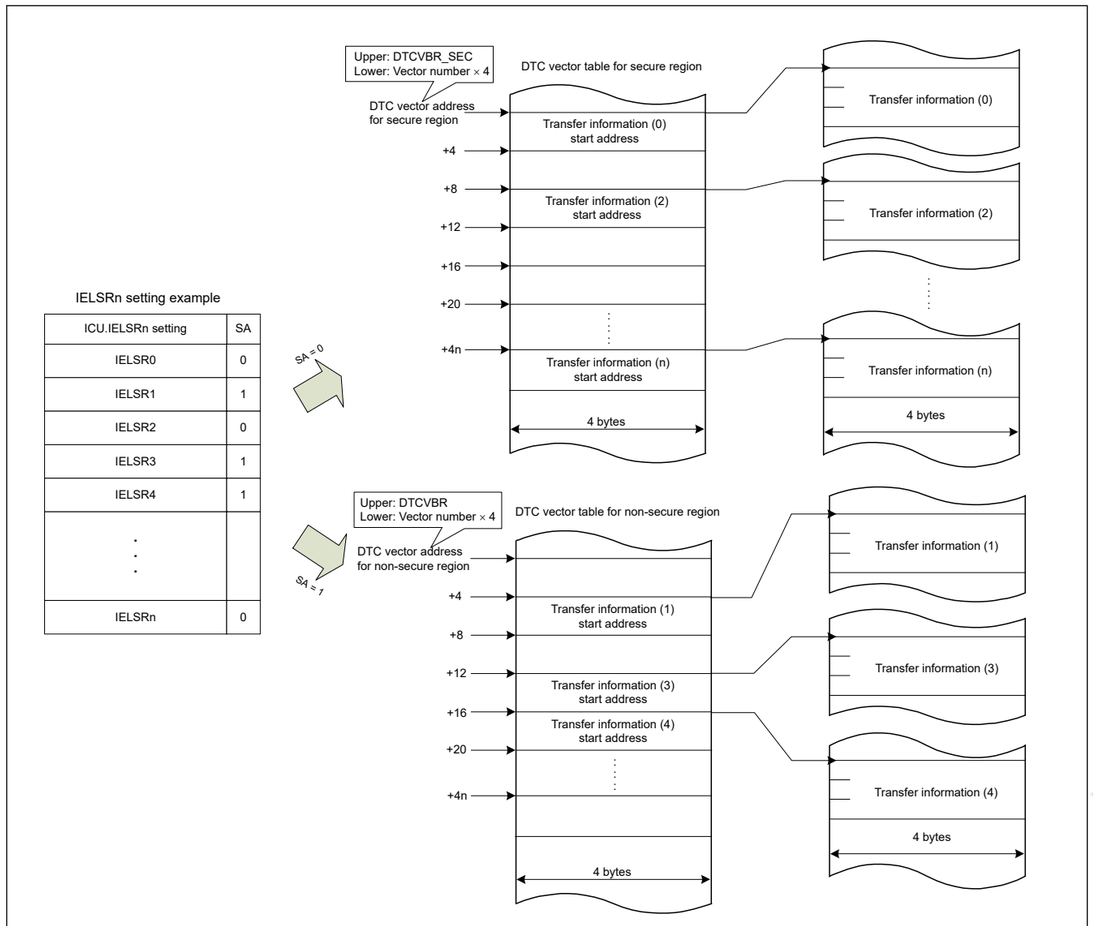


Figure 16.2 DTC vector table and transfer information

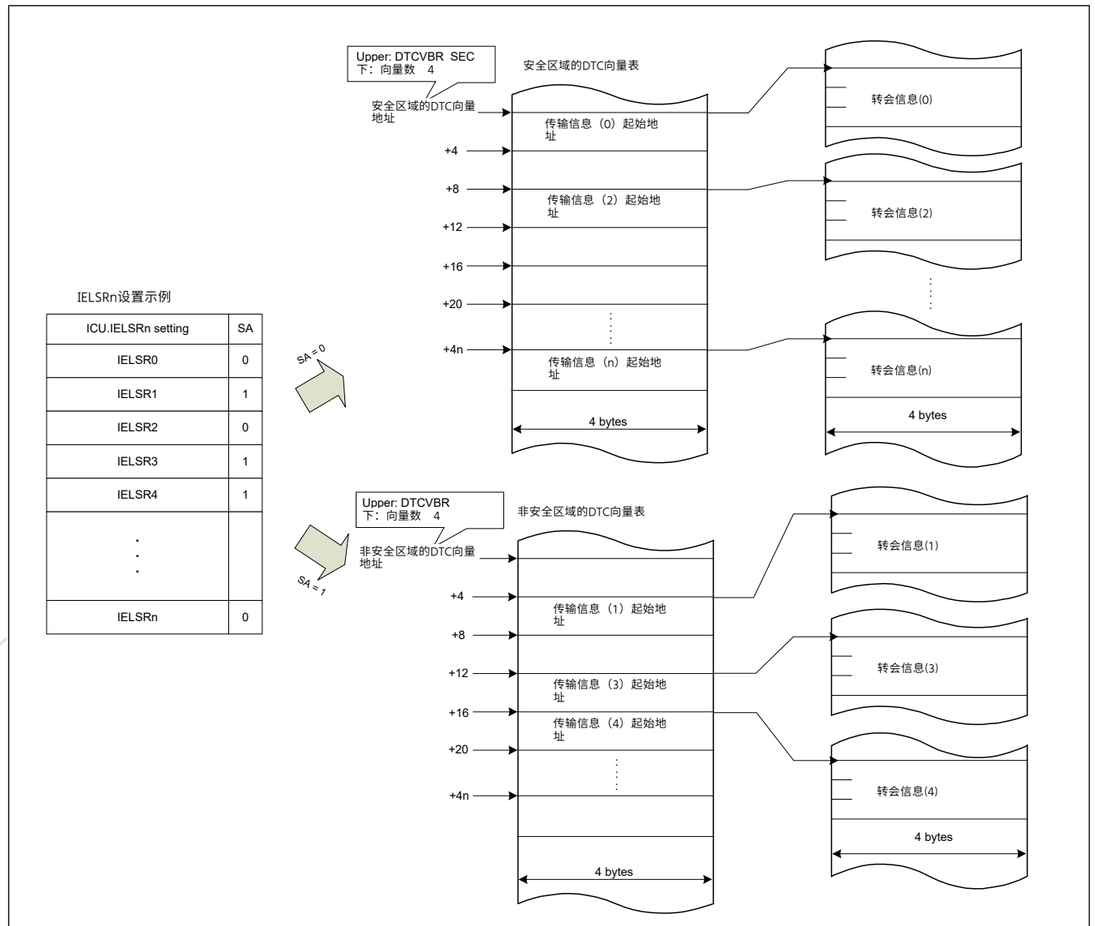


Figure 16.2 DTC向量表和传输信息

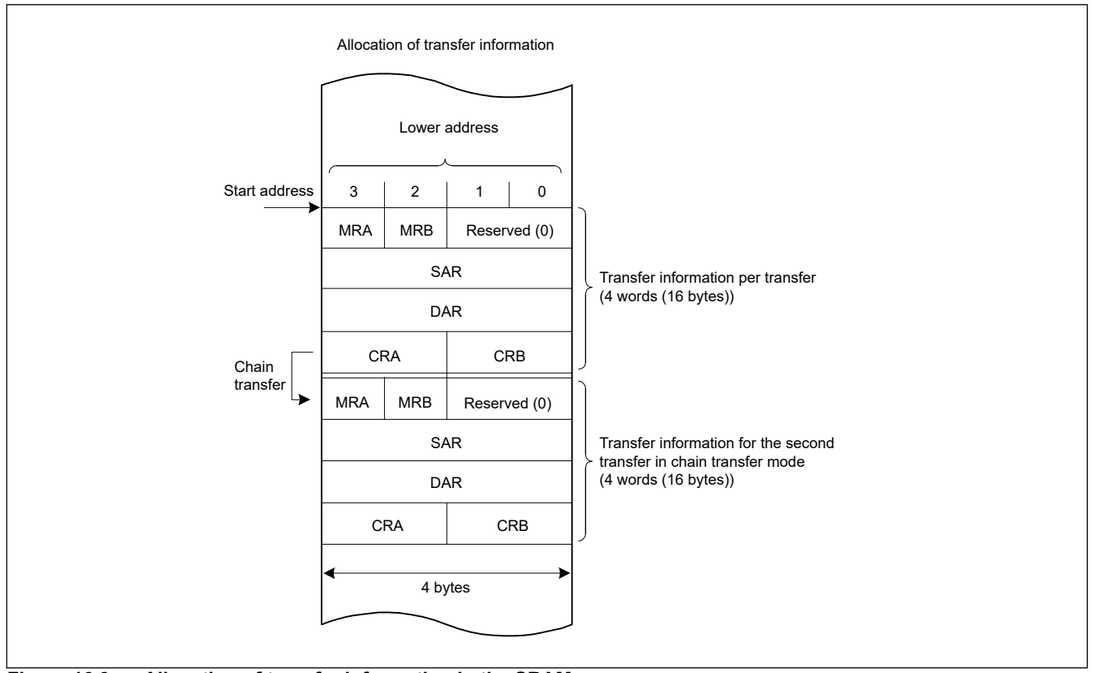


Figure 16.3 Allocation of transfer information in the SRAM area

16.4 Operation

The DTC transfers data according to the transfer information. Storage of the transfer information in the SRAM area is required before a DTC operation. When the DTC is activated, it reads the DTC vector associated with the vector number. The DTC reads the transfer information from the transfer information store address referenced by the DTC vector and transfers the data. After the data transfer, the DTC writes back the transfer information. Storing the transfer information in the SRAM area allows data transfer of any number of channels.

The transfer modes include:

- Normal transfer mode
- Repeat transfer mode
- Block transfer mode.

The DTC specifies a transfer source address in the SAR register and a transfer destination address in the DAR register. The values of these registers are incremented, decremented, or address-fixed independently after the data transfer.

Table 16.2 describes the DTC transfer modes.

Table 16.2 DTC transfer modes

Transfer mode	Data size transferred on single transfer request	Increment or decrement of memory address	Settable transfer count
Normal transfer mode	1 byte (8 bit), 1 halfword (16 bit), 1 word (32 bit)	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 65536
Repeat transfer mode*1	1 byte (8 bit), 1 halfword (16 bit), 1 word (32 bit)	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 256*3
Block transfer mode*2	Block size specified in CRAH (1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes))	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 65536

Note 1. Set the transfer source or transfer destination as the repeat area.
Note 2. Set the transfer source or transfer destination as the block area.
Note 3. After a data transfer of the specified count, the initial state is restored and operation restarts.

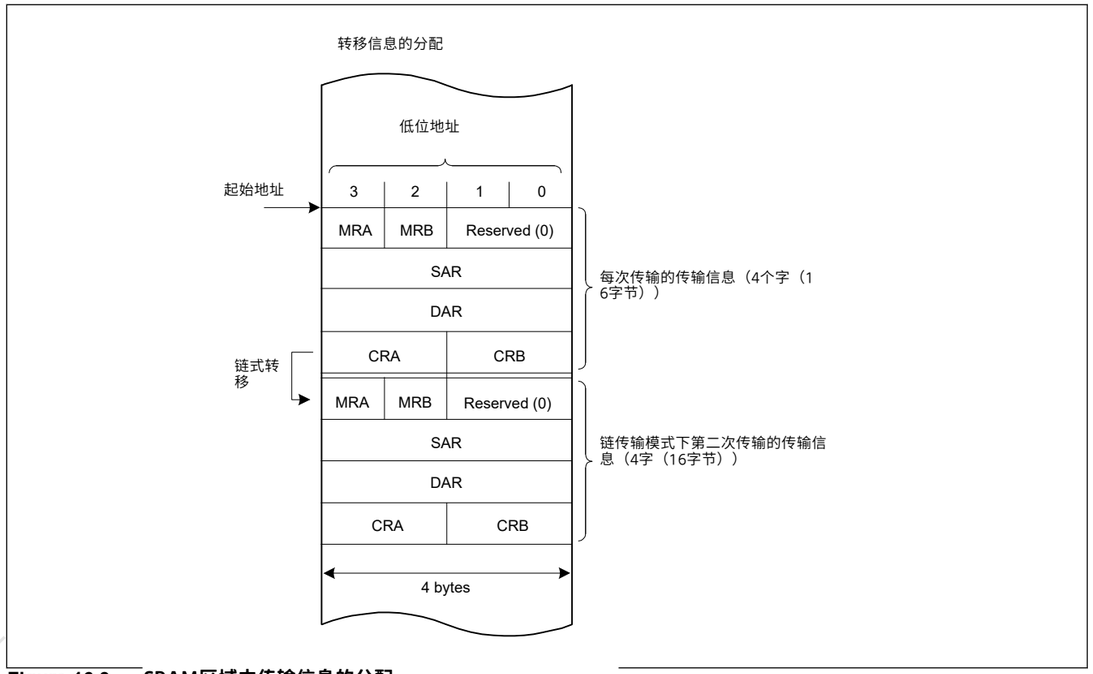


Figure 16.3 SRAM区域中传输信息的分配

16.4 Operation

DTC根据传输信息传输数据。在进行DTC操作之前，需要在SRAM区域中存储传输信息。当DTC被激活时，它会读取与向量编号相关联的DTC向量。DTC从DTC向量引用的传输信息存储地址中读取传输信息并传输数据。数据传输后，DTC写回传输信息。将传输信息存储在SRAM区域中可以实现任意数量的通道的数据传输。

传输模式包括：

- ●普通传输模式
- ●重复传输模式
- ●块传输模式。

DTC指定SAR寄存器中的传输源地址和DAR寄存器中的传输目标地址。这些寄存器的值在数据传输后独立地递增、递减或固定地址。

表16.2描述了DTC传输模式。

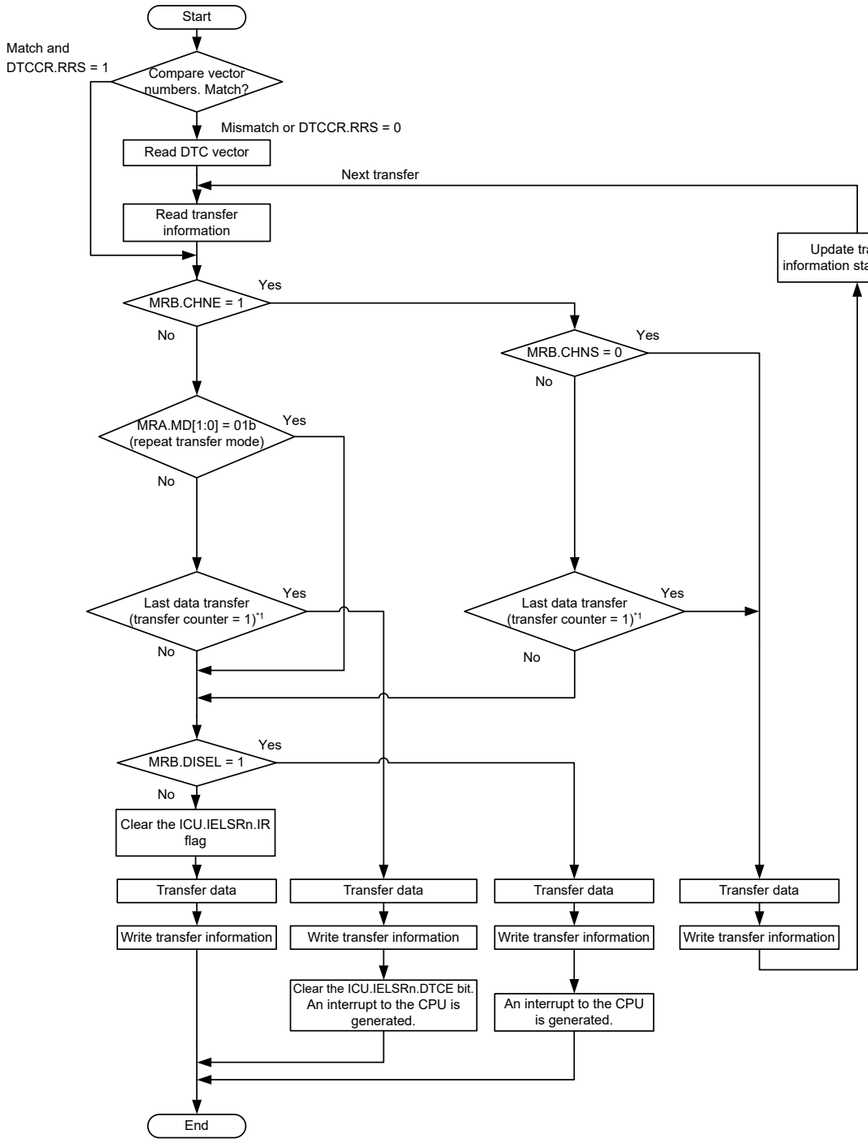
Table 16.2 DTC传输模式

传输模式	在单个传输请求上传输的数据大小	内存地址的递增或递减	可设置的传输次数
正常传输模式	1个字节（8位）、1个半字（16位）、1个字（32位）	递增或递减1、2或4或固定地址	1 to 65536
重复传输模式*1	1个字节（8位）、1个半字（16位）、1个字（32位）	递增或递减1、2或4或固定地址	1 to 256*3
块传输模式*2	CRAH中指定的块大小（1到256字节、1到256个半字（2到512字节）或1到256字（4到1024字节））	递增或递减1、2或4或固定地址	1 to 65536

注1.将传输源或传输目标设置为重复区域。注2.将传输源或传输目标设置为块区域。
注3.指定计数的数据传输后，恢复初始状态并重新开始操作。

Setting the MRB.CHNE bit to 1 allows multiple transfers or chain transfer on a single activation source. It also enables a chain transfer when the specified data transfer is complete.

Figure 16.4 shows the operation flow of the DTC. Table 16.3 lists the chain transfer conditions. The combination of control information for the second and subsequent transfers are omitted in this table.

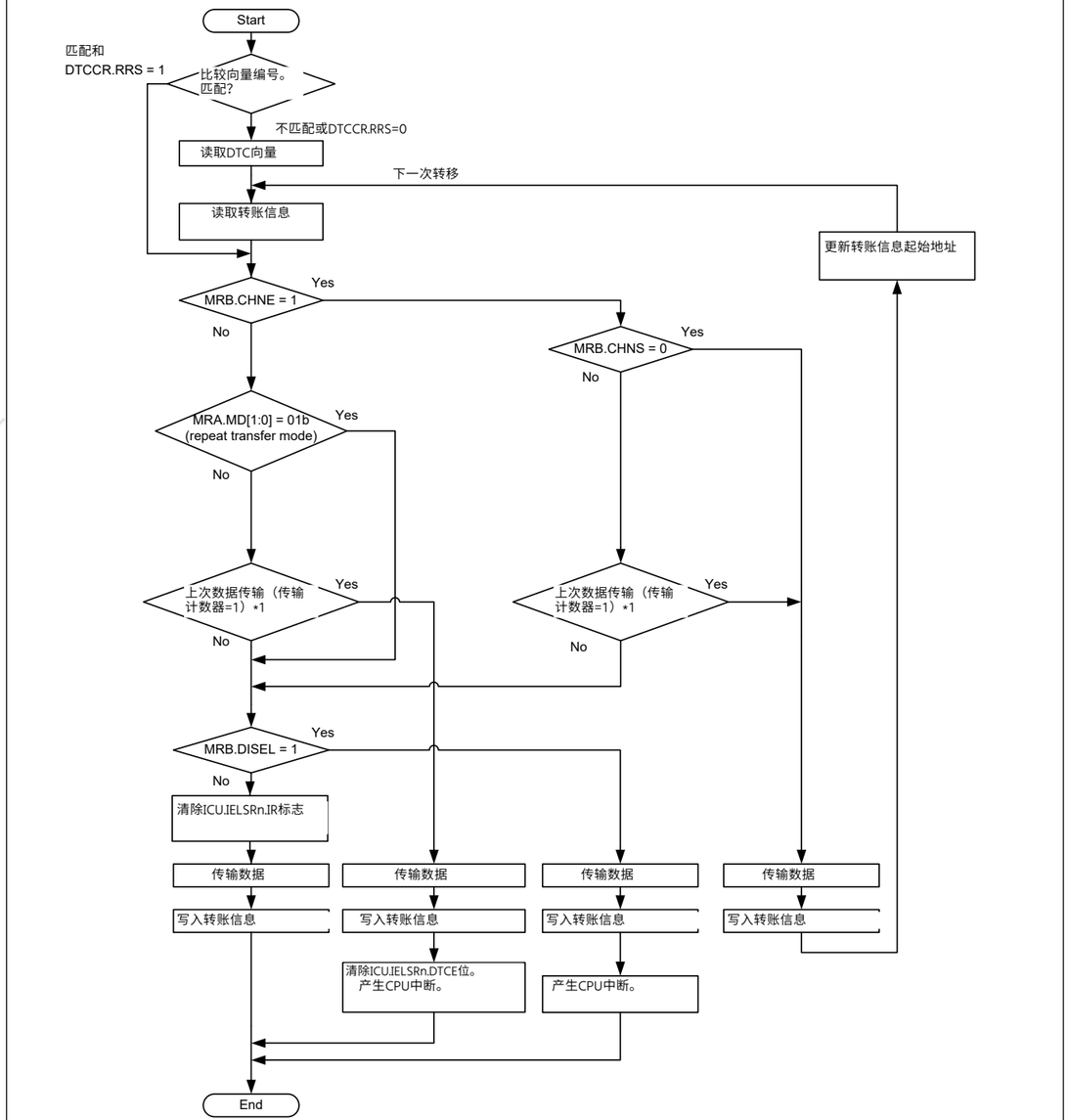


Note 1. Counter value before starting data transfer.

Figure 16.4 DTC operation flow

将MRB.CHNE位设置为1允许在单个激活源上进行多次传输或链式传输。当指定的数据传输完成时，它还启用链式传输。

图16.4显示了DTC的操作流程。表16.3列出了链转移条件。该表中省略了用于第二次和后续传输的控制信息的组合。



注1.开始数据传输前的计数器值。

Figure 16.4 DTC操作流程

Table 16.3 Chain transfer conditions

First transfer				Second transfer*3				DTC transfer
CHNE bit	CHNS bit	DISEL bit	Transfer counter*1 *2	CHNE bit	CHNS bit	DISEL bit	Transfer counter*1 *2	
0	—	0	Other than (1 → 0)	—	—	—	—	Ends after the first transfer
0	—	0	(1 → 0)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	0	Other than (1 → *)	—	—	—	—	Ends after the first transfer
1	1	—	(1 → *)	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	1	Other than (1 → *)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU

Note 1. The transfer counter used depends on the transfer modes as follows:
Normal transfer mode — CRA register
Repeat transfer mode — CRAL register
Block transfer mode — CRB register

Note 2. On completion of a data transfer, the counters operate as follows:
1 → 0 in normal and block transfer modes
1 → CRAH in repeat transfer mode
(1 → *) in the table indicates both of these two operations, depending on the mode.

Note 3. Chain transfer can be selected for the second or subsequent transfers. The conditions for the combination of the second transfer and CHNE = 1 is omitted.

16.4.1 Transfer Information Read Skip Function

Reading of vector addresses and transfer information can be skipped by setting the DTCCR.RRS bit. When a DTC activation request is generated, the current DTC vector number is compared with the DTC vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, the DTC data transfer is performed without reading the vector address and transfer information. However, when the previous transfer is a chain transfer, the vector address and transfer information are read. Additionally, when the transfer counter (CRA register) becomes 0 during the previous normal transfer, and when the transfer counter (CRB register) becomes 0 during the previous block transfer, transfer information is read regardless of the RRS bit. Figure 16.12 shows an example of a transfer information read skip.

To update the vector table and transfer information, set the RRS bit to 0, update the vector table and transfer information, then set the RRS bit to 1. The stored vector number is discarded by setting the RRS bit to 0. The updated DTC vector table and transfer information are read in the next activation process.

16.4.2 Transfer Information Write-Back Skip Function

When the MRA.SM[1:0] bits or the MRB.DM[1:0] bits are set to address fixed, a part of the transfer information is not written back. Table 16.4 lists the transfer information write-back skip conditions and the associated registers. The CRA and CRB registers are written back, and the write-back of the MRA and MRB registers is skipped.

Table 16.3 链转移条件

首次转让				二次转让*3				DTC transfer
CHNE bit	CHNS bit	DISEL bit	转帐计数器*1*2	CHNE bit	CHNS bit	DISEL bit	转帐计数器*1*2	
0	—	0	（1→0）以外	—	—	—	—	在第一次传输后结束
0	—	0	(1 → 0)	—	—	—	—	在第一次传输后结束，向CPU发出中断请求
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	（1→0）以外	在第二次转移后结束
				0	—	0	(1 → 0)	在第二次传输后结束，向CPU发出中断请求
				0	—	1	—	
1	1	0	(1→*)以外	—	—	—	—	在第一次传输后结束
1	1	—	(1 → *)	0	—	0	（1→0）以外	在第二次转移后结束
				0	—	0	(1 → 0)	在第二次传输后结束，向CPU发出中断请求
				0	—	1	—	
1	1	1	(1→*)以外	—	—	—	—	在第一次传输后结束，向CPU发出中断请求

注1.使用的传输计数器取决于传输模式，如下所示：
正常传输模式—CRA寄存器重复传输模式—CRAL寄存器
块传输模式——CRB寄存器

注2.数据传输完成后，计数器操作如下：1→0在正常和块传输模式下1→CRAH在重复传输模式下(1→*)表中表示这两种操作，具体取决于模式。

注3.第二次及以后的转账可选择链式转账。省略了二次传输和CHNE=1的组合条件。

16.4.1 传输信息读取跳过功能

通过设置DTCCR.RRS位可以跳过向量地址和传输信息的读取。当产生DTC激活请求时，将当前DTC向量编号与之前激活过程中的DTC向量编号进行比较。当这些向量编号匹配且RRS位设置为1时，执行DTC数据传输而不读取向量地址和传输信息。但是，当上一次传输是链式传输时，会读取向量地址和传输信息。此外，如果在上次正常传输期间传输计数器（CRA寄存器）变为0，并且在前一次块传输期间传输计数器（CRB寄存器）变为0，则无论RRS位如何，都将读取传输信息。图16.12显示了传输信息读取跳过的示例。

要更新向量表和传输信息，请将RRS位设置为0，更新向量表和传输信息，然后将RRS位设置为1。通过将RRS位设置为0，丢弃存储的向量编号。更新的DTC向量在下一个激活过程中读取表和传输信息。

16.4.2 传输信息回写跳过功能

当MRA.SM[1:0]位或MRB.DM[1:0]位设置为地址固定时，部分传输信息不会被写回。表16.4列出了传输信息回写跳过条件和相关寄存器。回写CRA和CRB寄存器，跳过回写MRA和MRB寄存器。

Table 16.4 Transfer information write-back skip conditions and applicable registers

MRA.SM[1:0] bits		MRB.DM[1:0] bits			
b3	b2	b3	b2	SAR register	DAR register
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

16.4.3 Normal Transfer Mode

The normal transfer mode allows a 1-byte (8 bit), 1-halfword (16 bit), 1-word (32 bit) data transfer on a single activation source. The transfer count can be set to 1 to 65536. Transfer source and destination addresses can be independently set to increment, decrement, or fixed. This mode enables an interrupt request to the CPU to be generated at the end of a specified-count transfer.

Table 16.5 lists register functions in normal transfer mode, and Figure 16.5 shows the memory map of normal transfer mode.

Table 16.5 Register functions in normal transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	Increment, decrement, or fixed*1
DAR	Transfer destination address	Increment, decrement, fixed*1
CRA	Transfer counter A	CRA - 1
CRB	Transfer counter B	Not updated

Note 1. Write-back operation is skipped in address-fixed mode.

Table 16.4 传输信息回写跳过条件和适用寄存器

MRA.SM[1:0] bits		MRB.DM[1:0] bits			
b3	b2	b3	b2	SAR寄存器	DAR寄存器
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

16.4.3 正常传输模式

正常传输模式允许在单个激活源上传输1字节（8位）、1半字（16位）、1字（32位）数据。传输计数可以设置为1到65536。传输源地址和目标地址可以独立设置为递增、递减或固定。此模式允许在指定计数传输结束时向CPU生成中断请求。

表16.5列出了正常传输模式下的寄存器功能，图16.5显示了正常传输模式下的内存映射。

Table 16.5 正常传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值
SAR	传输源地址	递增、递减或固定*1
DAR	转移目的地地址	递增、递减、固定*1
CRA	转帐柜台A	CRA - 1
CRB	转帐柜台B	未更新

注1.在地址固定模式下会跳过回写操作。

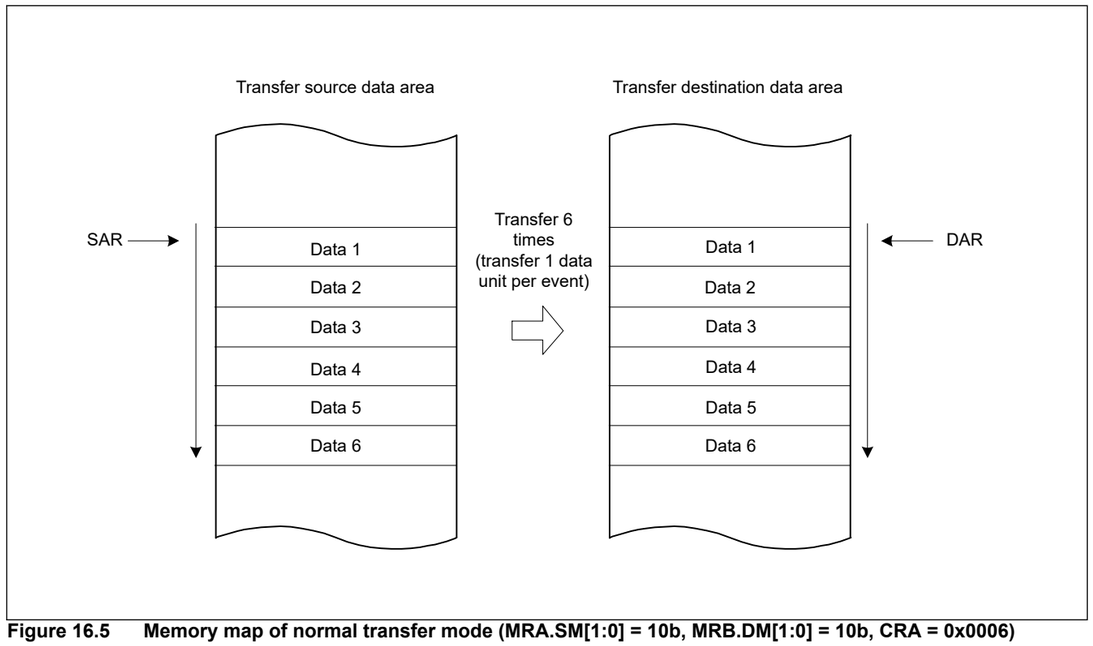


Figure 16.5 Memory map of normal transfer mode (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRA = 0x0006)

16.4.4 Repeat Transfer Mode

The repeat transfer mode allows a 1-byte (8-bit), 1-halfword (16-bit), or 1-word (32-bit) data transfer on a single activation source. Transfer source or transfer destination for the repeat area must be specified in the MRB.DTS bit. The transfer count can be set from 1 to 256. When the specified transfer count is complete, the initial value of the address register specified in the repeat area is restored, the initial value of the transfer counter is restored, and transfer is repeated. The other address register is incremented or decremented continuously or remains unchanged.

When the transfer counter CRAL decrements to 0x00 in repeat transfer mode, the CRAL value is updated to the value set in the CRAH register. As a result, the transfer counter does not clear to 0x00, which disables interrupt requests to the CPU when the MRB.DISEL bit is set to 0. An interrupt request to the CPU is generated when the specified data transfer completes.

Table 16.6 lists the register functions in repeat transfer mode, and Figure 16.6 shows the memory map of repeat transfer mode.

Table 16.6 Register functions in repeat transfer mode

Register	Description	Value written back by writing transfer information	
		When CRAL is not 1	When CRAL is 1
SAR	Transfer source address	Increment, decrement, fixed*1	• When the MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When the MRB.DTS bit is 1 SAR register initial value
DAR	Transfer destination address	Increment, decrement, or fixed*1	• When the MRB.DTS bit is 0 DAR register initial value • When the MRB.DTS bit is 1 Increment, decrement, or fixed*1
CRAH	Retains transfer counter	CRAH	CRAH
CRAL	Transfer counter A	CRAL - 1	CRAH
CRB	Transfer counter B	Not updated	Not updated

Note 1. Write-back is skipped in address-fixed mode.

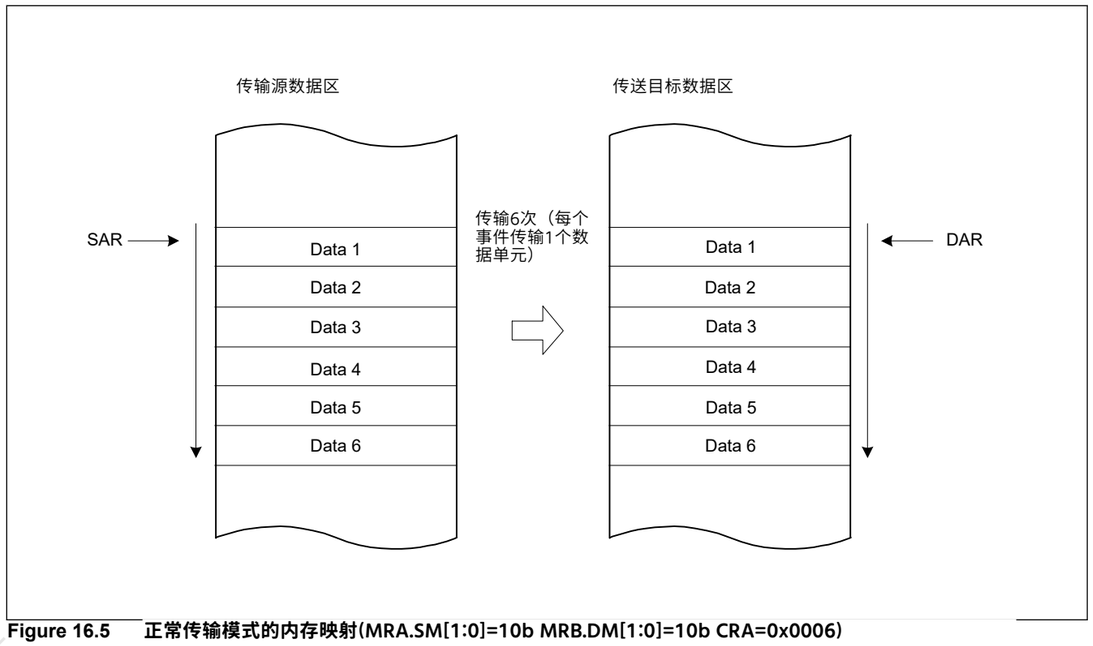


Figure 16.5 正常传输模式的内存映射(MRA.SM[1:0]=10b MRB.DM[1:0]=10b CRA=0x0006)

16.4.4 重复传输模式

重复传输模式允许在单个激活源上传输1字节（8位）、1半字（16位）或1字（32位）数据。重复区域的传输源或传输目标必须在MRB.DTS位中指定。传输计数可设置为1到256。当指定的传输计数完成时，将恢复重复区域中指定的地址寄存器的初始值，恢复传输计数器的初始值，并重复传输。另一个地址寄存器连续递增或递减或保持不变。

当传输计数器CRAL在重复传输模式下递减到0x00时，CRAL值将更新为CRAH寄存器中设置的值。因此，传输计数器不会清为0x00，这会在MRB.DISEL位设置为0时禁用对CPU的中断请求。当指定的数据传输完成时，会向CPU发出中断请求。

表16.6列出了重复传输模式下的寄存器功能，图16.6显示了重复传输模式的内存映射。

Table 16.6 重复传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值	
		当CRAL不为1时	当CRAL为1时
SAR	传输源地址	递增、递减、固定*1	• 当MRB.DTS位为0时 递增、递减或固定*1 • MRB.DTS位为1时 SAR寄存器初始值
DAR	转移目的地地址	递增、递减或固定*1	• 当MRB.DTS位为0时 DAR寄存器初始值 • MRB.DTS位为1时 递增、递减或固定*1
CRAH	保留转帐计数器	CRAH	CRAH
CRAL	转帐柜台A	CRAL - 1	CRAH
CRB	转帐柜台B	未更新	未更新

注1.在地址固定模式下会跳过回写。

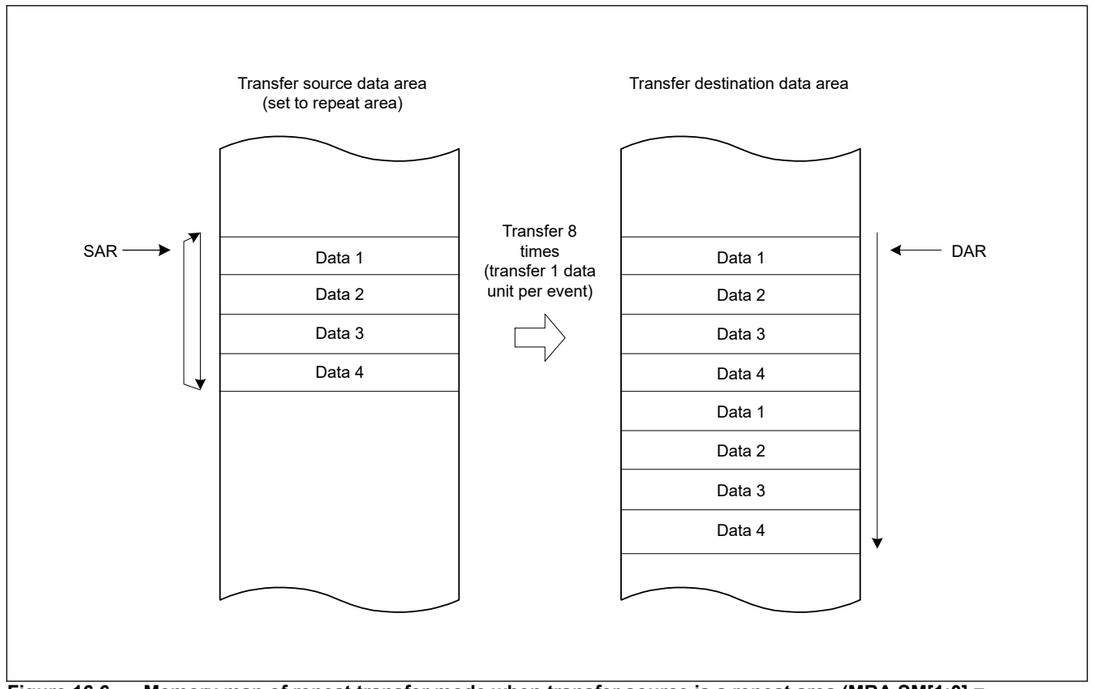


Figure 16.6 Memory map of repeat transfer mode when transfer source is a repeat area (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRAH = 0x04)

16.4.5 Block Transfer Mode

The block transfer mode allows single-block data transfer on a single activation source. Transfer source or transfer destination for the block area must be specified in the MRB.DTS bit. The block size can be set from 1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes). When transfer of the specified block completes, the initial values of the block size counter CRAL and the address register (the SAR register when the MRB.DTS = 1 or the DAR register when the DTS = 0) specified in the block area are restored. The other address register is incremented or decremented continuously or remains unchanged.

The transfer count (block count) can be set from 1 to 65536. This mode enables an interrupt request to the CPU to be generated at the end of the specified-count block transfer.

Table 16.7 lists the register functions in block transfer mode, and Figure 16.7 shows the memory map for block transfer mode.

Table 16.7 Register functions in block transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	• When MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When MRB.DTS bit is 1 SAR register initial value.
DAR	Transfer destination address	• When MRB.DTS bit is 0 DAR register initial value • When MRB.DTS bit is 1 Increment, decrement, or fixed*1.
CRAH	Holds block size	CRAH
CRAL	Block size counter	CRAH
CRB	Block transfer counter	CRB - 1

Note 1. Write-back is skipped in address-fixed mode.

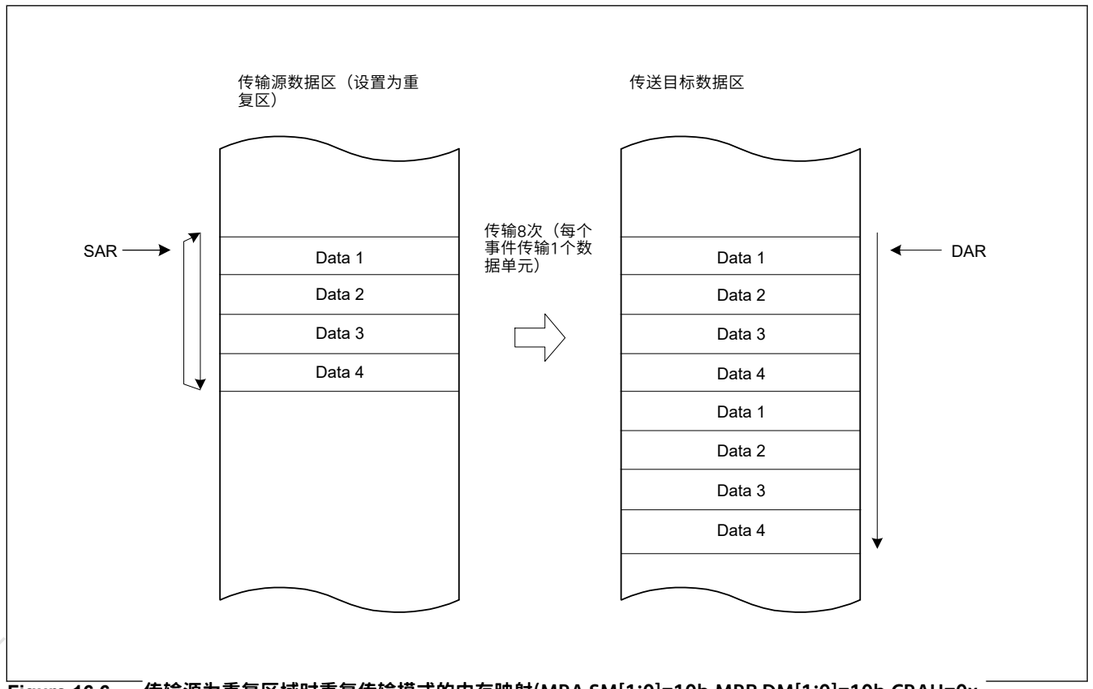


Figure 16.6 传输源为重复区域时重复传输模式的内存映射(MRA.SM[1:0]=10b MRB.DM[1:0]=10b CRAH=0x04)

16.4.5 块传输模式

块传输模式允许在单个激活源上进行单块数据传输。块区域的传输源或传输目标必须在MRB.DTS位中指定。块大小可以设置为1到256字节、1到256个半字（2到512字节）或1到256字（4到1024字节）。当指定块的传送完成时，块区域中指定的块大小计数器CRAL和地址寄存器（MRB.DTS=1时为SAR寄存器或DTS=0时为DAR寄存器）的初始值被恢复。另一个地址寄存器连续递增或递减或保持不变。

传输计数（块计数）可设置为1到65536。此模式允许在指定计数块传输结束时向CPU生成中断请求。

表16.7列出了块传输模式下的寄存器功能，图16.7显示了块传输模式下的存储器映射。

Table 16.7 块传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值
SAR	传输源地址	• 当MRB.DTS位为0时 递增、递减或固定*1 • 当MRB.DTS位为1时SAR 寄存器初始值。
DAR	转移目的地地址	• 当MRB.DTS位为0DAR寄 存器初始值 • 当MRB.DTS位为1时 递增、递减或固定*1。
CRAH	保持块大小	CRAH
CRAL	块大小计数器	CRAH
CRB	块传输计数器	CRB - 1

注1.在地址固定模式下会跳过回写。

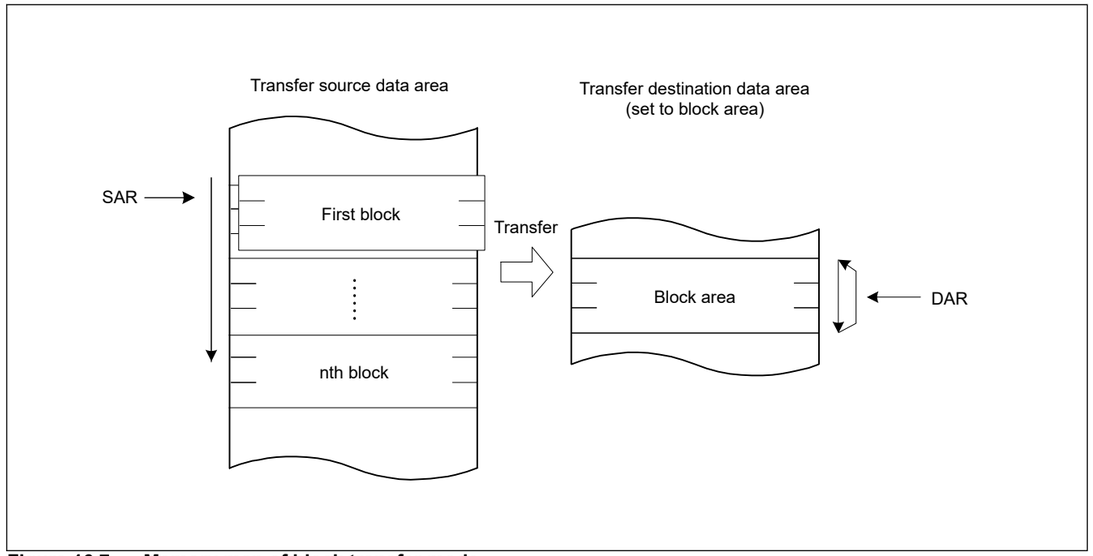


Figure 16.7 Memory map of block transfer mode

16.4.6 Chain Transfer

Setting the MRB.CHNE bit to 1 allows chain transfer to be performed continuously on a single activation source. If the MRB.CHNE is set to 1 and CHNS to 0, an interrupt request to the CPU is not generated on completion of the specified number of rounds of transfer or by setting the MRB.DISEL bit to 1. An interrupt request is sent to the CPU each time DTC data transfer is performed. Data transfer has no effect on the ICU.IELSRn.IR flag of the activation source.

The SAR, DAR, CRA, CRB, MRA, and MRB registers can be set independently of each other to define the data transfer. Figure 16.8 shows a chain transfer operation.

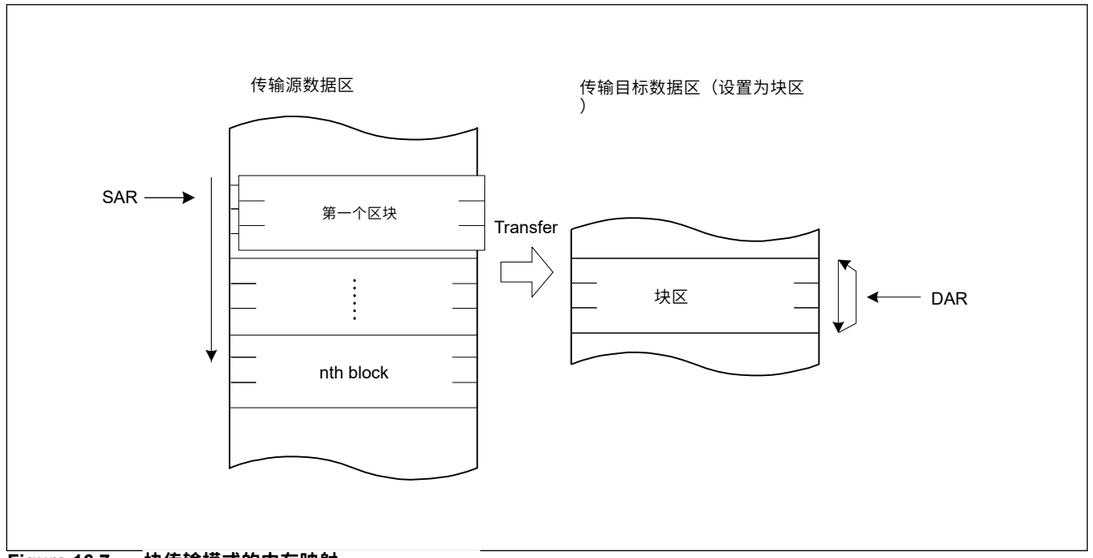


Figure 16.7 块传输模式的内存映射

16.4.6 链转移

将MRB.CHNE位设置为1允许在单个激活源上连续执行链传输。如果MRB.CHNE设置为1，CHNS设置为0，则在完成指定的传输轮数或将MRB.DISEL位设置为1时不会向CPU产生中断请求。中断请求被发送到每次执行DTC数据传输时CPU。数据传输对激活源的ICU.IELSRn.IR标志没有影响。

SAR、DAR、CRA、CRB、MRA和MRB寄存器可以相互独立设置以定义数据传输。
图16.8显示了链式转移操作。

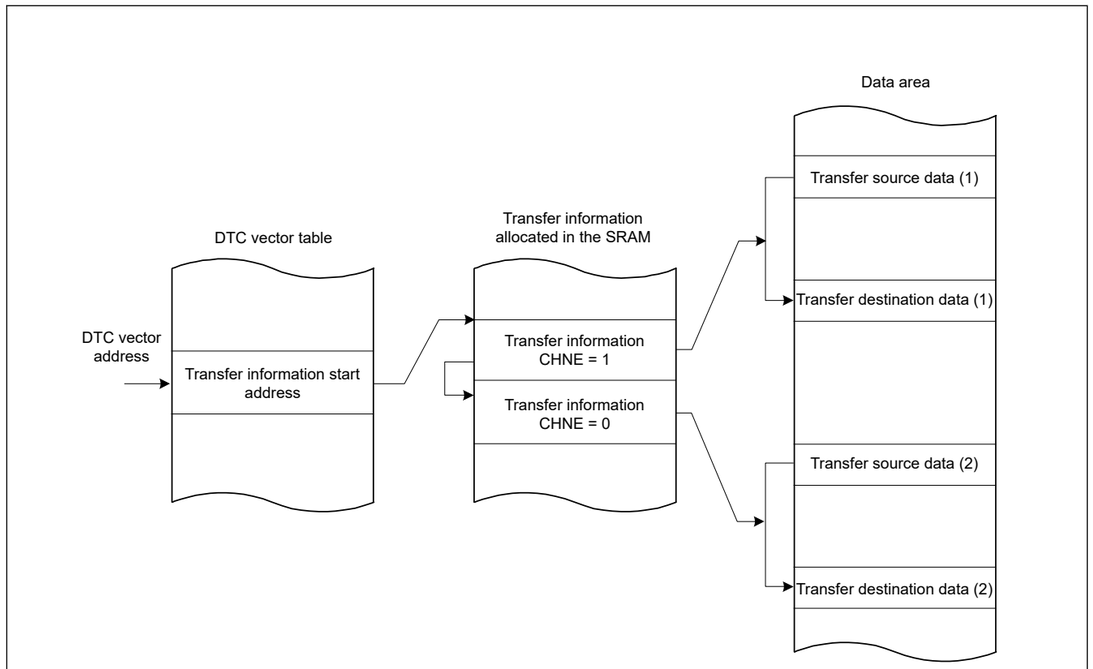


Figure 16.8 Chain transfer operation

Writing 1 to the MRB.CHNE and CHNS bits enables chain transfer to be performed only after completion of the specified data transfer. In repeat transfer mode, chain transfer is performed after completion of the specified data transfer. For details on chain transfer conditions, see Table 16.3.

16.4.7 Operation Timing

Figure 16.9 to Figure 16.12 are timing diagrams that show the minimum number of execution cycles.

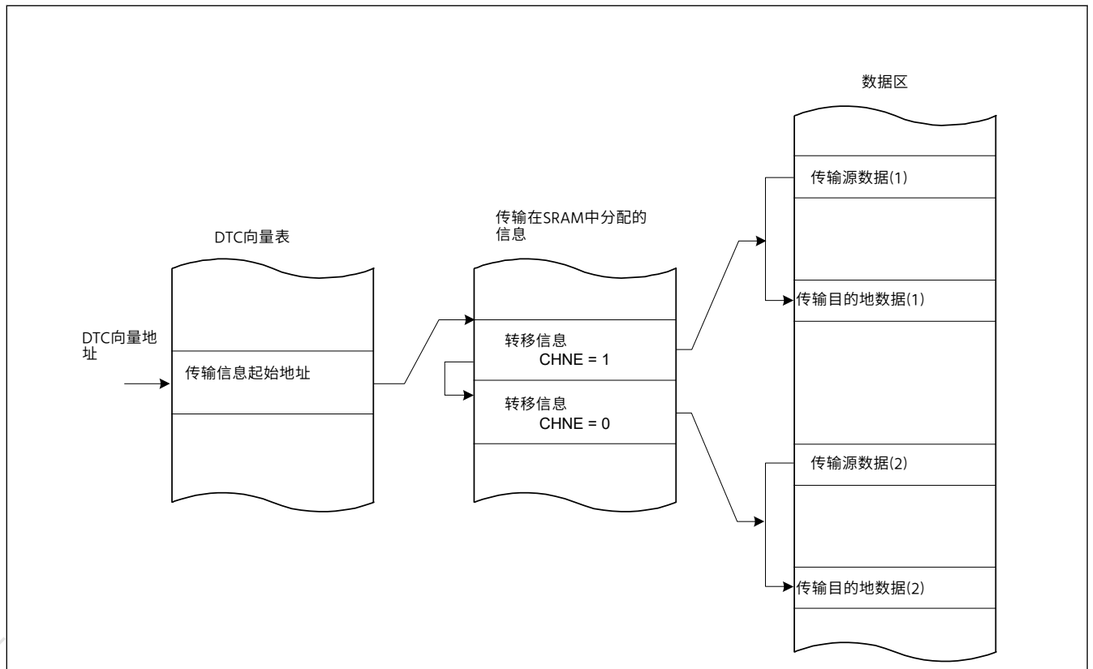


Figure 16.8 链转移操作

将1写入MRB.CHNE和CHNS位可以使链式传输仅在完成指定的数据传输后执行。在重复传输模式下，在完成指定的数据传输后执行链式传输。有关链转移条件的详细信息，请参见表16.3。

16.4.7 操作时间

图16.9至图16.12是显示最小执行周期数的时序图。

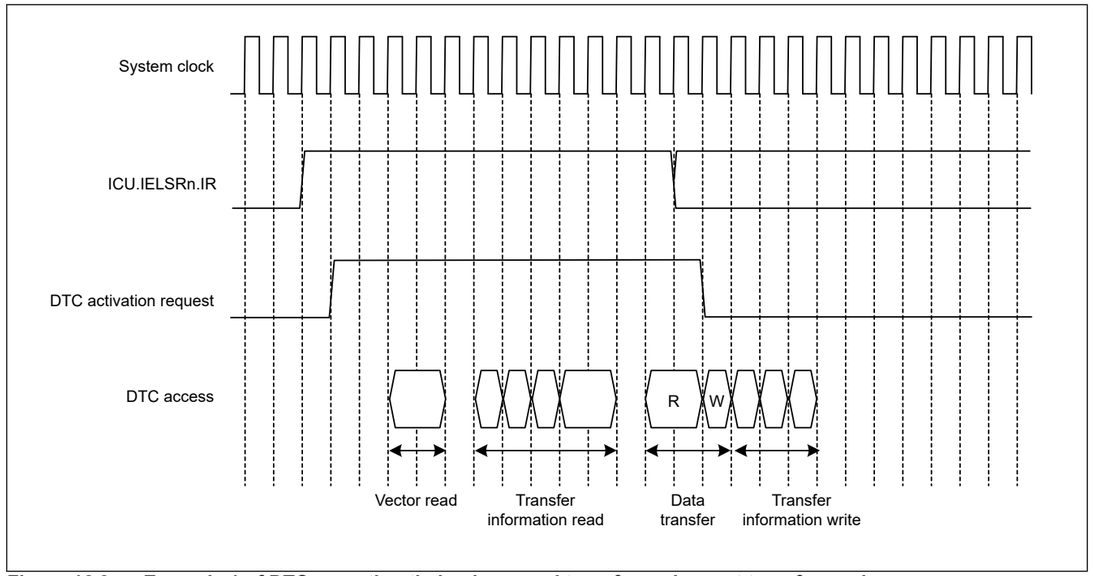


Figure 16.9 Example 1 of DTC operation timing in normal transfer and repeat transfer modes

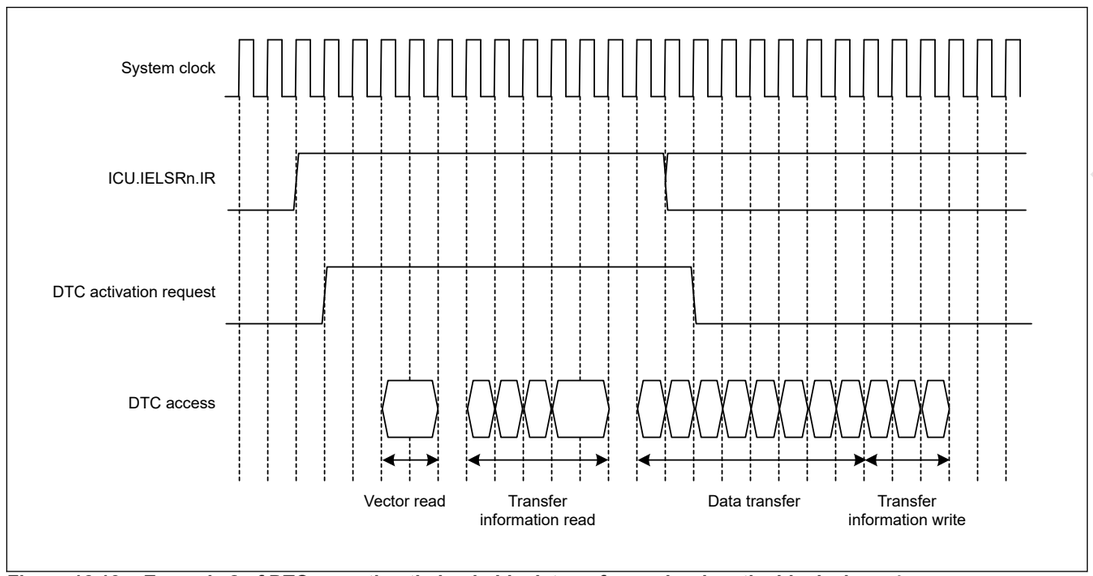


Figure 16.10 Example 2 of DTC operation timing in block transfer mode when the block size = 4

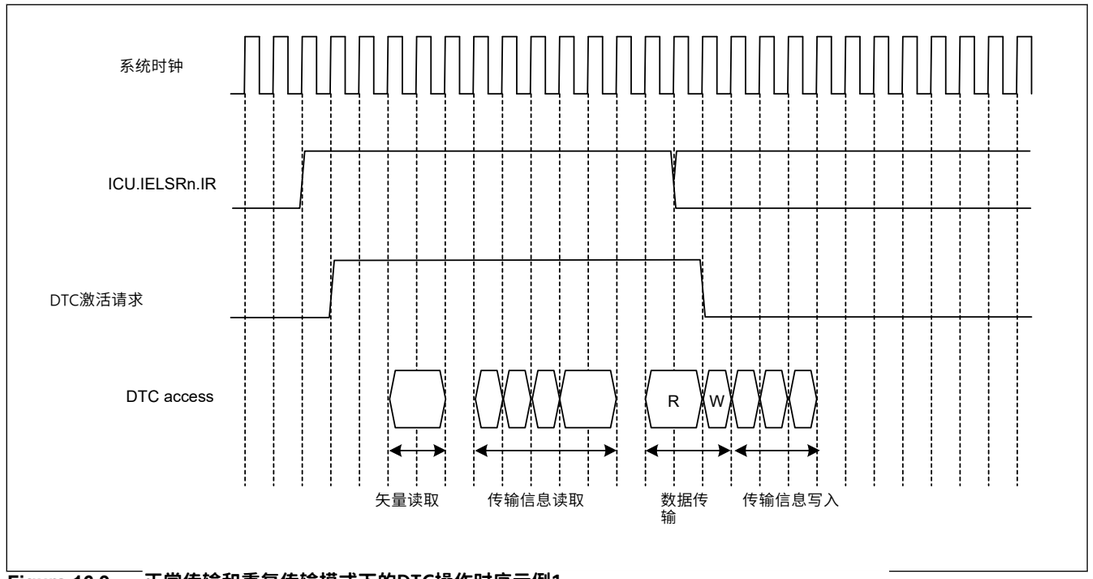


Figure 16.9 正常传输和重复传输模式下的DTC操作时序示例1

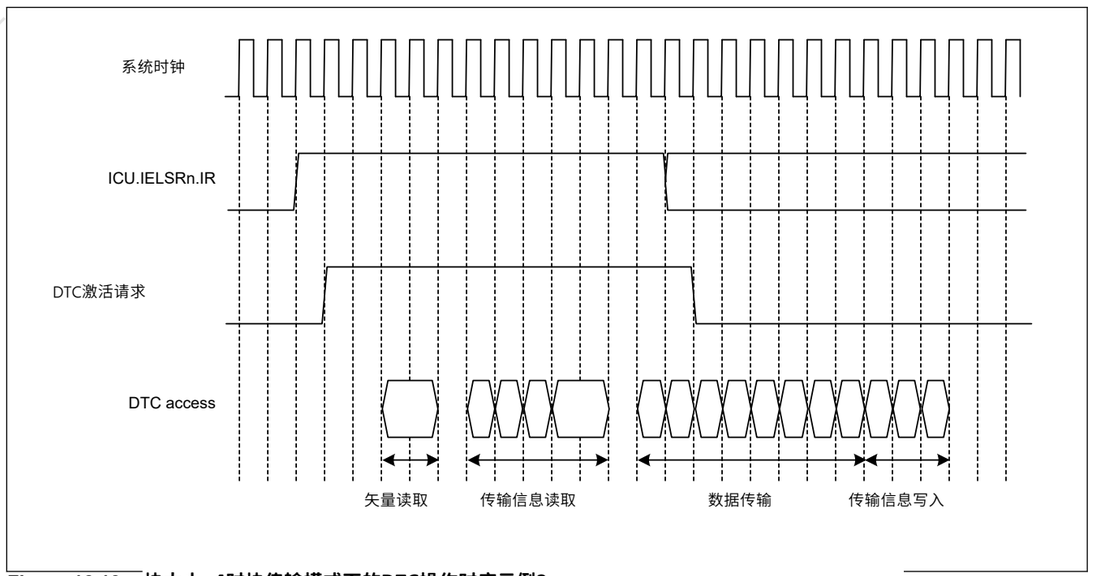


Figure 16.10 块大小=4时块传输模式下的DTC操作时序示例2

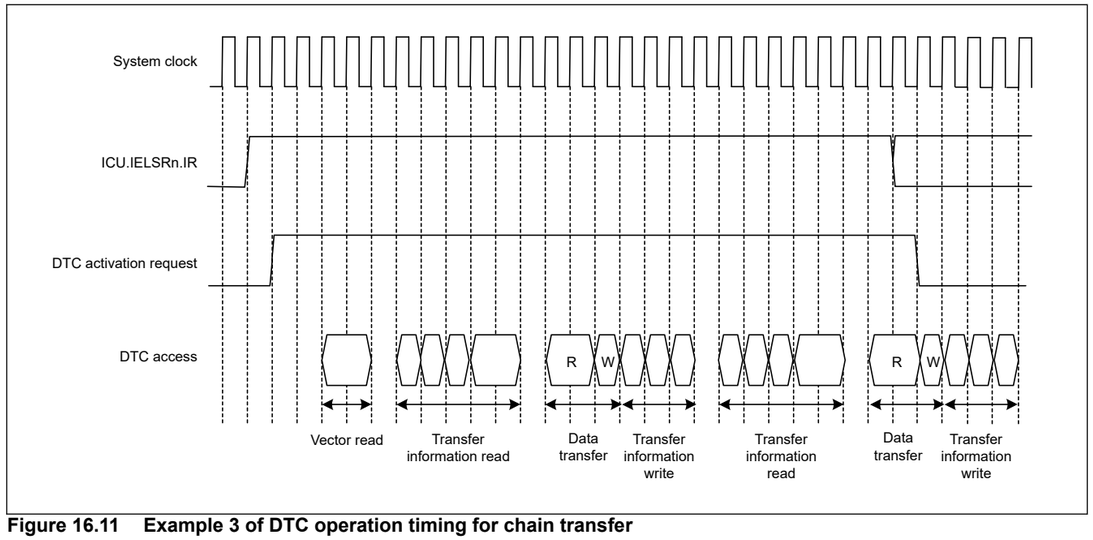
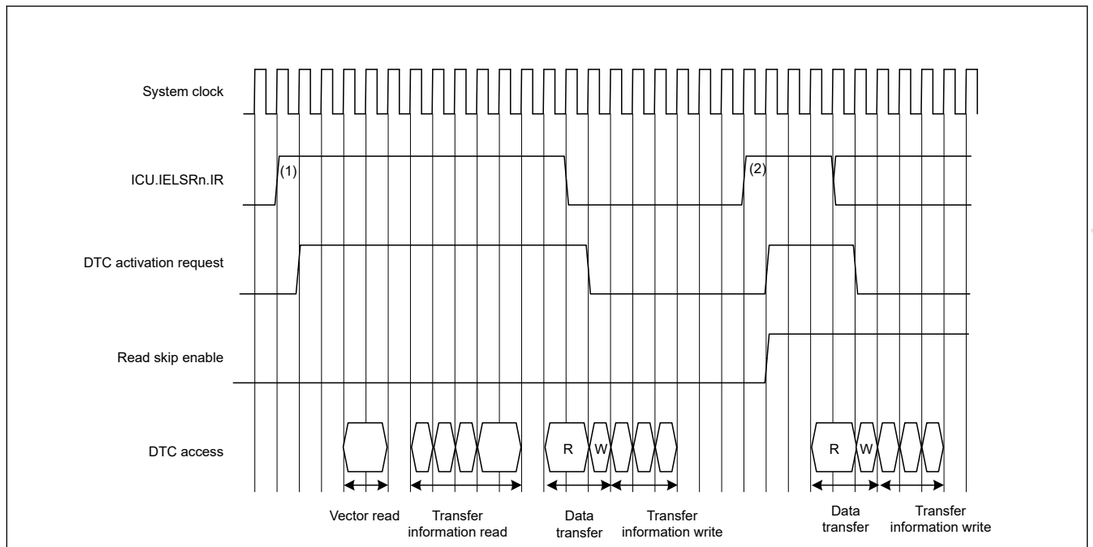


Figure 16.11 Example 3 of DTC operation timing for chain transfer



Note: When activation sources (vector numbers) of (1) and (2) are the same and the RRS = 1, the transfer information read for request (2) is skipped.

Figure 16.12 Example of operation when a transfer information read is skipped with the vector, transfer information, and transfer destination data on the SRAM, and the transfer source data on the peripheral module

16.4.8 Execution Cycles of DTC

Table 16.8 lists the execution cycles of single data transfer of the DTC. For the order of the execution states, see section 16.4.7. Operation Timing.

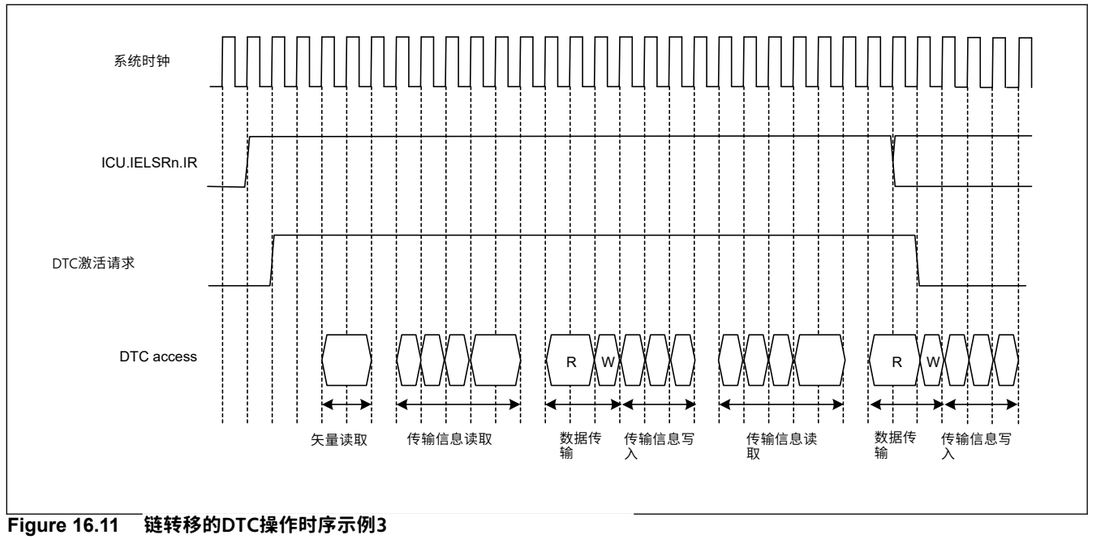
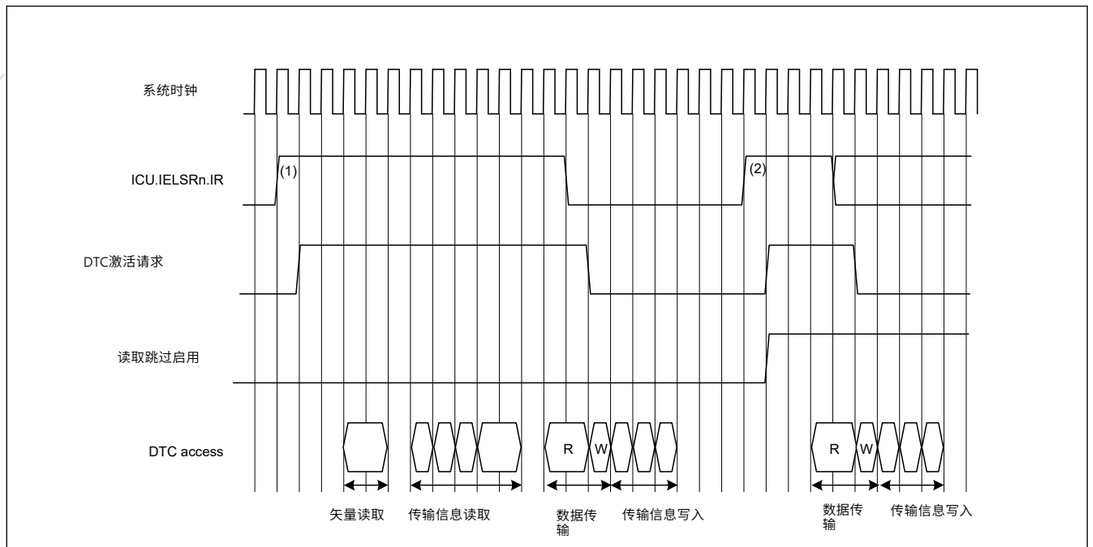


Figure 16.11 链转移的DTC操作时序示例3



Note: 当(1)和(2)的激活源(向量号)相同且RRS=1时，跳过请求(2)读取的传输信息。

Figure 16.12 使用SRAM上的向量、传输信息和传输目标数据以及外围模块上的传输源数据跳过传输信息读取时的操作示例

16.4.8 DTC的执行周期

表16.8列出了DTC单次数据传输的执行周期。有关执行状态的顺序，请参见第16.4.7节。操作时间。

Table 16.8 Execution cycles of DTC

P: Block size (initial settings of CRAH and CRAL)
Cv: Cycles for access to vector transfer information storage destination
Ci: Cycles for access to transfer information storage destination address
Cr: Cycles for access to data read destination
Cw: Cycles for access to data write destination
The unit is for system clocks (ICLK) + 1 in the Vector read, Transfer information read, and Data transfer read columns and 2 in the Internal operation column.
Cv, Ci, Cr, and Cw vary depending on the corresponding access destination. For the number of cycles for respective access destinations, see section 41, SRAM, section 43, Flash Memory, and section 13, Buses.
The frequency ratio of the system clock and peripheral clock is also taken into consideration.
The DTC response time is the time from when the DTC activation source is detected until DTC transfer starts.
Table 16.8 does not include the time until DTC data transfer starts after the DTC activation source becomes active.

Transfer mode	Vector read		Transfer information read		Transfer information write			Data transfer		Internal operation	
								Read	Write		
Normal	Cv + 1	0*1	4 × Ci + 1	0*1	3 × Ci + 1*2	2 × Ci + 1*3	Ci*4	Cr + 1	Cw + 1	2	0*1
Repeat								Cr + 1	Cw + 1		
Block*5								P × Cr	P × Cw		

Note 1. When transfer information read is skipped.
Note 2. When neither SAR nor DAR is set to address-fixed mode.
Note 3. When SAR or DAR is set to address-fixed mode.
Note 4. When SAR and DAR are set to address-fixed mode.
Note 5. When the block size is 2 or more. If the block size is 1, the cycle number for normal transfer applies.

16.4.9 DTC Bus Mastership Release Timing

The DTC does not release the bus mastership during transfer information reads. Before the transfer information is read or written, the bus is arbitrated according to the priority determined by the bus master arbitrator. For bus arbitration, see section 13, Buses.

16.4.10 Vector Security

The security attribute of transfer access of DTC vector n and security attribute of access to the IELSRn(n = 0 to 95) register of ICU are controlled by SAIELSRn bit of ICUSARx(x = G,H or I) registers in CPSCU. For details on the CPSCU.ICUSARx registers, see section 12, Interrupt Controller Unit (ICU).

When the CPSCU.ICUSARx.SAIELSRn bit is 0, transfer of DTC vector n is secure access for both read and write. At the same time, the IELSRn register are protected from a non-secure access.

When the CPSCU.ICUSARx.SAIELSRn bit is 1, transfer of DTC vector n is non-secure access for both read and write. At the same time, the IELSRn register are non-secure attributes.

Do not write to the CPSCU.ICUSARx.SAIELSRn bit while DTC transfer is enabled or a bus master is writing to the DTC registers of same channel.

section 16.3.1. Allocating Transfer Information and DTC Vector Table shows security attribute about each DTC vectors.

16.4.11 Master TrustZone Filter in DTC

DTC has the Master TrustZone Filter. The Master TrustZone Filter in DTC can detect the security areas of Flash area(code Flash and data Flash) and SRAM area defined by IDAU. When no-secure accesses those addresses, it detects the security violation. Access of violation address is not performed. Detected the error is handled as the Master TrustZone Filter error.

16.5 DTC Setting Procedure

Before using the DTC, set the DTC Vector Base Register (DTCVBR). Set the ICU.IELSRn.IELS[8:0] bits to 0 to disable the interrupt in the NVIC and follow the procedure in Table 16.9 to set the DTC.

Table 16.8 DTC的执行周期

P：块大小（CRAH和CRAL的初始设置）
Cv：访问向量传输信息存储目标的周期Ci：访问传输信息存储目标地址的周期
Cr：访问数据读取目标的周期Cw：访问数据写入目标的周期
单位为系统时钟(ICLK)+1在Vectorread、Transferinformationread和Datatransferread列中和2在内部操作列中。Cv、Ci、Cr和Cw根据相应的访问目的地而变化。有关各个访问目标的周期数，请参见第41节SRAM、第43节闪存和第13节总线。系统时钟和外设时钟的频率比也被考虑在内。

DTC响应时间是从检测到DTC激活源到DTC传输开始的时间。
表16.8不包括从DTC激活源激活到DTC数据传输开始的时间。

传输模式	矢量读取		传输信息读取		传输信息写入			数据传输		内部运作	
								Read	Write		
Normal	Cv + 1	0*1	4 × Ci + 1	0*1	3 × Ci + 1*2	2 × Ci + 1*3	Ci*4	Cr + 1	Cw + 1	2	0*1
Repeat								Cr + 1	Cw + 1		
Block*5								P × Cr	P × Cw		

注1.跳过传输信息读取时。
注2.当SAR和DAR均未设置为地址固定模式时。
注3.当SAR或DAR设置为地址固定模式时。
注4.当SAR和DAR设置为地址固定模式时。
注5.当块大小为2或更大时。如果块大小为1，则适用正常传输的周期数。

16.4.9 DTC总线主控释放时序

在传输信息读取期间，DTC不会释放总线主控权。在读取或写入传输信息之前，根据总线主仲裁器确定的优先级对总线进行仲裁。对于总线仲裁，请参见第13节，总线。

16.4.10 矢量安全

DTC向量n的传输访问的安全属性和对ICU的IELSRn(n=0到95)寄存器的访问的安全属性由CPSCU中ICUSARx(x=G H或I)寄存器的SAIELSRn位控制。有关CPSCU.ICUSARx寄存器的详细信息，请参见第12节，中断控制器单元(ICU)。

当CPSCU.ICUSARx.SAIELSRn位为0时，DTC向量n的传输对于读和写都是安全访问。同时，保护IELSRn寄存器免受非安全访问。

当CPSCU.ICUSARx.SAIELSRn位为1时，DTC向量n的传输对于读取和写入都是非安全访问。同时，IELSRn寄存器是非安全属性。

当DTC传输使能或总线主机正在写入同一通道的DTC寄存器时，请勿写入CPSCU.ICUSARx.SAIELSRn位。

第16.3.1节。分配传输信息和DTC向量表显示每个DTC向量的安全属性。

16.4.11 DTC中的主TrustZone过滤器

DTC具有MasterTrustZone过滤器。DTC中的MasterTrustZoneFilter可以检测IDAU定义的Flash区域（代码Flash和数据Flash）和SRAM区域的安全区域。当no-secure访问这些地址时，它会检测到安全违规。不执行违规地址的访问。检测到的错误作为MasterTrustZoneFilter错误处理。

16.5 DTC设置程序

在使用DTC之前，请设置DTC向量基址寄存器(DTCVBR)。将ICU.IELSRn.IELS[8:0]位设置为0以禁用NVIC中的中断，并按照表16.9中的程序设置DTC。

Table 16.9 DTC setting procedure

No.	Step Name	Description
1	Set the DTCCR*1.RRS bit to 0	Set the DTCCR*1.RRS bit to 0 to reset the transfer information read skip flag. After that, the transfer information read is not skipped while the DTC is activated. Be sure to specify this setting when the transfer information is updated.
2	Set transfer information (MRA, MRB, SAR, DAR, CRA, and CRB)	Allocate transfer information (MRA, MRB, SAR, DAR, CRA, and CRB) in the data area. To set transfer information, see section 16.2. Register Descriptions. To allocate transfer information, see section 16.3.1. Allocating Transfer Information and DTC Vector Table.
3	Set transfer information start addresses in the DTC vector table	Set the transfer information start addresses in the DTC vector table. To set the DTC vector table, see section 16.3.1. Allocating Transfer Information and DTC Vector Table.
4	Set the DTCCR*1.RRS bit to 1	Set the DTCCR*1.RRS bit to 1 to enable skipping of the second and subsequent transfer information read cycles for continuous DTC activation from the same interrupt source. The RRS bit can be set to 1, but if this is set during DTC transfer, it becomes valid from the next transfer.
5	Set the ICU.IELSRn.DTCE bit to 1. Set the ICU.IELSRn.IELS[8:0] as interrupt source. The interrupt should be enabled in the NVIC.	Set the ICU.IELSRn.DTCE bit to 1. Set ICU.IELSRn.IELS[8:0] as interrupt sources that trigger DTC. The interrupt must be enabled in the NVIC. See section 12.3.2. Event Number in section 12, Interrupt Controller Unit (ICU).
6	Set the enable bit for an activation source interrupt	Set the enable bit for the activation source interrupts to 1. When a source interrupt is generated, the DTC is activated. To set the interrupt source enable bit, see the settings for the modules that are to be the activation sources.
7	Set the DTCST.DTCST bit to 1	Set the DTC Module Start bit (DTCST.DTCST) to 1.

Note: The DTCST.DTCST bit can be set even if the setting for each activation source is not completed.
Note: When used in non-secure state, DTCSAR.DTCSTSA = 1 or DTCST.DTCST = 1 must be set.
Note 1. When used in secure state, access DTCCR_SEC instead of DTCCR.

16.6 Examples of DTC Usage

16.6.1 Normal Transfer

This section provides an example of DTC usage and its application when receiving 128 bytes of data from an SCI.

(1) Transfer information settings

In the MRA register, select a fixed source address (MRA.SM[1:0] = 00b), normal transfer mode (MRA.MD[1:0] = 00b), and byte-sized transfer (MRA.SZ[1:0] = 00b). In the MRB register, specify incrementation of the destination address (MRB.DM[1:0] = 10b) and single data transfer by a single interrupt (MRB.CHNE = 0 and MRB.DISEL = 0). The MRB.DTS bit can be set to any value. Set the RDR register address of the SCI in the SAR register, the start address of the SRAM area for data storage in the DAR register, and 128 (0x0080) in the CRA register. The CRB register can be set to any value.

(2) DTC vector table settings

The start address of the transfer information for the RXI interrupt is set in the vector table for the DTC.

(3) ICU settings and DTC module activation

Set the ICU.IELSRn.DTCE bit to 1 and set ICU.IELSRn.IELS[8:0] as the SCI interrupt. The interrupt must be enabled in the NVIC. Set the DTCST.DTCST bit to 1.

(4) SCI settings

Enable the SCIn_RXI interrupt by setting the CCR0.RIE bit in the SCI to 1. If a reception error occurs during the SCI receive operation, reception stops. To manage this, use settings that allow the CPU to accept receive error interrupts.

(5) DTC transfer

Each time a reception of 1 byte by the SCI is complete, an SCIn_RXI interrupt is generated to activate the DTC. The DTC transfers the received byte from the RDR of the SCI to the SRAM, after which the DAR register is incremented and the CRA register is decremented.

Table 16.9 DTC设置程序

No.	步骤名称	Description
1	将DTCCR*1.RRS位设置为0	将DTCCR*1.RRS位设置为0以重置传输信息读取跳过标志。之后，在激活DTC时不会跳过读取的传输信息。请务必在传输信息更新时指定此设置。
2	设置传输信息（MRA、MRB、SAR、DAR、CRA和CRB）	在数据区分配传输信息（MRA、MRB、SAR、DAR、CRA和CRB）。要设置传输信息，请参阅第16.2节。注册说明。要分配传输信息，请参阅第16.3.1节。分配传输信息和DTC向量表。
3	在DTC向量表中设置传输信息起始地址	在DTC向量表中设置传输信息起始地址。要设置DTC矢量表，请参阅第16.3.1节。分配传输信息和DTC向量表。
4	将DTCCR*1.RRS位设置为1	将DTCCR*1.RRS位设置为1，以允许跳过第二个和后续传输信息读取周期，以便从同一中断源连续激活DTC。RRS位可以设置为1，但如果在DTC传输期间设置，则从下一次传输开始生效。
5	将ICU.IELSRn.DTCE位设置为1。将ICU.IELSRn.IELS[8:0]设置为中断源。应在NVIC中启用中断。	将ICU.IELSRn.DTCE位设置为1。将ICU.IELSRn.IELS[8:0]设置为触发的中断源故障诊断码。必须在NVIC中启用中断。请参阅第12.3.2节。第12节中的事件编号，中断控制器单元（ICU）。
6	设置激活源中断的使能位	将激活源中断的使能位设置为1。当产生源中断时，将激活DTC。要设置中断源使能位，请参见要成为激活源的模块的设置。
7	将DTCST.DTCST位设置为1	将DTC模块起始位(DTCST.DTCST)设置为1。

Note: 即使每个激活源的设置未完成，也可以设置DTCST.DTCST位。
Note: 在非安全状态下使用时，必须设置DTCSAR.DTCSTSA=1或DTCST.DTCST=1。
注1.在安全状态下使用时，访问DTCCR_SEC而不是DTCCR。

16.6 DTC使用示例

16.6.1 正常转移

本节提供从SCI接收128字节数据时的DTC用法及其应用示例。

(1) 传输信息设置

在MRA寄存器中，选择固定源地址（MRA.SM[1:0]=00b）、正常传输模式（MRA.MD[1:0]=00b）和字节大小传输（MRA.SZ[1:0]=00b)。在MRB寄存器中，指定目标地址的递增(MRB.DM[1:0]=10b)和单个中断的单个数据传输(MRB.CHNE=0和MRB.DISEL=0)。MRB.DTS位可以设置为任何值。在SAR寄存器中设置SCI的RDR寄存器地址，

SRAM区域用于DAR寄存器中的数据存储，以及CRA寄存器中的128(0x0080)。CRB寄存器可以设置为任何值。

(2) DTC向量表设置

RXI中断的传输信息的起始地址在DTC的向量表中设置。

(3) ICU设置和DTC模块激活

将ICU.IELSRn.DTCE位设置为1，并将ICU.IELSRn.IELS[8:0]设置为SCI中断。必须在NVIC中启用中断。将DTCST.DTCST位设置为1。

(4) SCI设置

通过将SCI中的CCR0.RIE位设置为1来使能SCIn_RXI中断。如果在SCI接收操作期间发生接收错误，则接收停止。要管理此问题，请使用允许CPU接受接收错误中断的设置。

(5) DTC transfer

每次SCI完成1个字节的接收，就会产生一个SCIn_RXI中断来激活DTC。DTC将接收到的字节从SCI的RDR传输到SRAM，之后DAR寄存器递增，CRA寄存器递减。

(6) Interrupt handling

After 128 rounds of data transfer are complete and the value in the CRA register becomes 0, an SCIn_RXI interrupt request is generated for the CPU. Complete the process in the handling routine for this interrupt.

16.6.2 Chain transfer

This section provides an example of chain transfer by the DTC and describes its use in the output of pulses by the General PWM Timer (GPT). You can use chain transfer to transfer PWM timer compare data and change the period of the PWM timer for the GPT.

For the first of the chain transfers, normal transfer mode is specified for transfer to the GPTm.GTCCRC register (m = 320 to 329). For the second transfer, normal transfer mode is specified for transfer to the GPTm.GTCCRE register (m = 320 to 329). For the third transfer of the chained transfer, normal transfer mode for transfer to the GPTm.GTPBR register (m = 320 to 329) is specified. This is because clearing of the activation source and generation of an interrupt on completion of the specified number of transfers are restricted to the third of the chain transfers, that is, transfer while MRB.CHNE = 0.

The following example shows how to use the counter overflow interrupt with the GPT320.GTPR register as an activating source for the DTC.

(1) First transfer information setting

Set up transfer to the GPT320.GTCCRC register.

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up chain transfer (MRB.CHNE = 1 and MRB.CHNS = 0).
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTCCRC register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(2) Second transfer information setting

Set up for transfer to the GPT320.GTCCRE register.

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up chain transfer (MRB.CHNE = 1, MRB.CHNS = 0).
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTCCRE register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(3) Third transfer information set

Set up transfer to the GPT320.GTPBR register.

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up single data transfer per interrupt (MRB.CHNE = 0, MRB.DISEL = 0). The MRB.DTS bit can be set to any value.
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTPBR register.
6. Set the CRA register to the size of the data table. The CRB register can be set to any value.

(6) 中断处理

在128轮数据传输完成且CRA寄存器中的值变为0后，向CPU产生SCIn_RXI中断请求。完成该中断处理程序中的处理。

16.6.2 链式转移

本节提供了一个DTC链传输的示例，并描述了它在General输出脉冲中的使用
PWM定时器(GPT)。您可以使用链式传输来传输PWM定时器比较数据并更改GPT的PWM定时器的周期。

对于第一个链传输，指定正常传输模式以传输到GPTm.GTCCRC寄存器（m=320到329）。对于第二次传输，指定正常传输模式以传输到GPTm.GTCCRE寄存器（m=320到329）。对于链式传输的第三次传输，指定传输到GPTm.GTPBR寄存器（m=320到329）的正常传输模式。这是因为在完成指定数量的传输时清除激活源和产生中断仅限于链传输的第三个，即在MRB.CHNE=0时传输。

以下示例显示如何使用GPT320.GTPR寄存器的计数器溢出中断作为DTC的激活源。

(1) 首次转账信息设置

设置传输到GPT320.GTCCRC寄存器。

1.在MRA寄存器中，选择源地址的递增(MRA.SM[1:0]=10b)。

2.将传输设置为正常传输模式（MRA.MD[1:0]=00b）和字长传输（MRA.SZ[1:0]=10b）。

3.在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]=00b）并设置链传输（MRB.CHNE=1和MRB.CHNS=0）。

4.将SAR寄存器设置为数据表的首地址。

5.将DAR寄存器设置为GPT320.GTCCRC寄存器的地址。

6.将CRAH和CRAL寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(2) 二转信息设置

设置传输到GPT320.GTCCRE寄存器。

1.在MRA寄存器中，选择源地址的递增(MRA.SM[1:0]=10b)。

2.将传输设置为正常传输模式（MRA.MD[1:0]=00b）和字长传输（MRA.SZ[1:0]=10b）。

3.在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]=00b）并设置链传输（MRB.CHNE=1，MRB.CHNS=0）。

4.将SAR寄存器设置为数据表的首地址。

5.将DAR寄存器设置为GPT320.GTCCRE寄存器的地址。

6.将CRAH和CRAL寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(3) 三转信息集

设置传输到GPT320.GTPBR寄存器。

1.在MRA寄存器中，选择源地址的递增(MRA.SM[1:0]=10b)。

2.将传输设置为正常传输模式（MRA.MD[1:0]=00b）和字长传输（MRA.SZ[1:0]=10b）。

3.在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]=00b）并设置每次中断的单次数据传输（MRB.CHNE=0，MRB.DISEL=0）。MRB.DTS位可以设置为任何值。

4.将SAR寄存器设置为数据表的首地址。

5.将DAR寄存器设置为GPT320.GTPBR寄存器的地址。

6.将CRA寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(4) Transfer information assignment

Place the transfer information for use in the transfer to the GPT320.GTPBR immediately after the transfer control information for use in the GPT320.GTCCRC and GPT320.GTCCRE registers.

(5) DTC vector table

In the DTC vector table, set the address where the transfer control information for use in transfer to the GPT320.GTCCRC and GPT320.GTCCRE registers starts.

(6) ICU setting and DTC module activation

1. Set the ICU.IELSRn.DTCE bit associated with the GPT320 counter overflow interrupt.
2. Set the ICU.IELSRn.IELS[8:0] bits and specify the GPT320 counter overflow.
3. Set the DTCST.DTCST bit to 1.

(7) GPT settings

1. Set the GPT320.GTIOR register so that the GTCCRA and GTCCRB registers operate as output compare registers.
2. Set the default PWM timer compare values in the GPT320.GTCCRA and GPT320.GTCCRB registers and the next PWM timer compare values in the GPT320.GTCCRC and GPT320.GTCCRE registers.
3. Set the default PWM timer period values in the GPT320.GTPR register and the next PWM timer period values in the GPT320.GTPBR register.
4. Set 1 to the output bit in PmnPFS.PDR, and set 00011b to the Peripheral Select bits in PmnPFS.PSEL[4:0].

(8) GPT activation

Set the GPT320.GTSTR.CSTRT bits to 1 to start the GPT320.GTCNT counter.

(9) DTC transfer

Each time a GPT320 counter overflow is generated with the GPT320.GTPR register, the next PWM timer compare values are transferred to the GPT320.GTCCRC and GPT320.GTCCRE registers. The setting for the next PWM timer period is transferred to the GPT320.GTPBR register.

(10) Interrupt handling

After the specified rounds of data transfer are complete, for example when the value in the CRA register for GPT transfer becomes 0, a GPT320 counter overflow interrupt request is issued for the CPU. Complete the process for this interrupt in the handling routine.

16.6.3 Chain Transfer when Counter = 0

The second data transfer is performed only when the transfer counter is set to 0 in the first data transfer, and the first data transfer information is repeatedly changed in the second transfer. Chain transfer enables transfers to be repeated 256 times or more.

The following procedure shows an example of configuring a 1-KB input buffer, where the input buffer is set so that its lower address starts with 0x00. Figure 16.13 shows a chain transfer when the counter = 0.

1. Set the normal transfer mode to input data for the first data transfer. Set the following:
   (a) Transfer source address = fixed.
   (b) CRA register = 0x0200 (512) times.
   (c) MRB.CHNE bit = 1 (chain transfer is enabled).
   (d) MRB.CHNS bit = 1 (chain transfer is performed only when the transfer counter is 0).
   (e) MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
2. Prepare the upper 8-bit address of the start address at every 512 times of the transfer destination address for the first data transfer in different area such as the flash. For example, when setting the input buffer to 0x8000 to 0x83FF, prepare 0x82 and 0x80.

(4) 转移信息分配

将用于传输到GPT320.GTPBR的传输信息放置在GPT320.GTCCRC和GPT320.GTCCRE寄存器中使用的传输控制信息之后。

(5) DTC向量表

在DTC向量表中，设置用于传输到GPT320.GTCCRC和GPT320.GTCCRE寄存器的传输控制信息的起始地址。

(6) ICU设置和DTC模块激活

1.设置与GPT320计数器溢出中断相关的ICU.IELSRn.DTCE位。

2.设置ICU.IELSRn.IELS[8:0]位并指定GPT320计数器溢出。

3.将DTCST.DTCST位设置为1。

(7) GPT settings

1.设置GPT320.GTIOR寄存器，使GTCCRA和GTCCRB寄存器作为输出比较寄存器运行。

2.在GPT320.GTCCRA和GPT320.GTCCRB寄存器中设置默认PWM定时器比较值，在GPT320.GTCCRC和GPT320.GTCCRE寄存器中设置下一个PWM定时器比较值。

3.在GPT320.GTPR寄存器中设置默认PWM定时器周期值，在GPT320.GTPBR寄存器中设置下一个PWM定时器周期值。

4.将PmnPFS.PDR中的输出位设置为1，并将PmnPFS.PSEL[4:0]中的外设选择位设置为00011b。

(8) GPT activation

将GPT320.GTSTR.CSTRT位设置为1以启动GPT320.GTCNT计数器。

(9) DTC transfer

每次使用GPT320.GTPR寄存器产生GPT320计数器溢出时，下一个PWM定时器比较值被传送到GPT320.GTCCRC和GPT320.GTCCRE寄存器。下一个PWM定时器周期的设置被传送到GPT320.GTPBR寄存器。

(10)中断处理

在指定轮次的数据传输完成后，例如当GPT传输的CRA寄存器中的值变为0时，会向CPU发出GPT320计数器溢出中断请求。在处理例程中完成该中断的处理。

16.6.3 Counter=0时的链式转移

仅当在第一次数据传输中将传输计数器设置为0时才执行第二次数据传输，并且在第二次传输中重复改变第一数据传输信息。链式转移使转移可以重复256次或更多。

以下过程显示了配置1KB输入缓冲区的示例，其中输入缓冲区设置为使其低地址从0x00开始。图16.13显示了当计数器=0时的链式传输。

1.将普通传输模式设置为第一次数据传输的输入数据。设置以下内容：
   (a) 传输源地址=固定。
   (b) CRA寄存器=0x0200(512)次。
   (c) MRB.CHNE位=1（启用链式传输）。
   (d) MRB.CHNS位=1（仅当传输计数器为0时才执行链式传输）。
   (e) MRB.DISEL位=0（指定数据传输完成时向CPU产生中断请求）。

2.在flash等不同区域的第一次数据传输中，每512次传输目标地址准备起始地址的高8位地址。比如设置输入缓冲区为0x8000到0x83FF时，准备0x82和0x80。

3. For the second data transfer:
   (a) Set the repeat transfer mode (with transfer source and destination address = fixed.) to reset the transfer counter of the first data transfer.
   (b) Specify the CRA register in the first transfer information area for the transfer destination.
   (c) Set the MRB.CHNE bit = 1 (chain transfer is enabled).
   (d) Set the MRB.CHNS bit = 0 (select continuous chain transfer).
   (e) Set the MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
   (f) CRA register = 0x0101 (The transfer count is 1).
4. For the third data transfer:
   (a) Set the repeat transfer mode (with the source as the repeat area) to reset the transfer destination address of the first data transfer.
   (b) Specify the upper 8 bits of the DAR register in the first transfer information area for the transfer destination.
   (c) Set the MRB.CHNE bit = 0 (chain transfer is disabled).
   (d) Set the MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
   (e) When setting the input buffer to 0x8000 to 0x83FF, also set the transfer counter to 2.
5. The first data transfer is performed by an interrupt 512 times. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the transfer counter of the first data transfer to 0x0200. The lower 8 bits of the transfer destination address and the transfer counter of the first data transfer becomes 0x0200.
6. The second data transfer is performed by an interrupt 1 times. When the transfer counter of the first data transfer becomes 0, the third data transfer starts. Set the upper 8 bits of the transfer destination address of the first data transfer to 0x82. The lower 8 bits of the transfer destination address becomes 0x00 and the transfer counter of the first data transfer becomes 0x0200.
7. In succession, the first data transfer is performed by an interrupt 512 times as specified for the first data transfer. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the transfer counter of the first data transfer to 0x0200. The lower 8 bits of the transfer destination address and the transfer counter of the first data transfer becomes 0x0200.
8. The second data transfer is performed by an interrupt 1 times. When the transfer counter of the first data transfer becomes 0, the third data transfer starts. Set the upper 8 bits of the transfer destination address of the first data transfer to 0x80. The lower 8 bits of the transfer destination address becomes 0x00 and the transfer counter of the first data transfer becomes 0x0200.
9. Steps 5 to 8 are repeated indefinitely. Because the second data transfer is in repeat transfer mode, no interrupt request to the CPU is generated.

3.对于第二次数据传输：
   (a) 设置重复传输模式（传输源和目标地址=固定）以重置第一次数据传输的传输计数器。
   (b) 在传输目标的第一个传输信息区域中指定CRA寄存器。
   (c) 设置MRB.CHNE位=1（启用链式传输）。
   (d) 设置MRB.CHNS位=0（选择连续链传输）。
   (e) 设置MRB.DISEL位=0（当指定的数据传输完成时向CPU产生一个中断请求）。
   (f) CRA寄存器=0x0101（传输计数为1）。
4.对于第三次数据传输：
   (a) 设置重复传输模式（以源为重复区域）重置第一次数据传输的传输目标地址。
   (b) 在传输目标的第一个传输信息区域中指定DAR寄存器的高8位。
   (c) 设置MRB.CHNE位=0（禁用链传输）。
   (d) 设置MRB.DISEL位=0（当指定的数据传输完成时向CPU产生一个中断请求）。
   (e) 将输入缓冲区设置为0x8000到0x83FF时，还要将传输计数器设置为2。
5.第一次数据传输由中断执行512次。当第一次数据传输的传输计数器变为0，第二次数据传输开始。将第一次数据传输的传输计数器设置为0x0200。第一次数据传输的传输目标地址和传输计数器的低8位变为0x0200。
6.第二次数据传输由中断执行1次。当第一次数据传输的传输计数器变为0，开始第三次数据传输。将第一次数据传输的传输目标地址的高8位设置为0x82。传送目标地址的低8位变为0x00，第一次数据传送的传送计数器变为0x0200。
7.接连地，第一次数据传输由中断执行512次，如为第一次数据传输指定的那样。当第一次数据传输的传输计数器变为0时，第二次数据传输开始。将第一次数据传输的传输计数器设置为0x0200。第一次数据传输的传输目标地址和传输计数器的低8位变为0x0200。
8.第二次数据传输由中断执行1次。当第一次数据传输的传输计数器变为0，开始第三次数据传输。将第一次数据传输的传输目标地址的高8位设置为0x80。传送目标地址的低8位变为0x00，第一次数据传送的传送计数器变为0x0200。
9.步骤5到8无限重复。因为第二次数据传输是重复传输模式，所以不会产生对CPU的中断请求。

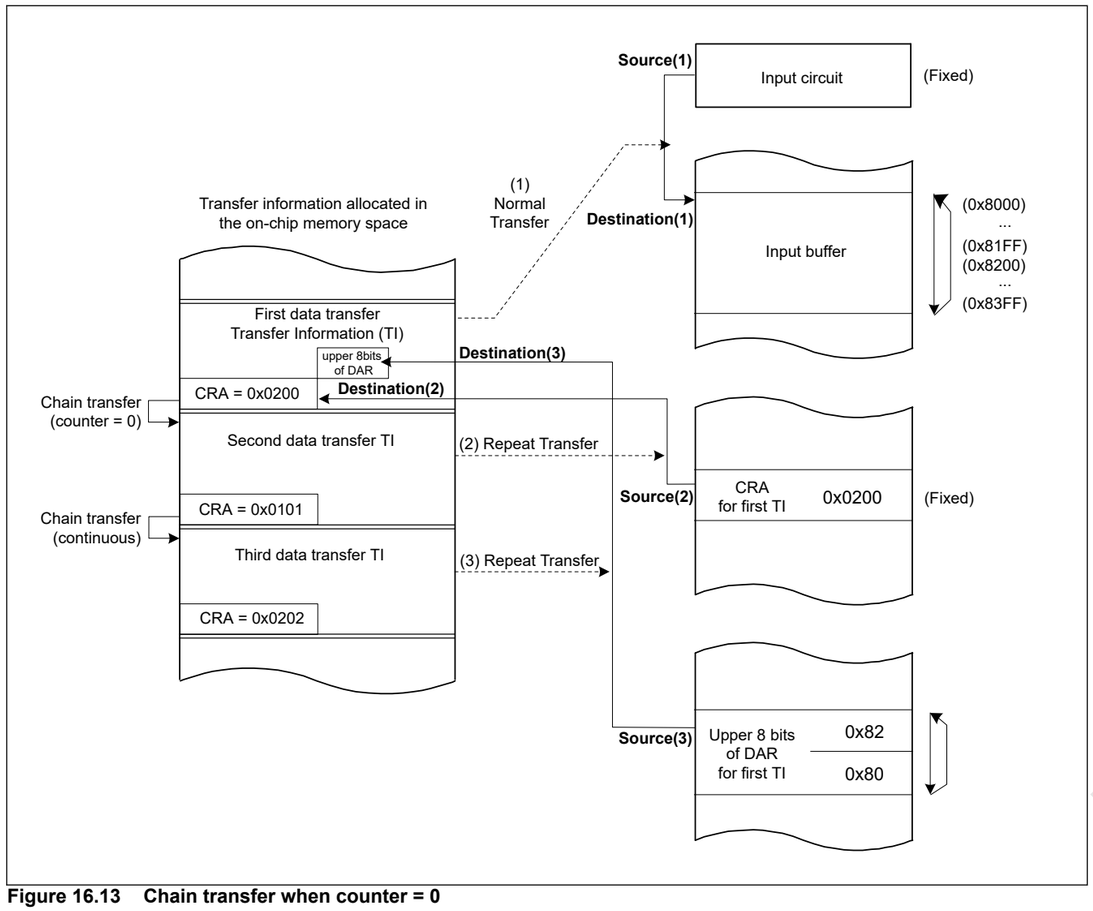


Figure 16.13 Chain transfer when counter = 0

16.7 Processing on DTC Transfer Error

If the access error occurs during DTC transfer, the DTC immediately stops access during transfer. To stop only the vector number that caused the error, inform the vector number that caused the error to the ICU and clear the corresponding ICU setting. After that, if there is a request other than the vector number which caused the error, it will be re-arbitration as it is. The condition under which the transfer error occurs is indicated when TrustZone Filter in DTC detects a violation.

The error response is informed to ICU when the transfer error occurs. ICU clears the ICU.IELSRn of the corresponding vector number which caused the transfer error. Furthermore, it generates an error response detection interrupt to notify that an error has occurred by DMAC/DTC transfer. (section 16.8.2. Interrupt Request of Transfer Error). Write back to SRAM is not performed.

When the Master TrustZone Filter error occurs, the Slave TrustZone error occurs or the Master MPU error occurs, it is possible to confirm the error information of DTC by selecting NMI. The DTC error vector register is cleared by selecting reset. Under the conditions where NMI is generated due to transfer error in DTC, two interrupts(NMI and DMA_TRANSERR) are generated. In this case, NMI always responds first.

The error response detection interrupt request (DMA_TRANSERR) occurs when the Slave Bus error or the Illegal Access error occurs. Furthermore, it occurs after NMI when the error response detection interrupt request (DMA_TRANSERR) is not cleared in NMI handler.

section 16.7.1. Processing on NMI handler describes how to confirm the error information of the DTC in the NMI handler. section 16.7.2. Processing on Error response detection interrupt request (DMA_TRANSERR) handler describes how to confirm the error information of the DTC in the DMA_TRANSERR handler.

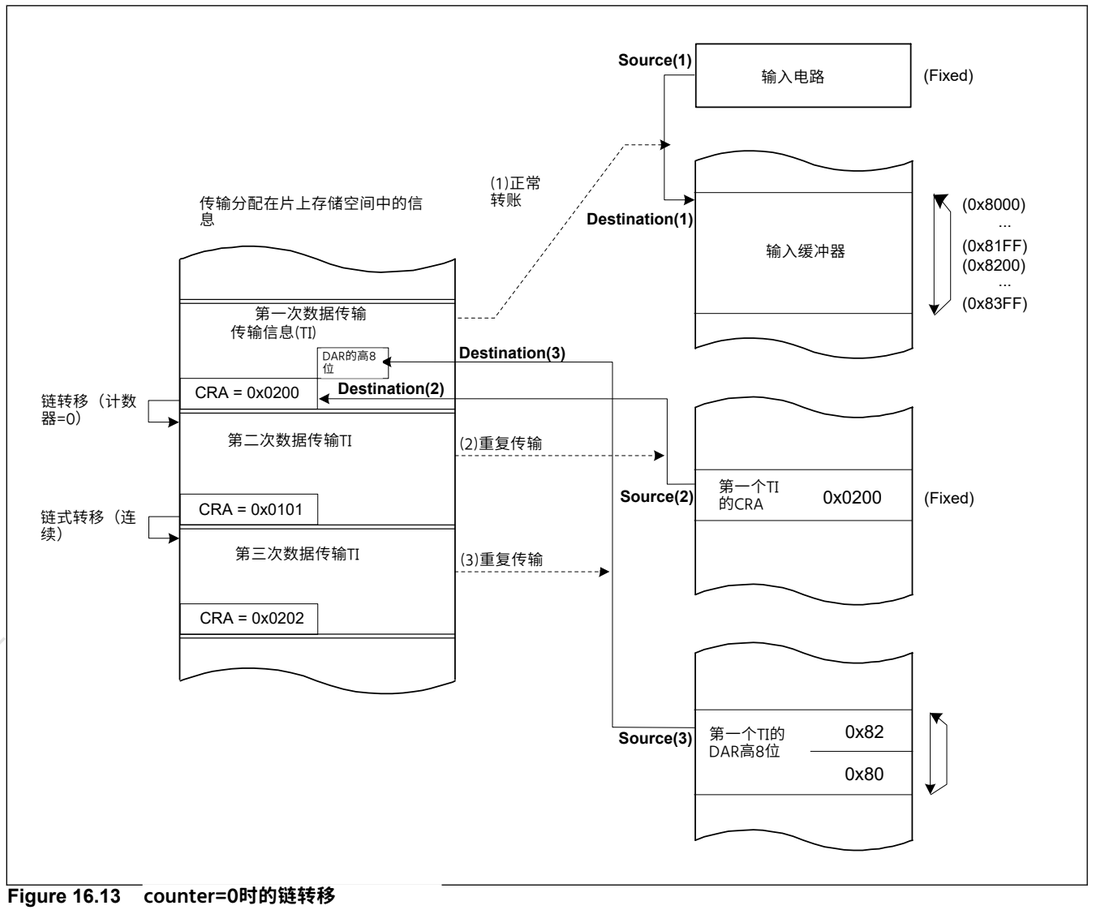


Figure 16.13 counter=0时的链转移

16.7 DTC传输错误的处理

如果在DTC传输过程中发生访问错误，则DTC会在传输过程中立即停止访问。要仅停止导致错误的向量编号，请将导致错误的向量编号通知ICU并清除相应的ICU设置。之后，如果有引起错误的向量号以外的请求，将按原样重新仲裁。当DTC中的TrustZone过滤器检测到违规时，会指示发生传输错误的条件。

当发生传输错误时，将错误响应通知给ICU。ICU清除导致传输错误的相应向量号的ICU.IELSRn。此外，它会生成错误响应检测中断，以通知DMACDTC传输发生错误。（第16.8.2节。传输错误的中断请求）。不执行回写到SRAM。

当MasterTrustZoneFilter发生错误、SlaveTrustZone错误或MasterMPU错误时，可以通过选择NMI来确认DTC的错误信息。通过选择复位清除DTC错误向量寄存器。在由于DTC中的传输错误而产生NMI的情况下，会产生两个中断（NMI和DMA_TRANSERR）。在这种情况下，NMI总是首先响应。

当发生SlaveBus错误或IllegalAccess错误时，会发生错误响应检测中断请求(DMA_TRANSERR)。此外，当NMI处理程序中未清除错误响应检测中断请求(DMA_TRANSERR)时，它会在NMI之后发生。

第16.7.1节。NMIhandler上的处理描述了如何在NMIhandler中确认DTC的错误信息。第16.7.2节。错误响应检测中断请求(DMA_TRANSERR)处理程序的处理描述了如何在DMA_TRANSERR处理程序中确认DTC的错误信息。

Interrupts and the error information generated due to transfer errors are shown in section 16.8.2. Interrupt Request of Transfer Error.

16.7.1 Processing on NMI handler

The cause of NMI due to the DMA transfer error is the Master TrustZone Filter error, the Slave TrustZone Filter error or the Master MPU error. When NMI occurs due to the DTC transfer error, the error response detection interrupt request (DMA_TRANSERR) will occur after the end of NMI handler. It is possible to confirm the cause of the error and the DTC vector number in which the error occurred. When NMI occurs, perform the necessary processing according to the flow described in the ICU chapter.

Figure 16.14 shows the flow for confirm the vector number that caused the Master TrustZone Filter Error in DTC

Figure 16.15 shows the flow for confirm the vector number that caused the Slave TrustZone Filter Error in DTC

Figure 16.16 shows the flow for confirm the vector number and Security Attribute that caused the Master MPU error in DTC

If completing all processing in NMI handler, it is possible to clear the error response detection interrupt request (DMA_TRANSERR) that occurs subsequently.

因传输错误产生的中断和错误信息见16.8.2节。中断请求
传输错误。

16.7.1 在NMI处理程序上处理

由于DMA传输错误导致NMI的原因是MasterTrustZoneFilter错误、SlaveTrustZoneFilter错误或
主控MPU错误。当由于DTC传输错误而发生NMI时，错误响应检测中断请求(DMA_TRANSERR)将在NMI处理程序结束后发生。可以确认错误的原因和发生错误的DTC向量编号。当发生NMI时，按照ICU章节中描述的流程进行必要的处理。

图16.14显示了在DTC中确认导致MasterTrustZoneFilterError的向量号的流程

图16.15显示了在DTC中确认导致SlaveTrustZoneFilterError的向量号的流程

图16.16显示了确认导致MasterMPU错误的向量号和安全属性的流程
DTC

如果完成NMI处理程序中的所有处理，则可以清除随后发生的错误响应检测中断请求(DMA_TRANSERR
)。

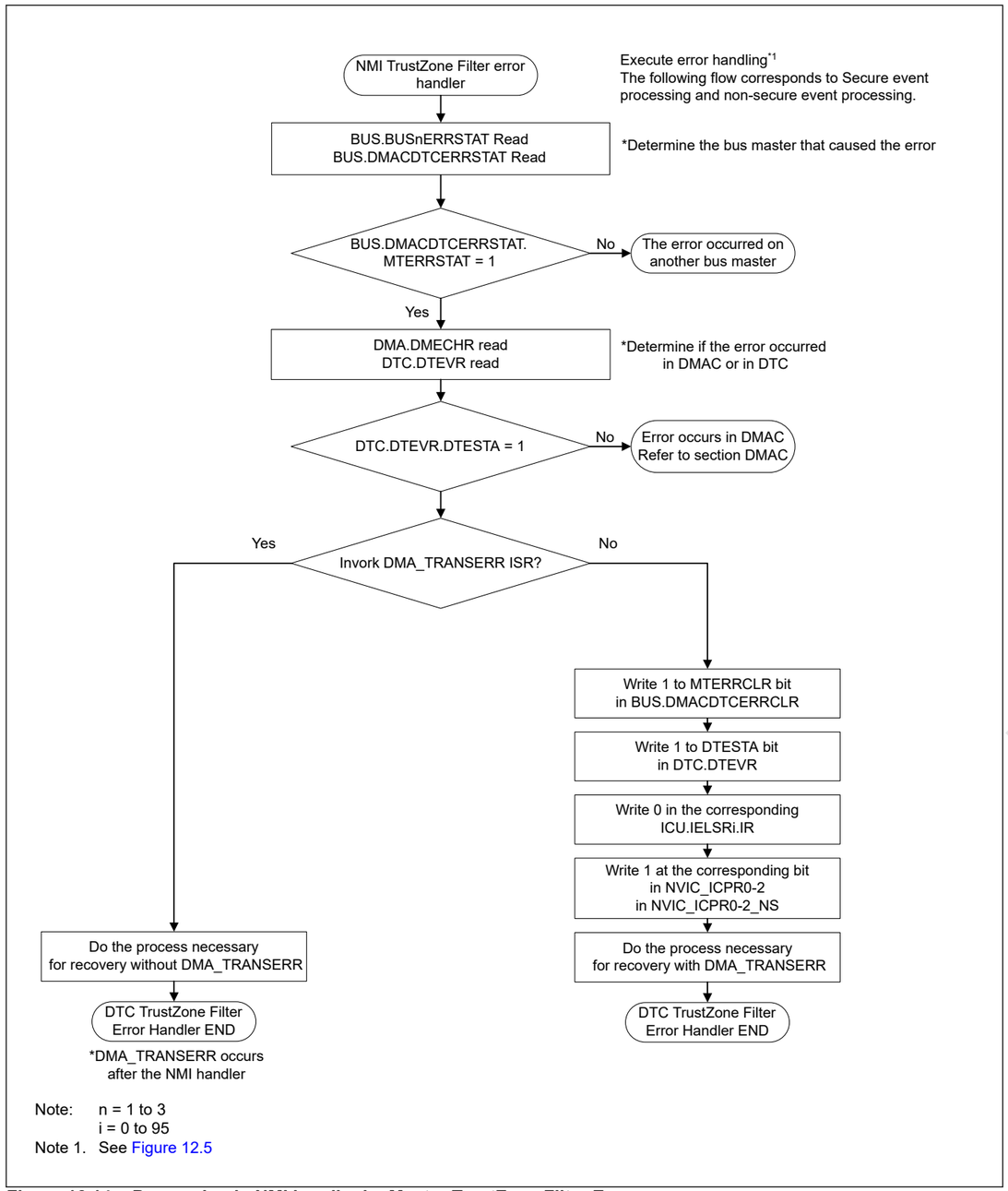


Figure 16.14 Processing in NMI handler by Master TrustZone Filter Error

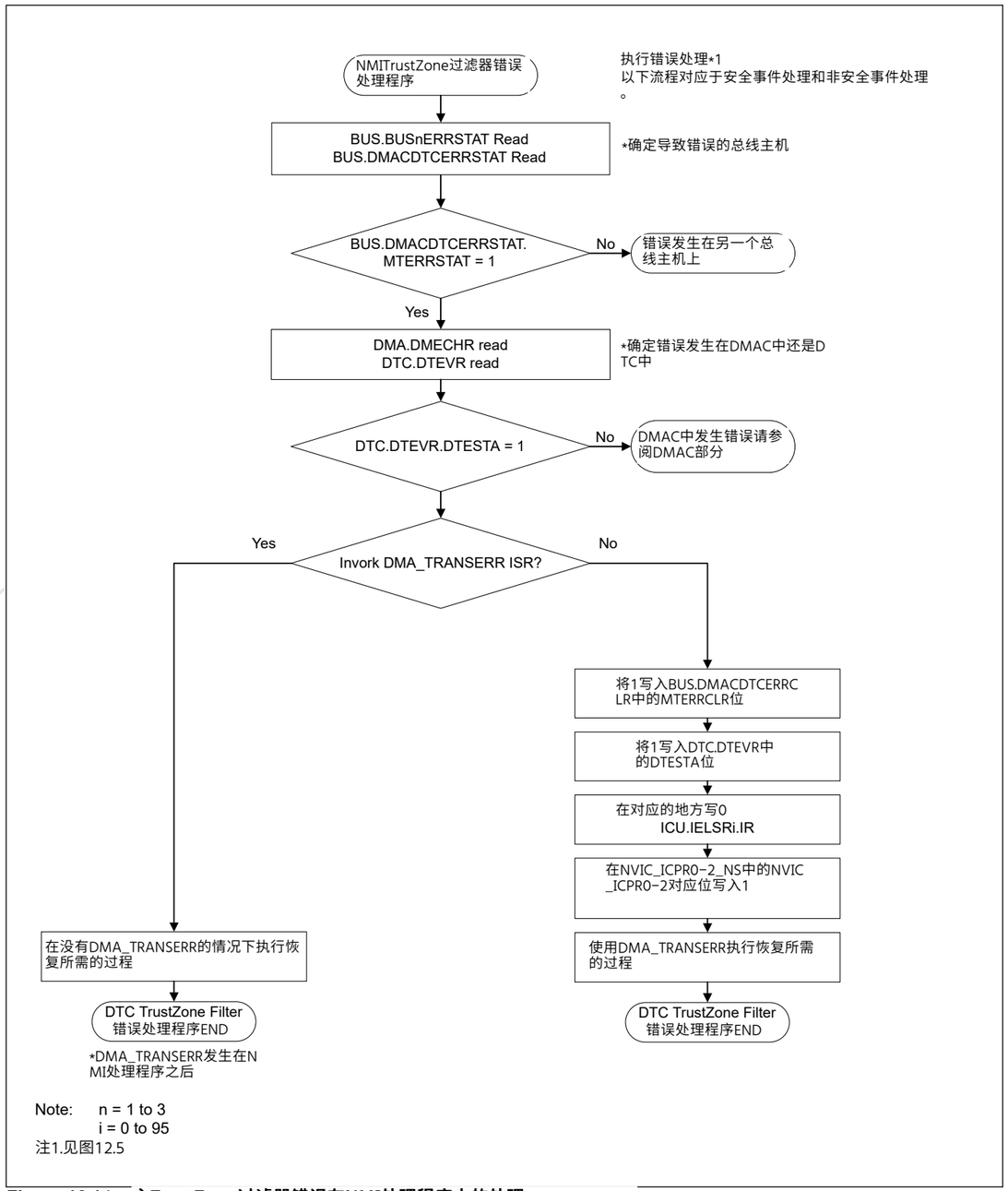


Figure 16.14 主TrustZone过滤器错误在NMI处理程序中的处理

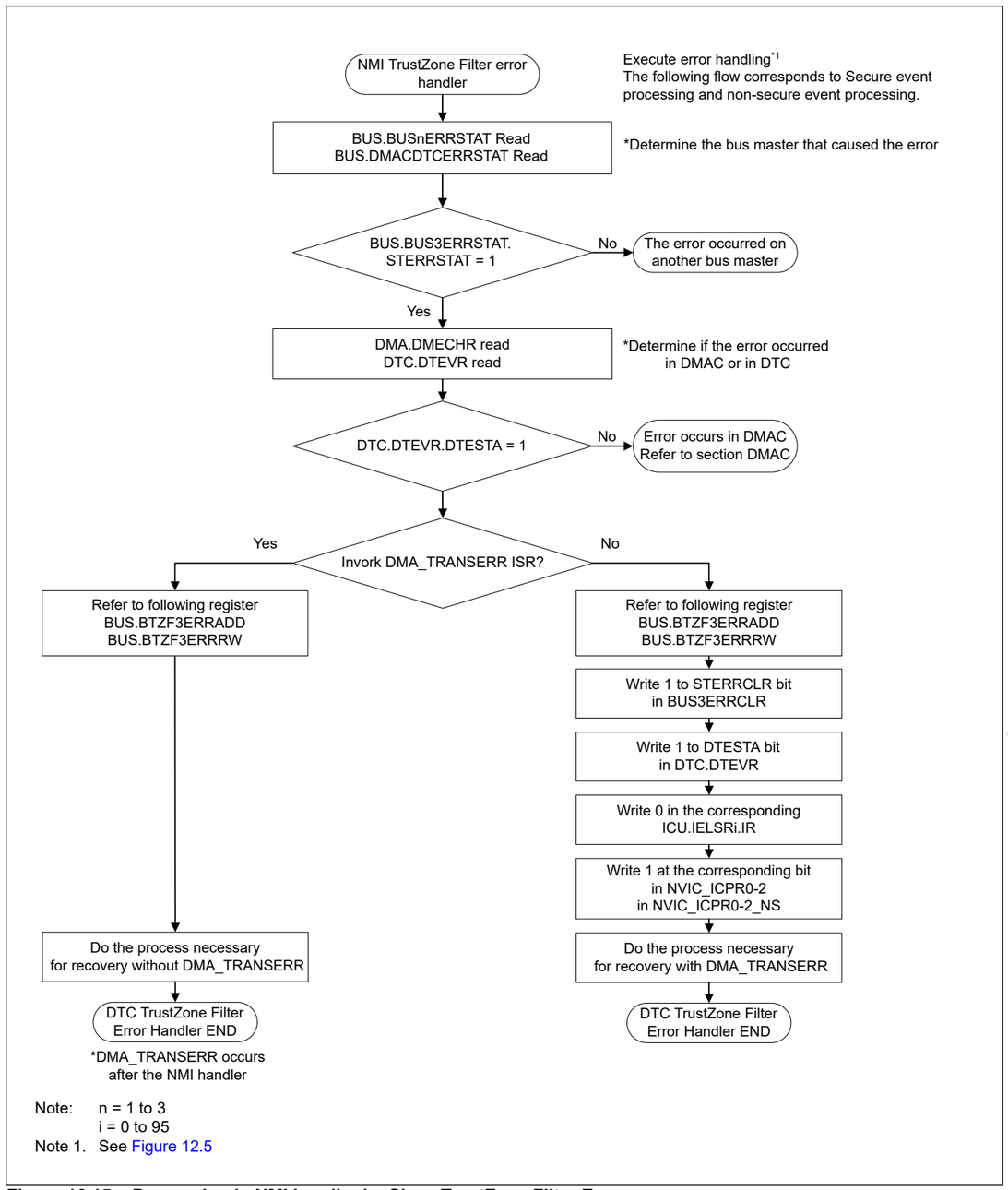


Figure 16.15 Processing in NMI handler by Slave TrustZone Filter Error

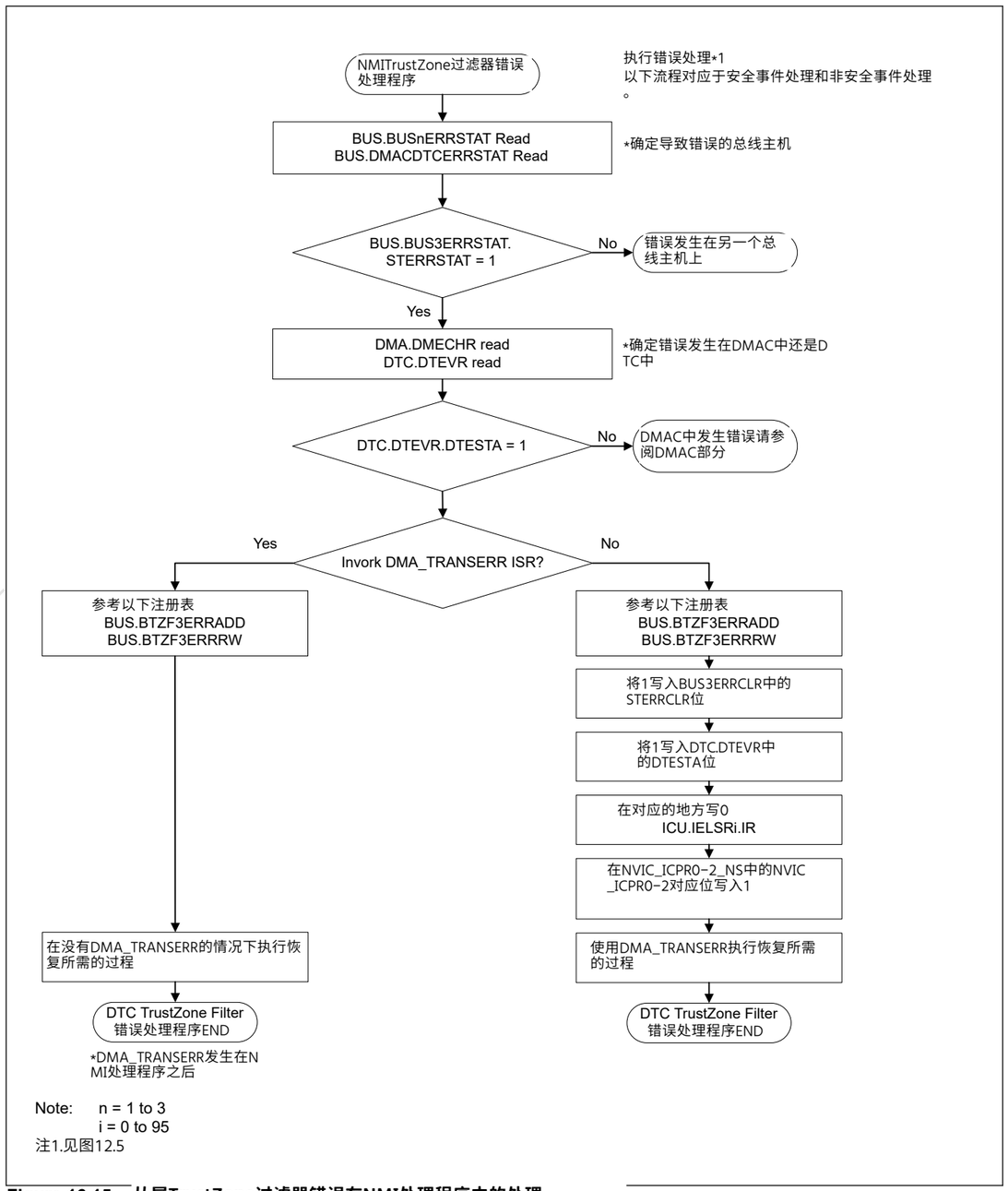


Figure 16.15 从属TrustZone过滤器错误在NMI处理程序中的处理

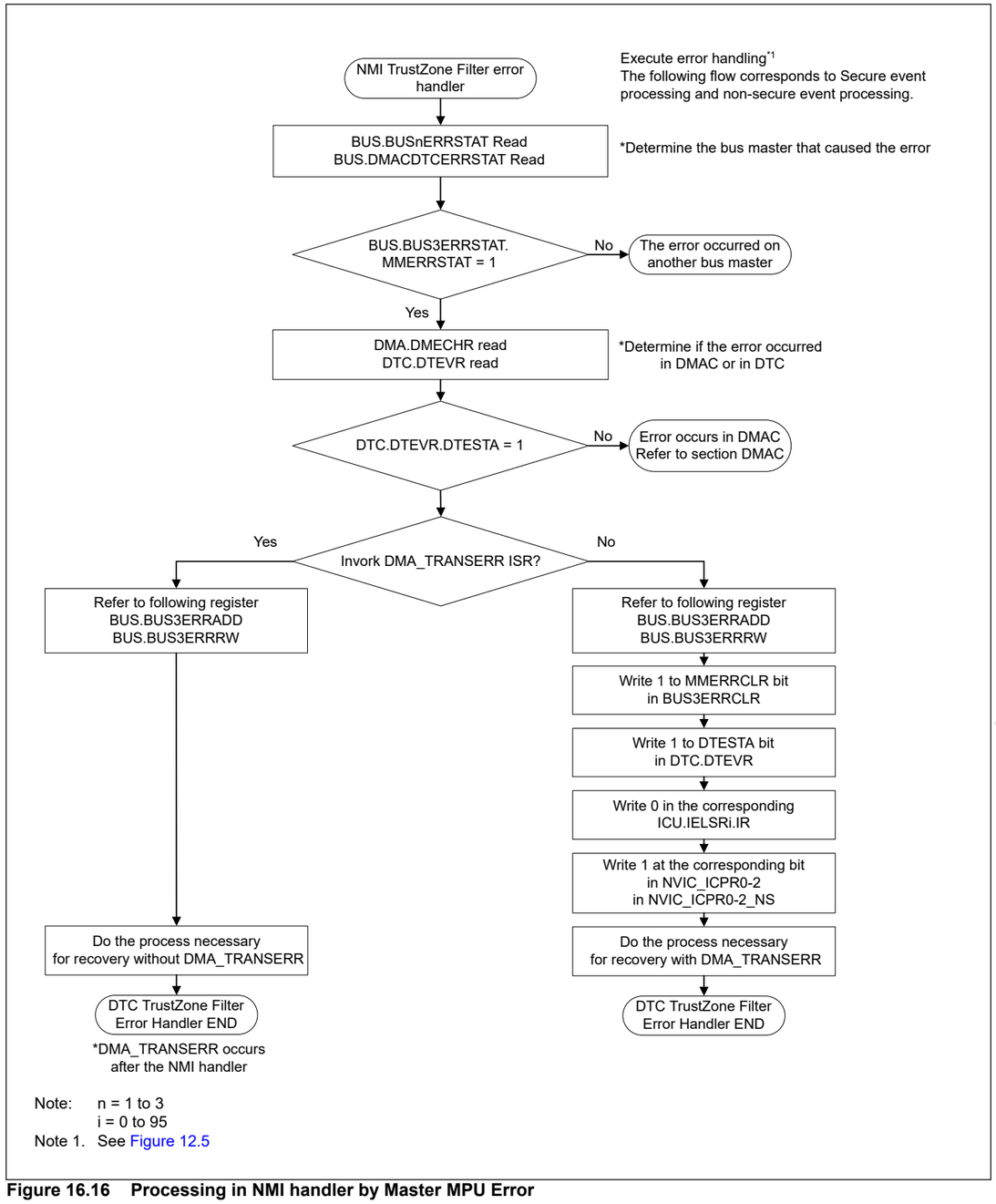


Figure 16.16 Processing in NMI handler by Master MPU Error

16.7.2 Processing on Error response detection interrupt request (DMA_TRANSERR) handler

The cause of error response detection interrupt request (DMA_TRANSERR) due to DMA transfer error is the Slave Bus Error or Illegal Access Error. Also, it occurs after the NMI handler error response detection interrupt request (DMA_TRANSERR) is not cleared by the NMI handler.

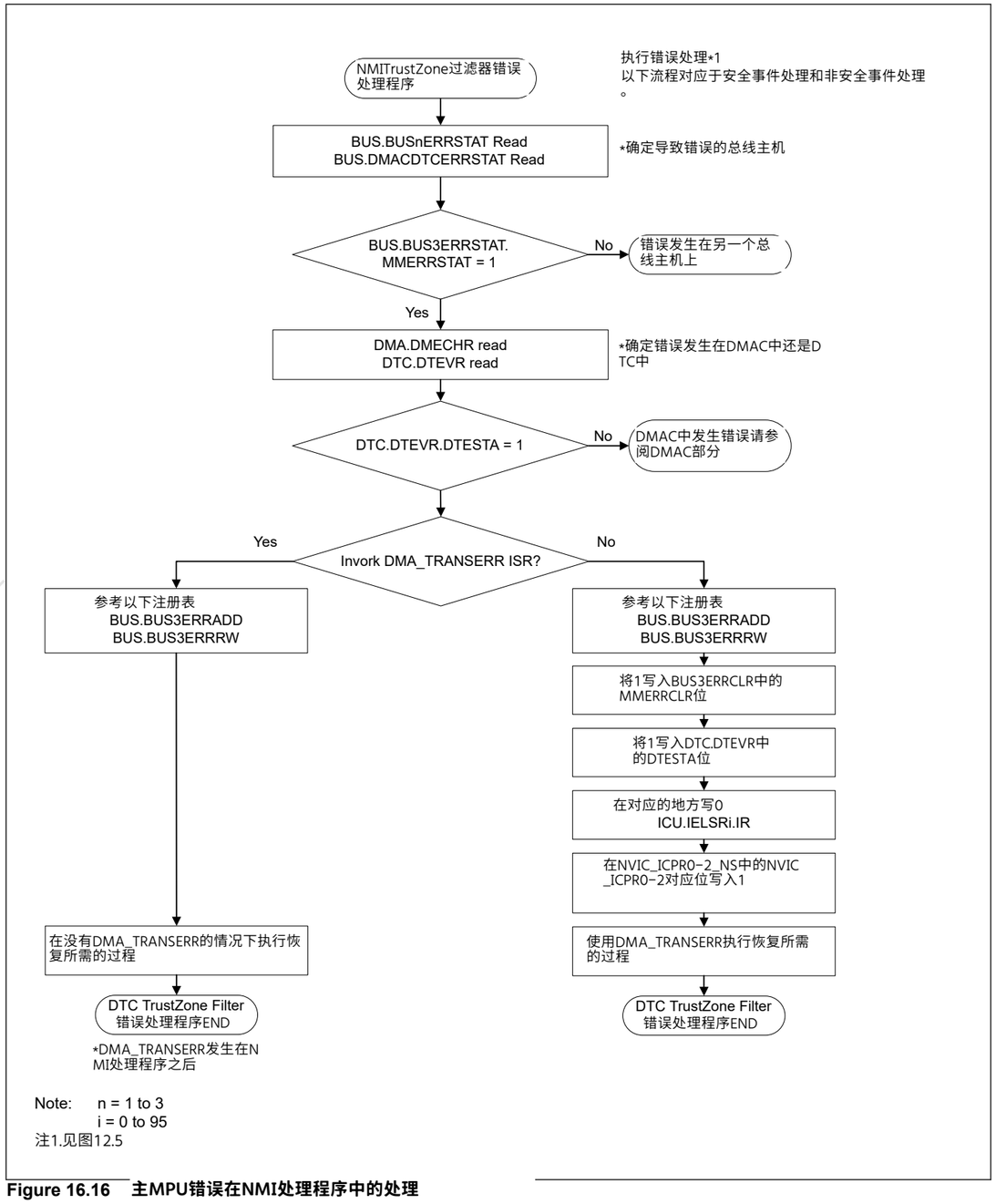


Figure 16.16 主MPU错误在NMI处理程序中的处理

16.7.2 错误响应检测中断请求(DMA_TRANSERR)处理程序的处理

由于DMA传输错误导致错误响应检测中断请求(DMA_TRANSERR)的原因是从总线错误或非法访问错误。此外，它发生在NMI处理程序错误响应检测中断请求(DMA_TRANSERR)未被NMI处理程序清除之后。

It is possible to confirm the cause of the error and the vector number of DTC in which the error occurred.

Error cause confirmation procedure is shown Figure 16.17.

Figure 16.18 shows the flow for confirm the vector number that caused the Master TrustZone Filter Error in DTC

Figure 16.19 shows the flow for confirm the vector number that caused the Slave TrustZone Filter Error in DTC

Figure 16.20 shows the flow for confirm the vector number and Security Attribute that caused the Master MPU Error in DTC

Figure 16.21 shows the flow for confirm the vector number and Security Attribute that caused the Slave Bus Error in DTC

Figure 16.22 shows the flow for confirm the vector number and Security Attribute that caused the Illegal Access Error in DTC

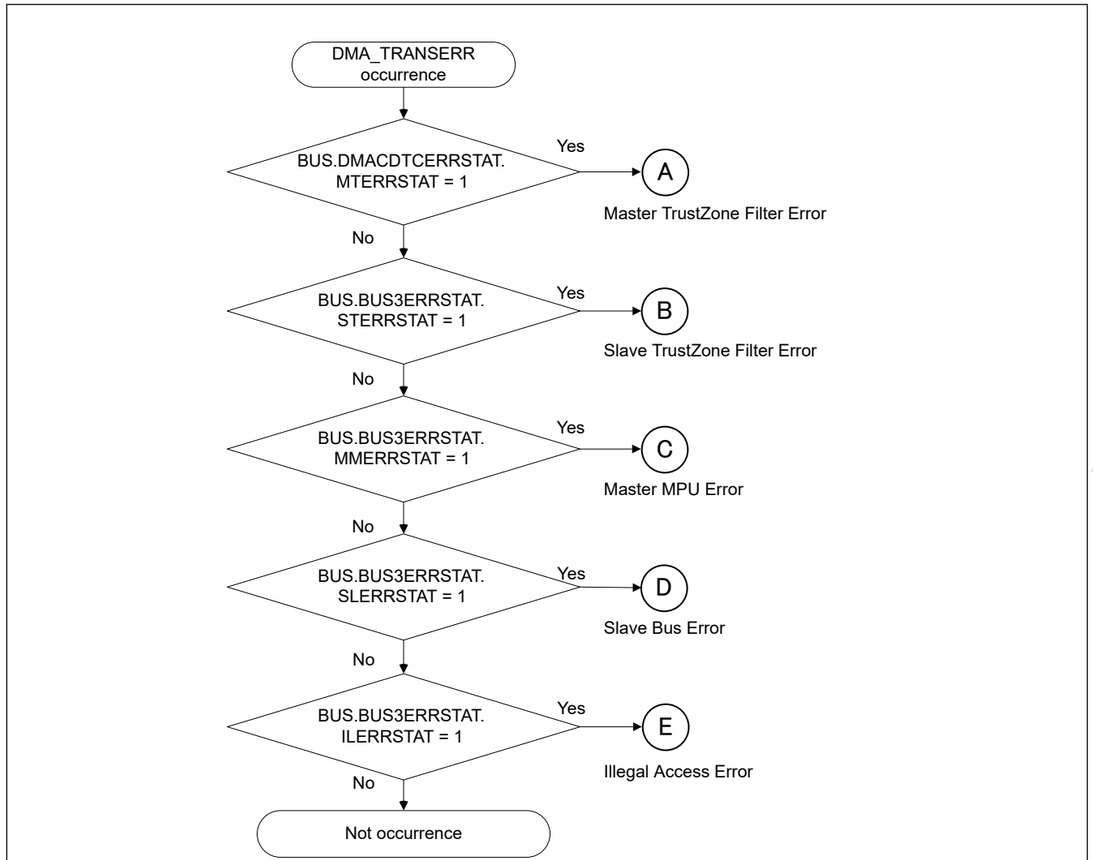


Figure 16.17 Transfer error factor judgment when the error response detection interrupt (DMA_TRANSERR) occurs

可以确认错误的原因和发生错误的DTC的向量号。

错误原因确认流程如图16.17所示。

图16.18显示了在DTC中确认导致MasterTrustZoneFilterError的向量号的流程

图16.19显示了在DTC中确认导致SlaveTrustZoneFilterError的向量号的流程

图16.20显示了确认导致MasterMPU错误的向量号和安全属性的流程
DTC

图16.21显示了在DTC中确认导致从总线错误的向量号和安全属性的流程

图16.22显示了确认导致非法访问错误的向量号和安全属性的流程
DTC

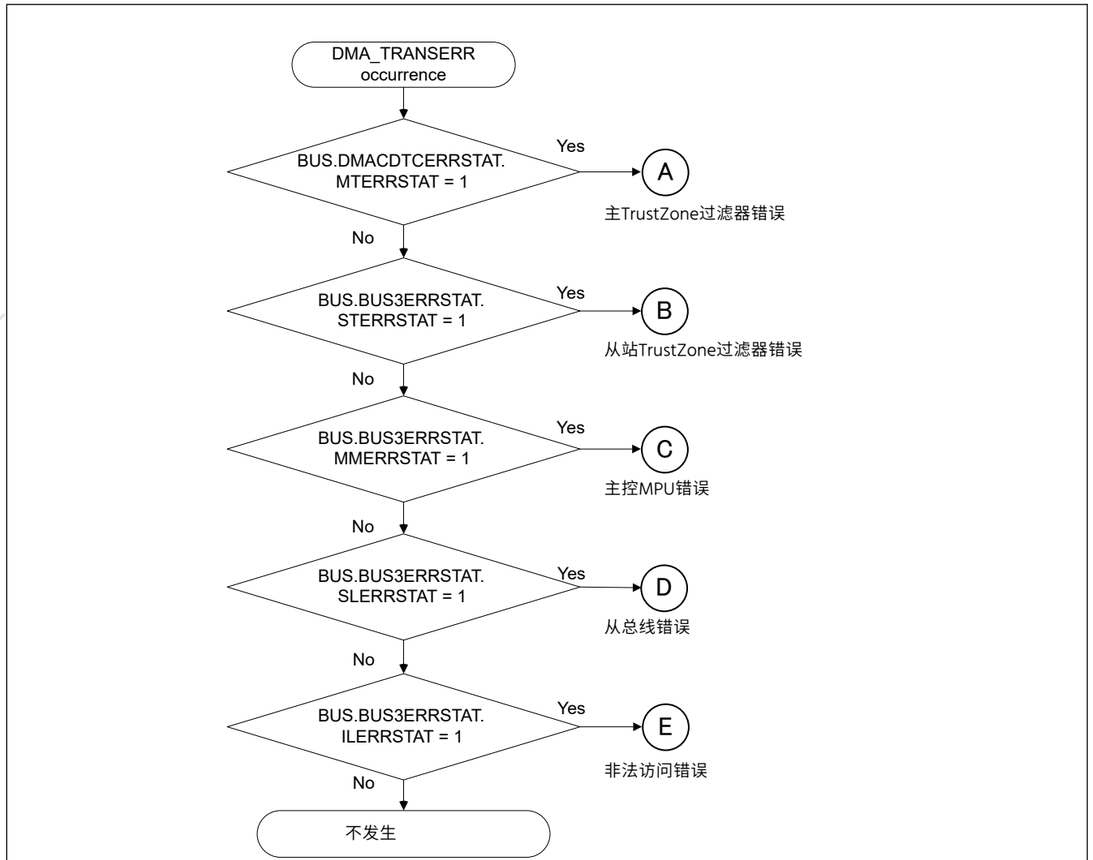


Figure 16.17 发生错误响应检测中断（DMA_TRANSERR）时的传输错误因素判断

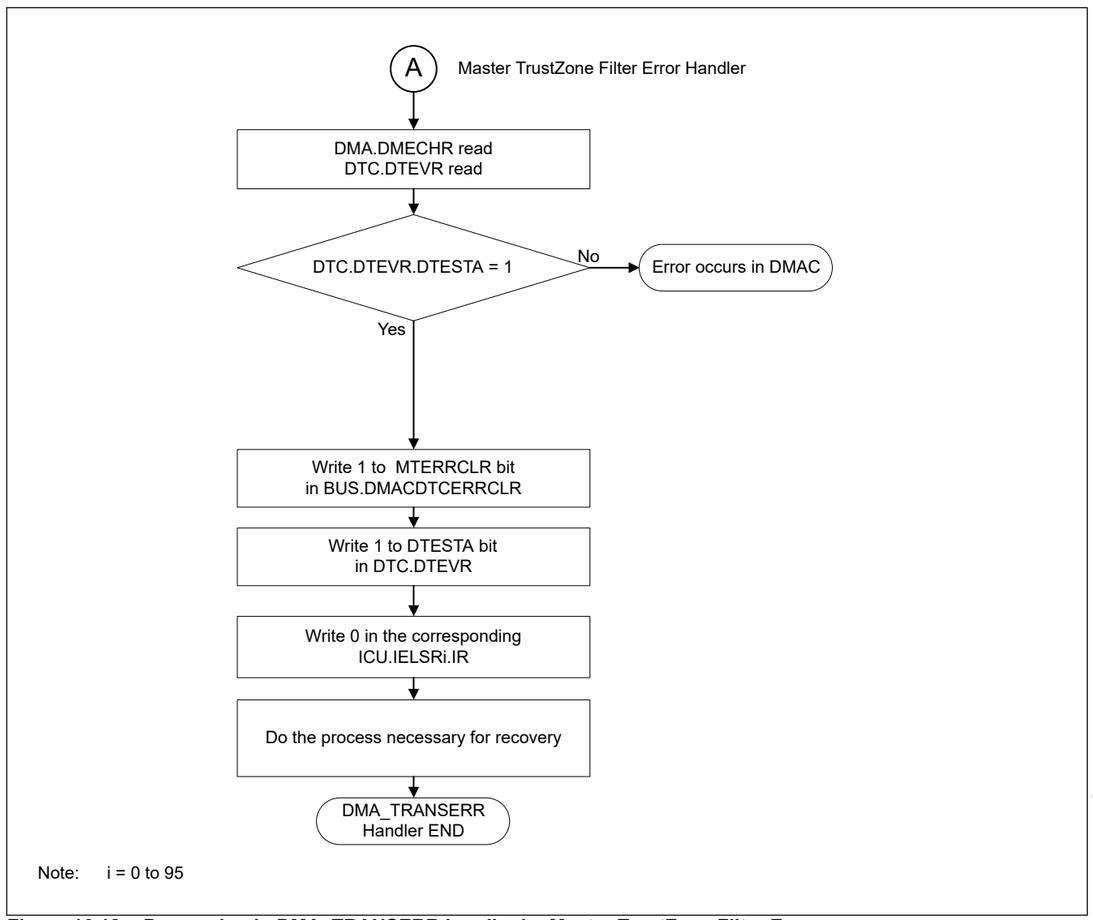


Figure 16.18 Processing in DMA_TRANSERR handler by Master TrustZone Filter Error

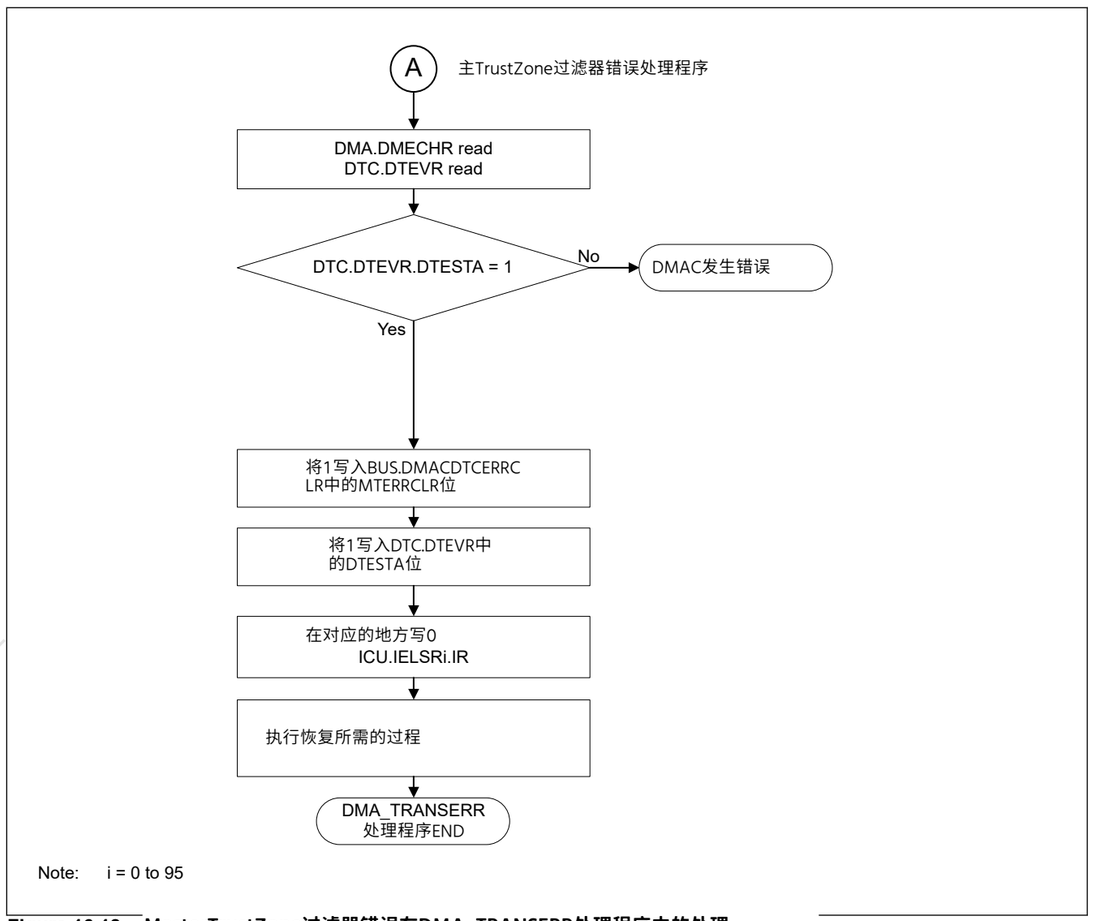


Figure 16.18 MasterTrustZone过滤器错误在DMA_TRANSERR处理程序中的处理

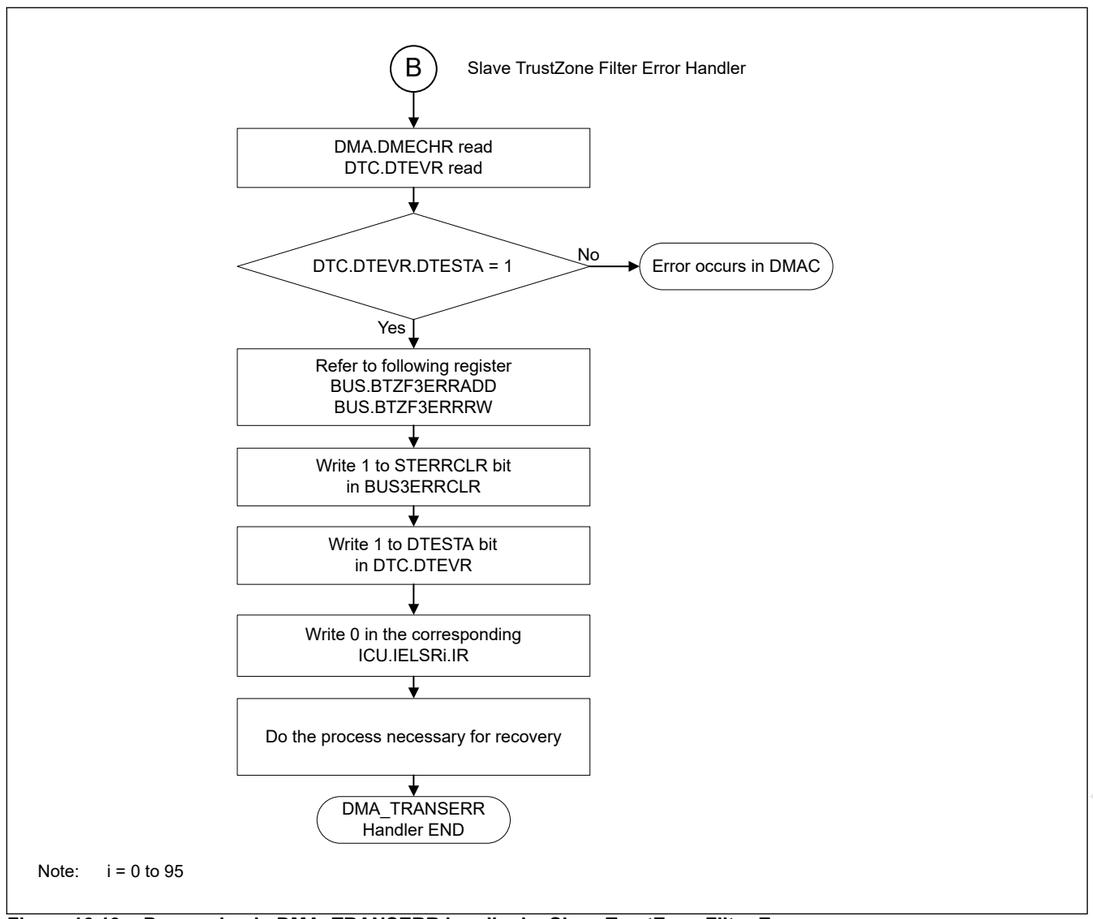


Figure 16.19 Processing in DMA_TRANSERR handler by Slave TrustZone Filter Error

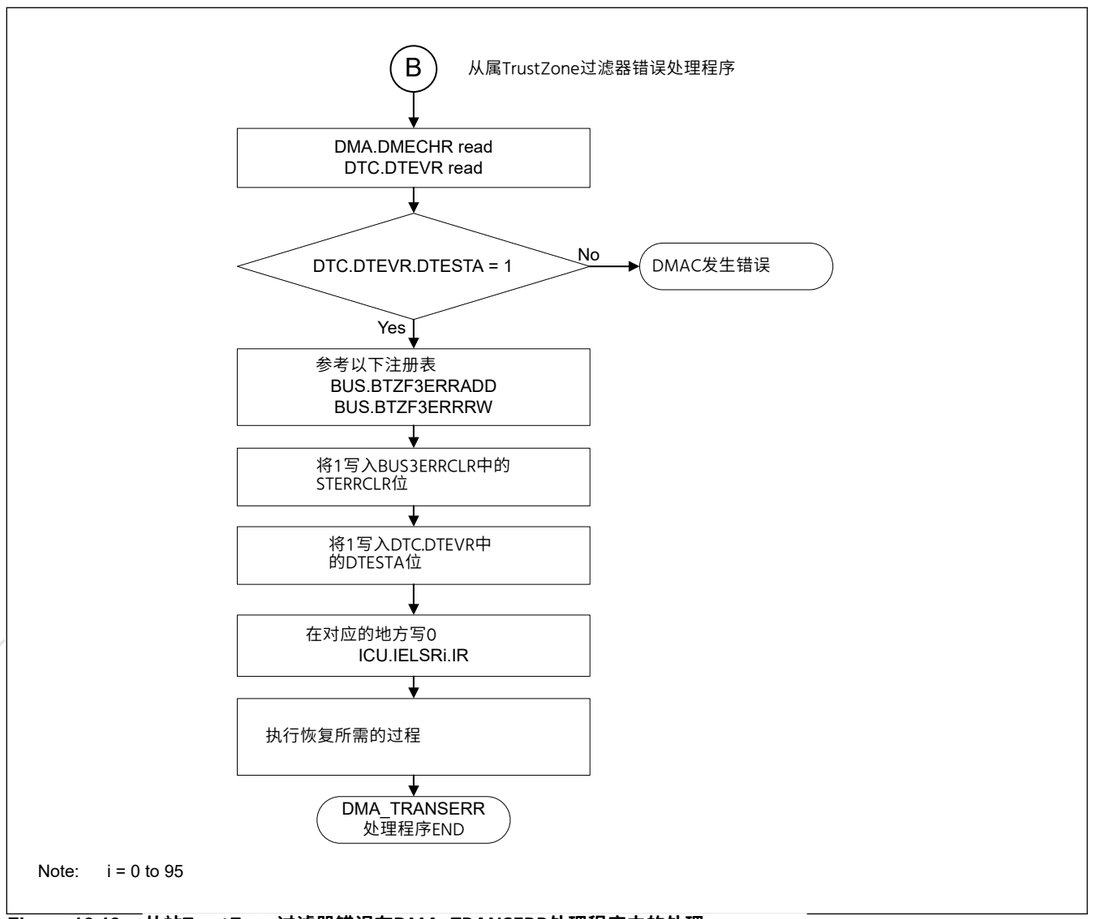


Figure 16.19 从站TrustZone过滤器错误在DMA_TRANSERR处理程序中的处理

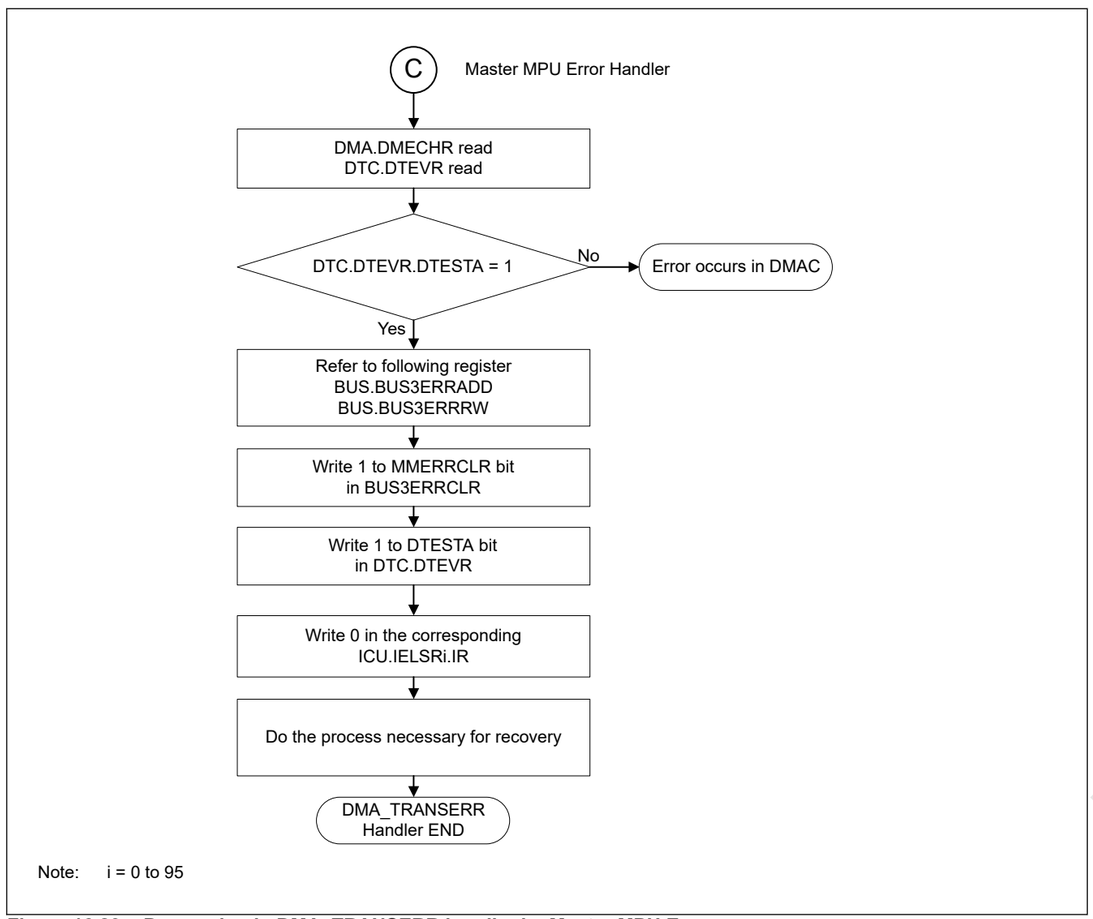


Figure 16.20 Processing in DMA_TRANSERR handler by Master MPU Error

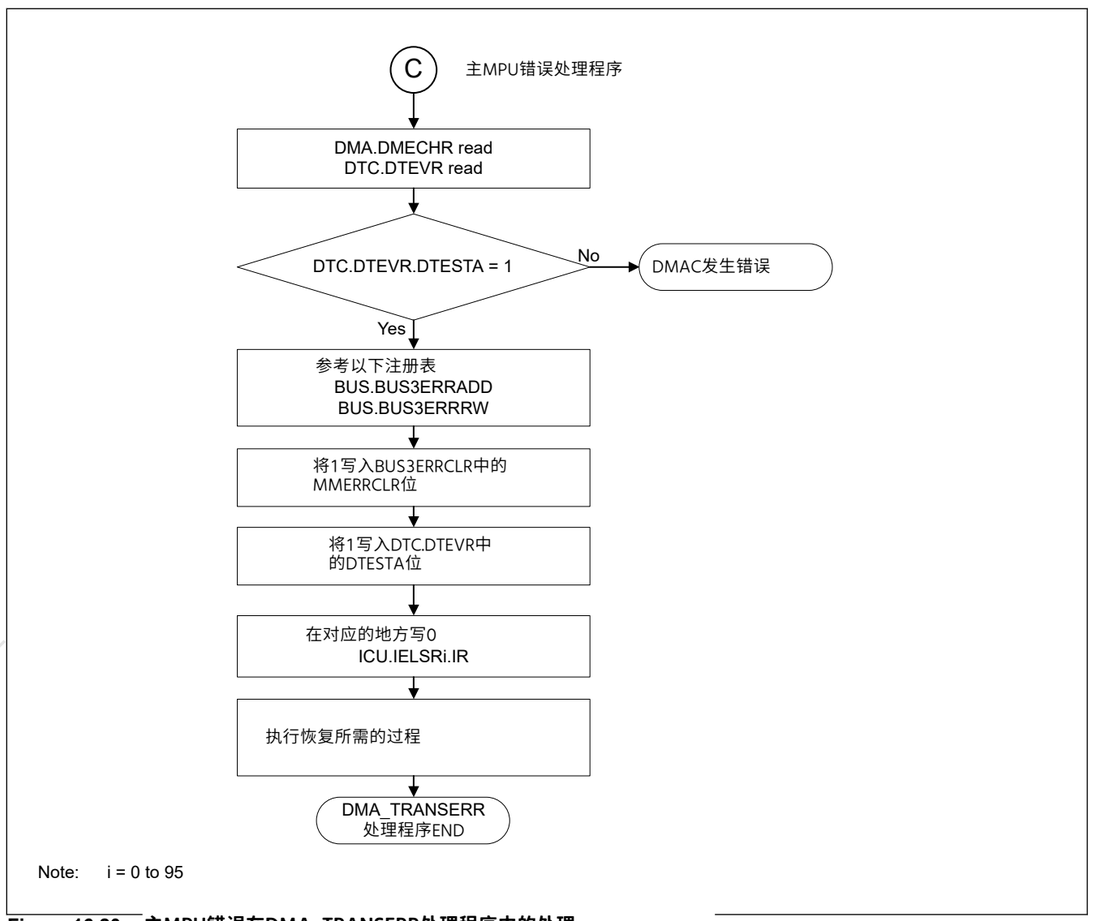


Figure 16.20 主MPU错误在DMA_TRANSERR处理程序中的处理

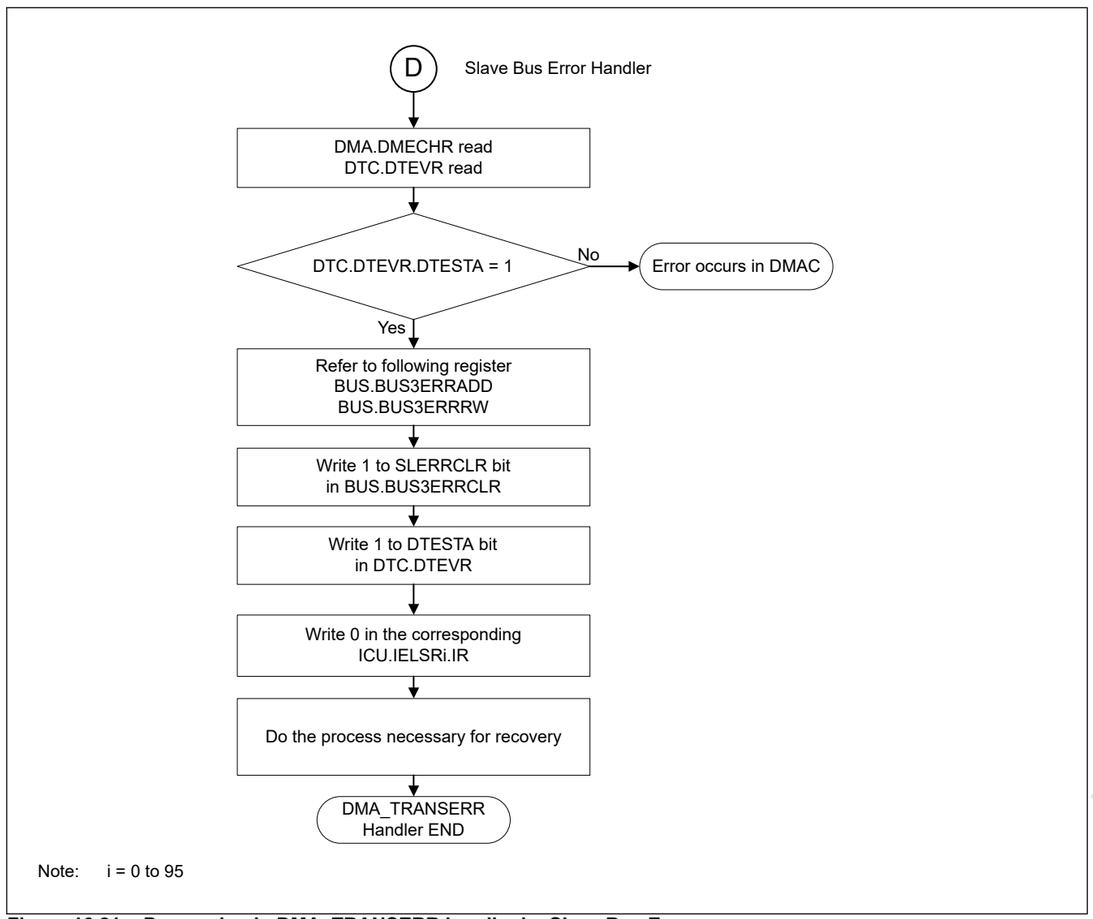


Figure 16.21 Processing in DMA_TRANSERR handler by Slave Bus Error

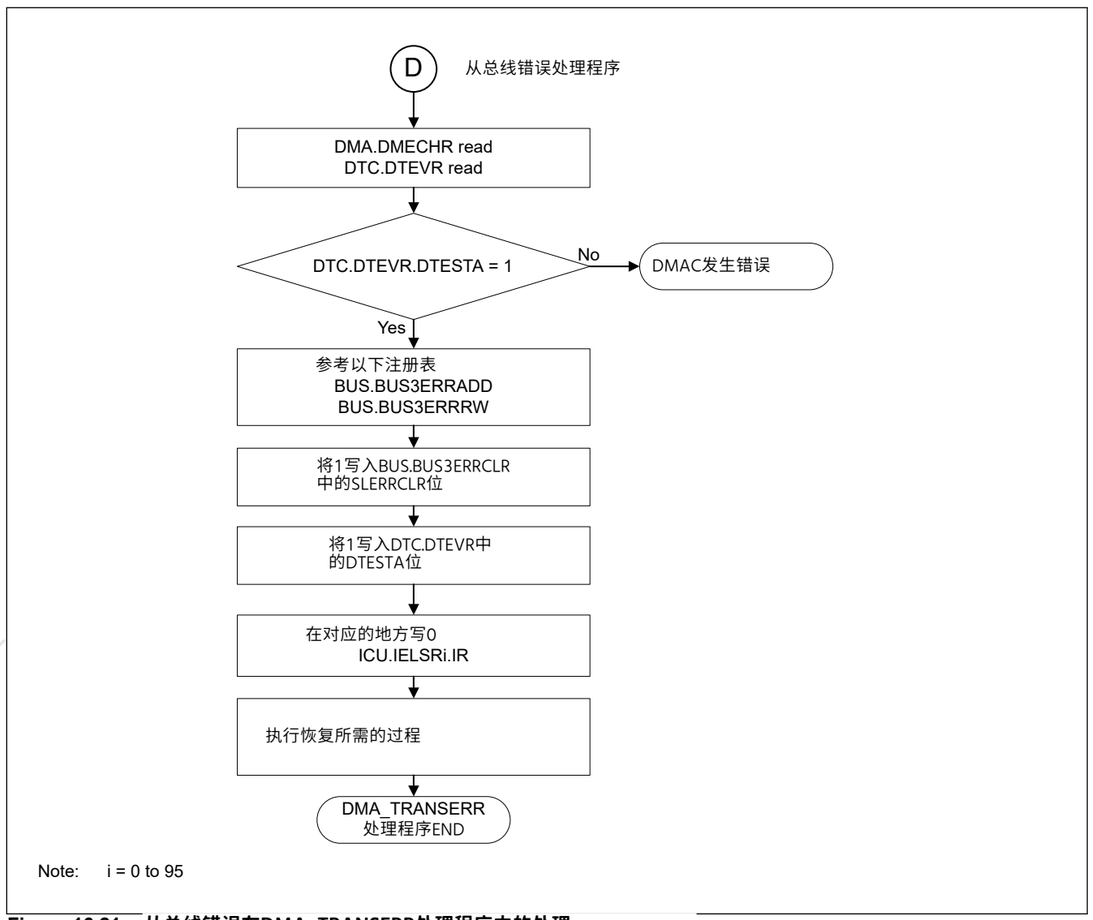


Figure 16.21 从总线错误在DMA_TRANSERR处理程序中的处理

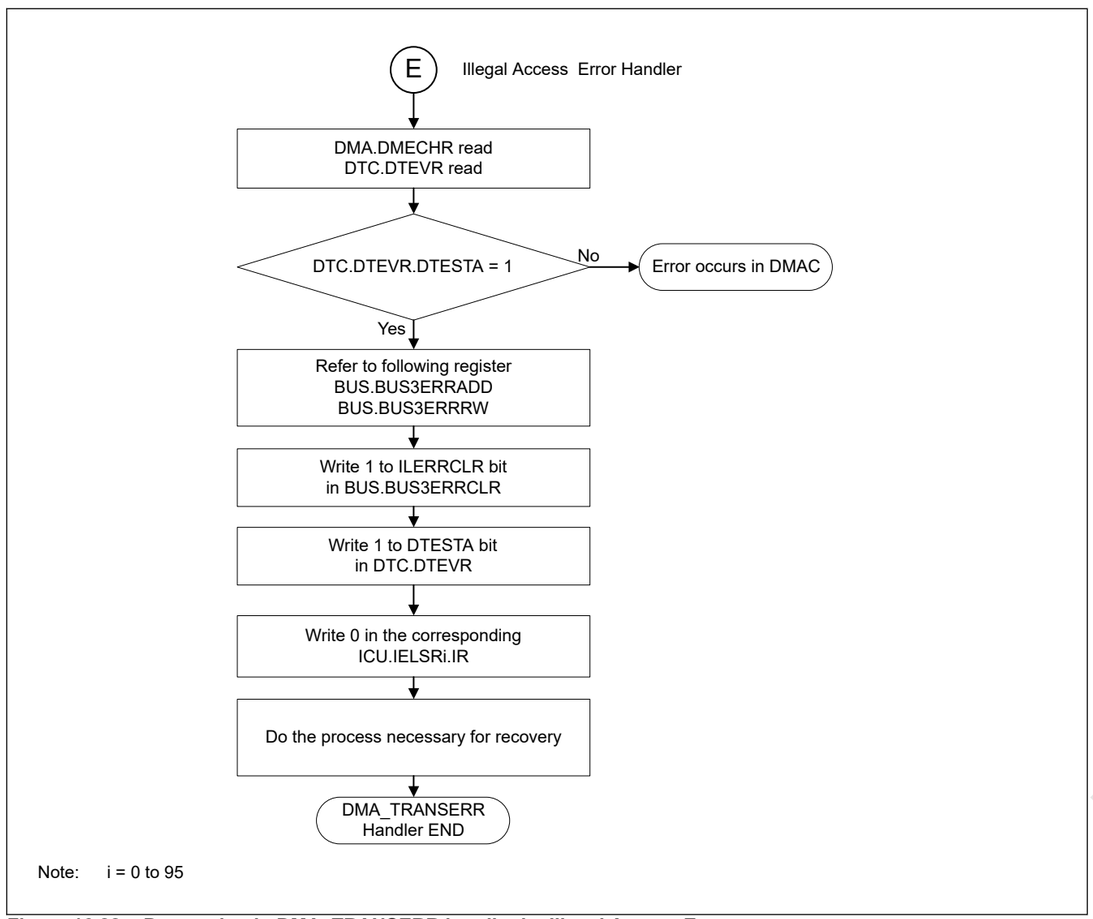


Figure 16.22 Processing in DMA_TRANSERR handler by Illegal Access Error

16.8 Interrupt

16.8.1 Interrupt Request of Transfer End

When the DTC completes data transfer of the specified count or when data transfer with MRB.DISEL set to 1 is complete, a DTC activation source generates an interrupt to the CPU. Two types of interrupt are available: interrupts triggered by a DTC activation (per channel) and an interrupt triggered by the event signal DTC_COMPLETE (common to all channels). Interrupts to the CPU are controlled according to the settings in the NVIC and the ICU.IELSRn.IELS[8:0] bits. See section 12, Interrupt Controller Unit (ICU). The DTC prioritizes activation sources by granting the smaller interrupt vector numbers higher priority. The priority of interrupts to the CPU is determined by the NVIC priority.

16.8.2 Interrupt Request of Transfer Error

The error response detection interrupt request (DMA_TRANSERR) is generated from the DMAC/DTC when the transfer error is detected during DTC transfer. The types of interrupts that occur when the DTC transfer error occurs are listed in the Table 16.10. The Table 16.10 also shows error information stored when a transfer error occurs.

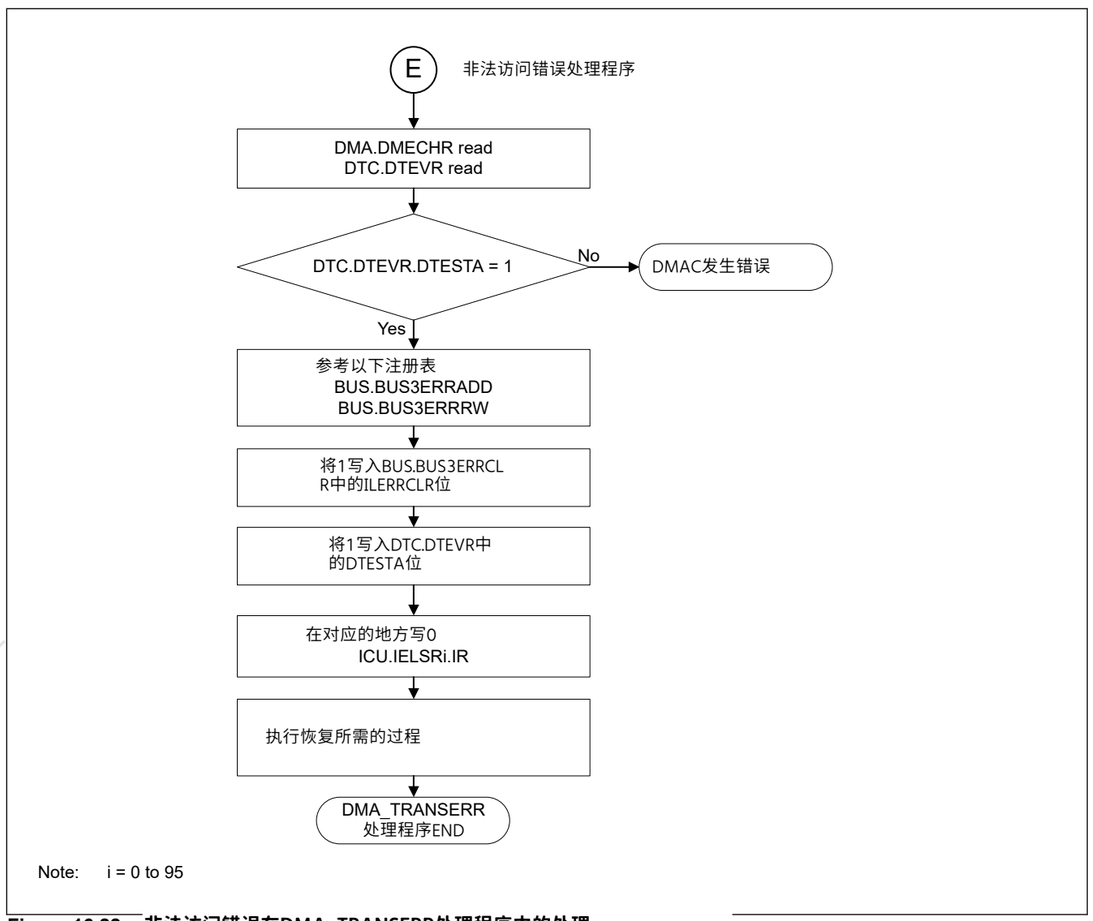


Figure 16.22 非法访问错误在DMA_TRANSERR处理程序中的处理

16.8 Interrupt

16.8.1 传输结束中断请求

当DTC完成指定计数的数据传输或MRB.DISEL设置为1的数据传输完成时，DTC激活源向CPU生成中断。有两种类型的中断可用：由DTC激活触发的中断（每个通道）和由事件信号DTC_COMPLETE触发的中断（所有通道通用）。CPU的中断根据NVIC和ICU.IELSRn.IELS[8:0]位中的设置进行控制。请参阅第12节，中断控制器单元(ICU)。DTC通过授予较小的中断向量编号较高的优先级来确定激活源的优先级。CPU中断的优先级由NVIC优先级决定。

16.8.2 传输错误中断请求

在DTC传输期间检测到传输错误时，从DMACDTC生成错误响应检测中断请求(DMA_TRANSERR)。发生DTC传输错误时发生的中断类型在表16.10中列出。表16.10还显示了发生传输错误时存储的错误信息。

Table 16.10 Interrupt and error information due to DMAC transfer error cause

Transfer error factor	NMI/RESET*1 Request	Interrupt Request	Bus Error Status	Error Address Error R/W	Error Channel Information
Master TrustZone Filter (in DMAC/DTC)	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.DMACDTCERRSTAT.MTERRSTAT*1	—	DTC.DTEVR
Slave TrustZone Filter	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.BUS3ERRSTAT.STERRSTAT*1	BUS.BTZF3ERRADD BUS.BTZF3ERRRW	DTC.DTEVR
Master MPU	ICU.NMISR.BUSMST	DMA_TRANSERR	BUS.BUS3ERRSTAT.MMERRSTAT	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR
Slave Bus Error	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.SLERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR
Illegal Access Error	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.ILERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR

Note 1. Interrupt generated, when NMI request selected as the operation after detection of the Master MPU error and The TrustZone Filter error. By confirming BUS.BUS3ERRSTAT and BUS.DMACDTCERRSTAT, judge whether it is the Master or the Slave.
Note 2. If the error response detection interrupt (DMA_TRANSERR) occurs and NMI of the Master MPU or NMI of the TrustZone Filter has not occurred, treat it as the Illegal address access error or the Slave Bus Error. It can be judged also by BUS.BUS3ERRSTAT and BUS. DMACDTCERRSTAT.

Note that if the bus error occurs when writing the last data of transfer, the transfer end event and the error response detection interrupt (DMA_TRANSERR) occurs.

16.9 Event Link

The DTC can produce an event link request on completion of one transfer request.

16.10 Low Power Consumption Function

Before transitioning to the module-stop function, Software Standby mode without Snooze mode transition, deep software standby mode, set the DTCST.DTCST bit to 0, and then perform the operations described in the following sections. The DTC is available in Snooze mode by setting the SYSTEM.SNZCR.SNZDTCEN bit to 1. See section 10, Low Power Modes.

(1) Module-stop function

Writing 1 to the MSTPCRA.MSTPA22 bit enables the module-stop function of the DTC. If a DTC transfer is in progress when 1 is written to the MSTPCRA.MSTPA22 bit, the transition to the module-stop state proceeds after the DTC transfer ends. While the MSTPCRA.MSTPA22 bit is 1, accessing the DTC registers is prohibited. Writing 0 to the MSTPCRA.MSTPA22 bit releases the DTC from the module-stop state.

(2) Software Standby mode, deep software standby mode

Use the settings described in section 10.7.1. Transitioning to Software Standby Mode or section 10.9.1. Transitioning to Deep Software Standby Mode.

If DTC transfer operations are in progress when the WFI instruction is executed, the transition to Software Standby mode or deep software standby mode follows the completion of the DTC transfer.

(3) Snooze Mode

When the snooze control circuit receives a snooze request in Software Standby mode, the MCU transfers to Snooze mode. See section 10.8.1. Transition to Snooze Mode. DTC operation in Snooze mode can be selected in the SYSTEM.SNZCR.SNZDTCEN bit. If DTC operation is enabled in Snooze mode, before transitioning to Software Standby mode, set the DTCST.DTCST bit to 1. To return to Software Standby mode through DTC, set SYSTEM.SNZEDCR0.DTCZRED or SYSTEM.SNZEDCR0.DTCNZRED to 1. See section 10.8.3. Returning from Snooze Mode to Software Standby Mode. SYSTEM.SNZEDCR0.DTCZRED enables or disables a snooze end request on completion of the last DTC transmission, detected on DTC transmission completion when CRA and CRB are 0. SYSTEM.SNZEDCR0.DTCNZRED enables or disables a snooze end request on a not last DTC transmission completion (CRA and CRB are not 0), detected on DTC transmission completion when CRA and CRB are not 0. The DTC activation request from the ICU is stopped during Software Standby mode but not stopped during Snooze mode.

Table 16.10 由于DMAC传输错误原因导致的中断和错误信息

传递误差因子	NMI/RESET*1 Request	中断请求	总线错误状态	错误地址 Error R/W	错误通道 Information
Master TrustZone Filter (in DMAC/DTC)	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.DMACDTCERRSTAT.MTERRSTAT*1	—	DTC.DTEVR
Slave TrustZone Filter	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.BUS3ERRSTAT.STERRSTAT*1	BUS.BTZF3ERRADD BUS.BTZF3ERRRW	DTC.DTEVR
Master MPU	ICU.NMISR.BUSMST	DMA_TRANSERR	BUS.BUS3ERRSTAT.MMERRSTAT	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR
从总线错误	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.SLERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR
非法访问错误	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.ILERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR

注意1.中断，当NMI请求在检测主MPU错误和Trustzone滤波器错误后选择为操作时中断。通过确认BUS.BUS3ERRSTAT和BUS.DMACDTCERRSTAT，判断是Master还是Slave。
注2.如果错误响应检测中断(DMA_TRANSERR)发生且MasterMPU的NMI或TrustZoneFilter的NMI未发生，则将其视为Illegaladdressaccesserror或SlaveBusError。也可以通过BUS.BUS3ERRSTAT和BUS来判断。DMACDTCERRSTAT。

请注意，如果在写入传输的最后一个数据时发生总线错误，则会发生传输结束事件和错误响应检测中断（DMA_TRANSERR）。

16.9 活动链接

DTC可以在一个传输请求完成时产生一个事件链接请求。

16.10 低功耗功能

在转换到模块停止功能、没有贪睡模式转换的软件待机模式、深度软件待机模式之前，将DTCST.DTCST位设置为0，然后执行以下部分中描述的操作。通过将SYSTEM.SNZCR.SNZDTCEN位设置为1，可以在贪睡模式下使用DTC。请参阅第10节，低功耗

Modes.

(1) Module-stop function

向MSTPCRA.MSTPA22位写入1可启用DTC的模块停止功能。如果在向MSTPCRA.MSTPA22位写入1时正在进行DTC传输，则在DTC传输结束后继续向模块停止状态的转换。当MSTPCRA.MSTPA22位为1时，禁止访问DTC寄存器。将0写入MSTPCRA.MSTPA22位可将DTC从模块停止状态释放。

(2) 软件待机模式，深度软件待机模式

使用第10.7.1节中描述的设置。转换到软件待机模式或第10.9.1节。过渡到深度软件待机模式。

如果在执行WFI指令时DTC传输操作正在进行，则在DTC传输完成后转换到软件待机模式或深度软件待机模式。

(3) 贪睡模式

当贪睡控制电路在软件待机模式下接收到贪睡请求时，MCU转入贪睡模式。请参阅第10.8.1节。过渡到贪睡模式。贪睡模式下的DTC操作可以在

SYSTEM.SNZCR.SNZDTCEN位。如果在贪睡模式下启用DTC操作，则在转换到软件待机模式之前，将DTCST.DTCST位设置为1。要通过DTC返回到软件待机模式，请将SYSTEM.SNZEDCR0.DTCZRED或SYSTEM.SNZEDCR0.DTCNZRED设置为1。请参阅第10.8.3节。从贪睡回来

模式到软件待机模式。SYSTEM.SNZEDCR0.DTCZRED在最后一次DTC传输完成时启用或禁用贪睡结束请求，当CRA和CRB为0时在DTC传输完成时检测到。SYSTEM.SNZEDCR0.DTCNZRED在非最后一次DTC传输时启用或禁用贪睡结束请求完成（CRA和CRB不为0），当CRA和CRB不为0时在DTC传输完成时检测到。来自ICU的DTC激活请求在软件待机模式期间停止，但在贪睡模式期间不停止。

(4) Notes on Low Power Consumption Function

For the WFI instruction and the register setting procedure, see section 10, Low Power Modes.

To perform a DTC transfer after returning from a low power mode without a Snooze mode transition, set the DTCST.DTCST bit to 1 again.

To use a request that is generated in Software Standby mode as an interrupt request to the CPU but not as a DTC activation request, specify the CPU as the interrupt request destination as described in section 12.4.1. Detecting Interrupts, then execute the WFI instruction. If DTC operation is enabled in Snooze mode, do not use the module-stop function of the DTC.

16.11 Usage Notes

16.11.1 Transfer Information Start Address

You must set multiples of 4 for the transfer information start addresses in the vector table. Otherwise, such addresses are accessed with their lowest 2 bits regarded as 00b.

(4) 低功耗功能注意事项

关于WFI指令和寄存器设置过程，请参见第10节，低功耗模式。

要在从低功耗模式返回后执行DTC传输而不进行贪睡模式转换，请将DTCST.DTCST位再次为1。

要将在软件待机模式下生成的请求用作对CPU的中断请求，但不用作DTC激活请求，请按照第12.4.1节中的说明将CPU指定为中断请求目标。检测中断，然后执行WFI指令。如果在贪睡模式下启用DTC操作，请勿使用DTC的模块停止功能。

16.11 使用说明

16.11.1 传输信息起始地址

您必须为向量表中的传输信息起始地址设置4的倍数。否则，这些地址的最低2位被视为00b。

17. Event Link Controller (ELC)

This is the ELC_B version of the ELC peripheral module.

ELC_B is referred to as ELC in this chapter.

17.1 Overview

The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 17.1 lists the ELC specifications, and Figure 17.1 shows a block diagram.

Table 17.1 ELC Specifications

Item	Description
Event link function	215 types of event signals can be directly connected to modules. The ELC generates the ELC event signal, and events that activate the DTC.
Module-stop function	Module-stop state can be set.
TrustZone Filter	Security attribution can be set for each registers

17. 事件链接控制器(ELC)

这是ELC外围模块的ELC_B版本。

ELC_B在本章中称为ELC。

17.1 Overview

EventLinkController(ELC)使用各种外围模块产生的事件请求作为源信号，将它们连接到不同的模块，允许模块之间直接链接，无需CPU干预。

表17.1列出了ELC规范，图17.1显示了框图。

Table 17.1 ELC Specifications

Item	Description
事件链接功能	215种事件信号可以直接连接到模块。ELC生成ELC事件信号和激活DTC的事件。
Module-stop function	可设置模块停止状态。
TrustZone Filter	可以为每个寄存器设置安全属性

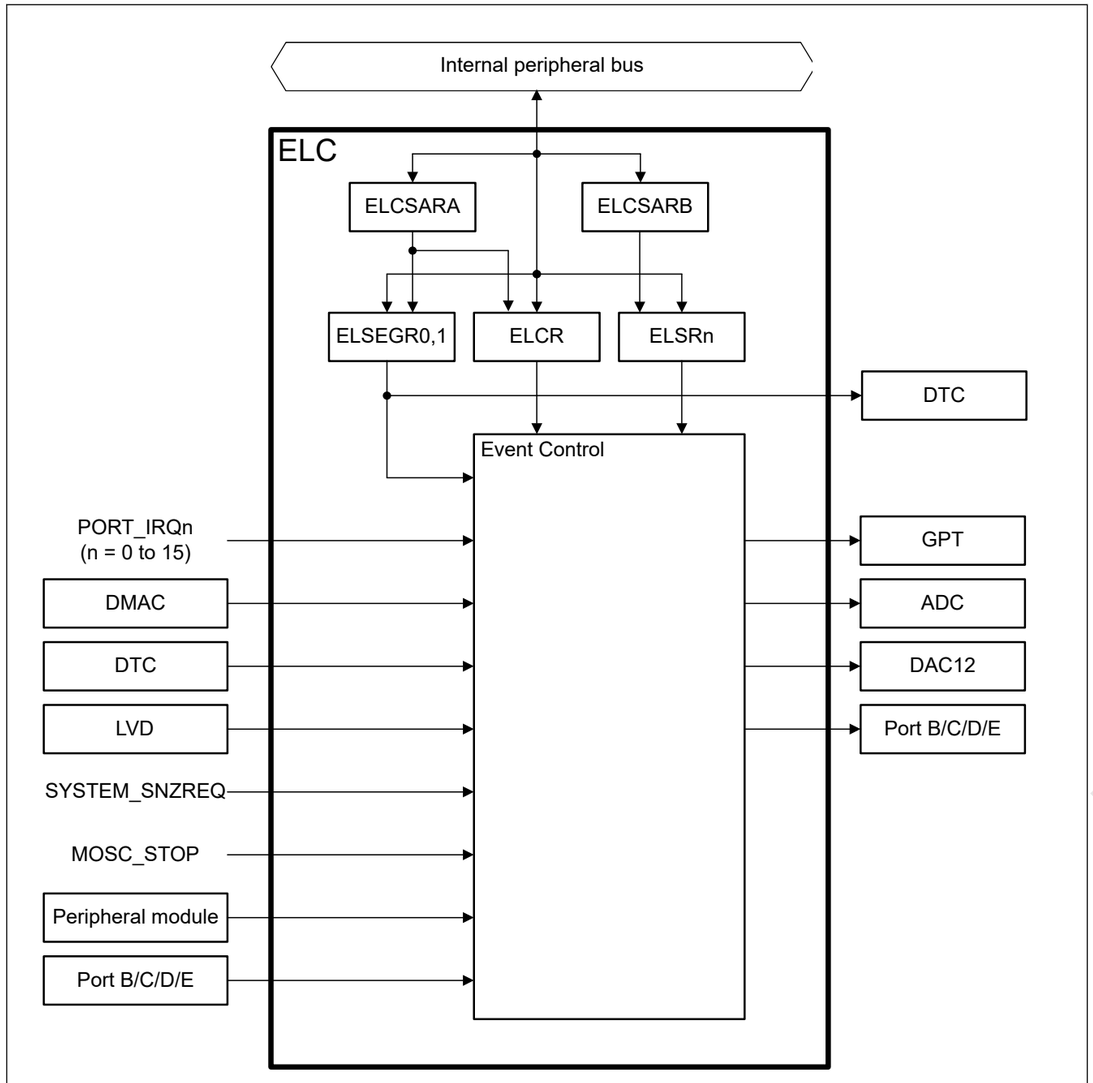


Figure 17.1 ELC block diagram

17.2 Register Descriptions

17.2.1 ELCR : Event Link Controller Register

Base address: ELC_B = 0x4008_2000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ELCON	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

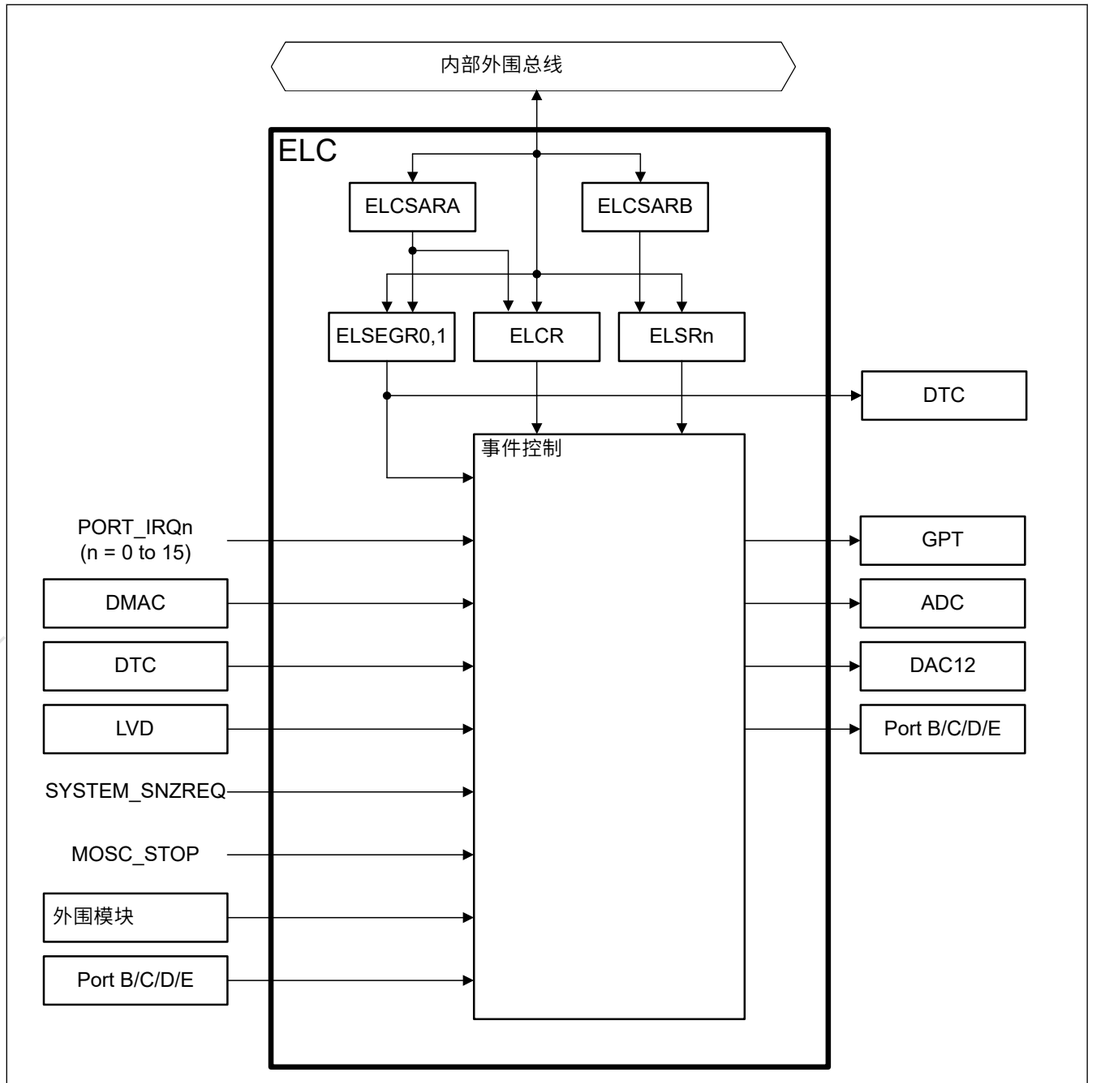


Figure 17.1 ELC框图

17.2 注册说明

17.2.1 ELCR:事件链接控制器寄存器

Base address: ELC_B = 0x4008_2000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ELCON	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	ELCON	All Event Link Enable 0: ELC function is disabled. 1: ELC function is enabled.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The ELCR register controls the ELC operation.

17.2.2 ELSEGRn : Event Link Software Event Generation Register n (n = 0, 1)

Base address: ELC_B = 0x4008_2000

Offset address: 0x04 + 0x04 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	WI	WE	—	—	—	—	—	SEG
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SEG	Software Event Generation 0: Normal operation 1: Software event is generated.	W
5:1	—	These bits are read as 0. The write value should be 0.	R/W
6	WE	SEG Bit Write Enable 0: Write to SEG bit disabled. 1: Write to SEG bit enabled.	R/W
7	WI	ELSEGR Register Write Disable 0: Write to ELSEGR register enabled. 1: Write to ELSEGR register disabled.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

SEG bit (Software Event Generation)

When 1 is written to the SEG bit while the WE bit is 1, a software event is generated. This bit is read as 0. Even when 1 is written to this bit, data is not stored. The WE bit must be set to 1 before writing to this bit.

A software event can trigger a linked DTC event.

WE bit (SEG Bit Write Enable)

The SEG bit can only be written to when the WE bit is 1. Clear the WI bit to 0 before writing to this bit.

[Setting condition]

- If 1 is written to this bit while the WI bit is 0, this bit becomes 1.

[Clearing condition]

- If 0 is written to this bit while the WI bit is 0, this bit becomes 0.

WI bit (ELSEGR Register Write Disable)

The ELSEGR register can only be written to when the write value to the WI bit is 0. This bit is read as 1. Before setting the WE or SEG bit, the WI bit must be set to 0.

Bit	Symbol	Function	R/W
6:0	—	这些位被读取为0。写入值应为0。	R/W
7	ELCON	所有事件链接启用 0：ELC功能关闭。1：ELC功能使能。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ELCR寄存器控制ELC操作。

17.2.2 ELSEGRn:事件链接软件事件生成寄存器n(n=0 1)

Base address: ELC_B = 0x4008_2000

Offset address: 0x04 + 0x04 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	WI	WE	—	—	—	—	—	SEG
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SEG	软件事件生成 0：正常操作1：产生软件事件。	W
5:1	—	这些位被读取为0。写入值应为0。	R/W
6	WE	SEG位写使能 0：禁止写入SEG位。1：写入SEG位使能。	R/W
7	WI	ELSEGR寄存器写入禁用 0：允许写入ELSEGR寄存器。1：禁止写入ELSEGR寄存器。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

SEG位（软件事件生成）

当WE位为1时向SEG位写入1时，将产生软件事件。该位被读取为0。即使向该位写入1，也不存储数据。在写入该位之前，WE位必须设置为1。

软件事件可以触发链接的DTC事件。

WE位（SEG位写使能）

SEG位只能在WE位为1时写入。在写入该位之前将WI位清零。

[Setting condition]

●如果在WI位为0时向该位写入1，则该位变为1。

[Clearing condition]

●如果在WI位为0时向该位写入0，则该位变为0。

WI位（ELSEGR寄存器写入禁止）

只有当WI位的写入值为0时，才能写入ELSEGR寄存器。该位读为1。在设置之前WE或SEG位，WI位必须设置为0。

17.2.3 ELSRn : Event Link Setting Register n (n = 0 to 7, 12 to 17, 19 to 24, 28, 29)

Base address: ELC_B = 0x4008_2000

Offset address: 0x20 + 0x04 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	ELS[8:0]	Event Link Select 0x000: Event output disabled for the associated peripheral module 0x001: Number setting for the event signal to be linked ⋮ 0x1DB: Number setting for the event signal to be linked Others: Settings prohibited	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The ELSRn register specifies an event signal to be linked to each peripheral module. Table 17.2 shows the association between the ELSRn register and the peripheral modules. Table 17.3 shows the association between the event signal names set in the ELSRn register and the signal numbers.

Table 17.2 Association between the ELSRn registers and peripheral functions (1 of 2)

Register name	Peripheral function (module)	Event name
ELSR0	GPT (A)	ELC_GPTA
ELSR1	GPT (B)	ELC_GPTB
ELSR2	GPT (C)	ELC_GPTC
ELSR3	GPT (D)	ELC_GPTD
ELSR4	GPT (E)	ELC_GPTE
ELSR5	GPT (F)	ELC_GPTF
ELSR6	GPT (G)	ELC_GPTG
ELSR7	GPT (H)	ELC_GPTH
ELSR12	DAC12 channel 0	ELC_DA0
ELSR13	DAC12 channel 1	ELC_DA1
ELSR14	PORT B	ELC_PORTB
ELSR15	PORT C	ELC_PORTC
ELSR16	PORT D	ELC_PORTD
ELSR17	PORT E	ELC_PORTE
ELSR19	ADCA0	ELC_AD00
ELSR20	ADCB0	ELC_AD01
ELSR21	ADCC0	ELC_AD02
ELSR22	ADCA1	ELC_AD10
ELSR23	ADCB1	ELC_AD11
ELSR24	ADCC1	ELC_AD12
ELSR28	DAC12 channel 2	ELC_DA2

17.2.3 ELSRn：事件链接设置寄存器n（n=0到7、12到17、19到24、28、29）

Base address: ELC_B = 0x4008_2000

Offset address: 0x20 + 0x04 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ELS[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	ELS[8:0]	活动链接选择 0x000：相关外围模块的事件输出禁用0x001：要链接的事件信号的编号设置 ⋮ 0x1DB：要联动的事件信号的编号设置其他：禁止设置	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ELSRn寄存器指定要链接到每个外围模块的事件信号。表17.2显示了ELSRn寄存器和外围模块之间的关联。表17.3显示了在ELSRn寄存器中设置的事件信号名称和信号编号之间的关联。

Table 17.2 ELSRn寄存器和外设功能之间的关联（1of2）

注册名称	外设功能（模块）	活动名称
ELSR0	GPT (A)	ELC_GPTA
ELSR1	GPT (B)	ELC_GPTB
ELSR2	GPT (C)	ELC_GPTC
ELSR3	GPT (D)	ELC_GPTD
ELSR4	GPT (E)	ELC_GPTE
ELSR5	GPT (F)	ELC_GPTF
ELSR6	GPT (G)	ELC_GPTG
ELSR7	GPT (H)	ELC_GPTH
ELSR12	DAC12 channel 0	ELC_DA0
ELSR13	DAC12 channel 1	ELC_DA1
ELSR14	PORT B	ELC_PORTB
ELSR15	PORT C	ELC_PORTC
ELSR16	PORT D	ELC_PORTD
ELSR17	PORT E	ELC_PORTE
ELSR19	ADCA0	ELC_AD00
ELSR20	ADCB0	ELC_AD01
ELSR21	ADCC0	ELC_AD02
ELSR22	ADCA1	ELC_AD10
ELSR23	ADCB1	ELC_AD11
ELSR24	ADCC1	ELC_AD12
ELSR28	DAC12 channel 2	ELC_DA2

Table 17.2 Association between the ELSRn registers and peripheral functions (2 of 2)

Register name	Peripheral function (module)	Event name
ELSR29	DAC12 channel 3	ELC_DA3

Table 17.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (1 of 6)

Event number	Interrupt request source	Name	Description
0x001	Port	PORT_IRQ0*1	External pin interrupt 0
0x002		PORT_IRQ1*1	External pin interrupt 1
0x003		PORT_IRQ2*1	External pin interrupt 2
0x004		PORT_IRQ3*1	External pin interrupt 3
0x005		PORT_IRQ4*1	External pin interrupt 4
0x006		PORT_IRQ5*1	External pin interrupt 5
0x007		PORT_IRQ6*1	External pin interrupt 6
0x008		PORT_IRQ7*1	External pin interrupt 7
0x009		PORT_IRQ8*1	External pin interrupt 8
0x00A		PORT_IRQ9*1	External pin interrupt 9
0x00B		PORT_IRQ10*1	External pin interrupt 10
0x00C		PORT_IRQ11*1	External pin interrupt 11
0x00D		PORT_IRQ12*1	External pin interrupt 12
0x00E		PORT_IRQ13*1	External pin interrupt 13
0x00F		PORT_IRQ14*1	External pin interrupt 14
0x010		PORT_IRQ15*1	External pin interrupt 15
0x020	DMAC0	DMAC0_INT	DMAC transfer end 0
0x021	DMAC1	DMAC1_INT	DMAC transfer end 1
0x022	DMAC2	DMAC2_INT	DMAC transfer end 2
0x023	DMAC3	DMAC3_INT	DMAC transfer end 3
0x024	DMAC4	DMAC4_INT	DMAC transfer end 4
0x025	DMAC5	DMAC5_INT	DMAC transfer end 5
0x026	DMAC6	DMAC6_INT	DMAC transfer end 6
0x027	DMAC7	DMAC7_INT	DMAC transfer end 7
0x02A	DTC	DTC_DTCEND*2	DTC transfer end
0x038	LVD	LVD_LVD1	Voltage monitor 1 interrupt
0x039		LVD_LVD2	Voltage monitor 2 interrupt
0x03B	MOSC	MOSC_STOP	Mail Clock oscillation stop
0x03C	LPW	SYSTEM_SNZREQ*2 *3	Snooze enrty
0x040	AGT0	AGT0_AGTI	AGT interrupt
0x041		AGT0_AGTCMAI	Compare match A
0x042		AGT0_AGTCMBI	Compare match B
0x043	AGT1	AGT1_AGTI	AGT interrupt
0x044		AGT1_AGTCMAI	Compare match A
0x045		AGT1_AGTCMBI	Compare match B
0x052	IWDT	IWDT_NMIUNDF	IWDT underflow
0x053	WDT	WDT_NMIUNDF	WDT underflow

Table 17.2 ELSRn寄存器与外围功能之间的关联（2之2）

注册名称	外设功能（模块）	活动名称
ELSR29	DAC12 channel 3	ELC_DA3

Table 17.3 在ELSRn.ELS[8:0]位中设置的事件信号名称与信号编号之间的关联（1of6）

事件编号	中断请求源	Name	Description
0x001	Port	PORT_IRQ0*1	外部引脚中断0
0x002		PORT_IRQ1*1	外部引脚中断1
0x003		PORT_IRQ2*1	外部引脚中断2
0x004		PORT_IRQ3*1	外部引脚中断3
0x005		PORT_IRQ4*1	外部引脚中断4
0x006		PORT_IRQ5*1	外部引脚中断5
0x007		PORT_IRQ6*1	外部引脚中断6
0x008		PORT_IRQ7*1	外部引脚中断7
0x009		PORT_IRQ8*1	外部引脚中断8
0x00A		PORT_IRQ9*1	外部引脚中断9
0x00B		PORT_IRQ10*1	外部引脚中断10
0x00C		PORT_IRQ11*1	外部引脚中断11
0x00D		PORT_IRQ12*1	外部引脚中断12
0x00E		PORT_IRQ13*1	外部引脚中断13
0x00F		PORT_IRQ14*1	外部引脚中断14
0x010		PORT_IRQ15*1	外部引脚中断15
0x020	DMAC0	DMAC0_INT	DMAC传输结束0
0x021	DMAC1	DMAC1_INT	DMAC传输结束1
0x022	DMAC2	DMAC2_INT	DMAC传输结束2
0x023	DMAC3	DMAC3_INT	DMAC传输结束3
0x024	DMAC4	DMAC4_INT	DMAC传输结束4
0x025	DMAC5	DMAC5_INT	DMAC传输结束5
0x026	DMAC6	DMAC6_INT	DMAC传输结束6
0x027	DMAC7	DMAC7_INT	DMAC传输结束7
0x02A	DTC	DTC_DTCEND*2	DTC传输结束
0x038	LVD	LVD_LVD1	电压监视器1中断
0x039		LVD_LVD2	电压监视器2中断
0x03B	MOSC	MOSC_STOP	邮件时钟振荡停止
0x03C	LPW	SYSTEM_SNZREQ*2 *3	Snooze enrty
0x040	AGT0	AGT0_AGTI	AGT interrupt
0x041		AGT0_AGTCMAI	比较匹配A
0x042		AGT0_AGTCMBI	比较匹配B
0x043	AGT1	AGT1_AGTI	AGT interrupt
0x044		AGT1_AGTCMAI	比较匹配A
0x045		AGT1_AGTCMBI	比较匹配B
0x052	IWDT	IWDT_NMIUNDF	IWDT underflow
0x053	WDT	WDT_NMIUNDF	WDT underflow

Table 17.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (2 of 6)

Event number	Interrupt request source	Name	Description
0x08F	ACMPHS	ACMP_HS0	High-Speed Analog Comparator interruput 0
0x090		ACMP_HS1	High-Speed Analog Comparator interruput 1
0x091		ACMP_HS2	High-Speed Analog Comparator interruput 2
0x092		ACMP_HS3	High-Speed Analog Comparator interruput 3
0x0B1	I/O Port	IOPORT_GROUPB	Port B event
0x0B2		IOPORT_GROUPC	Port C event
0x0B3		IOPORT_GROUPD	Port D event
0x0B4		IOPORT_GROUPE	Port E event
0x0B5	ELC	ELC_SWEVT0	Software event 0
0x0B6		ELC_SWEVT1	Software event 1
0x0C0	GPT0	GPT0_CCMPA	Compare match A
0x0C1		GPT0_CCMPB	Compare match B
0x0C2		GPT0_CMPC	Compare match C
0x0C3		GPT0_CMPD	Compare match D
0x0C4		GPT0_CMPE	Compare match E
0x0C5		GPT0_CMPF	Compare match F
0x0C6		GPT0_OVF	Overflow
0x0C7		GPT0_UDF	Underflow
0x0C8		GPT0_PC	Cycle count function end
0x0CA		GPT0_ADTRGA	A/D converter start request A
0x0CB		GPT0_ADTRGB	A/D converter start request B
0x0CC	GPT1	GPT1_CCMPA	Compare match A
0x0CD		GPT1_CCMPB	Compare match B
0x0CE		GPT1_CMPC	Compare match C
0x0CF		GPT1_CMPD	Compare match D
0x0D0		GPT1_CMPE	Compare match E
0x0D1		GPT1_CMPF	Compare match F
0x0D2		GPT1_OVF	Overflow
0x0D3		GPT1_UDF	Underflow
0x0D4		GPT1_PC	Cycle count function end
0x0D6		GPT1_ADTRGA	A/D converter start request A
0x0D7		GPT1_ADTRGB	A/D converter start request B

Table 17.3 在ELSRn.ELS[8:0]位中设置的事件信号名称和信号编号之间的关联（6个中的2个）

事件编号	中断请求源	Name	Description
0x08F	ACMPHS	ACMP_HS0	高速模拟比较器中断0
0x090		ACMP_HS1	高速模拟比较器中断1
0x091		ACMP_HS2	高速模拟比较器中断2
0x092		ACMP_HS3	高速模拟比较器中断3
0x0B1	I/O Port	IOPORT_GROUPB	端口B事件
0x0B2		IOPORT_GROUPC	端口C事件
0x0B3		IOPORT_GROUPD	端口D事件
0x0B4		IOPORT_GROUPE	端口E事件
0x0B5	ELC	ELC_SWEVT0	软件事件0
0x0B6		ELC_SWEVT1	软件事件1
0x0C0	GPT0	GPT0_CCMPA	比较匹配A
0x0C1		GPT0_CCMPB	比较匹配B
0x0C2		GPT0_CMPC	比较匹配C
0x0C3		GPT0_CMPD	比较匹配D
0x0C4		GPT0_CMPE	比较匹配E
0x0C5		GPT0_CMPF	比较匹配F
0x0C6		GPT0_OVF	Overflow
0x0C7		GPT0_UDF	Underflow
0x0C8		GPT0_PC	循环计数功能结束
0x0CA		GPT0_ADTRGA	AD转换器启动请求A
0x0CB		GPT0_ADTRGB	AD转换器启动请求B
0x0CC	GPT1	GPT1_CCMPA	比较匹配A
0x0CD		GPT1_CCMPB	比较匹配B
0x0CE		GPT1_CMPC	比较匹配C
0x0CF		GPT1_CMPD	比较匹配D
0x0D0		GPT1_CMPE	比较匹配E
0x0D1		GPT1_CMPF	比较匹配F
0x0D2		GPT1_OVF	Overflow
0x0D3		GPT1_UDF	Underflow
0x0D4		GPT1_PC	循环计数功能结束
0x0D6		GPT1_ADTRGA	AD转换器启动请求A
0x0D7		GPT1_ADTRGB	AD转换器启动请求B

Table 17.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (3 of 6)

Event number	Interrupt request source	Name	Description
0x0D8	GPT2	GPT2_CCMPA	Compare match A
0x0D9		GPT2_CCMPB	Compare match B
0x0DA		GPT2_CMPC	Compare match C
0x0DB		GPT2_CMPD	Compare match D
0x0DC		GPT2_CMPE	Compare match E
0x0DD		GPT2_CMPF	Compare match F
0x0DE		GPT2_OVF	Overflow
0x0DF		GPT2_UDF	Underflow
0x0E0		GPT2_PC	Cycle count function end
0x0E2		GPT2_ADTRGA	A/D converter start request A
0x0E3		GPT2_ADTRGB	A/D converter start request B
0x0E4	GPT3	GPT3_CCMPA	Compare match A
0x0E5		GPT3_CCMPB	Compare match B
0x0E6		GPT3_CMPC	Compare match C
0x0E7		GPT3_CMPD	Compare match D
0x0E8		GPT3_CMPE	Compare match E
0x0E9		GPT3_CMPF	Compare match F
0x0EA		GPT3_OVF	Overflow
0x0EB		GPT3_UDF	Underflow
0x0EC		GPT3_PC	Cycle count function end
0x0EE		GPT3_ADTRGA	A/D converter start request A
0x0EF		GPT3_ADTRGB	A/D converter start request B
0x0F0	GPT4	GPT4_CCMPA	Compare match A
0x0F1		GPT4_CCMPB	Compare match B
0x0F2		GPT4_CMPC	Compare match C
0x0F3		GPT4_CMPD	Compare match D
0x0F4		GPT4_CMPE	Compare match E
0x0F5		GPT4_CMPF	Compare match F
0x0F6		GPT4_OVF	Overflow
0x0F7		GPT4_UDF	Underflow
0x0FA		GPT4_ADTRGA	A/D converter start request A
0x0FB		GPT4_ADTRGB	A/D converter start request B
0x0FC	GPT5	GPT5_CCMPA	Compare match A
0x0FD		GPT5_CCMPB	Compare match B
0x0FE		GPT5_CMPC	Compare match C
0x0FF		GPT5_CMPD	Compare match D
0x100		GPT5_CMPE	Compare match E
0x101		GPT5_CMPF	Compare match F
0x102		GPT5_OVF	Overflow
0x103		GPT5_UDF	Underflow
0x106		GPT5_ADTRGA	A/D converter start request A
0x107		GPT5_ADTRGB	A/D converter start request B

Table 17.3 在ELSRn.ELS[8:0]位中设置的事件信号名称与信号编号之间的关联（3of6）

事件编号	中断请求源	Name	Description
0x0D8	GPT2	GPT2_CCMPA	比较匹配A
0x0D9		GPT2_CCMPB	比较匹配B
0x0DA		GPT2_CMPC	比较匹配C
0x0DB		GPT2_CMPD	比较匹配D
0x0DC		GPT2_CMPE	比较匹配E
0x0DD		GPT2_CMPF	比较匹配F
0x0DE		GPT2_OVF	Overflow
0x0DF		GPT2_UDF	Underflow
0x0E0		GPT2_PC	循环计数功能结束
0x0E2		GPT2_ADTRGA	AD转换器启动请求A
0x0E3		GPT2_ADTRGB	AD转换器启动请求B
0x0E4	GPT3	GPT3_CCMPA	比较匹配A
0x0E5		GPT3_CCMPB	比较匹配B
0x0E6		GPT3_CMPC	比较匹配C
0x0E7		GPT3_CMPD	比较匹配D
0x0E8		GPT3_CMPE	比较匹配E
0x0E9		GPT3_CMPF	比较匹配F
0x0EA		GPT3_OVF	Overflow
0x0EB		GPT3_UDF	Underflow
0x0EC		GPT3_PC	循环计数功能结束
0x0EE		GPT3_ADTRGA	AD转换器启动请求A
0x0EF		GPT3_ADTRGB	AD转换器启动请求B
0x0F0	GPT4	GPT4_CCMPA	比较匹配A
0x0F1		GPT4_CCMPB	比较匹配B
0x0F2		GPT4_CMPC	比较匹配C
0x0F3		GPT4_CMPD	比较匹配D
0x0F4		GPT4_CMPE	比较匹配E
0x0F5		GPT4_CMPF	比较匹配F
0x0F6		GPT4_OVF	Overflow
0x0F7		GPT4_UDF	Underflow
0x0FA		GPT4_ADTRGA	AD转换器启动请求A
0x0FB		GPT4_ADTRGB	AD转换器启动请求B
0x0FC	GPT5	GPT5_CCMPA	比较匹配A
0x0FD		GPT5_CCMPB	比较匹配B
0x0FE		GPT5_CMPC	比较匹配C
0x0FF		GPT5_CMPD	比较匹配D
0x100		GPT5_CMPE	比较匹配E
0x101		GPT5_CMPF	比较匹配F
0x102		GPT5_OVF	Overflow
0x103		GPT5_UDF	Underflow
0x106		GPT5_ADTRGA	AD转换器启动请求A
0x107		GPT5_ADTRGB	AD转换器启动请求B

Table 17.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (4 of 6)

Event number	Interrupt request source	Name	Description
0x108	GPT6	GPT6_CCMPA	Compare match A
0x109		GPT6_CCMPB	Compare match B
0x10A		GPT6_CMPC	Compare match C
0x10B		GPT6_CMPD	Compare match D
0x10C		GPT6_CMPE	Compare match E
0x10D		GPT6_CMPF	Compare match F
0x10E		GPT6_OVF	Overflow
0x10F		GPT6_UDF	Underflow
0x112		GPT6_ADTRGA	A/D converter start request A
0x113		GPT6_ADTRGB	A/D converter start request B
0x114	GPT7	GPT7_CCMPA	Compare match A
0x115		GPT7_CCMPB	Compare match B
0x116		GPT7_CMPC	Compare match C
0x117		GPT7_CMPD	Compare match D
0x118		GPT7_CMPE	Compare match E
0x119		GPT7_CMPF	Compare match F
0x11A		GPT7_OVF	Overflow
0x11B		GPT7_UDF	Underflow
0x11E		GPT7_ADTRGA	A/D converter start request A
0x11F		GPT7_ADTRGB	A/D converter start request B
0x120	GPT8	GPT8_CCMPA	Compare match A
0x121		GPT8_CCMPB	Compare match B
0x122		GPT8_CMPC	Compare match C
0x123		GPT8_CMPD	Compare match D
0x124		GPT8_CMPE	Compare match E
0x125		GPT8_CMPF	Compare match F
0x126		GPT8_OVF	Overflow
0x127		GPT8_UDF	Underflow
0x12A		GPT8_ADTRGA	A/D converter start request A
0x12B		GPT8_ADTRGB	A/D converter start request B
0x12C	GPT9	GPT9_CCMPA	Compare match A
0x12D		GPT9_CCMPB	Compare match B
0x12E		GPT9_CMPC	Compare match C
0x12F		GPT9_CMPD	Compare match D
0x130		GPT9_CMPE	Compare match E
0x131		GPT9_CMPF	Compare match F
0x132		GPT9_OVF	Overflow
0x133		GPT9_UDF	Underflow
0x136		GPT9_ADTRGA	A/D converter start request A
0x137		GPT9_ADTRGB	A/D converter start request B
0x138	GPT	GPT_UVWEDGE	UVW edge event

Table 17.3 在ELSRn.ELS[8:0]位中设置的事件信号名称与信号编号之间的关联（4of6）

事件编号	中断请求源	Name	Description
0x108	GPT6	GPT6_CCMPA	比较匹配A
0x109		GPT6_CCMPB	比较匹配B
0x10A		GPT6_CMPC	比较匹配C
0x10B		GPT6_CMPD	比较匹配D
0x10C		GPT6_CMPE	比较匹配E
0x10D		GPT6_CMPF	比较匹配F
0x10E		GPT6_OVF	Overflow
0x10F		GPT6_UDF	Underflow
0x112		GPT6_ADTRGA	AD转换器启动请求A
0x113		GPT6_ADTRGB	AD转换器启动请求B
0x114	GPT7	GPT7_CCMPA	比较匹配A
0x115		GPT7_CCMPB	比较匹配B
0x116		GPT7_CMPC	比较匹配C
0x117		GPT7_CMPD	比较匹配D
0x118		GPT7_CMPE	比较匹配E
0x119		GPT7_CMPF	比较匹配F
0x11A		GPT7_OVF	Overflow
0x11B		GPT7_UDF	Underflow
0x11E		GPT7_ADTRGA	AD转换器启动请求A
0x11F		GPT7_ADTRGB	AD转换器启动请求B
0x120	GPT8	GPT8_CCMPA	比较匹配A
0x121		GPT8_CCMPB	比较匹配B
0x122		GPT8_CMPC	比较匹配C
0x123		GPT8_CMPD	比较匹配D
0x124		GPT8_CMPE	比较匹配E
0x125		GPT8_CMPF	比较匹配F
0x126		GPT8_OVF	Overflow
0x127		GPT8_UDF	Underflow
0x12A		GPT8_ADTRGA	AD转换器启动请求A
0x12B		GPT8_ADTRGB	AD转换器启动请求B
0x12C	GPT9	GPT9_CCMPA	比较匹配A
0x12D		GPT9_CCMPB	比较匹配B
0x12E		GPT9_CMPC	比较匹配C
0x12F		GPT9_CMPD	比较匹配D
0x130		GPT9_CMPE	比较匹配E
0x131		GPT9_CMPF	比较匹配F
0x132		GPT9_OVF	Overflow
0x133		GPT9_UDF	Underflow
0x136		GPT9_ADTRGA	AD转换器启动请求A
0x137		GPT9_ADTRGB	AD转换器启动请求B
0x138	GPT	GPT_UVWEDGE	UVW边缘事件

Table 17.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (5 of 6)

Event number	Interrupt request source	Name	Description
0x140	IIC0	IIC0_RX	Rx Data buffer full
0x141		IIC0_TX	Tx Data buffer empty
0x142		IIC0_TEND	Transmit end
0x145		IIC0_COM	Communication event
0x146	IIC1	IIC1_RX	Rx Data buffer full
0x147		IIC1_TX	Tx Data buffer empty
0x148		IIC1_TEND	Transmit end
0x14A		IIC1_COM	Communication event
0x159	ADC	ADC_ADI0	A/D scan end for scan group 0
0x15A		ADC_ADI1	A/D scan end for scan group 1
0x15B		ADC_ADI2	A/D scan end for scan group 2
0x15E		ADC_CCMPM0*2	Composite compare match 0
0x167		ADC_ADI3	A/D scan end for scan group 3
0x168		ADC_ADI4	A/D scan end for scan group 4
0x169		ADC_ADI5678	A/D scan end for scan group 5 to 8
0x16C		ADC_CCMPM1*2	Composite compare match 1
0x18D	SCI0	SCI0_RXI*4	Receive data full
0x18E		SCI0_TXI*4	Transmit data empty
0x18F		SCI0_TEI*4	Transmit end
0x190		SCI0_ERI	Receive error
0x191		SCI0_AED	Effective edge detection
0x193		SCI0_AM	Address match event
0x195	SCI1	SCI1_RXI*4	Received data full
0x196		SCI1_TXI*4	Transmit data empty
0x197		SCI1_TEI*4	Transmit end
0x198		SCI1_ERI	Receive error
0x199		SCI1_AED	Effective edge detection
0x19B		SCI1_AM	Address match event
0x19C	SCI2	SCI2_RXI*4	Received data full
0x19D		SCI2_TXI*4	Transmit data empty
0x19E		SCI2_TEI*4	Transmit end
0x19F		SCI2_ERI	Receive error
0x1A0		SCI2_AED	Effective edge detection
0x1A2		SCI2_AM	Address match event
0x1A3	SCI3	SCI3_RXI*4	Received data full
0x1A4		SCI3_TXI*4	Transmit data empty
0x1A5		SCI3_TEI*4	Transmit end
0x1A6		SCI3_ERI	Receive error
0x1A7		SCI3_AED	Effective edge detection
0x1A9		SCI3_AM	Address match event

Table 17.3 在ELSRn.ELS[8:0]位中设置的事件信号名称与信号编号之间的关联（5of6）

事件编号	中断请求源	Name	Description
0x140	IIC0	IIC0_RX	Rx数据缓冲区已满
0x141		IIC0_TX	Tx数据缓冲区为空
0x142		IIC0_TEND	发射端
0x145		IIC0_COM	交流活动
0x146	IIC1	IIC1_RX	Rx数据缓冲区已满
0x147		IIC1_TX	Tx数据缓冲区为空
0x148		IIC1_TEND	发射端
0x14A		IIC1_COM	交流活动
0x159	ADC	ADC_ADI0	扫描组0的AD扫描结束
0x15A		ADC_ADI1	扫描组1的AD扫描结束
0x15B		ADC_ADI2	扫描组2的AD扫描结束
0x15E		ADC_CCMPM0*2	复合比较匹配0
0x167		ADC_ADI3	扫描组3的D扫描结束
0x168		ADC_ADI4	扫描组4的AD扫描结束
0x169		ADC_ADI5678	扫描组5到8的AD扫描结束
0x16C		ADC_CCMPM1*2	复合比较匹配1
0x18D	SCI0	SCI0_RXI*4	接收数据已满
0x18E		SCI0_TXI*4	传输数据为空
0x18F		SCI0_TEI*4	发射端
0x190		SCI0_ERI	接收错误
0x191		SCI0_AED	有效边缘检测
0x193		SCI0_AM	地址匹配事件
0x195	SCI1	SCI1_RXI*4	接收数据已满
0x196		SCI1_TXI*4	传输数据为空
0x197		SCI1_TEI*4	发射端
0x198		SCI1_ERI	接收错误
0x199		SCI1_AED	有效边缘检测
0x19B		SCI1_AM	地址匹配事件
0x19C	SCI2	SCI2_RXI*4	接收数据已满
0x19D		SCI2_TXI*4	传输数据为空
0x19E		SCI2_TEI*4	发射端
0x19F		SCI2_ERI	接收错误
0x1A0		SCI2_AED	有效边缘检测
0x1A2		SCI2_AM	地址匹配事件
0x1A3	SCI3	SCI3_RXI*4	接收数据已满
0x1A4		SCI3_TXI*4	传输数据为空
0x1A5		SCI3_TEI*4	发射端
0x1A6		SCI3_ERI	接收错误
0x1A7		SCI3_AED	有效边缘检测
0x1A9		SCI3_AM	地址匹配事件

Table 17.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (6 of 6)

Event number	Interrupt request source	Name	Description
0x1AA	SCI4	SCI4_RXI*4	Received data full
0x1AB		SCI4_TXI*4	Transmit data empty
0x1AC		SCI4_TEI*4	Transmit end
0x1AD		SCI4_ERI	Receive error
0x1AE		SCI4_AED	Effective edge detection
0x1B0		SCI4_AM	Address match event
0x1B1	SCI9	SCI9_RXI*4	Received data full
0x1B2		SCI9_TXI*4	Transmit data empty
0x1B3		SCI9_TEI*4	Transmit end
0x1B4		SCI9_ERI	Receive error
0x1B5		SCI9_AED	Effective edge detection
0x1B7		SCI9_AM	Address match event
0x1C4	SPI0	SPI0_SPRI	Receive buffer full
0x1C5		SPI0_SPTI	Transmit buffer empty
0x1C6		SPI0_SPII	Idle
0x1C7		SPI0_SPEI	Error
0x1C8		SPI0_SPCEND	Communication complete event
0x1C9	SPI1	SPI1_SPRI	Receive buffer full
0x1CA		SPI1_SPTI	Transmit buffer empty
0x1CB		SPI1_SPII	Idle
0x1CC		SPI1_SPEI	Error
0x1CD		SPI1_SPCEND	Transmission complete event
0x1DB	DOC	DOC_DOPCI*2	Data operation circuit interrupt

Note 1. Only pulse (edge detection) is supported.
Note 2. This event can occur in Snooze mode.
Note 3. ELSR14 to ELSR17 and ELSR19 to ELSR24 can select this event.
Note 4. This event is not supported in FIFO mode.

17.2.4 ELCSARA : Event Link Controller Security Attribution Register A

Base address: ELC_B = 0x4008_2000

Offset address: 0xE0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	ELSEGR1	ELSEGR0	ELCR
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 17.3 ELSRn.ELS[8:0]位中设置的事件信号名称与信号编号之间的关联（6个中的6个）

事件编号	中断请求源	Name	Description
0x1AA	SCI4	SCI4_RXI*4	接收数据已满
0x1AB		SCI4_TXI*4	传输数据为空
0x1AC		SCI4_TEI*4	发射端
0x1AD		SCI4_ERI	接收错误
0x1AE		SCI4_AED	有效边缘检测
0x1B0		SCI4_AM	地址匹配事件
0x1B1	SCI9	SCI9_RXI*4	接收数据已满
0x1B2		SCI9_TXI*4	传输数据为空
0x1B3		SCI9_TEI*4	发射端
0x1B4		SCI9_ERI	接收错误
0x1B5		SCI9_AED	有效边缘检测
0x1B7		SCI9_AM	地址匹配事件
0x1C4	SPI0	SPI0_SPRI	接收缓冲区已满
0x1C5		SPI0_SPTI	发送缓冲区为空
0x1C6		SPI0_SPII	Idle
0x1C7		SPI0_SPEI	Error
0x1C8		SPI0_SPCEND	通讯完成事件
0x1C9	SPI1	SPI1_SPRI	接收缓冲区已满
0x1CA		SPI1_SPTI	发送缓冲区为空
0x1CB		SPI1_SPII	Idle
0x1CC		SPI1_SPEI	Error
0x1CD		SPI1_SPCEND	传输完成事件
0x1DB	DOC	DOC_DOPCI*2	数据运算电路中断

注1.仅支持脉冲（边沿检测）。
注2.此事件可能在贪睡模式下发生。
注3.ELSR14到ELSR17和ELSR19到ELSR24可以选择此事件。
注4.FIFO模式不支持此事件。

17.2.4 ELCSARA:事件链接控制器安全属性寄存器A

Base address: ELC_B = 0x4008_2000

Offset address: 0xE0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	ELSEGR1	ELSEGR0	ELCR
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	ELCR	Event Link Controller Register Security Attribution Target register: ELCR 0: Secure 1: Non-secure	R/W
1	ELSEGR0	Event Link Software Event Generation Register 0 Security Attribution 0: Secure 1: Non-secure	R/W
2	ELSEGR1	Event Link Software Event Generation Register 1 Security Attribution 0: Secure 1: Non-secure	R/W
31:3	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The ELCR register controls operation of the ELC.

17.2.5 ELCSARB : Event Link Controller Security Attribution Register B

Base address: ELC_B = 0x4008_2000

Offset address: 0xE4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	ELSR29	ELSR28	—	—	—	ELSR24	ELSR23	ELSR22	ELSR21	ELSR20	ELSR19	—	ELSR17	ELSR16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ELSR15	ELSR14	ELSR13	ELSR12	—	—	—	—	ELSR7	ELSR6	ELSR5	ELSR4	ELSR3	ELSR2	ELSR1	ELSR0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	ELSR7 to ELSR0	Event Link Setting Register n Security Attribution Target register: ELSRn (n = 0 to 7) 0: Secure 1: Non-secure	R/W
11:8	—	These bits are read as 1. The write value should be 1.	R/W
17:12	ELSR17 to ELSR12	Event Link Setting Register n Security Attribution Target register: ELSRn (n = 12 to 17) 0: Secure 1: Non-secure	R/W
18	—	This bit is read as 1. The write value should be 1.	R/W
24:19	ELSR24 to ELSR19	Event Link Setting Register n Security Attribution Target register: ELSRn (n = 19 to 24) 0: Secure 1: Non-secure	R/W
27:25	—	These bits are read as 1. The write value should be 1.	R/W
29:28	ELSR29 to ELSR28	Event Link Setting Register n Security Attribution Target register: ELSRn (n = 28, 29) 0: Secure 1: Non-secure	R/W
31:30	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

Bit	Symbol	Function	R/W
0	ELCR	事件链接控制器注册安全属性 Target register: ELCR 0: Secure 1: Non-secure	R/W
1	ELSEGR0	事件链接软件事件生成寄存器0安全属性 0: Secure 1: Non-secure	R/W
2	ELSEGR1	事件链接软件事件生成寄存器1安全属性 0: Secure 1: Non-secure	R/W
31:3	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

ELCR寄存器控制ELC的操作。

17.2.5 ELCSARB:事件链接控制器安全属性寄存器B

Base address: ELC_B = 0x4008_2000

Offset address: 0xE4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	ELSR29	ELSR28	—	—	—	ELSR24	ELSR23	ELSR22	ELSR21	ELSR20	ELSR19	—	ELSR17	ELSR16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ELSR15	ELSR14	ELSR13	ELSR12	—	—	—	—	ELSR7	ELSR6	ELSR5	ELSR4	ELSR3	ELSR2	ELSR1	ELSR0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	ELSR7 to ELSR0	事件链接设置寄存器n安全属性 目标寄存器：ELSRn（n=0到7） 0: Secure 1: Non-secure	R/W
11:8	—	这些位被读取为1。写入值应为1。	R/W
17:12	ELSR17 to ELSR12	事件链接设置寄存器n安全属性 目标寄存器：ELSRn（n=12到17） 0: Secure 1: Non-secure	R/W
18	—	该位读取为1。写入值应为1。	R/W
24:19	ELSR24 to ELSR19	事件链接设置寄存器n安全属性 目标寄存器：ELSRn（n=19到24） 0: Secure 1: Non-secure	R/W
27:25	—	这些位被读取为1。写入值应为1。	R/W
29:28	ELSR29 to ELSR28	事件链接设置寄存器n安全属性 Target register: ELSRn (n = 28, 29) 0: Secure 1: Non-secure	R/W
31:30	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

This register specifies the security attribution for the Register ELSRn (n = 0 to 7, 12 to 17, 19 to 24, 28, 29).

17.3 Operation

17.3.1 Relation between Interrupt Handling and Event Linking

Event number for an event link is the same as that for the associated interrupt source. For information on generating event signals, see the explanation in the chapter for each event source module.

17.3.2 Linking Events

When an event occurs and that event is already set as a trigger in the Event Link Setting Register (ELSRn), the associated module is activated. The operation of the module must be set up in advance. Table 17.4 lists the operations of modules when an event occurs.

Table 17.4 Module operations when event occurs

Module	Operations When Event is Input
GPT	• Start counting • Stop counting • Clear counting • Up counting • Down counting • Input capture
DAC12	Start D/A conversion
I/O Ports	• Change pin output based on the EORR (reset) or EOSR (set) • Latch pin state to EIDR • The following ports can be used for the ELC: PORT B PORT C PORT D PORT E
ADC	Start A/D conversion
DTC	Start DTC data transfer

17.3.3 Example of Procedure for Linking Events

To link events:

1. Set the operation of the module for which an event is to be linked.
2. Set the appropriate ELSRn.ELS[8:0] bits for the module to be linked.
3. Set the ELCR.ELCON bit to 1 to enable linkage of all events.
4. Configure the module from which an event is output and activate the module. The link between the two modules is now active.
5. To stop event linkage of modules individually, set 0 to the ELSRn.ELS[8:0] bit associated with the modules. To stop linkage of all the events, set the ELCR.ELCON bit to 0.

If event link output from the LVD is to be used, set the ELC after setting the LVD. To disable the LVD, do so after setting 0x00 to the associated ELSRn register.

17.4 Usage Notes

17.4.1 Linking DMAC/DTC Transfer End Signals as Events

When linking the DMAC/DTC transfer end signals as events, do not set the same peripheral module as the DMAC/DTC transfer destination and event link destination. If set, the peripheral module might be started before DMAC/DTC transfer to the peripheral module is complete.

该寄存器指定寄存器ELSRn的安全属性（n=0到7、12到17、19到24、28、29）。

17.3 Operation

17.3.1 中断处理和事件链接的关系

事件链接的事件编号与关联中断源的事件编号相同。有关生成事件信号的信息，请参阅每个事件源模块的章节中的说明。

17.3.2 链接事件

当事件发生并且该事件已在事件链接设置寄存器(ELSRn)中设置为触发器时，将激活相关模块。模块的操作必须提前设置好。表17.4列出了事件发生时模块的操作。

Table 17.4 事件发生时的模块操作

Module	输入事件时的操作
GPT	• 开始计数 • 停止计数 • 清除计数 • 向上计数 • 向下计数 • 输入捕捉
DAC12	开始DA转换
I/O Ports	• 根据EORR（复位）或EOSR（设置）更改引脚输出 • EIDR的锁存器引脚状态 • 以下端口可用于ELC： PORT B PORT C PORT D PORT E
ADC	开始AD转换
DTC	开始DTC数据传输

17.3.3 链接事件的过程示例

链接事件：

1.设置要链接事件的模块的操作。

2.为要链接的模块设置适当的ELSRn.ELS[8:0]位。

3.将ELCR.ELCON位设置为1以启用所有事件的链接。

4.配置输出事件的模块并激活模块。两个模块之间的链接现在处于活动状态。

5.要单独停止模块的事件链接，请将与模块关联的ELSRn.ELS[8:0]位设置为0。要停止所有事件的链接，请将ELCR.ELCON位设置为0。

如果要使用来自LVD的事件链接输出，请在设置LVD后设置ELC。要禁用LVD，请在将0x00设置为相关的ELSRn寄存器后执行此操作。

17.4 使用说明

17.4.1 将DMACDTC传输结束信号作为事件链接

将DMACDTC传输结束信号作为事件链接时，请勿将外设模块设置为DMACDTC传输目标和事件链接目标。如果设置，则外围模块可能会在DMACDTC传输到外围模块完成之前启动。

17.4.2 Setting Clocks

To link events, you must enable the ELC and the related modules. The modules cannot operate if the related modules are in the module-stop state or in low power mode in which the module is stopped (Software Standby mode or Deep Software Standby mode).

Some modules can perform in Snooze mode. For more information, see Table 17.3 and section 10, Low Power Modes.

17.4.3 Module-Stop Function Setting

The Module Stop Control Register C (MSTPCRC) can enable or disable ELC operation. The ELC is initially stopped after reset. Releasing the module-stop state enables access to the registers. The ELCON bit must be set to 0 before disabling ELC operation using the Module Stop Control Register. For more information, see Table 17.3 and section 10, Low Power Modes.

17.4.4 ELC Delay Time

In Figure 17.2, module A accesses module B through the ELC. There is a delay time in the ELC between module A and module B. Table 17.5 shows the ELC delay time.

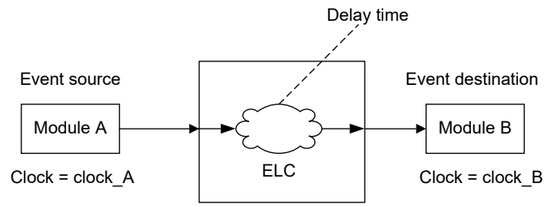


Figure 17.2 ELC delay time

Table 17.5 ELC delay time

Clock domain	Clock frequency	ELC delay time
clock_A = clock_B	clock_A = clock_B	0 cycle
clock_A ≠ clock_B	clock_A = clock_B	1 cycle to 2 cycles
	clock_A > clock_B	1 cycle to 2 cycles of clock_B
	clock_A < clock_B	1 cycle to 2 cycles of clock_A

17.4.5 Interval of Event Request

If the clocks of Event Source and Event Destination are combined as shown in Table 17.6, the Event request may be lost if the interval between one Event request and the next is less than the following value (Event_Interval) for the same Event request signal.

However, this restriction does not apply if the Event Destination is GPT or ADC and uses a different ELSR register.

Table 17.6 shows a combination of clocks with the restricted event interval, and Figure 17.3 shows an example of the event interval for GPT0_ADTRGA.

The event interval is expressed by the following formula.

Event_Interval [ns] = Period_of_Source_clock [ns] × 6 + Period_of_Destination_clock [ns] × 4

17.4.2 设置时钟

要链接事件，您必须启用ELC和相关模块。如果相关模块处于模块停止状态或模块停止的低功耗模式（软件待机模式或深度软件待机模式），则模块无法运行。

某些模块可以在贪睡模式下执行。有关详细信息，请参阅表17.3和第10节，低功耗模式。

17.4.3 模块停止功能设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用ELC操作。ELC在复位后最初停止。释放模块停止状态可以访问寄存器。在使用模块停止控制寄存器禁用ELC操作之前，必须将ELCON位设置为0。有关详细信息，请参阅表17.3和第10节，低功耗模式。

17.4.4 ELC延迟时间

在图17.2中，模块A通过ELC访问模块B。模块A和模块B之间的ELC中有一个延迟时间。表17.5显示了ELC延迟时间。

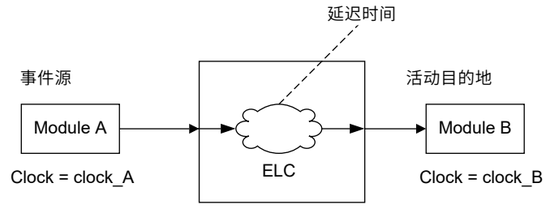


Figure 17.2 ELC延迟时间

Table 17.5 ELC延迟时间

时钟域	时钟频率	ELC延迟时间
clock_A = clock_B	clock_A = clock_B	0 cycle
clock_A ≠ clock_B	clock_A = clock_B	1个周期到2个周期
	clock_A > clock_B	1个周期到2个clock_B周期
	clock_A < clock_B	1个周期到2个clock_A周期

17.4.5 事件请求的间隔

如果EventSource和EventDestination的时钟如表17.6所示组合，如果一个Event请求与下一个Event请求之间的间隔小于同一Event请求信号的以下值(Event_Interval)，则该Event请求可能会丢失。

但是，如果事件目标是GPT或ADC并使用不同的ELSR寄存器，则此限制不适用。

表17.6显示了具有受限事件间隔的时钟组合，图17.3显示了GPT0_ADTRGA的事件间隔示例。

事件间隔由以下公式表示。

Event_Interval [ns] = Period_of_Source_clock [ns] × 6 + Period_of_Destination_clock [ns] × 4

Table 17.6 Combination of clocks with the restricted Event Interval

Event Source	Source clock	Event Destination	Destination clock
Other than GPT	PCLKA or PCLKB	GPT	GPTCLK
		ADC	GPTCLK or PCLKC
GPT	PCLKD	ADC	GPTCLK or PCLKC
	GPTCLK	ADC	PCLKA or PCLKC
		DAC12	PCLKA
		I/O Port	PCLKB

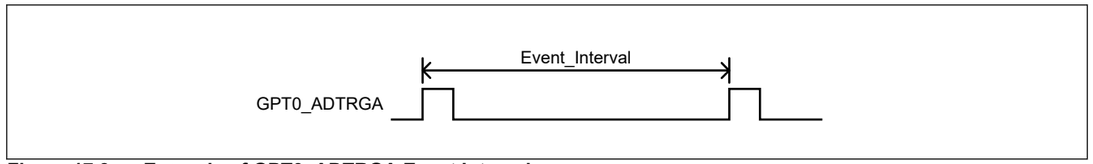


Figure 17.3 Example of GPT0_ADTRGA Event Interval

Table 17.6 时钟与受限事件间隔的组合

事件源	源时钟	活动目的地	目的地时钟
除了GPT	PCLKA or PCLKB	GPT	GPTCLK
		ADC	GPTCLK or PCLKC
GPT	PCLKD	ADC	GPTCLK or PCLKC
	GPTCLK	ADC	PCLKA or PCLKC
		DAC12	PCLKA
		I/O Port	PCLKB

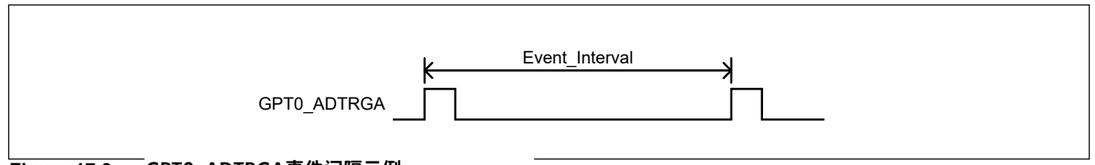


Figure 17.3 GPT0_ADTRGA事件间隔示例

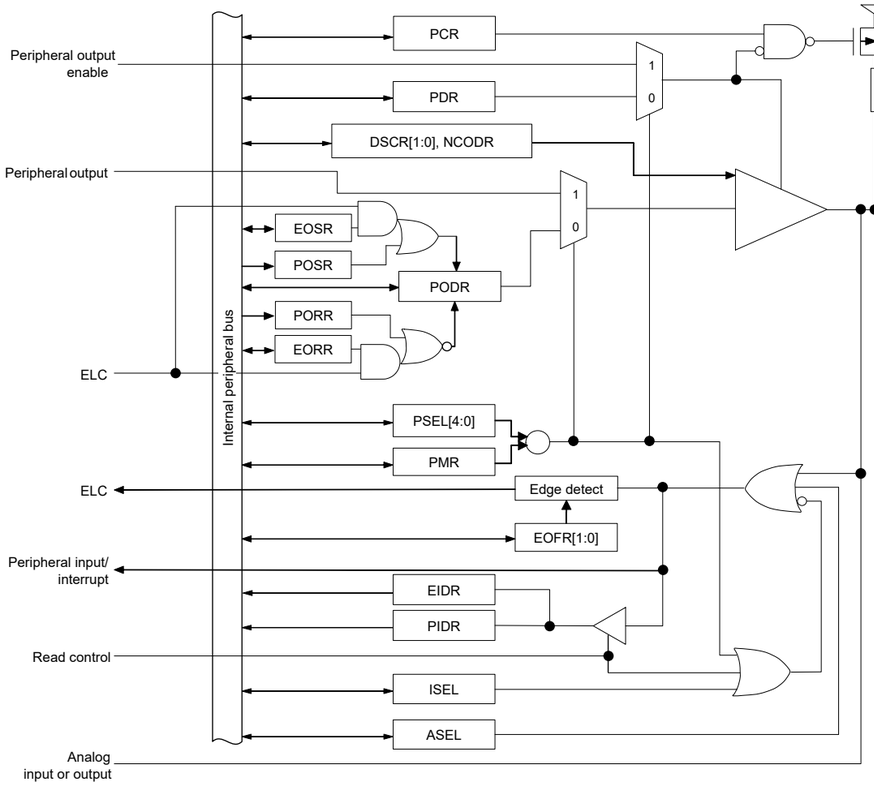
18. I/O Ports

18.1 Overview

The I/O port pins operate as general I/O port pins, I/O pins for peripheral modules, interrupt input pins, analog I/O, or port group function for the ELC.

All pins except PB03 (as TDO of JTAG ports) operate as input pins immediately after a reset, and pin functions are switched by register settings. The I/O ports and peripheral modules for each pin are specified in the associated registers.

Figure 18.1 shows a connection diagram for the I/O port registers. The configuration of the I/O ports differs for different packages. Table 18.1 lists the I/O port specifications by package, and Table 18.2 lists the port functions.



Note: This figure shows a basic port configuration. The configuration differs depending on the ports.

Figure 18.1 Connection diagram for I/O port registers

Table 18.1 I/O port specifications (1 of 2)

Port	Package 100 pins	Number of pins	Package 64 pins	Number of pins	Package 48 pins	Number of pins
PORT0	P000 to P002	3	P002	1	—	0
PORT2	P201, P212, P213	3	P201, P212, P213	3	P201, P212, P213	3
PORTA	PA00 to PA15	16	PA00 to PA15	16	PA00 to PA15	16

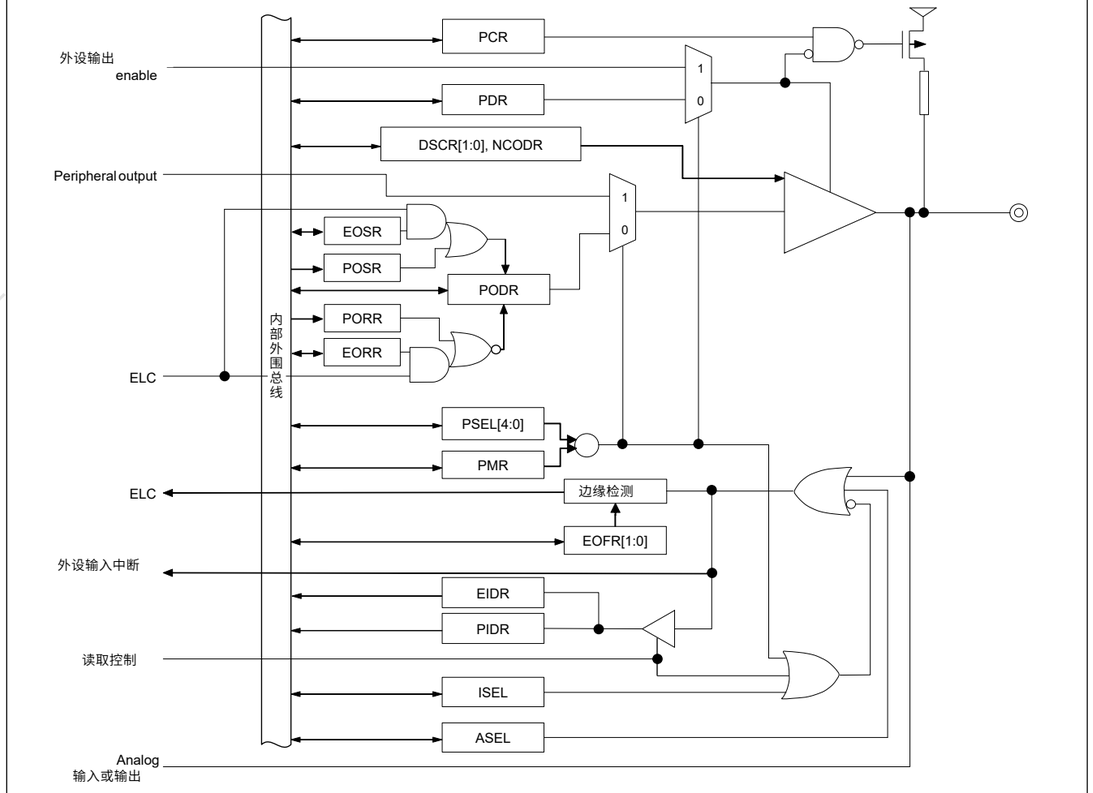
18. I/O Ports

18.1 Overview

IO端口引脚用作通用IO端口引脚、外围模块的IO引脚、中断输入引脚、模拟IO或ELC的端口组功能。

除PB03（作为JTAG端口的TDO）之外的所有引脚在复位后立即作为输入引脚工作，引脚功能通过寄存器设置切换。每个引脚的IO端口和外围模块在相关寄存器中指定。

图18.1显示了IO端口寄存器的连接图。不同封装的IO端口配置不同。表18.1按封装列出了IO端口规格，表18.2列出了端口功能。



Note: 此图显示了基本端口配置。配置因端口而异。

Figure 18.1 IO端口寄存器的连接图

Table 18.1 IO端口规格(1of2)

Port	Package 100 pins	引脚数	Package 64 pins	引脚数	Package 48 pins	引脚数
PORT0	P000 to P002	3	P002	1	—	0
PORT2	P201, P212, P213	3	P201, P212, P213	3	P201, P212, P213	3
PORTA	PA00 to PA15	16	PA00 to PA15	16	PA00 to PA15	16

Table 18.1 I/O port specifications (2 of 2)

Port	Package 100 pins	Number of pins	Package 64 pins	Number of pins	Package 48 pins	Number of pins
PORTB	PB00 to PB10, PB12 to PB15	15	PB00 to PB09, PB12 to PB15	14	PB00, PB01, PB03 to PB09, PB12 to PB15	13
PORTC	PC00 to PC15	16	PC00 to PC15	16	PC13 to PC15	3
PORTD	PD00 to PD15	16	PD02	1	—	0
PORTE	PE00 to PE06, PE08 to PE15	15	—	0	—	0

Table 18.2 I/O port functions

Port	Port name	Input pull-up	Open-drain output	Drive capacity switching	5V tolerant	I/O
PORT0	P000, P001	✓	—	—	—	Input
	P002	—	—	—	—	Input
PORT2	P201	✓	✓	Low	—	Input / Output
	P212, P213	✓	✓	Low, middle, high	—	Input / Output
PORTA	PA00 to PA05	—	—	—	—	Input
	PA06, PA07	✓	—	—	—	Input
	PA08 to PA11	✓	✓	Low, middle, high, High current drive	—	Input / Output
	PA12 to PA15	✓	✓	Low, middle, high	✓	Input / Output
PORTB	PB00, PB01	✓	—	—	—	Input
	PB02	—	—	—	—	Input
	PB03, PB05 to PB09	✓	✓	Low, middle, high	✓	Input / Output
	PB04, PB10	✓	✓	Low, middle, high	—	Input / Output
	PB12 to PB15	✓	✓	Low, middle, high, High current drive	—	Input / Output
PORTC	PC00 to PC05	✓	—	—	—	Input
	PC06 to PC09	✓	✓	Low, middle, high, High current drive	—	Input / Output
	PC10 to PC12	✓	✓	Low, middle, high	✓	Input / Output
	PC13	✓	—	—	—	Input
	PC14, PC15	✓	✓	Low	✓	Input / Output
PORTD	PD00 to PD07	✓	✓	Low, middle, high	✓	Input / Output
	PD08 to PD15	✓	✓	Low, middle, high, High current drive	—	Input / Output
PORTE	PE00, PE01	✓	✓	Low, middle, high	✓	Input / Output
	PE02 to PE06	✓	✓	Low, middle, high, high-speed high-drive	—	Input / Output
	PE08, PE09	✓	✓	Low, middle, high	—	Input / Output
	PE10 to PE15	✓	✓	Low, middle, high, High current drive	—	Input / Output

Note: ✓: Available
—: Setting prohibited

Table 18.1 IO端口规格(2of2)

Port	Package 100 pins	引脚数	Package 64 pins	引脚数	Package 48 pins	引脚数
PORTB	PB00 to PB10, PB12 to PB15	15	PB00 to PB09, PB12 to PB15	14	PB00, PB01, PB03 to PB09, PB12 to PB15	13
PORTC	PC00 to PC15	16	PC00 to PC15	16	PC13 to PC15	3
PORTD	PD00 to PD15	16	PD02	1	—	0
PORTE	PE00 to PE06, PE08 to PE15	15	—	0	—	0

Table 18.2 IO口功能

Port	端口名称	Input pull-up	Open-drain output	驱动容量切换	5V tolerant	I/O
PORT0	P000, P001	✓	—	—	—	Input
	P002	—	—	—	—	Input
PORT2	P201	✓	✓	Low	—	输入输出
	P212, P213	✓	✓	低、中、高	—	输入输出
PORTA	PA00 to PA05	—	—	—	—	Input
	PA06, PA07	✓	—	—	—	Input
	PA08 to PA11	✓	✓	低、中、高、大电流驱动	—	输入输出
	PA12 to PA15	✓	✓	低、中、高	✓	输入输出
PORTB	PB00, PB01	✓	—	—	—	Input
	PB02	—	—	—	—	Input
	PB03, PB05 to PB09	✓	✓	低、中、高	✓	输入输出
	PB04, PB10	✓	✓	低、中、高	—	输入输出
	PB12 to PB15	✓	✓	低、中、高、大电流驱动	—	输入输出
PORTC	PC00 to PC05	✓	—	—	—	Input
	PC06 to PC09	✓	✓	低、中、高、大电流驱动	—	输入输出
	PC10 to PC12	✓	✓	低、中、高	✓	输入输出
	PC13	✓	—	—	—	Input
	PC14, PC15	✓	✓	Low	✓	输入输出
PORTD	PD00 to PD07	✓	✓	低、中、高	✓	输入输出
	PD08 to PD15	✓	✓	低、中、高、大电流驱动	—	输入输出
PORTE	PE00, PE01	✓	✓	低、中、高	✓	输入输出
	PE02 to PE06	✓	✓	低、中、高、高速高速驱动	—	输入输出
	PE08, PE09	✓	✓	低、中、高	—	输入输出
	PE10 to PE15	✓	✓	低、中、高、大电流驱动	—	输入输出

Note: :可用一:禁止设置

18.2 Register Descriptions

18.2.1 PCNTR1/PODR/PDR : Port Control Register 1

Base address: PORTm = 0x4001_F000 + 0x0020 × m (m = 0, 2, A to E)

Offset address: 0x000 (PCNTR1/PDR)
0x002 (PODR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PODR15	PODR14	PODR13	PODR12	PODR11	PODR10	PODR09	PODR08	PODR07	PODR06	PODR05	PODR04	PODR03	PODR02	PODR01	PODR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR09	PDR08	PDR07	PDR06	PDR05	PDR04	PDR03	PDR02	PDR01	PDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	PDR15 to PDR00	Pmn Direction 0: Input (functions as an input pin) 1: Output (functions as an output pin)	R/W*1
31:16	PODR15 to PODR00	Pmn Output Data 0: Low output 1: High output	R/W*2

Note: m = 0, 2, A to E, n = 00 to 15
Note 1. If the security attribution is configured as Secure,
- Secure access and Non-secure read access are allowed,
- Non-secure write access is ignored, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure access are allowed.

Note 2. If the security attribution is configured as Secure,
- Secure access is allowed,
- Non-secure read value is 0, but TrustZone access error is not generated,
- Non-secure write access is ignored, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure access are allowed.

The Port Control Register 1 (PCNTR1/PODR/PDR) is a 32-bit or 16-bit read/write register that controls port direction and port output data. The PCNTR1 specifies the port direction and output data, and is accessed in 32-bit units. The PDRn (bits [15:0] in PCNTR1) and PODRn (bits [31:16] in PCNTR1) respectively, are accessed in 16-bit units.

PDRn bits (Pmn Direction)

The PDRn bits select the input or output direction for individual pins on the associated port when the pins are configured as general I/O pins. Each pin on port m is associated with a PORTm.PCNTR1.PDRn bit. The I/O direction can be specified in 1-bit unit. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0. In the case of input only ports, PDRn bits are reserved. See section 18.1. Overview. The PDRn bit in the PORTm.PCNTR1 register serves the same function as the PDR bit in the PFS.PmnPFS register.

PODRn bits (Pmn Output Data)

The PODRn bits hold data to be output from the general I/O pins. Bits of non-existent port m are reserved. Reserved bits are read as 0. The write value should be 0. In the case of input only ports, PODRn bits are reserved. See section 18.1. Overview. The PODRn bit in the PORTm.PCNTR1 register serves the same function as the PODR bit in the PFS.PmnPFS register.

18.2 注册说明

18.2.1 PCNTR1PODRPDR:端口控制寄存器1

Base address: PORTm = 0x4001_F000 + 0x0020 × m (m = 0, 2, A to E)

Offset address: 0x000 (PCNTR1/PDR)
0x002 (PODR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PODR15	PODR14	PODR13	PODR12	PODR11	PODR10	PODR09	PODR08	PODR07	PODR06	PODR05	PODR04	PODR03	PODR02	PODR01	PODR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR09	PDR08	PDR07	PDR06	PDR05	PDR04	PDR03	PDR02	PDR01	PDR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	PDR15 to PDR00	Pmn Direction 0：输入（用作输入引脚）1：输出（ 用作输出引脚）	R/W*1
31:16	PODR15 to PODR00	Pmn输出数据 0：低输出1： 高输出	R/W*2

Note: m = 0, 2, A to E, n = 00 to 15
注1.如果安全属性配置为Secure，●
允许安全访问和非安全读取访问，
- 忽略非安全写入访问，但不会生成TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全访问。

注2.如果安全属性配置为Secure，●
允许安全访问，
- 非安全读取值为0，但不会产生TrustZone访问错误，
- 忽略非安全写入访问，但不会生成TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全访问。

端口控制寄存器1(PCNTR1PODRPDR)是一个32位或16位读写寄存器，用于控制端口方向和端口输出数据。PCNTR1指定端口方向和输出数据，并以32位为单位进行访问。PDRn（PCNTR1中的位[15:0]）和PODRn（PCNTR1中的位[31:16]）分别以16位为单位进行访问。

PDRn bits (Pmn Direction)

当引脚配置为通用IO引脚时，PDRn位选择相关端口上各个引脚的输入或输出方向。端口m上的每个引脚都与一个PORTm.PCNTR1.PDRn位相关联。可以以1位为单位指定IO方向。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。在仅输入端口的情况下，保留PDRn位。请参阅第18.1节。概述。PORTm.PCNTR1寄存器中的PDRn位与PFS.PmnPFS寄存器中的PDR位具有相同的功能。

PODRn位（Pmn输出数据）

PODRn位保存要从通用IO引脚输出的数据。不存在的端口m的位被保留。保留位读取为0。写入值应为0。在仅输入端口的情况下，保留PODRn位。请参阅第18.1节。概述。PORTm.PCNTR1寄存器中的PODRn位与PFS.PmnPFS寄存器中的PODR位具有相同的功能。

18.2.2 PCNTR2/EIDR/PIDR : Port Control Register 2

Base address: PORTm = 0x4001_F000 + 0x0020 × m (m = 0, 2, A to E)

Offset address: 0x004 (PCNTR2/PIDR)
0x006 (EIDR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EIDR15	EIDR14	EIDR13	EIDR12	EIDR11	EIDR10	EIDR09	EIDR08	EIDR07	EIDR06	EIDR05	EIDR04	EIDR03	EIDR02	EIDR01	EIDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PIDR15	PIDR14	PIDR13	PIDR12	PIDR11	PIDR10	PIDR09	PIDR08	PIDR07	PIDR06	PIDR05	PIDR04	PIDR03	PIDR02	PIDR01	PIDR00
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
15:0	PIDR15 to PIDR00	Pmn State 0: Low level 1: High level	R
31:16	EIDR15 to EIDR00 *2	Port Event Input Data*1 When an ELC_PORTx signal occurs 0: Low input 1: High input	R

Note: If the security attribution is configured as Secure,
- Secure read access is allowed,
- Non-secure read value is 0, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure read access are allowed.

Note: m = 0, 2, A to E, n = 00 to 15
Note 1. x = B, C, D or E for EIDR only
Note 2. Supported by ports B, C, D or E.

The Port Control Register 2 (PCNTR2/EIDR/PIDR) allows read access to the Pmn state and the port event input data using 32-bit or 16-bit access.

The PCNTR2 specifies the Pmn state and the port event input data, and is accessed in 32-bit units.

The PIDRn (bits [15:0] in PCNTR2) and EIDRn (bits [31:16] in PCNTR2) respectively, are accessed in 16-bit units. Bits associated with non-existent pins are reserved. Reserved bits are read as undefined.

PIDRn bits (Pmn State)

The PIDRn bits reflect the individual pin states of the port, regardless of the values set in PmnPFS.PMR and PORTm.PCNTR1.PDRn. The PIDRn bit in the PORTm.PCNTR2 register serves the same function as the PIDR bit in the PFS.PmnPFS register.

A pin state cannot be reflected in PIDRn when the following functions is enabled:

- Analog function (ASEL = 1)

EIDRn bits (Port Event Input Data)

The EIDRn bits latch a pin state when an ELC_PORTx signal occurs. Pin states can only be input to EIDRn when PmnPFS.PMR and PORTm.PCNTR1.PDRn are 0. When the PmnPFS.ASEL bit is set to 1, the associated pin state is not reflected in EIDRn.

18.2.2 PCNTR2EIDRPIDR：端口控制寄存器2

Base address: PORTm = 0x4001_F000 + 0x0020 × m (m = 0, 2, A to E)

Offset address: 0x004 (PCNTR2/PIDR)
0x006 (EIDR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EIDR15	EIDR14	EIDR13	EIDR12	EIDR11	EIDR10	EIDR09	EIDR08	EIDR07	EIDR06	EIDR05	EIDR04	EIDR03	EIDR02	EIDR01	EIDR00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PIDR15	PIDR14	PIDR13	PIDR12	PIDR11	PIDR10	PIDR09	PIDR08	PIDR07	PIDR06	PIDR05	PIDR04	PIDR03	PIDR02	PIDR01	PIDR00
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
15:0	PIDR15 to PIDR00	Pmn State 0：低电平1 ：高电平	R
31:16	EIDR15 to EIDR00 *2	端口事件输入数据*1 当发生ELC_PORTx信号时 0：低输入1 ：高输入	R

Note: 如果安全属性配置为安全，●
允许安全读取访问，
- 非安全读取值为0，但不会产生TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全读取访问。

Note: m = 0, 2, A to E, n = 00 to 15
注1.x=B、C、D或E仅适用于EIDR
注2.端口B、C、D或E支持。

端口控制寄存器2(PCNTR2EIDRPIDR)允许使用32位或16位访问对Pmn状态和端口事件输入数据进行读取访问。

PCNTR2指定Pmn状态和端口事件输入数据，并以32位为单位进行访问。

PIDRn（PCNTR2中的位[15:0]）和EIDRn（PCNTR2中的位[31:16]）分别以16位为单位进行访问。与不存在的引脚相关的位被保留。保留位被读取为未定义。

PIDRn bits (Pmn State)

PIDRn位反映端口的各个引脚状态，与PmnPFS.PMR和
PORTm.PCNTR1.PDRn。PORTm.PCNTR2寄存器中的PIDRn位与
PFS.PmnPFS register.

当启用以下功能时，引脚状态不能反映在PIDRn中：

●模拟功能（ASEL=1）

EIDRn位（端口事件输入数据）

当ELC_PORTx信号出现时，EIDRn位锁存引脚状态。引脚状态只能输入到EIDRn时
PmnPFS.PMR和PORTm.PCNTR1.PDRn为0。当PmnPFS.ASEL位设置为1时，相关引脚状态不会反映在EIDRn中。

18.2.3 PCNTR3/PORR/POSR : Port Control Register 3

Base address: PORTm = 0x4001_F000 + 0x0020 × m (m = 0, 2, A to E)

Offset address: 0x008 (PCNTR3/POSR)
0x00A (PORR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PORR15	PORR14	PORR13	PORR12	PORR11	PORR10	PORR09	PORR08	PORR07	PORR06	PORR05	PORR04	PORR03	PORR02	PORR01	PORR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	POSR15	POSR14	POSR13	POSR12	POSR11	POSR10	POSR09	POSR08	POSR07	POSR06	POSR05	POSR04	POSR03	POSR02	POSR01	POSR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	POSR15 to POSR00	Pmn Output Set 0: No effect on output 1: High output	W
31:16	PORR15 to PORR00	Pmn Output Reset 0: No effect on output 1: Low output	W

Note: If the security attribution is configured as Secure,
- Secure write access is allowed,
- Non-secure write access is ignored, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure write access are allowed.

Note: m = 0, 2, A to E, n = 00 to 15

The Port Control Register 3 (PCNTR3/PORR/POSR) is a 32-bit or 16-bit write register that controls the setting or resetting of the port output data.

The PCNTR3 controls the setting or resetting of the port output data, and is accessed in 32-bit units.

The POSRn (bits [15:0] in PCNTR3) and the PORRn (bits [31:16] in PCNTR3) respectively, are accessed in 16-bit units.

POSRn bits (Pmn Output Set)

POSR changes PODR when set by a software write. For example, for PD00, when PORTD.PCNTR3.POSR00 = 1, PORTD.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. In the case of input only ports, POSRn bits are reserved. See section 18.1. Overview.

PORRn bits (Pmn Output Reset)

PORR changes PODR when reset by a software write. For example, for PD00, when PORTD.PCNTR3.PORR00 = 1, PORTD.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. In the case of input only ports, PORRn bits are reserved. See section 18.1. Overview.

Note: When EORRn or EOSRn is set, writing is prohibited to PODRn, PORRn, and POSRn.
Note: PORRn and POSRn should not be set at the same time.

18.2.3 PCNTR3PORRPOSR：端口控制寄存器3

Base address: PORTm = 0x4001_F000 + 0x0020 × m (m = 0, 2, A to E)

Offset address: 0x008 (PCNTR3/POSR)
0x00A (PORR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PORR15	PORR14	PORR13	PORR12	PORR11	PORR10	PORR09	PORR08	PORR07	PORR06	PORR05	PORR04	PORR03	PORR02	PORR01	PORR00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	POSR15	POSR14	POSR13	POSR12	POSR11	POSR10	POSR09	POSR08	POSR07	POSR06	POSR05	POSR04	POSR03	POSR02	POSR01	POSR00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	POSR15 to POSR00	Pmn输出设置 0：不影响输出1：高输出	W
31:16	PORR15 to PORR00	Pmn输出复位 0：对输出无影响1：低输出	W

Note: 如果安全属性配置为安全，●
允许安全写访问，
- 忽略非安全写入访问，但不会生成TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全写访问。

Note: m = 0, 2, A to E, n = 00 to 15

端口控制寄存器3(PCNTR3PORRPOSR)是一个32位或16位写寄存器，用于控制端口输出数据的设置或复位。

PCNTR3控制端口输出数据的设置或复位，并以32位为单位进行访问。

POSRn（PCNTR3中的位[15:0]）和PORRn（PCNTR3中的位[31:16]）分别以16位为单位进行访问。

POSRn位（Pmn输出设置）

POSR在通过软件写入设置时改变PODR。例如，对于PD00，当PORTD.PCNTR3.POSR00=1时，PORTD.PCNTR1.PODR00输出1。与不存在的引脚相关的位被保留。写入值应始终为0。在仅输入端口的情况下，保留POSRn位。请参阅第18.1节。概述。

PORRN位（Pmn输出复位）

PORR在通过软件写入复位时改变PODR。例如，对于PD00，当PORTD.PCNTR3.PORR00=1时，PORTD.PCNTR1.PODR00输出0。与不存在的引脚相关的位被保留。写入值应始终为0。在仅输入端口的情况下，保留PORRN位。请参阅第18.1节。概述。

Note: 当设置EORRn或EOSRn时，禁止写入PODRn、PORRn和POSRn。
Note: PORRn和POSRn不应同时设置。

18.2.4 PCNTR4/EORR/EOSR : Port Control Register 4

Base address: PORTm = 0x4001_F000 + 0x0020 × m (m = B to E)

Offset address: 0x00C (PCNTR4/EOSR)
0x00E (EORR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EORR15	EORR14	EORR13	EORR12	EORR11	EORR10	EORR09	EORR08	EORR07	EORR06	EORR05	EORR04	EORR03	EORR02	EORR01	EORR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EOSR15	EOSR14	EOSR13	EOSR12	EOSR11	EOSR10	EOSR09	EOSR08	EOSR07	EOSR06	EOSR05	EOSR04	EOSR03	EOSR02	EOSR01	EOSR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	EOSR15 to EOSR00	Pmn Event Output Set When an ELC_PORTx signal occurs 0: No effect on output 1: High output	R/W
31:16	EORR15 to EORR0	Pmn Event Output Reset When an ELC_PORTx signal occurs 0: No effect on output 1: Low output	R/W

Note: If the security attribution is configured as Secure,
- Secure access is allowed,
- Non-secure read value is 0, but TrustZone access error is not generated,
- Non-secure write access is ignored, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure access are allowed.

Note: m = B to E, n = 00 to 15, x = B to E

The Port Control Register 4 (PCNTR4/EORR/EOSR) is a 32-bit or 16-bit read/write register that controls the setting or resetting of the port output data by an event input from the ELC.

The PCNTR4 controls the setting or resetting of the port output data by an event input from the ELC, and is accessed in 32-bit units.

The EOSRn (bits [15:0] in PCNTR4) and EORRn (bits [31:16] in PCNTR4) respectively, are accessed in 16-bit units.

EOSRn bits (Pmn Event Output Set)

EOSR changes PODR when set because an ELC_PORTx signal occurs. For example, for PD00 if PORTD.PCNTR4.EOSR00 is set to 1 when the ELC_PORTx occurs, PORTD.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. In the case of input only ports, EOSRn bits are reserved. See section 18.1. Overview.

EORRn bits (Pmn Event Output Reset)

EORR changes PODR when reset because an ELC_PORTx signal occurs. For example, for PD00 if PORTD.PCNTR4.EORR00 = 1 when the ELC_PORTx occurs, PORTD.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. In the case of input only ports, EORRn bits are reserved. See section 18.1. Overview.

Note: When EORRn or EOSRn is set, writing is prohibited to PODRn, PORRn, and POSRn.

Note: EORRn and EOSRn should not be set at the same time.

18.2.4 PCNTR4EORREOSR：端口控制寄存器4

Base address: PORTm = 0x4001_F000 + 0x0020 × m (m = B to E)

Offset address: 0x00C (PCNTR4/EOSR)
0x00E (EORR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EORR15	EORR14	EORR13	EORR12	EORR11	EORR10	EORR09	EORR08	EORR07	EORR06	EORR05	EORR04	EORR03	EORR02	EORR01	EORR00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EOSR15	EOSR14	EOSR13	EOSR12	EOSR11	EOSR10	EOSR09	EOSR08	EOSR07	EOSR06	EOSR05	EOSR04	EOSR03	EOSR02	EOSR01	EOSR00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	EOSR15 to EOSR00	Pmn事件输出集 当发生ELC_PORTx信号时 0：不影响输出1：高输出	R/W
31:16	EORR15 to EORR0	Pmn事件输出复位 当发生ELC_PORTx信号时 0：对输出无影响1：低输出	R/W

Note: 如果安全属性配置为安全，●
允许安全访问，
- 非安全读取值为0，但不会产生TrustZone访问错误，
- 忽略非安全写入访问，但不会生成TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全访问。

Note: m = B to E, n = 00 to 15, x = B to E

端口控制寄存器4(PCNTR4EORREOSR)是一个32位或16位读写寄存器，通过来自ELC的事件输入来控制端口输出数据的设置或复位。

PCNTR4通过来自ELC的事件输入来控制端口输出数据的设置或复位，并以32位为单位进行访问。

分别以16位为单位访问EOSRn（PCNTR4中的位[15:0]）和EORRn（PCNTR4中的位[31:16]）。

EOSRn位（Pmn事件输出设置）

EOSR在设置时会更改PODR，因为发生ELC_PORTx信号。例如，对于PD00，如果当ELC_PORTx发生时，PORTD.PCNTR4.EOSR00设置为1，PORTD.PCNTR1.PODR00输出1。与不存在的引脚相关的位被保留。写入值应始终为0。在仅输入端口的情况下，保留EOSRn位。请参阅第18.1节。概述。

EORRN位（Pmn事件输出复位）

EORR会在复位时更改PODR，因为发生ELC_PORTx信号。例如，对于PD00，如果PORTD.PCNTR4.EORR00=1当ELC_PORTx发生时，PORTD.PCNTR1.PODR00输出0。与不存在的引脚相关的位被保留。写入值应始终为0。在仅输入端口的情况下，保留EORRn位。请参阅第18.1节。概述。

Note: 当设置EORRn或EOSRn时，禁止写入PODRn、PORRn和POSRn。

Note: EORRn和EOSRn不应同时设置。

18.2.5 PmnPFS/PmnPFS_HA/PmnPFS_BY : Port mn Pin Function Select Register (m = 0, 2, A to E, n = 00 to 15)

Base address: PFS_B = 0x4001_F800

Offset address: 0x000 + 0x040 × m + 0x004 × n (m = 0, 2, A to E)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASEL	ISEL	EOFR[1:0]		DSCR[1:0]		—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
Value after reset:	0*1	0	0	0	0	0*1	0	0	0	0	0	0*1	0	0	x	0

Bit	Symbol	Function	R/W
0	PODR	Port Output Data 0: Low output 1: High output	R/W*5
1	PIDR	Pmn State 0: Low level 1: High level	R*6
2	PDR	Port Direction 0: Input (functions as an input pin) 1: Output (functions as an output pin)	R/W*7
3	—	This bit is read as 0. The write value should be 0.	R/W
4	PCR	Pull-up Control 0: Disable input pull-up 1: Enable input pull-up	R/W*7
5	—	This bit is read as 0. The write value should be 0.	R/W
6	NCODR	N-Channel Open-Drain Control 0: CMOS output 1: NMOS open-drain output	R/W*7
9:7	—	These bits are read as 0. The write value should be 0.	R/W
11:10	DSCR[1:0]	Port Drive Capability 0 0: Low drive 0 1: Middle drive 1 0: High-speed high-drive*2 / High current drive*3 1 1: High drive	R/W*7
13:12	EOFR[1:0]	Event on Falling/Event on Rising*4 0 0: Don't care 0 1: Detect rising edge 1 0: Detect falling edge 1 1: Detect both edges	R/W*7
14	ISEL	IRQ Input Enable 0: Not used as an IRQn input pin 1: Used as an IRQn input pin	R/W*7
15	ASEL	Analog Input Enable 0: Not used as an analog pin 1: Used as an analog pin	R/W*7
16	PMR	Port Mode Control 0: Used as a general I/O pin 1: Used as an I/O port for peripheral functions	R/W*7
23:17	—	These bits are read as 0. The write value should be 0.	R/W

18.2.5 PmnPFSPmnPFS_HAPmnPFS_BY:端口mn引脚功能选择寄存器(m=0 2 AtoE n=00to 15)

Base address: PFS_B = 0x4001_F800

Offset address: 0x000 + 0x040 × m + 0x004 × n (m = 0, 2, A to E)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASEL	ISEL	EOFR[1:0]		DSCR[1:0]		—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
重置后的值:	0*1	0	0	0	0	0*1	0	0	0	0	0	0*1	0	0	x	0

Bit	Symbol	Function	R/W
0	PODR	端口输出数据 0：低输出1： 高输出	R/W*5
1	PIDR	Pmn State 0：低电平1 ：高电平	R*6
2	PDR	港口方向 0：输入（用作输入引脚）1：输出（ 用作输出引脚）	R/W*7
3	—	该位读取为0。写入值应为0。	R/W
4	PCR	Pull-up Control 0：禁止输入上拉1：使 能输入上拉	R/W*7
5	—	该位读取为0。写入值应为0。	R/W
6	NCODR	N-Channel Open-Drain Control 0: CMOS output 1: NMOS open-drain output	R/W*7
9:7	—	这些位被读取为0。写入值应为0。	R/W
11:10	DSCR[1:0]	端口驱动能力 00：低驱动01：中驱动10：高速高速驱动*2大电 流驱动*3 11：高驱动	R/W*7
13:12	EOFR[1:0]	下降事件上升事件*4 00：无关01：检测上升 沿10：检测下降沿11： 检测两个沿	R/W*7
14	ISEL	IRQ输入使能 0：不用作IRQn输入引脚1：用作I RQn输入引脚	R/W*7
15	ASEL	模拟输入使能 0：不用作模拟引脚1：用作模 拟引脚	R/W*7
16	PMR	端口模式控制 0：用作通用IO引脚1：用作外围功能的IO端口	R/W*7
23:17	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
28:24	PSEL[4:0]	Peripheral Select These bits select the peripheral function. For individual pin functions, see the associated tables in this chapter.	R/W*7
31:29	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The initial value of P002, P201, PA00 to PA05, PA13 to PA15, PB02 and PB03 is not 0x0000_0000. P002, PA00 to PA05 and PB02 is 0x0000_8000, P201 is 0x0000_0010, PA13 is 0x0001_0410, PA14 and PA15 is 0x0001_0010, and PB03 is 0x0001_0400.
Note 2. Only pins that support high speed and high drive can be set. Setting for other pins are prohibited.
Note 3. Only pins that support high current drive can be set. Setting for other pins are prohibited.
Note 4. Supported by PORTn (n = B to E).
Note 5. If the security attribution is configured as Secure,
- Secure access is allowed,
- Non-secure read value is 0, but TrustZone access error is not generated,
- Non-secure write access is ignored, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure access are allowed.

Note 6. If the security attribution is configured as Secure,
- Secure read access is allowed,
- Non-secure read value is 0, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure read access are allowed.

Note 7. If the security attribution is configured as Secure,
- Secure access and Non-secure read access are allowed,
- Non-secure write access is ignored, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure access are allowed.

Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) is a 32-bit, 16-bit, or 8-bit read/write control register that selects the port mn pin function, and is accessed in 32-bit units. PmnPFS_HA (PmnPFS [15:0] bits) is accessed in 16-bit units. PmnPFS_BY (PmnPFS[7:0] bits) is accessed in 8-bit units.

The available Port mn pin depends on the product. For details, see Table 18.1

PODR bit (Port Output Data), PIDR bit (Port State), PDR bit (Port Direction)

The PDR, PIDR, and PODR bits serve the same function as the PCNTR. When these bits are read, the PCNTR value is read.

PCR bit (Pull-up Control)

The PCR bit enables or disables an input pull-up resistor on the individual port pins. When a pin is in the input state with the associated bit in PmnPFS.PCR set to 1, the pull-up resistor connected to the pin is enabled. When a pin is set as a general port output pin, or a peripheral function output pin, the pull-up resistor for the pin is disabled regardless of the PCR setting. The pull-up resistor is also disabled in the reset state. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

NCODR bit (N-Channel Open-Drain Control)

The NCODR bit specifies the output type for the port pins. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

DSCR[1:0] bits (Port Drive Capability)

The DSCR[1:0] bits switches the drive capacity of the port. If the drive capacity of a pin is fixed, the associated bit is a read/write bit, but the drive capacity cannot be changed. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

EOFR[1:0] bits (Event on Falling/Event on Rising)

The EOFR[1:0] bits select the edge detection method for the port group input signal. These bits support rising, falling, or both edge detections. When the EOFR[1:0] bits are set to 01b, 10b, or 11b, the input enable of the I/O cell is asserted. Following that, the event pulse is input from the external pin, and the GPIO outputs the event pulse to the ELC. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

ISEL bit (IRQ Input Enable)

The ISEL bit specifies IRQ input pins. An IRQn (external pin interrupt) of the same number must only be enabled for one pin. The ISEL bit for an unspecified IRQn is reserved.

Bit	Symbol	Function	R/W
28:24	PSEL[4:0]	外设选择 这些位选择外设功能。对于各个引脚功能，请参见本章中的相关表格。	R/W*7
31:29	—	这些位被读取为0。写入值应为0。	R/W

注1.P002、P201、PA00～PA05、PA13～PA15、PB02、PB03的初始值不是0x0000_0000。P002，PA00到PA05和PB02是0x0000_8000，P201是0x0000_0010，PA13是0x0001_0410，PA14和PA15是0x0001_0010，PB03是0x0001_0400。
注2.只能设置支持高速和高驱动的引脚。禁止设置其他引脚。
注3.只能设置支持大电流驱动的引脚。禁止设置其他引脚。
注4.受PORTn支持（n=B到E）。
注5.如果安全属性配置为Secure，●
允许安全访问，
- 非安全读取值为0，但不会产生TrustZone访问错误，
- 忽略非安全写入访问，但不会生成TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全访问。
注6.如果安全属性配置为Secure，●
允许安全读取访问，
- 非安全读取值为0，但不会产生TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全读取访问。
注7.如果安全属性配置为Secure，●
允许安全访问和非安全读取访问，
- 忽略非安全写入访问，但不会生成TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全访问。

端口mn引脚功能选择寄存器（PmnPFSPmnPFS_HAPmnPFS_BY）是选择端口mn引脚功能的32位、16位或8位读写控制寄存器，以32位为单位进行访问。PmnPFS_HA（PmnPFS[15:0]位）以16位为单位进行访问。PmnPFS_BY（PmnPFS[7:0]位）以8位为单位进行访问。

可用的端口mn引脚取决于产品。详见表18.1

PODR位（端口输出数据）、PIDR位（端口状态）、PDR位（端口方向）

PDR、PIDR和PODR位的功能与PCNTR相同。读取这些位时，将读取PCNTR值。

PCR bit (Pull-up Control)

PCR位启用或禁用各个端口引脚上的输入上拉电阻。当引脚处于输入状态且PmnPFS.PCR中的相关位设置为1时，连接到该引脚的上拉电阻被启用。当引脚设置为通用端口输出引脚或外围功能输出引脚时，无论PCR设置如何，该引脚的上拉电阻都被禁用。上拉电阻在复位状态下也被禁用。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

NCODR bit (N-Channel Open-Drain Control)

NCODR位指定端口引脚的输出类型。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

DSCR[1:0]位（端口驱动能力）

DSCR[1:0]位切换端口的驱动能力。如果某个管脚的驱动能力是固定的，那么相关的位就是一个读写位，但是驱动能力是不能改变的。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

EOFR[1:0]位（下降事件事件上升事件）

EOFR[1:0]位选择端口组输入信号的边沿检测方法。这些位支持上升沿、下降沿或两个边沿检测。当EOFR[1:0]位设置为01b、10b或11b时，IO单元的输入使能有效。随后，事件脉冲从外部引脚输入，GPIO将事件脉冲输出到ELC。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

ISEL位（IRQ输入使能）

ISEL位指定IRQ输入引脚。一个相同数量的IRQn（外部引脚中断）只能为一个引脚启用。未指定的IRQn的ISEL位被保留。

ASEL bit (Analog Input Enable)

The ASEL bit specifies analog pins. When a pin is set as an analog pin by this bit:

1. Specify it as a general I/O port in the Port Mode Control bit (PmnPFS.PMR).
2. Disable the pull-up resistor in the Pull-up Control bit (PmnPFS.PCR).
3. Specify the input in the Port Direction bit (PmnPFS.PDR). The pin state cannot be read at this point. The PmnPFS register is protected by the Write-Protect Register (PWPR). Release write-protect before modifying the register.

The ASEL bit for an unspecified analog I/O pin is reserved.

PMR bit (Port Mode Control)

The PMR bit specifies the port pin function. Bits associated with non-existent pins are reserved. The write value should be 0.

PSEL[4:0] bits (Peripheral Select)

The PSEL[4:0] bits assign the peripheral function.

18.2.6 PWPR : Write-Protect Register

Base address: PFS_B = 0x4001_F800

Offset address: 0x50C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	PFSWE	PmnPFS Register Write Enable 0: Writing to the PmnPFS register is disabled 1: Writing to the PmnPFS register is enabled	R/W
7	B0WI	PFSWE Bit Write Disable 0: Writing to the PFSWE bit is enabled 1: Writing to the PFSWE bit is disabled	R/W

PFSWE bit (PmnPFS Register Write Enable)

Writing to the PmnPFS register is enabled only when the PFSWE bit is set to 1. You must first write 0 to the B0WI bit before setting PFSWE to 1.

B0WI bit (PFSWE Bit Write Disable)

Writing to the PFSWE bit is enabled only when the B0WI bit is set to 0.

18.2.7 PWPRS : Write-Protect Register for Secure

Base address: PFS_B = 0x4001_F800

Offset address: 0x514

Bit position:	7	6	5	4	3	2	1	0
Bit field:	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W

ASEL位（模拟输入使能）

ASEL位指定模拟引脚。当一个引脚被该位设置为模拟引脚时：

1.在端口模式控制位(PmnPFS.PMR)中将其指定为通用IO端口。

2.在上拉控制位(PmnPFS.PCR)中禁用上拉电阻。

3.在端口方向位(PmnPFS.PDR)中指定输入。此时无法读取引脚状态。PmnPFS寄存器受写保护寄存器(PWPR)保护。在修改寄存器之前释放写保护。

未指定的模拟IO引脚的ASEL位被保留。

PMR位（端口模式控制）

PMR位指定端口引脚功能。与不存在的引脚相关的位被保留。写入值应为0。

PSEL[4:0] bits (Peripheral Select)

PSEL[4:0]位分配外设功能。

18.2.6 PWPR : Write-Protect Register

Base address: PFS_B = 0x4001_F800

Offset address: 0x50C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	B0WI	PFSWE	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	这些位被读取为0。写入值应为0。	R/W
6	PFSWE	PmnPFS寄存器写使能 0：禁止写入PmnPFS寄存器1：允许写入PmnPFS寄存器	R/W
7	B0WI	PFSWE位写入禁用 0：允许写入PFSWE位1：禁止写入PFSWE位	R/W

PFSWE位（PmnPFS寄存器写使能）

仅当PFSWE位设置为1时才允许写入PmnPFS寄存器。您必须先将0写入B0WI位，然后再将PFSWE设置为1。

B0WI位（PFSWE位写入禁用）

仅当B0WI位设置为0时才允许写入PFSWE位。

18.2.7 PWPRS:安全的写保护寄存器

Base address: PFS_B = 0x4001_F800

Offset address: 0x514

Bit position:	7	6	5	4	3	2	1	0
Bit field:	B0WI	PFSWE	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
6	PFSWE	PmnPFS Register Write Enable 0: Disable writes to the PmnPFS register 1: Enable writes to the PmnPFS register	R/W
7	B0WI	PFSWE Bit Write Disable 0: Enable writes the PFSWE bit 1: Disable writes to the PFSWE bit	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

PFSWE bit (PmnPFS Register Write Enable)

Writing to the PmnPFS register of the IO port pin set as secure by the PmSAR register is enabled only when the PFSWE bit is set to 1. You must first write 0 to the B0WI bit before setting PFSWE to 1.

B0WI bit (PFSWE Bit Write Disable)

Writing to the PFSWE bit is enabled only when the B0WI bit is set to 0.

18.2.8 PmSAR : Port m Security Attribution register (m = 0, 2, A to E)

Base address: PFS_B = 0x4001_F800

Offset address: 0x530 + 0x004 × m

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PMNSA[15:0]															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	PMNSA[15:0]	Pmn Security Attribution Target I/O port pin : Pmn 0: Secure 1: Non Secure	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.
Note: m = 0, 2, A to E, n = 00 to 15

Port Security Attribution Register is a 16-bit register that setting the Security Attribution of the each port, the registers are accessed only in 16-bit units.

PMNSA[15:0] bits (Pmn Security Attribution)

The PmnSA bit specifies the Security Attribution of Pmn.

18.3 Operation

18.3.1 General I/O Ports

All pins except P002, PA00 to PA05, and PB02 operate as general I/O ports after reset. General I/O ports are organized as 16 bits per port and can be accessed by port with the Port Control Registers (PCNTRn, where n = 1 to 4), or by individual pins with the Port mn Pin Function Select register. For details on these registers, see section 18.2. Register Descriptions.

Each port has the following bits:

- Port Security Attribution register (PmSAR)(m = 0, 2, A to E), which indicates the security attribution.
- Port Direction bit (PDRn), which selects input or output direction
- Port Output Data bit (PODRn), which holds data for output
- Port Input Data bit (PIDRn), which indicates the pin states

Bit	Symbol	Function	R/W
6	PFSWE	PmnPFS寄存器写使能 0：禁止写入PmnPFS寄存器1：允许写入PmnPFS寄存器	R/W
7	B0WI	PFSWE位写入禁用 0：允许写入PFSWE位1：禁止写入PFSWE位	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

PFSWE位（PmnPFS寄存器写使能）

仅当PFSWE位设置为1时，才能写入由PmSAR寄存器设置为安全的IO端口引脚的PmnPFS寄存器。您必须先将0写入B0WI位，然后才能将PFSWE设置为1。

B0WI位（PFSWE位写入禁用）

仅当B0WI位设置为0时才允许写入PFSWE位。

18.2.8 PmSAR:端口m安全属性寄存器(m=0 2 AtoE)

Base address: PFS_B = 0x4001_F800

Offset address: 0x530 + 0x004 × m

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PMNSA[15:0]															
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	PMNSA[15:0]	Pmn安全属性目标IO端口引脚：Pmn 0：安全1：不安全	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。
Note: m = 0, 2, A to E, n = 00 to 15

端口安全属性寄存器是一个16位的寄存器，用于设置每个端口的安全属性，寄存器只能以16位为单位访问。

PMNSA[15:0]位（Pmn安全属性）

PmnSA位指定Pmn的安全属性。

18.3 Operation

18.3.1 通用IO端口

除P002、PA00至PA05和PB02外的所有引脚在复位后都作为通用IO端口工作。通用IO端口组织为每个端口16位，可以通过端口控制寄存器（PCNTRn，其中n=1到4）通过端口访问，或者通过端口mn引脚功能选择寄存器通过单个引脚访问。有关这些寄存器的详细信息，请参阅第18.2节。注册说明。

每个端口都有以下位：

- 端口安全属性寄存器(PmSAR)(m=0 2 AtoE)，表示安全属性。
- 端口方向位（PDRn），选择输入或输出方向
- 端口输出数据位(PODRn)，用于保存输出数据
- 端口输入数据位（PIDRn），指示引脚状态

- Event Input Data bit (EIDRn), which indicates the pin state when an ELC_PORTn (n = B, C, D or E) signal occurs
- Port Output Set bit (POSRn), which indicates the output value when a software write occurs
- Port Output Reset bit (PORRn), which indicates the output value when a software write occurs
- Event Output Set bit (EOSRn), which indicates the output value when an ELC_PORTn (n = B, C, D or E) signal occurs
- Event Output Reset bit (EORRn), which indicates the output value when an ELC_PORTn (n = B, C, D or E) signal occurs.

18.3.2 Port Function Select

The following port functions are available for configuring each pin:

- Security function: Security attribution for each pins
- I/O configuration: Complementary or open-drain output, pull-up control, and drive strength
- General I/O port: Port direction, output data setting, and read input data
- Alternate function: Configured function mapping to the pin.

Each pin is associated with a Port mn Pin Function Select register (PmnPFS), which includes the associated PODR, PIDR, and PDR bits. In addition, the PmnPFS register includes the following:

- PCR: Pull-up resistor control bit that turns the input pull-up MOS on or off
- NCODR: N-channel open-drain control bit that selects the output type for each pin
- DSCR[1:0]: Drive capacity control bit that selects the drive capacity
- EOFR[1:0]: For selecting the edge of the event that input from the port group
- ISEL: IRQ input enable bit to specify an IRQ input pin
- ASEL: Analog input enable bit to specify an analog pin
- PMR: Port mode bit to specify the pin function of each port
- PSEL[4:0]: Port function select bits to select the associated peripheral function.

These configurations can be made by a single-register access to the Port mn Pin Function Select register. For details, see section 18.2.5. PmnPFS/PmnPFS_HA/PmnPFS_BY : Port mn Pin Function Select Register (m = 0, 2, A to E, n = 00 to 15).

18.3.3 Port Group Function for ELC

In the MCU, Port B to Port E are assigned for the ELC port group function.

18.3.3.1 Behavior When ELC_PORTn (n = B, C, D or E) is Input from ELC

The MCU supports the two functions described in this section when an ELC_PORTn (n = B, C, D or E) signal comes from the ELC.

(1) Input to EIDR

For the GPI function (PDR = 0 and PMR = 0 in the PmnPFS register), when an ELC_PORTn (n = B, C, D or E) signal comes from the ELC, the input enable of the I/O cell is asserted, and data from the external pins is read into the EIDR bit. See Figure 18.2

For the GPO function (PDR = 1) or the peripheral mode (PMR = 1), 0 is input into the EIDR bit from the external pins.

●事件输入数据位（EIDRn），当ELC_PORTn（n=B、C、D或E）信号发生时指示引脚状态
●端口输出设置位（POSRn），表示发生软件写时的输出值
●端口输出复位位（PORRn），表示发生软件写入时的输出值
●事件输出设置位（EOSRn），表示发生ELC_PORTn（n=B、C、D或E）信号时的输出值
●事件输出复位位（EORRn），指示发生ELC_PORTn（n=B、C、D或E）信号时的输出值。

18.3.2 端口功能选择

以下端口功能可用于配置每个引脚：
●安全功能：每个引脚的安全属性
●IO配置：互补或开漏输出、上拉控制和驱动强度
●通用IO口：端口方向、输出数据设置、读取输入数据
●备用功能：配置的功能映射到引脚。

每个引脚都与一个端口mn引脚功能选择寄存器(PmnPFS)相关联，该寄存器包括相关的PODR、PIDR和PDR位。此外，PmnPFS寄存器包括以下内容：
●PCR：上拉电阻控制位，打开或关闭输入上拉MOS
●NCODR：N沟道开漏控制位，用于选择每个引脚的输出类型
●DSCR[1:0]：驱动容量控制位，选择驱动容量
●EOFR[1:0]：用于选择从端口组输入的事件的边沿
●ISEL：IRQ输入使能位，用于指定IRQ输入引脚
●ASEL：模拟输入使能位，用于指定模拟引脚
●PMR：端口模式位，指定每个端口的引脚功能
●PSEL[4:0]：端口功能选择位，用于选择相关的外设功能。

这些配置可以通过单个寄存器访问端口mn引脚功能选择寄存器来进行。详见18.2.5节。PmnPFSPmnPFS_HAPmnPFS_BY：端口mn引脚功能选择寄存器（m=0、2、A到E、n=00到15）。

18.3.3 ELC的端口组功能

在MCU中，端口B到端口E被分配用于ELC端口组功能。

18.3.3.1 当ELC_PORTn（n=B、C、D或E）从ELC输入时的行为

当ELC_PORTn（n=B、C、D或E）信号来自ELC时，MCU支持本节中描述的两种功能。

(1) 输入到EIDR

对于GPI功能（PmnPFS寄存器中的PDR=0和PMR=0），当ELC_PORTn（n=B、C、D或E）信号来自ELC时，IO单元的输入使能有效，并且数据从外部引脚读入EIDR位。见图18.2

对于GPO功能(PDR=1)或外设模式(PMR=1)，0从外部引脚输入到EIDR位。

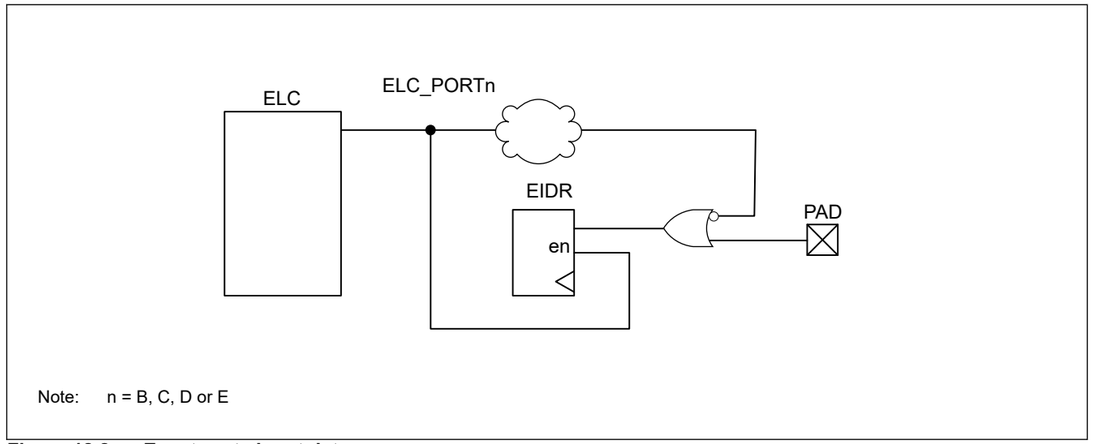


Figure 18.2 Event ports input data

(2) Output from PODR by EOSR and EORR

When an ELC_PORTn (n = B, C, D or E) signal occurs, the data is output from the PODR to the external pin based on the settings in the EOSR and EORR registers.

- If EOSR is set to 1, when an ELC_PORTn (n = B, C, D or E) signal occurs, the PODR register outputs 1 to the external pin. Otherwise, when EOSR = 0, the PODR value is retained.
- If EORR is set to 1, when ELC_PORTn (n = B, C, D or E) signal occurs, the PODR register outputs 0 to the external pin. Otherwise, when EORR = 0, the PODR value is retained.

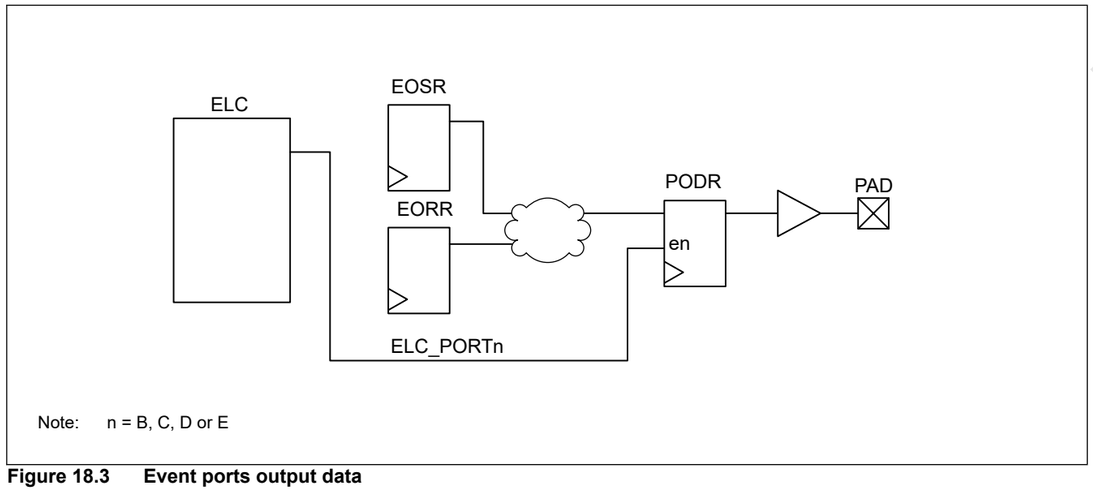


Figure 18.3 Event ports output data

18.3.3.2 Behavior When an Event Pulse is Output to ELC

To output the event pulse from the external pins to the ELC, set the EOFR[1:0] bits in the PmnPFS register. For details, see section 18.2.5. PmnPFS/PmnPFS_HA/PmnPFS_BY : Port mn Pin Function Select Register (m = 0, 2, A to E, n = 00 to 15). When the EOFR[1:0] bits are set, the input enable of the I/O cell is asserted.

Data from the external pin is the input. For example, for Port E, when the data is input from PE00 to PE15, the data of those 16 pins is organized by OR logic. This data is formed into a one-shot pulse that goes to the ELC. The operation of PORTn (n = B to D) is also the same as Port E. See Figure 18.4.

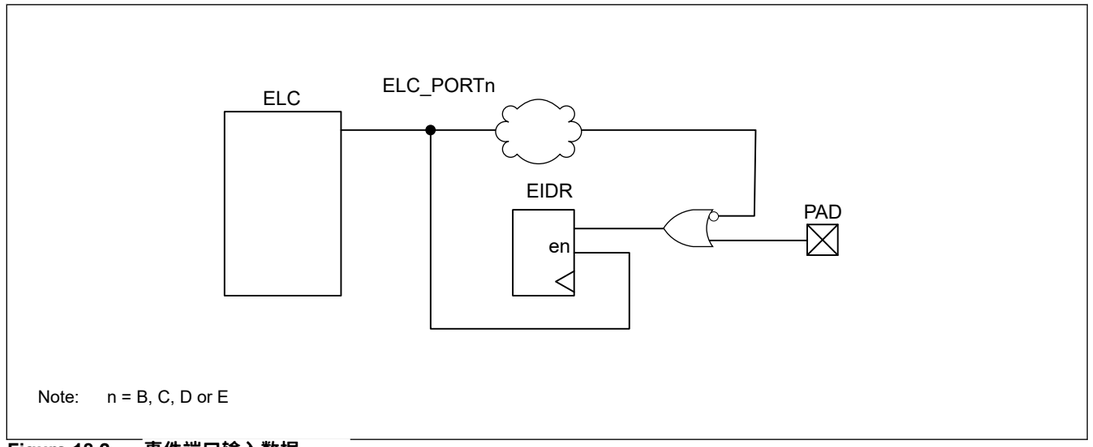


Figure 18.2 事件端口输入数据

(2) EOSR和EORR从PODR输出

当ELC_PORTn（n=B、C、D或E）信号发生时，数据会根据EOSR和EORR寄存器中的设置从PODR输出到外部引脚。

●如果EOSR设置为1，当ELC_PORTn（n=B、C、D或E）信号发生时，PODR寄存器输出1到外部引脚。否则，当EOSR=0时，保留PODR值。

●如果EORR设置为1，当ELC_PORTn（n=B、C、D或E）信号发生时，PODR寄存器输出0到外部引脚。否则，当EORR=0时，保留PODR值。

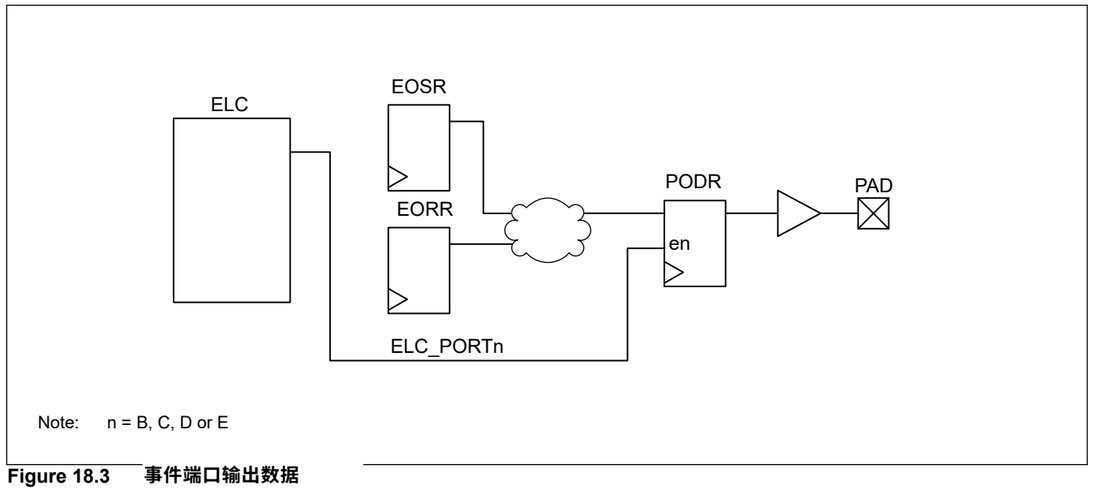


Figure 18.3 事件端口输出数据

18.3.3.2 事件脉冲输出到ELC时的行为

要将事件脉冲从外部引脚输出到ELC，请设置PmnPFS寄存器中的EOFR[1:0]位。详见18.2.5节。PmnPFSPmnPFS_HAPmnPFS_BY：端口mn引脚功能选择寄存器（m=0、2、A到E、n=00到15）。当EOFR[1:0]位被置位时，IO单元的输入使能被置位。

来自外部引脚的数据是输入。例如，对于端口E，当数据从PE00输入到PE15时，这16个引脚的数据由OR逻辑组织。该数据形成一个单次脉冲，该脉冲进入ELC。PORTn（n=B到D）的操作也与端口E相同。参见图18.4。

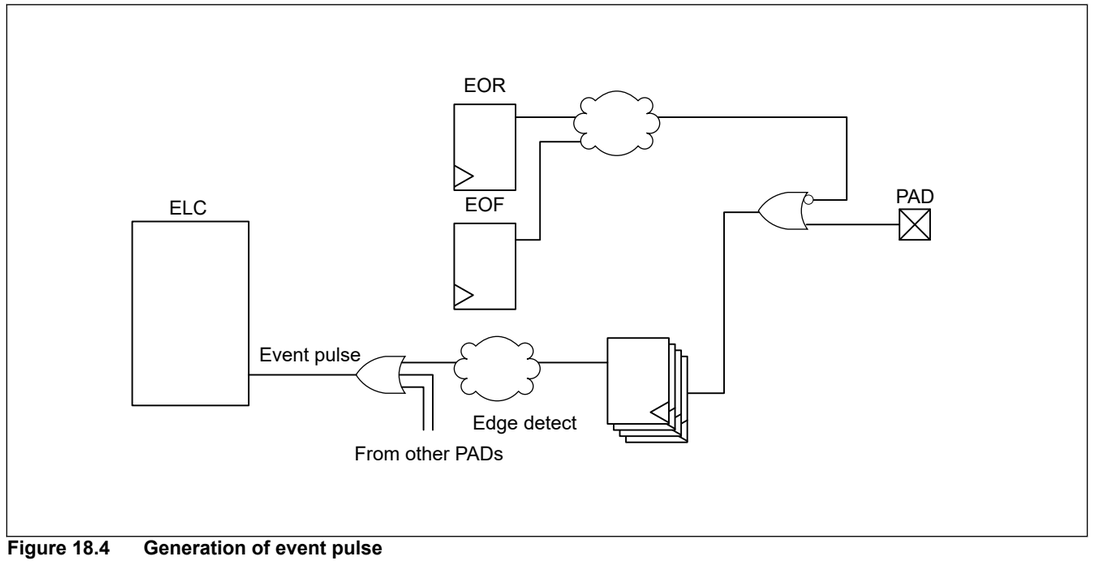


Figure 18.4 Generation of event pulse

18.4 Handling of Unused Pins

Table 18.3 shows how to handle unused pins.

Table 18.3 Handling of unused pins

Pin name	Description
MD	Use as a mode selection pin
RES	Connect to VCC through a resistor (pulling up)
PC13/NM1	Connect to VCC through a resistor (pulling up)
EXTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P212). When this pin is not used as port P212, configure it in the same way as ports A to E.
XTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P213). When the external clock is input to the EXTAL pin, the XTAL pin functions as P213. When this pin is not used as port P213, configure it in the same way as ports A to E.
P000, P001 PA00, PA02, PA04, PA06, PA07 PB00 to PB02 PC00 to PC05	Connect to AVCC0 (pulled up) through a resistor or to AVSS0 (pulled down) through a resistor*1
P002 PA01, PA03, PA05	Connect to AVCC0 (pulling up) through a resistor
Other ports	• If the direction is set to input (PCNTR1.PDRn = 0), connect the associated pin to VCC (pulled up) through a resistor or to VSS (pulled down) through a resistor.*1 *2 • If the direction is set to output (PCNTR1.PDRn = 1), keep pin open.*1 *3
VREFH0	Connect to AVCC0
VREFL0	Connect to AVSS0

Note 1. Clear the PmnPFS.PMR, PmnPFS.ISEL, PmnPFS.PCR, and PmnPFS.ASEL bits to 0.
Note 2. PA13 to PA15 are recommended for pull up VCC (pulled up) through a resistor, because these pins are input pull-up enabled from the initial value (PmnPFS.PCR = 1).
Note 3. PB03 is recommended for setting the direction to output (PCNTR1.PDRn = 1), because this pin is output from the initial value.

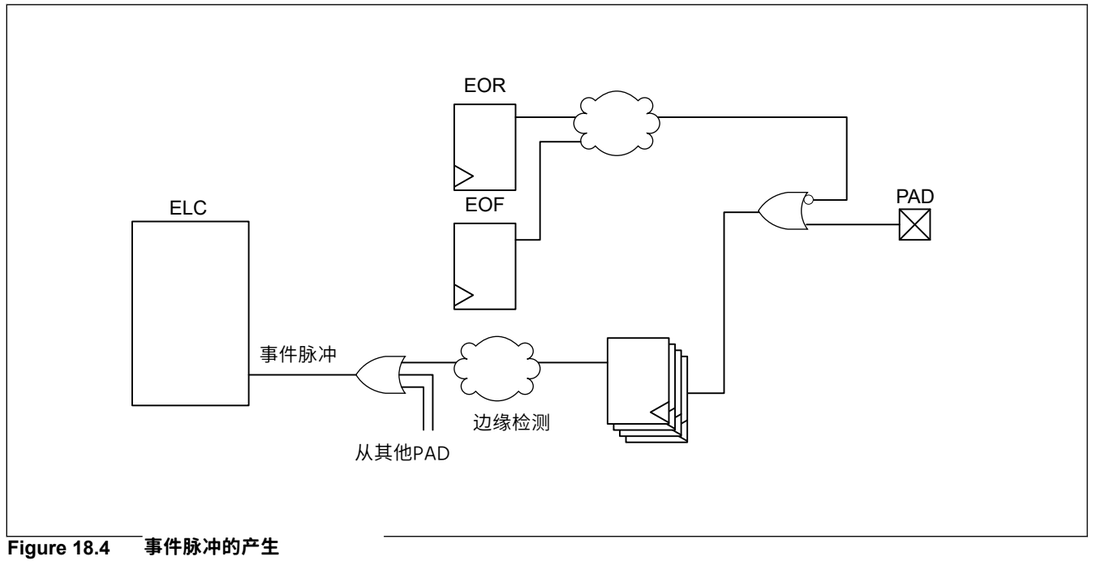


Figure 18.4 事件脉冲的产生

18.4 未使用引脚的处理

表18.3显示了如何处理未使用的引脚。

Table 18.3 处理未使用的引脚

引脚名称	Description
MD	用作模式选择引脚
RES	通过一个电阻连接到VCC（上拉）
PC13/NM1	通过一个电阻连接到VCC（上拉）
EXTAL	不使用主时钟振荡器时，将MOSCCR.MOSTP位设置为1（通用端口P212）。当该管脚不作为端口P212使用时，配置方法与端口A到E相同。
XTAL	不使用主时钟振荡器时，将MOSCCR.MOSTP位设置为1（通用端口P213）。当外部时钟输入到EXTAL引脚时，XTAL引脚起到P213的作用。当该管脚不作为端口P213使用时，配置方法与端口A到E相同。
P000, P001 PA00, PA02, PA04, PA06, PA07 PB00 to PB02 PC00 to PC05	通过电阻连接到AVCC0（上拉）或通过电阻连接到AVSS0（下拉）*1
P002 PA01, PA03, PA05	通过一个电阻连接到AVCC0（上拉）
其他端口	• 如果方向设置为输入(PCNTR1.PDRn=0)，则通过电阻将相关引脚连接到VCC（上拉）或通过电阻连接到VSS（下拉）。*1*2 • 如果方向设置为输出(PCNTR1.PDRn=1)，则保持引脚开路。*1*3
VREFH0	连接到AVCC0
VREFL0	连接到AVSS0

注1.将PmnPFS.PMR、PmnPFS.ISEL、PmnPFS.PCR和PmnPFS.ASEL位清零。
注2.PA13至PA15建议通过电阻上拉VCC（上拉），因为这些引脚从初始值（PmnPFS.PCR=1）开始输入上拉使能。

注3.PB03推荐用于设置输出方向（PCNTR1.PDRn=1），因为该引脚是从初始值输出的。

18.5 Usage Notes

18.5.1 Procedure for Specifying the Pin Functions

To specify the I/O pin functions:

1. Clear the B0WI bit in the PWPR register. This enables writing to the PFSWE bit in the PWPR register.*1
2. Set 1 to the PFSWE bit in the PWPR register. This enables writing to the PmnPFS register.*1
3. Clear the Port Mode Control bit in the PMR to 0 for the target pin to select the general I/O port.
4. Specify the I/O function for the pin through the PSEL[4:0] bits settings in the PmnPFS register.
5. Set the PMR bit to 1 as required to switch to the selected I/O function for the pin.
6. Clear the PFSWE bit in the PWPR register. This disables writing to the PmnPFS register.*1
7. Set 1 to the B0WI bit in the PWPR register. This disables writing to the PFSWE bit in the PWPR register.*1

Note 1. When the security attribution of Pmn is set to 0, set the PWPRS register to write to the PmnPFS register.

18.5.2 Procedure for Using Port Group Input

To use the port group input (port n (n = B to E)):

1. Set the ELSRx.ELS[8:0] bits to all 0 to ignore unexpected pulses. For more information, see section 17, Event Link Controller (ELC).
2. Set the EOFR[1:0] bits of the PmnPFS register to specify the rising, falling, or both edge detections.
3. Execute a dummy read or wait for a short time, for example 100 ns. Ignoring of unexpected pulses depends on the initial value of the external pin.
4. Set the ELSRx.ELS[8:0] bits to enable the event signals.

18.5.3 Port Output Data Register (PODR) Summary

This register outputs data as follows:

1. Outputs 0 if PCNTR4.EORR is set to 1 when ELC_PORTn (n = B, C, D or E) signal occurs.
2. Outputs 1 if PCNTR4.EOSR is set to 1 when ELC_PORTn (n = B, C, D or E) signal occurs.
3. Outputs 0 if PCNTR3.PORR is set to 1.
4. Outputs 1 if PCNTR3.POSR is set to 1.
5. Outputs 0 or 1 because PCNTR1.PODRn is set.
6. Outputs 0 or 1 because PmnPFS.PODRn is set.

Numbers in this list correspond to the priority for writing to the PODRn. For example, if 1. and 3. from the list occur at the same time, the higher priority event 1. is executed.

18.5.4 Notes on Using Analog Functions

To use an analog function, set the Port Mode Control bit (PMR) and the Port Direction bit (PDRn) to 0 so that the pin acts as a general input port. Next, set the Analog Input Enable bit (ASEL) in the Port mn Pin Function Select Register (PmnPFS.ASEL) to 1.

The pin to which the PGA function (PGAINn, PGAVSSn (n = 0 to 3)) is assigned cannot be used as general ports when the PGA is set to pseudo differential mode.

When using the corresponding pin as general ports, set the corresponding PGA to single-ended input mode (see section 36.3.13.2. PGA operation setting).

Then, set the corresponding pin to function as general ports.

18.5 使用说明

18.5.1 指定引脚功能的步骤

要指定IO引脚功能：

1.将PWPR寄存器中的B0WI位清零。这允许写入PWPR寄存器中的PFSWE位。*1

2.将PWPR寄存器中的PFSWE位设置为1。这允许写入PmnPFS寄存器。*1

3.将PMR中的PortModeControl位清为0，以便目标引脚选择通用IO端口。

4.通过PmnPFS寄存器中的PSEL[4:0]位设置指定引脚的IO功能。

5.根据需要将PMR位设置为1，以切换到为引脚选择的IO功能。

6.将PWPR寄存器中的PFSWE位清零。这将禁止写入PmnPFS寄存器。*1

7.将PWPR寄存器中的B0WI位设置为1。这将禁止写入PWPR寄存器中的PFSWE位。*1

注1.当Pmn的安全属性设置为0时，设置PWPRS寄存器写入PmnPFS寄存器。

18.5.2 使用端口组输入的过程

要使用端口组输入（端口n（n=B到E））：

1.将ELSRx.ELS[8:0]位设置为全0以忽略意外脉冲。有关详细信息，请参阅第17节，事件链接控制器(ELC)。

2.设置PmnPFS寄存器的EOFR[1:0]位以指定上升沿、下降沿或两个边沿检测。

3.执行虚拟读取或等待一小段时间，例如100ns。忽略意外脉冲取决于外部引脚的初始值。

4.设置ELSRx.ELS[8:0]位以启用事件信号。

18.5.3 端口输出数据寄存器(PODR)摘要

该寄存器输出数据如下：

1.如果在ELC_PORTn（n=B、C、D或E）信号发生时PCNTR4.EORR设置为1，则输出0。

2.如果PCNTR4.EOSR在ELC_PORTn（n=B、C、D或E）信号发生时设置为1，则输出1。

3.如果PCNTR3.PORR设置为1，则输出0。

4.如果PCNTR3.POSR设置为1，则输出1。

5.输出0或1，因为PCNTR1.PODRn已设置。

6.输出0或1，因为PmnPFS.PODRn已设置。

此列表中的数字对应于写入PODRn的优先级。例如，如果列表中的1.和3.同时发生，则执行优先级较高的事件1.。

18.5.4 使用模拟功能的注意事项

要使用模拟功能，请将端口模式控制位(PMR)和端口方向位(PDRn)设置为0，以便引脚用作通用输入端口。接下来，将端口mn引脚功能选择寄存器(PmnPFS.ASEL)中的模拟输入启用位(ASEL)设置为1。

PGA功能(PGAINn PGAVSSn(n=0to3))的引脚不能用作通用端口，当
PGA设置为伪差分模式。

将对应引脚用作通用端口时，将对应的PGA设置为单端输入模式（见36.3.13.2.PGA操作设置）。

然后，将相应的引脚设置为通用端口。

18.6 Peripheral Select Settings for Each Product

This section describes the pin function select configuration using the PmnPFS register. Some pin names have added _A, _B, _C, _D, _E or _F suffixes. When assigning IIC and SPI functionality, select the functional pins having the same suffix. The other pins can be selected regardless of the suffix. Assigning the same function to two or more pins simultaneously is prohibited.

1. In Pmn pin function select register(PmnPFS), the PSEL bits have to be set when the PMR bit of the target pin is 0. If the PSEL bits are set when the PMR bit is 1, the unexpected edges may be input at the input function or the unexpected pulses may be output to the external pin at the output function.
2. Only the allowed values (functions) should be specified in the PSEL bits of PmnPFS register. If a value which is not allowed for the register is specified, the correct operation is not guaranteed.
3. The single function should not be assigned to the multiple pins by PmnPFS register.
4. The PORT0 and A, B, C, E have the analog functions such as A/D converter. When these pins are used as an analog function, for avoiding the loss of resolution, the PMR bit should be set to 0 and PDR bit should be set to 0. After that, ASEL bit should be set to 1

Table 18.4 Register settings for input/output pin function (PORT0)

PSEL[4:0] settings	Function	pin		
		P000	P001	P002
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z		
ASEL bit		AN016/IVREF0	AN017/IVREF1	AN019/PGAVSS3
ISEL bit		IRQ0	IRQ2	—
DSCR[1:0] bits	Drive capacity control	—	—	—
NCODR bit	N-ch open-drain	—	—	—
PCR bit	Pull-up	✓	✓	—
100 pins product		✓	✓	✓
64 pins product		—	—	✓
48 pins product		—	—	—

✓: Available
—: Setting prohibited

Table 18.5 Register settings for input/output pin function (PORT2)

PSEL[4:0] settings	Function	Pin		
		P201	P212	P213
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z		
ASEL bit		—	—	—
ISEL bit		—	—	IRQ0
DSCR[1:0] bits	Drive capacity control	L*1	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓
100 pins product		✓	✓	✓
64 pins product		✓	✓	✓
48 pins product		✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. The driver strength of this port can not be controlled by PmnPFS.DSCR[1:0] bits.

Table 18.6 Register settings for input/output pin function (PORTA) (1 of 2)

PSEL[4:0] settings	Function	Pin															
		PA00	PA01	PA02	PA03	PA04	PA05	PA06	PA07	PA08	PA09	PA10	PA11	PA12	PA13	PA14	PA15
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z													TMS/SWDIO	TCK/SWCLK	TDI
00001b	AGT	—	—	—	—	—	—	—	—	AGTIO0	—	—	—	—	AGTO0	AGTO1	—
00010b	GPT	—	—	—	—	—	—	—	—	GTOUUP	GTOVUP	GTOWUP	GTETRGD	GTETRGB	—	—	GTETRGB

18.6 每个产品的外设选择设置

本节介绍使用PmnPFS寄存器的引脚功能选择配置。一些引脚名称添加了_A、_B、_C、_D、_E或_F后缀。分配IIC和SPI功能时，选择具有相同后缀的功能管脚。无论后缀如何，都可以选择其他引脚。禁止将相同的功能同时分配给两个或多个引脚。

1.在Pmn引脚功能选择寄存器（PmnPFS）中，当目标引脚的PMR位为0时，必须设置PSEL位。如果在PMR位为1时设置PSEL位，可能会在输入功能或意外脉冲可能会在输出功能处输出到外部引脚。

2.PmnPFS寄存器的PSEL位只能指定允许的值（功能）。如果指定了寄存器不允许的值，则不能保证正确操作。

3.PmnPFS寄存器不应将单一功能分配给多个引脚。

4.PORT0和A、B、C、E具有模数转换器等模拟功能。当这些引脚用作模拟功能时，为避免分辨率损失，PMR位应设置为0，PDR位应设置为0。之后，ASEL位应设置为1

Table 18.4 输入输出引脚功能（PORT0）的寄存器设置

PSEL[4:0] settings	Function	pin		
		P000	P001	P002
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z		
ASEL bit		AN016/IVREF0	AN017/IVREF1	AN019/PGAVSS3
ISEL bit		IRQ0	IRQ2	—
DSCR[1:0] bits	驱动容量控制	—	—	—
NCODR bit	N-ch open-drain	—	—	—
PCR bit	Pull-up	✓	✓	—
100针产品		✓	✓	✓
64针产品		—	—	✓
48针产品		—	—	—

:可用—:禁止设置

Table 18.5 输入输出引脚功能（PORT2）的寄存器设置

PSEL[4:0] settings	Function	Pin		
		P201	P212	P213
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z		
ASEL bit		—	—	—
ISEL bit		—	—	IRQ0
DSCR[1:0] bits	驱动容量控制	L*1	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓
100针产品		✓	✓	✓
64针产品		✓	✓	✓
48针产品		✓	✓	✓

:可用—:禁止设置

注1.此端口的驱动强度不能由PmnPFS.DSCR[1:0]位控制。

Table 18.6 输入输出引脚功能(PORTA)的寄存器设置(1of2)

PSEL[4:0] settings	Function	Pin															
		PA00	PA01	PA02	PA03	PA04	PA05	PA06	PA07	PA08	PA09	PA10	PA11	PA12	PA13	PA14	PA15
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z													TMS/SWDIO	TCK/SWCLK	TDI
00001b	AGT	—	—	—	—	—	—	—	—	AGTIO0	—	—	—	—	AGTO0	AGTO1	—
00010b	GPT	—	—	—	—	—	—	—	—	GTOUUP	GTOVUP	GTOWUP	GTETRGD	GTETRGB	—	—	GTETRGB

Table 18.6 Register settings for input/output pin function (PORTA) (2 of 2)

PSEL[4:0] settings	Function	Pin															
		PA00	PA01	PA02	PA03	PA04	PA05	PA06	PA07	PA08	PA09	PA10	PA11	PA12	PA13	PA14	PA15
00011b	GPT*1	—	—	—	—	—	—	—	—	GTIOC 8A	GTIOC 8B	GTIOC 9A	GTIOC 9B	GTCPP O0	—	—	—
00100b	SCI*3	—	—	—	—	—	—	—	—	SCK0_ A	TXD0_ A/ MOSI0 _A/ SDA0	RXD0_ A/ MISO0 _A/ SCL0	CTS0_ A	CTS0_ RTS0/ SS0_A	SCK0_ C	TXD0_ C/ MOSI0 _C/ SDA0	RXD0_ C/ MISO0 _C/ SCL0
00101b	SCI*3	—	—	—	—	—	—	—	—	SCK1_ C	—	—	RXD1_ C/ MISO1 _C/ SCL1	TXD1_ C/ MOSI1 _C/ SDA1	CTS1_ RTS1/ SS1_C	SCK9_ B	RXD9_ B/ MISO9 _B/ SCL9
00110b	SPI*2	—	—	—	—	—	—	—	—	SSLA1 _B	SSLA0 _B	RSPCK A_B	MOSIA _B	MISOA _B	—	—	SSLA0 _A
00111b	IIC*2	—	—	—	—	—	—	—	—	SCL0_ D	SCL1_ C	SDA1_ C	—	—	—	—	—
01000b	KINT	—	—	—	—	—	—	—	—	KR00	KR01	KR02	KR03	KR04	—	—	KR02
01001b	CLKOUT	—	—	—	—	—	—	—	—	CLKOU T	—	—	—	—	—	—	—
01010b	ADC	—	—	—	—	—	—	—	—	—	—	—	—	ADTRG 1	—	—	ADTRG 0
01100b	ACMPHS	—	—	—	—	—	—	—	—	CMPO UT2	CMPO UT3	CMPO UT0	CMPO UT1	—	—	—	CMPO UT012
01101b	SCI	—	—	—	—	—	—	—	—	DE1	—	—	—	—	DE1	DE9	—
01110b	SCI	—	—	—	—	—	—	—	—	DE0	—	—	—	DE0	DE0	—	—
10000b	CANFD	—	—	—	—	—	—	—	—	—	—	—	CTX0	CRX0	—	—	—
10100b	GPT*1	—	—	—	—	—	—	—	—	GTIOC 7B	GTIOC 8B	GTIOC 9B	GTETR GC	GTCPP O2	—	—	—
10101b	GPT*1	—	—	—	—	—	—	—	—	GTIOC 2A	GTIOC 2B	GTIOC 3A	GTIOC 3B	GTADS M0	—	—	GTADS M1
10110b	GPT*1	—	—	—	—	—	—	—	—	GTIOC 9A	GTIOC 7B	GTIOC 8B	—	GTCPP O7	—	—	GTCPP O4
11001b	CAC	—	—	—	—	—	—	—	—	—	—	—	—	CACRE F	—	—	—
ASEL bit		AN000/ PGAIN 0/ IVCMP 02/ IVCMP 03	AN001/ PGAVS S0	AN002/ PGAIN 1/ IVCMP 12/ IVCMP 13	AN003/ PGAVS S1	AN004/ PGAIN 2/ IVCMP 22/ IVCMP 23	AN005/ PGAVS S2	AN006/ DA0	AN007/ DA1	—	—	—	—	—	—	—	—
ISEL bit		IRQ0-DS	IRQ1	IRQ2	IRQ3	IRQ4	IRQ5	IRQ6	IRQ7	IRQ8	IRQ9	IRQ10	IRQ11	IRQ12	—	—	IRQ1
DSCR[1:0] bits	Drive capacity control	—	—	—	—	—	—	—	—	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC	L/M/H	L/M/H	L/M/H	L/M/H
NCODR	N-ch open-drain	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (tGTISK).

Note 2. Recommend using pins that have a letter appended to their names, for instance _A or _B or _C or _D, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.

Note 3. Recommend using pins that have a letter appended to their names, for instance _A or _B or _C, to indicate group membership. For details, see section 46, Electrical Characteristics.

Table 18.6 输入输出引脚功能(PORTA)的寄存器设置(2of2)

PSEL[4:0] settings	Function	Pin															
		PA00	PA01	PA02	PA03	PA04	PA05	PA06	PA07	PA08	PA09	PA10	PA11	PA12	PA13	PA14	PA15
00011b	GPT*1	—	—	—	—	—	—	—	—	GTIOC 8A	GTIOC 8B	GTIOC 9A	GTIOC 9B	GTCPP O0	—	—	—
00100b	SCI*3	—	—	—	—	—	—	—	—	SCK0_ A	TXD0_ A/ MOSI0 _A/ SDA0	RXD0_ A/ MISO0 _A/ SCL0	CTS0_ A	CTS0_ RTS0/ SS0_A	SCK0_ C	TXD0_ C/ MOSI0 _C/ SDA0	RXD0_ C/ MISO0 _C/ SCL0
00101b	SCI*3	—	—	—	—	—	—	—	—	SCK1_ C	—	—	RXD1_ C/ MISO1 _C/ SCL1	TXD1_ C/ MOSI1 _C/ SDA1	CTS1_ RTS1/ SS1_C	SCK9_ B	RXD9_ B/ MISO9 _B/ SCL9
00110b	SPI*2	—	—	—	—	—	—	—	—	SSLA1 _B	SSLA0 _B	RSPCK A_B	MOSIA _B	MISOA _B	—	—	SSLA0 _A
00111b	IIC*2	—	—	—	—	—	—	—	—	SCL0_ D	SCL1_ C	SDA1_ C	—	—	—	—	—
01000b	KINT	—	—	—	—	—	—	—	—	KR00	KR01	KR02	KR03	KR04	—	—	KR02
01001b	CLKOUT	—	—	—	—	—	—	—	—	CLKOU T	—	—	—	—	—	—	—
01010b	ADC	—	—	—	—	—	—	—	—	—	—	—	—	ADTRG 1	—	—	ADTRG 0
01100b	ACMPHS	—	—	—	—	—	—	—	—	CMPO UT2	CMPO UT3	CMPO UT0	CMPO UT1	—	—	—	CMPO UT012
01101b	SCI	—	—	—	—	—	—	—	—	DE1	—	—	—	—	DE1	DE9	—
01110b	SCI	—	—	—	—	—	—	—	—	DE0	—	—	—	DE0	DE0	—	—
10000b	CANFD	—	—	—	—	—	—	—	—	—	—	—	CTX0	CRX0	—	—	—
10100b	GPT*1	—	—	—	—	—	—	—	—	GTIOC 7B	GTIOC 8B	GTIOC 9B	GTETR GC	GTCPP O2	—	—	—
10101b	GPT*1	—	—	—	—	—	—	—	—	GTIOC 2A	GTIOC 2B	GTIOC 3A	GTIOC 3B	GTADS M0	—	—	GTADS M1
10110b	GPT*1	—	—	—	—	—	—	—	—	GTIOC 9A	GTIOC 7B	GTIOC 8B	—	GTCPP O7	—	—	GTCPP O4
11001b	CAC	—	—	—	—	—	—	—	—	—	—	—	—	CACRE F	—	—	—
ASEL bit		AN000/ PGAIN 0/ IVCMP 02/ IVCMP 03	AN001/ PGAVS S0	AN002/ PGAIN 1/ IVCMP 12/ IVCMP 13	AN003/ PGAVS S1	AN004/ PGAIN 2/ IVCMP 22/ IVCMP 23	AN005/ PGAVS S2	AN006/ DA0	AN007/ DA1	—	—	—	—	—	—	—	—
ISEL bit		IRQ0-DS	IRQ1	IRQ2	IRQ3	IRQ4	IRQ5	IRQ6	IRQ7	IRQ8	IRQ9	IRQ10	IRQ11	IRQ12	—	—	IRQ1
DSCR[1:0] bits	驱动容量控制	—	—	—	—	—	—	—	—	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC	L/M/H	L/M/H	L/M/H	L/M/H
NCODR	N沟道开漏	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

:可用一:禁止设置

注1.输出缓冲器有中驱动和高驱动两种。推荐使用相同的驱动缓冲器输出偏斜规格(tGTISK)。

注2.建议使用名称后附有字母的引脚，例如_A或_B或_C或_D，以指示组成员身份。对于接口，测量每组电气特性的交流部分。

注3.建议使用在名称后附加字母的引脚，例如_A或_B或_C，以指示组成员身份。有关详细信息，请参见第46节，电气特性。

Table 18.7 Register settings for input/output pin function (PORTB)

PSEL[4:0] settings	Function	pin														
		PB00	PB01	PB02	PB03	PB04	PB05	PB06	PB07	PB08	PB09	PB10	PB12	PB13	PB14	PB15
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z			TDO/SWO	Hi-Z										
00001b	AGT	—	—	—	AGTO1	AGTOA0	AGTOB0	AGTOA1	AGTOB1	AGTIO0	AGTIO1	—	—	—	—	—
00010b	GPT	—	—	—	—	—	GTIU	GTIV	GTIW	—	—	GTIU	GTETRGA	GTOULO	GTOVLO	GTOWLO
00011b	GPT*1	—	—	—	—	GTIOC4A	GTIOC4B	GTIOC5A	GTIOC5B	GTIOC6A	GTIOC6B	GTETRGB	GTIOC0A	GTIOC0B	GTIOC1A	GTIOC1B
00100b	SCI*3	—	—	—	TXD2_A/ MOSI2_A/ SDA2	RXD2_A/ MISO2_A/ SCL2	SCK2_A	TXD0_D/ MOSI0_D/ SDA0	RXD0_D/ MISO0_D/ SCL0	RXD4/ MISO4_C/ SCL4	TXD4/ MOSI4_C/ SDA4	TXD4_A/ MOSI4_A/ SDA4	SCK4_A	CTS4_A	CTS4_RTS4/ SS4_A	RXD4_A/ MISO4_A/ SCL4
00101b	SCI*3	—	—	—	TXD9_B/ MOSI9_B/ SDA9	RXD3_D/ MISO3_D/ SCL3	TXD3_D/ MOSI3_D/ SDA3	CTS3_RTS3/ SS3_D	CTS1_RTS1/ SS1_D	RXD1_D/ MISO1_D/ SCL1	TXD1_D/ MOSI1_D/ SDA1	CTS3_B	RXD3_B/ MISO3_B/ SCL3	TXD3_B/ MOSI3_B/ SDA3	SCK3_B	CTS3_RTS3/ SS3_B
00110b	SPI*2	—	—	—	RSPCKA_A	MISOA_A	MOSIA_A	—	—	—	—	—	SSLB0_A	RSPCKB_A	MISOB_A	MOSIB_A
00111b	IIC*2	—	—	—	—	—	—	SCL0_A	SDA0_A	SCL1_A	SDA1_A	—	—	—	SDA0_C	SCL0_C
01000b	KINT	—	—	—	KR03	KR04	KR05	KR06	KR07	KR00	KR01	—	—	—	—	—
01001b	CLKOUT	—	—	—	—	VCOUT	—	—	—	—	—	VCOUT	—	—	—	—
01010b	ADC	—	—	—	ADTRG1	—	—	—	—	—	—	—	ADTRG0	—	—	—
01100b	ACMPHS	—	—	—	CMPOUT3	—	—	—	—	—	—	—	—	—	—	—
01101b	SCI	—	—	—	—	—	—	DE3	DE1	—	—	—	—	—	DE3	DE3
01110b	SCI	—	—	—	—	—	DE2	—	—	—	—	—	DE4	—	DE4	—
10000b	CANFD	—	—	—	CRX0	CTX0	CRX0	CTX0	—	CRX0	CTX0	—	CRX0	CTX0	—	—
10100b	GPT*1	—	—	—	GTIOC4A	GTIOC5A	GTIOC6A	GTIOC4B	GTETRGC	GTIOC5B	—	GTETRGB	—	GTIOC7A	GTIOC8A	GTIOC9A
10101b	GPT*1	—	—	—	GTCPPO1	GTIOC0A	GTIOC0B	GTIOC1A	GTIOC1B	GTIOC2A	GTIOC2B	GTCPPO4	GTIOC4A	GTIOC5A	GTIOC6A	GTIOC4B
10110b	GPT	—	—	—	GTCPPO3	—	—	—	—	—	—	GTCPPO7	—	—	—	—
11001b	CAC	—	—	—	—	CACREF	—	—	—	—	—	CACREF	—	—	—	—
11101b + ASEL bit	PGAOUT*4	PGAOUT0	PGAOUT1	—	—	—	—	—	—	—	—	—	—	—	—	—
11110b + ASEL bit	PGAOUT*4	PGAOUT2	PGAOUT3	—	—	—	—	—	—	—	—	—	—	—	—	—
ASEL bit		AN008	AN009	AN018/ PGAIN3/ IVCMP32/ IVCMP33	—	—	—	—	—	—	—	AN028	—	—	—	—
ISEL bit		IRQ0	IRQ1	IRQ15-DS	IRQ0	IRQ13	IRQ3-DS	IRQ4-DS	IRQ5-DS	IRQ1-DS	IRQ2-DS	IRQ10-DS	IRQ2	IRQ3	IRQ4	IRQ5
DSCR[1:0] bits	Drive capacity control	—	—	—	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H/HC	L/M/H/HC	L/M/H/HC	L/M/H/HC
NCODR	N-ch open-drain	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓
48 pins product		✓	✓	—	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (tGTISK).

Note 2. Recommend using pins that have a letter appended to their names, for instance _A or _C, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.

Table 18.7 输入输出引脚功能（PORTB）的寄存器设置

PSEL[4:0] settings	Function	pin														
		PB00	PB01	PB02	PB03	PB04	PB05	PB06	PB07	PB08	PB09	PB10	PB12	PB13	PB14	PB15
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z			TDO/SWO	Hi-Z										
00001b	AGT	—	—	—	AGTO1	AGTOA0	AGTOB0	AGTOA1	AGTOB1	AGTIO0	AGTIO1	—	—	—	—	—
00010b	GPT	—	—	—	—	—	GTIU	GTIV	GTIW	—	—	GTIU	GTETRGA	GTOULO	GTOVLO	GTOWLO
00011b	GPT*1	—	—	—	—	GTIOC4A	GTIOC4B	GTIOC5A	GTIOC5B	GTIOC6A	GTIOC6B	GTETRGA	GTIOC0A	GTIOC0B	GTIOC1A	GTIOC1B
00100b	SCI*3	—	—	—	TXD2_A/ MOSI2_A/ SDA2	RXD2_A/ MISO2_A/ SCL2	SCK2_A	TXD0_D/ MOSI0_D/ SDA0	RXD0_D/ MISO0_D/ SCL0	RXD4/ MISO4_C/ SCL4	TXD4/ MOSI4_C/ SDA4	TXD4_A/ MOSI4_A/ SDA4	SCK4_A	CTS4_A	CTS4_RTS4/ SS4_A	RXD4_A/ MISO4_A/ SCL4
00101b	SCI*3	—	—	—	TXD9_B/ MOSI9_B/ SDA9	RXD3_D/ MISO3_D/ SCL3	TXD3_D/ MOSI3_D/ SDA3	CTS3_RTS3/ SS3_D	CTS1_RTS1/ SS1_D	RXD1_D/ MISO1_D/ SCL1	TXD1_D/ MOSI1_D/ SDA1	CTS3_B	RXD3_B/ MISO3_B/ SCL3	TXD3_B/ MOSI3_B/ SDA3	SCK3_B	CTS3_RTS3/ SS3_B
00110b	SPI*2	—	—	—	RSPCKA_A	MISOA_A	MOSIA_A	—	—	—	—	—	SSLB0_A	RSPCKB_A	MISOB_A	MOSIB_A
00111b	IIC*2	—	—	—	—	—	—	SCL0_A	SDA0_A	SCL1_A	SDA1_A	—	—	—	SDA0_C	SCL0_C
01000b	KINT	—	—	—	KR03	KR04	KR05	KR06	KR07	KR00	KR01	—	—	—	—	—
01001b	CLKOUT	—	—	—	—	VCOUT	—	—	—	—	—	VCOUT	—	—	—	—
01010b	ADC	—	—	—	ADTRG1	—	—	—	—	—	—	—	ADTRG0	—	—	—
01100b	ACMPHS	—	—	—	CMPOUT3	—	—	—	—	—	—	—	—	—	—	—
01101b	SCI	—	—	—	—	—	—	DE3	DE1	—	—	—	—	—	DE3	DE3
01110b	SCI	—	—	—	—	—	DE2	—	—	—	—	—	DE4	—	DE4	—
10000b	CANFD	—	—	—	CRX0	CTX0	CRX0	CTX0	—	CRX0	CTX0	—	CRX0	CTX0	—	—
10100b	GPT*1	—	—	—	GTIOC4A	GTIOC5A	GTIOC6A	GTIOC4B	GTETRGC	GTIOC5B	—	GTETRGB	—	GTIOC7A	GTIOC8A	GTIOC9A
10101b	GPT*1	—	—	—	GTCPPO1	GTIOC0A	GTIOC0B	GTIOC1A	GTIOC1B	GTIOC2A	GTIOC2B	GTCPPO4	GTIOC4A	GTIOC5A	GTIOC6A	GTIOC4B
10110b	GPT	—	—	—	GTCPPO3	—	—	—	—	—	—	GTCPPO7	—	—	—	—
11001b	CAC	—	—	—	—	CACREF	—	—	—	—	—	CACREF	—	—	—	—
11101b + ASEL bit	PGAOUT*4	PGAOUT0	PGAOUT1	—	—	—	—	—	—	—	—	—	—	—	—	—
11110b + ASEL bit	PGAOUT*4	PGAOUT2	PGAOUT3	—	—	—	—	—	—	—	—	—	—	—	—	—
ASEL bit		AN008	AN009	AN018/ PGAIN3/ IVCMP32/ IVCMP33	—	—	—	—	—	—	—	AN028	—	—	—	—
ISEL bit		IRQ0	IRQ1	IRQ15-DS	IRQ0	IRQ13	IRQ3-DS	IRQ4-DS	IRQ5-DS	IRQ1-DS	IRQ2-DS	IRQ10-DS	IRQ2	IRQ3	IRQ4	IRQ5
DSCR[1:0] bits	驱动容量控制	—	—	—	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H/HC	L/M/H/HC	L/M/H/HC	L/M/H/HC
NCODR	N沟道开漏	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓
48针产品		✓	✓	—	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓

:可用—:禁止设置

注1.输出缓冲器有中驱动和高驱动两种。推荐使用相同的驱动缓冲器输出偏斜规格(tGTISK)。

注2.建议使用在名称后附加字母的引脚，例如_A或_C，以表示组成员身份。对于接口，测量每组电气特性的交流部分。

Note 3. Recommend using pins that have a letter appended to their names, for instance _A or _B or _C or _D, to indicate group membership. For details, see section 46, Electrical Characteristics.
Note 4. The PGAOUTn (n = 0 to 3) function is selected when the ASEL bit of the corresponding pin = 1 and the PSEL [4:0] bits are the specified combination.When using the corresponding pin as PGAOUTn, do not use it with other analog pin functions.

Table 18.8 Register settings for input/output pin function (PORTC)

PSEL[4:0] settings	Function	pin															
		PC00	PC01	PC02	PC03	PC04	PC05	PC06	PC07	PC08	PC09	PC10	PC11	PC12	PC13	PC14	PC15
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z															
00001b	AGT	—	—	—	—	—	—	AGTO0	AGTEE0	AGTOA0	AGTOB0	AGTIO1	AGTOA1	AGTOB1	—	AGTIO0	AGTIO1
00010b	GPT	—	—	—	—	—	—	GTETRGD	GTETRGA	GTIV	GTIW	—	—	—	GTETRGD	GTETRGA	GTETRGB
00011b	GPT*1	—	—	—	—	—	—	GTIOC6A	GTIOC6B	GTIOC7A	GTIOC7B	—	—	—	—	GTIOC3A	GTIOC3B
00100b	SCI*3	—	—	—	—	—	—	TXD2_B/ MOSI2_B/ SDA2	RXD2_B/ MISO2_B/ SCL2	SCK2_B	CTS2_RTS2/ SS2_B	—	—	TXD4_B/ MOSI4_B/ SDA4	—	—	—
00101b	SCI*3	—	—	—	—	—	—	CTS9_RTS9/ SS9_C	CTS9_C	CTS3_RTS3/ SS3_C	CTS3_C	TXD1_B/ MOSI1_B/ SDA1	RXD1_B/ MISO1_B/ SCL1	SCK1_B	—	—	—
00110b	SPI*2	—	—	—	—	—	—	—	—	SSLA3_B	SSLA2_B	RSPCKB_B	MISOB_B	MOSIB_B	—	—	—
00111b	IIC*2	—	—	—	—	—	—	SCL1_E	SDA1_E	SCL0_E	SDA0_D/ SDA0_E	SCL0_B	SDA0_B	—	—	—	—
01000b	KINT	—	—	—	—	—	—	—	—	—	—	KR05	KR06	KR07	—	—	—
01001b	CLKOUT	—	—	—	—	—	—	—	—	—	CLKOUT	—	—	—	—	—	—
01010b	ADC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADTRG0	ADTRG1
01100b	ACMPHS	—	—	—	—	—	—	—	—	—	—	CMPOUT0	CMPOUT1	CMPOUT2	—	CMPOUT012	CMPOUT3
01101b	SCI	—	—	—	—	—	—	DE9	—	DE3	—	—	—	DE1	—	—	—
01110b	SCI	—	—	—	—	—	—	—	—	DE2	DE2	—	—	—	—	—	—
10100b	GPT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GTCPPO0	GTCPPO1
10101b	GPT*1	—	—	—	—	—	—	GTIOC5B	—	—	—	—	—	—	—	GTADSM0	GTADSM1
10110b	GPT*1	—	—	—	—	—	—	—	—	—	GTIOC8A	—	—	—	—	GTCPPO4	GTCPPO7
11001b	CAC	—	—	—	—	—	—	—	—	CACREF	—	—	—	—	—	—	—
11101b + ASEL bit	PGAOUT*4	PGAOUT0	PGAOUT1	PGAOUT2	PGAOUT3	—	—	—	—	—	—	—	—	—	—	—	—
ASEL bit		AN012/ IVCMP00	AN013/ IVCMP10	AN014/ IVCMP20	AN015/ IVCMP30	AN010/ DA2	AN011/ DA3	—	—	—	—	—	—	—	—	—	—
ISEL bit		IRQ11-DS	IRQ12-DS	IRQ13-DS	IRQ14-DS	IRQ10	IRQ11	IRQ6	IRQ7	IRQ8	IRQ9	IRQ6-DS	IRQ7-DS	IRQ8-DS	NMI	IRQ14	IRQ15
DSCR[1:0] bits	Drive capacity control	—	—	—	—	—	—	L/M/H/HC	L/M/H/HC	L/M/H/HC	L/M/H/HC	L/M/H	L/M/H	L/M/H	—	L*5	L*5
NCODR	N-ch open-drain	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	—	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48 pins product		—	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (tGTISK).

注3.建议使用名称后附有字母的引脚，例如_A或_B或_C或_D，以表示组成员身份。有关详细信息，请参见第46节，电气特性。

注4.当相应引脚的ASEL位=1和PSEL[4:0]位为指定组合时，选择PGAOUTn(n=0至3)功能。当使用相应引脚作为PGAOUTn时，请勿使用它与其他模拟引脚功能。

Table 18.8 输入输出引脚功能（PORTC）的寄存器设置

PSEL[4:0] settings	Function	pin															
		PC00	PC01	PC02	PC03	PC04	PC05	PC06	PC07	PC08	PC09	PC10	PC11	PC12	PC13	PC14	PC15
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z															
00001b	AGT	—	—	—	—	—	—	AGTO0	AGTEE0	AGTOA0	AGTOB0	AGTIO1	AGTOA1	AGTOB1	—	AGTIO0	AGTIO1
00010b	GPT	—	—	—	—	—	—	GTETRGD	GTETRGA	GTIV	GTIW	—	—	—	GTETRGD	GTETRGA	GTETRGB
00011b	GPT*1	—	—	—	—	—	—	GTIOC6A	GTIOC6B	GTIOC7A	GTIOC7B	—	—	—	—	GTIOC3A	GTIOC3B
00100b	SCI*3	—	—	—	—	—	—	TXD2_B/ MOSI2_B/ SDA2	RXD2_B/ MISO2_B/ SCL2	SCK2_B	CTS2_RTS2/ SS2_B	—	—	TXD4_B/ MOSI4_B/ SDA4	—	—	—
00101b	SCI*3	—	—	—	—	—	—	CTS9_RTS9/ SS9_C	CTS9_C	CTS3_RTS3/ SS3_C	CTS3_C	TXD1_B/ MOSI1_B/ SDA1	RXD1_B/ MISO1_B/ SCL1	SCK1_B	—	—	—
00110b	SPI*2	—	—	—	—	—	—	—	—	SSLA3_B	SSLA2_B	RSPCKB_B	MISOB_B	MOSIB_B	—	—	—
00111b	IIC*2	—	—	—	—	—	—	SCL1_E	SDA1_E	SCL0_E	SDA0_D/ SDA0_E	SCL0_B	SDA0_B	—	—	—	—
01000b	KINT	—	—	—	—	—	—	—	—	—	—	KR05	KR06	KR07	—	—	—
01001b	CLKOUT	—	—	—	—	—	—	—	—	—	CLKOUT	—	—	—	—	—	—
01010b	ADC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADTRG0	ADTRG1
01100b	ACMPHS	—	—	—	—	—	—	—	—	—	—	CMPOUT0	CMPOUT1	CMPOUT2	—	CMPOUT012	CMPOUT3
01101b	SCI	—	—	—	—	—	—	DE9	—	DE3	—	—	—	DE1	—	—	—
01110b	SCI	—	—	—	—	—	—	—	—	DE2	DE2	—	—	—	—	—	—
10100b	GPT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GTCPPO0	GTCPPO1
10101b	GPT*1	—	—	—	—	—	—	GTIOC5B	—	—	—	—	—	—	—	GTADSM0	GTADSM1
10110b	GPT*1	—	—	—	—	—	—	—	—	—	GTIOC8A	—	—	—	—	GTCPPO4	GTCPPO7
11001b	CAC	—	—	—	—	—	—	—	—	CACREF	—	—	—	—	—	—	—
11101b + ASEL bit	PGAOUT*4	PGAOUT0	PGAOUT1	PGAOUT2	PGAOUT3	—	—	—	—	—	—	—	—	—	—	—	—
ASEL bit		AN012/ IVCMP00	AN013/ IVCMP10	AN014/ IVCMP20	AN015/ IVCMP30	AN010/ DA2	AN011/ DA3	—	—	—	—	—	—	—	—	—	—
ISEL bit		IRQ11-DS	IRQ12-DS	IRQ13-DS	IRQ14-DS	IRQ10	IRQ11	IRQ6	IRQ7	IRQ8	IRQ9	IRQ6-DS	IRQ7-DS	IRQ8-DS	NMI	IRQ14	IRQ15
DSCR[1:0] bits	驱动容量控制	—	—	—	—	—	—	L/M/H/HC	L/M/H/HC	L/M/H/HC	L/M/H/HC	L/M/H	L/M/H	L/M/H	—	L*5	L*5
NCODR	N沟道开漏	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	—	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48针产品		—	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓	✓

:可用—:禁止设置

注1.输出缓冲器有中驱动和高驱动两种。推荐使用相同的驱动缓冲器输出偏斜规格(tGTISK)。

Note 2. Recommend using pins that have a letter appended to their names, for instance _B or _D or _E, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. Recommend using pins that have a letter appended to their names, for instance _B or _C, to indicate group membership. For details, see section 46, Electrical Characteristics.
Note 4. The PGAOUTn (n = 0 to 3) function is selected when the ASEL bit of the corresponding pin = 1 and the PSEL [4:0] bits are the specified combination.When using the corresponding pin as PGAOUTn, do not use it with other analog pin functions.
Note 5. The driver strength of this port can not be controlled by PmnPFS.DSCR[1:0] bits.

Table 18.9 Register settings for input/output pin function (PORTD)

PSEL[4:0] settings	Function	Pin															
		PD00	PD01	PD02	PD03	PD04	PD05	PD06	PD07	PD08	PD09	PD10	PD11	PD12	PD13	PD14	PD15
00000b (value after reset)	Hi-Z/ JTAG/SW D	Hi-Z															
00001b	AGT	—	—	AGTEE 1	—	—	—	—	—	—	—	—	—	—	—	—	—
00010b	GPT	—	—	—	—	—	—	—	—	—	—	GTETR GC	—	—	—	—	—
00011b	GPT*1	—	—	—	—	—	—	—	—	GTIOC 2A	GTIOC 2B	GTIOC 3A	GTIOC 3B	GTIOC 4A	GTIOC 4B	GTIOC 5A	GTIOC 5B
00100b	SCI*3	CTS2_ A	CTS2_ RTS2/ SS2_A	RXD4_ B/ MISO4 _B/ SCL4	SCK4_ B	CTS4_ RTS4/ SS4_B	—	—	—	CTS2_ B	CTS2_ RTS2/ SS2_B	SCK2_ C	RXD2_ C/ MISO2 _C/ SCL2	TXD2_ C/ MOSI2 _C/ SDA2	SCK4_ C	RXD4_ C/ MISO4 _C/ SCL4	TXD4_ C/ MOSI4 _C/ SDA4
00101b	SCI*3	RXD3_ C/ MISO3 _C/ SCL3	TXD3_ C/ MOSI3 _C/ SDA3	SCK3_ C	CTS9_ A	CTS9_ RTS9/ SS9_A	TXD9/ MOSI9 _A/ SDA9	RXD9_ A/ MISO9 _A/ SCL9	SCK9_ A	TXD1_ A/ MOSI1 _A/ SDA1	RXD1_ A/ MISO1 _A/ SCL1	SCK1_ A	CTS1_ A	CTS1_ RTS1/ SS1_A	SCK9_ C	RXD9_ C/ MISO9 _C/ SCL9	TXD9_ C/ MOSI9 _C/ SDA9
00110b	SPI*2	SSLB0 _B	SSLB1 _B	—	SSLB2 _B	SSLB3 _B	SSLA3 _A	SSLA2 _A	SSLA1 _A	SSLB1 _A	SSLB2 _A	SSLB3 _A	—	—	—	—	—
00111b	IIC*2	—	—	—	—	—	SDA1_ B	SCL1_ B	—	—	—	—	—	SCL1_ D	SDA1_ D	SCL0_ F	SDA0_ F
01000b	KINT	KR00	KR01	KR02	KR03	KR04	KR05	KR06	KR07	KR00	KR01	KR02	KR03	KR04	KR05	KR06	KR07
01001b	CLKOUT	—	—	CLKOU T	—	—	—	—	—	—	—	—	—	—	—	—	—
01100b	ACMPHS	—	—	CMPO UT3	CMPO UT0	CMPO UT1	—	—	—	—	—	—	—	—	—	—	—
01101b	SCI	—	—	DE3	—	DE9	—	—	DE9	—	—	DE1	—	DE1	DE9	—	DE9
01110b	SCI	—	DE2	—	DE4	DE4	—	—	—	—	DE2	DE2	—	—	DE4	—	—
10000b	CANFD	CRX0	CTX0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10101b	GPT	GTADS M0	GTADS M1	GTCPP O0	—	—	GTADS M0	—	GTADS M1	—	—	—	—	—	—	—	—
10110b	GPT	GTCPP O4	GTCPP O7	GTCPP O2	GTCPP O0	GTCPP O1	GTCPP O3	GTCPP O4	GTCPP O7	—	—	—	—	—	—	—	—
ISEL bit		—	—	IRQ9-DS	—	—	—	—	—	—	—	—	—	IRQ12	IRQ13	IRQ14	IRQ15
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC
NCODR	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64 pins product		—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—
48 pins product		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

✓: Available
—: Setting prohibited

Note 1. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (tGTISK).
Note 2. Recommend using pins that have a letter appended to their names, for instance _A or _B or _D or _F, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. Recommend using pins that have a letter appended to their names, for instance _A or _B or _C, to indicate group membership. For details, see section 46, Electrical Characteristics.

注2.建议使用在名称后附加字母的引脚，例如_B或_D或_E，以表示组成员身份。对于接口，测量每组电气特性的交流部分。

注3.建议使用在名称后附加字母的引脚，例如_B或_C，以指示组成员身份。有关详细信息，请参见第46节，电气特性。

注4.当相应引脚的ASEL位=1和PSEL[4:0]位为指定组合时，选择PGAOUTn(n=0至3)功能。当使用相应引脚作为PGAOUTn时，请勿使用它与其他模拟引脚功能。
注5.此端口的驱动强度不能由PmnPFS.DSCR[1:0]位控制。

Table 18.9 输入输出引脚功能（PORTD）的寄存器设置

PSEL[4:0] settings	Function	Pin															
		PD00	PD01	PD02	PD03	PD04	PD05	PD06	PD07	PD08	PD09	PD10	PD11	PD12	PD13	PD14	PD15
00000b (value after reset)	Hi-Z/ JTAG/SW D	Hi-Z															
00001b	AGT	—	—	AGTEE 1	—	—	—	—	—	—	—	—	—	—	—	—	—
00010b	GPT	—	—	—	—	—	—	—	—	—	—	GTETR GC	—	—	—	—	—
00011b	GPT*1	—	—	—	—	—	—	—	—	GTIOC 2A	GTIOC 2B	GTIOC 3A	GTIOC 3B	GTIOC 4A	GTIOC 4B	GTIOC 5A	GTIOC 5B
00100b	SCI*3	CTS2_ A	CTS2_ RTS2/ SS2_A	RXD4_ B/ MISO4 _B/ SCL4	SCK4_ B	CTS4_ RTS4/ SS4_B	—	—	—	CTS2_ B	CTS2_ RTS2/ SS2_B	SCK2_ C	RXD2_ C/ MISO2 _C/ SCL2	TXD2_ C/ MOSI2 _C/ SDA2	SCK4_ C	RXD4_ C/ MISO4 _C/ SCL4	TXD4_ C/ MOSI4 _C/ SDA4
00101b	SCI*3	RXD3_ C/ MISO3 _C/ SCL3	TXD3_ C/ MOSI3 _C/ SDA3	SCK3_ C	CTS9_ A	CTS9_ RTS9/ SS9_A	TXD9/ MOSI9 _A/ SDA9	RXD9_ A/ MISO9 _A/ SCL9	SCK9_ A	TXD1_ A/ MOSI1 _A/ SDA1	RXD1_ A/ MISO1 _A/ SCL1	SCK1_ A	CTS1_ A	CTS1_ RTS1/ SS1_A	SCK9_ C	RXD9_ C/ MISO9 _C/ SCL9	TXD9_ C/ MOSI9 _C/ SDA9
00110b	SPI*2	SSLB0 _B	SSLB1 _B	—	SSLB2 _B	SSLB3 _B	SSLA3 _A	SSLA2 _A	SSLA1 _A	SSLB1 _A	SSLB2 _A	SSLB3 _A	—	—	—	—	—
00111b	IIC*2	—	—	—	—	—	SDA1_ B	SCL1_ B	—	—	—	—	—	SCL1_ D	SDA1_ D	SCL0_ F	SDA0_ F
01000b	KINT	KR00	KR01	KR02	KR03	KR04	KR05	KR06	KR07	KR00	KR01	KR02	KR03	KR04	KR05	KR06	KR07
01001b	CLKOUT	—	—	CLKOU T	—	—	—	—	—	—	—	—	—	—	—	—	—
01100b	ACMPHS	—	—	CMPO UT3	CMPO UT0	CMPO UT1	—	—	—	—	—	—	—	—	—	—	—
01101b	SCI	—	—	DE3	—	DE9	—	—	DE9	—	—	DE1	—	DE1	DE9	—	DE9
01110b	SCI	—	DE2	—	DE4	DE4	—	—	—	—	DE2	DE2	—	—	DE4	—	—
10000b	CANFD	CRX0	CTX0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10101b	GPT	GTADS M0	GTADS M1	GTCPP O0	—	—	GTADS M0	—	GTADS M1	—	—	—	—	—	—	—	—
10110b	GPT	GTCPP O4	GTCPP O7	GTCPP O2	GTCPP O0	GTCPP O1	GTCPP O3	GTCPP O4	GTCPP O7	—	—	—	—	—	—	—	—
ISEL bit		—	—	IRQ9-DS	—	—	—	—	—	—	—	—	—	IRQ12	IRQ13	IRQ14	IRQ15
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC	L/M/H/ HC
NCODR	N沟道开漏	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64针产品		—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—
48针产品		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

:可用一:禁止设置

注1.输出缓冲器有中驱动和高驱动两种。推荐使用相同的驱动缓冲器输出偏斜规格(tGTISK)。

注2.建议使用名称后附有字母的引脚，例如_A或_B或_D或_F，以指示组成员身份。对于接口，测量每组电气特性的交流部分。

注3.建议使用在名称后附加字母的引脚，例如_A或_B或_C，以指示组成员身份。有关详细信息，请参见第46节，电气特性。

Table 18.10 Register settings for input/output pin function (PORTE)

PSEL[4:0] settings	Function	Pin														
		PE00	PE01	PE02	PE03	PE04	PE05	PE06	PE08	PE09	PE10	PE11	PE12	PE13	PE14	PE15
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z														
00001b	AGT	AGTEE0	AGTEE1	—	—	—	—	—	—	—	—	—	—	—	—	—
00010b	GPT	—	GTOULO	GTOVLO	GTOWLO	GTOUUP	GTOVUP	GTOWUP	GTIV	GTIW	GTOULO	GTOUUP	GTOVLO	GTOVUP	GTOWLO	GTOWUP
00011b	GPT*1	GTETRGA	GTIOC7A	GTIOC7B	GTIOC8A	GTIOC8B	GTIOC9A	GTIOC9B	GTIOC3A	GTIOC3B	GTIOC2A	GTIOC2B	GTIOC1A	GTIOC1B	GTIOC0A	GTIOC0B
00100b	SCI*3	TXD0_E/ MOSI0_E/ SDA0	RXD0_E/ MISO0_E/ SCL0	SCK0_B	RXD0_B/ MISO0_B/ SCL0	TXD0_B/ MOSI0_B/ SDA0	CTS0_RTS0/ SS0_B	CTS0_B	—	—	—	—	—	—	—	RXD4_A/ MISO4_A/ SCL4
00101b	SCI*3	TXD9_D/ MOSI9_D/ SDA9	RXD9_D/ MISO9_D/ SCL9	SCK3_A	CTS3_A	CTS3_RTS3/ SS3_A	RXD3_A/ MISO3_A/ SCL3	TXD3_A/ MOSI3_A/ SDA3	—	—	—	—	—	—	—	—
00110b	SPI*2	SSLB3_C	SSLB2_C	RSPCKB_C	SSLB0_C	SSLB1_C	MISOB_C	MOSIB_C	SSLA3_C	SSLA2_C	SSLA1_C	SSLA0_C	RSPCKA_C	MISOA_C	MOSIA_C	—
01000b	KINT	—	—	—	—	—	—	—	KR00	KR01	KR02	KR03	KR04	KR05	KR06	KR07
01001b	CLKOUT	—	—	CLKOUT	—	—	—	—	—	—	—	—	—	—	—	—
01010b	ADC	ADTRG0	ADTRG1	—	—	—	—	—	ADTRG0	ADTRG1	—	—	—	—	—	—
01100b	ACMPHS	—	—	CMPOUT0	CMPOUT1	CMPOUT2	CMPOUT3	—	CMPOUT012	CMPOUT3	—	—	—	—	—	—
01101b	SCI	—	—	DE3	—	DE3	—	—	—	—	—	—	—	—	—	—
01110b	SCI	—	—	DE0	—	—	DE0	—	—	—	—	—	—	—	—	—
10100b	GPT*1	GTIOC4A	GTIOC4B	GTIOC8A	GTIOC9A	GTIOC7B	GTIOC8B	—	GTETRGC	GTETRGD	GTIOC4A	GTIOC5A	GTIOC6A	GTIOC4B	GTIOC5B	GTIOC6B
10101b	GPT*1	GTADSM0	GTADSM1	—	—	—	—	—	GTADSM0	GTADSM1	GTIOC7A	GTIOC8A	GTIOC9A	GTIOC7B	GTIOC8B	GTIOC9B
10110b	GPT	—	—	—	—	—	GTCPPO2	GTCPPO3	—	—	—	—	—	—	—	—
11001b	CAC	CACREF	—	—	—	—	—	—	—	CACREF	—	—	—	—	—	—
11010b	Trace (Debug)	—	—	TRCLK	TRDATA0	TRDATA1	TRDATA2	TRDATA3	—	—	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	AN020	AN021	AN022	AN023	AN024	AN025	AN026	AN027
ISEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H	L/M/H	L/M/H/HC	L/M/H/HC	L/M/H/HC	L/M/H/HC	L/M/H/HC	L/M/H/HC
NCODR	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64 pins product		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
48 pins product		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

✓: Available
—: Setting prohibited

Note 1. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (tGTISK).

Note 2. Recommend using pins that have a letter appended to their names, for instance _C, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.

Note 3. Recommend using pins that have a letter appended to their names, for instance _A or _B or _D or _E, to indicate group membership. For details, see section 46, Electrical Characteristics.

Table 18.10 输入输出引脚功能（PORTE）的寄存器设置

PSEL[4:0] settings	Function	Pin														
		PE00	PE01	PE02	PE03	PE04	PE05	PE06	PE08	PE09	PE10	PE11	PE12	PE13	PE14	PE15
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z														
00001b	AGT	AGTEE0	AGTEE1	—	—	—	—	—	—	—	—	—	—	—	—	—
00010b	GPT	—	GTOULO	GTOVLO	GTOWLO	GTOUUP	GTOVUP	GTOWUP	GTIV	GTIW	GTOULO	GTOUUP	GTOVLO	GTOVUP	GTOWLO	GTOWUP
00011b	GPT*1	GTETRGA	GTIOC7A	GTIOC7B	GTIOC8A	GTIOC8B	GTIOC9A	GTIOC9B	GTIOC3A	GTIOC3B	GTIOC2A	GTIOC2B	GTIOC1A	GTIOC1B	GTIOC0A	GTIOC0B
00100b	SCI*3	TXD0_E/ MOSI0_E/ SDA0	RXD0_E/ MISO0_E/ SCL0	SCK0_B	RXD0_B/ MISO0_B/ SCL0	TXD0_B/ MOSI0_B/ SDA0	CTS0_RTS0/ SS0_B	CTS0_B	—	—	—	—	—	—	—	RXD4_A/ MISO4_A/ SCL4
00101b	SCI*3	TXD9_D/ MOSI9_D/ SDA9	RXD9_D/ MISO9_D/ SCL9	SCK3_A	CTS3_A	CTS3_RTS3/ SS3_A	RXD3_A/ MISO3_A/ SCL3	TXD3_A/ MOSI3_A/ SDA3	—	—	—	—	—	—	—	—
00110b	SPI*2	SSLB3_C	SSLB2_C	RSPCKB_C	SSLB0_C	SSLB1_C	MISOB_C	MOSIB_C	SSLA3_C	SSLA2_C	SSLA1_C	SSLA0_C	RSPCKA_C	MISOA_C	MOSIA_C	—
01000b	KINT	—	—	—	—	—	—	—	KR00	KR01	KR02	KR03	KR04	KR05	KR06	KR07
01001b	CLKOUT	—	—	CLKOUT	—	—	—	—	—	—	—	—	—	—	—	—
01010b	ADC	ADTRG0	ADTRG1	—	—	—	—	—	ADTRG0	ADTRG1	—	—	—	—	—	—
01100b	ACMPHS	—	—	CMPOUT0	CMPOUT1	CMPOUT2	CMPOUT3	—	CMPOUT012	CMPOUT3	—	—	—	—	—	—
01101b	SCI	—	—	DE3	—	DE3	—	—	—	—	—	—	—	—	—	—
01110b	SCI	—	—	DE0	—	—	DE0	—	—	—	—	—	—	—	—	—
10100b	GPT*1	GTIOC4A	GTIOC4B	GTIOC8A	GTIOC9A	GTIOC7B	GTIOC8B	—	GTETRGC	GTETRGD	GTIOC4A	GTIOC5A	GTIOC6A	GTIOC4B	GTIOC5B	GTIOC6B
10101b	GPT*1	GTADSM0	GTADSM1	—	—	—	—	—	GTADSM0	GTADSM1	GTIOC7A	GTIOC8A	GTIOC9A	GTIOC7B	GTIOC8B	GTIOC9B
10110b	GPT	—	—	—	—	—	GTCPPO2	GTCPPO3	—	—	—	—	—	—	—	—
11001b	CAC	CACREF	—	—	—	—	—	—	—	CACREF	—	—	—	—	—	—
11010b	Trace (Debug)	—	—	TRCLK	TRDATA0	TRDATA1	TRDATA2	TRDATA3	—	—	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	AN020	AN021	AN022	AN023	AN024	AN025	AN026	AN027
ISEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H	L/M/H	L/M/H/HC	L/M/H/HC	L/M/H/HC	L/M/H/HC	L/M/H/HC	L/M/H/HC
NCODR	N沟道开漏	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64针产品		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
48针产品		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

:可用—:禁止设置

注1.输出缓冲器有中驱动和高驱动两种。推荐使用相同的驱动缓冲器输出偏斜规格(tGTISK)。

注2.建议使用在名称后附加字母（例如_C）的引脚来表示组成员身份。对于接口，测量每组电气特性的交流部分。

注3.建议使用名称后附有字母的引脚，例如_A或_B或_D或_E，以指示组成员身份。有关详细信息，请参见第46节，电气特性。

19. Key Interrupt Function (KINT)

19.1 Overview

The key interrupt function (KINT) generates the key interrupt by detecting rising or falling edge on the key interrupt input pins. Figure 19.1 shows a block diagram and Table 19.1 lists the input pins.

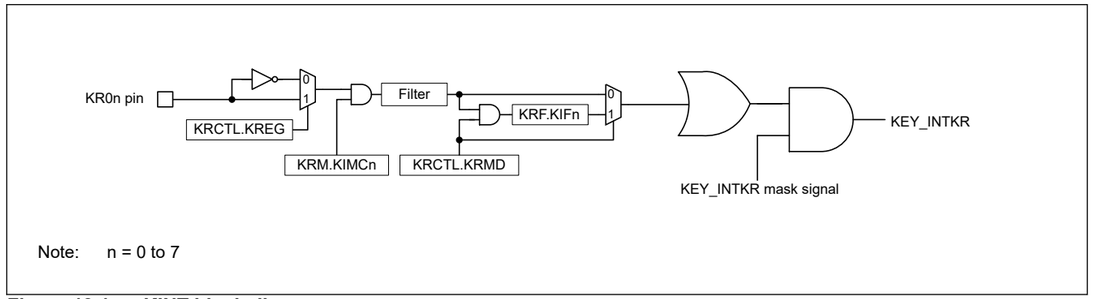


Figure 19.1 KINT block diagram

All key return factors are merged by an OR gate, and the key interrupt signal, KEY_INTKR, is the output of the AND gate to mask the merged key return factor by the KEY_INTKR mask signal. When using KRF.KIFn flag (KRCTL.KRMD = 1), the KEY_INTKR mask signal is used as the output mask that is asserted by clearing KRF.KIFn flag.

Table 19.1 KINT I/O pins

Pin name	I/O	Function
KR00 to KR07	Input	Key interrupt input pins

19.2 Register Descriptions

19.2.1 KRCTL : Key Return Control Register

Base address: KINT = 0x4008_5000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KRMD	—	—	—	—	—	—	KREG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	KREG	Detection Edge Selection (KR00 to KR07 pins) 0: Falling edge 1: Rising edge	R/W
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	KRMD	Usage of Key Interrupt Flags (KRF.KIF0 to KRF.KIF7) 0: Do not use key interrupt flags 1: Use key interrupt flags	R/W

The KRCTL register controls the usage of the key interrupt flags, KRF.KIFn (n = 0 to 7), and sets the detection edge.

19. 按键中断功能(KINT)

19.1 Overview

按键中断功能(KINT)通过检测按键中断输入引脚的上升沿或下降沿来产生按键中断。图19.1显示了框图，表19.1列出了输入引脚。

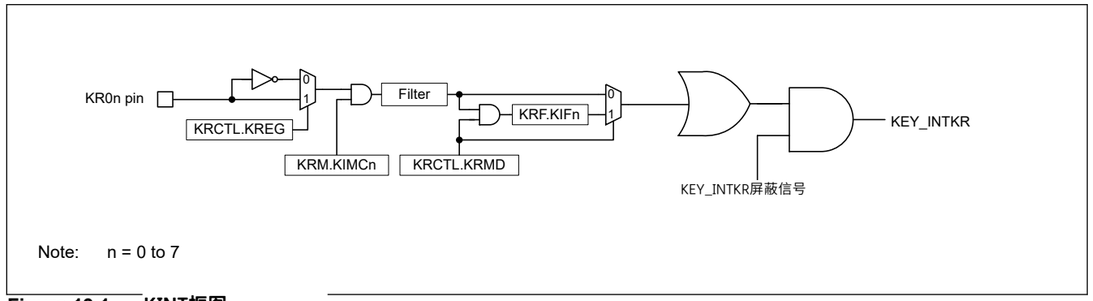


Figure 19.1 KINT框图

所有的键返回因子由一个或门合并，键中断信号KEY_INTKR是与门的输出，用于通过KEY_INTKR屏蔽信号屏蔽合并的键返回因子。当使用KRF.KIFn标志(KRCTL.KRMD=1)时，KEY_INTKR掩码信号用作通过清除KRF.KIFn标志而断言的输出掩码。

Table 19.1 KINT I/O pins

引脚名称	I/O	Function
KR00 to KR07	Input	按键中断输入引脚

19.2 注册说明

19.2.1 KRCTL:密钥返回控制寄存器

Base address: KINT = 0x4008_5000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KRMD	—	—	—	—	—	—	KREG
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	KREG	检测边缘选择（KR00至KR07引脚） 0：下降沿1： 上升沿	R/W
6:1	—	这些位被读取为0。写入值应为0。	R/W
7	KRMD	关键中断标志的使用（KRF.KIF0到KRF.KIF7） 0：不使用按键中断标志1：使用 按键中断标志	R/W

KRCTL寄存器控制按键中断标志KRF.KIFn（n=0到7）的使用，并设置检测沿。

19.2.2 KRF : Key Return Flag Register

Base address: KINT = 0x4008_5000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KIF7	KIF6	KIF5	KIF4	KIF3	KIF2	KIF1	KIF0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	KIF0 to KIF7	Key Interrupt Flag n 0: No interrupt detected 1: Interrupt detected	R/W

The KRF register controls the key interrupt flags, KIFn.

When KRCTL.KRMD = 0, setting the KIFn flag to 1 is prohibited. When setting the KIFn flag to 1, the KIFn value does not change.

To clear the KIFn flag, confirm the target flag is 1 before writing 0 to the bit, then write 1 to the other flags.

19.2.3 KRM : Key Return Mode Register

Base address: KINT = 0x4008_5000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KIMC7	KIMC6	KIMC5	KIMC4	KIMC3	KIMC2	KIMC1	KIMC0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	KIMC0 to KIMC7	Key Interrupt Mode Control n 0: Do not detect key interrupt signals 1: Detect key interrupt signals	R/W

The KRM register sets the key interrupt mode.

An interrupt is generated when the target bit in the KRM register is set while a low level (KRCTL.KREG = 0) or a high level (KRCTL.KREG = 1) is being input to the KR0n pin. To ignore this interrupt, set the KRM register after disabling the interrupt handling.

KINT can be assigned in the PmnPFS.PSEL[4:0] bits. The on-chip pull-up resistors can also be applied by setting the associated key interrupt input pin in the pull-up resistor. For details, see section 18, I/O Ports.

19.3 Operation

19.3.1 Operation When Not Using the Key Interrupt Flags (KRCTL.KRMD = 0)

A key interrupt signal, KEY_INTKR, is generated when the valid edge specified in the KRCTL.KREG bit is input to a KR0n pin. To identify the channel to which the valid edge is input, read the port register and check the port level after the KEY_INTKR signal is generated.

The KEY_INTKR signal changes based on the input level of the KR0n pin.

19.2.2 KRF:密钥返回标志寄存器

Base address: KINT = 0x4008_5000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KIF7	KIF6	KIF5	KIF4	KIF3	KIF2	KIF1	KIF0
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	KIF0 to KIF7	按键中断标志n 0：未检测到中断1：检测到中断	R/W

KRF寄存器控制关键中断标志KIFn。

当KRCTL.KRMD=0时，禁止将KIFn标志设置为1。将KIFn标志设置为1时，KIFn值不会改变。

要清除KIFn标志，在向该位写入0之前确认目标标志为1，然后向其他标志写入1。

19.2.3 KRM:密钥返回模式寄存器

Base address: KINT = 0x4008_5000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KIMC7	KIMC6	KIMC5	KIMC4	KIMC3	KIMC2	KIMC1	KIMC0
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	KIMC0 to KIMC7	按键中断模式控制n 0：不检测按键中断信号1：检测按键中断信号	R/W

KRM寄存器设置按键中断模式。

当低电平(KRCTL.KREG=0)或高电平(KRCTL.KREG=1)输入到KR0n引脚时，如果KRM寄存器中的目标位被置位，则会产生中断。要忽略此中断，请在禁用中断处理后设置KRM寄存器。

KINT可以在PmnPFS.PSEL[4:0]位中分配。片上上拉电阻也可以通过在上拉电阻中设置相关的按键中断输入引脚来应用。有关详细信息，请参阅第18节，IO端口。

19.3 Operation

19.3.1 不使用按键中断标志(KRCTL.KRMD=0)时的操作

当KRCTL.KREG位中指定的有效边沿输入到一个按键中断信号KEY_INTKR KR0n引脚。要识别输入有效边沿的通道，请读取端口寄存器并检查端口电平后KEY_INTKR信号产生。

KEY_INTKR信号根据KR0n引脚的输入电平而变化。

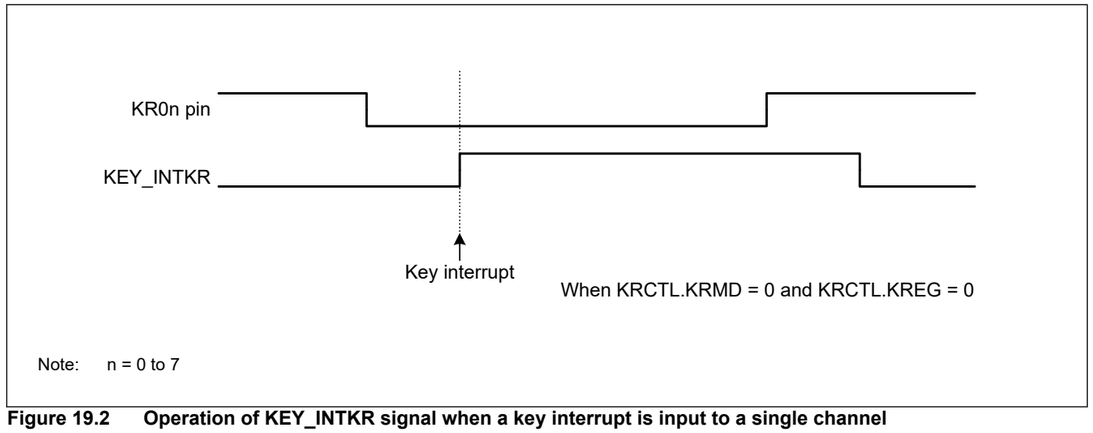


Figure 19.2 Operation of KEY_INTKR signal when a key interrupt is input to a single channel

Figure 19.3 shows the operation when a valid edge is input to multiple KR0n pins. The KEY_INTKR signal is set while a low level is being input to one pin (when KRCTL.KREG = 0). Therefore, even if a falling edge is input to another pin in this period, the KEY_INTKR signal is not generated again. See [1] in Figure 19.3.

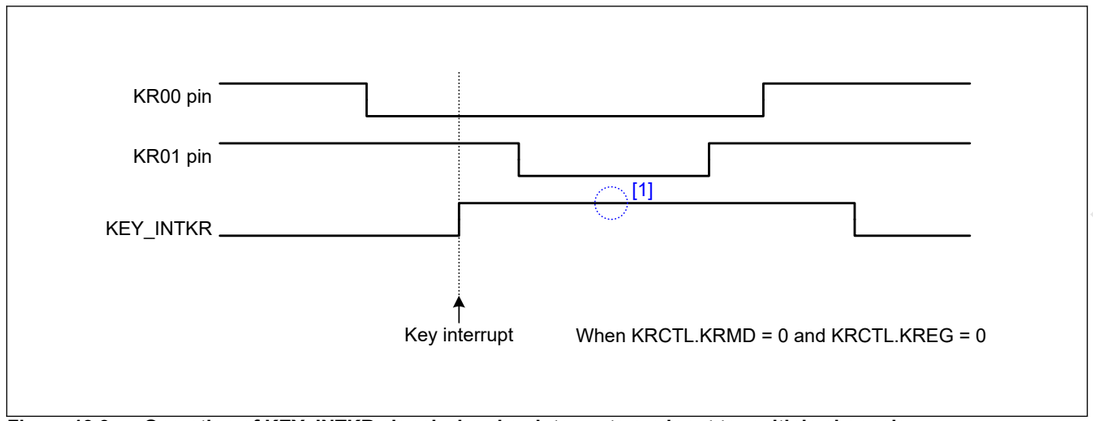


Figure 19.3 Operation of KEY_INTKR signal when key interrupts are input to multiple channels

19.3.2 Operation When Using the Key Interrupt Flags (KRCTL.KRMD = 1)

The KEY_INTKR signal is generated when the valid edge specified in the KRCTL.KREG bit is input to KR0n pins. To identify the channels to which the valid edge is input, read the KRF register after the KEY_INTKR signal is generated. If the KRCTL.KRMD bit is set to 1, clear the KEY_INTKR signal by clearing the associated bit in the KRF register.

As Figure 19.4 shows, only one interrupt is generated each time a falling edge is input to one channel, (when KRCTL.KREG = 0), regardless of whether the KRF.KIFn flag is cleared before or after a rising edge is input.

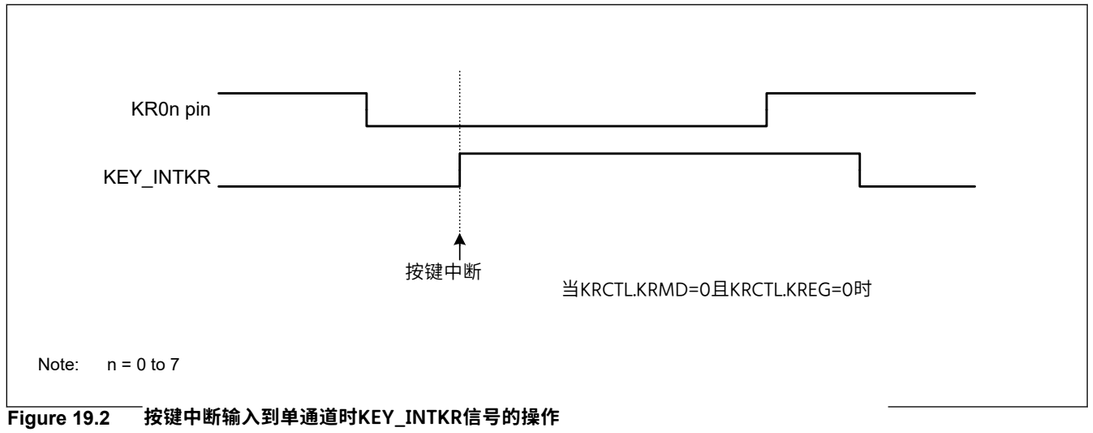


Figure 19.2 按键中断输入到单通道时KEY_INTKR信号的操作

图19.3显示了有效边沿输入到多个KR0n引脚时的操作。KEY_INTKR信号在低电平输入到一个引脚时设置（当KRCTL.KREG=0时）。因此，即使在此期间向另一个引脚输入下降沿，也不会再次产生KEY_INTKR信号。请参见图19.3中的[1]。

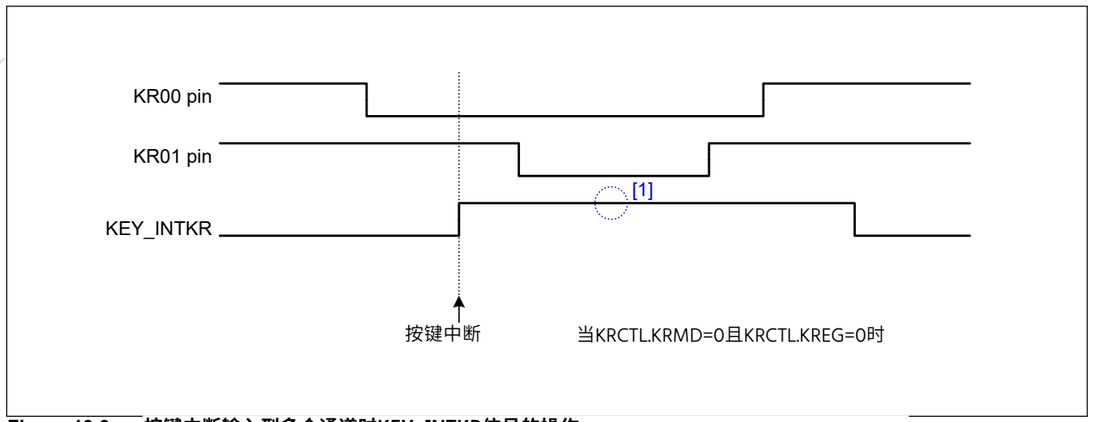


Figure 19.3 按键中断输入到多个通道时KEY_INTKR信号的操作

19.3.2 使用按键中断标志(KRCTL.KRMD=1)时的操作

当KRCTL.KREG位中指定的有效边沿输入到KR0n引脚时，会产生KEY_INTKR信号。要识别输入有效边沿的通道，请在生成KEY_INTKR信号后读取KRF寄存器。如果KRCTL.KRMD位设置为1，则通过清除KRF寄存器中的相关位来清除KEY_INTKR信号。

如图19.4所示，每次向一个通道输入下降沿时（当KRCTL.KREG=0时）只产生一个中断，无论KRF.KIFn标志是在输入上升沿之前还是之后清零。

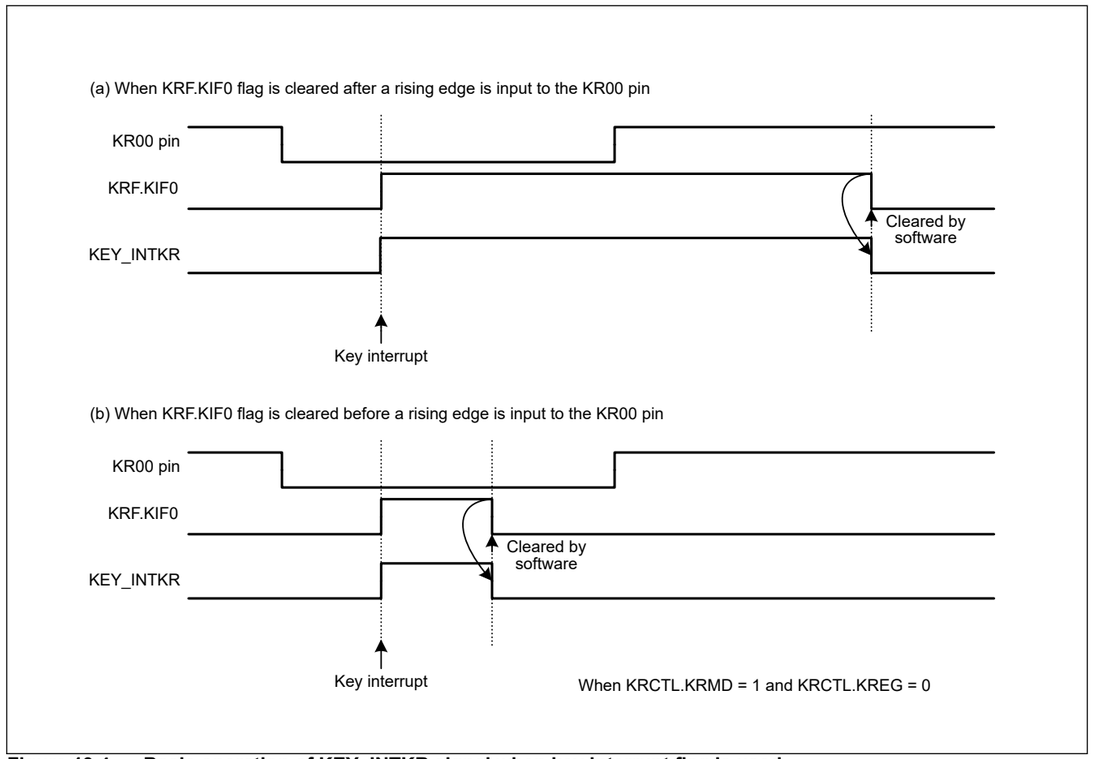


Figure 19.4 Basic operation of KEY_INTKR signal when key interrupt flag is used

Figure 19.5 shows the operation when a valid edge is input to multiple KR0n pins. A falling edge is also input to the KR00 and KR05 pins after a falling edge is input to the KR00 pin (when KRCTL.KREG = 0). The KRF.KIF1 flag is set when the KRF.KIF0 flag is cleared. The KEY_INTKR signal generates 1 PCLKB clock, after the KRF.KIF0 flag is cleared. See [1] in Figure 19.5.

Also, after a falling edge is input to the KR05 pin, the KRF.KIF5 flag is set. The KRF.KIF1 flag is cleared at time [2] in the figure. The KEY_INTKR signal generates 1 PCLKB clock, after the KRF.KIF1 flag is cleared. See [3] in the figure. It is therefore possible to generate the KEY_INTKR signal when a valid edge is input to multiple channels.

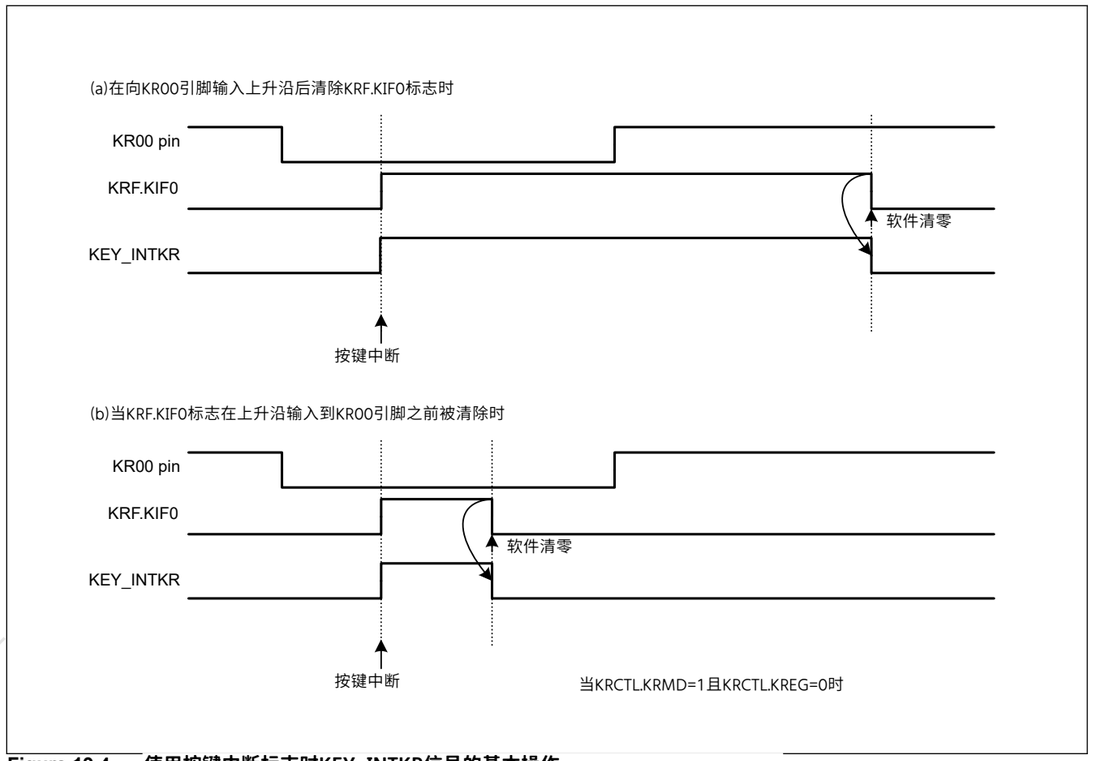


Figure 19.4 使用按键中断标志时KEY_INTKR信号的基本操作

图19.5显示了有效边沿输入到多个KR0n引脚时的操作。在向KR00引脚输入下降沿后（当KRCTL.KREG=0时），也会向KR00和KR05引脚输入一个下降沿。当KRF.KIF0标志被清除时，KRF.KIF1标志被设置。KRF.KIF0标志清零后，KEY_INTKR信号产生1个PCLKB时钟。见[1]

Figure 19.5.

此外，在向KR05引脚输入下降沿后，设置KRF.KIF5标志。KRF.KIF1标志在图中的时间[2]处被清除。KRF.KIF1标志清零后，KEY_INTKR信号产生1个PCLKB时钟。见图[3]。因此，当有效边沿输入到多个通道时，可以生成KEY_INTKR信号。

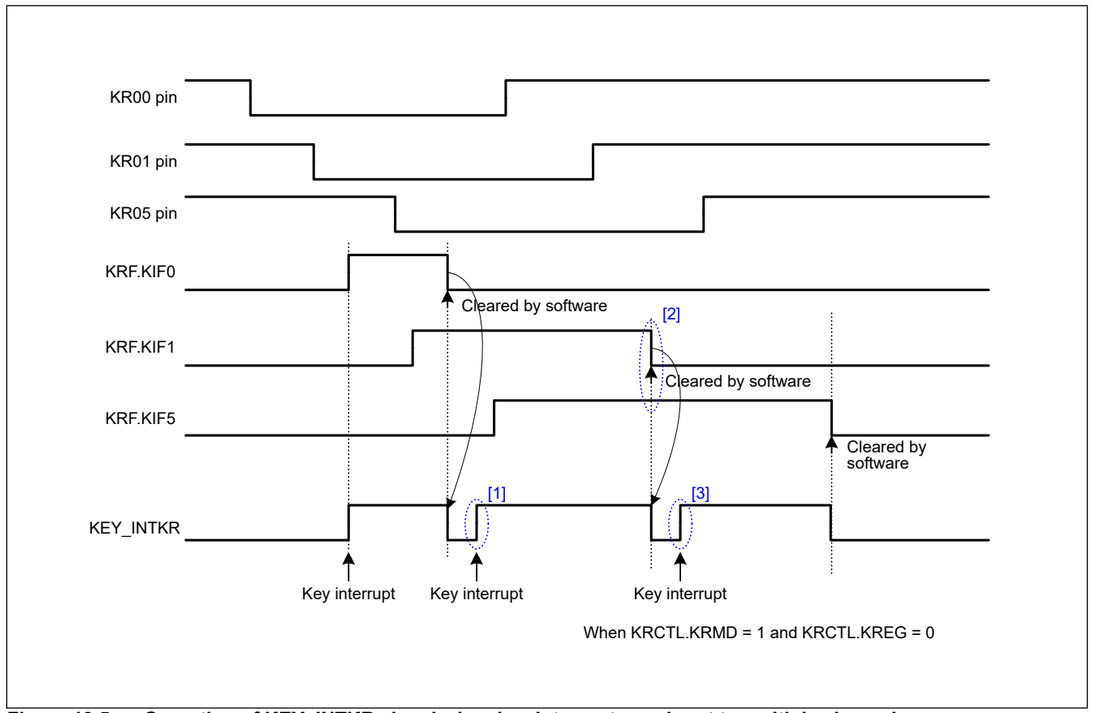


Figure 19.5 Operation of KEY_INTKR signal when key interrupts are input to multiple channels

19.4 Usage Notes

- If the KEY_INTKR signal is used as the snooze request, the KRCTL.KRMD bit should be set to 0.
- If the KEY_INTKR signal is used as the interrupt source for returning to Normal mode from Snooze and Software Standby modes, the KRCTL.KRMD bit should be set to 1.
- When KINT is assigned to a pin, this pin input is always enabled in the Software Standby mode, and if the pin level changes, the associated KRF.KIFn flag can be set. Therefore, a KEY_INTKR signal might be generated on canceling Software Standby mode. To ignore changes to the KR0n pin during a Software Standby, clear the associated KRM.KIMCn bit before entering Software Standby. After canceling Software Standby mode, the KRF.KIFn flag should be cleared before the associated KRM.KIMCn bit can be set.

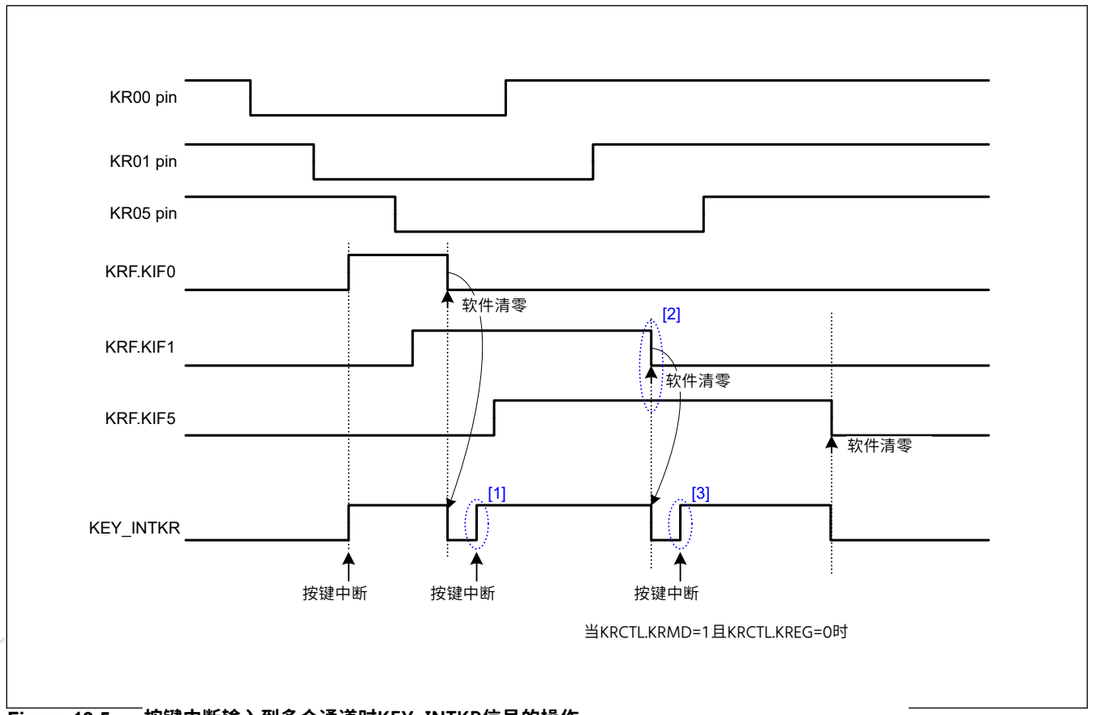


Figure 19.5 按键中断输入到多个通道时KEY_INTKR信号的操作

19.4 使用说明

●如果KEY_INTKR信号用作贪睡请求，则KRCTL.KRMD位应设置为0。

●如果KEY_INTKR信号用作从贪睡和软件待机模式返回正常模式的中断源，则KRCTL.KRMD位应设置为1。

●当KINT被分配给一个管脚时，该管脚输入在软件待机模式下总是使能的，如果管脚电平改变，可以设置相关的KRF.KIFn标志。因此，在取消软件待机模式时可能会生成KEY_INTKR信号。要在软件待机期间忽略对KR0n引脚的更改，请清除相关的

进入软件待机之前的KRM.KIMCn位。取消软件待机模式后，应先清除KRF.KIFn标志，然后才能设置相关的KRM.KIMCn位。

20. Port Output Enable for GPT (POEG)

20.1 Overview

The POEG issues requests to stop output from output pins of the general PWM timer (GPT). Select the method of detection for stopping the output from the list below.

- Input level detection of the GTETRGn pin (n = A to D)
- Detection from the GPT to stop output
- Detection by comparator (edge detection or level detection)
- Detection of stopping of oscillation by the oscillation stop detection circuit for the main clock
- Register setting

The GTETRGn pin can be used for output to the external trigger input pins of the GPT.

Table 20.1 shows specifications, Figure 20.1 shows a block diagram, and Table 20.2 shows input pins.

Table 20.1 POEG specifications

Item	Description
Request of output stopping in response to input level detection	• The request to stop output is issued to the GPT when a POEGGn.PIDF flag is set in response to the detection of input of the selected level on the corresponding GTETRGn pin (n = A to D). • The request to stop output is issued to the GPT immediately upon detection of input of the selected level on the corresponding GTETRGn pin.
Requests to stop output in the form of an output stopping signal from the GPT	• The request to stop output is issued to the GPT when the GPT detects the active level (high or low) on the GTIOCA and GTIOCB pins at the same time while the corresponding POEGGn.IOCF flag is set. • The request to stop output is issued to the GPT when the GPT detects a deadtime error while the corresponding POEGGn.IOCF flag is set.
Requests to stop output in response to detection by a comparator	• The request to stop output is issued to the GPT when a POEGGn.IOCF flag is set in response to edge-detection by a comparator. • The request to stop output is issued directly to the GPT upon detecting level on a comparator.
Requests to stop output in response to detecting the stopping of oscillation	A request to stop output is issued to the GPT when the oscillation stop detection circuit for the main clock detects the stopping of oscillation while the corresponding POEGGn.OSTPF flag is set.
Requests by software to stop output	The request to stop output is issued to the GPT when the software sets the POEGGn.SSF flag.
Interrupt	• An interrupt is generated in response to the request to stop output in the form of the POEGGn.PIDF flag. • An interrupt is generated in response to the request to stop output in the form of the POEGGn.IOCF flag.
External trigger output to the GPT	The GTETRGn pin is used for output as external triggers.
Noise removal	• Each GTETRGn pin has a digital noise filter. • Four types of sampling clock are selectable for the filter.
TrustZone Filter	• Security attribution can be set for each groups.

20. GPT(POEG)的端口输出使能

20.1 Overview

POEG发出请求以停止通用PWM定时器(GPT)的输出引脚的输出。从下表中选择停止输出的检测方法。

- ●GTETRn引脚的输入电平检测（n=A至D）
- ●从GPT检测到停止输出
- ●比较器检测（边沿检测或电平检测）
- ●通过主时钟的振荡停止检测电路检测振荡停止
- ●寄存器设置

GTETRn引脚可用于输出到GPT的外部触发输入引脚。

表20.1显示规格，图20.1显示框图，表20.2显示输入引脚。

Table 20.1 POEG specifications

Item	Description
响应输入电平检测的输出停止请求	• 当一个停止输出的请求被发送到GPT POEGGn.PIDF标志响应检测到相应GTETRn引脚（n=A到D）上的所选电平的输入而设置。 • 在检测到相应GTETRn引脚上所选电平的输入后，立即向GPT发出停止输出的请求。
以来自GPT的输出停止信号的形式请求停止输出	• 当GPT同时检测到GTIOCA和GTIOCB引脚上的有效电平（高或低）时，向GPT发出停止输出请求，同时相应的 POEGGn.IOCF标志已设置。 • 当相应的POEGGn.IOCF标志置位时，当GPT检测到死区时间错误时，将向GPT发出停止输出的请求。
请求停止输出以响应比较器的检测	• 当一个停止输出的请求被发送到GPT POEGGn.IOCF标志被设置以响应比较器的边沿检测。 • 检测到比较器的电平后，停止输出的请求直接发送到GPT。
响应检测到振荡停止请求停止输出	当相应的POEGGn.OSTPF标志置位时，当主时钟的振荡停止检测电路检测到振荡停止时，向GPT发出停止输出的请求。
软件请求停止输出	当软件设置POEGGn.SSF标志时，将向GPT发出停止输出的请求。
Interrupt	• 响应以POEGGn.PIDF标志的形式停止输出的请求产生一个中断。 • 以POEGGn.IOCF标志的形式响应停止输出的请求产生一个中断。
到GPT的外部触发输出	GTETRn引脚用于作为外部触发输出。
去噪	• 每个GTETRn引脚都有一个数字噪声滤波器。 • 滤波器有四种采样时钟可供选择。
TrustZone Filter	• 可以为每个组设置安全属性。

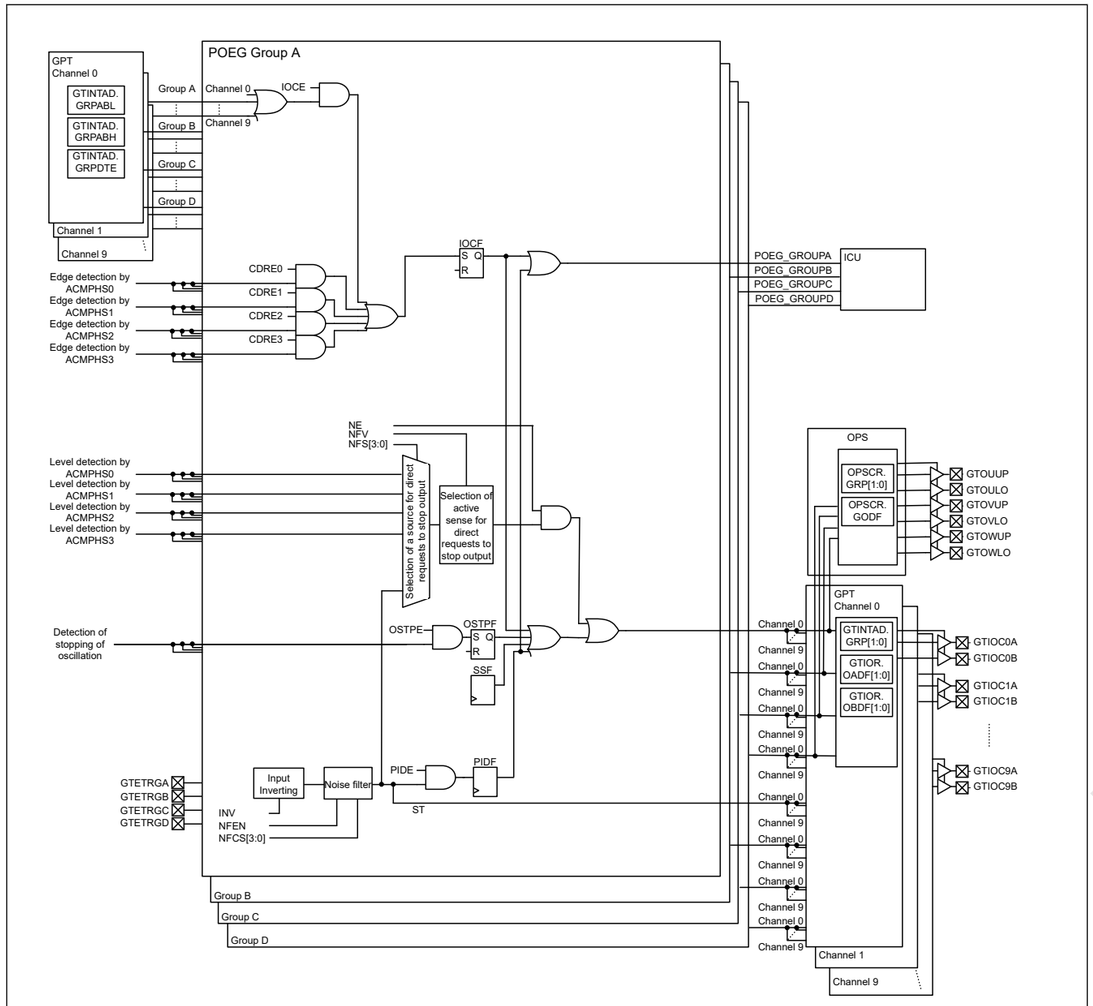


Figure 20.1 POEG Block Diagram

Table 20.2 POEG I/O pins

Pin name	I/O	Function
GTETRGA	Input	Output disable detection signal for GPT output pin and GPT external trigger input pin A
GTETRGB	Input	Output disable detection signal for GPT output pin and GPT external trigger input pin B
GTETRGC	Input	Output disable detection signal for GPT output pin and GPT external trigger input pin C
GTETRGD	Input	Output disable detection signal for GPT output pin and GPT external trigger input pin D

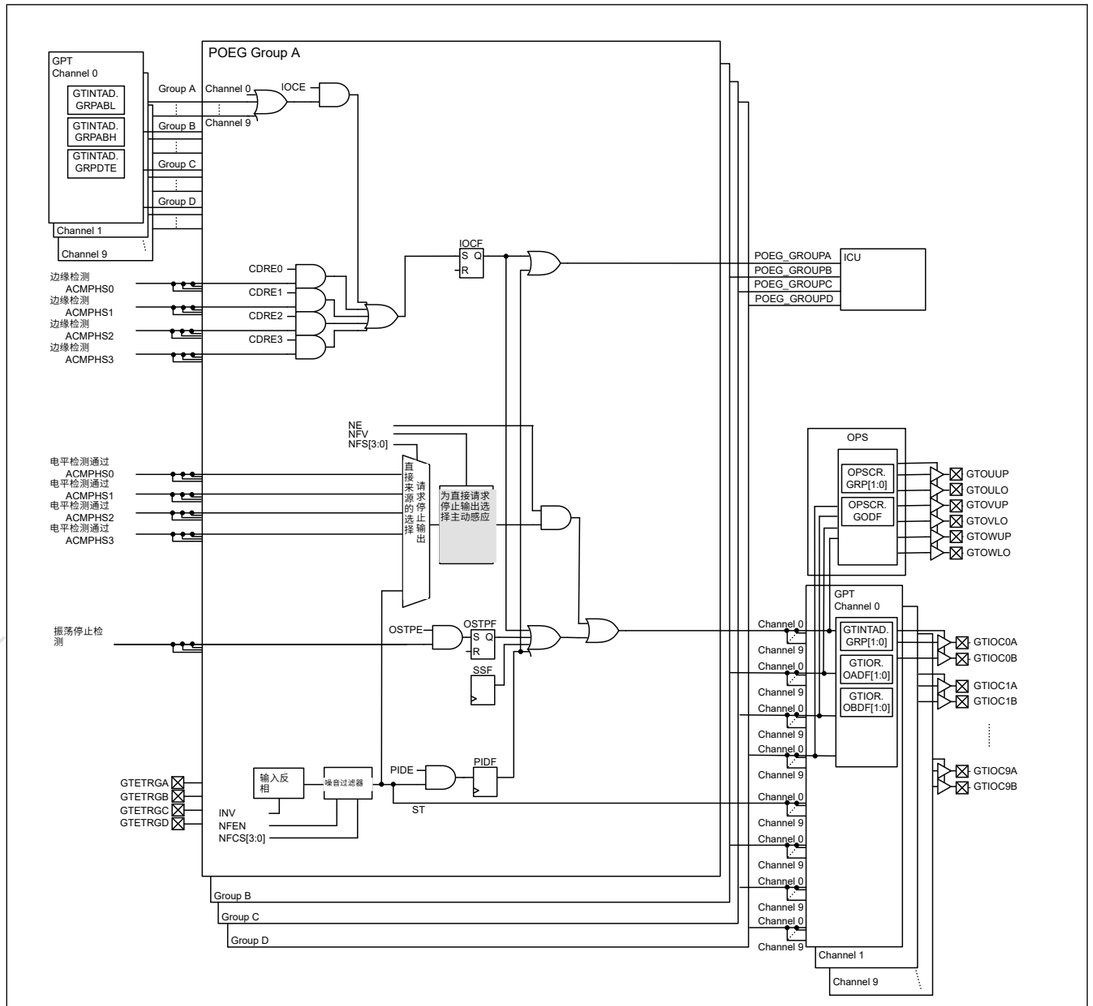


Figure 20.1 POEG框图

Table 20.2 POEG I/O pins

引脚名称	I/O	Function
GTETRGA	Input	GPT输出引脚和GPT外部触发输入引脚A的输出禁用检测信号
GTETRGB	Input	GPT输出引脚和GPT外部触发输入引脚B的输出禁用检测信号
GTETRGC	Input	GPT输出引脚和GPT外部触发输入引脚C的输出禁用检测信号
GTETRGD	Input	GPT输出引脚和GPT外部触发输入引脚D的输出禁用检测信号

20.2 Register Descriptions

20.2.1 POEGGn : POEG Group n Setting Register (n = A to D)

Base address: POEG = 0x4008_A000

Offset address: 0x000 (POEGGA)
0x100 (POEGGB)
0x200 (POEGGC)
0x300 (POEGGD)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	INV	—	—	—	—	—	—	—	—	—	—	—	ST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CDRE3	CDRE2	CDRE1	CDRE0	—	OSTPE	IOCE	PIDE	SSF	OSTPF	IOCF	PIDF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIDF	Port Input Detection Flag 0: The selected input level was not detected on the GTETRGn pin 1: The selected input level was detected on the GTETRGn pin	R/W*1
1	IOCF	GPT or ACMPHS Output Stop Request Detection Flag 0: Neither stopping of GPT output nor a comparator edge was detected 1: Either stopping of GPT output or comparator edge was detected	R/W*1
2	OSTPF	Oscillation Stop Detection Flag 0: Stopping of oscillation was not detected 1: Stopping of oscillation was detected	R/W*1
3	SSF	Software Stop Flag 0: Software has not stopped output 1: Software has stopped output	R/W
4	PIDE	Port Input Detection Enable 0: Detection of input levels on the corresponding GTETRGn pin is disabled 1: Detection of input levels on the corresponding GTETRGn pin is enabled	R/W*2
5	IOCE	GPT Output Stop Request Enable 0: Detection of stopping of output from the GPT is disabled 1: Detection of stopping of output from the GPT is enabled	R/W*2
6	OSTPE	Enable Stopping Output on Stopping of Oscillation 0: Detection of stopping of oscillation is disabled 1: Detection of stopping of oscillation is enabled	R/W*2
7	—	This bit is read as 0. The write value should be 0.	R/W
8	CDRE0	ACMPHS0 Enable 0: Comparator edge detection 0 is disabled 1: Comparator edge detection 0 is enabled	R/W*2
9	CDRE1	ACMPHS1 Enable 0: Comparator edge detection 1 is disabled 1: Comparator edge detection 1 is enabled	R/W*2
10	CDRE2	ACMPHS2 Enable 0: Comparator edge detection 2 is disabled 1: Comparator edge detection 2 is enabled	R/W*2
11	CDRE3	ACMPHS3 Enable 0: Comparator edge detection 3 is disabled 1: Comparator edge detection 3 is enabled	R/W*2
15:12	—	These bits are read as 0. The write value should be 0.	R/W

20.2 注册说明

20.2.1 POEGGn:POEG组n设置寄存器(n=A到D)

Base address: POEG = 0x4008_A000

Offset address: 0x000 (POEGGA)
0x100 (POEGGB)
0x200 (POEGGC)
0x300 (POEGGD)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	INV	—	—	—	—	—	—	—	—	—	—	—	ST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CDRE3	CDRE2	CDRE1	CDRE0	—	OSTPE	IOCE	PIDE	SSF	OSTPF	IOCF	PIDF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIDF	端口输入检测标志 0：在GTETRn引脚上未检测到所选输入电平1：在GTETRn引脚上检测到所选输入电平	R/W*1
1	IOCF	GPT或ACMPHS输出停止请求检测标志 0：未检测到GPT输出停止或比较器边沿1：检测到GPT输出停止或比较器边沿	R/W*1
2	OSTPF	振荡停止检测标志 0：未检测到振荡停止1：检测到振荡停止	R/W*1
3	SSF	软件停止标志 0：软件未停止输出1：软件已停止输出	R/W
4	PIDE	端口输入检测启用 0：禁用相应GTETRn引脚上的输入电平检测1：启用相应GTETRn引脚上的输入电平检测	R/W*2
5	IOCE	GPT输出停止请求启用 0：GPT输出停止检测无效1：GPT输出停止检测有效	R/W*2
6	OSTPE	在停止振荡时启用停止输出 0：振荡停止检测无效1：振荡停止检测有效	R/W*2
7	—	该位读取为0。写入值应为0。	R/W
8	CDRE0	ACMPHS0 Enable 0：比较器边沿检测0无效1：比较器边沿检测0有效	R/W*2
9	CDRE1	ACMPHS1 Enable 0：比较器边沿检测1无效1：比较器边沿检测1有效	R/W*2
10	CDRE2	ACMPHS2 Enable 0：比较器边沿检测2无效1：比较器边沿检测2有效	R/W*2
11	CDRE3	ACMPHS3 Enable 0：比较器边沿检测3无效1：比较器边沿检测3有效	R/W*2
15:12	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
16	ST	GTETRGn Input Status Flag 0: The corresponding external trigger for output to the GPT is 0 1: The corresponding external trigger for output to the GPT is 1	R
27:17	—	These bits are read as 0. The write value should be 0.	R/W
28	INV	GTETRGn Input Inverting 0: Input on the GTETRGn pin is not inverted 1: Input on the GTETRGn pin is inverted	R/W
29	NFEN	Noise filter Enable 0: Digital noise filter on the GTETRGn pin is disabled 1: Digital noise filter on the GTETRGn pin is enabled	R/W
31:30	NFCS[1:0]	Noise filter Clock Select 0 0: Samples the input level of GTETRGn pin three times per PCLKB/1 clock 0 1: Samples the input level of GTETRGn pin three times per PCLKB/8 clock 1 0: Samples the input level of GTETRGn pin three times per PCLKB/32 clock 1 1: Samples the input level of GTETRGn pin three times per PCLKB/128 clock	R/W

Note 1. Only 0 can be written to clear the flag.
Note 2. Can be modified only once after a reset.

The POEGGn register (n = A to D) controls requests for stopping output and an external trigger for the GPT based in response to the detection of various signals.

SSF Flag (Software Stop Flag)

Writing 1 to the SSF flag leads to a request to stop output being issued to the GPT, and writing 0 to the flag releases the GPT from the request to stop output. In addition, requests to stop output issued by software can be monitored by reading the flag.

20.2.2 GTONCWPn : GPT Output Stopping Control Group n Write Protection Register (n = A to D)

Base address: POEG = 0x4008_A000

Offset address: 0x040 (GTONCWPA)
0x140 (GTONCWPB)
0x240 (GTONCWPC)
0x340 (GTONCWPD)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	—	—	—	—	WP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WP	Register Writing Disable 0: Writing to the GTONCCRn register is enabled 1: Writing to the GTONCCRn register is disabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	PRKEY[7:0]	Key Code These bits control whether or not writing new values to the GTONCWPn register is possible. To write to the GTONCWPn register, write 0xA5 to the 8 higher-order bits and write any value to make up a 16-bit unit to the 8 lowerorder bits at the same time. These bits are read as 0x00.	R/W

The GTONCWPn register (n = A to D) enables writing to the GTONCCRn register in order to avoid incorrect

Bit	Symbol	Function	R/W
16	ST	GTETRn输入状态标志 0：对应输出到GPT的外部触发为01：对应输出到GPT的外部触发为1	R
27:17	—	这些位被读取为0。写入值应为0。	R/W
28	INV	GTETRn输入反相 0：GTETRn引脚上的输入不反相1：GTETRn引脚上的输入反相	R/W
29	NFEN	噪声滤波器启用 0：禁用GTETRn引脚上的数字噪声滤波器1：启用GTETRn引脚上的数字噪声滤波器	R/W
31:30	NFCS[1:0]	噪声滤波器时钟选择 00：每个PCLKB1个时钟对GTETRGn引脚的输入电平进行3次采样01：每个PCLKB8个时钟对GTETRn引脚的输入电平进行3次采样10：每个PCLKB32个时钟对GTETRn引脚的输入电平进行3次采样11：每个PCLKB128时钟对GTETRn引脚的输入电平进行3次采样	R/W

注1.只能写入0来清除标志。
注2.复位后只能修改一次。

POEGGn寄存器（n=A到D）根据检测到的各种信号控制停止输出的请求和GPT的外部触发。

SSF标志（软件停止标志）

向SSF标志写入1会导致向GPT发出停止输出的请求，向标志写入0会释放GPT从请求中停止输出。此外，可以通过读取标志来监控软件发出的停止输出请求。

20.2.2 GTONCWPn:GPT输出停止控制组n写保护寄存器(n=AtoD)

Base address: POEG = 0x4008_A000

Offset address: 0x040 (GTONCWPA)
0x140 (GTONCWPB)
0x240 (GTONCWPC)
0x340 (GTONCWPD)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	—	—	—	—	WP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WP	寄存器写入禁用 0：允许写入GTONCCRn寄存器1：禁止写入GTONCCRn寄存器	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	PRKEY[7:0]	关键代码 这些位控制是否可以将新值写入GTONCWPn寄存器。要写入GTONCWPn寄存器，向高8位写入0xA5，同时向低8位写入任意值以构成16位单元。这些位被读取为0x00。	R/W

GTONCWPn寄存器（n=A到D）允许写入GTONCCRn寄存器以避免错误

20.2.3 GTONCCRn : GPT Output Stopping Control Group n Controlling Register (n = A to D)

Base address: POEG = 0x4008_A000

Offset address: 0x044 (GTONCCRA)
0x144 (GTONCCRB)
0x244 (GTONCCRC)
0x344 (GTONCCRD)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	NFV	NFS[3:0]				—	—	—	NE
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	NE	Direct Stopping Request Setting 0: The signal for detection is not set as a direct stopping request signal 1: The signal for detection is set as a direct stopping request signal	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
7:4	NFS[3:0]	Direct Stopping Request Selection Other settings are prohibited. 0x0: Comparator level detection 0 0x1: Comparator level detection 1 0x2: Comparator level detection 2 0x4: Comparator level detection 3 0x7: GTETRGn pin input level detection (n = A to D) Others: Setting prohibited	R/W
8	NFV	Direct Stopping Request Active Sense 0: Stopping output is requested when the output stopping detection signal is 0 1: Stopping output is requested when the output stopping detection signal is 1	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

The GTONCCRn register (n = A to D) set up requests for stopping output in response to detected signals.

NE bit (Direct Stopping Request Setting)

Writing 1 to the NE bit leads to direct output of the stopping request signal in response to the signal for detection selected by the NFS[3:0] bits.

20.3 Operation

20.3.1 Request to Stop Output in Response to Detection of Input Level on the Corresponding GTETRGn Pin (n = A to D)

There are two types of output stopping request: requests in response to setting of the POEGGn.PIDF flag (n = A to D), and requests directly in response to the detected signal.

1. To request stopping of output in response to setting of the PIDF flag, the input set in the POEGGn register (inversion or non-inversion set in the INV bit, filtering enabled or disabled by the NFEN bit, sample clock for filtering set in the NFCS[1:0] bits) is detected while the POEGGn.PIDE bit is 1. After the POEGGn.PIDF flag is set to 1 in response to this, the request to disable output is issued per group to each channel of the GPT. To de-assert the request signal for stopping output, clear the POEGGn.PIDF flag. For cancelling requests to stop output, see section 20.3.6. Cancelling Requests to Stop Output.
2. To request stopping of output in direct response to detection of the input level of a selected signal, the input set in the POEGGn (inversion or non-inversion set in the INV bit, filtering enabled or disabled by the NFEN bit, sample clock for filtering set in the NFCS[1:0] bits) and GTONCCRn registers (active sense set in the NFV bit) to the GTETRGn pin selected in the GTONCCRn.NFS[3:0] bits is detected while the GTONCCRn.NE bit is 1, and a request to stop output is then directly issued per channel group of the GPT. The signal to request stopping of output is de-asserted when the

20.2.3 GTONCCRn:GPT输出停止控制组n控制寄存器(n=Ato D)

Base address: POEG = 0x4008_A000

Offset address: 0x044 (GTONCCRA)
0x144 (GTONCCRB)
0x244 (GTONCCRC)
0x344 (GTONCCRD)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	NFV	NFS[3:0]				—	—	—	NE
重置后的值:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	NE	直接停止请求设置 0：检测用信号未设定为直接停止请求信号1：检测用信号设定为直接停止请求信号	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
7:4	NFS[3:0]	直接停止请求选择 禁止其他设置。 0x0：比较器电平检测00x1：比较器电平检测10x2：比较器电平检测20x4：比较器电平检测30x7：GTETRn引脚输入电平检测（n=A到D） 其他：禁止设置	R/W
8	NFV	直接停止请求主动感知 0：输出停止检测信号为0时请求停止输出1：输出停止检测信号为1时请求停止输出	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

GTONCCRn寄存器（n=A到D）设置停止输出以响应检测到的信号的请求。

NE位（直接停止请求设置）

将1写入NE位会导致直接输出停止请求信号以响应由NFS[3:0]位选择的检测信号。

20.3 Operation

20.3.1 请求停止输出以响应对输入电平的检测对应的GTETRn引脚（n=A到D）

有两种类型的输出停止请求：响应POEGGn.PIDF标志（n=A到D）的设置的请求，以及响应检测到的信号的直接请求。

1.要请求停止输出以响应PIDF标志的设置，在POEGGn寄存器中设置输入（在INV位中设置反转或非反转，通过NFEN位启用或禁用过滤，用于过滤的采样时钟设置在当POEGGn.PIDE位为1时检测到NFCS[1:0]位.要取消断言停止输出的请求信号，请清除POEGGn.PIDF标志。关于取消停止输出的请求，请参阅第20.3.6节。取消停止输出的请求。

2.请求停止输出以直接响应检测到所选信号的输入电平，输入设置在
POEGGn（在INV位中设置反转或非反转，通过NFEN位启用或禁用过滤，在NFCS[1:0]位中设置用于过滤的采样时钟）和GTONCCRn寄存器（在NFV位中设置主动检测）到当GTONCCRn.NE位为1时，检测到GTONCCRn.NFS[3:0]位中选择的GTETRn引脚，然后直接向GPT的每个通道组发出停止输出的请求。请求停止输出的信号被取消断言，当

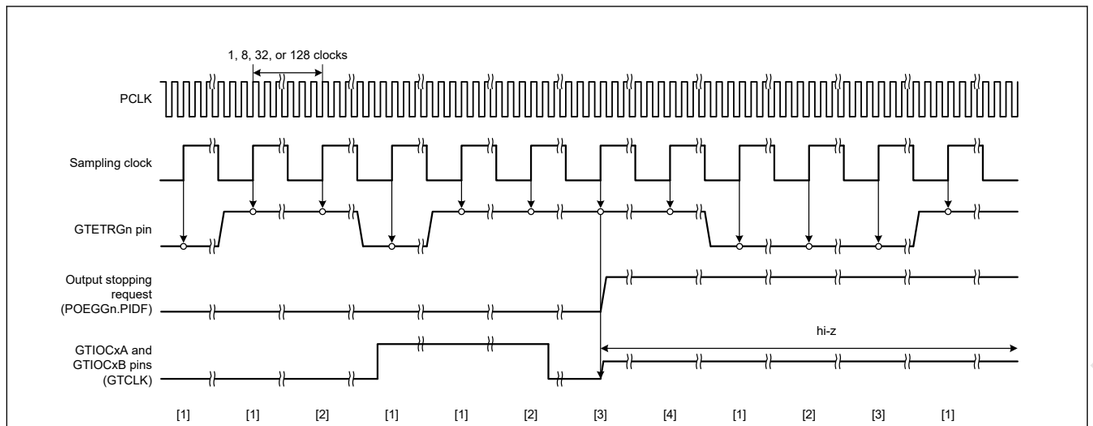
detected input level does not match the conditions for issuing a request. For details, see section 20.3.7. Requests to Stop Output in Response to Detected Signals and Cancelling the Requests.

20.3.1.1 Digital Noise Filter

Each GTETRGn pin input has a digital noise filter. Figure 20.2 shows the operation example in detection of the high level with the use of the filter. When the digital noise filter is enabled (POEGGn.NFEN bit = 1) and the high level is detected 3 consecutive times with the sampling clock cycle selected by the POEGGn.NFCS[1:0] bits while inverted or non-inverted according to the setting of the POEGGn.INV bit, this is regarded as detection of the high level, and the request to stop output is issued to the GPT.

At this time, if the low level is detected even once in the sequence, it is not regarded as detection of the high level. In addition, changes in the levels on pins GTETRGA through GTETRGD are ignored while the sampling clock is not being output.

Digital noise filters can be used with requests to stop output in response to setting of the POEGGn.PIDF flags (n = A to D), requests to stop output in direct response to a detected signal, and the output of external triggers to the GPT.



Note: Each channel output can be set by the GPT32x.
Note: The polarity can be inverted by setting the POEGGn.INV bit.
Note: PCLK = PCLKB

Figure 20.2 Example for Operation of Digital Noise Filter

20.3.2 Requests to Stop Output in Response to Detection of Output Stopping from GPT

When any among a dead-time error or simultaneous high- or low-level output from the GPT is detected, the corresponding POEGGn.IOCF flag is set to 1 and the request to stop output per group is issued to each channel in the GPT. The POEGGn.IOCF flag is used to indicate both edge detection by the comparator and requests to stop output. To cancel a request to stop output, clear the given POEGGn.IOCF flag. For details, see section 20.3.6. Cancelling Requests to Stop Output.

To detect any among a dead-time error or simultaneous high- or low-level output from the GPT, detection of output stopping must be permitted in the GRPDTE, GRPABH, and GRPABL bits of the given GPT32n.GTINTAD register. Specify the group of the GPT for which stopping is to be detected in the GPT32n.GTINTAD.GRP[1:0] bits. For details, see section 21.2.15. GTINTAD : General PWM Timer Interrupt Output Setting Register.

20.3.3 Request to Stop Output in Response to Comparator Detection

A request to stop output can be issued to the GPT in response to detection by a comparator. There are two types of request to stop output: requests output in response to setting of a POEGGn.IOCF flag (n = A to D) due to edge detection by the comparator and requests that are directly output in response to level detection by the comparator.

1. To stop output in response to setting of an IOCF flag, the corresponding edge is detected by the comparator while the POEGGn.CDRE[3:0] bits are 1. The POEGGn.IOCF flag is then set to 1, which leads to a request to stop output from

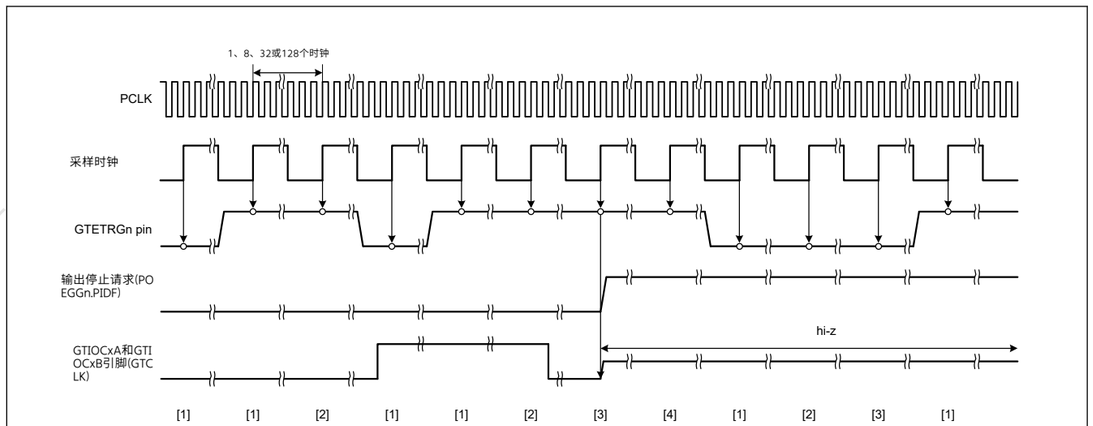
检测到输入电平与发出请求的条件不匹配。详见20.3.7节。请求停止输出以响应检测到的信号并取消请求。

20.3.1.1 数字噪声滤波器

每个GTETRn引脚输入都有一个数字噪声滤波器。图20.2显示了使用滤波器检测高电平的操作示例。当数字噪声滤波器被使能（POEGGn.NFEN位=1）并且高电平检测到连续3次时，使用POEGGn.NFCS[1:0]位选择的采样时钟周期，同时根据反相或非反相POEGGn.INV位的置位，视为检测到高电平，向GPT发出停止输出的请求。

此时，如果在序列中仅检测到一次低电平，则不认为检测到高电平。此外，在不输出采样时钟时，引脚GTETRGA至GTETRGD上的电平变化将被忽略。

数字噪声滤波器可用于请求停止输出以响应POEGGn.PIDF标志（n=A到D）的设置、请求停止输出以直接响应检测到的信号以及向GPT输出外部触发器.



Note: 每个通道输出都可以由GPT32x设置。
Note: 可以通过设置POEGGn.INV位来反转极性。
Note: PCLK = PCLKB

Figure 20.2 数字噪声滤波器的操作示例

20.3.2 请求停止输出以响应检测到来自GPT的输出停止

当检测到GPT出现死区错误或同时输出高电平或低电平时，相应的POEGGn.IOCF标志设置为1，并且向GPT中的每个通道发出停止每组输出的请求。这POEGGn.IOCF标志用于指示比较器的边沿检测和请求停止输出。要取消停止输出的请求，请清除给定的POEGGn.IOCF标志。详见20.3.6节。取消停止输出的请求。

要检测GPT的死区错误或同时高电平或低电平输出中的任何一个，必须在给定GPT32n.GTINTAD寄存器的GRPDTE、GRPABH和GRPABL位中允许检测输出停止。在GPT32n.GTINTAD.GRP[1:0]位中指定要检测停止的GPT组。有关详细信息，请参阅第21.2.15节。GTINTAD：通用PWM定时器中断输出设置寄存器。

20.3.3 请求停止输出以响应比较器检测

响应比较器的检测，可以向GPT发出停止输出的请求。有两种类型的输出停止请求：由于比较器的边沿检测，请求输出以响应POEGGn.IOCF标志(n=A到D)的设置，以及响应比较器的电平检测而直接输出的请求.

1.为了响应IOCF标志的设置停止输出，当POEGGn.CDRE[3:0]位为1时，比较器检测到相应的边沿。然后POEGGn.IOCF标志设置为1，这导致停止输出的请求

the given group for each channel of the GPT. The POEGGn.IOCF flag is used for both comparator edge detection and the request to stop output. To cancel the request to stop output, clear the POEGGn.IOCF flag. For details, see section 20.3.6. Cancelling Requests to Stop Output.

2. The output can also be stopped by using a detected signal as a direct request to stop output. When the comparator level detection signal selected in the GTONCCRn.NFS[3:0] bits matches the level set in the GTONCCRn.NFV bit, the request to stop output per group is issued to each channel of the GPT. The request to stop output is released when the comparator level detection does not match the issuing conditions. For details, see section 20.3.7. Requests to Stop Output in Response to Detected Signals and Cancelling the Requests.

20.3.4 Requests to Stop Output by Oscillation Stop Detection

When the circuit for detecting stopping of oscillation by the main clock oscillator detects the stopping of the oscillation while a POEGGn.OSTPE bit is 1, the POEGGn.OSTPF flag is set to 1 and a request to stop output per group is issued to each channel of the GPT. To cancel the request to stop output, clear the POEGGn.OSTPF flag. For details, see section 20.3.6. Cancelling Requests to Stop Output.

20.3.5 Requests to Stop Output by a Register

Writing 1 to the software stop flag (POEGGn.SSF) leads to a request to stop output per group to each channel in the GPT. To release from the request to disable output, clear the POEGGn.SSF flag. For details, see section 20.3.6. Cancelling Requests to Stop Output.

20.3.6 Cancelling Requests to Stop Output

Requests to stop output are cancelled in any of the following three ways.

1. Cancellation by a reset (return to the initial state)
2. Cancellation by clearing all flags in the POEGGn register
3. Cancellation in response to direct input of a detected signal

(1) Cancellation by a reset

Any type of reset can cancel a request to stop output. For details, see section 5, Resets.

(2) Cancellation by clearing all flags in the POEGGn register

- POEGGn.PIDF
- POEGGn.IOCF
- POEGGn.OSTPF
- POEGGn.SSF

Cancellation of the request is taken into the GPT at the end of the cycle of counting by the GPT, and the output pins are released from being stopped no less than 3 GTCLK cycles from that time. Figure 20.3 shows the timing of release from the output-stopped state. To clear each of the flags, read the status flag for each source to check that the source condition is not being detected, and then write 0. Sources other than the edge detection by the comparators cannot be cleared even if the flag is cleared in the detected state. Since the comparators detect edges in edge detection, writing 0 in the detected state clears the flag, and the flag is not set until the relevant source generates the next edge. Status flags for the respective sources are listed below.

Detection of input level	POEGGn.ST (GTETRGn input status flag)
Comparator edge detection	ACMPHSn.CMPMON.CMPMON (comparator output monitoring flag)
Oscillation stop detection	OSTDSR.OSTDF (oscillation stop detection flag)
Stopping detection from the GPT	GPT32n.GTST.DTEF (dead time error flag) GPT32n.GTST.OABLF (same time output level low flag) GPT32n.GTST.OABHF (same time output level high flag)

GPT的每个通道的给定组。POEGGn.IOCF标志用于比较器边沿检测和停止输出的请求。要取消停止输出的请求，请清除POEGGn.IOCF标志。详见20.3.6节。取消停止输出的请求。

2.也可以将检测到的信号作为停止输出的直接请求来停止输出。当GTONCCRn.NFS[3:0]位中选择的比较器电平检测信号与GTONCCRn.NFV位中设置的电平匹配时，将向GPT的每个通道发出停止每组输出的请求。当比较器电平检测与发出条件不匹配时，停止输出请求被释放。详见20.3.7节。请求停止输出以响应检测到的信号并取消请求。

20.3.4 通过振荡停止检测请求停止输出

当通过主时钟振荡器检测振荡停止的电路在POEGGn.OSTPE位为1时检测到振荡停止时，POEGGn.OSTPF标志设置为1，并且向每个通道发出停止每组输出的请求GPT的。要取消停止输出的请求，请清除POEGGn.OSTPF标志。详见20.3.6节。取消停止输出的请求。

20.3.5 通过寄存器请求停止输出

将1写入软件停止标志(POEGGn.SSF)会导致请求停止对GPT中每个通道的每组输出。
要解除禁用输出的请求，请清除POEGGn.SSF标志。详见20.3.6节。取消
请求停止输出。

20.3.6 取消停止输出的请求

通过以下三种方式中的任何一种取消停止输出的请求。

1.通过reset取消（返回初始状态）

2.通过清除POEGGn寄存器中的所有标志来取消

3.响应于检测信号的直接输入而取消

(1) 通过重置取消

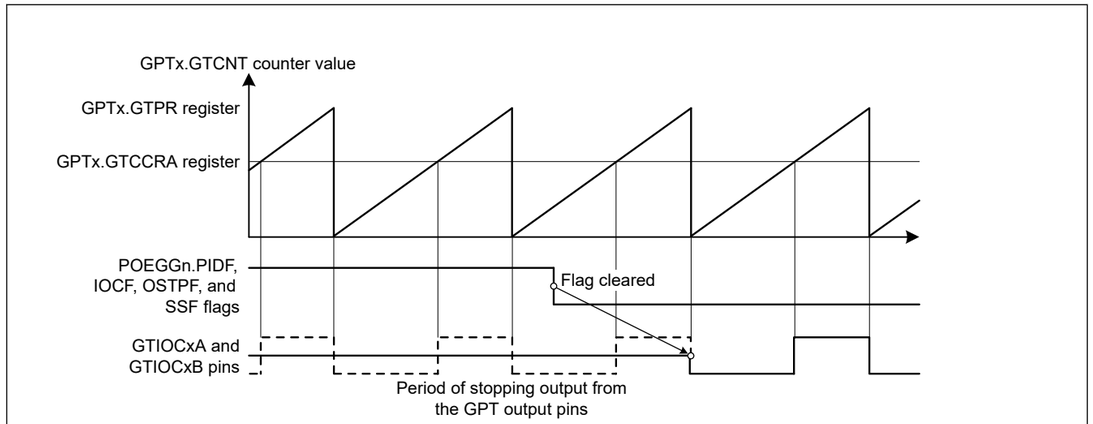
任何类型的复位都可以取消停止输出的请求。有关详细信息，请参阅第5节，重置。

(2) 通过清除POEGGn寄存器中的所有标志来取消

- POEGGn.PIDF
- POEGGn.IOCF
- POEGGn.OSTPF
- POEGGn.SSF

在GPT的计数周期结束时，请求的取消进入GPT，并且从那时起不少于3个GTCLK周期后，输出引脚被解除停止。图20.3显示了从输出停止状态释放的时间。要清除每个标志，请读取每个源的状态标志以检查未检测到源条件，然后写入0。即使在检测到的状态。由于比较器在边沿检测中检测边沿，因此在检测状态下写入0会清除标志，并且在相关源生成下一个边沿之前不会设置标志。下面列出了各个源的状态标志。

输入电平检测	POEGGn.ST（GTETRn输入状态标志）
比较器边缘检测	ACMPHSn.CMPMON.CMPMON（比较器输出监视标志）
振荡停止检测	OSTDSR.OSTDF（振荡停止检测标志）
停止从GPT检测	GPT32n.GTST.DTEF（死区时间错误标志） GPT32n.GTST.OABLF（同时输出电平低标志）GPT32n.GT ST.OABHF（同时输出电平高标志）



Note: GPTx indicates GPT32x.

Figure 20.3 Timing of Re-enabling Output from the GPT Output Pins Following Cancellation of a Request to Stop Output

(3) Cancellation in response to direct input of a detected signal

For details, see section 20.3.7. Requests to Stop Output in Response to Detected Signals and Cancelling the Requests.

20.3.7 Requests to Stop Output in Response to Detected Signals and Cancelling the Requests

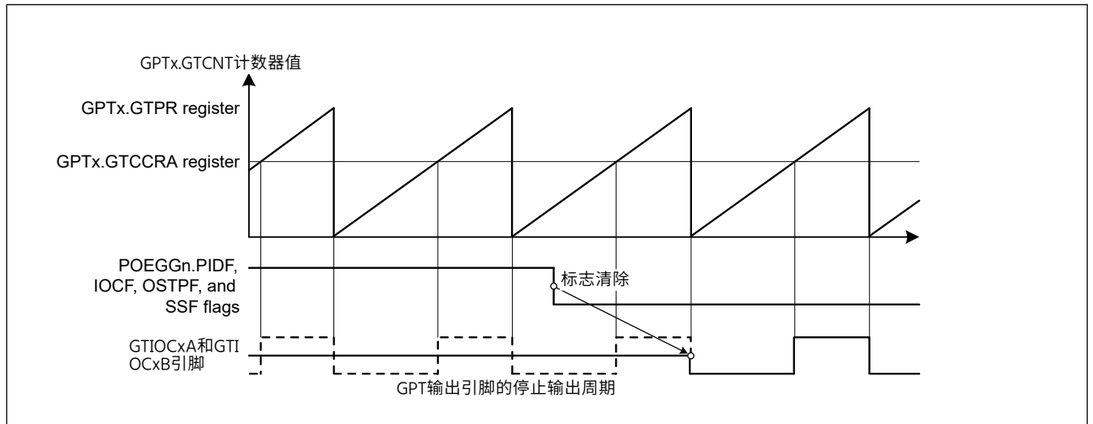
The input level detection signals on the GTETRGn pin (n = A to D) and comparator level detection signals on the ACMPHSm (m = 0 to 3) can be used as direct requests to stop output in response to detected signals. The sources of the signals for detection are selected in the GTONCCRn.NFS[3:0] bits, and the active senses of the signals for detection are set in the GTONCCRn.NFV bit. Setting a GTONCCRn.NE bit to activate direct requests to stop output results in the issuing of a request to stop output to the GPT when the selected source signal for output stopping detection is generated.

The request to stop output is released when the input level detection signals on the GTETRGn pin or comparator level detection does not match the issuing conditions. To cancel a request, confirm that the values of the PIDF and IOCF flags in the POEGGn register have become 0.

Figure 20.4 shows the operation of a request to stop output issued in response to level detection by the ACMPHS0. The example shows the case where the comparator detects the analog input voltage on ACMPHS0 becoming higher than the reference voltage while the GPT is producing PWM waveforms on the GTIOC0A pin on a cyclic-counting basis, and the level-detection signal from the comparator is input to the POEG. The POEG outputs a request to stop output to the GPT on the basis of detection as described above, and the GPT remains stopped until the end of the cycle of counting, even if the request to stop output is cancelled before then.

If the request to stop output has not been cancelled at the end of the cycle of counting cycle, output from the GPT remains stopped until the end of the next cycle of counting, and so on.

The output-stopped state can be checked by reading the ODF flag in General PWM Timer Status Register (GTST) of the GPT. For details, see the description of the ODF flag in section 21.2.16. GTST : General PWM Timer Status Register.
Figure 20.5 shows the procedure for setting requests to stop output in response to detected signals.



Note: GPTx indicates GPT32x.

Figure 20.3 取消请求后从GPT输出引脚重新启用输出的时序停止输出

(3) 响应于检测信号的直接输入而取消

详见20.3.7节。请求停止输出以响应检测到的信号并取消请求。

20.3.7 请求停止输出以响应检测到的信号并取消Requests

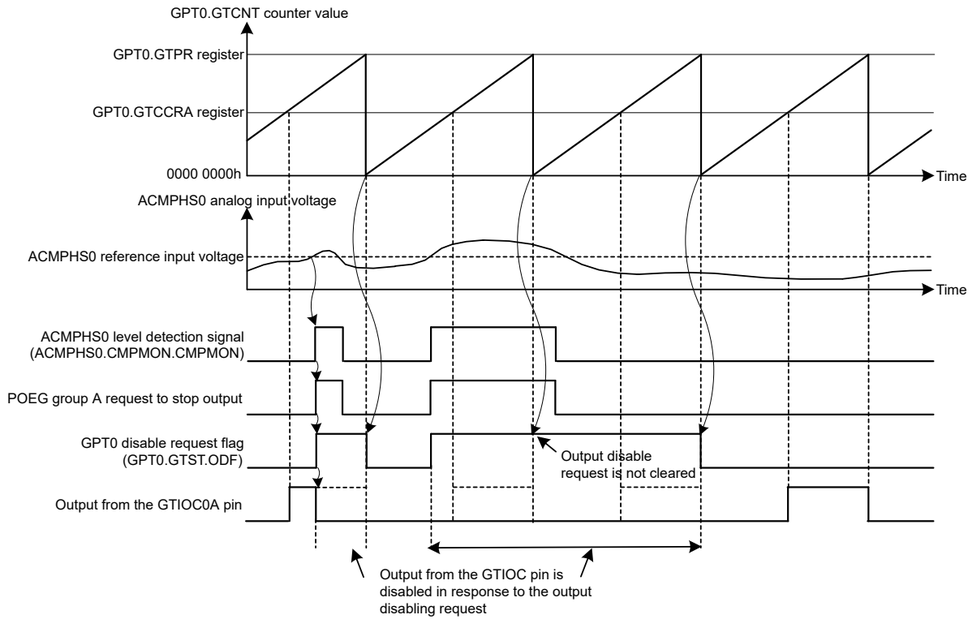
GTETRn引脚(n=A至D)上的输入电平检测信号和比较器电平检测信号
ACMPHSm（m=0到3）可用作响应检测到的信号停止输出的直接请求。检测信号源在GTONCCRn.NFS[3:0]位中选择，检测信号的有效检测在GTONCCRn.NFV位中设置。设置GTONCCRn.NE位以激活停止输出的直接请求会导致在生成用于输出停止检测的选定源信号时发出停止向GPT输出的请求。

当GTETRn引脚上的输入电平检测信号或比较器电平检测与发出条件不匹配时，停止输出的请求被解除。要取消请求，请确认POEGGn寄存器中的PIDF和IOCF标志的值已变为0。

图20.4显示了响应ACMPHS0的电平检测而发出的停止输出请求的操作。该示例显示了比较器检测到ACMPHS0上的模拟输入电压高于参考电压的情况，同时GPT在GTIOC0A引脚上循环计数产生PWM波形，输入比较器的电平检测信号到POEG。POEG基于上述检测向GPT输出停止输出请求，即使在此之前停止输出请求被取消，GPT也保持停止直到计数周期结束。

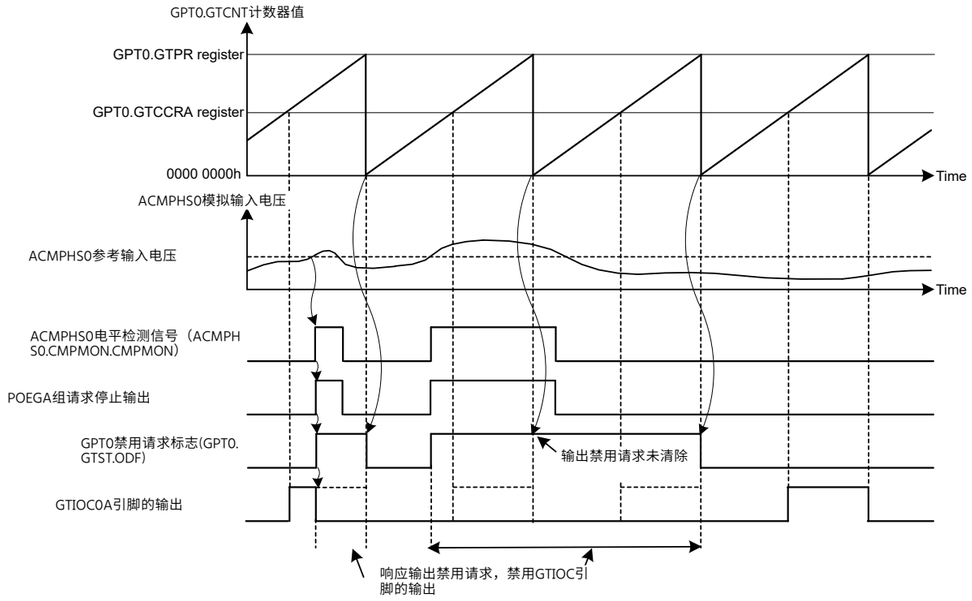
如果在计数周期结束时停止输出的请求没有被取消，则GPT的输出保持停止，直到下一个计数周期结束，依此类推。

输出停止状态可以通过读取通用PWM定时器状态寄存器(GTST)中的ODF标志来检查。
GPT。详见21.2.16节对ODF标志的描述。GTST：通用PWM定时器状态寄存器。
图20.5显示了设置请求以停止输出以响应检测到的信号的过程。



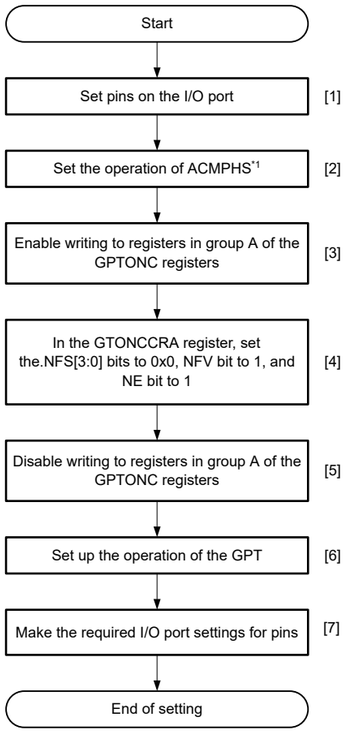
Note: GPT0 indicates GPT320.

Figure 20.4 Example of Operation to Stop Output from the GTIOC Pin In Response to Level Detection by a Comparator



Note: GPT0 indicates GPT320.

Figure 20.4 响应于电平检测而停止GTIOC引脚输出的操作示例



[1] Make the I/O port settings.
Set the corresponding pins of the I/O port to general purpose I/O port pins in order to use the ACMPHS0 analog input pin function and GPT output pin function.

[2] Set the operation of ACMPHS0 to output a level detection signal to the POEG in response to comparing the analog input voltage and reference input voltage.

[3] Write 0xA500 to the GTONCWPA register to enable writing to the GTONCCPRA register.

[4] Select level detection for the comparator by setting the GTONCCRA.NFS[3:0] bits to 0x0. Set the GTONCCRA.NFV bit to 1 so that the request to stop output is sent when the selected source indicates 1.
Set the GTONCCRA.NE bit to 1 to enable the output of requests to stop output.

[5] Write 0xA501 to the GTONCWPA register to disable writing to the GTONCCPRA register.

[6] Set the GPT for the output of a PWM waveform on its GTIOCn pin.

[7] Set the I/O port in order to use the required analog input pin of ACMPHS0 and output pin of the GPT.

The settings described above lead to the output of requests to stop output in response to comparison of the analog input voltage and reference input voltage while a PWM waveform is being output from the GPT pin, stopping output from the GPT pin.

Note 1. In this example, the comparator output is non-inverted.

Figure 20.5 Example of Settings to Stop Output on the GTIOC Pin in Response to Level Detection by a Comparator

20.4 Interrupt Sources

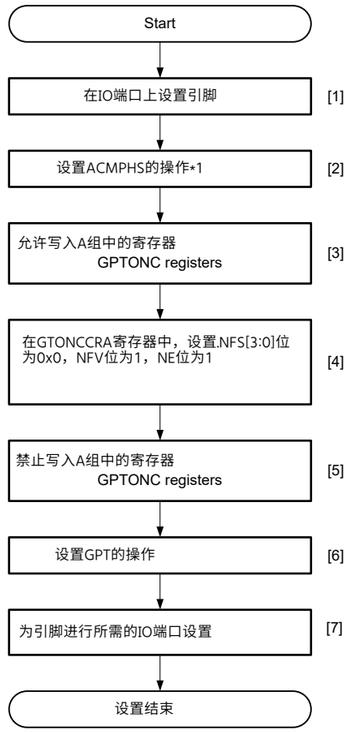
The POEG generates interrupts for the interrupt controller when any of the following is detected.

- Detection of level of input, indicated by the POEGGn.PIDF flag
- Detection of stopping of output from the GPT, indicated by the POEGGn.IOCF flag
- Detection of edges by the comparator, indicated by the POEGGn.IOCF flag

Table 20.3 shows interrupt sources and conditions.

Table 20.3 Interrupt sources and conditions (1 of 2)

Interrupt source	Symbol	Corresponding flag	Trigger condition
POEG Group A Interrupt	POEG_GROUPA	POEGGA.IOCF	Detection of stopping of output from the GPT
			Detection of edges by the comparator
		POEGGA.PIDF	Detection of the level input from the GTETRGA pin



[1]进行IO端口设置。将IO端口的相应引脚设置为通用IO端口引脚，以使用ACMPHS0模拟输入引脚功能和GPT输出引脚功能。

[2]设置ACMPHS0的操作，以响应比较模拟输入电压和参考输入电压，向POEG输出电平检测信号。

[3]将0xA500写入GTONCWPA寄存器以启用对GTONCCPRA寄存器的写入。

[4]通过将GTONCCRA.NFS[3:0]位设置为0x0来选择比较器的电平检测。将GTONCCRA.NFV位设置为1，以便在所选源指示1时发送停止输出请求。将GTONCCRA.NE位设置为1以启用停止输出请求的输出。

[5]将0xA501写入GTONCWPA寄存器以禁止写入GTONCCPRA寄存器。

[6]将GPT设置为在其GTIOCn引脚上输出PWM波形。

[7]设置IO端口以使用ACMPHS0所需的模拟输入引脚和GPT的输出引脚。

上述设置导致在从GPT引脚输出PWM波形时，响应模拟输入电压和参考输入电压的比较，发出停止输出请求，停止从GPT引脚输出。

注1.在本例中，比较器输出是非反相的。

Figure 20.5 响应于电平检测的GTIOC引脚上停止输出的设置示例 Comparator

20.4 中断源

当检测到以下任何情况时，POEG为中断控制器生成中断。

●检测输入电平，由POEGGn.PIDF标志指示
●检测到GPT输出停止，由POEGGn.IOCF标志指示
●比较器检测边缘，由POEGGn.IOCF标志指示

表20.3显示了中断源和条件。

Table 20.3 中断源和条件(1of2)

中断源	Symbol	对应标志	触发条件
POEGA组中断	POEG_GROUPA	POEGGA.IOCF	检测GPT的输出停止
			比较器检测边缘
		POEGGA.PIDF	检测从GTETRGA引脚输入的电平

Table 20.3 Interrupt sources and conditions (2 of 2)

Interrupt source	Symbol	Corresponding flag	Trigger condition
POEG Group B Interrupt	POEG_GROUPB	POEGGB.IOCF	Detection of stopping of output from the GPT
			Detection of edges by the comparator
		POEGGB.PIDF	Detection of the level input from the GTETRGB pin
POEG Group C Interrupt	POEG_GROUPC	POEGGC.IOCF	Detection of stopping of output from the GPT
			Detection of edges by the comparator
		POEGGC.PIDF	Detection of the level input from the GTETRGC pin
POEG Group D Interrupt	POEG_GROUPD	POEGGD.IOCF	Detection of stopping of output from the GPT
			Detection of edges by the comparator
		POEGGD.PIDF	Detection of the level input from the GTETRGD pin

20.5 External Trigger Output to GPT

Detection of the level input from the GTETRGD pin can be monitored by the POEGGn.ST flag via active-sense selection and digital noise filtering. The GPT can function as follows in response to external trigger signals.

- Count start
- Count stop
- Counter clearing
- Up-counting
- Down-counting
- Input capture

For details of the above functions, see section 21, General PWM Timer (GPT).

20.6 Usage Notes

20.6.1 Transitions to Low-Power Modes

When the POEG is used, it should not be transitioned to software standby or deep software standby modes. In this mode, the stopping of output cannot be requested since the POEG is stopped.

20.6.2 Setting the Function for Stopping the Module

The module-stop control register can be set to enable or disable operation of the POEG. The POEG is stopped immediately after a reset. Registers of the POEG become accessible following release from the module-stopped state. For details, see section 10, Low Power Modes.

20.6.3 Duplication of Requests to Stop Output

While either the PIDF or IOCF flag in the POEGGn register is 1, cancellation of requests to stop by the detection signal set in the GTONCCRn register does not work due to the request to stop still being output because of the value of the flag. That is, note that requests to stop output will not be cancelled when a corresponding flag is set stop output in response to detection. Request signals to stop output in response to flag setting are obtained as the logical OR of the corresponding detection signals for stopping output.

Table 20.3 中断源和条件(2of2)

中断源	Symbol	对应标志	触发条件
POEGB组中断	POEG_GROUPB	POEGGB.IOCF	检测GPT的输出停止
			比较器检测边缘
		POEGGB.PIDF	检测来自GTETRGB引脚的电平输入
POEGC组中断	POEG_GROUPC	POEGGC.IOCF	检测GPT的输出停止
			比较器检测边缘
		POEGGC.PIDF	检测从GTETRGC引脚输入的电平
POEGD组中断	POEG_GROUPD	POEGGD.IOCF	检测GPT的输出停止
			比较器检测边缘
		POEGGD.PIDF	检测从GTETRGD引脚输入的电平

20.5 外部触发输出到GPT

从GTETRGD引脚输入电平的检测可以通过POEGGn.ST标志通过有源检测选择和数字噪声过滤进行监控。GPT响应外部触发信号可以如下工作。

●计数开始
●计数停止
●清盘
- Up-counting
- Down-counting

●输入捕捉

有关上述功能的详细信息，请参见第21节，通用PWM定时器(GPT)。

20.6 使用说明

20.6.1 过渡到低功耗模式

使用POEG时，不应将其转换为软件待机或深度软件待机模式。在此模式下，由于POEG已停止，因此无法请求停止输出。

20.6.2 设置模块停止功能

模块停止控制寄存器可以设置为启用或禁用POEG的操作。POEG在复位后立即停止。POEG的寄存器在从模块停止状态释放后变得可访问。有关详细信息，请参阅第10节，低功耗模式。

20.6.3 停止输出的重复请求

当POEGGn寄存器中的PIDF或IOCF标志为1时，通过GTONCCRn寄存器中设置的检测信号取消停止请求不起作用，因为该标志的值仍在输出停止请求。即，请注意，当相应标志设置为响应检测停止输出时，停止输出的请求不会被取消。响应于标志设置停止输出的请求信号作为相应的停止输出检测信号的逻辑或获得。

21. General PWM Timer (GPT)

21.1 Overview

The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 10 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.

This GPT provides the high resolution PWM waveform generation function for the channel 0 to 3, the A/D conversion start request function, the asymmetric automatic dead time setting function, and the enhanced interrupt skipping function. In addition, it is enhanced with the external pulse width measuring function for the channel 0 to 3, the additional PWM modes for the channel 4 to 9, the extended buffer transfer function, the GTCPPO pin output function, and the inter-channel cooperation function.

Table 21.1 lists the GPT specifications, Table 21.2 shows the GPT functions, and Figure 21.1 shows a block diagram.

Table 21.1 GPT specifications

Parameter	Description
Functions	• 32 bits × 10 channels (GPT32n (n = 0 to 9)) • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter • Clock sources independently selectable for each channel • Two input/output pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms • Registers for setting up frame cycles in each channel with capability for generating interrupts at overflow or underflow • Generation of dead times in PWM operation • Generation of high accuracy duty in the vicinity of duty 0% and 100% PWM waveform • In output compare operation, setting compare register is immediately used to generate PWM waveform with dead times • Synchronous starting, stopping and clearing counters for arbitrary channels • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to a maximum of 8 ELC events • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to the status of two input pins • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to a maximum of 4 external triggers • Output pin disable function by dead time error and detected short-circuits between output pins • A/D conversion start request generation function • PWM waveform for controlling brushless DC motors can be generated • Compare match A to F event, overflow/underflow event, and input UVW edge event can be output to the ELC • Enables the noise filter for input capture and input UVW • Period count function • External pulse width measuring function • Logical operation between the channel output • Synchronous counter clearing/counter setting/input capture among channels • Bus clock: PCLKA, Core clock: GTCLK*1 • Frequency ratio: PCLKA:PCLKD = 1:N (N = 1/2/4/8/16/32/64) (when using synchronous clock), PCLKA ≤ GTCLK (when using asynchronous clock)

Note 1. GPT core clock (GTCLK) is PCLKD when synchronous clock is selected, and GPTCLK when asynchronous clock is selected. See Figure 21.3.

21. 通用PWM定时器(GPT)

21.1 Overview

通用PWM定时器(GPT)是一个具有GPT32×10通道的32位定时器。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。此外，可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。

该GPT提供通道0到3的高分辨率PWM波形生成功能、AD转换启动请求功能、非对称自动死区时间设置功能以及增强的中断跳过功能。此外，还增强了通道0至3的外部脉冲宽度测量功能、通道4至9的附加PWM模式、扩展缓冲区传输功能、GTCPPO引脚输出功能和通道间协作功能.

表21.1列出了GPT规范，表21.2显示了GPT功能，图21.1显示了框图。

Table 21.1 GPT specifications

Parameter	Description
Functions	• 32位×10通道(GPT32n(n=0to9)) • 每个计数器的递增计数或递减计数（锯齿波）或递增递减计数（三角波） • 每个通道可独立选择时钟源 • 每个通道两个输入输出引脚 • 每个通道两个输出比较输入捕捉寄存器 • 每个通道的两个输出比较输入捕捉寄存器，提供四个寄存器作为缓冲寄存器，在不使用缓冲时可以作为比较寄存器工作 • 在输出比较操作中，缓冲器切换可以处于波峰或波谷，从而能够生成横向不对称的PWM波形 • 用于在每个通道中设置帧周期的寄存器，能够在上溢或下溢时产生中断 • 在PWM操作中产生死区 • 在占空比0%和100%PWM波形附近产生高精度占空比 • 在输出比较操作中，设置比较寄存器立即用于生成带死区时间的PWM波形 • 任意通道的同步启动、停止和清除计数器 • 响应最多8个ELC事件的计数开始、计数停止、计数清除、递增计数、递减计数或输入捕获操作 • 计数开始、计数停止、计数清除、递增计数、递减计数或输入捕捉操作以响应两个输入引脚的状态 • 计数开始、计数停止、计数清除、递增计数、递减计数或输入捕捉操作，以响应最多4个外部触发 • 通过死区时间错误和检测到的输出引脚之间的短路来禁用输出引脚功能 • AD转换开始请求生成功能 • 可生成控制无刷直流电机的PWM波形 • 比较匹配A到F事件、上溢下溢事件和输入UVW边缘事件可以输出到ELC • 为输入捕获和输入UVW启用噪声滤波器 • 周期计数功能 • 外部脉宽测量功能 • 通道输出之间的逻辑运算 • 通道间同步计数器清零计数器设置输入捕捉 • 总线时钟：PCLKA，核心时钟：GTCLK*1 • 频率比：PCLKA:PCLKD=1:N(N=1248163264)（使用同步时钟时），PCLKA≤GTCLK（使用异步时钟时）

注1.选择同步时钟时GPT内核时钟(GTCLK)为PCLKD，选择异步时钟时为GPTCLK。看 Figure 21.3.

Table 21.2 GPT functions (1 of 2)

Parameter		Description
Count clock		GTCLK GTCLK/2 GTCLK/4 GTCLK/8 GTCLK/16 GTCLK/32 GTCLK/64 GTCLK/128 GTCLK/256 GTCLK/512 GTCLK/1024 GTETRGA, GTETRGB, GTETRGC, GTETRGD
Output compare/input capture registers (GTCCR)		GTCCRA GTCCRB
Compare/buffer registers		GTCCRC GTCCRD GTCCRE GTCCRF
Cycle setting register		GTPR
Cycle setting buffer register		GTPBR GTPDBR
I/O pins		GTIOCnA GTIOCnB (n = 0 to 9)
External trigger input pin*1		GTETRGA GTETRGB GTETRGC GTETRGD
Counter clear sources		GTPR register compare match Input capture Input pin status ELC event input GTETRGn (n = A to D) pin input GTCCR register compare match Other channel's counter clear sources
Period count function		Available (GPT32n (n = 0 to 3))
Compare match output	Low output	Available
	High output	Available
	Toggle output	Available
Input capture function		Available
Automatic addition of dead time		Available
PWM mode		Available
High accuracy PWM waveform		Available (GPT32n (n = 0 to 3))
Phase count function		Available (GPT32n (n = 0 to 3))
External pulse width measuring function		Available (GPT32n (n = 0 to 3))
Buffer operation		Double buffer Simultaneous operation disable control for multiple channels Buffer operation by counter clearing/compare match
One-shot operation		Available
DMAC/DTC activation		All the interrupt sources
A/D conversion start request		Compare match of GTADTRA or GTADTRB register
Brushless DC motor control function		Available

Table 21.2 GPT函数(1of2)

Parameter		Description
计数时钟		GTCLK GTCLK/2 GTCLK/4 GTCLK/8 GTCLK/16 GTCLK/32 GTCLK/64 GTCLK/128 GTCLK/256 GTCLK/512 GTCLK/1024 GTETRGA, GTETRGB, GTETRGC, GTETRGD
输出比较输入捕捉寄存器(GTCCR)		GTCCRA GTCCRB
Compare/buffer registers		GTCCRC GTCCRD GTCCRE GTCCRF
周期设定寄存器		GTPR
周期设置缓冲寄存器		GTPBR GTPDBR
I/O pins		GTIOCnA GTIOCnB (n = 0 to 9)
外部触发输入引脚*1		GTETRGA GTETRGB GTETRGC GTETRGD
反清源		GTPR寄存器比较匹配 输入捕捉 输入引脚状态EL C事件输入 GTETRn(n=AtoD)引脚输入GTCC R寄存器比较匹配 其他渠道反清源
周期计数功能		可用（GPT32n（n=0到3））
比较匹配输出	低输出	Available
	高输出	Available
	切换输出	Available
输入捕捉功能		Available
自动添加死区时间		Available
PWM mode		Available
高精度PWM波形		可用（GPT32n（n=0到3））
相位计数功能		可用（GPT32n（n=0到3））
外部脉宽测量功能		可用（GPT32n（n=0到3））
缓冲操作		双缓冲 多通道同时操作禁用控制 通过计数器清除比较匹配进行缓冲操作
One-shot operation		Available
DMAC/DTC activation		所有中断源
AD转换开始请求		比较GTADTRA或GTADTRB寄存器的匹配
直流无刷电机控制功能		Available

Table 21.2 GPT functions (2 of 2)

Parameter	Description
Interrupt sources	11 sources • GTCCRA compare match/input capture(GPTn_CCMPA) • GTCCRB compare match/input capture(GPTn_CCMPB) • GTCCRC compare match(GPTn_CMPC) • GTCCRD compare match(GPTn_CMPD) • GTCCRE compare match(GPTn_CMPE) • GTCCRF compare match(GPTn_CMPF) • GTADTRA compare match (GPTn_ADTRGA) • GTADTRB compare match (GPTn_ADTRGB) • GTCNT overflow (GTPR compare match) (GPTn_OVF) • GTCNT underflow (GPTn_UDF) • GTPC count stop(GPTx_PC) (x = 0 to 3)
Interrupt skipping function	• Skipping of interrupts of GTCNT counter overflow (GTPR register compare match) (GTPn_OVF) and GTCNT counter underflow (GTPn_UDF) (interlocked with other interrupts and A/D conversion start requests) • Skipping of GTADTRA and GTADTRB register compare match (GPT32y (y = 4 to 9)) • Buffer operation skipping function
Event linking (ELC) function	Available*2
Noise filtering function	Available
Logical operation between the channel output	Available
Synchronous counter clearing/counter setting/input capture	Available

Note 1. GTETRGn connects to GPT through the POEG module. Therefore, to use the GPT function, supply the POEG clock by clearing the MSTPCRD.MSTPDn (n = 11 to 14) bit.
Note 2. See section 21.6. Operations Linked by ELC.

Table 21.2 GPT功能（2个中的2个）

Parameter	Description
中断源	11 sources • GTCCRA compare match/input capture(GPTn_CCMPA) • GTCCRB compare match/input capture(GPTn_CCMPB) • GTCCRC compare match(GPTn_CMPC) • GTCCRD compare match(GPTn_CMPD) • GTCCRE compare match(GPTn_CMPE) • GTCCRF compare match(GPTn_CMPF) • GTADTRA比较匹配(GPTn_ADTRGA) • GTADTRB比较匹配(GPTn_ADTRGB) • GTCNT溢出（GTPR比较匹配）（GPTn_OVF） • GTCNT underflow (GPTn_UDF) • GTPC计数停止（GPTx_PC）（x=0到3）
中断跳跃功能	• 跳过GTCNT计数器溢出（GTPR寄存器比较匹配）（GTPn_OVF）和GTCNT计数器下溢（GTPn_UDF）的中断（与其他中断和AD转换开始请求互锁） • 跳过GTADTRA和GTADTRB寄存器比较匹配(GPT32y(y=4to9)) • 缓冲操作跳跃功能
事件链接(ELC)功能	Available*2
噪音过滤功能	Available
通道输出之间的逻辑运算	Available
同步计数器清除计数器设置输入捕捉	Available

注1.GTETRn通过POEG模块连接到GPT。因此，要使用GPT功能，通过清除MSTPCRD.MSTPDn（n=11到14）位。
注2：见第21.6节。由ELC链接的操作。

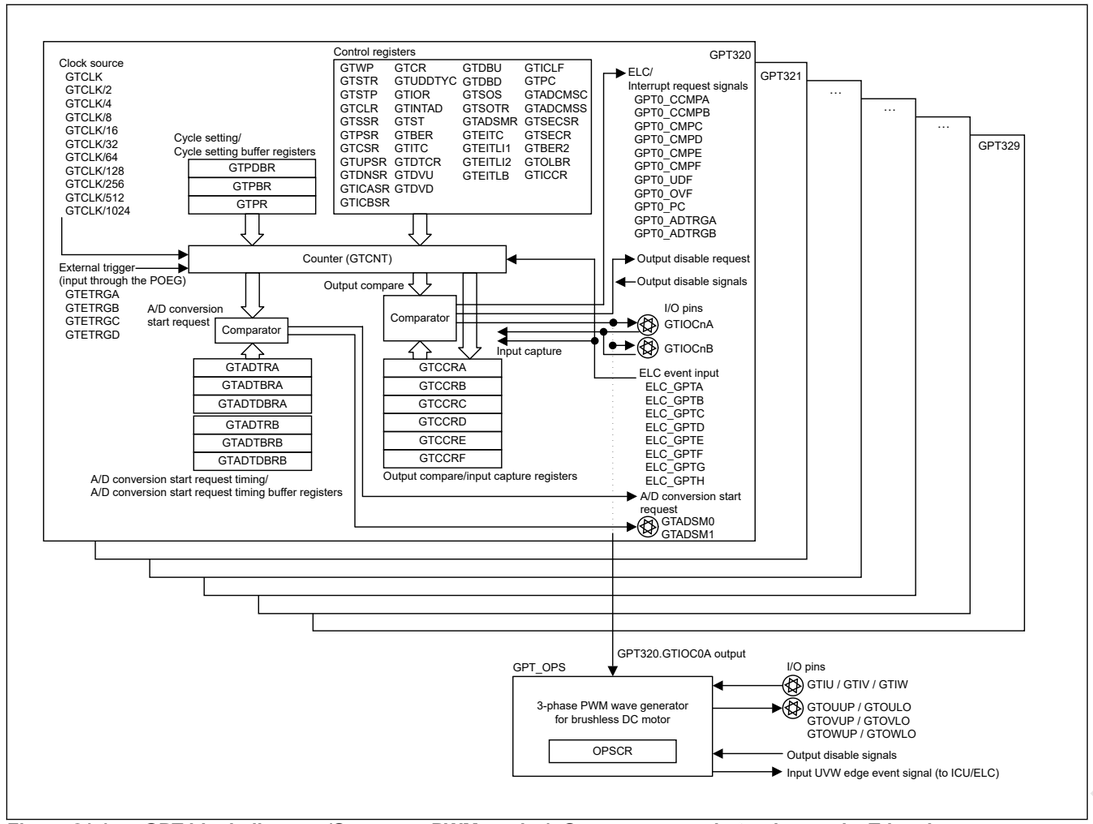


Figure 21.1 GPT block diagram (Saw-wave PWM mode 1, Saw-wave one-shot pulse mode, Triangle-wave PWM mode1,2,3)

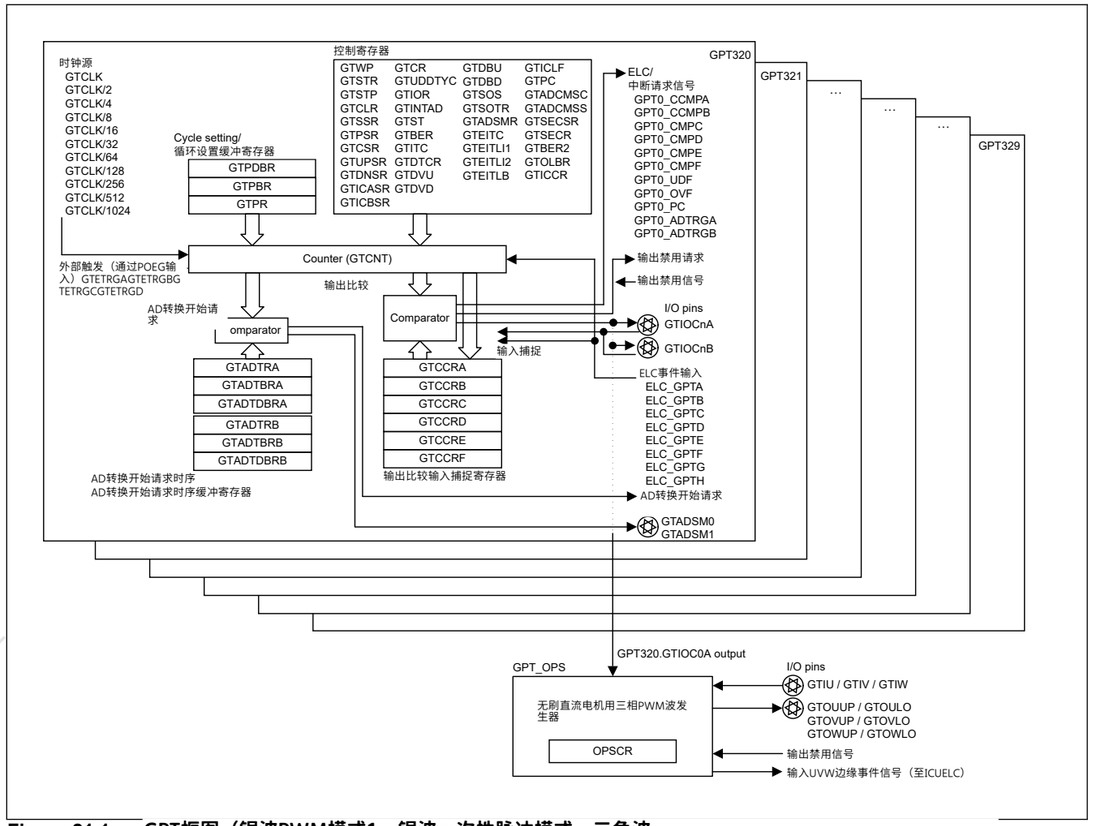


Figure 21.1 GPT框图（锯波PWM模式1、锯波一次性脉冲模式、三角波PWM mode1,2,3)

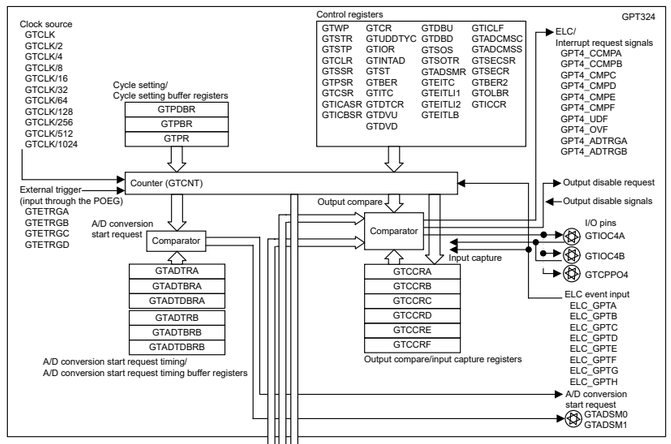


Figure 21.2 GPT block diagram (Saw-wave PWM mode 1, 2, Saw-wave one-shot pulse mode, Triangle-wave PWM mode1,2,3, Complementary PWM mode 1, 2, 3, 4)

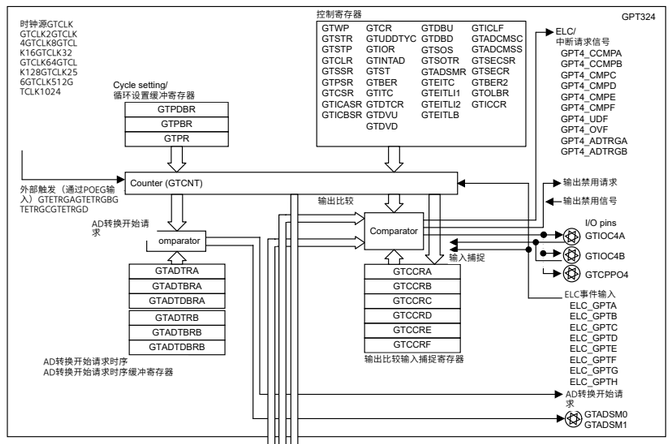


Figure 21.2 GPT框图（锯波PWM模式1、2、锯波一次性脉冲模式、三角波PWM模式1 2 3，互补PWM模式1 2 3 4）

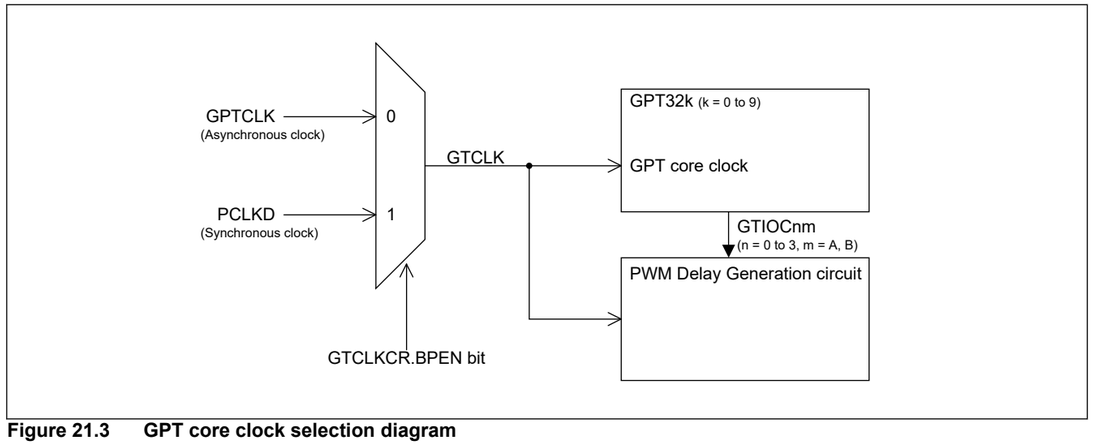


Figure 21.3 GPT core clock selection diagram

In this specification, three consecutive channels to configure complementary PWM mode is defined as complementary PWM mode channel group. The lowest position channel of complementary PWM mode channel group is defined as master channel. The second channel is defined as slave channel 1. The highest position channel is defined as slave channel 2.

Figure 21.4 shows an example using multiple GPTs.

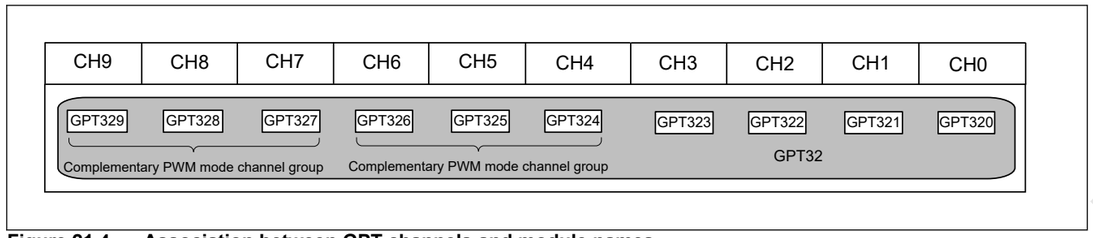


Figure 21.4 Association between GPT channels and module names

Table 21.3 lists the I/O pins.

Table 21.3 GPT I/O pins

Channel	Pin name	I/O	Function
Common	GTETRGx	Input	External trigger input pin x (input through the POEG)
	GTADSM0	Output	A/D conversion start request monitor 0 output pin
	GTADSM1	Output	A/D conversion start request monitor 1 output pin
GPT32n	GTIOCnA	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOCnB	I/O	GTCCRB register input capture input/output compare output/PWM output pin
	GTCPPOk	Output	Toggle output synchronized with PWM period
GPT_OPS	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U-phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U-phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V-phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V-phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W-phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W-phase)

Note: x: A to D

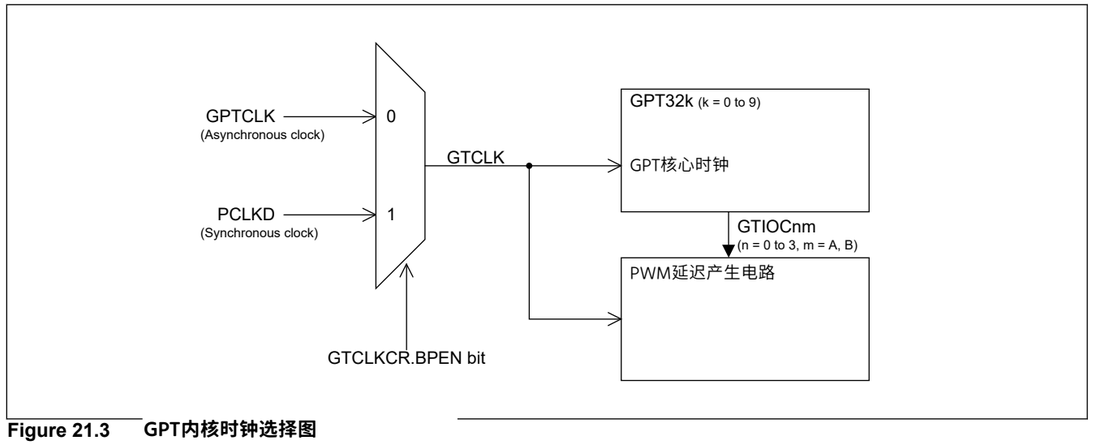


Figure 21.3 GPT内核时钟选择图

在本规范中，配置互补PWM模式的三个连续通道被定义为互补PWM模式通道组。互补PWM模式通道组的最低位置通道定义为主通道。第二个通道定义为从通道1。最高位置通道定义为从通道2。

图21.4显示了一个使用多个GPT的示例。

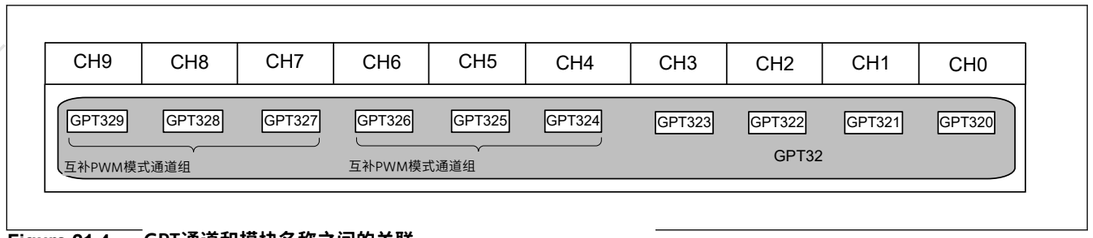


Figure 21.4 GPT通道和模块名称之间的关联

表21.3列出了IO引脚。

Table 21.3 GPT I/O pins

Channel	引脚名称	I/O	Function
Common	GTETRGx	Input	外部触发输入引脚x（通过POEG输入）
	GTADSM0	Output	AD转换开始请求监视器0输出引脚
	GTADSM1	Output	AD转换开始请求监视器1输出引脚
GPT32n	GTIOCnA	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOCnB	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTCPPOk	Output	与PWM周期同步的切换输出
GPT_OPS	GTIU	Input	霍尔传感器输入引脚U
	GTIV	Input	霍尔传感器输入引脚V
	GTIW	Input	霍尔传感器输入引脚W
	GTOUUP	Output	用于BLDC电机控制的3相PWM输出（正U相）
	GTOULO	Output	用于BLDC电机控制的3相PWM输出（负U相）
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出（正V相）
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出（负V相）
	GTOWUP	Output	用于BLDC电机控制的3相PWM输出（正W相）
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出（负W相）

Note: x: A to D

n: 0 to 9
k: 0 to 4, 7

21.2 Register Descriptions

21.2.1 GTWP : General PWM Timer Write-Protection Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	CMNWP	CLRWP	STPWP	STRWP	WP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WP	Register Write Disable 0: Write to the register enabled 1: Write to the register disabled	R/W
1	STRWP	GTSTR.CSTRT Bit Write Disable 0: Write to the bit is enabled 1: Write to the bit is disabled	R/W
2	STPWP	GTSTP.CSTOP Bit Write Disable 0: Write to the bit is enabled 1: Write to the bit is disabled	R/W
3	CLRWP	GTCLR.CCLR Bit Write Disable 0: Write to the bit is enabled 1: Write to the bit is disabled	R/W
4	CMNWP	Common Register Write Disabled 0: Write to the register is enabled 1: Write to the register is disabled	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
15:8	PRKEY[7:0]	GTWP Key Code When 0xA5 is written to these bits, writing to the WP, STRWP, STPWP, CLRWP, and CMNWP bits are permitted. These bits are read as 0.	W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

GTWP enables or disables writing to registers to prevent accidental modification. Protection by the GTWP register is only for the writes by the CPU. GTWP does not protect registers from updates that occur in association with CPU writes.

WP bit (Register Write Disable)

The following is a list of write enabled or disabled registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU, GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR, GTADSMR, GTEITC, GTEITLI1, GTEITLI2, GTEITLB, GTICLF, GTPC, GTADCMSC, GTADCMSS, GTBER2, GTOLBR, GTICCR.

STRWP bit (GTSTR.CSTRT Bit Write Disable)

The STRWP bit enables or disables starting the updating of counter values by writing to the CSTRTn bit (n = 0 to 9) corresponding to a channel number in the GTSTR register.

n: 0 to 9
k: 0 to 4, 7

21.2 注册说明

21.2.1 GTWP:通用PWM定时器写保护寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	CMNWP	CLRWP	STPWP	STRWP	WP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WP	寄存器写禁用 0：允许写入寄存器1：禁止写入寄存器	R/W
1	STRWP	GTSTR.CSTRT位写入禁止 0：允许写入位1：禁止写入位	R/W
2	STPWP	GTSTP.CSTOP位写禁止 0：允许写入位1：禁止写入位	R/W
3	CLRWP	GTCLR.CCLR位写入禁止 0：允许写入位1：禁止写入位	R/W
4	CMNWP	公共寄存器写入禁用 0：允许写入寄存器1：禁止写入寄存器	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
15:8	PRKEY[7:0]	GTWP密钥代码 当0xA5写入这些位时，写入WP、STRWP、STPWP、CLRWP和允许CMNWP位。这些位读为0。	W
31:16	—	这些位被读取为0。写入值应为0。	R/W

GTWP启用或禁用写入寄存器以防止意外修改。GTWP寄存器的保护只针对CPU的写操作。GTWP不保护寄存器免受与CPU写入相关的更新。

WP位（寄存器写禁止）

以下是写启用或禁用寄存器的列表：

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU, GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR, GTADSMR, GTEITC, GTEITLI1, GTEITLI2, GTEITLB, GTICLF, GTPC, GTADCMSC, GTADCMSS, GTBER2, GTOLBR, GTICCR.

STRWP位（GTSTR.CSTRT位写入禁用）

STRWP位通过写入与GTSTR寄存器中的通道号相对应的CSTRTn位（n=0到9）来启用或禁用开始更新计数器值。

The bit position of each CSTRTn bit in the GTSTR register is allocated to the channel with the corresponding number, and writing to the GTSTR register for any channel results in writing to the registers of all channels. The STRWP bit for each channel does not control writing but only controls updating of the CSTRT bit for the corresponding channel when simultaneously writing to all channels.

Therefore, when writing to the CSTRT bits of a channel for which the setting of the STRWP bit is 1(disabling writing), the CSTRT bit for the given channel is not updated, but the CSTRT bits corresponding to channel for which the setting of the STRWP bit is 0 (enabling writing) are updated. For example, when the setting of the GPT320.GTWP.STRWP bit is 0 (enabling writing), writing 1 to the GPT321.GTSTR.CSTRT0 bit when its current setting is 0 causes the value to be updated, and the GPT320.GTCNT counter starts to run. When the setting of the GPT320.GTWP.STRWP bit is 1 (disabling writing), writing 1 to the GPT321.GTSTR.CSTRT0 bit when its current setting is 0 leaves the bit with the value 0, and the GPT320.GTCNT counter does not run.

If you want to protect all bits in the GTSTR register from being updated, set the STRWP bits of all channels to 1.

STPWP bit (GTSTP.CSTOP Bit Write Disable)

The STPWP bit enables or disables starting the updating of counter values by writing to the CSTOPn bit (n = 0 to 9) corresponding to a channel number in the GTSTP register.

The bit position of each CSTOPn bit in the GTSTP registers is allocated to the channel with the corresponding number, and the writing to the GTSTP register for any channel results in writing to the registers of all channels. The STPWP bit for each channel does not control writing but only controls updating of the CSTOP bit for the corresponding channel when simultaneously writing to all channels.

Therefore, when writing to the CSTOP bits of a channel for which the setting of the STPWP bit is 1(disabling writing), the CSTOP bit for the given channel is not updated, but the CSTOP bits corresponding to channel for which the setting of the STPWP bit is 0 (enabling writing) are updated. For example, when the setting of the GPT320.GTWP.STPWP bit is 0 (enabling writing), writing 1 to the GPT321.GTSTP.CSTOP0 bit when its current setting is 0 causes the value to be updated, and the GPT320.GTCNT counter is stopped. When the setting of the GPT320.GTWP.STPWP bit is 1 (disabling writing), writing 1 to the GPT321.GTSTP.CSTOP0 bit when its current setting is 0 leaves the bit with the value 0, and the GPT320.GTCNT counter is not stopped.

If you want to protect all bits in the GTSTP register from being updated, set the STPWP bits of all channels to 1.

CLRWP bit (GTCLR.CCLR Bit Write Disable)

CLRWP bit enables or disables starting the updating of counter values by writing to the CCLRn bit (n = 0 to 9) corresponding to a channel number in the GTCLR register.

The bit position of each CCLRn bit in the GTCLR registers is allocated to the channel with the corresponding number, and the writing to the GTCLR register for any channel results in writing to the registers of all channels. The CLRWP bit for each channel does not control writing but only controls updating of the CCLR bit for the corresponding channel when simultaneously writing to all channels.

Therefore, when writing to the CCLR bits of a channel for which the setting of the CLRWP bit is 1(disabling writing), the CCLR bit for the given channel is not updated, but the CCLR bits corresponding to channel for which the setting of the CLRWP bit is 0 (enabling writing) are updated. For example, when the setting of the GPT320.GTWP.CLRWP bit is 0 (enabling writing), writing 1 to the GPT321.GTCLR.CCLR0 bit when its current setting is 0 causes the value to be updated, and the GPT320.GTCNT counter is cleared. When the setting of the GPT320.GTWP.CLRWP bit is 1 (disabling writing), writing 1 to the GPT321.GTCLR.CCLR0 bit when its current setting is 0 leaves the bit with the value 0, and the GPT320.GTCNT counter is not cleared.

If you want to protect all bits in the GTCLR register from being updated, set the CLRWP bits of all channels to 1.

CMNWP bit (Common Register Write Disabled)

CMNWP bit enables or disables starting the updating of counter values by writing to the SECSELn bit (n = 0 to 9) corresponding to a channel number in the GTSECSR register or to the GTSECR register.

The bit position of each SECSEL bit in the GTSECSR registers is allocated to the channel with the corresponding number, and the writing to the GTSECSR register for any channel results in writing to the registers of all channels. Writing to the GTSECR register of any channel leads to writing to the registers of all channels. The CMNWP bit for each channel does not control writing but only controls updating of the SECSEL bit and the GTSECR register value for the corresponding channel when simultaneously writing to all channels.

GTSTR寄存器中每个CSTRTn位的位位置分配给对应编号的通道，对任何通道写入GTSTR寄存器都会导致写入所有通道的寄存器。每个通道的STRWP位不控制写入，而仅在同时写入所有通道时控制相应通道的CSTRT位的更新。

因此，当写入STRWP位设置为1（禁止写入）的通道的CSTRT位时，
给定通道的CSTRT位不会更新，但对应于其设置的通道的CSTRT位
STRWP位为0（允许写入）被更新。例如，当GPT320.GTWP.STRWP位的设置为0（允许写入）时，当GPT321.GTSTR.CSTRT0位的当前设置为0时写入1会导致值被更新，并且GPT320.GTCNT计数器开始运行。当GPT320.GTWP.STRWP位设置为1时（禁止写入），当前设置为0时向GPT321.GTSTR.CSTRT0位写入1使该位保留值为0，并且GPT320.GTCNT计数器不跑。

如果要保护GTSTR寄存器中的所有位不被更新，请将所有通道的STRWP位设置为1。

STPWP位（GTSTP.CSTOP位写入禁用）

STPWP位通过写入与GTSTP寄存器中的通道号对应的CSTOPn位（n=0到9）来启用或禁用开始更新计数器值。

GTSTP寄存器中每个CSTOPn位的位位置分配给对应编号的通道，对任何通道写入GTSTP寄存器都会导致写入所有通道的寄存器。每个通道的STPWP位不控制写入，而仅控制同时写入所有通道时相应通道的CSTOP位的更新。

因此，当写入STPWP位设置为1的通道的CSTOP位（禁止写入）时，给定通道的CSTOP位不会更新，但对应于其设置的通道的CSTOP位
STPWP位为0（允许写入）被更新。例如，当GPT320.GTWP.STPWP位设置为0（允许写入）时，当GPT321.GTSTP.CSTOP0位的当前设置为0时写入1会导致值被更新，并且GPT320.GTCNT计数器停止。当GPT320.GTWP.STPWP位设置为1时（禁止写入），当前设置为0时向GPT321.GTSTP.CSTOP0位写入1使该位保留值为0，并且GPT320.GTCNT计数器不停了下来。

如果要保护GTSTP寄存器中的所有位不被更新，请将所有通道的STPWP位设置为1。

CLRWP位（GTCLR.CCLR位写入禁止）

CLRWP位通过写入与GTCLR寄存器中的通道号对应的CCLRn位（n=0到9）来启用或禁用开始更新计数器值。

GTCLR寄存器中每个CCLRn位的位位置分配给对应编号的通道，对任何通道写入GTCLR寄存器都会导致写入所有通道的寄存器。每个通道的CLRWP位不控制写入，而仅在同时写入所有通道时控制相应通道的CCLR位的更新。

因此，当写入CLRWP位设置为1（禁止写入）的通道的CCLR位时，
给定通道的CCLR位不会更新，但对应于其设置的通道的CCLR位
CLRWP位为0（允许写入）被更新。例如，当GPT320.GTWP.CLRWP位设置为0（允许写入）时，当GPT321.GTCLR.CCLR0位的当前设置为0时写入1会导致值被更新，并且GPT320.GTCNT计数器被清除。当GPT320.GTWP.CLRWP位设置为1时（禁止写入），当前设置为0时向GPT321.GTCLR.CCLR0位写入1使该位保留值为0，并且GPT320.GTCNT计数器不清除。

如果要保护GTCLR寄存器中的所有位不被更新，请将所有通道的CLRWP位设置为1。

CMNWP位（公共寄存器写入禁用）

CMNWP位通过写入与GTSECSR寄存器中的通道号或GTSECR寄存器中对应的SECSELn位（n=0至9）来启用或禁用开始更新计数器值。

GTSECSR寄存器中每个SECSEL位的位位置分配给对应编号的通道，对任何通道写入GTSECSR寄存器都会导致写入所有通道的寄存器。写入任何通道的GTSECR寄存器会导致写入所有通道的寄存器。每个通道的CMNWP位不控制写入，而仅在同时写入所有通道时控制相应通道的SECSEL位和GTSECR寄存器值的更新。

Therefore, when writing to the SECSEL bit and the GTSECR register value of a channel for which the setting of the CMNWP bit is 1(disabling writing), the SECSEL bit and the GTSECR register value for the given channel is not updated, but the SECSEL bit and the GTSECR register value corresponding to channel for which the setting of the CMNWP bit is 0 (enabling writing) are updated.

For example, when the setting of the GPT320.GTWP.CMNWP bit is 0 (enabling writing), writing to the GPT321.GTSECSR.SECSEL0 bit causes the value of the GPT320.GTSECSR.SECSEL0 bit to be updated. In the same way, writing to the GPT321.GTSECR register updates the value of the GPT320.GTSECR register. When the setting of the GPT320.GTWP.CMNWP bit is 1 (disabling writing), writing to the GPT321.GTSECSR.SECSEL0 bit does not cause the value of the GPT320.GTSECSR.SECSEL0 bit to be updated. In the same way, writing to the GPT321.GTSECR register does not update the value of the GPT320.GTSECR register.

If you want to protect all bits in the GTSECSR and GTSECR registers from being updated, set the CMNWP bits of all channels to 1.

PRKEY[7:0] bit (GTWP Key Code)

This bit controls whether the WP, STRWP, STPWP, CLRWP, and CMNWP bits can be overwritten.

21.2.2 GTSTR : General PWM Timer Software Start Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x04

Bit position:	31																												0
Bit field:	CSTRT31 to CSTRT0																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CSTRT0 to CSTRT31*1	Channel n GTCNT Count Start (n is the same as the bit position value) 0: GTCNT counter is not started 1: GTCNT counter is started	R/W

Note 1. The bits that can be used vary depending on the product. The n in CSTRTn is the same as the GPT channel number. For this product, n is 0 to 9.

The GTSTR starts the GTCNT counter operation for each channel n, where n = 0 to 9.

The GTSTR bit number represents the channel number. The GTSTR register of each channel is shared by all of the channels. The GTCNT counter starts for the channel associated with the GTSTR bit number where 1 is written. Writing 0 has no effect on the status of GTCNT counter and the value of GTSTR register.

In complementary PWM mode, writing to the CSTRTn bit of master channel is only valid. The bit on slave channels reflects the bit value of master channel.

For the association between module names and channel numbers, see Figure 21.4.

CSTRTn bits (Channel n GTCNT Count Start (n = 0 to 9))

The CSTRTn bits start channel n of the GTCNT counter operation. Writing to the GTSTR.CSTRTn bit (n = 0 to 9) has no effect unless the GTSSR.CSTRT bit is set to 1.

The read data shows the counter status of each channel (GTCR.CST bit). A value of 0 means the counter is stopped and 1 means the counter is running.

因此，当写入通道的SECSEL位和GTSECR寄存器值时，
CMNWP位为1（禁止写入），给定通道的SECSEL位和GTSECR寄存器值不更新，但与CMNWP位设置为0的通道对应的SECSEL位和GTSECR寄存器值（允许写入）)已更新。

例如，当GPT320.GTWP.CMNWP位设置为0（允许写入）时，写入GPT321.GTSECSR.SECSEL0位导致GPT320.GTSECSR.SECSEL0位的值被更新。同样，写入GPT321.GTSECR寄存器会更新GPT320.GTSECR寄存器的值。当GPT320.GTWP.CMNWP位设置为1（禁止写入）时，写入GPT321.GTSECSR.SECSEL0位不会导致GPT320.GTSECSR.SECSEL0位的值更新。同样，写入GPT321.GTSECR寄存器不会更新GPT320.GTSECR寄存器的值。

如果要保护GTSECSR和GTSECR寄存器中的所有位不被更新，请将所有通道的CMNWP位设置为1。

PRKEY[7:0]位（GTWP密钥代码）

该位控制是否可以覆盖WP、STRWP、STPWP、CLRWP和CMNWP位。

21.2.2 GTSTR:通用PWM定时器软件启动寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x04

Bit position:	31																												0
Bit field:	CSTRT31 to CSTRT0																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CSTRT0 to CSTRT31*1	ChannelnGTCNTCountStart（n与位位置值相同） 0：GTCNT计数器不启动1：GTC NT计数器启动	R/W

注1.可使用的钻头因产品而异。CSTRTn中的n与GPT通道号相同。对于本产品，n为0到9。

GTSTR启动每个通道n的GTCNT计数器操作，其中n=0到9。

GTSTR位号代表通道号。每个通道的GTSTR寄存器由所有通道共享。GTCNT计数器针对与写入1的GTSTR位号关联的通道启动。写0对GTCNT计数器的状态和GTSTR寄存器的值没有影响。

在互补PWM模式下，写入主通道的CSTRTn位仅有效。从通道上的位反映主通道的位值。

模块名称与通道号的对应关系见图21.4。

CSTRTn位（通道nGTCNT计数开始（n=0到9））

CSTRTn位启动GTCNT计数器操作的通道n。除非GTSSR.CSTRT位设置为1，否则写入GTSTR.CSTRTn位（n=0到9）无效。

读取的数据显示每个通道的计数器状态（GTCR.CST位）。0表示计数器停止，1表示计数器正在运行。

21.2.3 GTSTP : General PWM Timer Software Stop Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x08

Bit position:	31																												0
Bit field:	CSTOP31 to CSTOP0																												
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	CSTOP0 to CSTOP31*1	Channel n GTCNT Count Stop (n is the same as the bit position value) 0: GTCNT counter is not stopped 1: GTCNT counter stopped	R/W

Note 1. The bits that can be used vary depending on the product. The n in CSTOPn is the same as the GPT channel number. For this product, n is 0 to 9.

The GTSTP stops the GTCNT counter operation for each channel n, where n = 0 to 9.

The GTSTP bit number represents the channel number. The GTSTP register of each channel is shared by all the channels. The GTCNT counter stops for the channel associated with the GTSTP bit number where 1 is written. Writing 0 has no effect on the status of the GTCNT counter and the value of GTSTP register.

In complementary PWM mode, writing to the CSTOPn bit of master channel is only valid. The bit on slave channels reflects the bit value of master channel.

For the association between module names and channel numbers, see Figure 21.4.

CSTOPn bits (Channel n GTCNT Count Stop (n = 0 to 9))

The CSTOPn bits stop channel n of the GTCNT counter operation. Writing to the GTSTP.CSTOPn bit (n = 0 to 9) has no effect unless the GTPSR.CSTOP bit is set to 1. The read data shows the counter status of each channel (invert of GTCR.CST bit). A value of 0 means the counter is running and 1 means the counter is stopped.

21.2.4 GTCLR : General PWM Timer Software Clear Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x0C

Bit position:	31																												0
Bit field:	CCLR31 to CCLR0																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CCLR0 to CCLR31*1	Channel n GTCNT Count Clear (n : the same as bit position value) 0: GTCNT counter is not cleared 1: GTCNT counter is cleared	W

Note 1. The bits that can be used vary depending on the product. The n of CCLRn is the same as the GPT channel number. For this product, n is 0 to 9.

The GTCLR is a write-only register that clears the GTCNT counter operation for each channel n, where n = 0 to 9.

The GTCLR bit number represents the channel number. The GTCLR register of each channel is shared by all the channels. The GTCNT counter is cleared for the channel associated with the GTCLR bit number where 1 is written. Writing 0 has no effect on the status of GTCNT counter.

In complementary PWM mode, writing to the CCLRn bit of master channel is only valid. The bit on slave channels reflects the bit value of master channel.

For the association between module names and channel numbers, see Figure 21.4.

21.2.3 GTSTP:通用PWM定时器软件停止寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x08

Bit position:	31																												0
Bit field:	CSTOP31 to CSTOP0																												
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	CSTOP0 to CSTOP31*1	通道nGTCNT计数停止（n与位位置值相同） 0：GTCNT计数器不停止1：GTCN T计数器停止	R/W

注1.可使用的钻头因产品而异。CSTOPn中的n与GPT通道号相同。对于本产品，n为0到9。

GTSTP停止每个通道n的GTCNT计数器操作，其中n=0到9。

GTSTP位号代表通道号。每个通道的GTSTP寄存器由所有通道共享。
对于与写入1的GTSTP位号相关的通道，GTCNT计数器停止。写0对GTCNT计数器的状态和GTSTP寄存器的值没有影响。

在互补PWM模式下，写入主通道的CSTOPn位仅有效。从通道上的位反映主通道的位值。

模块名称与通道号的对应关系见图21.4。

CSTOPn位（通道nGTCNT计数停止（n=0到9））

CSTOPn位停止GTCNT计数器操作的通道n。除非GTPSR.CSTOP位设置为1，否则写入GTSTP.CSTOPn位（n=0至9）无效。读取的数据显示每个通道的计数器状态（反转GTCR.CST位）。值0表示计数器正在运行，1表示计数器停止。

21.2.4 GTCLR:通用PWM定时器软件清零寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x0C

Bit position:	31																												0
Bit field:	CCLR31 to CCLR0																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CCLR0 to CCLR31*1	ChannelnGTCNTCountClear（n：与位位置值相同） 0：GTCNT计数器不清零1：GTCN T计数器清零	W

注1.可使用的钻头因产品而异。CCLRn的n与GPT通道号相同。对于本产品，n为0到9。

GTCLR是一个只写寄存器，用于清除每个通道n的GTCNT计数器操作，其中n=0到9。

GTCLR位号代表通道号。每个通道的GTCLR寄存器由所有通道共享。与写入1的GTCLR位号关联的通道的GTCNT计数器清零。写0对GTCNT计数器的状态没有影响。

在互补PWM模式下，只对主通道的CCLRn位进行写有效。从通道上的位反映主通道的位值。

模块名称与通道号的对应关系见图21.4。

CCLRn bits (Channel n GTCNT Count Clear (n = 0 to 9))

When the counting direction flag is set for decrement (GTST.TUCF flag = 0) with saw-wave mode selected in the GTCR.MD[2:0] bits, the value of the GTCNT counter becomes that of the corresponding GTPR register in response to writing 1 to the CCLRn bit. The value of the counter becomes 0x0000 0000 with other settings. These bits are read as 0.

21.2.5 GTSSR : General PWM Timer Start Source Select Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTRT	—	—	—	—	—	—	—	SSELCH	SSELCG	SSELCF	SSELCE	SSELCD	SSELCC	SSELCB	SSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	SSGTRGDF	SSGTRGDR	SSGTRGCF	SSGTRGCR	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSGTRGAR	GTETRGA Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGA input 1: Counter start enabled on the rising edge of GTETRGA input	R/W*1
1	SSGTRGAF	GTETRGA Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGA input 1: Counter start enabled on the falling edge of GTETRGA input	R/W*1
2	SSGTRGBR	GTETRGB Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGB input 1: Counter start enabled on the rising edge of GTETRGB input	R/W*1
3	SSGTRGBF	GTETRGB Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGB input 1: Counter start enabled on the falling edge of GTETRGB input	R/W*1
4	SSGTRGCR	GTETRGC Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGC input 1: Counter start enabled on the rising edge of GTETRGC input	R/W*1
5	SSGTRGCF	GTETRGC Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGC input 1: Counter start enabled on the falling edge of GTETRGC input	R/W*1
6	SSGTRGDR	GTETRGD Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGD input 1: Counter start enabled on the rising edge of GTETRGD input	R/W*1
7	SSGTRGDF	GTETRGD Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGD input 1: Counter start enabled on the falling edge of GTETRGD input	R/W*1
8	SSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter start enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	SSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter start enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W

CCLRn位（通道nGTCNT计数清除（n=0至9））

当计数方向标志设置为递减（GTST.TUCF标志=0）且在GTCR.MD[2:0]位，GTCNT计数器的值变为相应GTPR寄存器的值以响应向CCLRn位写入1。使用其他设置，计数器的值变为0x00000000。这些位读为0。

21.2.5 GTSSR：通用PWM定时器启动源选择寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTRT	—	—	—	—	—	—	—	SSELCH	SSELCG	SSELCF	SSELCE	SSELCD	SSELCC	SSELCB	SSELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	SSGTRGDF	SSGTRGDR	SSGTRGCF	SSGTRGCR	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSGTRGAR	GTETRGA引脚上升输入源计数器启动使能 0：在GTETRGA输入的上升沿禁止计数器启动1：在GTETRGA输入的上升沿使能计数器启动	R/W*1
1	SSGTRGAF	GTETRGA引脚下降输入源计数器启动使能 0：在GTETRGA输入的下降沿禁用计数器启动1：在GTETRGA输入的下降沿启用计数器启动	R/W*1
2	SSGTRGBR	GTETRGB引脚上升输入源计数器启动使能 0：在GTETRGB输入的上升沿禁止计数器启动1：在GTETRGB输入的上升沿使能计数器启动	R/W*1
3	SSGTRGBF	GTETRGB引脚下降输入源计数器启动使能 0：在GTETRGB输入的下降沿禁用计数器启动1：在GTETRGB输入的下降沿启用计数器启动	R/W*1
4	SSGTRGCR	GTETRGC引脚上升沿输入源计数器启动使能 0：在GTETRGC输入的上升沿禁止计数器启动1：在GTETRGC输入的上升沿使能计数器启动	R/W*1
5	SSGTRGCF	GTETRGC引脚下降输入源计数器启动使能 0：在GTETRGC输入的下降沿禁止计数器启动1：在GTETRGC输入的下降沿使能计数器启动	R/W*1
6	SSGTRGDR	GTETRGD引脚上升沿输入源计数器启动使能 0：在GTETRGD输入的上升沿禁止计数器启动1：在GTETRGD输入的上升沿使能计数器启动	R/W*1
7	SSGTRGDF	GTETRGD引脚下降输入源计数器启动使能 0：在GTETRGD输入的下降沿禁止计数器启动1：在GTETRGD输入的下降沿使能计数器启动	R/W*1
8	SSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器启动使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器启动 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿启用计数器启动	R/W
9	SSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器启动使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器启动 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿启用计数器启动	R/W

Bit	Symbol	Function	R/W
10	SSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter start enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	SSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter start enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	SSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter start enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	SSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter start enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	SSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter start enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	SSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter start enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	SSELCA	ELC_GPTA Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTA input 1: Counter start enabled at the ELC_GPTA input	R/W*1
17	SSELCB	ELC_GPTB Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTB input 1: Counter start enabled at the ELC_GPTB input	R/W*1
18	SSELCC	ELC_GPTC Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTC input 1: Counter start enabled at the ELC_GPTC input	R/W*1
19	SSELCD	ELC_GPTD Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTD input 1: Counter start enabled at the ELC_GPTD input	R/W*1
20	SSELCE	ELC_GPTE Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTE input 1: Counter start enabled at the ELC_GPTE input	R/W*1
21	SSELCF	ELC_GPTF Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTF input 1: Counter start enabled at the ELC_GPTF input	R/W*1
22	SSELCG	ELC_GPTG Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTG input 1: Counter start enabled at the ELC_GPTG input	R/W*1
23	SSELCH	ELC_GPTH Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTH input 1: Counter start enabled at the ELC_GPTH input	R/W*1
30:24	—	These bits are read as 0. The write value should be 0.	R/W
31	CSTRT	Software Source Counter Start Enable 0: Counter start disabled by the GTSTR register 1: Counter start enabled by the GTSTR register	R/W*1

Bit	Symbol	Function	R/W
10	SSCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源计数器启动使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器启动 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿启用计数器启动	R/W
11	SSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器启动使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器启动 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿启用计数器启动	R/W
12	SSCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器启动使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止计数器启动 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿启用计数器启动	R/W
13	SSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器启动使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器启动 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿启用计数器启动	R/W
14	SSCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源计数器启动使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器启动 1：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿启用计数器启动	R/W
15	SSCBFAH	GTIOCnA值高电平期间的GTIOCnB引脚下降输入源计数器启动使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器启动 1：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿启用计数器启动	R/W
16	SSELCA	ELC_GPTA事件源计数器启动启用 0：在ELC_GPTA输入处禁用计数器启动1：在ELC_GPTA输入处启用计数器启动	R/W*1
17	SSELCB	ELC_GPTB事件源计数器启动启用 0：在ELC_GPTB输入处禁用计数器启动1：在ELC_GPTB输入处启用计数器启动	R/W*1
18	SSELCC	ELC_GPTC事件源计数器启动启用 0：在ELC_GPTC输入处禁用计数器启动1：在ELC_GPTC输入处启用计数器启动	R/W*1
19	SSELCD	ELC_GPTD事件源计数器启动启用 0：在ELC_GPTD输入处禁用计数器启动1：在ELC_GPTD输入处启用计数器启动	R/W*1
20	SSELCE	ELC_GPTE事件源计数器启动启用 0：在ELC_GPTE输入处禁用计数器启动1：在ELC_GPTE输入处启用计数器启动	R/W*1
21	SSELCF	ELC_GPTF事件源计数器启动启用 0：在ELC_GPTF输入处禁用计数器启动1：在ELC_GPTF输入处启用计数器启动	R/W*1
22	SSELCG	ELC_GPTG事件源计数器启动启用 0：在ELC_GPTG输入处禁用计数器启动1：在ELC_GPTG输入处启用计数器启动	R/W*1
23	SSELCH	ELC_GPTH事件源计数器启动启用 0：在ELC_GPTH输入处禁用计数器启动1：在ELC_GPTH输入处启用计数器启动	R/W*1
30:24	—	这些位被读取为0。写入值应为0。	R/W
31	CSTRT	软件源计数器启动使能 0：由GTSTR寄存器禁止计数器启动1：由GTSTR寄存器使能计数器启动	R/W*1

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.

The GTSSR sets the source to start the GTCNT counter.

Input from GTETRGn (n = A to D) pins are input to the GPT via the POEG. Set the polarity of these signals with the POEG.

SSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Start Enable)

The SSGTRGAR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGA pin input.

SSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Start Enable)

The SSGTRGAF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGA pin input.

SSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Start Enable)

The SSGTRGBR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGB pin input.

SSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Start Enable)

The SSGTRGBF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGB pin input.

SSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Start Enable)

The SSGTRGCR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGC pin input.

SSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Start Enable)

The SSGTRGCF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGC pin input.

SSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Start Enable)

The SSGTRGDR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGD pin input.

SSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Start Enable)

The SSGTRGDF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGD pin input.

SSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Start Enable)

The SSCARBL bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

In complementary PWM mode, this setting is invalid.

SSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Start Enable)

The SSCARBH bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

In complementary PWM mode, this setting is invalid.

SSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Start Enable)

The SSCAFBL bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

In complementary PWM mode, this setting is invalid.

SSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Start Enable)

The SSCAFBH bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

In complementary PWM mode, this setting is invalid.

SSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Start Enable)

The SSCBRAL bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

In complementary PWM mode, this setting is invalid.

注1.在互补PWM模式下，无论写入主通道从通道1从通道2的哪个寄存器，都会同时写入三个通道。

GTSSR设置启动GTCNT计数器的源。

GTETRn（n=A到D）引脚的输入通过POEG输入到GPT。设置这些信号的极性POEG.

SSGTRGAR位（GTETRGA引脚上升沿输入源计数器启动使能）

SSGTRGAR位启用或禁用GTCNT计数器在GTETRGA引脚输入的上升沿启动。

SSGTRGAF位（GTETRGA引脚下降输入源计数器启动使能）

SSGTRGAF位启用或禁用GTCNT计数器在GTETRGA引脚输入的下降沿启动。

SSGTRGBR位（GTETRGB引脚上升沿输入源计数器启动使能）

SSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器启动。

SSGTRGBF位（GTETRGB引脚下降输入源计数器启动使能）

SSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器启动。

SSGTRGCR位（GTETRGC引脚上升沿输入源计数器启动使能）

SSGTRGCR位启用或禁用GTCNT计数器在GTETRGC引脚输入的上升沿启动。

SSGTRGCF位（GTETRGC引脚下降输入源计数器启动使能）

SSGTRGCF位启用或禁用GTCNT计数器在GTETRGC引脚输入的下降沿启动。

SSGTRGDR位（GTETRGD引脚上升沿输入源计数器启动使能）

SSGTRGDR位启用或禁用GTCNT计数器在GTETRGD引脚输入的上升沿启动。

SSGTRGDF位（GTETRGD引脚下降输入源计数器启动使能）

SSGTRGDF位启用或禁用GTCNT计数器在GTETRGD引脚输入的下降沿启动。

SSCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器启动使能）

SSCARBL位启用或禁用GTCNT计数器在GTIOCnA引脚输入的上升沿启动，当GTIOCnB输入为0。

在互补PWM模式下，此设置无效。

SSCARBH位（GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器启动使能）

SSCARBH位启用或禁用GTCNT计数器在GTIOCnA引脚输入的上升沿启动，当GTIOCnB输入为1。

在互补PWM模式下，此设置无效。

SSCAFBL位（在GTIOCnB值低电平源计数器启动使能期间GTIOCnA引脚下降输入）

SSCAFBL位启用或禁用GTCNT计数器在GTIOCnA引脚输入的下降沿启动，当GTIOCnB输入为0。

在互补PWM模式下，此设置无效。

SSCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源计数器启动使能）

SSCAFBH位启用或禁用GTCNT计数器在GTIOCnA引脚输入的下降沿启动，当GTIOCnB输入为1。

在互补PWM模式下，此设置无效。

SSCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器启动使能）

SSCBRAL位启用或禁用GTCNT计数器在GTIOCnB引脚输入的上升沿启动，当GTIOCnA输入为0。

在互补PWM模式下，此设置无效。

SSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Start Enable)

The SSCBRAH bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

In complementary PWM mode, this setting is invalid.

SSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Start Enable)

The SSCBFAL bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

In complementary PWM mode, this setting is invalid.

SSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Start Enable)

The SSCBFAH bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

In complementary PWM mode, this setting is invalid.

SSELCm bit (ELC_GPTm Event Source Counter Start Enable) (m = A to H)

The SSELCm bit enables or disables the GTCNT counter start at the ELC_GPTm event input.

CSTRT bit (Software Source Counter Start Enable)

The CSTRT bit enables or disables the GTCNT counter start by GTSTR register.

21.2.6 GTPSR : General PWM Timer Stop Source Select Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTOP	—	—	—	—	—	—	—	PSELCH	PSELCG	PSELCF	PSELCE	PSELCD	PSELCC	PSELCB	PSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PSCBFAH	PSCBFAL	PSCBRAH	PSCBRAL	PSCAFBH	PSCAFBL	PSCARBH	PSCARBL	PSGTRGDF	PSGTRGDR	PSGTRGCF	PSGTRGCR	PSGTRGBF	PSGTRGBR	PSGTRGAF	PSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PSGTRGAR	GTETRGA Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGA input 1: Counter stop enabled on the rising edge of GTETRGA input	R/W*1
1	PSGTRGAF	GTETRGA Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGA input 1: Counter stop enabled on the falling edge of GTETRGA input	R/W*1
2	PSGTRGBR	GTETRGB Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGB input 1: Counter stop enabled on the rising edge of GTETRGB input	R/W*1
3	PSGTRGBF	GTETRGB Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGB input 1: Counter stop enabled on the falling edge of GTETRGB input	R/W*1
4	PSGTRGCR	GTETRGC Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGC input 1: Counter stop enabled on the rising edge of GTETRGC input	R/W*1
5	PSGTRGCF	GTETRGC Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGC input 1: Counter stop enabled on the falling edge of GTETRGC input	R/W*1

SSCBRAH位（GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器启动使能）

SSCBRAH位使能或禁止GTCNT计数器在GTIOCnB引脚输入的上升沿启动，当GTIOCnA输入为1。

在互补PWM模式下，此设置无效。

SSCBFAL位（GTIOCnA值低电平源计数器启动使能期间GTIOCnB引脚下降输入）

SSCBFAL位使能或禁止GTCNT计数器在GTIOCnB引脚输入的下降沿启动，当GTIOCnA输入为0。

在互补PWM模式下，此设置无效。

SSCBFAH位（GTIOCnA值高电平源计数器启动使能期间的GTIOCnB引脚下降输入）

SSCBFAH位启用或禁用GTCNT计数器在GTIOCnB引脚输入的下降沿启动，当GTIOCnA输入为1。

在互补PWM模式下，此设置无效。

SSELCm位（ELC_GPTm事件源计数器启动启用）（m=A到H）

SSELCm位启用或禁用在ELC_GPTm事件输入时启动的GTCNT计数器。

CSTRT位（软件源计数器启动使能）

CSTRT位启用或禁用由GTSTR寄存器启动的GTCNT计数器。

21.2.6 GTPSR：通用PWM定时器停止源选择寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTOP	—	—	—	—	—	—	—	PSELCH	PSELCG	PSELCF	PSELCE	PSELCD	PSELCC	PSELCB	PSELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PSCBFAH	PSCBFAL	PSCBRAH	PSCBRAL	PSCAFBH	PSCAFBL	PSCARBH	PSCARBL	PSGTRGDF	PSGTRGDR	PSGTRGCF	PSGTRGCR	PSGTRGBF	PSGTRGBR	PSGTRGAF	PSGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PSGTRGAR	GTETRGA引脚上升输入源计数器停止使能 0：在GTETRGA输入的上升沿禁止计数器停止1：在GTETRGA输入的上升沿使能计数器停止	R/W*1
1	PSGTRGAF	GTETRGA引脚下降输入源计数器停止使能 0：在GTETRGA输入的下降沿禁止计数器停止1：在GTETRGA输入的下降沿使能计数器停止	R/W*1
2	PSGTRGBR	GTETRGB引脚上升输入源计数器停止使能 0：在GTETRGB输入的上升沿禁止计数器停止1：在GTETRGB输入的上升沿使能计数器停止	R/W*1
3	PSGTRGBF	GTETRGB引脚下降输入源计数器停止使能 0：在GTETRGB输入的下降沿禁用计数器停止1：在GTETRGB输入的下降沿启用计数器停止	R/W*1
4	PSGTRGCR	GTETRGC引脚上升输入源计数器停止使能 0：在GTETRGC输入的上升沿禁止计数器停止1：在GTETRGC输入的上升沿使能计数器停止	R/W*1
5	PSGTRGCF	GTETRGC引脚下降输入源计数器停止使能 0：在GTETRGC输入的下降沿禁止计数器停止1：在GTETRGC输入的下降沿使能计数器停止	R/W*1

Bit	Symbol	Function	R/W
6	PSGTRGDR	GTETRGD Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGD input 1: Counter stop enabled on the rising edge of GTETRGD input	R/W*1
7	PSGTRGDF	GTETRGD Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGD input 1: Counter stop enabled on the falling edge of GTETRGD input	R/W*1
8	PSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter stop enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	PSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter stop enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	PSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter stop enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	PSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter stop enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	PSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter stop enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	PSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter stop enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	PSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter stop enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	PSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter stop enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	PSELCA	ELC_GPTA Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTA input 1: Counter stop enabled at the ELC_GPTA input	R/W*1
17	PSELCB	ELC_GPTB Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTB input 1: Counter stop enabled at the ELC_GPTB input	R/W*1
18	PSELCC	ELC_GPTC Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTC input 1: Counter stop enabled at the ELC_GPTC input	R/W*1
19	PSELCD	ELC_GPTD Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTD input 1: Counter stop enabled at the ELC_GPTD input	R/W*1

Bit	Symbol	Function	R/W
6	PSGTRGDR	GTETRGD引脚上升输入源计数器停止使能 0：在GTETRGD输入的上升沿禁止计数器停止1：在GTETRGD输入的上升沿使能计数器停止	R/W*1
7	PSGTRGDF	GTETRGD引脚下降输入源计数器停止使能 0：在GTETRGD输入的下降沿禁止计数器停止1：在GTETRGD输入的下降沿使能计数器停止	R/W*1
8	PSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器停止使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器停止 1：当GTIOCnB输入为0时，在GTIOCnA输入上升沿使能计数器停止	R/W
9	PSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器停止使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器停止 1：当GTIOCnB输入为1时，在GTIOCnA输入上升沿使能计数器停止	R/W
10	PSCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源计数器停止使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器停止 1：当GTIOCnB输入为0时，在GTIOCnA输入下降沿使能计数器停止	R/W
11	PSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器停止使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器停止 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿使能计数器停止	R/W
12	PSCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器停止使能 0：当GTIOCnA输入为0时，在GTIOCnB输入上升沿禁止计数器停止 1：当GTIOCnA输入为0时，在GTIOCnB输入上升沿使能计数器停止	R/W
13	PSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器停止使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器停止 1：当GTIOCnA输入为1时，在GTIOCnB输入上升沿使能计数器停止	R/W
14	PSCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源计数器停止使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器停止 1：当GTIOCnA输入为0时，在GTIOCnB输入下降沿使能计数器停止	R/W
15	PSCBFAH	GTIOCnA值高电平期间的GTIOCnB引脚下降输入源计数器停止使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器停止 1：当GTIOCnA输入为1时，在GTIOCnB输入下降沿使能计数器停止	R/W
16	PSELCA	ELC_GPTA事件源计数器停止启用 0：在ELC_GPTA输入处禁用计数器停止1：在ELC_GPTA输入处启用计数器停止	R/W*1
17	PSELCB	ELC_GPTB事件源计数器停止启用 0：在ELC_GPTB输入处禁用计数器停止1：在ELC_GPTB输入处启用计数器停止	R/W*1
18	PSELCC	ELC_GPTC事件源计数器停止使能 0：在ELC_GPTC输入处禁用计数器停止1：在ELC_GPTC输入处启用计数器停止	R/W*1
19	PSELCD	ELC_GPTD事件源计数器停止启用 0：在ELC_GPTD输入处禁用计数器停止1：在ELC_GPTD输入处启用计数器停止	R/W*1

Bit	Symbol	Function	R/W
20	PSELCE	ELC_GPTE Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTE input 1: Counter stop enabled at the ELC_GPTE input	R/W*1
21	PSELCF	ELC_GPTF Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTF input 1: Counter stop enabled at the ELC_GPTF input	R/W*1
22	PSELCG	ELC_GPTG Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTG input 1: Counter stop enabled at the ELC_GPTG input	R/W*1
23	PSELCH	ELC_GPTH Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTH input 1: Counter stop enabled at the ELC_GPTH input	R/W*1
30:24	—	These bits are read as 0. The write value should be 0.	R/W
31	CSTOP	Software Source Counter Stop Enable 0: Counter stop disabled by the GTSTP register 1: Counter stop enabled by the GTSTP register	R/W*1

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.

The GTPSR sets the source to stop the GTCNT counter.

Inputs from GTETRGn (n = A to D) pins are input to the GPT via the POEG. Set the polarity of these signals with the POEG.

PSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Stop Enable)

The PSGTRGAR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGA pin input.

PSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Stop Enable)

The PSGTRGAF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGA pin input.

PSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Stop Enable)

PSGTRGBR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGB pin input.

PSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Stop Enable)

The PSGTRGBF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGB pin input.

PSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Stop Enable)

PSGTRGCR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGC pin input.

PSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Stop Enable)

The PSGTRGCF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGC pin input.

PSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Stop Enable)

PSGTRGDR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGD pin input.

PSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Stop Enable)

The PSGTRGDF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGD pin input.

PSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Stop Enable)

The PSCARBL bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

In complementary PWM mode, this setting is invalid.

PSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Stop Enable)

The PSCARBH bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

Bit	Symbol	Function	R/W
20	PSELCE	ELC_GPTE事件源计数器停止启用 0：在ELC_GPTE输入处禁用计数器停止1：在ELC_GPTE输入处启用计数器停止	R/W*1
21	PSELCF	ELC_GPTF事件源计数器停止启用 0：在ELC_GPTF输入处禁用计数器停止1：在ELC_GPTF输入处启用计数器停止	R/W*1
22	PSELCG	ELC_GPTG事件源计数器停止使能 0：在ELC_GPTG输入处禁用计数器停止1：在ELC_GPTG输入处启用计数器停止	R/W*1
23	PSELCH	ELC_GPTH事件源计数器停止启用 0：在ELC_GPTH输入处禁用计数器停止1：在ELC_GPTH输入处启用计数器停止	R/W*1
30:24	—	这些位被读取为0。写入值应为0。	R/W
31	CSTOP	软件源计数器停止使能 0：GTSTP寄存器禁止计数器停止1：GTSTP寄存器使能计数器停止	R/W*1

注1.在互补PWM模式下，无论写入主通道从通道1从通道2的哪个寄存器，都会同时写入三个通道。

GTPSR设置源以停止GTCNT计数器。

来自GTETRn（n=A到D）引脚的输入通过POEG输入到GPT。设置这些信号的极性POEG.

PSGTRGAR位（GTETRGA引脚上升沿输入源计数器停止使能）

PSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSGTRGAF位（GTETRGA引脚下降输入源计数器停止使能）

PSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSGTRGBR位（GTETRGB引脚上升沿输入源计数器停止使能）

PSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSGTRGBF位（GTETRGB引脚下降输入源计数器停止使能）

PSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSGTRGCR位（GTETRGC引脚上升沿输入源计数器停止使能）

PSGTRGCR位使能或禁止GTCNT计数器在GTETRGC引脚输入的上升沿停止。

PSGTRGCF位（GTETRGC引脚下降输入源计数器停止使能）

PSGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSGTRGDR位（GTETRGD引脚上升沿输入源计数器停止使能）

PSGTRGDR位启用或禁用GTCNT计数器在GTETRGD引脚输入的上升沿停止。

PSGTRGDF位（GTETRGD引脚下降输入源计数器停止使能）

PSGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器停止使能）

PSCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器停止，当GTIOCnB输入为0。

在互补PWM模式下，此设置无效。

PSCARBH位（GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器停止使能）

PSCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器停止，当GTIOCnB输入为1。

In complementary PWM mode, this setting is invalid.

PSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Stop Enable)

The PSCAFBL bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

In complementary PWM mode, this setting is invalid.

PSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Stop Enable)

The PSCAFBH bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

In complementary PWM mode, this setting is invalid.

PSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Stop Enable)

The PSCBRAL bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

In complementary PWM mode, this setting is invalid.

PSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Stop Enable)

The PSCBRAH bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

In complementary PWM mode, this setting is invalid.

PSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Stop Enable)

The PSCBFAL bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

In complementary PWM mode, this setting is invalid.

PSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Stop Enable)

The PSCBFAH bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

In complementary PWM mode, this setting is invalid.

PSELCm bit (ELCm Event Source Counter Stop Enable) (m = A to H)

The PSELCm bit enables or disables the GTCNT counter stop at the ELC_GPTm event input.

CSTOP bit (Software Source Counter Stop Enable)

The CSTOP bit enables or disables the GTCNT counter stop by the GTSTP register.

21.2.7 GTCSR : General PWM Timer Clear Source Select Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CCLR	—	—	—	CP1CCE	CSCMSC[2:0]			CSELCH	CSELCG	CSELCF	CSELCE	CSELCD	CSELCC	CSELCB	CSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	CSGTRGDF	CSGTRGDR	CSGTRGCF	CSGTRGCR	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

在互补PWM模式下，此设置无效。

PSCAFBL位（GTIOCnB值低电平源计数器停止使能期间GTIOCnA引脚下降输入）

PSCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCnB输入为0。

在互补PWM模式下，此设置无效。

PSCAFBH位（GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器停止使能）

PSCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCnB输入为1。

在互补PWM模式下，此设置无效。

PSCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器停止使能）

PSCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器停止，当GTIOCnA输入为0。

在互补PWM模式下，此设置无效。

PSCBRAH位（GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器停止使能）

PSCBRAH位使能或禁止GTCNT计数器在GTIOCnB引脚输入的上升沿停止，当GTIOCnA输入为1。

在互补PWM模式下，此设置无效。

PSCBFAL位（GTIOCnA值低源计数器停止使能期间GTIOCnB引脚下降输入）

PSCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCnA输入为0。

在互补PWM模式下，此设置无效。

PSCBFAH位（GTIOCnA值高电平源计数器停止使能期间的GTIOCnB引脚下降输入）

PSCBFAH位使能或禁止GTCNT计数器在GTIOCnB引脚输入的下降沿停止，当GTIOCnA输入为1。

在互补PWM模式下，此设置无效。

PSELCm位（ELCm事件源计数器停止使能）（m=A到H）

PSELCm位启用或禁用GTCNT计数器在ELC_GPTm事件输入处停止。

CSTOP位（软件源计数器停止使能）

CSTOP位通过GTSTP寄存器启用或禁用GTCNT计数器停止。

21.2.7 GTCSR：通用PWM定时器清零源选择寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CCLR	—	—	—	CP1CCE	CSCMSC[2:0]			CSELCH	CSELCG	CSELCF	CSELCE	CSELCD	CSELCC	CSELCB	CSELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	CSGTRGDF	CSGTRGDR	CSGTRGCF	CSGTRGCR	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CSGTRGAR	GTETRGA Pin Rising Input Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTETRGA input 1: Counter clear enabled on the rising edge of GTETRGA input	R/W*1
1	CSGTRGAF	GTETRGA Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGA input 1: Counter clear enabled on the falling edge of GTETRGA input	R/W*1
2	CSGTRGBR	GTETRGB Pin Rising Input Source Counter Clear Enable 0: Disable counter clear on the rising edge of GTETRGB input 1: Enable counter clear on the rising edge of GTETRGB input	R/W*1
3	CSGTRGBF	GTETRGB Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGB input 1: Counter clear enabled on the falling edge of GTETRGB input	R/W*1
4	CSGTRGCR	GTETRGC Pin Rising Input Source Counter Clear Enable 0: Disable counter clear on the rising edge of GTETRGC input 1: Enable counter clear on the rising edge of GTETRGC input	R/W*1
5	CSGTRGCF	GTETRGC Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGC input 1: Counter clear enabled on the falling edge of GTETRGC input	R/W*1
6	CSGTRGDR	GTETRGD Pin Rising Input Source Counter Clear Enable 0: Disable counter clear on the rising edge of GTETRGD input 1: Enable counter clear on the rising edge of GTETRGD input	R/W*1
7	CSGTRGDF	GTETRGD Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGD input 1: Counter clear enabled on the falling edge of GTETRGD input	R/W*1
8	CSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter clear enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	CSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter clear enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	CSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter clear enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	CSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter clear enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	CSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter clear enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	CSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter clear enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	CSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter clear enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W

Bit	Symbol	Function	R/W
0	CSGTRGAR	GTETRGA引脚上升输入源计数器清零使能 0：在GTETRGA输入的上升沿禁止计数器清除1：在GTETRGA输入的上升沿使能计数器清除	R/W*1
1	CSGTRGAF	GTETRGA引脚下降输入源计数器清零使能 0：在GTETRGA输入的下降沿禁止计数器清除1：在GTETRGA输入的下降沿使能计数器清除	R/W*1
2	CSGTRGBR	GTETRGB引脚上升输入源计数器清零使能 0：在GTETRGB输入的上升沿禁止计数器清零1：在GTETRGB输入的上升沿使能计数器清零	R/W*1
3	CSGTRGBF	GTETRGB引脚下降输入源计数器清除启用 0：在GTETRGB输入的下降沿禁用计数器清除1：在GTETRGB输入的下降沿启用计数器清除	R/W*1
4	CSGTRGCR	GTETRGC引脚上升沿输入源计数器清零使能 0：在GTETRGC输入的上升沿禁止计数器清零1：在GTETRGC输入的上升沿使能计数器清零	R/W*1
5	CSGTRGCF	GTETRGC引脚下降输入源计数器清零使能 0：在GTETRGC输入的下降沿禁止计数器清除1：在GTETRGC输入的下降沿使能计数器清除	R/W*1
6	CSGTRGDR	GTETRGD引脚上升沿输入源计数器清零使能 0：在GTETRGD输入的上升沿禁止计数器清零1：在GTETRGD输入的上升沿使能计数器清零	R/W*1
7	CSGTRGDF	GTETRGD引脚下降输入源计数器清零使能 0：在GTETRGD输入的下降沿禁止计数器清除1：在GTETRGD输入的下降沿使能计数器清除	R/W*1
8	CSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器清零使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器清零 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿使能计数器清零	R/W
9	CSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器清零使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器清零 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿使能计数器清零	R/W
10	CSCAFBL	GTIOCnB值低电平源计数器清除启用期间的GTIOCnA引脚下降输入 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器清零 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿使能计数器清零	R/W
11	CSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器清零使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器清零 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿使能计数器清零	R/W
12	CSCBRAL	GTIOCnB引脚在GTIOCnA值低电平期间的上升沿输入源计数器清零使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止计数器清零 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿使能计数器清零	R/W
13	CSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器清零使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器清零 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿使能计数器清零	R/W
14	CSCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源计数器清零使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器清零 1：当GTIOCnA输入为0时，在GTIOCnB输入下降沿使能计数器清零	R/W

Bit	Symbol	Function	R/W
15	CSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter clear enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	CSELCA	ELC_GPTA Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTA input 1: Counter clear enabled at the ELC_GPTA input	R/W*1
17	CSELCB	ELC_GPTB Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTB input 1: Counter clear enabled at the ELC_GPTB input	R/W*1
18	CSELCC	ELC_GPTC Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTC input 1: Counter clear enabled at the ELC_GPTC input	R/W*1
19	CSELCD	ELC_GPTD Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTD input 1: Counter clear enabled at the ELC_GPTD input	R/W*1
20	CSELCE	ELC_GPTE Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTE input 1: Counter clear enabled at the ELC_GPTE input	R/W*1
21	CSELCF	ELC_GPTF Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTF input 1: Counter clear enabled at the ELC_GPTF input	R/W*1
22	CSELCG	ELC_GPTG Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTG input 1: Counter clear enabled at the ELC_GPTG input	R/W*1
23	CSELCH	ELC_GPTH Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTH input 1: Counter clear enabled at the ELC_GPTH input	R/W*1
26:24	CSCMSC[2:0]	Compare Match/Input Capture/Synchronous counter clearing Source Counter Clear Enable 0 0 0: Counter clear disabled by Compare match/ Input capture/ Synchronous counter clearing group 0 0 1: Counter clear enabled at the GTCCRA register compare match/ Input capture 0 1 0: Counter clear enabled at the GTCCRB register compare match/ Input capture 0 1 1: Counter clear enabled at the GTCCRC register compare match 1 0 0: Counter clear enabled at the GTCCRD register compare match 1 0 1: Counter clear enabled at the GTCCRE register compare match 1 1 0: Counter clear enabled at the GTCCRF register compare match 1 1 1: Counter clear enabled at the synchronous counter clearing group	R/W
27	CP1CCE	Complementary PWM mode1 Crest Source Counter Clear Enable*2 0: Counter clear disabled at the crest of complementary PWM mode1 1: Counter clear enabled at the crest of complementary PWM mode1	R/W*1
30:28	—	These bits are read as 0. The write value should be 0.	R/W
31	CCLR	Software Source Counter Clear Enable 0: Counter clear disabled by the GTCLR register 1: Counter clear enabled by the GTCLR register	R/W*1

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.

Note 2. This bit is only available in GPT324 to GPT329.
In GPT320 to GPT323, this bit is read as 0. The write value should be 0.

The GTCSR sets the source to clear the GTCNT counter.

Counter clearing can be executed whether the counter is running (GTCR.CST=1) or stopped (GTCR.CST=0).

Inputs from GTETRGn (n = A to D) pins are input to the GPT via the POEG. Set the polarity of these signals with the POEG.

CSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Clear Enable)

The CSGTRGAR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGA pin input.

Bit	Symbol	Function	R/W
15	CSCBFAH	GTIOCnA值高电平期间GTIOCnB引脚下降输入源计数器清零使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器清零 1：当GTIOCnA输入为1时，在GTIOCnB输入下降沿启用计数器清零	R/W
16	CSELCA	ELC_GPTA事件源计数器清除启用 0：在ELC_GPTA输入处禁用计数器清除1：在ELC_GPTA输入处启用计数器清除	R/W*1
17	CSELCB	ELC_GPTB事件源计数器清除启用 0：在ELC_GPTB输入处禁用计数器清除1：在ELC_GPTB输入处启用计数器清除	R/W*1
18	CSELCC	ELC_GPTC事件源计数器清除启用 0：在ELC_GPTC输入处禁用计数器清除1：在ELC_GPTC输入处启用计数器清除	R/W*1
19	CSELCD	ELC_GPTD事件源计数器清除启用 0：在ELC_GPTD输入处禁用计数器清除1：在ELC_GPTD输入处启用计数器清除	R/W*1
20	CSELCE	ELC_GPTE事件源计数器清除启用 0：在ELC_GPTE输入处禁用计数器清除1：在ELC_GPTE输入处启用计数器清除	R/W*1
21	CSELCF	ELC_GPTF事件源计数器清除启用 0：在ELC_GPTF输入处禁用计数器清除1：在ELC_GPTF输入处启用计数器清除	R/W*1
22	CSELCG	ELC_GPTG事件源计数器清除启用 0：在ELC_GPTG输入处禁用计数器清除1：在ELC_GPTG输入处启用计数器清除	R/W*1
23	CSELCH	ELC_GPTH事件源计数器清除启用 0：在ELC_GPTH输入处禁用计数器清除1：在ELC_GPTH输入处启用计数器清除	R/W*1
26:24	CSCMSC[2:0]	比较匹配输入捕获同步计数器清除源计数器清除启用 000：比较匹配禁止计数器清除输入捕捉同步计数器清除组 001：在GTCCRA寄存器比较匹配时使能计数器清除输入捕捉010：在GTCCRB寄存器比较匹配时使能计数器清除输入捕捉011：在GTCCRC寄存器比较匹配时使能计数器清除100：在计数器清除使能在GTCCRD寄存器比较匹配时101：在GTCCRE寄存器比较匹配时使能计数器清除110：在GTCCRF寄存器比较匹配时使能计数器清除111：在同步计数器清除组中使能计数器清除	R/W
27	CP1CCE	互补PWM模式1波峰源计数器清零使能*2 0：在互补PWM模式1的峰值禁止计数器清零1：在互补PWM模式1的峰值使能计数器清零	R/W*1
30:28	—	这些位被读取为0。写入值应为0。	R/W
31	CCLR	软件源计数器清除启用 0：GTCLR寄存器禁止计数器清零1：GTCLR寄存器使能计数器清零	R/W*1

注1.在互补PWM模式下，无论写入主通道从通道1从通道2的哪个寄存器，都会同时写入三个通道。

注2.该位仅在GPT324至GPT329中可用。
在GPT320到GPT323中，该位读取为0。写入值应为0。

GTCSR设置源以清除GTCNT计数器。

无论计数器正在运行(GTCR.CST=1)还是停止(GTCR.CST=0)，都可以执行计数器清除。

来自GTETRn（n=A到D）引脚的输入通过POEG输入到GPT。设置这些信号的极性
POEG.

CSGTRGAR位（GTETRGA引脚上升沿输入源计数器清零使能）

CSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Clear Enable)

The CSGTRGAF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGA pin input.

CSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Clear Enable)

The CSGTRGBR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGB pin input.

CSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Clear Enable)

The CSGTRGBF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGB pin input.

CSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Clear Enable)

The CSGTRGCR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGC pin input.

CSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Clear Enable)

The CSGTRGCF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGC pin input.

CSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Clear Enable)

The CSGTRGDR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGD pin input.

CSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Clear Enable)

The CSGTRGDF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGD pin input.

CSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Clear Enable)

The CSCARBL bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

In complementary PWM mode, this setting is invalid.

CSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Clear Enable)

The CSCARBH bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

In complementary PWM mode, this setting is invalid.

CSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Clear Enable)

The CSCAFBL bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

In complementary PWM mode, this setting is invalid.

CSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Clear Enable)

The CSCAFBH bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

In complementary PWM mode, this setting is invalid.

CSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Clear Enable)

The CSCBRAL bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

In complementary PWM mode, this setting is invalid.

CSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Clear Enable)

The CSCBRAH bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

In complementary PWM mode, this setting is invalid.

CSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Clear Enable)

The CSCBFAL bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

CSGTRGAF位（GTETRGA引脚下降输入源计数器清零使能）

CSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSGTRGBR位（GTETRGB引脚上升沿输入源计数器清零使能）

CSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGBF位（GTETRGB引脚下降输入源计数器清零使能）

CSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSGTRGCR位（GTETRGC引脚上升沿输入源计数器清零使能）

CSGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGCF位（GTETRGC引脚下降输入源计数器清零使能）

CSGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSGTRGDR位（GTETRGD引脚上升沿输入源计数器清零使能）

CSGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGDF位（GTETRGD引脚下降输入源计数器清零使能）

CSGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器清零使能）

CSCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器清零，当GTIOCnB输入为0。

在互补PWM模式下，此设置无效。

CSCARBH位（GTIOCnB值高电平期间GTIOCnA引脚上升沿输入源计数器清零使能）

CSCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器清零，当GTIOCnB输入为1。

在互补PWM模式下，此设置无效。

CSCAFBL位（GTIOCnB值低电平源计数器清除使能期间GTIOCnA引脚下降输入）

CSCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器清零，当GTIOCnB输入为0。

在互补PWM模式下，此设置无效。

CSCAFBH位（GTIOCnB值高电平源计数器清零使能期间GTIOCnA引脚下降输入）

CSCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器清零，当GTIOCnB输入为1。

在互补PWM模式下，此设置无效。

CSCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器清零使能）

CSCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器清零，当GTIOCnA输入为0。

在互补PWM模式下，此设置无效。

CSCBRAH位（GTIOCnA值高电平期间GTIOCnB引脚上升沿输入源计数器清零使能）

CSCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器清零，当GTIOCnA输入为1。

在互补PWM模式下，此设置无效。

CSCBFAL位（GTIOCnA值低电平源计数器清零使能期间GTIOCnB引脚下降输入）

CSCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器清零，当GTIOCnA输入为0。

In complementary PWM mode, this setting is invalid.

CSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Clear Enable)

The CSCBFAH bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

In complementary PWM mode, this setting is invalid.

CSELCm bit (ELCm Event Source Counter Clear Enable) (m = A to H)

The CSELCm bit enables or disables the GTCNT counter clear at the ELC_GPTm event input.

CSCMSC[2:0] bit (Compare Match/Input Capture/Synchronous counter clearing Source Counter Clear Enable)

Select enable or disable for the counter clear of the GTCNT counter by compare match/input capture/synchronous counter clearing group.

Since the compare match by the register that is performing the buffer operation (including the wave mode specific case) does not occur, the counter clear enable setting that makes the target register of the buffer operation the compare match factor is invalid.

In complementary PWM mode, the counter clear enable setting for compare match of the GTCCRB register, GTCCRE register, and GTCCRF register is invalid even when the buffer operation is not performed.

CP1CCE bit (Complementary PWM mode1 Crest Source Counter Clear Enable)

Select enable or disable for the counter clear at the crest of complementary PWM mode 1.

To enable this bit, do not set 1 to the PSYE bit of the GTIOR register.

It is valid only for the master channel in complementary PWM mode. The master channel setting also clears the GTCNT counter of the slave channel in complementary PWM mode.

CCLR bit (Software Source Counter Clear Enable)

The CCLR bit enables or disables the GTCNT counter clear by the GTCLR register.

21.2.8 GTUPSR : General PWM Timer Up Count Source Select Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)

Offset address: 0x1C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	USILVL[3:0]				USELCH	USELCG	USELCF	USELCE	USELCD	USELCC	USELCB	USELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	USGTRGDF	USGTRGDR	USGTRGCF	USGTRGCR	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	USGTRGAR	GTETRGA Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGA input 1: Counter count up enabled on the rising edge of GTETRGA input	R/W
1	USGTRGAF	GTETRGA Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGA input 1: Counter count up enabled on the falling edge of GTETRGA input	R/W
2	USGTRGBR	GTETRGB Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGB input 1: Counter count up enabled on the rising edge of GTETRGB input	R/W

在互补PWM模式下，此设置无效。

CSCBFAH位（GTIOCnA值高电平期间GTIOCnB引脚下降输入源计数器清零使能）

CSCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器清零，当GTIOCnA输入为1。

在互补PWM模式下，此设置无效。

CSELCm位（ELCm事件源计数器清除启用）（m=A到H）

CSELCm位在ELC_GPTm事件输入处启用或禁用GTCNT计数器清零。

CSCMSC[2:0]位（比较匹配输入捕捉同步计数器清除源计数器清除Enable)

通过比较匹配输入捕捉同步计数器清除组选择GTCNT计数器的计数器清除的启用或禁用。

由于执行缓冲操作（包括波形模式特定情况）的寄存器的比较匹配不会发生，使缓冲操作的目标寄存器成为比较匹配因素的计数器清除启用设置无效。

在互补PWM模式下，即使未执行缓冲操作，GTCCRB寄存器、GTCCRE寄存器和GTCCRF寄存器的比较匹配的计数器清除使能设置也无效。

CP1CCE位（互补PWM模式1波峰源计数器清零使能）

在互补PWM模式1的波峰选择启用或禁用计数器清零。

要启用该位，请勿将GTIOR寄存器的PSYE位设置为1。

仅对互补PWM模式下的主通道有效。在互补PWM模式下，主通道设置也会清除从通道的GTCNT计数器。

CCLR位（软件源计数器清除启用）

CCLR位启用或禁用由GTCLR寄存器清除的GTCNT计数器。

21.2.8 GTUPSR：通用PWM定时器向上计数源选择寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)

Offset address: 0x1C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	USILVL[3:0]				USELCH	USELCG	USELCF	USELCE	USELCD	USELCC	USELCB	USELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	USGTRGDF	USGTRGDR	USGTRGCF	USGTRGCR	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	USGTRGAR	GTETRGA引脚上升输入源计数器向上计数使能 0：在GTETRGA输入的上升沿禁止向上计数1：在GTETRGA输入的上升沿使能向上计数	R/W
1	USGTRGAF	GTETRGA引脚下降输入源计数器向上计数使能 0：在GTETRGA输入的下降沿禁止向上计数1：在GTETRGA输入的下降沿使能向上计数	R/W
2	USGTRGBR	GTETRGB引脚上升输入源计数器向上计数使能 0：在GTETRGB输入的上升沿禁止向上计数1：在GTETRGB输入的上升沿使能向上计数	R/W

Bit	Symbol	Function	R/W
3	USGTRGBF	GTETRGB Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGB input 1: Counter count up enabled on the falling edge of GTETRGB input	R/W
4	USGTRGCR	GTETRGC Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGC input 1: Counter count up enabled on the rising edge of GTETRGC input	R/W
5	USGTRGCF	GTETRGC Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGC input 1: Counter count up enabled on the falling edge of GTETRGC input	R/W
6	USGTRGDR	GTETRGD Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGD input 1: Counter count up enabled on the rising edge of GTETRGD input	R/W
7	USGTRGDF	GTETRGD Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGD input 1: Counter count up enabled on the falling edge of GTETRGD input	R/W
8	USCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count up enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	USCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count up enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	USCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count up enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	USCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count up enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	USCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count up enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	USCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count up enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	USCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count up enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	USCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count up enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	USELCA	ELC_GPTA Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTA input 1: Counter count up enabled at the ELC_GPTA input	R/W

Bit	Symbol	Function	R/W
3	USGTRGBF	GTETRGB引脚下降输入源计数器向上计数使能 0：在GTETRGB输入的下降沿禁止向上计数1：在GTETRGB输入的下降沿使能向上计数	R/W
4	USGTRGCR	GTETRGC引脚上升沿输入源计数器向上计数使能 0：在GTETRGC输入的上升沿禁止向上计数1：在GTETRGC输入的上升沿使能向上计数	R/W
5	USGTRGCF	GTETRGC引脚下降输入源计数器向上计数使能 0：在GTETRGC输入的下降沿禁止向上计数1：在GTETRGC输入的下降沿使能向上计数	R/W
6	USGTRGDR	GTETRGD引脚上升输入源计数器向上计数使能 0：在GTETRGD输入的上升沿禁止计数器向上计数1：在GTETRGD输入的上升沿使能计数器向上计数	R/W
7	USGTRGDF	GTETRGD引脚下降输入源计数器向上计数使能 0：在GTETRGD输入的下降沿禁止向上计数1：在GTETRGD输入的下降沿使能向上计数	R/W
8	USCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器向上计数使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器向上计数 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿使能计数器向上计数	R/W
9	USCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器向上计数使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器向上计数 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿使能计数器向上计数	R/W
10	USCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源计数器向上计数使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器向上计数 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿使能计数器向上计数	R/W
11	USCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器向上计数使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器向上计数 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿使能计数器向上计数	R/W
12	USCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器向上计数使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止计数器向上计数 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿使能计数器向上计数	R/W
13	USCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器向上计数使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器向上计数 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿使能计数器向上计数	R/W
14	USCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源计数器向上计数使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器向上计数 1：当GTIOCnA输入为0时，在GTIOCnB输入下降沿使能计数器向上计数	R/W
15	USCBFAH	GTIOCnA值高电平期间GTIOCnB引脚下降输入源计数器向上计数使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器向上计数 1：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿使能计数器向上计数	R/W
16	USELCA	ELC_GPTA事件源计数器向上计数启用 0：在ELC_GPTA输入处禁用计数器向上计数1：在ELC_GPTA输入处启用计数器向上计数	R/W

Bit	Symbol	Function	R/W
17	USELCB	ELC_GPTB Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTB input 1: Counter count up enabled at the ELC_GPTB input	R/W
18	USELCC	ELC_GPTC Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTC input 1: Counter count up enabled at the ELC_GPTC input	R/W
19	USELCD	ELC_GPTD Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTD input 1: Counter count up enabled at the ELC_GPTD input	R/W
20	USELCE	ELC_GPTE Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTE input 1: Counter count up enabled at the ELC_GPTE input	R/W
21	USELCF	ELC_GPTF Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTF input 1: Counter count up enabled at the ELC_GPTF input	R/W
22	USELCG	ELC_GPTG Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTG input 1: Counter count up enabled at the ELC_GPTG input	R/W
23	USELCH	ELC_GPTH Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTH input 1: Counter count up enabled at the ELC_GPTH input	R/W
27:24	USILVL[3:0]	External Input Level Source Count-Up Enable 0 0 0 0: Disables count-up by external input level 0 0 0 1: Setting prohibited 0 0 1 0: Enables count-up by GTIOCnA pin input level 0 0 0 1 1: Enables count-up by GTIOCnA pin input level 1 0 1 0 0: Enables count-up by GTIOCnB pin input level 0 0 1 0 1: Enables count-up by GTIOCnB pin input level 1 0 1 1 0: Setting prohibited 0 1 1 1: Setting prohibited 1 0 0 0: Enables count-up by GTETRGA pin input level 0 1 0 0 1: Enables count-up by GTETRGA pin input level 1 1 0 1 0: Enables count-up by GTETRGB pin input level 0 1 0 1 1: Enables count-up by GTETRGB pin input level 1 1 1 0 0: Enables count-up by GTETRGC pin input level 0 1 1 0 1: Enables count-up by GTETRGC pin input level 1 1 1 1 0: Enables count-up by GTETRGD pin input level 0 1 1 1 1: Enables count-up by GTETRGD pin input level 1	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The GTUPSR sets the source to count up the GTCNT counter.

When at least one bit in the GTUPSR register is set to 1, the GTCNT counter is counted up by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

Number of increment in counting is one even when multiple sources are generated simultaneously.

Inputs from GTETRGn (n = A to D) pins are input to the GPT via the POEG. Set the polarity of these signals with the POEG.

USGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Up Enable)

The USGTRGAR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGA pin input.

USGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Up Enable)

The USGTRGAF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGA pin input.

USGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Up Enable)

The USGTRGBR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGB pin input.

Bit	Symbol	Function	R/W
17	USELCB	ELC_GPTB事件源计数器向上计数使能 0：在ELC_GPTB输入处禁用计数器向上计数1：在ELC_GPTB输入处启用计数器向上计数	R/W
18	USELCC	ELC_GPTC事件源计数器向上计数使能 0：在ELC_GPTC输入处禁用计数器向上计数1：在ELC_GPTC输入处启用计数器向上计数	R/W
19	USELCD	ELC_GPTD事件源计数器向上计数启用 0：在ELC_GPTD输入处禁用计数器向上计数1：在ELC_GPTD输入处启用计数器向上计数	R/W
20	USELCE	ELC_GPTE事件源计数器向上计数启用 0：在ELC_GPTE输入处禁用计数器向上计数1：在ELC_GPTE输入处启用计数器向上计数	R/W
21	USELCF	ELC_GPTF事件源计数器向上计数启用 0：在ELC_GPTF输入处禁用计数器向上计数1：在ELC_GPTF输入处启用计数器向上计数	R/W
22	USELCG	ELC_GPTG事件源计数器向上计数使能 0：在ELC_GPTG输入处禁用计数器向上计数1：在ELC_GPTG输入处启用计数器向上计数	R/W
23	USELCH	ELC_GPTH事件源计数器向上计数启用 0：在ELC_GPTH输入处禁用计数器向上计数1：在ELC_GPTH输入处启用计数器向上计数	R/W
27:24	USILVL[3:0]	外部输入电平源计数启用 0000：禁止通过外部输入电平递增计数0001：设置禁止0010：允许通过GTIOCnA引脚输入电平递增计数00011：允许通过GTIOCnA引脚输入电平递增计数10100：通过GTIOCnB引脚输入电平使能向上计数00101：通过GTIOCnB引脚输入电平使能向上计数10110：设置禁止0111：设置禁止1000：使能通过GTETRGA引脚输入电平进行计数01001：启用通过GTETRGA引脚输入电平进行计数11010：启用通过GTETRGB引脚输入电平进行计数01011：启用通过GTETRGB进行计数引脚输入电平11100：允许通过GTETRGC引脚输入电平进行递增计数01101：允许通过GTETRGC引脚输入电平进行递增计数11110：允许通过GTETRGD引脚输入电平进行递增计数01111：通过GTETRGD引脚输入电平1启用计数	R/W
31:28	—	这些位被读取为0。写入值应为0。	R/W

GTUPSR将源设置为对GTCNT计数器进行计数。

当GTUPSR寄存器中的至少一位设置为1时，GTCNT计数器由该寄存器中设置为1的源进行计数。在这种情况下，GTCR.TPCS无效。

即使同时生成多个源，计数中的增量数也是1。

来自GTETRn（n=A到D）引脚的输入通过POEG输入到GPT。设置这些信号的极性
POEG.

USGTRGAR位（GTETRGA引脚上升沿输入源计数器向上计数使能）

USGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGAF位（GTETRGA引脚下降输入源计数器向上计数使能）

USGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USGTRGBR位（GTETRGB引脚上升沿输入源计数器向上计数使能）

USGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Up Enable)

The USGTRGBF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGB pin input.

USGTRGCR bit (GTETRGC Pin Rising Input Source Counter Count Up Enable)

The USGTRGCR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGC pin input.

USGTRGCF bit (GTETRGC Pin Falling Input Source Counter Count Up Enable)

The USGTRGCF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGC pin input.

USGTRGDR bit (GTETRGD Pin Rising Input Source Counter Count Up Enable)

The USGTRGDR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGD pin input.

USGTRGDF bit (GTETRGD Pin Falling Input Source Counter Count Up Enable)

The USGTRGDF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGD pin input.

USCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Up Enable)

The USCARBL bit enables or disables GTCNT counter count up on the rising edge of GTIOCnA pin input, when GTIOCnB input is 0.

USCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Up Enable)

The USCARBH bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

USCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Up Enable)

The USCAFBL bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

USCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Up Enable)

The USCAFBH bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

USCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Up Enable)

The USCBRAL bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

USCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Up Enable)

The USCBRAH bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnB pin input, when the GTIOCnA input is 1.

USCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Up Enable)

The USCBFAL bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnB pin input, when the GTIOCnA input is 0.

USCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Up Enable)

The USCBFAH bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnB pin input, when the GTIOCnA input is 1.

USELCm bit (ELC_GPTm Event Source Counter Count Up Enable) (m = A to H)

The USELCm bit enables or disables the GTCNT counter count up at the ELC_GPTm event input.

USILVL[3:0] bit (External Input Level Source Count-Up Enable)

Select enable or disable for the count-up of the GTCNT counter by the GTIOCnA pin input level, GTIOCnB pin input level, and GTETRGA/GTETRGB/GTETRGC/GTETRGD input level.

USGTRGBF位（GTETRGB引脚下降输入源计数器向上计数使能）

USGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USGTRGCR位（GTETRGC引脚上升沿输入源计数器向上计数使能）

USGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGCF位（GTETRGC引脚下降输入源计数器向上计数使能）

USGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USGTRGDR位（GTETRGD引脚上升沿输入源计数器向上计数使能）

USGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGDF位（GTETRGD引脚下降输入源计数器向上计数使能）

USGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器向上计数使能）

USCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCnB输入为0。

USCARBH位（GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器向上计数使能）

USCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCnB输入为1。

USCAFBL位（GTIOCnB值低电平源计数器向上计数启用期间的GTIOCnA引脚下降输入）

USCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器向上计数，当GTIOCnB输入为0。

USCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源计数器向上计数使能）

USCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器向上计数，当GTIOCnB输入为1。

USCBRAL位（GTIOCnA值低电平源计数器向上计数启用期间的GTIOCnB引脚上升沿输入）

USCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCnA输入为0。

USCBRAH位（GTIOCnA值高电平期间GTIOCnB引脚上升沿输入源计数器向上计数使能）

当GTIOCnA输入为1时，USCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USCBFAL位（GTIOCnA值低电平源计数器向上计数启用期间的GTIOCnB引脚下降输入）

当GTIOCnA输入为0时，USCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USCBFAH位（GTIOCnA值高电平期间的GTIOCnB引脚下降输入源计数器向上计数使能）

当GTIOCnA输入为1时，USCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USELCm位（ELC_GPTm事件源计数器向上计数启用）（m=A到H）

USELCm位在ELC_GPTm事件输入处启用或禁用GTCNT计数器向上计数。

USILVL[3:0]位（外部输入电平源计数使能）

通过GTIOCnA引脚输入电平、GTIOCnB引脚输入电平和GTETRGAGTETRGBGTETRGCGTETRGD输入电平选择GTCNT计数器的计数的启用或禁用。

21.2.9 GTDNSR : General PWM Timer Down Count Source Select Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	DSILVL[3:0]				DSELCH	DSELCG	DSELCF	DSELCE	DSELCD	DSELCC	DSELCB	DSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	DSGTRGDF	DSGTRGDR	DSGTRGCF	DSGTRGCR	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DSGTRGAR	GTETRGA Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGA input 1: Counter count down enabled on the rising edge of GTETRGA input	R/W
1	DSGTRGAF	GTETRGA Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGA input 1: Counter count down enabled on the falling edge of GTETRGA input	R/W
2	DSGTRGBR	GTETRGB Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGB input 1: Counter count down enabled on the rising edge of GTETRGB input	R/W
3	DSGTRGBF	GTETRGB Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGB input 1: Counter count down enabled on the falling edge of GTETRGB input	R/W
4	DSGTRGCR	GTETRGC Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGC input 1: Counter count down enabled on the rising edge of GTETRGC input	R/W
5	DSGTRGCF	GTETRGC Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGC input 1: Counter count down enabled on the falling edge of GTETRGC input	R/W
6	DSGTRGDR	GTETRGD Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGD input 1: Counter count down enabled on the rising edge of GTETRGD input	R/W
7	DSGTRGDF	GTETRGD Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGD input 1: Counter count down enabled on the falling edge of GTETRGD input	R/W
8	DSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count down enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	DSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count down enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	DSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count down enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W

21.2.9 GTDNSR：通用PWM定时器递减计数源选择寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	DSILVL[3:0]				DSELCH	DSELCG	DSELCF	DSELCE	DSELCD	DSELCC	DSELCB	DSELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	DSGTRGDF	DSGTRGDR	DSGTRGCF	DSGTRGCR	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DSGTRGAR	GTETRGA引脚上升输入源计数器倒计时使能 0：在GTETRGA输入的上升沿禁用计数器递减计数1：在GTETRGA输入的上升沿启用计数器递减计数	R/W
1	DSGTRGAF	GTETRGA引脚下降输入源计数器倒计时使能 0：在GTETRGA输入的下降沿禁用计数器递减计数1：在GTETRGA输入的下降沿启用计数器递减计数	R/W
2	DSGTRGBR	GTETRGB引脚上升输入源计数器倒计时使能 0：在GTETRGB输入的上升沿禁用计数器递减计数1：在GTETRGB输入的上升沿启用计数器递减计数	R/W
3	DSGTRGBF	GTETRGB引脚下降输入源计数器倒计时使能 0：在GTETRGB输入的下降沿禁用计数器递减计数1：在GTETRGB输入的下降沿启用计数器递减计数	R/W
4	DSGTRGCR	GTETRGC引脚上升输入源计数器倒计时使能 0：在GTETRGC输入的上升沿禁用计数器递减计数1：在GTETRGC输入的上升沿启用计数器递减计数	R/W
5	DSGTRGCF	GTETRGC引脚下降输入源计数器倒计时使能 0：在GTETRGC输入的下降沿禁用计数器减计数1：在GTETRGC输入的下降沿启用计数器减计数	R/W
6	DSGTRGDR	GTETRGD引脚上升输入源计数器倒计时使能 0：在GTETRGD输入的上升沿禁用计数器递减计数1：在GTETRGD输入的上升沿启用计数器递减计数	R/W
7	DSGTRGDF	GTETRGD引脚下降输入源计数器倒计时使能 0：在GTETRGD输入的下降沿禁用计数器递减计数1：在GTETRGD输入的下降沿启用计数器递减计数	R/W
8	DSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器向下计数Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器递减计数 1：当GTIOCnB输入为0时，在GTIOCnA输入上升沿使能计数器递减计数	R/W
9	DSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器向下计数Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器递减计数 1：当GTIOCnB输入为1时，在GTIOCnA输入上升沿使能计数器递减计数	R/W
10	DSCAFBL	GTIOCnB值低源计数器倒计时期间的GTIOCnA引脚下降输入Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器递减计数 1：当GTIOCnB输入为0时，在GTIOCnA输入下降沿使能计数器递减计数	R/W

Bit	Symbol	Function	R/W
11	DSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count down enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	DSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count down enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	DSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count down enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	DSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count down enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	DSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count down enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	DSELCA	ELC_GPTA Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTA input 1: Counter count down enabled at the ELC_GPTA input	R/W
17	DSELCB	ELC_GPTB Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTB input 1: Counter count down enabled at the ELC_GPTB input	R/W
18	DSELCC	ELC_GPTC Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTC input 1: Counter count down enabled at the ELC_GPTC input	R/W
19	DSELCD	ELC_GPTD Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTD input 1: Counter count down enabled at the ELC_GPTD input	R/W
20	DSELCE	ELC_GPTE Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTE input 1: Counter count down enabled at the ELC_GPTE input	R/W
21	DSELCF	ELC_GPTF Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTF input 1: Counter count down enabled at the ELC_GPTF input	R/W
22	DSELCG	ELC_GPTG Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTG input 1: Counter count down enabled at the ELC_GPTG input	R/W
23	DSELCH	ELC_GPTF Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTF input 1: Counter count down enabled at the ELC_GPTF input	R/W

Bit	Symbol	Function	R/W
11	DSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器倒计时 Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器递减计数 1：当GTIOCnB输入为1时，在GTIOCnA输入下降沿使能计数器递减计数	R/W
12	DSCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器向下计数 Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止计数器递减计数 1：当GTIOCnA输入为0时，在GTIOCnB输入上升沿使能计数器递减计数	R/W
13	DSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器向下计数 Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器递减计数 1：当GTIOCnA输入为1时，在GTIOCnB输入上升沿使能计数器递减计数	R/W
14	DSCBFAL	GTIOCnA值低源计数器倒计时期间的GTIOCnB引脚下降输入 Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器递减计数 1：当GTIOCnA输入为0时，在GTIOCnB输入下降沿使能计数器递减计数	R/W
15	DSCBFAH	GTIOCnA值高电平期间的GTIOCnB引脚下降输入源计数器倒计时 Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器递减计数 1：当GTIOCnA输入为1时，在GTIOCnB输入下降沿使能计数器递减计数	R/W
16	DSELCA	ELC_GPTA事件源计数器倒计时启用 0：在ELC_GPTA输入处禁用计数器递减计数1：在ELC_GPTA输入处启用计数器递减计数	R/W
17	DSELCB	ELC_GPTB事件源计数器倒计时启用 0：在ELC_GPTB输入处禁用计数器递减计数1：在ELC_GPTB输入处启用计数器递减计数	R/W
18	DSELCC	ELC_GPTC事件源计数器倒计时使能 0：在ELC_GPTC输入处禁用计数器递减计数1：在ELC_GPTC输入处启用计数器递减计数	R/W
19	DSELCD	ELC_GPTD事件源计数器倒计时启用 0：在ELC_GPTD输入处禁用计数器递减计数1：在ELC_GPTD输入处启用计数器递减计数	R/W
20	DSELCE	ELC_GPTE事件源计数器倒计时启用 0：在ELC_GPTE输入处禁用计数器递减计数1：在ELC_GPTE输入处启用计数器递减计数	R/W
21	DSELCF	ELC_GPTF事件源计数器倒计时启用 0：在ELC_GPTF输入处禁用计数器递减计数1：在ELC_GPTF输入处启用计数器递减计数	R/W
22	DSELCG	ELC_GPTG事件源计数器倒计时使能 0：在ELC_GPTG输入处禁用计数器递减计数1：在ELC_GPTG输入处启用计数器递减计数	R/W
23	DSELCH	ELC_GPTF事件源计数器倒计时启用 0：在ELC_GPTF输入处禁用计数器递减计数1：在ELC_GPTF输入处启用计数器递减计数	R/W

Bit	Symbol	Function	R/W
27:24	DSILVL[3:0]	External Input Level Source Count-Down Enable 0 0 0 0: Disables count-down by external input level 0 0 0 1: Setting prohibited 0 0 1 0: Enables count-down by GTIOCnA pin input level 0 0 0 1 1: Enables count-down by GTIOCnA pin input level 1 0 1 0 0: Enables count-down by GTIOCnB pin input level 0 0 1 0 1: Enables count-down by GTIOCnB pin input level 1 0 1 1 0: Setting prohibited 0 1 1 1: Setting prohibited 1 0 0 0: Enables count-down by GTETRGA pin input level 0 1 0 0 1: Enables count-down by GTETRGA pin input level 1 1 0 1 0: Enables count-down by GTETRGB pin input level 0 1 0 1 1: Enables count-down by GTETRGB pin input level 1 1 1 0 0: Enables count-down by GTETRGC pin input level 0 1 1 0 1: Enables count-down by GTETRGC pin input level 1 1 1 1 0: Enables count-down by GTETRGD pin input level 0 1 1 1 1: Enables count-down by GTETRGD pin input level 1	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The GTDNSR sets the source to count down the GTCNT counter.

When at least one bit in the GTDNSR register is set to 1, the GTCNT counter is counted down by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

Number of decrement in counting is one even when multiple sources are generated simultaneously.

Inputs from GTETRGn (n = A to D) pins are input to the GPT via the POEG. Set the polarity of these signals with the POEG.

DSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Down Enable)

The DSGTRGAR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGA pin input.

DSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Down Enable)

The DSGTRGAF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGA pin input.

DSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Down Enable)

The DSGTRGBR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGB pin input.

DSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Down Enable)

The DSGTRGBF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGB pin input.

DSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Count Down Enable)

The DSGTRGCR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGC pin input.

DSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Count Down Enable)

The DSGTRGCF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGC pin input.

DSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Count Down Enable)

The DSGTRGDR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGD pin input.

DSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Count Down Enable)

The DSGTRGDF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGD pin input.

DSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Down Enable)

The DSCARBL bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnA pin input, when the GTIOCnB input is 0.

Bit	Symbol	Function	R/W
27:24	DSILVL[3:0]	外部输入电平源倒计时启用 0000：通过外部输入电平禁用倒计时0001：设置禁止0010：通过GTIOCnA引脚输入电平启用倒计时00011：通过GTIOCnA引脚输入电平启用倒计时10100：通过GTIOCnB引脚输入电平启用倒计时00101：通过GTIOCnB引脚输入电平启用倒计时10110：设置禁止0111：设置禁止1000：启用通过GTETRGA引脚输入电平进行倒计数01001：通过GTETRGA引脚输入电平启用倒计数11010：通过GTETRGB引脚输入电平启用倒计数01011：通过GTETRGB启用倒计数引脚输入电平11100：通过GTETRGC引脚输入电平启用倒数01101：通过GTETRGC引脚输入电平启用倒数11110：通过GTETRGD引脚输入电平启用倒数01111：通过GTETRGD引脚输入电平1启用倒计时	R/W
31:28	—	这些位被读取为0。写入值应为0。	R/W

GTDNSR将源设置为对GTCNT计数器进行倒计时。

当GTDNSR寄存器中的至少一位设置为1时，GTCNT计数器由该寄存器中设置为1的源进行倒数计数。在这种情况下，GTCR.TPCS无效。

即使同时生成多个源，计数的减量也是一。

来自GTETRn（n=A到D）引脚的输入通过POEG输入到GPT。设置这些信号的极性POEG.

DSGTRGAR位（GTETRGA引脚上升沿输入源计数器倒计时使能）

DSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGAF位（GTETRGA引脚下降输入源计数器倒计时使能）

DSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSGTRGBR位（GTETRGB引脚上升输入源计数器倒计时使能）

DSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGBF位（GTETRGB引脚下降输入源计数器倒计时使能）

DSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSGTRGCR位（GTETRGC引脚上升沿输入源计数器向下计数使能）

DSGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGCF位（GTETRGC引脚下降输入源计数器倒计时使能）

DSGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSGTRGDR位（GTETRGD引脚上升沿输入源计数器倒计时使能）

DSGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGDF位（GTETRGD引脚下降输入源计数器倒计时使能）

DSGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSCARBL位（GTIOCnB值低电平期间GTIOCnA引脚上升沿输入源计数器向下计数Enable)

当GTIOCnB输入为0时，DSCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Down Enable)

The DSCARBH bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

DSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Down Enable)

The DSCAFBL bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

DSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Down Enable)

The DSCAFBH bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

DSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Down Enable)

The DSCBRAL bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

DSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Down Enable)

The DSCBRAH bit enables or disables the GTCNT counter count down on the rising edge of GTIOCnB pin input, when GTIOCnA input is 1.

DSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Down Enable)

The DSCBFAL bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

DSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Down Enable)

The DSCBFAH bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

DSELCm bit (ELC_GPTm Event Source Counter Count Down Enable) (m = A to H)

The DSELCm bit enables or disables the GTCNT counter count down at the ELC_GPTm event input.

DSILVL[3:0] bit (External Input Level Source Count-Down Enable)

Select enable or disable for the count-down of the GTCNT counter by the GTIOCnA pin input level, GTIOCnB pin input level, and GTETRGA/GTETRGB/GTETRGC/GTETRGD input level.

21.2.10 GTICASR : General PWM Timer Input Capture Source Select Register A

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x24

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	ASOC	ASELCH	ASELCG	ASELCF	ASELCE	ASELCD	ASELCC	ASELCB	ASELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	ASGTRGDF	ASGTRGDR	ASGTRGCF	ASGTRGCR	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSCARBH位（GTIOCnB值高电平期间GTIOCnA引脚上升沿输入源计数器向下计数Enable)

DSCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器倒计时，当GTIOCnB输入为1。

DSCAFBL位（GTIOCnB值低电平期间GTIOCnA引脚下降输入源计数器倒计时Enable)

当GTIOCnB输入为0时，DSCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源计数器向下计数Enable)

当GTIOCnB输入为1时，DSCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器向下计数Enable)

DSCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器倒计时，当GTIOCnA输入为0。

DSCBRAH位（GTIOCnA值高电平期间GTIOCnB引脚上升沿输入源计数器向下计数Enable)

DSCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器倒计时，当GTIOCnA输入为1。

DSCBFAL位（GTIOCnA值低电平期间GTIOCnB引脚下降输入源计数器向下计数Enable)

DSCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器倒计时，当GTIOCnA输入为0。

DSCBFAH位（GTIOCnA值高电平期间GTIOCnB引脚下降输入源计数器倒计时Enable)

当GTIOCnA输入为1时，DSCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSELCm位（ELC_GPTm事件源计数器倒计时启用）（m=A到H）

DSELCm位在ELC_GPTm事件输入处启用或禁用GTCNT计数器倒计时。

DSILVL[3:0]位（外部输入电平源倒计时使能）

通过GTIOCnA引脚输入电平、GTIOCnB引脚输入电平和GTETRGAGTETRGBGTETRGCGTETRGD输入电平选择GTCNT计数器的倒计数的启用或禁用。

21.2.10 GTICASR：通用PWM定时器输入捕捉源选择寄存器A

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x24

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	ASOC	ASELCH	ASELCG	ASELCF	ASELCE	ASELCD	ASELCC	ASELCB	ASELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	ASGTRGDF	ASGTRGDR	ASGTRGCF	ASGTRGCR	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ASGTRGAR	GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGA input 1: GTCCRA input capture enabled on the rising edge of GTETRGA input	R/W
1	ASGTRGAF	GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGA input 1: GTCCRA input capture enabled on the falling edge of GTETRGA input	R/W
2	ASGTRGBR	GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGB input 1: GTCCRA input capture enabled on the rising edge of GTETRGB input	R/W
3	ASGTRGBF	GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGB input 1: GTCCRA input capture enabled on the falling edge of GTETRGB input	R/W
4	ASGTRGCR	GTETRGC Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGC input 1: GTCCRA input capture enabled on the rising edge of GTETRGC input	R/W
5	ASGTRGCF	GTETRGC Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGC input 1: GTCCRA input capture enabled on the falling edge of GTETRGC input	R/W
6	ASGTRGDR	GTETRGD Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGD input 1: GTCCRA input capture enabled on the rising edge of GTETRGD input	R/W
7	ASGTRGDF	GTETRGD Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGD input 1: GTCCRA input capture enabled on the falling edge of GTETRGD input	R/W
8	ASCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRA input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	ASCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRA input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	ASCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRA input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	ASCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRA input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	ASCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRA input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W

Bit	Symbol	Function	R/W
0	ASGTRGAR	GTETRGA引脚上升输入源GTCCRA输入捕捉使能 0：在GTETRGA输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGA输入的上升沿启用GTCCRA输入捕捉	R/W
1	ASGTRGAF	GTETRGA引脚下降输入源GTCCRA输入捕捉使能 0：在GTETRGA输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGA输入的下降沿启用GTCCRA输入捕捉	R/W
2	ASGTRGBR	GTETRGB引脚上升输入源GTCCRA输入捕捉使能 0：在GTETRGB输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGB输入的上升沿启用GTCCRA输入捕捉	R/W
3	ASGTRGBF	GTETRGB引脚下降输入源GTCCRA输入捕捉使能 0：在GTETRGB输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGB输入的下降沿启用GTCCRA输入捕捉	R/W
4	ASGTRGCR	GTETRGC引脚上升沿输入源GTCCRA输入捕捉使能 0：在GTETRGC输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGC输入的上升沿启用GTCCRA输入捕捉	R/W
5	ASGTRGCF	GTETRGC引脚下降输入源GTCCRA输入捕捉使能 0：在GTETRGC输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGC输入的下降沿启用GTCCRA输入捕捉	R/W
6	ASGTRGDR	GTETRGD引脚上升沿输入源GTCCRA输入捕捉使能 0：在GTETRGD输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGD输入的上升沿启用GTCCRA输入捕捉	R/W
7	ASGTRGDF	GTETRGD引脚下降输入源GTCCRA输入捕捉使能 0：在GTETRGD输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGD输入的下降沿启用GTCCRA输入捕捉	R/W
8	ASCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源GTCCRA输入捕捉 Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止GTCCRA输入捕捉 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿使能GTCCRA输入捕捉	R/W
9	ASCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升输入源GTCCRA输入捕捉 Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止GTCCRA输入捕捉 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿使能GTCCRA输入捕捉	R/W
10	ASCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源GTCCRA输入捕捉 Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止GTCCRA输入捕捉 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿使能GTCCRA输入捕捉	R/W
11	ASCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源GTCCRA输入捕捉 Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止GTCCRA输入捕捉 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿启用GTCCRA输入捕捉	R/W
12	ASCBRAL	GTIOCnB引脚在GTIOCnA值低电平期间的上升沿输入源GTCCRA输入捕捉 Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止GTCCRA输入捕捉 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿使能GTCCRA输入捕捉	R/W

Bit	Symbol	Function	R/W
13	ASCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRA input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	ASCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRA input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	ASCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRA input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	ASELCA	ELC_GPTA Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTA input 1: GTCCRA input capture enabled at the ELC_GPTA input	R/W
17	ASELCB	ELC_GPTB Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTB input 1: GTCCRA input capture enabled at the ELC_GPTB input	R/W
18	ASELCC	ELC_GPTC Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTC input 1: GTCCRA input capture enabled at the ELC_GPTC input	R/W
19	ASELCD	ELC_GPTD Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTD input 1: GTCCRA input capture enabled at the ELC_GPTD input	R/W
20	ASELCE	ELC_GPTE Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTE input 1: GTCCRA input capture enabled at the ELC_GPTE input	R/W
21	ASELCF	ELC_GPTF Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTF input 1: GTCCRA input capture enabled at the ELC_GPTF input	R/W
22	ASELCG	ELC_GPTG Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTG input 1: GTCCRA input capture enabled at the ELC_GPTG input	R/W
23	ASELCH	ELC_GPTH Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTH input 1: GTCCRA input capture enabled at the ELC_GPTH input	R/W
24	ASOC	Other channel Source GTCCRA Input Capture Enable 0: Disables GTCCRA input capture by other channel factor 1: Enables GTCCRA input capture by other channel factor	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

The GTICASR sets the source of input capture for GTCCRA.

When at least one bit among bits in the GTICASR register is set to 1, input capture operation making the GTCCRA register as an input capture register is performed.

Inputs from GTETRGn (n = A to D) pins are input to the GPT via the POEG. Set the polarity of these signals with the POEG.

ASGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGAR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGA pin input.

Bit	Symbol	Function	R/W
13	ASCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源GTCCRA输入捕捉Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止GTCCRA输入捕捉 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿使能GTCCRA输入捕捉	R/W
14	ASCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源GTCCRA输入捕捉Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁用GTCCRA输入捕捉 1：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿启用GTCCRA输入捕捉	R/W
15	ASCBFAH	GTIOCnA值高电平期间GTIOCnB引脚下降输入源GTCCRA输入捕捉Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁用GTCCRA输入捕捉 1：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿启用GTCCRA输入捕捉	R/W
16	ASELCA	ELC_GPTA事件源GTCCRA输入捕获启用 0：在ELC_GPTA输入处禁用GTCCRA输入捕捉1：在ELC_GPTA输入处启用GTCCRA输入捕捉	R/W
17	ASELCB	ELC_GPTB事件源GTCCRA输入捕获启用 0：在ELC_GPTB输入处禁用GTCCRA输入捕捉1：在ELC_GPTB输入处启用GTCCRA输入捕捉	R/W
18	ASELCC	ELC_GPTC事件源GTCCRA输入捕捉使能 0：在ELC_GPTC输入处禁用GTCCRA输入捕捉1：在ELC_GPTC输入处启用GTCCRA输入捕捉	R/W
19	ASELCD	ELC_GPTD事件源GTCCRA输入捕获启用 0：在ELC_GPTD输入处禁用GTCCRA输入捕捉1：在ELC_GPTD输入处启用GTCCRA输入捕捉	R/W
20	ASELCE	ELC_GPTE事件源GTCCRA输入捕获启用 0：在ELC_GPTE输入处禁用GTCCRA输入捕捉1：在ELC_GPTE输入处启用GTCCRA输入捕捉	R/W
21	ASELCF	ELC_GPTF事件源GTCCRA输入捕获启用 0：在ELC_GPTF输入处禁用GTCCRA输入捕捉1：在ELC_GPTF输入处启用GTCCRA输入捕捉	R/W
22	ASELCG	ELC_GPTG事件源GTCCRA输入捕捉使能 0：在ELC_GPTG输入处禁用GTCCRA输入捕捉1：在ELC_GPTG输入处启用GTCCRA输入捕捉	R/W
23	ASELCH	ELC_GPTH事件源GTCCRA输入捕获启用 0：在ELC_GPTH输入处禁用GTCCRA输入捕捉1：在ELC_GPTH输入处启用GTCCRA输入捕捉	R/W
24	ASOC	其他通道源GTCCRA输入捕捉使能 0：禁用其他通道因子的GTCCRA输入捕获1：启用其他通道因子的GTCCRA输入捕获	R/W
31:25	—	这些位被读取为0。写入值应为0。	R/W

GTICASR设置GTCCRA的输入捕获源。

当GTICASR寄存器中的至少一位被设置为1时，执行将GTCCRA寄存器作为输入捕捉寄存器的输入捕捉操作。

来自GTETRn（n=A到D）引脚的输入通过POEG输入到GPT。设置这些信号的极性
POEG.

ASGTRGAR位（GTETRGA引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGAF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGA pin input.

ASGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGBR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGB pin input.

ASGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGBF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGB pin input.

ASGTRGCR bit (GTETRGC Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGCR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGC pin input.

ASGTRGCF bit (GTETRGC Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGCF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGC pin input.

ASGTRGDR bit (GTETRGD Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGDR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGD pin input.

ASGTRGDF bit (GTETRGD Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGDF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGD pin input.

ASCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable)

The ASCARBL bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

ASCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRA Input Capture Enable)

The ASCARBH bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

ASCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable)

The ASCAFBL bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

ASCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRA Input Capture Enable)

The ASCAFBH bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnA pin input, when the GTIOCnB input is 1.

ASCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable)

The ASCBRAL bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnB pin input, when the GTIOCnA input is 0.

ASCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRA Input Capture Enable)

The ASCBRAH bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

ASCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable)

The ASCBFAL bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

ASGTRGAF位（GTETRGA引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASGTRGBR位（GTETRGB引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGBF位（GTETRGB引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASGTRGCR位（GTETRGC引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGCF位（GTETRGC引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASGTRGDR位（GTETRGD引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGDF位（GTETRGD引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源GTCCRA输入捕捉Enable)

ASCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCnB输入为0。

ASCARBH位（GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源GTCCRA输入捕捉Enable)

ASCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCnB输入为1。

ASCAFBL位（GTIOCnB值低电平期间GTIOCnA引脚下降输入源GTCCRA输入捕捉Enable)

ASCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCnB输入为0。

ASCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源GTCCRA输入捕捉Enable)

当GTIOCnB输入为1时，ASCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源GTCCRA输入捕捉Enable)

当GTIOCnA输入为0时，ASCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASCBRAH位（GTIOCnA值高电平期间GTIOCnB引脚上升沿输入源GTCCRA输入捕捉Enable)

ASCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCnA输入为1。

ASCBFAL位（GTIOCnA值低电平期间GTIOCnB引脚下降输入源GTCCRA输入捕捉Enable)

ASCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCnA输入为0。

ASCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRA Input Capture Enable)

The ASCBFAH bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

ASELCm bit (ELC_GPTm Event Source Counter GTCCRA Input Capture Enable) (m = A to H)

The ASELCm bit enables or disables the input capture for GTCCRA at the ELC_GPTm event input.

ASOC bit (Other channel Source GTCCRA Input Capture Enable)

Select enable or disable for an input capture to the GTCCRA register by other channel factor.

Input capture of other channel factors is not subject to input capture factors to other channels set by the ICAFA and ICBFA bits of the GTICCR register.

21.2.11 GTICBSR : General PWM Timer Input Capture Source Select Register B

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	BSOC	BSELCH	BSELCG	BSELCF	BSELCE	BSELCD	BSELCC	BSELCB	BSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	BSGTRGDF	BSGTRGDR	BSGTRGCF	BSGTRGCR	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BSGTRGAR	GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGA input 1: GTCCRB input capture enabled on the rising edge of GTETRGA input	R/W
1	BSGTRGAF	GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGA input 1: GTCCRB input capture enabled on the falling edge of GTETRGA input	R/W
2	BSGTRGBR	GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGB input 1: GTCCRB input capture enabled on the rising edge of GTETRGB input	R/W
3	BSGTRGBF	GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGB input 1: GTCCRB input capture enabled on the falling edge of GTETRGB input	R/W
4	BSGTRGCR	GTETRGC Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGC input 1: GTCCRB input capture enabled on the rising edge of GTETRGC input	R/W
5	BSGTRGCF	GTETRGC Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGC input 1: GTCCRB input capture enabled on the falling edge of GTETRGC input	R/W
6	BSGTRGDR	GTETRGD Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGD input 1: GTCCRB input capture enabled on the rising edge of GTETRGD input	R/W
7	BSGTRGDF	GTETRGD Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGD input 1: GTCCRB input capture enabled on the falling edge of GTETRGD input	R/W

ASCBFAH位（GTIOCnA值高电平期间GTIOCnB引脚下降输入源GTCCRA输入捕捉Enable)

ASCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCnA输入为1。

ASELCm位（ELC_GPTm事件源计数器GTCCRA输入捕捉使能）（m=A到H）

ASELCm位在ELC_GPTm事件输入处启用或禁用GTCCRA的输入捕捉。

ASOC位（其他通道源GTCCRA输入捕捉使能）

通过其他通道因子选择启用或禁用GTCCRA寄存器的输入捕捉。

其他通道因子的输入捕获不受GTICCR寄存器的ICAFA和ICBFA位设置的其他通道的输入捕获因子的影响。

21.2.11 GTICBSR：通用PWM定时器输入捕捉源选择寄存器B

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	BSOC	BSELCH	BSELCG	BSELCF	BSELCE	BSELCD	BSELCC	BSELCB	BSELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	BSGTRGDF	BSGTRGDR	BSGTRGCF	BSGTRGCR	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BSGTRGAR	GTETRGA引脚上升沿输入源GTCCRB输入捕捉使能 0：在GTETRGA输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGA输入的上升沿启用GTCCRB输入捕捉	R/W
1	BSGTRGAF	GTETRGA引脚下降输入源GTCCRB输入捕捉使能 0：在GTETRGA输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGA输入的下降沿启用GTCCRB输入捕捉	R/W
2	BSGTRGBR	GTETRGB引脚上升输入源GTCCRB输入捕捉使能 0：在GTETRGB输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGB输入的上升沿启用GTCCRB输入捕捉	R/W
3	BSGTRGBF	GTETRGB引脚下降输入源GTCCRB输入捕捉使能 0：在GTETRGB输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGB输入的下降沿启用GTCCRB输入捕捉	R/W
4	BSGTRGCR	GTETRGC引脚上升沿输入源GTCCRB输入捕捉使能 0：在GTETRGC输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGC输入的上升沿启用GTCCRB输入捕捉	R/W
5	BSGTRGCF	GTETRGC引脚下降输入源GTCCRB输入捕捉使能 0：在GTETRGC输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGC输入的下降沿启用GTCCRB输入捕捉	R/W
6	BSGTRGDR	GTETRGD引脚上升沿输入源GTCCRB输入捕捉使能 0：在GTETRGD输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGD输入的上升沿启用GTCCRB输入捕捉	R/W
7	BSGTRGDF	GTETRGD引脚下降输入源GTCCRB输入捕捉使能 0：在GTETRGD输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGD输入的下降沿启用GTCCRB输入捕捉	R/W

Bit	Symbol	Function	R/W
8	BSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRB input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	BSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRB input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	BSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRB input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	BSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRB input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	BSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRB input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	BSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRB input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	BSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRB input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	BSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRB input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	BSELCA	ELC_GPTA Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTA input 1: GTCCRB input capture enabled at the ELC_GPTA input	R/W
17	BSELCB	ELC_GPTB Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTB input 1: GTCCRB input capture enabled at the ELC_GPTB input	R/W
18	BSELCC	ELC_GPTC Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTC input 1: GTCCRB input capture enabled at the ELC_GPTC input	R/W
19	BSELCD	ELC_GPTD Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTD input 1: GTCCRB input capture enabled at the ELC_GPTD input	R/W

Bit	Symbol	Function	R/W
8	BSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源GTCCRB输入捕捉Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止GTCCRB输入捕捉 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿使能GTCCRB输入捕捉	R/W
9	BSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源GTCCRB输入捕捉Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止GTCCRB输入捕捉 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿使能GTCCRB输入捕捉	R/W
10	BSCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源GTCCRB输入捕捉Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止GTCCRB输入捕捉 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿使能GTCCRB输入捕捉	R/W
11	BSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源GTCCRB输入捕捉Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止GTCCRB输入捕捉 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿使能GTCCRB输入捕捉	R/W
12	BSCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源GTCCRB输入捕捉Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止GTCCRB输入捕捉 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿使能GTCCRB输入捕捉	R/W
13	BSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源GTCCRB输入捕捉Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止GTCCRB输入捕捉 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿使能GTCCRB输入捕捉	R/W
14	BSCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源GTCCRB输入捕捉Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止GTCCRB输入捕捉 1：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿使能GTCCRB输入捕捉	R/W
15	BSCBFAH	GTIOCnA值高电平期间的GTIOCnB引脚下降输入源GTCCRB输入捕捉Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止GTCCRB输入捕捉 1：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿启用GTCCRB输入捕捉	R/W
16	BSELCA	ELC_GPTA事件源GTCCRB输入捕获启用 0：在ELC_GPTA输入处禁用GTCCRB输入捕捉1：在ELC_GPTA输入处启用GTCCRB输入捕捉	R/W
17	BSELCB	ELC_GPTB事件源GTCCRB输入捕捉使能 0：在ELC_GPTB输入处禁用GTCCRB输入捕捉1：在ELC_GPTB输入处启用GTCCRB输入捕捉	R/W
18	BSELCC	ELC_GPTC事件源GTCCRB输入捕捉使能 0：在ELC_GPTC输入处禁用GTCCRB输入捕捉1：在ELC_GPTC输入处启用GTCCRB输入捕捉	R/W
19	BSELCD	ELC_GPTD事件源GTCCRB输入捕获启用 0：在ELC_GPTD输入处禁用GTCCRB输入捕捉1：在ELC_GPTD输入处启用GTCCRB输入捕捉	R/W

Bit	Symbol	Function	R/W
20	BSELCE	ELC_GPTE Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTE input 1: GTCCRB input capture enabled at the ELC_GPTE input	R/W
21	BSELCF	ELC_GPTF Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTF input 1: GTCCRB input capture enabled at the ELC_GPTF input	R/W
22	BSELCG	ELC_GPTG Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTG input 1: GTCCRB input capture enabled at the ELC_GPTG input	R/W
23	BSELCH	ELC_GPTH Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTH input 1: GTCCRB input capture enabled at the ELC_GPTH input	R/W
24	BSOC	Other channel Source GTCCRB Input Capture Enable 0: Disables GTCCRB input capture by other channel factor 1: Enables GTCCRB input capture by other channel factor	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

The GTICBSR sets the source of input capture for GTCCRB.

When at least one bit among bits in the GTICBSR register is set to 1, input capture operation making the GTCCRB register as an input capture register is performed.

Inputs from GTETRGn (n = A to D) pins are input to the GPT via the POEG. Set the polarity of these signals with the POEG.

BSGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGAR bit enables or disables the input capture for GTCCRB on the rising edge of the GTETRGA pin input.

BSGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGAF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGA pin input.

BSGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGBR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGB pin input.

BSGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGBF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGB pin input.

BSGTRGCR bit (GTETRGC Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGCR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGC pin input.

BSGTRGCF bit (GTETRGC Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGCF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGC pin input.

BSGTRGDR bit (GTETRGD Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGDR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGD pin input.

BSGTRGDF bit (GTETRGD Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGDF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGD pin input.

BSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable)

The BSCARBL bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnA pin input, when the GTIOCnB input is 0.

Bit	Symbol	Function	R/W
20	BSELCE	ELC_GPTE事件源GTCCRB输入捕获启用 0：在ELC_GPTE输入处禁用GTCCRB输入捕捉1：在ELC_GPTE输入处启用GTCCRB输入捕捉	R/W
21	BSELCF	ELC_GPTF事件源GTCCRB输入捕获启用 0：在ELC_GPTF输入处禁用GTCCRB输入捕捉1：在ELC_GPTF输入处启用GTCCRB输入捕捉	R/W
22	BSELCG	ELC_GPTG事件源GTCCRB输入捕捉使能 0：在ELC_GPTG输入处禁用GTCCRB输入捕捉1：在ELC_GPTG输入处启用GTCCRB输入捕捉	R/W
23	BSELCH	ELC_GPTH事件源GTCCRB输入捕捉使能 0：在ELC_GPTH输入处禁用GTCCRB输入捕捉1：在ELC_GPTH输入处启用GTCCRB输入捕捉	R/W
24	BSOC	其他通道源GTCCRB输入捕捉使能 0：禁止GTCCRB其他通道因子输入捕捉1：启用GTCCRB其他通道因子输入捕捉	R/W
31:25	—	这些位被读取为0。写入值应为0。	R/W

GTICBSR设置GTCCRB的输入捕获源。

当GTICBSR寄存器中的至少一位被设置为1时，执行将GTCCRB寄存器作为输入捕捉寄存器的输入捕捉操作。

来自GTETRn（n=A到D）引脚的输入通过POEG输入到GPT。设置这些信号的极性
POEG.

BSGTRGAR位（GTETRGA引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGAF位（GTETRGA引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSGTRGBR位（GTETRGB引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGBF位（GTETRGB引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSGTRGCR位（GTETRGC引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGCF位（GTETRGC引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSGTRGDR位（GTETRGD引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGDF位（GTETRGD引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSCARBL位（GTIOCnB值低电平期间GTIOCnA引脚上升沿输入源GTCCRB输入捕捉Enable)

当GTIOCnB输入为0时，BSCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRB Input Capture Enable)

The BSCARBH bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

BSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable)

The BSCAFBL bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

BSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRB Input Capture Enable)

The BSCAFBH bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

BSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable)

The BSCBRAL bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

BSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRB Input Capture Enable)

The BSCBRAH bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

BSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable)

The BSCBFAL bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

BSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRB Input Capture Enable)

The BSCBFAH bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

BSELCm bit (ELC_GPTm Event Source Counter GTCCRB Input Capture Enable) (m = A to H)

The BSELCm bit enables or disables the input capture for GTCCRB at the ELC_GPTm event input.

BSOC bit (Other channel Source GTCCRB Input Capture Enable)

Select enable or disable for an input capture to the GTCCRB register by other channel factor.

Input capture of other channel factors is not subject to input capture factors to other channels set by the ICAFB and ICBFB bits of the GTICCR register.

21.2.12 GTCR : General PWM Timer Control Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	CKEG[1:0]		TPCS[3:0]				—	—	—	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BSCARBH位（GTIOCnB值高电平期间GTIOCnA引脚的上升沿输入源GTCCRB输入捕捉Enable)

BSCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCnB输入为1。

BSCAFBL位（GTIOCnB值低电平期间GTIOCnA引脚下降输入源GTCCRB输入捕捉Enable)

BSCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCnB输入为0。

BSCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源GTCCRB输入捕捉Enable)

BSCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCnB输入为1。

BSCBRAL位（GTIOCnA值低电平期间GTIOCnB引脚上升沿输入源GTCCRB输入捕捉Enable)

BSCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCnA输入为0。

BSCBRAH位（GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源GTCCRB输入捕捉Enable)

BSCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCnA输入为1。

BSCBFAL位（GTIOCnA值低电平期间GTIOCnB引脚下降输入源GTCCRB输入捕捉Enable)

BSCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCnA输入为0。

BSCBFAH位（GTIOCnA值高电平期间GTIOCnB引脚下降输入源GTCCRB输入捕捉Enable)

BSCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCnA输入为1。

BSELCm位（ELC_GPTm事件源计数器GTCCRB输入捕捉使能）（m=A到H）

BSELCm位在ELC_GPTm事件输入处启用或禁用GTCCRB的输入捕捉。

BSOC位（其他通道源GTCCRB输入捕捉使能）

通过其他通道因素选择启用或禁用GTCCRB寄存器的输入捕捉。

其他通道因子的输入捕获不受GTICCR寄存器的ICAFB和ICBFB位设置的其他通道的输入捕获因子的影响。

21.2.12 GTCR:通用PWM定时器控制寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	CKEG[1:0]		TPCS[3:0]				—	—	—	MD[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSCEN	—	—	CPSCD	SSCGRP[1:0]		SCGTIOC	ICDS	—	—	—	—	—	—	—	CST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CST	Count Start 0: Count operation is stopped 1: Count operation is performed	R/W*1
7:1	—	These bits are read as 0. The write value should be 0.	R/W
8	ICDS	Input Capture Operation Select During Count Stop 0: Input capture is operated during count stop. 1: Input capture is not operated during count stop.	R/W
9	SCGTIOC	GTIOC input Source Synchronous Clear Enable 0: Disables to use the counter clear by GTIOC input as the clear factor for other channels 1: Enables to use the counter clear by GTIOC input as the clear factor for other channels	R/W
11:10	SSCGRP[1:0]	Synchronous Set/Clear Group Select 0 0: Select synchronous set/clear group A 0 1: Select synchronous set/clear group B 1 0: Select synchronous set/clear group C 1 1: Select synchronous set/clear group D	R/W*1
12	CPSCD	Complementary PWM Mode Synchronous Clear Disable*2 0: Enable synchronous counter clear by other channel other than the section of trough in complementary PWM mode 1: Disable synchronous counter clear by other channel other than the section of trough in complementary PWM mode	R/W*1
14:13	—	These bits are read as 0. The write value should be 0.	R/W
15	SSCEN	Synchronous Set/Clear Enable 0: Disable Synchronous set/clear of the GTCNT counter 1: Enable Synchronous set/clear of the GTCNT counter	R/W*1
19:16	MD[3:0]	Mode Select*3 0 0 0 0: Saw-wave PWM mode 1(single buffer or double buffer possible) 0 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 0 1 0: Saw-wave PWM mode 2(single buffer or double buffer possible) 0 0 1 1: Setting prohibited 0 1 0 0: Triangle-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer possible) 0 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer possible) 0 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 0 1 1 1: Setting prohibited 1 0 0 0: Setting prohibited 1 0 0 1: Setting prohibited 1 0 1 0: Setting prohibited 1 0 1 1: Setting prohibited 1 1 0 0: Complementary PWM mode 1(transfer at crest) 1 1 0 1: Complementary PWM mode 2(transfer at trough) 1 1 1 0: Complementary PWM mode 3(transfer at crest and trough) 1 1 1 1: Complementary PWM mode 4(immediate transfer)	R/W*1
22:20	—	These bits are read as 0. The write value should be 0.	R/W

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSCEN	—	—	CPSCD	SSCGRP[1:0]		SCGTIOC	ICDS	—	—	—	—	—	—	—	CST
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CST	计数开始 0：停止计数1：进行计数	R/W*1
7:1	—	这些位被读取为0。写入值应为0。	R/W
8	ICDS	计数停止期间的输入捕捉操作选择 0：计数停止时输入捕捉动作。1：计数停止期间不进行输入捕捉。	R/W
9	SCGTIOC	GTIOC输入源同步清除使能 0：禁止使用GTIOC输入的计数器清零作为其他通道的清零因子 1：允许使用GTIOC输入的计数器清零作为其他通道的清零因子	R/W
11:10	SSCGRP[1:0]	同步设置清除组选择 00：选择同步设置清除组A01：选择同步设置清除组B10：选择同步设置清除组C11：选择同步设置清除组D	R/W*1
12	CPSCD	互补PWM模式同步清除禁用*2 0：在互补PWM模式下使能除波谷段以外的其他通道同步计数器清零 1：互补PWM模式下除波谷段以外的其他通道禁止同步计数器清零	R/W*1
14:13	—	这些位被读取为0。写入值应为0。	R/W
15	SSCEN	同步设置清除启用 0：禁止GTCNT计数器同步清零1：使能GTCNT计数器同步清零	R/W*1
19:16	MD[3:0]	模式选择*3 0000：Saw-wavePWM模式1（单缓冲器或双缓冲器均可）0001：Saw-waveone-shot脉冲模式（固定缓冲器操作）0010：Saw-wavePWM模式2（单缓冲器）缓冲区或双缓冲区可能）0011：设置禁止0100：三角波PWM模式1（32位传输在谷）（单缓冲区或双缓冲区可能） 0101：三角波PWM模式2（波峰和波谷32位传输）（单缓冲器或双缓冲器可能） 0110：三角波PWM模式3（谷底64位传输）（固定缓冲操作）0111：禁止设置1000：禁止设置1001：禁止设置1010：设置禁止1011：设置禁止1100：互补PWM模式1（波峰传输）1101：互补PWM模式2（波谷传输）1110：互补PWM模式3（波峰传输）和波谷）1111：互补PWM模式4（立即传输）	R/W*1
22:20	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
26:23	TPCS[3:0]	Timer Prescaler Select 0 0 0 0: GTCLK/1 0 0 0 1: GTCLK/2 0 0 1 0: GTCLK/4 0 0 1 1: GTCLK/8 0 1 0 0: GTCLK/16 0 1 0 1: GTCLK/32 0 1 1 0: GTCLK/64 0 1 1 1: GTCLK/128 1 0 0 0: GTCLK/256 1 0 0 1: GTCLK/512 1 0 1 0: GTCLK/1024 1 0 1 1: Setting prohibited 1 1 0 0: GTETRGA (Via the POEG) 1 1 0 1: GTETRGB (Via the POEG) 1 1 1 0: GTETRGC (Via the POEG) 1 1 1 1: GTETRGD (Via the POEG)	R/W*1
28:27	CKEG[1:0]	Clock Edge Select 0 0: Select rising edge of GTETRG for clock count 0 1: Select falling edge of GTETRG for clock count Others: Select both edge of GTETRG for clock count	R/W*1
31:29	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.
Note 2. This bit is only available in GPT324 to GPT329.
In GPT320 to GPT323, this bit is read as 0. The write value should be 0.
Note 3. MD[3] bit is only available in GPT324 to GPT329. GPT320 to GPT323 only support Saw-wave PWM mode and Triangle-wave PWM mode except Saw-wave PWM mode 2.

The GTCR controls GTCNT.

Access in 8 bit unit to GTCR is prohibited.

CST bit (Count Start)

The CST bit controls the GTCNT counter start and stop.

[Setting conditions]

- The GTSTR value where the channel number associated with the bit number is set to 1 with the GTSSR.CSTRT bit at 1
- The ELC event input, the external trigger, or the GTIOCnA/GTIOCnB input that are enabled by GTSSR for the starting counter source, occurs (n = 0 to 9)
- 1 is written by software directly.

[Clearing conditions]

- The GTSTP value where the channel number associated with the bit number is set to 1 with the GTPSR.CSTOP bit at 1
- The ELC event input, the external trigger, or the GTIOCnA/GTIOCnB input enabled by GTSSR as the counter stop source, occurs (n = 0 to 9)
- 0 is written by software directly.
- When the period count function is finished while the GTPC.ASTP bit is 1.

ICDS bit (Input Capture Operation Select During Count Stop)

This bit selects input capture operation during count stop, when the input capture function is selected.

SCGTIOC bit (GTIOC input Source Synchronous Clear Enable)

Select enable or disable the use of the counter clear by GTIOCnA/GTIOCnB input pin selected by the GTCSR register as the counter clear factor for other channels.

SSCGRP[1:0] bits (Synchronous Set/Clear Group Select)

Select the channel group of synchronous set/clear.

Bit	Symbol	Function	R/W
26:23	TPCS[3:0]	定时器预分频器选择 0000：GTCLK10001：GTCLK20010：GTCLK40011：GTCLK80100：GTCLK160101：GTCLK320110：GTCLK640111：GTCLK1281000：GTCLK2561001：GTCLK5121010：GTCLK10241011：禁止设置1100：GTETRGA（通过POEG）1101：GTETRGB（通过POEG）1110：GTETRGC（通过POEG）1111：GTETRGD（通过POEG）	R/W*1
28:27	CKEG[1:0]	时钟边沿选择 00：时钟计数选择GTETRG的上升沿01：时钟计数选择GTETRG的下降沿 其他：选择GTETRG的两个沿作为时钟计数	R/W*1
31:29	—	这些位被读取为0。写入值应为0。	R/W

注1.在互补PWM模式下，无论写入主通道从通道1从通道2的哪个寄存器，都会同时写入三个通道。

注2.该位仅在GPT324至GPT329中可用。
在GPT320到GPT323中，该位读取为0。写入值应为0。
注3.MD[3]位仅在GPT324至GPT329中可用。GPT320至GPT323仅支持Saw-wavePWM模式和Triangle-wavePWM模式，Saw-wavePWM模式2除外。

GTCR控制GTCNT。

禁止以8位为单位访问GTCR。

CST bit (Count Start)

CST位控制GTCNT计数器的启动和停止。

[Setting conditions]

●GTSTR值，其中与位号关联的通道号设置为1，GTSSR.CSTRT位为1
●发生由GTSSR为启动计数器源启用的ELC事件输入、外部触发或GTIOCnAGTIOCnB输入（n=0到9）
●1由软件直接写入。

[Clearing conditions]

●GTSTP值，其中与位号关联的通道号设置为1，且GTPSR.CSTOP位为1
●发生ELC事件输入、外部触发或GTSSR作为计数器停止源使能的GTIOCnAGTIOCnB输入（n=0至9）
●0由软件直接写入。
●当GTPC.ASTP位为1时，周期计数功能完成。

ICDS位（计数停止期间的输入捕捉操作选择）

Thisbitselectsinputcaptureoperationduringcountstop whentheinputcapturefunctionisselected.

SCGTIOC位（GTIOC输入源同步清除使能）

通过GTCSR寄存器选择的GTIOCnAGTIOCnB输入引脚选择启用或禁用计数器清零作为其他通道的计数器清零因子。

SSCGRP[1:0]位（同步设置清除组选择）

选择同步设置清除的通道组。

In complementary PWM mode, slave channels are also controlled by setting the SSCGRP[1:0] bits of the master channel.

CPSCD bit (Complementary PWM Mode Synchronous Clear Disable)

Select disable or enable of counter clear when synchronous clear from other channel occurs except section of trough in complementary PWM mode.

The slave channel is also controlled by setting the CPSCD bit of the master channel.

SSCEN bit (Synchronous Set/Clear Enable)

Select disable or enable of Synchronous set/clear.

In complementary PWM mode, slave channels are also controlled by setting the SSCEN bits of the master channel.

MD[3:0] bits (Mode Select)

These bits select the GPT operating mode.

In complementary PWM mode, slave channels are also controlled by setting the MD bits of the master channel.

Only the MD[3:2] bit (MD[2] for GPT320 to GPT323) is valid at input capture. Counting in saw-wave mode is performed with 00 for the MD[3:2] bit (0 for the MD[2] of GPT320 to GPT323), and counting in triangle-wave mode is performed with 01 for the MD[3:2] bit (1 for MD[2] of GPT320 to GPT323), and counting in complementary PWM mode is performed with 1 for the MD[3].

The MD bits must be set while the GTCNT operation is stopped.

During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), setting of the MD bits are ignored, where counting in saw-wave or triangle-wave or complementary PWM modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed.

TPCS[3:0] bits (Timer Prescaler Select)

The TPCS[3:0] bits select the clock for GTCNT. A clock prescaler can be selected independently for each channel. The TPCS[3:0] bits must be set while the GTCNT operation is stopped.

CKEG[1:0] bits (Clock Edge Select)

When GTETRG input is selected by TPCS[3:0] bits, select the edge of GTETRG input used as the clock of GTCNT counter.

Set the CKEG[1:0] bits only when the GTCNT counter operation is stopped.

21.2.13 GTUDDTYC : General PWM Timer Count Direction and Duty Setting Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	OBDTYR	OBDTYF	OBDTY[1:0]		—	—	—	—	OADTYR	OADTYF	OADTY[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	UD	Count Direction Setting 0: GTCNT counts down 1: GTCNT counts up	R/W
1	UDF	Forcible Count Direction Setting 0: Not forcibly set 1: Forcibly set	R/W

在互补PWM模式下，从通道也通过设置主通道的SSCGRP[1:0]位来控制。

CPSCD位（互补PWM模式同步清除禁止）

选择在互补PWM模式下发生除波谷部分以外的其他通道同步清除时计数器清除的禁用或启用。

从通道也通过设置主通道的CPSCD位来控制。

SSCEN bit (Synchronous Set/Clear Enable)

选择同步设置清除的禁用或启用。

在互补PWM模式下，从通道也通过设置主通道的SSCEN位来控制。

MD[3:0] bits (Mode Select)

这些位选择GPT操作模式。

在互补PWM模式下，从通道也通过设置主通道的MD位来控制。

只有MD[3:2]位（GPT320到GPT323的MD[2]）在输入捕捉时有效。锯齿波模式计数用00对应MD[3:2]位（0对应GPT320到GPT323的MD[2]），三角波模式计数用01对应MD[3：2]位（GPT320到GPT323的MD[2]为1），互补PWM模式下的计数以1为MD[3]执行。

当GTCNT操作停止时，必须设置MD位。

在事件计数操作期间（当GTUPSR和GTDNSR寄存器的位中至少有一位设置为1时），MD位的设置被忽略，其中锯齿波或三角波或互补PWM模式下的计数不是执行。相反，由GTUPSR和GTDNSR寄存器设置的源执行递增计数或递减计数。

TPCS[3:0] bits (Timer Prescaler Select)

TPCS[3:0]位选择GTCNT的时钟。可为每个通道独立选择时钟预分频器。这

当GTCNT操作停止时，必须设置TPCS[3:0]位。

CKEG[1:0]位（时钟沿选择）

当通过TPCS[3:0]位选择GTETRG输入时，选择GTETRG输入的边沿用作GTCNT计数器的时钟。

只有在GTCNT计数器操作停止时才设置CKEG[1:0]位。

21.2.13 GTUDDTYC:通用PWM定时器计数方向和占空比设置寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	OBDTYR	OBDTYF	OBDTY[1:0]		—	—	—	—	OADTYR	OADTYF	OADTY[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	UD	计数方向设置 0：GTCNT向下计数1：GTCNT向上计数	R/W
1	UDF	强制计数方向设置 0：不强制设置1 ：强制设置	R/W

Bit	Symbol	Function	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
17:16	OADTY[1:0]	GTIOCnA Output Duty Setting 0 0: GTIOCnA pin duty depends on the compare match 0 1: GTIOCnA pin duty depends on the compare match 1 0: GTIOCnA pin duty 0% 1 1: GTIOCnA pin duty 100%	R/W
18	OADTYF	Forcible GTIOCnA Output Duty Setting 0: Not forcibly set 1: Forcibly set	R/W
19	OADTYR	GTIOCnA Output Value Selecting after Releasing 0%/100% Duty Setting 0: The function selected by the GTIOA[3:2] bits is applied to the output value when the duty cycle is set after release from the 0 or 100% duty-cycle setting. 1: The function selected by the GTIOA[3:2] bits is applied to the compare match output value which is masked after release from the 0 or 100% duty-cycle setting.	R/W
23:20	—	These bits are read as 0. The write value should be 0.	R/W
25:24	OBDTY[1:0]	GTIOCnB Output Duty Setting 0 0: GTIOCnB pin duty depends on the compare match 0 1: GTIOCnB pin duty depends on the compare match 1 0: GTIOCnB pin duty 0% 1 1: GTIOCnB pin duty 100%	R/W
26	OBDTYF	Forcible GTIOCnB Output Duty Setting 0: Not forcibly set 1: Forcibly set	R/W
27	OBDTYR	GTIOCnB Output Value Selecting after Releasing 0%/100% Duty Setting 0: The function selected by the GTIOB[3:2] bits is applied to the output value when the duty cycle is set after release from the 0 or 100% duty-cycle setting. 1: The function selected by the GTIOB[3:2] bits is applied to the compare match output value which is masked after release from the 0 or 100% duty-cycle setting.	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The GTUDDTYC sets the direction in which the GTCNT counts (up-counting or down-counting), and sets the duty of the GTIOCnA/GTIOCnB pin output.

The setting is invalid during the event count operation, Saw-wave PWM mode 2, Complementary PWM mode.

Count Direction:

- In saw-wave mode.
  When the UD value is set to 0 during up-counting, the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value is set to 1 during down-counting, the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).
  When the UD value changes from 1 to 0 with the UDF bit being 0 and while counting stops, the counter starts up-counting and the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value changes from 0 to 1 with the UDF bit being 0 and while counting stops, the counter starts down-counting and the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).
  When the UDF bit is set to 1 while counting stops, the UD bit value is reflected in the count direction when counting starts.
- In triangle-wave mode.
  When the UD value changes during counting, the count direction does not change. When the UD value changes while the UDF bit is 0 and counting stops, the change is not reflected in the count direction when counting starts.
  When the UDF bit is set to 1 while counting is stopped, the UD value is reflected in the count direction when counting starts.

UD bit (Count Direction Setting)

The UD bit sets the count direction (up-counting or down-counting) for GTCNT.

Bit	Symbol	Function	R/W
15:2	—	这些位被读取为0。写入值应为0。	R/W
17:16	OADTY[1:0]	GTIOCnA输出占空比设置 00：GTIOCnA引脚占空比取决于比较匹配01：GTIOCnA引脚占空比取决于比较匹配10：GTIOCnA引脚占空比0% 11：GTIOCnA引脚占空比100%	R/W
18	OADTYF	强制GTIOCnA输出占空比设置 0：不强制设置1 ：强制设置	R/W
19	OADTYR	解除0%100%占空比设置后GTIOCnA输出值选择 0：当从0或100%占空比设置释放后设置占空比时，由GTIOA[3:2]位选择的功能应用于输出值。 1：由GTIOA[3:2]位选择的功能应用于比较匹配从0或100%占空比设置释放后被屏蔽的输出值。	R/W
23:20	—	这些位被读取为0。写入值应为0。	R/W
25:24	OBDTY[1:0]	GTIOCnB输出占空比设置 00：GTIOCnB引脚占空比取决于比较匹配01：GTIOCnB引脚占空比取决于比较匹配10：GTIOCnB引脚占空比0% 11：GTIOCnB引脚占空比100%	R/W
26	OBDTYF	强制GTIOCnB输出占空比设置 0：不强制设置1 ：强制设置	R/W
27	OBDTYR	GTIOCnB释放后输出值选择0%100%占空比设置 0：在解除0或100%占空比设置后设置占空比时，由GTIOB[3:2]位选择的功能应用于输出值。 1：GTIOB[3:2]位选择的功能应用于比较匹配从0或100%占空比设置释放后被屏蔽的输出值。	R/W
31:28	—	这些位被读取为0。写入值应为0。	R/W

GTUDDTYC设置GTCNT计数的方向（向上计数或向下计数），并设置GTIOCnAGTIOCnB引脚输出。

该设置在事件计数操作、锯波PWM模式2、互补PWM模式期间无效。

Count Direction:

●在锯齿波模式下。
如果在向上计数期间将UD值设置为0，则计数方向会在溢出时发生变化（GTCNT值变为GTPR值后与计数时钟同步的时序）。在递减计数期间将UD值设置为1时，计数方向会在下溢（GTCNT值变为0后与计数时钟同步的时序）下发生变化。当UDF位为0时UD值从1变为0并且在计数停止时，计数器开始计数并且计数方向在溢出时改变（GTCNT值变为GTPR值后与计数时钟同步的时序）。当UDF位为0且UD值从0变为1且计数停止时，计数器开始递减计数并且计数方向在下溢时改变（GTCNT值变为0后与计数时钟同步的时序）。当计数停止时UDF位设置为1时，UD位值在计数开始时反映在计数方向上。

●三角波模式。
计数过程中UD值变化时，计数方向不变。当UDF位为0时UD值发生变化并且计数停止时，该变化不会反映在计数开始时的计数方向上。当计数停止时UDF位设置为1时，UD值在计数开始时反映在计数方向上。

UD位（计数方向设置）

UD位设置GTCNT的计数方向（向上计数或向下计数）。

UDF bit (Forcible Count Direction Setting)

The UDF bit forcibly sets the count direction when GTCNT starts operation as the UD value. Only 0 should be written to this bit during counter operation. When 1 is written to this bit while counting stops, return this bit to 0 before counting starts.

Output duty

- In saw-wave mode.
  When the OADTY/OBDTY value changes during up-counting, the duty is reflected at an overflow (GTCNT = GTPR).
  When the OADTY/OBDTY value is changed during down-counting, the duty is reflected at an underflow (GTCNT = 0).
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 0 and while counting stops the output duty is not reflected at the starting counter operation. When the count direction is up, the output duty is reflected at an overflow (GTCNT = GTPR). When the count direction is down, the output duty is reflected at an underflow (GTCNT = 0).
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at starting counter operation.
- In triangle-wave mode.
  When the OADTY/OBDTY value changes during counting, the duty is reflected at an underflow.
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 0 and while counting stops, the output duty is not reflected at the starting counter operation. The output duty is reflected at an underflow.
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at starting counter operation.

In both saw-wave mode and triangle-wave mode, when the OADTYF/OBDTYF bit is set back to 0 and the OADTY[1:0]/OBDTY[1:0] bits are set after setting the OADTYF/OBDTYF bit to 1 and setting the OADTY[1:0]/OBDTY[1:0] bits for the duty of first cycle while count operation is stopped, these duty-cycle set during stopping count operation are reflected in the first cycle and the second cycle after starting count operation.

OmDTY[1:0] bits (GTIOCnm Output Duty Setting) (m = A, B)

The OmDTY[1:0] bits set the output duty (0%, 100% or compare match control) of the GTIOCm pin.

OmDTYF bit (Forcible GTIOCnm Output Duty Setting) (m = A, B)

The OmDTYF bit forcibly sets the output duty cycle to the OmDTY setting. Set this bit to 0 during counter operation.

OmDTYR bit (GTIOCnm Output Value Selecting after Releasing 0%/100% Duty Setting) (m = A, B)

The OmDTYR bit selects the value that is the object of output retained or toggled at cycle end, when the control changes from 0% or 100% duty setting to compare match for the GTIOCm pin and GTIOR.GTIOm[3:2] bits are set to 00b (output retained at cycle end) or the GTIOR.GTIOm[3:2] bits are set to 11b (output toggled at cycle end).

The GPT internally continues to perform compare match operation during duty-cycle 0% or 100% operation. When the OmDTYR bit is 1, the value after the period has elapsed due this compare match operation is target for the GTIOm[3:2] bits.

21.2.14 GTIOR : General PWM Timer I/O Control Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCSB[1:0]		NFBEN	—	OBEOCD	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	NFCSA[1:0]		NFAEN	PSYE	OAEOCD	OADF[1:0]		OAE	OAHLD	OADFLT	CPSCIR	GTIOA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

UDF位（强制计数方向设置）

当GTCNT开始操作时，UDF位将计数方向强制设置为UD值。在计数器操作期间，只能将0写入该位。当计数停止时向该位写入1时，在计数开始前将该位返回0。

输出占空比

●在锯齿波模式下。
当OADTYOBDTY值在递增计数期间发生变化时，占空比反映在溢出处(GTCNT=GTPR)。
在递减计数期间更改OADTYOBDTY值时，占空比反映为下溢(GTCNT=0)。在OADTYFOBDTYF位为0的情况下更改OADTYOBDTY值并且在计数停止时，输出占空比不会反映在启动计数器操作中。当计数方向向上时，输出占空比反映在溢出处(GTCNT=GTPR)。当计数方向向下时，输出占空比反映为下溢(GTCNT=0)。当OADTYFOBDTYF位为1并改变OADTYOBDTY值时，当计数停止时，输出占空比反映在开始计数器操作时。

●三角波模式。
当计数期间OADTYOBDTY值发生变化时，占空比反映为下溢。
在OADTYFOBDTYF位为0的情况下更改OADTYOBDTY值并且在计数停止时，输出占空比不会反映在开始计数器操作中。输出占空比反映在下溢处。当OADTYFOBDTYF位为1并改变OADTYOBDTY值时，当计数停止时，输出占空比反映在开始计数器操作时。

在锯齿波模式和三角波模式中，当OADTYFOBDTYF位被设置回0并且OADTY[1:0]OBDTY[1:0]位在设置OADTYFOBDTYF位为1并设置OADTY[1:0]OBDTY[1:0]位用于计数操作停止时第一个周期的占空比，这些在停止计数操作期间设置的占空比反映在开始计数操作后的第一个周期和第二个周期中。

OmDTY[1:0]位（GTIOCnm输出占空比设置）（m=A，B）

OmDTY[1:0]位设置GTIOCm引脚的输出占空比（0%、100%或比较匹配控制）。

OmDTYF位（强制GTIOCnm输出占空比设置）（m=A，B）

OmDTYF位强制将输出占空比设置为OmDTY设置。在计数器操作期间将此位设置为0。

OmDTYR位（释放0%100%占空比设置后选择GTIOCnm输出值）（m=A、B）

当控制从0%或100%占空比设置更改为GTIOCm引脚的比较匹配且GTIOR.GTIOm[3:2]位设置时，OmDTYR位选择作为输出对象的值，该值是在周期结束时保留或切换00b（输出在循环结束时保留）或GTIOR.GTIOm[3:2]位设置为11b（输出在循环结束时切换）。

在占空比0%或100%操作期间，GPT在内部继续执行比较匹配操作。当OmDTYR位为1时，由于此比较匹配操作而经过一段时间后的值是GTIOm[3:2]位的目标。

21.2.14 GTIOR：通用PWM定时器IO控制寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCSB[1:0]		NFBEN	—	OBEOCD	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	NFCSA[1:0]		NFAEN	PSYE	OAEOCD	OADF[1:0]		OAE	OAHLD	OADFLT	CPSCIR	GTIOA[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	GTIOA[4:0]	GTIOCnA Pin Function Select See Table 21.4 and Table 21.5.	R/W
5	CPSCIR*1	Complementary PWM Mode Initial Output at Synchronous Clear Disable 0: Output the initial value set by the GTIOR.GTIOA and GTIOB bits when synchronous clear occurs in Trough section of complementary PWM mode 1: Disable output the initial value	R/W
6	OADFLT	GTIOCnA Pin Output Value Setting at the Count Stop 0: The GTIOCnA pin outputs low when counting stops 1: The GTIOCnA pin outputs high when counting stops	R/W
7	OAHLD	GTIOCnA Pin Output Setting at the Start/Stop Count 0: The GTIOCnA pin output level at the start or stop of counting depends on the register setting 1: The GTIOCnA pin output level is retained at the start or stop of counting	R/W
8	OAE	GTIOCnA Pin Output Enable 0: Output is disabled 1: Output is enabled	R/W
10:9	OADF[1:0]	GTIOCnA Pin Disable Value Setting 0 0: Output disable is prohibited 0 1: GTIOCnA pin is set to Hi-Z on output disable 1 0: GTIOCnA pin is set to 0 on output disable 1 1: GTIOCnA pin is set to 1 on output disable	R/W
11	OAEOCD*1	GTCCRA Compare Match Cycle End Output Invalidate 0: Validate GTIOA[3:2] setting 1: Invalidate GTIOA[3:2] setting (GTIOCnA pin output is retained)	R/W
12	PSYE	PWM Synchronous output Enable 0: Disable GTCPPOm pin output 1: Enable GTCPPOm pin output	R/W
13	NFAEN	Noise Filter A Enable 0: The noise filter for the GTIOCnA pin is disabled 1: The noise filter for the GTIOCnA pin is enabled	R/W
15:14	NFCSA[1:0]	Noise Filter A Sampling Clock Select 0 0: GTCLK/1 0 1: GTCLK/4 1 0: GTCLK/16 1 1: GTCLK/64	R/W
20:16	GTIOB[4:0]	GTIOCnB Pin Function Select See Table 21.4 and Table 21.5.	R/W
21	—	This bit is read as 0. The write value should be 0.	R/W
22	OBDFLT	GTIOCnB Pin Output Value Setting at the Count Stop 0: The GTIOCnB pin outputs low when counting stops 1: The GTIOCnB pin outputs high when counting stops	R/W
23	OBHLD	GTIOCnB Pin Output Setting at the Start/Stop Count 0: The GTIOCnB pin output level at the start/stop of counting depends on the register setting 1: The GTIOCnB pin output level is retained at the start/stop of counting	R/W
24	OBE	GTIOCnB Pin Output Enable 0: Output is disabled 1: Output is enabled	R/W
26:25	OBDF[1:0]	GTIOCnB Pin Disable Value Setting 0 0: Output disable is prohibited 0 1: GTIOCnB pin is set to Hi-Z on output disable 1 0: GTIOCnB pin is set to 0 on output disable 1 1: GTIOCnB pin is set to 1 on output disable	R/W

Bit	Symbol	Function	R/W
4:0	GTIOA[4:0]	GTIOCnA引脚功能选择见表21.4和表21.5。	R/W
5	CPSCIR*1	同步清除禁用时的互补PWM模式初始输出 0：输出由GTIOR.GTIOA和GTIOB位设置的初始值，当同步清零发生在互补PWM模式的波谷部分 1：禁止输出初始值	R/W
6	OADFLT	计数停止时的GTIOCnA引脚输出值设置 0：计数停止时GTIOCnA引脚输出低电平1：计数停止时GTIOCnA引脚输出高电平	R/W
7	OAHLD	开始停止计数时的GTIOCnA引脚输出设置 0：GTIOCnA引脚在计数开始或停止时的输出电平取决于寄存器设置 1：GTIOCnA引脚输出电平在计数开始或停止时保持不变	R/W
8	OAE	GTIOCnA引脚输出使能 0：禁用输出1：启用输出	R/W
10:9	OADF[1:0]	GTIOCnA引脚禁用值设置 00：禁止输出01：GTIOCnA引脚设置为Hi-Z，输出禁止10：GTIOCnA引脚设置为0，输出禁止11：GTIOCnA引脚设置为1，输出禁止	R/W
11	OAEOCD*1	GTCCRA比较匹配周期结束输出无效 0：使GTIOA[3:2]设置有效1：使GTIOA[3:2]设置无效（保留GTIOCnA引脚输出）	R/W
12	PSYE	PWM同步输出使能 0：禁用GTCPPOm引脚输出1：启用GTCPPOm引脚输出	R/W
13	NFAEN	噪声滤波器A启用 0：GTIOCnA引脚的噪声滤波器禁用1：GTIOCnA引脚的噪声滤波器启用	R/W
15:14	NFCSA[1:0]	噪声滤波器A采样时钟选择 0 0: GTCLK/1 0 1: GTCLK/4 1 0: GTCLK/16 1 1: GTCLK/64	R/W
20:16	GTIOB[4:0]	GTIOCnB引脚功能选择见表21.4和表21.5。	R/W
21	—	该位读取为0。写入值应为0。	R/W
22	OBDFLT	计数停止时GTIOCnB引脚输出值设置 0：计数停止时GTIOCnB引脚输出低电平1：计数停止时GTIOCnB引脚输出高电平	R/W
23	OBHLD	开始停止计数时的GTIOCnB引脚输出设置 0：GTIOCnB引脚在计数开始停止时的输出电平取决于寄存器设置 1：GTIOCnB引脚输出电平在计数开始停止时保持	R/W
24	OBE	GTIOCnB引脚输出使能 0：禁用输出1：启用输出	R/W
26:25	OBDF[1:0]	GTIOCnB引脚禁用值设置 00：禁止输出01：GTIOCnB引脚在输出禁止时设置为Hi-Z10：GTIOCnB引脚在输出禁止时设置为0 11：GTIOCnB引脚在输出禁止时设置为1	R/W

Bit	Symbol	Function	R/W
27	OBEOCD*1	GTCCRB Compare Match Cycle End Output Invalidate 0: When Saw-wave PWM mode 1, validate GTIOB[3:2] setting When Saw-wave PWM mode 2, validate GTIOA[3:2] setting 1: When Saw-wave PWM mode 1, invalidate GTIOB[3:2] setting (GTIOCnB pin output is retained) When Saw-wave PWM mode 2, invalidate GTIOA[3:2] setting (GTIOCnA pin output is retained)	R/W
28	—	This bit is read as 0. The write value should be 0.	R/W
29	NFBEN	Noise Filter B Enable 0: The noise filter for the GTIOCnB pin is disabled 1: The noise filter for the GTIOCnB pin is enabled	R/W
31:30	NFCSB[1:0]	Noise Filter B Sampling Clock Select 0 0: GTCLK/1 0 1: GTCLK/4 1 0: GTCLK/16 1 1: GTCLK/64	R/W

Note 1. This bit is only available in GPT324 to GPT329.
In GPT320 to GPT323, this bit is read as 0. The write value should be 0.

The GTIOR sets the functions of the GTIOCnA, GTIOCnB and GTCPPOm pins. (n = 0 to 9, m = 0 to 4, 7)

GTIOA[4:0] bits (GTIOCnA Pin Function Select)

The GTIOA[4:0] bits select the GTIOCnA pin function. For details, see Table 21.4 and Table 21.5.

CPSCIR bit (Complementary PWM Mode Initial Output at Synchronous Clear Disable)

Select the output waveform when synchronous clear occurs in complementary PWM mode.

The initial output is disabled by this function only when synchronous clear occurs in the trough section in complementary PWM mode. If a synchronous clear occurs at any other time, the initial value set by the GTIOA[4]/GTIOB[4] bits is output regardless of the CPSCIR bit setting. In addition, the initial value set by the GTIOA[4]/GTIOB[4] bits is output even when the synchronous clear occurs in the trough section immediately after the count starts.

OADFLT bit (GTIOCnA Pin Output Value Setting at the Count Stop)

The OADFLT bit sets whether the GTIOCnA pin outputs high or low when counting stops.

OAHLD bit (GTIOCnA Pin Output Setting at the Start/Stop Count)

The OAHLD bit specifies whether the GTIOCnA pin output level is retained or the level at the start or stop of counting depends on the register setting.

When the OAHLD bit is set to 0:

- The value specified in bit [4] of the GTIOA[4:0] bits is output when counting starts
- The value specified in the OADFLT bit is output when counting stops
- If the OADFLT bit is modified while counting stops, the new value is immediately reflected in the output.

When the OAHLD bit is set to 1:

- The output is retained when counting starts or stops.

OAE bit (GTIOCnA Pin Output Enable)

The OAE bit disables or enables the GTIOCnA pin output.

When GTCCRA register is used as the input capture register (at least one bit in the GTICASR register is set to 1), the GTIOCnA pin does not output regardless of the OAE bit value.

OADF[1:0] bits (GTIOCnA Pin Disable Value Setting)

The OADF[1:0] bits select the output value of the GTIOCnA pin when an output disable request occurs.

Bit	Symbol	Function	R/W
27	OBEOCD*1	GTCCRB比较匹配周期结束输出无效 0：当Saw-wavePWM模式1时，使GTIOB[3:2]设置有效当Saw-wavePWM模式2时，使GTIOA[3:2]设置有效 1：Saw-wavePWM模式1时，GTIOB[3:2]设置无效（GTIOCnB引脚输出保持）当Saw-wavePWM模式2时，GTIOA[3:2]设置无效（GTIOCnA引脚输出保持）	R/W
28	—	该位读取为0。写入值应为0。	R/W
29	NFBEN	噪声滤波器B启用 0：GTIOCnB引脚的噪声滤波器禁用1：GTIOCnB引脚的噪声滤波器启用	R/W
31:30	NFCSB[1:0]	噪声滤波器B采样时钟选择 0 0: GTCLK/1 0 1: GTCLK/4 1 0: GTCLK/16 1 1: GTCLK/64	R/W

注1.该位仅在GPT324至GPT329中可用。
在GPT320到GPT323中，该位读取为0。写入值应为0。

GTIOR设置GTIOCnA、GTIOCnB和GTCPPOm引脚的功能。（n=0到9，m=0到4、7）

GTIOA[4:0]位（GTIOCnA引脚功能选择）

GTIOA[4:0]位选择GTIOCnA引脚功能。详见表21.4和表21.5。

CSCIR位（同步清除禁止时的互补PWM模式初始输出）

选择互补PWM模式下发生同步清零时的输出波形。

只有在互补PWM模式下的波谷部分发生同步清零时，该功能才会禁用初始输出。如果在任何其他时间发生同步清零，则输出由GTIOA[4]GTIOB[4]位设置的初始值，而与CSCIR位设置无关。此外，即使在计数开始后立即在波谷部分发生同步清零时，也会输出由GTIOA[4]GTIOB[4]位设置的初始值。

OADFLT位（计数停止时的GTIOCnA引脚输出值设置）

OADFLT位设置当计数停止时GTIOCnA引脚输出高电平还是低电平。

OAHLD位（开始停止计数时的GTIOCnA引脚输出设置）

OAHLD位指定是保留GTIOCnA引脚输出电平还是计数开始或停止时的电平取决于寄存器设置。

当OAHLD位设置为0时：

- ●GTIOA[4:0]位的位[4]中指定的值在计数开始时输出
- ●计数停止时输出OADFLT位中指定的值
- ●如果在计数停止时修改OADFLT位，则新值会立即反映在输出中。

当OAHLD位设置为1时：

- ●计数开始或停止时保持输出。

OAE位（GTIOCnA引脚输出使能）

OAE位禁用或启用GTIOCnA引脚输出。

当GTCCRA寄存器用作输入捕捉寄存器时（GTICASR寄存器中至少有一位设置为1），无论OAE位值如何，GTIOCnA引脚都不输出。

OADF[1:0]位（GTIOCnA引脚禁用值设置）

当出现输出禁用请求时，OADF[1:0]位选择GTIOCnA引脚的输出值。

OAEOCD bit (GTCCRA Compare Match Cycle End Output Invalidate)

If the cycle end matches the GTCCRA compare match timing in Saw-wave PWM mode 1 and 2, select invalid/valid of the setting of GTIOA[3:2] bits. When 1 (disabled) is set, the GTIOCnA pin holds the output when the cycle end and the GTCCRA compare match timing match.

PSYE bit (PWM Synchronous output Enable)

This bit set Enable/disable of output signal from GTCPPOm pin synchronized with the PWM cycle that toggles at the crest/trough/GTCNT counter clear of complementary PWM mode and Triangle-wave mode or the end of the cycle of the Saw-wave mode.

The initial output of the GTCPPOn output pin is Low, and the count start results in High.

NFAEN bit (Noise Filter A Enable)

The NFAEN bit disables or enables the noise filter for input from the GTIOCnA pin. Because changing the value of the bit might lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSA[1:0] bits (Noise Filter A Sampling Clock Select)

The NFCSA[1:0] bits set the sampling interval for the noise filter of the GTIOCnA pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

GTIOB[4:0] bits (GTIOCnB Pin Function Select)

The GTIOB[4:0] bits select the GTIOCnB pin function. For details, see Table 21.4 and Table 21.5.

In Saw-wave PWM mode 2, only the GTIOB[1:0] bits are valid, and the GTIOCnA pin output is selected instead of the GTIOCnB pin by the GTCCRB register compare match.

OBDFLT bit (GTIOCnB Pin Output Value Setting at the Count Stop)

The OBDFLT bit sets whether the GTIOCnB pin outputs high or low when counting stops.

OBHLD bit (GTIOCnB Pin Output Setting at the Start/Stop Count)

The OBHLD bit specifies whether theGTIOCnB pin output level is retained or the level at the start or stop of counting depends on the register setting.

When the OBHLD bit is set to 0:

- The value specified in bit [4] of the GTIOB[4:0] bits is output when counting starts
- The value specified in the OBDFLT bit is output when counting stops
- If the OBDFLT bit is modified while counting stops, the new value is immediately reflected in the output.

When the OBHLD bit is set to 1:

- The output is retained when counting starts or stops.

OBE bit (GTIOCnB Pin Output Enable)

The OBE bit disables or enables the GTIOCnB pin output.

When GTCCRB register is used as the input capture register (at least one bit in the GTICBSR register is set to 1), the GTIOCnB pin does not output regardless of the OBE bit value.

OBDF[1:0] bits (GTIOCnB Pin Disable Value Setting)

The OBDF[1:0] bits select the output value of the GTIOCnB pin, when an output disable request occurs.

OBEOCD bit (GTCCRB Compare Match Cycle End Output Invalidate)

If the cycle end matches the GTCCRB compare match timing in Saw-wave PWM mode 1 and 2, select invalid/valid of the GTIOB[3:2] bits setting in saw-wave PWM mode 1 or the GTIOA[3:2] bit setting in saw-wave PWM mode 2. When 1 (disabled) is set, the GTIOCnB pin in saw-wave PWM mode 1 or the GTIOCnA pin in saw-wave PWM mode 2 holds the output when the cycle end and the GTCCRB compare match timing match.

OAEOCD位（GTCCRA比较匹配周期结束输出无效）

如果周期结束与Saw-wavePWM模式1和2中的GTCCRA比较匹配时序匹配，则选择GTIOA[3:2]位设置的无效有效。当设置为1（禁用）时，GTIOCnA引脚在周期结束和GTCCRA比较匹配时序匹配时保持输出。

PSYE位（PWM同步输出使能）

该位设置使能禁用来自GTCPPOm引脚的输出信号，该信号与PWM周期同步，在波峰波谷切换GTCNT计数器清除互补PWM模式和三角波模式或Sawwave模式的周期结束。

GTCPPOn输出引脚的初始输出为低电平，计数开始结果为高电平。

NFAEN位（噪声滤波器A使能）

NFAEN位禁用或启用来自GTIOCnA引脚的输入的噪声滤波器。因为更改位的值可能会导致内部产生意外边沿，所以在此之前选择GTIOR寄存器中相关引脚的输出比较功能。

NFCSA[1:0]位（噪声滤波器A采样时钟选择）

NFCSA[1:0]位设置GTIOCnA引脚噪声滤波器的采样间隔。设置这些位时，请等待所选采样间隔的2个周期，然后再设置输入捕捉功能。

GTIOB[4:0]位（GTIOCnB引脚功能选择）

GTIOB[4:0]位选择GTIOCnB引脚功能。详见表21.4和表21.5。

在Saw-wavePWM模式2中，只有GTIOB[1:0]位有效，选择GTIOCnA引脚输出而不是GTOCnB引脚由GTCCRB寄存器比较匹配。

OBDFLT位（计数停止时GTIOCnB引脚输出值设置）

OBDFLT位设置当计数停止时GTIOCnB引脚输出高电平还是低电平。

OBHLD位（GTIOCnB引脚输出设置在开始停止计数）

OBHLD位指定是保留GTIOCnB引脚输出电平还是计数开始或停止时的电平取决于寄存器设置。

当OBHLD位设置为0时：

- ●GTIOB[4:0]位的位[4]中指定的值在计数开始时输出
- ●计数停止时输出OBDFLT位中指定的值
- ●如果在计数停止时修改了OBDFLT位，则新值会立即反映在输出中。

当OBHLD位设置为1时：

- ●计数开始或停止时保持输出。

OBE位（GTIOCnB引脚输出使能）

OBE位禁用或启用GTIOCnB引脚输出。

当GTCCRB寄存器用作输入捕捉寄存器时（GTICBSR寄存器中至少有一位设置为1），无论OBE位值如何，GTIOCnB引脚都不输出。

OBDF[1:0]位（GTIOCnB引脚禁用值设置）

当输出禁用请求发生时，OBDF[1:0]位选择GTIOCnB引脚的输出值。

OBEOCD位（GTCCRB比较匹配周期结束输出无效）

如果周期结束与锯齿波PWM模式1和2中的GTCCRB比较匹配时序匹配，则选择锯齿波PWM模式1中GTIOB[3:2]位设置或GTIOA[3:2]位设置无效有效在锯齿波PWM模式2中。当设置为1（禁用）时，锯齿波PWM模式1中的GTIOCnB引脚或锯齿波PWM模式2中的GTIOCnA引脚在周期结束和GTCCRB比较匹配时序时保持输出匹配。

NFBEN bit (Noise Filter B Enable)

The NFBEN bit disables or enables the noise filter for input from the GTIOCnB pin. Because changing the value of the bit might lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSB[1:0] bits (Noise Filter B Sampling Clock Select)

The NFCSB[1:0] bits set the sampling interval for the noise filter of the GTIOCnB pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

Table 21.4 Settings of GTIOA[4:0] and GTIOB[4:0] bits (Saw-wave mode, Triangle-wave mode)

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4*4	b3, b2*1 *2 *3 *4	b1, b0*2
0	0	0	0	0	Initial output is low	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	0	1	0			High output at GTCCRA/GTCCRB compare match
0	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	1	1	0			High output at GTCCRA/GTCCRB compare match
0	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	0	1	0			High output at GTCCRA/GTCCRB compare match
0	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	1	1	0			High output at GTCCRA/GTCCRB compare match
0	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	0	0	0	0	Initial output is high	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	0	1	0			High output at GTCCRA/GTCCRB compare match
1	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	1	1	0			High output at GTCCRA/GTCCRB compare match
1	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	0	1	0			High output at GTCCRA/GTCCRB compare match
1	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	1	1	0			High output at GTCCRA/GTCCRB compare match
1	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match

Note 1. The cycle end means an overflow (GTCNT changes from GTPR to 0 in up-counting), an underflow (GTCNT changes from 0 to GTPR in down-counting), or counter clearing for saw-wave mode, and a trough (GTCNT changes from 0 to 1) for triangle-wave mode.

NFBEN位（噪声滤波器B启用）

NFBEN位禁用或启用来自GTIOCnB引脚的输入的噪声滤波器。因为更改位的值可能会导致内部产生意外边沿，所以在此之前选择GTIOR寄存器中相关引脚的输出比较功能。

NFCSB[1:0]位（噪声滤波器B采样时钟选择）

NFCSB[1:0]位设置GTIOCnB引脚噪声滤波器的采样间隔。设置这些位时，请等待所选采样间隔的2个周期，然后再设置输入捕捉功能。

Table 21.4 GTIOA[4:0]和GTIOB[4:0]位的设置（锯波模式、三角波模式）

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4*4	b3, b2*1 *2 *3 *4	b1, b0*2
0	0	0	0	0	初始输出低	输出在循环结束时保留	GTCCRAGTCCRB比较匹配时保留的输出
0	0	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	0	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	0	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	0	1	0	0		循环结束时输出低	GTCCRAGTCCRB比较匹配时保留的输出
0	0	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	0	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	0	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	1	0	0	0		循环结束时的高输出	GTCCRAGTCCRB比较匹配时保留的输出
0	1	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	1	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	1	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	1	1	0	0		输出在循环结束时切换	GTCCRAGTCCRB比较匹配时保留的输出
0	1	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	1	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	1	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	0	0	0	0	初始输出高	输出在循环结束时保留	GTCCRAGTCCRB比较匹配时保留的输出
1	0	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	0	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	0	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	0	1	0	0		循环结束时输出低	GTCCRAGTCCRB比较匹配时保留的输出
1	0	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	0	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	0	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	1	0	0	0		循环结束时的高输出	GTCCRAGTCCRB比较匹配时保留的输出
1	1	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	1	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	1	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	1	1	0	0		输出在循环结束时切换	GTCCRAGTCCRB比较匹配时保留的输出
1	1	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	1	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	1	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出

注1.循环结束意味着上溢（GTCNT在向上计数时从GTPR变为0），下溢（GTCNT从0变为GTPR向下计数），或锯波模式的计数器清除，以及三角波模式的波谷（GTCNT从0变为1）。

Note 2. When the timing of a cycle end and the timing of a GTCCRA/GTCCRB compare match are the same in a compare-match operation, if the OAEOCD and OBEOCD bits are set to 0 and the end of cycle output is enabled, the b3 and b2 settings are given priority in saw-wave PWM mode, and the b1 and b0 settings are given priority in any other mode.
Note 3. In event count operation where at least one bit in GTUPSR or GTDNSR is set to 1, the setting of b3 and b2 is ignored.(GPT320 to GPT323)
Note 4. In Saw-wave PWM mode 2, GTIOB[4:2] bits is invalid. Since only GTIOCnA pins are output pins, set GTIOA[4] bit for initial output. Set GTIOA[3:2] bits for output at the end of a cycle.

Table 21.5 Settings of GTIOA[4:0] and GTIOB[4:0] bits (Complementary PWM mode)

GTIOA/GTIOB[4:0] bits*1 *2 *3					Function		
					Initial output, Active level	Up count Compare Match output	Down count Compare Match output
b4	b3	b2	b1	b0	b4	b3, b2	b1, b0
0	0	1	1	0	Initial output is Low. Active level is High.	Low output	High output
0	1	0	0	1		High output	Low output
1	0	1	1	0	Initial output is High. Active level is Low.	Low output	High output
1	1	0	0	1		High output	Low output

Note 1. In complementary PWM mode, the only values that can be set in the GTIOA[4:0] bits are 01001b, and 10110b. Setting other values is prohibited.
Note 2. In complementary PWM mode, the only values that can be set in the GTIOB[4:0] bits are 00110b, and 11001b. Setting other values is prohibited.
Note 3. In complementary PWM mode, setting GTIOB[4:0] bits does not use compare match of GTCCRB register. The combination of counter and register that is the target of compare match depends on the operation period of complementary PWM mode. For details, see section 21.3.3.7. Complementary PWM mode 1,2,3.

21.2.15 GTINTAD : General PWM Timer Interrupt Output Setting Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	GRPABL	GRPABH	GRPDTE	—	—	GRP[1:0]		—	—	—	—	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SCFPU	SCFPO	SCFF	SCFE	SCFD	SCFC	SCFB	SCFA	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	These bits are read as 0. The write value should be 0.	R/W
8	SCFA	GTCCRA Register Compare Match/Input Capture Source Synchronous Clear Enable 0: Disable use of GTCCRA register compare match/input capture as a clear factor for other channels. 1: Enable use of GTCCRA register compare match/input capture as a clear factor for other channels.	R/W
9	SCFB	GTCCRB Register Compare Match/Input Capture Source Synchronous Clear Enable 0: Disable use of GTCCRB register compare match/input capture as a clear factor for other channels. 1: Enable use of GTCCRB register compare match/input capture as a clear factor for other channels.	R/W
10	SCFC	GTCCRC Register Compare Match Source Synchronous Clear Enable 0: Disable use of GTCCRC register compare match as a clear factor for other channels. 1: Enable use of GTCCRC register compare match as a clear factor for other channels.	R/W

注2.在比较匹配操作中，当一个周期结束的时序和GTCCRAGTCCRB比较匹配的时序相同时，如果OAEOCD和OBEOCD位设置为0，并且使能了周期结束输出，则b3b2和b2设置在锯齿波PWM模式下优先，而b1和b0设置在任何其他模式下优先。

注3.在GTUPSR或GTDNSR中至少一位设置为1的事件计数操作中，忽略b3和b2的设置。（GPT320至GPT323)
注4.在Saw-wavePWM模式2中，GTIOB[4:2]位无效。因为只有GTIOCnA管脚是输出管脚，所以将GTIOA[4]位设置为初始输出。在循环结束时设置GTIOA[3:2]位用于输出。

Table 21.5 GTIOA[4:0]和GTIOB[4:0]位的设置（互补PWM模式）

GTIOA/GTIOB[4:0] bits*1 *2 *3					Function		
					初始输出，活动电平	向上计数比较匹配输出	向下计数比较匹配输出
b4	b3	b2	b1	b0	b4	b3, b2	b1, b0
0	0	1	1	0	初始输出为低。活动级别为高。	低输出	高输出
0	1	0	0	1		高输出	低输出
1	0	1	1	0	初始输出为高。活动电平为低。	低输出	高输出
1	1	0	0	1		高输出	低输出

注1.在互补PWM模式下，可以在GTIOA[4:0]位中设置的唯一值是01001b和10110b。禁止设置其他值。

注2.在互补PWM模式下，可以在GTIOB[4:0]位中设置的唯一值是00110b和11001b。禁止设置其他值。

注3.在互补PWM模式下，设置GTIOB[4:0]位不会使用GTCCRB寄存器的比较匹配。作为比较匹配目标的计数器和寄存器的组合取决于互补PWM模式的操作周期。详见21.3.3.7节。互补PWM模式1 2 3。

21.2.15 GTINTAD:通用PWM定时器中断输出设置寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	GRPABL	GRPABH	GRPDTE	—	—	GRP[1:0]		—	—	—	—	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SCFPU	SCFPO	SCFF	SCFE	SCFD	SCFC	SCFB	SCFA	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	这些位被读取为0。写入值应为0。	R/W
8	SCFA	GTCCRA寄存器比较匹配输入捕捉源同步清除使能 0：禁止使用GTCCRA寄存器比较匹配输入捕捉作为其他通道的清除因子。 1：启用GTCCRA寄存器比较匹配输入捕捉作为其他通道的清除因子。	R/W
9	SCFB	GTCCRB寄存器比较匹配输入捕捉源同步清除使能 0：禁止使用GTCCRB寄存器比较匹配输入捕捉作为其他通道的清除因子。 1：允许使用GTCCRB寄存器比较匹配输入捕捉作为其他通道的清除因子。	R/W
10	SCFC	GTCCRC寄存器比较匹配源同步清除使能 0：禁止使用GTCCRC寄存器比较匹配作为其他通道的清除因素。 1：允许使用GTCCRC寄存器比较匹配作为其他通道的明确因素。	R/W

Bit	Symbol	Function	R/W
11	SCFD	GTCCRD Register Compare Match Source Synchronous Clear Enable 0: Disable use of GTCCRD register compare match as a clear factor for other channels. 1: Enable use of GTCCRD register compare match as a clear factor for other channels.	R/W
12	SCFE	GTCCRE Register Compare Match Source Synchronous Clear Enable 0: Disable use of GTCCRE register compare match as a clear factor for other channels. 1: Enable use of GTCCRE register compare match as a clear factor for other channels	R/W
13	SCFF	GTCCRF Register Compare Match Source Synchronous Clear Enable 0: Disable use of GTCCRF register compare match as a clear factor for other channels. 1: Enable use of GTCCRF register compare match as a clear factor for other channels	R/W
14	SCFPO	Overflow Source Synchronous Clear Enable 0: Disable use of overflow as a clear factor for other channels. 1: Enable use of overflow as a clear factor for other channels.	R/W
15	SCFPU	Underflow Source Synchronous Clear Enable 0: Disable use of underflow as a clear factor for other channels 1: Enable use of underflow as a clear factor for other channels	R/W
16	ADTRAUEN	GTADTRA Register Compare Match (Up-Counting) A/D Conversion Start Request Enable 0: A/D conversion start request is disabled. 1: A/D conversion start request is enabled.	R/W
17	ADTRADEN	GTADTRA Register Compare Match (Down-Counting) A/D Conversion Start Request Enable 0: A/D conversion start request is disabled. 1: A/D conversion start request is enabled.	R/W
18	ADTRBUEN	GTADTRB Register Compare Match (Up-Counting) A/D Conversion Start Request Enable 0: A/D conversion start request is disabled. 1: A/D conversion start request is enabled.	R/W
19	ADTRBDEN	GTADTRB Register Compare Match (Down-Counting) A/D Conversion Start Request Enable 0: A/D conversion start request is disabled. 1: A/D conversion start request is enabled.	R/W
23:20	—	These bits are read as 0. The write value should be 0.	R/W
25:24	GRP[1:0]	Output Disable Source Select 0 0: Group A output disable source is selected 0 1: Group B output disable source is selected 1 0: Group C output disable source is selected 1 1: Group D output disable source is selected	R/W
27:26	—	These bits are read as 0. The write value should be 0.	R/W
28	GRPDTE	Dead Time Error Output Disable Request Enable 0: Dead time error output disable request is disabled. 1: Dead time error output disable request is enabled.	R/W
29	GRPABH	Same Time Output Level High Disable Request Enable 0: Same time output level high disable request disabled 1: Same time output level high disable request enabled	R/W
30	GRPABL	Same Time Output Level Low Disable Request Enable 0: Same time output level low disable request disabled 1: Same time output level low disable request enabled	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

The GTINTAD enables or disables interrupt requests, A/D conversion start request, and output disable requests.

SCFA bit (GTCCRA Register Compare Match/Input Capture Source Synchronous Clear Enable)

This bit enables or disables use of GTCCRA register compare match/input capture as a clear factor for other channels.

Bit	Symbol	Function	R/W
11	SCFD	GTCCRD寄存器比较匹配源同步清除使能 0：禁止使用GTCCRD寄存器比较匹配作为其他通道的清除因素。 1：允许使用GTCCRD寄存器比较匹配作为其他通道的清除因素。	R/W
12	SCFE	GTCCRE寄存器比较匹配源同步清除使能 0：禁止使用GTCCRE寄存器比较匹配作为其他通道的清除因素。 1：允许使用GTCCRE寄存器比较匹配作为其他通道的明确因素	R/W
13	SCFF	GTCCRF寄存器比较匹配源同步清除使能 0：禁止使用GTCCRF寄存器比较匹配作为其他通道的清除因素。 1：允许使用GTCCRF寄存器比较匹配作为其他通道的明确因素	R/W
14	SCFPO	溢出源同步清除使能 0：禁止使用溢出作为其他通道的清除因子。1：允许使用溢出作为其他通道的明确因素。	R/W
15	SCFPU	下溢源同步清除使能 0：禁止将下溢用作其他通道的清除因子1：启用将下溢用作其他通道的清除因子	R/W
16	ADTRAUEN	GTADTRA寄存器比较匹配（向上计数）AD转换启动请求使能 0：AD转换启动请求无效。1：D转换启动请求有效。	R/W
17	ADTRADEN	GTADTRA寄存器比较匹配（递减计数）AD转换开始请求Enable 0：AD转换启动请求无效。1：D转换启动请求有效。	R/W
18	ADTRBUEN	GTADTRB寄存器比较匹配（向上计数）AD转换启动请求使能 0：AD转换启动请求无效。1：D转换启动请求有效。	R/W
19	ADTRBDEN	GTADTRB寄存器比较匹配（递减计数）AD转换开始请求Enable 0：AD转换启动请求无效。1：D转换启动请求有效。	R/W
23:20	—	这些位被读取为0。写入值应为0。	R/W
25:24	GRP[1:0]	输出禁用源选择 0 0: 选择A组输出禁用源选择B组输出禁用源选 0 1: 择C 组输出禁用源选择D组输出禁用源 1 0: 1 1:	R/W
27:26	—	这些位被读取为0。写入值应为0。	R/W
28	GRPDTE	死区时间错误输出禁用请求启用 0：死区错误输出禁用请求被禁用。1：使能死区错误输出禁用请求。	R/W
29	GRPABH	同时输出电平高禁用请求启用 0：禁止同时输出电平高禁止请求1：允许同时输出电平高禁止请求	R/W
30	GRPABL	同时输出电平低禁用请求启用 0：禁止同时输出电平低禁止请求1：允许同时输出电平低禁止请求	R/W
31	—	该位读取为0。写入值应为0。	R/W

GTINTAD启用或禁用中断请求、AD转换启动请求和输出禁用请求。

SCFA位（GTCCRA寄存器比较匹配输入捕捉源同步清除使能）

该位启用或禁用GTCCRA寄存器比较匹配输入捕捉作为其他通道的清除因素。

SCFB bit (GTCCRB Register Compare Match/Input Capture Source Synchronous Clear Enable)

This bit enables or disables use of GTCCRB register compare match/input capture as a clear factor for other channels.

The setting is invalid in complementary PWM mode.

SCFC bit (GTCCRC Register Compare Match Source Synchronous Clear Enable)

This bit enables or disables use of GTCCRC register compare match as a clear factor for other channels.

The setting is invalid in complementary PWM mode.

SCFD bit (GTCCRD Register Compare Match Source Synchronous Clear Enable)

This bit enables or disables use of GTCCRD register compare match as a clear factor for other channels.

The setting is invalid in complementary PWM mode.

SCFE bit (GTCCRE Register Compare Match Source Synchronous Clear Enable)

This bit enables or disables use of GTCCRE register compare match as a clear factor for other channels.

The setting is invalid in complementary PWM mode.

SCFF bit (GTCCRF Register Compare Match Source Synchronous Clear Enable)

This bit enables or disables use of GTCCRF register compare match as a clear factor for other channels.

The setting is invalid in complementary PWM mode.

SCFPO bit (Overflow Source Synchronous Clear Enable)

This bit enables or disables use of overflow as a clear factor for other channels.

In complementary PWM mode, it is valid only for the master channel.

SCFPU bit (Underflow Source Synchronous Clear Enable)

This bit enables or disables use of underflow as a clear factor for other channels.

In complementary PWM mode, it is valid only for the master channel.

ADTRAUEN bit (GTADTRA Register Compare Match (Up-Counting) A/D Conversion Start Request Enable)

This bit enables or disables A/D conversion start requests generated by GTADTRA register compare matches during GTCNT counter up-counting.

In complementary PWM mode, it is valid only for the master channel.

The setting is invalid during the event count operation, and A/D conversion start request is not generated.

ADTRADEN bit (GTADTRA Register Compare Match (Down-Counting) A/D Conversion Start Request Enable)

This bit enables or disables A/D conversion start requests generated by GTADTRA register compare matches during GTCNT counter down-counting.

In complementary PWM mode, it is valid only for the master channel.

The setting is invalid during the event count operation, and A/D conversion start request is not generated.

ADTRBUEN bit (GTADTRB Register Compare Match (Up-Counting) A/D Conversion Start Request Enable)

This bit enables or disables A/D conversion start requests generated by GTADTRB register compare matches during GTCNT counter up-counting.

In complementary PWM mode, it is valid only for the master channel.

The setting is invalid during the event count operation, and A/D conversion start request is not generated.

SCFB位（GTCCRB寄存器比较匹配输入捕捉源同步清除使能）

该位启用或禁用GTCCRB寄存器比较匹配输入捕捉作为其他通道的清除因素。

该设置在互补PWM模式下无效。

SCFC位（GTCCRC寄存器比较匹配源同步清除使能）

该位启用或禁用GTCCRC寄存器比较匹配作为其他通道的清除因素。

该设置在互补PWM模式下无效。

SCFD位（GTCCRD寄存器比较匹配源同步清除使能）

该位启用或禁用GTCCRD寄存器比较匹配作为其他通道的清除因素。

该设置在互补PWM模式下无效。

SCFE位（GTCCRE寄存器比较匹配源同步清除使能）

该位启用或禁用GTCCRE寄存器比较匹配作为其他通道的清除因素。

该设置在互补PWM模式下无效。

SCFF位（GTCCRF寄存器比较匹配源同步清除使能）

该位启用或禁用GTCCRF寄存器比较匹配作为其他通道的清除因素。

该设置在互补PWM模式下无效。

SCFPO位（溢出源同步清除使能）

该位启用或禁用使用溢出作为其他通道的清除因子。

在互补PWM模式下，仅对主通道有效。

SCFPU位（下溢源同步清除使能）

该位启用或禁用使用下溢作为其他通道的清除因素。

在互补PWM模式下，仅对主通道有效。

ADTRAUEN位（GTADTRA寄存器比较匹配（向上计数）AD转换开始请求Enable)

该位启用或禁用GTADTRA寄存器比较匹配期间生成的AD转换启动请求GTCNT counter up-counting.

在互补PWM模式下，仅对主通道有效。

事件计数操作中设置无效，不产生AD转换启动请求。

ADTRADEN位（GTADTRA寄存器比较匹配（递减计数）AD转换开始请求Enable)

该位启用或禁用GTADTRA寄存器比较匹配期间生成的AD转换启动请求GTCNT counter down-counting.

在互补PWM模式下，仅对主通道有效。

事件计数操作中设置无效，不产生AD转换启动请求。

ADTRBUEN位（GTADTRB寄存器比较匹配（向上计数）AD转换开始请求Enable)

该位启用或禁用由GTADTRB寄存器比较匹配产生的AD转换启动请求GTCNT counter up-counting.

在互补PWM模式下，仅对主通道有效。

事件计数操作中设置无效，不产生AD转换启动请求。

ADTRBDEN bit (GTADTRB Register Compare Match (Down-Counting) A/D Conversion Start Request Enable)

This bit enables or disables A/D conversion start requests generated by GTADTRB register compare matches during GTCNT counter down-counting.

In complementary PWM mode, it is valid only for the master channel.

The setting is invalid during the event count operation, and A/D conversion start request is not generated.

GRP[1:0] bits (Output Disable Source Select)

These bits select the group of output disable request from GPT to POEG and the group of output disable for GTIOCnA pin and GTIOCnB pin from POEG to GPT.

The output disable request to POEG is output to the group selected in the GRP[1:0] bit, with dead-time errors, simultaneous high output, and simultaneous low output factors following their respective disable request enable bits.

GTST.ODF shows the request of the output disable source group that is selected with the GRP[1:0] bits. Set the GRP[1:0] bits when both GTIOR.OAE and GTIOR.OBE bits are 0.

GRPDTE bit (Dead Time Error Output Disable Request Enable)

This bit enables or disables the output disable request by a dead time error.

The dead time error output disable request is not generated during the event count operation.

GRPABH bit (Same Time Output Level High Disable Request Enable)

The GRPABH bit enables or disables the output disable request when the GTIOCnA pin and GTIOCnB pin output 1 at the same time.

GRPABL bit (Same Time Output Level Low Disable Request Enable)

The GRPABL bit enables or disables the output disable request when the GTIOCnA pin and GTIOCnB pin output 0 at the same time.

21.2.16 GTST : General PWM Timer Status Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x3C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PCF	OABLF	OABHF	DTEF	—	—	—	ODF	—	—	—	—	ADTRBDF	ADTRBUF	ADTRADF	ADTRAUF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TUCF	—	—	—	—	ITCNT[2:0]			TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCFA	Input Capture/Compare Match Flag A 0: No input capture/compare match of GTCCRA is generated 1: An input capture/compare match of GTCCRA is generated	R/W*1
1	TCFB	Input Capture/Compare Match Flag B 0: No input capture/compare match of GTCCRB is generated 1: An input capture/compare match of GTCCRB is generated	R/W*1
2	TCFC	Input Compare Match Flag C 0: No compare match of GTCCRC is generated 1: A compare match of GTCCRC is generated	R/W*1
3	TCFD	Input Compare Match Flag D 0: No compare match of GTCCRD is generated 1: A compare match of GTCCRD is generated	R/W*1

ADTRBDEN位（GTADTRB寄存器比较匹配（递减计数）AD转换开始请求 Enable)

该位启用或禁用由GTADTRB寄存器比较匹配产生的AD转换启动请求
GTCNT counter down-counting.

在互补PWM模式下，仅对主通道有效。

事件计数操作中设置无效，不产生AD转换启动请求。

GRP[1:0]位（输出禁用源选择）

这些位选择从GPT到POEG的输出禁用请求组以及从POEG到GPT的GTIOCnA引脚和GTIOCnB引脚的输出禁用组。

对POEG的输出禁用请求输出到在GRP[1:0]位中选择的组，在其各自的禁用请求启用位之后具有死区错误、同时高输出和同时低输出因子。

GTST.ODF显示了使用GRP[1:0]位选择的输出禁用源组的请求。当GTIOR.OAE和GTIOR.OBE位均为0时，设置GRP[1:0]位。

GRPDTE位（死区错误输出禁用请求启用）

该位通过死区时间错误启用或禁用输出禁用请求。

在事件计数操作期间不生成死区错误输出禁用请求。

GRPABH位（同时输出电平高禁用请求启用）

GRPABH位允许或禁止GTIOCnA引脚和GTIOCnB引脚同时输出1时的输出禁止请求。

GRPABL位（同时输出电平低禁用请求启用）

当GTIOCnA引脚和GTIOCnB引脚同时输出0时，GRPABL位允许或禁止输出禁止请求。

21.2.16 GTST：通用PWM定时器状态寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x3C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PCF	OABLF	OABHF	DTEF	—	—	—	ODF	—	—	—	—	ADTRBDF	ADTRBUF	ADTRADF	ADTRAUF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TUCF	—	—	—	—	ITCNT[2:0]			TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
重置后的值:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCFA	输入捕捉比较匹配标志A 0：不产生GTCCRA的输入捕捉比较匹配1：产生GTCCRA的输入捕捉比较匹配	R/W*1
1	TCFB	输入捕捉比较匹配标志B 0：不生成GTCCRB的输入捕捉比较匹配1：生成GTCCRB的输入捕捉比较匹配	R/W*1
2	TCFC	输入比较匹配标志C 0：没有生成GTCCRC的比较匹配1：生成了GTCCRC的比较匹配	R/W*1
3	TCFD	输入比较匹配标志D 0：不产生GTCCRD的比较匹配1：产生GTCCRD的比较匹配	R/W*1

Bit	Symbol	Function	R/W
4	TCFE	Input Compare Match Flag E 0: No compare match of GTCCRE is generated 1: A compare match of GTCCRE is generated	R/W*1
5	TCFF	Input Compare Match Flag F 0: No compare match of GTCCRF is generated 1: A compare match of GTCCRF is generated	R/W*1
6	TCFPO	Overflow Flag 0: No overflow (crest) occurred 1: An overflow (crest) occurred	R/W*1
7	TCFPU	Underflow Flag 0: No underflow (trough) occurred 1: An underflow (trough) occurred	R/W*1
10:8	ITCNT[2:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Count Counter	R
14:11	—	These bits are read as 0. The write value should be 0.	R/W
15	TUCF	Count Direction Flag 0: GTCNT counter counts downward 1: GTCNT counter counts upward	R
16	ADTRAUF	GTADTRA Register Compare Match (Up-Counting) A/D Conversion Start Request Flag 0: No GTADTRA register compare match has occurred in up-counting. 1: A GTADTRA register compare match has occurred in up-counting.	R/W*1
17	ADTRADF	GTADTRA Register Compare Match (Down-Counting) A/D Conversion Start Request Flag 0: No GTADTRA register compare match has occurred in down-counting. 1: A GTADTRA register compare match has occurred in down-counting.	R/W*1
18	ADTRBUF	GTADTRB Register Compare Match (Up-Counting) A/D Conversion Start Request Flag 0: No GTADTRB register compare match has occurred in up-counting. 1: A GTADTRB register compare match has occurred in up-counting.	R/W*1
19	ADTRBDF	GTADTRB Register Compare Match (Down-Counting) A/D Conversion Start Request Flag 0: No GTADTRB register compare match has occurred in down-counting. 1: A GTADTRB register compare match has occurred in down-counting.	R/W*1
23:20	—	These bits are read as 0. The write value should be 0.	R/W
24	ODF	Output Disable Flag 0: No output disable request is generated 1: An output disable request is generated	R
27:25	—	These bits are read as 0. The write value should be 0.	R/W
28	DTEF	Dead Time Error Flag 0: No dead time error has occurred. 1: A dead time error has occurred.	R
29	OABHF	Same Time Output Level High Flag 0: No simultaneous generation of 1 both for the GTIOCA and GTIOCB pins has occurred. 1: A simultaneous generation of 1 both for the GTIOCA and GTIOCB pins has occurred.	R
30	OABLF	Same Time Output Level Low Flag 0: No simultaneous generation of 0 both for the GTIOCA and GTIOCB pins has occurred. 1: A simultaneous generation of 0 both for the GTIOCA and GTIOCB pins has occurred.	R
31	PCF*2	Period Count Function Finish Flag 0: No period count function finish has occurred 1: A period count function finish has occurred	R/W*1

Note 1. Only 0 can be written to this bit. Do not write 1.
When clearing the ADTRAUF, ADTRADF, ADTRBUF, or ADTRBDF flag, be sure to write 0 only to the target flag or flags for clearing and to write 1 to the other flags not for clearing.
Note 2. This bit is only available in GPT320 to GPT323.
In GPT324 to GPT329, this bit is read as 0. The write value should be 0.

The GTST indicates the status of the GPT.

Bit	Symbol	Function	R/W
4	TCFE	输入比较匹配标志E 0：不生成GTCCRE的比较匹配1：生成GTCCRE的比较匹配	R/W*1
5	TCFF	输入比较匹配标志F 0：不产生GTCCRF的比较匹配1：产生GTCCRF的比较匹配	R/W*1
6	TCFPO	溢出标志 0：未发生溢出（波峰）1：发生溢出（波峰）	R/W*1
7	TCFPU	Underflow Flag 0：未发生下溢（波谷）1：发生下溢（波谷）	R/W*1
10:8	ITCNT[2:0]	GPTn_OVFGPTn_UDF中断跳过计数计数器	R
14:11	—	这些位被读取为0。写入值应为0。	R/W
15	TUCF	计数方向标志 0：GTCNT计数器向下计数1：GTCNT计数器向上计数	R
16	ADTRAUF	GTADTRA寄存器比较匹配（向上计数）AD转换开始请求标志 0：向上计数时未发生GTADTRA寄存器比较匹配。1：在递增计数中发生GTADTRA寄存器比较匹配。	R/W*1
17	ADTRADF	GTADTRA寄存器比较匹配（递减计数）AD转换开始请求标志 0：递减计数时未发生GTADTRA寄存器比较匹配。1：向下计数时发生GTADTRA寄存器比较匹配。	R/W*1
18	ADTRBUF	GTADTRB寄存器比较匹配（向上计数）AD转换开始请求标志 0：向上计数时未发生GTADTRB寄存器比较匹配。1：在递增计数中发生GTADTRB寄存器比较匹配。	R/W*1
19	ADTRBDF	GTADTRB寄存器比较匹配（递减计数）AD转换开始请求标志 0：递减计数时未发生GTADTRB寄存器比较匹配。1：向下计数时发生GTADTRB寄存器比较匹配。	R/W*1
23:20	—	这些位被读取为0。写入值应为0。	R/W
24	ODF	输出禁用标志 0：不产生输出禁止请求1：产生输出禁止请求	R
27:25	—	这些位被读取为0。写入值应为0。	R/W
28	DTEF	死区错误标志 0：未发生死区时间错误。1：发生死区时间错误。	R
29	OABHF	同时输出电平高标志 0：没有同时为GTIOCA和GTIOCB引脚生成1。 1：GTIOCA和GTIOCB引脚同时产生1。	R
30	OABLF	同时输出电平低标志 0：没有同时为GTIOCA和GTIOCB引脚生成0。 1：GTIOCA和GTIOCB引脚同时产生0。	R
31	PCF*2	周期计数功能完成标志 0：未发生周期计数功能完成1：已发生周期计数功能完成	R/W*1

注1.该位只能写入0。不要写1。
清除ADTRAUF、ADTRADF、ADTRBUF或ADTRBDF标志时，请务必仅将0写入目标标志或用于清除的标志，并将1写入其他不用于清除的标志。
注2.该位仅在GPT320至GPT323中可用。
在GPT324到GPT329中，该位读取为0。写入值应为0。

GTST指示GPT的状态。

TCFA flag (Input Capture/Compare Match Flag A)

The TCFA flag indicates the status for the input capture or compare match of GTCCRA.

[Setting conditions]

- GTCNT = GTCCRA, when the GTCCRA register functions as a compare match register
- GTCNT counter value is transferred to GTCCRA by the input capture signal when the GTCCRA register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFB flag (Input Capture/Compare Match Flag B)

The TCFB flag indicates the status for the input capture or compare match of GTCCRB.

[Setting conditions]

- GTCNT = GTCCRB, when the GTCCRB register functions as a compare match register
- GTCNT counter value is transferred to GTCCRB by the input capture signal when the GTCCRB register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFC flag (Input Compare Match Flag C)

The TCFC flag indicates the status for the compare match of GTCCRC.

When GTCCRC performs buffer operation, GTCCRC doesn't perform compare match.

[Setting condition]

- GTCNT = GTCCRC.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (GTCCRC performs buffer operation).

TCFD flag (Input Compare Match Flag D)

The TCFD flag indicates the status for the compare match of GTCCRD.

When GTCCRD performs buffer operation, GTCCRD doesn't perform compare match.

[Setting condition]

- GTCNT = GTCCRD.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (GTCCRD performs buffer operation).

TCFA标志（输入捕捉比较匹配标志A）

TCFA标志指示GTCCRA的输入捕获或比较匹配的状态。

[Setting conditions]

●GTCNT=GTCCRA，当GTCCRA寄存器用作比较匹配寄存器时

●当GTCCRA寄存器用作输入捕捉寄存器时，GTCNT计数器值通过输入捕捉信号传送到GTCCRA。

[Clearing condition]

●0写入此标志。

TCFB标志（输入捕捉比较匹配标志B）

TCFB标志指示GTCCRB的输入捕获或比较匹配的状态。

[Setting conditions]

●GTCNT=GTCCRB，当GTCCRB寄存器用作比较匹配寄存器时

●当GTCCRB寄存器用作输入捕捉寄存器时，GTCNT计数器值通过输入捕捉信号传送到GTCCRB。

[Clearing condition]

●0写入此标志。

TCFC标志（输入比较匹配标志C）

TCFC标志指示GTCCRC比较匹配的状态。

当GTCCRC执行缓冲操作时，GTCCRC不执行比较匹配。

[Setting condition]

- GTCNT = GTCCRC.

[Clearing condition]

●0写入此标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)

●GTBER.CCRA[1:0]=01b 10b 11b（GTCCRC执行缓冲操作）。

TCFD标志（输入比较匹配标志D）

TCFD标志指示GTCCRD比较匹配的状态。

当GTCCRD执行缓冲操作时，GTCCRD不执行比较匹配。

[Setting condition]

- GTCNT = GTCCRD.

[Clearing condition]

●0写入此标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)

●GTBER.CCRA[1:0]=10b 11b（GTCCRD执行缓冲操作）。

TCFE flag (Input Compare Match Flag E)

The TCFE flag indicates the status for the compare match of GTCCRE.

When GTCCRE performs buffer operation, GTCCRE doesn't perform compare match.

[Setting condition]

- GTCNT = GTCCRE.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (GTCCRE performs buffer operation).

TCFF flag (Input Compare Match Flag F)

The TCFF flag indicates the status for the compare match of GTCCRF.

When GTCCRF performs buffer operation, GTCCRF doesn't perform compare match.

[Setting condition]

- GTCNT = GTCCRF.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (GTCCRF performs buffer operation).

TCFPO flag (Overflow Flag)

The TCFPO flag indicates when an overflow or crest has occurred.

[Setting conditions]

- In saw-wave mode, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred
- In triangle-wave mode, a crest (GTCNT changes from GTPR to GTPR - 1) has occurred
- In counting by hardware sources, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred.

[Clearing condition]

- 0 is written to this flag.

TCFPU flag (Underflow Flag)

The TCFPU flag indicates when an underflow or trough has occurred.

[Setting conditions]

- In saw-wave mode, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred
- In triangle-wave mode, a trough (GTCNT changes from 0 to 1) has occurred
- In counting by hardware sources, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred.

[Clearing condition]

- 0 is written to this bit.

TCFE标志（输入比较匹配标志E）

TCFE标志指示GTCCRE比较匹配的状态。

当GTCCRE执行缓冲操作时，GTCCRE不执行比较匹配。

[Setting condition]

- GTCNT = GTCCRE.

[Clearing condition]

●0写入此标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)

●GTBER.CCRB[1:0]=01b 10b 11b（GTCCRE执行缓冲操作）。

TCFF标志（输入比较匹配标志F）

TCFF标志表示GTCCRF比较匹配的状态。

当GTCCRF执行缓冲操作时，GTCCRF不执行比较匹配。

[Setting condition]

- GTCNT = GTCCRF.

[Clearing condition]

●0写入此标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)

●GTBER.CCRB[1:0]=10b 11b（GTCCRF执行缓冲操作）。

TCFPO flag (Overflow Flag)

TCFPO标志指示何时发生溢出或波峰。

[Setting conditions]

●在锯齿波模式下，发生溢出（GTCNT在递增计数中从GTPR变为0）

●在三角波模式中，出现波峰（GTCNT从GTPR变为GTPR1）

●在硬件源的计数中，发生了溢出（GTCNT在递增计数中从GTPR变为0）。

[Clearing condition]

●0写入此标志。

TCFPU flag (Underflow Flag)

TCFPU标志指示何时发生下溢或波谷。

[Setting conditions]

●在锯齿波模式下，发生下溢（GTCNT在向下计数中从0变为GTPR）

●在三角波模式下，出现了一个波谷（GTCNT从0变为1）

●在硬件源计数中，发生了下溢（向下计数时GTCNT从0变为GTPR）。

[Clearing condition]

●0写入该位。

ITCNT[2:0] flag (GPTn_OVF/GPTn_UDF Interrupt Skipping Count Counter)

When the GPTn_OVF/GPTn_UDF interrupt skipping function is used (the GTITC.IVTC[1:0] bits are set to a value other than 00b), the counter is incremented by 1 every time the GPTn_OVF/GPTn_UDF interrupt source which is selected in GTITC.IVTC[1:0] is generated.

These bits are operated independently from the extended interrupt skipping by the GTEITC register.

[Clearing conditions]

- The GPTn_OVF/GPTn_UDF interrupt skipping function is not used (the GTITC.IVTT[2:0] bits are 000b when the IVTC[1:0] bits are 00b).
- The GPTn_OVF/GPTn_UDF interrupt skipping count matches the specified count (the ITCNT[2:0] bits match the skipping count specified by the IVTT[2:0] bits).
- When the count operation is stopped

TUCF flag (Count Direction Flag)

The TUCF flag indicates the count direction of GTCNT. In event count operation, this flag is set to 1 in up-counting and to 0 in down-counting.

ADTRAUF flag (GTADTRA Register Compare Match (Up-Counting) A/D Conversion Start Request Flag)

This status flag indicates generation of a GTADTRA register compare match in up-counting.

[Setting condition]

- The GTCNT counter matches the GTADTRA register in up-counting.

[Clearing condition]

- 0 is written to the ADTRAUF flag.

ADTRADF flag (GTADTRA Register Compare Match (Down-Counting) A/D Conversion Start Request Flag)

This status flag indicates generation of a GTADTRA register compare match in down-counting.

[Setting condition]

- The GTCNT counter matches the GTADTRA register in down-counting.

[Clearing condition]

- 0 is written to the ADTRADF flag.

ADTRBUF flag (GTADTRB Register Compare Match (Up-Counting) A/D Conversion Start Request Flag)

This status flag indicates generation of a GTADTRB register compare match in up-counting.

[Setting condition]

- The GTCNT counter matches the GTADTRB register in up-counting.

[Clearing condition]

- 0 is written to the ADTRBUF flag.

ADTRBDF flag (GTADTRB Register Compare Match (Down-Counting) A/D Conversion Start Request Flag)

This status flag indicates generation of a GTADTRB register compare match in down-counting.

[Setting condition]

- The GTCNT counter matches the GTADTRB register in down-counting.

[Clearing condition]

- 0 is written to the ADTRBDF flag.

ITCNT[2:0]标志（GPTn_OVFGPTn_UDF中断跳过计数计数器）

当使用GPTn_OVFGPTn_UDF中断跳过功能时（GTITC.IVTC[1:0]位设置为00b以外的值），每次在GTITC.IVTC中选择的GPTn_OVFGPTn_UDF中断源时计数器加1[1:0]生成。

这些位的操作独立于GTEITC寄存器的扩展中断跳过。

[Clearing conditions]

●不使用GPTn_OVFGPTn_UDF中断跳过功能（当IVTC[1:0]位为00b时GTITC.IVTT[2:0]位为000b）。

●GPTn_OVFGPTn_UDF中断跳过计数与指定计数匹配（ITCNT[2:0]位与IVTT[2:0]位指定的跳过计数匹配）。

●计数操作停止时

TUCF标志（计数方向标志）

TUCF标志表示GTCNT的计数方向。在事件计数操作中，该标志在递增计数时设置为1，在递减计数时设置为0。

ADTRAUF标志（GTADTRA寄存器比较匹配（向上计数）AD转换开始请求标志）

该状态标志指示在递增计数中产生了GTADTRA寄存器比较匹配。

[Setting condition]

●GTCNT计数器在递增计数时与GTADTRA寄存器匹配。

[Clearing condition]

●0写入ADTRAUF标志。

ADTRADF标志（GTADTRA寄存器比较匹配（递减计数）AD转换开始请求Flag)

该状态标志指示在递减计数中产生了GTADTRA寄存器比较匹配。

[Setting condition]

●GTCNT计数器与GTADTRA寄存器的递减计数相匹配。

[Clearing condition]

●0写入ADTRADF标志。

ADTRBUF标志（GTADTRB寄存器比较匹配（向上计数）AD转换开始请求标志）

该状态标志指示在递增计数中产生了GTADTRB寄存器比较匹配。

[Setting condition]

●GTCNT计数器在递增计数时与GTADTRB寄存器匹配。

[Clearing condition]

●0写入ADTRBUF标志。

ADTRBDF标志（GTADTRB寄存器比较匹配（递减计数）AD转换开始请求Flag)

该状态标志指示在递减计数中产生了GTADTRB寄存器比较匹配。

[Setting condition]

●GTCNT计数器与GTADTRB寄存器在递减计数时匹配。

[Clearing condition]

●0写入ADTRBDF标志。

ODF flag (Output Disable Flag)

The ODF flag shows the request of the output disable source group that is selected in the GRP[1:0] bits.

When output is disabled, an output disable control is not released within the same cycle in which an output disable request is negated. It is released in the next cycle.

DTEF flag (Dead Time Error Flag)

This flag indicates that the timer output toggle point after the automatic addition of dead time has exceeded the count period.

This flag returns to 0 when the timer output toggle point after the automatic addition of dead time is back within the period.

This flag can only be read from. (Writing 0 to clear the flag is not allowed.)

When the output disable request by the DTEF flag is enabled (when GTINTAD.GRPDTE bit is 1), the DTEF flag is output as the output disable request to the POEG. The GPT does not have a dead time error interrupt. Use the interrupt function in the POEG if this is necessary.

[Setting condition]

- When a change point of the waveform after the automatic setting of dead time has exceeded the count period (in the following cases).
  - Up-counting in triangle-wave mode:
    GTCCRA register – GTDVU register ≤ 0
  - Down-counting in triangle-wave mode:
    GTCCRA register – GTDVD register < 0
  - Up-counting in saw-wave one-shot pulse mode:
    GTCCRA register – GTDVU register < 0, or
    GTCCRA register + GTDVD register > GTPR register
  - Down-counting in saw-wave one-shot pulse mode:
    GTCCRA register + GTDVU register > GTPR register, or
    GTCCRA register - GTDVD register < 0

[Clearing condition]

- The timer output toggle point after the automatic addition of dead time is within the count period.

OABHF flag (Same Time Output Level High Flag)

The OABHF flag indicates that the GTIOCnA pin and GTIOCnB pin output 1 at the same time.

When the GTIOCnA or GTIOCnB pin outputs 0, this flag returns to 0. This flag is read only. Writing 0 to clear the flag is prohibited.

When the output disable request by the OABHF flag is enabled (GTINTAD.GRPABH = 1), the OABHF flag is output to POEG as an output disable request. The GPT does not have an interrupt to indicate that outputs have been simultaneous driven to the high level. Use the interrupt function in the POEG if this is necessary.

[Setting condition]

- The GTIOCnA and GTIOCnB pins output 1 at the same time when both OAE and OBE bits are set to 1.

[Clearing conditions]

- The GTIOCnA pin output value is different from the GTIOCnB pin output value when both OAE and OBE bits are set to 1
- The GTIOCnA and GTIOCnB pins output 0 at the same time when both OAE and OBE bits are set to 1
- Either the OAE bit or OBE bit is set to 0.

OABLF flag (Same Time Output Level Low Flag)

The OABLF flag indicates that the GTIOCnA and GTIOCnB pins output 0 at the same time.

When the GTIOCnA pin or GTIOCnB pin outputs 1, this flag returns to 0. This flag is read only. Writing 0 to clear the flag is prohibited.

ODF标志（输出禁用标志）

ODF标志显示在GRP[1:0]位中选择的输出禁用源组的请求。

当输出禁用时，输出禁用控制不会在输出禁用请求被否定的同一周期内释放。它在下一个周期中发布。

DTEF标志（死区错误标志）

该标志表示自动添加死区时间后的定时器输出切换点已超过计数周期。

当自动添加死区时间后的定时器输出切换点回到该周期内时，该标志返回0。

这个标志只能被读取。（不允许写入0来清除标志。）

当DTEF标志的输出禁用请求被启用时（当GTINTAD.GRPDTE位为1时），DTEF标志作为输出禁用请求输出到POEG。GPT没有死区时间错误中断。如有必要，请使用POEG中的中断功能。

[Setting condition]

●死区时间自动设置后的波形变化点超过计数周期时（以下情况）。

- Up-counting in triangle-wave mode:
  GTCCRA register – GTDVU register ≤ 0

三角波模式下的递减计数：GTCCRA寄存器 GTDVD寄存器<0

锯波单次脉冲模式中的递增计数：GTCCRA寄存器 GTDVU寄存器<0，或
GTCCRA register + GTDVD register > GTPR register

锯波单发脉冲模式下的递减计数：
GTCCRA寄存器+GTDVU寄存器>GTPR寄存器，或
GTCCRA register - GTDVD register < 0

[Clearing condition]

●自动添加死区时间后的定时器输出切换点在计数周期内。

OABHF标志（同时输出电平高标志）

OABHF标志表示GTIOCnA引脚和GTIOCnB引脚同时输出1。

当GTIOCnA或GTIOCnB引脚输出0时，该标志返回0。该标志为只读。禁止写入0清除标志。

当OABHF标志的输出禁用请求被启用(GTINTAD.GRPABH=1)时，OABHF标志作为输出禁用请求输出到POEG。GPT没有中断来指示输出已同时驱动为高电平。如有必要，请使用POEG中的中断功能。

[Setting condition]

●当OAE和OBE位都设置为1时，GTIOCnA和GTIOCnB引脚同时输出1。

[Clearing conditions]

●当OAE和OBE位都设置为1时，GTIOCnA引脚输出值与GTIOCnB引脚输出值不同

●当OAE和OBE位都设置为1时，GTIOCnA和GTIOCnB引脚同时输出0

●OAE位或OBE位设置为0。

OABLF标志（同时输出电平低标志）

OABLF标志表示GTIOCnA和GTIOCnB管脚同时输出0。

当GTIOCnA引脚或GTIOCnB引脚输出1时，该标志返回0。该标志为只读。禁止写入0清除标志。

When the output disable request by the OABLF flag is enabled (GTINTAD.GRPABL = 1), the OABLF flag is output to POEG as an output disable request. The GPT does not have an interrupt to indicate that outputs have been simultaneous driven to the low level. Use the interrupt function in the POEG if this is necessary.

[Setting condition]

- The GTIOCnA and GTIOCnB pins output 0 at the same time when both OAE and OBE bits are set to 1.

[Clearing conditions]

- The GTIOCnA pin output value is different from the GTIOCnB pin output value when both OAE and OBE bits are set to 1
- The GTIOCnA and GTIOCnB pins output 1 at the same time when both OAE and OBE bits are set to 1
- Either the OAE bit or the OBE bit is set to 0.

The compare-target signals to generate the OABHF/OABLF flag are the compare match outputs (PWM outputs) signals before they are masked by the output disable function. Even during the output disable condition, compare match operation continues internally, where the OABHF or OABLF flag is updated based on the operation results.

PCF flag (Period Count Function Finish Flag)

This bit is status flag of period count function finish.

[Setting condition]

- The GTPC.PCEN bit is 1 and the GTPC.PCNT counter is 1 at the end of cycle.
- The GTPC.PCEN bit is 1 and the GTPC.PCNT counter is 0 at the count clock.

[Clearing condition]

- 0 is written to this bit.

21.2.17 GTBER : General PWM Timer Buffer Enable Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	DBRTECB	—	DBRTECA	—	—	—	—	BD3	BD2	BD1	BD0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BD0	GTCCR Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
1	BD1	GTPR Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W*1
2	BD2	GTADTRA/GTADTRB Registers Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
3	BD3	GTDVU/GTDVD Registers Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

当启用OABLF标志的输出禁用请求时(GTINTAD.GRPABL=1)，OABLF标志作为输出禁用请求输出到POEG。GPT没有中断来指示输出已同时驱动为低电平。如有必要，请使用POEG中的中断功能。

[Setting condition]

●当OAE和OBE位都设置为1时，GTIOCnA和GTIOCnB引脚同时输出0。

[Clearing conditions]

●当OAE和OBE位都设置为1时，GTIOCnA引脚输出值与GTIOCnB引脚输出值不同

●当OAE和OBE位都设置为1时，GTIOCnA和GTIOCnB管脚同时输出1

●OAE位或OBE位都设置为0。

生成OABHFOABLF标志的比较目标信号是比较匹配输出（PWM输出）信号，在它们被输出禁用功能屏蔽之前。即使在输出禁用条件下，比较匹配操作也会在内部继续进行，其中OABHF或OABLF标志会根据操作结果进行更新。

PCF标志（周期计数功能完成标志）

该位是周期计数功能完成的状态标志。

[Setting condition]

●GTPC.PCEN位为1，GTPC.PCNT计数器在周期结束时为1。

●GTPC.PCEN位为1，GTPC.PCNT计数器在计数时钟为0。

[Clearing condition]

●0写入该位。

21.2.17 GTBER:通用PWM定时器缓冲器使能寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	DBRTECB	—	DBRTECA	—	—	—	—	BD3	BD2	BD1	BD0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BD0	GTCCR缓冲区操作禁用 0：启用缓冲操作1：禁用缓冲操作	R/W
1	BD1	GTPR缓冲区操作禁用 0：启用缓冲操作1：禁用缓冲操作	R/W*1
2	BD2	GTADTRAGTADTRB寄存器缓冲区操作禁用 0：启用缓冲操作1：禁用缓冲操作	R/W
3	BD3	GTDVUGTDVD寄存器缓冲区操作禁用 0：启用缓冲操作1：禁用缓冲操作	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
8	DBRTECA	GTCCRA Register Double Buffer Repeat Operation Enable 0: GTCCRA register double buffer repeat operation is disabled 1: GTCCRA register double buffer repeat operation is enabled	R/W
9	—	This bit is read as 0. The write value should be 0.	R/W
10	DBRTECB	GTCCRB Register Double Buffer Repeat Operation Enable 0: GTCCRB register double buffer repeat operation is disabled 1: GTCCRB register double buffer repeat operation is enabled	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W
17:16	CCRA[1:0]	GTCCRA Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTCCRA ↔GTCCRC) Others: Double buffer operation (GTCCRA ↔ GTCCRC ↔ GTCCRD)	R/W
19:18	CCRB[1:0]	GTCCRB Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTCCRB ↔ GTCCRE) Others: Double buffer operation (GTCCRB ↔ GTCCRE ↔ GTCCRF)	R/W
21:20	PR[1:0]	GTPR Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTPBR → GTPR) Others: Double buffer operation (GTPDBR → GTPBR → GTPR)	R/W
22	CCRSWT	GTCCRA and GTCCRB Forcible Buffer Operation Writing 1 to this bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after 1 is written. This bit is read as 0.	W
23	—	This bit is read as 0. The write value should be 0.	R/W
25:24	ADTTA[1:0]	GTADTRA Register Buffer Transfer Timing Select 0 0: In triangle wave or complementary PWM mode, no transfer. In saw-wave mode, no transfer. 0 1: In triangle wave or complementary PWM mode, transfer at crest. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing. 1 0: In triangle wave or complementary PWM mode, transfer at trough. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing. 1 1: In triangle wave or complementary PWM mode, transfer at both crest and trough. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing.	R/W
26	ADTDA	GTADTRA Register Double Buffer Operation 0: Single buffer operation (GTADTBRA → GTADTRA) 1: Double buffer operation (GTADTDBRA → GTADTBRA → GTADTRA)	R/W
27	—	This bit is read as 0. The write value should be 0.	R/W
29:28	ADTTB[1:0]	GTADTRB Register Buffer Transfer Timing Select 0 0: In triangle wave or complementary PWM mode, no transfer. In saw-wave mode, no transfer. 0 1: In triangle wave or complementary PWM mode, transfer at crest. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing. 1 0: In triangle wave or complementary PWM mode, transfer at trough. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing. 1 1: In triangle wave or complementary PWM mode, transfer at both crest and trough. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing.	R/W
30	ADTDB	GTADTRB Register Double Buffer Operation 0: Single buffer operation (GTADTBRB → GTADTRB) 1: Double buffer operation (GTADTDBRB → GTADTBRB → GTADTRB)	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.

Bit	Symbol	Function	R/W
8	DBRTECA	GTCCRA寄存器双缓冲区重复操作使能 0：禁止GTCCRA寄存器双缓冲重复操作1：使能GTCCRA寄存器双缓冲重复操作	R/W
9	—	该位读取为0。写入值应为0。	R/W
10	DBRTECB	GTCCRB寄存器双缓冲区重复操作使能 0：禁止GTCCRB寄存器双缓冲重复操作1：使能GTCCRB寄存器双缓冲重复操作	R/W
15:11	—	这些位被读取为0。写入值应为0。	R/W
17:16	CCRA[1:0]	GTCCRA缓冲区操作 00：无缓冲操作01：单缓冲操作（GTCCRA↔GTCCRC） 其他：双缓冲操作（GTCCRA↔GTCCRC↔GTCCRD）	R/W
19:18	CCRB[1:0]	GTCCRB缓冲区操作 00：无缓冲操作01：单缓冲操作（GTCCRB↔GTCCRE） 其他：双缓冲操作（GTCCRB↔GTCCRE↔GTCCRF）	R/W
21:20	PR[1:0]	GTPR缓冲区操作 00：无缓冲操作01：单缓冲操作（GTPBR→GTPR） 其他：双缓冲操作（GTPDBR→GTPBR→GTPR）	R/W
22	CCRSWT	GTCCRA和GTCCRB强制缓冲区操作向该位写入1会强制GTCCRA和GTCCRB进行缓冲区传输。该位在写入1后自动返回0。该位读为0。	W
23	—	该位读取为0。写入值应为0。	R/W
25:24	ADTTA[1:0]	GTADTRA寄存器缓冲区传输时序选择 00：在三角波或互补PWM模式下，不传输。在锯波模式下，没有传输。 01：在三角波或互补PWM模式下，在波峰传输。 在锯齿波模式下，在下溢（向下计数）、溢出（向上计数）或计数器清零时传输。 10：在三角波或互补PWM模式下，在波谷转换。 在锯齿波模式下，在下溢（向下计数）、溢出（向上计数）或计数器清零时传输。 11：在三角波或互补PWM模式下，波峰和波谷都传输。在锯齿波模式下，在下溢（递减计数）、溢出（递增计数）或计数器清零时传输。	R/W
26	ADTDA	GTADTRA寄存器双缓冲区操作 0：单缓冲操作（GTADTBRA→GTADTRA）1：双缓冲操作（GTADTBRA→GTADTBRA→GTADTRA）	R/W
27	—	该位读取为0。写入值应为0。	R/W
29:28	ADTTB[1:0]	GTADTRB寄存器缓冲区传输时序选择 00：在三角波或互补PWM模式下，不传输。在锯波模式下，没有传输。 01：在三角波或互补PWM模式下，在波峰传输。 在锯齿波模式下，在下溢（向下计数）、溢出（向上计数）或计数器清零时传输。 10：在三角波或互补PWM模式下，在波谷转换。 在锯齿波模式下，在下溢（向下计数）、溢出（向上计数）或计数器清零时传输。 11：在三角波或互补PWM模式下，波峰和波谷都传输。在锯齿波模式下，在下溢（递减计数）、溢出（递增计数）或计数器清零时传输。	R/W
30	ADTDB	GTADTRB寄存器双缓冲操作 0：单缓冲操作（GTADTBRB→GTADTRB）1：双缓冲操作（GTADTDBRB→GTADTBRB→GTADTRB）	R/W
31	—	该位读取为0。写入值应为0。	R/W

注1.在互补PWM模式下，无论写入主通道从通道1从通道2的哪个寄存器，都会同时写入三个通道。

The GTBER register provides settings for the buffer operation. Set the GTBER register except the BDx (x = 0 to 3) bits while the GTCNT counter is stopped.

BD0 bit (GTCCR Buffer Operation Disable)

The BD0 bit disables the buffer operation using GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, and GTCCRF combined.

When GTDTCR.TDE is 1 and when BD0 is set to 0, GTCCRB does not perform buffer operation in Saw-wave one-shot pulse mode or Triangle-wave PWM mode. The GTCCRB register is automatically set to a compare match value for negative-phase waveform with dead time.

In complementary PWM mode, it is valid only for the buffer operation of GTCCRC register and GTCCRE register. The buffer operation of GTCCRA registers can not be disabled. Buffer operation of GTCCRE register and GTCCRF register is enabled/disabled by CP3DB bit of GTBER2 register. No buffer transfer to GTCCRB is performed in complementary PWM mode.

A value for the BD0 bit in the channel related to the position of the bit written with 1 by the GTSECSR register can be set when 1 is written to the GTSECR.SBDCE or GTSECR.SBDCD.

When the DBRTECm (m = A, B) bit is 1, setting the BD0 bit to 1 while the mode of operation is saw-wave one-shot pulse mode or triangle-wave PWM mode 3 results in transfer from the intermediate buffer to the GTCCRm register.

BD1 bit (GTPR Buffer Operation Disable)

The BD1 bit disables the buffer operation using GTPR, GTPDBR, and GTPBR combined.

A value for the BD1 bit in the channel related to the position of the bit written with 1 by the GTSECSR register can be set when 1 is written to the GTSECR.SBDPE or GTSECR.SBDPD.

In complementary PWM mode, the slave channel is also controlled by setting the BD1 bit of the master channel.

BD2 bit (GTADTRA/GTADTRB Registers Buffer Operation Disable)

This bit disables buffer operation using the GTADTRA, GTADTBRA, and GTADTDBRA registers together and buffer operation using the GTADTRB, GTADTBRB, and GTADTDBRB registers together.

The setting is invalid during the event count operation, and the buffer operation using the GTADTRA and GTADTRB registers is not performed.

A value for the BD2 bit in the channel related to the position of the bit written with 1 by the GTSECSR register can be set when 1 is written to the SBDAE or SBDAD bit in the GTSECR register.

BD3 bit (GTDVU/GTDVD Registers Buffer Operation Disable)

In Saw-wave PWM mode 1, Saw-wave one-shot pulse mode or Triangle-wave PWM mode, this bit disables buffer operation using the GTDVU and GTDBU registers together and buffer operation using the GTDVD and GTDBD registers together.

Even though the BD3 bit is set to 0, buffer operation in the GTDVD register is not performed if the GTDTCR.TDFER bit is set to 1. Instead, the value in the GTDVU register is set automatically.

In Saw-wave PWM mode 2 or complementary PWM mode, this bit is invalid and GTDVU and GTDVD registers don't perform buffer operation.

The setting is invalid during the event count operation, and the buffer operation using the GTDVU and GTDVD registers is not performed.

A value for the BD3 bit in the channel related to the position of the bit written with 1 by the GTSECSR register can be set when 1 is written to the SBDDE or SBDDD bit in the GTSECR register.

DBRTECm bits (GTCCRm Register Double Buffer Repeat Operation Enable) (m = A,B)

This setting enables the operation to repeat a transfer to the GTCCRm register from the intermediate buffer by cycle during the buffer transfer disable period when performing the double buffer operation using the GTCCRm register.

It is valid in saw-wave one-shot pulse mode and triangle-wave PWM mode 3.

The disabling period of buffer transfer indicates the period that buffer transfer is stopped by setting of the BD0 bit (CPU writing or simultaneous buffer operation control by the GTSECSR register) and the period for buffer transfer extended skipping (except the case for skipping by counting both crests and troughs) by the GTEITLB register.

GTBER寄存器提供缓冲区操作的设置。当GTCNT计数器停止时，设置除BDx（x=0到3）位之外的GTBER寄存器。

BD0位（GTCCR缓冲区操作禁用）

BD0位使用GTCCRA、GTCCRB、GTCCRC、GTCCRD、GTCCRE和GTCCRF组合禁用缓冲区操作。

当GTDTCR.TDE为1且BD0设置为0时，GTCCRB在Saw-waveone-shot脉冲模式或Triangle-wavePWM模式下不进行缓冲操作。GTCCRB寄存器自动设置为带有死区时间的负相位波形的比较匹配值。

在互补PWM模式下，仅对GTCCRC寄存器和GTCCRE寄存器的缓冲操作有效。GTCCRA寄存器的缓冲操作不能被禁用。GTCCRE寄存器和GTCCRF寄存器的缓冲操作由GTBER2寄存器的CP3DB位使能禁用。在互补PWM模式下，没有缓冲区传输到GTCCRB。

当向GTSECR.SBDCE或GTSECR.SBDCD写入1时，可以设置与由GTSECSR寄存器写入1的位的位置相关的通道中的BD0位的值。

当DBRTECm(m=A B)位为1时，将BD0位设置为1，而操作模式为锯齿波单次脉冲模式或三角波PWM模式3会导致从中间缓冲器传输到GTCCRm寄存器。

BD1位（GTPR缓冲区操作禁用）

BD1位禁用使用GTPR、GTPDBR和GTPBR组合的缓冲区操作。

当向GTSECR.SBDPE或GTSECR.SBDPD写入1时，可以设置与由GTSECSR寄存器写入1的位的位置相关的通道中的BD1位的值。

在互补PWM模式下，从通道也通过设置主通道的BD1位来控制。

BD2位（GTADTRAGTADTRB寄存器缓冲区操作禁用）

该位禁用一起使用GTADTRA、GTADTBRA和GTADTBRA寄存器的缓冲操作以及一起使用GTADTRB、GTADTBRB和GTADTDBRB寄存器的缓冲操作。

该设置在事件计数操作期间无效，并且不执行使用GTADTRA和GTADTRB寄存器的缓冲操作。

在GTSECR寄存器的SBDAE或SBDAD位写入1时，可以设置与GTSECSR寄存器写入1的位的位置相关的通道中BD2位的值。

BD3位（GTDVUGTDVD寄存器缓冲区操作禁用）

在Saw-wavePWM模式1、Saw-waveone-shot脉冲模式或三角波PWM模式下，该位禁用同时使用GTDVU和GTDBU寄存器的缓冲操作以及同时使用GTDVD和GTDBD寄存器的缓冲操作。

即使BD3位设置为0，如果GTDTCR.TDFER位设置为1，则不会执行GTDVD寄存器中的缓冲操作。而是自动设置GTDVU寄存器中的值。

在Saw-wavePWM模式2或互补PWM模式下，该位无效，GTDVU和GTDVD寄存器不执行缓冲操作。

事件计数操作期间设置无效，不执行使用GTDVU和GTDVD寄存器的缓冲操作。

在GTSECR寄存器的SBDDE或SBDDD位写入1时，可以设置与GTSECSR寄存器写入1的位的位置相关的通道中BD3位的值。

DBRTECm位（GTCCRm寄存器双缓冲区重复操作使能）（m=A B）

当使用GTCCRm寄存器执行双缓冲操作时，此设置允许操作在缓冲区传输禁用期间按周期从中间缓冲区重复传输到GTCCRm寄存器。

在锯齿波单发脉冲模式和三角波PWM模式3中有效。

缓冲传送禁止期间是指通过设置BD0位（CPU写入或由GTSECSR寄存器同时进行缓冲操作控制）而停止缓冲传送的期间和缓冲传送扩展跳过的期间（通过同时计数来跳过的情况除外）波峰和波谷）由GTEITLB寄存器。

When the DBRTECm bit is 1, writing by the CPU to the GTCCRm register sets the same value in temporary register x (x = C, E). The value of the GTCCRx (x = C, E) register is also transferred to the temporary register x (x = C, E) by forcible buffer transfer.

CCRA[1:0] bits (GTCCRA Buffer Operation)

The CCRA[1:0] bits set the buffer operation with GTCCRA, GTCCRC, and GTCCRD combined. When the buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.

The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (64-bit transfer at trough), or compementary PWM mode.

CCRB[1:0] bits (GTCCRB Buffer Operation)

The CCRB[1:0] bits set the buffer operation using GTCCRB, GTCCRE, and GTCCRF combined. When the buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.

The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (64-bit transfer at trough), or compementary PWM mode.

PR[1:0] bits (GTPR Buffer Operation)

The PR[1:0] bits set the buffer operation with GTPR, GTPDBR, and GTPBR combined.

The setting is invalid in complementary PWM mode. Buffer operation unique to complementary PWM mode is performed regardless of the setting value of the PR[1:0] bits.

CCRSWT bit (GTCCRA and GTCCRB Forcible Buffer Operation)

Writing 1 to the CCRSWT bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after the 1 is written. This bit is read as 0, and is valid only when counting is stopped with a compare match operation specified.

The setting is invalid in complementary PWM mode.

ADTTA[1:0] bits (GTADTRA Register Buffer Transfer Timing Select)

These bits set the transfer timing for buffer operation of the GTADTRA, GTADTBRA, and GTADTDBRA registers.

The setting is invalid during the event count operation.

ADTDA bit (GTADTRA Register Double Buffer Operation)

These bits set buffer operation with the GTADTRA, GTADTBRA, and GTADTDBRA registers combined.

The setting is invalid during the event count operation.

ADTTB[1:0] bits (GTADTRB Register Buffer Transfer Timing Select)

These bits set the transfer timing for buffer operation of the GTADTRB, GTADTBRB, and GTADTDBRB registers.

The setting is invalid during the event count operation.

ADTDB bit (GTADTRB Register Double Buffer Operation)

These bits set buffer operation with the GTADTRB, GTADTBRB, and GTADTDBRB registers combined.

The setting is invalid during the event count operation.

当DBRTECm位为1时，CPU写入GTCCRm寄存器会在临时寄存器x中设置相同的值（x= C、E)。GTCCRx(x=C E)寄存器的值也通过强制缓冲传输传送到临时寄存器x(x=C E)。

CCRA[1:0]位（GTCCRA缓冲区操作）

CCRA[1:0]位设置与GTCCRA、GTCCRC和GTCCRD组合的缓冲区操作。当缓冲操作受到GTCR中设置的操作模式限制时，GTCR设置优先。

缓冲器操作模式固定为锯齿波单次脉冲模式或三角波PWM模式3（波谷64位传输）或互补PWM模式。

CCRB[1:0]位（GTCCRB缓冲区操作）

CCRB[1:0]位使用GTCCRB、GTCCRE和GTCCRF组合设置缓冲区操作。当缓冲操作受到GTCR中设置的操作模式限制时，GTCR设置优先。

缓冲器操作模式固定为锯齿波单次脉冲模式或三角波PWM模式3（波谷64位传输）或互补PWM模式。

PR[1:0]位（GTPR缓冲区操作）

PR[1:0]位设置与GTPR、GTPDBR和GTPBR组合的缓冲区操作。

该设置在互补PWM模式下无效。无论PR[1:0]位的设置值如何，都会执行互补PWM模式特有的缓冲操作。

CCRSWT位（GTCCRA和GTCCRB强制缓冲操作）

向CCRSWT位写入1会强制GTCCRA和GTCCRB进行缓冲区传输。该位在写入1后自动返回0。该位读为0，仅当计数停止并指定比较匹配操作时才有效。

该设置在互补PWM模式下无效。

ADTTA[1:0]位（GTADTRA寄存器缓冲区传输时序选择）

这些位设置GTADTRA、GTADTBRA和GTADTBRA寄存器的缓冲操作的传输时序。

该设置在事件计数操作期间无效。

ADTDA位（GTADTRA寄存器双缓冲器操作）

这些位设置与GTADTRA、GTADTBRA和GTADTBRA寄存器相结合的缓冲区操作。

该设置在事件计数操作期间无效。

ADTTB[1:0]位（GTADTRB寄存器缓冲区传输时序选择）

这些位设置GTADTRB、GTADTBRB和GTADTDRBB寄存器的缓冲操作的传输时序。

该设置在事件计数操作期间无效。

ADTDB位（GTADTRB寄存器双缓冲区操作）

这些位设置与GTADTRB、GTADTBRB和GTADTDRBB寄存器相结合的缓冲区操作。

该设置在事件计数操作期间无效。

21.2.18 GTITC : General PWM Timer Interrupt and A/D Conversion Start Request Skipping Setting Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x44

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	ADTBL	—	ADTAL	—	IVTT[2:0]			IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ITLA	GTCCRA Register Compare Match/Input Capture Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
1	ITLB	GTCCRB Register Compare Match/Input Capture Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
2	ITLC	GTCCRC Register Compare Match Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
3	ITLD	GTCCRD Register Compare Match Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
4	ITLE	GTCCRE Register Compare Match Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
5	ITLF	GTCCRF Register Compare Match Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
7:6	IVTC[1:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Function Select 0 0: Skipping is not performed. 0 1: Both overflow and underflow for saw waves*1 and crest for triangle waves and complementary PWM mode are counted and skipped. 1 0: Both overflow and underflow for saw waves*1 and trough for triangle waves and complementary PWM mode are counted and skipped. 1 1: Both overflow and underflow for saw waves*1 and both crest and trough for triangle waves and complementary PWM mode are counted and skipped.	R/W
10:8	IVTT[2:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Count Select 0 0 0: Skipping is not performed 0 0 1: Skipping count of 1 0 1 0: Skipping count of 2 0 1 1: Skipping count of 3 1 0 0: Skipping count of 4 1 0 1: Skipping count of 5 1 1 0: Skipping count of 6 1 1 1: Skipping count of 7	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
12	ADTAL	GTADTRA Register A/D Conversion Start Request Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
13	—	This bit is read as 0. The write value should be 0.	R/W

21.2.18 GTITC：通用PWM定时器中断和AD转换开始请求跳过设置寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x44

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	ADTBL	—	ADTAL	—	IVTT[2:0]			IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ITLA	GTCCRA寄存器比较匹配输入捕捉中断链接 0：不与GPTn_OVFGPTn_UDF中断跳过功能联动。1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
1	ITLB	GTCCRB寄存器比较匹配输入捕捉中断链接 0：不与GPTn_OVFGPTn_UDF中断跳过功能联动。1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
2	ITLC	GTCCRC寄存器比较匹配中断链接 0：不与GPTn_OVFGPTn_UDF中断跳过功能联动。1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
3	ITLD	GTCCRD寄存器比较匹配中断链接 0：不与GPTn_OVFGPTn_UDF中断跳过功能联动。1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
4	ITLE	GTCCRE寄存器比较匹配中断链接 0：不与GPTn_OVFGPTn_UDF中断跳过功能联动。1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
5	ITLF	GTCCRF寄存器比较匹配中断链接 0：不与GPTn_OVFGPTn_UDF中断跳过功能联动。1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
7:6	IVTC[1:0]	GPTn_OVFGPTn_UDF中断跳过功能选择 00：不执行跳过。01:对锯齿波*1的上溢和下溢以及三角波和互补PWM模式的波峰进行计数和跳过。 10：锯齿波*1的上溢和下溢以及三角波和互补PWM模式的波谷都被计数和跳过。 11:对锯齿波*1的上溢和下溢以及三角波和互补PWM模式的波峰和波谷都进行计数和跳过。	R/W
10:8	IVTT[2:0]	GPTn_OVFGPTn_UDF中断跳过计数选择 000：不执行跳过001：跳过计数1010：跳过计数2011：跳过计数3100：跳过计数4101：跳过计数5110：跳过计数6111：跳过计数7	R/W
11	—	该位读取为0。写入值应为0。	R/W
12	ADTAL	GTADTRA寄存器AD转换开始请求链接 0：不与GPTn_OVFGPTn_UDF中断跳过功能联动。1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
13	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
14	ADTBL	GTADTRB Register A/D Conversion Start Request Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
31:15	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Saw-wave PWM mode 2 is not the target of this function.

The GTITC register sets the skipping function for the GTCNT counter overflow (GTPR compare match) interrupt (GPTn_OVF) and underflow interrupt (GPTn_UDF) and also sets whether to link the other interrupts and A/D conversion start requests with the GPTn_OVF/GPTn_UDF interrupt skipping function. Note the output disable request to POEG cannot be linked with the GPTn_OVF/GPTn_UDF interrupt skipping function. Additionally, if the interrupt skipping function is performed, the change in the status flag is also skipped.

The setting is invalid during the event count operation.

The setting is operated independently from the extended interrupt skipping by the GTEITC register.

ITLA bit (GTCCRA Register Compare Match/Input Capture Interrupt Link)

This bit specifies whether to link the GTCCRA compare match/input capture interrupt (GPTn_CCMPA) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLB bit (GTCCRB Register Compare Match/Input Capture Interrupt Link)

This bit specifies whether to link the GTCCRB compare match/input capture interrupt (GPTn_CCMPB) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLC bit (GTCCRC Register Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRC compare match interrupt (GPTn_CMPC) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLD bit (GTCCRD Register Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRD compare match interrupt (GPTn_CMPD) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLE bit (GTCCRE Register Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRE compare match interrupt (GPTn_CMPE) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLF bit (GTCCRF Register Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRF compare match interrupt (GPTn_CMPF) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

IVTC[1:0] bit (GPTn_OVF/GPTn_UDF Interrupt Skipping Function Select)

These bits set the skipping function for the GTPR compare match (GTCNT counter overflow) interrupt (GPTn_OVF) and GTCNT counter underflow interrupt (GPTn_UDF).

IVTT[2:0] bit (GPTn_OVF/GPTn_UDF Interrupt Skipping Count Select)

These bits set the skipping count for the GTPR compare match (GTCNT counter overflow) interrupt (GPTn_OVF) and GTCNT counter underflow interrupt (GPTn_UDF).

When modifying the IVTT[2:0] bits, first set the IVTC[1:0] bits to 00b.

ADTAL bit (GTADTRA Register A/D Conversion Start Request Link)

This bit specifies whether to link the GTADTRA A/D conversion start request, which is generated in response to a compare match with the GTCNT counter and the GTADTRA register, with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ADTBL bit (GTADTRB Register A/D Conversion Start Request Link)

This bit specifies whether to link the GTADTRB A/D conversion start request, which is generated in response to a compare match with the GTCNT counter and the GTADTRB register, with the GPTn_OVF/GPTn_UDF interrupt skipping function.

Bit	Symbol	Function	R/W
14	ADTBL	GTADTRB寄存器AD转换开始请求链接 0：不与GPTn_OVFGPTn_UDF中断跳过功能联动。1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
31:15	—	这些位被读取为0。写入值应为0。	R/W

注1.锯波PWM模式2不是该函数的目标。

GTITC寄存器设置GTCNT计数器溢出（GTPR比较匹配）中断（GPTn_OVF）和下溢中断（GPTn_UDF）的跳过功能，并设置是否将其他中断和AD转换开始请求与GPTn_OVFGPTn_UDF中断跳过功能链接。请注意，对POEG的输出禁用请求不能与GPTn_OVFGPTn_UDF中断跳过函数链接。此外，如果执行中断跳过功能，状态标志的变化也会被跳过。

该设置在事件计数操作期间无效。

该设置独立于GTEITC寄存器的扩展中断跳过操作。

ITLA位（GTCCRA寄存器比较匹配输入捕捉中断链接）

该位指定是否将GTCCRA比较匹配输入捕捉中断(GPTn_CCMPA)与GPTn_OVFGPTn_UDF中断跳过函数。

ITLB位（GTCCRB寄存器比较匹配输入捕捉中断链接）

该位指定是否将GTCCRB比较匹配输入捕捉中断(GPTn_CCMPB)与GPTn_OVFGPTn_UDF中断跳过函数。

ITLC位（GTCCRC寄存器比较匹配中断链接）

该位指定是否将GTCCRC比较匹配中断(GPTn_CMPC)与GPTn_OVFGPTn_UDF中断跳过功能链接。

ITLD位（GTCCRD寄存器比较匹配中断链接）

该位指定是否将GTCCRD比较匹配中断(GPTn_CMPD)与GPTn_OVFGPTn_UDF中断跳过功能链接。

ITLE位（GTCCRE寄存器比较匹配中断链接）

该位指定是否将GTCCRE比较匹配中断(GPTn_CMPE)与GPTn_OVFGPTn_UDF中断跳过功能链接。

ITLF位（GTCCRF寄存器比较匹配中断链接）

该位指定是否将GTCCRF比较匹配中断(GPTn_CMPF)与GPTn_OVFGPTn_UDF中断跳过功能链接。

IVTC[1:0]位（GPTn_OVFGPTn_UDF中断跳过功能选择）

这些位设置GTPR比较匹配（GTCNT计数器溢出）中断(GPTn_OVF)和GTCNT计数器下溢中断(GPTn_UDF)。

IVTT[2:0]位（GPTn_OVFGPTn_UDF中断跳过计数选择）

这些位设置GTPR比较匹配（GTCNT计数器溢出）中断(GPTn_OVF)和GTCNT计数器下溢中断(GPTn_UDF)。

修改IVTT[2:0]位时，首先将IVTC[1:0]位设置为00b。

ADTAL位（GTADTRA寄存器AD转换开始请求链接）

该位指定是否将GTADTRAAD转换开始请求与GPTn_OVFGPTn_UDF中断跳过功能链接，该请求是响应与GTCNT计数器和GTADTRA寄存器的比较匹配而产生的。

ADTBL位（GTADTRB寄存器AD转换开始请求链接）

该位指定是否将GTADTRBAD转换开始请求与GPTn_OVFGPTn_UDF中断跳过功能链接，该请求是响应与GTCNT计数器和GTADTRB寄存器的比较匹配而产生的。

21.2.19 GTCNT : General PWM Timer Counter

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x48

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	GTCNT is a 32-bit read/write counter for GPT32n (n = 0 to 9). GTCNT can only be written to after counting stops. Access in 8-bit or 16-bit units to the GTCNT counter is prohibited, and it should be accessed in 32-bit units. In saw waves or triangle waves, GTCNT must be set within the range of 0 ≤ GTCNT ≤ GTPR.	R/W

21.2.20 GTCCRk : General PWM Timer Compare Capture Register k (k = A to F)

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x4C (GTCCRA)
0x50 (GTCCRB)
0x54 (GTCCRC)
0x58 (GTCCRE)
0x5C (GTCCRD)
0x60 (GTCCRF)

Bit position:	31																												0
Bit field:																													
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTCCRk registers are read/write registers. Access in 8-bit or 16-bit units to the GTCCRk register is prohibited, and it should be accessed in 32-bit units. GTCCRA and GTCCRB are registers used for both output compare and input capture. GTCCRC and GTCCRE are compare match registers, and can also function as buffer registers for GTCCRA and GTCCRB. GTCCRD and GTCCRF are compare match registers, and can also function as buffer registers for GTCCRC and GTCCRE (double-buffer registers for GTCCRA and GTCCRB).	R/W

21.2.21 GTPR : General PWM Timer Cycle Setting Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x64

Bit position:	31																												0
Bit field:																													
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

21.2.19 GTCNT:通用PWM定时器计数器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x48

Bit position:	31																												0
Bit field:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	GTCNT是GPT32n（n=0到9）的32位读写计数器。GTCNT只能在计数停止后写入。禁止以8位或16位为单位访问GTCNT计数器，应以32位为单位进行访问。在锯齿波或三角波中，GTCNT必须设置在0≤GTCNT≤范围内 GTPR.	R/W

21.2.20 GTCCRk:通用PWM定时器比较捕捉寄存器k(k=AtoF)

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x4C (GTCCRA)
0x50 (GTCCRB)
0x54 (GTCCRC)
0x58 (GTCCRE)
0x5C (GTCCRD)
0x60 (GTCCRF)

Bit position:	31																												0
Bit field:																													
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTCCRk寄存器是读写寄存器。禁止以8位或16位为单位访问GTCCRk寄存器，应以32位为单位进行访问。GTCCRA和GTCCRB是用于输出比较和输入捕捉的寄存器。GTCCRC和GTCCRE是比较匹配寄存器，也可以作为GTCCRA和GTCCRB的缓冲寄存器。GTCCRD和GTCCRF是比较匹配寄存器，也可以作为GTCCRC和GTCCRE的缓冲寄存器（GTCCRA和GTCCRB的双缓冲寄存器）。	R/W

21.2.21 GTPR：通用PWM定时器周期设置寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x64

Bit position:	31																												0
Bit field:																													
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPR is a read/write register that sets the maximum count value of GTCNT. Access in 8-bit or 16-bit units to the GTPR register is prohibited, and it should be accessed in 32-bit units. The setting is invalid in the Saw-wave PWM mode 2. For Saw waves except the Saw-wave PWM mode 2, the value of (GTPR + 1) is the cycle. For triangle waves or complementary PWM mode, the value of (GTPR value × 2) is the cycle. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.	R/W

21.2.22 GTPBR : General PWM Timer Cycle Setting Buffer Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x68

Bit position:	31																												0
Bit field:																													
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPBR is a read/write register that functions as a buffer register for GTPR. Access in 8-bit or 16-bit units to the GTPBR register is prohibited, and it should be accessed in 32-bit units. The setting is invalid in Saw-wave PWM mode 2. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.	R/W

21.2.23 GTPDBR : General PWM Timer Cycle Setting Double-Buffer Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x6C

Bit position:	31																												0
Bit field:																													
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	The buffer register for the GTPBR register (double buffer register for the GTPR register) Access in 8-bit or 16-bit units to the GTPDBR register is prohibited, and it should be accessed in 32-bit units. The setting is invalid in Saw-wave PWM mode 2. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.	R/W

21.2.24 GTADTRk : A/D Conversion Start Request Timing Register k (k = A, B)

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x70 (GTADTRA)
0x7C (GTADTRB)

Bit position:	31																												0
Bit field:																													
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPR是一个读写寄存器，设置GTCNT的最大计数值。禁止以8位或16位为单位访问GTPR寄存器，应以32位为单位进行访问。在Saw-wavePWM模式2中设置无效。对于Saw-wave以外的Saw PWM模式2，(GTPR+1)的值为周期。对于三角波或互补 PWM模式下，（GTPR值×2）的值为周期。 在互补PWM模式下，无论写入主通道从通道1从通道2的哪个寄存器，都会同时写入三个通道。	R/W

21.2.22 GTPBR:通用PWM定时器周期设置缓冲寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x68

Bit position:	31																												0
Bit field:																													
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPBR是一个读写寄存器，用作GTPR的缓冲寄存器。禁止以8位或16位为单位访问GTPBR寄存器，应以32位为单位进行访问。Saw-wavePWM模式2设置无效。 在互补PWM模式下，无论写入主通道从通道1从通道2的哪个寄存器，都会同时写入三个通道。	R/W

21.2.23 GTPDBR:通用PWM定时器周期设置双缓冲寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x6C

Bit position:	31																												0
Bit field:																													
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPBR寄存器的缓冲寄存器（GTPR寄存器的双缓冲寄存器） 禁止以8位或16位为单位访问GTPDBR寄存器，应以32位为单位进行访问。Saw-wavePWM模式2设置无效。 在互补PWM模式下，无论写入主通道从通道1从通道2的哪个寄存器，都会同时写入三个通道。	R/W

21.2.24 GTADTRk:AD转换开始请求时序寄存器k(k=A B)

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x70 (GTADTRA)
0x7C (GTADTRB)

Bit position:	31																												0
Bit field:																													
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	Set the timing of A/D conversion start request generation Access in 8-bit or 16-bit units to the GTADTRk register is prohibited, and it should be accessed in 32-bit units. When the GTADTRk register value matches the GTCNT counter value, an A/D conversion start request is generated. In complementary PWM mode, A/D conversion start request is generated when the GTCNT counter of the master channel matches this register.	R/W

21.2.25 GTADTBRk : A/D Conversion Start Request Timing Buffer Register k (k = A, B)

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x74 (GTADTBRA)
0x80 (GTADTBRB)

Bit position:	31																												0
Bit field:																													
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	The buffer registers for the GTADTRk register Access in 8-bit or 16-bit units to the GTADTBRk register is prohibited, and it should be accessed in 32-bit units.	R/W

21.2.26 GTADTDBRk : A/D Conversion Start Request Timing Double-Buffer Register k (k = A, B)

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x78 (GTADTDBRA)
0x84 (GTADTDBRB)

Bit position:	31																												0
Bit field:																													
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	The buffer registers for the GTADTBRk register (double buffer registers for the GTADTRk register) Access in 8-bit or 16-bit units to the GTADTDBRk register is prohibited, and it should be accessed in 32-bit units.	R/W

21.2.27 GTDTCR : General PWM Timer Dead Time Control Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x88

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TDFER	—	—	TDBDE	TDBUE	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	设置AD转换开始请求生成的时序 禁止以8位或16位为单位访问GTADTRk寄存器，应以32位为单位进行访问。当GTADTRk寄存器值与GTCNT计数器值匹配时，会产生AD转换开始请求。在互补PWM模式下，当主通道的GTCNT计数器与该寄存器匹配时，会产生AD转换开始请求。	R/W

21.2.25 GTADTBRk:AD转换开始请求时序缓冲寄存器k(k=A B)

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x74 (GTADTBRA)
0x80 (GTADTBRB)

Bit position:	31																												0
Bit field:																													
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTADTRk寄存器的缓冲寄存器 禁止以8位或16位为单位访问GTADTBRk寄存器，应以32位为单位进行访问。	R/W

21.2.26 GTADTDBRk:AD转换开始请求时序双缓冲寄存器k(k=A B)

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x78 (GTADTDBRA)
0x84 (GTADTDBRB)

Bit position:	31																												0
Bit field:																													
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTADTDBRk寄存器的缓冲寄存器（GTADTRk寄存器的双缓冲寄存器）禁止以8位或16位为单位访问GTADTDBRk寄存器，应以32位为单位进行访问。	R/W

21.2.27 GTDTCR:通用PWM定时器死区时间控制寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x88

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TDFER	—	—	TDBDE	TDBUE	—	—	—	TDE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDE	Negative-Phase Waveform Setting 0: GTCCRB is set without using GTDVU and GTDVD 1: GTDVU and GTDVD are used to set the compare match value for negative-phase waveform with dead time automatically in GTCCRB	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	TDBUE	GTDVU Register Buffer Operation Enable 0: GTDVU register buffer operation is disabled 1: GTDVU register buffer operation is enabled	R/W
5	TDBDE	GTDVD Register Buffer Operation Enable 0: GTDVD register buffer operation is disabled 1: GTDVD register buffer operation is enabled	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
8	TDFER	GTDVD Register Setting 0: GTDVU and GTDVD registers are set separately. 1: The value written to GTDVU register is automatically set to GTDVD register.	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

GTDTCR enables automatic setting of a compare match value for negative-phase waveform with dead time. GPT has a dead time control function and GTDVU and GTDVD registers are used for setting dead time value.

This register is invalid in Saw-wave PWM mode 2 or complementary PWM mode.

The setting is invalid during the event count operation.

TDE bit (Negative-Phase Waveform Setting)

The TDE bit specifies whether to use GTDVU and GTDVD. When GTDVU and GTDVD are used, the compare match value for a negative-phase waveform with dead time obtained by the compare match value of a positive-phase waveform (GTCCRA) and the dead time value (GTDVU and GTDVD) is automatically set in GTCCRB.

The TDE bit setting is ignored in saw-wave PWM mode, and the GTCCRB is not automatic setting.

The GTCCRB value is automatically set and has the following upper and lower limit values. If the obtained GTCCRB value is not within the upper or lower limit, the following limit value is set in GTCCRB, and GTST.DTEF flag becomes 1. However, if the obtained GTCCRB value exceeds the upper limit in triangle-wave PWM mode, DTEF flag becomes 0.

- Triangle waves:
  Upper limit value: GTPR − 1
  Lower limit value: 1 in up-counting, 0 in down-counting
- Saw-wave one-shot pulse mode:
  Upper limit value: GTPR
  Lower limit value: 0.

TDBUE bit (GTDVU Register Buffer Operation Enable)

This bit enables buffer operation with the GTDVU and GTDBU registers combined.

The timing of buffer transfer is at troughs in triangle-wave mode, and at overflows or underflows in saw-wave mode.

TDBDE bit (GTDVD Register Buffer Operation Enable)

This bit enables buffer operation with the GTDVD and GTDBD registers combined.

The buffer transfer timing is the trough in triangle-wave mode, and at an overflow or underflow in saw-wave mode.

When this bit and the TDFER bit are set to 1 simultaneously, the TDFER bit setting is given priority.

TDFER bit (GTDVD Register Setting)

This bit sets whether or not the value written to the GTDVU register is also set to the GTDVD register automatically.

Bit	Symbol	Function	R/W
0	TDE	负相位波形设置 0：不使用GTDVU和GTDVD设置GTCCRB1：GTDVU和GTDVD用于在GTCCRB中自动设置带死区时间的负相波形的比较匹配值	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
4	TDBUE	GTDVU寄存器缓冲区操作使能 0：禁止GTDVU寄存器缓冲操作1：使能GTDVU寄存器缓冲操作	R/W
5	TDBDE	GTDVD寄存器缓冲区操作使能 0：禁止GTDVD寄存器缓冲操作1：使能GTDVD寄存器缓冲操作	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
8	TDFER	GTDVD寄存器设置 0：GTDVU和GTDVD寄存器分开设置。1：写入GTDVU寄存器的值自动设置到GTDVD寄存器。	R/W
31:9	—	这些位被读取为0。写入值应为0。	R/W

GTDTCR可以自动设置带死区时间的负相位波形的比较匹配值。GPT具有死区时间控制功能，GTDVU和GTDVD寄存器用于设置死区时间值。

该寄存器在Saw-wavePWM模式2或互补PWM模式下无效。

该设置在事件计数操作期间无效。

TDE位（负相位波形设置）

TDE位指定是否使用GTDVU和GTDVD。使用GTDVU和GTDVD时，通过正相波形的比较匹配值(GTCCRA)和死区时间值(GTDVU和GTDVD)获得的带死区时间的负相波形的比较匹配值自动设置在GTCCRB.

TDE位设置在锯齿波PWM模式下被忽略，GTCCRB不是自动设置。

GTCCRB值是自动设置的，具有以下上下限值。如果获得的GTCCRB值不在上限或下限范围内，则在GTCCRB中设置以下限制值，并且GTST.DTEF标志变为1。但是，如果获得的GTCCRB值在三角波PWM模式下超过上限，则DTEF标志变为0。

- Triangle waves:
  上限值：GTPR-1
  下限值：加1，减0

●锯波单发脉冲模式：上限值：
GTPR
下限值：0。

TDBUE位（GTDVU寄存器缓冲区操作使能）

该位使能结合GTDVU和GTDBU寄存器的缓冲器操作。

缓冲区传输的时序在三角波模式中处于波谷，而在锯齿波模式中处于溢出或下溢。

TDBDE位（GTDVD寄存器缓冲区操作使能）

该位启用与GTDVD和GTDBD寄存器组合的缓冲区操作。

缓冲区传输时序在三角波模式下是波谷，而在锯波模式下是上溢或下溢。

当该位和TDFER位同时设置为1时，TDFER位设置优先。

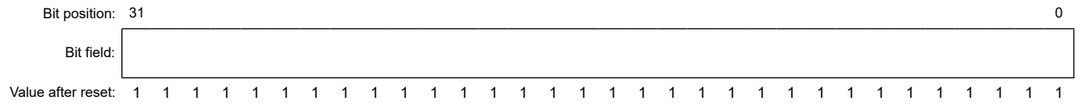
TDFER位（GTDVD寄存器设置）

该位设置写入GTDVU寄存器的值是否也自动设置到GTDVD寄存器。

21.2.28 GTDVk : General PWM Timer Dead Time Value Register k (k = U, D)

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x8C (GTDVU)
0x90 (GTDVD)

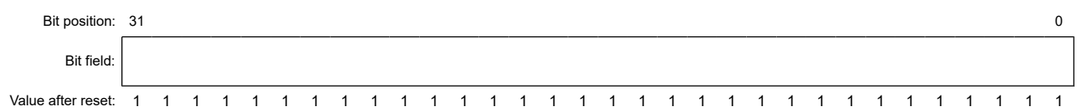


Bit	Symbol	Function	R/W
31:0	n/a	GTDVk is a read/write register that sets the dead time for generating PWM waveforms with dead time. Access in 8-bit or 16-bit units to the GTDVk register is prohibited, and it should be accessed in 32-bit units. The setting is invalid in Saw-wave PWM mode 2. In complementary PWM mode, the GTDVD register is invalid and the GTDVU register is used as the dead time value during both up-counting and down-counting. No matter which GTDVU register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time. In Triangle-waves, The GTDVU register is used for up-counting. The GTDVD register is used for down-counting. In the case of a saw-waves, the GTDVU register controls the front dead time and the GTDVD register controls the rear dead time, regardless of whether the count is up or down. Setting a GTDVk value greater than or equal to GTPR is prohibited. In complementary PWM mode, set the GTDVU register to meet the following conditions: ● GTDVU > 0 ● GTDVU < GTPR/2 ● GTDVU + GTPR ≤ 0xffffffff When using the automatic dead time setting function, do not set a value that makes a change point of the waveform exceeding the count period. The change point of the negative-phase waveform, which is automatically calculated, is obtained by reading the GTCCRB register. When GTDVk is used, writing to GTCCRB is prohibited. Other than complementary PWM mode, when this register is set to 0, waveforms without dead time are output. When the GTDTCR.TDFER bit is 1, the writing to the GTDVD register has no effect. At this time, when the GTDVD register is read, the value for the GTDVU register is read. While GPT is running, changing the GTDVk values is prohibited. To change GTDVk to a new value, stop the GPT with the CST bit in the GTCR register.	R/W

21.2.29 GTDBk: General PWM Timer Dead Time Buffer Register k (k = U, D)

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x94 (GTDBU)
0x98 (GTDBD)

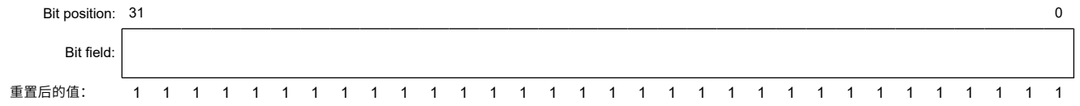


Bit	Symbol	Function	R/W
31:0	n/a	The buffer register for the GTDVk register Access in 8-bit or 16-bit units to the GTDBk register is prohibited, and it should be accessed in 32-bit units.	R/W

21.2.28 GTDVk：通用PWM定时器死区值寄存器k(k=U D)

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x8C (GTDVU)
0x90 (GTDVD)

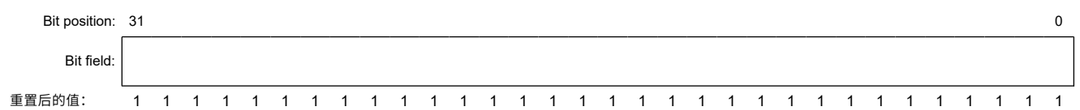


Bit	Symbol	Function	R/W
31:0	n/a	GTDVk是一个读写寄存器，用于设置死区时间，以生成带死区时间的PWM波形。禁止以8位或16位为单位访问GTDVk寄存器，应以32位为单位进行访问。Saw-wavePWM模式2设置无效。 在互补PWM模式下，GTDVD寄存器无效，GTDVU寄存器在递增计数和递减计数期间都用作死区值。无论写入主通道从通道1从通道2的哪个GTDVU寄存器，都是同时写入三个通道。在三角波中，GTDVU寄存器用于递增计数。GTDVD寄存器用于向下计数。在锯齿波的情况下，GTDVU寄存器控制前死区时间和 GTDVD寄存器控制后死区时间，无论计数是向上还是向下。 禁止将GTDVk值设置为大于或等于GTPR。 在互补PWM模式下，设置GTDVU寄存器满足以下条件：● ● GTDVU < GTPR/2 ● GTDVU + GTPR ≤ 0xffffffff 使用自动死区时间设置功能时，请勿设置使波形变化点超过计数周期的值。通过读取GTCCRB寄存器，自动计算出反相波形的变化点。 使用GTDVk时，禁止写入GTCCRB。除互补PWM模式外，当该寄存器设置为0时，输出无死区时间的波形。当GTDTCR.TDFER位为1时，写入GTDVD寄存器无效。此时，当读取GTDVD寄存器时，读取的是GTDVU寄存器的值。在GPT运行期间，禁止更改GTDVk值。要将GTDVk更改为新值，请使用GTCR寄存器中的CST位停止GPT。	R/W

21.2.29 GTDBk：通用PWM定时器死区缓冲寄存器k(k=U D)

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x94 (GTDBU)
0x98 (GTDBD)



Bit	Symbol	Function	R/W
31:0	n/a	GTDVk寄存器的缓冲寄存器 禁止以8位或16位为单位访问GTDBk寄存器，应以32位为单位进行访问。	R/W

21.2.30 GTSOS : General PWM Timer Output Protection Function Status Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x9C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SOS[1:0]	Output Protection Function Status 0 0: Normal operation 0 1: Protected state (GTCCRA = 0 is set during transfer at trough or crest) 1 0: Protected state (GTCCRA ≥ GTPR is set during transfer at trough) 1 1: Protected state (GTCCRA ≥ GTPR is set during transfer at crest)	R
7:2	—	These bits are read as 0.	R
9:8	—	The read value is undefined.	R
31:10	—	These bits are read as 0.	R

The GTSOS register is a status register that indicates the status of the output protection function. The output protection function is enabled only when the dead time is automatically set (GTDTCR.TDE bit = 1) in triangle-wave mode.

SOS[1:0] bit (Output Protection Function Status)

This bit indicates the status of the output protection function in triangle-wave PWM mode. For details of the output protection function, see section 21.8.4. Output Protection Function for GTIOCnm Pin Output (n = 0 to 9; m = A, B).

21.2.31 GTSOTR : General PWM Timer Output Protection Function Temporary Release Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xA0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOTR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SOTR	Output Protection Function Temporary Release 0: Protected state is not released 1: Protected state is released	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

The GTSOTR register temporarily releases the protected state of GTIOCnB pin output (n = 0 to 9) when output protection has been set.

21.2.30 GTSOS:通用PWM定时器输出保护功能状态寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0x9C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SOS[1:0]	输出保护功能状态 00：正常运行01：保护状态（在波谷或波峰转移期间设置GTCCRA=0）10：保护状态（在波谷转移期间设置GTCCRA≥GTPR）11：保护状态（GTCCRA≥GTPR设置在波峰转移期间）	R
7:2	—	这些位读为0。	R
9:8	—	读取值未定义。	R
31:10	—	这些位读为0。	R

GTSOS寄存器是指示输出保护功能状态的状态寄存器。只有在三角波模式下自动设置死区时间（GTDTCR.TDE位=1）时，才会启用输出保护功能。

SOS[1:0]位（输出保护功能状态）

该位指示三角波PWM模式下输出保护功能的状态。关于输出保护功能的详细内容，请参阅21.8.4节。GTIOCnm引脚输出的输出保护功能（n=0至9；m=A、B）。

21.2.31 GTSOTR:通用PWM定时器输出保护功能临时解除Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xA0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOTR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SOTR	输出保护功能临时解除 0：不解除保护状态1：解除保护状态	R/W
31:1	—	这些位被读取为0。写入值应为0。	R/W

当设置了输出保护时，GTSOTR寄存器暂时解除GTIOCnB引脚输出（n=0到9）的保护状态。

The protected state can be released only for the case of GTSOS.SOS[1:0] bits are 10b (protected state in which GTCCRA register ≥ GTPR register has occurred during transfer at trough). The protected state cannot be released for any other case.

SOTR bit (Output Protection Function Temporary Release)

This bit sets whether to temporarily release the protected state of the GTIOCnB pin output in an output protected state.

After the SOTR bit has been set to 1, the output protection function is canceled from the first trough. After the SOTR bit has been set to 0, output protection is resumed from the first trough.

21.2.32 GTADSMR : General PWM Timer A/D Conversion Start Request Signal Monitoring Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xA4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	ADSMEN1	—	—	—	—	—	—	ADSMS1[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ADSMEN0	—	—	—	—	—	—	ADSMS0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ADSMS0[1:0]	A/D Conversion Start Request Signal Monitor 0 Selection 0 0: A/D conversion start request signal generated by the GTADTRA register during up-counting. 0 1: A/D conversion start request signal generated by the GTADTRA register during down-counting. 1 0: A/D conversion start request signal generated by the GTADTRB register during up-counting. 1 1: A/D conversion start request signal generated by the GTADTRB register during down-counting.	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	ADSMEN0	A/D Conversion Start Request Signal Monitor 0 Output Enabling 0: Output of A/D conversion start request signal monitor 0 is disabled. 1: Output of A/D conversion start request signal monitor 0 is enabled.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
17:16	ADSMS1[1:0]	A/D Conversion Start Request Signal Monitor 1 Selection 0 0: A/D conversion start request signal generated by the GTADTRA register during up-counting. 0 1: A/D conversion start request signal generated by the GTADTRA register during down-counting. 1 0: A/D conversion start request signal generated by the GTADTRB register during up-counting. 1 1: A/D conversion start request signal generated by the GTADTRB register during down-counting.	R/W
23:18	—	These bits are read as 0. The write value should be 0.	R/W
24	ADSMEN1	A/D Conversion Start Request Signal Monitor 1 Output Enabling 0: Output of A/D conversion start request signal monitor 1 is disabled. 1: Output of A/D conversion start request signal monitor 1 is enabled.	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

The GTADSMR register is used to control monitors for the A/D conversion start request signal that is synchronized with a frame period.

保护状态只能在GTSOS.SOS[1:0]位为10b的情况下解除（在低谷传输期间出现GTCCRA寄存器≥GTPR寄存器的保护状态）。对于任何其他情况，不能释放受保护状态。

SOTR位（输出保护功能临时释放）

该位设置是否在输出保护状态下暂时解除GTIOCnB引脚输出的保护状态。

在SOTR位被设置为1后，输出保护功能从第一个波谷取消。在SOTR位被设置为0后，输出保护从第一个波谷恢复。

21.2.32 GTADSMR:通用PWM定时器AD转换开始请求信号监控寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xA4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	ADSMEN1	—	—	—	—	—	—	ADSMS1[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ADSMEN0	—	—	—	—	—	—	ADSMS0[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ADSMS0[1:0]	AD转换开始请求信号监视器0选择 00：在递增计数期间由GTADTRA寄存器产生的D转换开始请求信号。 01：向下计数期间由GTADTRA寄存器产生的D转换开始请求信号。 10：在递增计数期间由GTADTRB寄存器产生的D转换开始请求信号。 11：向下计数期间由GTADTRB寄存器产生的D转换开始请求信号。	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
8	ADSMEN0	AD转换开始请求信号监视器0输出使能 0:AD转换开始请求信号监视器0的输出无效。1:AD转换开始请求信号监视器0的输出有效。	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
17:16	ADSMS1[1:0]	AD转换开始请求信号监视器1选择 00：在递增计数期间由GTADTRA寄存器产生的D转换开始请求信号。 01：向下计数期间由GTADTRA寄存器产生的D转换开始请求信号。 10：在递增计数期间由GTADTRB寄存器产生的D转换开始请求信号。 11：向下计数期间由GTADTRB寄存器产生的D转换开始请求信号。	R/W
23:18	—	这些位被读取为0。写入值应为0。	R/W
24	ADSMEN1	AD转换开始请求信号监视器1输出使能 0:AD转换开始请求信号监视器1的输出无效。1：AD转换开始请求信号监视器1的输出有效。	R/W
31:25	—	这些位被读取为0。写入值应为0。	R/W

GTADSMR寄存器用于控制与帧周期同步的AD转换开始请求信号的监视器。

ADSMSk[1:0] bits (A/D Conversion Start Request Signal Monitor k Selection) (k = 0, 1)

These bits are used to select A/D conversion start request signal synchronized with a frame period which is monitored by the GTASMk pin.

In triangle-wave PWM mode or complementary PWM mode, the following settings are prohibited:

- Set ADSMSk[1:0] bit to 00b (A/D conversion start request during up-counting) when GTADTRA = 0
- Set ADSMSk[1:0] bit to 10b (A/D conversion start request during up-counting) when GTADTRB = 0
- Set ADSMSk[1:0] bit to 01b (A/D conversion start request during down-counting) when GTADTRA = GTPR
- Set ADSMSk[1:0] bit to 11b (A/D conversion start request during down-counting) when GTADTRB = GTPR

ADSMENk bit (A/D Conversion Start Request Signal Monitor k Output Enabling) (k = 0, 1)

This bit enables or disables the monitor output to the GTADSMk pin.

When the output is disabled, the GTADSMk pin goes to the low level.

When the bit is 1, the signal on the GTADSMk pin goes to the high level on assertion of the signal to request to the start of A/D conversion selected by the ADSMSk[1:0] bits and returns to the low level at the end of the current cycle of the timer for the channel that generated the given signal to request the start of A/D conversion. When the counter stops, the value when the counter stopped is retained for output. Set the ADSMENk bit to 0 to output the low level.

When a signal to request the start of A/D conversion is generated at the end of a timer period, the generation of this signal has priority in terms of monitoring output and the output remains at the high level till the end of the next period.

When the output of the same A/D conversion start request signal monitoring output is enabled for multiple channels, ORed signals will be output from the GPT.

21.2.33 GTEITC : General PWM Timer Extended Interrupt Skipping Counter Control Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xA8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EITCNT2[3:0]				EITCNT2IV[3:0]				EIVTT2[3:0]				—	—	EIVTC2[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EITCNT1[3:0]				—	—	—	—	EIVTT1[3:0]				—	—	EIVTC1[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	EIVTC1[1:0]	Extended Interrupt Skipping Counter 1 Count Source Select 0 0: Not counted (not skipped) 0 1: Counting both at overflow or underflow in saw-wave mode, and counting crests in triangle-wave mode or complementary PWM mode 1 0: Counting both at overflow or underflow in saw-wave mode, and counting troughs in triangle-wave mode or complementary PWM mode 1 1: Counting both at overflow or underflow in saw-wave mode, and counting both crests and troughs in triangle-wave mode or complementary PWM mode	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
7:4	EIVTT1[3:0]	Extended Interrupt Skipping 1 Skipping Count Setting Skipping count for the extended interrupt skipping 1	R/W
11:8	—	These bits are read as 0. The write value should be 0.	R/W
15:12	EITCNT1[3:0]	Extended Interrupt Skipping Counter 1	R

ADSMSk[1:0]位（AD转换开始请求信号监控k选择）（k=0 1）

这些位用于选择与GTASMk引脚监控的帧周期同步的AD转换开始请求信号。

在三角波PWM模式或互补PWM模式下，禁止以下设置：

- ●GTADTRA=0时，将ADSMSk[1:0]位设置为00b（递增计数期间的AD转换开始请求）
- ●当GTADTRB=0时，将ADSMSk[1:0]位设置为10b（递增计数期间的AD转换开始请求）
- ●当GTADTRA=GTPR时，将ADSMSk[1:0]位设置为01b（递减计数期间的AD转换开始请求）
- ●当GTADTRB=GTPR时，将ADSMSk[1:0]位设置为11b（递减计数期间的AD转换开始请求）

ADSMENk位（AD转换开始请求信号监视器k输出使能）（k=0 1）

该位启用或禁用到GTADSMk引脚的监视器输出。

当输出被禁用时，GTADSMk引脚变为低电平。

当该位为1时，GTADSMk引脚上的信号在信号置位时变为高电平以请求开始由ADSMSk[1:0]位选择的AD转换，并在产生给定信号的通道的定时器当前周期结束时返回低电平，以请求开始AD转换。当计数器停止时，计数器停止时的值被保留用于输出。将ADSENk位设置为0以输出低电平。

当在定时器周期结束时产生请求开始AD转换的信号时，该信号的产生在监视输出方面具有优先权，并且输出保持高电平直到下一个周期结束。

当多个通道的相同AD转换开始请求信号监视输出启用时，将从GPT输出ORed信号。

21.2.33 GTEITC:通用PWM定时器扩展中断跳过计数器控制 Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xA8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EITCNT2[3:0]				EITCNT2IV[3:0]				EIVTT2[3:0]				—	—	EIVTC2[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EITCNT1[3:0]				—	—	—	—	EIVTT1[3:0]				—	—	EIVTC1[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	EIVTC1[1:0]	扩展中断跳过计数器1计数源选择 00：不计数（不跳过）01：在锯齿波模式下在上溢或下溢时计数，在三角波模式或互补PWM模式下计数波峰 10：在锯齿波模式下上溢或下溢计数，在三角波模式或互补PWM模式下计数波谷 11：在锯齿波模式下同时计数上溢或下溢，在三角波模式或互补PWM模式下同时计数波峰和波谷	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
7:4	EIVTT1[3:0]	扩展中断跳过1跳过计数设置 扩展中断跳过的跳过计数1	R/W
11:8	—	这些位被读取为0。写入值应为0。	R/W
15:12	EITCNT1[3:0]	扩展中断跳过计数器1	R

Bit	Symbol	Function	R/W
17:16	EIVTC2[1:0]	Extended Interrupt Skipping Counter 2 Count Source select 0 0: Not counted (not skipped) 0 1: Counting both at overflow or underflow in saw-wave mode, and counting crests in triangle-wave mode or complementary PWM mode 1 0: Counting both at overflow or underflow in saw-wave mode, and counting troughs in triangle-wave mode or complementary PWM mode 1 1: Counting both at overflow or underflow in saw-wave mode, and counting both crests and troughs in triangle-wave mode or complementary PWM mode	R/W
19:18	—	These bits are read as 0. The write value should be 0.	R/W
23:20	EIVTT2[3:0]	Extended Interrupt Skipping 2 Skipping Count Setting Skipping count for the extended interrupt skipping 2	R/W
27:24	EITCNT2IV[3:0]	Extended Interrupt Skipping Counter 2 Initial Value	R/W*1
31:28	EITCNT2[3:0]	Extended Interrupt Skipping Counter 2	R

Note 1. The EITCNT2IV[3:0] bits are only writable when the value other than 00b is written to the EIVTC2[1:0] bits that have been 00b.

GTEITC register sets the extended interrupt skipping function to skip the interrupts, A/D conversion start requests, and buffer transfers independently by counting at overflow and underflow in the GTCNT counter.

The setting is operated independently from the interrupt skipping by the GTITC register or the GTADCMSC register.

The setting is invalid during the event count operation.

Access in 8-bit units to GTEITC is prohibited.

EIVTCk[1:0] bits (Extended Interrupt Skipping Counter k Count Source Select) (k = 1, 2)

These bits select the way of counting for the extended interrupt skipping counter k.

Setting only with these bits does not skip the interrupts, A/D conversion start requests, and buffer transfers. Skipping function for the interrupt, A/D conversion start request, and buffer transfer, all of which are a target of skipping, is set individually with the GTEITLI1, GTEITLI2, and GTEITLB registers.

EIVTTk[3:0] bits (Extended Interrupt Skipping k Skipping Count Setting) (k = 1, 2)

A count for the period with continuous skipping is set as a skipping count, where a period is from a generation of a count source selected by the EIVTCk[1:0] bits to the next generation of the count source.

When the count source is generated while the EIVTTk[3:0] bits match the EITCNTk[3:0] bits, the EITCNTk[3:0] bits are cleared.

When these bits are 0x0, skipping is not performed.

EITCNT1[3:0] bits (Extended Interrupt Skipping Counter 1)

The counting is incremented by 1 every time a count source (overflow/underflow/crest/trough) selected by the EIVTC1[1:0] bits is generated.

Counting is performed periodically within the range between 0 and the EIVTT1[3:0] bits.

Even if the GTCNT counter is stopped, the value is not cleared, and value at stop of the GTCNT counter is retained.

[Clearing conditions]

- 00b is written to the EIVTC1[1:0] bits.
- 0x0 is written to the EIVTT1[3:0] bits.
- A count source (overflow/underflow/crest/trough) selected by the EIVTC1[1:0] bits is generated when the extended interrupt skipping 1 skipping count set by the EIVTT1[3:0] bits match the value for the EITCNT1[3:0]

EITCNT2IV[3:0] bit (Extended Interrupt Skipping Counter 2 Initial Value)

These bits are the value of the initial value for the extended interrupt skipping counter 2.

Writing to the EITCNT2IV[3:0] is performed only when the writing value to the EIVTC2[1:0] bits are other than 00b and when the GTEITC register is written by the access of upper 16 bits or 32 bits while the EITCNT2[3:0] bits are set not to count (EIVTC2[1:0] bits are 00b). When the EITCNT2IV[3:0] bits are written, the value written to the EITCNT2IV[3:0] bits is written to the EITCNT2[3:0] bits simultaneously.

Bit	Symbol	Function	R/W
17:16	EIVTC2[1:0]	扩展中断跳过计数器2计数源选择 00：不计数（不跳过）01：在锯齿波模式下在上溢或下溢时计数，在三角波模式或互补PWM模式下计数波峰 10：在锯齿波模式下上溢或下溢计数，在三角波模式或互补PWM模式下计数波谷 11：在锯齿波模式下同时计数上溢或下溢，在三角波模式或互补PWM模式下同时计数波峰和波谷	R/W
19:18	—	这些位被读取为0。写入值应为0。	R/W
23:20	EIVTT2[3:0]	扩展中断跳过2跳过计数设置 扩展中断跳过的跳过计数2	R/W
27:24	EITCNT2IV[3:0]	扩展中断跳过计数器2初始值	R/W*1
31:28	EITCNT2[3:0]	扩展中断跳过计数器2	R

注1.EITCNT2IV[3:0]位仅在将00b以外的值写入已为00b的EIVTC2[1:0]位时才可写。

GTEITC寄存器设置扩展中断跳过功能，通过在GTCNT计数器中的溢出和下溢计数独立地跳过中断、AD转换开始请求和缓冲区传输。

该设置独立于GTITC寄存器或GTADCMSC寄存器的中断跳过操作。

该设置在事件计数操作期间无效。

禁止以8位为单位访问GTEITC。

EIVTCk[1:0]位（扩展中断跳过计数器k计数源选择）（k=1 2）

这些位选择扩展中断跳过计数器k的计数方式。

仅用这些位设置不会跳过中断、AD转换开始请求和缓冲区传输。中断、AD转换开始请求和缓冲区传输的跳过功能都是跳过的目标，通过GTEITLI1、GTEITLI2和GTEITLB寄存器单独设置。

EIVTTk[3:0]位（扩展中断跳过k跳过计数设置）（k=1 2）

将连续跳过的周期的计数设置为跳过计数，其中周期是从EIVTk[1:0]位选择的计数源的一代到下一代计数源。

当EIVTTk[3:0]位与EITCNTk[3:0]位匹配时产生计数源时，EITCNTk[3:0]位被清零。

当这些位为0x0时，不执行跳过。

EITCNT1[3:0]位（扩展中断跳过计数器1）

每次产生由EIVTC1[1:0]位选择的计数源（上溢下溢波峰波谷）时，计数加1。

在0和EIVTT1[3:0]位之间的范围内定期执行计数。

即使GTCNT计数器停止，该值也不会被清除，而是保留GTCNT计数器停止时的值。

[Clearing conditions]

- 00b被写入EIVTC1[1:0]位。
- 0x0写入EIVTT1[3:0]位。
- 当EIVTT1[3:0]位设置的扩展中断跳过1跳过计数与EITCNT1[3:0]

EITCNT2IV[3:0]位（扩展中断跳过计数器2初始值）

这些位是扩展中断跳过计数器2的初始值。

仅当写入EIVTC2[1:0]位的值不是00b并且通过访问高16位或32位而写入GTEITC寄存器时，才会执行对EITCNT2IV[3:0]的写入，而EITCNT2[3:0]位设置为不计数（EIVTC2[1:0]位为00b）。写入EITCNT2IV[3:0]位时，写入EITCNT2IV[3:0]位的值同时写入EITCNT2[3:0]位。

The writing to the EITCNT2IV[3:0] bits are ignored when the EITCNT2[3:0] bits are set to count (EIVTC2[1:0] bits are other than 00b) or perform the setting of not to count (00b is written to the EIVTC2[1:0] bits).

The EITCNT2IV[3:0] bits are not reset by the writing 00b to the EIVTC2[1:0] bits.

EITCNT2[3:0] bit (Extended Interrupt Skipping Counter 2)

The counting is incremented by 1 every time a count source (overflow/underflow/crest/trough) selected by the EIVTC2[1:0] bits is generated.

Counting is performed periodically within the range between 0 and the EIVTT2[3:0] bits.

Even if the GTCNT counter is stopped, the value is not cleared, and value at stop of the GTCNT counter is retained.

Setting of the initial value for the EITCNT2[3:0] bits are performed only when the writing value to the EIVTC2[1:0] bits are other than 00b and when the GTEITC register is written by the access of upper 16 bits or 32 bits while the extended interrupt skipping counter 2 is set as not to count (EIVTC2[1:0] bits are 00b).

When the initial value is set, the written value to the EITCNT2IV[3:0] bits is written to the EITCNT2[3:0] bits as the initial value.

[Clearing condition]

- 00b is written to the EIVTC2[1:0] bits.
- 0x0 is written to the EIVTT2[3:0] bits.
- The value other than 00b is written to the EIVTC2[1:0] bits and the 0x0 is written to the EITCNT2IV[3:0] bits simultaneously while 00b is set to the EIVTC2[1:0] bits.
- A count source (overflow/underflow/crest/trough) selected by the EIVTC2[1:0] bits is generated when the extended interrupt skipping 2 skipping count set by the EIVTT2[3:0] bits match the value for the EITCNT2[3:0].

21.2.34 GTEITLI1 : General PWM Timer Extended Interrupt Skipping Setting Register 1

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xAC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	EITLU[2:0]			—	EITLV[2:0]			—	EITLF[2:0]			—	EITLE[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	EITLD[2:0]			—	EITLC[2:0]			—	EITLB[2:0]			—	EITLA[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	EITLA[2:0]	GTCCRA Register Compare Match/Input Capture Interrupt Extended Skipping Function Select See Table 21.6.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	EITLB[2:0]	GTCCRB Register Compare Match/Input Capture Interrupt Extended Skipping Function Select See Table 21.6.	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
10:8	EITLC[2:0]	GTCCRC Register Compare Match Interrupt Extended Skipping Function Select See Table 21.6.	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
14:12	EITLD[2:0]	GTCCRD Register Compare Match Interrupt Extended Skipping Function Select See Table 21.6.	R/W
15	—	This bit is read as 0. The write value should be 0.	R/W

当EITCNT2[3:0]位设置为计数（EIVTC2[1:0]位不是00b）或执行不计数设置（00b为写入EIVTC2[1:0]位）。

将00b写入EIVTC2[1:0]位不会复位EITCNT2IV[3:0]位。

EITCNT2[3:0]位（扩展中断跳过计数器2）

每次产生由EIVTC2[1:0]位选择的计数源（上溢下溢波峰波谷）时，计数加1。

在0和EIVTT2[3:0]位之间的范围内定期执行计数。

即使GTCNT计数器停止，该值也不会被清除，而是保留GTCNT计数器停止时的值。

仅当写入EIVTC2[1:0]位的值不是00b以及通过访问高16位或32位来写入GTEITC寄存器时，才执行EITCNT2[3:0]位的初始值设置位，而扩展中断跳过计数器2设置为不计数（EIVTC2[1:0]位为00b）。

设置初始值时，写入EITCNT2IV[3:0]位的值将作为初始值写入EITCNT2[3:0]位。

[Clearing condition]

●00b写入EIVTC2[1:0]位。

●0x0写入EIVTT2[3:0]位。

●00b以外的值写入EIVTC2[1:0]位，同时将0x0写入EITCNT2IV[3:0]位，同时将00b设置为EIVTC2[1:0]位。

●当EIVTT2[3:0]位设置的扩展中断跳过2跳过计数与EITCNT2[3:0]。

21.2.34 GTEITLI1：通用PWM定时器扩展中断跳过设置寄存器1

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xAC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	EITLU[2:0]			—	EITLV[2:0]			—	EITLF[2:0]			—	EITLE[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	EITLD[2:0]			—	EITLC[2:0]			—	EITLB[2:0]			—	EITLA[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	EITLA[2:0]	GTCCRA寄存器比较匹配输入捕捉中断扩展跳过功能Select 见表21.6。	R/W
3	—	该位读取为0。写入值应为0。	R/W
6:4	EITLB[2:0]	GTCCRB寄存器比较匹配输入捕捉中断扩展跳过功能Select 见表21.6。	R/W
7	—	该位读取为0。写入值应为0。	R/W
10:8	EITLC[2:0]	GTCCRC寄存器比较匹配中断扩展跳过功能选择 见表21.6。	R/W
11	—	该位读取为0。写入值应为0。	R/W
14:12	EITLD[2:0]	GTCCRD寄存器比较匹配中断扩展跳过功能选择 见表21.6。	R/W
15	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
18:16	EITLE[2:0]	GTCCRE Register Compare Match Interrupt Extended Skipping Function Select See Table 21.6.	R/W
19	—	This bit is read as 0. The write value should be 0.	R/W
22:20	EITLF[2:0]	GTCCRF Register Compare Match Interrupt Extended Skipping Function Select See Table 21.6.	R/W
23	—	This bit is read as 0. The write value should be 0.	R/W
26:24	EITLV[2:0]	Overflow Interrupt Extended Skipping Function Select See Table 21.6.	R/W
27	—	This bit is read as 0. The write value should be 0.	R/W
30:28	EITLU[2:0]	Underflow Interrupt Extended Skipping Function Select See Table 21.6.	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

The GTEITLI1 register sets the extended skipping function for interrupts such as compare match/input capture, overflow and underflow.

Setting only with this register does not perform skipping. The GTEITC register should be set so that a corresponding extended interrupt skipping counter operates the counting.

The setting is operated independently from the interrupt skipping by the GTITC register or the GTADCMSC register.

The setting is invalid during the event count operation.

EITLm[2:0] bits (GTCCRm Register Compare Match/Input Capture Interrupt Extended Skipping Function Select) (m = A, B)

These bits select the extended interrupt skipping function to skip the compare match/input capture interrupt (GPTn_CCMPm) in the GTCCRm register. See Table 21.6.

EITLx[2:0] bits (GTCCRx Register Compare Match Interrupt Extended Skipping Function Select) (x = C, D, E, F)

These bits select the extended interrupt skipping function to skip the compare match interrupt (GPTn_CMPx) in the GTCCRx register. See Table 21.6.

EITLV[2:0] bit (Overflow Interrupt Extended Skipping Function Select)

These bits select the extended interrupt skipping function to skip the interrupt at overflow(GPTn_OVF). See Table 21.6.

EITLU[2:0] bit (Underflow Interrupt Extended Skipping Function Select)

These bits select the extended interrupt skipping function to skip the interrupt at underflow (GPTn_UDF). See Table 21.6.

Table 21.6 Setting the Function select for the GTEITLI1 (1 of 2)

EITLy[2:0]	Function
0 0 0	Do not perform an extended interrupt skipping
0 0 1	Skip an interrupt in the period when the value for the extended interrupt skipping counter 1 is other than 0 (An interrupt is output in the period of the EITCNT1[3:0] bits = 0)
0 1 0	Skip an interrupt in the period when the value for the extended interrupt skipping counter 2 is other than 0 (An interrupt is output in the period of the EITCNT2[3:0] bits = 0)
0 1 1	Skip an interrupt in the period the value for the extended interrupt skipping counter 1 or 2 is other than 0 (An interrupt is output in the period of the EITCNT1[3:0] bits = 0 and the EITCNT2[3:0] bits = 0)
1 0 0	Setting prohibited
1 0 1	Skip an interrupt in the period when the value for the extended interrupt skipping counter 1 is other than the skipping count (An interrupt is output in the period of the EITCNT1[3:0] bits = the EIVTT1[3:0] bits)
1 1 0	Skip an interrupt in the period when the value for the extended interrupt skipping counter 2 is other than the skipping count (An interrupt is output in the period of the EITCNT2[3:0] bits = the EIVTT2[3:0] bits)

Bit	Symbol	Function	R/W
18:16	EITLE[2:0]	GTCCRE寄存器比较匹配中断扩展跳过功能选择 见表21.6。	R/W
19	—	该位读取为0。写入值应为0。	R/W
22:20	EITLF[2:0]	GTCCRF寄存器比较匹配中断扩展跳过功能选择 见表21.6。	R/W
23	—	该位读取为0。写入值应为0。	R/W
26:24	EITLV[2:0]	溢出中断扩展跳过功能选择 见表21.6。	R/W
27	—	该位读取为0。写入值应为0。	R/W
30:28	EITLU[2:0]	下溢中断扩展跳过功能选择 见表21.6。	R/W
31	—	该位读取为0。写入值应为0。	R/W

GTEITLI1寄存器为比较匹配输入捕捉、上溢和下溢等中断设置扩展跳过功能。

仅使用该寄存器进行设置不会执行跳过。应该设置GTEITC寄存器，以便相应的扩展中断跳过计数器操作计数。

该设置独立于GTITC寄存器或GTADCMSC寄存器的中断跳过操作。

该设置在事件计数操作期间无效。

EITLm[2:0]位（GTCCRm寄存器比较匹配输入捕捉中断扩展跳过功能Select) (m = A, B)

这些位选择扩展中断跳过功能以跳过GTCCRm寄存器中的比较匹配输入捕捉中断(GPTn_CCMPm)。见表21.6。

EITLx[2:0]位（GTCCRx寄存器比较匹配中断扩展跳过功能选择）（x=C，D, E, F)

这些位选择扩展中断跳过功能以跳过比较匹配中断（GPTn_CMPx）GTCCRx寄存器。见表21.6。

EITLV[2:0]位（溢出中断扩展跳过功能选择）

这些位选择扩展中断跳过功能以跳过溢出中断（GPTn_OVF）。见表21.6。

EITLU[2:0]位（下溢中断扩展跳过功能选择）

这些位选择扩展中断跳过功能以跳过下溢中断（GPTn_UDF）。见表21.6。

Table 21.6 设置GTEITLI1的功能选择(1of2)

EITLy[2:0]	Function
0 0 0	不要执行扩展的中断跳过
0 0 1	在扩展中断跳过计数器1的值不为0时跳过中断（在EITCNT1[3:0]位=0的时段内输出中断）
0 1 0	在扩展中断跳过计数器2的值不为0时跳过中断（在EITCNT2[3:0]位=0的时段内输出中断）
0 1 1	在扩展中断跳过计数器1或2的值不为0的时段内跳过一个中断（在EITCNT1[3:0]位=0和EITCNT2[3:0]位=的时段内输出一个中断0）
1 0 0	禁止设定
1 0 1	在扩展中断跳过计数器1的值不是跳过计数的周期内跳过中断（在EITCNT1[3:0]位=EIVTT1[3:0]位的周期内输出中断）
1 1 0	在扩展中断跳过计数器2的值不是跳过计数的周期内跳过一个中断（在EITCNT2[3:0]位=EIVTT2[3:0]位的周期内输出中断）

Table 21.6 Setting the Function select for the GTEITLI1 (2 of 2)

EITLy[2:0]	Function
1 1 1	Skip an interrupt in the period when the value for the extended interrupt skipping counter 1 or 2 is other than the skipping count (An interrupt is output in the period of the EITCNT1[3:0] bits = the EIVTT1[3:0] bits and the EITCNT2[3:0] bits = the EIVTT2[3:0] bits)

Note:
- y = A, B, C, D, E, F, V, U
- When the intended skipping counter is set as not to count (the EIVTCk[1:0] bits = 00b or the EIVTTk[3:0] bits = 0x0), skipping is not performed.(k = 1, 2)
- When the EITLy[2:0] bits are set to 011b or 111b, and when one of the skipping counter 1 or 2 is set as not to count, skipping is not performed.

21.2.35 GTEITLI2 : General PWM Timer Extended Interrupt Skipping Setting Register 2

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xB0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	EADTBL[2:0]			—	EADTAL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	EADTAL[2:0]	GTADTRA Register A/D Conversion Start Request Extended Skipping Function Select See Table 21.7.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	EADTBL[2:0]	GTADTRB Register A/D Conversion Start Request Extended Skipping Function Select See Table 21.7.	R/W
31:7	—	These bits are read as 0. The write value should be 0.	R/W

The GTEITLI2 register sets the extended skipping function for A/D conversion start requests.

Setting only with this register does not perform skipping. The GTEITC register should be set so that a corresponding extended interrupt skipping counter operates the counting.

The setting is operated independently from the interrupt skipping by the GTITC register or the GTADCMSC register.

The setting is invalid during the event count operation.

EADTmL[2:0] bits (GTADTRm Register A/D Conversion Start Request Extended Skipping Function Select) (m = A, B)

These bits select the extended skipping function to skip A/D conversion start requests for the compare match in the GTADTRm register. See Table 21.7.

Table 21.7 Setting the Function Select for the GTEITLI2 Register (1 of 2)

EADTmL[2:0]	Function
0 0 0	Do not perform an extended interrupt skipping
0 0 1	Skip an A/D conversion start request in the period when the value for the extended interrupt skipping counter 1 is other than 0 (An A/D conversion start request is output in the period of the EITCNT1[3:0] bits = 0)
0 1 0	Skip an A/D conversion start request in the period when the value for the extended interrupt skipping counter 2 is other than 0 (An A/D conversion start request is output in the period of the EITCNT2[3:0] bits = 0)

Table 21.6 设置GTEITLI1的功能选择(2of2)

EITLy[2:0]	Function
1 1 1	在扩展中断跳过计数器1或2的值不是跳过计数的周期内跳过中断（在EITCNT1[3:0]位=EIVTT1[3:0]位的周期内输出中断EITCNT2[3:0]位=EIVTT2[3:0]位）

Note:
- y = A, B, C, D, E, F, V, U
- 当预期的跳过计数器设置为不计数时（EIVTCk[1:0]位=00b或EIVTTk[3:0]位=0x0），不执行跳过。（k=1 2）
- 当EITLy[2:0]位设置为011b或111b时，并且当跳过计数器1或2之一设置为不计数时，不执行跳过。

21.2.35 GTEITLI2：通用PWM定时器扩展中断跳过设置寄存器2

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xB0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	EADTBL[2:0]			—	EADTAL[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	EADTAL[2:0]	GTADTRA寄存器AD转换开始请求扩展跳过功能选择 见表21.7。	R/W
3	—	该位读取为0。写入值应为0。	R/W
6:4	EADTBL[2:0]	GTADTRB寄存器AD转换开始请求扩展跳过功能选择 见表21.7。	R/W
31:7	—	这些位被读取为0。写入值应为0。	R/W

GTEITLI2寄存器设置AD转换开始请求的扩展跳过功能。

仅使用该寄存器进行设置不会执行跳过。应该设置GTEITC寄存器，以便相应的扩展中断跳过计数器操作计数。

该设置独立于GTITC寄存器或GTADCMSC寄存器的中断跳过操作。

该设置在事件计数操作期间无效。

EADTmL[2:0]位（GTADTRm寄存器AD转换开始请求扩展跳过功能Select) (m = A, B)

这些位选择扩展跳过功能以跳过AD转换开始请求以进行比较匹配GTADTRm寄存器。见表21.7。

Table 21.7 设置GTEITLI2寄存器的功能选择(1of2)

EADTmL[2:0]	Function
0 0 0	不要执行扩展的中断跳过
0 0 1	在扩展中断跳过计数器1的值不为0时跳过AD转换开始请求（在EITCNT1[3:0]位=0的时段内输出AD转换开始请求）
0 1 0	在扩展中断跳过计数器2的值不为0时跳过AD转换开始请求（在EITCNT2[3:0]位=0的时段内输出AD转换开始请求）

Table 21.7 Setting the Function Select for the GTEITLI2 Register (2 of 2)

EADTmL[2:0]	Function
0 1 1	Skip an A/D conversion start request in the period when the value for the extended interrupt skipping counter 1 or 2 is other than 0 (An A/D conversion start request is output in the period of the EITCNT1[3:0] bits = 0 and the EITCNT2[3:0] bits = 0)
1 0 0	Setting prohibited
1 0 1	Skip an A/D conversion start request in the period when the value for the extended interrupt skipping counter 1 is other than the skipping count (An A/D conversion start request is output in the period of the EITCNT1[3:0] bits = the EIVTT1[3:0] bits)
1 1 0	Skip an A/D conversion start request in the period when the value for the extended interrupt skipping counter 2 is other than the skipping count (An A/D conversion start request is output in the period of the EITCNT2[3:0] bits = the EIVTT2[3:0] bits)
1 1 1	Skip an A/D conversion start request in the period when the value for the extended interrupt skipping counter 1 or 2 is other than the skipping count (An A/D conversion start request is output in the period of the EITCNT1[3:0] bits = the EIVTT1[3:0] bits and the EITCNT2[3:0] bits = the EIVTT2[3:0] bits)

Note:
- m = A, B
- When the intended skipping counter is set as not to count (the EIVTCk[1:0] bits = 00b or the EIVTTk[3:0] bits = 0x0), skipping is not performed. (k = 1, 2)
- When the EADTmL[2:0] bits are set to 011b or 111b, and when one of the skipping counter 1 or 2 is set as not to count, skipping is not performed.

21.2.36 GTEITLB : General PWM Timer Extended Buffer Transfer Skipping Setting Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xB4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	EBTLDVD[2:0]			—	EBTLDVU[2:0]			—	EBTLADB[2:0]			—	EBTLADA[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	EBTLPR[2:0]			—	EBTLCB[2:0]			—	EBTLCA[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	EBTLCA[2:0]	GTCCRA Register Buffer Transfer Extended Skipping Function Select See Table 21.8.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	EBTLCB[2:0]	GTCCRB Register Buffer Transfer Extended Skipping Function Select See Table 21.8.	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
10:8	EBTLPR[2:0]	GTPR Register Buffer Transfer Extended Skipping Function Select See Table 21.8.	R/W*1
15:11	—	These bits are read as 0. The write value should be 0.	R/W
18:16	EBTLADA[2:0]	GTADTRA Register Buffer Transfer Extended Skipping Function Select See Table 21.8.	R/W
19	—	This bit is read as 0. The write value should be 0.	R/W
22:20	EBTLADB[2:0]	GTADTRB Register Buffer Transfer Extended Skipping Function Select See Table 21.8.	R/W
23	—	This bit is read as 0. The write value should be 0.	R/W

Table 21.7 设置GTEITLI2寄存器的功能选择(2of2)

EADTmL[2:0]	Function
0 1 1	在扩展中断跳过计数器1或2的值不为0的时段内跳过AD转换开始请求（在EITCNT1[3:0]位=0和EITCNT2的时段内输出AD转换开始请求[3:0]位=0）
1 0 0	禁止设定
1 0 1	在扩展中断跳过计数器1的值不是跳过计数的时段内跳过AD转换开始请求（在EITCNT1[3:0]位=EIVTT1[3的时段内输出AD转换开始请求:0]位）
1 1 0	在扩展中断跳过计数器2的值不是跳过计数的时段内跳过AD转换开始请求（在EITCNT2[3:0]位=EIVTT2[3的时段内输出AD转换开始请求:0]位）
1 1 1	在扩展中断跳过计数器1或2的值不是跳过计数的周期内跳过AD转换启动请求（在EITCNT1[3:0]位=EIVTT1的周期内输出AD转换启动请求[3:0]位和EITCNT2[3:0]位=EIVTT2[3:0]位）

Note:
- m = A, B
- 当预期的跳过计数器设置为不计数时（EIVTCk[1:0]位=00b或EIVTTk[3:0]位=0x0），不执行跳过。(k=1 2)
- 当EADTmL[2:0]位设置为011b或111b时，并且当跳过计数器1或2之一设置为不计数时，不执行跳过。

21.2.36 GTEITLB：通用PWM定时器扩展缓冲区传输跳过设置 Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xB4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	EBTLDVD[2:0]			—	EBTLDVU[2:0]			—	EBTLADB[2:0]			—	EBTLADA[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	EBTLPR[2:0]			—	EBTLCB[2:0]			—	EBTLCA[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	EBTLCA[2:0]	GTCCRA寄存器缓冲区传输扩展跳过功能选择 见表21.8。	R/W
3	—	该位读取为0。写入值应为0。	R/W
6:4	EBTLCB[2:0]	GTCCRB寄存器缓冲区传输扩展跳过功能选择 见表21.8。	R/W
7	—	该位读取为0。写入值应为0。	R/W
10:8	EBTLPR[2:0]	GTPR寄存器缓冲区传输扩展跳过功能选择 见表21.8。	R/W*1
15:11	—	这些位被读取为0。写入值应为0。	R/W
18:16	EBTLADA[2:0]	GTADTRA寄存器缓冲区传输扩展跳过功能选择 见表21.8。	R/W
19	—	该位读取为0。写入值应为0。	R/W
22:20	EBTLADB[2:0]	GTADTRB寄存器缓冲区传输扩展跳过功能选择 见表21.8。	R/W
23	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
26:24	EBTLDVU[2:0]	GTDVU Register Buffer Transfer Extended Skipping Function Select See Table 21.8.	R/W
27	—	This bit is read as 0. The write value should be 0.	R/W
30:28	EBTLDVD[2:0]	GTDVD Register Buffer Transfer Extended Skipping Function Select See Table 21.8.	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.

The GTEITLB register sets the extended skipping function for buffer transfers.

Setting only this register does not perform skipping. The GTEITC register should be set so that a corresponding extended interrupt skipping counter operates the counting.

The setting is operated independently from the interrupt skipping by the GTITC register.

The buffer transfer from the GTOLBR register to the GTIOR.GTIOA[4:0], GTIOB[4:0] bits is not target of the extended buffer transfer skipping function.

The setting is invalid during the event count operation.

EBTLCA[2:0] bit (GTCCRA Register Buffer Transfer Extended Skipping Function Select)

These bits select the extended buffer transfer skipping function to skip buffer transfers (transfers among the GTCCRA, GTCCRC, GTCCRD registers and a temporary register A) in the GTCCRA register. See Table 21.8.

An extended skipping of buffer transfers in the GTCCRA register is valid for forcible buffer transfers by the GTBER.CCRSWT bit while the count operation is stopped. Forcible buffer transfers in the GTCCRA register should be performed in the condition of not performing the extended buffer transfer skipping.

The buffer transfer between the GTCCRC, GTCCRE, and GTCCRA in complementary PWM mode can not be skipped.

EBTLCB[2:0] bit (GTCCRB Register Buffer Transfer Extended Skipping Function Select)

These bits select the extended buffer transfer skipping function to skip buffer transfers (transfers among the GTCCRB, GTCCRE, GTCCRF registers and a temporary register B) in the GTCCRB register. See Table 21.8.

An extended skipping of buffer transfers in the GTCCRB register is valid for forcible buffer transfers by the GTBER.CCRSWT bit while the count operation is stopped. Forcible buffer transfers in the GTCCRB register should be performed in the condition of not performing the extended buffer transfer skipping.

EBTLPR[2:0] bit (GTPR Register Buffer Transfer Extended Skipping Function Select)

These bits select the extended buffer transfer skipping function to skip buffer transfers (transfers among the GTPR, GTPBR, and GTPDBR registers) in the GTPR register. See Table 21.8.

If the buffer transfer of GTPR is skipped in complementary PWM mode, GTEITC setting of slave channel should be matched to the master channel so that the buffer transfer timing of the slave channel matches the master channel.

EBTLADm[2:0] bits (GTADTRm Register Buffer Transfer Extended Skipping Function Select) (m = A, B)

These bits select the extended buffer transfer skipping function to skip buffer transfers (transfers among the GTADTRm, GTADTBRm, and GTADTDBRm registers) in the GTADTRm register. See Table 21.8.

EBTLDVm[2:0] bits (GTDVm Register Buffer Transfer Extended Skipping Function Select) (m = U, D)

These bits select the extended buffer transfer skipping function to skip buffer transfers (transfers between the GTDVm and GTDBm registers) in the GTDVm register. See Table 21.8.

Table 21.8 Setting the Function Select for the GTEITLB Register (1 of 2)

EBTLx[2:0] bits	Function
0 0 0	Do not perform an extended interrupt skipping
0 0 1	Skip a buffer transfer in the period when the value for the extended interrupt skipping counter 1 is other than 0 (Buffer is transferred in the period of the EITCNT1[3:0] bits = 0)

Bit	Symbol	Function	R/W
26:24	EBTLDVU[2:0]	GTDVU寄存器缓冲区传输扩展跳过功能选择 见表21.8。	R/W
27	—	该位读取为0。写入值应为0。	R/W
30:28	EBTLDVD[2:0]	GTDVD寄存器缓冲区传输扩展跳过功能选择 见表21.8。	R/W
31	—	该位读取为0。写入值应为0。	R/W

注1.在互补PWM模式下，无论写入主通道从通道1从通道2的哪个寄存器，都会同时写入三个通道。

GTEITLB寄存器设置缓冲区传输的扩展跳过功能。

仅设置此寄存器不会执行跳过。应该设置GTEITC寄存器，以便相应的扩展中断跳过计数器操作计数。

该设置独立于GTITC寄存器的中断跳过操作。

从GTOLBR寄存器到GTIOR.GTIOA[4:0]、GTIOB[4:0]位的缓冲区传输不是扩展缓冲区传输跳过功能的目标。

该设置在事件计数操作期间无效。

EBTLCA[2:0]位（GTCCRA寄存器缓冲区传输扩展跳过功能选择）

这些位选择扩展缓冲区传输跳过功能以跳过缓冲区传输（GTCCRA之间的传输，GTCCRC、GTCCRD寄存器和GTCCRA寄存器中的一个临时寄存器A)。见表21.8。

GTCCRA寄存器中的缓冲区传输的扩展跳过对于由计数操作停止时的GTBER.CCRSWT位。GTCCRA寄存器中的强制缓冲区传输应在不执行扩展缓冲区传输跳过的情况下执行。

互补PWM模式下GTCCRC、GTCCRE和GTCCRA之间的缓冲区传输不能跳过。

EBTLCB[2:0]位（GTCCRB寄存器缓冲区传输扩展跳过功能选择）

这些位选择扩展缓冲区传输跳过功能以跳过缓冲区传输（GTCCRB之间的传输，GTCCRE、GTCCRF寄存器和一个临时寄存器B)在GTCCRB寄存器中。见表21.8。

GTCCRB寄存器中的缓冲区传输的扩展跳过对于由计数操作停止时的GTBER.CCRSWT位。GTCCRB寄存器中的强制缓冲区传输应在不执行扩展缓冲区传输跳过的情况下执行。

EBTLPR[2:0]位（GTPR寄存器缓冲区传输扩展跳过功能选择）

这些位选择扩展缓冲区传输跳过功能以跳过GTPR寄存器中的缓冲区传输（GTPR、GTPBR和GTPDBR寄存器之间的传输）。见表21.8。

如果在互补PWM模式下跳过GTPR的缓冲传输，则从通道的GTEITC设置应与主通道匹配，以使从通道的缓冲传输时序与主通道匹配。

EBTLADm[2:0]位（GTADTRm寄存器缓冲区传输扩展跳过功能选择）（m=A，B）

这些位选择扩展缓冲区传输跳过功能以跳过缓冲区传输（GTADTRm之间的传输，GTADTRm寄存器中的GTADTDBRm和GTADTDBRm寄存器）。见表21.8。

EBTLDVm[2:0]位（GTDVm寄存器缓冲区传输扩展跳过功能选择）（m=U，D）

这些位选择扩展缓冲区传输跳过功能以跳过缓冲区传输（GTDVm和GTDBm寄存器）在GTDVm寄存器中。见表21.8。

Table 21.8 设置GTEITLB寄存器的功能选择(1of2)

EBTLx[2:0] bits	Function
0 0 0	不要执行扩展的中断跳过
0 0 1	在扩展中断跳过计数器1的值不为0时跳过缓冲区传输（在EITCNT1[3:0]位=0期间传输缓冲区）

Table 21.8 Setting the Function Select for the GTEITLB Register (2 of 2)

EBTLx[2:0] bits	Function
0 1 0	Skip a buffer transfer in the period when the value for the extended interrupt skipping counter 2 is other than 0 (Buffer is transferred in the period of the EITCNT2[3:0] bits = 0)
0 1 1	Skip a buffer transfer in the period when the value for the extended interrupt skipping counter 1 or 2 is other than 0 (Buffer is transferred in the period of the EITCNT1[3:0] bits = 0 and the EITCNT2[3:0] bits = 0)
1 0 0	Setting prohibited
1 0 1	Skip a buffer transfer in the period when the value for the extended interrupt skipping counter 1 is other than the skipping count (Buffer is transferred in the period of the EITCNT1[3:0] bits = the EIVTT1[3:0] bits)
1 1 0	Skip a buffer transfer in the period when the value for the extended interrupt skipping counter 2 is other than the skipping count (Buffer is transferred in the period of the EITCNT2[3:0] bits = the EIVTT2[3:0] bits)
1 1 1	Skip a buffer transfer in the period when the value for the extended interrupt skipping counter 1 or 2 is other than the skipping count (Buffer is transferred in the period of the EITCNT1[3:0] bits = the EIVTT1[3:0] bits and the EITCNT2[3:0] bits = the EIVTT2[3:0] bits)

Note:
- x = CA, CB, PR, ADA, ADB, DVU, DVD
- When the intended skipping counter is set as not to count (EIVTCk[1:0]bits = 00b or EIVTTk[3:0] bits = 0x0), skipping is not performed. (k = 1, 2)
- When the EBTLx[2:0] bits are set to 011b or 111b, and when one of the skipping counter 1 or 2 is set as not to count, skipping is not performed.

21.2.37 GTICLF : General PWM Timer Inter Channel Logical Operation Function Setting Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xB8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	ICLFSELD[5:0]						—	ICLFB[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ICLFSELC[5:0]						—	ICLFA[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ICLFA[2:0]	GTIOCnA Output Logical Operation Function Select 0 0 0: A (no delay) 0 0 1: NOT A (no delay) 0 1 0: C (1GTCLK delay) 0 1 1: NOT C (1GTCLK delay) 1 0 0: A AND C (1GTCLK delay)*2 1 0 1: A OR C (1GTCLK delay)*2 1 1 0: A EXOR C (1GTCLK delay)*2 1 1 1: A NOR C (1GTCLK delay)*2	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W

Table 21.8 设置GTEITLB寄存器的功能选择(2of2)

EBTLx[2:0] bits	Function
0 1 0	在扩展中断跳过计数器2的值不为0时跳过缓冲区传输（在EITCNT2[3:0]位=0期间传输缓冲区）
0 1 1	在扩展中断跳过计数器1或2的值不为0时跳过缓冲区传输（缓冲区在EITCNT1[3:0]位=0和EITCNT2[3:0]位的周期内传输）=0）
1 0 0	禁止设定
1 0 1	在扩展中断跳过计数器1的值不是跳过计数的周期内跳过缓冲区传输（缓冲区在EITCNT1[3:0]位=EIVTT1[3:0]位的周期内传输）
1 1 0	在扩展中断跳过计数器2的值不是跳过计数的周期内跳过缓冲区传输（缓冲区在EITCNT2[3:0]位=EIVTT2[3:0]位的周期内传输）
1 1 1	在扩展中断跳过计数器1或2的值不是跳过计数的周期内跳过缓冲区传输（缓冲区在EITCNT1[3:0]位=EIVTT1[3:0]位的周期内传输）EITCNT2[3:0]位=EIVTT2[3:0]位）

Note:
- x=CA、CB、PR、ADA、ADB、DVU、DVD
- 当预期的跳跃计数器设置为不计数时（EIVTCk[1:0]位=00b或EIVTTk[3:0]位=0x0），不执行跳跃。(k=1 2)
- 当EBTLx[2:0]位设置为011b或111b时，并且当跳过计数器1或2之一设置为不计数时，不执行跳过。

21.2.37 GTICLF:通用PWM定时器通道间逻辑运算功能设置 Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xB8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	ICLFSELD[5:0]						—	ICLFB[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ICLFSELC[5:0]						—	ICLFA[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ICLFA[2:0]	GTIOCnA输出逻辑运算功能选择 000：A（无延迟）001：NOTA（无延迟）010：C（1GTCLK延迟）011：NOTC（1GTCLK延迟）100：AANDC（1GTCLK延迟）*2 101: A OR C (1GTCLK delay)*2 110: A EXOR C (1GTCLK delay)*2 111: A NOR C (1GTCLK delay)*2	R/W
3	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
9:4	ICLFSELC[5:0]	Inter Channel Signal C Select*1*2 0x00: GTIOC0A 0x01: GTIOC0B 0x02: GTIOC1A 0x03: GTIOC1B 0x04: GTIOC2A 0x05: GTIOC2B 0x06: GTIOC3A 0x07: GTIOC3B ⋮ ⋮ 0x3E: GTIOC31A 0x3F: GTIOC31B	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
18:16	ICLFB[2:0]	GTIOCnB Output Logical Operation Function Select 0 0 0: B (no delay) 0 0 1: NOT B (no delay) 0 1 0: D (1GTCLK delay) 0 1 1: NOT D (1GTCLK delay) 1 0 0: B AND D (1GTCLK delay)*3 1 0 1: B OR D (1GTCLK delay)*3 1 1 0: B EXOR D (1GTCLK delay)*3 1 1 1: B NOR D (1GTCLK delay)*3	R/W
19	—	This bit is read as 0. The write value should be 0.	R/W
25:20	ICLFSELD[5:0]	Inter Channel Signal D Select*1*3 0x00: GTIOC0A 0x01: GTIOC0B 0x02: GTIOC1A 0x03: GTIOC1B 0x04: GTIOC2A 0x05: GTIOC2B 0x06: GTIOC3A 0x07: GTIOC3B ⋮ ⋮ 0x3E: GTIOC31A 0x3F: GTIOC31B	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The signal before performing output disable control is selected.
Note 2. When channel's own GTIOCnA is selected, C is treated as "1".
Note 3. When channel's own GTIOCnB is selected, D is treated as "1".

The GTICLF register sets the logical operation function between compare match outputs. The logical operation is performed with the signals that the duty 0%/100% control is performed after compare match control. (The output disable control is performed with the signal after logical operation.)

Access in 8-bit units to GTICLF is prohibited.

ICLFm[2:0] bit (GTIOCm Output Logical Operation Function Select) (m = A, B)

These bits select the logical operation function between signals before performing output disable control for GTIOCm. To prevent hazard to the GPT output, the signal after logical operation is latched with GTCLK. After latching, the output disable control is performed. When the logical operation function which causes the delay of 1 GTCLK is selected, the output enable signal is also delayed with 1 GTCLK and input to the output disable control.

When the same signal to operate logical function AND, OR, EXOR and NOR is selected, one signal is treated as "1".

ICLFSELk[5:0] bit (Inter Channel Signal k Select) (k = C, D)

These bits select the signal k that the logical operation is performed with the signal before performing output disable control for GTIOCnm.

Bit	Symbol	Function	R/W
9:4	ICLFSELC[5:0]	通道间信号C选择*1*2 0x00: GTIOC0A 0x01: GTIOC0B 0x02: GTIOC1A 0x03: GTIOC1B 0x04: GTIOC2A 0x05: GTIOC2B 0x06: GTIOC3A 0x07: GTIOC3B ⋮ ⋮ 0x3E: GTIOC31A 0x3F: GTIOC31B	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W
18:16	ICLFB[2:0]	GTIOCnB输出逻辑运算功能选择 000：B（无延迟）001：NOTB（无延迟）010：D（1GTCLK延迟）011：NOTD（1GTCLK延迟）100：BANDD（1GTCLK延迟）*3 1 0 1: B OR D (1GTCLK delay)*3 1 1 0: B EXOR D (1GTCLK delay)*3 1 1 1: B NOR D (1GTCLK delay)*3	R/W
19	—	该位读取为0。写入值应为0。	R/W
25:20	ICLFSELD[5:0]	通道间信号D选择*1*3 0x00: GTIOC0A 0x01: GTIOC0B 0x02: GTIOC1A 0x03: GTIOC1B 0x04: GTIOC2A 0x05: GTIOC2B 0x06: GTIOC3A 0x07: GTIOC3B ⋮ ⋮ 0x3E: GTIOC31A 0x3F: GTIOC31B	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

注1.选择执行输出禁用控制之前的信号。注意2.选择频道自己的GTIOCNA时，C将其视为"1"。注意3.选择频道自己的GTIOCNB时，D将视为"1"。

GTICLF寄存器设置比较匹配输出之间的逻辑运算功能。通过比较匹配控制后执行占空比0%100%控制的信号执行逻辑运算。（输出禁止控制是通过逻辑运算后的信号进行的。）

禁止以8位为单位访问GTICLF。

ICLFm[2:0]位（GTIOCm输出逻辑运算功能选择）（m=A B）

这些位在执行GTIOCm的输出禁用控制之前选择信号之间的逻辑运算功能。为防止对GPT输出造成危害，逻辑运算后的信号由GTCLK锁存。锁存后，执行输出禁用控制。Whenthelogicaloperationfunctionwhichcausesthedelayof1GTCLKisselected theoutputenablesignalisalsodelayedwith1GTCLKandinputtotheoutputdisablecontrol.

当相同的信号运行逻辑函数，或者选择exorand也没有选择时，一个信号被视为"1"。

ICLFSELk[5:0]位（通道间信号k选择）（k=C D）

这些位选择在执行GTIOCnm的输出禁用控制之前的信号执行逻辑运算的信号k。

21.2.38 GTPC : General PWM Timer Period Count Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)

Offset address: 0xBC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	PCNT[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ASTP	—	—	—	—	—	—	—	PCEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PCEN	Period Count Function Enable 0: Period count function is disabled 1: Period count function is enabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
8	ASTP	Automatic Stop Function Enable 0: Automatic stop function is disabled 1: Automatic stop function is enabled	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
27:16	PCNT[11:0]	Period Counter Counter for the number of period	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The GTPC register counts the number of period.

PCEN bit (Period Count Function Enable)

This bit enables or disables period count function.

Writing is available when counting is both in progress and stopped.

When 1 is written to either the GTSECR.SPCE bit or the GTSECR.SPCD bit, the value is simultaneously set to the PCEN bit in the channels set to 1 by the GTSECSR register.

ASTP bit (Automatic Stop Function Enable)

This bit enables or disables the GTCNT counter automatic stopping after finishing counting the number of period.

When the PCEN bis is 0, writing is available.

When the PCEN bit is 1, writing is disabled.

When the PCEN bit is 1, the ASTP bit is 1, and the PCNT counter is stopped at PCNT = 0, the GTCNT counter is also stopped. When the ASTP bit is 0, the GTCNT counter continues to count.

PCNT[11:0] bit (Period Counter)

This counter counts the number of period.

When the PCEN bis is 0, writing the number of period is available.

When the PCEN bit is 1, writing is disabled, and down-counting is performed at the end of period. In saw-wave mode, the end of period refers to overflow, underflow, or counter clearing. In triangle-wave mode or complementary PWM mode, it refers to trough.

When the PCNT counter is 1 at the end of period, it becomes 0 and counting is stopped.

When the GTCNT counter is stopped while period count function is enabled, the PCNT counter keeps its value. When the GTCNT counter restarts counting and the PCEN bit is 1, the PCNT counter restarts down-counting from the hold value.

21.2.38 GTPC：通用PWM定时器周期计数寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)

Offset address: 0xBC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	PCNT[11:0]											
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ASTP	—	—	—	—	—	—	—	PCEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PCEN	周期计数功能启用 0：周期计数功能无效1：周期计数功能有效	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
8	ASTP	自动停止功能启用 0：自动停机功能无效1：自动停机功能有效	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
27:16	PCNT[11:0]	周期计数器 周期数计数器	R/W
31:28	—	这些位被读取为0。写入值应为0。	R/W

GTPC寄存器计算周期数。

PCEN位（周期计数功能使能）

该位启用或禁用周期计数功能。

当计数正在进行和停止时，可以写入。

当1写入GTSECR.SPCE位或GTSECR.SPCD位时，该值同时设置到由GTSECSR寄存器设置为1的通道中的PCEN位。

ASTP位（自动停止功能使能）

该位使能或禁止GTCNT计数器在完成周期数计数后自动停止。

当PCENbis为0时，可以写入。

当PCEN位为1时，禁止写入。

当PCEN位为1，ASTP位为1，PCNT计数器在PCNT=0时停止，GTCNT计数器也停止。当ASTP位为0时，GTCNT计数器继续计数。

PCNT[11:0] bit (Period Counter)

该计数器计算周期数。

当PCENbis为0时，可写入周期数。

当PCEN位为1时，写入被禁止，并且在周期结束时执行递减计数。在锯齿波模式下，周期结束是指上溢、下溢或计数器清零。在三角波模式或互补PWM模式下，它是指波谷。

当PCNT计数器在周期结束时为1时，它变为0并停止计数。

当GTCNT计数器停止而周期计数功能使能时，PCNT计数器保持其值。当。。。的时候GTCNT计数器重新开始计数且PCEN位为1，PCNT计数器重新从保持值开始向下计数。

When the PCEN bit is changed from 0 to 1 while the PCNT counter is 0 and the ASTP bit is 1, the GTCNT counter is stopped at the count clock immediately after that.

21.2.39 GTADCMSC : General PWM Timer A/D Conversion Start Request Compare Match Skipping Control Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 4 to 9)

Offset address: 0xC0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ADCMSCNT2[3:0]				ADCMSCNT2IV[3:0]				ADCMST2[3:0]				—	—	ADCMSC2[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADCMSCNT1[3:0]				ADCMSCNT1IV[3:0]				ADCMST1[3:0]				—	—	ADCMSC1[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ADCMSC1[1:0]	A/D Conversion Start Request Compare Match Skipping Counter 1 Count Source Select 0 0: Not counted (not skipped) 0 1: Counting GTADTRA register compare match 1 0: Counting GTADTRB register compare match 1 1: Counting both GTADTRA register compare match and GTADTRB register compare match	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
7:4	ADCMST1[3:0]	A/D Conversion Start Request Compare Match Skipping 1 Skipping Count Setting Skipping count for the A/D conversion start request compare match skipping 1.	R/W
11:8	ADCMSCNT1IV[3:0]	A/D Conversion Start Request Compare Match Skipping Counter 1 Initial Value	R/W*1
15:12	ADCMSCNT1[3:0]	A/D Conversion Start Request Compare Match Skipping Counter 1	R
17:16	ADCMSC2[1:0]	A/D Conversion Start Request Compare Match Skipping Counter 2 Count Source Select 0 0: Not counted (not skipped) 0 1: Counting GTADTRA register compare match 1 0: Counting GTADTRB register compare match 1 1: Counting both GTADTRA register compare match and GTADTRB register compare match	R/W
19:18	—	These bits are read as 0. The write value should be 0.	R/W
23:20	ADCMST2[3:0]	A/D Conversion Start Request Compare Match Skipping 2 Skipping Count Setting Skipping count for the A/D conversion start request compare match skipping 2	R/W
27:24	ADCMSCNT2IV[3:0]	A/D Conversion Start Request Compare Match Skipping Counter 2 Initial Value	R/W*2
31:28	ADCMSCNT2[3:0]	A/D Conversion Start Request Compare Match Skipping Counter 2	R

Note 1. Writing is possible only when the ADCMSC1[1:0] bits are 00b and a value other than 00b is written to the ADCMSC1[1:0] bits.
Note 2. Writing is possible only when the ADCMSC2[1:0] bits are 00b and a value other than 00b is written to the ADCMSC2[1:0] bits.

The GTADCMSC register is a register that controls the skipping counter of the A/D conversion start request compare match skipping function that counts compare matches of GTADTRA register and GTADTRB register, and skipping A/D conversion start request and buffer transfer independently.

This register setting is operated independently from the interrupt skipping by the GTITC register or GTEITC register.

Access in 8-bit units to GTADCMSC is prohibited.

ADCMSCk[1:0] bits (A/D Conversion Start Request Compare Match Skipping Counter k Count Source Select) (k = 1, 2)

These bits select the way of counting for the A/D conversion start request compare match skipping counter k.

当PCEN位从0变为1且PCNT计数器为0且ASTP位为1时，GTCNT计数器立即在计数时钟处停止。

21.2.39 GTADCMSC:通用PWM定时器AD转换开始请求比较匹配跳过控制寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 4 to 9)

Offset address: 0xC0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ADCMSCNT2[3:0]				ADCMSCNT2IV[3:0]				ADCMST2[3:0]				—	—	ADCMSC2[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADCMSCNT1[3:0]				ADCMSCNT1IV[3:0]				ADCMST1[3:0]				—	—	ADCMSC1[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ADCMSC1[1:0]	AD转换开始请求比较匹配跳过计数器1计数源选择 00：不计数（不跳过）01：计数GTADTRA寄存器比较匹配10：计数GTADTRB寄存器比较匹配11：计数GTADTRA寄存器比较匹配和GTADTRB寄存器比较匹配	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
7:4	ADCMST1[3:0]	AD转换开始请求比较匹配跳过1跳过计数设置 AD转换开始请求比较匹配跳过1的跳过计数。	R/W
11:8	ADCMSCNT1IV[3:0]	AD转换开始请求比较匹配跳过计数器1初始值	R/W*1
15:12	ADCMSCNT1[3:0]	AD转换开始请求比较匹配跳过计数器1	R
17:16	ADCMSC2[1:0]	AD转换开始请求比较匹配跳过计数器2计数源选择 00：不计数（不跳过）01：计数GTADTRA寄存器比较匹配10：计数GTADTRB寄存器比较匹配11：计数GTADTRA寄存器比较匹配和GTADTRB寄存器比较匹配	R/W
19:18	—	这些位被读取为0。写入值应为0。	R/W
23:20	ADCMST2[3:0]	AD转换开始请求比较匹配跳过2跳过计数设置 AD转换开始请求比较匹配跳过的跳过计数2	R/W
27:24	ADCMSCNT2IV[3:0]	AD转换开始请求比较匹配跳过计数器2初始值	R/W*2
31:28	ADCMSCNT2[3:0]	AD转换开始请求比较匹配跳过计数器2	R

注1.仅当ADCMSC1[1:0]位为00b并且00b以外的值写入ADCMSC1[1:0]位时，才可以写入。注2.仅当ADCMSC2[1:0]位为00b并且00b以外的值写入ADCMSC2[1:0]位时，才可以写入。

GTADCMSC寄存器是控制AD转换开始请求比较匹配跳过功能的跳过计数器的寄存器，该功能对GTADTRA寄存器和GTADTRB寄存器的比较匹配进行计数，并独立跳过AD转换开始请求和缓冲区传输。

该寄存器设置独立于GTITC寄存器或GTEITC寄存器的中断跳过操作。

禁止以8位为单位访问GTADCMSC。

ADCMSCk[1:0]位（AD转换开始请求比较匹配跳过计数器k计数源Select) (k = 1, 2)

这些位选择AD转换开始请求比较匹配跳过计数器k的计数方式。

Setting only with these bits does not skip the A/D conversion start requests and buffer transfers. Skipping function for the A/D conversion start request and buffer transfer which are a target of skipping is set individually with the GTADCMSS register.

ADCMSTk[3:0] bits (A/D Conversion Start Request Compare Match Skipping k Skipping Count Setting) (k = 1, 2)

A count for the period with continuous skipping is set as a skipping count, where a period is from a generation of a count source selected by the ADCMSCk[1:0] bits to the next generation of the count source.

When the count source is generated while the ADCMSTk[3:0] bits match the ADCMSCNTk[3:0] bits, the ADCMSCNTk[3:0] bits are cleared.

When these bits are 0x0, skipping is not performed.

ADCMSCNTkIV[3:0] bits (A/D Conversion Start Request Compare Match Skipping Counter k Initial Value) (k = 1, 2)

These bits are the value of the initial value for the A/D conversion start request compare match skipping counter k.

Writing to the ADCMSCNTkIV[3:0] is performed only when the writing value to the ADCMSCk[1:0] bits are other than 00b and when the GTADCMSC register is written by the access of 16 bits or 32 bits while the ADCMSCNTk[3:0] bits are set not to count (ADCMSCk[1:0] bits are 00b). When the ADCMSCNTkIV[3:0] bits are written, the value written to the ADCMSCNTkIV[3:0] bits is written to the ADCMSCNTk[3:0] bits simultaneously.

The writing to the ADCMSCNTkIV[3:0] bits are ignored when the ADCMSCNTk[3:0] bits are set to count (ADCMSCk[1:0] bits are other than 00b) or perform the setting of not to count (00b is written to the ADCMSCk[1:0] bits).

The ADCMSCNTkIV[3:0] bits are not reset by the writing 00b to the ADCMSCk[1:0] bits.

ADCMSCNTk[3:0] bits (A/D Conversion Start Request Compare Match Skipping Counter k) (k=1,2)

The counting is incremented by 1 every time a count source selected by the ADCMSCk[1:0] bits is generated.

Counting is performed periodically within the range between 0 and the ADCMSTk[3:0] bits.

Even if the GTCNT counter is stopped, the value is not cleared, and value at stop of the GTCNT counter is retained.

Setting of the initial value for the ADCMSCNTk[3:0] bits are performed only when the writing value to the ADCMSCk[1:0] bits are other than 00b and when the GTADCMSC register is written by the access of 16 bits or 32 bits while the A/D conversion start request compare match skipping counter k is set as not to count (ADCMSCk[1:0] bits are 00b).

When the initial value is set, the written value to the ADCMSCNTkIV[3:0] bits is written to the ADCMSCNTk[3:0] bits as the initial value.

[Clearing condition]

- 00b is written to the ADCMSCk[1:0] bits.
- 0x0 is written to the ADCMSTk[3:0] bits.
- The value other than 00b is written to the ADCMSCk[1:0] bits and the 0x0 is written to the ADCMSCNTkIV[3:0] bits simultaneously while 00b is set to the ADCMSCk[1:0] bits.
- A count source selected by the ADCMSCk[1:0] bits is generated when the extended interrupt skipping 2 skipping count set by the ADCMSTk[3:0] bits match the value for the ADCMSCNTk[3:0].

仅用这些位设置不会跳过AD转换开始请求和缓冲区传输。的跳过功能
作为跳过目标的D转换开始请求和缓冲区传输由GTADCMSS寄存器单独设置。

ADCMSTk[3:0]位（AD转换开始请求比较匹配跳过k跳过计数设置）（k=1 2）

将连续跳过的周期的计数设置为跳过计数，其中周期是从ADCMSCk[1:0]位选择的计数源的一代到下一代计数源。

当在ADCMSTk[3:0]位与ADCMSCNTk[3:0]位匹配时产生计数源时，
ADCMSCNTk[3:0]位被清零。

当这些位为0x0时，不执行跳过。

ADCMSCNTkIV[3:0]位（AD转换开始请求比较匹配跳过计数器k初始值）（k=1 2）

这些位是AD转换开始请求比较匹配跳过计数器k的初始值。

仅当ADCMSCk[1:0]位的写入值不是00b并且通过16位或32位访问写入GTADCMSC寄存器而ADCMSCNTk[3:0]位设置为不计数（ADCMSCk[1:0]位为00b）。写入ADCMSCNTkIV[3:0]位时，写入ADCMSCNTkIV[3:0]位的值会同时写入ADCMSCNTk[3:0]位。

当ADCMSCNTk[3:0]位设置为计数（ADCMSCk[1:0]位不是00b）或执行不计数设置（00b为写入ADCMSCk[1:0]位）。

ADCMSCNTkIV[3:0]位不会通过将00b写入ADCMSCk[1:0]位来复位。

ADCMSCNTk[3:0]位（AD转换开始请求比较匹配跳过计数器k）（k=1 2）

每次产生由ADCMSCk[1:0]位选择的计数源时，计数就加1。

在0和ADCMSTk[3:0]位之间的范围内定期执行计数。

即使GTCNT计数器停止，该值也不会被清除，而是保留GTCNT计数器停止时的值。

ADCMSCNTk[3:0]位的初始值设置仅在写入值到
ADCMSCk[1:0]位不是00b并且当通过16位或32位访问写入GTADCMSC寄存器同时AD转换开始请求比较匹配跳过计数器k设置为不计数时（ADCMSCk[1:0]位为00b)。

设置初始值后，写入ADCMSCNTkIV[3:0]位的值将作为初始值写入ADCMSCNTk[3:0]位。

[Clearing condition]

●00b写入ADCMSCk[1:0]位。

●0x0写入ADCMSTk[3:0]位。

●00b以外的值被写入ADCMSCk[1:0]位，同时0x0被写入ADCMSCNTkIV[3:0]位，同时00b被设置到ADCMSCk[1:0]位。

●当ADCMSCTk[3:0]位设置的扩展中断跳过2跳过计数与ADCMSCNTk[3:0]的值匹配时，会生成一个由ADCMSCk[1:0]位选择的计数源。

21.2.40 GTADCMSS : General PWM Timer A/D Conversion Start Request Compare Match Skipping Setting Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 4 to 9)

Offset address: 0xC4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	ADCMBSB[2:0]			—	ADCMBSA[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	ADCMSBL[2:0]			—	ADCMSAL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ADCMSAL[2:0]	GTADTRA Register A/D Conversion Start Request Compare Match Skipping Function Select See Table 21.9.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	ADCMSBL[2:0]	GTADTRB Register A/D Conversion Start Request Compare Match Skipping Function Select See Table 21.9.	R/W
15:7	—	These bits are read as 0. The write value should be 0.	R/W
18:16	ADCMBSA[2:0]	GTADTRA Register Buffer Transfer by A/D Conversion Start Request Compare Match Skipping Function Select See Table 21.10.	R/W
19	—	This bit is read as 0. The write value should be 0.	R/W
22:20	ADCMBSB[2:0]	GTADTRB Register Buffer Transfer by A/D Conversion Start Request Compare Match Skipping Function Select See Table 21.10.	R/W
31:23	—	These bits are read as 0. The write value should be 0.	R/W

The GTADCMSS register is a register that selects the A/D conversion start request compare match skipping function or the GTADTRm (m = A, B) register buffer transfer by A/D conversion start request compare match skipping function.

Setting only with this register does not perform skipping. The GTADCMSC register should be set so that a corresponding A/D conversion start request compare match skipping counter operates the counting.

This register setting is operated independently from the interrupt skipping by the GTITC register or GTEITC register.

ADCMSmL[2:0] bits (GTADTRm Register A/D Conversion Start Request Compare Match Skipping Function Select) (m = A, B)

These bits select the A/D conversion start request compare match skipping function of the GTADTRm (m = A, B) register.Table 21.9.

ADCMBSm[2:0] bits (GTADTRm Register Buffer Transfer by A/D Conversion Start Request Compare Match Skipping Function Select) (m = A, B)

These bits select the GTADTRm (m = A, B) register buffer transfer by A/D conversion start request compare match skipping function which skips the buffer transfer of GTADTRm (m = A, B) register(Transfer between GTADTRm register, GTADTBRm register, GTADTDBRm register). See Table 21.10.

Table 21.9 Setting of the GTADTRm Register A/D Conversion Start Request Compare Match Skipping Function Select bit (m = A ,B) (1 of 2)

ADCMSmL[2:0]	Function
0 0 0	Do not perform an A/D conversion start request compare match skipping

21.2.40 GTADCMSS：通用PWM定时器AD转换开始请求比较匹配跳过设置寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 4 to 9)

Offset address: 0xC4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	ADCMBSB[2:0]			—	ADCMBSA[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	ADCMSBL[2:0]			—	ADCMSAL[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ADCMSAL[2:0]	GTADTRA寄存器AD转换开始请求比较匹配跳过功能 Select 见表21.9。	R/W
3	—	该位读取为0。写入值应为0。	R/W
6:4	ADCMSBL[2:0]	GTADTRB寄存器AD转换开始请求比较匹配跳过功能 Select 见表21.9。	R/W
15:7	—	这些位被读取为0。写入值应为0。	R/W
18:16	ADCMBSA[2:0]	通过AD转换开始请求比较匹配的GTADTRA寄存器缓冲区传输 跳过功能选择 见表21.10。	R/W
19	—	该位读取为0。写入值应为0。	R/W
22:20	ADCMBSB[2:0]	通过AD转换开始请求比较匹配的GTADTRB寄存器缓冲区传输 跳过功能选择 见表21.10。	R/W
31:23	—	这些位被读取为0。写入值应为0。	R/W

GTADCMSS寄存器是选择AD转换开始请求比较匹配跳过功能或
GTADTRm(m=A B)通过AD转换开始请求比较匹配跳过功能进行寄存器缓冲区传输。

仅使用该寄存器进行设置不会执行跳过。GTADCMSC寄存器应设置为相应的
D转换开始请求比较匹配跳过计数器操作计数。

该寄存器设置独立于GTITC寄存器或GTEITC寄存器的中断跳过操作。

**ADCMSmL[2:0]位（GTADTRm寄存器AD转换开始请求比较匹配跳过
Function Select) (m = A, B)**

这些位选择GTADTRm(m=A B)寄存器的AD转换开始请求比较匹配跳过功能。表21.9。

**ADCMBSm[2:0]位（通过AD转换开始请求比较的GTADTRm寄存器缓冲区传输
匹配跳过功能选择）（m=A，B）**

这些位通过AD转换开始请求比较匹配跳过功能选择GTADTRm(m=A B)寄存器缓冲区传输，该功能跳过GTADTRm(m=A B)寄存器的缓冲区传输（在GTADTRm寄存器、GTADTBRm寄存器、GTADTDBRm寄存器之间传输）。见表21.10。

**Table 21.9 GTADTRm寄存器的设置AD转换开始请求比较匹配跳过功能
选择位(m=A B)(1of2)**

ADCMSmL[2:0]	Function
0 0 0	不执行AD转换开始请求比较匹配跳过

Table 21.9 Setting of the GTADTRm Register A/D Conversion Start Request Compare Match Skipping Function Select bit (m = A ,B) (2 of 2)

ADCMSmL[2:0]	Function
0 0 1	Skip an A/D conversion start request in the period when the value for the A/D conversion start request compare match skipping counter 1 is other than 0 (An A/D conversion start request is output in the period of the ADCMSCNT1[3:0] bits = 0)
0 1 0	Skip an A/D conversion start request in the period when the value for the A/D conversion start request compare match skipping counter 2 is other than 0 (An A/D conversion start request is output in the period of the ADCMSCNT2[3:0] bits = 0)
0 1 1	Skip an A/D conversion start request in the period when the value for the A/D conversion start request compare match skipping counter 1 or 2 is other than 0 (An A/D conversion start request is output in the period of the ADCMSCNT1[3:0] bits = 0 and the ADCMSCNT2[3:0] bits = 0)
1 0 0	Setting prohibited
1 0 1	Skip an A/D conversion start request in the period when the value for the A/D conversion start request compare match skipping counter 1 is other than the skipping count (An A/D conversion start request is output in the period of the ADCMSCNT1[3:0] bits = the ADCMST1[3:0] bits)
1 1 0	Skip an A/D conversion start request in the period when the value for the A/D conversion start request compare match skipping counter 2 is other than the skipping count (An A/D conversion start request is output in the period of the ADCMSCNT2[3:0] bits = the ADCMST2[3:0] bits)
1 1 1	Skip an A/D conversion start request in the period when the value for the A/D conversion start request compare match skipping counter 1 or 2 is other than the skipping count (An A/D conversion start request is output in the period of the ADCMSCNT1[3:0] bits = the ADCMST1[3:0] bits and the ADCMSCNT2[3:0] bits = the ADCMST2[3:0] bits)

Note:
- m = A, B
- When the intended skipping counter is set as not to count (the ADCMSCk[1:0] bits = 00b or the ADCMSTk[3:0] bits = 0x0), skipping is not performed. (k = 1, 2)
- When the ADCMSmL[2:0] bits are set to 011b or 111b, and when one of the skipping counters is set as not to count, skipping is not performed.

Table 21.10 Setting of the GTADTRm Register Buffer Transfer by A/D Conversion Start Request Compare Match Skipping Function Select bit (m = A, B)

ADCMBSm[2:0]	Function
0 0 0	Do not perform an GTADTRm register buffer transfer by A/D conversion start request compare match skipping
0 0 1	Skip a buffer transfer in the period when the value for the A/D conversion start request compare match skipping counter 1 is other than 0 (Buffer is transferred in the period of the ADCMSCNT1[3:0] bits = 0)
0 1 0	Skip a buffer transfer in the period when the value for the A/D conversion start request compare match skipping counter 2 is other than 0 (Buffer is transferred in the period of the ADCMSCNT2[3:0] bits = 0)
0 1 1	Skip a buffer transfer in the period when the value for the A/D conversion start request compare match skipping counter 1 or 2 is other than 0 (Buffer is transferred in the period of the ADCMSCNT1[3:0] bits = 0 and the ADCMSCNT2[3:0] bits = 0)
1 0 0	Setting prohibited
1 0 1	Skip a buffer transfer in the period when the value for the A/D conversion start request compare match skipping counter 1 is other than the skipping count (Buffer is transferred in the period of the ADCMSCNT1[3:0] bits = the ADCMST1[3:0] bits)
1 1 0	Skip a buffer transfer in the period when the value for the A/D conversion start request compare match skipping counter 2 is other than the skipping count (Buffer is transferred in the period of the ADCMSCNT2[3:0] bits = the ADCMST2[3:0] bits)
1 1 1	Skip a buffer transfer in the period when the value for the A/D conversion start request compare match skipping counter 1 or 2 is other than the skipping count (A Buffer is transferred in the period of the ADCMSCNT1[3:0] bits = the ADCMST1[3:0] bits and the ADCMSCNT2[3:0] bits = the ADCMST2[3:0] bits)

Note:
- m = A, B
- When the intended skipping counter is set as not to count (the ADCMSCk[1:0] bits = 00b or the ADCMSTk[3:0] bits = 0x0), skipping is not performed. (k = 1, 2)
- When the ADCMSmL[2:0] bits are set to 011b or 111b, and when one of the skipping counters is set as not to count, skipping is not performed.

Table 21.9 GTADTRm寄存器的设置AD转换开始请求比较匹配跳过功能选择位(m=A B)(2of2)

ADCMSmL[2:0]	Function
0 0 1	在AD转换开始请求比较匹配跳过计数器1的值不为0的时段内跳过AD转换开始请求（在ADCMSCNT1[3:0]位=0的时段内输出AD转换开始请求）
0 1 0	在AD转换开始请求比较匹配跳过计数器2的值不为0时跳过AD转换开始请求（在ADCMSCNT2[3:0]位=0的时段内输出AD转换开始请求）
0 1 1	在AD转换开始请求比较匹配跳过计数器1或2的值不为0的时段内跳过AD转换开始请求（在ADCMSCNT1[3:0]位的时段内输出AD转换开始请求=0和ADCMSCNT2[3:0]位=0）
1 0 0	禁止设定
1 0 1	在AD转换开始请求比较匹配跳过计数器1的值不是跳过计数的周期内跳过AD转换开始请求（在ADCMSCNT1[3:0]位的周期内输出AD转换开始请求=ADCMST1[3:0]位）
1 1 0	在AD转换开始请求比较匹配跳过计数器2的值不是跳过计数的时段内跳过AD转换开始请求（在ADCMSCNT2[3:0]位的时段内输出AD转换开始请求=ADCMST2[3:0]位）
1 1 1	在AD转换开始请求比较匹配跳过计数器1或2的值不是跳过计数的时段内跳过AD转换开始请求（在ADCMSCNT1[3:0]的时段内输出AD转换开始请求位=ADCMST1[3:0]位和ADCMSCNT2[3:0]位=ADCMST2[3:0]位）

Note:
- m = A, B
- 当预期的跳跃计数器设置为不计数时（ADCMSCk[1:0]位=00b或ADCMSTk[3:0]位=0x0），不执行跳跃。(k=1 2)
- 当ADCMSmL[2:0]位设置为011b或111b时，并且当跳过计数器之一设置为不计数时，不执行跳过。

Table 21.10 通过AD转换开始请求比较匹配设置GTADTRm寄存器缓冲区传输跳过功能选择位(m=A B)

ADCMBSm[2:0]	Function
0 0 0	不要通过AD转换开始请求比较匹配跳过执行GTADTRm寄存器缓冲区传输
0 0 1	在AD转换开始请求比较匹配跳过计数器1的值不为0时跳过缓冲区传输（在ADCMSCNT1[3:0]位=0期间传输缓冲区）
0 1 0	在AD转换开始请求比较匹配跳过计数器2的值不为0时跳过缓冲区传输（在ADCMSCNT2[3:0]位=0期间传输缓冲区）
0 1 1	在AD转换开始请求比较匹配跳过计数器1或2的值不为0时跳过缓冲区传输（在ADCMSCNT1[3:0]位=0和ADCMSCNT2[3:0]位=0）
1 0 0	禁止设定
1 0 1	在AD转换开始请求比较匹配跳过计数器1的值不是跳过计数的周期内跳过缓冲区传输（缓冲区在ADCMSCNT1[3:0]位=ADCMST1[3:0]的周期内传输]位）
1 1 0	在AD转换开始请求比较匹配跳过计数器2的值不是跳过计数的周期内跳过缓冲区传输（在ADCMSCNT2[3:0]位=ADCMST2[3:0]的周期内传输缓冲区]位）
1 1 1	当AD转换开始请求比较匹配跳过计数器1或2的值不是跳过计数时跳过缓冲区传输（在ADCMSCNT1[3:0]位=ADCMST1[3:0]位和ADCMSCNT2[3:0]位=ADCMST2[3:0]位）

Note:
- m = A, B
- 当预期的跳跃计数器设置为不计数时（ADCMSCk[1:0]位=00b或ADCMSTk[3:0]位=0x0），不执行跳跃。(k=1 2)
- 当ADCMSmL[2:0]位设置为011b或111b时，并且当跳过计数器之一设置为不计数时，不执行跳过。

21.2.41 GTSECSR : General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xD0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SECSEL9	SECSEL8	SECSEL7	SECSEL6	SECSEL5	SECSEL4	SECSEL3	SECSEL2	SECSEL1	SECSEL0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SECSEL0	Channel 0 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
1	SECSEL1	Channel 1 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
2	SECSEL2	Channel 2 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
3	SECSEL3	Channel 3 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
4	SECSEL4	Channel 4 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
5	SECSEL5	Channel 5 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
6	SECSEL6	Channel 6 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
7	SECSEL7	Channel 7 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
8	SECSEL8	Channel 8 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
9	SECSEL9	Channel 9 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

The GTSECSR register selects an intended channel n (n = 0 to 9) for updating an operation enable bit by the GTSECR register. A bit position for the GTSECSR register indicates a channel number. The GTSECSR register of each channel is a common register, and writing 1 to a bit in the GTSECSR register in any channel and updating it changes a channel, related to the position of the bit written with 1 by the GTSECSR register, to be simultaneously controlled of the operation enable bit by the GTSECR register.

Access in 8-bit or 16-bit units to GTSECSR is prohibited, and it should be accessed in 32-bit units.

21.2.41 GTSECSR：通用PWM定时器操作使能位同时控制通道选择寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xD0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SECSEL9	SECSEL8	SECSEL7	SECSEL6	SECSEL5	SECSEL4	SECSEL3	SECSEL2	SECSEL1	SECSEL0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SECSEL0	通道0操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
1	SECSEL1	通道1操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
2	SECSEL2	通道2操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
3	SECSEL3	通道3操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
4	SECSEL4	通道4操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
5	SECSEL5	通道5操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
6	SECSEL6	通道6操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
7	SECSEL7	通道7操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
8	SECSEL8	通道8操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
9	SECSEL9	通道9操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
31:10	—	这些位被读取为0。写入值应为0。	R/W

GTSECSR寄存器选择预期的通道n（n=0到9），用于通过GTSECR寄存器更新操作使能位。GTSECSR寄存器的位位置表示通道号。每个通道的GTSECSR寄存器是一个公共寄存器，在任何通道的GTSECSR寄存器中写入1并更新它会改变一个通道，与GTSECSR寄存器写入1的位的位置有关，被同时控制GTSECR寄存器的操作使能位。

禁止以8位或16位为单位访问GTSECSR，应以32位为单位进行访问。

SECSELn bit (Operation Enable Bit Simultaneous Control Channel Select) (n = 0 to 9)

This bit enables or disables the simultaneous control of operation enable in channel n.

When the bit is set to 1, the simultaneous control is enabled, and disabled when the bit is 0.

21.2.42 GTSECR : General PWM Timer Operation Enable Bit Simultaneous Control Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xD4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	SSCD	SPCD	—	—	—	—	—	—	SSCE	SPCE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	SBDDD	SBDAD	SBDPD	SBDCD	—	—	—	—	SBDDE	SBDAE	SBDPE	SBDCE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SBDCE	GTCCR Register Buffer Operation Simultaneous Enable 0: Disable simultaneous enabling GTCCR buffer operations 1: Enable GTCCR register buffer operations simultaneously	R/W
1	SBDPE	GTPR Register Buffer Operation Simultaneous Enable 0: Disable simultaneous enabling GTPR buffer operations 1: Enable GTPR register buffer operations simultaneously	R/W*1
2	SBDAE	GTADTR Register Buffer Operation Simultaneous Enable 0: Disable simultaneous enabling GTADTR buffer operations 1: Enable GTADTR register buffer operations simultaneously	R/W
3	SBDDE	GTDV Register Buffer Operation Simultaneous Enable 0: Disable simultaneous enabling GTDV buffer operations 1: Enable GTDV register buffer operations simultaneously	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	SBDCD	GTCCR Register Buffer Operation Simultaneous Disable 0: Disable simultaneous disabling GTCCR buffer operations 1: Disable GTCCR register buffer operations simultaneously	R/W
9	SBDPD	GTPR Register Buffer Operation Simultaneous Disable 0: Disable simultaneous disabling GTPR buffer operations 1: Disable GTPR register buffer operations simultaneously	R/W*1
10	SBDAD	GTADTR Register Buffer Operation Simultaneous Disable 0: Disable simultaneous disabling GTADTR buffer operations 1: Disable GTADTR register buffer operations simultaneously	R/W
11	SBDDD	GTDV Register Buffer Operation Simultaneous Disable 0: Disable simultaneous disabling GTDV buffer operations 1: Disable GTDV register buffer operations simultaneously	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
16	SPCE	Period Count Function Simultaneous Enable*2 0: Disable simultaneous enabling period count function 1: Enable period count function simultaneously	R/W
17	SSCE	Synchronous Set/Clear Simultaneous Enable 0: Disable simultaneous enabling synchronous set/clear 1: Enable synchronous set/clear simultaneously	R/W*1
23:18	—	These bits are read as 0. The write value should be 0.	R/W

SECSELn位（操作使能位同时控制通道选择）（n=0至9）

该位启用或禁用通道n中操作启用的同时控制。

该位设置为1时启用同步控制，该位设置为0时禁用同步控制。

21.2.42 GTSECR：通用PWM定时器操作使能位同时控制 Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xD4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	SSCD	SPCD	—	—	—	—	—	—	SSCE	SPCE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	SBDDD	SBDAD	SBDPD	SBDCD	—	—	—	—	SBDDE	SBDAE	SBDPE	SBDCE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SBDCE	GTCCR寄存器缓冲器操作同时使能 0：禁止同时使能GTCCR缓冲操作1：同时使能GTCCR寄存器缓冲操作	R/W
1	SBDPE	GTPR寄存器缓冲区操作同时使能 0：禁止同时使能GTPR缓冲区操作1：同时使能GTPR寄存器缓冲区操作	R/W*1
2	SBDAE	GTADTR寄存器缓冲区操作同时使能 0：禁止同时使能GTADTR缓冲区操作1：同时使能GTADTR寄存器缓冲区操作	R/W
3	SBDDE	GTDV寄存器缓冲器操作同时使能 0：禁止同时使能GTDV缓冲操作1：同时使能GTDV寄存器缓冲操作	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	SBDCD	GTCCR寄存器缓冲区操作同时禁用 0：禁用同时禁用GTCCR缓冲区操作1：同时禁用GTCCR寄存器缓冲区操作	R/W
9	SBDPD	GTPR寄存器缓冲区操作同时禁用 0：禁用同时禁用GTPR缓冲区操作1：同时禁用GTPR寄存器缓冲区操作	R/W*1
10	SBDAD	GTADTR寄存器缓冲区操作同时禁用 0：禁用同时禁用GTADTR缓冲区操作1：同时禁用GTADTR寄存器缓冲区操作	R/W
11	SBDDD	GTDV寄存器缓冲区操作同时禁用 0：禁止同时禁止GTDV缓冲操作1：同时禁止GTDV寄存器缓冲操作	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W
16	SPCE	周期计数功能同时启用*2 0：禁用同时启用周期计数功能1：同时启用周期计数功能	R/W
17	SSCE	同步设置清除同时启用 0：禁止同时使能同步清零1：使能同时清零	R/W*1
23:18	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
24	SPCD	Period Count Function Simultaneous Disable*2 0: Disable simultaneous disabling period count function 1: Disable period count function simultaneously	R/W
25	SSCD	Synchronous Set/Clear Simultaneous Disable 0: Disable simultaneous disabling synchronous set/clear 1: Disable synchronous set/clear simultaneously	R/W*1
31:26	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.
Note 2. This bit is only available in GPT320 to GPT323.
In GPT324 to GPT329, this bit is read as 0. The write value should be 0.

The GTSECR register simultaneously updates the value for operation enable bits of a channel set by the GTSECSR register.

Writing 1 to a bit in the GTSECR register in any channel and updating it updates an operation enable bit for all channels, related to the position of the bit written with 1 by the all GTSECSR registers.

Setting enable and disable bits for the same operation enable bit to 1 in the GTSECR is prohibited.

A bit written to 1 is automatically cleared. When the GTSECR is read, 0 is read.

Access in 8-bit or 16-bit units to the GTSECR register is prohibited, and it should be accessed in 32-bit units.

SBDCE bit (GTCCR Register Buffer Operation Simultaneous Enable)

When 1 is written to this bit, 0 is simultaneously set to a GTBER.BD[0] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTCCRA, GTCCRC, and GTCCRD registers and using the GTCCRB, GTCCRE, and GTCCRF registers are enabled.

Simultaneous setting of SBDCE and SBDCD bits to 1 is prohibited.

SBDPE bit (GTPR Register Buffer Operation Simultaneous Enable)

When 1 is written to this bit, 0 is simultaneously set to a GTBER.BD[1] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTPR, GTPDBR, and GTPBR registers are enabled.

Simultaneous setting of SBDPE and SBDPD bits to 1 is prohibited.

SBDAE bit (GTADTR Register Buffer Operation Simultaneous Enable)

When 1 is written to this bit, 0 is simultaneously set to a GTBER.BD[2] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTADTRA, GTADTBRA, and GTADTDBRA registers and using the GTADTRB, GTADTBRB, and GTADTDBRB registers are enabled.

Simultaneous setting of SBDAE and SBDAD bits to 1 is prohibited.

SBDDE bit (GTDV Register Buffer Operation Simultaneous Enable)

When 1 is written to this bit, 0 is simultaneously set to a GTBER.BD[3] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTDVU and GTDBU registers and using the GTDVD and GTDBD registers are enabled.

Simultaneous setting of SBDDE and SBDDD bits to 1 is prohibited.

SBDCD bit (GTCCR Register Buffer Operation Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTBER.BD[0] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTCCRA, GTCCRC, and GTCCRD registers and using the GTCCRB, GTCCRE, and GTCCRF registers are disabled.

Simultaneous setting of SBDCE and SBDCD bits to 1 is prohibited.

SBDPD bit (GTPR Register Buffer Operation Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTBER.BD[1] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTPR, GTPDBR, and GTPBR registers are disabled.

Simultaneous setting of SBDPE and SBDPD bits to 1 is prohibited.

Bit	Symbol	Function	R/W
24	SPCD	期间计数功能同时禁用*2 0：禁用同时禁用周期计数功能1：同时禁用周期计数功能	R/W
25	SSCD	同步设置清除同时禁用 0：禁止同时禁止同步设置清除1：禁止同步设置同时清除	R/W*1
31:26	—	这些位被读取为0。写入值应为0。	R/W

注1.在互补PWM模式下，无论写入主通道从通道1从通道2的哪个寄存器，都会同时写入三个通道。

注2.该位仅在GPT320至GPT323中可用。
在GPT324到GPT329中，该位读取为0。写入值应为0。

GTSECR寄存器同时更新由GTSECSR寄存器设置的通道的操作使能位的值。

将1写入任何通道的GTSECR寄存器中的某个位并更新它会更新所有通道的操作使能位，该位与所有GTSECSR寄存器写入1的位的位置有关。

禁止在GTSECR中将同一操作使能位的使能位和禁用位设置为1。

写入1的位会自动清除。读取GTSECR时，读取0。

禁止以8位或16位为单位访问GTSECR寄存器，应以32位为单位进行访问。

SBDCE位（GTCCR寄存器缓冲区操作同时使能）

向该位写入1时，同时将GTSECSR寄存器设置为1的通道中的GTBER.BD[0]位设置为0，并使用GTCCRA、GTCCRC和GTCCRD寄存器以及使用GTCCRB、GTCCRE进行缓冲操作 和GTCCRF寄存器被启用。

禁止将SBDCE和SBDCD位同时设置为1。

SBDPE位（GTPR寄存器缓冲区操作同时使能）

向该位写入1时，同时将GTSECSR寄存器设置为1的通道中的GTBER.BD[1]位设置为0，并启用使用GTPR、GTPDBR和GTPBR寄存器的缓冲操作。

禁止将SBDPE和SBDPD位同时设置为1。

SBDAE位（GTADTR寄存器缓冲区操作同时使能）

向该位写入1时，通过GTSECSR寄存器设置为1的通道中的GTBER.BD[2]位同时设置为0，并使用GTADTRA、GTADTBRA和GTADTBRA寄存器以及使用GTADTRB、GTADTBRB进行缓冲操作 和GTADTDRBB寄存器被启用。

禁止将SBDAE和SBDAD位同时设置为1。

SBDDE位（GTDV寄存器缓冲区操作同时使能）

当向该位写入1时，同时在GTSECSR寄存器设置为1的通道中将0设置为GTBER.BD[3]位，并启用使用GTDVU和GTDBU寄存器以及使用GTDVD和GTDBD寄存器的缓冲操作.

禁止将SBDDE和SBDDD位同时设置为1。

SBDCD位（GTCCR寄存器缓冲区操作同时禁用）

当向该位写入1时，同时将1设置为由GTSECSR寄存器设置为1的通道中的GTBER.BD[0]位，并使用GTCCRA、GTCCRC和GTCCRD寄存器以及使用GTCCRB、GTCCRE进行缓冲操作 和GTCCRF寄存器被禁用。

禁止将SBDCE和SBDCD位同时设置为1。

SBDPD位（GTPR寄存器缓冲区操作同时禁用）

当向该位写入1时，同时将1设置到由GTSECSR寄存器设置为1的通道中的GTBER.BD[1]位，并且禁用使用GTPR、GTPDBR和GTPBR寄存器的缓冲操作。

禁止将SBDPE和SBDPD位同时设置为1。

SBDAD bit (GTADTR Register Buffer Operation Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTBER.BD[2] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTADTRA, GTADTBRA, and GTADTDBRA registers and using the GTADTRB, GTADTBRB, and GTADTDBRB registers are disabled.

Simultaneous setting of SBDAE and SBDAD bits to 1 is prohibited.

SBDDD bit (GTDV Register Buffer Operation Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTBER.BD[3] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTDVU and GTDBU registers and using the GTDVD and GTDBD registers are disabled.

Simultaneous setting of SBDDE and SBDDD bits to 1 is prohibited.

SPCE bit (Period Count Function Simultaneous Enable)

When 1 is written to this bit, 1 is simultaneously set to GTPC.PCEN bit in the channels set to 1 by the GTSECSR register, and period count function is enabled.

Simultaneous setting of SPCE and SPCD bits to 1 is prohibited.

SSCE bit (Synchronous Set/Clear Simultaneous Enable)

When 1 is written to this bit, 1 is simultaneously set to GTCR.SSCEN bit in the channels set to 1 by the GTSECSR register and Enable synchronous set/clear function.

Simultaneous setting of SSCE and SSCD bits to 1 is prohibited.

SPCD bit (Period Count Function Simultaneous Disable)

When 1 is written to this bit, 0 is simultaneously set to GTPC.PCEN bit in the channels set to 1 by the GTSECSR register, and period count function is disabled.

Simultaneous setting of SPCE and SPCD bits to 1 is prohibited.

SSCD bit (Synchronous Set/Clear Simultaneous Disable)

When 1 is written to this bit, 0 is simultaneously set to GTCR.SSCEN bit in the channels set to 1 by the GTSECSR register and Disable synchronous set/clear function.

Simultaneous setting of SSCE and SSCD bits to 1 is prohibited.

21.2.43 GTBER2 : General PWM Timer Buffer Enable Register 2

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xE0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	OLTTB[1:0]		OLTTA[1:0]		CPBTD	CP3DB	—		CPTDV	CPTADB	CPTADA	CPTPR	CPTCB	CPTCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	CMTADB	CMTADA	—	CMTCB[1:0]		CMTCA[1:0]		—	—	CCTDV	CCTADB	CCTADA	CCTPR	CCTCB	CCTCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CCTCA	Counter Clear Source GTCCRA Register Buffer Transfer Disable 0: Enable GTCCRA register buffer transfer by counter clear 1: Disable GTCCRA register buffer transfer by counter clear	R/W
1	CCTCB	Counter Clear Source GTCCRB Register Buffer Transfer Disable 0: Enable GTCCRB register buffer transfer by counter clear 1: Disable GTCCRB register buffer transfer by counter clear	R/W

SBDAD位（GTADTR寄存器缓冲区操作同时禁用）

当向该位写入1时，同时将1设置为由GTSECSR寄存器设置为1的通道中的GTBER.BD[2]位，并使用GTADTRA、GTADTBRA和GTADTBRA寄存器以及使用GTADTRB、GTADTBRB进行缓冲操作 和GTADTDBRB寄存器被禁用。

禁止将SBDAE和SBDAD位同时设置为1。

SBDDD位（GTDV寄存器缓冲区操作同时禁用）

当向该位写入1时，同时将1设置到由GTSECSR寄存器设置为1的通道中的GTBER.BD[3]位，并且使用GTDVU和GTDBU寄存器以及使用GTDVD和GTDBD寄存器的缓冲操作被禁用.

禁止将SBDDE和SBDDD位同时设置为1。

SPCE位（周期计数功能同时使能）

向该位写入1时，通过GTSECSR寄存器设置为1的通道中的GTPC.PCEN位同时设置为1，并启用周期计数功能。

禁止将SPCE和SPCD位同时设置为1。

SSCE位（同步设置清除同时使能）

向该位写入1时，通过GTSECSR寄存器和启用同步设置清除功能将通道中的GTCR.SSCEN位同时设置为1。

禁止将SSCE和SSCD位同时设置为1。

SPCD位（周期计数功能同时禁用）

向该位写入1时，通过GTSECSR寄存器设置为1的通道中的GTPC.PCEN位同时设置为0，并且禁用周期计数功能。

禁止将SPCE和SPCD位同时设置为1。

SSCD位（同步设置清除同时禁用）

向该位写入1时，通过GTSECSR寄存器和禁用同步设置清除功能将通道中的GTCR.SSCEN位同时设置为0。

禁止将SSCE和SSCD位同时设置为1。

21.2.43 GTBER2：通用PWM定时器缓冲器使能寄存器2

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xE0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	OLTTB[1:0]		OLTTA[1:0]		CPBTD	CP3DB	—		CPTDV	CPTADB	CPTADA	CPTPR	CPTCB	CPTCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	CMTADB	CMTADA	—	CMTCB[1:0]		CMTCA[1:0]		—	—	CCTDV	CCTADB	CCTADA	CCTPR	CCTCB	CCTCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CCTCA	计数器清零源GTCCRA寄存器缓冲区传输禁用 0：通过计数器清除启用GTCCRA寄存器缓冲区传输1：通过计数器清除禁用GTCCRA寄存器缓冲区传输	R/W
1	CCTCB	计数器清零源GTCCRB寄存器缓冲区传输禁用 0：通过计数器清除启用GTCCRB寄存器缓冲区传输1：通过计数器清除禁用GTCCRB寄存器缓冲区传输	R/W

Bit	Symbol	Function	R/W
2	CCTPR	Counter Clear Source GTPR Register Buffer Transfer Disable 0: Enable GTPR register buffer transfer by counter clear 1: Disable GTPR register buffer transfer by counter clear	R/W
3	CCTADA	Counter Clear Source GTADTRA Register Buffer Transfer Disable 0: Enable GTADTRA register buffer transfer by counter clear 1: Disable GTADTRA register buffer transfer by counter clear	R/W
4	CCTADB	Counter Clear Source GTADTRB Register Buffer Transfer Disable 0: Enable GTADTRB register buffer transfer by counter clear 1: Disable GTADTRB register buffer transfer by counter clear	R/W
5	CCTDV	Counter Clear Source GTDVU/GTDVD Register Buffer Transfer Disable 0: Enable GTDVU/GTDVD register buffer transfer by counter clear 1: Disable GTDVU/GTDVD register buffer transfer by counter clear	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
9:8	CMTCA[1:0]	Compare Match Source GTCCRA Register Buffer Transfer Enable 0 0: Disable GTCCRA register Buffer Transfer by compare match of GTCCRA register and GTCCRB register 0 1: Enable GTCCRA register Buffer Transfer by compare match of GTCCRA register 1 0: Enable GTCCRA register Buffer Transfer by compare match of GTCCRB register 1 1: Enable GTCCRA register Buffer Transfer by compare match of GTCCRA register and GTCCRB register	R/W
11:10	CMTCB[1:0]	Compare Match Source GTCCRB Register Buffer Transfer Enable 0 0: Disable GTCCRB register Buffer Transfer by compare match of GTCCRA register and GTCCRB register 0 1: Enable GTCCRB register Buffer Transfer by compare match of GTCCRA register 1 0: Enable GTCCRB register Buffer Transfer by compare match of GTCCRB register 1 1: Enable GTCCRB register Buffer Transfer by compare match of GTCCRA register and GTCCRB register	R/W
12	—	This bit is read as 0. The write value should be 0.	R/W
13	CMTADA	Compare Match Source GTADTRA Register Buffer Transfer Enable 0: Disable GTADTRA register buffer transfer by compare match of GTADTRA register 1: Enable GTADTRA register buffer transfer by compare match of GTADTRA register	R/W
14	CMTADB	Compare Match Source GTADTRB Register Buffer Transfer Enable 0: Disable GTADTRB register buffer transfer by compare match of GTADTRB register 1: Enable GTADTRB register buffer transfer by compare match of GTADTRB register	R/W
15	—	This bit is read as 0. The write value should be 0.	R/W
16	CPTCA	Overflow/Underflow Source GTCCRA Register Buffer Transfer Disable 0: Enable GTCCRA register buffer transfer by overflow/underflow 1: Disable GTCCRA register buffer transfer by overflow/underflow	R/W
17	CPTCB	Overflow/Underflow Source GTCCRB Register Buffer Transfer Disable 0: Enable GTCCRB register buffer transfer by overflow/underflow 1: Disable GTCCRB register buffer transfer by overflow/underflow	R/W
18	CPTPR	Overflow/Underflow Source GTPR Register Buffer Transfer Disable 0: Enable GTPR register buffer transfer by overflow/underflow 1: Disable GTPR register buffer transfer by overflow/underflow	R/W
19	CPTADA	Overflow/Underflow Source GTADTRA Register Buffer Transfer Disable 0: Enable GTADTRA register buffer transfer by overflow/underflow 1: Disable GTADTRA register buffer transfer by overflow/underflow	R/W
20	CPTADB	Overflow/Underflow Source GTADTRB Register Buffer Transfer Disable 0: Enable GTADTRB register buffer transfer by overflow/underflow 1: Disable GTADTRB register buffer transfer by overflow/underflow	R/W
21	CPTDV	Overflow/Underflow Source GTDVU/GTDVD Register Buffer Transfer Disable 0: Enable GTDVU/GTDVD register buffer transfer by overflow/underflow 1: Disable GTDVU/GTDVD register buffer transfer by overflow/underflow	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
2	CCTPR	计数器清除源GTPR寄存器缓冲区传输禁用 0：通过计数器清除启用GTPR寄存器缓冲区传输1：通过计数器清除禁用GTPR寄存器缓冲区传输	R/W
3	CCTADA	计数器清零源GTADTRA寄存器缓冲区传输禁用 0：通过计数器清除启用GTADTRA寄存器缓冲区传输1：通过计数器清除禁用GTADTRA寄存器缓冲区传输	R/W
4	CCTADB	计数器清零源GTADTRB寄存器缓冲区传输禁用 0：通过计数器清除启用GTADTRB寄存器缓冲区传输1：通过计数器清除禁用GTADTRB寄存器缓冲区传输	R/W
5	CCTDV	CounterClearSourceGTDVUGTDVDRegisterBufferTransferDisable 0：通过计数器清除启用GTDVUGTDVD寄存器缓冲区传输1：通过计数器清除禁用GTDVUGTDVD寄存器缓冲区传输	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
9:8	CMTCA[1:0]	比较匹配源GTCCRA寄存器缓冲区传输使能 00:通过GTCCRA寄存器和GTCCRB寄存器的比较匹配禁用GTCCRA寄存器缓冲区传输 01：使能GTCCRA寄存器通过GTCCRA寄存器1的比较匹配进行缓冲区传输0：使能GTCCRA寄存器通过GTCCRB寄存器的比较匹配进行缓冲区传输11：使能GTCCRA寄存器通过GTCCRA寄存器和GTCCRB寄存器的比较匹配进行缓冲区传输	R/W
11:10	CMTCB[1:0]	比较匹配源GTCCRB寄存器缓冲区传输使能 00:通过GTCCRA寄存器和GTCCRB寄存器的比较匹配禁用GTCCRB寄存器缓冲区传输 01：使能GTCCRB寄存器通过GTCCRA寄存器的比较匹配进行缓冲区传输10：使能GTCCRB寄存器通过GTCCRB寄存器的比较匹配进行缓冲区传输11：使能GTCCRB寄存器通过GTCCRA寄存器和GTCCRB寄存器的比较匹配进行缓冲区传输	R/W
12	—	该位读取为0。写入值应为0。	R/W
13	CMTADA	比较匹配源GTADTRA寄存器缓冲区传输使能 0：通过GTADTRA寄存器的比较匹配禁用GTADTRA寄存器缓冲区传输 1：通过GTADTRA寄存器的比较匹配使能GTADTRA寄存器缓冲区传输	R/W
14	CMTADB	比较匹配源GTADTRB寄存器缓冲区传输使能 0：通过GTADTRB寄存器的比较匹配禁用GTADTRB寄存器缓冲区传输 1：通过GTADTRB寄存器的比较匹配使能GTADTRB寄存器缓冲传输	R/W
15	—	该位读取为0。写入值应为0。	R/W
16	CPTCA	上溢下溢源GTCCRA寄存器缓冲区传输禁用 0：上溢下溢启用GTCCRA寄存器缓冲区传输1：上溢下溢禁用GTCCRA寄存器缓冲区传输	R/W
17	CPTCB	上溢下溢源GTCCRB寄存器缓冲区传输禁用 0：通过上溢下溢启用GTCCRB寄存器缓冲区传输1：通过上溢下溢禁用GTCCRB寄存器缓冲区传输	R/W
18	CPTPR	上溢下溢源GTPR寄存器缓冲区传输禁用 0：通过上溢下溢启用GTPR寄存器缓冲区传输1：通过上溢下溢禁用GTPR寄存器缓冲区传输	R/W
19	CPTADA	上溢下溢源GTADTRA寄存器缓冲区传输禁用 0：通过上溢下溢启用GTADTRA寄存器缓冲区传输1：通过上溢下溢禁用GTADTRA寄存器缓冲区传输	R/W
20	CPTADB	上溢下溢源GTADTRB寄存器缓冲区传输禁用 0：通过上溢下溢启用GTADTRB寄存器缓冲区传输1：通过上溢下溢禁用GTADTRB寄存器缓冲区传输	R/W
21	CPTDV	溢出下溢源GTDVUGTDVD寄存器缓冲区传输禁用 0：通过上溢下溢启用GTDVUGTDVD寄存器缓冲区传输1：通过上溢下溢禁用GTDVUGTDVD寄存器缓冲区传输	R/W
23:22	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
24	CP3DB	Complementary PWM mode 3,4 Double Buffer select*1 0: Disable double buffer function in complementary PWM mode 3, 4 1: Enable double buffer function in complementary PWM mode 3, 4	R/W
25	CPBTD	Complementary PWM mode Buffer Transfer Disable*1 0: Enable buffer transfer from temporary register to GTCCRC and GTPBR register 1: Disable buffer transfer from temporary register to GTCCRC and GTPBR register	R/W
27:26	OLTTA[1:0]	GTIOCnA Output Level Buffer Transfer Timing Select*1 0 0: No transfer 0 1: Triangle waves, complementary PWM mode: Transfer at crest Saw waves: Transfer at the end of period 1 0: Triangle waves, complementary PWM mode: Transfer at trough Saw waves: Transfer by compare match of GTCCRA register 1 1: Triangle waves, complementary PWM mode: Transfer at both crest and trough Saw waves: Setting prohibited	R/W
29:28	OLTTB[1:0]	GTIOCnB Output Level Buffer Transfer Timing Select*1 0 0: No transfer 0 1: Triangle waves, complementary PWM mode: Transfer at crest Saw waves: Transfer at the end of period 1 0: Triangle waves, complementary PWM mode: Transfer at trough Saw waves: Transfer by compare match of GTCCRB register 1 1: Triangle waves, complementary PWM mode: Transfer at both crest and trough Saw waves: Setting prohibited	R/W
31:30	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is only available in GPT324 to GPT329.
In GPT320 to GPT323, this bit is read as 0. The write value should be 0.

The GTBER2 register makes settings for buffer operation.

Set the CP3DB bit and OLTTm[1:0] (m = A, B) bits when the GTCNT counter is stopped.

CCTCA bit (Counter Clear Source GTCCRA Register Buffer Transfer Disable)

This bit disables buffer transfer by counter clear using the GTCCRA, GTCCRC, and GTCCRD registers together.

This bit is effective when the GTBER.BD[0] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.CCRA[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode. Even if the CCTCA bit is 0, buffer transfer is not performed by counter clear.

If there is a conflict with the CMTCA bit setting, the CCTCA bit setting has priority.

The setting is invalid during the event count operation.

CCTCB bit (Counter Clear Source GTCCRB Register Buffer Transfer Disable)

This bit disables buffer transfer by counter clear using the GTCCRB, GTCCRE, and GTCCRF registers together.

This bit is effective when the GTBER.BD[0] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.CCRB[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode. Even if the CCTCB bit is 0, buffer transfer is not performed by counter clear.

If there is a conflict with the CMTCB bit setting, the CCTCB bit setting has priority.

The setting is invalid during the event count operation.

CCTPR bit (Counter Clear Source GTPR Register Buffer Transfer Disable)

This bit disables buffer transfer by counter clear using the GTPR, GTPBR, and GTPDBR registers together.

This bit is effective when the GTBER.BD[1] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.PR[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode. Even if the CCTPR bit is 0, buffer transfer is not performed by counter clear.

Bit	Symbol	Function	R/W
24	CP3DB	互补PWM模式3 4双缓冲器选择*1 0：在互补PWM模式3、4下禁用双缓冲功能1：在互补PWM模式3、4下启用双缓冲功能	R/W
25	CPBTD	互补PWM模式缓冲区传输禁用*1 0：启用从临时寄存器到GTCCRC和GTPBR寄存器的缓冲区传输1：禁用从临时寄存器到GTCCRC和GTPBR寄存器的缓冲区传输	R/W
27:26	OLTTA[1:0]	GTIOCnA输出电平缓冲器传输时序选择*1 00：无传输01：三角波，互补PWM模式：波峰传输锯齿波：周期结束传输 10：三角波，互补PWM模式：在波谷传输锯齿波：通过GTCCRA寄存器的比较匹配传输 11：三角波，互补PWM模式：波峰和波谷传输锯波：禁止设置	R/W
29:28	OLTTB[1:0]	GTIOCnB输出电平缓冲器传输时序选择*1 00：无传输01：三角波，互补PWM模式：波峰传输锯齿波：周期结束传输 10：三角波，互补PWM模式：在波谷传输锯齿波：通过GTCCRB寄存器的比较匹配传输 11：三角波，互补PWM模式：波峰和波谷传输锯波：禁止设置	R/W
31:30	—	这些位被读取为0。写入值应为0。	R/W

注1.该位仅在GPT324至GPT329中可用。
在GPT320到GPT323中，该位读取为0。写入值应为0。

GTBER2寄存器用于设置缓冲区操作。

当GTCNT计数器停止时，设置CP3DB位和OLTTm[1:0](m=A B)位。

CCTCA位（计数器清零源GTCCRA寄存器缓冲区传输禁止）

该位通过同时使用GTCCRA、GTCCRC和GTCCRD寄存器清除计数器来禁用缓冲区传输。

当GTBER.BD[0]位为0（使能缓冲操作）且缓冲操作由GTBER.CCRA[1:0]位带锯齿波。

该设置在三角波或互补PWM模式下无效。即使CCTCA位为0，也不会通过计数器清零来执行缓冲区传输。

如果与CMTCA位设置冲突，CCTCA位设置优先。

该设置在事件计数操作期间无效。

CCTCB位（计数器清零源GTCCRB寄存器缓冲区传输禁止）

该位通过一起使用GTCCRB、GTCCRE和GTCCRF寄存器清除计数器来禁用缓冲区传输。

当GTBER.BD[0]位为0（使能缓冲操作）且缓冲操作由GTBER.CCRB[1:0]位带锯齿波。

该设置在三角波或互补PWM模式下无效。即使CCTCB位为0，也不会通过计数器清零来执行缓冲区传输。

如果与CMTCB位设置冲突，CCTCB位设置优先。

该设置在事件计数操作期间无效。

CCTPR位（计数器清零源GTPR寄存器缓冲区传输禁止）

该位通过一起使用GTPR、GTPBR和GTPDBR寄存器清除计数器来禁用缓冲区传输。

当GTBER.BD[1]位为0（缓冲操作使能）且缓冲操作由GTBER.PR[1:0]位带锯齿波。

该设置在三角波或互补PWM模式下无效。即使CCTPR位为0，也不会通过计数器清零来执行缓冲区传输。

The setting is invalid during the event count operation.

CCTADm bit (Counter Clear Source GTADTRm Register Buffer Transfer Disable) (m = A, B)

This bit disables buffer transfer by counter clear using the GTADTRm, GTADTBRm and GTADTDBRm registers together.

This bit is effective when the GTBER.BD[2] bit is 0 (buffer operation enabled) and the buffer operation is selected by the ADTTm[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode. Even if the CCTADm bit is 0, buffer transfer is not performed by counter clear.

If there is a conflict with the CMTADm bit setting, the CCTADm bit setting has priority.

The setting is invalid during the event count operation.

CCTDV bit (Counter Clear Source GTDVU/GTDVD Register Buffer Transfer Disable)

This bit disables buffer transfer by counter clear using the GTDVU and GTDBU or GTDVD and GTDBD registers together.

This bit is effective when the GTBER.BD[3] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTDTCR.TDBUE or GTDTCR.TDBDE bit with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode. Even if the CCTDV bit is 0, buffer transfer is not performed by counter clear.

The setting is invalid during the event count operation.

CMTCA[1:0] bit (Compare Match Source GTCCRA Register Buffer Transfer Enable)

This bit enables buffer transfer by compare match of GTCCRA using the GTCCRA, GTCCRC, and GTCCRD registers together.

This bit is effective when the GTBER.BD[0] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.CCRA[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

If there is a conflict with the CCTCA bit setting, the CCTCA bit setting has priority.

The setting is invalid during the event count operation.

CMTCB[1:0] bit (Compare Match Source GTCCRB Register Buffer Transfer Enable)

This bit enables buffer transfer by compare match of GTCCRB using the GTCCRB, GTCCRE, and GTCCRF registers together.

This bit is effective when the GTBER.BD[0] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.CCRB[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

If there is a conflict with the CCTCB bit setting, the CCTCB bit setting has priority.

The setting is invalid during the event count operation.

CMTADm bit (Compare Match Source GTADTRm Register Buffer Transfer Enable) (m = A, B)

This bit enables buffer transfer by compare match of GTADTRm using the GTADTRm, GTADTBRm and GTADTDBRm registers together.

This bit is effective when the GTBER.BD[2] bit is 0 (buffer operation enabled) and the buffer operation is selected by the ADTTm[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

If there is a conflict with the CCTADm bit setting, the CCTADm bit setting has priority.

The setting is invalid during the event count operation.

CPTCA bit (Overflow/Underflow Source GTCCRA Register Buffer Transfer Disable)

This bit disables buffer transfer by overflow/underflow in saw-waves using the GTCCRA, GTCCRC, and GTCCRD registers together.

该设置在事件计数操作期间无效。

CCTADm位（计数器清零源GTADTRm寄存器缓冲区传输禁止）（m=A，B）

该位通过同时使用GTADTRm、GTADTDBRm和GTADTDBRm寄存器清除计数器来禁用缓冲区传输。

当GTBER.BD[2]位为0（使能缓冲操作）且缓冲操作由
ADTTm[1:0]位带锯齿波。

该设置在三角波或互补PWM模式下无效。即使CCTADm位为0，也不会通过计数器清零来执行缓冲区传输。

如果与CMTADm位设置冲突，CCTADm位设置具有优先权。

该设置在事件计数操作期间无效。

CCTDV位（计数器清零源GTDVUGTDVD寄存器缓冲区传输禁止）

该位通过使用GTDVU和GTDBU或GTDVD和GTDBD寄存器一起清除计数器来禁用缓冲区传输。

当GTBER.BD[3]位为0（使能缓冲操作）且缓冲操作由
GTDTCR.TDBUE或GTDTCR.TDBDE位带锯齿波。

该设置在三角波或互补PWM模式下无效。即使CCTDV位为0，也不会通过计数器清零来执行缓冲区传输。

该设置在事件计数操作期间无效。

CMTCA[1:0]位（比较匹配源GTCCRA寄存器缓冲区传输使能）

该位通过一起使用GTCCRA、GTCCRC和GTCCRD寄存器的GTCCRA比较匹配来启用缓冲区传输。

当GTBER.BD[0]位为0（使能缓冲操作）且缓冲操作由
GTBER.CCRA[1:0]位带锯齿波。

该设置在三角波或互补PWM模式下无效。

如果与CCTCA位设置冲突，CCTCA位设置优先。

该设置在事件计数操作期间无效。

CMTCB[1:0]位（比较匹配源GTCCRB寄存器缓冲区传输使能）

该位通过一起使用GTCCRB、GTCCRE和GTCCRF寄存器的GTCCRB比较匹配来启用缓冲区传输。

当GTBER.BD[0]位为0（使能缓冲操作）且缓冲操作由
GTBER.CCRB[1:0]位带锯齿波。

该设置在三角波或互补PWM模式下无效。

如果与CCTCB位设置冲突，CCTCB位设置优先。

该设置在事件计数操作期间无效。

CMTADm位（比较匹配源GTADTRm寄存器缓冲区传输使能）（m=A，B）

该位通过一起使用GTADTRm、GTADTBRm和GTADTDBRm寄存器的GTADTRm比较匹配来启用缓冲区传输。

当GTBER.BD[2]位为0（使能缓冲操作）且缓冲操作由
ADTTm[1:0]位带锯齿波。

该设置在三角波或互补PWM模式下无效。

如果与CCTADm位设置冲突，CCTADm位设置具有优先权。

该设置在事件计数操作期间无效。

CPTCA位（上溢下溢源GTCCRA寄存器缓冲区传输禁止）

该位通过同时使用GTCCRA、GTCCRC和GTCCRD寄存器的锯齿波中的上溢下溢来禁用缓冲区传输。

This bit is effective when the CCTCA bit is 0 (GTCCRA register buffer transfer by counter clear is enabled), the GTBER.BD[0] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.CCRA[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

The setting is invalid during the event count operation.

CPTCB bit (Overflow/Underflow Source GTCCRB Register Buffer Transfer Disable)

This bit disables buffer transfer by overflow/underflow in saw-waves using the GTCCRB, GTCCRE and GTCCRF registers together.

This bit is effective when the CCTCB bit is 0 (GTCCRB register buffer transfer by counter clear is enabled), the GTBER.BD[0] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.CCRB[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

The setting is invalid during the event count operation.

CPTPR bit (Overflow/Underflow Source GTPR Register Buffer Transfer Disable)

This bit disables buffer transfer by overflow/underflow in saw-waves using the GTPR, GTPBR, and GTPDBR registers together.

This bit is effective when the CCTPR bit is 0 (GTPR register buffer transfer by counter clear is enabled), the GTBER.BD[1] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.PR[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

The setting is invalid during the event count operation.

CPTADm bit (Overflow/Underflow Source GTADTRm Register Buffer Transfer Disable) (m = A, B)

This bit disables buffer transfer by overflow/underflow in saw-waves using the GTADTRm, GTADTBRm and GTADTDBRm registers together.

This bit is effective when the CCTADm bit is 0 (GTADTRm register buffer transfer by counter clear is enabled), the GTBER.BD[2] bit is 0 (buffer operation enabled) and the buffer operation is selected by the ADTTm[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

The setting is invalid during the event count operation.

CPTDV bit (Overflow/Underflow Source GTDVU/GTDVD Register Buffer Transfer Disable)

This bit disables buffer transfer by overflow/underflow in saw-waves using the GTDVU and GTDBU or GTDVD and GTDBD registers together.

This bit is effective when the CCTDV bit is 0 (GTDVU/GTDVD register buffer transfer by counter clear is enabled), the GTBER.BD[3] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTDTCR.TDBUE or GTDTCR.TDBDE bit with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

The setting is invalid during the event count operation.

CP3DB bit (Complementary PWM mode 3,4 Double Buffer select)

This bit enables buffer transfer using the GTCCRA, GTCCRE and GTCCRF registers together in complementary PWM mode 3,4.

CPBTD bit (Complementary PWM mode Buffer Transfer Disable)

This bit disables buffer transfer from temporary register(temporary register A and temporary register P) to the GTCCRC and GTPBR registers during timer counting in complementary PWM mode 1, 2 and 3. When CP3DB bit is 1, the buffer transfer from temporary register B to GTCCRE register is also disabled. The setting is invalid in complementary PWM mode 4.

OLTTm[1:0] bits (GTIOCnA Output Level Buffer Transfer Timing Select) (m = A, B)

This bit set the timing of buffer transfer from GTOLBR.GTIOmB[4:0] bits to GTIOR.GTIOm[4:0] bits.

当CCTCA位为0（通过计数器清除GTCCRA寄存器缓冲区传输使能）时，该位有效，
GTBER.BD[0]位为0（使能缓冲器操作），缓冲器操作由GTBER.CCRA[1:0]位用锯齿波选择。

该设置在三角波或互补PWM模式下无效。

该设置在事件计数操作期间无效。

CPTCB位（上溢下溢源GTCCRB寄存器缓冲区传输禁止）

该位通过同时使用GTCCRB、GTCCRE和GTCCRF寄存器在锯齿波中通过上溢下溢来禁用缓冲区传输。

当CCTCB位为0（通过计数器清除GTCCRB寄存器缓冲区传输使能）时，该位有效，
GTBER.BD[0]位为0（启用缓冲区操作），缓冲区操作由带有锯齿波的GTBER.CCRB[1:0]位选择。

该设置在三角波或互补PWM模式下无效。

该设置在事件计数操作期间无效。

CPTPR位（上溢下溢源GTPR寄存器缓冲区传输禁用）

该位通过同时使用GTPR、GTPBR和GTPDBR寄存器的锯齿波中的上溢下溢来禁用缓冲区传输。

当CCTPR位为0（通过计数器清零使能GTPR寄存器缓冲区传输）、GTBER.BD[1]位为0（使能缓冲区操作）且缓冲区操作由GTBER.PR[1选择时，该位有效:0]位带锯齿波。

该设置在三角波或互补PWM模式下无效。

该设置在事件计数操作期间无效。

CPTADm位（上溢下溢源GTADTRm寄存器缓冲区传输禁止）（m=A，B）

该位使用GTADTRm、GTADTBRm和
GTADTDBRm一起注册。

当CCTADm位为0（通过计数器清除GTADTRm寄存器缓冲区传输使能）时，该位有效，
GTBER.BD[2]位为0（使能缓冲器操作），缓冲器操作由ADTTm[1:0]位用锯齿波选择。

该设置在三角波或互补PWM模式下无效。

该设置在事件计数操作期间无效。

CPTDV位（溢出下溢源GTDVUGTDVD寄存器缓冲区传输禁止）

该位通过使用GTDVU和GTDBU或GTDVD的锯齿波中的溢出下溢来禁用缓冲区传输，并且
GTDBD一起注册。

该位在CCTDV位为0时有效（通过计数器清除GTDVUGTDVD寄存器缓冲区传输使能），
GTBER.BD[3]位为0（启用缓冲操作），缓冲操作由GTDTCR.TDBUE或
GTDTCR.TDBDE位带锯齿波。

该设置在三角波或互补PWM模式下无效。

该设置在事件计数操作期间无效。

CP3DB位（互补PWM模式3 4双缓冲器选择）

该位使能在互补PWM模式3 4下一起使用GTCCRA、GTCCRE和GTCCRF寄存器进行缓冲区传输。

CPBTD位（互补PWM模式缓冲区传输禁用）

该位禁止在互补PWM模式1、2和3的定时器计数期间从临时寄存器（临时寄存器A和临时寄存器P）到GTCCRC和GTPBR寄存器的缓冲区传输。当CP3DB位为1时，缓冲区从临时寄存器B传输到GTCCRE寄存器也被禁用。该设置在互补PWM模式4下无效。

OLTTm[1:0]位（GTIOCnA输出电平缓冲器传输时序选择）（m=A，B）

该位设置从GTOLBR.GTIOmB[4:0]位到GTIOR.GTIOm[4:0]位的缓冲区传输时序。

21.2.44 GTOLBR : General PWM Timer Output Level Buffer Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 4 to 9)

Offset address: 0xE4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	GTIOBB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	GTIOAB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	GTIOAB[4:0]	GTIOA buffer bits	R/W
15:5	—	These bits are read as 0. The write value should be 0.	R/W
20:16	GTIOBB[4:0]	GTIOB buffer bits	R/W
31:21	—	These bits are read as 0. The write value should be 0.	R/W

The GTOLBR register is a buffer register for the GTIOR.GTIOA[4:0] bits and GTIOR.GTIOB[4:0] bits.

GTIOmB[4:0] bits (GTIOm buffer bits) (m = A, B)

These bits are buffer bits of GTIOR.GTIOm[4:0] bits.

These bits are transferred to the GTIOR.GTIOm[4:0] bits at the transfer timing selected by the GTBER2.OLTTm[1:0] (m = A, B) bits.

21.2.45 GTICCR : General PWM Timer Inter Channel Cooperation Input Capture Control Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xEC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ICBGRP[1:0]		—	—	—	—	—	ICBCLK	ICBFPU	ICBFPO	ICBFF	ICBFE	ICBFD	ICBFC	ICBFB	ICBFA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ICAGRP[1:0]		—	—	—	—	—	ICACLK	ICAFPU	ICAFPO	ICAFF	ICAFE	ICAFD	ICAFC	ICAFB	ICAFA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ICAFA	Forwarding GTCCRA register Compare Match/Input Capture to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding GTCCRA register compare match/input capture to GTCCRA input capture source of other channels 1: Enable forwarding GTCCRA register compare match/input capture to GTCCRA input capture source of other channels	R/W

21.2.44 GTOLBR:通用PWM定时器输出电平缓冲寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 4 to 9)

Offset address: 0xE4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	GTIOBB[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	GTIOAB[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	GTIOAB[4:0]	GTIOA缓冲区位	R/W
15:5	—	这些位被读取为0。写入值应为0。	R/W
20:16	GTIOBB[4:0]	GTIOB缓冲区位	R/W
31:21	—	这些位被读取为0。写入值应为0。	R/W

GTOLBR寄存器是GTIOR.GTIOA[4:0]位和GTIOR.GTIOB[4:0]位的缓冲寄存器。

GTIOmB[4:0]位（GTIOm缓冲区位）（m=A，B）

这些位是GTIOR.GTIOm[4:0]位的缓冲区位。

这些位在GTBER2.OLTTm[1:0](m=A, B)位选择的传输时序下传输到GTIOR.GTIOm[4:0]位。

21.2.45 GTICCR:通用PWM定时器通道间协作输入捕捉控制 Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)

Offset address: 0xEC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ICBGRP[1:0]		—	—	—	—	—	ICBCLK	ICBFPU	ICBFPO	ICBFF	ICBFE	ICBFD	ICBFC	ICBFB	ICBFA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ICAGRP[1:0]		—	—	—	—	—	ICACLK	ICAFPU	ICAFPO	ICAFF	ICAFE	ICAFD	ICAFC	ICAFB	ICAFA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ICAFA	将GTCCRA寄存器比较匹配输入捕获转发到其他通道GTCCRA 输入捕捉源使能 0：禁止将GTCCRA寄存器比较匹配输入捕捉转发到其他通道的GTCCRA输入捕捉源 1：使能将GTCCRA寄存器比较匹配输入捕捉转发到其他通道的GTCCRA输入捕捉源	R/W

Bit	Symbol	Function	R/W
1	ICAFB	Forwarding GTCCRB register Compare Match/Input Capture to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding GTCCRB register compare match/input capture to GTCCRA input capture source of other channels 1: Enable forwarding GTCCRB register compare match/input capture to GTCCRA input capture source of other channels	R/W
2	ICAFC	Forwarding GTCCRC register Compare Match to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding GTCCRC register compare match to GTCCRA input capture source of other channels 1: Enable forwarding GTCCRC register compare match to GTCCRA input capture source of other channels	R/W
3	ICAFD	Forwarding GTCCRD register Compare Match to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding GTCCRD register compare match to GTCCRA input capture source of other channels 1: Enable forwarding GTCCRD register compare match to GTCCRA input capture source of other channels	R/W
4	ICAFE	Forwarding GTCCRE register Compare Match to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding GTCCRE register compare match to GTCCRA input capture source of other channels 1: Enable forwarding GTCCRE register compare match to GTCCRA input capture source of other channels	R/W
5	ICAFF	Forwarding GTCCRF register Compare Match to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding GTCCRF register compare match to GTCCRA input capture source of other channels 1: Enable forwarding GTCCRF register compare match to GTCCRA input capture source of other channels	R/W
6	ICAFPO	Forwarding Overflow to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding overflow in saw-waves or the crest in triangle-waves or complementary PWM mode to GTCCRA input capture source of other channels 1: Enable forwarding overflow in saw-waves or the crest in triangle-waves or complementary PWM mode to GTCCRA input capture source of other channels	R/W
7	ICAFPU	Forwarding Underflow to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding underflow in saw-waves or the trough in triangle-waves or complementary PWM mode to GTCCRA input capture source of other channels 1: Enable forwarding underflow in saw-waves or the trough in triangle-waves or complementary PWM mode to GTCCRA input capture source of other channels	R/W
8	ICACLK	Forwarding Count Clock to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding count clock to GTCCRA input capture source of other channels 1: Enable forwarding count clock to GTCCRA input capture source of other channels	R/W
13:9	—	These bits are read as 0. The write value should be 0.	R/W
15:14	ICAGRP[1:0]	GTCCRA Input Capture Group Select 0 0: Select group A 0 1: Select group B 1 0: Select group C 1 1: Select group D	R/W
16	ICBFA	Forwarding GTCCRA register Compare Match/Input Capture to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding GTCCRA register compare match/input capture to GTCCRB input capture source of other channels 1: Enable forwarding GTCCRA register compare match/input capture to GTCCRB input capture source of other channels	R/W

Bit	Symbol	Function	R/W
1	ICAFB	将GTCCRB寄存器比较匹配输入捕获转发到其他通道GTCCRA输入捕捉源使能 0：禁止将GTCCRB寄存器比较匹配输入捕捉转发到其他通道的GTCCRA输入捕捉源 1：使能将GTCCRB寄存器比较匹配输入捕捉转发到其他通道的GTCCRA输入捕捉源	R/W
2	ICAFC	转发GTCCRC寄存器比较匹配到其他通道GTCCRA输入捕捉源启用 0：禁止将GTCCRC寄存器比较匹配转发到其他通道的GTCCRA输入捕捉源 1：使能转发GTCCRC寄存器比较匹配到其他通道的GTCCRA输入捕捉源	R/W
3	ICAFD	转发GTCCRD寄存器比较匹配到其他通道GTCCRA输入捕捉源启用 0：禁止将GTCCRD寄存器比较匹配转发到其他通道的GTCCRA输入捕捉源 1：使能转发GTCCRD寄存器比较匹配到其他通道的GTCCRA输入捕捉源	R/W
4	ICAFE	转发GTCCRE寄存器比较匹配到其他通道GTCCRA输入捕捉源启用 0：禁止将GTCCRE寄存器比较匹配转发到其他通道的GTCCRA输入捕捉源 1：使能转发GTCCRE寄存器比较匹配到其他通道的GTCCRA输入捕捉源	R/W
5	ICAFF	转发GTCCRF寄存器比较匹配到其他通道GTCCRA输入捕捉源启用 0：禁止将GTCCRF寄存器比较匹配转发到其他通道的GTCCRA输入捕捉源 1：使能转发GTCCRF寄存器比较匹配到其他通道的GTCCRA输入捕捉源	R/W
6	ICAFPO	将溢出转发到其他通道GTCCRA输入捕捉源使能 0：禁用锯齿波或三角波波峰的转发溢出或对其他通道GTCCRA输入捕捉源的互补PWM模式 1：启用锯齿波中的转发溢出或三角波中的波峰或对其他通道GTCCRA输入捕捉源的互补PWM模式	R/W
7	ICAFPU	将下溢转发到其他通道GTCCRA输入捕捉源使能 0：禁止将锯齿波或三角波波谷或互补PWM模式的下溢转发到其他通道的GTCCRA输入捕捉源 1：启用锯齿波中的转发下溢或三角波中的波谷或对其他通道GTCCRA输入捕捉源的互补PWM模式	R/W
8	ICACLK	将计数时钟转发到其他通道GTCCRA输入捕捉源使能 0：禁止向其他通道的GTCCRA输入捕获源转发计数时钟1：使能向其他通道的GTCCRA输入捕获源转发计数时钟	R/W
13:9	—	这些位被读取为0。写入值应为0。	R/W
15:14	ICAGRP[1:0]	GTCCRA输入捕获组选择 00：选择A组01：选择B组10：选择C组1 1：选择D组	R/W
16	ICBFA	将GTCCRA寄存器比较匹配输入捕获转发到其他通道GTCCRB输入捕捉源使能 0：禁止将GTCCRA寄存器比较匹配输入捕捉转发到其他通道的GTCCRB输入捕捉源 1：使能将GTCCRA寄存器比较匹配输入捕捉转发到其他通道的GTCCRB输入捕捉源	R/W

Bit	Symbol	Function	R/W
17	ICBFB	Forwarding GTCCRB register Compare Match/Input Capture to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding GTCCRB register compare match/input capture to GTCCRB input capture source of other channels 1: Enable forwarding GTCCRB register compare match/input capture to GTCCRB input capture source of other channels	R/W
18	ICBFC	Forwarding GTCCRC register Compare Match to Other Channel GTCCRB Input Source Capture Enable 0: Disable forwarding GTCCRD register compare match to GTCCRB input capture source of other channels 1: Enable forwarding GTCCRD register compare match to GTCCRB input capture source of other channels	R/W
19	ICBFD	Forwarding GTCCRD register Compare Match to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding GTCCRD register compare match to GTCCRB input capture source of other channels 1: Enable forwarding GTCCRD register compare match to GTCCRB input capture source of other channels	R/W
20	ICBFE	Forwarding GTCCRE register Compare Match to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding GTCCRE register compare match to GTCCRB input capture source of other channels 1: Enable forwarding GTCCRE register compare match to GTCCRB input capture source of other channels	R/W
21	ICBFF	Forwarding GTCCRF register Compare Match to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding GTCCRF register compare match to GTCCRB input capture source of other channels 1: Enable forwarding GTCCRF register compare match to GTCCRB input capture source of other channels	R/W
22	ICBFPO	Forwarding Overflow to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding overflow in saw-waves or the crest in triangle-waves or complementary PWM mode to GTCCRB input capture source of other channels 1: Enable forwarding overflow in saw-waves or the crest in triangle-waves or complementary PWM mode to GTCCRB input capture source of other channels	R/W
23	ICBFPU	Forwarding Underflow to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding underflow in saw-waves or the trough in triangle-waves or complementary PWM mode to GTCCRB input capture source of other channels 1: Enable forwarding underflow in saw-waves or the trough in triangle-waves or complementary PWM mode to GTCCRB input capture source of other channels	R/W
24	ICBCLK	Forwarding Count Clock to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding count clock to GTCCRB input capture source of other channels 1: Enable forwarding count clock to GTCCRB input capture source of other channels	R/W
29:25	—	These bits are read as 0. The write value should be 0.	R/W
31:30	ICBGRP[1:0]	GTCCRB Input Capture Group Select 0 0: Select group A 0 1: Select group B 1 0: Select group C 1 1: Select group D	R/W

The GTICCR register is a register that controls input capture by inter channel cooperation.

For channels that perform input capture by inter channel cooperation, the forwarding enable bit of the input capture source corresponding to the GTCCRA register or GTCCRB register where the input capture occurs is invalid.

ICAFm bit (Forwarding GTCCRm register Compare Match/Input Capture to Other Channel GTCCRA Input Capture Source Enable) (m = A, B)

Enables/disables the use of compare match/input capture of GTCCRm register as the input capture source of other channel's GTCCRA register.

Bit	Symbol	Function	R/W
17	ICBFB	将GTCCRB寄存器比较匹配输入捕获转发到其他通道GTCCRB输入捕捉源使能 0：禁止将GTCCRB寄存器比较匹配输入捕捉转发到其他通道的GTCCRB输入捕捉源 1：使能将GTCCRB寄存器比较匹配输入捕捉转发到其他通道的GTCCRB输入捕捉源	R/W
18	ICBFC	转发GTCCRC寄存器比较匹配到其他通道GTCCRB输入源捕获启用 0：禁止将GTCCRD寄存器比较匹配转发到其他通道的GTCCRB输入捕捉源 1：使能转发GTCCRD寄存器比较匹配到其他通道的GTCCRB输入捕捉源	R/W
19	ICBFD	转发GTCCRD寄存器比较匹配到其他通道GTCCRB输入捕捉源启用 0：禁止将GTCCRD寄存器比较匹配转发到其他通道的GTCCRB输入捕捉源 1：使能转发GTCCRD寄存器比较匹配到其他通道的GTCCRB输入捕捉源	R/W
20	ICBFE	转发GTCCRE寄存器比较匹配到其他通道GTCCRB输入捕捉源启用 0：禁止将GTCCRE寄存器比较匹配转发到其他通道的GTCCRB输入捕捉源 1：使能转发GTCCRE寄存器比较匹配到其他通道的GTCCRB输入捕捉源	R/W
21	ICBFF	转发GTCCRF寄存器比较匹配到其他通道GTCCRB输入捕捉源启用 0：禁止将GTCCRF寄存器比较匹配转发到其他通道的GTCCRB输入捕捉源 1：使能转发GTCCRF寄存器比较匹配到其他通道的GTCCRB输入捕捉源	R/W
22	ICBFPO	将溢出转发到其他通道GTCCRB输入捕捉源使能 0：禁用锯齿波或三角波波峰的转发溢出或对其他通道GTCCRB输入捕捉源的互补PWM模式 1：启用锯齿波中的转发溢出或三角波中的波峰或对其他通道GTCCRB输入捕捉源的互补PWM模式	R/W
23	ICBFPU	将下溢转发到其他通道GTCCRB输入捕捉源使能 0：禁止将锯齿波或三角波波谷或互补PWM模式下的转发下溢到其他通道的GTCCRB输入捕捉源 1：启用锯齿波中的转发下溢或三角波中的波谷或对其他通道GTCCRB输入捕捉源的互补PWM模式	R/W
24	ICBCLK	将计数时钟转发到其他通道GTCCRB输入捕捉源使能 0：禁止向其他通道的GTCCRB输入捕获源转发计数时钟1：使能向其他通道的GTCCRB输入捕获源转发计数时钟	R/W
29:25	—	这些位被读取为0。写入值应为0。	R/W
31:30	ICBGRP[1:0]	GTCCRB输入捕获组选择 00：选择A组01：选择B组10：选择C组1 1：选择D组	R/W

GTICCR寄存器是通过通道间协作控制输入捕获的寄存器。

对于通道间协同进行输入捕捉的通道，发生输入捕捉的GTCCRA寄存器或GTCCRB寄存器对应的输入捕捉源的转发使能位无效。

ICAFm位（将GTCCRm寄存器比较匹配输入捕捉转发到其他通道GTCCRA输入捕获源启用）（m=A，B）

使能禁止使用GTCCRm寄存器的比较匹配输入捕捉作为其他通道的输入捕捉源
GTCCRA register.

ICAFx bit (Forwarding GTCCRx register Compare Match to Other Channel GTCCRA Input Capture Source Enable) (x = C, D, E, F)

Enables/disables the use of compare match of GTCCRx register as the input capture source of other channel's GTCCRA register.

ICAFPO bit (Forwarding Overflow to Other Channel GTCCRA Input Capture Source Enable)

Enable/disable to use the overflow of saw-waves, the crest of triangle-waves or complementary PWM mode as the input capture source of other channel's GTCCRA register.

ICAFPU bit (Forwarding Underflow to Other Channel GTCCRA Input Capture Source Enable)

Enable/disable to use the underflow of saw-waves, the trough of triangle-waves or complementary PWM mode as the input capture source of other channel's GTCCRA register.

ICACLK bit (Forwarding Count Clock to Other Channel GTCCRA Input Capture Source Enable)

Enable/disable to use count clock as the input capture source of other channel's GTCCRA register.

ICAGRP[1:0] bit (GTCCRA Input Capture Group Select)

Select the group of input capture by inter channel cooperation for GTCCRA register.

For channels that accept input capture of the GTCCRA register due to input capture sources from other channels, set the GTICASR.ASOC bit to 1 and select the group of inter channel cooperation with the ICAGRP[1:0] bits.

ICBFm bit (Forwarding GTCCRm register Compare Match/Input Capture to Other Channel GTCCRB Input Capture Source Enable) (m = A, B)

Enables/disables the use of compare match/input capture of GTCCRm register as the input capture source of other channel's GTCCRB register.

ICBFx bit (Forwarding GTCCRx register Compare Match to Other Channel GTCCRB Input Capture Source Enable) (x = C, D, E, F)

Enables/disables the use of compare match of GTCCRx register as the input capture source of other channel's GTCCRB register.

ICBFPO bit (Forwarding Overflow to Other Channel GTCCRB Input Capture Source Enable)

Enable/disable to use the overflow of saw-waves, the crest of triangle-waves or complementary PWM mode as the input capture source of other channel's GTCCRB register.

ICBFPU bit (Forwarding Underflow to Other Channel GTCCRB Input Capture Source Enable)

Enable/disable to use the underflow of saw-waves, the trough of triangle-waves or complementary PWM mode as the input capture source of other channel's GTCCRB register.

ICBCLK bit (Forwarding Count Clock to Other Channel GTCCRB Input Capture Source Enable)

Enable/disable to use count clock as the input capture source of other channel's GTCCRB register.

ICBGRP[1:0] bit (GTCCRB Input Capture Group Select)

Select the group of input capture by inter channel cooperation for GTCCRB register.

For channels that accept input capture of the GTCCRB register due to input capture sources from other channels, set the GTICBSR.BSOC bit to 1 and select the group of inter channel cooperation with the ICBGRP[1:0] bits.

ICAFx位（将GTCCRx寄存器比较匹配转发到其他通道GTCCRA输入捕捉Source Enable) (x = C, D, E, F)

使能禁止使用GTCCRx寄存器的比较匹配作为其他通道GTCCRA寄存器的输入捕捉源。

ICAFPO位（将溢出转发到其他通道GTCCRA输入捕捉源使能）

使能禁止使用锯齿波溢出、三角波波峰或互补PWM模式作为其他通道GTCCRA寄存器的输入捕捉源。

ICAFPU位（将下溢转发到其他通道GTCCRA输入捕捉源使能）

使能禁止使用锯齿波下溢、三角波波谷或互补PWM模式作为其他通道GTCCRA寄存器的输入捕捉源。

ICACLK位（将计数时钟转发到其他通道GTCCRA输入捕捉源使能）

使能禁用以使用计数时钟作为其他通道GTCCRA寄存器的输入捕捉源。

ICAGRP[1:0]位（GTCCRA输入捕捉组选择）

为GTCCRA寄存器选择通道间协作的输入捕捉组。

对于由于来自其他通道的输入捕捉源而接受GTCCRA寄存器的输入捕捉的通道，设置GTICASR.ASOC位为1并使用ICAGRP[1:0]位选择通道间协作组。

ICBFm位（将GTCCRm寄存器比较匹配输入捕捉转发到其他通道GTCCRB输入捕获源启用）（m=A，B）

使能禁止使用GTCCRm寄存器的比较匹配输入捕捉作为其他通道的输入捕捉源GTCCRB register.

ICBFx位（转发GTCCRx寄存器比较匹配到其他通道GTCCRB输入捕捉Source Enable) (x = C, D, E, F)

使能禁止使用GTCCRx寄存器的比较匹配作为其他通道的GTCCRB寄存器的输入捕捉源。

ICBFPO位（将溢出转发到其他通道GTCCRB输入捕捉源使能）

使能禁止使用锯齿波溢出、三角波波峰或互补PWM模式作为其他通道GTCCRB寄存器的输入捕捉源。

ICBFPU位（将下溢转发到其他通道GTCCRB输入捕捉源使能）

使能禁止使用锯齿波下溢、三角波波谷或互补PWM模式作为其他通道GTCCRB寄存器的输入捕捉源。

ICBCLK位（将计数时钟转发到其他通道GTCCRB输入捕捉源使能）

使能禁用以使用计数时钟作为其他通道GTCCRB寄存器的输入捕捉源。

ICBGRP[1:0]位（GTCCRB输入捕捉组选择）

为GTCCRB寄存器选择通道间协作的输入捕捉组。

对于由于来自其他通道的输入捕捉源而接受GTCCRB寄存器的输入捕捉的通道，设置GTICBSR.BSOC位为1并通过ICBGRP[1:0]位选择通道间协作组。

21.2.46 OPSCR : Output Phase Switching Control Register

Base address: GPT_OPS = 0x4016_9A00

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	RV	INV	N	P	FB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	UF	Input Phase Soft Setting These bits set the input phase from software settings. Setting these bits is valid when OPSCR.FB = 1.	R/W
1	VF		R/W
2	WF		R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	U	Input U-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by GTCLK OPSCR.FB = 1 : Software settings (UF)	R
5	V	Input V-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by GTCLK OPSCR.FB = 1 : Software settings (VF)	R
6	W	Input W-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by GTCLK OPSCR.FB = 1 : Software settings (WF)	R
7	—	This bit is read as 0. The write value should be 0.	R/W
8	EN	Output Phase Enable 0: Do not output (Hi-Z external pin) 1: Output*1	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	FB	External Feedback Signal Enable This bit selects the input phase from software settings and external input. 0: Select the external input 1: Select the soft setting (OPSCR.UF, VF, WF)	R/W
17	P	Positive-Phase Output (P) Control 0: Level signal output 1: PWM signal output	R/W
18	N	Negative-Phase Output (N) Control 0: Level signal output 1: PWM signal output	R/W
19	INV	Output Phase Invert Control 0: Positive logic (active-high) output 1: Negative logic (active-low) output	R/W
20	RV	Output Phase Rotation Direction Reversal Control 0: Positive rotation 1: Reverse rotation	R/W
21	ALIGN	Input Phase Alignment 0: Input phase aligned to GTCLK 1: Input phase aligned to the falling edge of PWM	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W

21.2.46 OPSCR：输出相位切换控制寄存器

Base address: GPT_OPS = 0x4016_9A00

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	RV	INV	N	P	FB
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	UF	输入相位软设置 这些位通过软件设置设置输入相位。 当OPSCR.FB=1时，设置这些位有效。	R/W
1	VF		R/W
2	WF		R/W
3	—	该位读取为0。写入值应为0。	R/W
4	U	输入U相监视器 该位监控输入相位的状态。 OPSCR.FB=0：由GTCLK同步的外部输入 OPSCR.FB=1：软件设置（UF）	R
5	V	输入V相监视器 该位监控输入相位的状态。 OPSCR.FB=0：由GTCLK同步的外部输入 OPSCR.FB=1：软件设置（VF）	R
6	W	输入W相监视器 该位监控输入相位的状态。 OPSCR.FB=0：由GTCLK同步的外部输入 OPSCR.FB=1：软件设置（WF）	R
7	—	该位读取为0。写入值应为0。	R/W
8	EN	输出相位使能 0：不输出（Hi-Z外部引脚）1：输出*1	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
16	FB	外部反馈信号使能 该位从软件设置和外部输入中选择输入相位。 0：选择外部输入1：选择软设置（OPSCR.UF、VF、WF）	R/W
17	P	正相输出(P)控制 0：电平信号输出1：PWM信号输出	R/W
18	N	负相输出(N)控制 0：电平信号输出1：PWM信号输出	R/W
19	INV	输出相位反转控制 0：正逻辑（高电平有效）输出1：负逻辑（低电平有效）输出	R/W
20	RV	输出相位旋转方向反转控制 0：正转1：反转	R/W
21	ALIGN	输入相位对齐 0：输入相位与GTCLK对齐1：输入相位与PWM下降沿对齐	R/W
23:22	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
25:24	GRP[1:0]	Output Disabled Source Selection 0 0: Select group A output disable source 0 1: Select group B output disable source 1 0: Select group C output disable source 1 1: Select group D output disable source	R/W
26	GODF	Group Output Disable Function 0: This bit function is ignored 1: Group disable clears the OPSCR.EN bit*1	R/W
28:27	—	These bits are read as 0. The write value should be 0.	R/W
29	NFEN	External Input Noise Filter Enable 0: Do not use a noise filter on the external input 1: Use a noise filter on the external input	R/W
31:30	NFCS[1:0]	External Input Noise Filter Clock Selection Noise filter sampling clock setting of the external input. 0 0: GTCLK/1 0 1: GTCLK/4 1 0: GTCLK/16 1 1: GTCLK/64	R/W

Note 1. When OPSCR.GODF = 1 and the signal value selected by the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0.

The OPSCR register sets the output of the signal waveform required for brushless DC motor control.

UF , VF , WF bits (Input Phase Soft Setting)

The UF , VF , WF bits set the input phase from the software settings. When OPSCR.FB bit is 1, these bits are valid. The set value of the UF /VF /WF takes the place of the U/V/W external input.

U, V, W bits (Input Phase Monitor)

When the OPSCR.FB bit is 0, external inputs that are synchronized by GTCLK are monitored by these bits. When the OPSCR.FB bit is 1, the OPSCR.U, OPSCR.V, and OPSCR.W bits can read the OPSCR.UF , OPSCR.VF , and OPSCR.WF bits.

EN bit (Output Phase Enable)

The EN bit controls the output enable signal of output phase (positive phase/negative phase).

When the OPSCR.EN bit is 1, the signal waveform is output.

When the OPSCR.EN bit is 0, first set OPSCR.FB, OPSCR.UF /VF /WF (software setting is selected), OPSCR.P/N, OPSCR.INV, OPSCR.RV, OPSCR.ALIGN, OPSCR.GRP[1:0], OPSCR.GODF, OPSCR.NFEN, OPSCR.NFCS. Then, set the bit to 1. The EN bit should be set when output disable request doesn't occur from POEG. Also when OPSCR.GODF is 1 and the signal value selected in the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0. And 1 by software to be written, the EN bit remains at 0.

For the return, after clearing the Output Disable Request by software, please set the EN = 1.

EN bit priority order (conflict).

When 1 write by software and cleared to 0 by the Output Disable Request has been conflicting for EN bit, cleared to 0 by the Output Disable Request is activated.

FB bit (External Feedback Signal Enable)

The FB bit selects the input phase from the software settings (OPSCR.UF, VF, WF) and external input such as a Hall element.

P bit (Positive-Phase Output (P) Control)

The P bit selects one of the level signal output or PWM signal output for the positive-phase output (GTOUUP, GTOVUP and GTOWUP pins).

Bit	Symbol	Function	R/W
25:24	GRP[1:0]	输出禁用源选择 0 0: 选择A组输出禁用源选择B组输出禁用 0 1: 源选择C 组输出禁用源选择D组输出禁 1 0: 用源 1 1:	R/W
26	GODF	组输出禁用功能 0：忽略该位功能1：组禁止清除OPSCR.EN位* 1	R/W
28:27	—	这些位被读取为0。写入值应为0。	R/W
29	NFEN	外部输入噪声滤波器启用 0：外部输入不使用噪声滤波器1：外部输入使用 噪声滤波器	R/W
31:30	NFCS[1:0]	外部输入噪声滤波器时钟选择 外部输入的噪声滤波器采样时钟设置。 0 0: GTCLK/1 0 1: GTCLK/4 1 0: GTCLK/16 1 1: GTCLK/64	R/W

注1.当OPSCR.GODF=1且OPSCR.GRP[1:0]位选择的信号值为高时，OPSCR.EN位设置为0。

OPSCR寄存器设置无刷直流电机控制所需的信号波形输出。

UF VF WF位（输入相位软设置）

UF、VF、WF位从软件设置中设置输入相位。当OPSCR.FB位为1时，这些位有效。UFVFWF的设定值代替了UVW外部输入。

U、V、W位（输入相位监视器）

当OPSCR.FB位为0时，由GTCLK同步的外部输入由这些位监控。当。。。的时候
OPSCR.FB位为1，OPSCR.U、OPSCR.V和OPSCR.W位可以读取OPSCR.UF、OPSCR.VF和OPSCR.WF位。

EN位（输出相位使能）

EN位控制输出相位（正相负相）的输出使能信号。

当OPSCR.EN位为1时，输出信号波形。

当OPSCR.EN位为0时，先设置OPSCR.FB、OPSCR.UFVFWF（选择软件设置）、OPSCR.PN、OPSCR.INV、OPSCR.RV、OPSCR.ALIGN、OPSCR.GRP[1:0]、OPSCR.GODF、OPSCR.NFEN、OPSCR.NFCS。然后，将该位设置为1。当POEG未发生输出禁用请求时，应设置EN位。此外，当OPSCR.GODF为1且在OPSCR.GRP[1:0]位中选择的信号值为高时，OPSCR.EN位设置为0。由要写入的软件设置为1，EN位保持为0.

返回时，请在软件清除OutputDisableRequest后，设置EN=1。

EN位优先级顺序（冲突）。

当软件写入1且输出禁用请求清0与EN位冲突时，输出禁用请求清0被激活。

FB位（外部反馈信号使能）

FB位从软件设置（OPSCR.UF、VF、WF）和霍尔元件等外部输入中选择输入相位。

P位（正相输出(P)控制）

P位为正相输出（GTOUUP、GTOVUP和GTOWUP引脚）选择电平信号输出或PWM信号输出之一。

N bit (Negative-Phase Output (N) Control)

The N bit selects one of the level signal output or PWM signal output for the negative-phase output (GTOULO, GTOVLO and GTOWLO pins).

INV bit (Output Phase Invert Control)

The INV bit selects one of the positive logic (active-high) output or negative logic (active-low) output for the output phase.

RV bit (Output Phase Rotation Direction Reversal Control)

The RV bit reverses the direction of rotation of the motor by inverting the input phase.

ALIGN bit (Input Phase Alignment)

The ALIGN bit selects the GTCLK or PWM for the sampling of the input phase (input phase is specified in the OPSCR.FB bit).

When OPSCR.ALIGN bit is 0, input phase is aligned to GTCLK.

Note: When the chopping is performed, there are cases where the PWM width of output is shorter than the width of the PWM used to chop just before or after switching of output phase, depending on the phase difference between the phase output switch timing and the phase of PWM.

When OPSCR.ALIGN bit is 1, input phase is aligned with the falling edge of PWM.

GRP[1:0] bit (Output Disabled Source Selection)

The GRP[1:0] bit selects the output disable source.

The GRP bits should be set when GODF bit is 0. If GRP bits select a POEG except for the connected groups, the status of output pin never change to disable.

GODF bit (Group Output Disable Function)

When OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0.

When OPSCR.GODF bit is 0, this bit is ignored.

The GODF bit should be set when output disable request doesn't occur from POEG.

NFEN bit (External Input Noise Filter Enable)

The NFEN bit selects the noise filter for external input. When OPSCR.NFEN bit is 0, a noise filter for the external input is not used.

Note: Set this bit during the EN bit is 0 to avoid generation of unintentional internal edge caused by switching this bit.

NFCS[1:0] bits (External Input Noise Filter Clock Selection)

The NFCS[1:0] bits select the clock for the external input noise filter. When the OPSCR.NFEN bit is 1, noise filter sampling clock setting of the external input is enabled.

1. Set the NFCS[1:0].
2. Wait for 2 cycles.
3. Set the OPSCR.EN bit to 1.

N位（负相输出(N)控制）

N位为反相输出（GTOULO、GTOVLO和GTOWLO引脚）选择电平信号输出或PWM信号输出之一。

INV位（输出相位反转控制）

INV位选择输出相位的正逻辑（高电平有效）输出或负逻辑（低电平有效）输出之一。

RV位（输出相位旋转方向反转控制）

RV位通过反转输入相位来反转电机的旋转方向。

ALIGN位（输入相位对齐）

ALIGN位选择GTCLK或PWM用于输入相位的采样（输入相位在OPSCR.FB位中指定）。

当OPSCR.ALIGN位为0时，输入相位与GTCLK对齐。

Note: 进行斩波时，输出的PWM宽度有时会比输出相位切换前后的斩波宽度短，这取决于相位输出切换时序和相位之间的相位差。脉宽调制。

当OPSCR.ALIGN位为1时，输入相位与PWM的下降沿对齐。

GRP[1:0]位（输出禁用源选择）

GRP[1:0]位选择输出禁用源。

当GODF位为0时，应设置GRP位。如果GRP位选择除连接组以外的POEG，则输出引脚的状态永远不会变为禁用。

GODF位（组输出禁用功能）

当OPSCR.GODF为1且OPSCR.GRP[1:0]位选择的信号值为高时，OPSCR.EN位设置为0。

当OPSCR.GODF位为0时，该位被忽略。

当POEG没有出现输出禁用请求时，应该设置GODF位。

NFEN位（外部输入噪声滤波器使能）

NFEN位选择外部输入的噪声滤波器。当OPSCR.NFEN位为0时，不使用外部输入的噪声滤波器。

Note: 在EN位为0期间设置该位，以避免由于切换该位而产生意外的内部边沿。

NFCS[1:0]位（外部输入噪声滤波器时钟选择）

NFCS[1:0]位选择外部输入噪声滤波器的时钟。当OPSCR.NFEN位为1时，使能外部输入的噪声滤波器采样时钟设置。

1.设置NFCS[1:0]。

2.等待2个周期。

3.将OPSCR.EN位设置为1。

21.2.47 GTCLKCR : General PWM Timer Clock Control Register

Base address: GPT_GTCLK = 0x4016_9B00

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BPEN	Synchronization Circuit Bypass Enable 0: In case of using Bus Clock and GPT Core Clock asynchronously 1: In case of using Bus Clock and GPT Core Clock synchronously	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

The GTCLKCR register is a register that controls the clock.

Set first of initial setting after resetting.

If MSTPCRE.MSTPE31 bit is 0, changing this register is prohibited.

BPEN bit (Synchronization Circuit Bypass Enable)

Enable or disable the synchronization bypass function between the bus clock (PCLKA) and GPT core clock (GTCLK).

Set 0 when using an asynchronous clock (GPTCLK) or 1 when using a synchronous clock (PCLKD) as the core clock.

21.3 Operation

21.3.1 Basic Operation

Each channel has a 32-bit timer that performs a periodic count operation using the count clock and hardware sources. The count function provides both up-counting and down-counting. The GTPR or GTCCRm (m = A to F) controls the count cycle.

When the GTCNT counter value matches the value in GTCCRA or GTCCRB, the output from the associated GTIOCnA or GTIOCnB can be changed (n = 0 to 9) . GTCCRA or GTCCRB can be used as an input capture register with hardware resources.

GTCCRC and GTCCRD can function as buffer registers for GTCCRA. GTCCRE and GTCCRF can function as buffer registers for GTCCRB.

21.3.1.1 Counter operation

(1) Counter start and stop

The counter of each channel starts the count operation when GTCR.CST is set to 1, and stops counting when the bit is set to 0. The GTCR.CST bit value is changed by the following sources:

- Writing to GTCR register
- Writing 1 to the bit in GTSTR associated with the GPT channel number when the GTSSR.CSTRT bit set to 1
- Writing 1 to the bit in GTSTP associated with the GPT channel number when the GTPSR.CSTOP bit set to 1
- The hardware source selected in the GTSSR register
- The hardware source selected in the GTPSR register.
- Completion of the period count function while the GTPC.ASTP bit is 1.

21.2.47 GTCLKCR:通用PWM定时器时钟控制寄存器

Base address: GPT_GTCLK = 0x4016_9B00

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BPEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BPEN	同步电路旁路使能 0：在异步使用总线时钟和GPT内核时钟的情况下1：在同时使用总线时钟和GPT内核时钟的情况下	R/W
31:1	—	这些位被读取为0。写入值应为0。	R/W

GTCLKCR寄存器是一个控制时钟的寄存器。

复位后设置第一个初始设置。

如果MSTPCRE.MSTPE31位为0，则禁止更改此寄存器。

BPEN位（同步电路旁路使能）

启用或禁用总线时钟(PCLKA)和GPT内核时钟(GTCLK)之间的同步旁路功能。

使用异步时钟(GPTCLK)时设置为0，使用同步时钟(PCLKD)作为核心时钟时设置为1。

21.3 Operation

21.3.1 基本操作

每个通道都有一个32位定时器，它使用计数时钟和硬件源执行周期性计数操作。计数功能提供向上计数和向下计数。GTPR或GTCCRm（m=A到F）控制计数周期。

当GTCNT计数器值与GTCCRA或GTCCRB中的值匹配时，相关GTIOCnA或GTIOCnB可以更改（n=0到9）。GTCCRA或GTCCRB可用作具有硬件资源的输入捕捉寄存器。

GTCCRC和GTCCRD可以作为GTCCRA的缓冲寄存器。GTCCRE和GTCCRF可以作为GTCCRB的缓冲寄存器。

21.3.1.1 计数器操作

(1) 计数器启动和停止

当GTCR.CST设置为1时，每个通道的计数器开始计数操作，并在该位设置为0时停止计数。GTCR.CST位值由以下来源改变：

- ●写入GTCR寄存器
- ●当GTSSR.CSTRT位设置为1时，将1写入GTSTR中与GPT通道号相关的位
- ●当GTPSR.CSTOP位设置为1时，将1写入GTSTP中与GPT通道号相关的位
- ●GTSSR寄存器中选择的硬件源
- ●GTPSR寄存器中选择的硬件源。
- ●GTPC.ASTP位为1时完成周期计数功能。

(2) Periodic count operation in up-counting by count clock

The GTCNT counter in each channel starts up-counting when the associated GTCR.CST bit is set to 1 with GTUPSR and GTDNSR registers set to 0x00000000. When the GTCNT value changes from the GTPR value to 0 (overflow) or the GTCCRm (m = A to F) value selected by the GTCSR.CSCMSC[2:0] bits to 0 in Saw-wave PWM mode 2, the GTST.TCFPO flag is set to 1, and the overflow interrupt(GPTn_OVF) is also generated. After GTCNT overflows, up-counting resumes from 0x00000000.

Figure 21.5 shows an example of a periodic count operation in up-counting by the count clock.

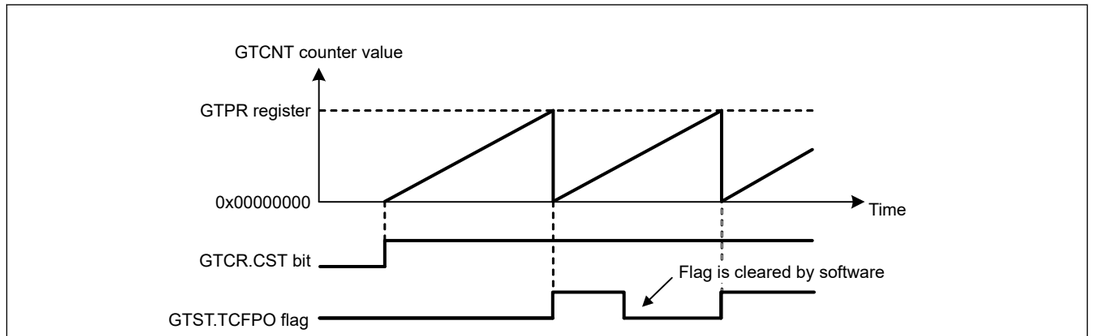


Figure 21.5 Example of periodic count operation in up-counting by the count clock

Table 21.11 shows an example for setting periodic count operation in up-counting by the count clock.

Table 21.11 Example for setting a periodic count operation in up-counting by the count clock

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.5, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.5, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode2, set the cycle in the GTPR register. In the saw-wave PWM mode2, select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 21.5, 0x00000000 is set.
6	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

(3) Periodic count operation in down-counting by count clock

The GTCNT counter in each channel can perform down-counting by setting GTUDDTYC.UD with GTUPSR and GTDNSR registers set to 0x00000000. When GTCNT changes from 0 to the GTPR value (underflow), GTST.TCFPU is set to 1, and the underflow interrupt(GPTn_UDF) is also generated. After the GTCNT counter underflows, down-counting resumes from the GTPR value.

Figure 21.6 shows an example of periodic count operation in down-counting by the count clock.

(2) 计数时钟递增计数中的周期计数操作

当相关的GTCR.CST位通过GTUPSR和
GTDNSR寄存器设置为0x00000000。当GTCNT值从GTPR值变为0（溢出）或
在锯波PWM模式2中，由GTCSR.CSCMSC[2:0]位选择的GTCCRm(m=AtoF)值为0，则
GTST.TCFPO标志置1，同时产生溢出中断(GPTn_OVF)。GTCNT溢出后，向上计数从0x00000000重新开始。

图21.5显示了计数时钟递增计数中的周期性计数操作的示例。

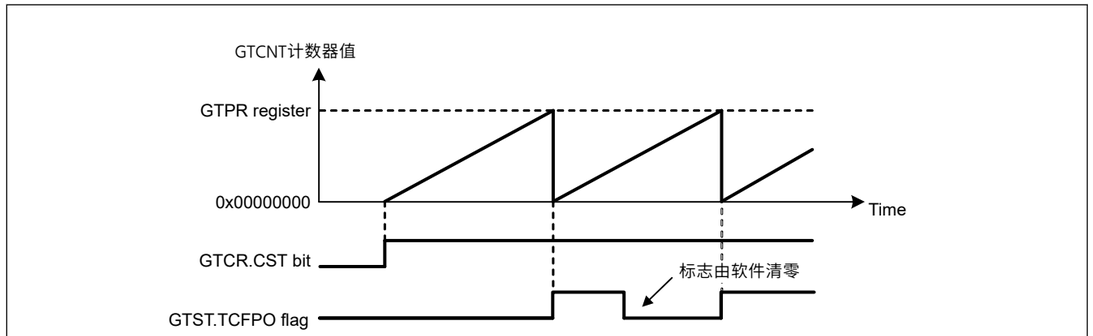


Figure 21.5 计数时钟递增计数中的周期计数操作示例

表21.11显示了在计数时钟的递增计数中设置周期性计数操作的示例。

Table 21.11 使用计数时钟在递增计数中设置周期性计数操作的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.5中，设置了000b或0000b（锯齿波PWM模式1）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.5中，在GTUDDTYC[1:0]位中设置了11b之后，在GTUDDTYC[1:0]位中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	除了锯齿波PWM模式2，在GTPR寄存器中设置周期。 在锯齿波PWM模式2中，通过GTCSR.CSCMSC[2:0]位选择计数器清零源比较匹配寄存器GTCCRx（x=A到F）并在该寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。在图21.5中，设置了0x00000000。
6	开始计数操作	将GTCR.CST位设置为1以启动计数操作。

(3) 计数时钟递减计数中的周期计数操作

每个通道中的GTCNT计数器可以通过使用GTUPSR设置GTUDDTYC.UD和
GTDNSR寄存器设置为0x00000000。当GTCNT从0变为GTPR值（下溢）时，GTST.TCFPU置1，同时产生下溢中断（GPTn_UDF）。GTCNT计数器下溢后，从GTPR值开始向下计数。

图21.6显示了计数时钟递减计数中周期性计数操作的示例。

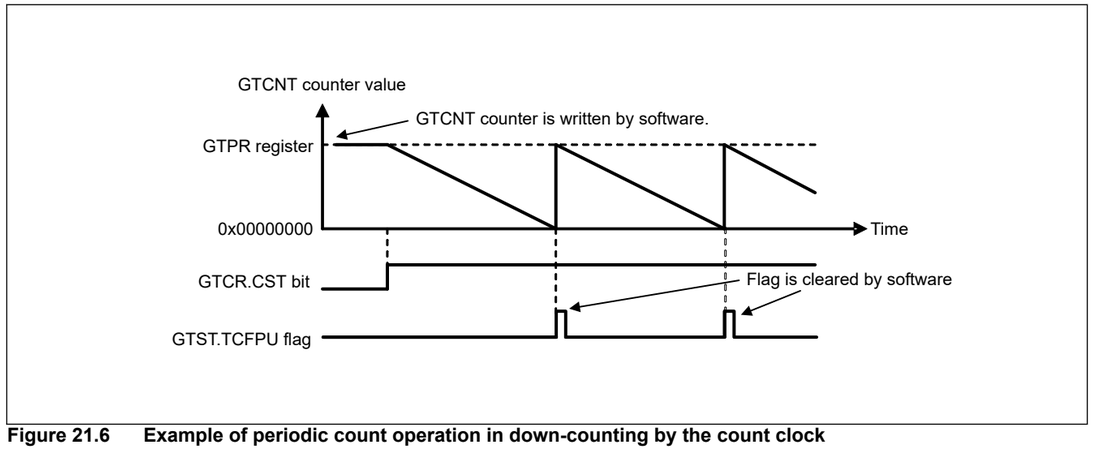


Figure 21.6 Example of periodic count operation in down-counting by the count clock

Table 21.12 shows an example for setting periodic count operation in down-counting by the count clock.

Table 21.12 Example for setting periodic count operation in down-counting by count clock

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.6, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction with the GTUDDTYC register. In Figure 21.6, after 10b is set in the GTUDDTYC[1:0] bits, 00b is set in the GTUDDTYC[1:0] bits (down-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 21.6, the GTPR register value is set.
6	Start count operation	Set the GTCR.CST bit to 1 to start count operation. In Figure 21.6, 1 is set in the CST bit.

(4) Event count operation in up-counting using hardware sources

The GTCNT counter in each channel can perform up-counting using hardware sources as set in GTUPSR.

When GTUPSR is set to enable, the count clock selected in GTCR.TPCS[3:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The overflow behavior when up-counting using hardware sources is the same as when up-counting by the count clock.

When GTCR.CST bit is set to 1 to count up using hardware sources, the count operation is enabled. After GTCR.CST is set to 1, the counter cannot count up for 1 clock cycle as specified in GTCR.TPCS[3:0] because the count operation is synchronized by the count clock selected in GTCR.TPCS[3:0]. Set GTCR.TPCS[3:0] to 000b to count up with a 1 GTCLK delay after GTCR.CST is set to 1.

Figure 21.7 and Figure 21.8 show an example of an event count operation in up-counting by a hardware resource (the rising edge of GTETRGA pin input and the rising edge of GTIOCnA pin input).

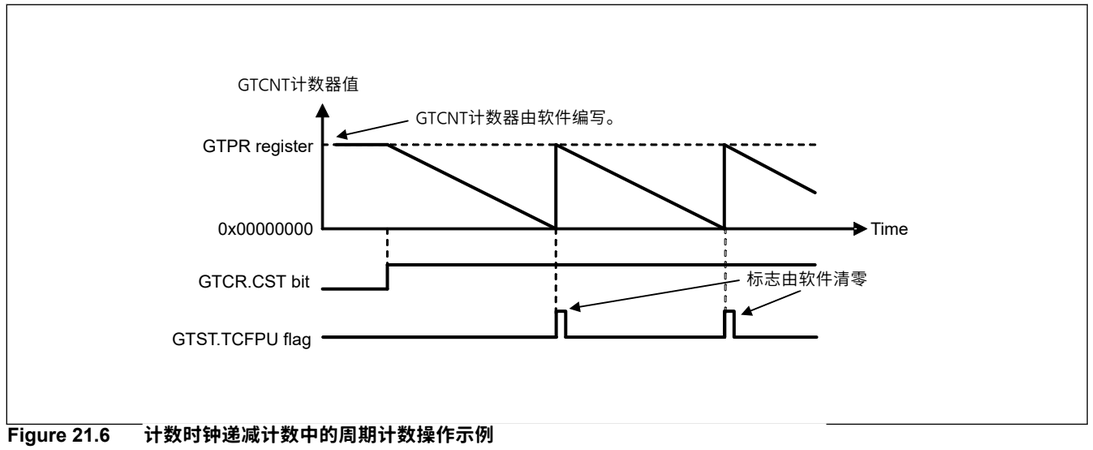


Figure 21.6 计数时钟递减计数中的周期计数操作示例

表21.12显示了在计数时钟的递减计数中设置周期性计数操作的示例。

Table 21.12 计数时钟递减计数中设置周期计数操作的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.6中，设置了000b或0000b（锯齿波PWM模式1）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向。 在图21.6中，在GTUDDTYC[1:0]位中设置10b后，在GTUDDTYC[1:0]位中设置00b（向下计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	在GTPR寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图21.6中，设置了GTPR寄存器的值。
6	开始计数操作	将GTCR.CST位设置为1以启动计数操作。 在图21.6中，CST位设置为1。

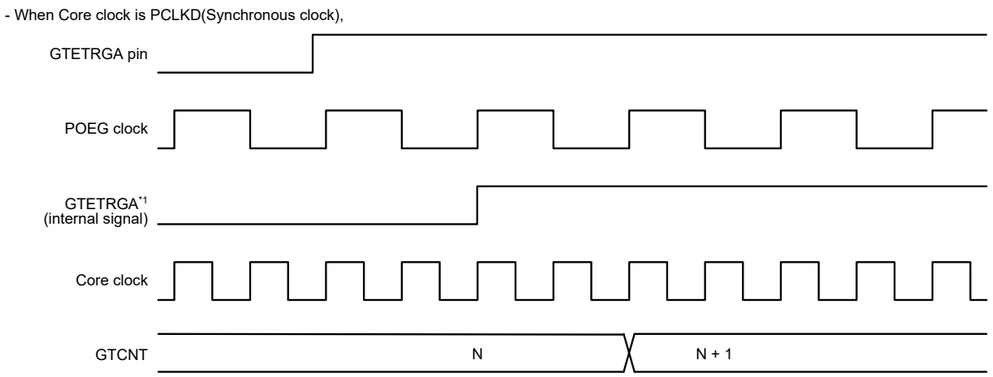
(4) 使用硬件源的递增计数中的事件计数操作

每个通道中的GTCNT计数器可以使用GTUPSR中设置的硬件源执行递增计数。

当GTUPSR设置为使能时，在GTCR.TPCS[3:0]中选择的计数时钟和在GTUDDTYC.UD被忽略。如果同时使用硬件源进行向上计数和向下计数，则GTCNT计数器值不会改变。使用硬件源递增计数时的溢出行为与使用计数时钟递增计数时的溢出行为相同。

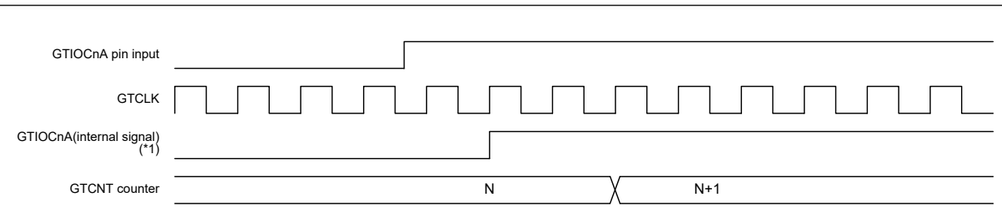
当GTCR.CST位设置为1以使用硬件源进行计数时，计数操作被启用。GTCR.CST设置为1后，计数器无法按GTCR.TPCS[3:0]中指定的1个时钟周期向上计数，因为计数操作与GTCR.TPCS[3:0]中选择的计数时钟同步。将GTCR.TPCS[3:0]设置为000b以在GTCR.CST设置为1后以1GTCLK延迟向上计数。

图21.7和图21.8显示了硬件资源递增计数中的事件计数操作示例（GTETRGA引脚输入的上升沿和GTIOCnA引脚输入的上升沿）。



Note: POEG clock: PCLKB
Note 1. The GTETRGA internal signal reflects the signal being input to the GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use.

Figure 21.7 Example of event count operation in up-counting using hardware sources



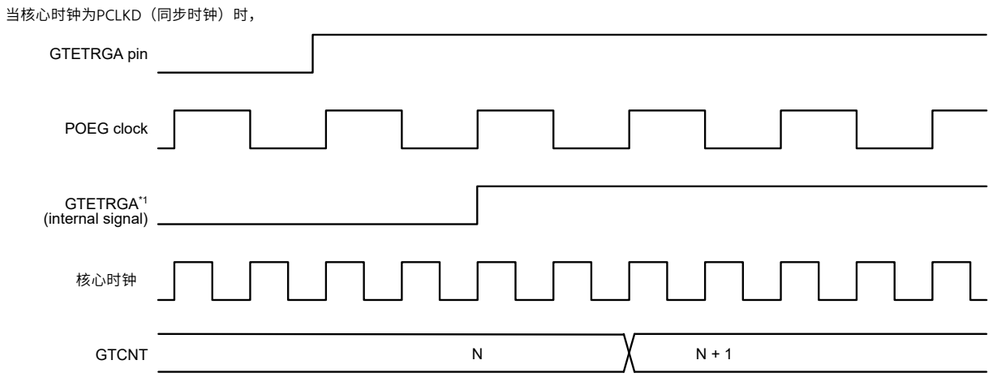
Note 1. This is the case when the digital noise filter is not in use.

Figure 21.8 Example of Event Count Operation (Up-Counting of Rising Edges of the Input on the GTIOCnA Pin)

Figure 21.9 shows an example of event count operation by ELC_GPTA event input.

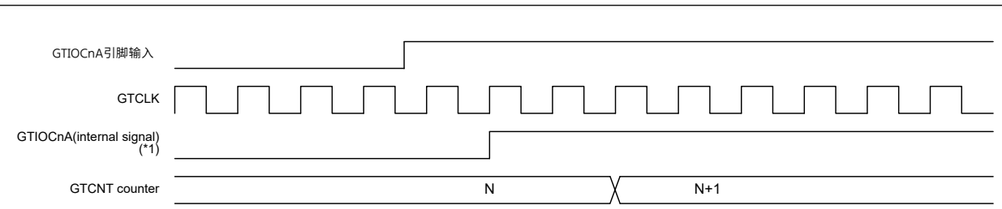
This is an example of event count operation of GPT321.GTCNT counter. An event signal is output to the ELC after matches in comparison with the GPT320.GTCCRA register. This is selected as a trigger for output to the GPT321 by the ELC as ELC_GPTA.

ELC passes the event signal output from GPT320 without delay to GPT321.



Note: POEG clock: PCLKB
注1.GTETRGA内部信号反映了当POEG中GTETRGA引脚的数字噪声滤波器未使用时输入到GPT的信号。

Figure 21.7 使用硬件源进行递增计数的事件计数操作示例



注1.这是不使用数字噪声滤波器时的情况。

Figure 21.8 事件计数操作示例（GTIOCnA上输入的上升沿递增计数 Pin)

图21.9显示了ELC_GPTA事件输入的事件计数操作示例。

这是GPT321.GTCNT计数器的事件计数操作示例。与GPT320.GTCCRA寄存器比较匹配后，向ELC输出一个事件信号。这被ELC选作ELC_GPTA输出到GPT321的触发器。

ELC将GPT320输出的事件信号无延迟地传递给GPT321。

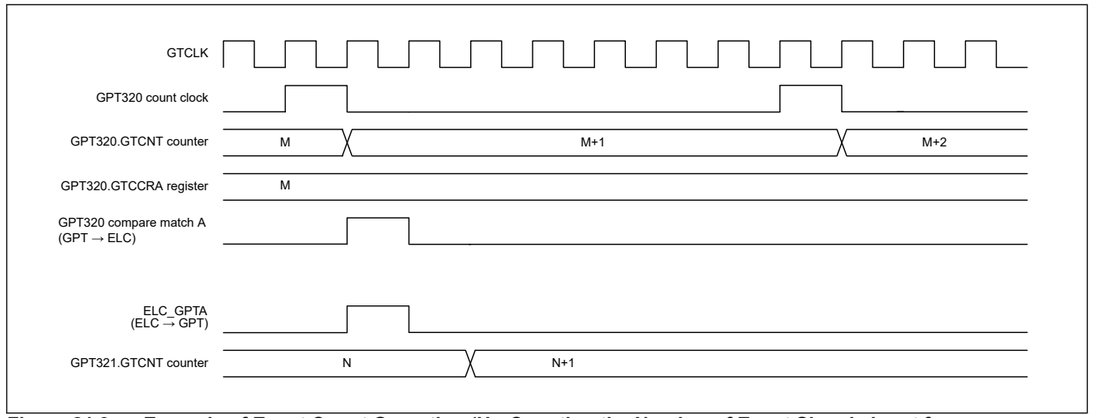


Figure 21.9 Example of Event Count Operation (Up-Counting the Number of Event Signals Input from ELC_GPTA)

Table 21.13 shows an example for setting event count operation in up-counting by a hardware source.

Table 21.13 Example for setting an event count operation in up-counting using hardware sources

No.	Step Name	Description
1	Set count source	Select the counting-up source with the GTUPSR register.
2	Set cycle	Set the cycle in the GTPR register.
3	Set initial value for counter	Set the initial value in the GTCNT counter.
4	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

(5) Event count operation in down-counting using hardware sources

The GTCNT counter in each channel can perform down-counting using hardware sources set in the GTDNSR.

When GTDNSR is set to enable, the count clock selected in GTCR.TPCS[3:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The underflow behavior when down-counting using hardware sources is the same as when down-counting by the count clock.

When GTCR.CST bit is set to 1 to count down using hardware sources, the count operation is enabled. After GTCR.CST is set to 1, the counter cannot count down for 1 clock cycle as specified in GTCR.TPCS[3:0] because the count operation is synchronized with the count clock selected in GTCR.TPCS[3:0]. Set GTCR.TPCS[3:0] to 000b to count down with a 1 GTCLK delay after GTCR.CST is set to 1.

Figure 21.10 shows an example of a event count operation in down-counting by a hardware resource (rising edge of GTETRGA pin).

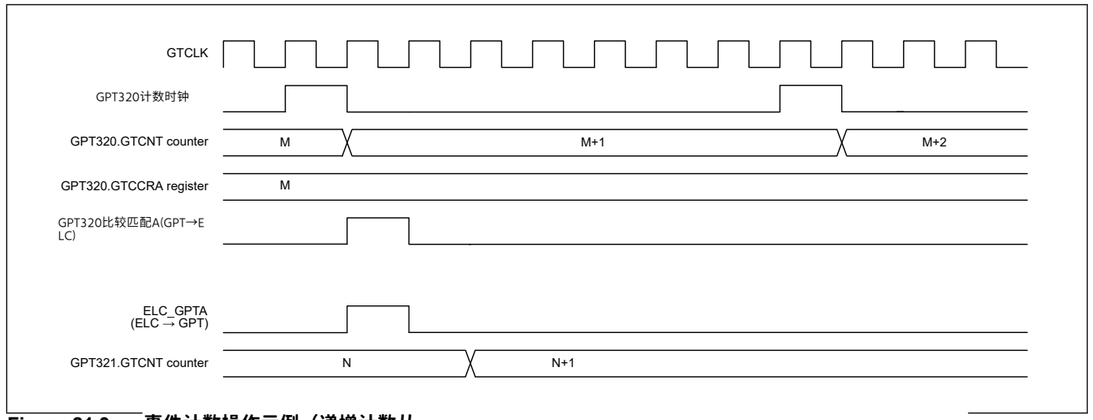


Figure 21.9 事件计数操作示例（递增计数从ELC_GPTA)

表21.13显示了通过硬件源在递增计数中设置事件计数操作的示例。

Table 21.13 使用硬件源在递增计数中设置事件计数操作的示例

No.	步骤名称	Description
1	设置计数源	使用GTUPSR寄存器选择递增计数源。
2	设置周期	在GTPR寄存器中设置周期。
3	设置计数器的初始值	在GTCNT计数器中设置初始值。
4	开始计数操作	将GTCR.CST位设置为1以启动计数操作。

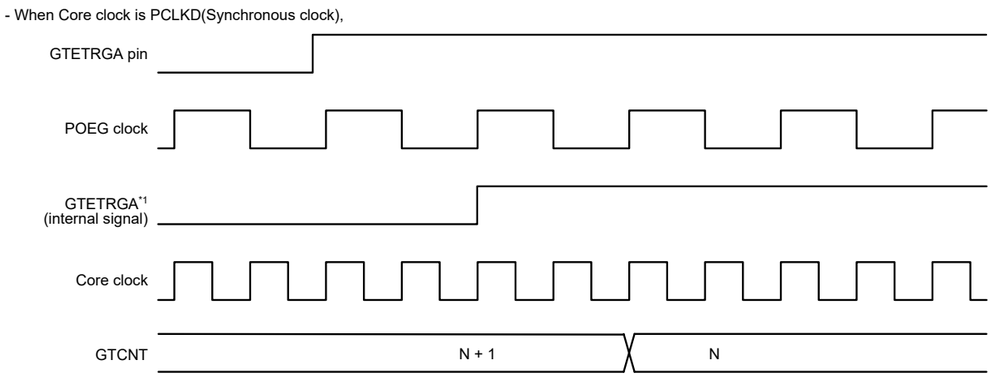
(5) 使用硬件源的递减计数中的事件计数操作

每个通道中的GTCNT计数器可以使用GTDNSR中设置的硬件源进行递减计数。

当GTDNSR设置为使能时，在GTCR.TPCS[3:0]中选择的计数时钟和在GTUDDTYC.UD被忽略。如果同时使用硬件源进行向上计数和向下计数，则GTCNT计数器值不会改变。使用硬件源向下计数时的下溢行为与使用计数时钟向下计数时相同。

当GTCR.CST位设置为1以使用硬件源进行递减计数时，启用计数操作。在GTCR.CST设置为1后，计数器无法按照GTCR.TPCS[3:0]中的规定向下计数1个时钟周期，因为计数操作与GTCR.TPCS[3:0]中选择的计数时钟同步。将GTCR.TPCS[3:0]设置为000b以在GTCR.CST设置为1后以1GTCLK延迟倒计时。

图21.10显示了一个硬件资源递减计数的事件计数操作示例（上升沿GTETRGA pin).



Note: POEG clock: PCLKB
Note 1. The GTETRGA internal signal reflects the signal being input to the GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use.

Figure 21.10 Example of event count operation in down-counting using hardware sources

Table 21.14 shows an example for setting a periodic count operation in down-counting using a hardware resource.

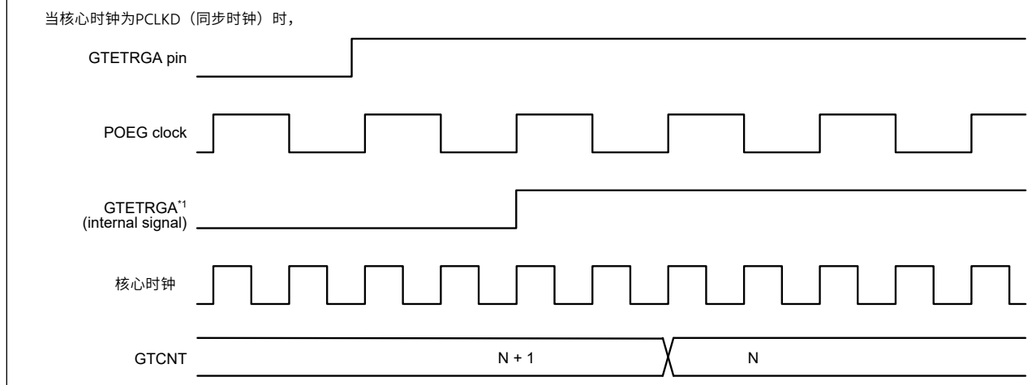
Table 21.14 Example for setting an event count operation in down-counting using hardware sources

No.	Step Name	Description
1	Set count source	Select the counting-down source with the GTDNSR register.
2	Set cycle	Set the cycle in the GTPR register.
3	Set initial value for counter	Set the initial value in the GTCNT counter.
4	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

(6) Counter clear operation

The counter of each channel is cleared by following sources:

- Writing 0 to GTCNT register
- Writing 1 to the bit in GTCLR associated with the GPT channel number when the GTCSR.CCLR bit set to 1
- The hardware source selected in GTCSR register.



Note: POEG clock: PCLKB
注1.GTETRGA内部信号反映了当POEG中GTETRGA引脚的数字噪声滤波器未使用时输入到GPT的信号。

Figure 21.10 使用硬件源递减计数中的事件计数操作示例

表21.14显示了使用硬件资源在递减计数中设置周期性计数操作的示例。

Table 21.14 使用硬件源在递减计数中设置事件计数操作的示例

No.	步骤名称	Description
1	设置计数源	使用GTDNSR寄存器选择倒计时源。
2	设置周期	在GTPR寄存器中设置周期。
3	设置计数器的初始值	在GTCNT计数器中设置初始值。
4	开始计数操作	将GTCR.CST位设置为1以启动计数操作。

(6) 计数器清零操作

每个通道的计数器由以下来源清零：

- ●将0写入GTCNT寄存器
- ●当GTCSR.CCLR位设置为1时，将1写入GTCLR中与GPT通道号相关的位
- ●GTCSR寄存器中选择的硬件源。

Writing to the GTCNT register is prohibited during count operation. Write access during counting (when CST = 1) is disabled. The GTCNT counter can be cleared both by writing 1 to the GTCLR and by the clear request of hardware sources, whether GTCNT is counting (GTCR.CST is 1) or not (GTCR.CST is 0).

When the count direction flag is set as decrement (GTST.TCUF flag = 0) in saw-wave mode (Except saw-wave PWM mode 2) selected with GTCR.MD[2:0] bits or GTCR.MD[3:0] bits, the GTCNT register is set to the value of the GTPR register when writing 1 to the GTCLR register and when clearing by hardware sources are performed.

When not in saw-waves mode (except saw-wave PWM mode 2) and down-counting, the GTCNT register is set to 0 when writing 1 to the GTCLR register and when clearing by hardware sources are performed.

In event count operation when at least 1 bit in the GTUPSR or GTDNSR is set to 1, after clear sources occur, both writing to GTCLR register and clearing by hardware sources are performed immediately to synchronize with GTCLK. If other settings are used, clear is synchronized with the counter clock selected in GTCR.TPCS[3:0].

21.3.1.2 Waveform output by compare match

Compare match means that the GTCNT counter value matches the value of GTCCRA or GTCCRB. When a compare match occurs, the compare match flag is generated synchronously with the count clock, including the event count. At the same time, the GPT can output low, high, or toggled output from the associated GTIOCnA or GTIOCnB output pin (n = 0 to 9). In addition, the GTIOCnA or GTIOCnB pin output can be low, high, or toggled at the cycle end which is determined by GTPR or GTCCRm selected as a counter clear source by the GTCSR.CSCMSC[2:0] bits in saw-wave PWM mode 2 (n = 0 to 9, m = A to F).

The cycle end is:

- For saw waves (except saw-wave PWM mode 2) in up-counting – when GTCNT changes from the GTPR value to 0 (overflow)
- For saw waves (except saw-wave PWM mode 2) in down-counting – when GTCNT changes from 0 to GTPR value (underflow)
- For saw-wave PWM mode 2 and GTCCRm register (m = A to F) selected as a counter clear source by the GTCSR.CSCMSC[2:0] bits – When the GTCNT counter value changes from the GTCCRm register value to 0x0000 0000
- For saw waves – when the GTCNT counter is cleared
- For triangle waves or complementary PWM mode – when the GTCNT changes from 0 to 1 (trough).

(1) Low output and high output

Figure 21.11 shows an example of low output and high output operation by a compare match of GTCCRA and GTCCRB.

In this example, the GTCNT counter performs up-counting, and settings are made so that high is output from the GTIOCnA pin by a GTCCRA compare match, and low is output from the GTIOCnB pin by a GTCCRB compare match. The pin level does not change when the specified level and pin level match.

计数操作期间禁止写入GTCNT寄存器。计数期间的写访问（当CST=1时）被禁用。GTCNT计数器可以通过向GTCLR写入1和硬件源的清除请求来清除，无论GTCNT正在计数（GTCR.CST为1）还是不计数（GTCR.CST为0）。

在使用GTCR.MD[2:0]位或GTCR.MD[3:0]位，当向GTCLR寄存器写入1和执行硬件源清除时，GTCNT寄存器设置为GTPR寄存器的值。

当不处于锯齿波模式（锯齿波PWM模式2除外）和向下计数时，当向GTCLR寄存器写入1和执行硬件源清零时，GTCNT寄存器设置为0。

在GTUPSR或GTDNSR中至少有1位设置为1的事件计数操作中，在清除源发生后，立即执行对GTCLR寄存器的写入和硬件源清除，以与GTCLK同步。如果使用其他设置，则清除与GTCR.TPCS[3:0]中选择的计数器时钟同步。

21.3.1.2 比较匹配的波形输出

比较匹配意味着GTCNT计数器值与GTCCRA或GTCCRB的值匹配。当比较匹配发生时，比较匹配标志与计数时钟同步生成，包括事件计数。同时，GPT可以从相关的GTIOCnA或GTIOCnB输出引脚（n=0到9）输出低电平、高电平或翻转输出。此外，GTIOCnA或GTIOCnB引脚输出可以是低电平、高电平或在周期结束时切换，由下式确定

GTPR或GTCCRm在锯齿波PWM模式2（n=0到9，m=A到F）中由GTCSR.CSCMSC[2:0]位选择作为计数器清零源。

循环结束为：

●对于递增计数中的锯齿波（锯齿波PWM模式2除外） 当GTCNT从GTPR值变为0时（溢出）

●对于向下计数中的锯齿波（锯齿波PWM模式2除外） 当GTCNT从0变为GTPR值时（下溢）

●对于锯齿波PWM模式2和GTCCRm寄存器（m=A到F）被选择为计数器清零源
GTCSR.CSCMSC[2:0]位——当GTCNT计数器值从GTCCRm寄存器值变为0x00000000时

●对于锯齿波 当GTCNT计数器清零时

●对于三角波或互补PWM模式 当GTCNT从0变为1（波谷）时。

(1) 低输出和高输出

图21.11显示了通过GTCCRA和GTCCRB比较匹配的低输出和高输出操作示例。

在本例中，GTCNT计数器进行递增计数，设定为通过GTCCRA比较匹配从GTIOCnA引脚输出高电平，通过GTCCRB比较匹配从GTIOCnB引脚输出低电平。当指定电平和引脚电平匹配时，引脚电平不会改变。

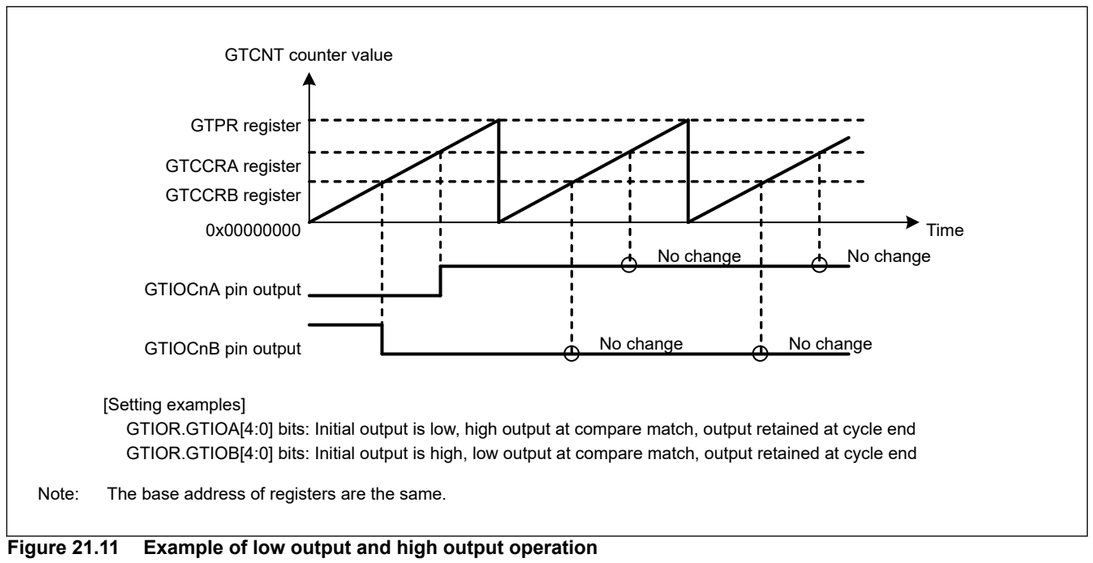


Figure 21.11 Example of low output and high output operation

Table 21.15 shows an example for setting low output and high output operation.

Table 21.15 Example for setting low output and high output operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.11, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.11, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode2, set the cycle in the GTPR register. In the saw-wave PWM mode2, select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 21.11, GTIOA[4:0] = 00010b, GTIOB[4:0] = 10001b.
7	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set compare match value*1	Set compare match values in the GTCCRA and GTCCRB registers.
9	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

Note: n: 0 to 9
m: A, B
Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnm pin output enable and setting for a compare match value.

(2) Toggled output

Figure 21.12 and Figure 21.13 show examples of toggled output operation by compare matches of GTCCRA and GTCCRB.

In Figure 21.12, the GTCNT counter performs up-counting, and settings are made so that the GTIOCnA pin output by a GTCCRA compare match and GTIOCnB pin output by a GTCCRB compare match are toggled.

In Figure 21.13, the GTCNT counter performs up-counting, and settings are made so that a GTCCRA compare match toggles the GTIOCnA pin output level and a cycle end toggles the GTIOCnB pin output level.

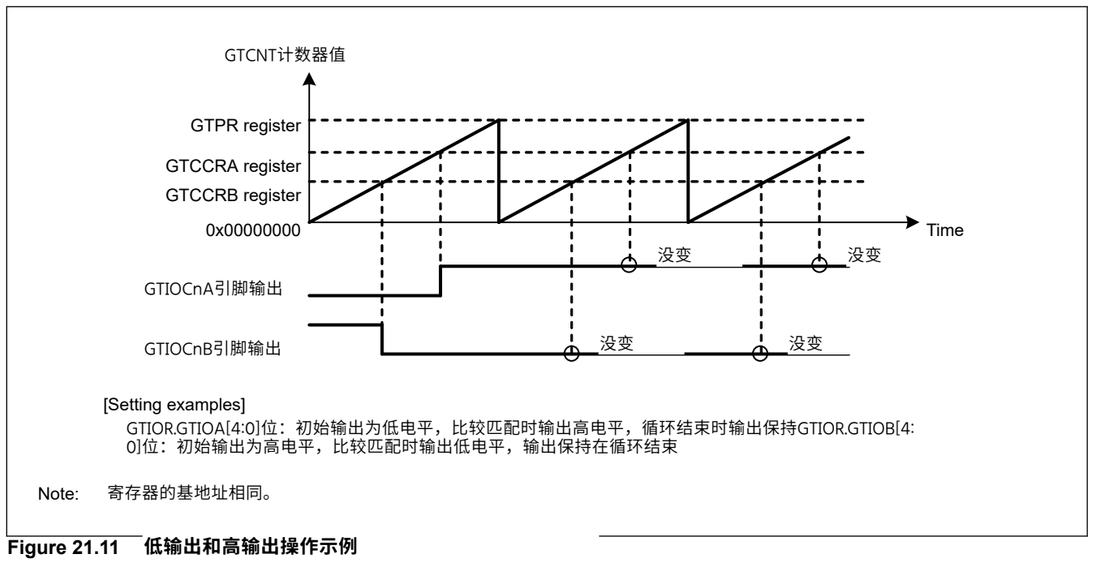


Figure 21.11 低输出和高输出操作示例

表21.15显示了设置低输出和高输出操作的示例。

Table 21.15 设置低输出和高输出操作的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.11中，设置了000b或0000b（锯齿波PWM模式1）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.11中，在GTUDDTYC[1:0]位中设置了11b之后，在GTUDDTYC[1:0]位中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	除了锯齿波PWM模式2，在GTPR寄存器中设置周期。 在锯齿波PWM模式2中，通过GTCSR.CSCMSC[2:0]位选择计数器清零源比较匹配寄存器GTCCRx（x=A到F）并在该寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR寄存器中的GTIOA[4:0]和GTIOB[4:0]位设置GTIOCnm引脚功能。 在图21.11中，GTIOA[4:0]=00010b，GTIOB[4:0]=10001b。
7	启用GTIOCnm引脚输出*1	通过GTIOR寄存器中的OAE和OBE位设置使能GTIOCnm引脚输出。
8	设置比较匹配值*1	在GTCCRA和GTCCRB寄存器中设置比较匹配值。
9	开始计数操作	将GTCR.CST位设置为1以启动计数操作。

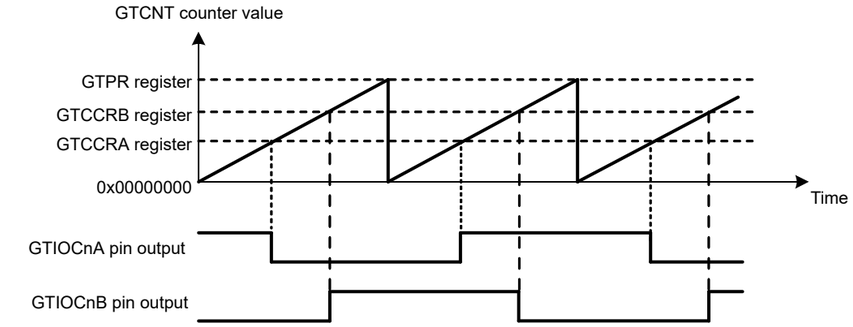
Note: n: 0 to 9
m: A, B
注1.使用PWM延迟产生电路时，更改GTIOCnm引脚输出使能设置和比较匹配值设置的顺序。

(2) Toggled output

图21.12和图21.13通过GTCCRA和GTCCRB的比较匹配显示了切换输出操作的示例。

在图21.12中，GTCNT计数器进行递增计数，并进行设置以使GTIOCnA引脚输出GTCCRA比较匹配和GTCCRB比较匹配的GTIOCnB引脚输出被切换。

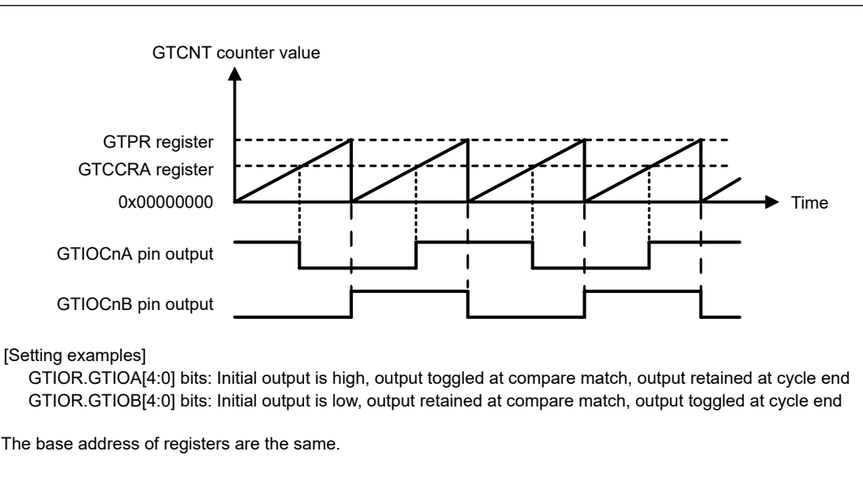
在图21.13中，GTCNT计数器执行递增计数，并进行设置，以便GTCCRA比较匹配切换GTIOCnA引脚输出电平，循环结束切换GTIOCnB引脚输出电平。



[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial output is high, output toggled at compare match, output retained at cycle end
GTIOR.GTIOB[4:0] bits: Initial output is low, output toggled at compare match, output retained at cycle end

Note: The base address of registers are the same.

Figure 21.12 Example of toggled output operation (1)



[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial output is high, output toggled at compare match, output retained at cycle end
GTIOR.GTIOB[4:0] bits: Initial output is low, output retained at compare match, output toggled at cycle end

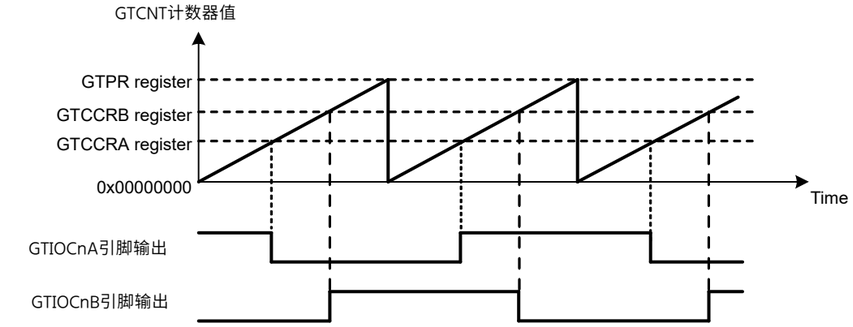
Note: The base address of registers are the same.

Figure 21.13 Example of toggled output operation (2)

Table 21.16 shows an example for setting toggled output operation.

Table 21.16 Example for setting toggled output operation (1 of 2)

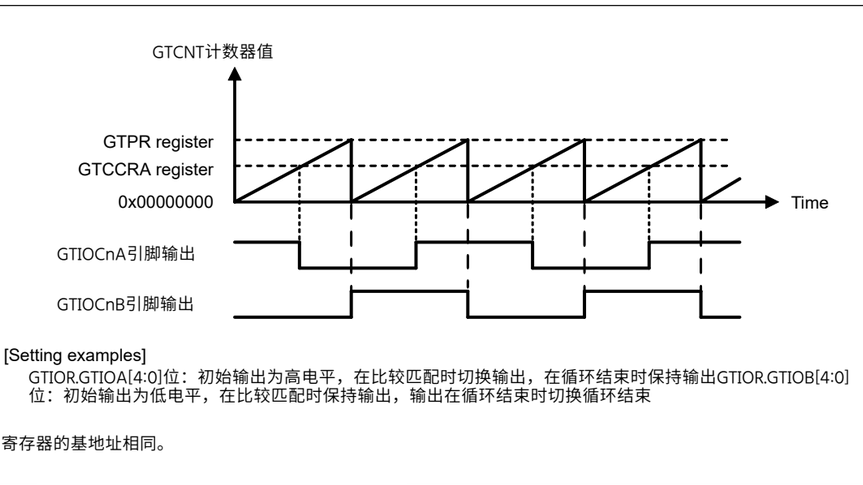
No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.12 and Figure 21.13, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.12 and Figure 21.13, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode2, set the cycle in the GTPR register. In the saw-wave PWM mode2, select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.



[Setting examples]
GTIOR.GTIOA[4:0]位：初始输出为高电平，在比较匹配时触发输出，在循环结束时保持输出GTIOR.GTIOB[4:0]位：初始输出为低电平，在比较匹配时触发输出，输出保持在循环结束

Note: 寄存器的基地址相同。

Figure 21.12 切换输出操作示例(1)



[Setting examples]
GTIOR.GTIOA[4:0]位：初始输出为高电平，在比较匹配时切换输出，在循环结束时保持输出GTIOR.GTIOB[4:0]位：初始输出为低电平，在比较匹配时保持输出，输出在循环结束时切换循环结束

Note: 寄存器的基地址相同。

Figure 21.13 切换输出操作示例(2)

表21.16显示了设置切换输出操作的示例。

Table 21.16 设置切换输出操作的示例(1of2)

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.12和图21.13中，设置了000b或0000b（锯齿波PWM模式1）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。在图21.12和图21.13中，在GTUDDTYC[1:0]位中设置11b后，在GTUDDTYC[1:0]位中设置01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	除了锯齿波PWM模式2，在GTPR寄存器中设置周期。 在锯齿波PWM模式2中，通过GTCSR.CSCMSC[2:0]位选择计数器清零源比较匹配寄存器GTCCRx（x=A到F）并在该寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。

Table 21.16 Example for setting toggled output operation (2 of 2)

No.	Step Name	Description
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 21.12, GTIOA[4:0] = 10011b, GTIOB[4:0] = 00011b, and in Figure 21.13, GTIOA[4:0] = 10011b, GTIOB[4:0] = 01100b.
7	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set compare match value*1	Set compare match values in the GTCCRA and GTCCRB registers.
9	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

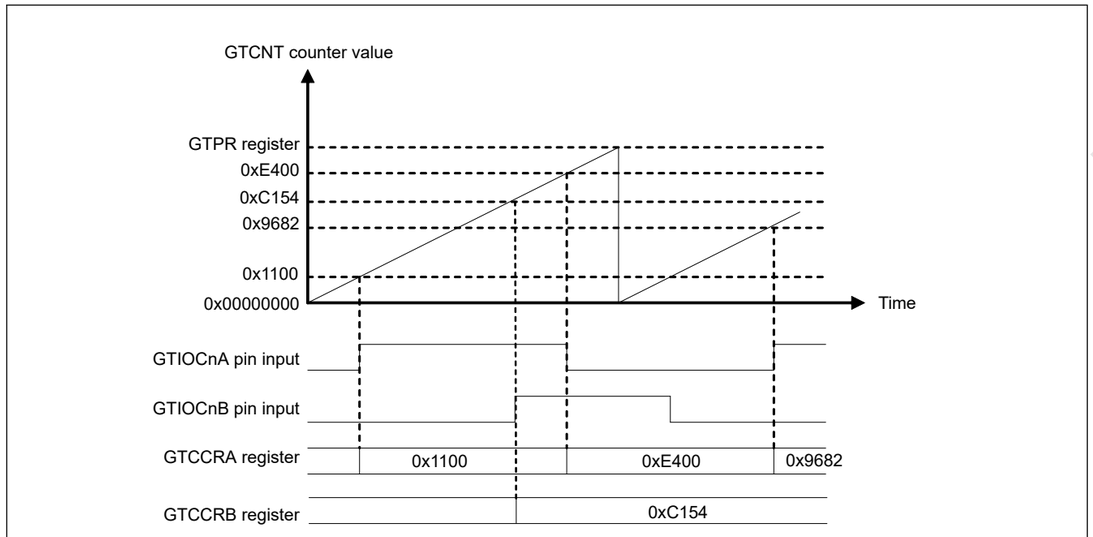
Note: n: 0 to 9
m: A, B
Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnm pin output enable and setting for a compare match value.

21.3.1.3 Input Capture Function

The GTCNT counter value can be transferred to either GTCCRA or GTCCRB on detection of the hardware source that is set in GTICASR and GTICBSR. In complementary PWM mode, GTCCRA and GTCCRB registers do not function as input capture registers.

Figure 21.14 shows an example of the input capture function.

In this example, the GTCNT counter performs up-counting by the count clock, and settings are made so that an input capture is performed to GTCCRA at both edges of the GTIOCnA input pin and to GTCCRB on the rising edge of the GTIOCnB input pin.



Note: The base address of registers are the same.
Note: [Setting examples]
GTICASR setting: input capture at both edges
GTICBSR setting: input capture at the rising edge

Figure 21.14 Example of input capture operation

Table 21.17 and Table 21.21 show the example for setting an input capture operation with count operation by the count clock.

Table 21.16 设置切换输出操作的示例(2of2)

No.	步骤名称	Description
6	设置GTIOCnm引脚功能	使用GTIOR寄存器中的GTIOA[4:0]和GTIOB[4:0]位设置GTIOCnm引脚功能。在图21.12中，GTIOA[4:0]=10011b，GTIOB[4:0]=00011b，在图21.13中，GTIOA[4:0]=10011b，GTIOB[4:0]=01100b。
7	启用GTIOCnm引脚输出*1	通过GTIOR寄存器中的OAE和OBE位设置使能GTIOCnm引脚输出。
8	设置比较匹配值*1	在GTCCRA和GTCCRB寄存器中设置比较匹配值。
9	开始计数操作	将GTCR.CST位设置为1以启动计数操作。

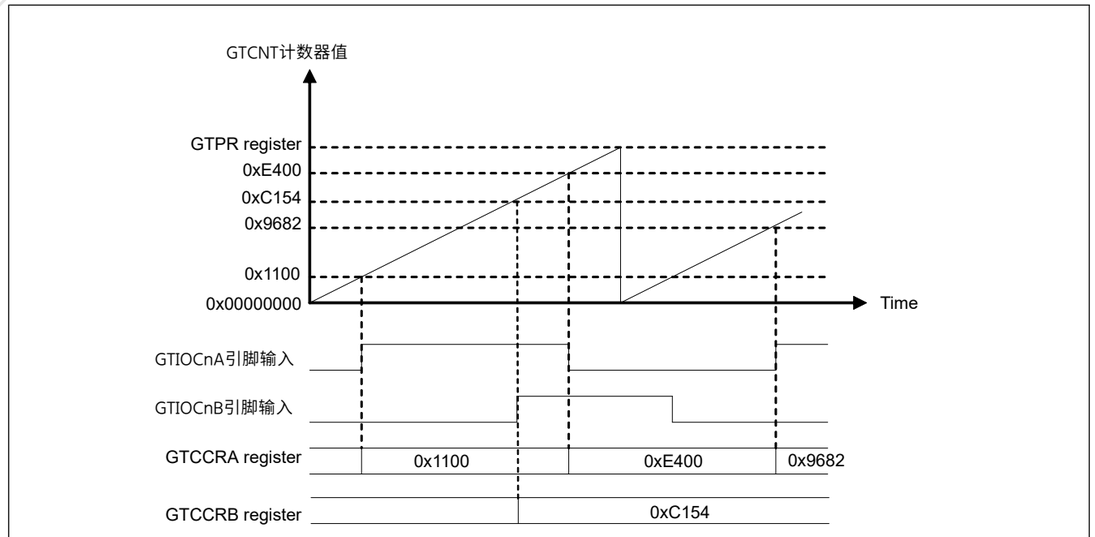
Note: n: 0 to 9
m: A, B
注1.使用PWM延迟产生电路时，更改GTIOCnm引脚输出使能设置和比较匹配值设置的顺序。

21.3.1.3 输入捕捉功能

在检测到在GTICASR和GTICBSR中设置的硬件源时，可以将GTCNT计数器值传输到GTCCRA或GTCCRB。在互补PWM模式下，GTCCRA和GTCCRB寄存器不用作输入捕捉寄存器。

图21.14显示了输入捕获函数的示例。

在本例中，GTCNT计数器通过计数时钟进行递增计数，并设置为在GTIOCnA输入引脚的两个边沿对GTCCRA执行输入捕捉，在GTIOCnB输入引脚的上升沿对GTCCRB执行输入捕捉。



Note: 寄存器的基地址相同。
Note: [设置示例]GTICASR设置：双边缘输入捕获
GTICBSR设置：在上升沿输入捕捉

Figure 21.14 输入捕捉操作示例

表21.17和表21.21显示了通过计数时钟设置计数操作的输入捕捉操作的示例。

Table 21.17 Example for setting input capture operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.14, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.14, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode2, set the cycle in the GTPR register. In the saw-wave PWM mode2, select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Select input capture source	Select the input capture source in the GTICASR and GTICBSR registers. In Figure 21.14, GTICASR = 0x00000F00, GTICBSR = 0x00003000. When input capture by other channel sources is used, set the GTICmSR.mSOC bit (m = A or B) to 1 and allow input capture by other channel sources, and select the group that cooperates with other channel sources by the GTICCR register.
7	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

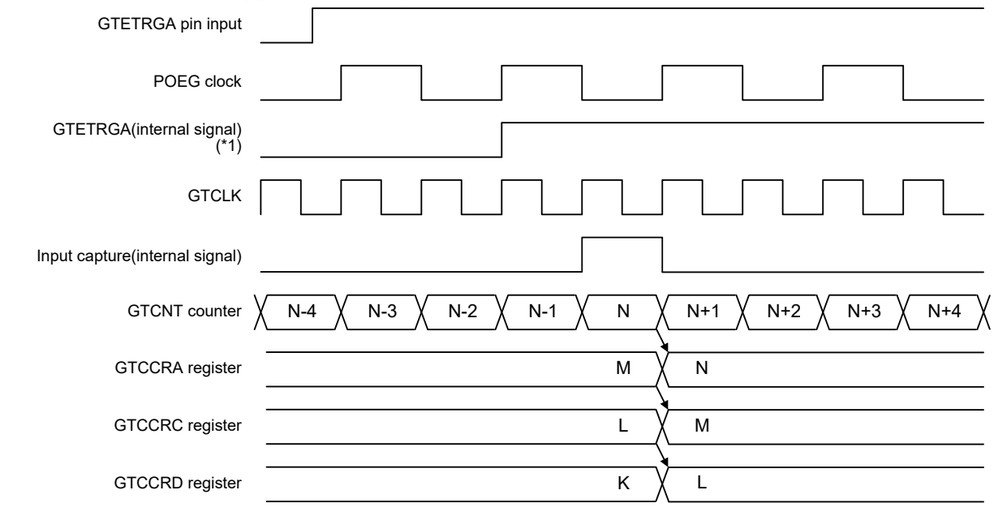
Figure 21.15 shows an example of the timing of input capture operation in response to a rising edge of the input on the GTETRGA pin.

Table 21.17 设置输入捕捉操作的示例

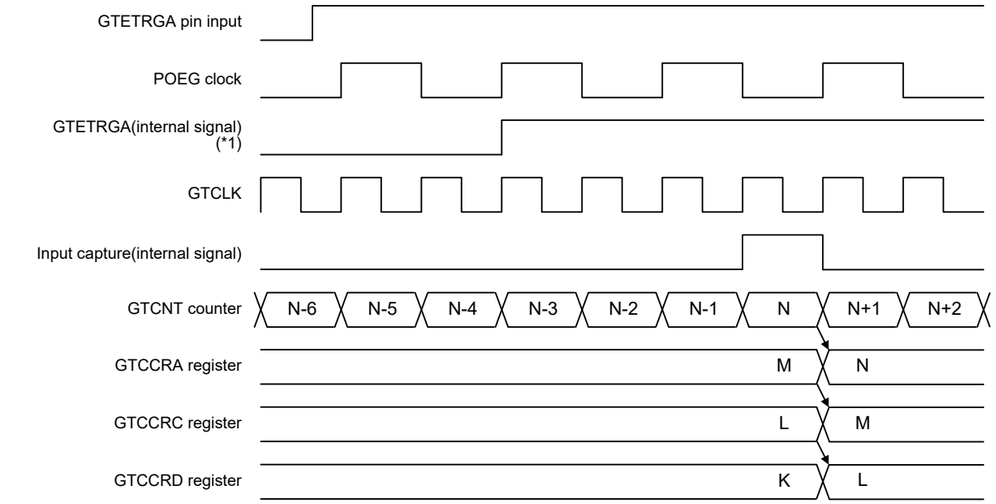
No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.14中，设置了000b或0000b（锯齿波PWM模式1）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.14中，在GTUDDTYC[1:0]位中设置11b后，在GTUDDTYC[1:0]位中设置01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	除了锯齿波PWM模式2，在GTPR寄存器中设置周期。 在锯齿波PWM模式2中，通过GTCSR.CSCMSC[2:0]位选择计数器清零源比较匹配寄存器GTCCRx（x=A到F）并在该寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	选择输入捕捉源	在GTICASR和GTICBSR寄存器中选择输入捕捉源。 在图21.14中，GTICASR=0x00000F00，GTICBSR=0x00003000。 当使用其他通道源的输入捕获时，将GTICmSR.mSOC位（m=A或B）设置为1并允许其他通道源的输入捕获，并通过GTICCR寄存器选择与其他通道源配合的组。
7	开始计数操作	将GTCR.CST位设置为1以启动计数操作。

图21.15显示了响应输入的上升沿的输入捕捉操作的时序示例
GTETRGA pin.

- When Core clock is PCLKD(Synchronous clock),



- When Core clock is GPTCLK(Asynchronous clock),

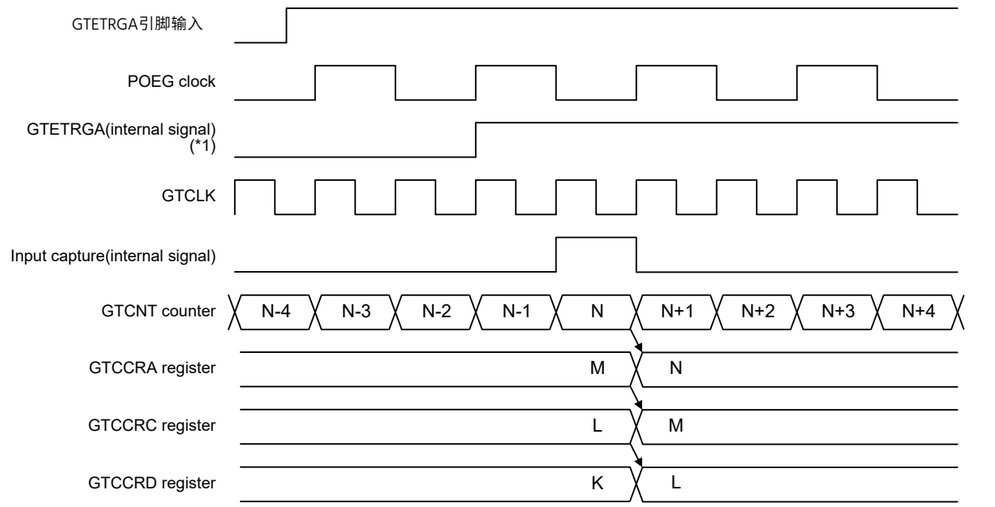


Note: POEG clock: PCLKB
Note 1. The GTETRGA internal signal reflects the signal being input to GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use.

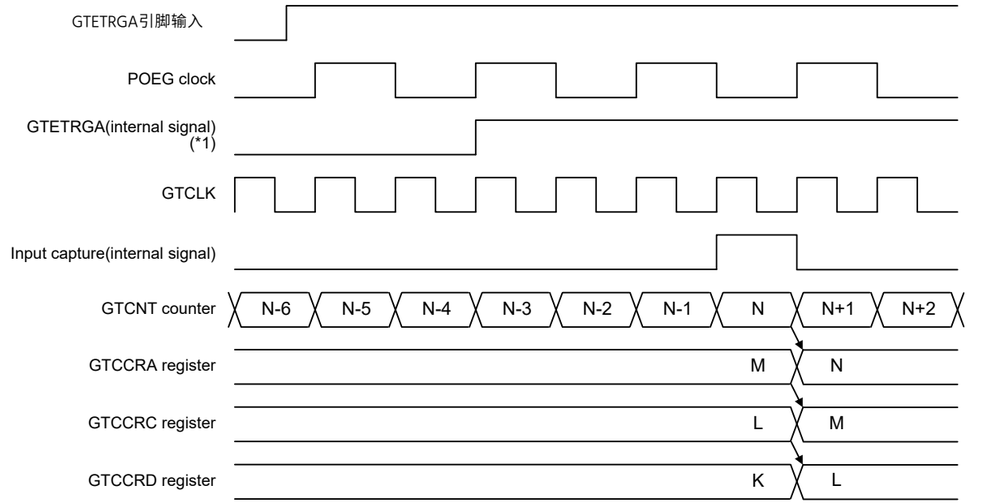
Figure 21.15 Example of the Timing of Input Capture Operation in Response to a Rising Edge of the Input on the GTETRGA Pin

Figure 21.16 shows an example of the timing of input capture operation in response to a rising edge of the input on the GTIOCnA pin.

当核心时钟为PCLKD（同步时钟）时，



当核心时钟为GPTCLK（异步时钟）时，



Note: POEG clock: PCLKB
注1.GTETRGA内部信号反映了当POEG中GTETRGA引脚的数字噪声滤波器未使用时输入到GPT的信号。

Figure 21.15 响应GTETRGA引脚上的输入上升沿的输入捕捉操作时序示例

图21.16显示了响应于输入的上升沿的输入捕捉操作的时序示例
GTIOCnA pin.

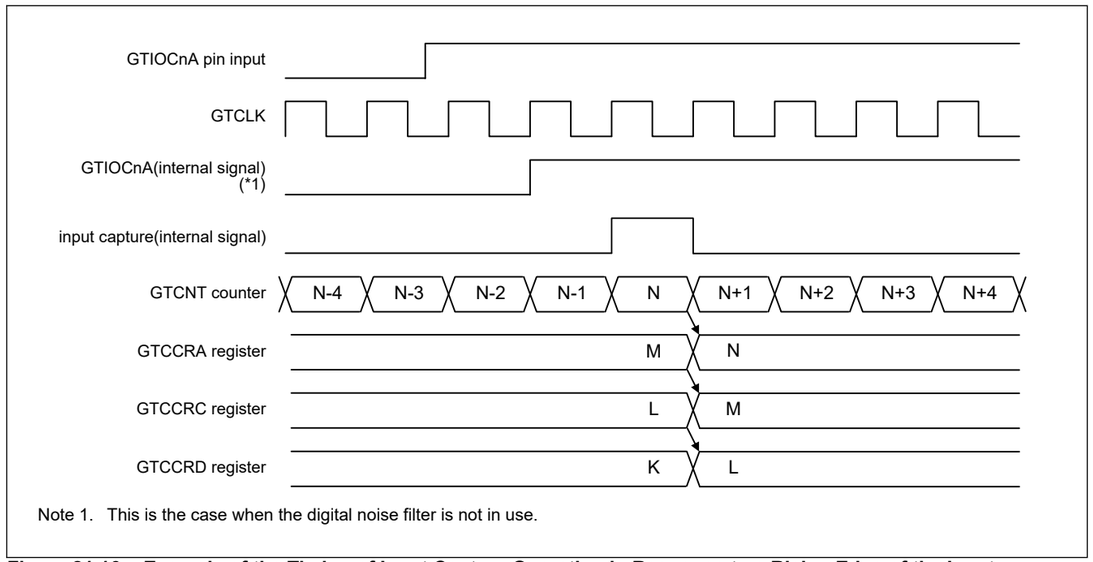


Figure 21.16 Example of the Timing of Input Capture Operation in Response to a Rising Edge of the Input on the GTIOCnA Pin

Figure 21.17 shows an example of the timing of input capture operation in response to ELC_GPTA event input.

This is an example of capture of the counter value by the GPT321.GTCCRA register in response to an input signal. An event signal is output to the ELC after matches in comparison with the GPT320.GTCCRA register. This is selected as a trigger for output to the GPT321 by the ELC as ELC_GPTA.

ELC passes the event signal output from GPT320 without delay to GPT321.

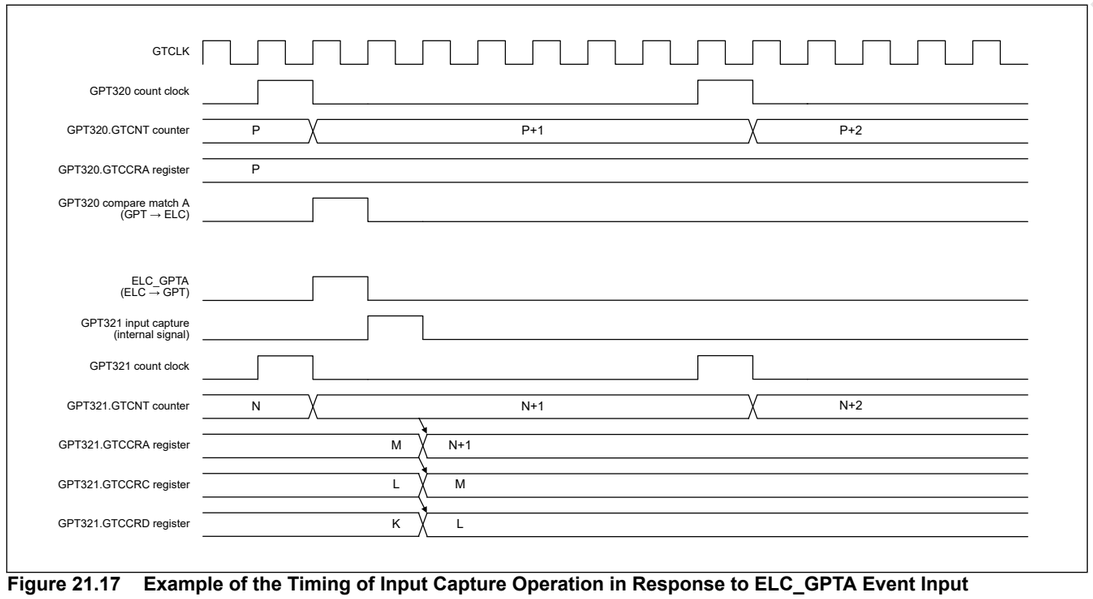


Figure 21.17 Example of the Timing of Input Capture Operation in Response to ELC_GPTA Event Input

Figure 21.18 shows an example of the timing of input capture operation in response to count clock from other channel.

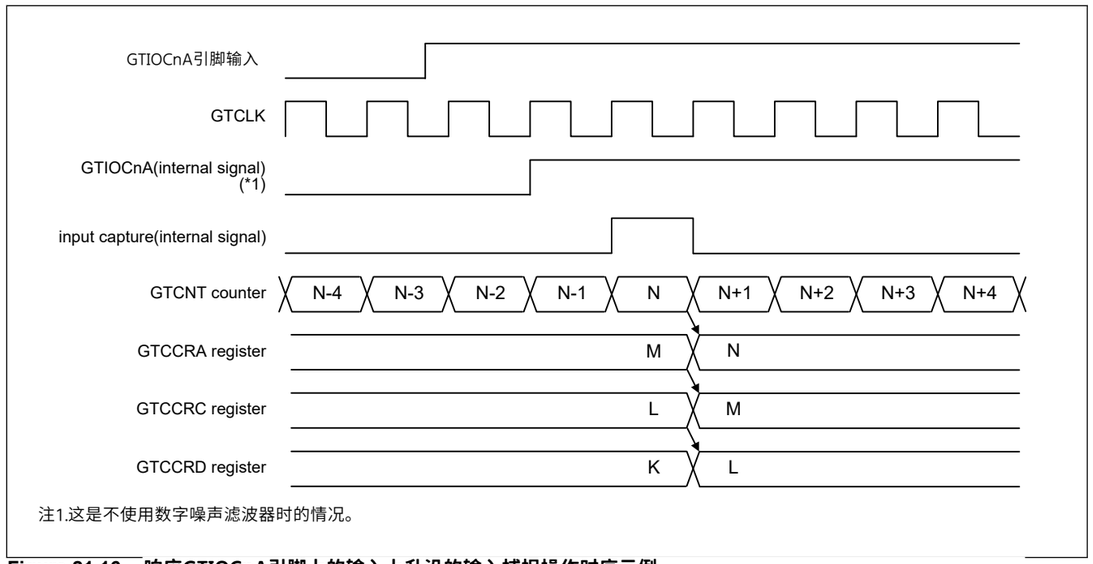


Figure 21.16 响应GTIOCnA引脚上的输入上升沿的输入捕捉操作时序示例

图21.17显示了响应ELC_GPTA事件输入的输入捕获操作的时序示例。

这是GPT321.GTCCRA寄存器响应输入信号捕获计数器值的示例。与GPT320.GTCCRA寄存器比较匹配后，向ELC输出一个事件信号。这被ELC选作ELC_GPTA输出到GPT321的触发器。

ELC将GPT320输出的事件信号无延迟地传递给GPT321。

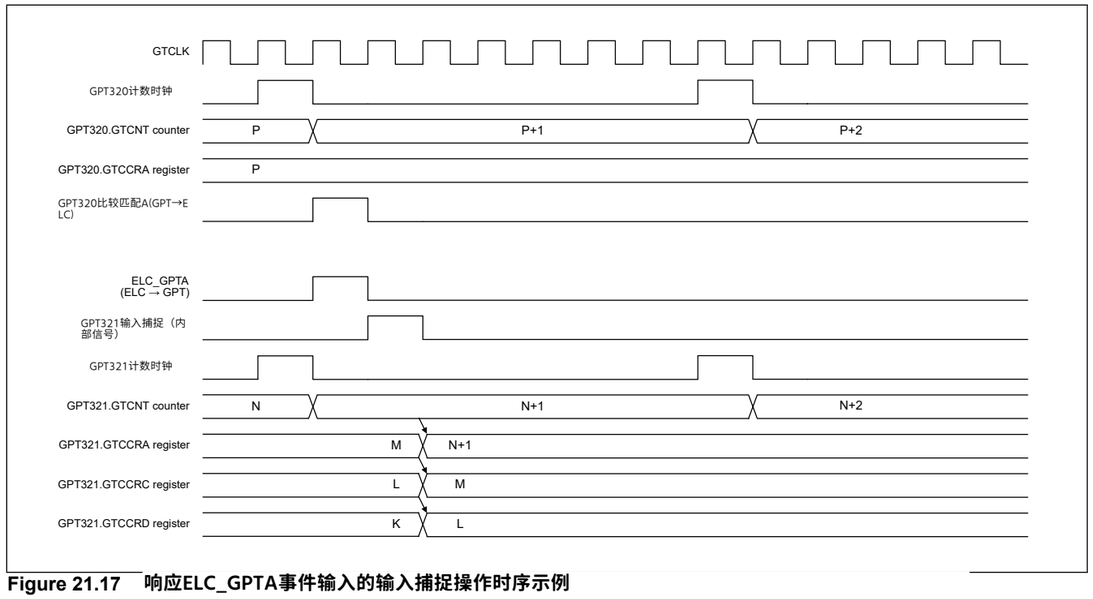


Figure 21.17 响应ELC_GPTA事件输入的输入捕捉操作时序示例

图21.18显示了响应来自其他通道的计数时钟的输入捕捉操作的时序示例。

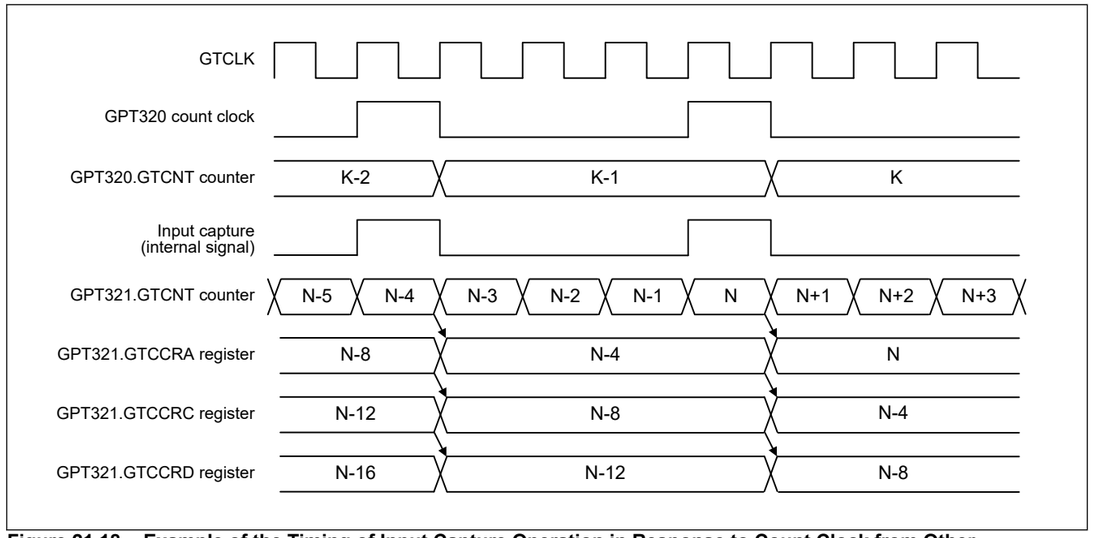


Figure 21.18 Example of the Timing of Input Capture Operation in Response to Count Clock from Other Channel

21.3.2 Buffer Operation

The following buffer operations can be set with GTBER:

- GTPR, GTPBR, and GTPDBR
- GTCCRA, GTCCRC, and GTCCRD
- GTCCRB, GTCCRE, and GTCCRF
- GTADTRA, GTADTBRA, and GTADTDBRA
- GTADTRB, GTADTBRB, and GTADTDBRB

The following buffer operation is enabled by setting GTDTCR:

- GTDVU and GTDBU
- GTDVD and GTDBD

The following buffer operation is enabled by setting GTBER2:

- GTCCRA, GTCCRE, and GTCCRF (in complementary PWM mode 3, 4)
- GTOLBR.GTIOAB[4:0] bits and GTIOR.GTIOA[4:0] bits
- GTOLBR.GTIOBB[4:0] bits and GTIOR.GTIOB[4:0] bits

21.3.2.1 GTPR Register Buffer Operation

GTPBR can function as a buffer register for GTPR.

GTPDBR register can function as a buffer register for the GTPBR register (double-buffer register for the GTPR register).

In complementary PWM mode, the buffer transfer from the GTPDBR register to temporary register P is performed only in the master channel (GPT32n). The temporary register P is transferred to each GTPBR register of master channel, slave channel 1 (GPT32n+1), and slave channel 2 (GPT32n+2). Transfer from the GTPBR register to the GTPR register is made concurrently in three channels. Therefore, the same value is stored in the same register of the three channels. The GTPR register of the master channel represents the GTCNT counter's (GTCNTn) period of the master channel. In the slave channels, periods are controlled using the GTPR register value and the GTDVU register value.

The setting is invalid in the Saw-wave PWM mode 2.

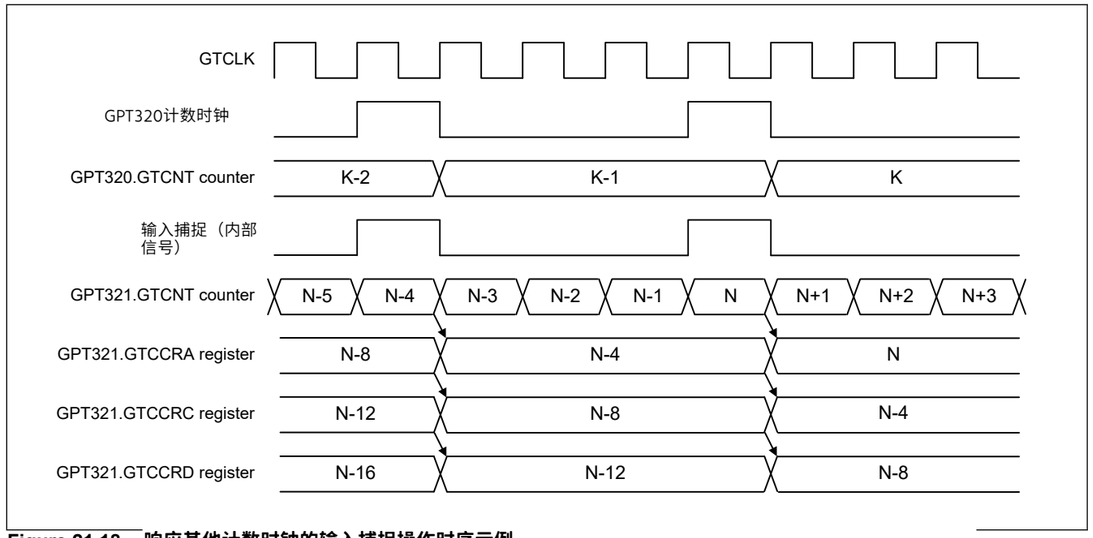


Figure 21.18 响应其他计数时钟的输入捕捉操作时序示例 Channel

21.3.2 缓冲操作

可以使用GTBER设置以下缓冲区操作：

- GTPR, GTPBR, and GTPDBR
- GTCCRA, GTCCRC, and GTCCRD
- GTCCRB, GTCCRE, and GTCCRF
- GTADTRA, GTADTBRA, and GTADTDBRA
- GTADTRB, GTADTBRB, and GTADTDBRB

通过设置GTDTCR启用以下缓冲区操作：

- GTDVU and GTDBU
- GTDVD and GTDBD

通过设置GTBER2启用以下缓冲区操作：

- ●GTCCRA、GTCCRE和GTCCRF（互补PWM模式3、4）
- ●GTOLBR.GTIOAB[4:0]位和GTIOR.GTIOA[4:0]位
- ●GTOLBR.GTIOBB[4:0]位和GTIOR.GTIOB[4:0]位

21.3.2.1 GTPR寄存器缓冲区操作

GTPBR可以作为GTPR的缓冲寄存器。

GTPDBR寄存器可以作为GTPBR寄存器的缓冲寄存器（GTPR寄存器的双缓冲寄存器）。

在互补PWM模式下，从GTPDBR寄存器到临时寄存器P的缓冲区传输仅在主通道(GPT32n)中执行。临时寄存器P传送到主通道、从通道1(GPT32n+1)和从通道2(GPT32n+2)的每个GTPBR寄存器。从GTPBR寄存器到GTPR寄存器的传输在三个通道中同时进行。因此，相同的值存储在三个通道的相同寄存器中。主通道的GTPR寄存器代表主通道的GTCNT计数器（GTCNTn）周期。在从通道中，周期由GTPR寄存器值和GTDVU寄存器值控制。

在Saw-wavePWM模式2中设置无效。

The buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count, and at a trough in triangle-wave mode.

In saw-wave mode or in event count, the buffer transfer is performed when the following counter clear operations occur during counting:

- Clear by hardware sources (the clear source is selected in GTCSR register)
- Clear by software (when GTCSR.CCLR bit is 1 and GTCLR.CCLRn bit is set to 1, n = 0 to 9).

In the case of saw waves, the buffer transfer by clearing counter can be prohibited by GTBER2.CCTPR bit.

Table 21.18 shows the buffer transfer timing in the complementary PWM mode.

Table 21.18 GTPR Buffer Transfer Timing in Complementary PWM Mode

	Complementary PWM mode 1	Complementary PWM mode 2	Complementary PWM mode 3, 4
GTPDBR ↓ Temporary register P	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)
Temporary register P ↓ GTPBR	(1) When data is transferred to temporary register P during up-counting middle section: After one GTCLK cycle from data transfer to temporary register P (2) When data is transferred to temporary register P during a section other than up-counting middle section: At the end of trough section	(1) When data is transferred to temporary register P during down-counting middle section: After one GTCLK cycle from data transfer to temporary register P (2) When data is transferred to temporary register P during a section other than down-counting middle section: At the end of crest section	(1) When data is transferred to temporary register P during middle section: After one GTCLK cycle from data transfer to temporary register P (2) When data is transferred to temporary register P during a section other than middle section: At the end of crest/ trough sections
GTPBR ↓ GTPR	At the end of crest section Synchronous clear	At the end of trough section Synchronous clear	At the end of crest section At the end of trough section Synchronous clear

To set GTPR to function as a buffer, set the GTBER.PR bit to 1. To set GTPR not to function as a buffer, set the GTBER.PR bit to 0.

To set the GTPR register to function as double buffer, set the GTBER.PR[1:0] bits to 10b or 11b. For single buffer operation, set 01b. Not to function as buffer, set 00b.

In complementary PWM mode, complementary PWM mode-specific buffer operation is performed regardless of the GTBER.PR[1:0] bit setting.

Figure 21.19 to Figure 21.24 show examples of GTPR buffer operation and Table 21.19 shows an example for setting GTPR buffer operation. For details of operation settings in complementary PWM mode, see section 21.3.3.7. Complementary PWM mode 1,2,3.

缓冲区传输在锯齿波模式或事件计数中的上溢（向上计数期间）或下溢（向下计数期间）以及三角波模式的波谷处执行。

在锯齿波模式或事件计数中，当计数期间发生以下计数器清零操作时，将执行缓冲区传输：

●通过硬件源清除（清除源在GTCSR寄存器中选择）
●软件清零（当GTCSR.CCLR位为1且GTCLR.CCLRn位设置为1时，n=0至9）。

在锯齿波的情况下，通过清除计数器进行的缓冲区传输可以通过GTBER2.CCTPR位来禁止。

表21.18显示了互补PWM模式下的缓冲区传输时序。

Table 21.18 互补PWM模式下的GTPR缓冲区传输时序

	互补PWM模式1	互补PWM模式2	互补PWM模式3，4
GTPDBR ↓临时寄存器P	从一个GTCLK周期后 从通道2(GPT32n+2)的GTCCRD寄存器写入	从一个GTCLK周期后 从通道2(GPT32n+2)的GTCCRD寄存器写入	从一个GTCLK周期后 从通道2(GPT32n+2)的GTCCRD寄存器写入
临时登记册P ↓ GTPBR	(1)在递增计数中间段中向临时寄存器P传输数据时：从数据传输到临时寄存器P的一个GTCLK周期后(2)在递增计数中间段以外的段中向临时寄存器P传输数据时：At槽段的末端	(1)在递减计数中段期间将数据传输到临时寄存器P时：从数据传输到临时寄存器P的一个GTCLK周期后(2)当在递减中间段以外的段期间将数据传输到临时寄存器P时：在波峰部分的末端	(1)在中间部分将数据传输到临时寄存器P时：从数据传输到临时寄存器P的一个GTCLK周期后(2)在中间部分以外的部分将数据传输到临时寄存器P时：波峰结束时槽段
GTPBR ↓ GTPR	在波峰段的末端 同步清零	在槽段的末端 同步清零	在波峰段的末端 在槽段的末端 同步清零

要将GTPR设置为缓冲区，请将GTBER.PR位设置为1。要将GTPR设置为不作为缓冲区，请将GTBER.PR位设置为0。

要将GTPR寄存器设置为双缓冲器，请将GTBER.PR[1:0]位设置为10b或11b。对于单缓冲操作，设置01b。不用作缓冲器，设置为00b。

在互补PWM模式下，会执行互补PWM模式特定的缓冲器操作，而不管GTBER.PR[1:0]位设置。

图21.19至图21.24显示了GTPR缓冲区操作的示例，表21.19显示了设置GTPR缓冲区操作的示例。有关互补PWM模式下的操作设置的详细信息，请参阅第21.3.3.7节。互补PWM模式1 2 3。

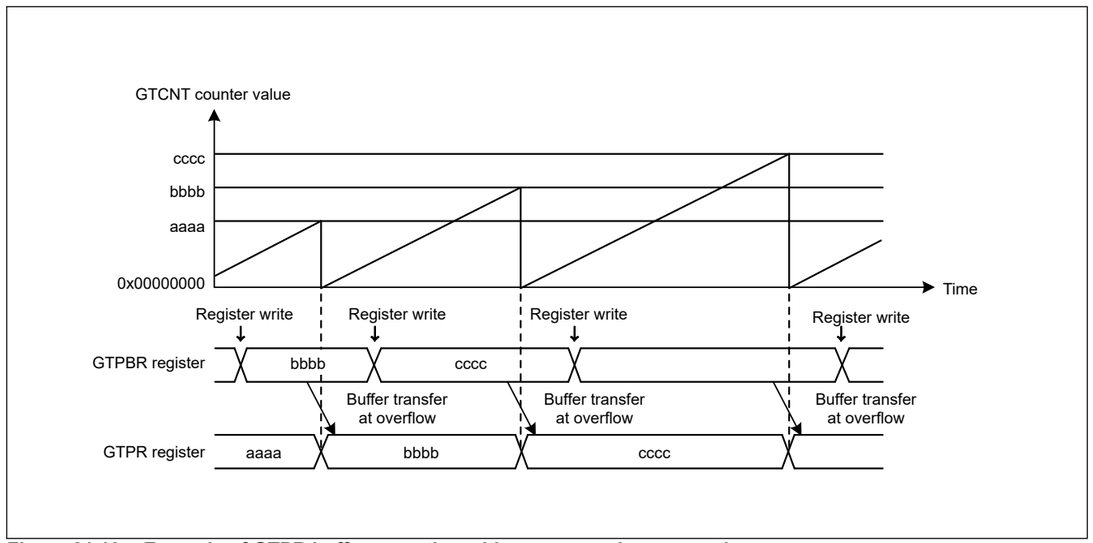


Figure 21.19 Example of GTPR buffer operation with saw waves in up-counting

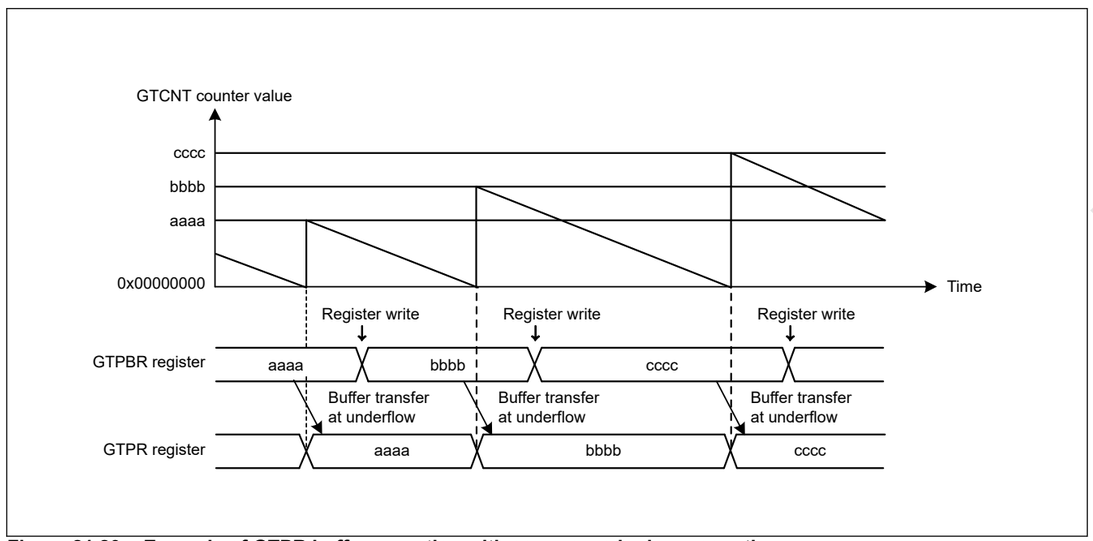


Figure 21.20 Example of GTPR buffer operation with saw waves in down-counting

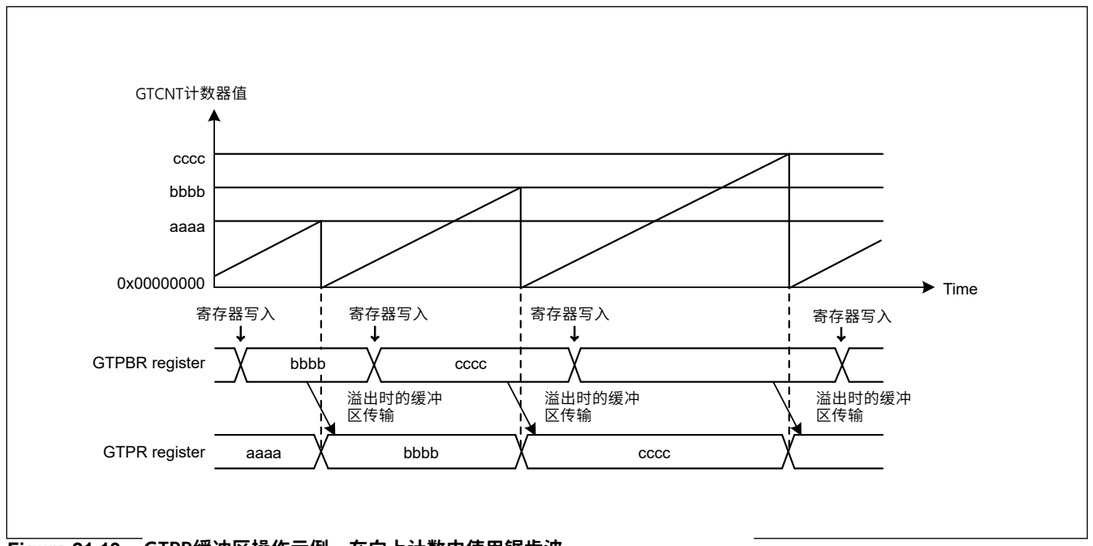


Figure 21.19 GTPR缓冲区操作示例，在向上计数中使用锯齿波

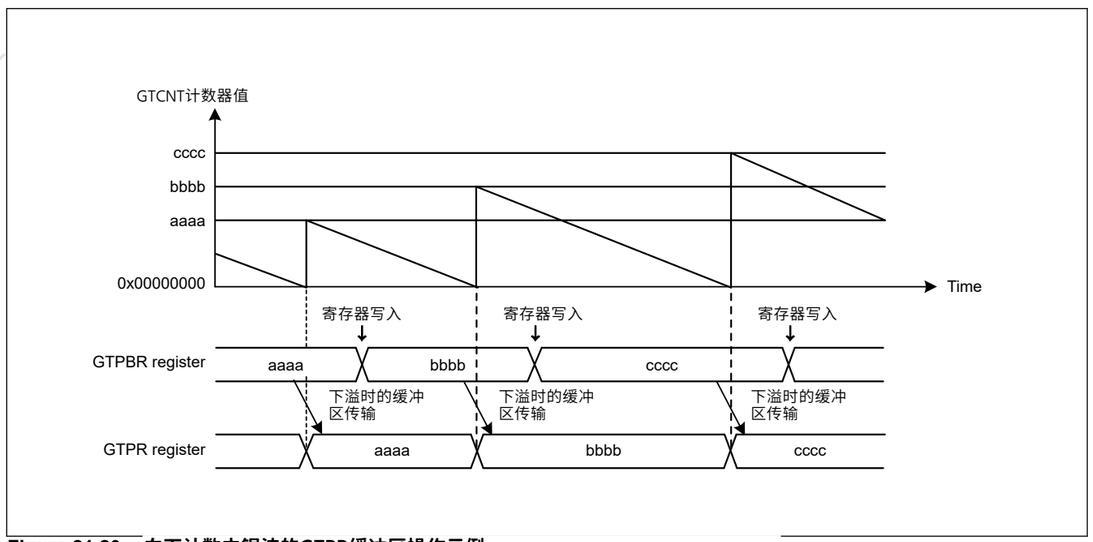


Figure 21.20 向下计数中锯波的GTPR缓冲区操作示例

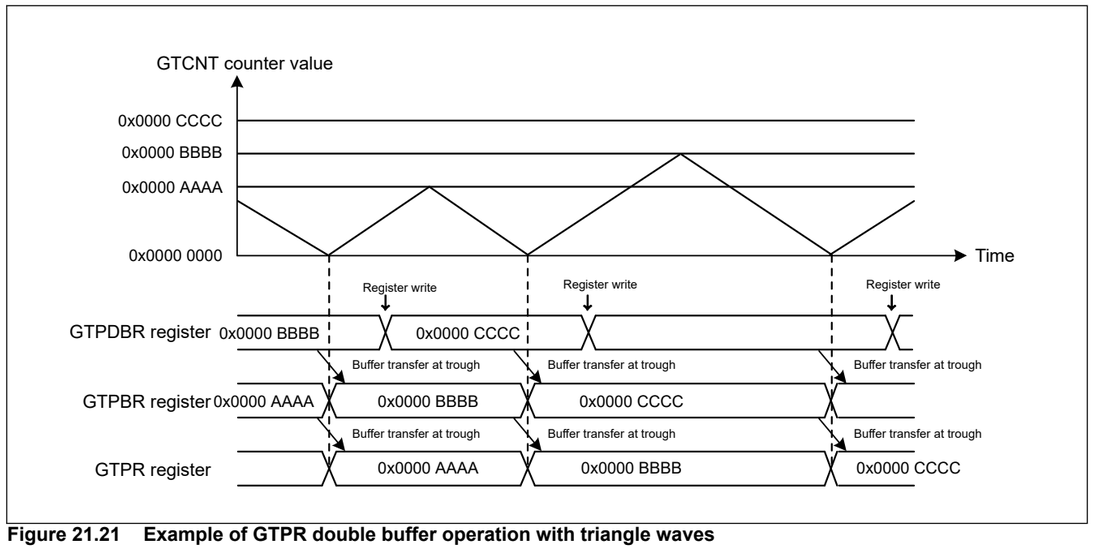


Figure 21.21 Example of GTPR double buffer operation with triangle waves

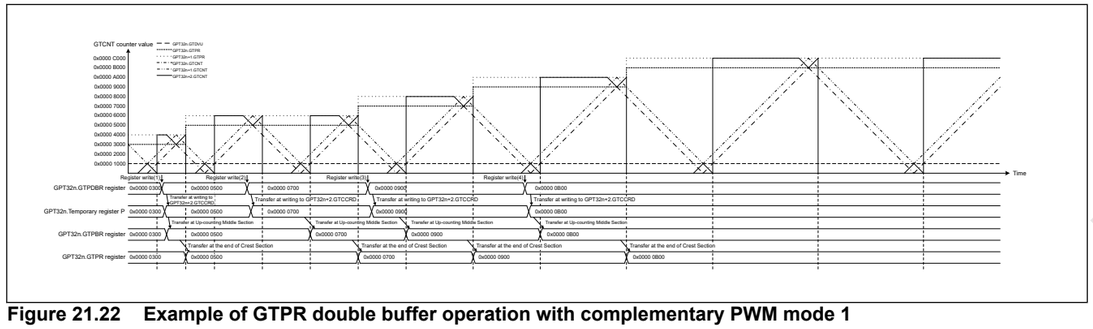


Figure 21.22 Example of GTPR double buffer operation with complementary PWM mode 1

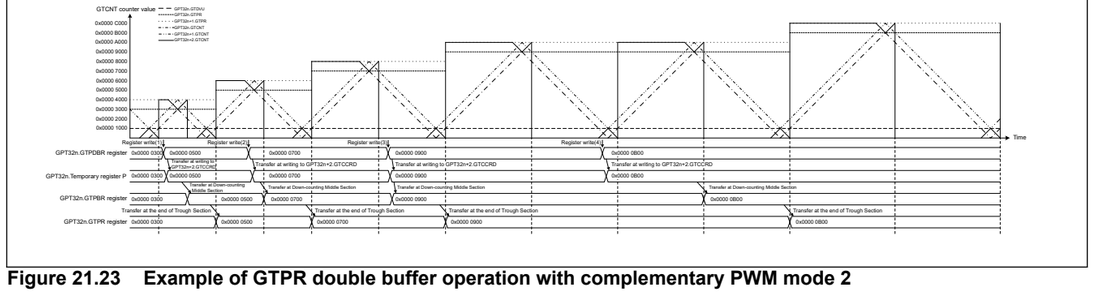


Figure 21.23 Example of GTPR double buffer operation with complementary PWM mode 2

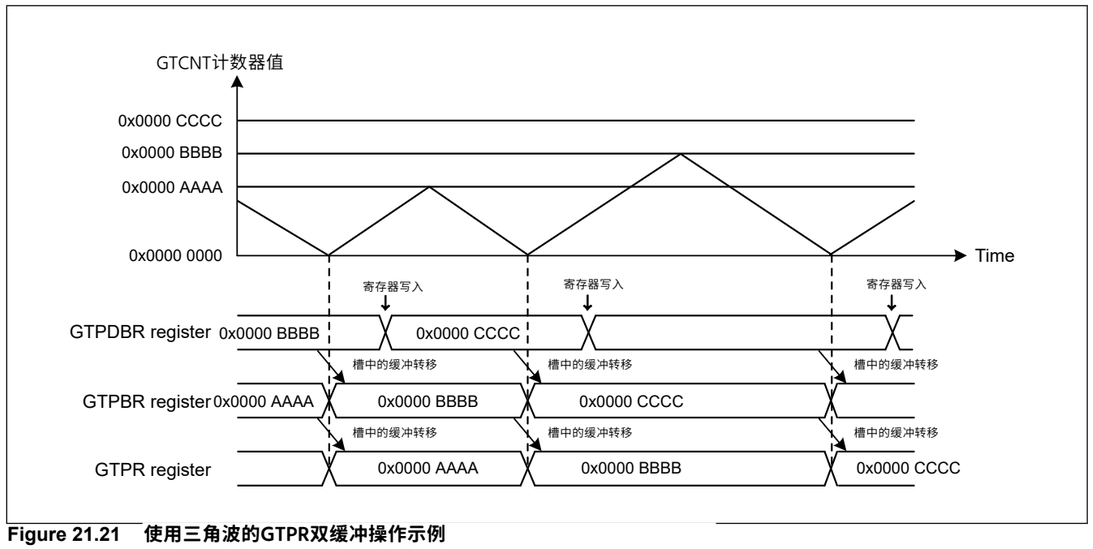


Figure 21.21 使用三角波的GTPR双缓冲操作示例

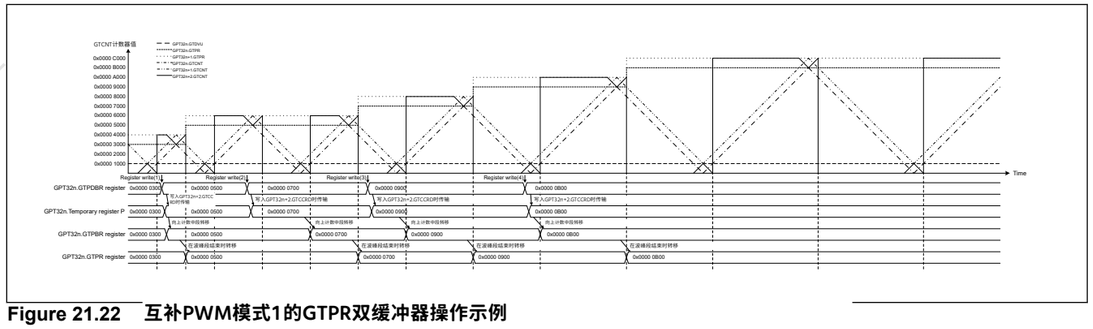


Figure 21.22 互补PWM模式1的GTPR双缓冲器操作示例

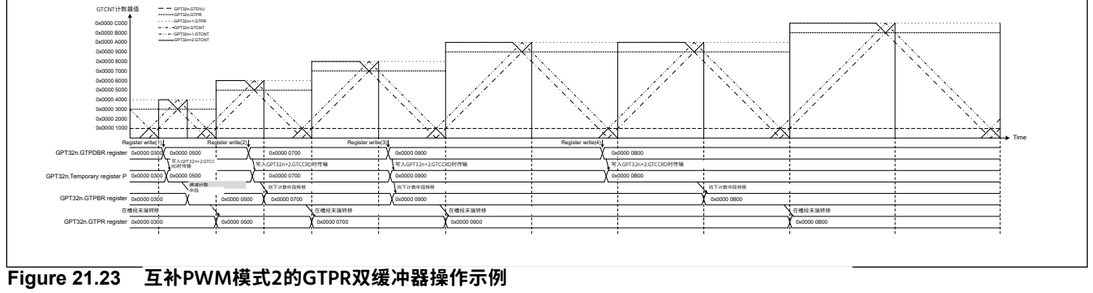


Figure 21.23 互补PWM模式2的GTPR双缓冲器操作示例

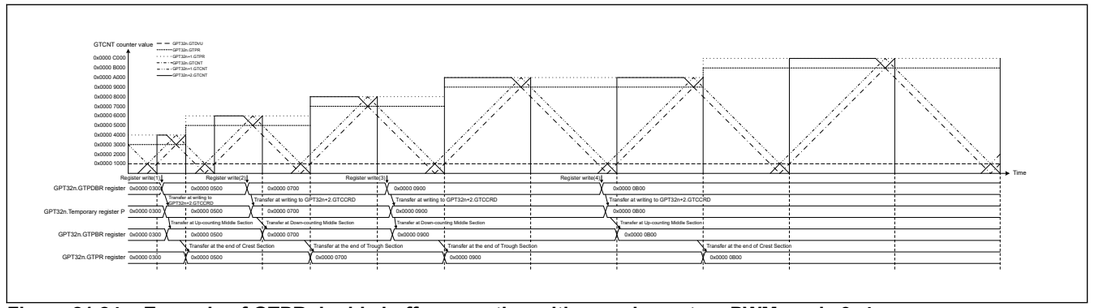


Figure 21.24 Example of GTPR double buffer operation with complementary PWM mode 3, 4

Table 21.19 Example for setting GTPR register buffer operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.19 and Figure 21.20, 000b or 0000b (saw-wave PWM mode 1) is set, and in Figure 21.21, 100b or 0100b (triangle-wave PWM mode 1) is set. In Figure 21.22 to Figure 21.24, 11xxb (complementary PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.19, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting). In Figure 21.20, after 10b is set in the GTUDDTYC[1:0] bits, 00b is set in the GTUDDTYC[1:0] bits (down-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set buffer operation	Set buffer operation with the GTBER.PR[1:0] bits. In Figure 21.19 and Figure 21.20, PR[1:0] = 01b. In Figure 21.21, PR[1:0] = 1xb. In Figure 21.22 to Figure 21.24, no PR[1:0] bits setting required.
7	Set buffer value	For buffer operation, set a value in one cycle after the current cycle in the GTPBR register. For double buffer operation, also set a value of the period for the cycle after the next cycle in the GTPDBR register.
8	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
9	Set buffer value for each cycle	For buffer operation, set a value in one cycle after the current cycle in the GTPBR register. For double buffer operation, also set a value of the period for the cycle after the next cycle in the GTPDBR register. In complementary PWM mode 1 (crest transfer), when the GTPDBR register is set in the up-counting trough or middle section, a value of the period for the next cycle is set. In other sections, a value of the period for the cycle after the next cycle is set. In complementary PWM mode 2 (trough transfer), when the GTPDBR register is set in the up-counting sect ion or the down-counting crest or middle sections, a value of the period for the next cycle is set. In other sections, a value of the period for the cycle after the next cycle is set. In complementary PWM mode 3 or 4 (crest/trough immediate transfer), when the GTPDBR register is set in a section other than the down-counting trough section, a value of the period for the next cycle is set. In the down-counting trough section, a value of the period for the cycle after the next cycle is set.

21.3.2.2 Buffer Operation for GTCCRA and GTCCRB Registers

GTCCRC can function as the GTCCRA buffer register and GTCCRD can function as the GTCCRC buffer register (double-buffer register for GTCCRA). Similarly, GTCCRE can function as the GTCCRB buffer register and GTCCRF can function as the GTCCRE buffer register (double-buffer register for GTCCRB).

To set GTCCRA or GTCCRB to function as a double buffer, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 10b or 11b. For single buffer operation, set 01b. To set GTCCRA or GTCCRB to not function as a buffer, set 00b.

In saw-wave one-shot pulse mode, triangle-wave PWM mode 3, complementary PWM mode, the buffer operations that specific each PWM output operation mode are performed regardless of the setting of GTBER.CCRA [1:0] bits and GTBER.CCRB [1:0] bits.

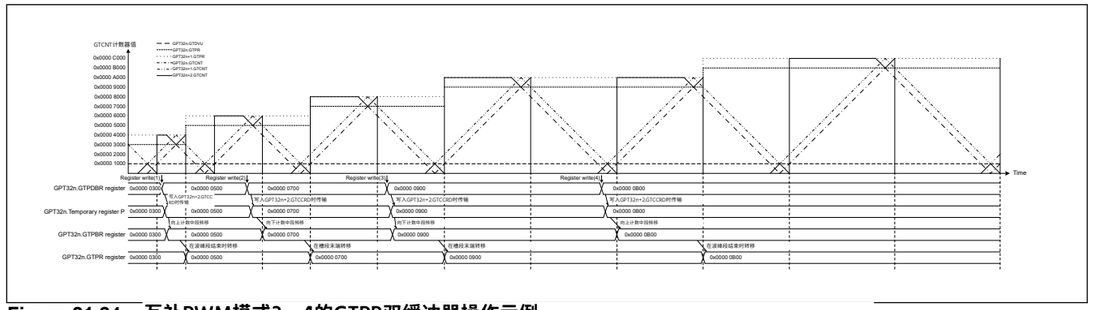


Figure 21.24 互补PWM模式3、4的GTPR双缓冲器操作示例

Table 21.19 设置GTPR寄存器缓冲操作示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.19和图21.20中，设置了000b或0000b（锯齿波PWM模式1），在图21.21中，设置了100b或0100b（三角波PWM模式1）。在图21.22至图21.24中，设置了11xxb（互补PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.19中，在GTUDDTYC[1:0]位中设置11b后，在GTUDDTYC[1:0]位中设置01b（向上计数）。 在图21.20中，在GTUDDTYC[1:0]位中设置10b后，在GTUDDTYC[1:0]位中设置00b（向下计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	在GTPR寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置缓冲操作	使用GTBER.PR[1:0]位设置缓冲区操作。在图21.19和图21.20中，PR[1:0]=01b。在图21.21中，PR[1:0]=1xb。在图21.22到图21.24中，不需要设置PR[1:0]位。
7	设置缓冲区值	对于缓冲操作，在GTPBR寄存器中的当前周期之后的一个周期内设置一个值。 对于双缓冲操作，还要设置一个周期值，用于在下一个周期之后的周期 GTPDBR register.
8	开始计数操作	将GTCR.CST位设置为1以启动计数操作。
9	为每个周期设置缓冲区值	对于缓冲操作，在GTPBR寄存器中的当前周期之后的一个周期内设置一个值。 对于双缓冲操作，还要设置一个周期值，用于在下一个周期之后的周期 GTPDBR register. 在互补PWM模式1（峰值传输）中，当GTPDBR寄存器设置在向上计数波谷或中间部分时，设置下一个周期的周期值。在其他部分中，设置下一周期之后的周期的周期值。在互补PWM模式2（通过传输）中，当GTPDBR寄存器设置在向上计数部分或向下计数峰值或中间部分时，设置下一个周期的周期值。在其他部分中，设置下一周期之后的周期的周期值。在互补PWM模式3或4（波峰波谷立即传输）中，当GTPDBR寄存器设置在向下计数波谷部分以外的部分时，将设置下一个周期的周期值。在向下计数谷部分中，设置下一周期之后的周期的周期值。

21.3.2.2 GTCCRA和GTCCRB寄存器的缓冲操作

GTCCRC可以作为GTCCRA缓冲寄存器，GTCCRD可以作为GTCCRC缓冲寄存器（GTCCRA的双缓冲寄存器）。同样，GTCCRE可以作为GTCCRB缓冲寄存器，GTCCRF可以作为GTCCRE缓冲寄存器（GTCCRB的双缓冲寄存器）。

要将GTCCRA或GTCCRB设置为双缓冲区，请将GTBER.CCRA[1:0]或GTBER.CCRB[1:0]设置为10b或11b。
对于单缓冲操作，设置01b。要将GTCCRA或GTCCRB设置为不用作缓冲区，请设置00b。

在锯齿波单发脉冲模式、三角波PWM模式3、互补PWM模式下，无论GTBER.CCRA[1:0]位和GTBER的设置如何，都会执行特定于每个PWM输出操作模式的缓冲操作。CCRB[1:0]位。

(1) When GTCCRA or GTCCRB Functions as Output Compare Register

In saw-wave one-shot pulse mode, triangle-wave PWM mode 3, complementary PWM mode, the buffer operations that specific each PWM output operation mode are performed regardless of the setting of GTBER.CCRA [1:0] bits and GTBER.CCRB [1:0] bits. For details, see section 21.3.3. PWM Output Operating Mode. Other than above PWM output operation mode, Buffer transfer occurs in the following situations:

- Buffer transfer by overflow or underflow
  Buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count operation. In triangle-wave mode, buffer transfer is performed at a trough (triangle-wave PWM mode 1) or a crest and trough (triangle-wave PWM mode 2).
- Buffer transfer by counter clear
  In saw-wave mode or in event count operation, during counting, buffer transfer (which is the same as an overflow during up-counting or an underflow during down-counting) is performed by the counter clear sources similar to the case shown in section 21.3.2.1. GTPR Register Buffer Operation.
  In saw-wave, the buffer transfer of GTCCRm register by counter clearing is possible to be disabled with GTBER2.CCTCm bit (m = A, B).
  In triangle-wave mode, buffer transfer is not performed by the counter clear.
- Buffer transfer by compare match
  In saw-wave, the buffer transfer by the compare match of GTCCRm register enabled by GTBER2.CMTCm (m = A, B) bit is performed.
- Forcible buffer transfer
  When GTBER.CCRSWT bit is set to 1 while the count operation is stopped, the GTCCRA and the GTCCRB register buffer transfer are performed forcibly in saw-wave mode, in event count operation and in triangle-wave mode. Additionally buffer transfer from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B are performed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3.

When the setting of the GTBER.DBRTECm (m = A, B) bit is 1 in saw-wave one-shot pulse mode or triangle-wave PWM mode 3, transfer from the intermediate buffers to the GTCCRm (m = A, B) registers is repeated on a cyclic basis even while buffer transfer is disabled by the setting of the GTBER.BD[0] bit or buffer transfer extended skipping function (function for repeated double-buffer operation while buffer transfer is disabled). For details, refer to section 21.8.2.2. Repeated Double-Buffered Operation When Disabling GTCCR Buffer Transfer.

Figure 21.25 to Figure 21.28 show examples of GTCCRA and GTCCRB buffer operation and Table 21.20 shows an example for setting GTCCRA and GTCCRB buffer operation.

(1) 当GTCCRA或GTCCRB用作输出比较寄存器时

在锯齿波单发脉冲模式、三角波PWM模式3、互补PWM模式下，无论GTBER.CCRA[1:0]位和GTBER的设置如何，都会执行特定于每个PWM输出操作模式的缓冲操作。CCRB[1:0]位。详见21.3.3节。PWM输出工作模式。除上述PWM输出操作模式外，缓冲区传输发生在以下情况：

●上溢或下溢的缓冲区传输
在锯齿波模式或事件计数操作中，在溢出（向上计数期间）或下溢（向下计数期间）时执行缓冲区传输。在三角波模式中，缓冲区传输在波谷（三角波PWM模式1）或波峰和波谷（三角波PWM模式2）处执行。

●通过计数器清除缓冲区传输
在锯齿波模式或事件计数操作中，在计数期间，缓冲区传输（与向上计数期间的溢出或向下计数期间的下溢相同）由计数器清零源执行，类似于章节中所示的情况21.3.2.1。GTPR寄存器缓冲区操作。在锯齿波中，通过计数器清除对GTCCRm寄存器的缓冲区传输可以禁用

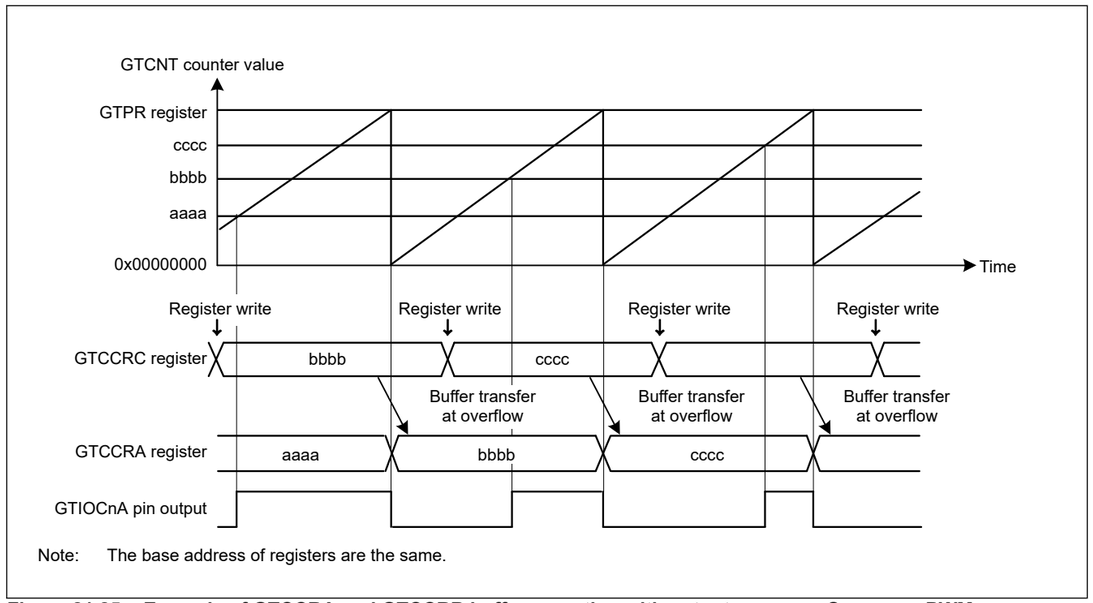
GTBER2.CCTCm bit (m = A, B).
在三角波模式下，计数器清零不执行缓冲区传输。

●通过比较匹配传输缓冲区
在锯齿波中，通过GTBER2.CMTCm(m=A B)位启用的GTCCRm寄存器的比较匹配来执行缓冲区传输。

●强制缓冲转移
当GTBER.CCRSWT位在计数操作停止时设置为1时，在锯齿波模式、事件计数操作和三角波模式下强制执行GTCCRA和GTCCRB寄存器缓冲传输。此外，从GTCCRD寄存器到临时寄存器A以及从GTCCRF寄存器到临时寄存器B的缓冲区传输是在锯齿波一次性脉冲模式或三角波PWM模式3中执行的。

当GTBER.DBRTECm(m=A B)位在锯齿波单发脉冲模式或三角波PWM模式3中设置为1时，从中间缓冲器传输到GTCCRm(m=A B)即使通过设置GTBER.BD[0]位或缓冲区传输扩展跳过功能（在缓冲区传输被禁用时重复双缓冲区操作的功能）禁用缓冲区传输，寄存器也会循环重复。有关详细信息，请参阅第21.8.2.2节。禁用GTCCR缓冲区传输时重复双缓冲操作。

图21.25至图21.28显示了GTCCRA和GTCCRB缓冲操作的示例，表21.20显示了设置GTCCRA和GTCCRB缓冲操作的示例。



Note: The base address of registers are the same.

Figure 21.25 Example of GTCCRA and GTCCRB buffer operation with output compare, Saw-wave PWM mode 1 in up- counting, high output at GTCCRA compare match, and low output at cycle end

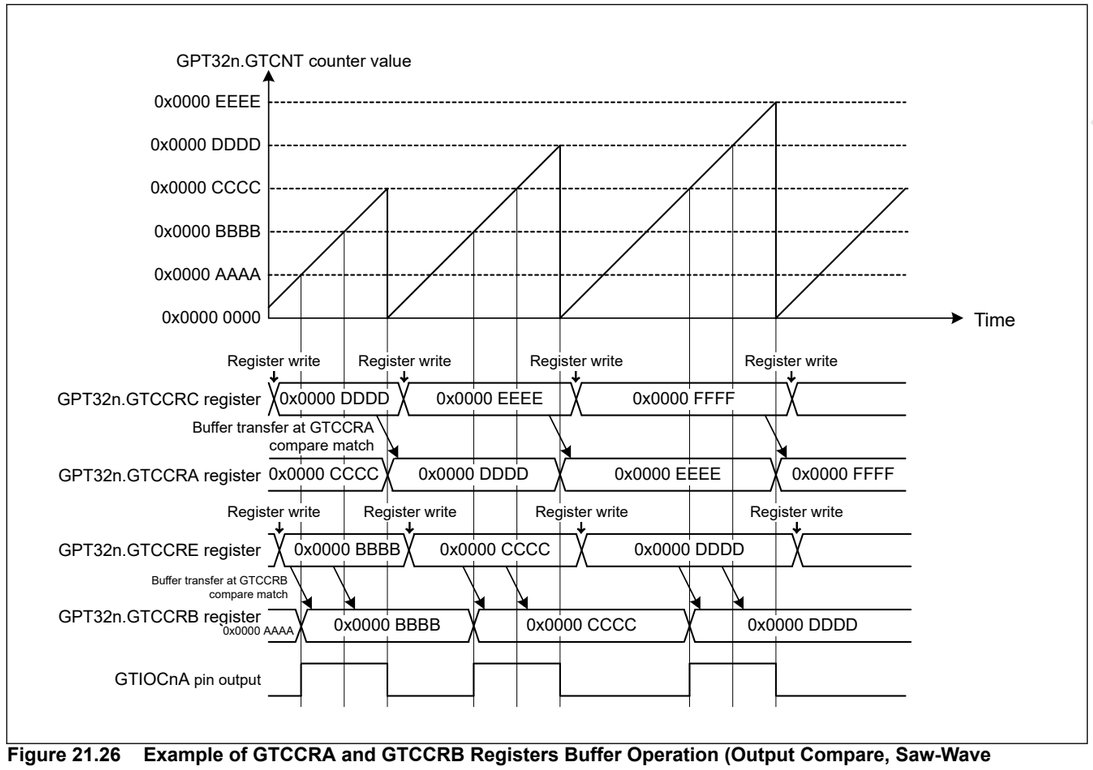
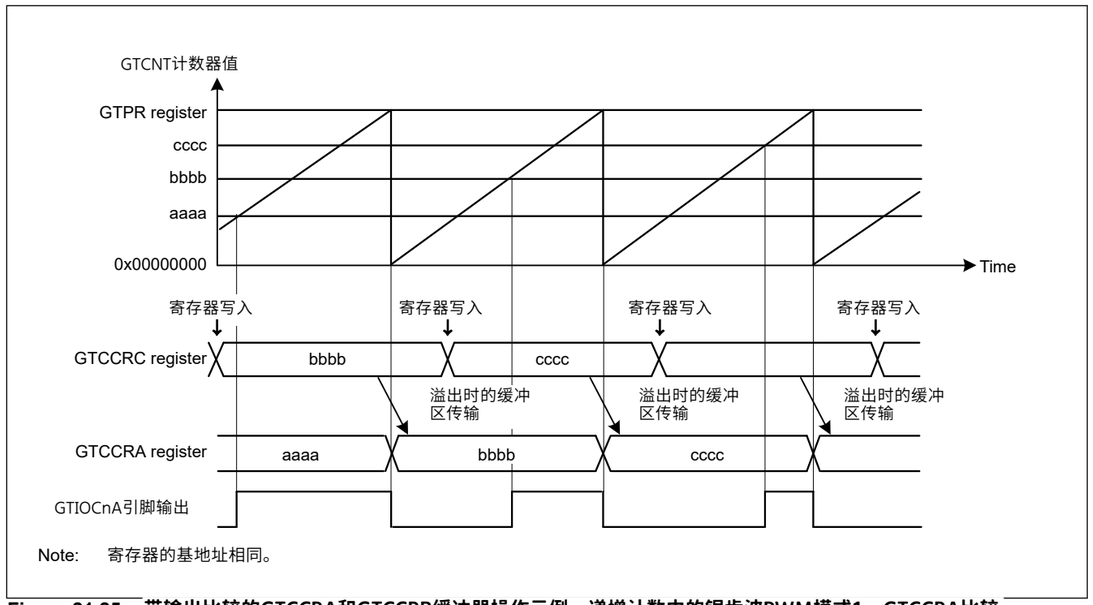


Figure 21.26 Example of GTCCRA and GTCCRB Registers Buffer Operation (Output Compare, Saw-Wave PWM Mode 2, Buffer Transfer at GTCCRA Register Compare Match, Counter Clearing, Low Output, Buffer Transfer at GTCCRB Register Compare Match, High Output) (n = 4 to 9)



Note: 寄存器的基地址相同。

Figure 21.25 带输出比较的GTCCRA和GTCCRB缓冲器操作示例，递增计数中的锯齿波PWM模式1，GTCCRA比较匹配时的高输出和周期结束时的低输出

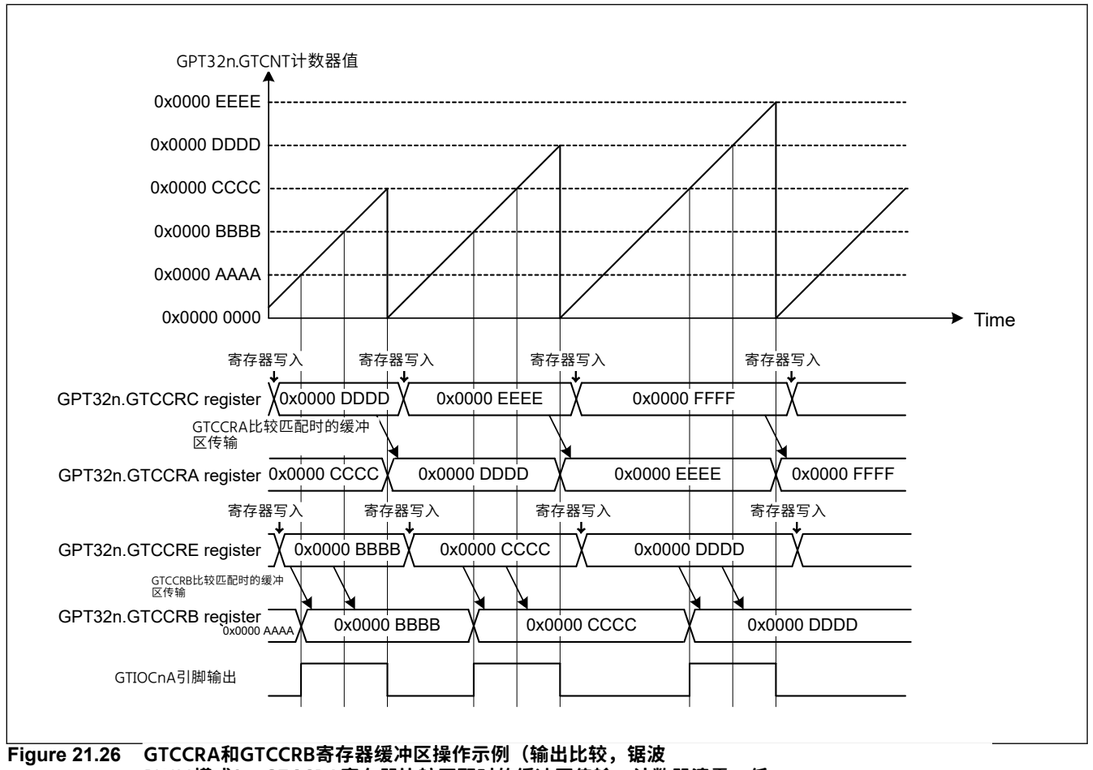


Figure 21.26 GTCCRA和GTCCRB寄存器缓冲区操作示例（输出比较，锯波PWM模式2，GTCCRA寄存器比较匹配时的缓冲区传输，计数器清零，低输出，GTCCRB寄存器比较匹配时的缓冲区传输，高输出）（n=4到9）

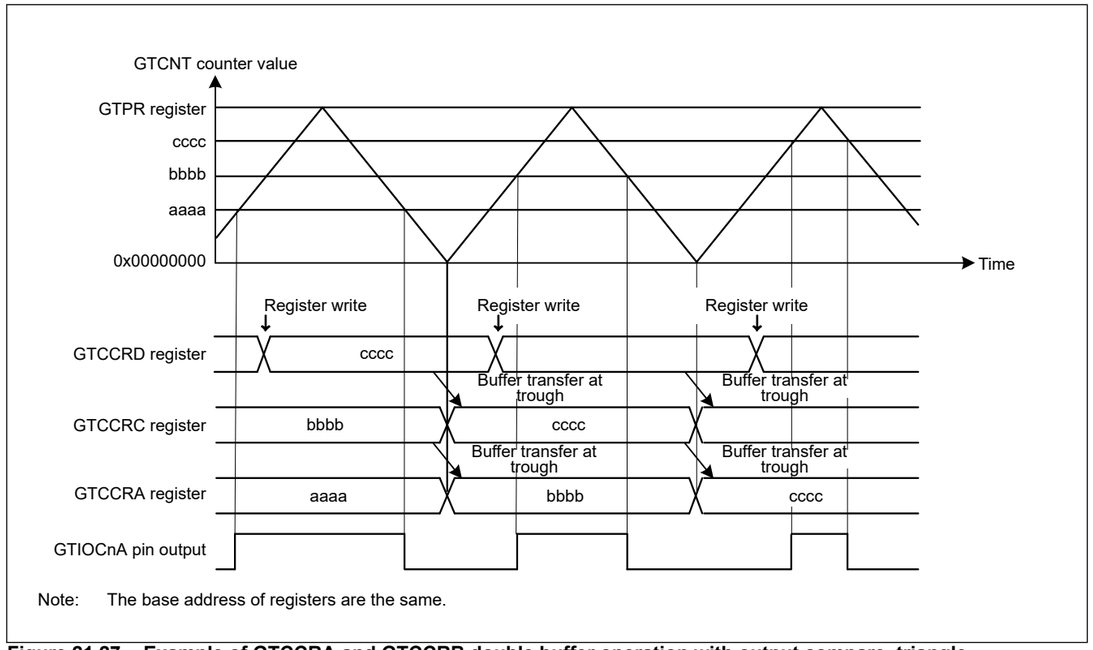


Figure 21.27 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at trough, output toggled at GTCCRA compare match, and output retained at cycle end

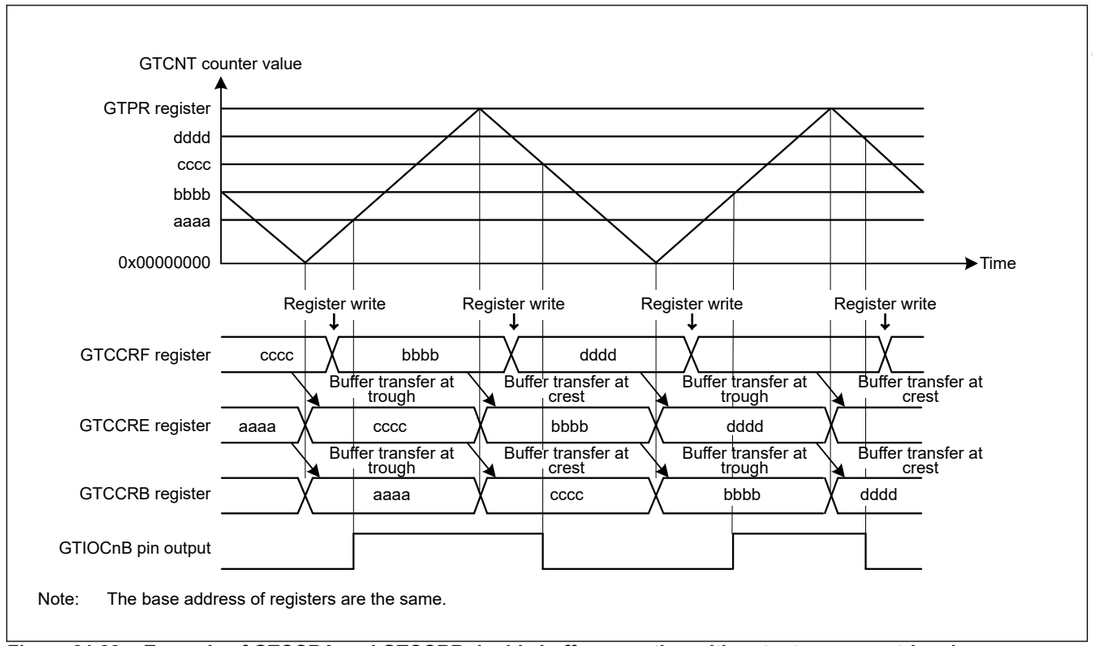


Figure 21.28 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at both troughs and crests, output toggled at GTCCRB compare match, and output retained at cycle end

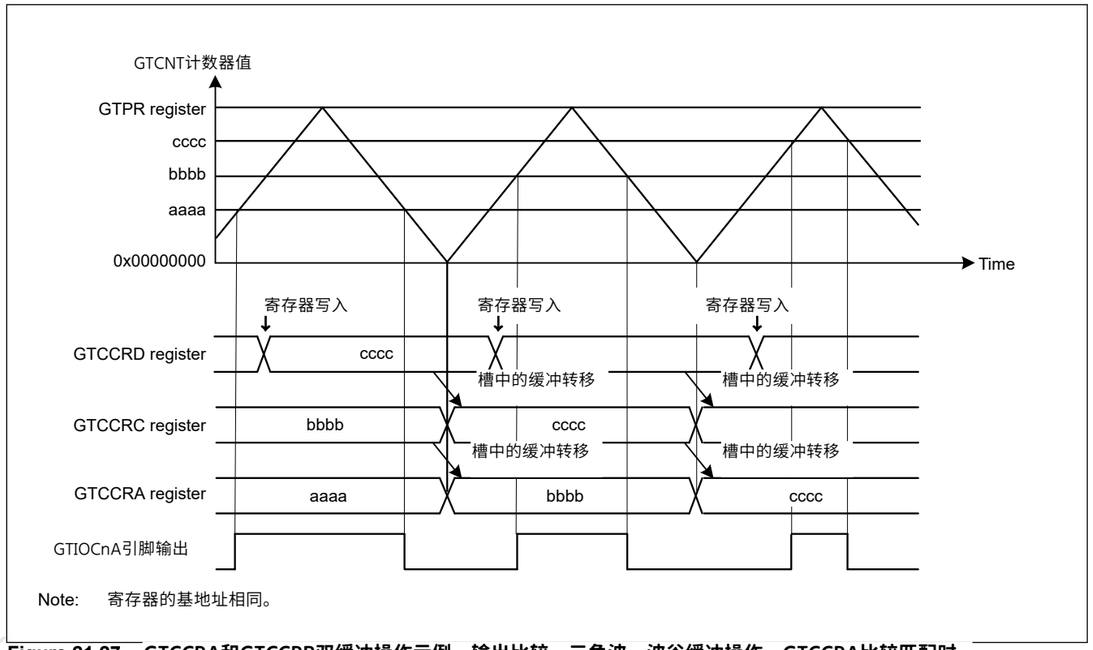


Figure 21.27 GTCCRA和GTCCRB双缓冲操作示例，输出比较、三角波、波谷缓冲操作、GTCCRA比较匹配时切换输出、循环结束时保留输出

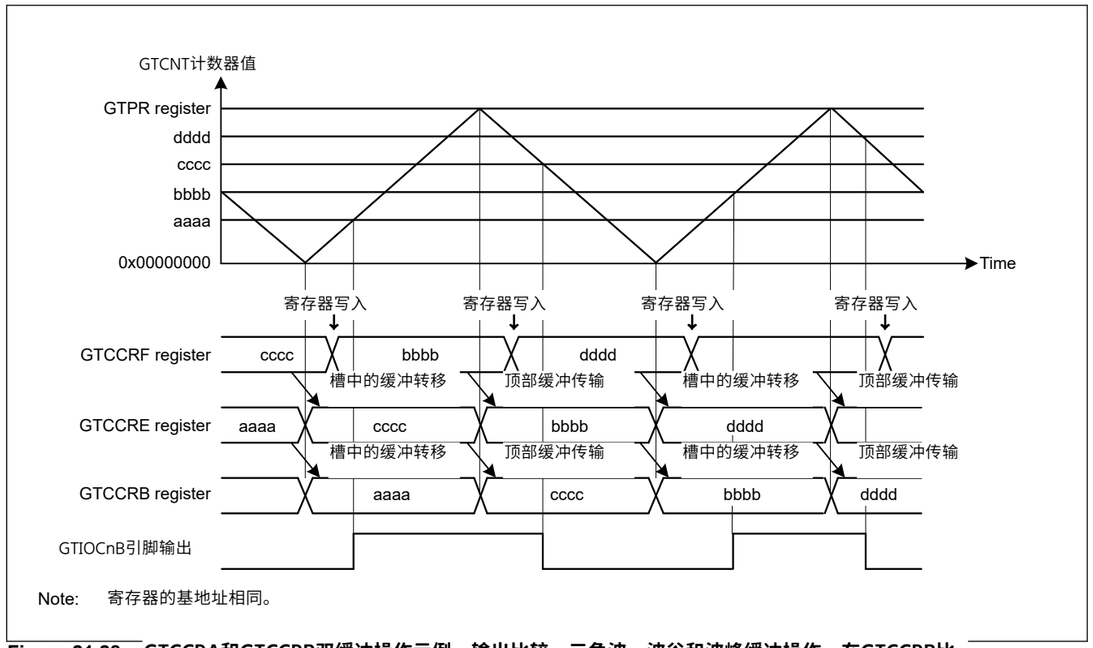


Figure 21.28 GTCCRA和GTCCRB双缓冲操作示例，输出比较、三角波、波谷和波峰缓冲操作、在GTCCRB比较匹配时切换输出以及在周期结束时保留输出

Table 21.20 Example for setting GTCCRA and GTCCRB buffer operation for output compare

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.25, 000b or 0000b (saw-wave PWM mode 1) is set, in Figure 21.26, 0010b (saw-wave PWM mode 2) is set, in Figure 21.27, 100b or 0100b (triangle-wave PWM mode 1) is set, and in Figure 21.28, 101b or 0101b (triangle-wave PWM mode 2) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.25, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode2, set the cycle in the GTPR register. In the saw-wave PWM mode2, select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 21.25, GTIOA[4:0] = 00110b, in Figure 21.26, GTIOA[4:0] = 00101b and GTIOB[1:0] = 10b, in Figure 21.27, GTIOA[4:0] = 00011b, and in Figure 21.28, GTIOB[4:0] = 00011b.
7	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set buffer operation	Set buffer operation with the CCRA[1:0] and CCRB[1:0] bits in the GTBER register. In Figure 21.25, CCRA[1:0] = 01b, in Figure 21.26, CCRA[1:0] = 01b and CCRB[1:0] = 01b, in Figure 21.27, CCRA[1:0] = 1xb, and in Figure 21.28, CCRB[1:0] = 1xb.
9	Set compare match value*1	Set the GTIOCnA pin transition in the GTCCRA register and the GTIOCnB pin transition in the GTCCRB register.
10	Set buffer value	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or 1 cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTCCRD and GTCCRF registers, respectively.
11	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
12	Set buffer value for each cycle	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or 1 cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTCCRD and GTCCRF registers, respectively.

Note: n: 0 to 9
m: A, B
Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnm pin output enable and setting for a compare match value.

(2) When GTCCRA or GTCCRB Functions as Input Capture Register

When an input capture is generated, the GTCNT counter value is transferred to GTCCRA and GTCCRB and the stored GTCCRA and GTCCRB register values are transferred to the buffer registers. In input capture operation, the buffer transfer is not performed by the counter clear.

Figure 21.29 and Figure 21.30 show examples of GTCCRA and GTCCRB buffer operation and Table 21.21 shows an example for setting GTCCRA and GTCCRB buffer operation.

Table 21.20 为输出比较设置GTCCRA和GTCCRB缓冲操作的示例

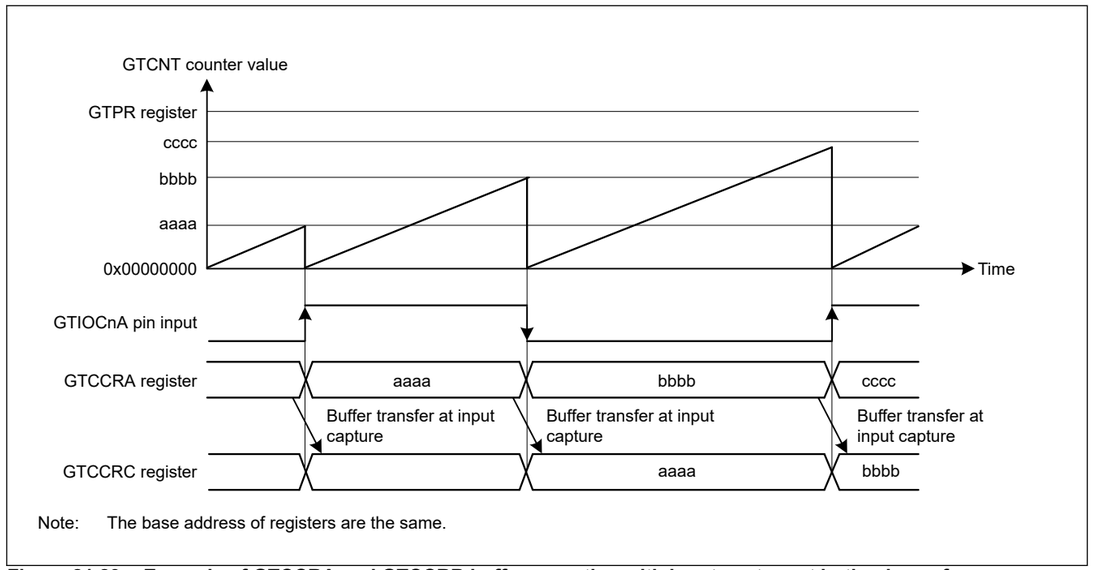
No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.25中，设置了000b或0000b（锯齿波PWM模式1），在图21.26中，设置了0010b（锯齿波设置PWM模式2），在图21.27中，设置100b或0100b（三角波PWM模式1），并在 图21.28 101b或0101b(三角波PWM模式2)被设置。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.25中，在GTUDDTYC[1:0]位中设置了11b之后，在GTUDDTYC[1:0]位中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	除了锯齿波PWM模式2，在GTPR寄存器中设置周期。 在锯齿波PWM模式2中，通过GTCSR.CSCMSC[2:0]位选择计数器清零源比较匹配寄存器GTCCRx（x=A到F）并在该寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR寄存器中的GTIOA[4:0]和GTIOB[4:0]位设置GTIOCnm引脚功能。 在图21.25中，GTIOA[4:0]=00110b，在图21.26中，GTIOA[4:0]=00101b和GTIOB[1:0]=10b，在图21.27中，GTIOA[4:0]=00011b，在图21.28，GTIOB[4:0]=00011b。
7	启用GTIOCnm引脚输出*1	通过GTIOR寄存器中的OAE和OBE位设置使能GTIOCnm引脚输出。
8	设置缓冲操作	使用GTBER寄存器中的CCRA[1:0]和CCRB[1:0]位设置缓冲区操作。 在图21.25中，CCRA[1:0]=01b，在图21.26中，CCRA[1:0]=01b和CCRB[1:0]=01b，在 在图21.27中，CCRA[1:0]=1xb，在图21.28中，CCRB[1:0]=1xb。
9	设置比较匹配值*1	设置GTCCRA寄存器中的GTIOCnA引脚转换和GTIOCnB引脚转换 GTCCRB register.
10	设置缓冲区值	对于缓冲操作，将GTIOCnA和GTIOCnB引脚设置为在当前周期后1个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的半个周期（在三角波模式GTCCRC和GTCCRE寄存器中的缓冲区传输）分别。 对于双缓冲器操作，还设置GTIOCnA和GTIOCnB引脚在当前周期后的2个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的1个周期（在三角形-GTCCRD和GTCCRF寄存器中的波形模式，在波谷和波峰都有缓冲传输）。
11	开始计数操作	将GTCR.CST位设置为1以启动计数操作。
12	为每个周期设置缓冲区值	对于缓冲操作，将GTIOCnA和GTIOCnB引脚设置为在当前周期后1个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的半个周期（在三角波模式GTCCRC和GTCCRE寄存器中的缓冲区传输）分别。 对于双缓冲器操作，还设置GTIOCnA和GTIOCnB引脚在当前周期后的2个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的1个周期（在三角形-GTCCRD和GTCCRF寄存器中的波形模式，在波谷和波峰都有缓冲传输）。

Note: n: 0 to 9
m: A, B
注1.使用PWM延迟产生电路时，更改GTIOCnm引脚输出使能设置和比较匹配值设置的顺序。

(2) 当GTCCRA或GTCCRB用作输入捕捉寄存器时

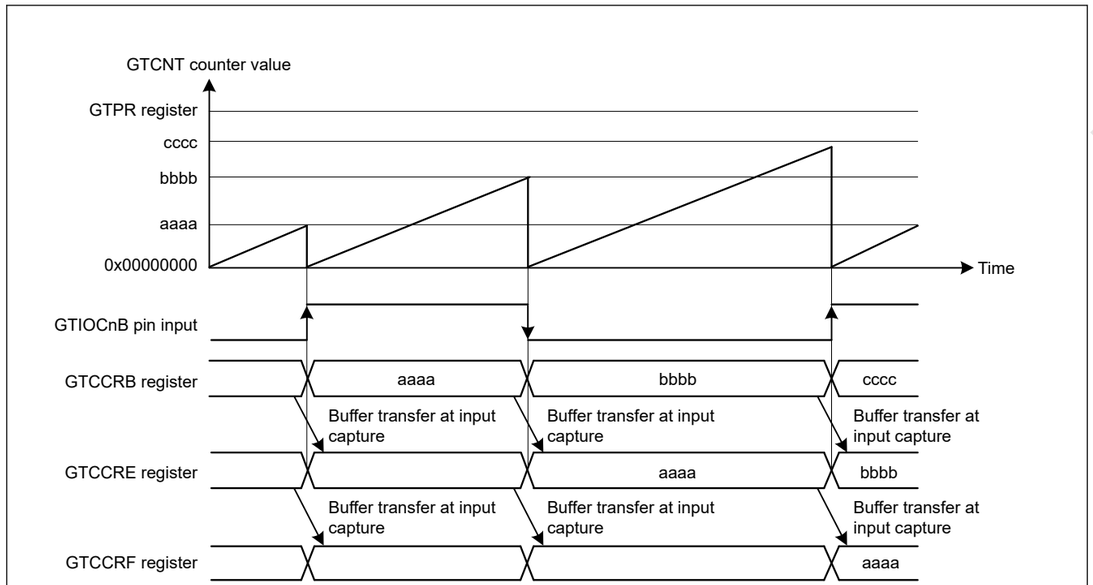
当产生输入捕捉时，GTCNT计数器值被传送到GTCCRA和GTCCRB并存储
GTCCRA和GTCCRB寄存器值被传送到缓冲寄存器。在输入捕捉操作中，缓冲区传输不是由计数器清零来执行的。

图21.29和图21.30显示了GTCCRA和GTCCRB缓冲操作的示例，表21.21显示了设置GTCCRA和GTCCRB缓冲操作的示例。



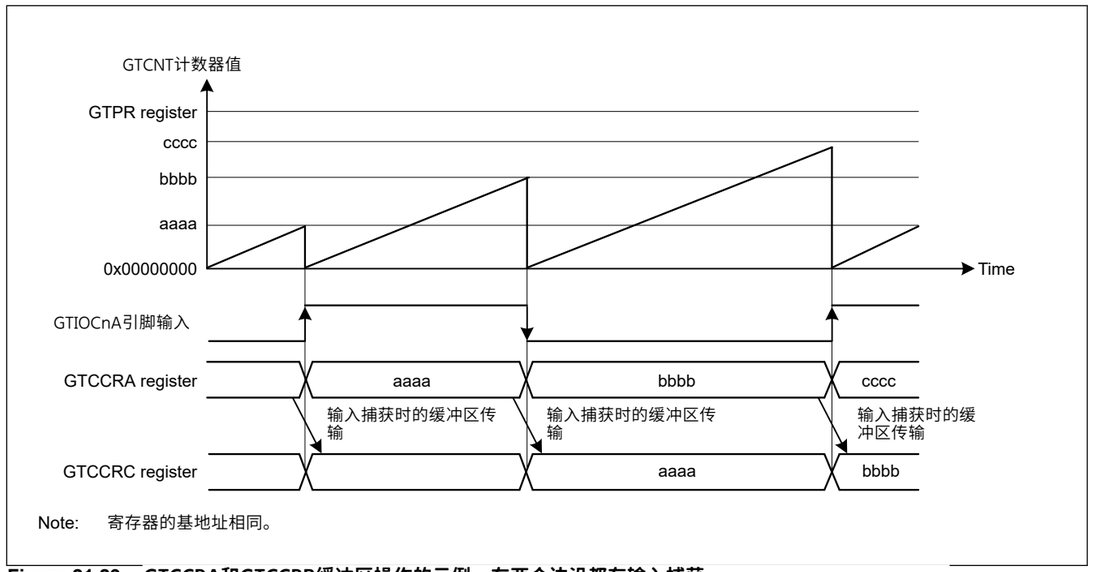
Note: The base address of registers are the same.

Figure 21.29 Example of GTCCRA and GTCCRB buffer operation with input capture at both edges of GTIOCnA input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOCnA input



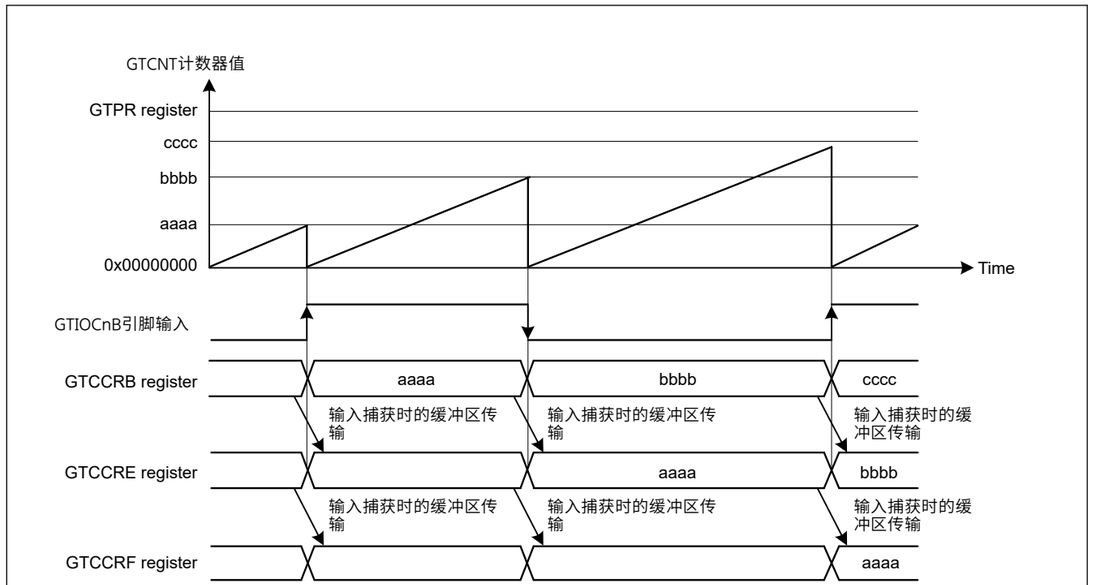
Note: The base address of registers are the same.

Figure 21.30 Example of GTCCRA and GTCCRB double buffer operation with input capture at both edges of GTIOCnB input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOCnB input



Note: 寄存器的基地址相同。

Figure 21.29 GTCCRA和GTCCRB缓冲区操作的示例，在两个边沿都有输入捕获GTIOCnA输入，递增计数中的锯齿波，并且GTCNT计数器在GTIOCnA input



Note: 寄存器的基地址相同。

Figure 21.30 GTCCRA和GTCCRB双缓冲操作示例，在两个边沿进行输入捕获GTIOCnB输入，递增计数中的锯齿波，GTCNT计数器在两个边缘清零GTIOCnB input

Table 21.21 Example for setting GTCCRA and GTCCRB buffer operation for input capture

No.	Step Name	Description
1	Set operating mode and counter clear sources	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits and count clear source with the GTCSR register. In Figure 21.29, MD[2:0] = 000b or MD[3:0] = 0000b (saw-wave PWM mode 1) and GTCSR = 0x00000F00, and in Figure 21.30, MD[2:0] = 000b or MD[3:0] = 0000b (saw-wave PWM mode 1) and GTCSR = 0x0000F000.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.29, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode2, set the cycle in the GTPR register. In the saw-wave PWM mode2, select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Select input capture source	Select input capture source in the GTICASR register and GTICBSR register. In Figure 21.29, GTICASR = 0x00000F00, and in Figure 21.30, GTICBSR = 0x0000F000. To perform input capture with sources of other channels, select a group that performs inter-channel cooperation by the GTICCR.ICmGRP bit (m = A or B). For the output-side channel of the input capture sources, set the GTICCR register to enables the input capture sources to output to other channels. For input-side channels, set the GTIOmSR.mSOC bit (m = A or B) to 1 to enable input capture with sources of other channels.
7	Set buffer operation	Set buffer operation with the CCRA and CCRB bits in the GTBER register. In Figure 21.29, CCRA[1:0] = 01b, and in Figure 21.30, CCRB[1:0] = 1xb.
8	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

21.3.2.3 Buffer Operation for GTADTRA and GTADTRB Registers

The GTADTBRA register can function as the GTADTRA buffer register and the GTADTDBRA register can function as the GTADTBRA buffer register (double buffer register for the GTADTRA register). Similarly, the GTADTBRB register can function as the GTADTRB buffer register and the GTADTDBRB register can function as the GTADTBRB buffer register (double buffer register for the GTADTRB register).

To set the GTADTRA or GTADTRB register to function as a double buffer, set the GTBER.ADTDA or ADTDB bit to 1. For single buffer operation, set 0. Not to function as buffer, set the GTBER.ADTTA[1:0] or ADTTB[1:0] bits to 00b.

The buffer transfer timing can be set with the ADTTA[1:0] and ADTTB[1:0] bits to an overflow (in up-counting) or an underflow (in down-counting) in saw-wave mode, with ADTTA[1:0] and ADTTB[1:0] bits to 01b for a crest, to 10b for a trough, or to 11b for both crest and trough in triangle-wave mode or complementary PWM mode.

In saw-wave mode, when the ADTTA[1:0] and ADTTB[1:0] bits are set to value other than 00b and in count operation, the buffer transfer, by similar counter clearing sources in section 21.3.2.1. GTPR Register Buffer Operation, is performed in the same way at an overflow (in up-counting) or an underflow (in down-counting).

In complementary PWM mode, the buffer transfer is performed after one GTCLK cycle from GTCCRD register write of slave channel 2.

In saw-wave mode, the buffer transfer of GTADTRm register by counter clearing can be disabled by GTBER2.CCTADm (m = A, B) bit setting.

In saw-wave mode, the buffer transfer of GTADTRm register by its own compare match can be enabled by the GTBER2.CMTADm (m = A, B) bit setting.

Figure 21.31 to Figure 21.35 show examples of buffer operation of the GTADTRA and GTADTRB registers, and Table 21.22 shows an example for setting buffer operation of the GTADTRA and GTADTRB registers.

Table 21.21 为输入捕捉设置GTCCRA和GTCCRB缓冲操作的示例

No.	步骤名称	Description
1	设置操作模式和计数器清除源	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式，并使用GTCSR寄存器清除计数源。在图21.29中，MD[2:0]=000b或MD[3:0]=0000b（锯齿波PWM模式1）和GTCSR=0x00000F00，在图21.30中，MD[2:0]=000b或MD[3:0]=0000b（锯波PWM模式1）和GTCSR=0x0000F000。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.29中，在GTUDDTYC[1:0]位中设置11b后，在GTUDDTYC[1:0]位中设置01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	除了锯齿波PWM模式2，在GTPR寄存器中设置周期。 在锯齿波PWM模式2中，通过GTCSR.CSCMSC[2:0]位选择计数器清零源比较匹配寄存器GTCCRx（x=A到F）并在该寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	选择输入捕捉源	在GTICASR寄存器和GTICBSR寄存器中选择输入捕捉源。 在图21.29中，GTICASR=0x00000F00，在图21.30中，GTICBSR=0x0000F000。 要使用其他通道的源执行输入捕获，请通过GTICCR.ICmGRP位（m=A或B）选择执行通道间协作的组。对于输入捕捉源的输出侧通道，设置GTICCR寄存器使输入捕捉源能够输出到其他通道。对于输入侧通道，将GTIOmSR.mSOC位（m=A或B）设置为1以启用其他通道源的输入捕捉。
7	设置缓冲操作	使用GTBER寄存器中的CCRA和CCRB位设置缓冲区操作。在图21.29中，CCRA[1:0]=01b，在图21.30中，CCRB[1:0]=1xb。
8	开始计数操作	将GTCR.CST位设置为1以启动计数操作。

21.3.2.3 GTADTRA和GTADTRB寄存器的缓冲区操作

GTADTBRA寄存器可用作GTADTRA缓冲寄存器，GTADTBRA寄存器可用作GTADTBRA缓冲寄存器（GTADTRA寄存器的双缓冲寄存器）。类似地，GTADTBRB寄存器可以用作GTADTRB缓冲寄存器，GTADTDRBB寄存器可以用作GTADTBRB缓冲寄存器（GTADTRB寄存器的双缓冲寄存器）。

要将GTADTRA或GTADTRB寄存器设置为双缓冲器，请将GTBER.ADTDA或ADTDB位设置为1。
对于单缓冲区操作，设置为0。不用作缓冲区，将GTBER.ADTTA[1:0]或ADTTB[1:0]位设置为00b。

缓冲区传输时序可以通过ADTTA[1:0]和ADTTB[1:0]位设置为锯齿波模式中的上溢（递增计数）或下溢（递减计数），使用ADTTA[1:0]和ADTTB[1:0]位到01b表示波峰，10b表示波谷，或11b表示三角波模式或互补PWM模式的波峰和波谷。

在锯齿波模式下，当ADTTA[1:0]和ADTTB[1:0]位设置为00b以外的值并且在计数操作中，缓冲区传输，由21.3.2.1节中类似的计数器清除源。GTPR寄存器缓冲区操作，在上溢（向上计数）或下溢（向下计数）时以相同的方式执行。

在互补PWM模式下，缓冲区传输在从通道2的GTCCRD寄存器写入开始的一个GTCLK周期后执行。

在锯齿波模式下，通过设置GTBER2.CCTADm(m=A B)位可以禁止通过计数器清零对GTADTRm寄存器的缓冲传输。

在锯齿波模式下，GTADTRm寄存器的缓冲区传输通过其自身的比较匹配可以通过GTBER2.CMTADm(m=A B)位设置。

图21.31至图21.35显示了GTADTRA和GTADTRB寄存器的缓冲操作示例，表21.22显示了设置GTADTRA和GTADTRB寄存器的缓冲操作示例。

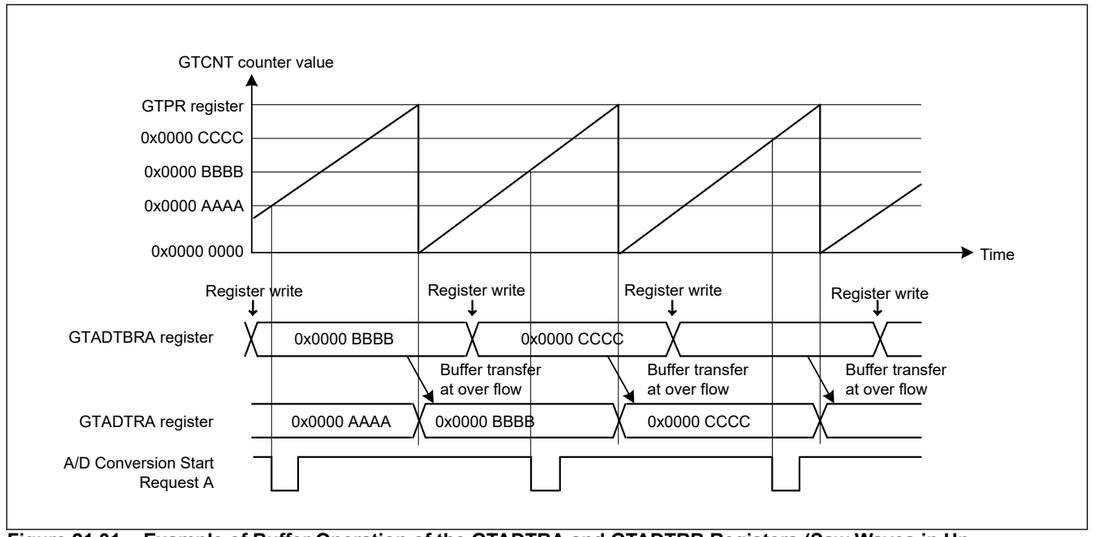


Figure 21.31 Example of Buffer Operation of the GTADTRA and GTADTRB Registers (Saw Waves in Up-Counting, A/D Conversion Start Request Generated by Up-Counting)

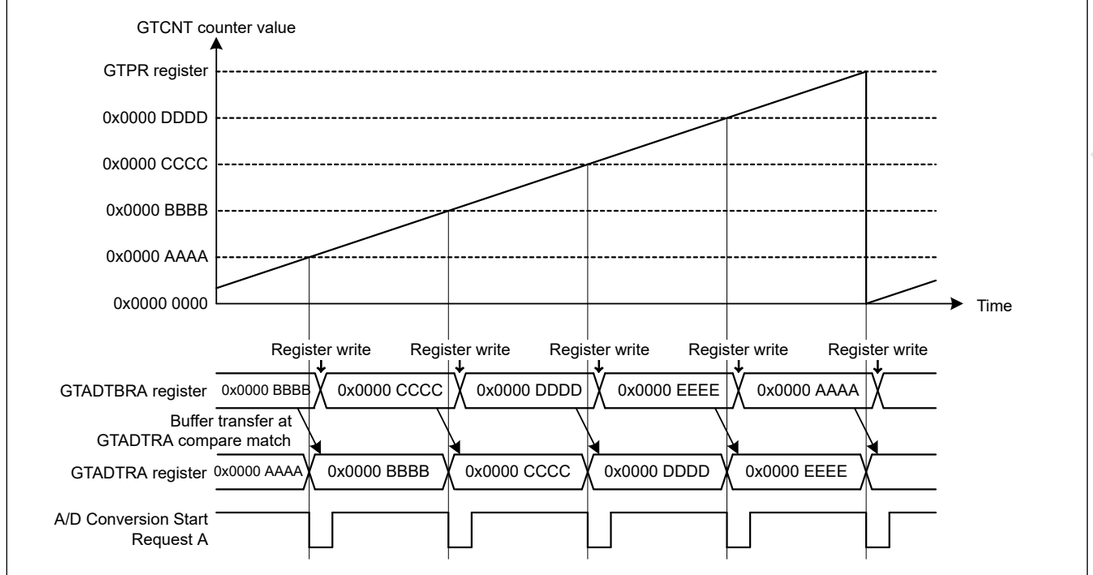


Figure 21.32 Example of Buffer Operation of the GTADTRA and GTADTRB Registers (Saw Waves in Up-Counting, Buffer Transfer at GTADTRA Compare Match, A/D Conversion Start Request Generated by Up-Counting)

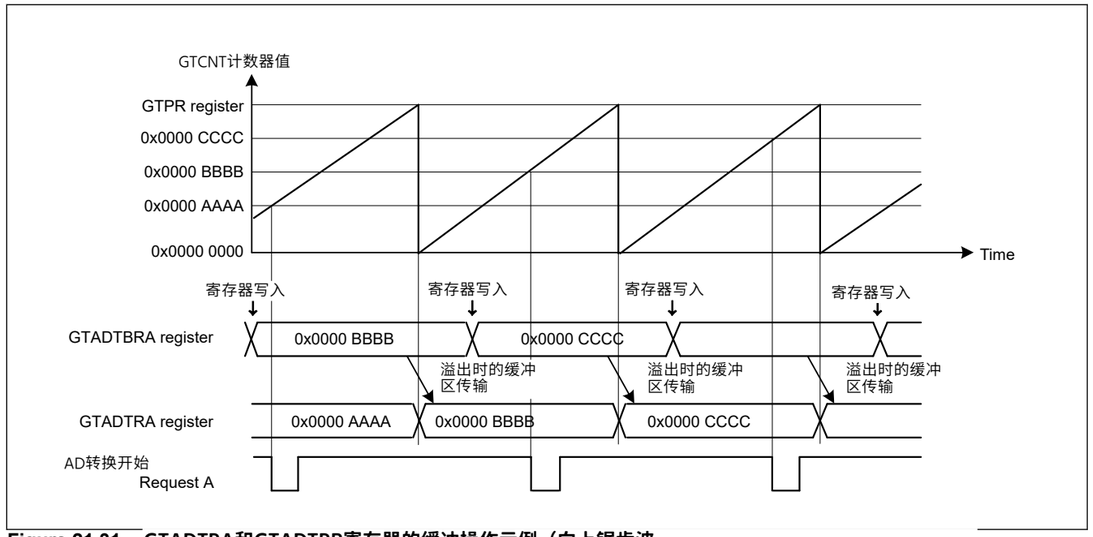


Figure 21.31 GTADTRA和GTADTRB寄存器的缓冲操作示例（向上锯齿波计数，向上计数产生的AD转换开始请求）

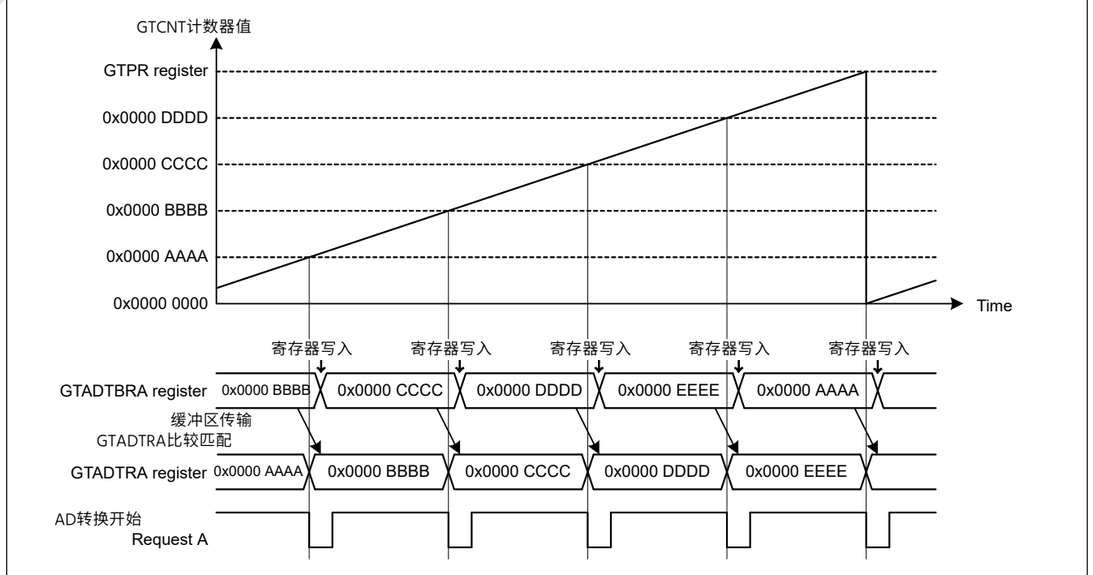


Figure 21.32 GTADTRA和GTADTRB寄存器的缓冲操作示例（向上锯齿波计数、GTADTRA比较匹配时的缓冲区传输、AD转换开始请求由向上计数生成）

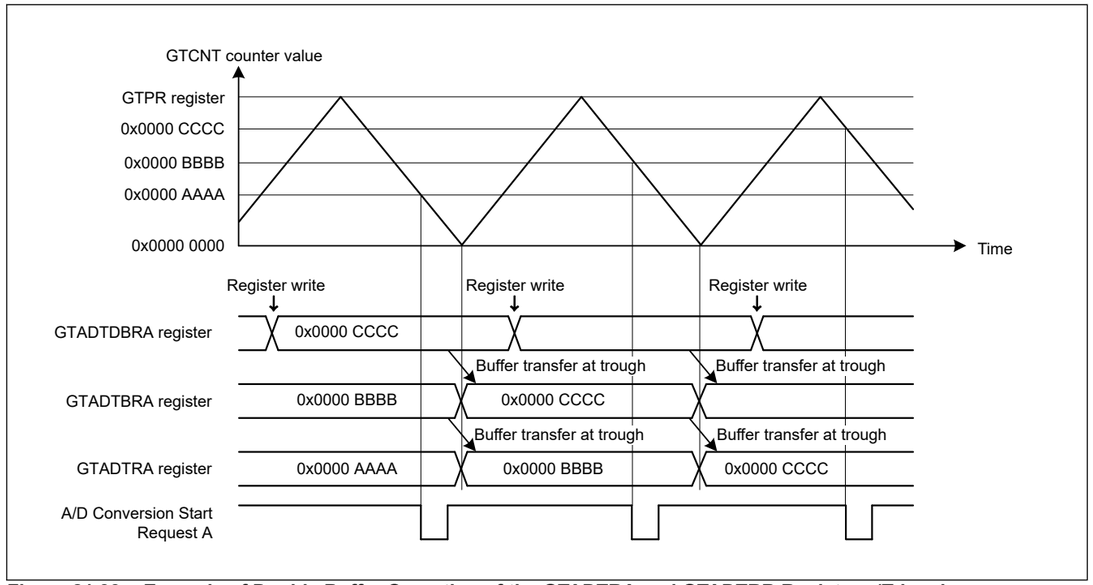


Figure 21.33 Example of Double Buffer Operation of the GTADTRA and GTADTRB Registers (Triangle Waves, Buffer Transfer at Troughs, A/D Conversion Start Request Generated by Down-Counting)

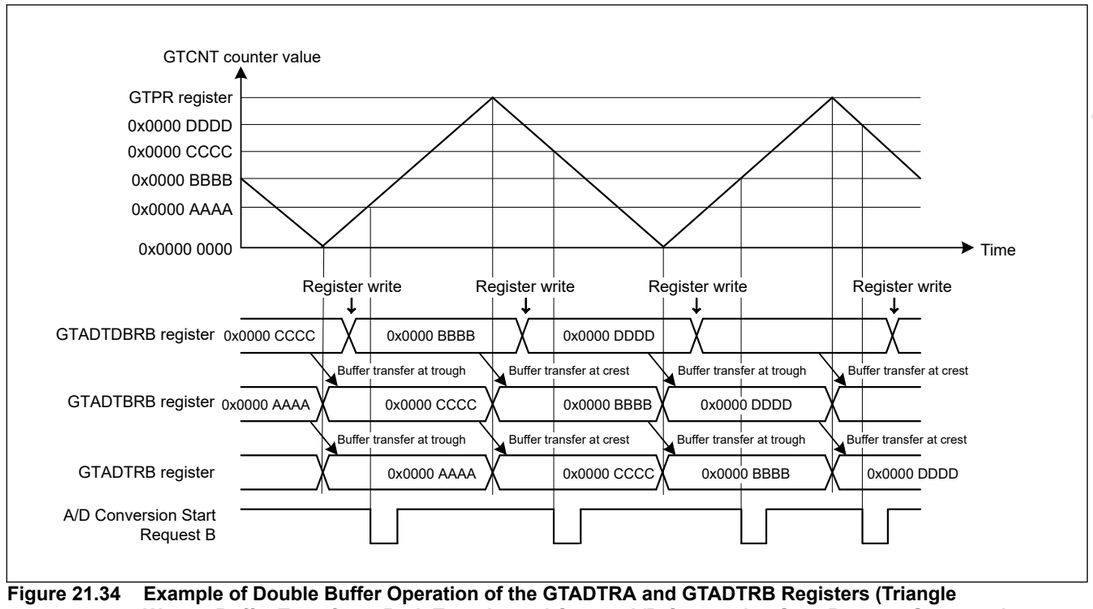


Figure 21.34 Example of Double Buffer Operation of the GTADTRA and GTADTRB Registers (Triangle Waves, Buffer Transfer at Both Troughs and Crests, A/D Conversion Start Request Generated by Both Up- and Down-Counting)

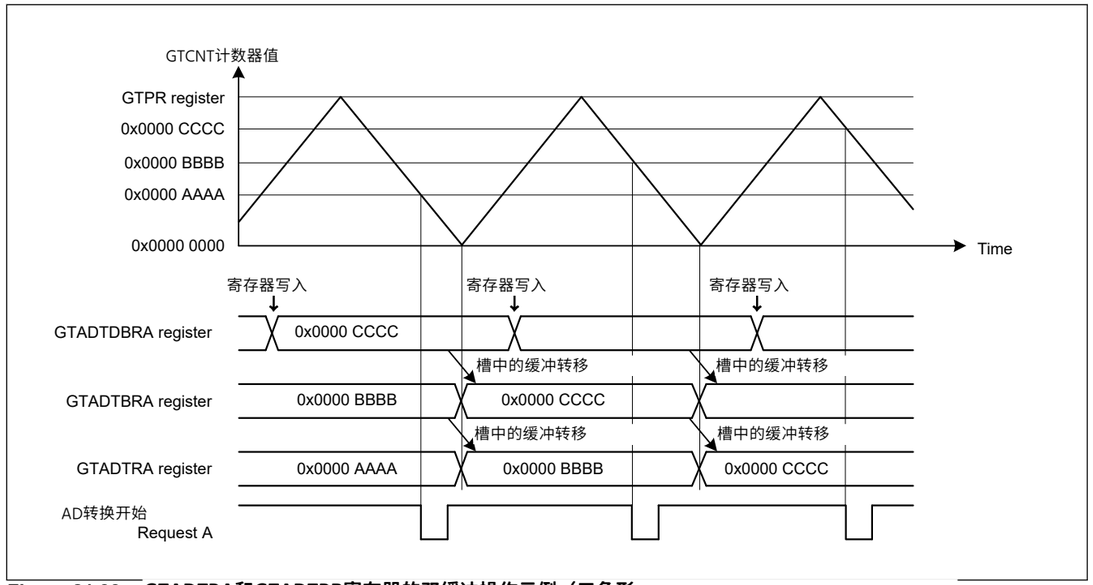


Figure 21.33 GTADTRA和GTADTRB寄存器的双缓冲操作示例（三角形 Waves BufferTransferatTroughs Down产生的AD转换开始请求 Counting)

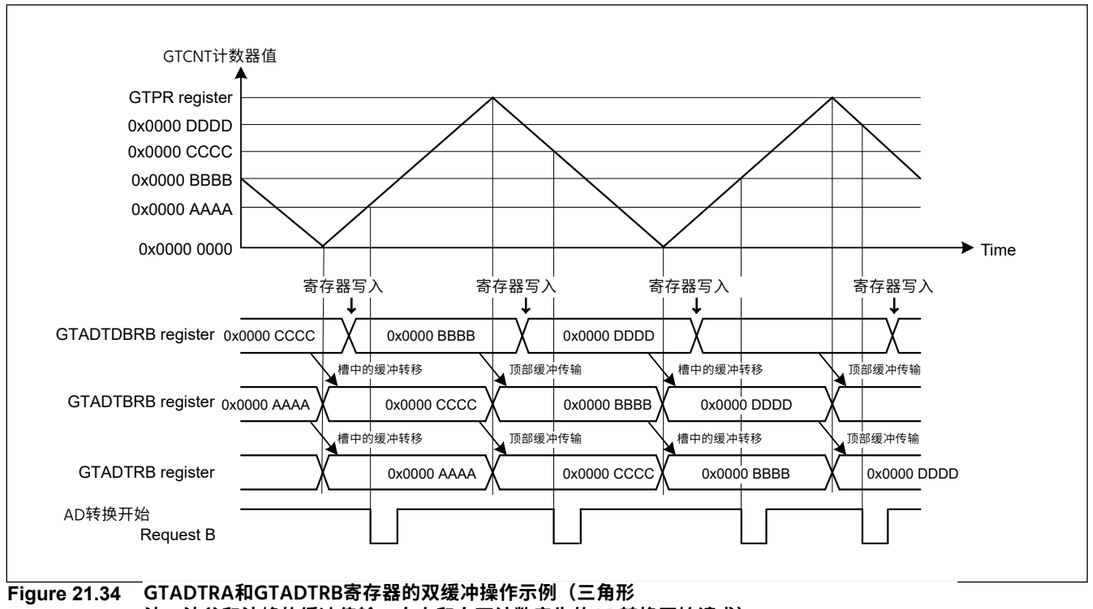


Figure 21.34 GTADTRA和GTADTRB寄存器的双缓冲操作示例（三角形 波、波谷和波峰的缓冲传输、向上和向下计数产生的AD转换开始请求）

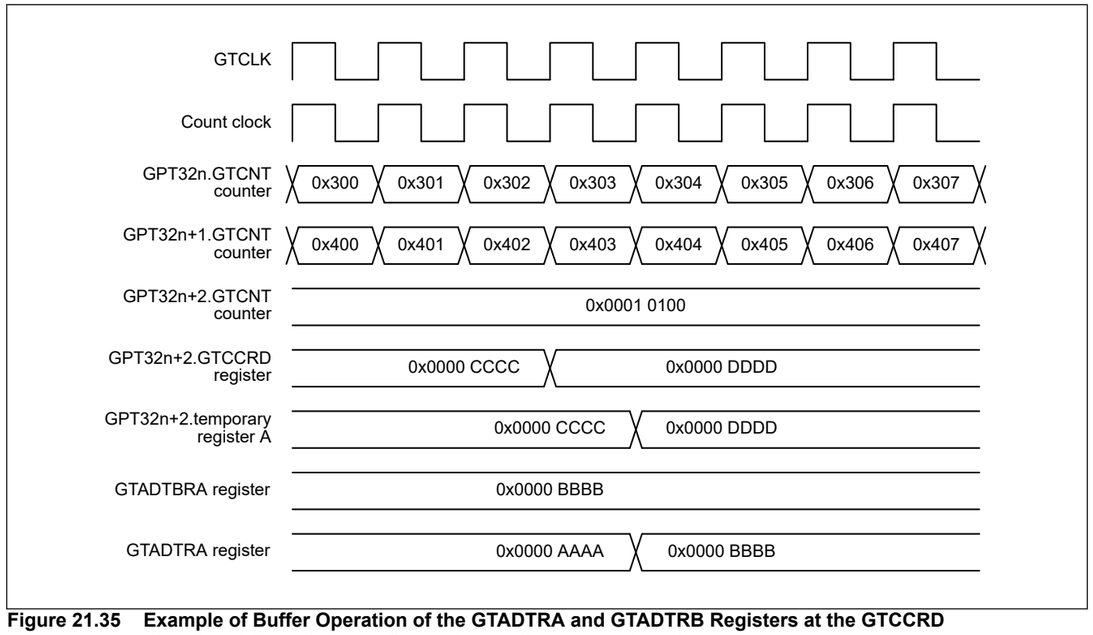


Figure 21.35 Example of Buffer Operation of the GTADTRA and GTADTRB Registers at the GTCCRD Register of Slave Channel 2 Updating in Complementary PWM Mode

Table 21.22 Example for Setting Buffer Operation of the GTADTRA and GTADTRB registers (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. (In Figure 21.31 and Figure 21.32, 000b or 0000b (saw-wave PWM mode 1) is set, in Figure 21.33 and Figure 21.34, 100b, 101b, 110b, 0100b, 0101b, or 0110b (triangle-wave PWM mode) is set.)
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. (In Figure 21.31 and Figure 21.32, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).)
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode 2, set the cycle in the GTPR register. In the saw-wave PWM mode 2, select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set buffer operation	Set buffer operation with the ADTTA[1:0], ADTTB[1:0], ADTDA, and ADTDB bits in GTBER register. To perform buffer transfer at a compare match of the ADTRAm (m = A, B) register, set the GTBER2.CMTADm bit to 1. (In Figure 21.31, ADTTA[1:0] bits = 01b, 10b, or 11b and ADTDA bit = 0, in Figure 21.32, CMTADA bit = 1, in Figure 21.33, ADTTA[1:0] bits = 10b and ADTDA bit = 1, and in Figure 21.34, ADTTB[1:0] bits = 11b and ADTDB bit = 1.)
7	Set compare match value	Set the A/D conversion start request point in the GTADTRA and GTADTRB registers.
8	Set buffer value	For buffer operation, set the A/D conversion start request point in one cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTBRA and GTADTBRB registers. For double buffer operation, also set the A/D conversion start request point in two cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or one cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTDBRA and GTADTDBRB registers.

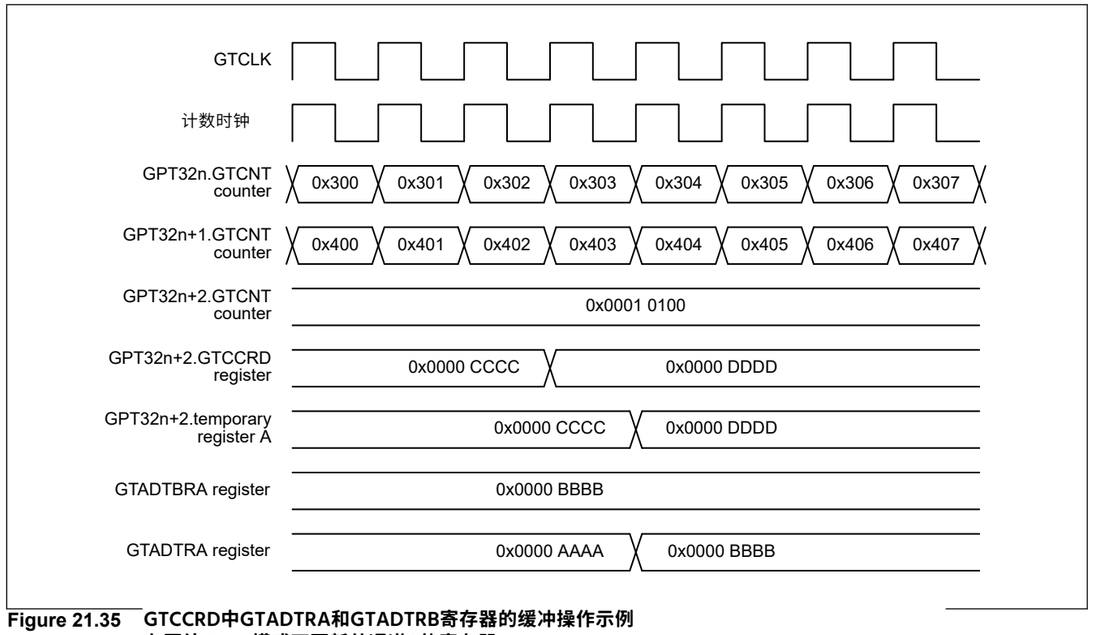


Figure 21.35 GTCCRD中GTADTRA和GTADTRB寄存器的缓冲操作示例 在互补PWM模式下更新从通道2的寄存器

Table 21.22 设置GTADTRA和GTADTRB寄存器的缓冲操作的示例（1of2）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。（在图21.31和图21.32中，设置了000b或000b（锯齿波PWM模式1），在图21.33和图21.34中，设置了100b、101b、110b、0100b、0101b或0110b（三角波PWM模式）.）
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。（在图21.31和图21.32中，在GTUDDTYC[1:0]位中设置了11b后，在GTUDDTYC[1:0]位中设置了01b（向上计数）。）
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	除了锯齿波PWM模式2，在GTPR寄存器中设置周期。在锯齿波PWM模式2中，通过GTCSR.CSCMSC[2:0]位选择计数器清零源比较匹配寄存器GTCCRx（x=A到F）并在该寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置缓冲操作	使用GTBER寄存器中的ADTTA[1:0]、ADTTB[1:0]、ADTDA和ADTDB位设置缓冲区操作。要在ADTRAm(m=A B)寄存器的比较匹配时执行缓冲区传输，请将 GTBER2.CMTADm位为1。（在图21.31中，ADTTA[1:0]位=01b、10b或11b且ADTDA位=0，在图21.32中，CMTADA位=1，在图21.33中，ADTTA[1:0]位=10b和ADTDA位=1，在图21.34中，ADTTB[1:0]位=11b和ADTDB位=1。）
7	设置比较匹配值	在GTADTRA和GTADTRB寄存器中设置AD转换开始请求点。
8	设置缓冲区值	对于缓冲操作，将AD转换开始请求点设置在当前周期后的一个周期（锯齿波模式或三角波模式，在波谷或波峰处缓冲传输）或当前周期后的半个周期（三角波模式GTADTBRA和GTADTBRB寄存器中的波谷和波峰缓冲传输）。 对于双缓冲操作，还要在当前周期后的两个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的一个周期（在三角波模式下）设置AD转换开始请求点GTADTDBRA和GTADTDBRB寄存器中的波谷模式和波峰缓冲传输）。

Table 21.22 Example for Setting Buffer Operation of the GTADTRA and GTADTRB registers (2 of 2)

No.	Step Name	Description
9	Enable A/D conversion start request	Set to enable A/D conversion start request with the ADTRAUEN, ADTRADEN, ADTRBUEN, and ADTRBDEN bits in the GTINTAD register. (In Figure 21.31 and Figure 21.32, ADTRAUEN bit = 1, in Figure 21.33, ADTRADEN bit = 1, and in Figure 21.34, ADTRBUEN bit = 1 and ADTRBDEN bit = 1.)
10	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
11	Set buffer value of each cycle	For buffer operation, set the A/D conversion start request point in one cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTBRA and GTADTBRB registers. For double buffer operation, also set the A/D conversion start request point in two cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or one cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTDBRA and GTADTDBRB registers.

21.3.2.4 Buffer operation for GTIOA and GTIOB

The GTOLBR.GTIOAB[4:0] bits can function as the buffer register of the GTIOR.GTIOA[4:0] bits and the GTOLBR.GTIOBB[4:0] bits can function as the buffer register of the GTIOR.GTIOB[4:0] bits.

Buffer transfer timing can be set with the GTBER2.OLTTm[1:0] bits (m = A, B). It can be selected from the end of cycle or GTCCR register compare match (in saw-wave mode), from crest, trough, or both crest and trough (in triangle-wave mode and complementary PWM mode). In the case that the GTBER2.OLTTm[1:0] bits are 00b, buffer transfer is not performed.

In complementary PWM mode, it is prohibited to set the buffer transfer timing to overlap with the dead time. Therefore, when the buffer transfer timing is crest, set the GTCCRm(m = A,C,E) register to satisfy GTCCRm < GTPR. And when the buffer transfer timing is trough, set the GTCCRm register to satisfy GTDVU < GTCCRm.

Figure 21.36 to Figure 21.38 show examples of buffer operation of the GTIOR.GTIOA[4:0] and GTIOR.GTIOB[4:0] bits.

Table 21.23 shows an example for setting buffer operation of the GTIOR.GTIOA[4:0] and GTIOR.GTIOB[4:0] bits.

Table 21.22 设置GTADTRA和GTADTRB寄存器的缓冲操作示例（2of2）

No.	步骤名称	Description
9	启用AD转换启动请求	通过ADTRAUEN、ADTRADEN、ADTRBUEN和GTINTAD寄存器中的ADTRBDEN位。（在图21.31和图21.32中，ADTRAUEN位=1，在图21.33中，ADTRADEN位=1，在图21.34中，ADTRBUEN位=1和ADTRBDEN位=1。）
10	开始计数操作	将GTCR.CST位设置为1以启动计数操作。
11	设置每个周期的缓冲值	对于缓冲操作，将AD转换开始请求点设置在当前周期后的一个周期（锯齿波模式或三角波模式，在波谷或波峰处缓冲传输）或当前周期后的半个周期（三角波模式GTADTBRA和GTADTBRB寄存器中的波谷和波峰缓冲传输）。 对于双缓冲操作，还要在当前周期后的两个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的一个周期（在三角波模式下）设置AD转换开始请求点GTADTDBRA和GTADTDBRB寄存器中的波谷模式和波峰缓冲传输）。

21.3.2.4 GTIOA和GTIOB的缓冲操作

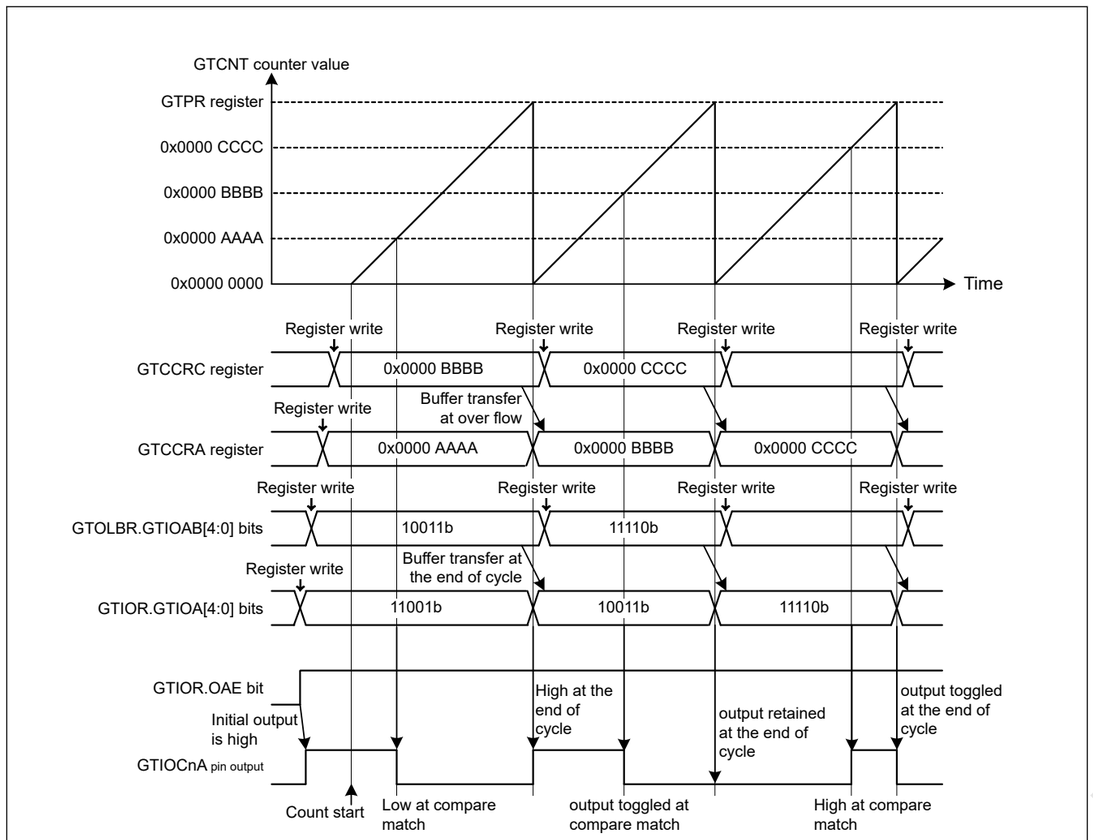
GTOLBR.GTIOAB[4:0]位可以作为GTIOR.GTIOA[4:0]位的缓冲寄存器和GTOLBR.GTIOBB[4:0]位可用作GTIOR.GTIOB[4:0]位的缓冲寄存器。

可以使用GTBER2.OLTTm[1:0]位(m=A B)设置缓冲区传输时序。它可以从周期结束或GTCCR寄存器比较匹配中选择（在锯齿波模式下），从波峰、波谷或波峰和波谷（在三角波模式和互补PWM模式下）中选择。在GTBER2.OLTTm[1:0]位为00b的情况下，不执行缓冲区传输。

在互补PWM模式下，禁止将缓冲区传输时序设置为与死区时间重叠。因此，当缓冲传输时序为峰值时，设置GTCCRm(m=A C E)寄存器以满足GTCCRm<GTPR。并且当缓冲区传输时序低谷时，将GTCCRm寄存器设置为满足GTDVU<GTCCRm。

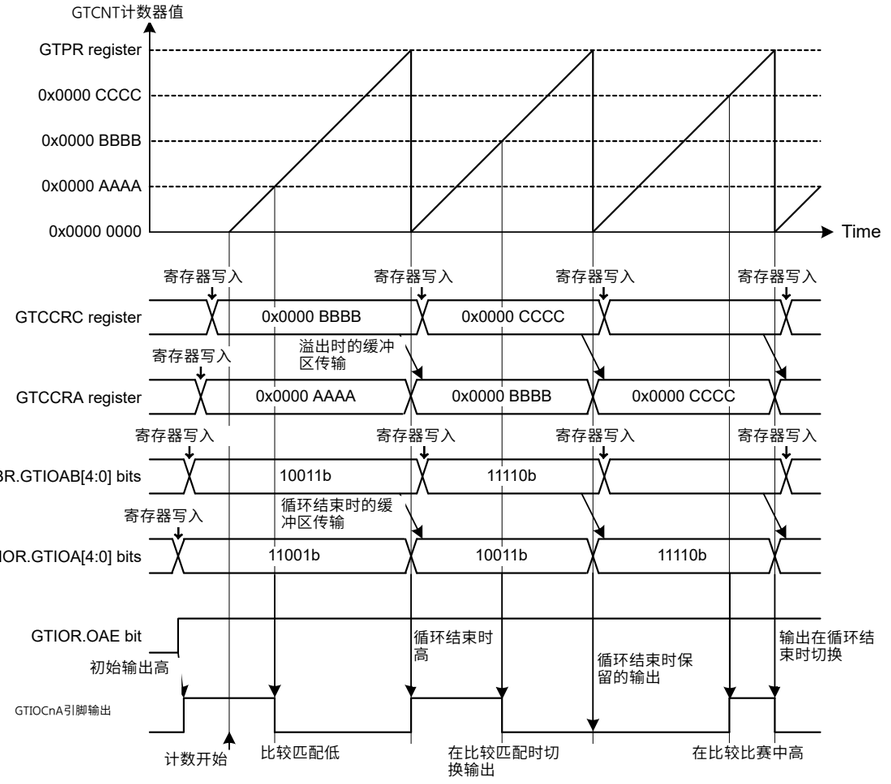
图21.36至图21.38显示了GTIOR.GTIOA[4:0]和GTIOR.GTIOB[4:0]位的缓冲区操作示例。

表21.23显示了设置GTIOR.GTIOA[4:0]和GTIOR.GTIOB[4:0]位的缓冲区操作的示例。



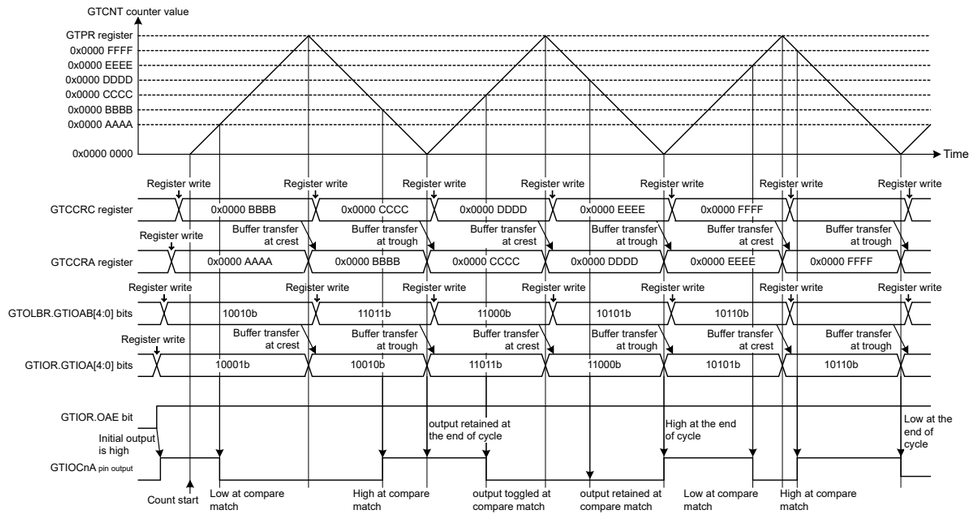
Note: Initial output is synchronized to the count clock.

Figure 21.36 Example of Buffer Operation of the GTIOA and GTIOB Bits (Up-Counting in Saw-Wave PWM Mode 1, Buffer Transfer at the End of Cycle)



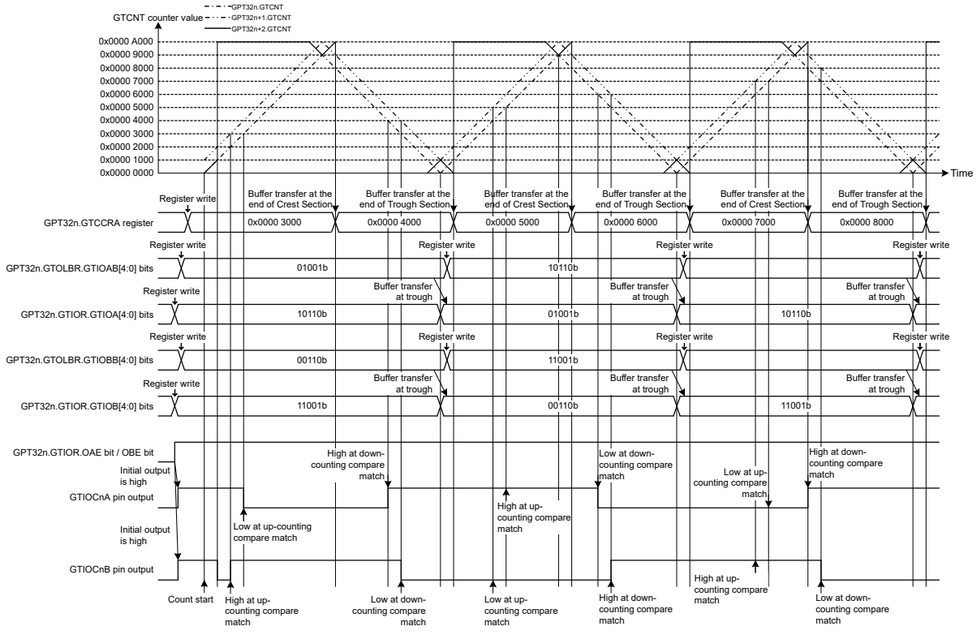
Note: 初始输出与计数时钟同步。

Figure 21.36 GTIOA和GTIOB位的缓冲器操作示例（锯波PWM中的向上计数）模式1，循环结束时的缓冲区传输）



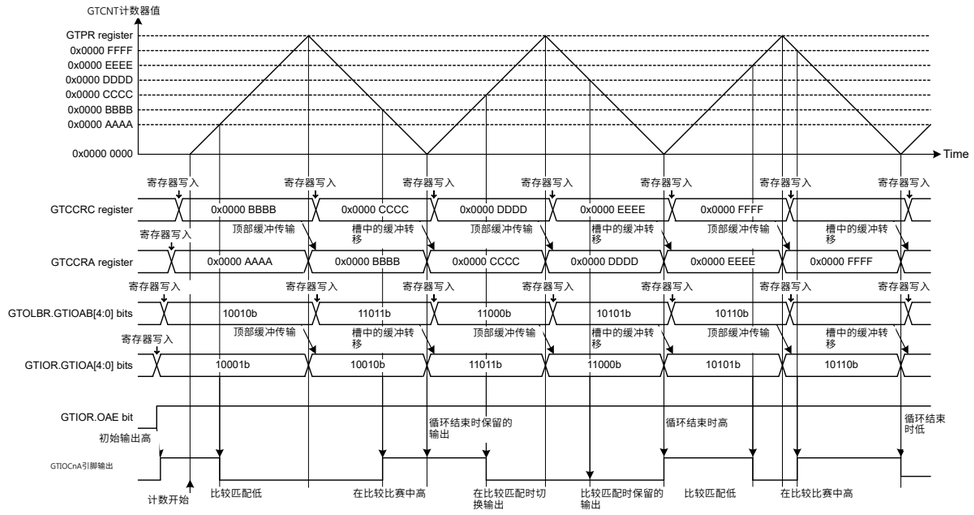
Note: Initial output is synchronized to the count clock.

Figure 21.37 Example of Buffer Operation of the GTIOA and GTIOB Bits (Triangle-Wave PWM Mode 2, Buffer Transfer at Crests and Troughs)



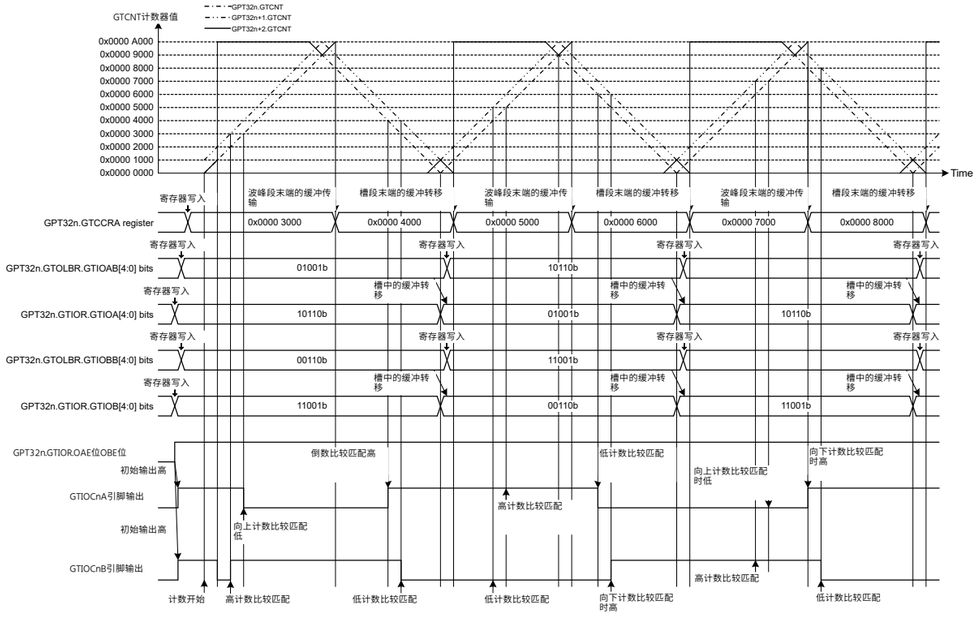
Note: Initial output is synchronized to the count clock.

Figure 21.38 Example of Buffer Operation of the GTIOA and GTIOB Bits (Complementary PWM Mode 3, Buffer Transfer at Troughs)



Note: 初始输出与计数时钟同步。

Figure 21.37 GTIOA和GTIOB位的缓冲器操作示例（三角波PWM模式2，缓冲器在波峰和波谷转移）



Note: 初始输出与计数时钟同步。

Figure 21.38 GTIOA和GTIOB位的缓冲操作示例（互补PWM模式3，槽处的缓冲转移）

Table 21.23 Example for Setting Buffer Operation of the GTIOA and GTIOB

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[3:0]. (In Figure 21.36, 0000b (saw-wave PWM mode 1) is set, in Figure 21.37, 0101b (triangle-wave PWM mode 2) is set, in Figure 21.38, 1110b (complementary PWM mode 3) is set.)
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. (In Figure 21.36, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).)
3	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode 2, Set the cycle in GTPR. In the saw-wave PWM mode 2, Select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. (In Figure 21.36, GTIOA[4:0] = 11001b, in Figure 21.37, GTIOA[4:0] = 10001b, in Figure 21.38, GTIOA[4:0] = 10110b and GTIOB[4:0] = 11001b.)
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set buffer operation	Set buffer operation with OLTTm[1:0] bits in GTBER2 register. (In Figure 21.36, 01b is set in OLTTA[1:0], in Figure 21.37, 11b is set in OLTTA[1:0], in Figure 21.38, 10b is set in OLTTA[1:0] and 10b is set in OLTTB[1:0].)
9	Set buffer value	For buffer operation, set the GTIOCnm pin function in one cycle after the current cycle (in saw-wave mode and in triangle-wave/complementary PWM mode with buffer transfer at crest or trough) or half cycle after the current cycle (in triangle-wave/complementary PWM mode with buffer transfer at crest and trough) in the GTOLBR register.
10	Start count operation	Set GTCR.CST to 1 to start count operation.
11	Set buffer value of each cycle	For buffer operation, set the GTIOCnm pin function in one cycle after the current cycle (in saw-wave mode and in triangle-wave/complementary PWM mode with buffer transfer at crest or trough) or half cycle after the current cycle (in triangle-wave/complementary PWM mode with buffer transfer at crest and trough) in the GTOLBR register.

Note: n = 4 to 9
m = A, B

21.3.3 PWM Output Operating Mode

The GPT can output PWM waveforms to the GTIOCnA or GTIOCnB pin (n = 0 to 9) by a compare match between the GTCNT counter and GTCCRA or GTCCRB.

By setting GTDTCR, GTDVU, and GTDVD, the compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

In complementary PWM mode, it is possible to output PWM waveforms (positive phase, negative phase) with dead time that guarantees the linearity of the PWM output pulse width near 0% and 100% duty.

In saw-wave mode other than saw-wave PWM mode 2, or triangle-wave mode, or the master channel of complementary PWM mode, the signal synchronized with the PWM cycle can be output from the GTCPPOn output terminal by setting the GTIOR.PSYE bit to 1. The GTCPPOn output is toggled at the end of cycle in saw-wave mode or at the timing of crest / trough / GTCNT counter clearing in triangle-wave mode or complementary PWM mode. The initial output of GTCPPOn is low, and it becomes high when the count starts.

21.3.3.1 Saw-Wave PWM Mode 1

In saw-wave PWM mode 1, GTCNT performs saw-wave (half-wave) operation by setting the cycle in GTPR and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 9) when a GTCCRA or GTCCRB compare match occurs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

When 0 is set in the GTIOR.OxEOCD (x = A, B) bit and the timing of the end of cycle and the timing of GTCCRx register compare match are the same time, the output pin performs along the PWM output setting for the end of cycle set by the GTIOR.GTIOx[3:2] bit.

When 1 is set in the GTIOR.OxEOCD bit, GTIOCnx output is retained.

Table 21.23 设置GTIOA和GTIOB的缓冲操作示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[3:0]设置操作模式。（在图21.36中，设置了0000b（锯齿波PWM模式1），在图21.37中，设置了0101b（三角波PWM模式2），在图21.38中，设置了1110b（互补PWM模式3）。）
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。（在图21.36中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。）
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	除了锯齿波PWM模式2，在GTPR中设置周期。 在锯齿波PWM模式2中，通过GTCSR.CSCMSC[2:0]位选择计数器清零源比较匹配寄存器GTCCRx（x=A到F）并在该寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。（在图21.36中，GTIOA[4:0]=11001b，在图21.37中，GTIOA[4:0]=10001b，在图21.38中，GTIOA[4:0]=10110b和GTIOB[4:0]=11001b。）
7	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
8	设置缓冲操作	使用GTBER2寄存器中的OLTTm[1:0]位设置缓冲区操作。（在图21.36中，01b设置在OLTTA[1:0]中，在图21.37中，11b设置在OLTTA[1:0]中，在图21.38中，10b设置在OLTTA[1:0]中，10b设置在OLTTB[1:0]。）
9	设置缓冲区值	对于缓冲操作，将GTIOCnm引脚功能设置在当前周期之后的一个周期（锯齿波模式和三角波互补PWM模式，在波峰或波谷缓冲传输）或当前周期后的半个周期（三角波互补GTOLBR寄存器中的波峰和波谷缓冲传输的PWM模式。
10	开始计数操作	将GTCR.CST设置为1以启动计数操作。
11	设置每个周期的缓冲值	对于缓冲操作，将GTIOCnm引脚功能设置在当前周期之后的一个周期（锯齿波模式和三角波互补PWM模式，在波峰或波谷缓冲传输）或当前周期后的半个周期（三角波互补GTOLBR寄存器中的波峰和波谷缓冲传输的PWM模式。

Note: n = 4 to 9
m = A, B

21.3.3 PWM输出工作模式

GPT可以通过比较匹配输出PWM波形到GTIOCnA或GTIOCnB引脚（n=0到9）。
GTCNT计数器和GTCCRA或GTCCRB。

通过设置GTDTCR、GTDVU和GTDVD，可以自动将带死区时间的负相波形的比较匹配值设置为GTCCRB。

在互补PWM模式下，可以输出带有死区时间的PWM波形（正相、负相），保证PWM输出脉冲宽度在0%和100%占空比附近的线性度。

在锯齿波PWM模式2以外的锯齿波模式，或三角波模式，或互补PWM模式的主通道，可以通过设置GTIOR.PSYE从GTCPPOn输出端输出与PWM周期同步的信号位为1。GTCPPOn输出在锯齿波模式下的周期结束时切换，或者在三角波模式或互补PWM模式下在波峰波谷GTCNT计数器清零时切换。GTCPPOn的初始输出为低电平，计数开始时变为高电平。

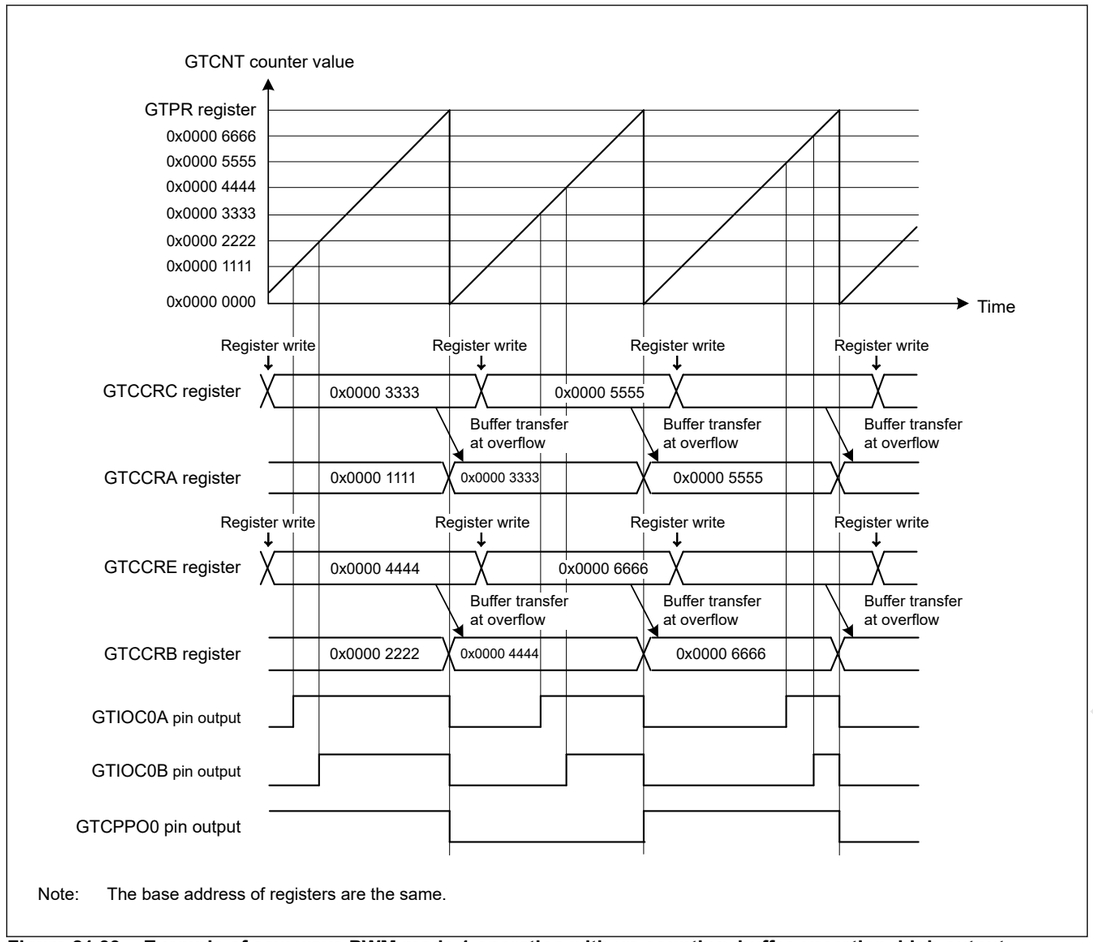
21.3.3.1 Saw-Wave PWM Mode 1

在锯齿波PWM模式1中，GTCNT通过设置GTPR的周期执行锯齿波（半波）操作，当GTCCRA或GTCCRB比较时，PWM波形输出到GTIOCnA或GTIOCnB引脚（n=0至9）匹配发生。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

当GTIOR.OxEOCD(x=A B)位设置为0并且周期结束的时序和GTCCRx寄存器比较匹配的时序相同时，输出引脚执行结束的PWM输出设置GTIOR.GTIOx[3:2]位设置的周期。

当GTIOR.OxEOCD位设置为1时，GTIOCnx输出保持不变。

Figure 21.39 shows an example of saw-wave PWM mode 1 operation, and Table 21.24 shows an example for setting saw-wave PWM mode 1.



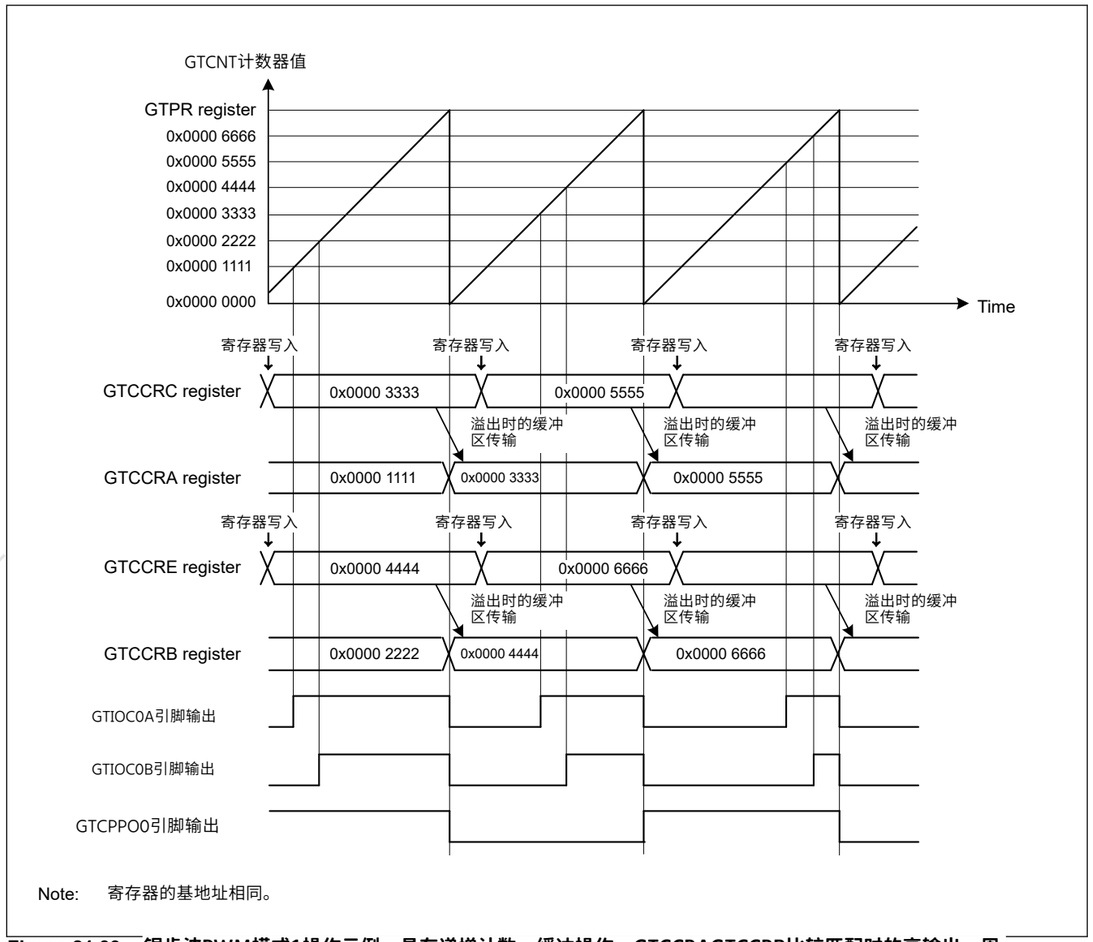
Note: The base address of registers are the same.

Figure 21.39 Example of saw-wave PWM mode 1 operation with up-counting, buffer operation, high output at GTCCRA/GTCCRB compare match, low output at cycle end, and GTIOR.PSYE = 1

Table 21.24 Example for setting saw-wave PWM mode 1 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.39, 000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.39, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 21.39, GTIOA[4:0] = 00110b and GTIOB[4:0] = 00110b.
7	Enable GTCPPOn pin output	Set to enable/disable the GTCPPOn pin output with the PSYE bit in the GTIOR register.

图21.39显示了锯齿波PWM模式1操作的示例，表21.24显示了设置锯齿波PWM模式1的示例。



Note: 寄存器的基地址相同。

Figure 21.39 锯齿波PWM模式1操作示例，具有递增计数、缓冲操作、GTCCRAGTCCRB比较匹配时的高输出、周期结束时的低输出和GTIOR.PSYE=1

Table 21.24 设置锯齿波PWM模式1的示例（1of2）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。在图21.39中，设置了000b（锯齿波PWM模式1）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.39中，在GTUDDTYC[1:0]位中设置了11b之后，在GTUDDTYC[1:0]位中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	在GTPR寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR寄存器中的GTIOA[4:0]和GTIOB[4:0]位设置GTIOCnm引脚功能。 在图21.39中，GTIOA[4:0]=00110b和GTIOB[4:0]=00110b。
7	启用GTCPPOn引脚输出	使用GTIOR寄存器中的PSYE位设置启用禁用GTCPPOn引脚输出。

Table 21.24 Example for setting saw-wave PWM mode 1 (2 of 2)

No.	Step Name	Description
8	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
9	Set buffer operation	Set buffer operation with the CCRA[1:0] and CCRB[1:0] bits in the GTBER register. In Figure 21.39, CCRA[1:0] = 01b and CCRB[1:0] = 01b.
10	Set compare match value*1	Set the GTIOCnA pin transition in the GTCCRA register and the GTIOCnB pin transition in the GTCCRB register.
11	Set buffer value	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.
12	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
13	Set buffer value for each cycle	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.

Note: n: 0 to 9
m: A, B
Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnm pin output enable and setting for a compare match value.

21.3.3.2 Saw-Wave PWM Mode 2

The saw-wave PWM mode 2 is a mode in which the GTCNT counter is operated as a saw wave by up-counting without using the GTPR register, and the PWM waveform is output by the compare match of the GTCCRA and GTCCRB registers. The pin output level can be selected from low output, high output, or toggle output separately for a compare match according to the GTIOR register setting.

The GTIOCnA pin is used as an output pin. Use the GTIOR.GTIOB[1:0] bits for setting the GTIOCnA pin output at a compare match of the GTCCRB register.

When a counter clear occurs due to the GTCNT counter clearing source selected in the GTCSR register, this is handled at the end of cycle and PWM output operation at the end of the cycle selected with the GTIOR.GTIOA[3:2] bits is performed. If a counter clear (at the end of cycle) conflicts with a PWM output change due to a GTCCRx (x = A, B) register compare match, PWM output operation is performed at the end of cycle (in the case of the GTIOR.OxEOCD bit = 0) or the PWM output is retained (in the case of GTIOR.OxEOCD bit = 1).

Figure 21.40 to Figure 21.42 shows an example of saw-wave PWM mode 2 operation. Table 21.25 shows an example for setting saw-wave PWM mode 2.

Table 21.24 设置锯齿波PWM模式1(2of2)的示例

No.	步骤名称	Description
8	启用GTIOCnm引脚输出*1	通过GTIOR寄存器中的OAE和OBE位设置使能GTIOCnm引脚输出。
9	设置缓冲操作	使用GTBER寄存器中的CCRA[1:0]和CCRB[1:0]位设置缓冲区操作。在图21.39中，CCRA[1:0]=01b和CCRB[1:0]=01b。
10	设置比较匹配值*1	设置GTCCRA寄存器中的GTIOCnA引脚转换和GTIOCnB引脚转换 GTCCRB register.
11	设置缓冲区值	对于缓冲器操作，分别在GTCCRC和GTCCRE寄存器中的当前周期之后的1个周期内设置GTIOCnA和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF寄存器中的当前周期之后的2个周期内设置GTIOCnA和GTIOCnB引脚转换。
12	开始计数操作	将GTCR.CST位设置为1以启动计数操作。
13	为每个周期设置缓冲区值	对于缓冲器操作，分别在GTCCRC和GTCCRE寄存器中的当前周期之后的1个周期内设置GTIOCnA和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF寄存器中的当前周期之后的2个周期内设置GTIOCnA和GTIOCnB引脚转换。

Note: n: 0 to 9
m: A, B
注1.使用PWM延迟产生电路时，更改GTIOCnm引脚输出使能设置和比较匹配值设置的顺序。

21.3.3.2 Saw-Wave PWM Mode 2

锯齿波PWM模式2是一种模式，其中GTCNT计数器通过递增计数而不使用GTPR寄存器作为锯齿波操作，并且通过GTCCRA和GTCCRB寄存器的比较匹配输出PWM波形。引脚输出电平可以根据GTIOR寄存器设置分别从低输出、高输出或切换输出中选择，以进行比较匹配。

GTIOCnA引脚用作输出引脚。使用GTIOR.GTIOB[1:0]位在GTCCRB寄存器的比较匹配时设置GTIOCnA引脚输出。

当由于在GTCSR寄存器中选择的GTCNT计数器清除源而发生计数器清除时，这将在周期结束时进行处理，并在使用GTIOR.GTIOA[3:2]位选择的周期结束时执行PWM输出操作.如果由于GTCCRx(x=A B)寄存器比较匹配而导致计数器清零（在周期结束时）与PWM输出变化冲突，则在周期结束时执行PWM输出操作（在GTIOR的情况下）。OxEOCD位=0）或保持PWM输出（在GTIOR.OxEOCD位=1的情况下）。

图21.40至图21.42显示了锯齿波PWM模式2操作的示例。表21.25显示了设置锯齿波PWM模式2的示例。

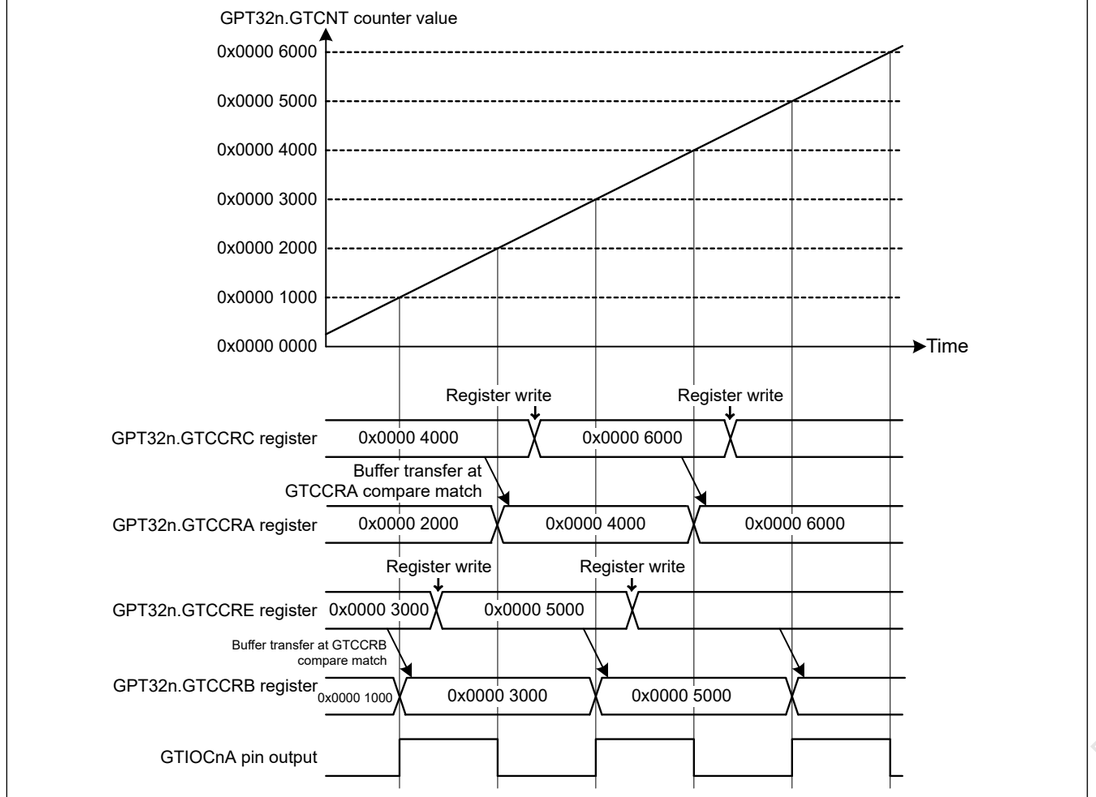


Figure 21.40 Example of Saw-Wave PWM Mode 2 Operation (Low Output at GTCCRA Register Compare Match, High Output at GTCCRB Register Compare Match, Single Buffer Operation, No Clear Setting) (n = 4 to 9)

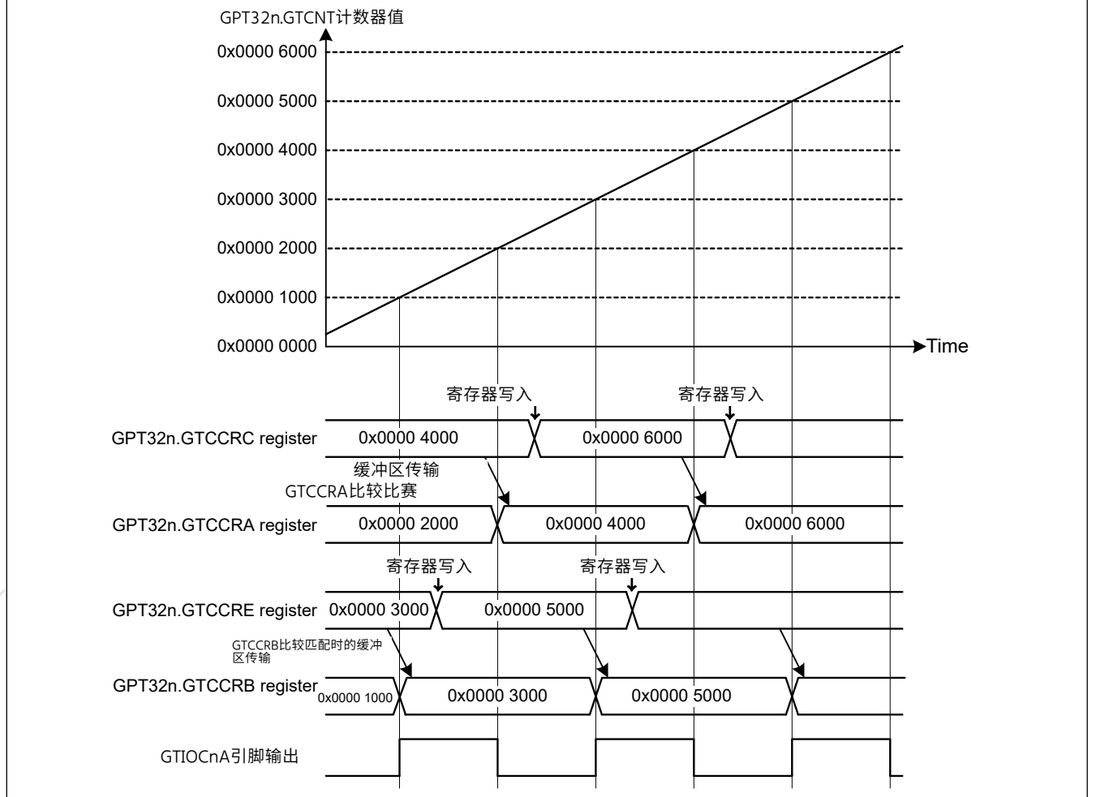


Figure 21.40 锯波PWM模式2操作示例（GTCCRA寄存器比较的低输出匹配，GTCCRB寄存器比较匹配的高输出，单缓冲器操作，无清除 Setting) (n = 4 to 9)

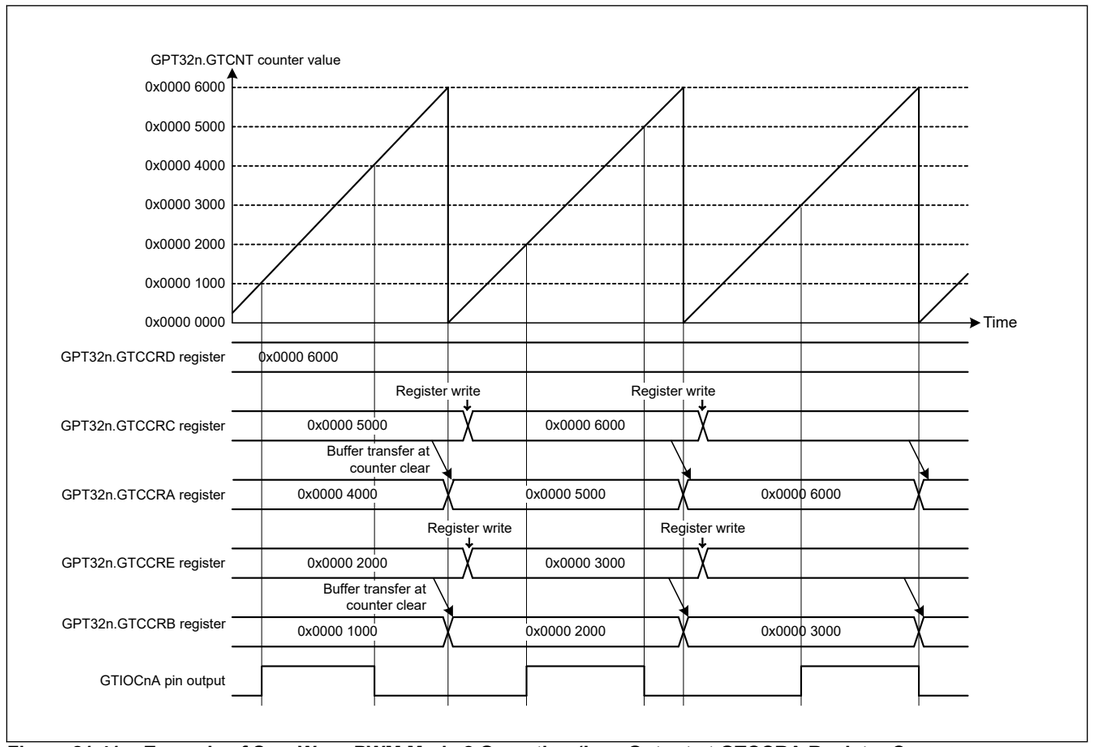


Figure 21.41 Example of Saw-Wave PWM Mode 2 Operation (Low Output at GTCCRA Register Compare Match, High Output at GTCCRB Register Compare Match, Low Output at the End of Cycle, Single Buffer Operation, Cleared at GTCCRD Register Compare Match, GTIOR.OAEOCD Bit = 0) (n = 4 to 9)

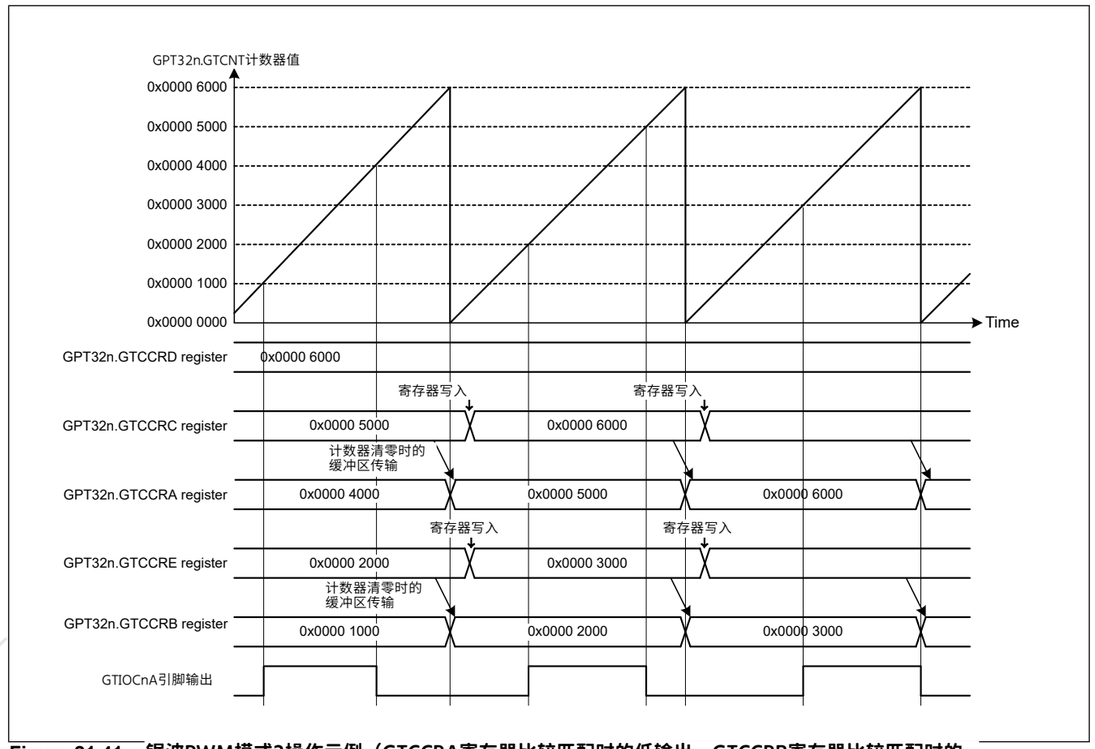


Figure 21.41 锯波PWM模式2操作示例（GTCCRA寄存器比较匹配时的低输出，GTCCRB寄存器比较匹配时的高输出，周期结束时的低输出，单缓冲区操作，在GTCCRD寄存器比较匹配时清零，GTIOR.OAEOCD位=0)(n=4到9)

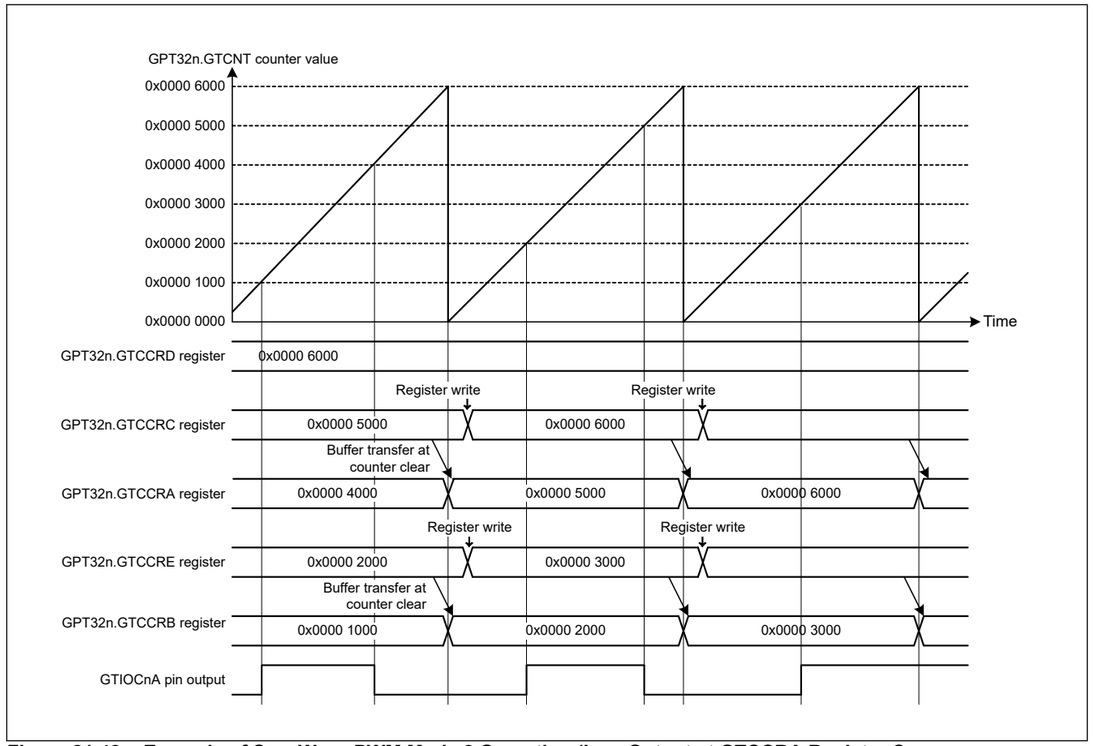


Figure 21.42 Example of Saw-Wave PWM Mode 2 Operation (Low Output at GTCCRA Register Compare Match, High Output at GTCCRB Register Compare Match, Low Output at the End of Cycle, Single Buffer Operation, Cleared at GTCCRD Register Compare Match, GTIOR.OAEOCD Bit =1) (n = 4 to 9)

Table 21.25 Example for Setting Saw-wave PWM mode 2

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[3:0]. (In Figure 21.40 to Figure 21.42, 0010b (saw-wave PWM mode 2) is set.)
2	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits.
3	Set initial value for counter	Set the initial value in the GTCNT counter.
4	Set GTIOCnA pin function	Set the GTIOCnA pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. (In Figure 21.40 to Figure 21.42, GTIOA[4:0] = 00001b and GTIOB[1:0] = 10b.)
5	Enable GTIOCnA pin output*1	Set to enable the GTIOCnA pin output with OAE in GTIOR.
6	Set buffer operation	Set buffer operation with CCRA[1:0] and CCRB[1:0] bits in GTBER (In Figure 21.40 to Figure 21.42, CCRA[1:0] = 01b and CCRB[1:0] = 01b.)
7	Set compare match value*1	Set the GTIOCnA pin changing point in GTCCRA and GTCCRB.
8	Set buffer value	For buffer operation, set the GTCCRA register value and the GTCCRB register value which used in one cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTCCRA register value and the GTCCRB register value which used in two cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.
9	Start count operation	Set GTCR.CST to 1 to start count operation.
10	Set buffer value of each cycle	For buffer operation, set the GTCCRA register value and the GTCCRB register value which used in one cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTCCRA register value and the GTCCRB register value which used in two cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.

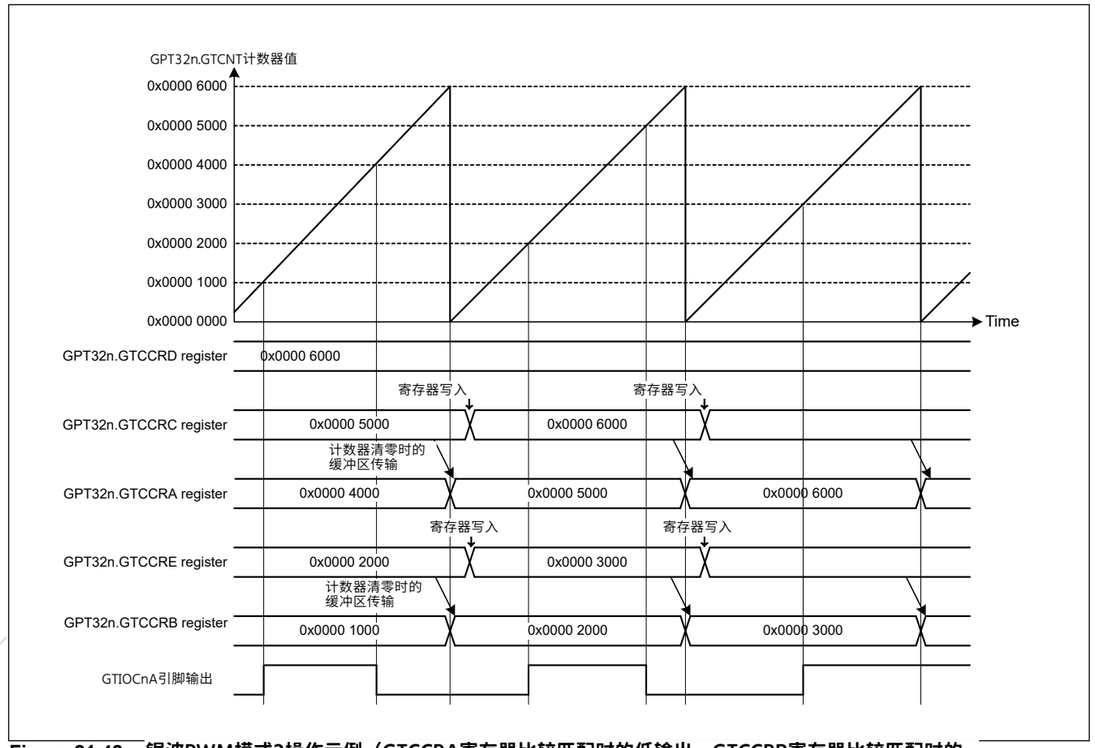


Figure 21.42 锯波PWM模式2操作示例（GTCCRA寄存器比较匹配时的低输出，GTCCRB寄存器比较匹配时的高输出，周期结束时的低输出，单缓冲器操作，在GTCCRD寄存器比较匹配时清零，GTIOR.OAEOCD位=1)(n=4到9)

Table 21.25 设置锯齿波PWM模式2的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[3:0]设置操作模式。（在图21.40到图21.42中，设置了0010b（锯齿波PWM模式2）。）
2	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
3	设置计数器的初始值	在GTCNT计数器中设置初始值。
4	设置GTIOCnA引脚功能	通过GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnA引脚功能。（在图21.40到图21.42中，GTIOA[4:0]=00001b和GTIOB[1:0]=10b。）
5	启用GTIOCnA引脚输出*1	通过GTIOR中的OAE设置以启用GTIOCnA引脚输出。
6	设置缓冲操作	使用GTBER中的CCRA[1:0]和CCRB[1:0]位设置缓冲区操作（在图21.40到图21.42中，CCRA[1:0]=01b和CCRB[1:0]=01b。）
7	设置比较匹配值*1	在GTCCRA和GTCCRB中设置GTIOCnA引脚转换点。
8	设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE寄存器中设置当前周期后一个周期使用的GTCCRA寄存器值和GTCCRB寄存器值。对于双缓冲操作，还要分别在GTCCRD和GTCCRF寄存器中设置当前周期后两个周期使用的GTCCRA寄存器值和GTCCRB寄存器值。
9	开始计数操作	将GTCR.CST设置为1以启动计数操作。
10	设置每个周期的缓冲值	对于缓冲操作，分别在GTCCRC和GTCCRE寄存器中设置当前周期后一个周期使用的GTCCRA寄存器值和GTCCRB寄存器值。对于双缓冲操作，还要分别在GTCCRD和GTCCRF寄存器中设置当前周期后两个周期使用的GTCCRA寄存器值和GTCCRB寄存器值。

Note: n: 4 to 9
Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnA pin output enable and setting for a compare match value.

21.3.3.3 Saw-Wave One-Shot Pulse Mode

The saw-wave one-shot pulse mode is a mode in which the cycle is set in GTPR, the GTCNT counter performs saw-wave (half-wave) operation and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 9) at a compare match of GTCCRA or GTCCRB with buffer operation fixed.

Buffer operation in saw-wave one-shot pulse mode is different from the usual buffer operation. Buffer transfer is performed from:

- GTCCRC to GTCCRA at the cycle end
- GTCCRE to GTCCRB at the cycle end
- GTCCRD to temporary register A at the cycle end
- GTCCRF to temporary register B at the cycle end
- Temporary register A to GTCCRA at a GTCCRA compare match
- Temporary register B to GTCCRB at a GTCCRB compare match.

The pin output value can be selected from low output, high output, or toggled output separately for a compare match and the cycle end according to the GTIOR setting. When the GTBER.CCRSWT bit is set to 1 while count operation is stopped, the buffer is transferred forcibly from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B. By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

When the GTBER.DBRTECm (m = A, B) bit is set to 1, transfer from an intermediate buffer to the GTCCRm register is repeated on a cyclic basis with using the temporary register x (x = C, E) and temporary register m which operate as intermediate buffers for the GTCCRx and GTCCRm registers, respectively, even while buffer transfer is disabled (repeated double buffer operation function during disabling of buffer transfer). For details, refer to section 21.8.2.2. Repeated Double-Buffered Operation When Disabling GTCCR Buffer Transfer.

Figure 21.43 shows an example of saw-wave one-shot pulse mode operation, and Table 21.26 shows an example for setting saw-wave one-shot pulse mode.

Note: n: 4 to 9
注1.使用PWM延迟产生电路时，更改GTIOCnA引脚输出使能设置和比较匹配值设置的顺序。

21.3.3.3 锯波单发脉冲模式

锯齿波单次脉冲模式是在GTPR中设置周期，GTCNT计数器执行锯齿波（半波）操作并将PWM波形输出到GTIOCnA或GTIOCnB引脚（n=0到9)在GTCCRA或GTCCRB的比较匹配中，缓冲区操作固定。

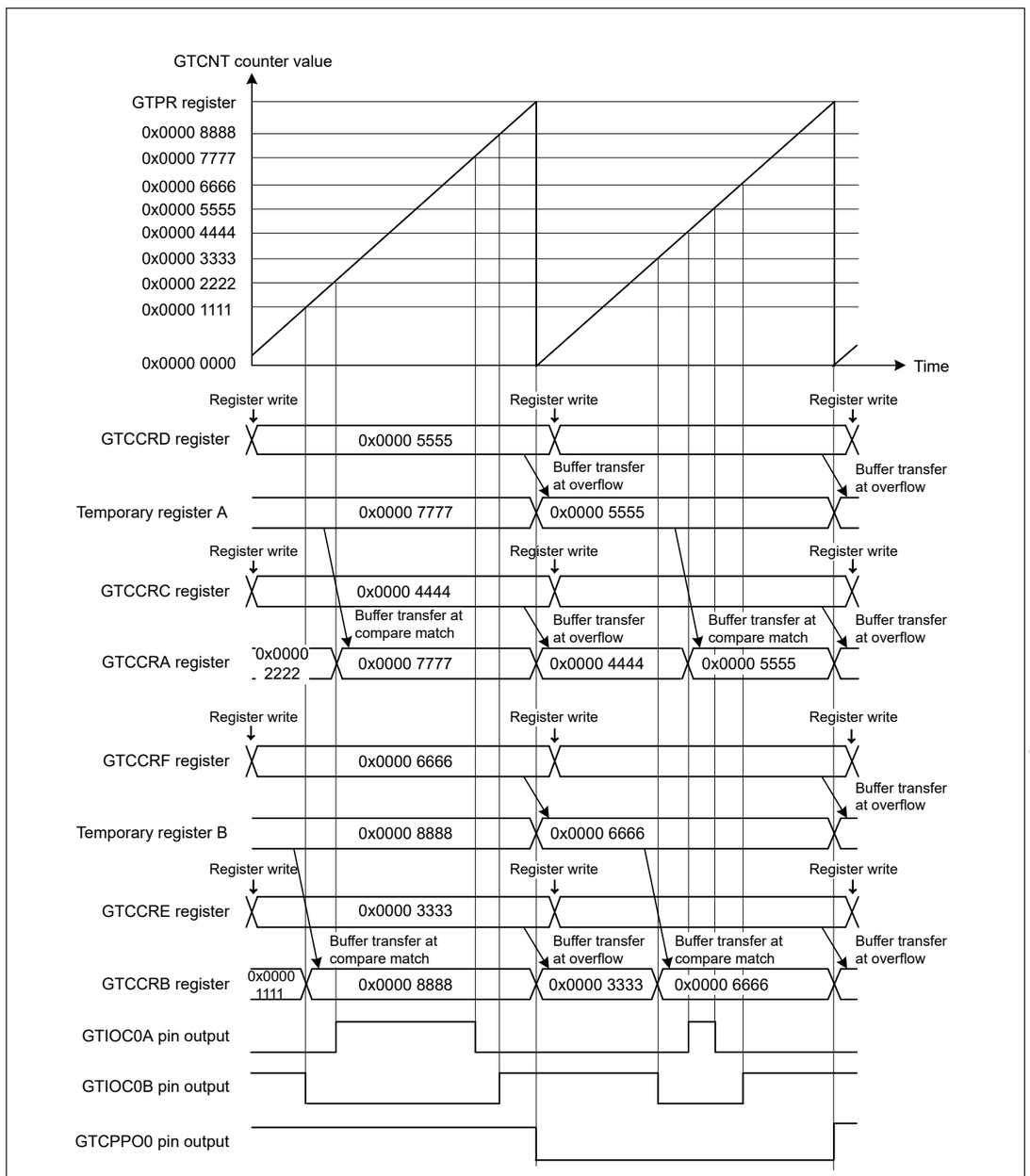
锯波单次脉冲模式中的缓冲操作不同于通常的缓冲操作。缓冲区传输从以下位置执行：

●GTCCRC到GTCCRA在循环结束
●循环结束时GTCCRE到GTCCRB
●GTCCRD在循环结束时到临时寄存器A
●GTCCRF在循环结束时到临时寄存器B
●GTCCRA比较匹配时到GTCCRA的临时寄存器A
●GTCCRB比较匹配时的临时寄存器B到GTCCRB。

引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，以进行比较匹配和循环结束。当计数操作停止时GTBER.CCRSWT位设置为1时，缓冲区被强制从GTCCRD寄存器传送到临时寄存器A，并从GTCCRF寄存器传送到临时寄存器B。通过设置GTDTCR、GTDVU和GTDVD，比较具有死区时间的负相位波形的匹配值可以自动设置为GTCCRB。

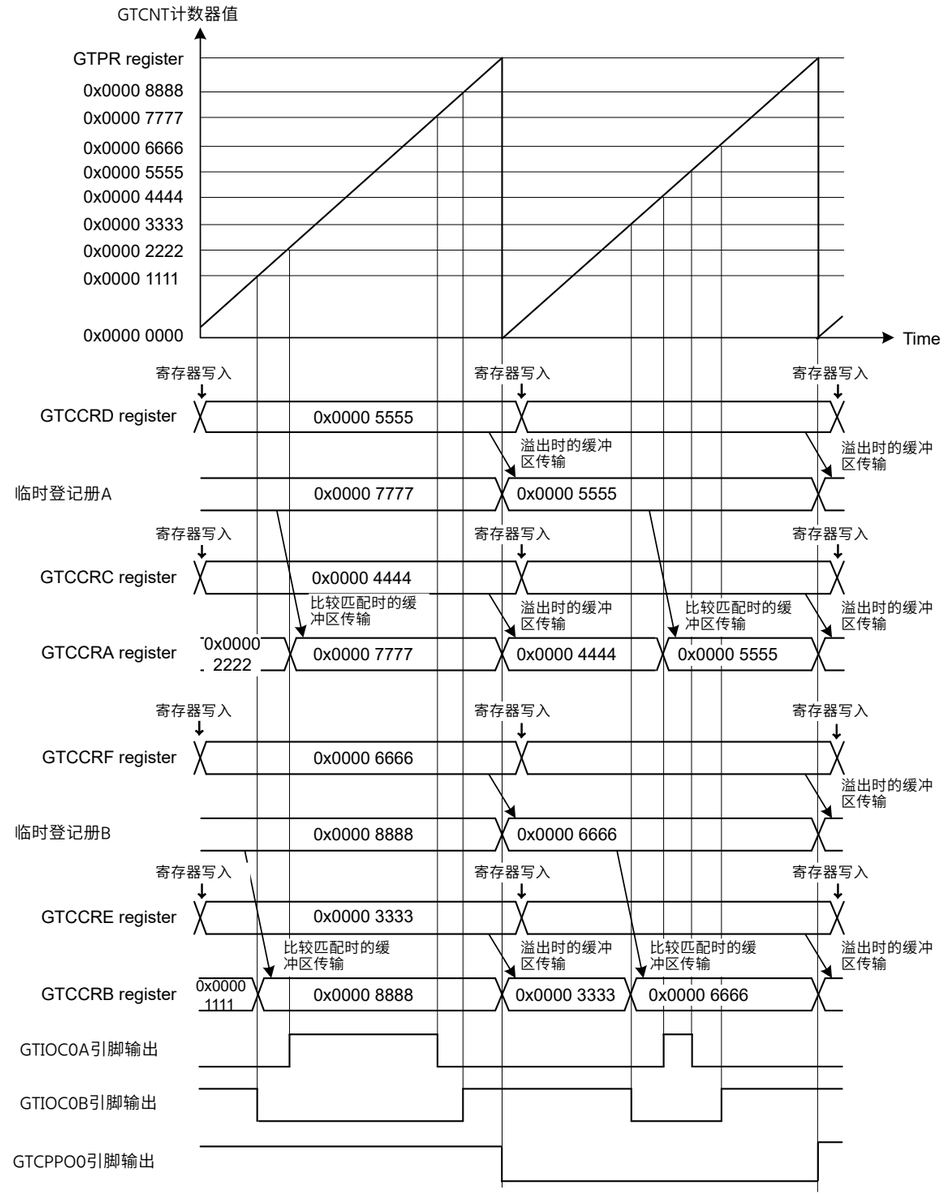
当GTBER.DBRTECm(m=A B)位设置为1时，使用临时寄存器x(x=C E)和临时寄存器m循环重复从中间缓冲区到GTCCRm寄存器的传输它们分别作为GTCCRx和GTCCRm寄存器的中间缓冲区运行，即使在禁用缓冲区传输时也是如此（在禁用缓冲区传输期间重复双缓冲区操作功能）。有关详细信息，请参阅第21.8.2.2节。禁用GTCCR缓冲区传输时重复双缓冲操作。

图21.43显示了锯齿波单次脉冲模式操作的示例，表21.26显示了设置锯齿波单次脉冲模式的示例。



Note: The base address of registers are the same.

Figure 21.43 Example of saw-wave one-shot pulse mode operation with up-counting, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB compare match, output retained at cycle end, and GTIOR.PSYE = 1



Note: 寄存器的基地址相同。

Figure 21.43 具有递增计数、低输出的锯齿波单次脉冲模式操作示例 GTIOCnA引脚和GTIOCnB引脚在计数开始时的高电平输出，输出在GTCCRA切换 GTCCRB比较匹配，在循环结束时保留输出，并且GTIOR.PSYE=1

Table 21.26 Example setting for saw-wave one-shot pulse mode

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.43, 001b (saw-wave one-shot pulse mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.43, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 21.43, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
7	Enable GTCPPOn pin output	Set to enable/disable the GTCPPOn pin output with the PSYE bit in the GTIOR register.
8	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
9	Set compare match value*1	Set the GTIOCnA pin transition immediately after the count start in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.
10	Set forcible buffer transfer*1	Set the GTBER.CCRSWT bit to 1 to transfer buffer register data forcibly.
11	Set buffer value	For buffer operation, set the GTIOCnA pin transition in one cycle after the current cycle in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.
12	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
13	Set buffer value for each cycle	For buffer operation, set the GTIOCnA pin transition in one cycle after the current cycle in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.

Note: n: 0 to 9
m: A, B
Note 1. When using PWM Delay Generation circuit, change the order of Enable GTIOCnm pin output and Set compare match value + Set forcible buffer transfer.

21.3.3.4 Triangle-Wave PWM Mode 1 (32-Bit Transfer at Trough)

The triangle-wave PWM mode 1 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 9) when a GTCCRA or GTCCRB compare match occurs. Buffer transfer is performed at the trough. The pin output value can be selected from low output, high output, or toggled output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 21.44 shows an example of a triangle-wave PWM mode 1 operation, and Table 21.27 shows an example for setting a triangle-wave PWM mode 1.

Table 21.26 锯波单发脉冲模式设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.43中，设置了001b（锯波单次脉冲模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.43中，在GTUDDTYC[1:0]位中设置11b后，在GTUDDTYC[1:0]位中设置01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	在GTPR寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR寄存器中的GTIOA[4:0]和GTIOB[4:0]位设置GTIOCnm引脚功能。 在图21.43中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
7	启用GTCPPOn引脚输出	使用GTIOR寄存器中的PSYE位设置启用禁用GTCPPOn引脚输出。
8	启用GTIOCnm引脚输出*1	通过GTIOR寄存器中的OAE和OBE位设置使能GTIOCnm引脚输出。
9	设置比较匹配值*1	在GTCCRC和GTCCRD寄存器中的计数开始以及GTCCRE和GTCCRF寄存器中的GTIOCnB引脚转换后立即设置GTIOCnA引脚转换。
10	设置强制缓冲传输*1	将GTBER.CCRSWT位设置为1以强制传输缓冲寄存器数据。
11	设置缓冲区值	对于缓冲操作，设置GTIOCnA引脚转换在当前周期后的一个周期内GTCCRC和GTCCRD寄存器以及GTCCRE和GTCCRF寄存器中的GTIOCnB引脚转换。
12	开始计数操作	将GTCR.CST位设置为1以启动计数操作。
13	为每个周期设置缓冲区值	对于缓冲操作，设置GTIOCnA引脚转换在当前周期后的一个周期内GTCCRC和GTCCRD寄存器以及GTCCRE和GTCCRF寄存器中的GTIOCnB引脚转换。

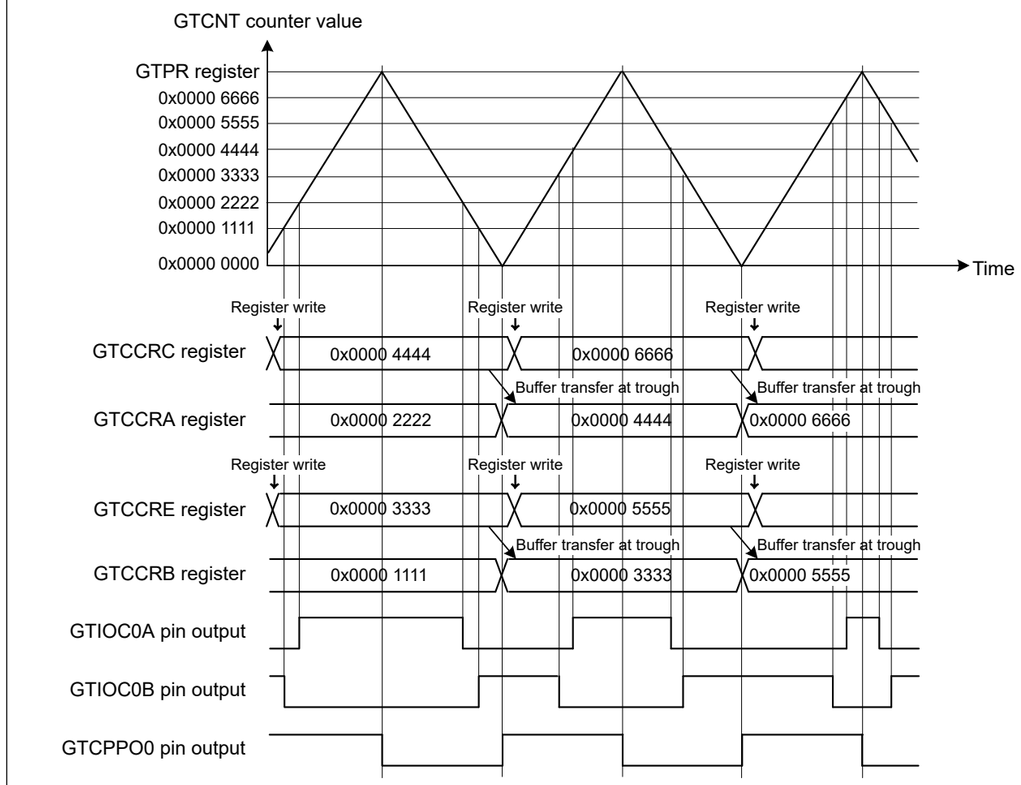
Note: n: 0 to 9
m: A, B
注1.当使用PWM延迟产生电路时，改变EnableGTIOCnmpinoutput和Setcomparematchvalue+Setforceforcebuffertransfer的顺序。

21.3.3.4 三角波PWM模式1（波谷32位传输）

三角波PWM模式1是在GTPR中设定周期的模式。GTCNT计数器执行三角波（全波）操作，当发生GTCCRA或GTCCRB比较匹配时，PWM波形输出到GTIOCnA或GTIOCnB引脚（n=0至9）。在槽中进行缓冲转移。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

通过设置GTDTCR、GTDVU和GTDVD，可以自动将带死区时间的负相位波形的比较匹配值设置为GTCCRB。

图21.44显示了三角波PWM模式1操作的示例，表21.27显示了设置三角波PWM模式1的示例。

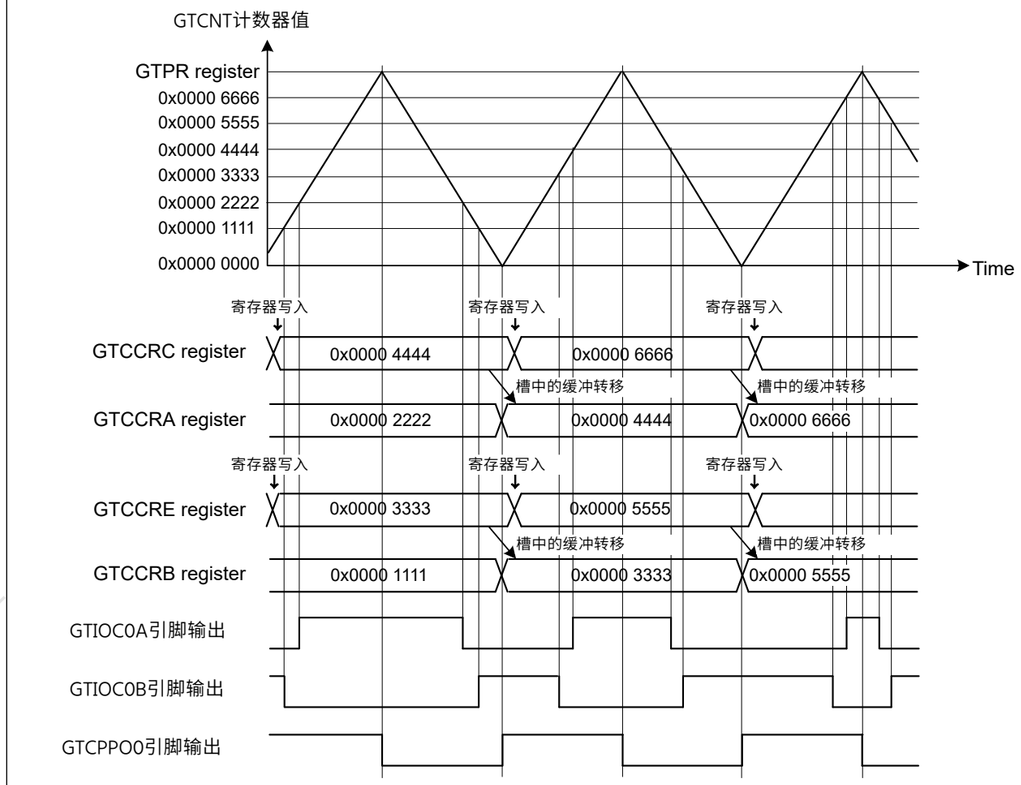


Note: The base address of registers are the same.

Figure 21.44 Example of triangle-wave PWM mode 1 operation with buffer operation, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB register compare match, output retained at cycle end, and GTIOR.PSYE = 1

Table 21.27 Example setting for triangle-wave PWM mode 1 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.44, 100b (triangle-wave PWM mode 1) is set.
2	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
3	Set cycle	Set the cycle in the GTPR register.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 21.44, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTCPPOn pin output	Set to enable/disable the GTCPPOn pin output with the PSYE bit in the GTIOR register.
7	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set buffer operation	Set buffer operation with the CCRA[1:0] and CCRB[1:0] bits in the GTBER register. In Figure 21.44, CCRA[1:0] = 01b and CCRB[1:0] = 01b.
9	Set compare match value*1	Set the GTIOCnA and GTIOCnB pins transitions in the GTCCRA and GTCCRB registers, respectively.



Note: 寄存器的基地址相同。

Figure 21.44 带缓冲操作的三角波PWM模式1操作示例，从GTIOCnA引脚和GTIOCnB引脚在计数开始时的高电平输出，输出在GTCCRA切换GTCCRB寄存器比较匹配，输出在周期结束时保留，并且GTIOR.PSYE=1

Table 21.27 三角波PWM模式1的设置示例（1of2）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.44中，设置了100b（三角波PWM模式1）。
2	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
3	设置周期	在GTPR寄存器中设置周期。
4	设置计数器的初始值	在GTCNT计数器中设置初始值。
5	设置GTIOCnm引脚功能	使用GTIOR寄存器中的GTIOA[4:0]和GTIOB[4:0]位设置GTIOCnm引脚功能。 在图21.44中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
6	启用GTCPPOn引脚输出	使用GTIOR寄存器中的PSYE位设置启用禁用GTCPPOn引脚输出。
7	启用GTIOCnm引脚输出*1	通过GTIOR寄存器中的OAE和OBE位设置使能GTIOCnm引脚输出。
8	设置缓冲操作	使用GTBER寄存器中的CCRA[1:0]和CCRB[1:0]位设置缓冲区操作。 在图21.44中，CCRA[1:0]=01b和CCRB[1:0]=01b。
9	设置比较匹配值*1	分别在GTCCRA和GTCCRB寄存器中设置GTIOCnA和GTIOCnB引脚转换。

Table 21.27 Example setting for triangle-wave PWM mode 1 (2 of 2)

No.	Step Name	Description
10	Set buffer value	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.
11	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
12	Set buffer value for each cycle	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.

Note: n: 0 to 9
m: A, B
Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnm pin output enable and setting for a compare match value.

21.3.3.5 Triangle-Wave PWM Mode 2 (32-Bit Transfer at Crest and Trough)

Similarly to triangle-wave PWM mode 1, in triangle-wave PWM mode 2 the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 9) when a GTCCRA or GTCCRB compare match occurs. The buffer transfer is performed at both crests and troughs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 21.45 shows an example of triangle-wave PWM mode 2 operation, and Table 21.28 shows an example for setting triangle-wave PWM mode 2.

Table 21.27 三角波PWM模式1(2of2)的示例设置

No.	步骤名称	Description
10	设置缓冲区值	对于缓冲器操作，分别在GTCCRC和GTCCRE寄存器中的当前周期之后的1个周期内设置GTIOCnA和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF寄存器中的当前周期之后的2个周期内设置GTIOCnA和GTIOCnB引脚转换。
11	开始计数操作	将GTCR.CST位设置为1以启动计数操作。
12	为每个周期设置缓冲区值	对于缓冲器操作，分别在GTCCRC和GTCCRE寄存器中的当前周期之后的1个周期内设置GTIOCnA和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF寄存器中的当前周期之后的2个周期内设置GTIOCnA和GTIOCnB引脚转换。

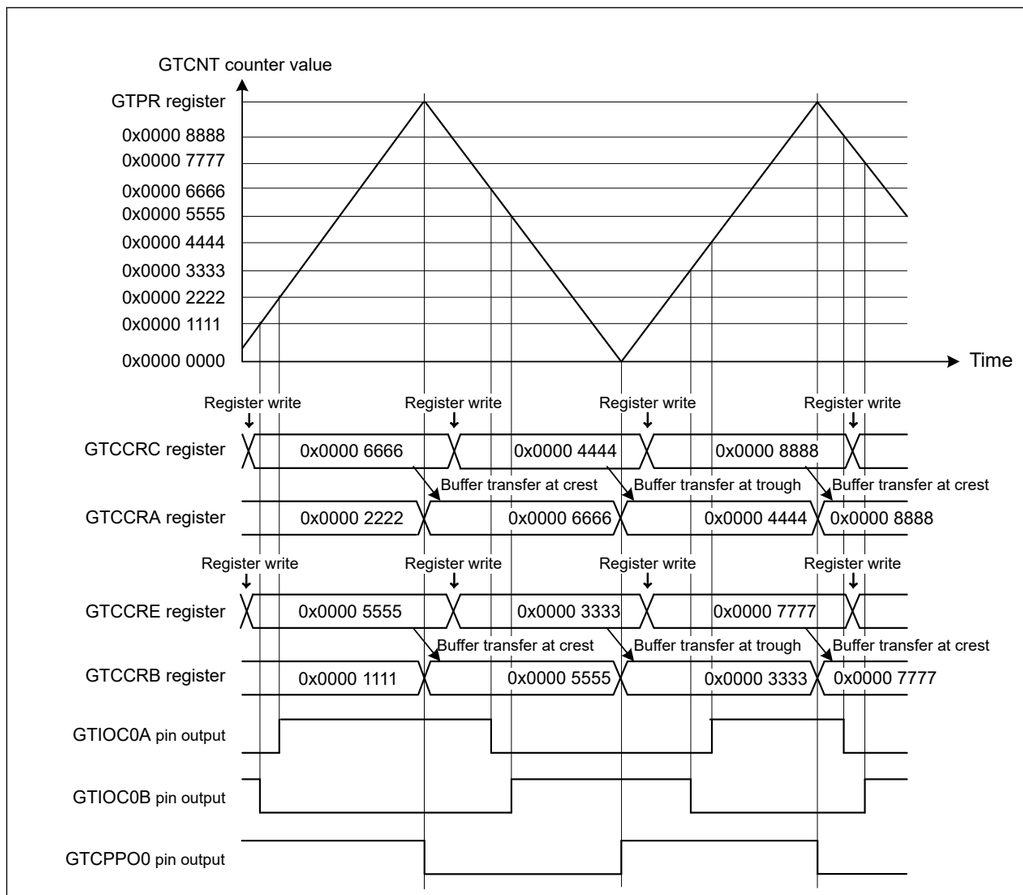
Note: n: 0 to 9
m: A, B
注1.使用PWM延迟产生电路时，更改GTIOCnm引脚输出使能设置和比较匹配值设置的顺序。

21.3.3.5 三角波PWM模式2（波峰和波谷的32位传输）

与三角波PWM模式1类似，在三角波PWM模式2中，周期在GTPR中设置。GTCNT计数器执行三角波（全波）操作，当发生GTCCRA或GTCCRB比较匹配时，PWM波形输出到GTIOCnA或GTIOCnB引脚（n=0至9）。缓冲转移在波峰和波谷进行。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

通过设置GTDTCR、GTDVU和GTDVD，可以自动将带死区时间的负相位波形的比较匹配值设置为GTCCRB。

图21.45显示了三角波PWM模式2操作的示例，表21.28显示了设置三角波PWM模式2的示例。

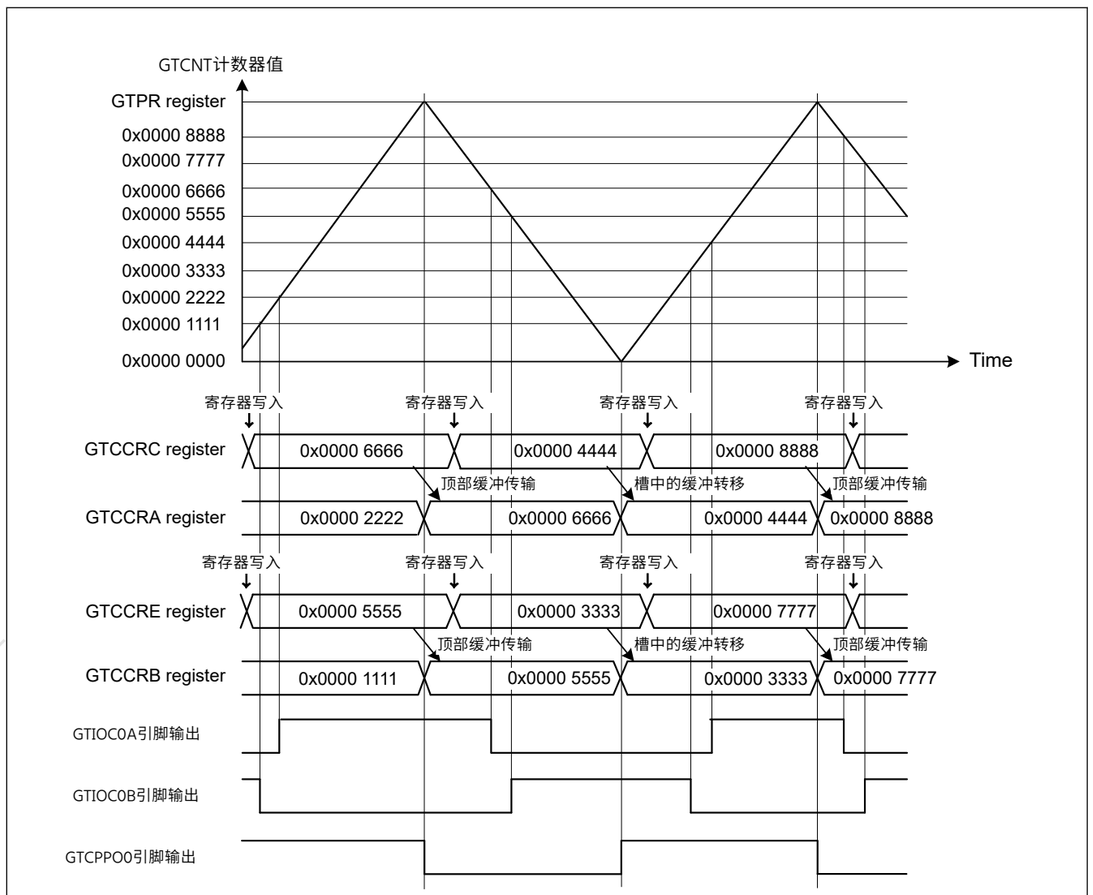


Note: The base address of registers are the same.

Figure 21.45 Example of triangle-wave PWM mode 2 operation with buffer operation, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB compare match, output retained at cycle end, and GTIOR.PSYE = 1

Table 21.28 Example for setting triangle-wave PWM mode 2 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.45, 101b (triangle-wave PWM mode 2) is set.
2	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
3	Set cycle	Set the cycle in the GTPR register.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 21.45, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTCPPOn pin output	Set to enable/disable the GTCPPOn pin output with the PSYE bit in the GTIOR register.
7	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set buffer operation	Set buffer operation with the CCRA[1:0] and CCRB[1:0] bits in the GTBER register. In Figure 21.45, CCRA[1:0] = 01b and CCRB[1:0] = 01b.
9	Set compare match value*1	Set the GTIOCnA and GTIOCnB pins transitions in the GTCCRA and GTCCRB registers, respectively.



Note: 寄存器的基地址相同。

Figure 21.45 带缓冲操作的三角波PWM模式2操作示例，从GTIOCnA引脚和GTIOCnB引脚在计数开始时的高电平输出，输出在GTCCRA切换GTCCRB比较匹配，在循环结束时保留输出，并且GTIOR.PSYE=1

Table 21.28 设置三角波PWM模式2的示例（1of2）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.45中，设置了101b（三角波PWM模式2）。
2	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
3	设置周期	在GTPR寄存器中设置周期。
4	设置计数器的初始值	在GTCNT计数器中设置初始值。
5	设置GTIOCnm引脚功能	使用GTIOR寄存器中的GTIOA[4:0]和GTIOB[4:0]位设置GTIOCnm引脚功能。 在图21.45中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
6	启用GTCPPOn引脚输出	使用GTIOR寄存器中的PSYE位设置启用禁用GTCPPOn引脚输出。
7	启用GTIOCnm引脚输出*1	通过GTIOR寄存器中的OAE和OBE位设置使能GTIOCnm引脚输出。
8	设置缓冲操作	使用GTBER寄存器中的CCRA[1:0]和CCRB[1:0]位设置缓冲区操作。 在图21.45中，CCRA[1:0]=01b和CCRB[1:0]=01b。
9	设置比较匹配值*1	分别在GTCCRA和GTCCRB寄存器中设置GTIOCnA和GTIOCnB引脚转换。

Table 21.28 Example for setting triangle-wave PWM mode 2 (2 of 2)

No.	Step Name	Description
10	Set buffer value	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in half cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRD and GTCCRF registers, respectively.
11	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
12	Set buffer value for each half cycle	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in half cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in GTCCRD and GTCCRF registers, respectively.

Note: n: 0 to 9
m: A, B
Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnm pin output enable and setting for a compare match value.

21.3.3.6 Triangle-Wave PWM Mode 3 (64-Bit Transfer at Trough)

The triangle-wave PWM mode 3 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 9) at a compare match of GTCCRA or GTCCRB with buffer operation fixed. Buffer operation in triangle-wave PWM mode 3 is different from the usual buffer operation. Buffer transfer is performed from the following:

- GTCCRC to GTCCRA at the trough
- GTCCRE to GTCCRB at the trough
- GTCCRD to temporary register A at the trough
- GTCCRF to temporary register B at the trough
- Temporary register A to GTCCRA at the crest
- Temporary register B to GTCCRB at the crest.

The pin output value can be selected from low output, high output, or toggled output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 21.46 shows an example of triangle-wave PWM mode 3 operation, and Table 21.29 shows an example for setting triangle-wave PWM mode 3.

Table 21.28 设置三角波PWM模式2的示例(2of2)

No.	步骤名称	Description
10	设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE寄存器中设置GTIOCnA和GTIOCnB引脚在当前周期之后的半个周期内转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF寄存器中的当前周期之后的1个周期内设置GTIOCnA和GTIOCnB引脚转换。
11	开始计数操作	将GTCR.CST位设置为1以启动计数操作。
12	为每个半周期设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE寄存器中设置GTIOCnA和GTIOCnB引脚在当前周期之后的半个周期内转换。对于双缓冲操作，还分别在GTCCRD和GTCCRF寄存器中的当前周期之后的1个周期内设置GTIOCnA和GTIOCnB引脚转换。

Note: n: 0 to 9
m: A, B
注1.使用PWM延迟产生电路时，更改GTIOCnm引脚输出使能设置和比较匹配值设置的顺序。

21.3.3.6 三角波PWM模式3（波谷64位传输）

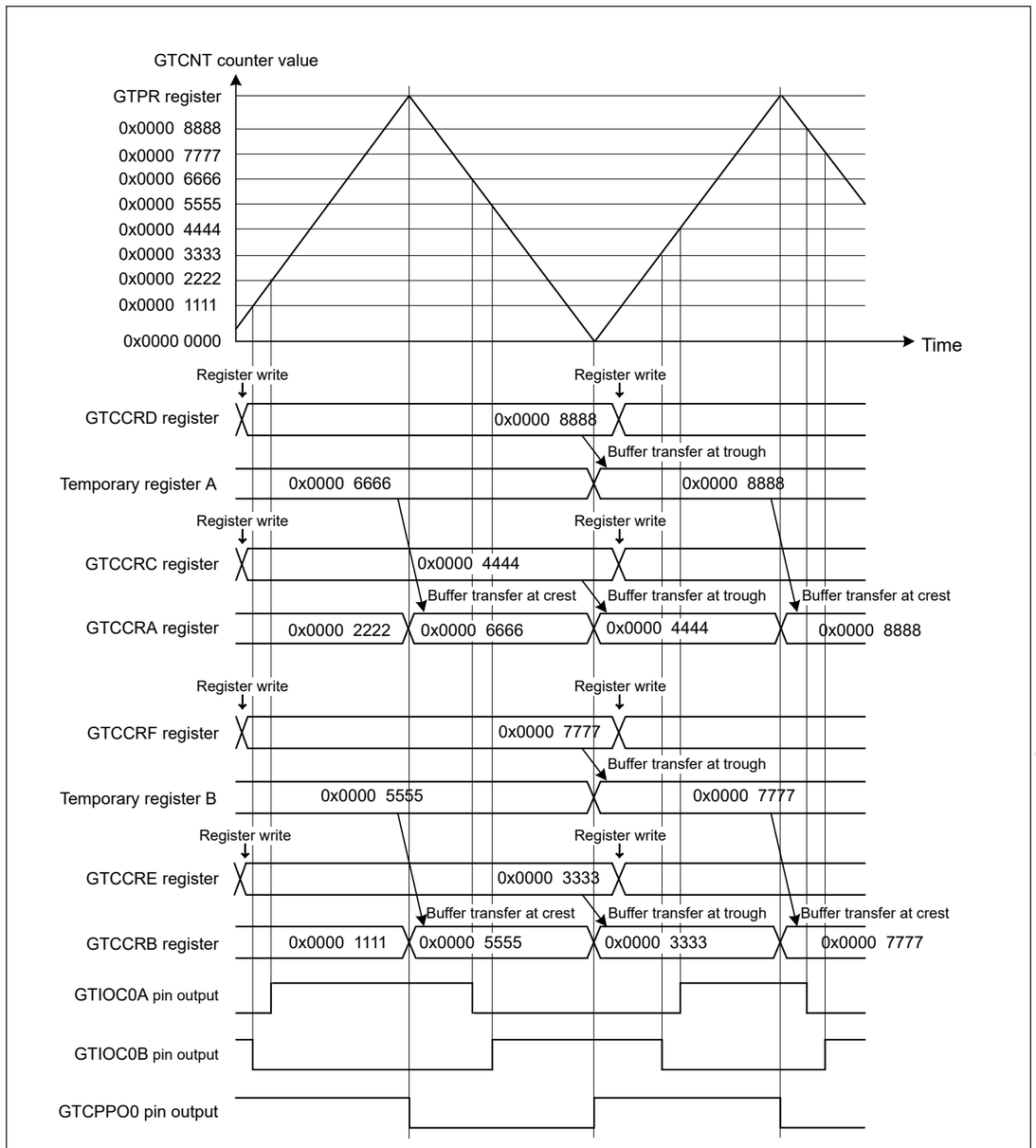
三角波PWM模式3是在GTPR中设定周期的模式。GTCNT计数器执行三角波（全波）操作，并且在固定缓冲器操作的GTCCRA或GTCCRB比较匹配时将PWM波形输出到GTIOCnA或GTIOCnB引脚（n=0至9）。三角波PWM模式3中的缓冲操作与通常的缓冲操作不同。缓冲区传输从以下位置执行：

●GTCCRC到GTCCRA处于低谷
●GTCCRE至GTCCRB处于低谷
●GTCCRD到谷底临时寄存器A
●GTCCRF到波谷的临时寄存器B
●顶部为GTCCRA的临时寄存器A
●在顶部的GTCCRB临时寄存器B。

引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

通过设置GTDTCR、GTDVU和GTDVD，可以自动将带死区时间的负相位波形的比较匹配值设置为GTCCRB。

图21.46显示了三角波PWM模式3操作的示例，表21.29显示了设置三角波PWM模式3的示例。

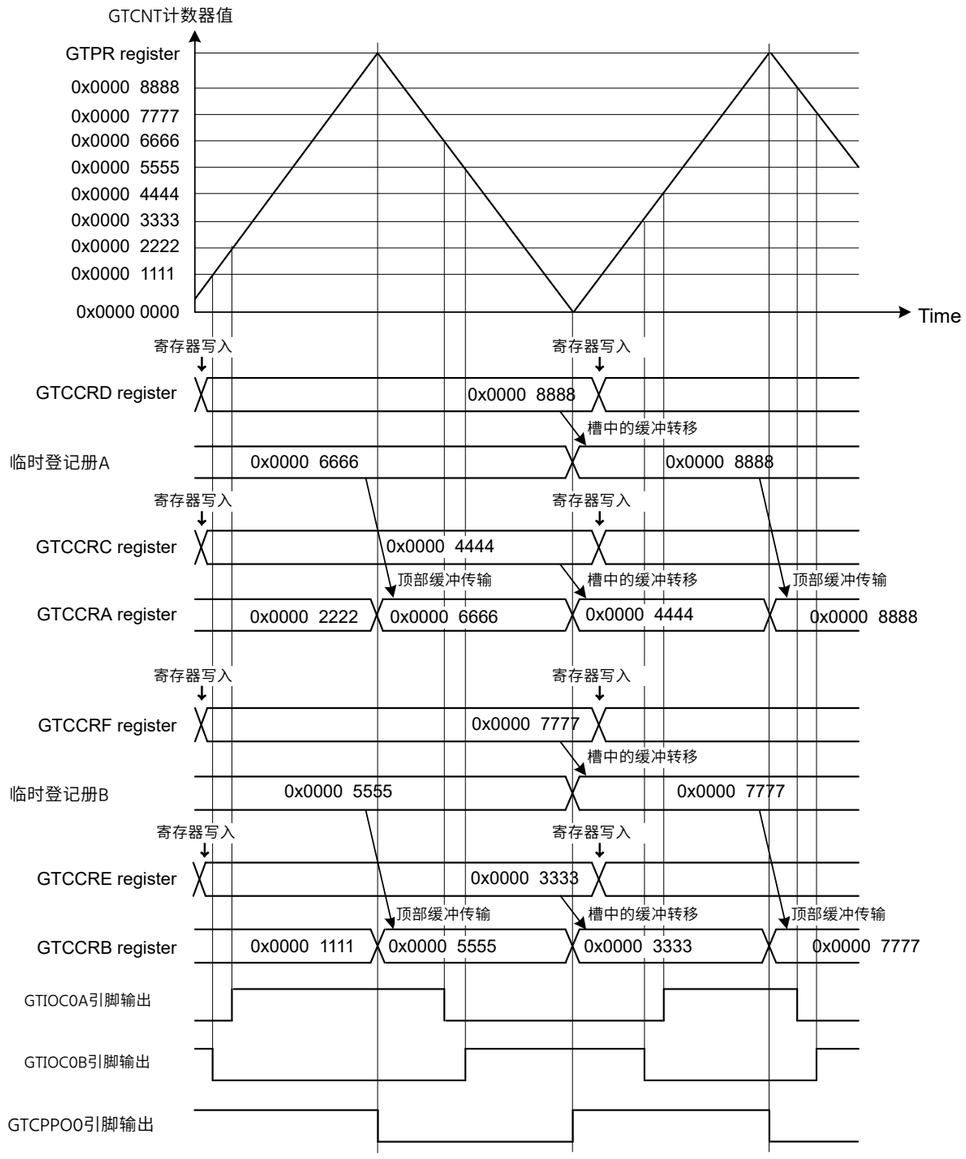


Note: The base address of registers are the same.

Figure 21.46 Example of triangle-wave PWM mode 3 operation with low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/GTCCRB compare match, output retained at cycle end, and GTIOR.PSYE = 1

Table 21.29 Example setting for triangle-wave PWM mode 3 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.46, 110b (triangle-wave PWM mode 3) is set.



Note: 寄存器的基地址相同。

Figure 21.46 三角波PWM模式3操作示例，计数开始时GTIOCnA引脚输出低电平，GTIOCnB引脚输出高电平，在GTCCRAGTCCRB比较匹配时切换输出，在周期结束时保持输出，GTIOR.PSYE=1

Table 21.29 三角波PWM模式3的设置示例（1of2）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.46中，设置了110b（三角波PWM模式3）。

Table 21.29 Example setting for triangle-wave PWM mode 3 (2 of 2)

No.	Step Name	Description
2	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
3	Set cycle	Set the cycle in the GTPR register.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 21.46, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTCPPOn pin output	Set to enable/disable the GTCPPOn pin output with the PSYE bit in the GTIOR register.
7	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set compare match value*1	Set the GTIOCnA pin transition immediately after the count start in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.
9	Set forcible buffer transfer*1	Set the GTBER.CCRSWT bit to 1 to transfer buffer register data forcibly.
10	Set buffer value	Set the GTIOCnA pin transition in 1 cycle after the current cycle in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.
11	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
12	Set buffer value for each cycle	Set the GTIOCnA pin transition in 1 cycle after the current cycle in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.

Note: n: 0 to 9
m: A, B

Note 1. When using PWM Delay Generation circuit, change the order of Enable GTIOCnm pin output and Set compare match value + Set forcible buffer transfer.

21.3.3.7 Complementary PWM mode 1,2,3

In complementary PWM mode, a three-phase PWM waveform with dead time that ensures the linearity in the vicinity of duty 0% and 100% can be output using the GTCNT counter of consecutive three channels. There are four modes depending on differences in buffer operation: (1) complementary PWM mode 1 (transfer at crests), (2) complementary PWM mode 2 (transfer at troughs), (3) complementary PWM mode 3 (transfer at crests and troughs), and (4) complementary PWM mode 4 (immediate transfer).

Figure 21.47 shows the block diagram in complementary PWM modes 1 to 3.

Among consecutive three channels, the lowest channel is referred to as master channel, and the adjacent upper two channels are referred to as slave channel 1 (lower) and slave channel 2 (upper).

The GTCNT counter of each channel performs individual count operation under the cycle operation by the master channel. In each channel, compare match with the GTCCRA register is performed selecting one of the three GTCNT counters in each operation section, and a positive-phase waveform and a negative-phase waveform are output from the GTIOCn+iA pin (i = 0, 1, 2) and the GTIOCn+iB pin respectively with a non-overlapping section of the dead time value set in the GTDVU register of the master channel.

The GTCCRA register performs buffer operation by the GTCCRC register, temporary register A, and GTCCRD register. In complementary PMW mode 3, setting the GTBER2.CP3DB bit to 1 also enables buffer operation of the GTCCRA register by the GTCCRE register, temporary register B, and GTCCRF register, allowing double buffer operation.

Table 21.29 三角波PWM模式3(2of2)的示例设置

No.	步骤名称	Description
2	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
3	设置周期	在GTPR寄存器中设置周期。
4	设置计数器的初始值	在GTCNT计数器中设置初始值。
5	设置GTIOCnm引脚功能	使用GTIOR寄存器中的GTIOA[4:0]和GTIOB[4:0]位设置GTIOCnm引脚功能。 在图21.46中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
6	启用GTCPPOn引脚输出	使用GTIOR寄存器中的PSYE位设置启用禁用GTCPPOn引脚输出。
7	启用GTIOCnm引脚输出*1	通过GTIOR寄存器中的OAE和OBE位设置使能GTIOCnm引脚输出。
8	设置比较匹配值*1	在GTCCRC和GTCCRD寄存器中的计数开始以及GTCCRE和GTCCRF寄存器中的GTIOCnB引脚转换后立即设置GTIOCnA引脚转换。
9	设置强制缓冲传输*1	将GTBER.CCRSWT位设置为1以强制传输缓冲寄存器数据。
10	设置缓冲区值	在GTCCRC和GTCCRD寄存器中的当前周期以及GTCCRE和GTCCRF寄存器中的GTIOCnB引脚转换之后的1个周期内设置GTIOCnA引脚转换。
11	开始计数操作	将GTCR.CST位设置为1以启动计数操作。
12	为每个周期设置缓冲区值	在GTCCRC和GTCCRD寄存器中的当前周期以及GTCCRE和GTCCRF寄存器中的GTIOCnB引脚转换之后的1个周期内设置GTIOCnA引脚转换。

Note: n: 0 to 9
m: A, B

注1.当使用PWM延迟产生电路时，改变EnableGTIOCnmpinoutput和Setcomparematchvalue+Setforceforcebuffertransfer的顺序。

21.3.3.7 互补PWM模式1 2 3

在互补PWM模式下，可以使用连续三个通道的GTCNT计数器输出具有死区时间的三相PWM波形，以确保占空比0%和100%附近的线性度。根据缓冲器操作的不同，有四种模式：(1)互补PWM模式1（波峰传输），(2)互补PWM模式2（波谷传输），(3)互补PWM模式3（波峰和波谷传输）)和(4)互补PWM模式4（立即传输）。

图21.47显示了互补PWM模式1到3的框图。

在连续的三个通道中，最低通道称为主通道，相邻的上两个通道称为从通道1（下）和从通道2（上）。

每个通道的GTCNT计数器在主通道的循环操作下执行单独的计数操作。在每个通道中，选择每个操作部分中的三个GTCNT计数器之一执行与GTCCRA寄存器的比较匹配，并从GTIOCn+iA引脚（i=0、1）输出正相波形和负相波形2)和GTIOCn+iB引脚分别与主通道的GTDVU寄存器中设置的死区时间值的非重叠部分。

GTCCRA寄存器通过GTCCRC寄存器、临时寄存器A和GTCCRD寄存器执行缓冲操作。在互补PMW模式3中，将GTBER2.CP3DB位设置为1还可以通过GTCCRE寄存器、临时寄存器B和GTCCRF寄存器对GTCCRA寄存器进行缓冲操作，从而允许双缓冲操作。

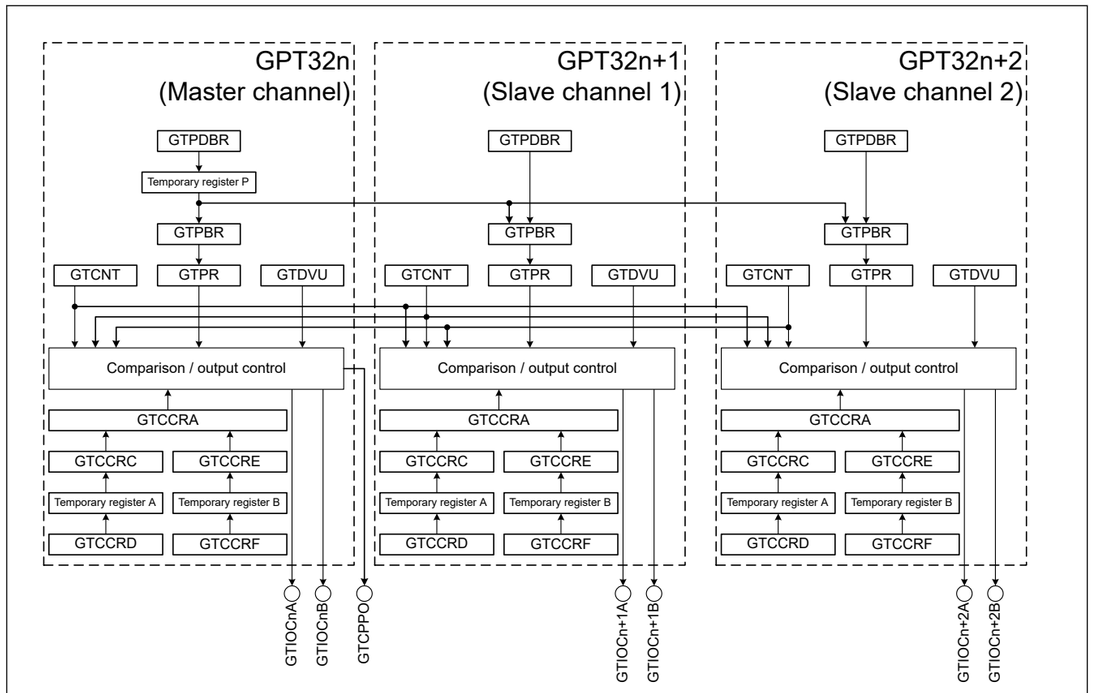


Figure 21.47 Block Diagram in Complementary PWM Mode 1, 2, 3 (n = 4, 7)

The GPT32n.GTCNT counter performs count operation for triangle waves using the GPT32n.GTPR register as a cycle register. A section where the GPT32n.GTCNT counter value is not larger than the dead time value is referred to as trough section.

The GPT32n+1.GTCNT counter performs count operation with the value (GPT32n.GTCNT counter value + dead time value set in the GPT32n.GTDVU register). A section where the GPT32n+1.GTCNT counter value is larger than the GPT32n.GTPR register value is referred to as crest section.

Crest section and trough section are classified into up-counting crest section, down-counting crest section, up-counting trough section, and down-counting trough section according to counting direction. A section between trough section and crest section is referred to as up-counting middle section or down-counting middle section according to counting direction. A section equivalent to the up-counting trough section after starting count operation is referred to as initial output section where operation differs partially from other up-counting trough sections.

The GPT32n+2.GTCNT counter functions as a counter to ensure the linearity in the vicinity of duty 0% and 100%. In a crest section, this counter performs count operation for a triangle wave (up-counting after down-counting) with the value (GPT32n.GTPR register value + dead time value) as an initial value and the GPT32n.GTPR register value as a trough. This counter is cleared to 0 at the end of the crest section, and then stops counting until the next trough section. In a trough section, this counter performs count operation for a triangle wave with an initial value of 0 and dead time value as a crest. This counter becomes the value (GPT32n.GTPR register value + dead time value) at the end of the trough section, and then stops counting until the next crest section. In the initial output section, however, this counter counts up with an initial value of 0 until the dead time value, and then becomes the value (GPT32n.GTPR register value + dead time value).

If the counter stops and then restarts in complementary PWM mode, the counter of each channel returns to the initial value after starting count operation, and then starts counting from the initial output section.

Table 21.30 and Table 21.31 shows count operation (counting direction/counting range) in each section. In these tables, registers with no channel identification indicate that the same value is stored in them of the master channel, slave channel 1, and slave channel 2.

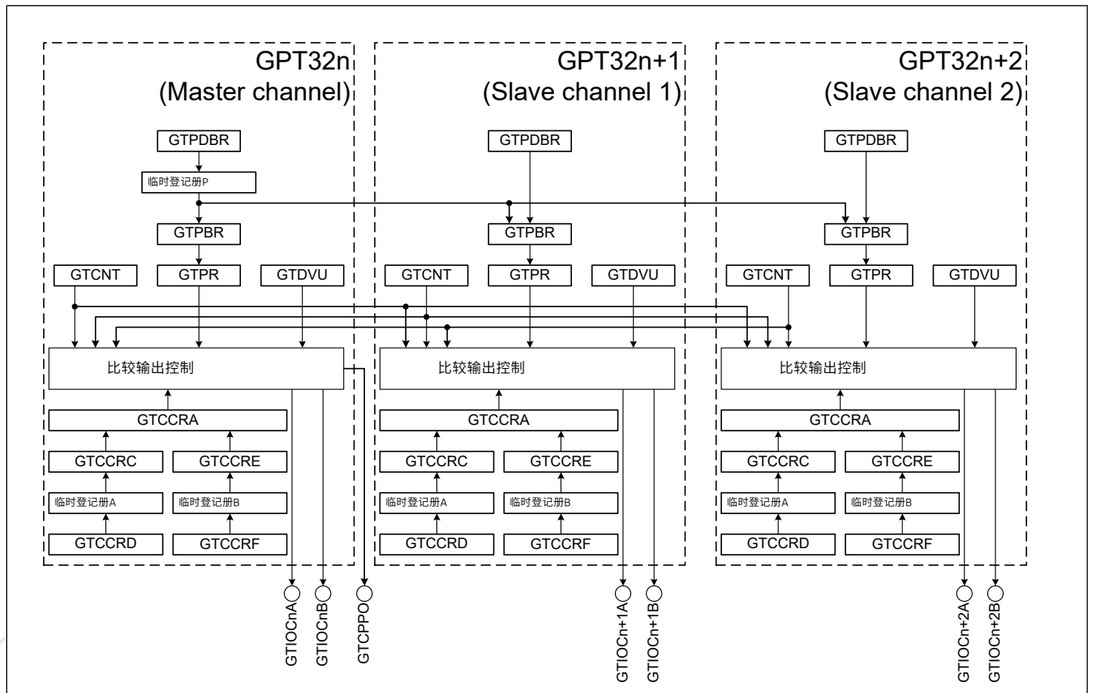


Figure 21.47 互补PWM模式1、2、3（n=4、7）中的框图

GPT32n.GTCNT计数器使用GPT32n.GTPR寄存器作为周期寄存器对三角波进行计数操作。GPT32n.GTCNT计数器值不大于死区时间值的部分称为波谷部分。

GPT32n+1.GTCNT计数器使用值（GPT32n.GTCNT计数器值+GPT32n.GTDVU寄存器中设置的死区时间值）执行计数操作。GPT32n+1.GTCNT计数器值大于GPT32n.GTPR寄存器值的部分称为波峰部分。

波峰段和波谷段按计数方向分为向上计数波峰段、向下计数波峰段、向上计数槽段和向下计数槽段。波谷段和波峰段之间的一段按计数方向称为向上计数中间段或向下计数中间段。在开始计数操作之后相当于递增计数谷部分的部分被称为初始输出部分，其中操作部分不同于其他递增计数谷部分。

GPT32n+2.GTCNT计数器用作计数器以确保占空比0%和100%附近的线性度。在波峰部分，该计数器以（GPT32n.GTPR寄存器值+死区时间值）为初始值，以GPT32n.GTPR寄存器值为槽。该计数器在波峰段结束时清零，然后停止计数，直到下一个波谷段。在波谷部分，该计数器对初始值为0且死区时间值作为波峰的三角波执行计数操作。该计数器在波谷部分结束时变为值（GPT32n.GTPR寄存器值+死区时间值），然后停止计数，直到下一个波峰部分。然而，在初始输出部分，此计数器以初始值0向上计数，直到死区时间值，然后变为值（GPT32n.GTPR寄存器值+死区时间值）。

如果计数器在互补PWM模式下停止然后重新启动，则每个通道的计数器在开始计数操作后返回初始值，然后从初始输出部分开始计数。

表21.30和表21.31显示了每个部分的计数操作（计数方向计数范围）。在这些表中，没有通道标识的寄存器表示主通道、从通道1和从通道2中存储的值相同。

Table 21.30 Count Operation in Complementary PWM Mode

Counter	Initial Value	Initial Output Section (After Start)	Up-Counting Middle Section	Up-Counting Crest Section	Down-Counting Crest Section
GPT32n.GTCNT	0	Up-counting 0 to GTDVU	Up-counting GTDVU +1 to GTPR-GTDVU	Up-counting GTPR-GTDVU+1 to GTPR	Down-counting GTPR-1 to GTPR-GTDVU
GPT32n+1.GTCNT	GTDVU	Up-counting GTDVU to GTDVU×2	Up-counting GTDVU×2+1 to GTPR	Up-counting GTPR+1 to GTPR+GTDVU	Down-counting GTPR+GTDVU-1 to GTPR
GPT32n+2.GTCNT	0	Up-counting 0 to GTDVU	Stop GTPR+GTDVU	Down-counting GTPR+GTDVU-1 to GTPR	Up-counting GTPR+1 to GTPR+GTDVU

Table 21.31 Count Operation in Complementary PWM Mode

Counter	Down-Counting Middle Section	Down-Counting Trough Section	Up-Counting Trough Section
GPT32n.GTCNT	Down-counting GTPR-GTDVU-1 to GTDVU	Down-counting GTDVU-1 to 0	Up-counting 1 to GTDVU
GPT32n+1.GTCNT	Down-counting GTPR-1 to GTDVU×2	Down-counting GTDVU×2-1 to GTDVU	Up-counting GTDVU+1 to GTDVU×2
GPT32n+2.GTCNT	Stop 0	Up-counting 1 to GTDVU	Down-counting GTDVU-1 to 0

In complementary PWM mode, the GTCCRA register performs unusual buffer operation.

Data transfers from the GTCCRD register to the temporary register A and from the GTCCRF register to the temporary register B are performed at the same time in three channels by writing a value to the GTCCRD register of the GPT32n+2 channel.

Data transfers from the temporary register A and temporary register B to the GTCCRC and GTCCRE registers vary depending on the transfer timing to the temporary register A and temporary register B. Data transfers from the GTCCRC and GTCCRE registers to the GTCCRA register are performed according to each complementary PWM mode name (crest transfer, trough transfer, and crest/trough transfer).

Buffer operation of the GTPR register in complementary PWM mode is described in section 21.3.2.1. GTPR Register Buffer Operation. Do not perform buffer operation for the GTDVU register in complementary PWM mode.

Table 21.32 shows buffer transfer timing during single buffer operation in complementary PWM modes 1 to 3. Table 21.33 shows buffer transfer timing during double buffer operation in complementary PWM mode 3.

Table 21.32 Single Buffer Transfer Timing in Complementary PWM Mode 1, 2, 3

Buffer Transfer	Complementary PWM Mode 1	Complementary PWM Mode 2	Complementary PWM Mode 3 (Single Buffer)
GTCCRD ↓ Temporary register A	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)
Temporary register A ↓ GTCCRC	(1) When data is transferred to temporary register A in up-counting middle section After one GTCLK cycle from transfer to temporary register A (2) When data is transferred to temporary register A in a section other than up-counting middle section At the end of trough section	(1) When data is transferred to temporary register A in down-counting middle section After one GTCLK cycle from transfer to temporary register A (2) When data is transferred to temporary register A in a section other than down-counting middle section At the end of crest section	(1) When data is transferred to temporary register A in middle section After one GTCLK cycle from transfer to temporary register A (2) When data is transferred to temporary register A in a section other than middle section At the end of crest and trough sections
GTCCRC ↓ GTCCRA	At the end of crest section Counter clear in up-counting middle section and crest section	At the end of trough section (excluding initial output section) Counter clear in down-counting middle section and trough section	At the end of crest section At the end of trough section (excluding initial output section) Counter clear

Table 21.30 互补PWM模式下的计数操作

Counter	初始值	初始输出 Section (After Start)	Up-Counting Middle Section	Up-Counting Crest Section	Down-Counting 波峰部分
GPT32n.GTCNT	0	Up-counting 0 to GTDVU	Up-counting GTDVU +1 to GTPR-GTDVU	Up-counting GTPR-GTDVU+1 to GTPR	Down-counting GTPR-1 to GTPR-GTDVU
GPT32n+1.GTCNT	GTDVU	Up-counting GTDVU to GTDVU×2	Up-counting GTDVU×2+1 to GTPR	Up-counting GTPR+1 to GTPR+GTDVU	Down-counting GTPR+GTDVU-1 to GTPR
GPT32n+2.GTCNT	0	Up-counting 0 to GTDVU	Stop GTPR+GTDVU	Down-counting GTPR+GTDVU-1 to GTPR	Up-counting GTPR+1 to GTPR+GTDVU

Table 21.31 互补PWM模式下的计数操作

Counter	向下计数的中间部分	Down-Counting Trough Section	向上计数槽部分
GPT32n.GTCNT	Down-counting GTPR-GTDVU-1 to GTDVU	Down-counting GTDVU-1 to 0	Up-counting 1 to GTDVU
GPT32n+1.GTCNT	Down-counting GTPR-1 to GTDVU×2	Down-counting GTDVU×2-1 to GTDVU	Up-counting GTDVU+1 to GTDVU×2
GPT32n+2.GTCNT	Stop 0	Up-counting 1 to GTDVU	Down-counting GTDVU-1 to 0

在互补PWM模式下，GTCCRA寄存器执行异常缓冲操作。

从GTCCRD寄存器到临时寄存器A和从GTCCRF寄存器到临时寄存器B的数据传输通过向GPT32n+2通道的GTCCRD寄存器写入值在三个通道中同时执行。

从临时寄存器A和临时寄存器B到GTCCRC和GTCCRE寄存器的数据传输取决于到临时寄存器A和临时寄存器B的传输时序。从GTCCRC和GTCCRE寄存器到GTCCRA寄存器的数据传输是根据每个互补PWM模式名称（波峰传输、波谷传输和波峰波谷传输）。

GTPR寄存器在互补PWM模式下的缓冲操作在第21.3.2.1节中描述。GTPR寄存器缓冲操作。不要在互补PWM模式下对GTDVU寄存器执行缓冲操作。

表21.32显示了互补PWM模式1至3中单缓冲器操作期间的缓冲器传输时序。表21.33显示了互补PWM模式3中双缓冲器操作期间的缓冲器传输时序。

Table 21.32 互补PWM模式1、2、3中的单缓冲器传输时序

缓冲传输	互补PWM模式1	互补PWM模式2	互补PWM模式3（单缓冲器）
GTCCRD ↓临时寄存器A	从一个GTCLK周期后 从通道2(GPT32n+2)的GTCCRD寄存器写入	从一个GTCLK周期后 从通道2(GPT32n+2)的GTCCRD寄存器写入	从一个GTCLK周期后 从通道2(GPT32n+2)的GTCCRD寄存器写入
临时登记册A ↓ GTCCRC	(1)向上计数中间段向临时寄存器A传输数据时向临时寄存器A传输一个GTCLK周期后(2)向上计数中间段以外的段向临时寄存器A传输数据时结束槽段	(1)当数据在递减计数中间部分被传送到临时寄存器A从传送到临时寄存器A的一个GTCLK周期后(2)当数据在递减计数中间部分以外的部分传送到临时寄存器A结束时波峰部分	(1)当数据传输到中间部分的临时寄存器A传输到临时寄存器A的一个GTCLK周期后(2)当数据传输到中间部分以外的部分的临时寄存器A波峰和波谷部分的末端
GTCCRC ↓ GTCCRA	在波峰段的末端 加计数中段和波峰段计数器清零	槽段末端（不包括初始输出段）递减计数中段和槽段计数器清零	在波峰段的末端 波谷段结束时（不包括初始输出段）计数器清零

Table 21.33 Double Buffer Transfer Timing in Complementary PWM Mode 3

Transfer from GTCCRD to GTCCRA		Transfer from GTCCRF to GTCCRA	
Buffer Transfer	**Transfer Timing**	**Buffer Transfer**	**Transfer Timing**
GTCCRD ↓ Temporary register A	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	GTCCRF ↓ Temporary register B	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)
Temporary register A ↓ GTCCRC	(1) When data is transferred to temporary register A in middle section After one GTCLK cycle from transfer to temporary register A (2) When data is transferred to temporary register A in a section other than middle section At the end of crest and trough sections	Temporary register B ↓ GTCCRE	(1) When data is transferred to temporary register B in middle section After one GTCLK cycle from transfer to temporary register B (2) When data is transferred to temporary register B in a section other than middle section At the end of crest and trough sections
GTCCRC ↓ GTCCRA	At the end of crest section Counter clear	GTCCRE ↓ GTCCRA	At the end of trough section (excluding initial output section)

An output level change in the positive-phase waveform from the GTIOCn+iA pin (i = 0, 1, 2) and the negative-phase waveform from the GTIOCn+iB pin occurs at a compare match in combination of counters and registers determined for each operation section. In middle sections, the positive-phase waveform output level changes at a compare match of the GPT32n.GTCNT counter and the GTCCRA register, and the negative-phase waveform output level changes at a compare match between the GPT32n+1.GTCNT counter and the GTCCRA register. In crest and trough sections, compare match operation is performed using the GPT32n+2.GTCNT counter, GTCCRC register, and GTCCRE register to ensure the linearity in the vicinity of duty 0% and 100%.

In the case that the compare match value equals to or larger than the GPT32n.GTPR register value, the duty becomes 0% (positive-phase waveform OFF, negative-phase waveform ON). In the case that the compare match value is 0, the duty becomes 100% (positive-phase waveform ON, negative-phase waveform OFF).

Table 21.34 lists combinations of counters and registers used for compare match operation to generate a positive-phase waveform and a negative-phase waveform in each operation section.

Table 21.34 Combinations of Counters and Registers for Compare Match Operation in Complementary PWM Mode

	Up-Counting Middle Section	Up-Counting Crest Section	Down-Counting Crest Section	Down-Counting Middle Section	Down-Counting Trough Section	Up-Counting Trough Section
Negative-phase OFF	GPT32n +1.GTCNT	GPT32n +1.GTCNT	—	GPT32n +2.GTCNT*1	GPT32n +2.GTCNT	GPT32n +1.GTCNT
	GTCCRA	GTCCRA	—	GTCCRC (GTCCRE for double buffer operation)	GTCCRC (GTCCRE for double buffer operation)	GTCCRC (GTCCRE for double buffer operation)
Positive-phase ON	GPT32n.GTCNT	GPT32n.GTCNT	GPT32n +2.GTCNT	—	GPT32n.GTCNT *1	GPT32n.GTCNT
	GTCCRA	GTCCRA	GTCCRA	—	GTCCRC (GTCCRE for double buffer operation)	GTCCRC (GTCCRE for double buffer operation)
Positive-phase OFF	GPT32n +2.GTCNT*1	GPT32n +2.GTCNT	GPT32n.GTCNT	GPT32n.GTCNT	GPT32n.GTCNT	—
	GTCCRC	GTCCRC	GTCCRC	GTCCRA	GTCCRA	—
Negative-phase ON	—	GPT32n +1.GTCNT*1	GPT32n +1.GTCNT	GPT32n +1.GTCNT	GPT32n +1.GTCNT	GPT32n +2.GTCNT
	—	GTCCRC	GTCCRC	GTCCRA	GTCCRA	GTCCRA

Note 1. Compare match is performed only at the time of final count in the target section, but is not performed at count values other than the final count.

Table 21.33 互补PWM模式3中的双缓冲器传输时序

从GTCCRD转移到GTCCRA		从GTCCRF转移到GTCCRA	
缓冲传输	**传输时间**	**缓冲传输**	**传输时间**
GTCCRD ↓临时寄存器A	从一个GTCLK周期后 从通道2(GPT32n+2)的GTCCRD寄存器写入	GTCCRF ↓临时登记簿B	从一个GTCLK周期后 从通道2(GPT32n+2)的GTCCRD寄存器写入
临时登记册A ↓ GTCCRC	(1)当数据传输到中间部分的临时寄存器A传输到临时寄存器A的一个GTCLK周期后(2)当数据传输到中间部分以外的部分的临时寄存器A波峰和波谷部分的末端	临时登记册B ↓ GTCCRE	(1)当数据被传送到中间部分的临时寄存器B从传送到临时寄存器B的一个GTCLK周期后(2)当数据在中间部分以外的部分被传送到临时寄存器B波峰和波谷部分的末端
GTCCRC ↓ GTCCRA	在波峰段的末端 计数器清零	GTCCRE ↓ GTCCRA	波谷段末端（不包括初始输出段）

GTIOCn+iA引脚的正相波形(i=0 1 2)和GTIOCn+iB引脚的负相波形的输出电平变化发生在计数器和寄存器组合的比较匹配中每个操作部分。在中间部分，正相波形输出电平在GPT32n.GTCNT计数器和GTCCRA寄存器的比较匹配时发生变化，而负相波形输出电平在GPT32n+1.GTCNT计数器和GTCCRA寄存器比较匹配时发生变化。GTCCRA寄存器。在波峰和波谷部分，使用GPT32n+2.GTCNT计数器、GTCCRC寄存器和GTCCRE寄存器执行比较匹配操作，以确保占空比0%和100%附近的线性度。

在比较匹配值等于或大于GPT32n.GTPR寄存器值的情况下，占空比变为0%（正相波形关闭，反相波形开启）。在比较匹配值为0的情况下，占空比变为100%（正相波形开启，反相波形关闭）。

表21.34列出了用于比较匹配操作的计数器和寄存器的组合，以在每个操作部分生成正相波形和负相波形。

Table 21.34 互补PWM中比较匹配操作的计数器和寄存器组合 Mode

	Up-Counting 中段	向上计数波峰部分	Down-Counting 波峰部分	向下计数的中间部分	向下计数槽段	Up-Counting 槽段
Negative-phase OFF	GPT32n +1.GTCNT	GPT32n +1.GTCNT	—	GPT32n +2.GTCNT*1	GPT32n +2.GTCNT	GPT32n +1.GTCNT
	GTCCRA	GTCCRA	—	GTCCRC（用于双缓冲操作的GTCCRE）	GTCCRC（用于双缓冲操作的GTCCRE）	GTCCRC（用于双缓冲操作的GTCCRE）
Positive-phase ON	GPT32n.GTCNT	GPT32n.GTCNT	GPT32n +2.GTCNT	—	GPT32n.GTCNT *1	GPT32n.GTCNT
	GTCCRA	GTCCRA	GTCCRA	—	GTCCRC（用于双缓冲操作的GTCCRE）	GTCCRC（用于双缓冲操作的GTCCRE）
Positive-phase OFF	GPT32n +2.GTCNT*1	GPT32n +2.GTCNT	GPT32n.GTCNT	GPT32n.GTCNT	GPT32n.GTCNT	—
	GTCCRC	GTCCRC	GTCCRC	GTCCRA	GTCCRA	—
Negative-phase ON	—	GPT32n +1.GTCNT*1	GPT32n +1.GTCNT	GPT32n +1.GTCNT	GPT32n +1.GTCNT	GPT32n +2.GTCNT
	—	GTCCRC	GTCCRC	GTCCRA	GTCCRA	GTCCRA

注1.比较匹配仅在目标部分的最终计数时执行，但在最终计数以外的计数值时不执行。

In the case of normal complementary PWM mode waveform, a PWM waveform change occurs in the order of negative-phase OFF → positive-phase ON → positive-phase OFF → negative-phase ON. However, this order may vary depending on operation section and register values. In this case, OFF takes precedence in trough sections and ON takes precedence in crest sections (for negative-phase waveforms), and ON takes precedence in trough sections and OFF takes precedence in crest sections (for positive-phase waveforms). A lower-priority compare match that occurs at the same time or after a higher-priority compare match is ignored.

In the initial output section, the initial output set in the GTIOR register is retained. In the case that the GTCCRA register value is larger than the GTDVU register value at the end of the initial output section, negative phase is enabled. In the case that the GTCCRA register value is not larger than the GTDVU register value, positive phase is enabled.

As operation examples of normal complementary PWM mode waveform where compare match operation occurs in the middle section, Figure 21.48 and Figure 21.49 show complementary PWM mode 1, Figure 21.50 and Figure 21.51 show complementary PWM mode 2, Figure 21.52 and Figure 21.53 show single buffer complementary PWM mode 3, and Figure 21.54 and Figure 21.55 show double buffer complementary PWM mode 3.

Figure 21.56 to Figure 21.67 show complementary PWM mode waveforms where compare match operation occurs in crest sections and trough sections and differences due to compare match occurrence order.

Figure 21.68 and Figure 21.69 show examples of initial output operation according to the GTCCRA register value.

Table 21.35 shows an example for setting complementary PWM modes 1 to 3.

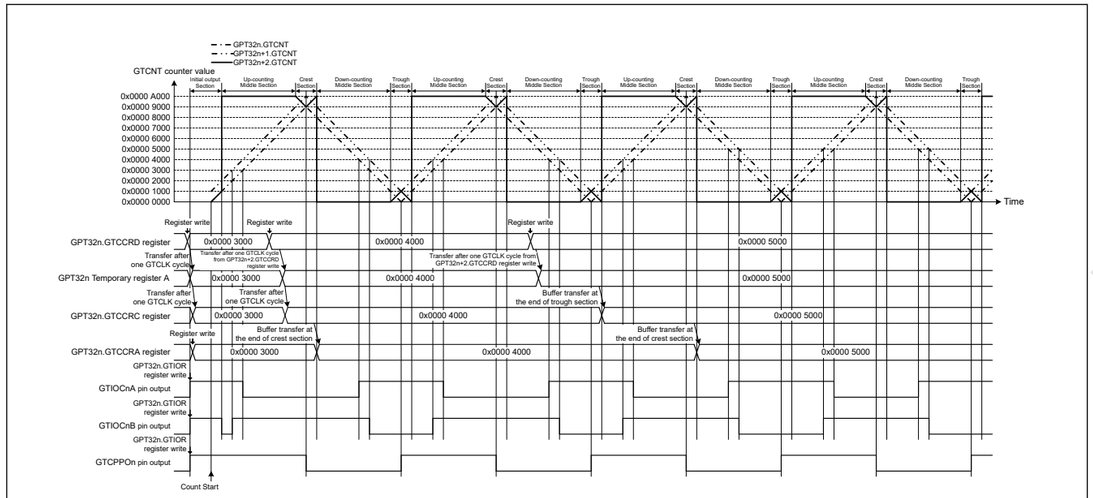


Figure 21.48 Example of Complementary PWM Mode 1 Operation (GTIOCnA pin = High / GTIOCnB pin = High as initial output, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in middle section) (n = 4, 7)

在正常的互补PWM模式波形的情况下，PWM波形按照负相OFF→正相ON→正相OFF→负相ON的顺序发生变化。但是，此顺序可能会因操作部分和寄存器值而异。在这种情况下，OFF优先于波谷部分，ON优先于波峰部分（对于负相波形），ON优先于波谷部分，OFF优先于波峰部分（对于正相波形）。忽略与较高优先级比较匹配同时或之后发生的较低优先级比较匹配。

在初始输出部分，保留GTIOR寄存器中设置的初始输出。如果GTCCRA寄存器值大于初始输出部分末尾的GTDVU寄存器值，则启用负相位。在GTCCRA寄存器值不大于GTDVU寄存器值的情况下，正相使能。

作为在中间部分发生比较匹配操作的正常互补PWM模式波形的操作示例，图21.48和图21.49显示了互补PWM模式1，图21.50和图21.51显示了互补PWM模式2，图21.52和图21.53显示了单缓冲器互补PWM模式3，图21.54和图21.55显示了双缓冲器互补PWM模式3。

图21.56至图21.67显示了互补PWM模式波形，其中比较匹配操作发生在波峰部分和波谷部分，以及由于比较匹配发生顺序而产生的差异。

图21.68和图21.69显示了根据GTCCRA寄存器值的初始输出操作示例。

表21.35显示了设置互补PWM模式1至3的示例。

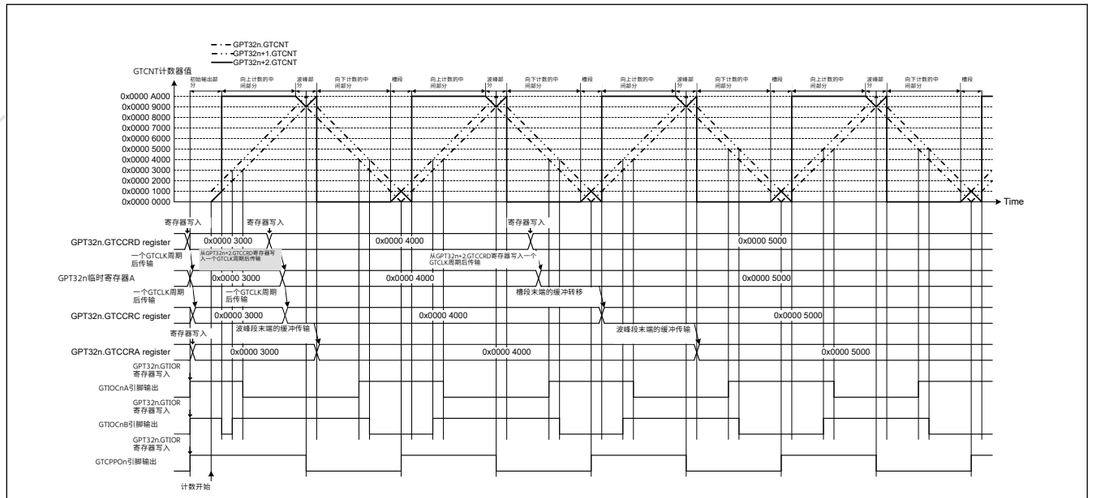


Figure 21.48 互补PWM模式1操作示例（GTIOCnA引脚=高GTIOCnB引脚=高作为初始输出，GTIOCnA引脚=低GTIOCnB引脚=向上计数期间GTCCRA寄存器比较匹配时为高，GTIOCnA引脚=高GTIOCnB引脚=在GTCCRA寄存器比较时为低向下计数期间匹配，死区时间值为0x00001000并更新中间部分的GTCCRD寄存器）（n=4 7）

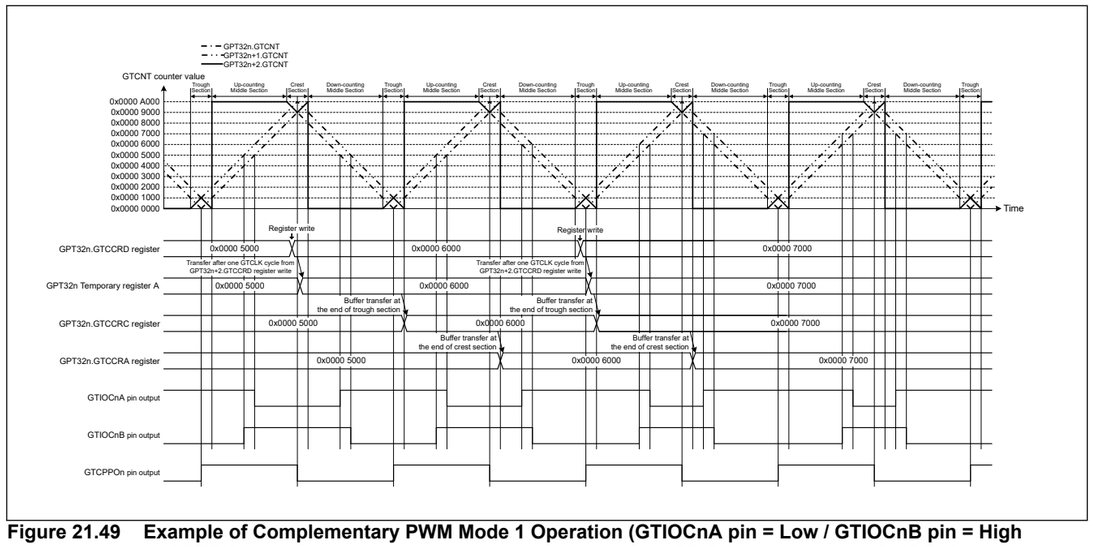


Figure 21.49 Example of Complementary PWM Mode 1 Operation (GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in crest and trough sections) (n = 4, 7)

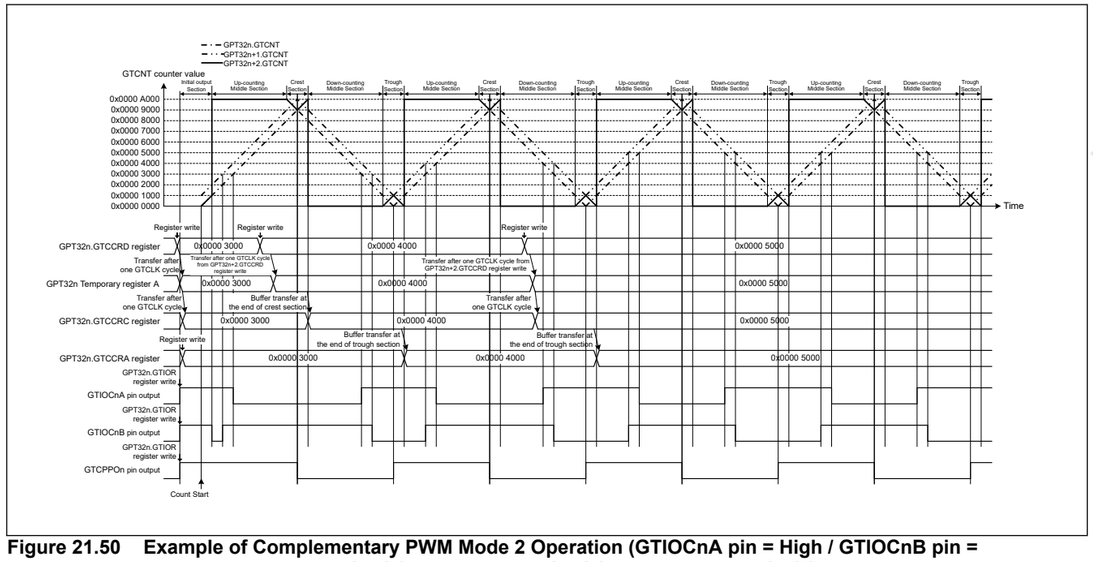


Figure 21.50 Example of Complementary PWM Mode 2 Operation (GTIOCnA pin = High / GTIOCnB pin = High as initial output, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in middle section) (n = 4, 7)

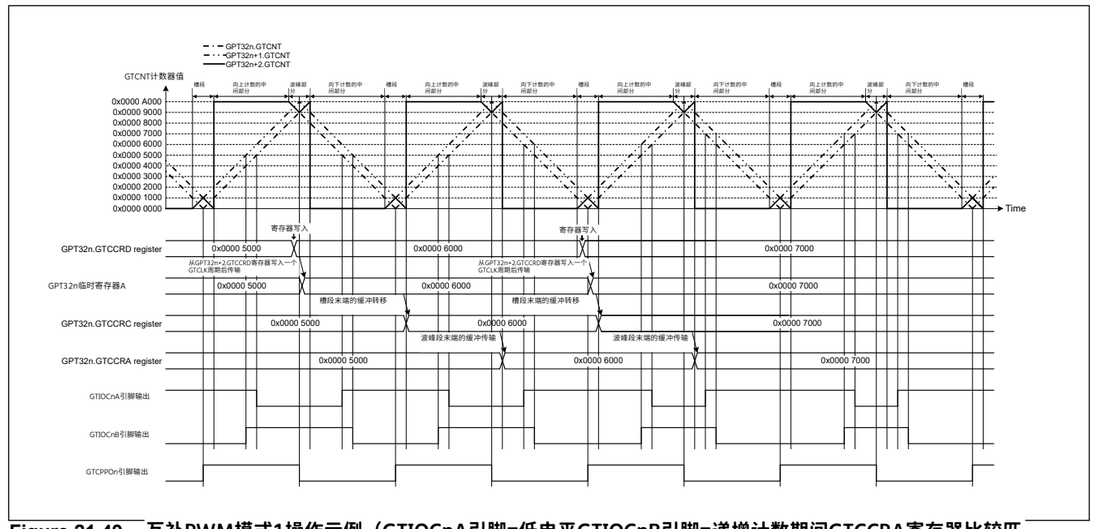


Figure 21.49 互补PWM模式1操作示例（GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=递减计数期间GTCCRA寄存器比较匹配时为低电平，死区时间值为0x00001000和更新波峰和波谷部分的GTCCRD寄存器）（n=4、7）

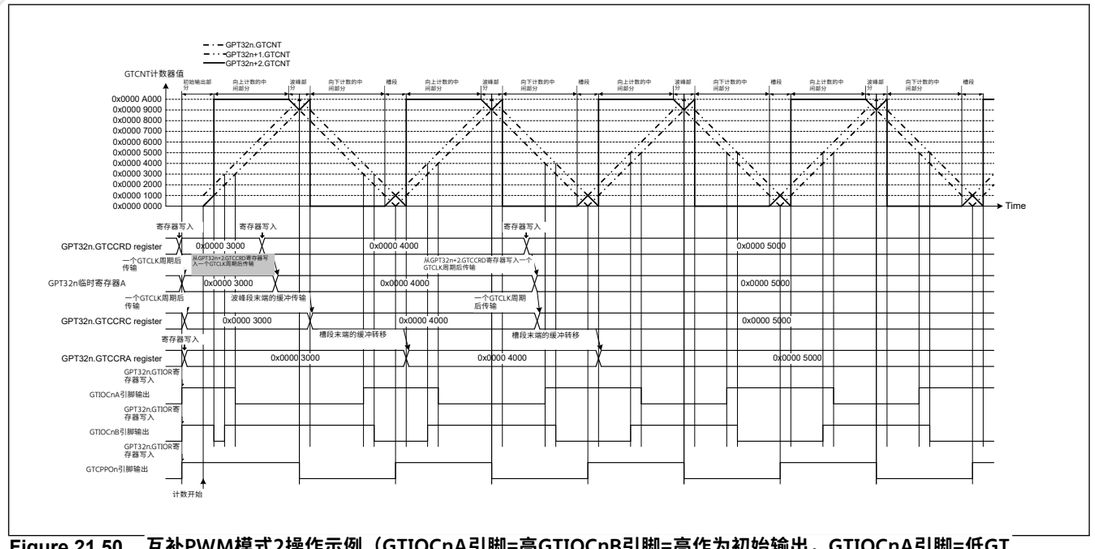


Figure 21.50 互补PWM模式2操作示例（GTIOCnA引脚=高GTIOCnB引脚=高作为初始输出，GTIOCnA引脚=低GTIOCnB引脚=在递增计数期间GTCCRA寄存器比较匹配时为高，GTIOCnA引脚=高GTIOCnB引脚=在GTCCRA寄存器比较时为低向下计数期间匹配，死区时间值为0x00001000并更新中间部分的GTCCRD寄存器）（n=4 7）

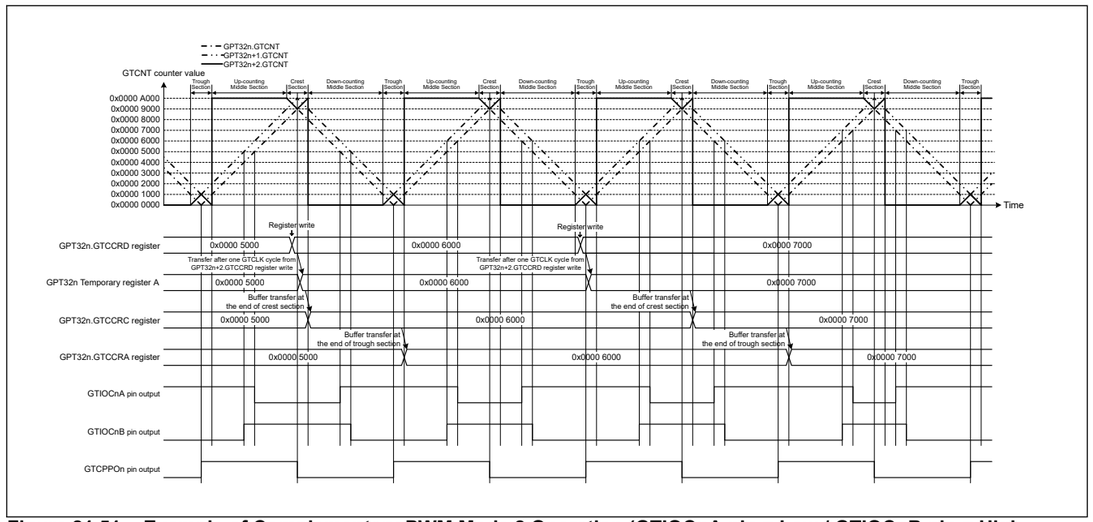


Figure 21.51 Example of Complementary PWM Mode 2 Operation (GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in crest and trough sections) (n = 4, 7)

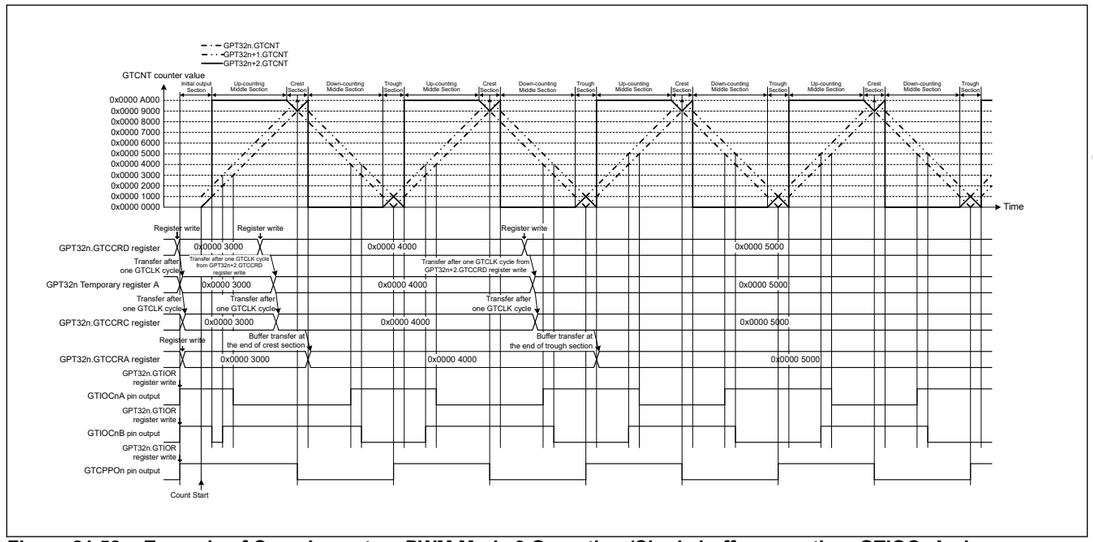


Figure 21.52 Example of Complementary PWM Mode 3 Operation (Single buffer operation, GTIOCnA pin = High / GTIOCnB pin = High as initial output, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in middle section) (n = 4, 7)

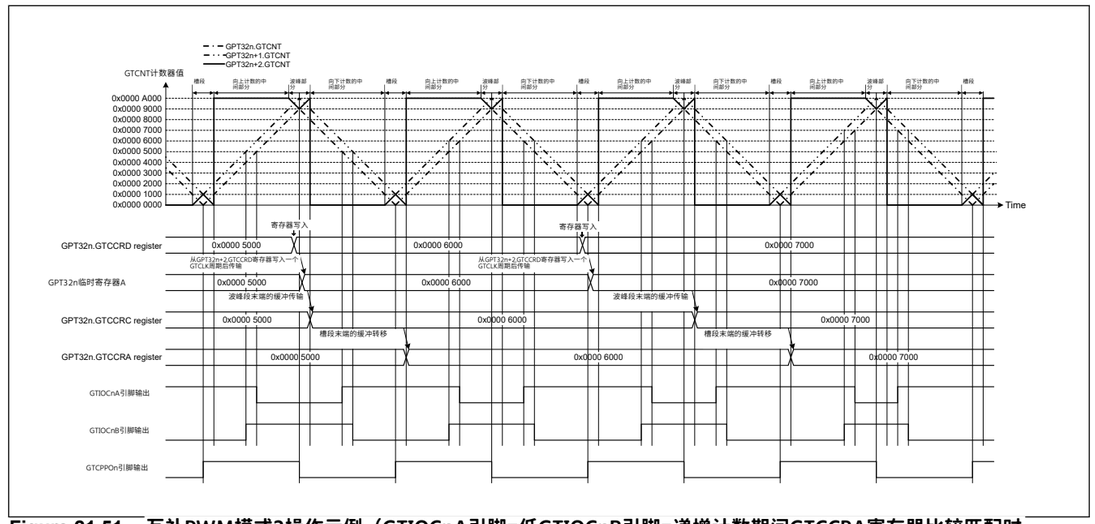


Figure 21.51 互补PWM模式2操作示例（GTIOCnA引脚=低GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=递减计数期间GTCCRA寄存器比较匹配时为低电平，死区时间值为0x00001000和更新波峰和波谷部分的GTCCRD寄存器）（n=4、7）

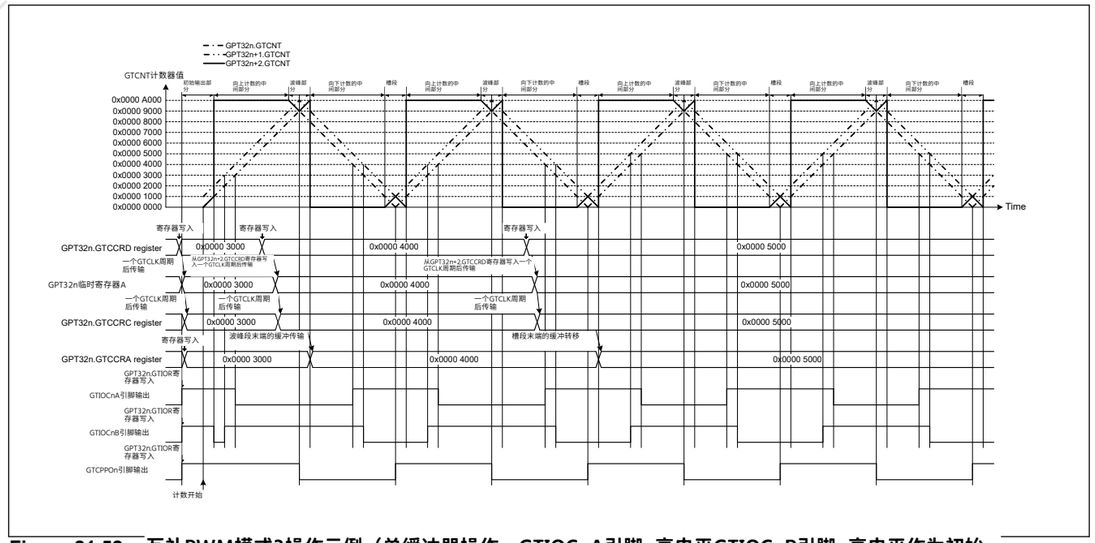


**Figure 21.52 互补PWM模式3操作示例（单缓冲器操作，GTIOCnA引脚=高电平GTIOCnB引脚=高电平作为初始输出，GTIOCnA引脚=低电平GTIOCnB引脚=高电平
递增计数期间GTCCRA寄存器比较匹配，GTIOCnA引脚=高GTIOCnB引脚=
在向下计数期间GTCCRA寄存器比较匹配时为低，死区时间值为0x00001000并在中间部分更新GTCCRD寄存器）（n=4 7）**

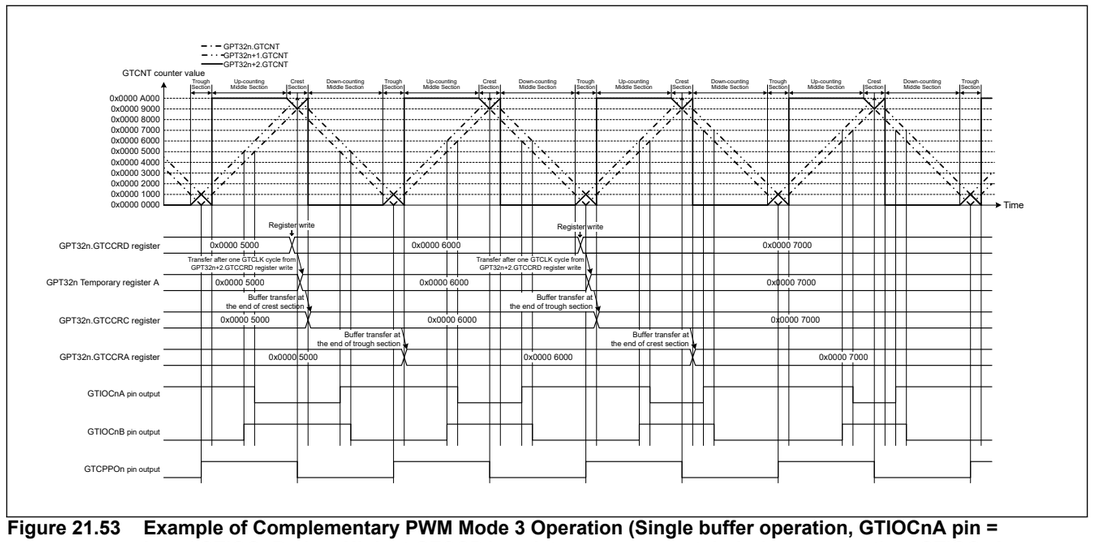


Figure 21.53 Example of Complementary PWM Mode 3 Operation (Single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in crest and trough sections) (n = 4, 7)

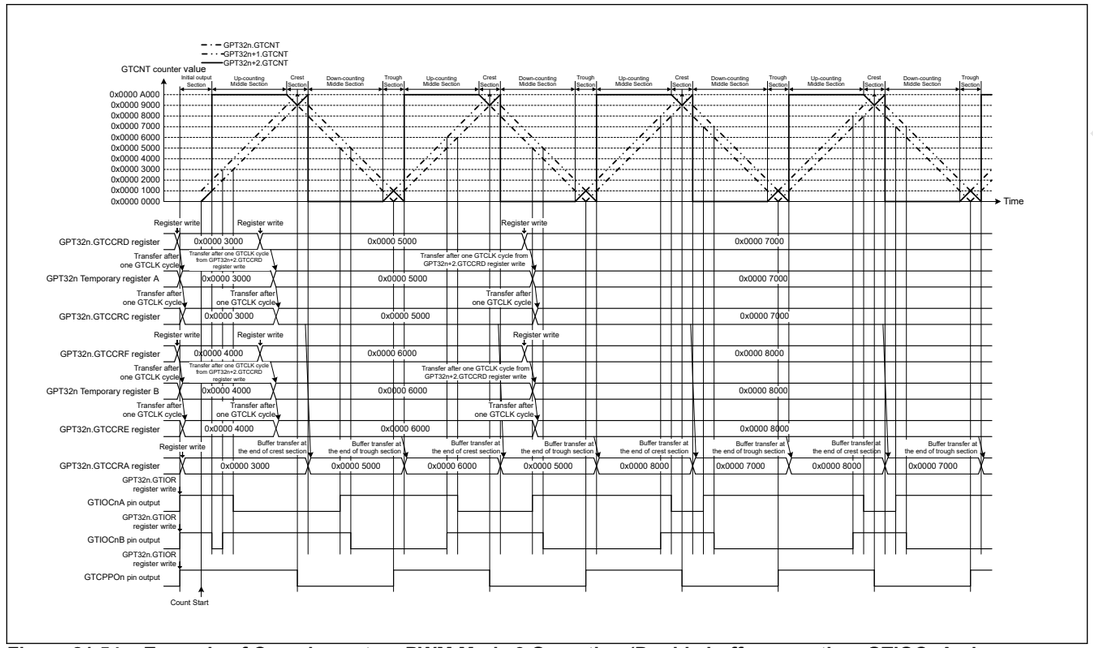


Figure 21.54 Example of Complementary PWM Mode 3 Operation (Double buffer operation, GTIOCnA pin = High / GTIOCnB pin = High as initial output, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in middle section) (n = 4, 7)

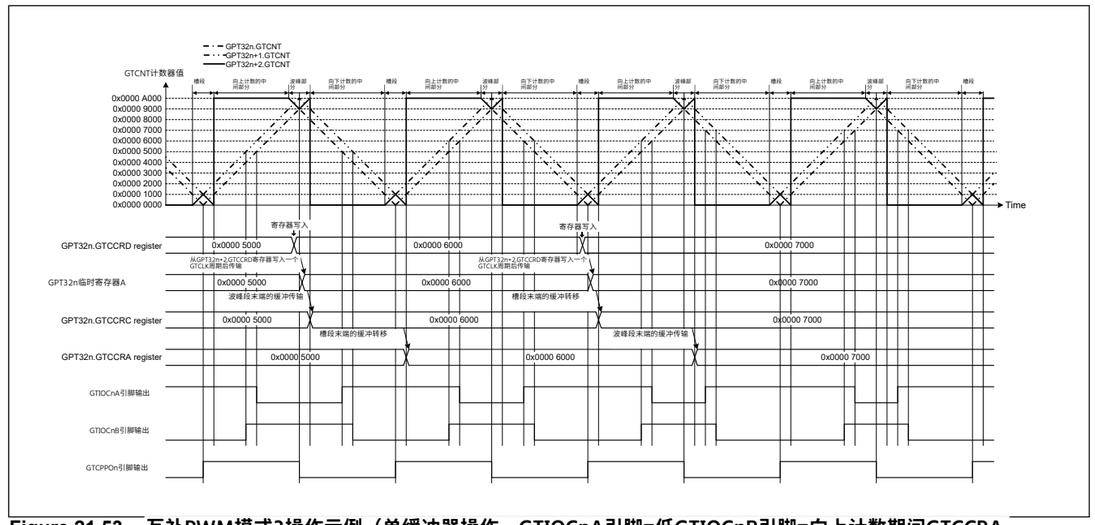


Figure 21.53 互补PWM模式3操作示例（单缓冲器操作，GTIOCnA引脚=低GTIOCnB引脚=向上计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=向下计数期间GTCCRA寄存器比较匹配时为低电平，死时间值为0x00001000并在波峰和波谷部分更新GTCCRD寄存器）（n=4 7）

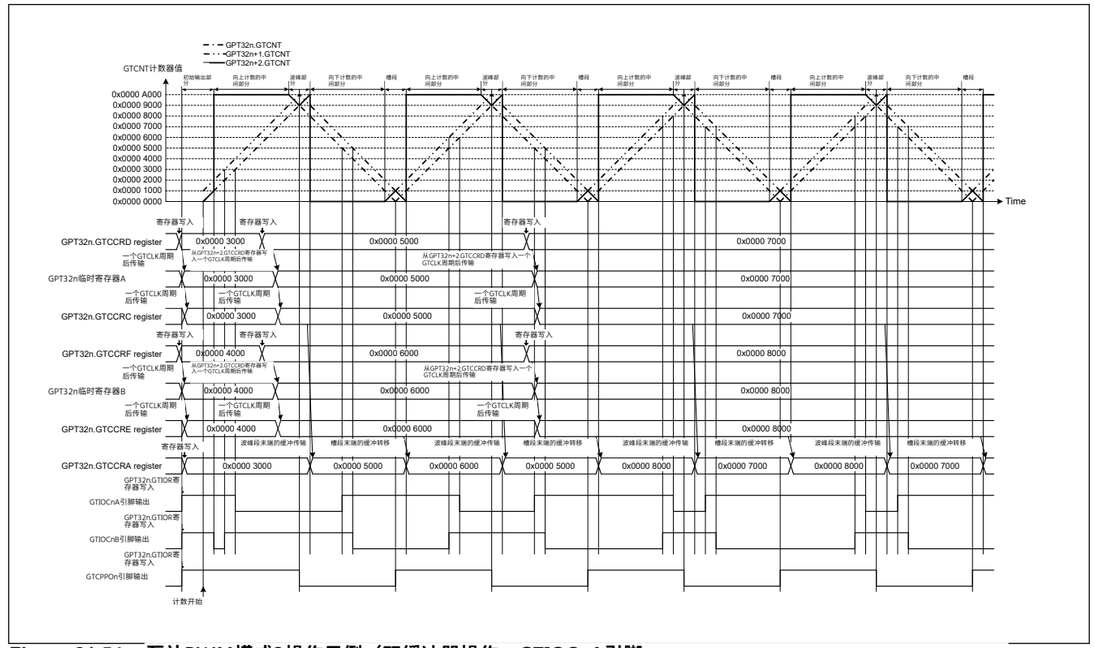


Figure 21.54 互补PWM模式3操作示例（双缓冲器操作，GTIOCnA引脚=高GTIOCnB引脚=高作为初始输出，GTIOCnA引脚=低GTIOCnB引脚=高递增计数期间GTCCRA寄存器比较匹配，GTIOCnA引脚=高GTIOCnB引脚=在向下计数期间GTCCRA寄存器比较匹配时为低，死区时间值为0x00001000并在中间部分更新GTCCRD寄存器）（n=4 7）

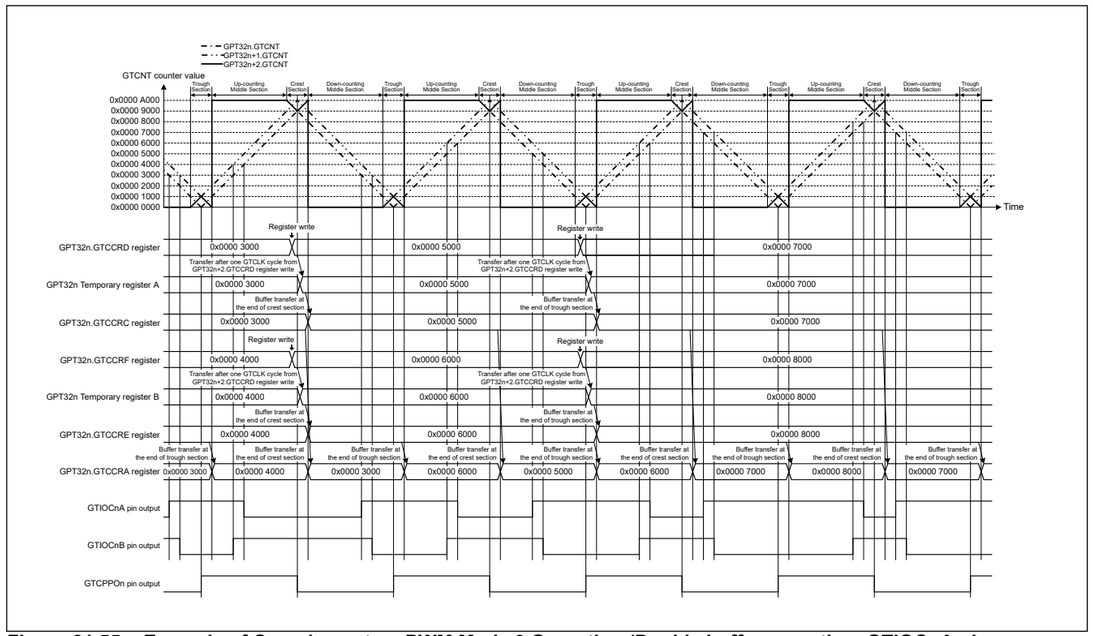


Figure 21.55 Example of Complementary PWM Mode 3 Operation (Double buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in crest and trough sections) (n = 4, 7)

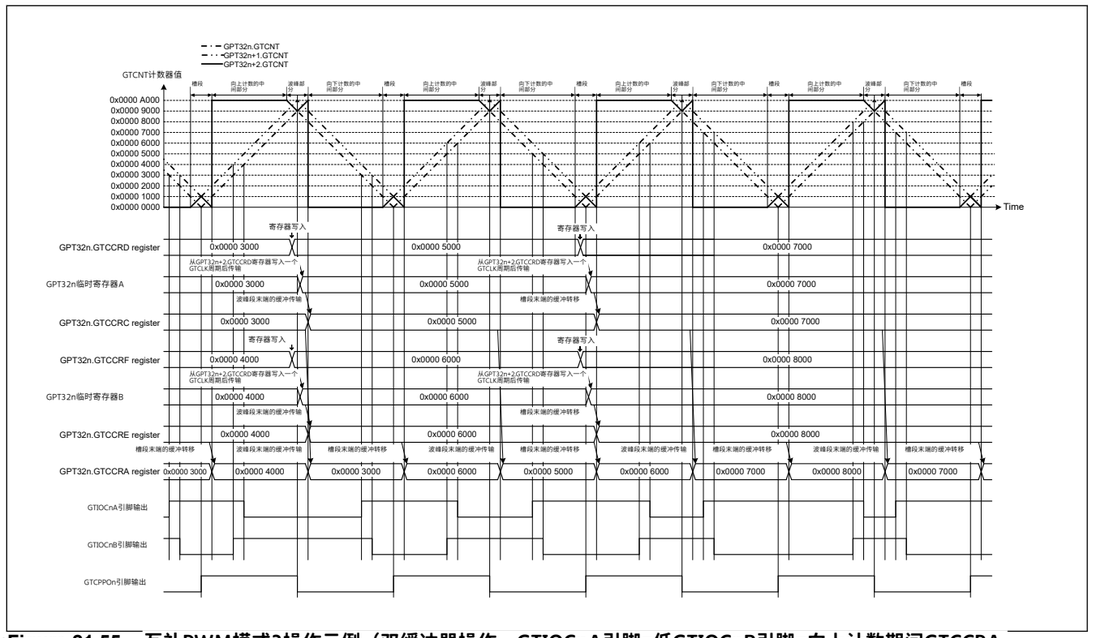


Figure 21.55 互补PWM模式3操作示例（双缓冲器操作，GTIOCnA引脚=低GTIOCnB引脚=向上计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=向下计数期间GTCCRA寄存器比较匹配时为低电平，死时间值为0x00001000并在波峰和波谷部分更新GTCCRD寄存器）（n=4 7）

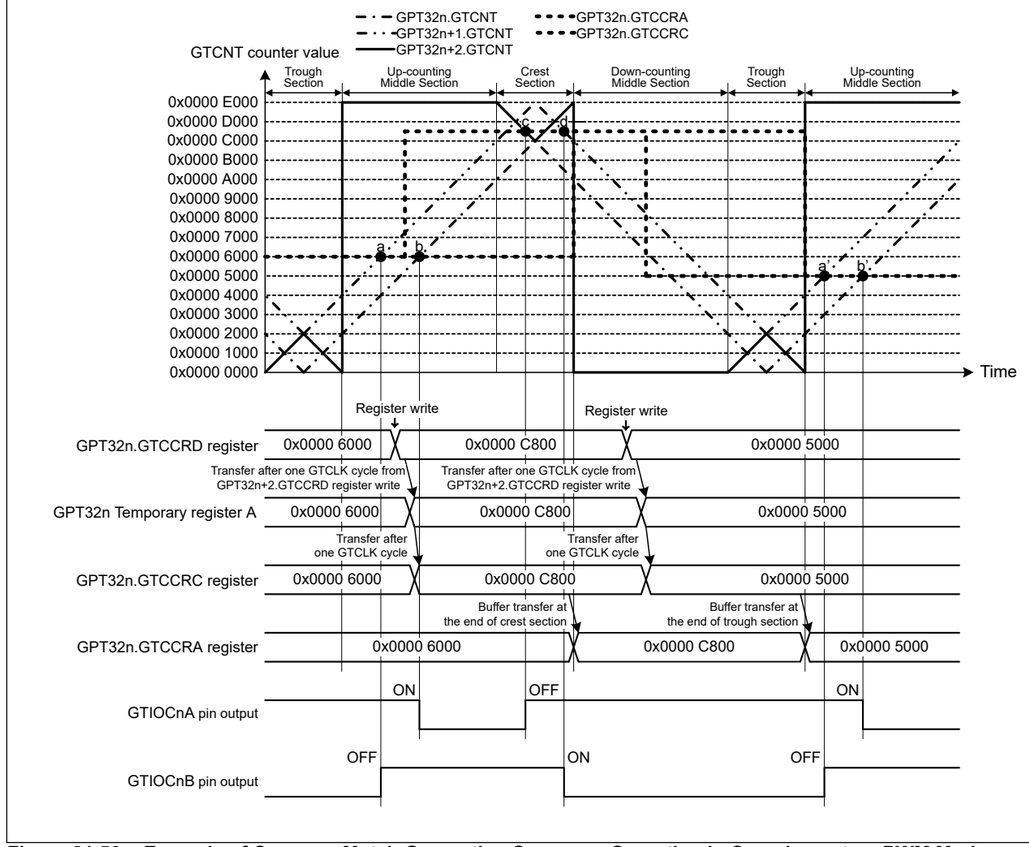


Figure 21.56 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: a → b → c → d) (n = 4, 7)

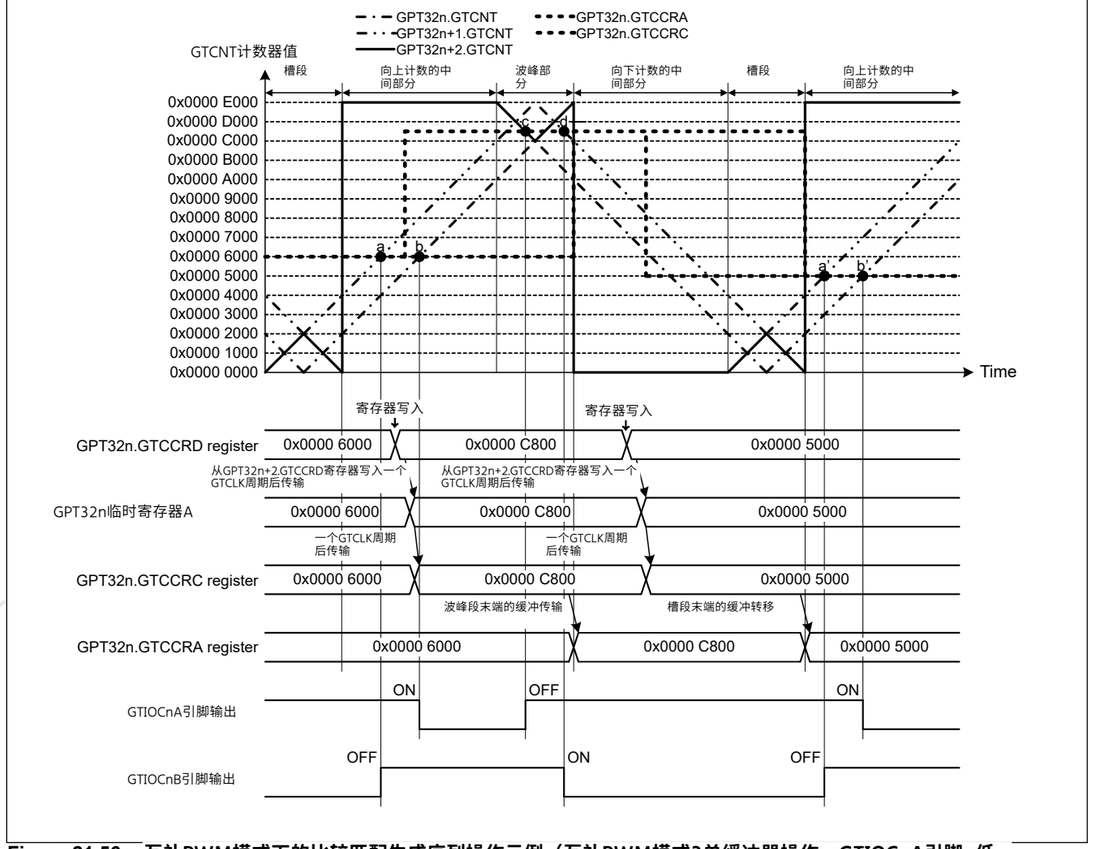


Figure 21.56 互补PWM模式下的比较匹配生成序列操作示例（互补PWM模式3单缓冲器操作，GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=GTCCRA寄存器比较时为低电平向下计数时匹配，死区时间值为0x00002000，比较匹配生成顺序：a→b→c→d)(n=4 7)

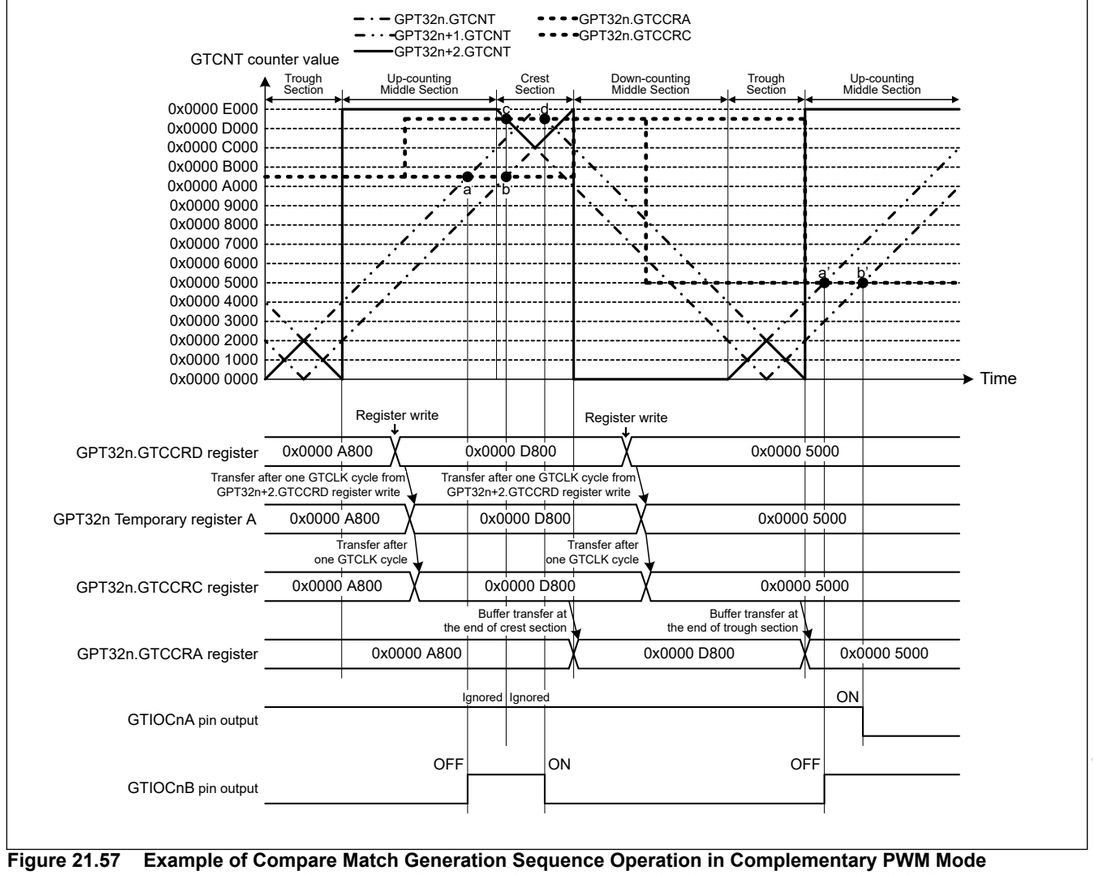


Figure 21.57 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: a → (b, c) → d) (n = 4, 7)

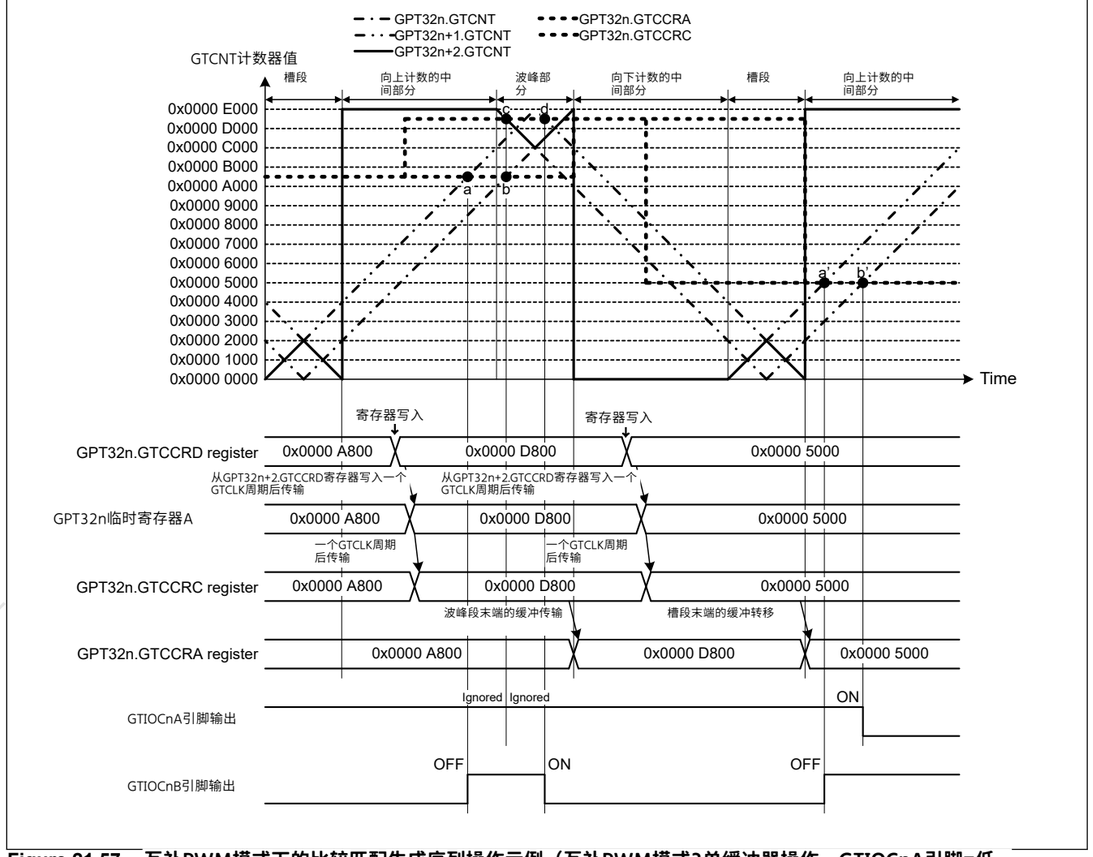


Figure 21.57 互补PWM模式下的比较匹配生成序列操作示例（互补PWM模式3单缓冲器操作，GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=GTCCRA寄存器比较时为低电平向下计数时匹配，死区时间值为0x00002000，比较匹配生成顺序：a→(b c)→d)(n=4 7)

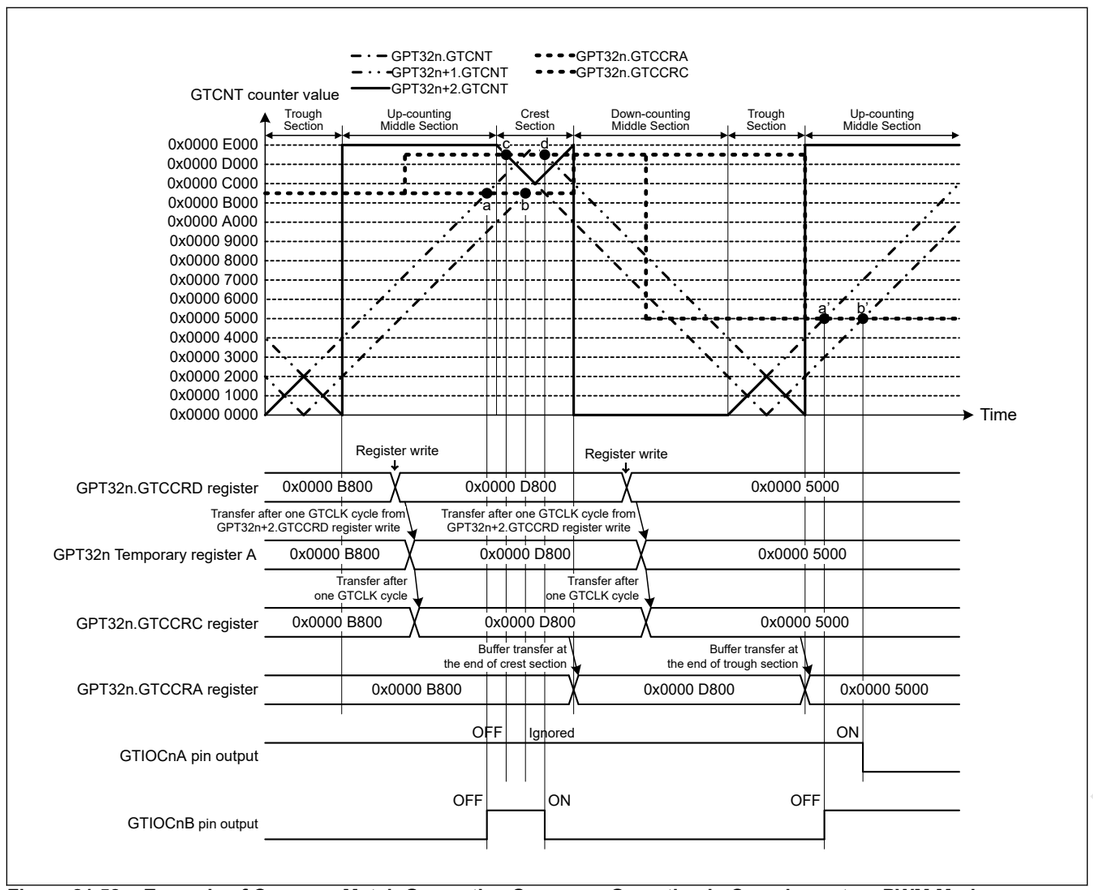


Figure 21.58 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: a → c → b → d) (n = 4, 7)

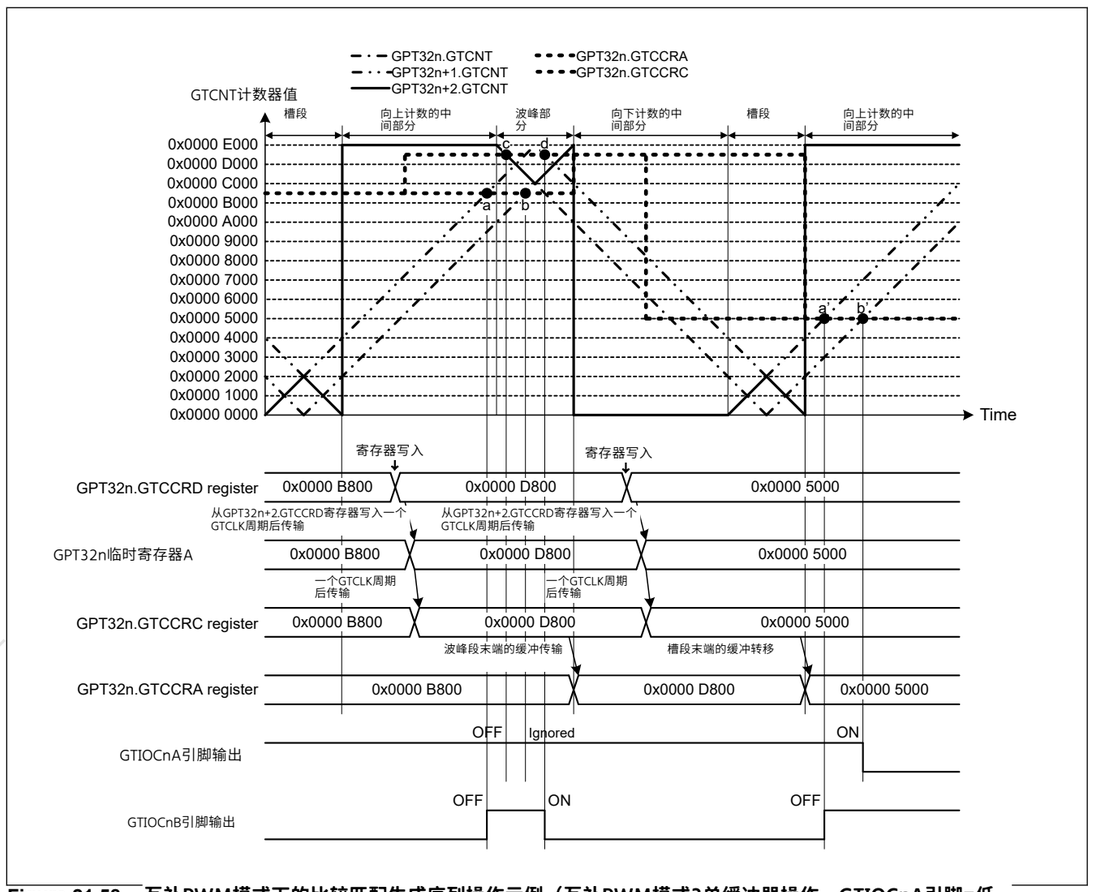


Figure 21.58 互补PWM模式下的比较匹配生成序列操作示例（互补PWM模式3单缓冲器操作，GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=GTCCRA寄存器比较时为低电平向下计数时匹配，死区时间值为0x00002000，比较匹配生成顺序：a→c→b→d)(n=4 7)

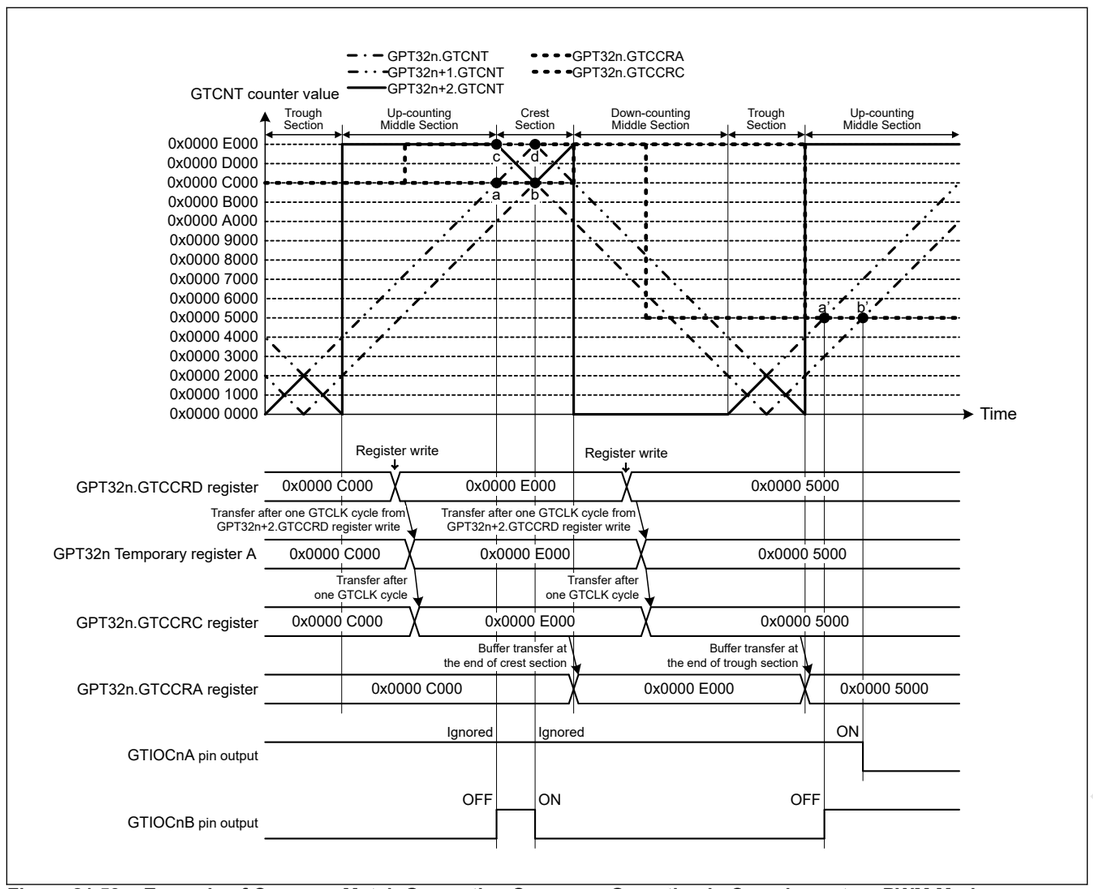


Figure 21.59 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: (a, c) → (b, d)) (n = 4, 7)

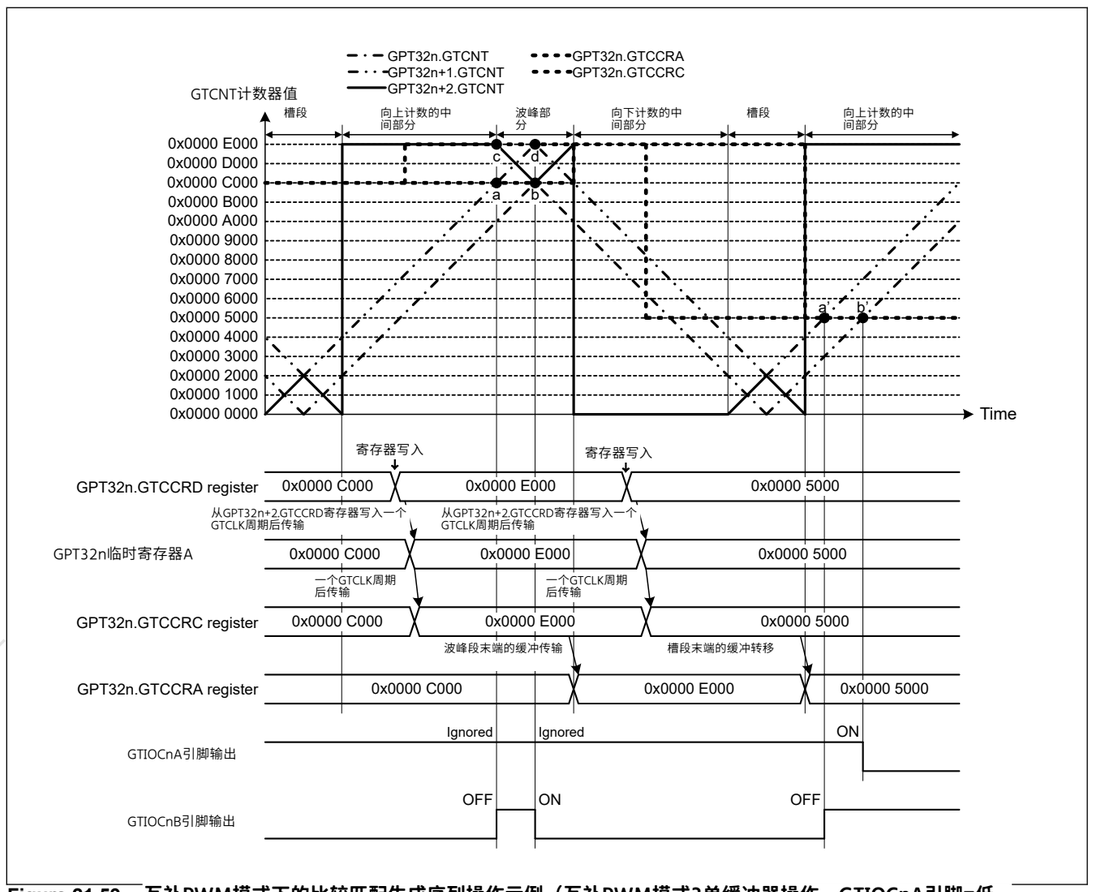


Figure 21.59 互补PWM模式下的比较匹配生成序列操作示例（互补PWM模式3单缓冲器操作，GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=GTCCRA寄存器比较时为低电平向下计数时匹配，死区时间值为0x00002000，比较匹配生成顺序：(a c)→(b d))(n=4 7)

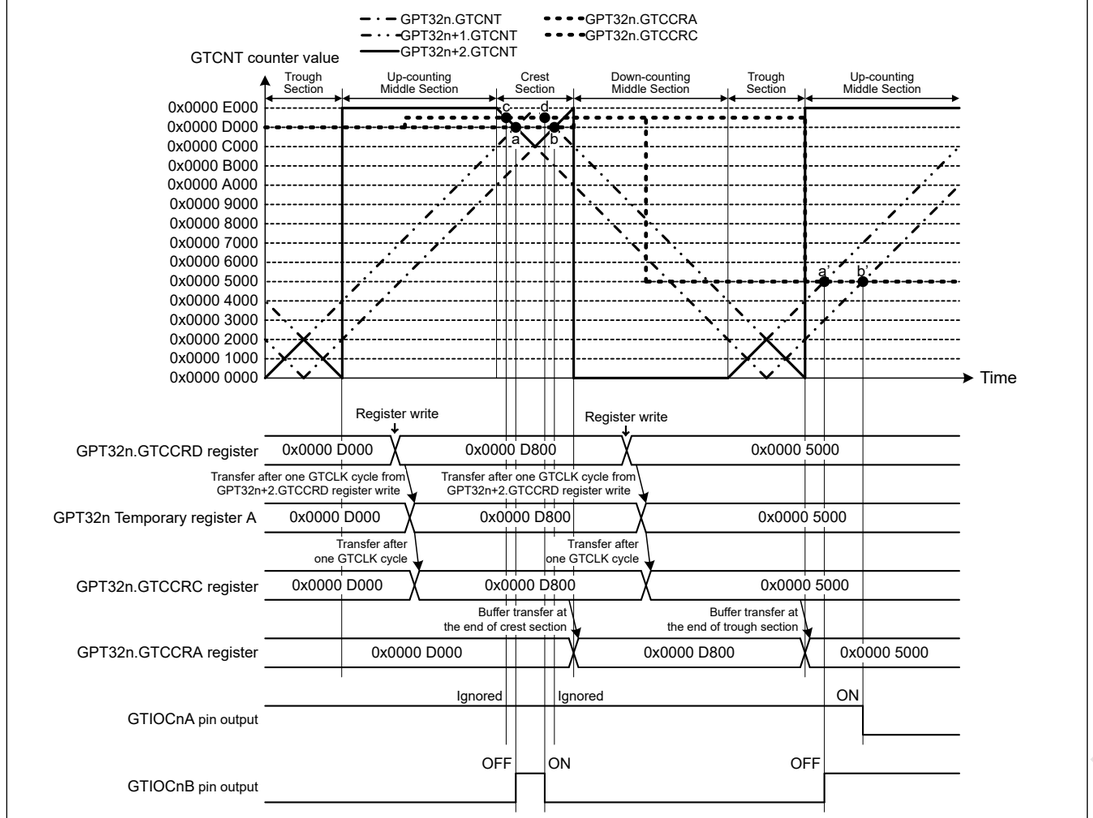


Figure 21.60 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: c → a → d → b) (n = 4, 7)

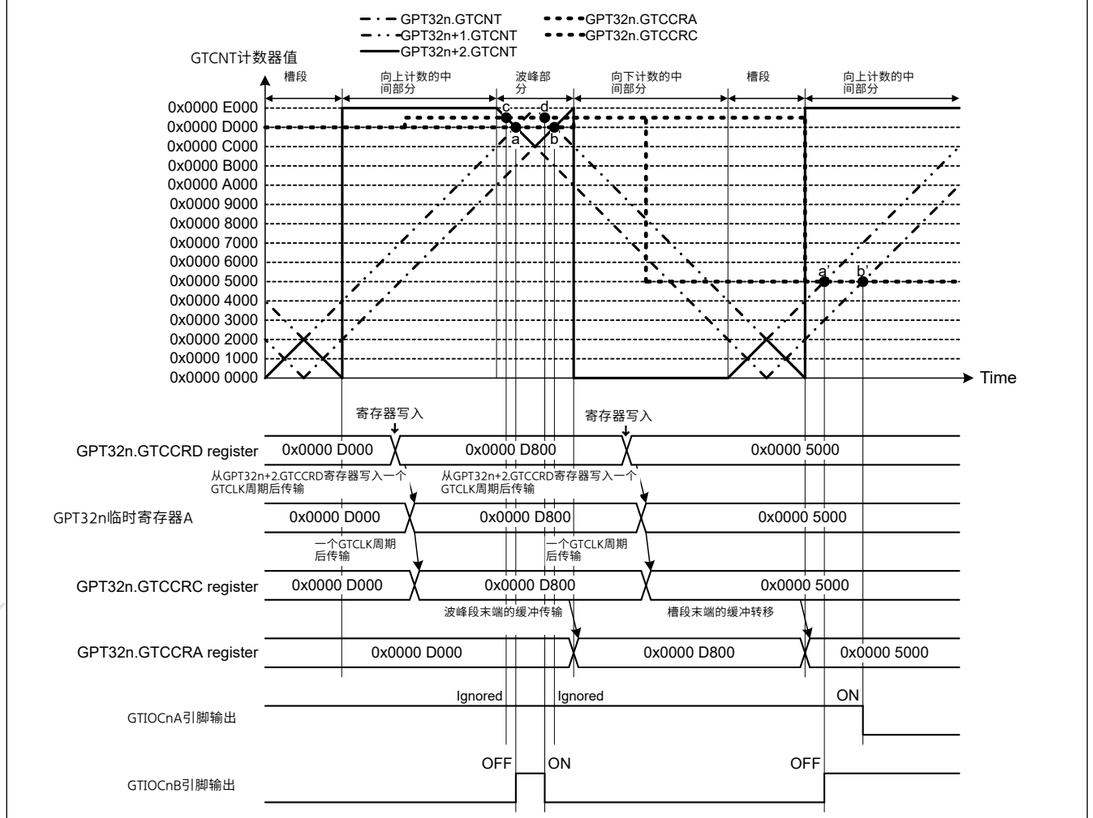


Figure 21.60 互补PWM模式下的比较匹配生成序列操作示例（互补PWM模式3单缓冲器操作，GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=GTCCRA寄存器比较时为低电平向下计数时匹配，死区时间值为0x00002000，比较匹配生成顺序：c→a→d→b)(n=4 7)

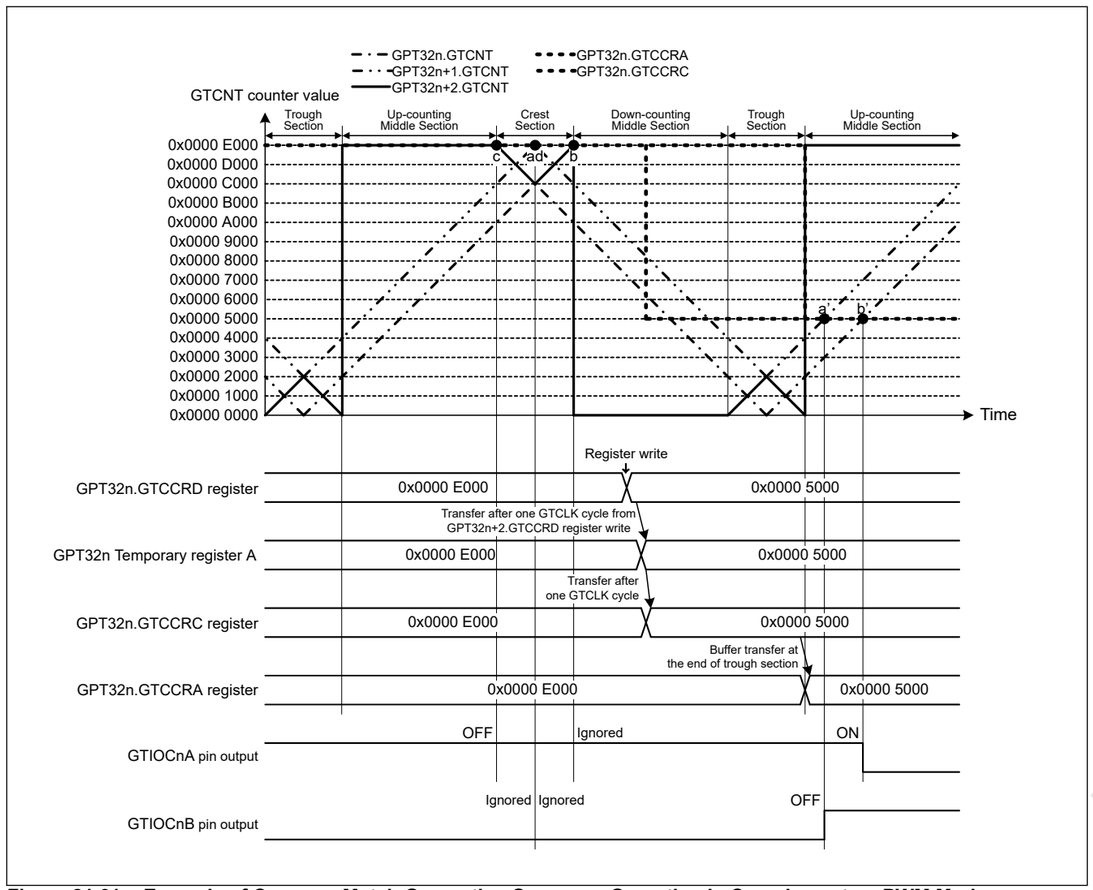


Figure 21.61 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: c → (a, d) → b) (n = 4, 7)

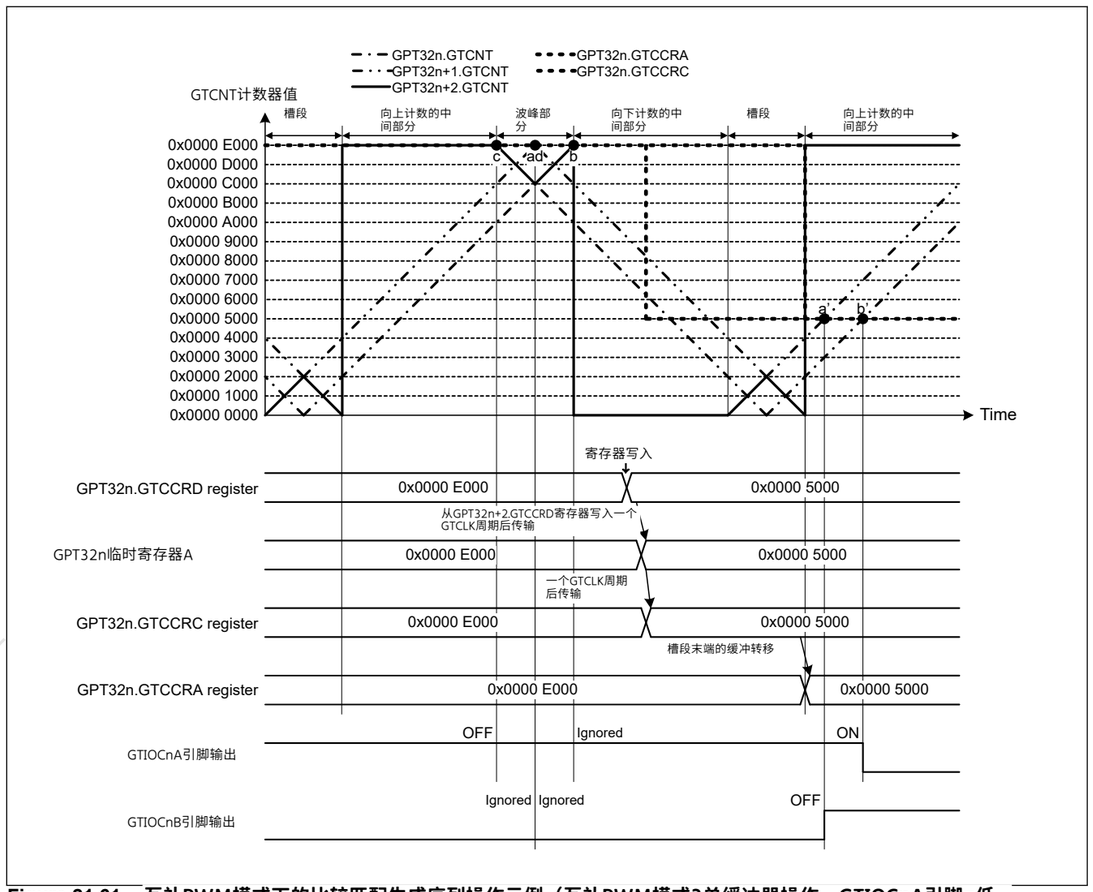


Figure 21.61 互补PWM模式下的比较匹配生成序列操作示例（互补PWM模式3单缓冲器操作，GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=GTCCRA寄存器比较时为低电平向下计数时匹配，死区时间值为0x00002000，比较匹配生成顺序：c→(a d)→b)(n=4 7)

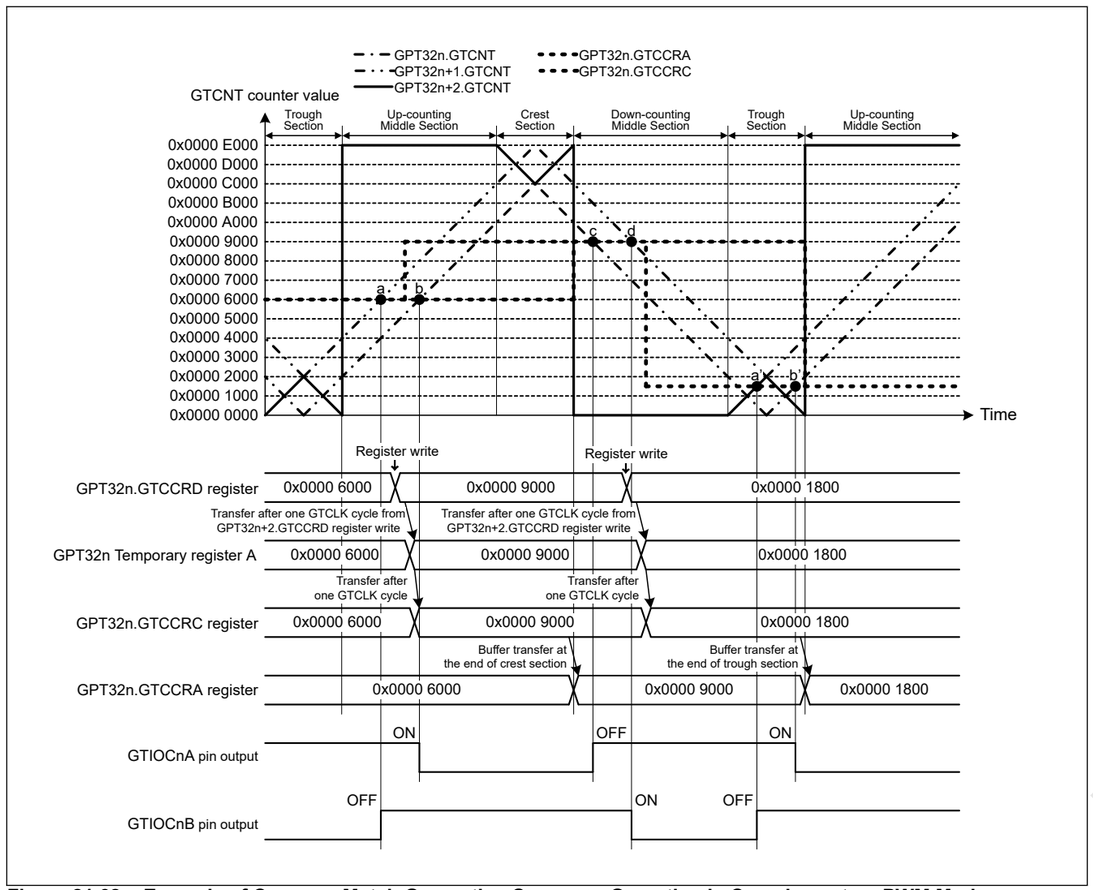


Figure 21.62 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: c → d → a' → b') (n = 4, 7)

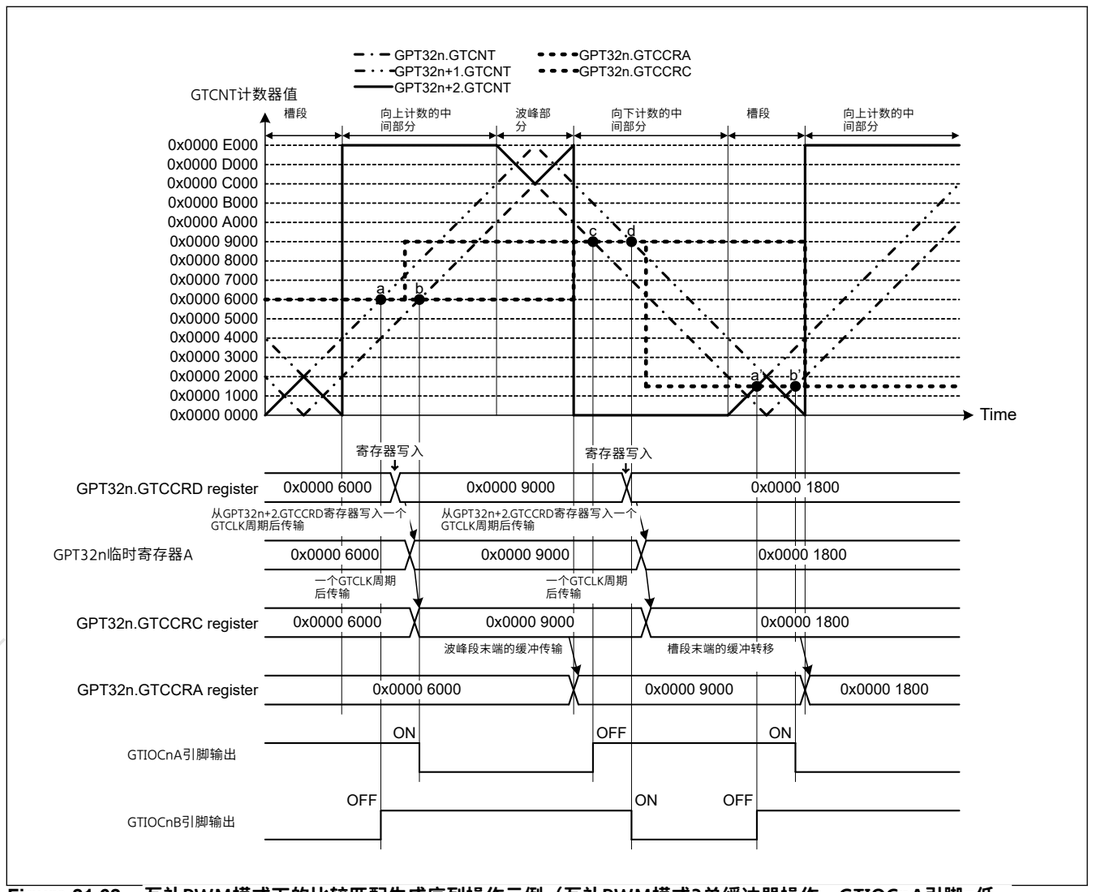


Figure 21.62 互补PWM模式下的比较匹配生成序列操作示例（互补PWM模式3单缓冲器操作，GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=GTCCRA寄存器比较时为低电平向下计数时匹配，死区时间值为0x00002000，比较匹配生成顺序：c→d→a'→b')(n=4 7)

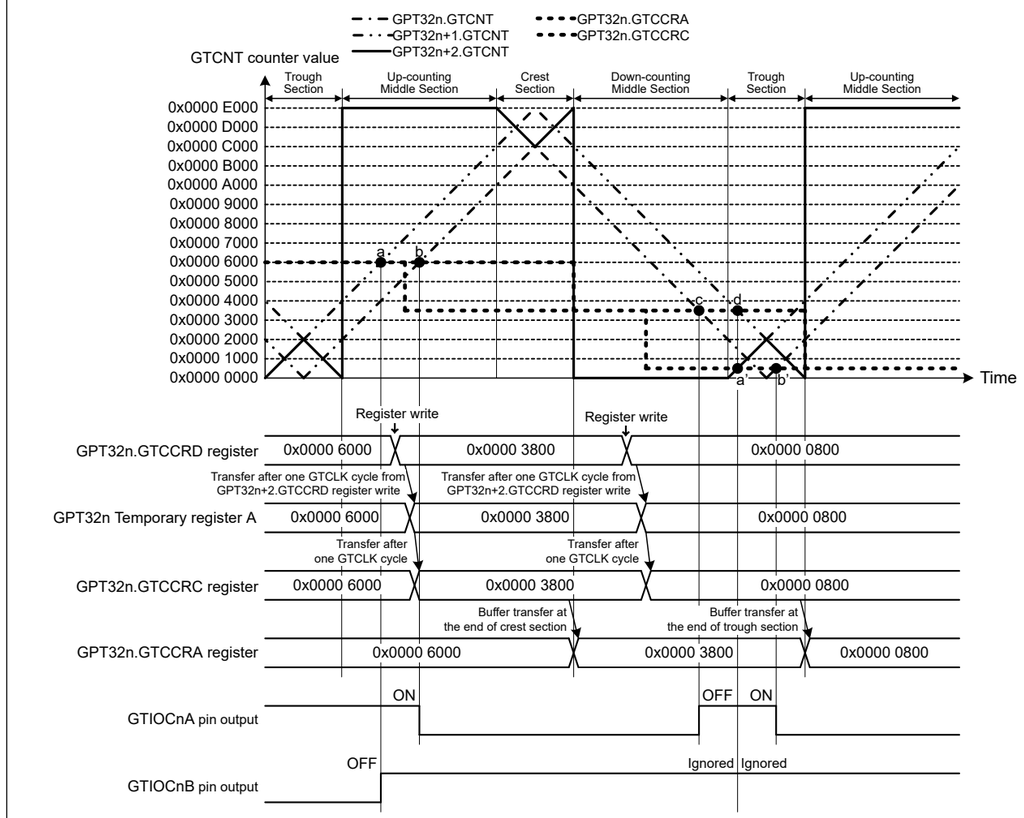


Figure 21.63 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: c → (d, a') → b') (n = 4, 7)

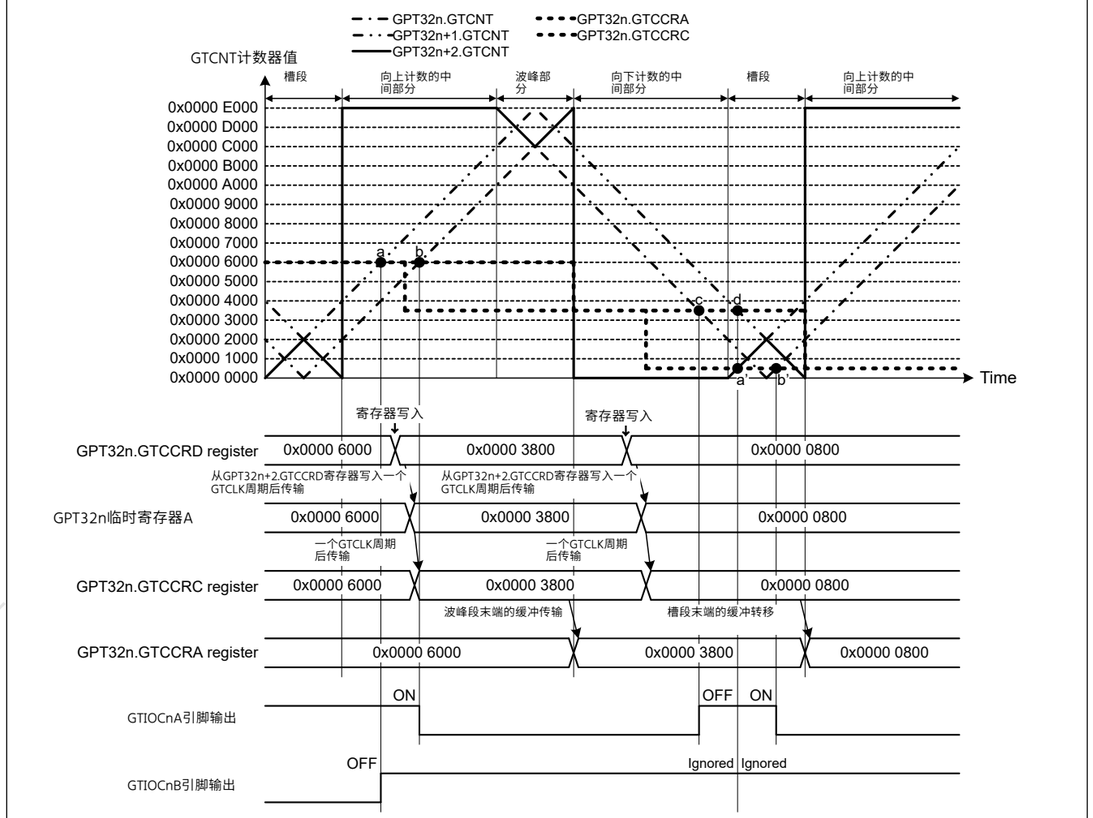


Figure 21.63 互补PWM模式下的比较匹配生成序列操作示例（互补PWM模式3单缓冲器操作，GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=GTCCRA寄存器比较时为低电平向下计数时匹配，死区时间值为0x00002000，比较匹配生成顺序：c→(d a')→b')(n=4 7)

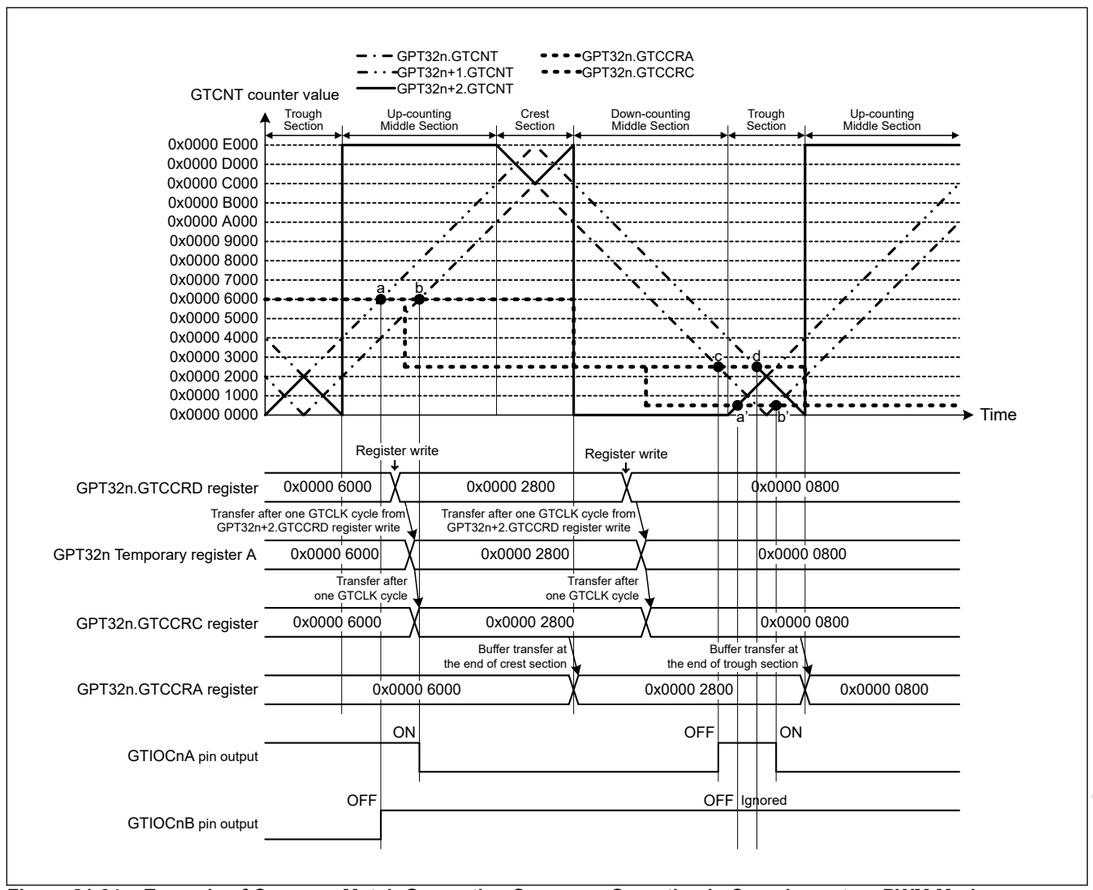


Figure 21.64 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: c → a' → d → b') (n = 4, 7)

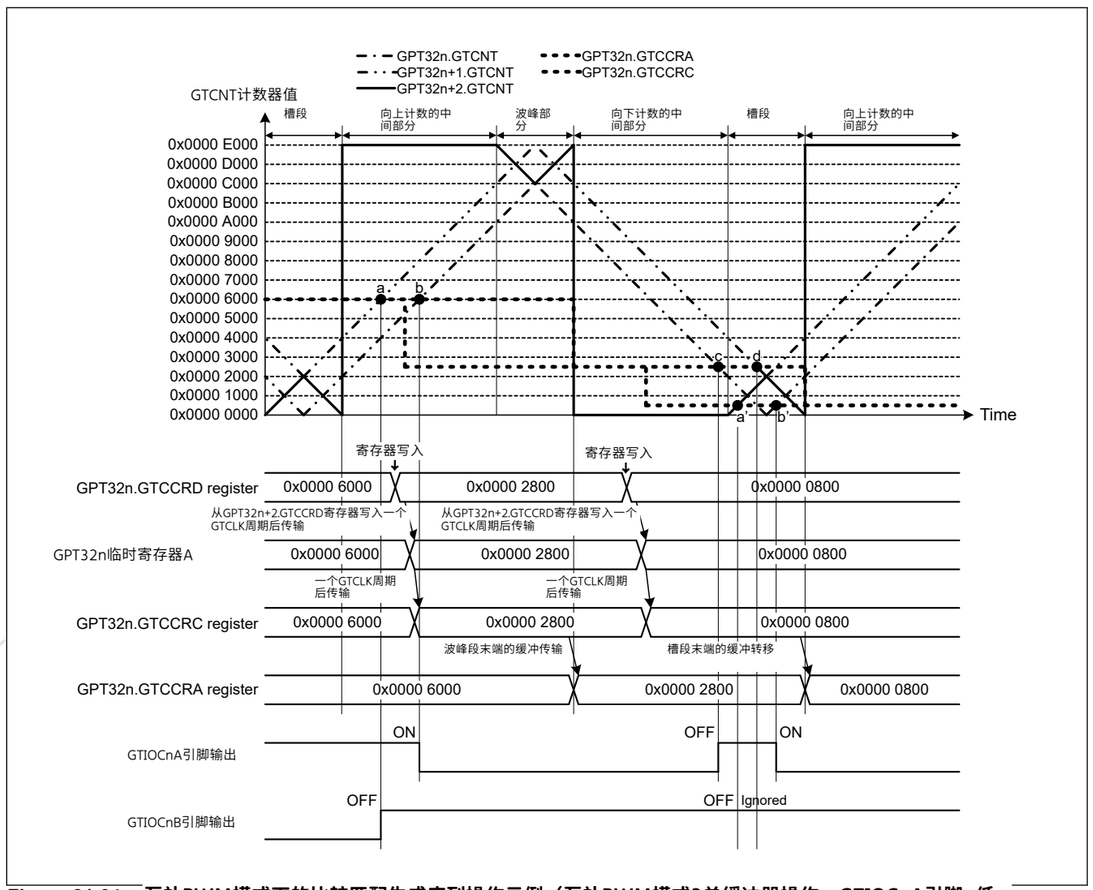


Figure 21.64 互补PWM模式下的比较匹配生成序列操作示例（互补PWM模式3单缓冲器操作，GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=GTCCRA寄存器比较时为低电平向下计数时匹配，死区时间值为0x00002000，比较匹配生成顺序：c→a'→d→b')(n=4 7)

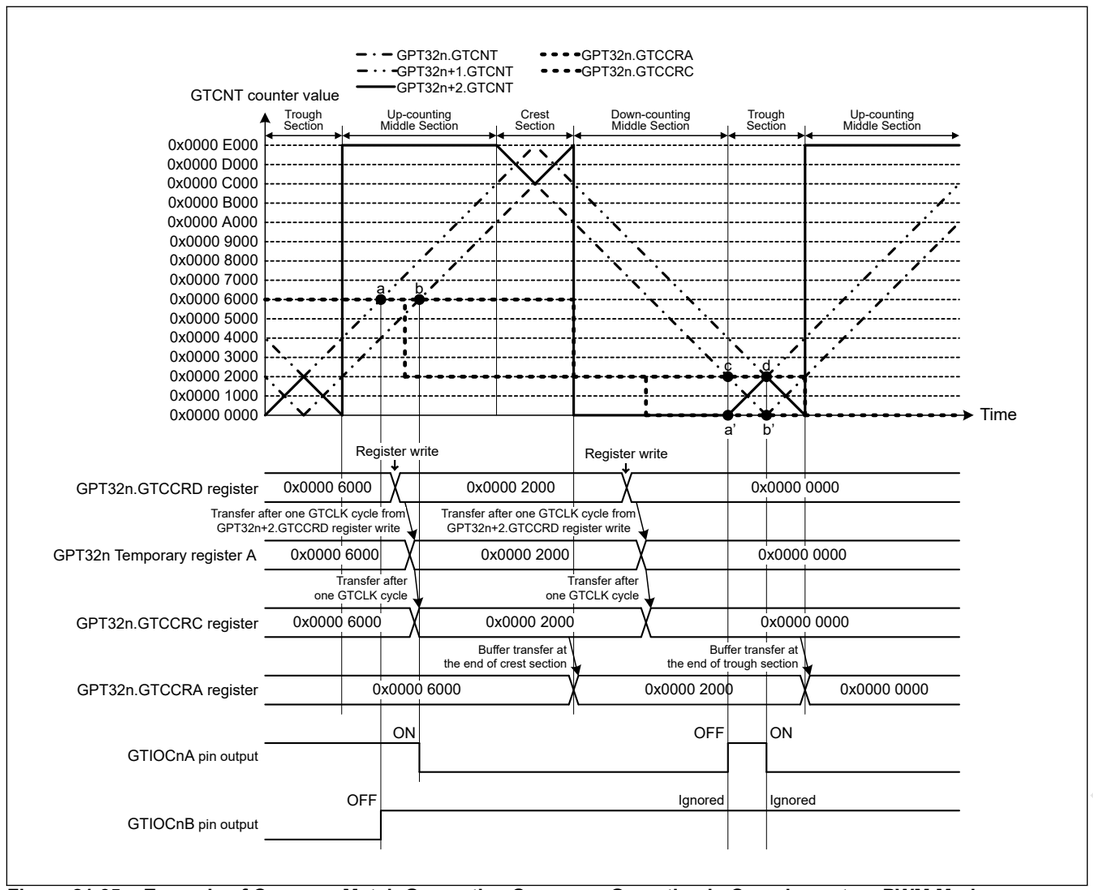


Figure 21.65 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: (c, a') → (d, b')) (n = 4, 7)

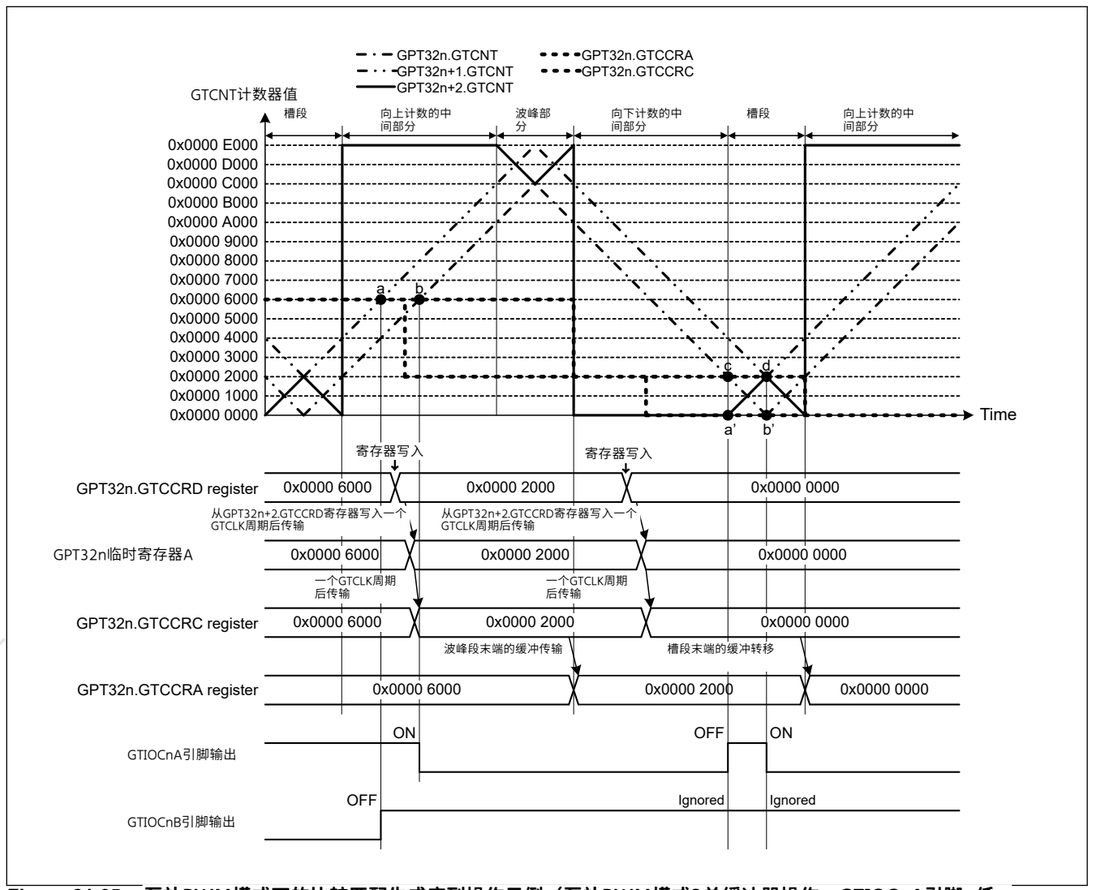


Figure 21.65 互补PWM模式下的比较匹配生成序列操作示例（互补PWM模式3单缓冲器操作，GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=GTCCRA寄存器比较时为低电平向下计数时匹配，死区时间值为0x00002000，比较匹配生成顺序：(c a')→(d b'))(n=4 7)

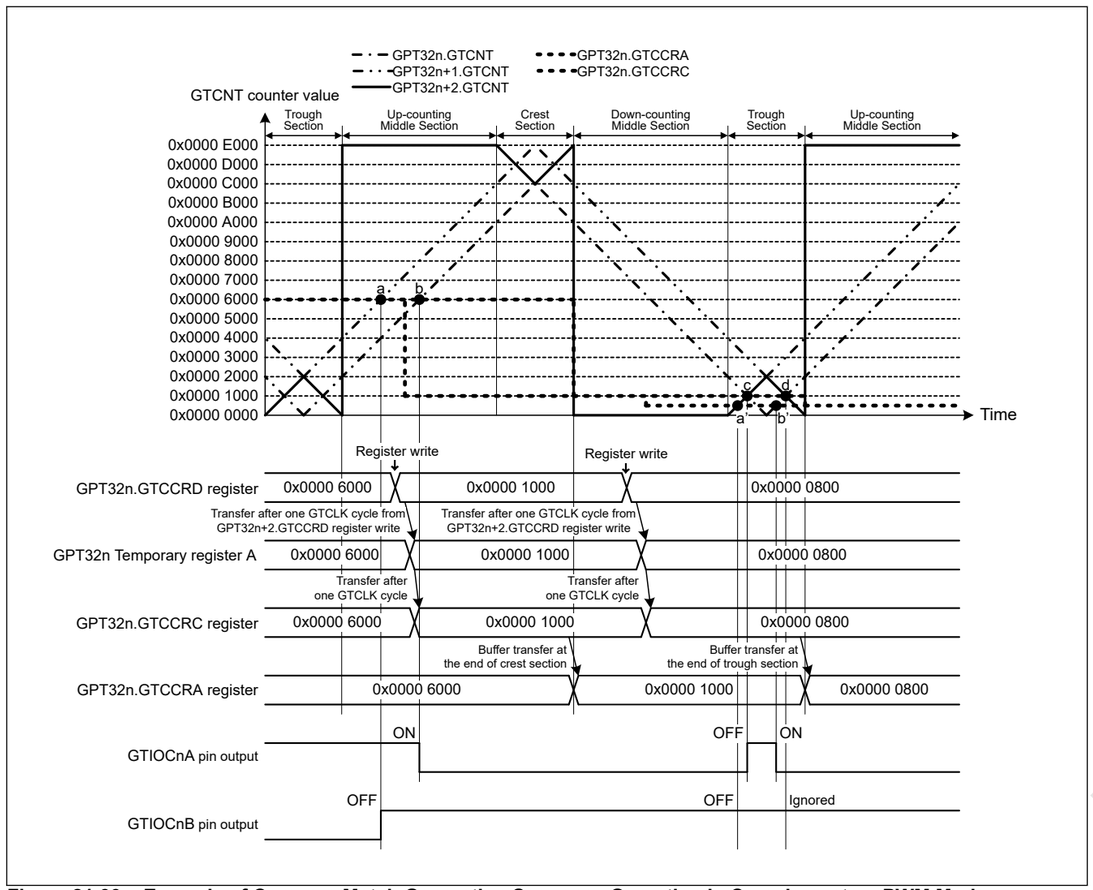


Figure 21.66 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: a' → c → b' → d) (n = 4, 7)

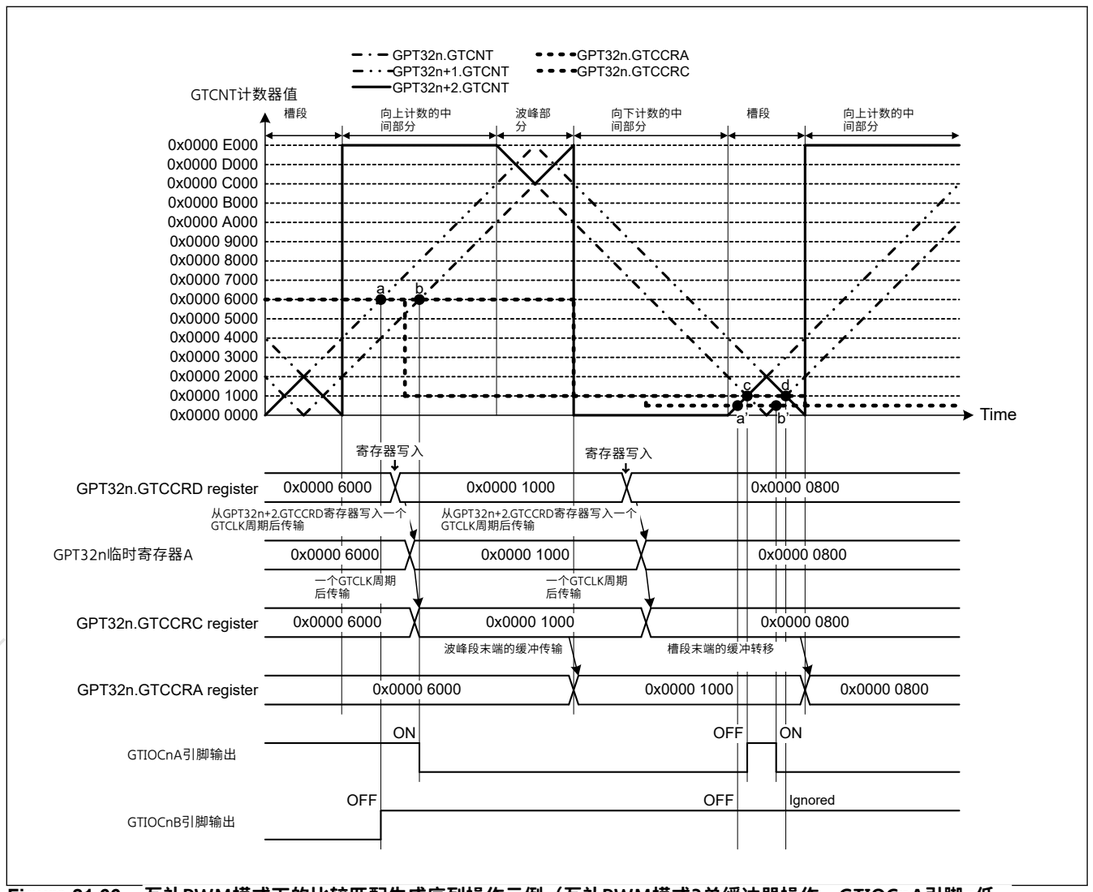


Figure 21.66 互补PWM模式下的比较匹配生成序列操作示例（互补PWM模式3单缓冲器操作，GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=GTCCRA寄存器比较时为低电平向下计数时匹配，死区时间值为0x00002000，比较匹配生成顺序：a'→c→b'→d)(n=4 7)

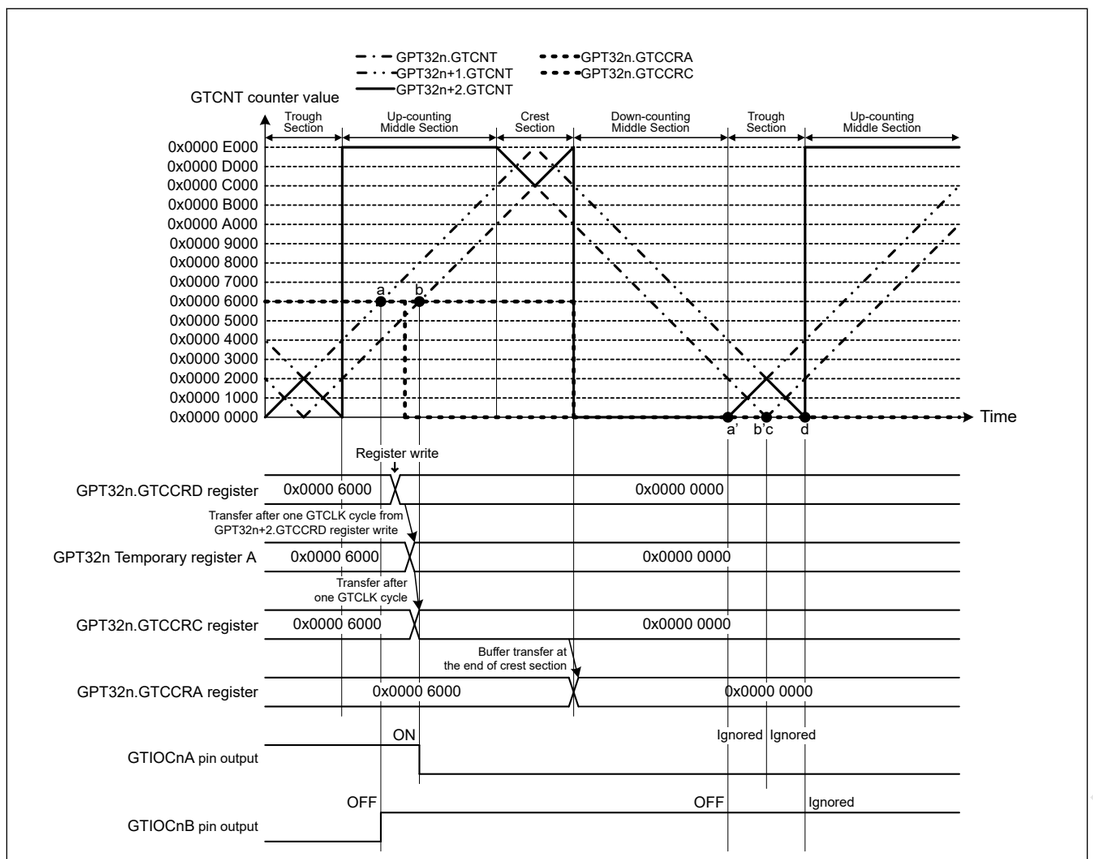


Figure 21.67 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: a' → (b', c) → d) (n = 4, 7)

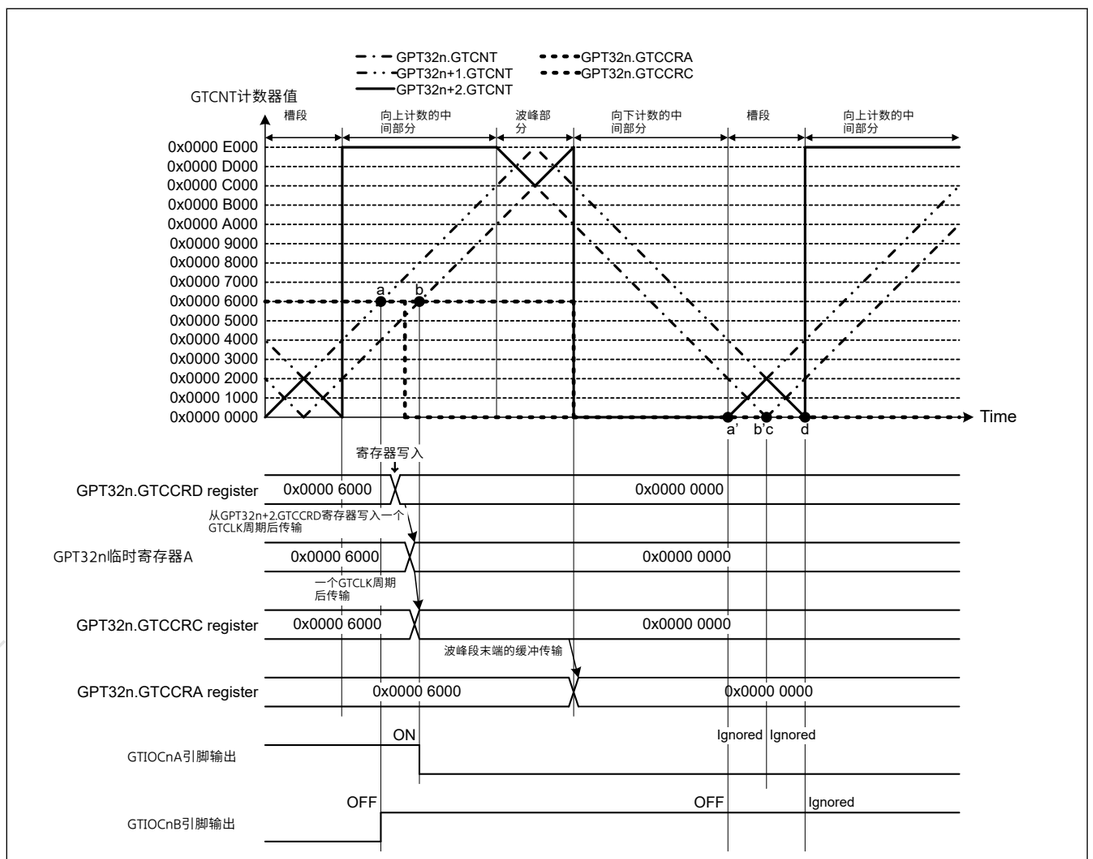


Figure 21.67 互补PWM模式下的比较匹配生成序列操作示例（互补PWM模式3单缓冲器操作，GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=GTCCRA寄存器比较时为低电平向下计数时匹配，死区时间值为0x00002000，比较匹配生成顺序：a'→(b' c)→d)(n=4 7)

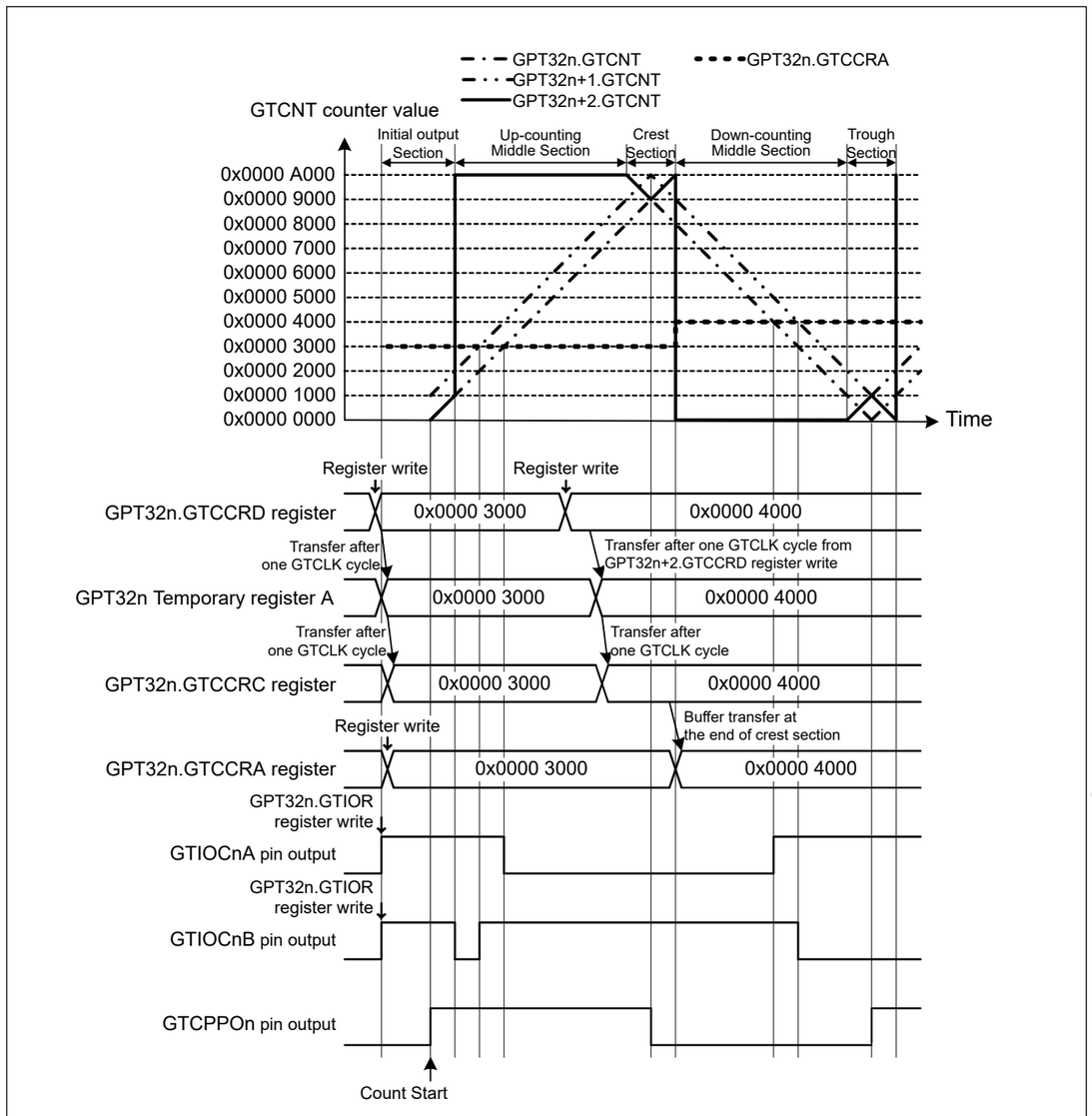


Figure 21.68 Example of Complementary PWM Mode Initial Output Operation (Complementary PWM mode 1 operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000, in the case that the initial GTCCRA register value is larger than the dead time value) (n = 4, 7)

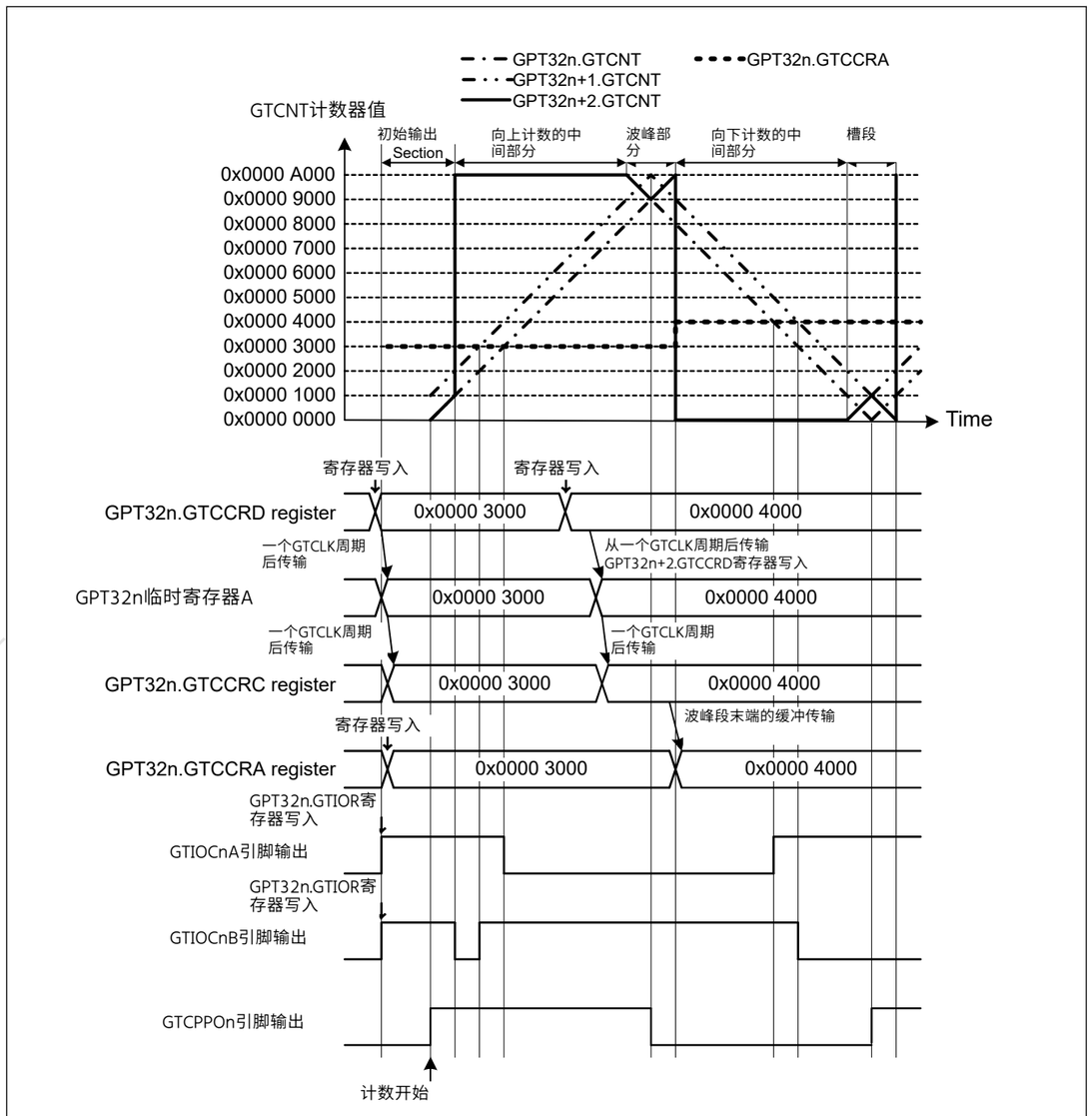


Figure 21.68 互补PWM模式初始输出操作示例（互补PWM模式1操作，GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=递减计数期间GTCCRA寄存器比较匹配时为低电平，死区时间值为0x00001000，在GTCCRA寄存器初始值大于死区时间值的情况下）（n=4 7）

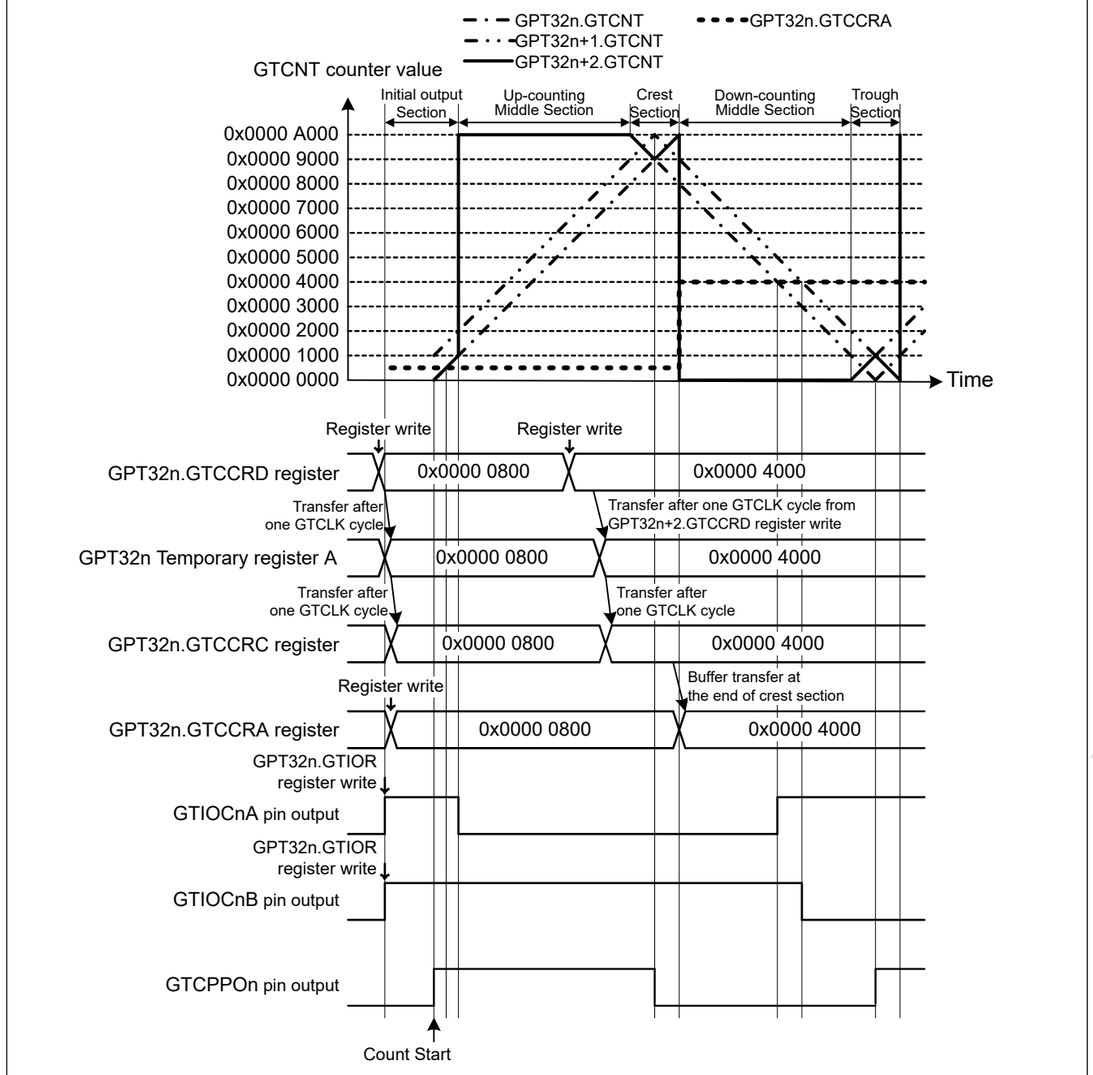


Figure 21.69 Example of Complementary PWM Mode Initial Output Operation (Complementary PWM mode 1 operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000, in the case that the initial GTCCRA register value is equal to or less than the dead time value) (n = 4, 7)

Table 21.35 Example for Setting Complementary PWM Mode 1,2,3 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[3:0] bits of GTP32n channel.
2	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits of GPT32n channel.
3	Set cycle	Set the cycle in GTPR of GPT32n channel.
4	Set GTIOCnm /GTIOCn+1m / GTIOCn+2m pin function	Set the function of the GTIOCnm, GTIOCn+1m, and GTIOCn+2m pins with GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register of the GPT32n, GPT32n+1, and GPT32n+2 channels.

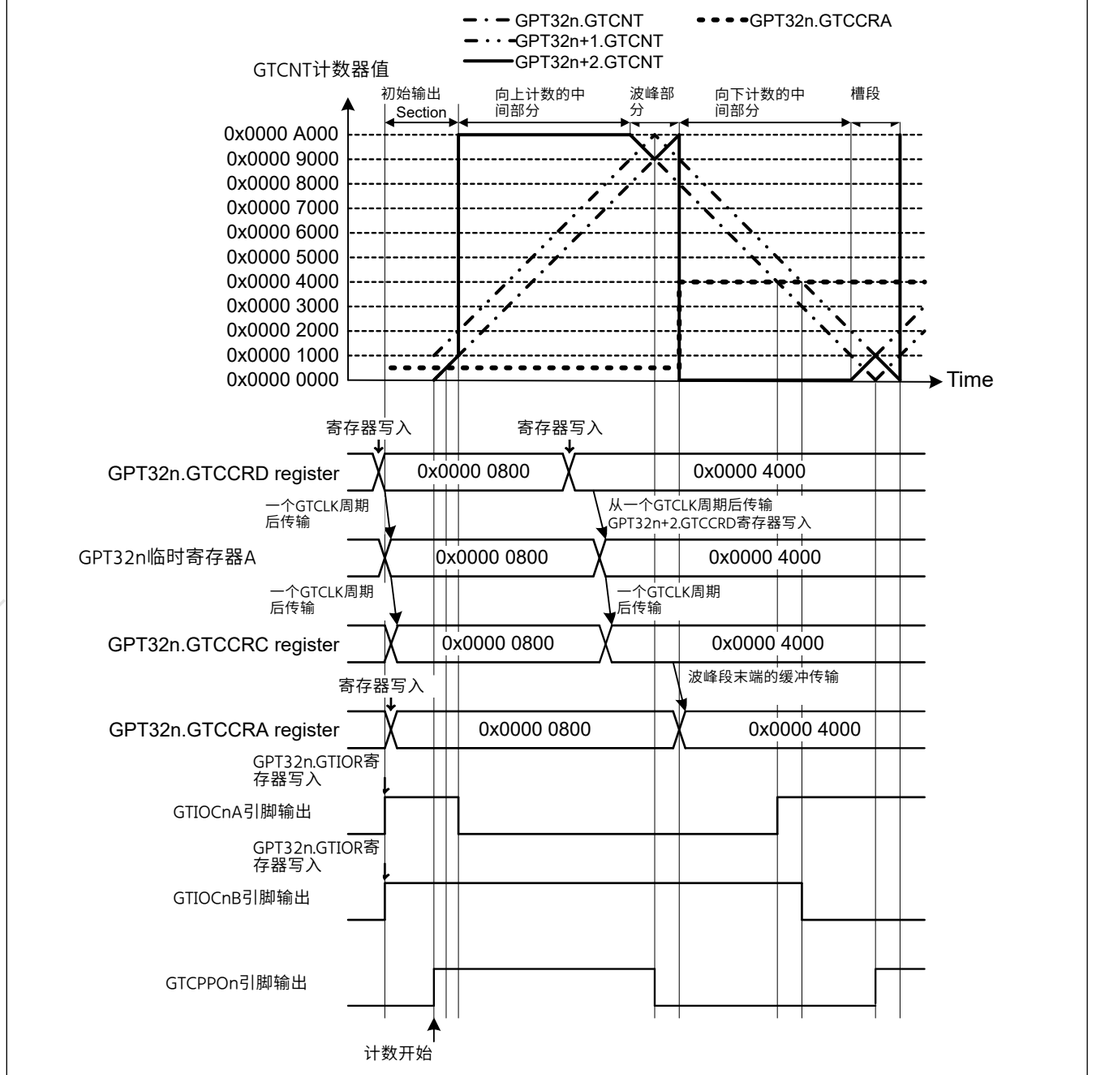


Figure 21.69 互补PWM模式初始输出操作示例（互补PWM模式1操作，GTIOCnA引脚=低电平GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=递减计数期间GTCCRA寄存器比较匹配时为低电平，死区时间值为0x00001000，在GTCCRA寄存器初始值等于或小于死区时间值的情况下）（n=4 7）

Table 21.35 设置互补PWM模式的示例1 2 3(1of2)

No.	步骤名称	Description
1	设置操作模式	使用GTP32n通道的GTCR.MD[3:0]位设置工作模式。
2	选择计数时钟	使用GPT32n通道的GTCR.TPCS[3:0]位选择计数时钟。
3	设置周期	在GPT32n通道的GTPR中设置周期。
4	Set GTIOCnm /GTIOCn+1m / GTIOCn+2m引脚功能	通过GPT32n、GPT32n+1和GPT32n+2通道的GTIOR寄存器中的GTIOA[4:0]和GTIOB[4:0]位设置GTIOCnm、GTIOCn+1m和GTIOCn+2m引脚的功能。

Table 21.35 Example for Setting Complementary PWM Mode 1,2,3 (2 of 2)

No.	Step Name	Description
5	Enable GTCPPOn pin output	Set to enable or disable PWM synchronous output from the GTCPPOn pin with the PSYE bit in the GTIOR register of the GPT32n channel.
6	Enable GTIOCnm /GTIOCn +1m /GTIOCn+2m pin output	Set to enable the output from the GTIOCnm, GTIOCn+1m, and GTIOCn+2m pins with the OAE and OBE bits in the GTIOR register of the GPT32n, GPT32n+1, and GPT32n+2 channels.
7	Set buffer operation	In complementary PWM mode 3, set buffer operation with the GTBER2.CP3DB bit of the GPT32n, GPT32n+1, and GPT32n+2 channels.
8	Set compare match value	Set the output pin changing point during up-counting after count start in the GTCCRA register of the GPT32n, GPT32n+1, and GPT32n+2 channels.
9	Set buffer value	For single buffer operation, set data (to be transferred for the first buffer transfer to the GTCCRA register after count start) in the GTCCRD register. For buffer operation in complementary PWM mode 2, set the same value as the GTCCRA register in the GTCCRD register because the first buffer transfer does not take place. For double buffer operation in complementary PWM mode 3, set data to be transferred at the first end of crest in the GTCCRD register and set data to be transferred at the first end of trough in the GTCCRF register.
10	Set dead time value	Set the dead time value in GTDVU of GTP32n channel.
11	Start count operation	Set GTCR.CST of GPT32n channel to 1 to start count operation.
12	Set buffer value for each cycle	For single buffer operation, set data (to be transferred for the next buffer transfer to the GTCCRA register) in the GTCCRD register. For double buffer operation in complementary PWM mode 3, set data to be transferred for the next buffer transfer in the GTCCRF register. Make settings for the GPT32n+2.GTCCRD register finally. (Data is transferred to the temporary register.)

Note: n = 4, 7
m = A, B

21.3.3.8 Complementary PWM mode 4

In complementary PWM mode 4, the value written to the GTCCRD and GTCCRF registers is immediately applied to compare match operation by transferring data also to the GTCCRA register during buffer transfer to a temporary register before crest or trough transfer timing.

Figure 21.70 shows the block diagram in complementary PWM mode 4.

In the configuration of complementary PWM mode 4, a buffer transfer path from the GTCCRD register to the GTCCRC and GTCCRA registers and a buffer transfer path from the GTCCRF register to the GTCCRE and GTCCRA registers are added to other complementary PWM modes shown in Table 21.35.

Table 21.35 设置互补PWM模式的示例1 2 3(2of2)

No.	步骤名称	Description
5	启用GTCPPOn引脚输出	通过GTCPPOn引脚的PSYE位设置启用或禁用PWM同步输出 GPT32n通道的GTIOR寄存器。
6	使能GTIOCnmGTIOCn+1mGTIOCn+2m管脚输出	使用GPT32n、GPT32n+1和GPT32n+2通道的GTIOR寄存器中的OAE和OBE位设置以启用GTIOCnm、GTIOCn+1m和GTIOCn+2m引脚的输出。
7	设置缓冲操作	在互补PWM模式3中，使用GPT32n的GTBER2.CP3DB位设置缓冲区操作， GPT32n+1和GPT32n+2通道。
8	设置比较匹配值	在GPT32n、GPT32n+1和GPT32n+2通道的GTCCRA寄存器中设置计数开始后向上计数期间的输出引脚变化点。
9	设置缓冲区值	对于单缓冲区操作，在GTCCRD寄存器中设置数据（在计数开始后第一次缓冲区传输到GTCCRA寄存器时要传输的数据）。对于互补PWM模式2中的缓冲区操作，在GTCCRD寄存器中设置与GTCCRA寄存器相同的值，因为第一次缓冲区传输不会发生。对于互补PWM模式3中的双缓冲器操作，在GTCCRD寄存器中设置要在波峰的第一端传输的数据，在GTCCRF寄存器中设置要在波谷的第一端传输的数据。
10	设置死区时间值	在GTP32n通道的GTDVU中设置死区时间值。
11	开始计数操作	将GPT32n通道的GTCR.CST设置为1，开始计数操作。
12	为每个周期设置缓冲区值	对于单缓冲区操作，在GTCCRD寄存器中设置数据（为下一次缓冲区传输到GTCCRA寄存器而传输）。对于互补PWM模式3中的双缓冲器操作，在GTCCRF寄存器中设置要传输的数据以进行下一次缓冲器传输。最后对GPT32n+2.GTCCRD寄存器进行设置。（数据被传送到临时寄存器。）

Note: n = 4, 7
m = A, B

21.3.3.8 互补PWM模式4

在互补PWM模式4中，写入GTCCRD和GTCCRF寄存器的值立即应用于比较匹配操作，方法是在波峰或波谷传输时序之前的缓冲区传输期间将数据也传输到GTCCRA寄存器。

图21.70显示了互补PWM模式4的框图。

在互补PWM模式4的配置中，从GTCCRD寄存器到GTCCRC和GTCCRA寄存器的缓冲区传输路径以及从GTCCRF寄存器到GTCCRE和GTCCRA寄存器的缓冲区传输路径被添加到表21.35所示的其他互补PWM模式。

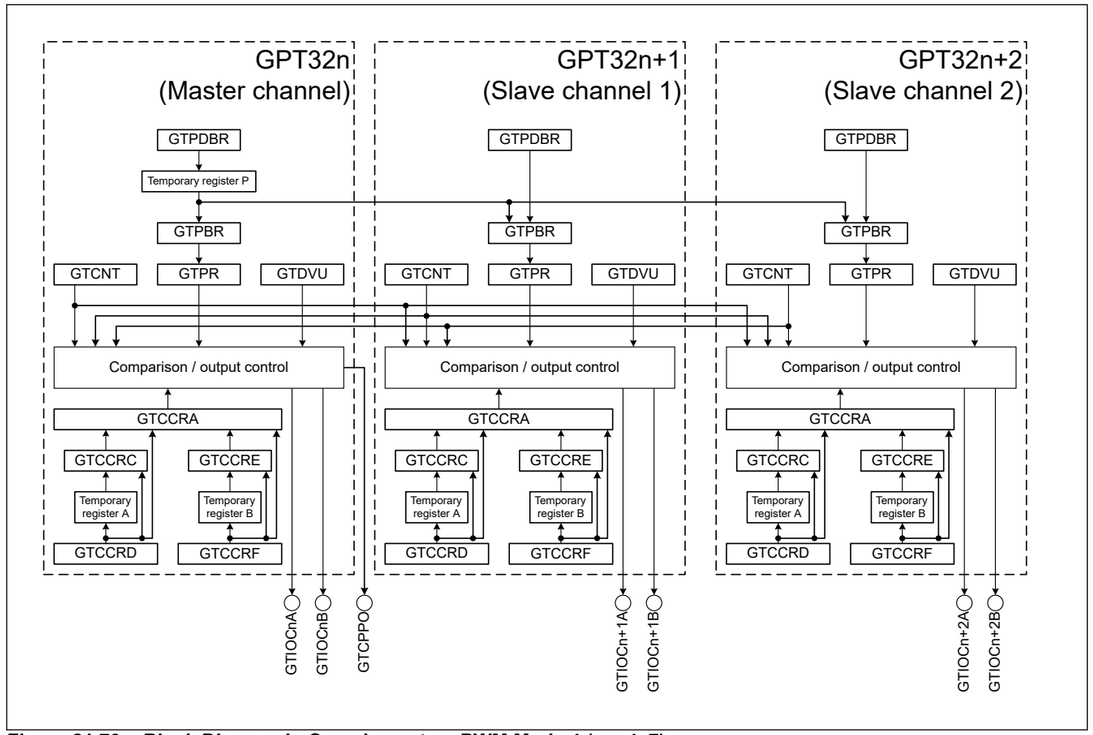


Figure 21.70 Block Diagram in Complementary PWM Mode 4 (n = 4, 7)

Count operation is performed in the same way as complementary PWM modes 1 to 3. See Table 21.30 and Table 21.31.

With respect to buffer operation and PWM waveform changes in complementary PWM mode 4, buffer transfer (shown in Figure 21.70) from the GTCCRD and GTCCRF registers is added based on the complementary PWM mode 3 operation. Buffer transfer and PWM waveform are controlled according to operation section, state of comparison with the GTCCRA register, and write value.

The double buffer function by writing to the GTCCRF register can be enabled or disabled with the GTBER2.CP3DB bit. In double buffer operation, the value written to the GTCCRD register is used as a compare match value for positive-phase OFF (negative-phase ON) during down-counting, and the value written to the GTCCRF register is used as a compare match value for negative-phase OFF (positive-phase ON) during up-counting. Transfer register, transfer value, and PWM output changes are controlled by operation section (where the value is written), state of comparison with the GTCCRA register, and write value.

Double buffer operation is guaranteed only in the up-counting middle section and down-counting middle section. Setting a value not larger than the dead time value and not less than the count cycle is prohibited.

In single buffer operation, a compare match value is written only to the GTCCRD register, and transfer register, transfer value, and PWM output changes are controlled by operation section (where the value is written), state of comparison with the GTCCRA register, and write value.

Transfer from the GTCCRD register to the temporary register A and transfer from the GTCCRF register to the temporary register B are performed in the same way as other complementary PWM modes. Transfers are concurrently performed in three channels by writing a value to the GPT32n+2.GTCCRD register. Transfer from the GTCCRD register to the GTCCRC register, GTCCRA register, temporary register B, and GTCCRE register and transfer from the GTCCRF register to the GTCCRE register and the GTCCRA register are performed at the same time as the above-mentioned transfer to the temporary register.

Table 21.36 and Table 21.37 show immediate buffer transfer (for transfer to the temporary register by writing a value to the GPT32n+2.GTCCRD register) to the GTCCRC and GTCCRA registers by writing a value to the GTCCRD register during single buffer operation in complementary PWM mode 4 for each compare match state in each operation section. Transfers (from the GTCCRD register to the temporary register A, from the temporary register A to the GTCCRC register, and from

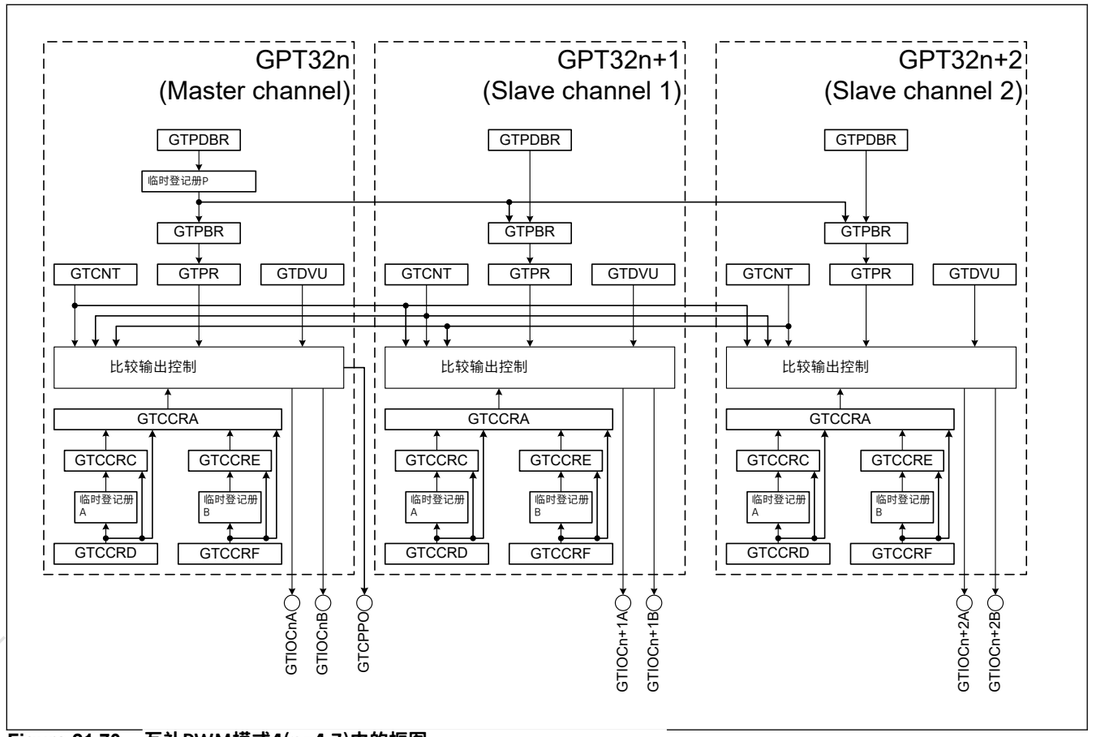


Figure 21.70 互补PWM模式4(n=4 7)中的框图

计数操作的执行方式与互补PWM模式1至3相同。请参见表21.30和表21.31。

关于互补PWM模式4中的缓冲器操作和PWM波形变化，基于互补PWM模式3操作添加了来自GTCCRD和GTCCRF寄存器的缓冲器传输（如图21.70所示）。缓冲区传输和PWM波形根据操作部分、与GTCCRA寄存器的比较状态和写入值进行控制。

可通过GTBER2.CP3DB位启用或禁用通过写入GTCCRF寄存器的双缓冲功能。在双缓冲操作中，写入GTCCRD寄存器的值在递减计数期间用作正相OFF（负相ON）的比较匹配值，写入GTCCRF寄存器的值用作比较匹配值向上计数时为负相关（正相开）。传输寄存器、传输值和PWM输出变化由操作部分（写入值的位置）、与GTCCRA寄存器的比较状态和写入值控制。

仅在向上计数中间段和向下计数中间段保证双缓冲操作。禁止设置不大于死区时间值且不小于计数周期的值。

在单缓冲器操作中，比较匹配值仅写入GTCCRD寄存器，传输寄存器、传输值和PWM输出变化由操作部分（写入值的位置）、与GTCCRA寄存器的比较状态以及写值。

从GTCCRD寄存器传送到临时寄存器A和从GTCCRF寄存器传送到临时寄存器B的执行方式与其他互补PWM模式相同。通过将值写入GPT32n+2.GTCCRD寄存器，在三个通道中同时执行传输。从GTCCRD寄存器到GTCCRC寄存器、GTCCRA寄存器、临时寄存器B和GTCCRE寄存器的传送以及从GTCCRF寄存器到GTCCRE寄存器和GTCCRA寄存器的传送与上述到临时寄存器的传送同时进行.

表21.36和表21.37显示了在互补PWM中的单缓冲区操作期间，通过向GTCCRD寄存器写入值来立即将缓冲区传输（通过向GPT32n+2.GTCCRD寄存器写入值来传输到临时寄存器）到GTCCRD和GTCCRA寄存器模式4用于每个操作部分中的每个比较匹配状态。传输（从GTCCRD寄存器到临时寄存器A，从临时寄存器A到GTCCRC寄存器，从

the GTCCRC register to the GTCCRA register) other than those shown in Table 21.36 and Table 21.37 are the same as single buffer transfer in complementary PWM mode 3 shown in Table 21.32.

Table 21.38 and Table 21.39 show immediate buffer transfer (for transfer to the temporary register by writing a value to the GPT32n+2.GTCCRD register) to each register by writing a value to the GTCCRD and GTCCRF registers during double buffer operation in complementary PWM mode 4 for each compare match state in each operation section. Transfers (from the GTCCRD register to the temporary register A, from the GTCCRF register to the temporary register B, from the temporary register A to the GTCCRC register, from the temporary register B to the GTCCRE register, and from the GTCCRC and GTCCRE registers to the GTCCRA register) other than those shown in Table 21.38 and Table 21.39 are the same as double buffer transfer in complementary PWM mode 3 shown in Table 21.33.

Table 21.36 Immediate Single Buffer Transfer from GTCCRD Register in Complementary PWM Mode 4 (1 of 2)

Operation Section	Compare Match State	Immediate Transfer Destination Register	
		GTCCRC	GTCCRA
Up- counting middle section	Before up-counting compare match	GTCCRD	(i) In the case of GTCCRD > GPT32n+1.GTCNT GTCCRD (ii) In the case of GTCCRD < = GPT32+1.GTCNT GPT32n+1.GTCNT Negative-phase OFF
	Up-counting dead time period	GTCCRD	No transfer
	After up-counting compare match	GTCCRD	No transfer
Up-counting crest section	Before up-counting compare match	Before down-counting compare match GTCCRD After down-counting dead time start No transfer	Before down-counting compare match (i) In the case of GTCCRD > GPT32n+1.GTCNT GTCCRD (ii) In the case of GTCCRD < = GPT32n+1.GTCNT GPT32n+1.GTCNT Negative-phase OFF After down-counting dead time start No transfer
	Up-counting dead time period	Before down-counting compare match GTCCRD After down-counting dead time start No transfer	No transfer
	After up-counting compare match	Before down-counting compare match (i) In the case of GTCCRD < GPT32n+2.GTCNT GTCCRD (ii) In the case of GTCCRD = > GPT32n+2.GTCNT GPT32n+2.GTCNT Positive-phase OFF After down-counting dead time start No transfer	No transfer

GTCCRC寄存器到GTCCRA寄存器）除表21.36和表21.37所示之外，与表21.32所示互补PWM模式3中的单缓冲区传输相同。

表21.38和表21.39显示了立即缓冲区传输（通过向临时寄存器写入值来传输到临时寄存器）GPT32n+2.GTCCRD寄存器）通过在互补PWM模式4的双缓冲操作期间为每个操作部分中的每个比较匹配状态向GTCCRD和GTCCRF寄存器写入一个值来写入每个寄存器。传输（从GTCCRD寄存器到临时寄存器A，从GTCCRF寄存器到临时寄存器B，从临时寄存器A到GTCCRC寄存器，从临时寄存器B到GTCCRE寄存器，从GTCCRC和GTCCRE寄存器到GTCCRA寄存器）除了表21.38和表21.39中所示的内容外，与表21.33中所示的互补PWM模式3中的双缓冲传输相同。

Table 21.36 在互补PWM模式4中从GTCCRD寄存器立即进行单缓冲区传输（1of2）

运营科	比较匹配状态	立即传送目的地寄存器	
		GTCCRC	GTCCRA
正数中段	在向上计数比较匹配之前	GTCCRD	(i)在GTCCRD>GPT32n+1.GTCNT的情况下 GTCCRD(ii)在GTCCRD<=GPT32+1.GTCNT的情况下 GPT32n+1.GTCNT Negative-phase OFF
	向上计数的死区时间	GTCCRD	无转让
	向上计数比较匹配后	GTCCRD	无转让
向上计数的波峰部分	在向上计数比较匹配之前	在向下计数比较匹配之前 GTCCRD 倒计时死区时间开始后 无转让	在向下计数比较匹配之前(i)在GTCCRD>GPT32n+1.GTCNT的情况下 GTCCRD(ii)在GTCCRD<=GPT32n+1.GTCNT的情况下 GPT32n+1.GTCNT Negative-phase OFF 倒计时死区时间开始后 无转让
	向上计数的死区时间	在向下计数比较匹配之前 GTCCRD 倒计时死区时间开始后 无转让	无转让
	向上计数比较匹配后	向下计数比较匹配之前(i)在GTCCRD<GPT32n+2.GTCNT的情况下 GTCCRD(ii)在GTCCRD=>GPT32n+2.GTCNT的情况下 GPT32n+2.GTCNT Positive-phase OFF 倒计时死区时间开始后 无转让	无转让

Table 21.36 Immediate Single Buffer Transfer from GTCCRD Register in Complementary PWM Mode 4 (2 of 2)

Operation Section	Compare Match State	Immediate Transfer Destination Register	
		GTCCRC	GTCCRA
Down-counting crest section	Before down-counting compare match	Up-counting dead time period (i) In the case of GTCCRD < GPT32n+1.GTCNT GTCCRD (ii) In the case of GTCCRD = > GPT32n+1.GTCNT GPT32n+1.GTCNT Negative-phase ON After up-counting compare match (i) In the case of GTCCRD < GPT32n.GTCNT GTCCRD (ii) In the case of GTCCRD = > GPT32n.GTCNT GPT32n.GTCNT Positive-phase OFF	No transfer
	Down-counting dead time period	No transfer	No transfer
	After down-counting compare match	No transfer	No transfer

Table 21.37 Immediate Single Buffer Transfer from GTCCRD Register in Complementary PWM Mode 4 (1 of 2)

Operation Section	Compare Match State	Immediate Transfer Destination Register	
		GTCCRC	GTCCRA
Down-counting middle section	Before down-counting compare match	GTCCRD	(i) In the case of GTCCRD < GPT32n.GTCNT GTCCRD (ii) In the case of GTCCRD = > GPT32n.GTCNT GPT32n.GTCNT Positive-phase OFF
	Down-counting dead time period	GTCCRD	No transfer
	After down-counting compare match	GTCCRD	No transfer

Table 21.36 在互补PWM模式4中从GTCCRD寄存器立即进行单缓冲区传输（2之2）

运营科	比较匹配状态	立即传送目的地寄存器	
		GTCCRC	GTCCRA
向下计数的波峰部分	在向下计数比较匹配之前	递增计数死区时间(i)在GTCCRD<GPT32n+1.GTCNT的情况下 GTCCRD(ii)在GTCCRD=>GPT32n+1.GTCNT的情况下 GPT32n+1.GTCNT Negative-phase ON 向上计数比较匹配后(i)在GTCCRD<GPT32n.GTCNT的情况下 GTCCRD(ii)在GTCCRD=>GPT32n.GTCNT的情况下 GPT32n.GTCNT Positive-phase OFF	无转让
	向下计数死区时间	无转让	无转让
	向下计数比较匹配后	无转让	无转让

Table 21.37 在互补PWM模式4中从GTCCRD寄存器立即进行单缓冲区传输（1of2）

运营科	比较匹配状态	立即传送目的地寄存器	
		GTCCRC	GTCCRA
向下计数中段	在向下计数比较匹配之前	GTCCRD	(i)在GTCCRD<GPT32n.GTCNT的情况下 GTCCRD(ii)在GTCCRD=>GPT32n.GTCNT的情况下 GPT32n.GTCNT Positive-phase OFF
	向下计数死区时间	GTCCRD	无转让
	向下计数比较匹配后	GTCCRD	无转让

Table 21.37 Immediate Single Buffer Transfer from GTCCRD Register in Complementary PWM Mode 4 (2 of 2)

Operation Section	Compare Match State	Immediate Transfer Destination Register	
		GTCCRC	GTCCRA
Down-counting trough section	Before down-counting compare match	Before up-counting compare match GTCCRD After up-counting dead time start No transfer	Before up-counting compare match (i) In the case of GTCCRD < GPT32n.GTCNT GTCCRD (ii) In the case of GTCCRD = > GPT32n.GTCNT GPT32n.GTCNT Positive-phase OFF After up-counting dead time start No transfer
	Down-counting dead time period	Before up-counting compare match GTCCRD After up-counting dead time start No transfer	No transfer
	After down-counting compare match	Before up-counting compare match (i) In the case of GTCCRD > GPT32n+2.GTCNT GTCCRD (ii) In the case of GTCCRD < = GPT32n+2.GTCNT GPT32n+2.GTCNT Negative-phase OFF After up-counting dead time start No transfer	No transfer
Up- counting trough section	Before up-counting compare match	Down-counting dead time period (i) In the case of GTCCRD > GPT32n.GTCNT GTCCRD (ii) In the case of GTCCRD < = GPT32n.GTCNT GPT32n.GTCNT Positive-phase ON After down-counting compare match (i) In the case of GTCCRD > GPT32n+1.GTCNT GTCCRD (ii) In the case of GTCCRD < = GPT32n+1.GTCNT GPT32n+1.GTCNT Negative-phase OFF	No transfer
	Up-counting dead time period	No transfer	No transfer
	After up-counting compare match	No transfer	No transfer

Table 21.37 在互补PWM模式4中从GTCCRD寄存器立即进行单缓冲区传输（2之2）

运营科	比较匹配状态	立即传送目的地寄存器	
		GTCCRC	GTCCRA
向下计数槽段	在向下计数比较匹配之前	在向上计数比较匹配之前 GTCCRD 加计数死区时间后开始 无转让	在向上计数比较匹配之前(i)在GTCCRD<GPT32n.GTCNT的情况下 GTCCRD(ii)在GTCCRD=>GPT32n.GTCNT的情况下 GPT32n.GTCNT Positive-phase OFF 加计数死区时间后开始 无转让
	向下计数死区时间	在向上计数比较匹配之前 GTCCRD 加计数死区时间后开始 无转让	无转让
	向下计数比较匹配后	在向上计数比较匹配之前(i)在GTCCRD>GPT32n+2.GTCNT的情况下 GTCCRD(ii)在GTCCRD<=GPT32n+2.GTCNT的情况下 GPT32n+2.GTCNT Negative-phase OFF 加计数死区时间后开始 无转让	无转让
倒数槽段	在向上计数比较匹配之前	向下计数死区时间段(i)在GTCCRD>GPT32n.GTCNT的情况下 GTCCRD(ii)在GTCCRD<=GPT32n.GTCNT的情况下 GPT32n.GTCNT Positive-phase ON 向下计数比较匹配后(i)在GTCCRD>GPT32n+1.GTCNT的情况下 GTCCRD(ii)在GTCCRD<=GPT32n+1.GTCNT的情况下 GPT32n+1.GTCNT Negative-phase OFF	无转让
	向上计数的死区时间	无转让	无转让
	向上计数比较匹配后	无转让	无转让

Table 21.38 Immediate Double Buffer Transfer from GTCCRD and GTCCRF Registers in Complementary PWM Mode 4

Operation Section	Compare Match State	Immediate Transfer Destination Register		
		GTCCRC	GTCCRE	GTCCRA
Up-counting middle section	Before up-counting compare match	GTCCRD	GTCCRF	(i) In the case of GTCCRF > GPT32n+1.GTCNT GTCCRF (ii) In the case of GTCCRF < = GPT32+1.GTCNT GPT32n+1.GTCNT Negative-phase OFF
	Up-counting dead time period	GTCCRD	GTCCRF	No transfer
	After up-counting compare match	GTCCRD	GTCCRF	No transfer

Table 21.39 Immediate Double Buffer Transfer from GTCCRD and GTCCRF Registers in Complementary PWM Mode 4

Operation Section	Compare Match State	Immediate Transfer Destination Register		
		GTCCRC	GTCCRE	GTCCRA
Down-counting middle section	Before down-counting compare match	GTCCRD	GTCCRF	(i) In the case of GTCCRD < GPT32n.GTCNT GTCCRD (ii) In the case of GTCCRD => GPT32n.GTCNT GPT32n.GTCNT Positive-phase OFF
	Down-counting dead time period	GTCCRD	GTCCRF	No transfer
	After down-counting compare match	GTCCRD	GTCCRF	No transfer

Figure 21.71 to Figure 21.75 show examples of single buffer operation for each operation section in complementary PWM mode 4.

Figure 21.76 to Figure 21.79 show examples of double buffer operation for each operation section in complementary PWM mode 4.

Table 21.40 shows an example for setting complementary PWM mode 4.

Table 21.38 互补PWM中GTCCRD和GTCCRF寄存器的立即双缓冲区传输 Mode 4

运营科	比较匹配状态	立即传送目的地寄存器		
		GTCCRC	GTCCRE	GTCCRA
递增计数中段	在向上计数比较匹配之前	GTCCRD	GTCCRF	(i)GTCCRF>GPT32n+1.GTCNTGTCCRF(ii)GTCCRF<= GPT32+1.GTCNT GPT32n+1.GTCNT Negative-phase OFF
	向上计数的死区时间	GTCCRD	GTCCRF	无转让
	向上计数比较匹配后	GTCCRD	GTCCRF	无转让

Table 21.39 互补PWM中GTCCRD和GTCCRF寄存器的立即双缓冲区传输 Mode 4

运营科	比较匹配状态	立即传送目的地寄存器		
		GTCCRC	GTCCRE	GTCCRA
向下计数中段	在向下计数比较匹配之前	GTCCRD	GTCCRF	(i)在GTCCRD< GPT32n.GTCNTGTCCRD(ii)在GTCCRD的情况下=> GPT32n.GTCNT GPT32n.GTCNT Positive-phase OFF
	向下计数死区时间	GTCCRD	GTCCRF	无转让
	向下计数比较匹配后	GTCCRD	GTCCRF	无转让

图21.71至图21.75显示了互补PWM模式4中每个操作部分的单缓冲器操作示例。

图21.76至图21.79显示了互补PWM模式4中每个操作部分的双缓冲器操作示例。

表21.40显示了设置互补PWM模式4的示例。

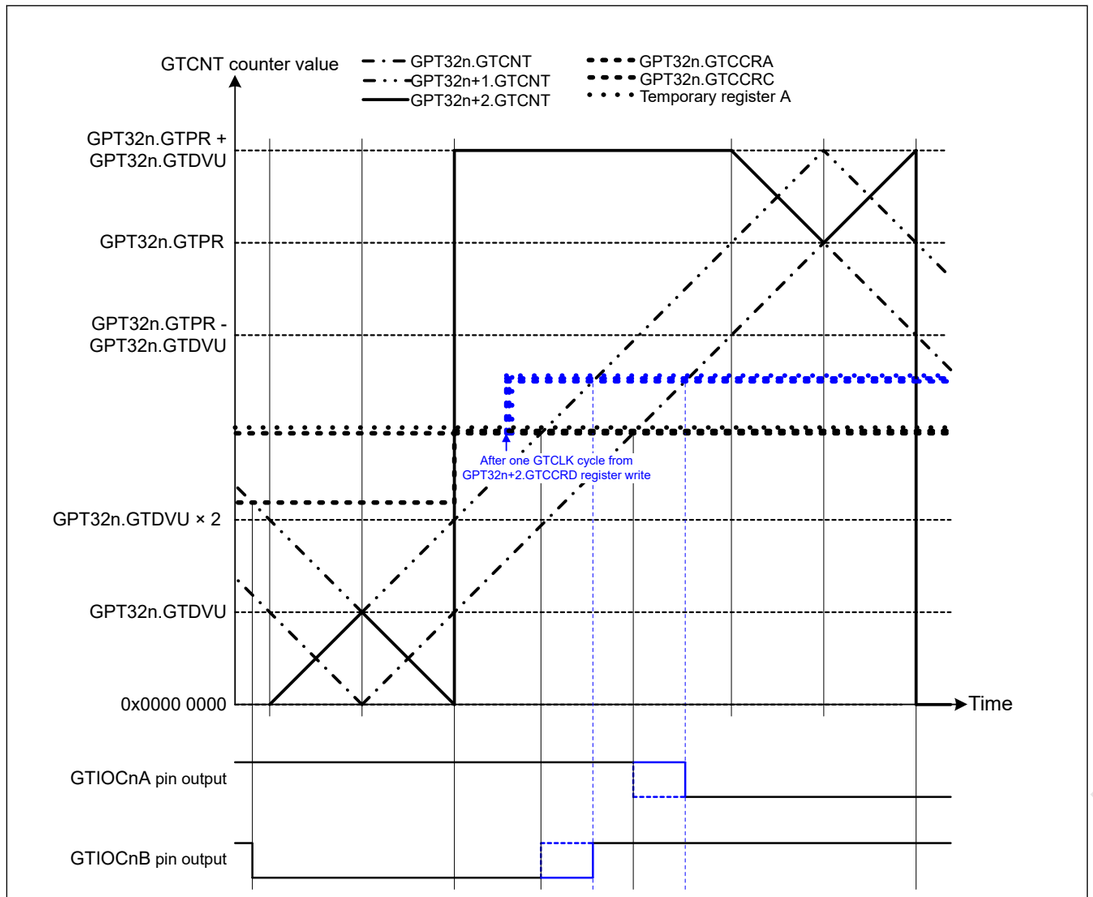


Figure 21.71 Example of Complementary PWM Mode 4 Single Buffer Operation (Up-Counting Middle Section) (Complementary PWM mode 4 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value larger than the GPT32n+1.GTCNT value is written to GTCCRD register before up-counting compare match) (n = 4, 7)

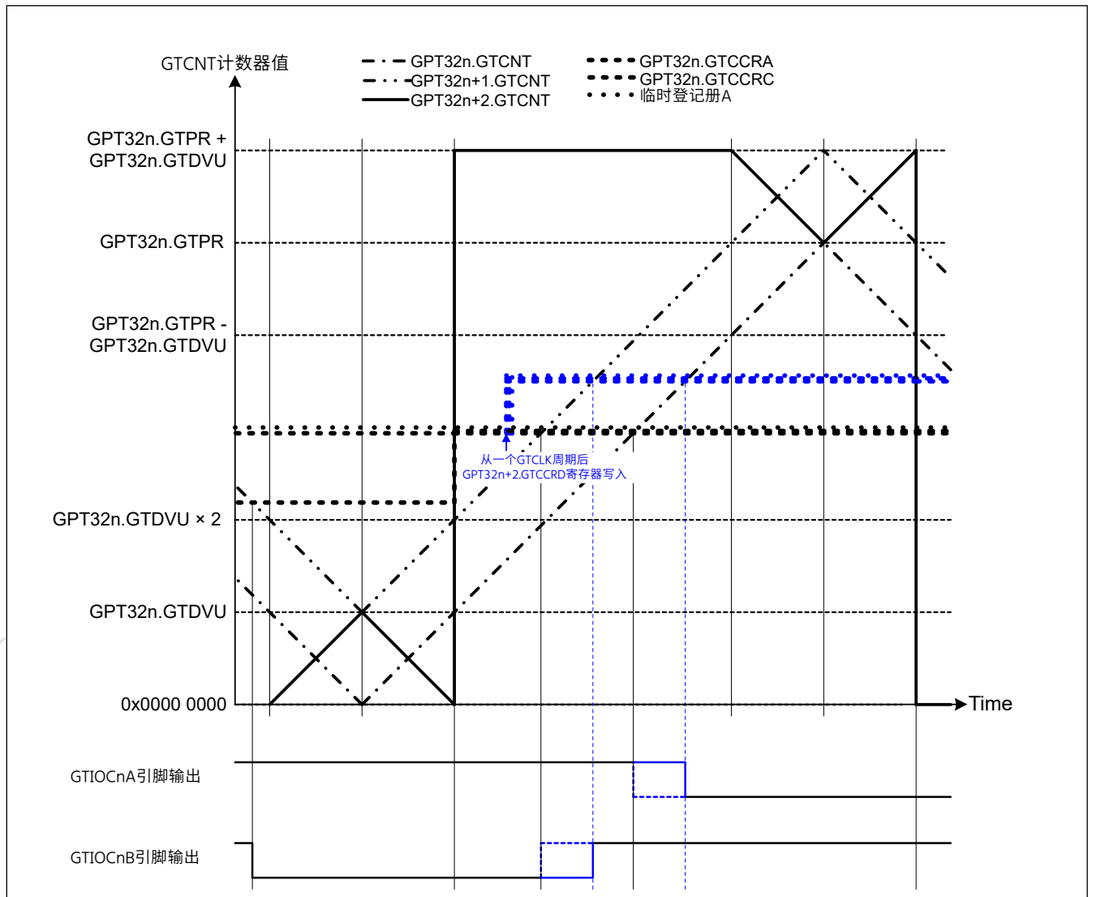


Figure 21.71 互补PWM模式4单缓冲器操作示例（向上计数中间部分）（互补PWM模式4单缓冲器操作，GTIOCnA引脚=低GTIOCnB引脚=向上计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=高电平GTIOCnB引脚=向下计数期间GTCCRA寄存器比较匹配时为低电平，当一个值大于GPT32n+1.GTCNT值在向上计数比较匹配之前写入GTCCRD寄存器）（n= 4 7）

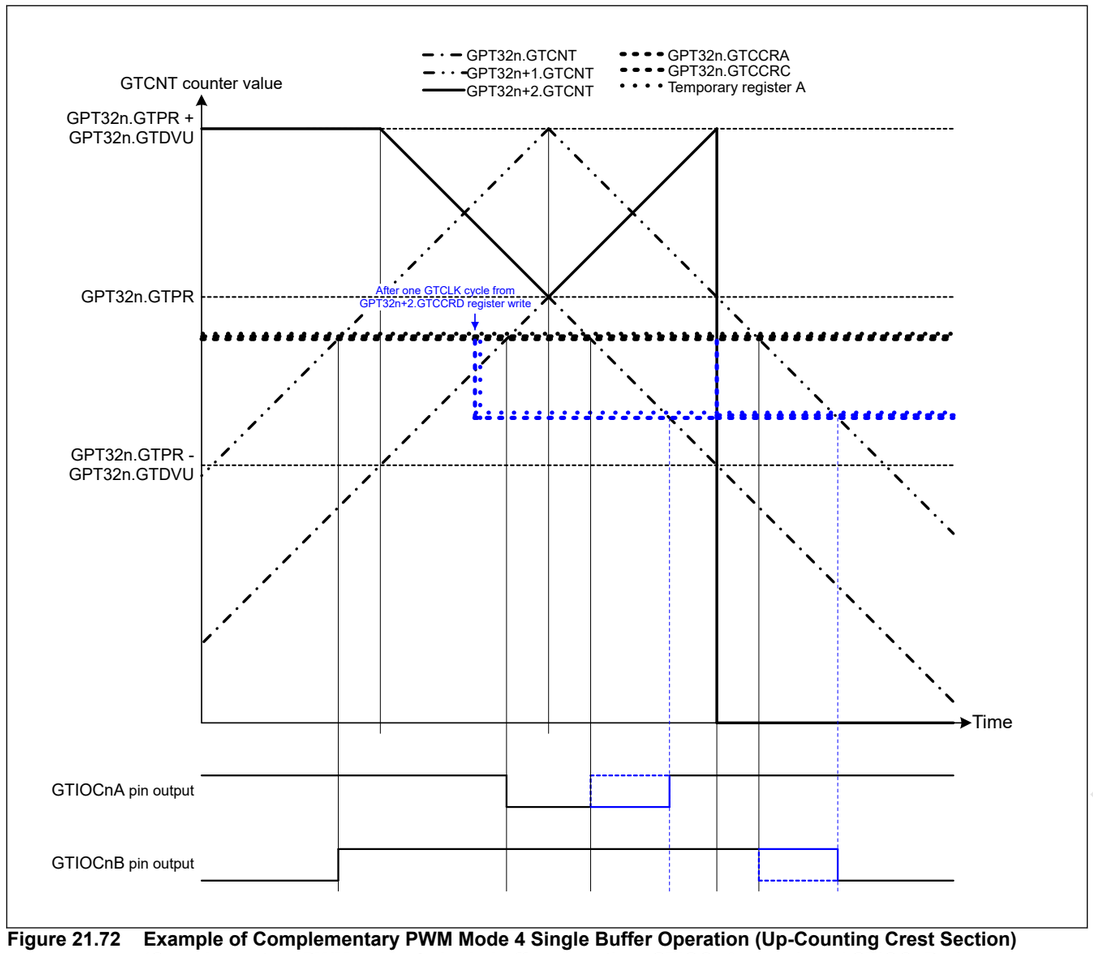


Figure 21.72 Example of Complementary PWM Mode 4 Single Buffer Operation (Up-Counting Crest Section) (Complementary PWM mode 4 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value is written to GTCCRD register during the up-counting dead time) (n = 4, 7)

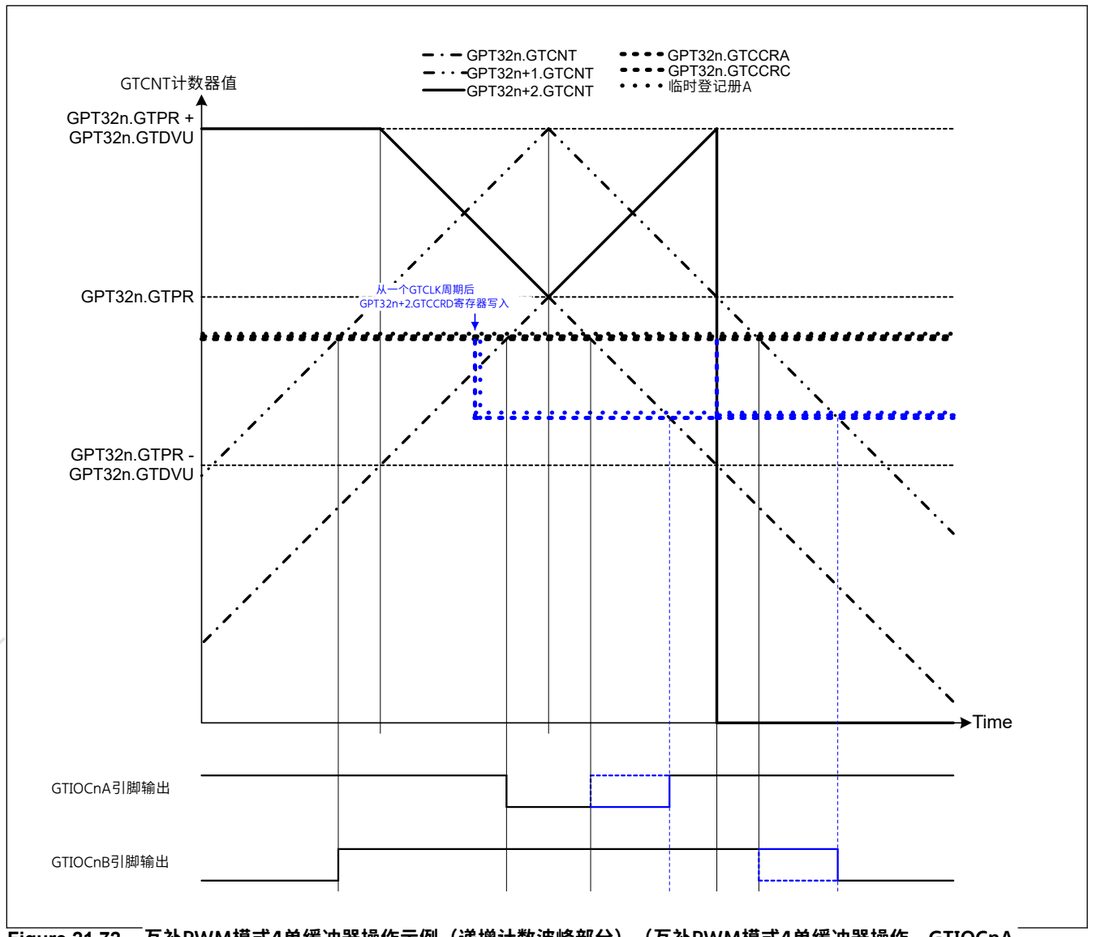


Figure 21.72 互补PWM模式4单缓冲器操作示例（递增计数波峰部分）（互补PWM模式4单缓冲器操作，GTIOCnA引脚=低GTIOCnB引脚=递增期间GTCCRA寄存器比较匹配时为高，GTIOCnA引脚=高GTIOCnB引脚=向下计数期间GTCCRA寄存器比较匹配时为低电平，当在向上计数死区期间将值写入GTCCRD寄存器时）（n=4 7）

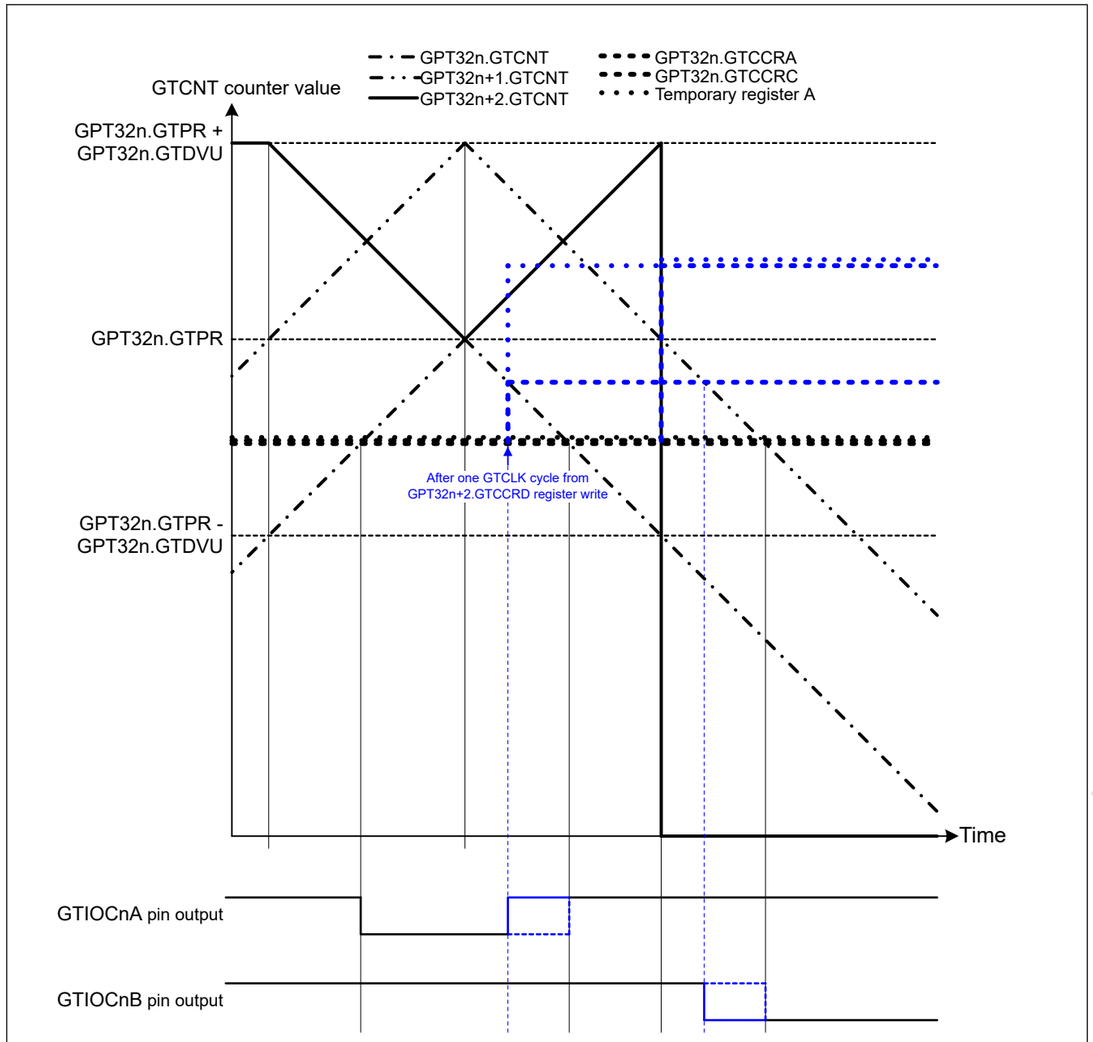


Figure 21.73 Example of Complementary PWM Mode 4 Single Buffer Operation (Down-Counting Crest Section) (Complementary PWM mode 4 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value not less than the GPT32n.GTCNT value is written to GTCCRD register after up-counting compare match before down-counting compare match) (n = 4, 7)

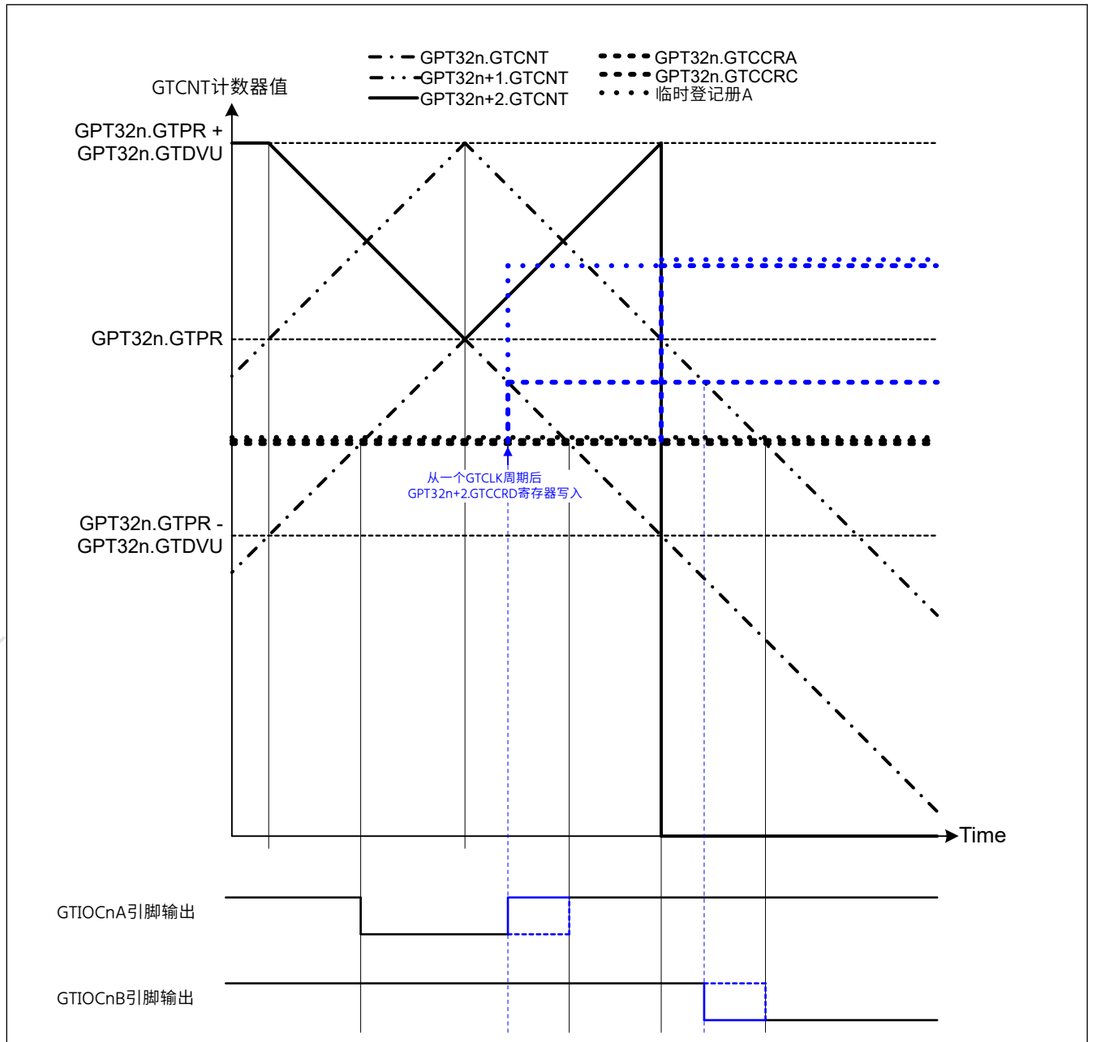


Figure 21.73 互补PWM模式4单缓冲器操作示例（向下计数波峰部分）（互补PWM模式4单缓冲器操作，GTIOCnA引脚=低GTIOCnB引脚=向上计数期间GTCCRA寄存器比较匹配时为高，GTIOCnA引脚=高GTIOCnB引脚=向下计数期间GTCCRA寄存器比较匹配时为低电平，当在向下计数比较匹配之前向上计数比较匹配后将不小于GPT32n.GTCNT值写入GTCCRD寄存器时）（n=4 7）

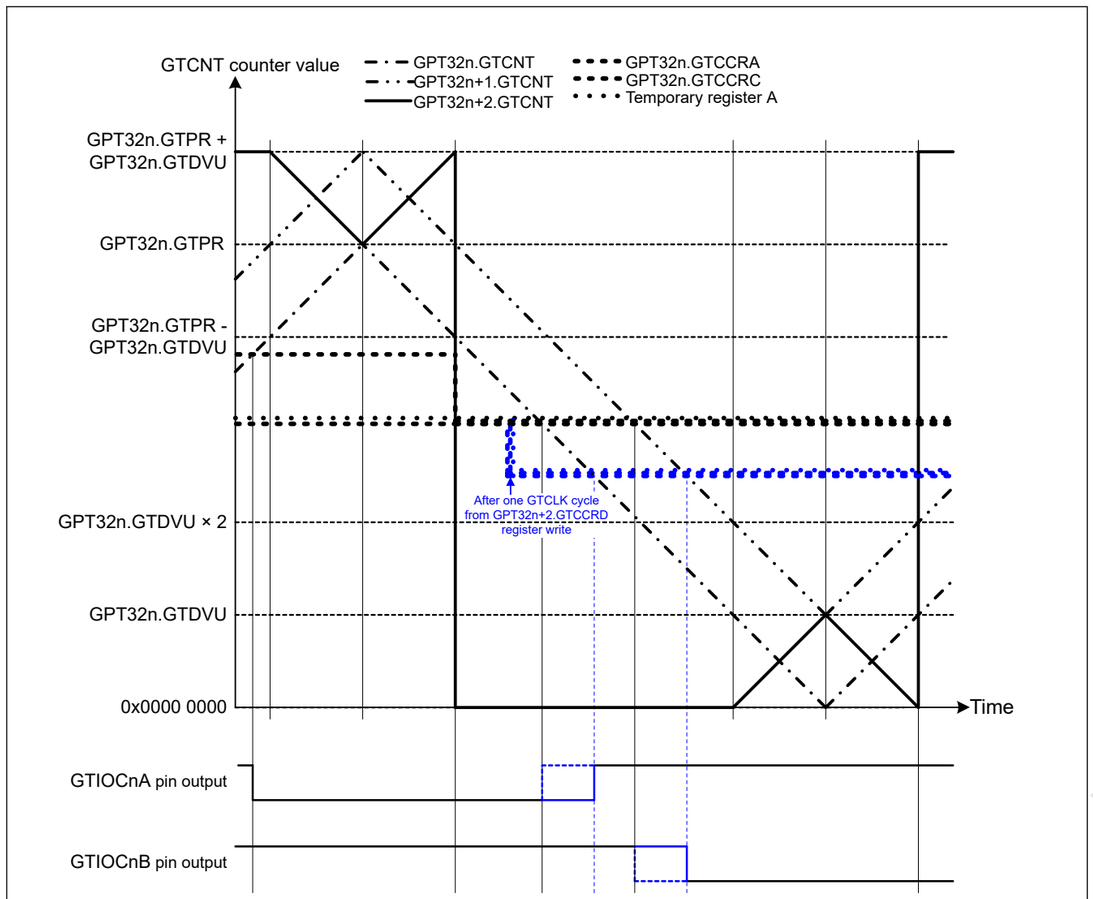


Figure 21.74 Example of Complementary PWM Mode 4 Single Buffer Operation (Down-Counting Middle Section) (Complementary PWM mode 4 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value smaller than the GPT32n.GTCNT value is written to GTCCRD register before down-counting compare match) (n = 4, 7)

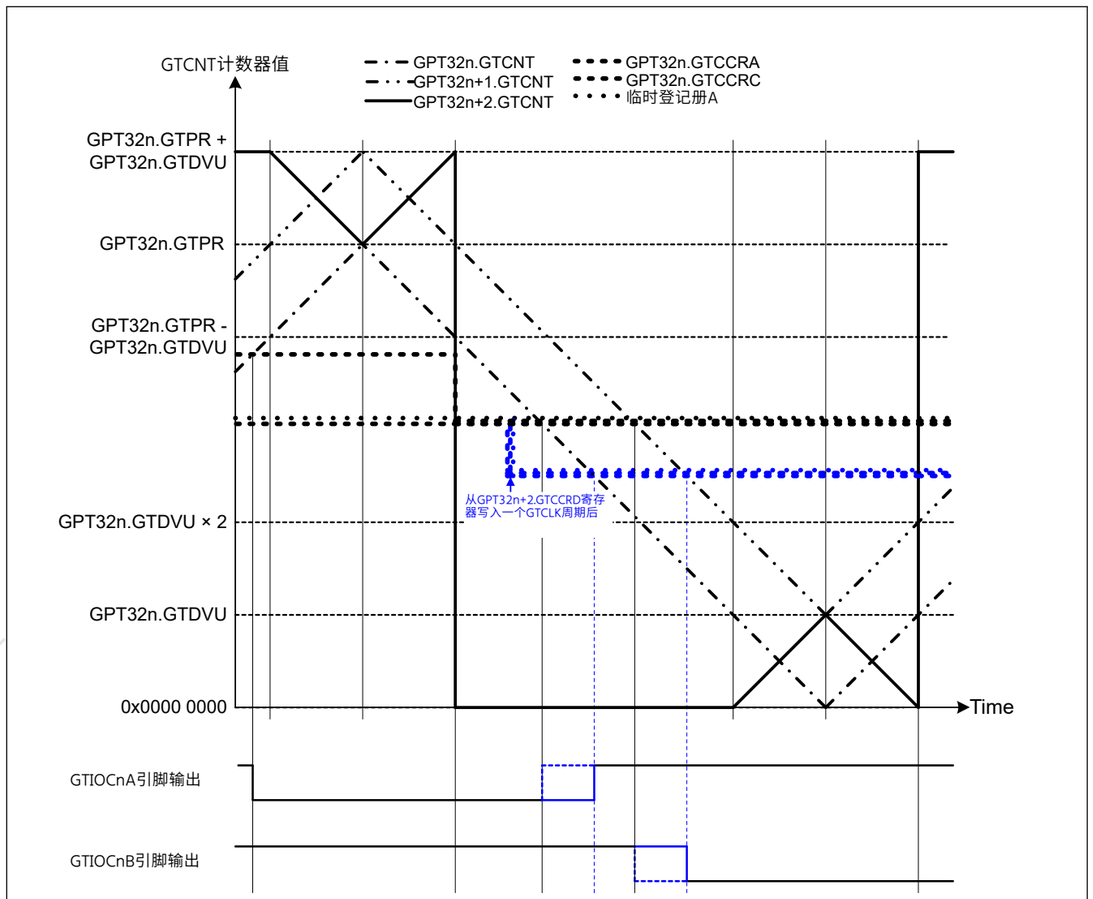


Figure 21.74 互补PWM模式4单缓冲器操作示例（向下计数中间部分）（互补PWM模式4单缓冲器操作，GTIOCnA引脚=低GTIOCnB引脚=向上计数期间GTCCRA寄存器比较匹配时为高，GTIOCnA引脚=高GTIOCnB引脚=向下计数期间GTCCRA寄存器比较匹配时为低电平，当小于GPT32n.GTCNT值的值在向下计数比较匹配之前写入GTCCRD寄存器时）（n=4 7）

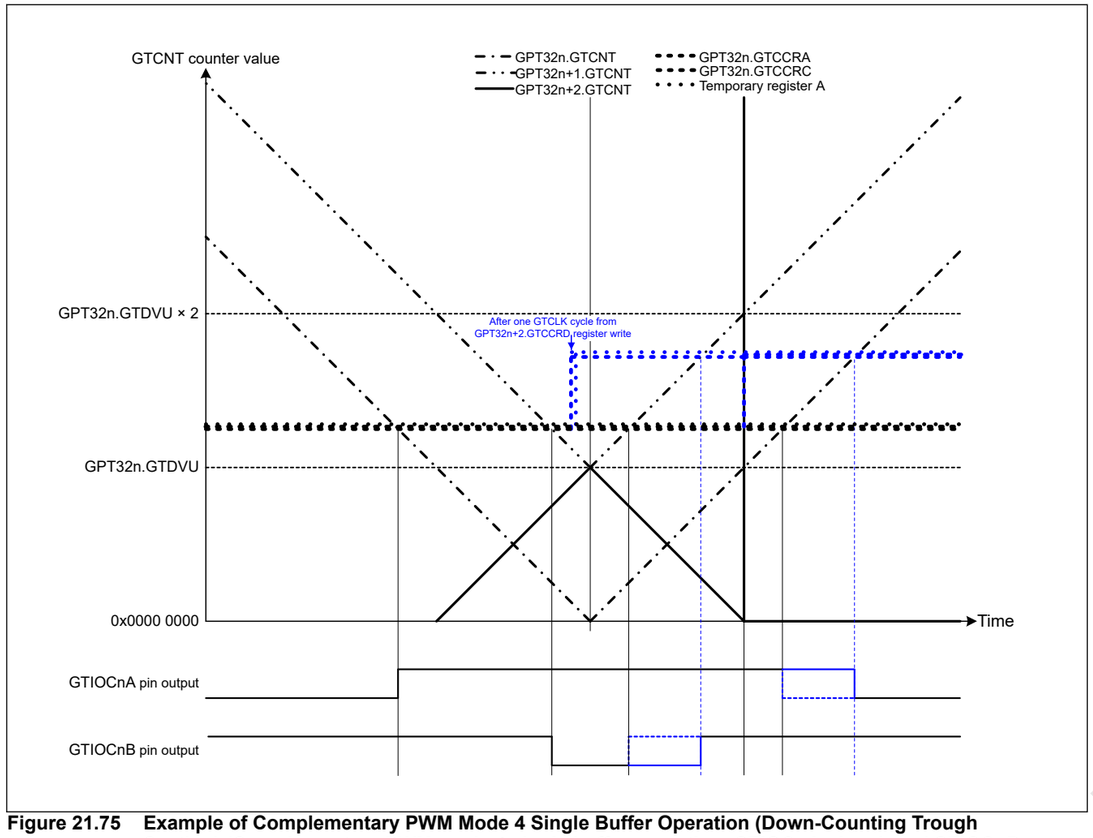


Figure 21.75 Example of Complementary PWM Mode 4 Single Buffer Operation (Down-Counting Trough Section) (Complementary PWM mode 4 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value larger than the GPT32n+2.GTCNT value is written to GTCCRD register after down-counting compare match) (n = 4, 7)

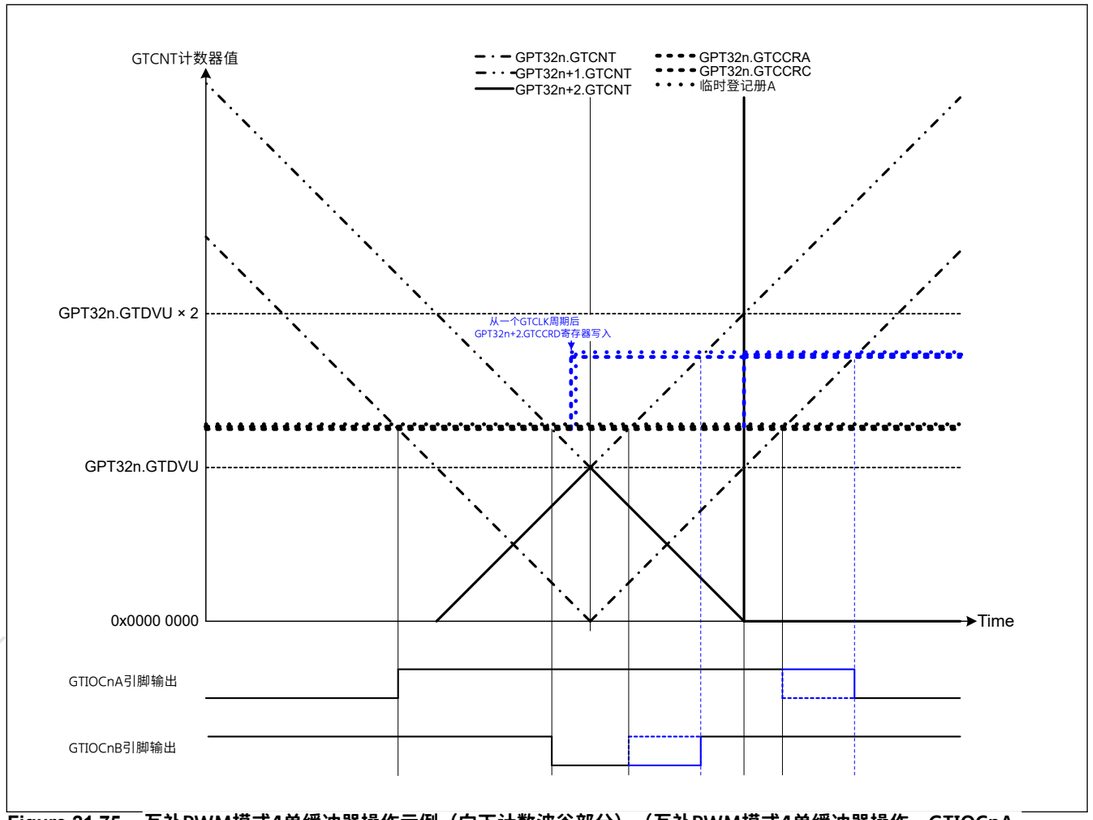


Figure 21.75 互补PWM模式4单缓冲器操作示例（向下计数波谷部分）（互补PWM模式4单缓冲器操作，GTIOCnA引脚=低GTIOCnB引脚=向上计数期间GTCCRA寄存器比较匹配时为高，GTIOCnA引脚=高GTIOCnB引脚=递减计数期间GTCCRA寄存器比较匹配时为低电平，当递减计数比较匹配后将大于GPT32n+2.GTCNT值的值写入GTCCRD寄存器时）（n=4 7）

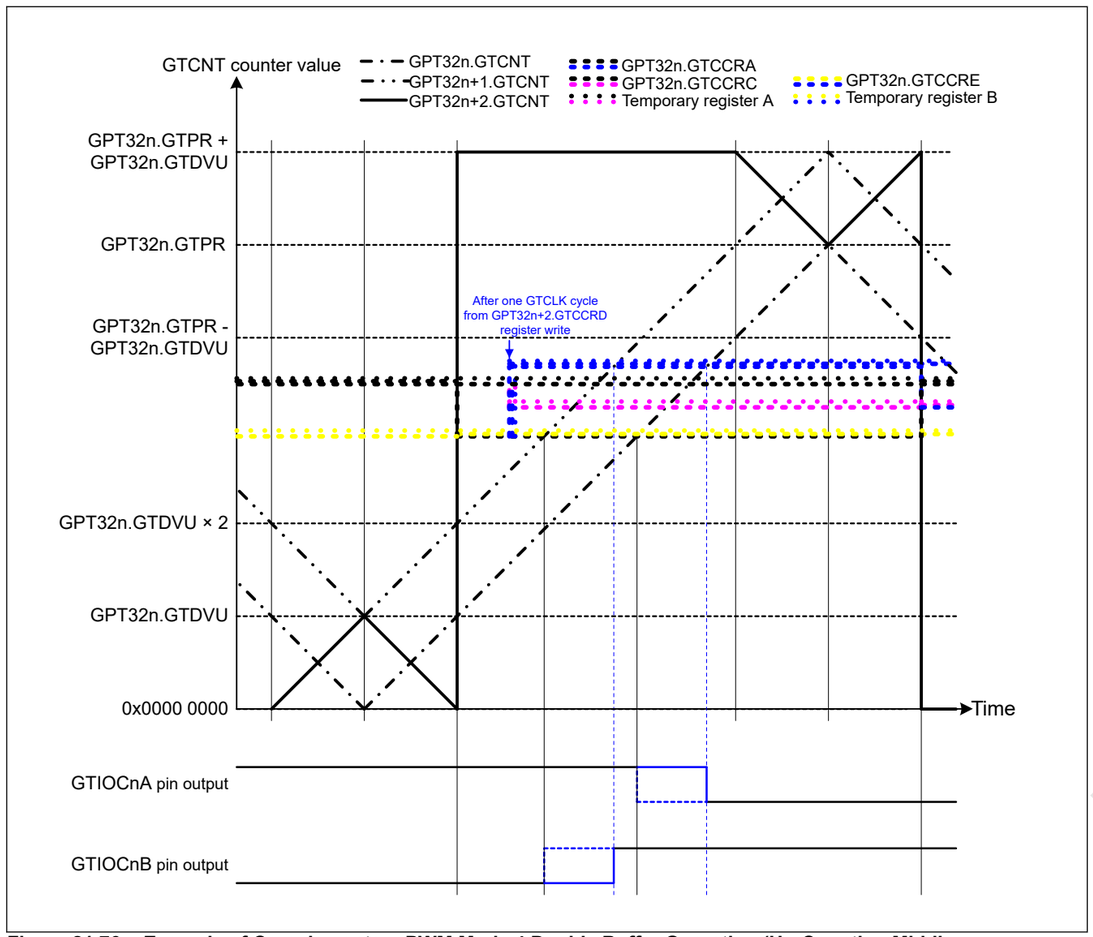


Figure 21.76 Example of Complementary PWM Mode 4 Double Buffer Operation (Up-Counting Middle Section) (Complementary PWM mode 4 double buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value larger than the GPT32n+1.GTCNT value is written to GTCCRF register before up-counting compare match) (n = 4, 7)

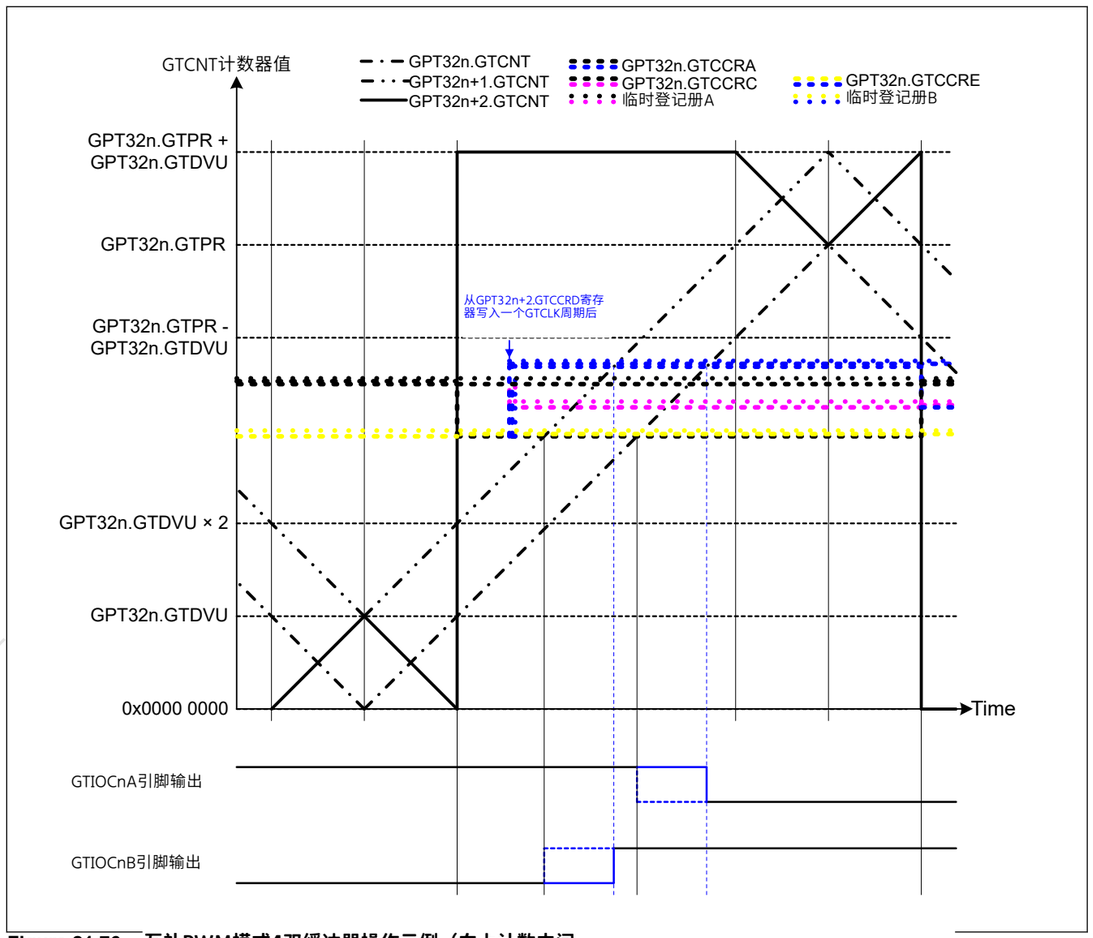


Figure 21.76 互补PWM模式4双缓冲器操作示例（向上计数中间部分）（互补PWM模式4双缓冲器操作，GTIOCnA引脚=低 GTIOCnB引脚=向上计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=向下计数期间GTCCRA寄存器比较匹配时为低电平，当一个大于GPT32n+1的值被写入GTCCRF寄存器之前向上计数比较匹配）（n=4 7）

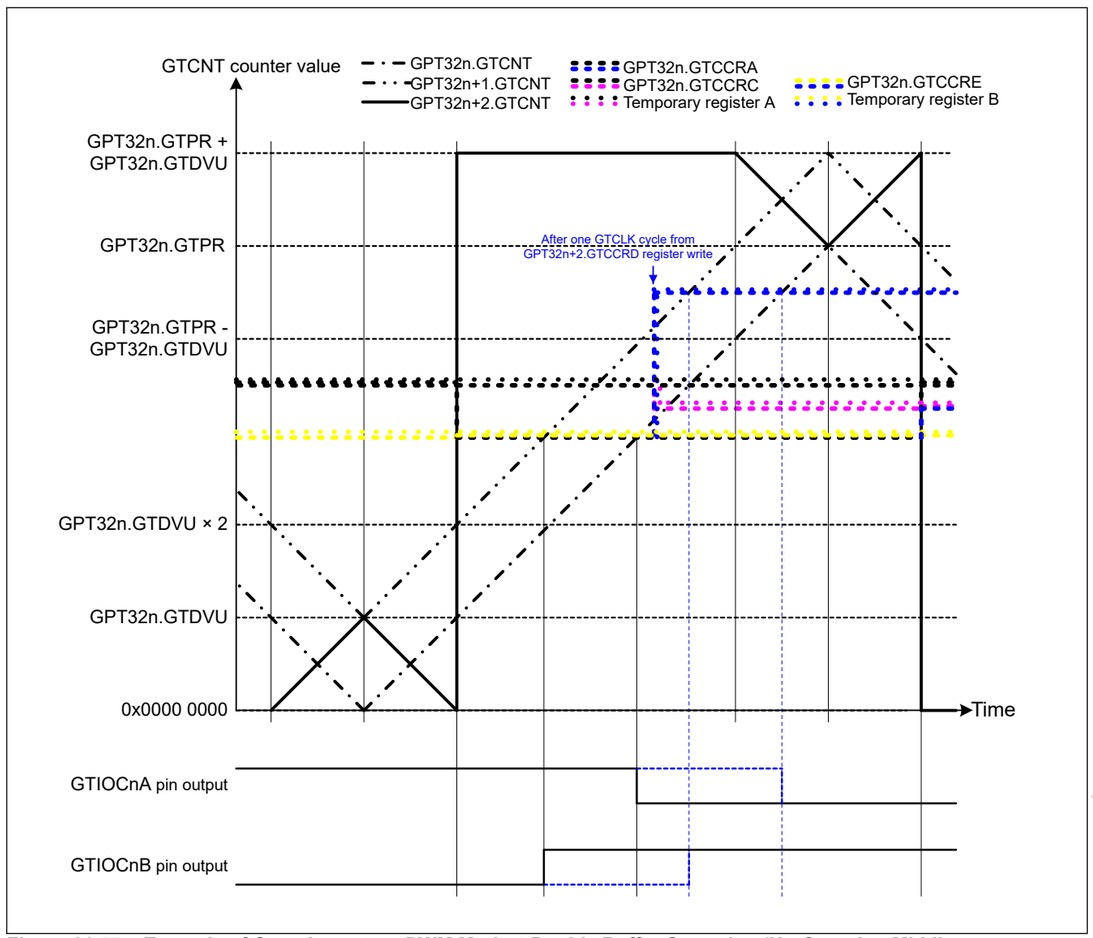


Figure 21.77 Example of Complementary PWM Mode 4 Double Buffer Operation (Up-Counting Middle Section) (Complementary PWM mode 4 double buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value is written to GTCCRF register after up-counting compare match) (n = 4, 7)

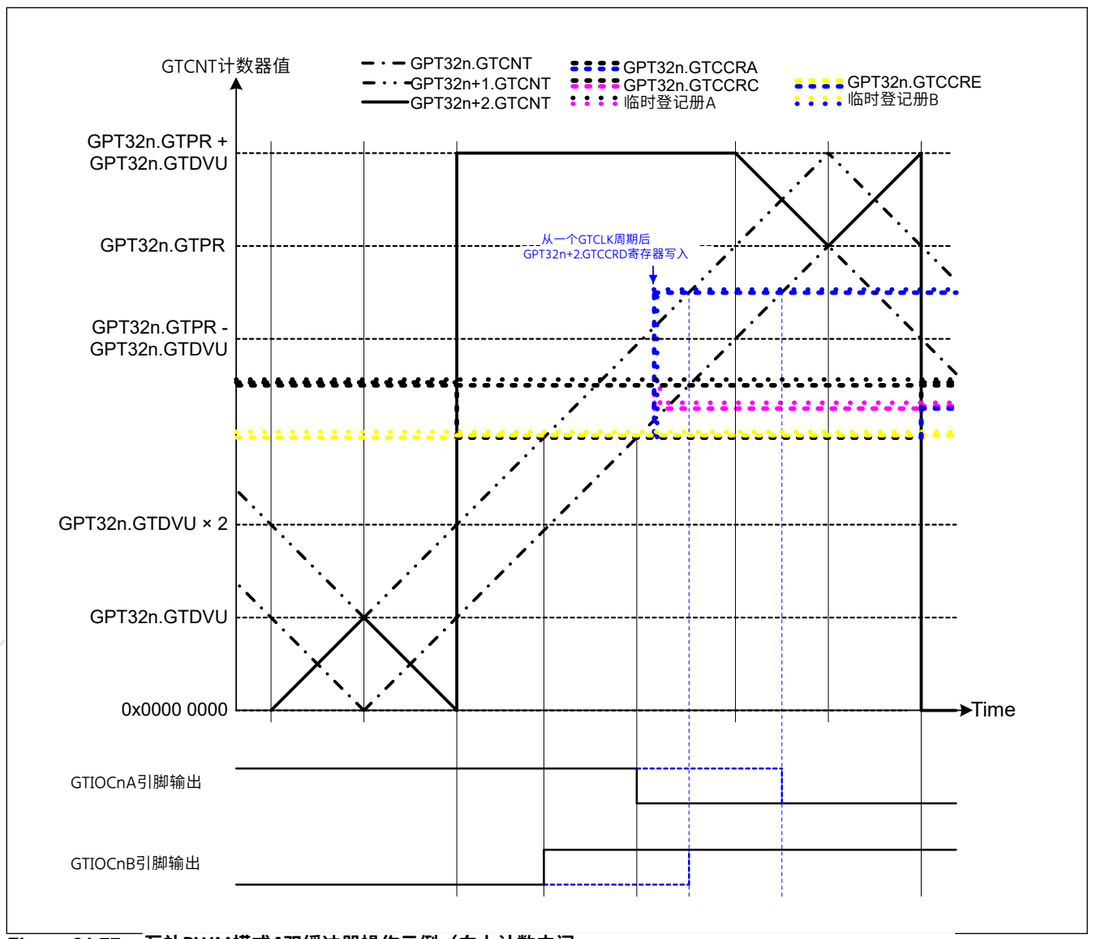


Figure 21.77 互补PWM模式4双缓冲器操作示例（向上计数中间部分）（互补PWM模式4双缓冲器操作，GTIOCnA引脚=低 GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=递减计数期间GTCCRA寄存器比较匹配时为低电平，当递增计数比较匹配后将值写入GTCCRF寄存器时）（n=4、7）

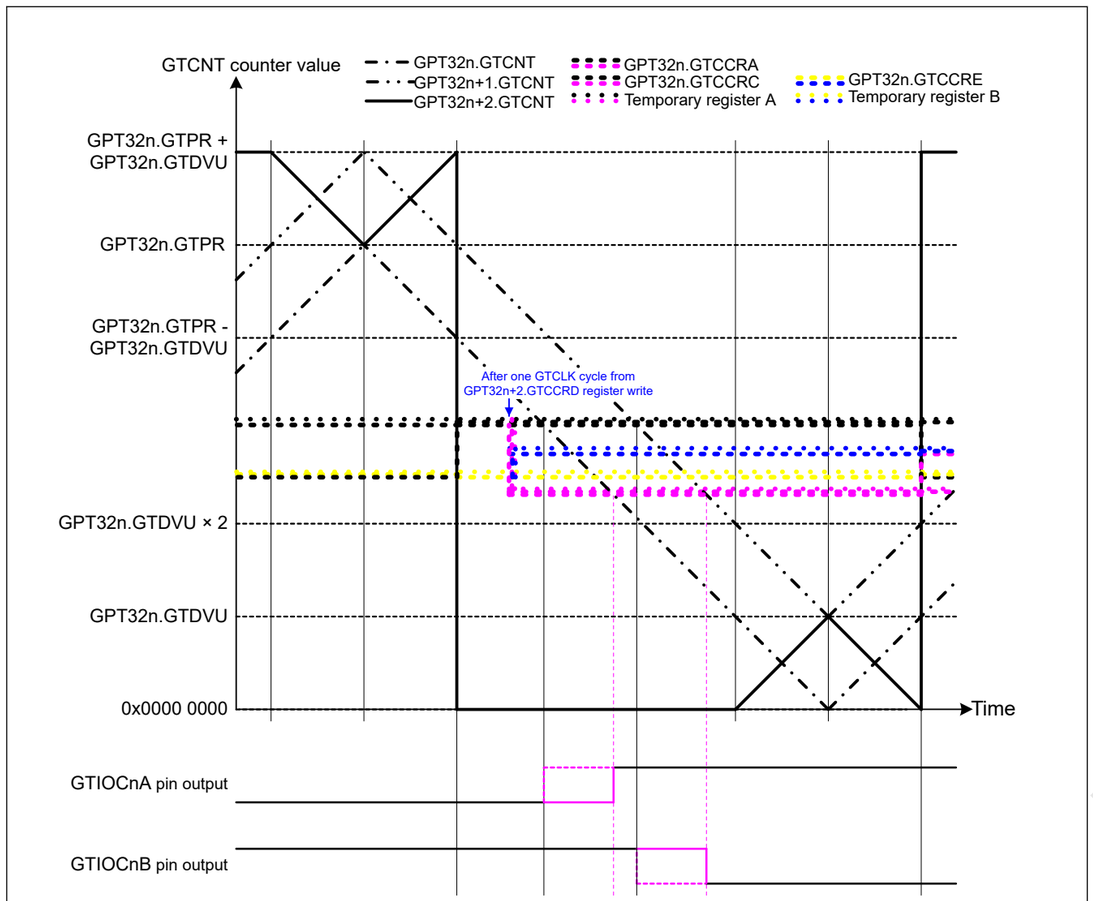


Figure 21.78 Example of Complementary PWM Mode 4 Double Buffer Operation (Down-Counting Middle Section) (Complementary PWM mode 4 double buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value smaller than the GPT32n.GTCNT value is written to GTCCRD register before down-counting compare match) (n = 4, 7)

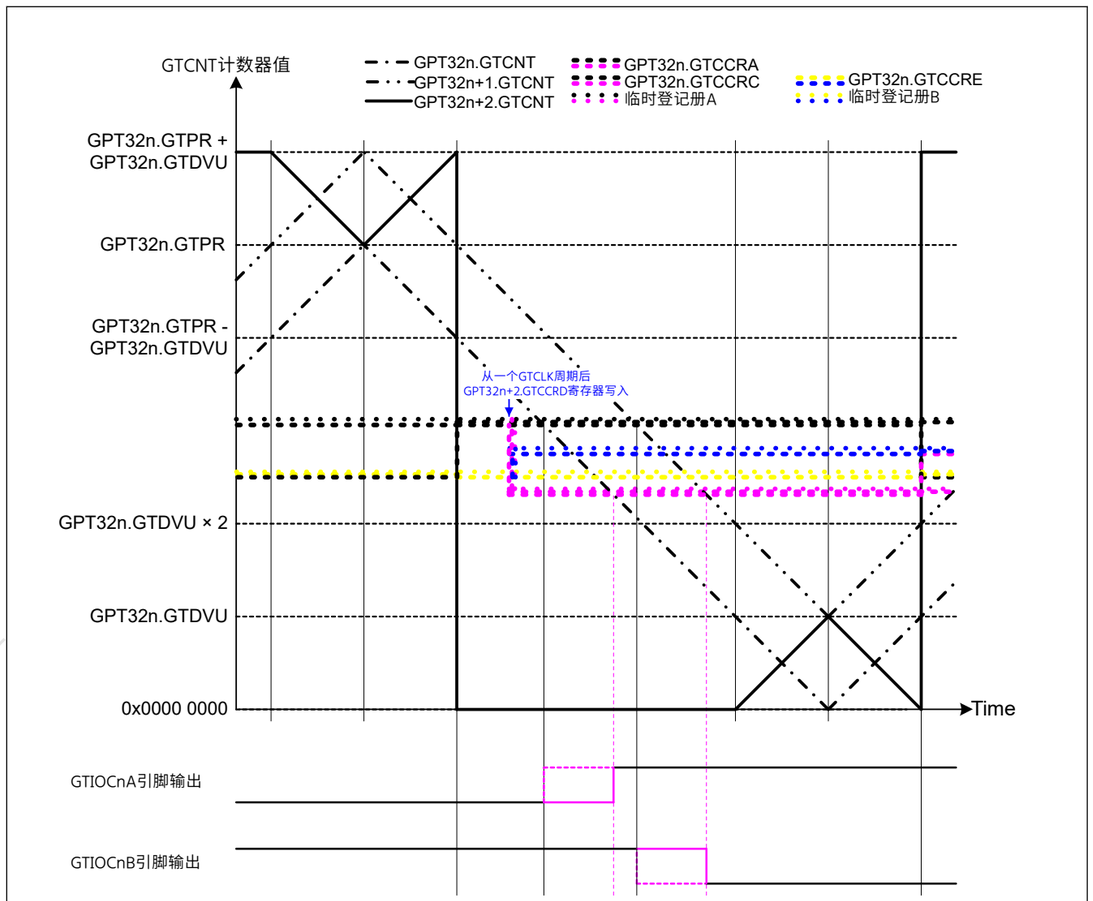


Figure 21.78 互补PWM模式4双缓冲器操作示例（向下计数中间部分）（互补PWM模式4双缓冲器操作，GTIOCnA引脚=低 GTIOCnB引脚=向上计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=向下计数期间GTCCRA寄存器比较匹配时为低电平，当小于GPT32n.GTCNT值的值在向下计数之前写入GTCCRD寄存器时比较匹配)(n=4 7)

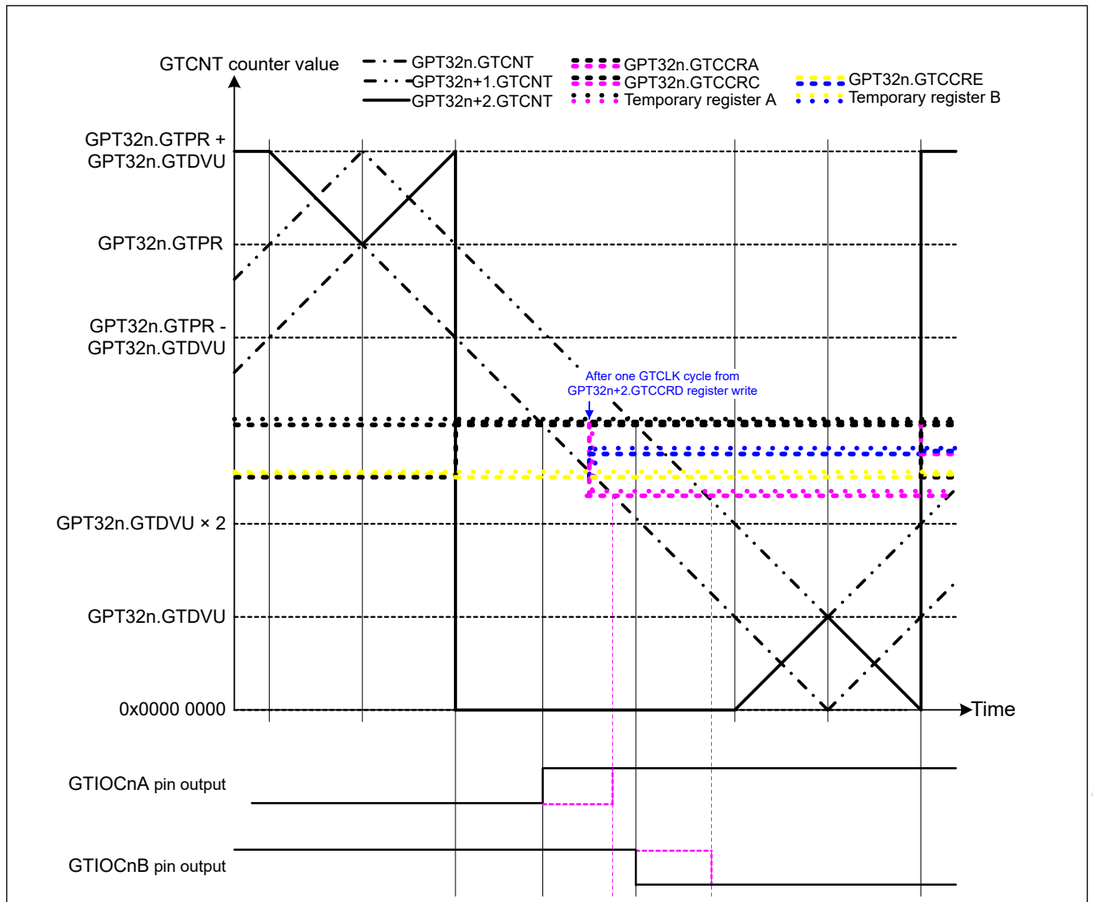


Figure 21.79 Example of Complementary PWM Mode 4 Double Buffer Operation (Down-Counting Middle Section) (Complementary PWM mode 4 double buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value is written to GTCCRD register during the down-counting dead time) (n = 4, 7)

Table 21.40 Example for Setting Complementary PWM Mode 4 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode (1111b) with GTCR.MD[3:0] of GTP32n channel.
2	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits of GPT32n channel.
3	Set cycle	Set the cycle in GTPR of GPT32n channel.
4	Set GTIOCnm /GTIOCn+1m / GTIOCn+2m pin function	Set the function of the GTIOCnm, GTIOCn+1m, and GTIOCn+2m pins with GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register of the GPT32n, GPT32n+1, and GPT32n+2 channels.
5	Enable GTIOCnm /GTIOCn +1m /GTIOCn+2m pin output	Set to enable the output from the GTIOCnm, GTIOCn+1m, and GTIOCn+2m pins with the OAE and OBE bits in the GTIOR register of the GPT32n, GPT32n+1, and GPT32n+2 channels.
6	Set buffer operation	Set buffer operation with the GTBER2.CP3DB bit of the GPT32n, GPT32n+1, and GPT32n+2 channels.
7	Set compare match value	Set the output pin changing point during up-counting after count start in the GTCCRA register of the GPT32n, GPT32n+1, and GPT32n+2 channels.

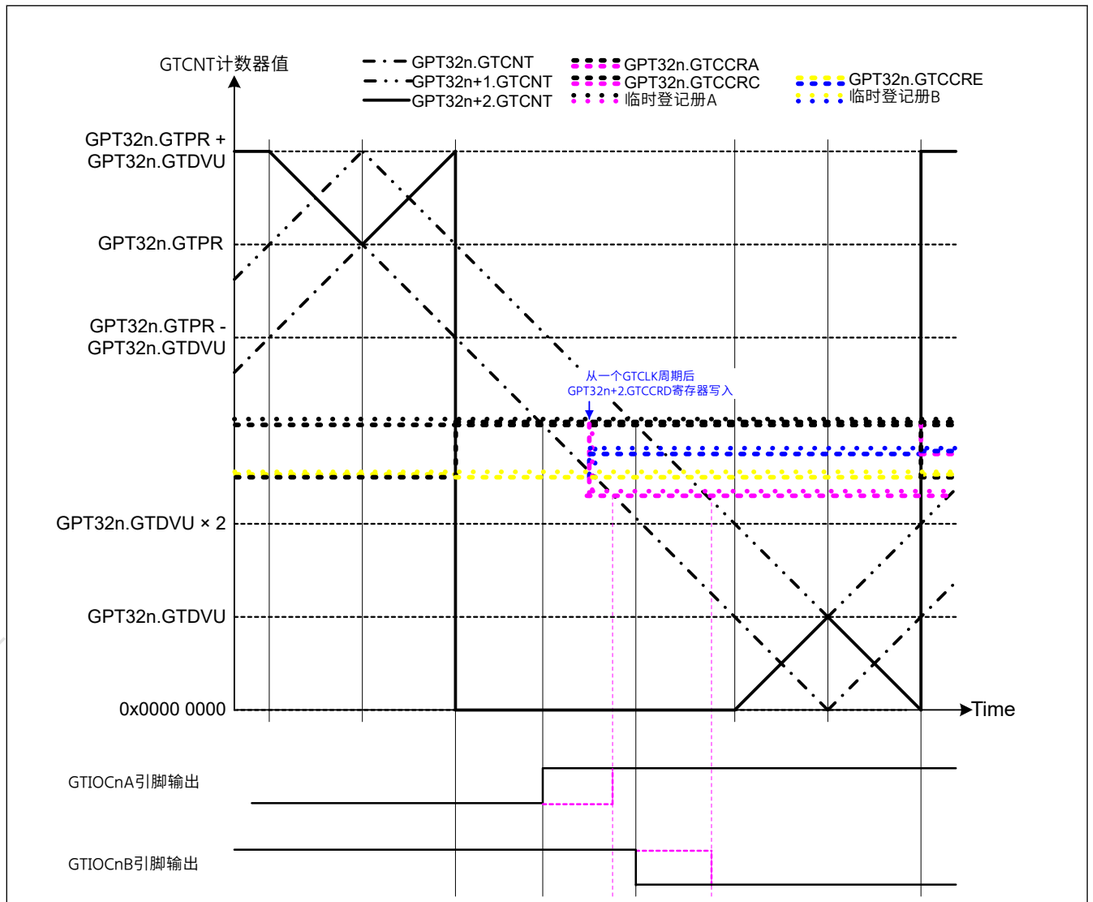


Figure 21.79 互补PWM模式4双缓冲器操作示例（向下计数中间部分）（互补PWM模式4双缓冲器操作，GTIOCnA引脚=低 GTIOCnB引脚=递增计数期间GTCCRA寄存器比较匹配时为高电平，GTIOCnA引脚=递减计数期间GTCCRA寄存器比较匹配时为低电平，当在递减计数死区期间将值写入GTCCRD寄存器时）（n=4 7）

Table 21.40 设置互补PWM模式4的示例（1of2）

No.	步骤名称	Description
1	设置操作模式	使用GTP32n通道的GTCR.MD[3:0]设置工作模式(1111b)。
2	选择计数时钟	使用GPT32n通道的GTCR.TPCS[3:0]位选择计数时钟。
3	设置周期	在GPT32n通道的GTPR中设置周期。
4	Set GTIOCnm /GTIOCn+1m / GTIOCn+2m引脚功能	通过GPT32n、GPT32n+1和GPT32n+2通道的GTIOR寄存器中的GTIOA[4:0]和GTIOB[4:0]位设置GTIOCnm、GTIOCn+1m和GTIOCn+2m引脚的功能。
5	使能GTIOCnmGTIOCn+1mGTIOCn+2m管脚输出	使用GPT32n、GPT32n+1和GPT32n+2通道的GTIOR寄存器中的OAE和OBE位设置以启用GTIOCnm、GTIOCn+1m和GTIOCn+2m引脚的输出。
6	设置缓冲操作	使用GPT32n、GPT32n+1和GPT32n+2通道的GTBER2.CP3DB位设置缓冲区操作。
7	设置比较匹配值	在GPT32n、GPT32n+1和GPT32n+2通道的GTCCRA寄存器中设置计数开始后向上计数期间的输出引脚变化点。

Table 21.40 Example for Setting Complementary PWM Mode 4 (2 of 2)

No.	Step Name	Description
8	Set buffer value	For single buffer operation, set data (to be transferred for the first buffer transfer to the GTCCRA register after count start) in the GTCCRD register. For double buffer operation, set data to be transferred at the first end of crest in the GTCCRD register and set data to be transferred at the first end of trough in the GTCCRF register.
9	Set dead t ime value	Set the dead time value in GTDVU of GTP32n channel.
10	Start count operation	Set GTCR.CST of GPT32n channel to 1 to start count operation.
11	Set compare match value to be transferred immediately	For single buffer operation, set data (to be transferred immediately to the GTCCRA register) in the GTCCRD register. For double buffer operation, set the compare match value for down-counting to be transferred immediately in the GTCCRD register and the compare match value for up-counting in the GTCCRF register. Make settings for the GPT32n+2.GTCCRD register finally. (Data is transferred to the temporary register.)

Note: n = 4, 7
m = A, B

21.3.4 Automatic Dead Time Setting Function

By setting GTDTCR, a compare match value for a negative waveform with dead time obtained by a compare match value for a positive waveform (GTCCRA value) and specified dead time value (GTDVU and GTDVD value) can automatically be set to GTCCRB.

The automatic dead time setting function can be used in saw-wave one-shot pulse mode and all the triangle PWM modes.

Dead time can be separately set for the first half and second half of a waveform. Dead time for the changing point in the first half of a negative waveform is set in the GTDVU register and that in the second half is set in GTDVD register. The same dead time can also be set for the first and second halves by setting the GTDTCR.TDFER bit to 1.

The GTDBU register can be used as a buffer register of the GTDVU register, and the GTDBD register can be used as a buffer register of the GTDVD registers. Buffer transfer is performed at the end of the cycle (in saw-wave mode: either of an overflow of the GTCNT counter (up-counting), an underflow (down-counting), or the GTCNT counter clearing; in triangle-wave mode: a trough).

The change point of the negative-phase waveform, which is automatically calculated, is obtained by reading the GTCCRB register. Writing to GTCCRB is prohibited when the automatic dead time setting function is used.

Do not set the dead time that makes the change point of the waveform exceeding the count period. When any dead-time setting which would generate a dead-time error is made, adjust the change points of the positive- and negative-phase waveforms to generate waveforms with secured dead-time as shown in Table 21.41. The adjusted change point of the negative-phase waveform is automatically set in the GTCCRB register. An internal signal is used to judge the change point of the positive-phase waveform, thus the value of the GTCCRA register is not updated by the adjusted value.

In saw-wave one-shot pulse mode, if the order of the change point becomes inconsistent by adjustment of the waveform change point due to occurrence of dead time errors, or if the change point exceeds the count period even after the adjustment, the complementary relation between the positive- and negative-phases cannot be guaranteed.

In triangle-wave PWM mode, if dead time exceeds the count period by setting 0x0000 0000 or a value greater than or equal to the setting value of the GTPR register is set in the GTCCRA register, output change is controlled by the output protection function (refer to section 21.8.4. Output Protection Function for GTIOCnm Pin Output (n = 0 to 9; m = A, B). When the GTCCRA register is greater than or equal to [GTPR register + GTDVm (m = U, D) register], [GTPR register - 1] is set in the GTCCRB register as the upper limit.

Automatic setting for a dead time value to the GTCCRB register is performed at the next count clock after the register value for calculating the automatic setting value is updated. In triangle-wave mode, it also can be done at the next count clock from the current crest.

Table 21.40 设置互补PWM模式4的示例(2of2)

No.	步骤名称	Description
8	设置缓冲区值	对于单缓冲区操作，在GTCCRD寄存器中设置数据（在计数开始后第一次缓冲区传输到GTCCRA寄存器时要传输的数据）。对于双缓冲操作，在GTCCRD寄存器中设置要在波峰的第一端传输的数据，在GTCCRF寄存器中设置要在波谷的第一端传输的数据。
9	设置死区时间值	在GTP32n通道的GTDVU中设置死区时间值。
10	开始计数操作	将GPT32n通道的GTCR.CST设置为1，开始计数操作。
11	设置要立即传输的比较匹配值	对于单缓冲区操作，设置数据（立即传送到GTCCRA寄存器）在 GTCCRD register. 对于双缓冲操作，将向下计数的比较匹配值设置为立即传送到GTCCRD寄存器中，并将向上计数的比较匹配值设置在GTCCRF寄存器中。 最后对GPT32n+2.GTCCRD寄存器进行设置。（数据被传送到临时寄存器。）

Note: n = 4, 7
m = A, B

21.3.4 自动死区时间设置功能

通过设置GTDTCR，可以自动将正波形的比较匹配值（GTCCRA值）和指定死区时间值（GTDVU和GTDVD值）得到的负波形与死区时间的比较匹配值设置为GTCCRB。

自动死区时间设置功能可用于锯齿波一次性脉冲模式和所有三角PWM模式。

可以为波形的前半部分和后半部分分别设置死区时间。负波形前半部分变化点的死区时间设置在GTDVU寄存器中，后半部分的死区时间设置在GTDVD寄存器中。通过将GTDTCR.TDFER位设置为1，也可以为前半部分和后半部分设置相同的死区时间。

GTDBU寄存器可以作为GTDVU寄存器的缓冲寄存器，GTDBD寄存器可以作为GTDVD寄存器的缓冲寄存器。缓冲区传输在周期结束时执行（在锯齿波模式下：GTCNT计数器上溢（向上计数）、下溢（向下计数）或GTCNT计数器清零；在三角波模式下：a槽）。

通过读取GTCCRB寄存器，自动计算出反相波形的变化点。使用自动死区时间设置功能时，禁止写入GTCCRB。

不要设置使波形变化点超过计数周期的死区时间。当进行任何会产生死区时间错误的死区时间设置时，调整正反相波形的变化点，以生成具有可靠死区时间的波形，如表21.41所示。调整后的反相波形变化点自动设置在GTCCRB寄存器中。内部信号用于判断正相波形的变化点，因此GTCCRA寄存器的值不会被调整后的值更新。

在锯齿波单发脉冲模式下，如果由于出现死区时间误差而通过调整波形变化点而导致变化点的顺序不一致，或者即使在调整后变化点超过了计数周期，则互补不能保证正反相之间的关系。

在三角波PWM模式下，如果通过设置0x00000000或在GTCCRA寄存器中设置大于或等于GTPR寄存器设置值的值超过计数周期，则输出变化由输出保护功能控制（参考21.8.4.GTIOCnm引脚输出的输出保护功能(n=0to9;m=A B).当GTCCRA寄存器大于等于[GTPR寄存器+GTDVm(m=U D)寄存器]、[GTPR寄存器1]在GTCCRB寄存器中设置为上限。

GTCCRB寄存器的死区时间值的自动设置在用于计算自动设置值的寄存器值更新后的下一个计数时钟执行。在三角波模式下，它也可以在当前波峰的下一个计数时钟完成。

Table 21.41 Adjustment of the Waveform Change Point When a Dead-Time Error Occurs

PWM Output Operating Mode	Count Direction	Period	Condition for Dead Time Error	Change Point of the Positive-Phase Waveform after Adjustment	Change Point of the Negative-Phase Waveform after Adjustment
Saw-wave one-shot pulse mode	Up-counting	First half	GTCCRA - GTDVU < 0	GTDVU	0
		Second half	GTCCRA + GTDVD > GTPR (GTCCRA + GTDVU > GTPR)*1	GTPR - GTDVD (GTPR - GTDVU)*1	GTPR
	Down-counting	First half	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
		Second half	GTCCRA - GTDVD < 0 (GTCCRA - GTDVU < 0)*1	GTDVD (GTDVU)*1	0
Triangle-wave PWM mode 1/2/3	Up-counting	(First half)	GTCCRA - GTDVU ≤ 0	GTDVU + 1	1
	Down-counting	(Second half)	GTCCRA - GTDVD < 0 (GTCCRA - GTDVU < 0)*1	GTDVD (GTDVU)*1	0

Note 1. In the case of GTDTCR.TDFER = 1.

Figure 21.80 to Figure 21.83 show examples of automatic dead time setting function operation. Table 21.42 and Table 21.43 show the setting examples.

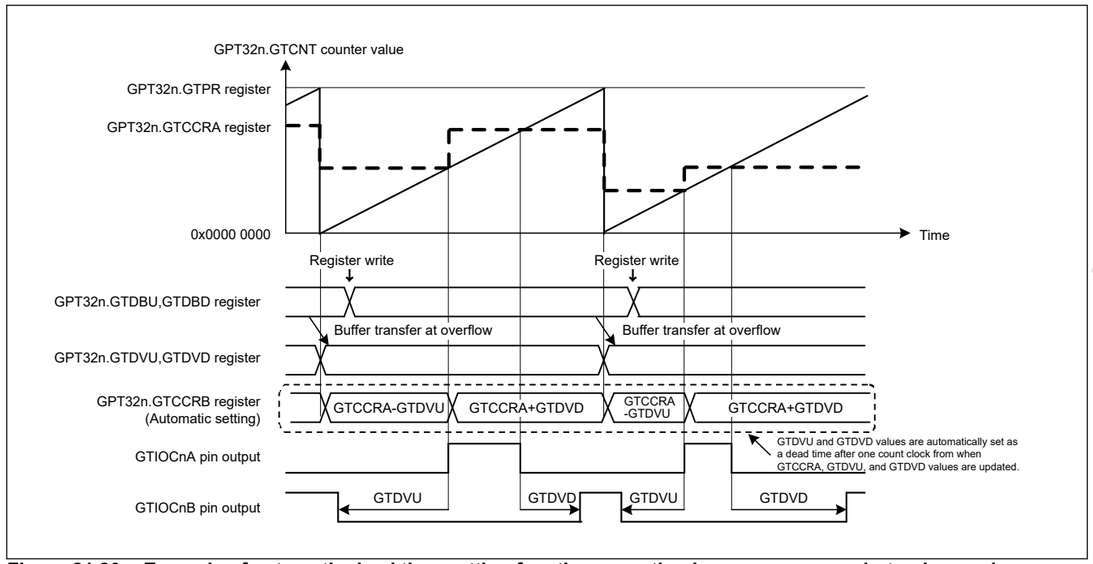


Figure 21.80 Example of automatic dead time setting function operation in saw-wave one-shot pulse mode, up-counting, GTDVU and GTDVD set to buffer operation, and active-high

Table 21.41 发生死区错误时波形变化点的调整

PWM Output Operating Mode	Count Direction	Period	死区时间错误的条件	变化点 正相波形后 Adjustment	变化点 后的负相位波形 Adjustment
锯波单脉冲模式	Up-counting	上半场	GTCCRA - GTDVU < 0	GTDVU	0
		下半场	GTCCRA + GTDVD > GTPR (GTCCRA + GTDVU > GTPR)*1	GTPR - GTDVD (GTPR - GTDVU)*1	GTPR
	Down-counting	上半场	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
		下半场	GTCCRA - GTDVD < 0 (GTCCRA - GTDVU < 0)*1	GTDVD (GTDVU)*1	0
Triangle-wave PWM mode 1/2/3	Up-counting	(First half)	GTCCRA - GTDVU ≤ 0	GTDVU + 1	1
	Down-counting	(Second half)	GTCCRA - GTDVD < 0 (GTCCRA - GTDVU < 0)*1	GTDVD (GTDVU)*1	0

注1.在GTDTCR.TDFER=1的情况下。

图21.80至图21.83显示了自动死区时间设置功能操作的示例。表21.42和表21.43显示了设置示例。

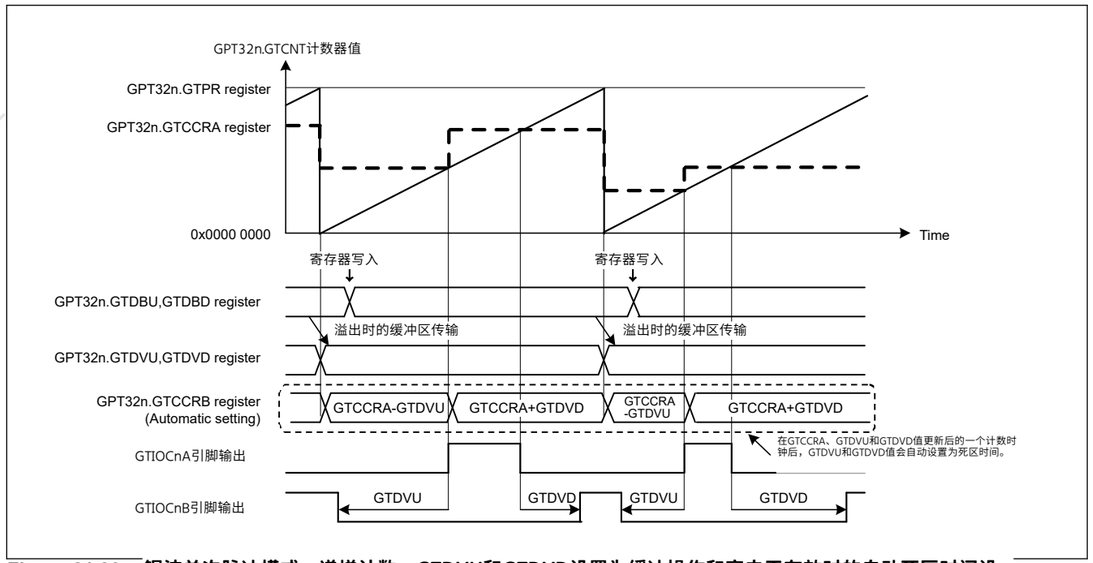


Figure 21.80 锯波单次脉冲模式、递增计数、GTDVU和GTDVD设置为缓冲操作和高电平有效时的自动死区时间设置功能操作示例

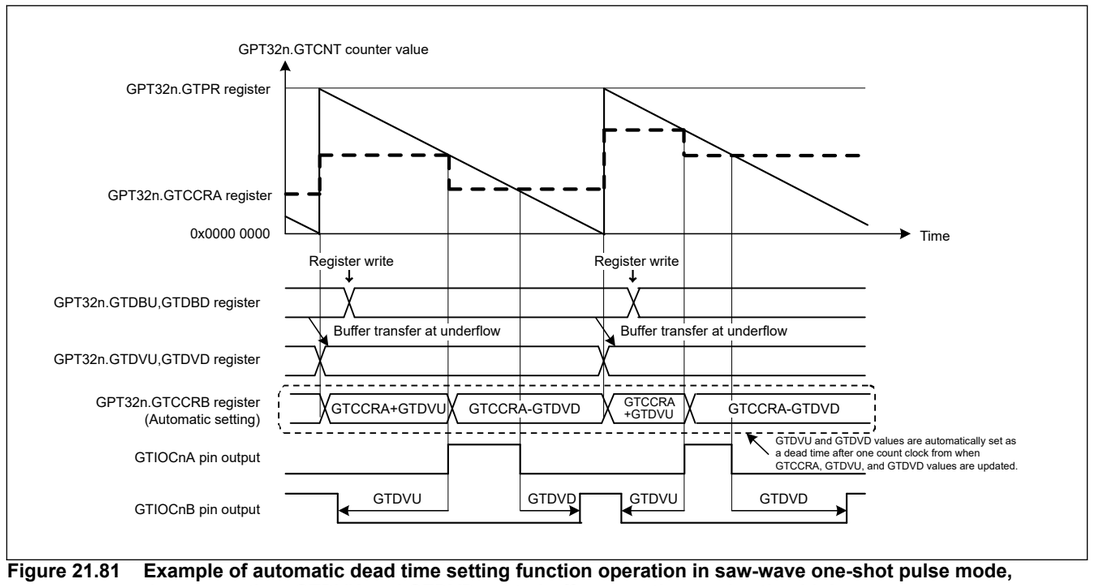


Figure 21.81 Example of automatic dead time setting function operation in saw-wave one-shot pulse mode, down-counting, GTDVU and GTDVD set to buffer operation, and active-high

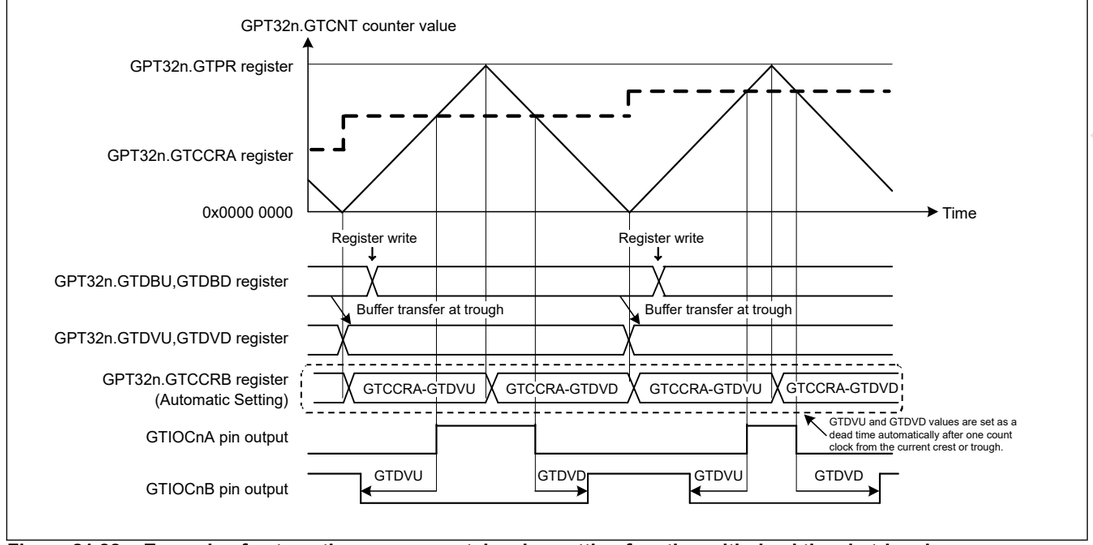


Figure 21.82 Example of automatic compare-match value setting function with dead time in triangle-wave PWM mode 1, GTDVU and GTDVD set to buffer operation, and active-high

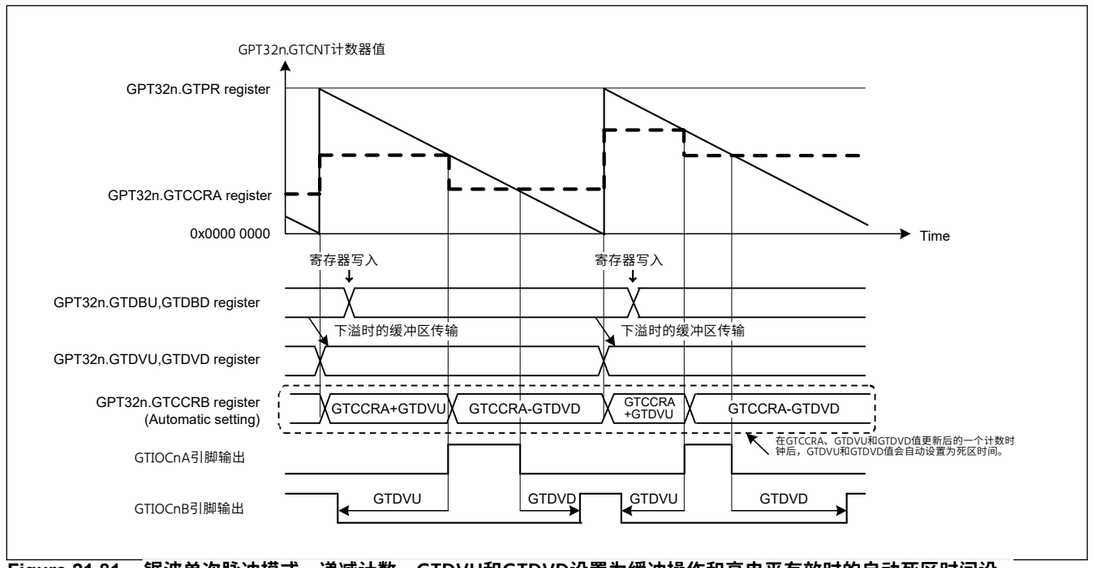


Figure 21.81 锯波单次脉冲模式、递减计数、GTDVU和GTDVD设置为缓冲操作和高电平有效时的自动死区时间设置功能操作示例

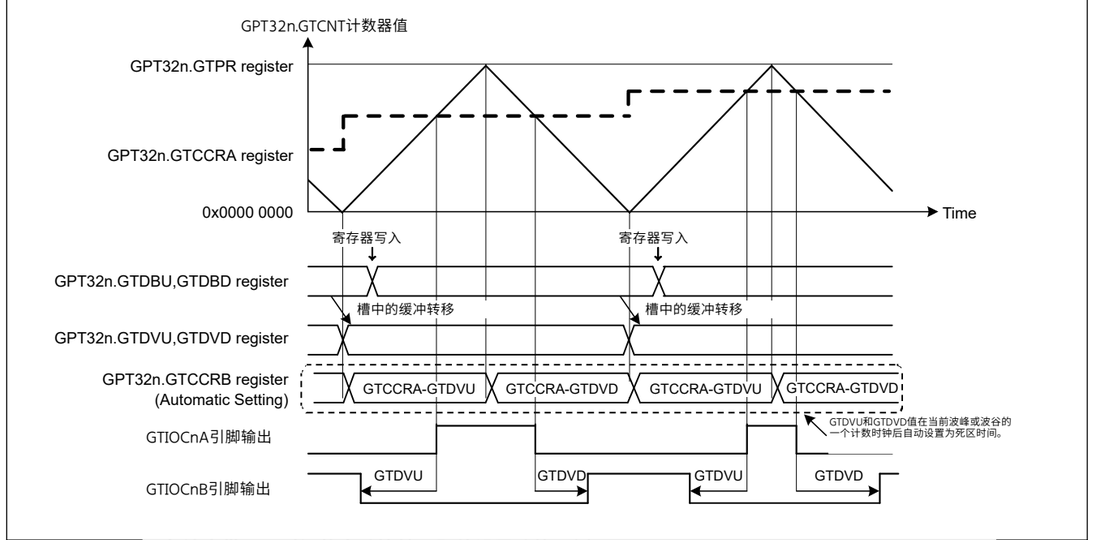


Figure 21.82 三角波中带死区时间的自动比较匹配值设置功能示例 PWM模式1，GTDVU和GTDVD设置为缓冲操作，高电平有效

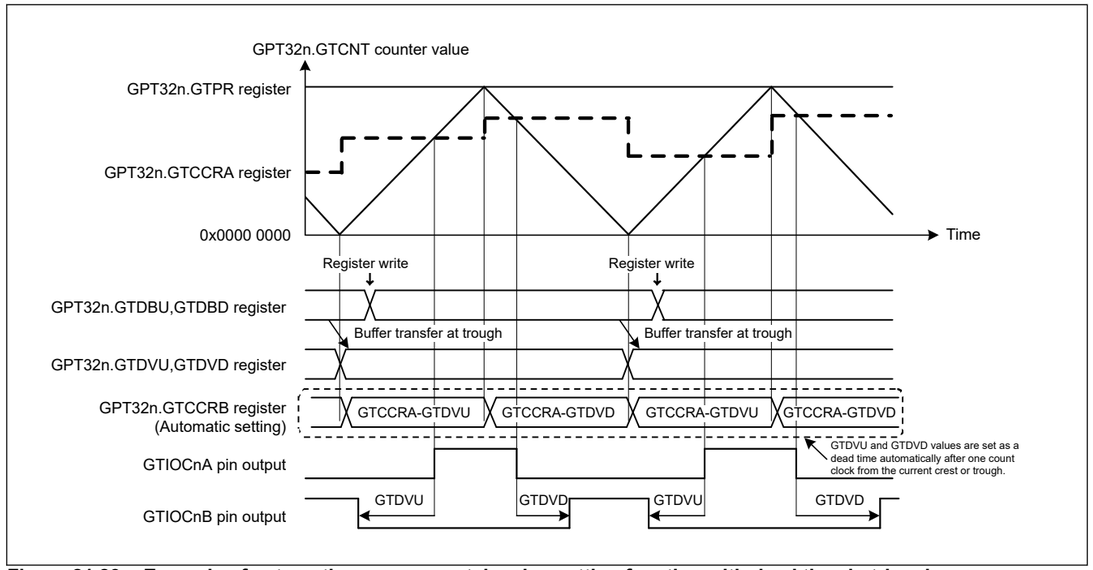


Figure 21.83 Example of automatic compare-match value setting function with dead time in triangle-wave PWM mode 2 or 3, GTDVU and GTDVD set to buffer operation, and active-high

Table 21.42 Example setting for automatic dead time setting function in saw-wave one-shot pulse mode, and triangle-wave PWM mode 3 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0] or GTCR.MD[3:0]. In Figure 21.80 and Figure 21.81, 001b or 0001b (saw-wave one-shot pulse mode) is set. In Figure 21.83, 110b or 0110b (triangle-wave PWM mode 3) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.80, 01b is set after 11b is set in GTUDDTYC[1:0] (up count). In Figure 21.81, 00b is set after 10b is set in GTUDDTYC[1:0] (down count).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 21.80, Figure 21.81, and Figure 21.83, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
7	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set buffer value for compare match*1	Set the GTIOCnA pin transition immediately after the count start in GTCCRC and GTCCRD.
9	Set forcible buffer transfer for compare match*1	Set GTBER.CCRSWT to 1 to transfer buffer register data forcibly to GTCCRA.
10	Set buffer value for compare match	Set the GTIOCnA pin transition in 1 cycle after the current cycle in GTCCRC and GTCCRD.
11	Set automatic dead time setting function	Set GTDTCR.TDE to 1 to enable the automatic dead time setting function.
12	Set buffer operation for dead time setting	Set buffer operation with TDBUE and TDBDE bits in GTDTCR.
13	Set dead time value	Set the first half dead time value in GTDVU and the second half dead time in GTDVD. When GTDVU is set with GTDTCR.TDFER bit set to 1, the same value is also set to GTDVD, the same dead time value can be set for the first and second halves.
14	Set buffer value for dead time	For buffer operation, set the first half dead time in one cycle after the current cycle in GTDBU and the second half dead time in GTDBD.

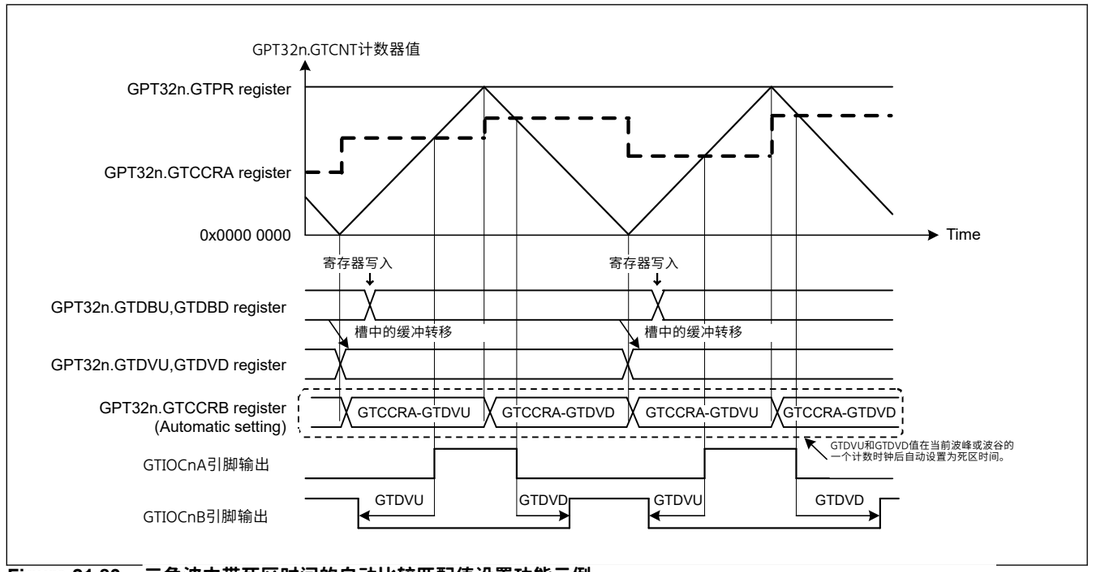


Figure 21.83 三角波中带死区时间的自动比较匹配值设置功能示例 PWM模式2或3，GTDVU和GTDVD设置为缓冲操作，高电平有效

Table 21.42 锯齿波一次性脉冲模式和三角波PWM模式3(1of2)中自动死区时间设置功能的示例设置

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]或GTCR.MD[3:0]设置操作模式。 在图21.80和图21.81中，设置了001b或0001b（锯波单发脉冲模式）。在图21.83中，设置了110b或0110b（三角波PWM模式3）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.80中，在GTUDDTYC[1:0]中设置了11b之后设置了01b（向上计数）。在图21.81中，在GTUDDTYC[1:0]中设置了10b之后设置了00b（向下计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图21.80、图21.81和图21.83中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
7	启用GTIOCnm引脚输出*1	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
8	为比较匹配设置缓冲区值*1	在GTCCRC和GTCCRD中计数开始后立即设置GTIOCnA引脚转换。
9	为比较匹配设置强制缓冲区传输*1	将GTBER.CCRSWT设置为1以强制将缓冲寄存器数据传输到GTCCRA。
10	设置比较匹配的缓冲区值	在GTCCRC和GTCCRD中的当前周期之后的1个周期内设置GTIOCnA引脚转换。
11	设置自动死区时间设置功能	将GTDTCR.TDE设置为1以启用自动死区时间设置功能。
12	设置死区时间设置的缓冲操作	使用GTDTCR中的TDBUE和TDBDE位设置缓冲区操作。
13	设置死区时间值	在GTDVU中设置前半死时间值，在GTDVD中设置后半死时间值。什么时候GTDVU设置为GTDTCR.TDFER位设置为1，GTDVD也设置相同的值，可以为前半部分和后半部分设置相同的死区时间值。
14	设置死区时间的缓冲区值	对于缓冲操作，在GTDBU中设置当前周期后一个周期的前半死区时间，在GTDBD中设置后半死区时间。

Table 21.42 Example setting for automatic dead time setting function in saw-wave one-shot pulse mode, and triangle-wave PWM mode 3 (2 of 2)

No.	Step Name	Description
15	Start count operation	Set GTCR.CST to 1 to start count operation.
16	Set buffer value for each cycle	Set the GTIOCnA pin transition in 1 cycle after the current cycle in GTCCRC and GTCCRD. When the dead time register is used for buffer operation, set the dead time value in the first half of the next cycle from the current cycle to GTDBU and the dead time value in the second half to GTDBD.

Note: n: 0 to 9
m: A, B
Note 1. When using PWM Delay Generation circuit, change the order of setting for Enable GTIOCnm pin output and setting for Set buffer value for compare match + Set forcible buffer transfer for compare match.

Table 21.43 Example setting for automatic dead time setting function in triangle-wave PWM mode 1 or 2

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0] or GTCR.MD[3:0]. In Figure 21.82, 100b or 0100b (triangle-wave PWM mode 1) is set. In Figure 21.83, 101b or 0101b (triangle-wave PWM mode 2) is set.
2	Select count clock	Select the count clock with GTCR.TPCS[3:0].
3	Set cycle	Set the cycle in GTPR.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 21.82 and Figure 21.83, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
7	Set buffer operation for compare match	Set buffer operation with CCRA in GTBER.
8	Set compare match value*1	Set the GTIOCnA pin transition in GTCCRA.
9	Set buffer value for compare match	For buffer operation, set the GTIOCnA pin transition in 1 cycle after the current cycle (in triangle-wave PWM mode 1) or half cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRC. For double buffer operation, also set the GTIOCnA pin transition in 2 cycles after the current cycle (in triangle-wave PWM mode 1) or 1 cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRD.
10	Set automatic dead time setting function	Set GTDTCR.TDE to 1 to enable the automatic dead time setting function.
11	Set buffer operation for dead time setting	Set buffer operation with TDBUE and TDBDE bits in GTDTCR.
12	Set dead time value	Set the first half dead time value in GTDVU and the second half dead time in GTDVD. When GTDVU is set with GTDTCR.TDFER bit set to 1, the same value is also set to GTDVD, the same dead time value can be set for the first and second halves.
13	Set buffer value for dead time	For buffer operation, set the first half dead time in one cycle after the current cycle in GTDBU and the second half dead time in GTDBD.
14	Start count operation	Set GTCR.CST to 1 to start count operation.
15	Set buffer value for each cycle	When the compare match register is used for buffer operation, set the GTIOCnA pin transition in 1 cycle after the current cycle (in triangle-wave PWM mode 1) or half cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRC. When the compare match register is used for double-buffered operation, set the GTIOCnA pin changing point in two cycles after the current cycle (in triangle-wave PWM mode 1) or one cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRD. In the same way, set the dead time value in the first half of the cycle after current cycle in GTDBU and the dead time in the second half in GTDBD.

Note: n: 0 to 9
m: A, B
Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnm pin output enable and setting for a compare match value.

Table 21.42 锯齿波一次性脉冲模式和三角波PWM模式3(2of2)中自动死区时间设置功能的示例设置

No.	步骤名称	Description
15	开始计数操作	将GTCR.CST设置为1以启动计数操作。
16	为每个周期设置缓冲区值	在GTCCRC和GTCCRD中的当前周期之后的1个周期内设置GTIOCnA引脚转换。当死区时间寄存器用于缓冲操作时，将当前周期下一个周期前半部分的死区时间值设置为GTDBU，后半部分的死区时间值设置为GTDBD。

Note: n: 0 to 9
m: A, B
注1.使用PWM延迟产生电路时，更改EnableGTIOCnmpinoutput的设置顺序和Setbuffervalueforcomparematch+Setforforcebuffertransferforcomparematch的设置顺序。

Table 21.43 三角波PWM模式1或2中自动死区时间设置功能的设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]或GTCR.MD[3:0]设置操作模式。 在图21.82中，设置了100b或0100b（三角波PWM模式1）。在图21.83中，设置了101b或0101b（三角波PWM模式2）。
2	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
3	设置周期	在GTPR中设置循环。
4	设置计数器的初始值	在GTCNT计数器中设置初始值。
5	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图21.82和图21.83中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
6	启用GTIOCnm引脚输出*1	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
7	为比较匹配设置缓冲区操作	在GTBER中使用CCRA设置缓冲区操作。
8	设置比较匹配值*1	在GTCCRA中设置GTIOCnA引脚转换。
9	设置比较匹配的缓冲区值	对于缓冲操作，在GTCCRC中将GTIOCnA引脚转换设置为当前周期后的1个周期（三角波PWM模式1）或当前周期后的半个周期（三角波PWM模式2）。 对于双缓冲器操作，在GTCCRD中还设置GTOCnA引脚在当前周期后2个周期（三角波PWM模式1）或当前周期后1个周期（三角波PWM模式2）。
10	设置自动死区时间设置功能	将GTDTCR.TDE设置为1以启用自动死区时间设置功能。
11	设置死区时间设置的缓冲操作	使用GTDTCR中的TDBUE和TDBDE位设置缓冲区操作。
12	设置死区时间值	在GTDVU中设置前半死时间值，在GTDVD中设置后半死时间值。什么时候GTDVU设置为GTDTCR.TDFER位设置为1，GTDVD也设置相同的值，可以为前半部分和后半部分设置相同的死区时间值。
13	设置死区时间的缓冲区值	对于缓冲操作，在GTDBU中设置当前周期后一个周期的前半死区时间，在GTDBD中设置后半死区时间。
14	开始计数操作	将GTCR.CST设置为1以启动计数操作。
15	为每个周期设置缓冲区值	当比较匹配寄存器用于缓冲操作时，在GTCCRC中设置GTIOCnA引脚在当前周期后1个周期（三角波PWM模式1）或当前周期后半个周期（三角波PWM模式2）.当比较匹配寄存器用于双缓冲操作时，在当前周期后两个周期（三角波PWM模式1）或当前周期后一个周期（三角波PWM模式2）设置GTIOCnA引脚变化点)在GTCCRD中。同理，在GTDBU中设置当前周期后的前半个周期的死区时间值，在GTDBD中设置后半个周期的死区时间值。

Note: n: 0 to 9
m: A, B
注1.使用PWM延迟产生电路时，更改GTIOCnm引脚输出使能设置和比较匹配值设置的顺序。

21.3.5 Count Direction Changing Function

The count direction of the GTCNT counter can be changed by modifying the UD bit in GTUDDTYC.

In saw-wave mode, if the UD bit in GTUDDTYC is modified during count operation, the count direction is changed at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.UD bit is modified while the count operation stops and the GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit modification is not reflected at the start of counting and the count direction is changed at an overflow or an underflow. If the UDF bit is set to 1 while the count operation stops, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

In triangle-wave mode, the count direction does not change even though the UD bit in GTUDDTYC is modified during the count operation. Similarly, even though the GTUDDTYC.UD bit is modified while the count operation stops and GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit value is not reflected to the count operation. If the GTUDDTYC.UDF bit is set to 1 while the count operation is stopped, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

If the count direction changes during a saw-wave count operation, the GTPR value after the start of up-counting is reflected in the count cycle during up-counting and the GTPR value after the start of down-counting is reflected in the count cycle during down-counting.

Figure 21.84 shows an example of count direction changing function operation.

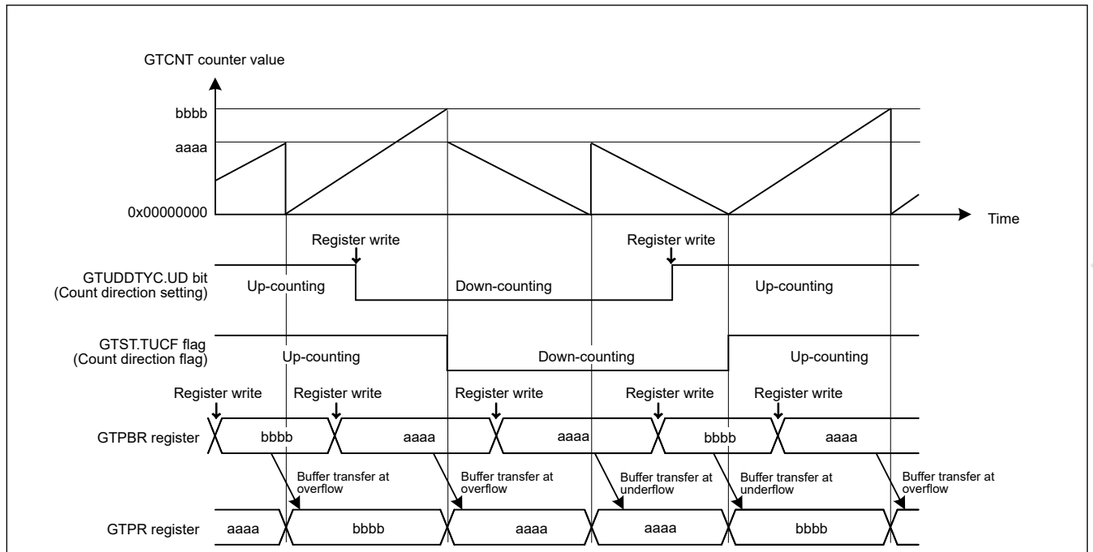


Figure 21.84 Example of a count direction changing function operation during buffer operation

21.3.6 Function of Output Duty 0% and 100%

The output duty of the GTIOCnA pin and the GTIOCnB pin (n = 0 to 9) are set to 0% or 100% by changing the GTUDDTYC.OADTY bit or GTUDDTYC.OBDTY bit.

This function is invalid in saw-wave PWM mode 2 or complementary PWM mode.

In saw-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an overflow or an underflow. If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 1, the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit value at that time is reflected at the start of counting.

21.3.5 计数方向改变功能

GTCNT计数器的计数方向可以通过修改GTUDDTYC中的UD位来改变。

在锯齿波模式下，如果在计数操作期间修改GTUDDTYC中的UD位，则计数方向会在溢出（在向上计数期间修改时）或下溢（在向下计数期间修改时）改变。如果在计数操作停止时修改GTUDDTYC.UD位且GTUDDTYC.UDF位为0，则GTUDDTYC.UD位的修改不会反映在计数开始时，并且计数方向会在上溢或下溢时改变。如果在计数操作停止时UDF位设置为1，则此时的GTUDDTYC.UD位值将反映在计数开始时。

在三角波模式下，即使在计数操作期间修改GTUDDTYC中的UD位，计数方向也不会改变。同样，即使在计数操作停止且GTUDDTYC.UDF位为0时修改GTUDDTYC.UD位，GTUDDTYC.UD位的值也不会反映到计数操作中。如果在计数操作停止时将GTUDDTYC.UDF位设置为1，则此时的GTUDDTYC.UD位值将反映在计数开始时。

如果在锯齿波计数操作期间计数方向发生变化，则加计数开始后的GTPR值反映在加计数期间的计数周期中，而减计数开始后的GTPR值反映在计数周期中在向下计数期间。

图21.84显示了计数方向改变功能操作的示例。

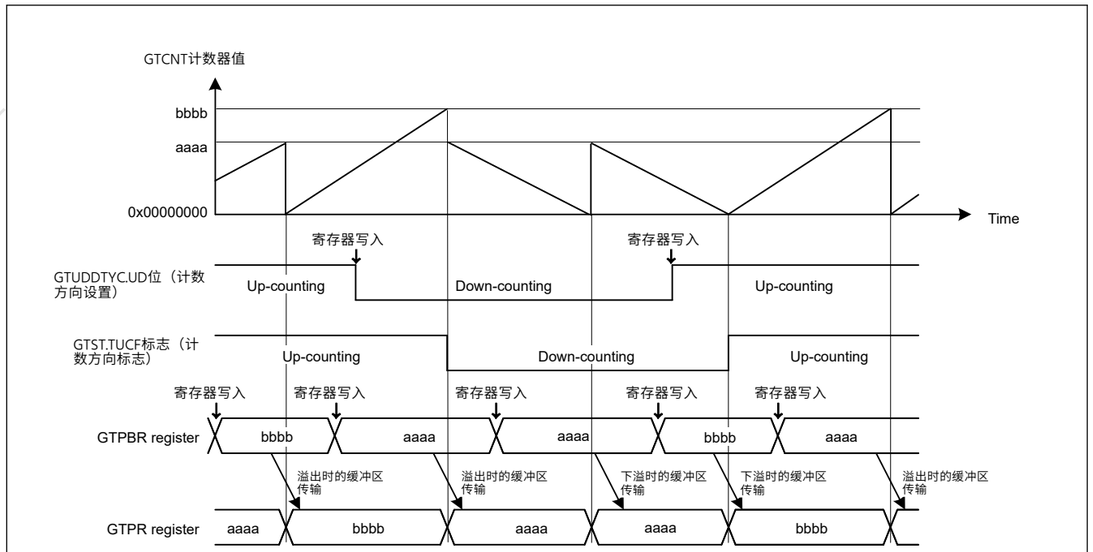


Figure 21.84 缓冲操作期间的计数方向改变功能操作示例

21.3.6 输出占空比0%和100%的功能

GTIOCnA引脚和GTIOCnB引脚（n=0至9）的输出占空比通过更改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位。

该功能在锯齿波PWM模式2或互补PWM模式下无效。

在锯齿波模式下，如果在计数操作期间修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则输出占空比设置反映在溢出（在向上计数期间修改时）或下溢（在向下期间修改时–数数）。如果在计数操作停止且GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位为0时修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则在计数开始时不反映输出占空比修改。输出占空比在上溢或下溢时发生变化。如果GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位在计数操作停止并且

GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位为1，此时的GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位的值反映在计数开始时。

In triangle-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected an underflow.

If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an underflow. If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation stops and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 1, the output duty modification is reflected at the start of counting.

In performing 0% or 100% duty operation, GPT internally continues to:

- Perform compare match operation
- Set compare match flag
- Output interrupt
- Perform buffer operation.

When the control is changed from 0% or 100% duty setting to compare match, the output value of GTIOCnA pin at cycle end is decided by GTIOR.GTIOA[3:2] and GTUDDTYC.OADTYR. The output value of GTIOCnB pin at cycle end is decided by GTIOR.GTIOB[3:2] and GTUDDTYC.OBDTYR.

When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 01b, the output pins output low at cycle end. When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 10b, the output pins output high at cycle end.

GTUDDTYC.OADTYR selects the value that is the object of output retained/toggled at cycle end, when GTIOR.GTIOm[3:2] are set to 00b (output retained at cycle end) or when GTIOR.GTIOm[3:2] are set to 11b (output toggled at cycle end). Table 21.44 shows the values of GTIOCnA and GTIOCnB pin output at cycle end.

Table 21.44 Output values after releasing 0% or 100% duty setting (m = A, B)

GTIOR.GTIOm[3:2]	Compare match value at cycle end masked by 0% or 100% duty setting	GTUDDTYC.OmDTYR in duty 0% setting		GTUDDTYC.OmDTYR in duty 100% setting	
		0	1	0	1
00 (output retained at cycle end)	0	0	0	1	0
	1	0	1	1	1
01 (low output at cycle end)	—	0	0	0	0
10 (high output at cycle end)	—	1	1	1	1
11 (output toggled at cycle end)	0	1	1	0	1
	1	1	0	0	0

Figure 21.85 shows an example of output duty 0% and 100% function.

在三角波模式下，如果在计数操作期间修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则输出占空比设置反映为下溢。

如果在计数操作停止且GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位为0时修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则在计数开始时不反映输出占空比修改。输出占空比在下溢时发生变化。如果在计数操作停止且GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位为1时修改了GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则输出占空比修改将反映在计数开始时。

在执行0%或100%占空比操作时，GPT在内部继续：

- ●执行比较匹配操作
- ●设置比较匹配标志
- ●输出中断
- ●执行缓冲操作。

当控制从0%或100%占空比设置更改为比较匹配时，周期结束时GTIOCnA引脚的输出值由GTIOR.GTIOA[3:2]和GTUDDTYC.OADTYR决定。周期结束时GTIOCnB引脚的输出值由GTIOR.GTIOB[3:2]和GTUDDTYC.OBDTYR决定。

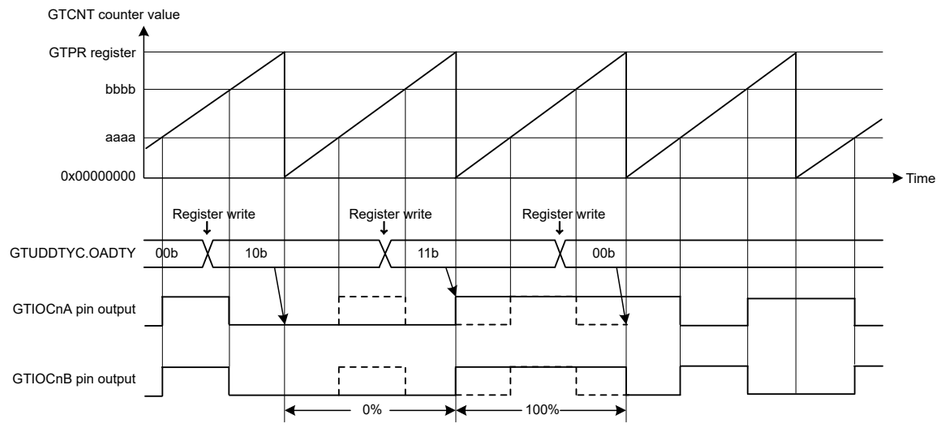
当GTIOR.GTIOA[3:2]和GTIOR.GTIOB[3:2]设置为01b时，输出引脚在周期结束时输出低电平。什么时候GTIOR.GTIOA[3:2]和GTIOR.GTIOB[3:2]设置为10b，输出引脚在周期结束时输出高电平。

GTUDDTYC.OADTYR当GTIOR.GTIOm[3:2]设置为00b（在循环结束时保持输出）或GTIOR.GTIOm[3:2]设置时，选择作为在循环结束时切换的输出保留对象的值到11b（输出在循环结束时切换）。表21.44显示了循环结束时GTIOCnA和GTIOCnB引脚输出的值。

Table 21.44 释放0%或100%占空比设置后的输出值(m=A B)

GTIOR.GTIOm[3:2]	比较被0%或100%占空比设置屏蔽的循环结束时的匹配值	GTUDDTYC.OmDTYR在占空比0%设置		GTUDDTYC.OmDTYR占空比100%设置	
		0	1	0	1
00（循环结束时保留输出）	0	0	0	1	0
	1	0	1	1	1
01（循环结束时输出低）	—	0	0	0	0
10（循环结束时的高输出）	—	1	1	1	1
11（循环结束时切换输出）	0	1	1	0	1
	1	1	0	0	0

图21.85显示了输出占空比0%和100%功能的示例。



Note: The base address of registers are the same.

Note: [Setting examples]

GTIOR.GTIOA[4:0] bits:	00011b initial low output, output toggled at compare match, output retained at cycle end
GTUDDTYC.OADTYR bit:	0b The function selected by GTIOA[3:2] is applied to the output value when the duty cycle is set after release from 0 or 100% duty-cycle setting.
GTIOR.GTIOB[4:0] bits:	00011b initial low output, output toggled at compare match, output retained at cycle end
GTUDDTYC.OBDTYR bit:	1 The function of GTIOB[3:2] is applied to the compare match output value which is masked after 0 or 100% duty setting release.

Figure 21.85 Example of output duty 0% and 100% function

21.3.7 Hardware Count Start/Count Stop and Clear Operation

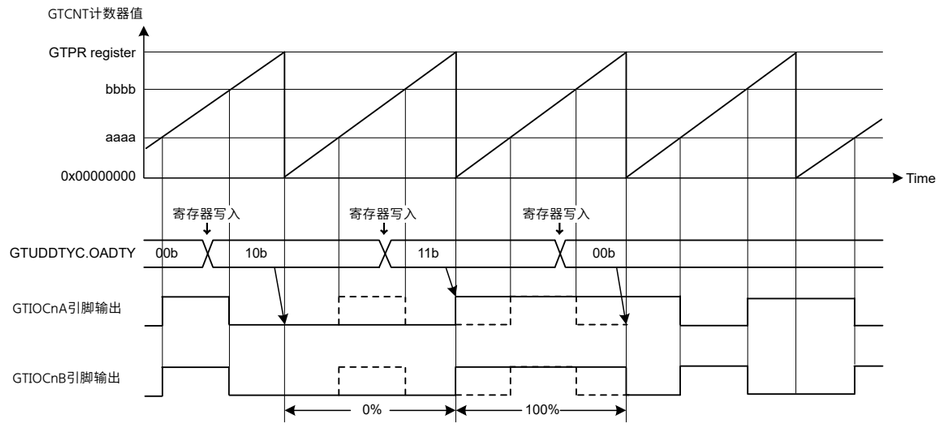
The GTCNT counter can be started, stopped, or cleared by the following hardware sources:

- External trigger input
- ELC event input
- GTIOCnA and GTIOCnB pin input (n = 0 to 9).

21.3.7.1 Hardware Start Operation

The GTCNT counter can be started by selecting a hardware source using GTSSR.

Figure 21.86 shows an example of a count start operation by a hardware source. Table 21.45 shows the setting example.



Note: 寄存器的基地址相同。

Note: [Setting examples]

GTIOR.GTIOA[4:0] bits:	00011b初始低输出，在比较匹配时切换输出，在循环结束时保持输出
GTUDDTYC.OADTYR bit:	0b在从0或100%占空比设置释放后设置占空比时，由GTIOA[3:2]选择的功能应用于输出值。
GTIOR.GTIOB[4:0] bits:	00011b初始低输出，在比较匹配时切换输出，在循环结束时保持输出
GTUDDTYC.OBDTYR bit:	1GTIOB[3:2]的功能应用于在0或100%占空比设置释放后被屏蔽的比较匹配输出值。

Figure 21.85 输出占空比0%和100%功能示例

21.3.7 硬件计数开始计数停止和清除操作

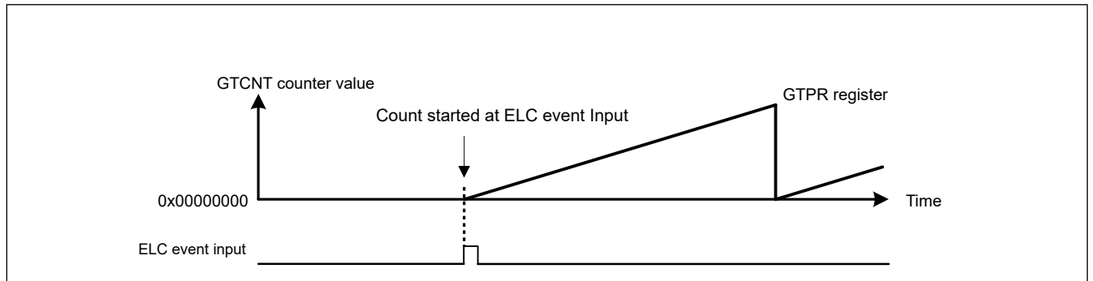
GTCNT计数器可以由以下硬件源启动、停止或清除：

- ●外部触发输入
- ●ELC事件输入
- ●GTIOCnA和GTIOCnB引脚输入（n=0到9）。

21.3.7.1 硬件启动操作

GTCNT计数器可以通过使用GTSSR选择硬件源来启动。

图21.86显示了一个硬件源的计数开始操作示例。表21.45显示了设置示例。



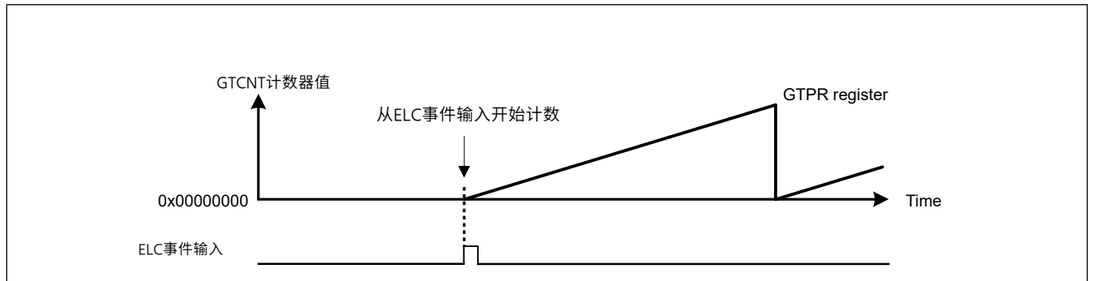
Note: ELC event input: ELC_GPTA event input

Figure 21.86 Example of count start operation by a hardware source started at the input of the signal from the ELC_GPTA event

Table 21.45 Example setting for count start operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.86, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.86, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 21.86, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation in the GTSSR register. In Figure 21.86, GTSSR.SSELCA = 1
7	Set hardware source operation	Set operation of the hardware source selected by the GTSSR register and start counting. In Figure 21.86, the ELC_GPTA event input operation is set.

Figure 21.87 shows an example of timing of operations to start counting in response to a rising edge of the input on the GTETRGA pin.



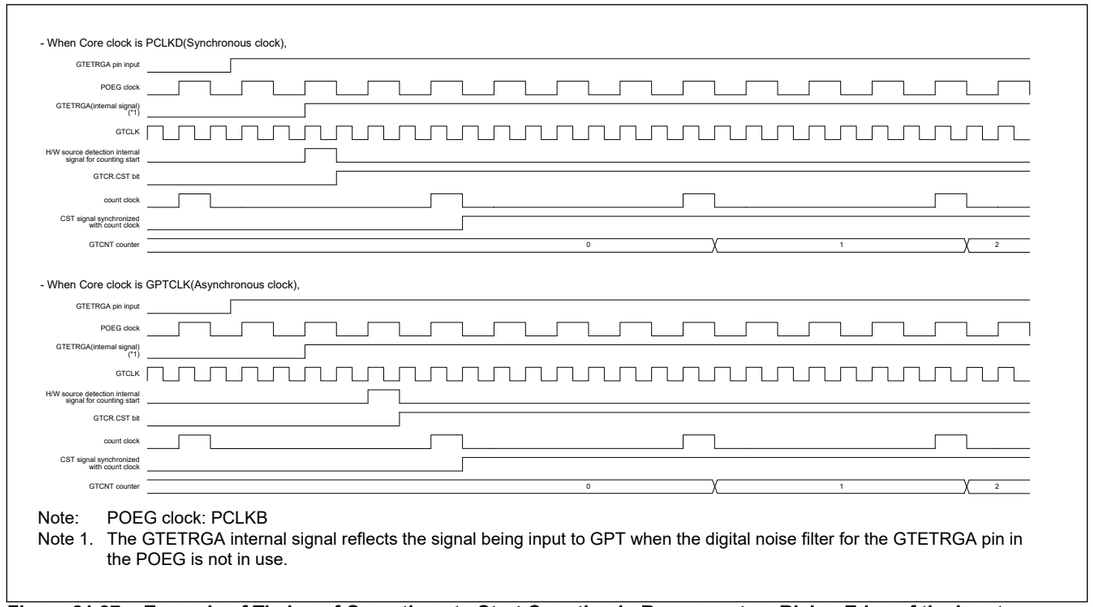
Note: ELC事件输入：ELC_GPTA事件输入

Figure 21.86 从ELC_GPTA事件的信号输入开始的硬件源的计数开始操作示例

Table 21.45 硬件源的计数开始操作设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.86中，设置了000b或0000b（锯齿波PWM模式1）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.86中，在GTUDDTYC[1:0]位中设置了11b之后，在GTUDDTYC[1:0]位中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	在GTPR寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图21.86中，设置了0x00000000。
6	设置硬件计数开始	在GTSSR寄存器中选择开始计数操作的硬件源。 在图21.86中，GTSSR.SSELCA=1
7	设置硬件源操作	设置GTSSR寄存器选择的硬件源的操作并开始计数。 在图21.86中，设置了ELC_GPTA事件输入操作。

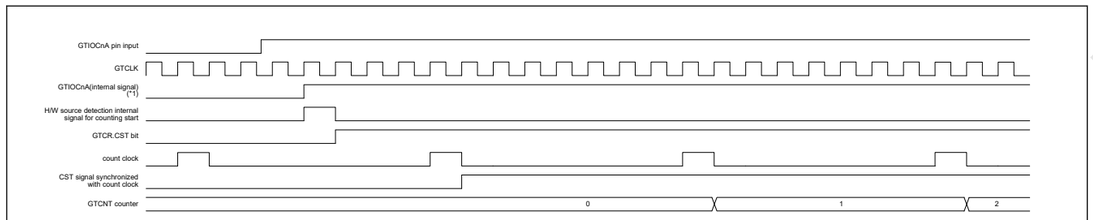
图21.87显示了响应于输入的上升沿开始计数的操作时序示例
GTETRGA pin.



Note: POEG clock: PCLKB
Note 1. The GTETRGA internal signal reflects the signal being input to GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use.

Figure 21.87 Example of Timing of Operations to Start Counting in Response to a Rising Edge of the Input on the GTETRGA Pin

Figure 21.88 shows an example of timing of operations to start counting in response to a rising edge of the input on the GTIOCnA pin.



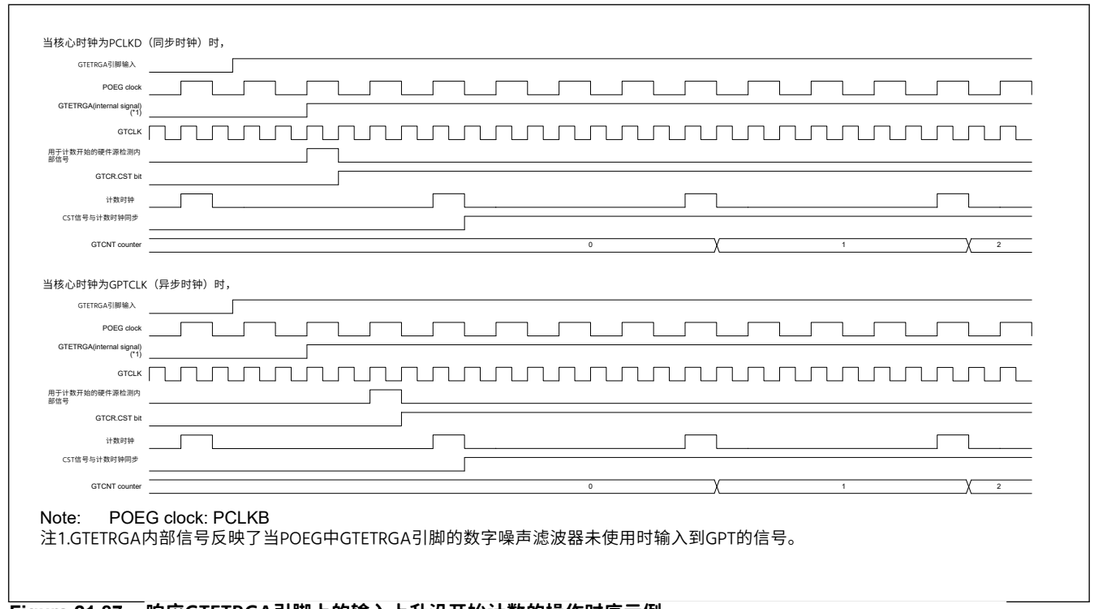
Note 1. This is the case when the digital noise filter is not in use.

Figure 21.88 Example of Timing of Operations to Start Counting in Response to a Rising Edge of the Input on the GTIOCnA Pin

Figure 21.89 shows an example of the timing of operations to start counting in response to ELC_GPTA event input.

This is an example of operations to start counting by the GPT321.GTCNT counter in response to a signal. An event signal is output to the ELC after matches in comparison with the GPT320.GTCCRA register. This is selected as a trigger for output to the GPT321 by the ELC as ELC_GPTA.

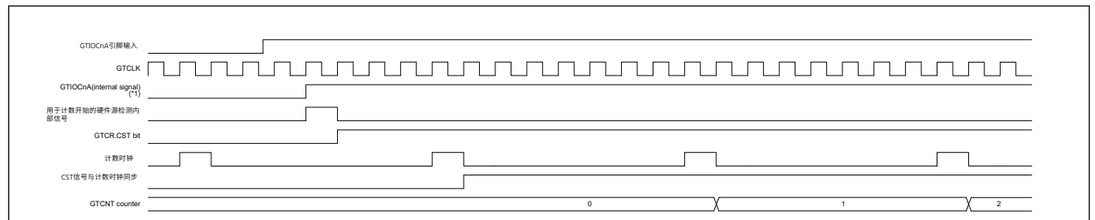
ELC passes the event signal output from GPT320 without delay to GPT321.



Note: POEG clock: PCLKB
注1.GTETRGA内部信号反映了当POEG中GTETRGA引脚的数字噪声滤波器未使用时输入到GPT的信号。

Figure 21.87 响应GTETRGA引脚上的输入上升沿开始计数的操作时序示例

图21.88显示了响应于输入的上升沿开始计数的操作时序示例
GTIOCnA pin.



注1.这是不使用数字噪声滤波器时的情况。

Figure 21.88 响应GTIOCnA引脚上的输入上升沿开始计数的操作时序示例

图21.89显示了响应ELC_GPTA事件输入开始计数的操作时序示例。

这是GPT321.GTCNT计数器响应信号开始计数的操作示例。与GPT320.GTCCRA寄存器比较匹配后，向ELC输出一个事件信号。这被ELC选作ELC_GPTA输出到GPT321的触发器。

ELC将GPT320输出的事件信号无延迟地传递给GPT321。

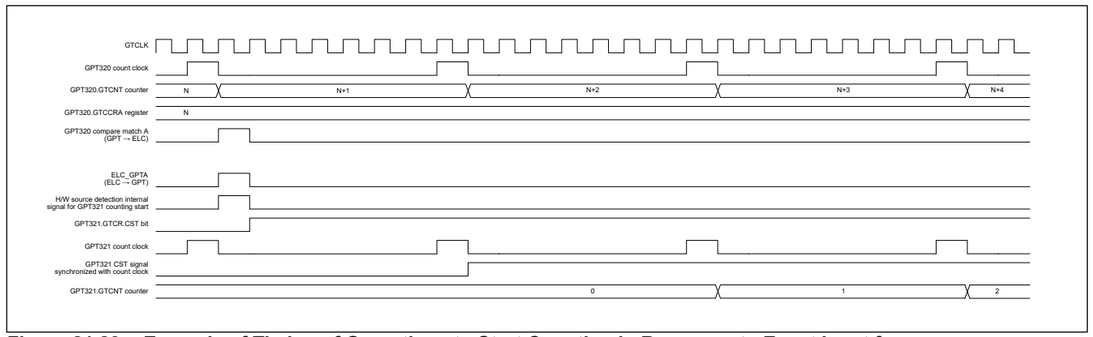
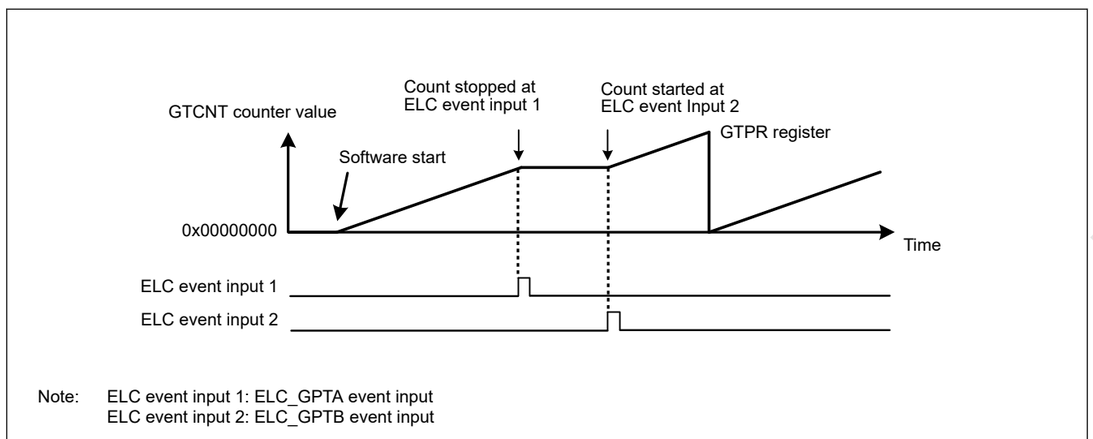


Figure 21.89 Example of Timing of Operations to Start Counting in Response to Event Input from ELC_GPTA

21.3.7.2 Hardware Stop Operation

The GTCNT counter can be stopped by selecting a hardware source using GTPSR.

Figure 21.90 shows an example of a count stop operation by a hardware source. Table 21.46 shows the setting example. In this example, the count operation stops at the ELC_GPTA event input and restarts at the ELC_GPTB event input.



Note: ELC event input 1: ELC_GPTA event input
ELC event input 2: ELC_GPTB event input

Figure 21.90 Example of count stop operation by hardware source started by software, stopped at ELC_GPTA input, and restarted at ELC_GPTB input

Table 21.46 Example setting for count stop operation by a hardware source (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0] or GTCR.MD[3:0]. In Figure 21.90, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.90, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 21.90, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation in GTSSR register, and wait for count start by the hardware source. In Figure 21.90, GTSSR.SSELCB = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation in GTPSR register and wait for count stop by the hardware source. In Figure 21.90, GTPSR.PSELCA = 1.

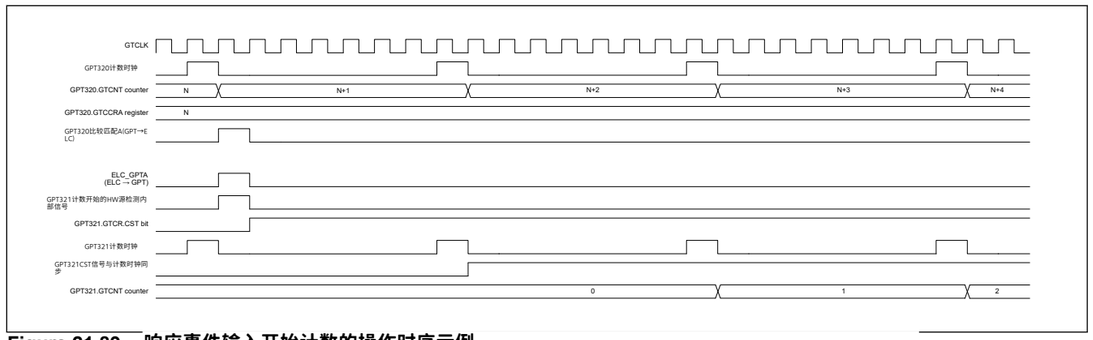
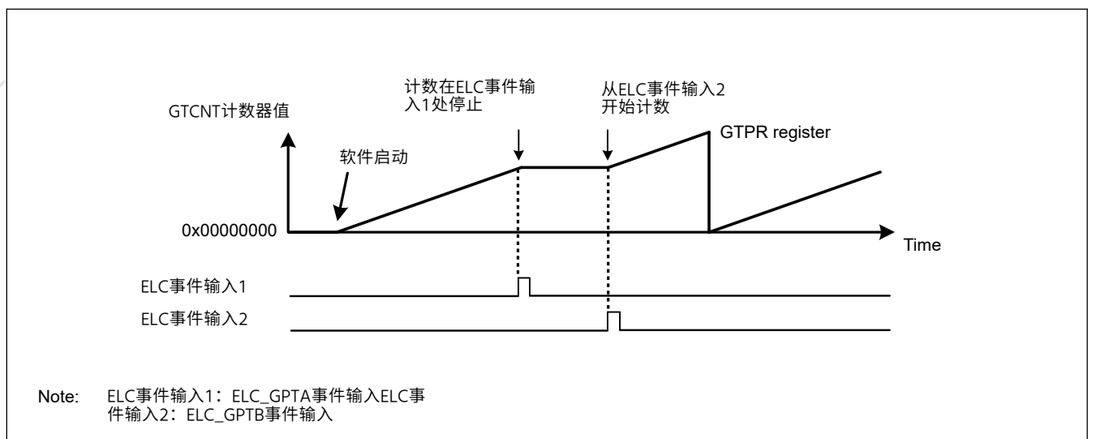


Figure 21.89 响应事件输入开始计数的操作时序示例 ELC_GPTA

21.3.7.2 硬件停止操作

GTCNT计数器可以通过使用GTPSR选择硬件源来停止。

图21.90显示了一个硬件源的计数停止操作示例。设置示例如表21.46所示。在此示例中，计数操作在ELC_GPTA事件输入处停止，并在ELC_GPTB事件输入处重新开始。



Note: ELC事件输入1：ELC_GPTA事件输入ELC事件输入2：ELC_GPTB事件输入

Figure 21.90 由软件启动的硬件源的计数停止操作示例，停止于ELC_GPTA输入，并在ELC_GPTB输入处重新启动

Table 21.46 硬件源的计数停止操作设置示例（2个中的1个）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]或GTCR.MD[3:0]设置操作模式。 在图21.90中，设置了000b或0000b（锯齿波PWM模式1）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.90中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图21.90中，设置了0x00000000。
6	设置硬件计数开始	在GTSSR寄存器中选择一个开始计数操作的硬件源，等待硬件源开始计数。在图21.90中，GTSSR.SSELCB=1。
7	设置硬件计数停止	在GTPSR寄存器中选择一个停止计数操作的硬件源，等待硬件源停止计数。在图21.90中，GTPSR.PSELCA=1。

Table 21.46 Example setting for count stop operation by a hardware source (2 of 2)

No.	Step Name	Description
8	Set hardware source operation	Set operation of the hardware source selected in GTSSR register or GTPSR register, and start or stop counting. In Figure 21.90, ELC_GPTA input operation and ELC_GPTB input operation are set.

Figure 21.91 shows an example of a count start/stop operation by a hardware source. Table 21.47 shows the setting example. In this example, the counter operates during the high-level periods of the external trigger input GTETRGA.

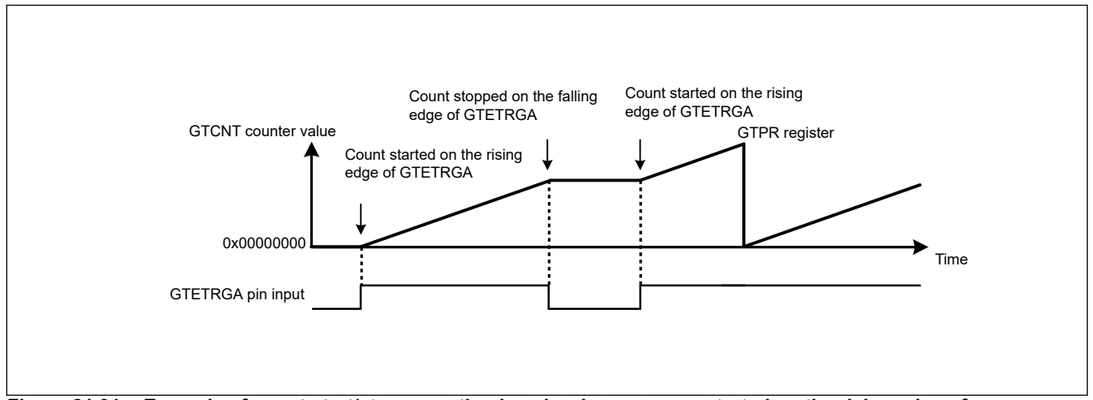


Figure 21.91 Example of count start/stop operation by a hardware source started on the rising edge of GTETRGA pin input, and stopped on the falling edge of GTETRGA pin input

Table 21.47 Example setting for count start/stop operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.91, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.91, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 21.91, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation with the GTSSR register, and wait for count start by the hardware source. In Figure 21.91, GTSSR.SSGTRGAR = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation with the GTPSR register, and wait for count stop by the hardware source. In Figure 21.91, GTPSR.PSGTRGAF = 1.
8	Set hardware source operation	Set operation of the hardware source selected in the GTSSR register or GTPSR register and start or stop counting. In Figure 21.91, the GTETRGA pin operation is set.

Figure 21.92 shows an example of timing of operations to stop counting in response to a rising edge of the input on the GTETRGA pin.

Table 21.46 硬件源的计数停止操作设置示例（2of2）

No.	步骤名称	Description
8	设置硬件源操作	设置在GTSSR寄存器或GTPSR寄存器中选择的硬件源的操作，并开始或停止计数。在图21.90中，设置了ELC_GPTA输入操作和ELC_GPTB输入操作。

图21.91显示了一个硬件源的计数开始停止操作示例。表21.47显示了设置示例。
在本例中，计数器在外部触发输入GTETRGA的高电平期间运行。

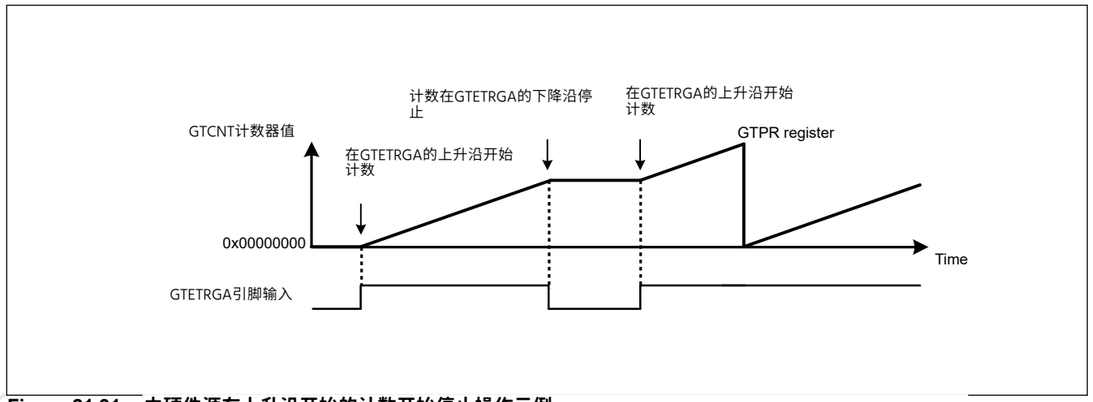
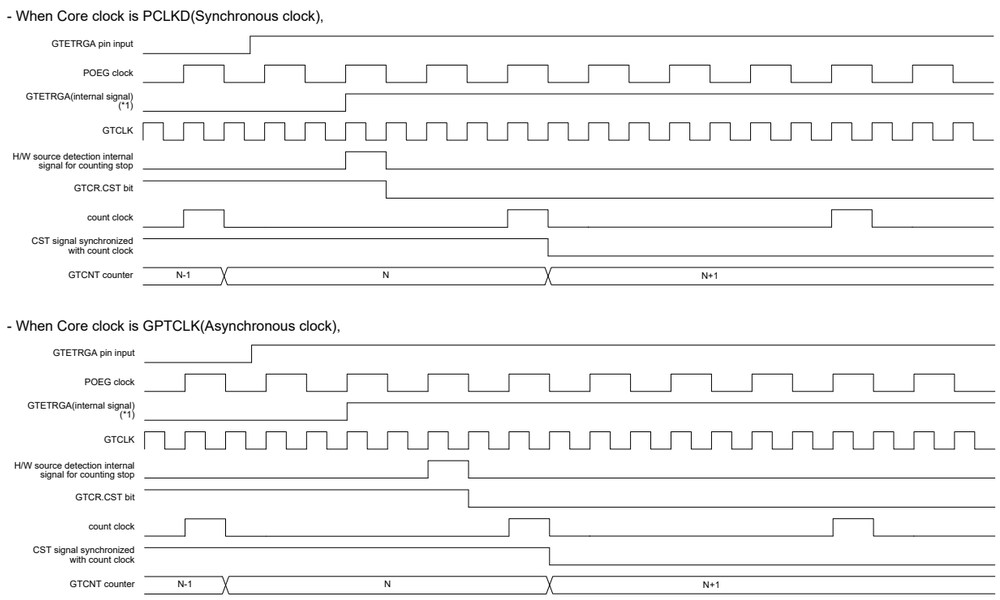


**Figure 21.91 由硬件源在上升沿开始的计数开始停止操作示例
GTETRGA引脚输入，并在GTETRGA引脚输入的下降沿停止**

Table 21.47 硬件源的计数开始停止操作设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.91中，设置了000b或0000b（锯齿波PWM模式1）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.91中，在GTUDDTYC[1:0]位中设置了11b之后，在GTUDDTYC[1:0]位中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	在GTPR寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图21.91中，设置了0x00000000。
6	设置硬件计数开始	通过GTSSR寄存器选择开始计数操作的硬件源，并等待硬件源开始计数。在图21.91中，GTSSR.SSGTRGAR=1。
7	设置硬件计数停止	使用GTPSR寄存器选择停止计数操作的硬件源，并等待硬件源停止计数。在图21.91中，GTPSR.PSGTRGAF=1。
8	设置硬件源操作	设置在GTSSR寄存器或GTPSR寄存器中选择的硬件源的操作并开始或停止计数。在图21.91中，设置了GTETRGA引脚操作。

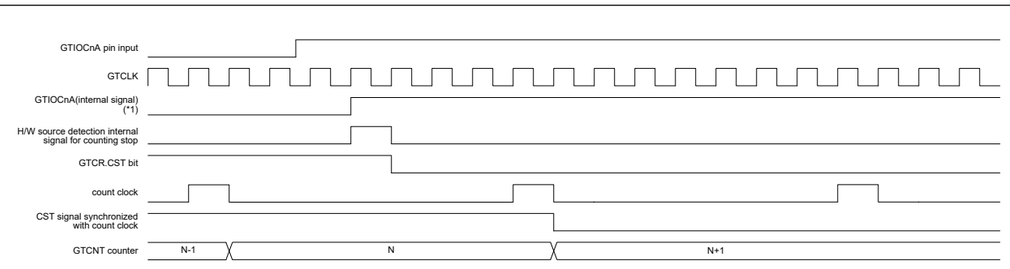
图21.92显示了响应于输入的上升沿停止计数的操作时序示例
GTETRGA pin.



Note: POEG clock: PCLKB
Note 1. The GTETRGA internal signal reflects the signal being input to GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use

Figure 21.92 Example of Timing of Operations to Stop Counting in Response to a Rising Edge of the Input on the GTETRGA Pin

Figure 21.93 shows an example of timing of operations to stop counting in response to a rising edge of the input on the GTIOCnA pin.



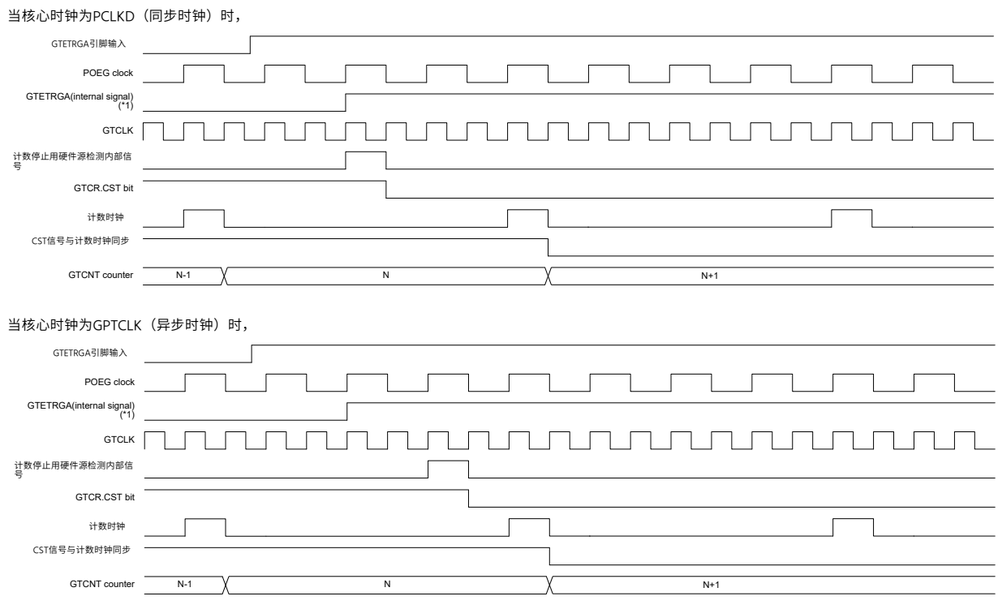
Note 1. This is the case when the digital noise filter is not in use.

Figure 21.93 Example of Timing of Operations to Stop Counting in Response to a Rising Edge of the Input on the GTIOCnA Pin

Figure 21.94 shows an example of timing of operations to stop counting in response to event input from ELC_GPTA.

This is an example of operations to stop counting by the GPT321.GTCNT counter in response to a signal. An event signal is output to the ELC after matches in comparison with the GPT320.GTCCRA register. This is selected as a trigger for output to the GPT321 by the ELC as ELC_GPTA.

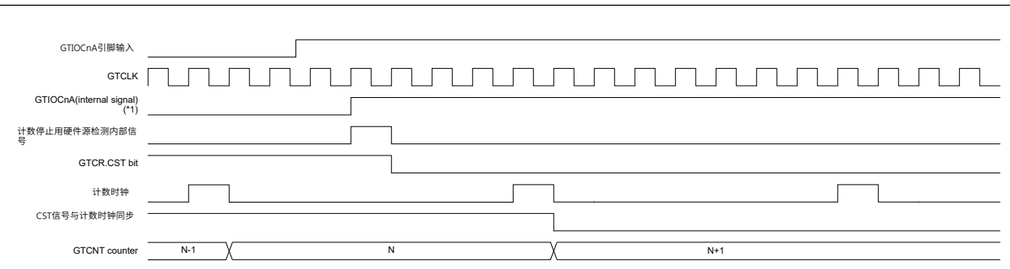
ELC passes the event signal output from GPT320 without delay to GPT321.



Note: POEG clock: PCLKB
注1.GTETRGA内部信号反映了当POEG中GTETRGA引脚的数字噪声滤波器未使用时输入到GPT的信号

Figure 21.92 响应GTETRGA引脚上的输入上升沿停止计数的操作时序示例

图21.93显示了响应于输入的上升沿停止计数的操作时序示例
GTIOCnA pin.



注1.这是不使用数字噪声滤波器时的情况。

Figure 21.93 响应GTIOCnA引脚上的输入上升沿停止计数的操作时序示例

图21.94显示了响应来自ELC_GPTA的事件输入而停止计数的操作时序示例。

这是GPT321.GTCNT计数器响应信号停止计数的操作示例。与GPT320.GTCCRA寄存器比较匹配后，向ELC输出一个事件信号。这被ELC选作ELC_GPTA输出到GPT321的触发器。

ELC将GPT320输出的事件信号无延迟地传递给GPT321。

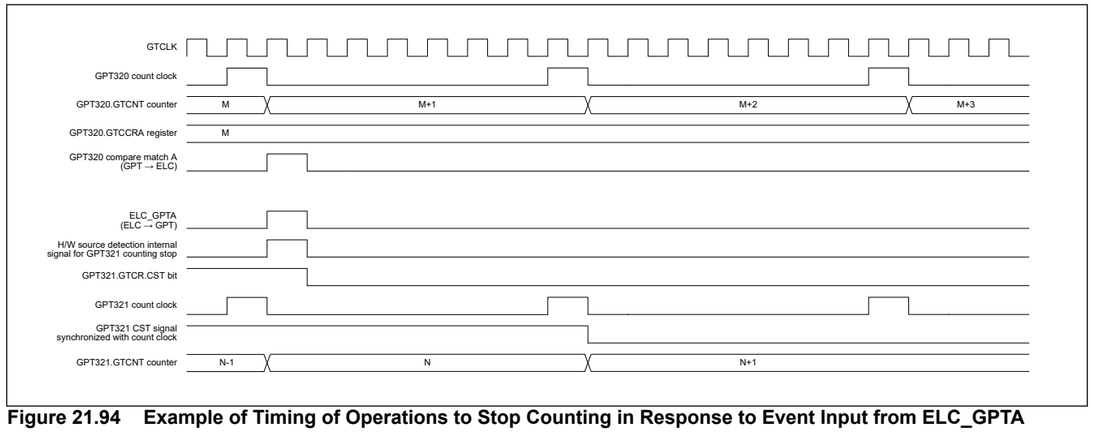


Figure 21.94 Example of Timing of Operations to Stop Counting in Response to Event Input from ELC_GPTA

21.3.7.3 Hardware Clear Operation

The GTCNT counter can be cleared by selecting a hardware source using GTCSR. The GPTn_OVF/GPTn_UDF (n = 0 to 9) interrupt (overflow/underflow interrupt) is not generated when the GTCNT counter is cleared by a hardware source or by software.

Figure 21.95 and Figure 21.96 show examples of the GTCNT counter clearing operation by a hardware source. Table 21.48 shows the setting example. In this example, the GTCNT counter starts at the ELC_GPTA input, and the counter stops and clears at the ELC_GPTB input.

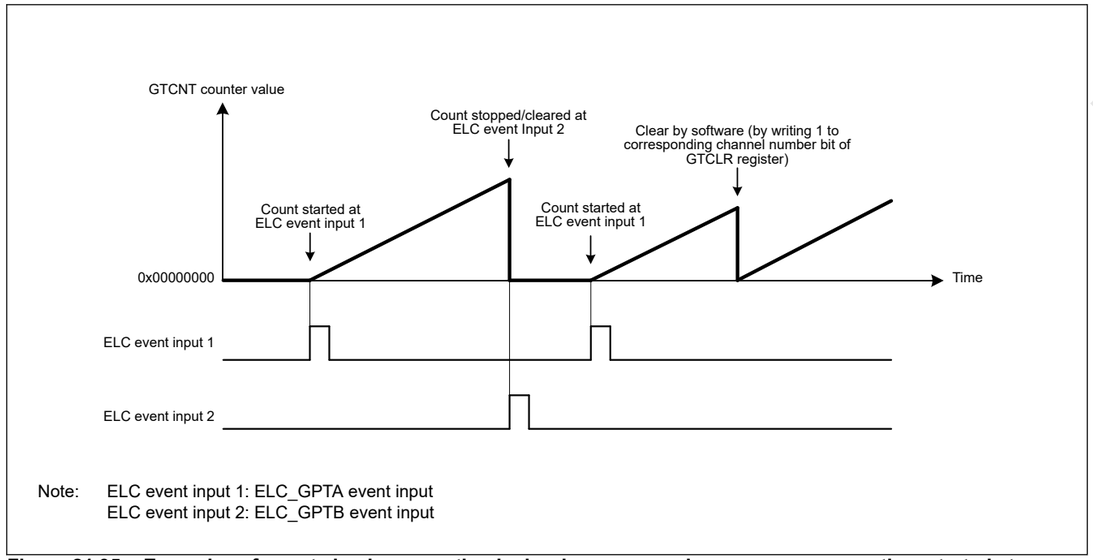


Figure 21.95 Examples of count clearing operation by hardware source in saw wave up-counting, started at ELC_GPTA input, and stopped/cleared at ELC_GPTB input

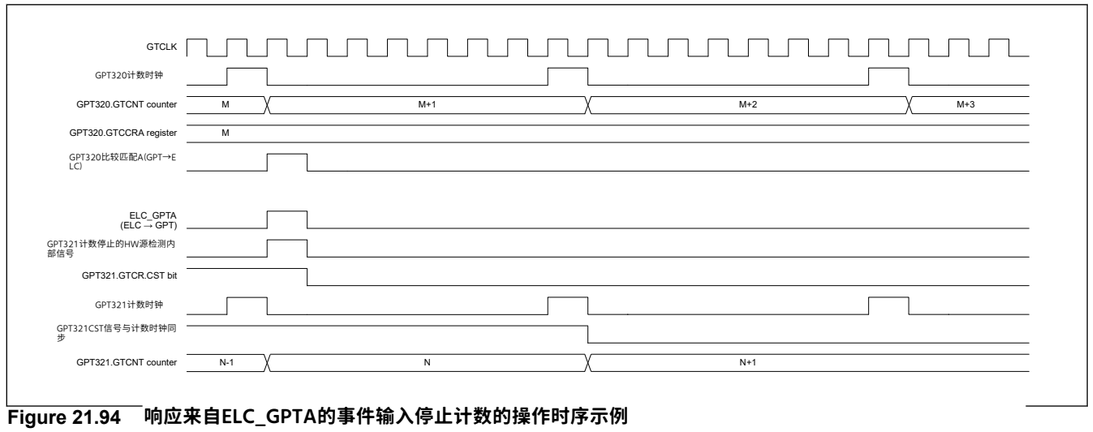


Figure 21.94 响应来自ELC_GPTA的事件输入停止计数的操作时序示例

21.3.7.3 硬件清除操作

GTCNT计数器可以通过使用GTCSR选择硬件源来清除。GPTn_OVFGPTn_UDF(n=0to9)中断（上溢下溢中断）不会在GTCNT计数器被硬件或软件清零时产生。

图21.95和图21.96显示了通过硬件源清除GTCNT计数器操作的示例。设置示例如表21.48所示。在本例中，GTCNT计数器在ELC_GPTA输入处开始，计数器在ELC_GPTB输入处停止并清零。

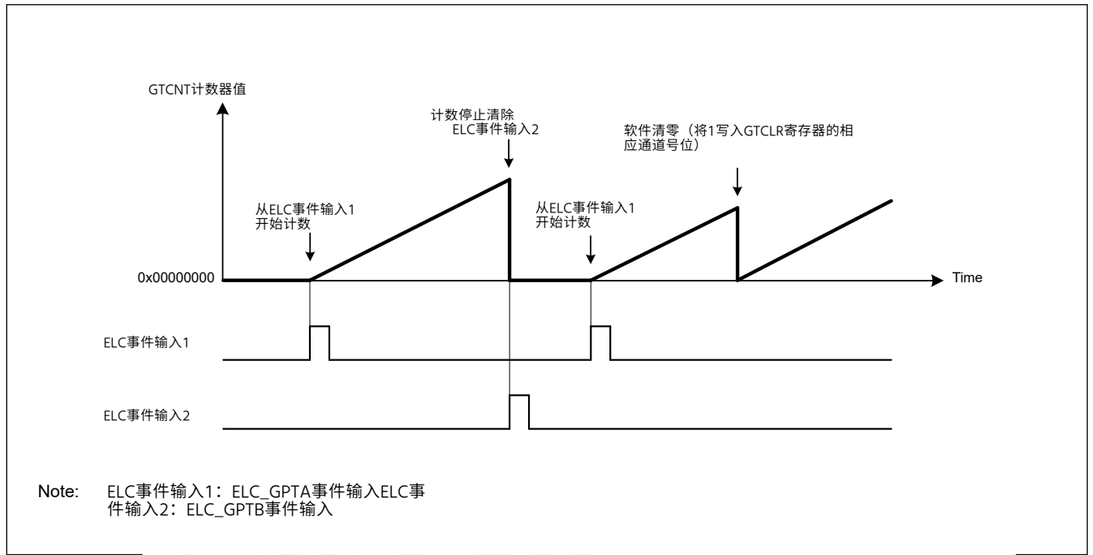
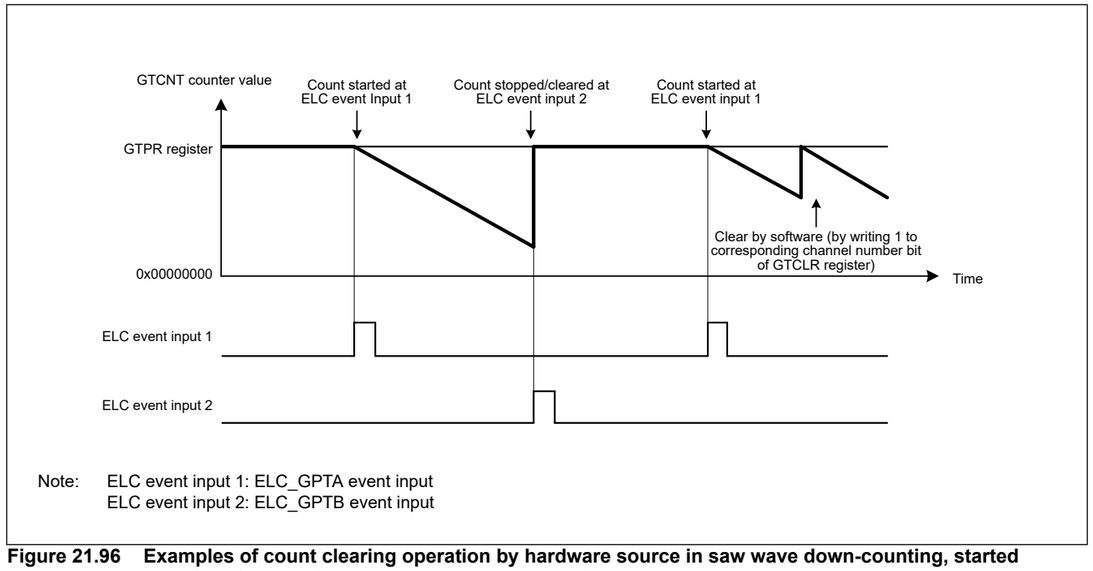


Figure 21.95 锯波递增计数中硬件源的计数清除操作示例，开始于ELC_GPTA输入，并在ELC_GPTB输入处停止清除



Note: ELC event input 1: ELC_GPTA event input
ELC event input 2: ELC_GPTB event input

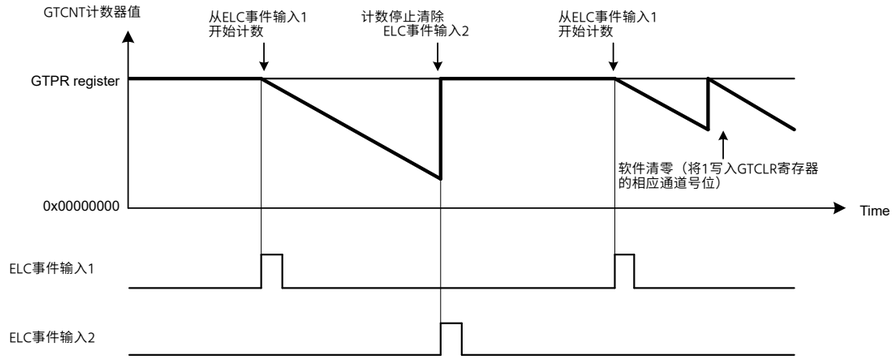
Figure 21.96 Examples of count clearing operation by hardware source in saw wave down-counting, started at ELC_GPTA input, and stopped/cleared at ELC_GPTB input

Table 21.48 Example setting for count clearing operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.95 and Figure 21.96, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.95, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting). In Figure 21.96, after 10b is set in the GTUDDTYC[1:0] bits, 00b is set in the GTUDDTYC[1:0] bits (down-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 21.95, 0x00000000 is set. In Figure 21.96, the GTPR register value is set.
6	Set hardware count start	Select a hardware source for starting count operation in the GTSSR register, and wait for count start by the hardware source. In Figure 21.95 and Figure 21.96, GTSSR.SSELCA = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation in the GTPSR register, and wait for count stop by the hardware source. In Figure 21.95 and Figure 21.96, GTPSR.PSELCB = 1.
8	Set hardware count clear	Select a hardware source for clearing count operation in the GTCSR register, and wait for count clear by the hardware source. In Figure 21.95 and Figure 21.96, GTCSR.CSELCB = 1.
9	Set hardware source operation	Set operation of the hardware source selected in the GTSSR register, GTPSR register or GTCSR register and start, stop or clear counting. In Figure 21.95 and Figure 21.96, the ELC_GPTA input and ELC_GPTB input are set.

The GPTn_OVF/GPTn_UDF (n = 0 to 9) interrupt (overflow/underflow interrupt) is not generated when the counter is cleared by a hardware source or by software.

Figure 21.97 shows the relationship between the counter clearing by a hardware source and the GPTn_OVF (n = 0 to 9) interrupt.



Note: ELC事件输入1：ELC_GPTA事件输入ELC事件输入2：ELC_GPTB事件输入

Figure 21.96 锯波递减计数中硬件源的计数清除操作示例，从ELC_GPTA输入开始，在ELC_GPTB输入停止清除

Table 21.48 通过硬件源进行计数清除操作的示例设置

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.95和图21.96中，设置了000b或0000b（锯齿波PWM模式1）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.95中，在GTUDDTYC[1:0]位中设置11b后，在GTUDDTYC[1:0]位中设置01b（向上计数）。 在图21.96中，在GTUDDTYC[1:0]位中设置10b后，在GTUDDTYC[1:0]位中设置00b（向下计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	在GTPR寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图21.95中，设置了0x00000000。在图21.96中，设置了GTPR寄存器的值。
6	设置硬件计数开始	在GTSSR寄存器中选择开始计数操作的硬件源，等待硬件源开始计数。在图21.95和图21.96中，GTSSR.SSELCA=1。
7	设置硬件计数停止	在GTPSR寄存器中选择一个停止计数操作的硬件源，并等待硬件源停止计数。在图21.95和图21.96中，GTPSR.PSELCB=1。
8	设置硬件计数清除	在GTCSR寄存器中选择清除计数操作的硬件源，等待硬件源清除计数。在图21.95和图21.96中，GTCSR.CSELCB=1。
9	设置硬件源操作	设置在GTSSR寄存器、GTPSR寄存器或GTCSR寄存器中选择的硬件源的操作以及开始、停止或清除计数。在图21.95和图21.96中，设置了ELC_GPTA输入和ELC_GPTB输入。

GPTn_OVFGPTn_UDF（n=0到9）中断（溢出下溢中断）不会在计数器被硬件源或软件清零时产生。

图21.97显示了通过硬件源清除计数器和GPTn_OVF（n=0到9）中断之间的关系。

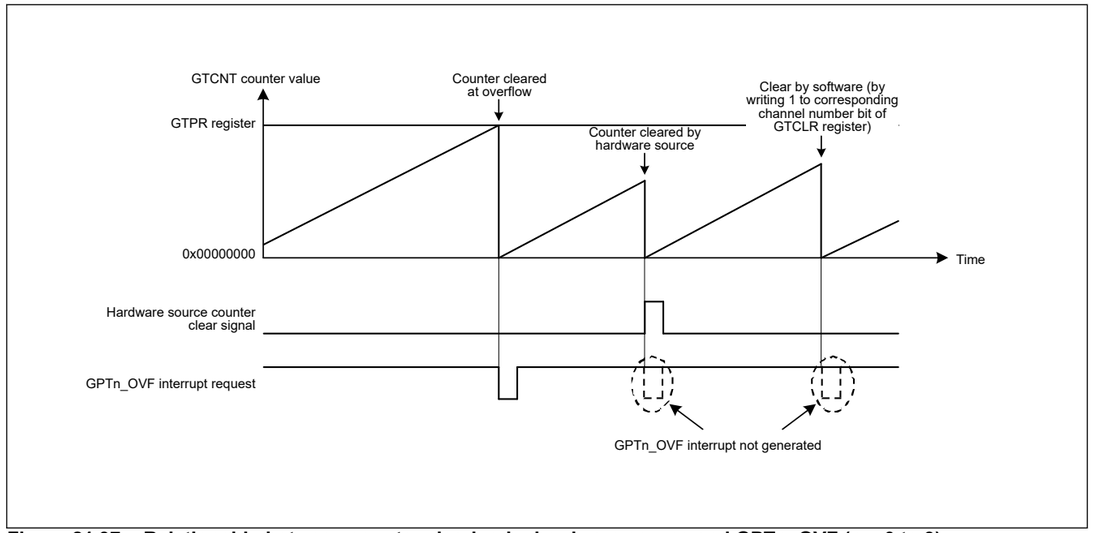
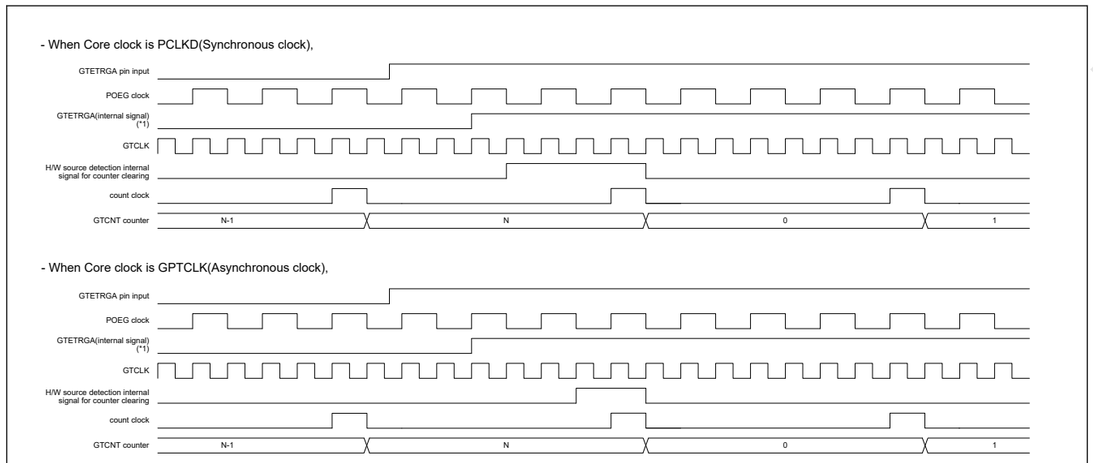


Figure 21.97 Relationship between counter clearing by hardware source and GPTn_OVF (n = 0 to 9) interrupt

Figure 21.98 shows an example of the timing of operations to clear the counter in response to a rising edge of the input on the GTETRGA pin when a clock signal produced by frequency-dividing the GTCLK signal is used as the counter clock for the GTCNT counter.

The GTCNT counter is cleared when counting is in progress after the GPT32 has detected the internal clearing signal.



Note: POEG clock: PCLKB
Note 1. The GTETRGA internal signal reflects the signal being input to GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use.

Figure 21.98 Examples of the Timing of Operations for Counter Clearing in Response to a Rising Edge of the Input on the GTETRGA Pin (During the Counting of Cycles of Clock Signal Produced by Dividing the GTCLK Frequency)

Figure 21.99 shows an example of the timing of operations to clear the counter in response to a rising edge of the input on the GTIOCnA pin when a clock signal produced by frequency-dividing the GTCLK signal is used as the counter clock for the GTCNT counter.

The GTCNT counter is cleared when counting is in progress after the GPT32 has detected the internal clearing signal.

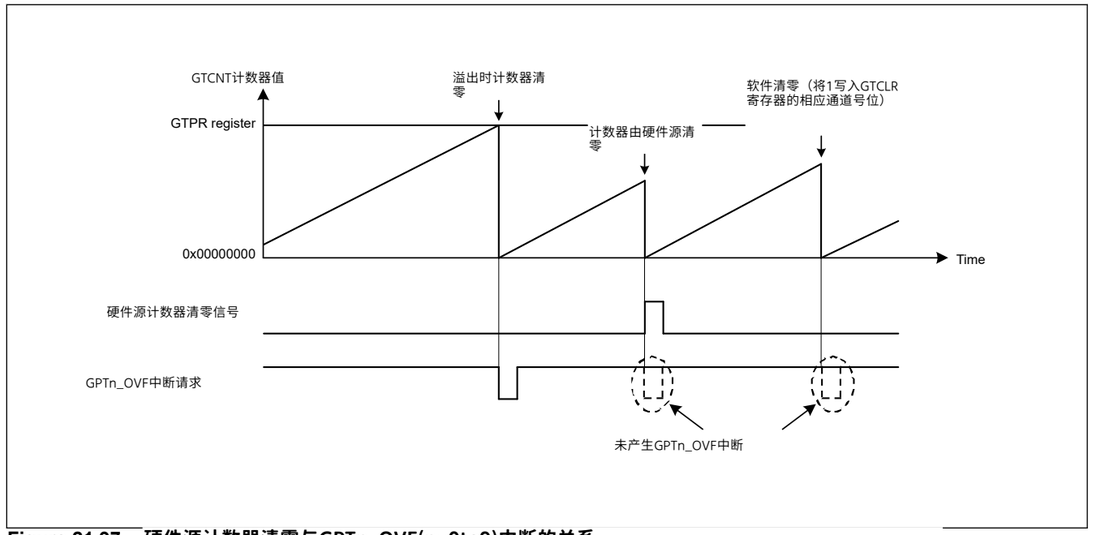
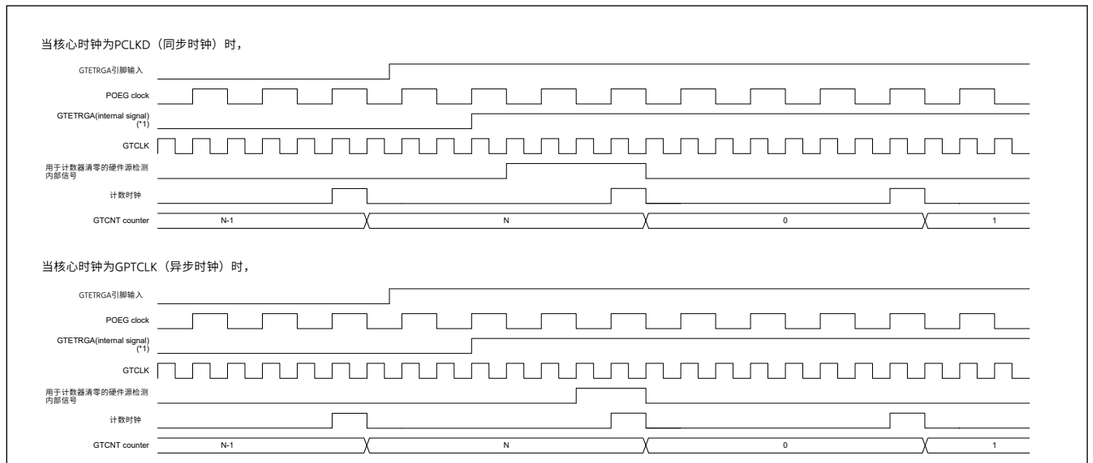


Figure 21.97 硬件源计数器清零与GPTn_OVF(n=0to9)中断的关系

图21.98显示了当通过对GTCLK信号进行分频产生的时钟信号用作GTCNT计数器的计数器时钟时，响应GTETRGA引脚上输入的上升沿清除计数器的操作时序示例。

GPT32检测到内部清零信号后，当计数正在进行时，GTCNT计数器被清零。

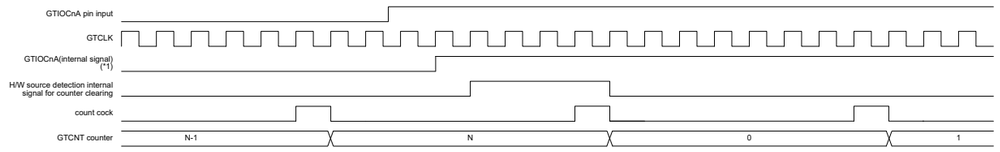


Note: POEG clock: PCLKB
注1.GTETRGA内部信号反映了当POEG中GTETRGA引脚的数字噪声滤波器未使用时输入到GPT的信号。

Figure 21.98 响应GTETRGA引脚上输入的上升沿的计数器清除操作时序示例（在通过划分GTCLK频率产生的时钟信号的周期计数期间）

图21.99显示了当通过对GTCLK信号进行分频产生的时钟信号用作GTCNT计数器的计数器时钟时，响应GTIOCnA引脚上输入的上升沿清除计数器的操作时序示例。

GPT32检测到内部清零信号后，当计数正在进行时，GTCNT计数器被清零。



Note 1. This is the case when the digital noise filter is not in use.

Figure 21.99 Examples of Timing of Operations for Counter Clearing in Response to a Rising Edge of the Input on the GTIOCnA Pin (During the Counting of Cycles of Clock Signal Produced by Dividing the GTCLK Frequency)

Figure 21.100 shows an example of the timing of operations to clear the counter in response to event input from ELC_GPTA when a clock signal produced by frequency-dividing the GTCLK signal is used as the counter clock for the GTCNT counter.

This is an example of operations to clear counting by the GPT321.GTCNT counter in response to a signal. An event signal is output to the ELC after matches in comparison with the GPT320.GTCCRA register. This is selected as a trigger for output to the GPT321 by the ELC as ELC_GPTA.

ELC passes the event signal output from GPT320 without delay to GPT321.

The GTCNT counter is cleared when counting is in progress after the GPT32 has detected the internal clearing signal.

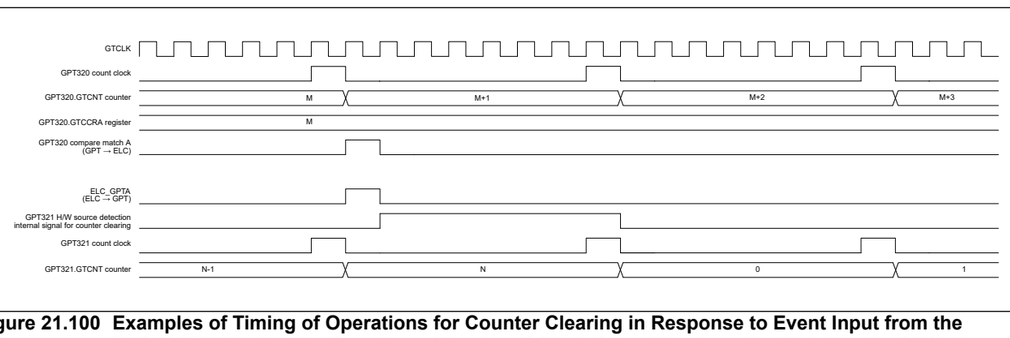
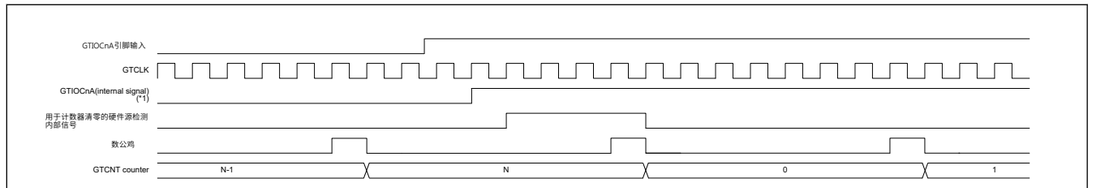


Figure 21.100 Examples of Timing of Operations for Counter Clearing in Response to Event Input from the ELC_GPTA (During the Counting of Cycles of Clock Signal Produced by Dividing the GTCLK Frequency)

Figure 21.101 shows an example of the timing of operations to clear the counter in response to a rising edge of the input on the GTETRGA pin input when counting is triggered by a hardware source.

The GTCNT counter is cleared in synchronization with GTCLK after the GPT32 has detected the internal clearing signal.



注1.这是不使用数字噪声滤波器时的情况。

Figure 21.99 响应于上升沿的柜台清算操作时间示例 GTIOCnA引脚上的输入（在计数时钟信号周期期间由 划分GTCLK频率）

图21.100显示了清除计数器以响应来自
ELC_GPTA当通过对GTCLK信号进行分频产生的时钟信号用作计数器时钟时
GTCNT counter.

这是通过GPT321.GTCNT计数器响应信号清除计数的操作示例。与GPT320.GTCCRA寄存器比较匹配后，向ELC输出一个事件信号。这被ELC选作ELC_GPTA输出到GPT321的触发器。

ELC将GPT320输出的事件信号无延迟地传递给GPT321。

GPT32检测到内部清零信号后，当计数正在进行时，GTCNT计数器被清零。

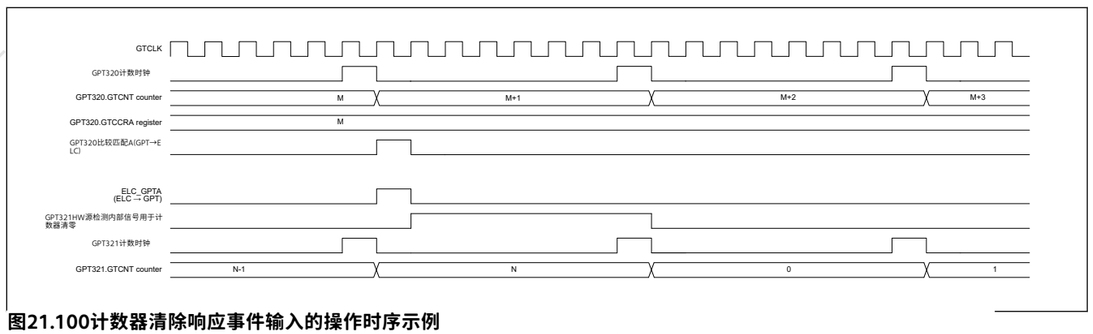
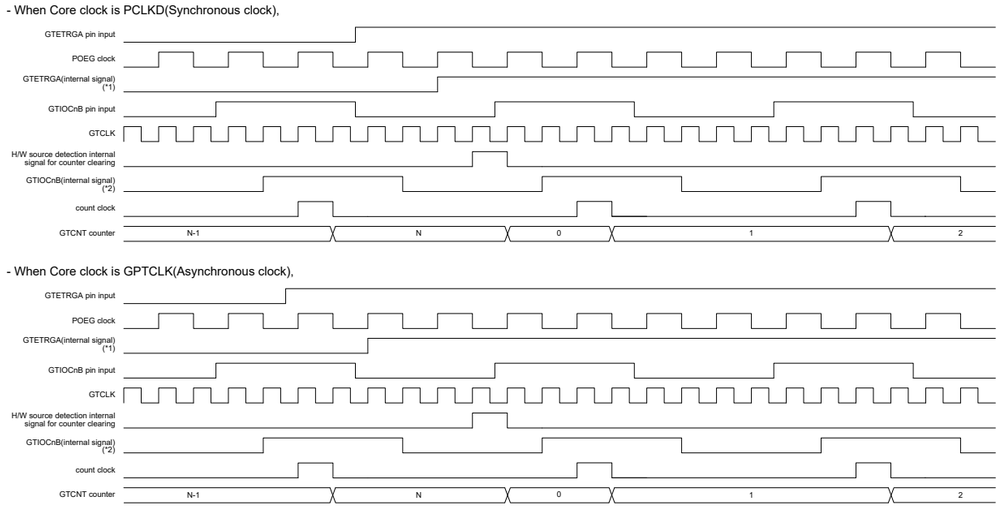


图21.100计数器清除响应事件输入的操作时序示例 ELC_GPTA（在对GTCLK分频产生的时钟信号的周期计数期间 Frequency)

图21.101显示了当计数由硬件源触发时，响应GTETRGA引脚输入的上升沿清除计数器的操作时序示例。

在GPT32检测到内部清零信号后，GTCNT计数器与GTCLK同步清零。

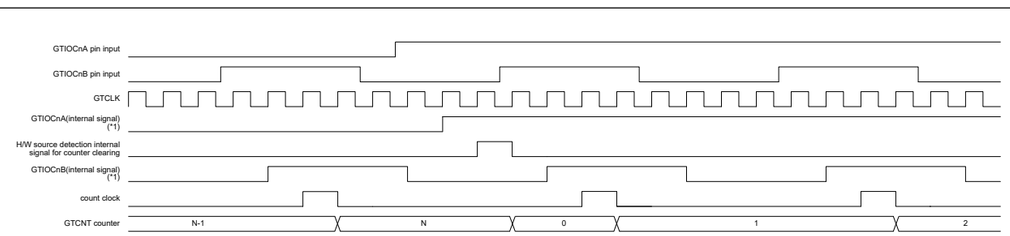


Note: POEG clock: PCLKB
Note 1. The GTETRGA internal signal reflects the signal being input to GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use.
Note 2. This is the case when the digital noise filter is not in use.

Figure 21.101 Examples of the Timing of Operations for Counter Clearing in Response to a Rising Edge of the Input on the GTETRGA Pin (During Counting Triggered by Hardware Source)

Figure 21.102 shows an example of the timing of operations to clear the counter in response to a rising edge of the input on the GTIOCnA pin input when counting is triggered by a hardware source.

The GTCNT counter is cleared in synchronization with GTCLK after the GPT32 has detected the internal clearing signal.



Note 1. This is the case when the digital noise filter is not in use.

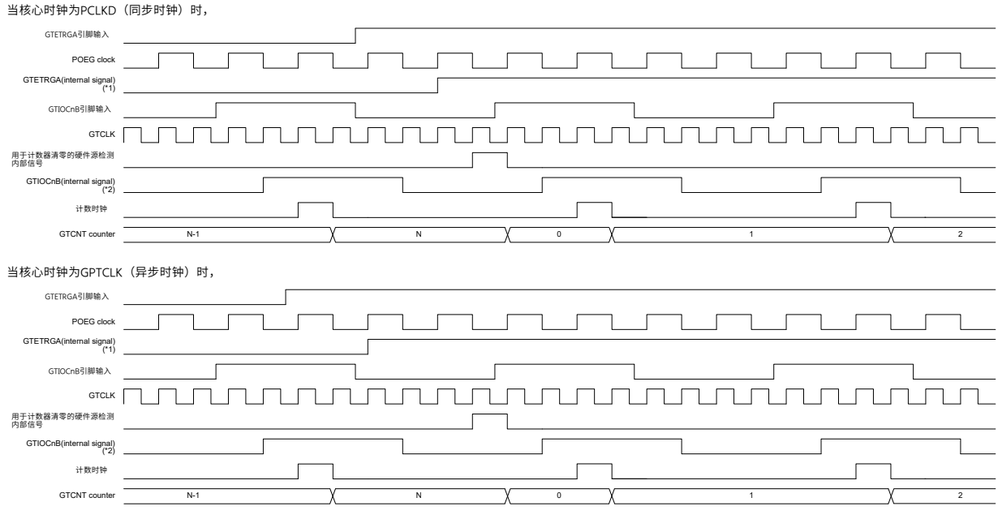
Figure 21.102 Examples of the Timing of Operations for Counter Clearing in Response to a Rising Edge of the Input on the GTIOCnA Pin (During Counting Triggered by Hardware Source)

Figure 21.103 shows an example of the timing of operations for clearing the counter in response to the input of an event signal from the ELC_GPTA when counting is triggered by a hardware source.

This is an example of operations to clear counting by the GPT321.GTCNT counter in response to a signal. An event signal is output to the ELC after matches in comparison with the GPT320.GTCCRA register. This is selected as a trigger for output to the GPT321 by the ELC as ELC_GPTA.

ELC passes the event signal output from GPT320 without delay to GPT321.

The GTCNT counter is cleared in synchronization with GTCLK after the GPT32 has detected the internal clearing signal.



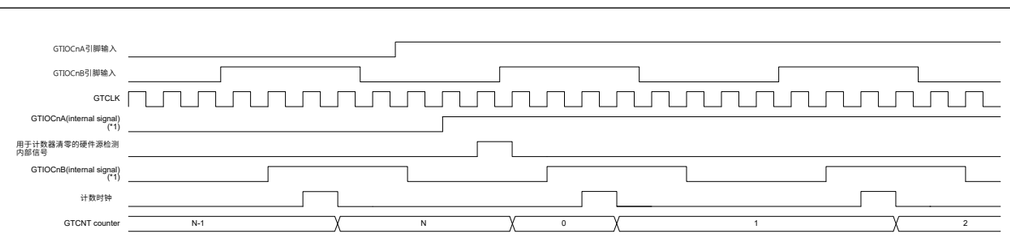
Note: POEG clock: PCLKB
注1.GTETRGA内部信号反映了当POEG中GTETRGA引脚的数字噪声滤波器未使用时输入到GPT的信号。

注2.这是不使用数字噪声滤波器时的情况。

图21.101响应GTETRGA引脚输入上升沿的计数器清零操作时序示例（在硬件源触发的计数期间）

图21.102显示了当计数由硬件源触发时，清除计数器以响应GTIOCnA引脚输入的上升沿的操作时序示例。

在GPT32检测到内部清零信号后，GTCNT计数器与GTCLK同步清零。



注1.这是不使用数字噪声滤波器时的情况。

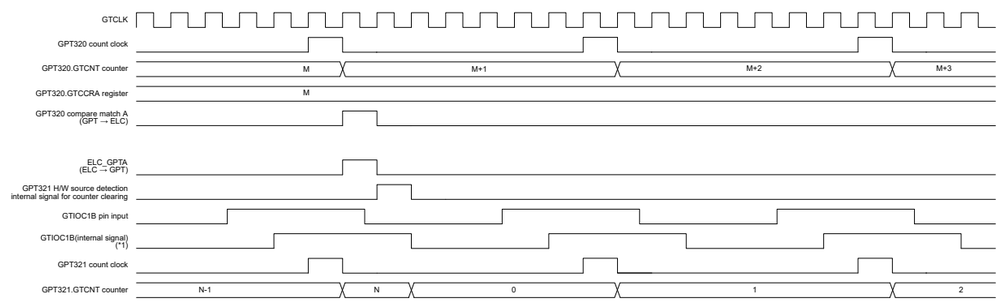
图21.102响应GTIOCnA引脚上的输入上升沿清除计数器的操作时序示例（在硬件源触发的计数期间）

图21.103显示了在硬件源触发计数时，响应来自ELC_GPTA的事件信号输入而清除计数器的操作时序示例。

这是通过GPT321.GTCNT计数器响应信号清除计数的操作示例。与GPT320.GTCCRA寄存器比较匹配后，向ELC输出一个事件信号。这被ELC选作ELC_GPTA输出到GPT321的触发器。

ELC将GPT320输出的事件信号无延迟地传递给GPT321。

在GPT32检测到内部清零信号后，GTCNT计数器与GTCLK同步清零。



Note 1. This is the case when the digital noise filter is not in use.

Figure 21.103 Examples of the Timing of Operations for Counter Clearing in Response to Event Input from the ELC_GPTA (During Counting Triggered by Hardware Source)

21.3.8 Synchronized Operation

Synchronized operation on channels such as a synchronized start, stop, and clear operation can be performed.

21.3.8.1 Synchronized Operation by Software

The GTCNT counters can be started, stopped, and cleared on multiple channels by setting the associated GTSTR, GTSTP, or GTCLR bits simultaneously to 1.

Count start with a phase difference is possible by setting the initial value in the GTCNT counter and setting the associated GTSTR bits simultaneously to 1.

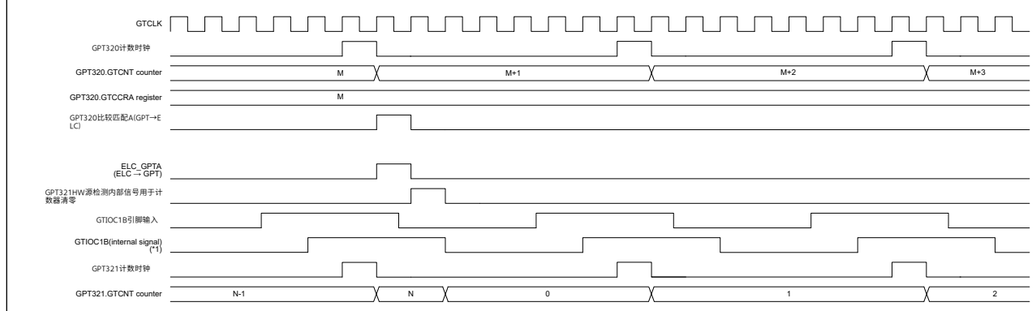
When the GTCNT synchronous set/clear function is enabled on the GTCR.SSCEN bit, the GTCNT registers of the channel set in same group on the GTCR.SSCGRP [1:0] bits can be written at the same time.

The synchronous GTCNT write is invalid in complementary PWM mode.

When either the SSCE bit or the SSCD bit of the GTSECR register is set to 1, the GTCR.SSCEN bits of the channels that selected on the GTSECSR register are set to 0 or 1 and the GTCNT synchronous set/clear function of multiple channels are enabled or disabled at the same time.

Because the clock of count operation is selected by GTCR.TPCS[3:0] bits in respective channels, if the clock period of each channel that performs synchronous operation (count start/stop/clear) is different from others, the synchronous operation timings of every channels are not exact same.

Figure 21.104 shows an example of a simultaneous start, stop, and clear by software. Figure 21.105 shows an example of phase start operation by software. Figure 21.106, Figure 21.107, Figure 21.108 show an example of simultaneous start/stop/clearing with different count period.



注1.这是不使用数字噪声滤波器时的情况。

图21.103响应来自ELC_GPTA的事件输入的计数器清除操作时序示例（在硬件源触发的计数期间）

21.3.8 同步操作

可以对通道进行同步操作，例如同步启动、停止和清除操作。

21.3.8.1 软件同步操作

通过将相关的GTSTR、GTSTP或GTCLR位同时设置为1，可以在多个通道上启动、停止和清除GTCNT计数器。

通过在GTCNT计数器中设置初始值并设置相关的
GTSTR位同时为1。

当GTCR.SSCEN位使能GTCNT同步设置清除功能时，GTCR.SSCGRP[1:0]位上设置在同一组中的通道的GTCNT寄存器可以同时被写入。

同步GTCNT写入在互补PWM模式下无效。

当GTSECR寄存器的SSCE位或SSCD位设置为1时，在GTSECSR寄存器上选择的通道的GTCR.SSCEN位设置为0或1，并启用多通道的GTCNT同步设置清除功能或同时禁用。

由于计数操作的时钟由各个通道的GTCR.TPCS[3:0]位选择，如果执行同步操作（计数开始停止清除）的每个通道的时钟周期与其他通道不同，则每个通道的同步操作时序渠道不完全相同。

图21.104显示了通过软件同时启动、停止和清除的示例。图21.105显示了通过软件进行相位启动操作的示例。图21.106、图21.107、图21.108显示了不同计数周期同时清零的示例。

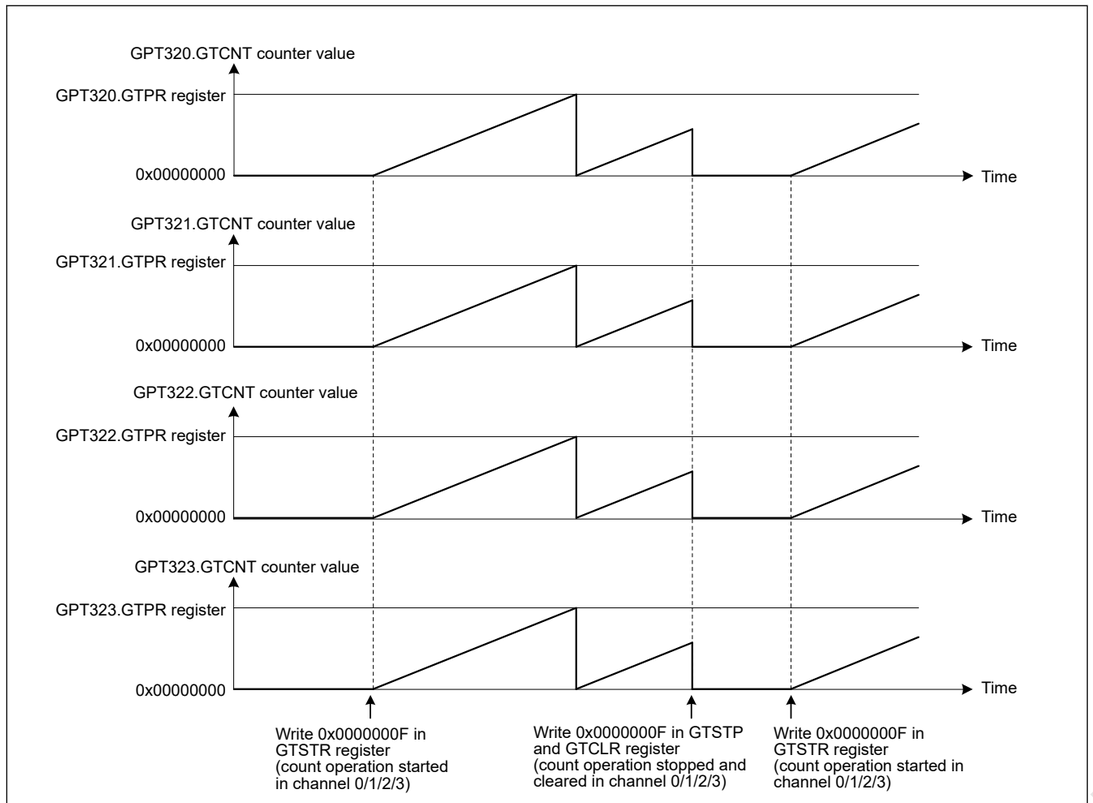


Figure 21.104 Example of a simultaneous start, stop, and clear by software with the same count cycle (GTPR register value)

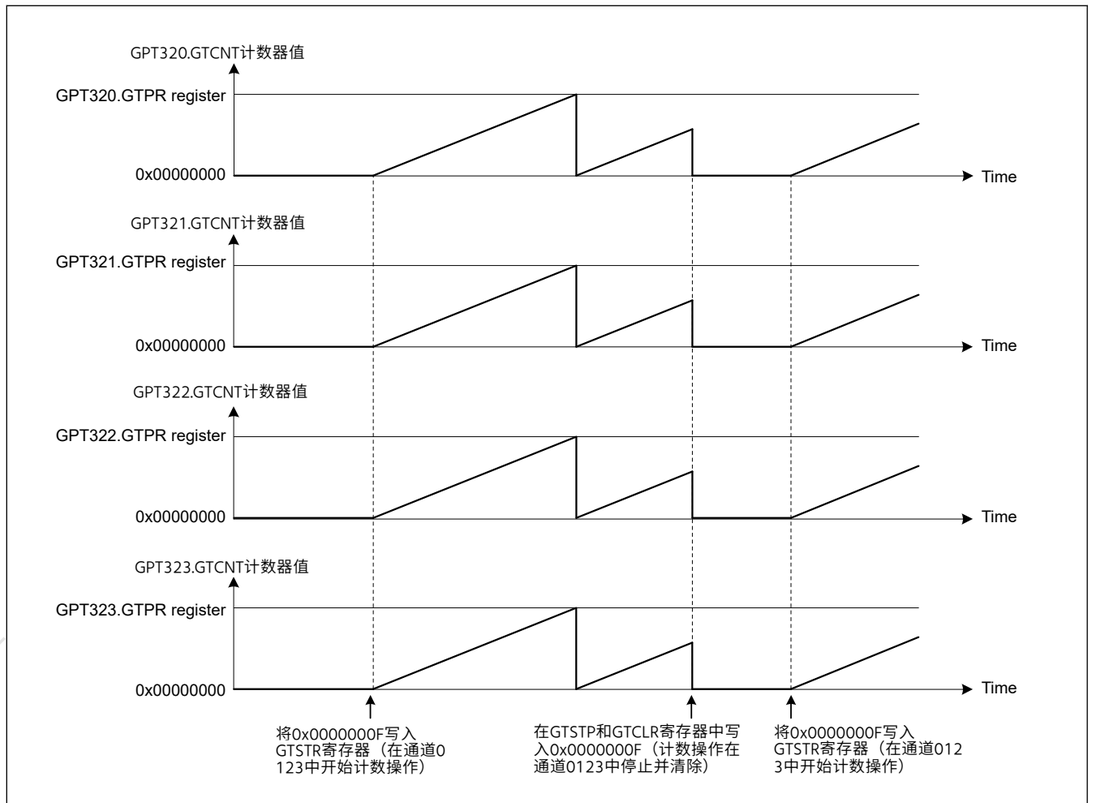


图21.104使用相同计数周期的软件同时启动、停止和清除示例（GTPR寄存器值）

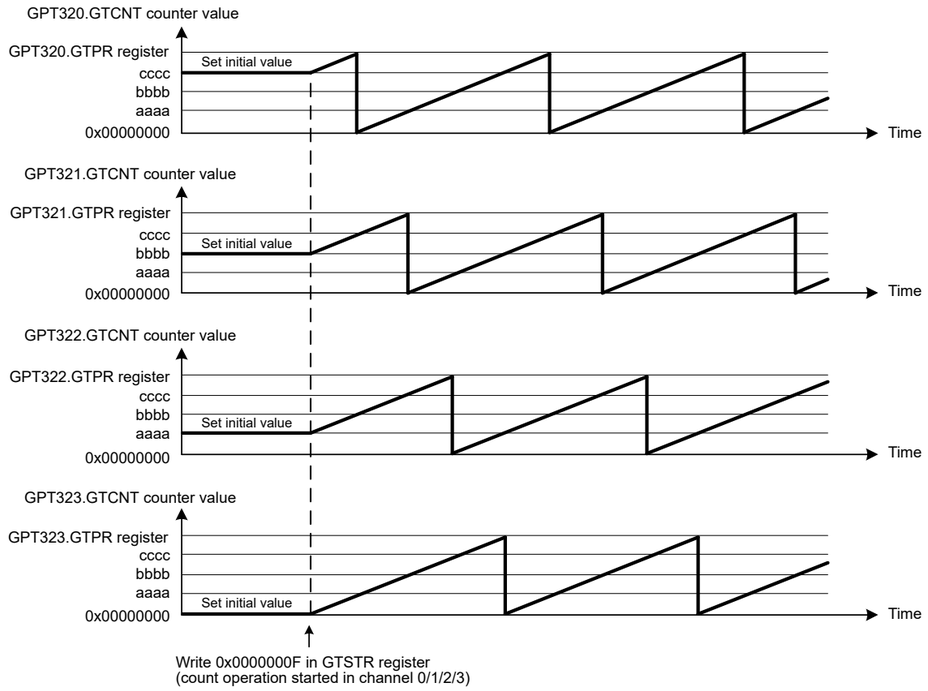


Figure 21.105 Example of software phase start with the same count cycle (GTPR register value)

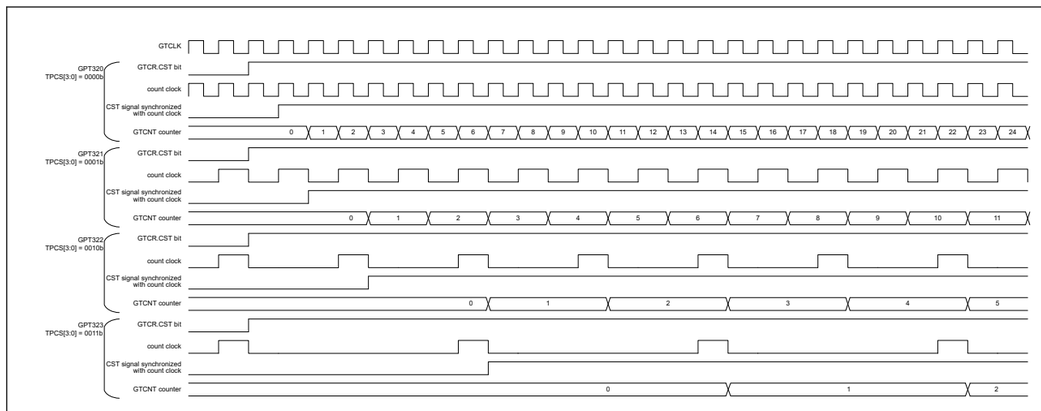


Figure 21.106 Example of Simultaneous Start Operation by Software (with Different Count Period)

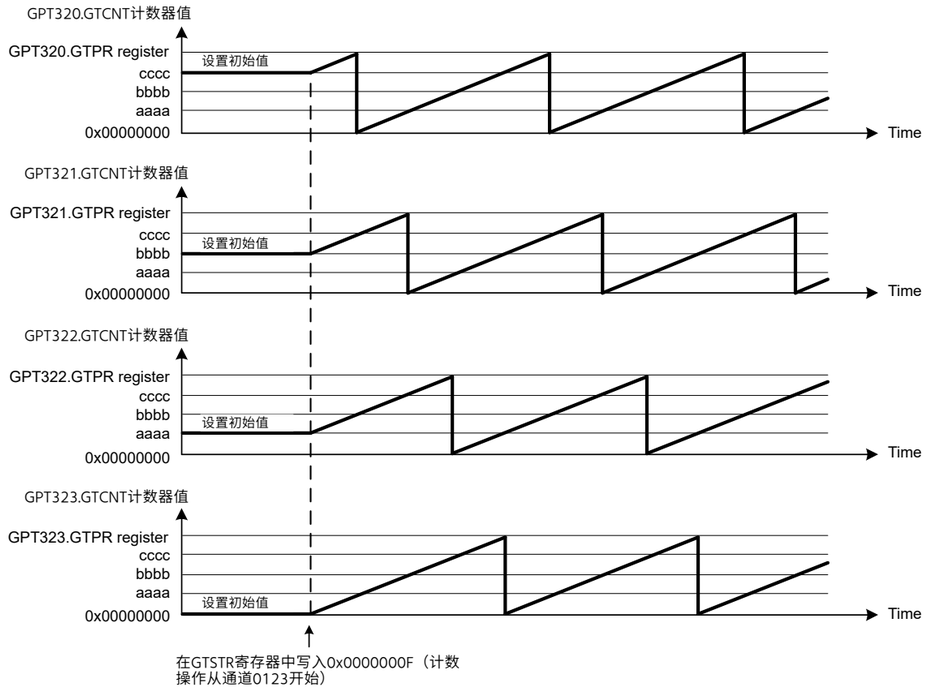


图21.105相同计数周期的软件阶段启动示例（GTPR寄存器值）

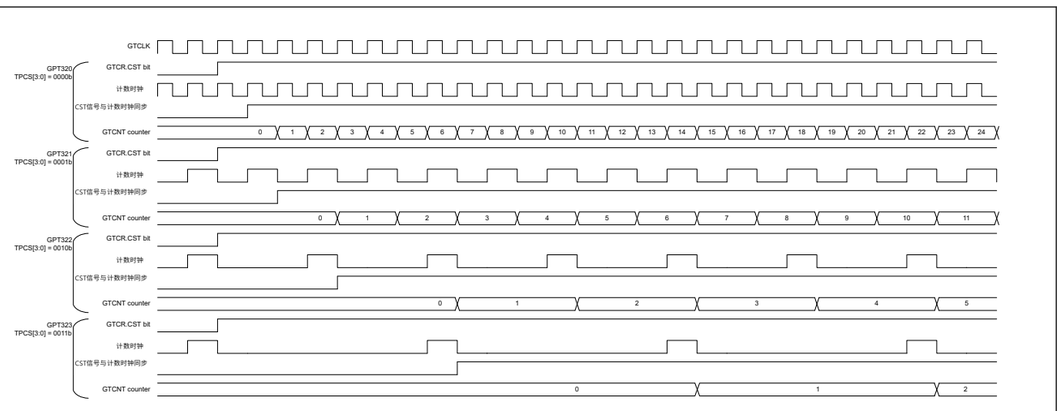


图21.106软件同时启动操作示例（具有不同的计数周期）

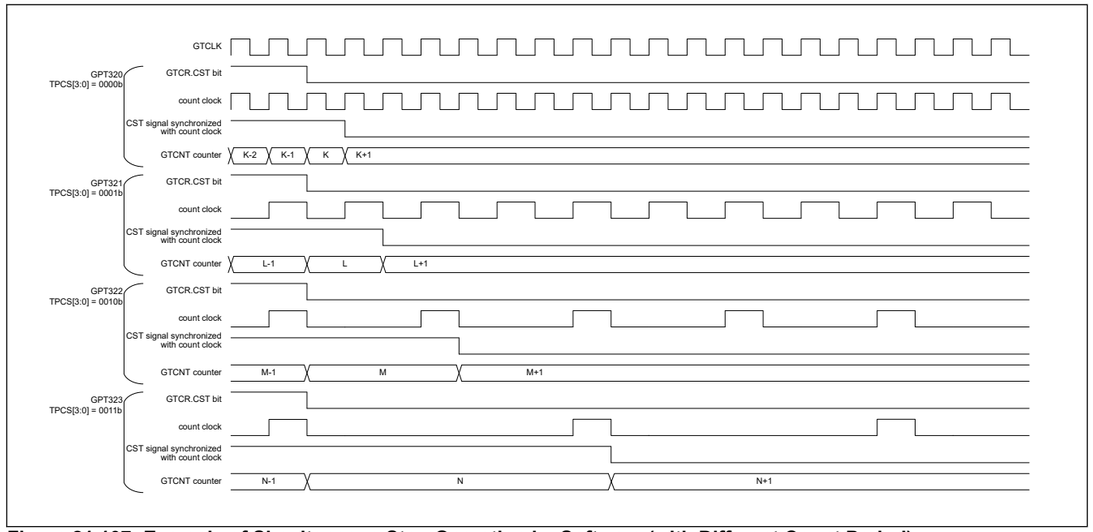


Figure 21.107 Example of Simultaneous Stop Operation by Software (with Different Count Period)

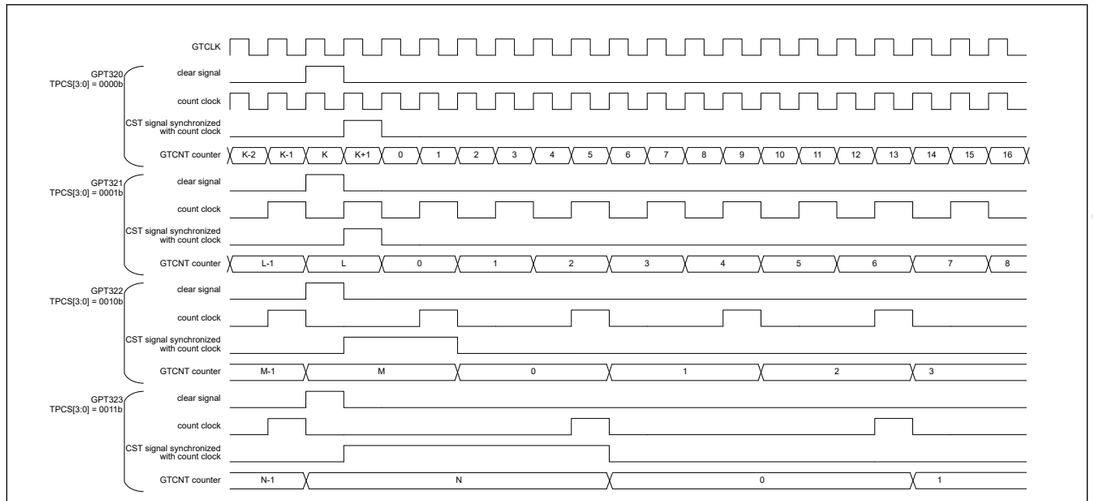


Figure 21.108 Example of Simultaneous Clearing Operation by Software (with Different Count Period)

21.3.8.2 Synchronized Operation by Hardware

The counters for multiple channels can be started, stopped, and cleared simultaneously by the following hardware sources. Hardware sources that can cause a synchronized operation are external trigger input and ELC event input. Synchronized operation through the GTIOCnA and GTIOCnB pin inputs is possible by setting an ELC event due to input capture as a hardware source (n = 0 to 9).

Figure 21.109 shows an example of a simultaneous start, stop, and clear operation by a hardware source. Table 21.49 shows the setting example.

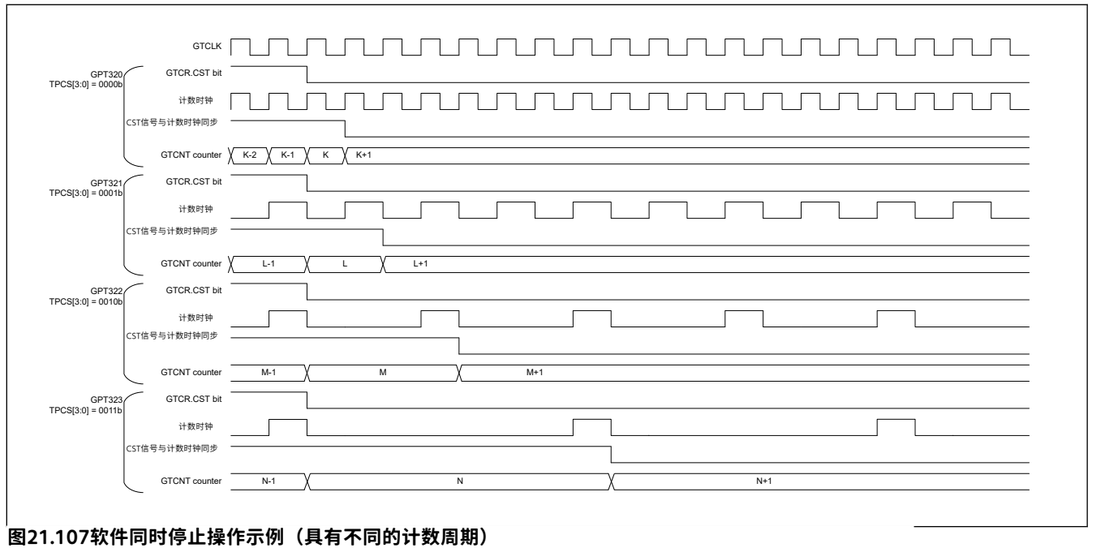


图21.107软件同时停止操作示例（具有不同的计数周期）

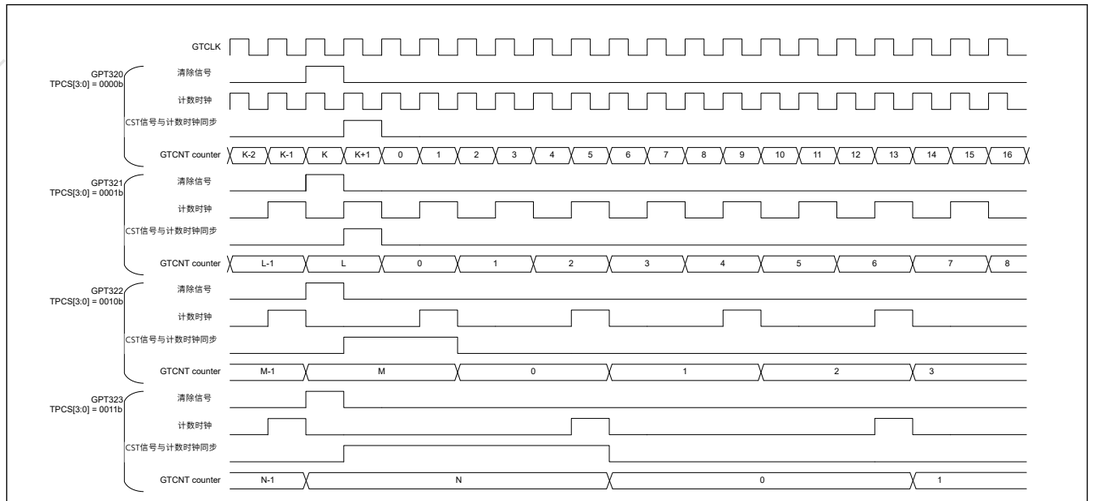
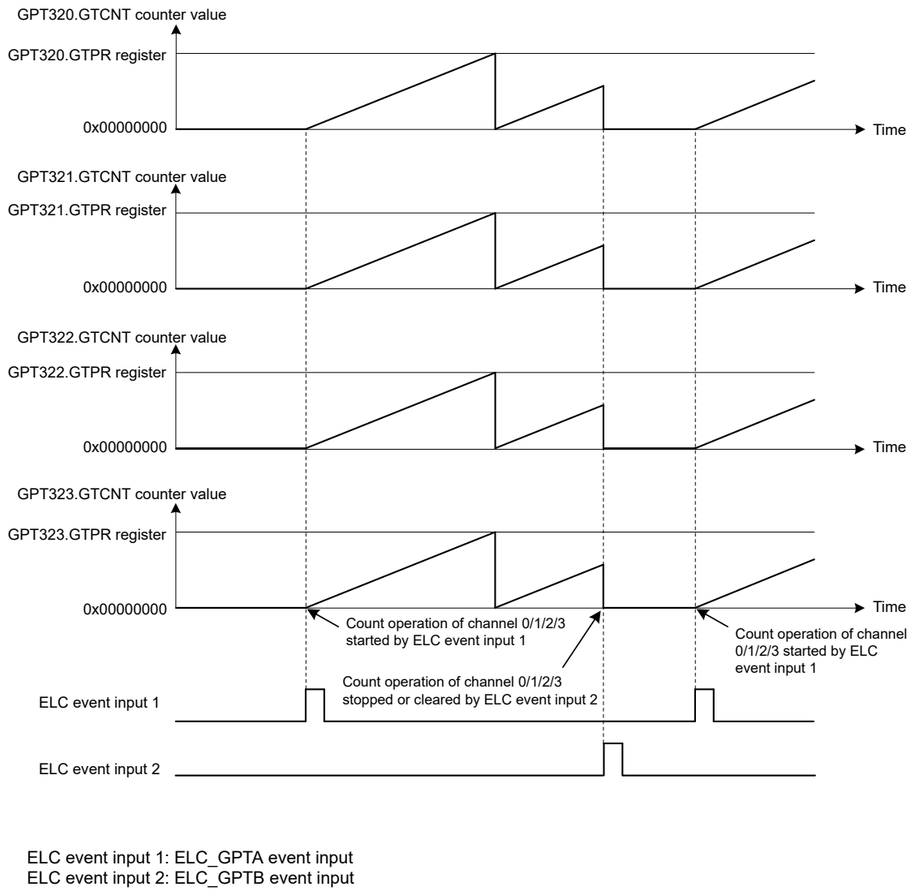


图21.108软件同时清零操作示例（不同计数周期）

21.3.8.2 硬件同步操作

多个通道的计数器可以通过以下硬件源同时启动、停止和清除。
可以导致同步操作的硬件源是外部触发输入和ELC事件输入。通过将输入捕获导致的ELC事件设置为硬件源（n=0到9），可以通过GTIOCnA和GTIOCnB引脚输入进行同步操作。

图21.109显示了一个硬件源同时启动、停止和清除操作的示例。设置示例如表21.49所示。

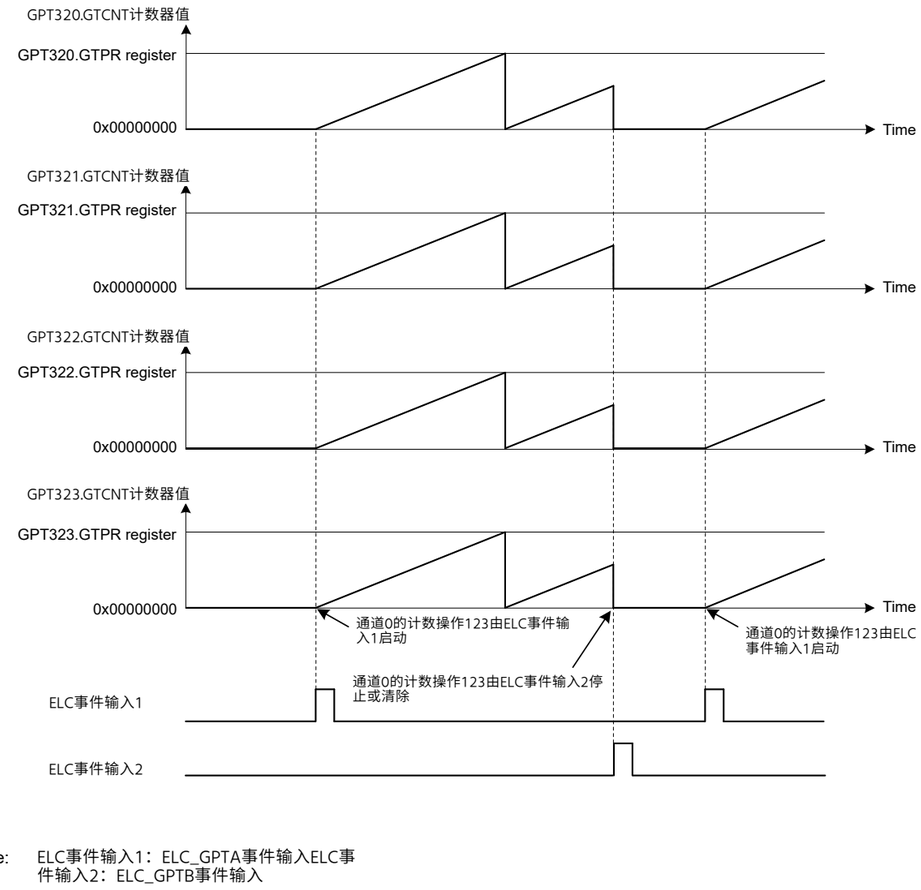


Note: ELC event input 1: ELC_GPTA event input
ELC event input 2: ELC_GPTB event input

Figure 21.109 Example of a simultaneous start, stop, and clear by a hardware source with the same count cycle (GTPR register value)

Table 21.49 Example setting for simultaneous start by a hardware source (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.109, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.109, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 21.109, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation with the GTSSR register, and wait for count start by the hardware source. In Figure 21.109, GTSSR.SSELCA = 1.



Note: ELC事件输入1：ELC_GPTA事件输入ELC事件输入2：ELC_GPTB事件输入

图21.109具有相同计数周期（GTPR寄存器值）的硬件源同时启动、停止和清除的示例

Table 21.49 通过硬件源同时启动的示例设置（2个中的1个）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.109中，设置了000b或0000b（锯齿波PWM模式1）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.109中，在GTUDDTYC[1:0]位中设置了11b之后，在GTUDDTYC[1:0]位中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	在GTPR寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图21.109中，设置了0x00000000。
6	设置硬件计数开始	通过GTSSR寄存器选择开始计数操作的硬件源，并等待硬件源开始计数。在图21.109中，GTSSR.SSELCA=1。

Table 21.49 Example setting for simultaneous start by a hardware source (2 of 2)

No.	Step Name	Description
7	Set hardware count stop	Select a hardware source for stopping count operation with the GTPSR register, and wait for count stop by the hardware source. In Figure 21.109, GTPSR.PSELCB = 1.
8	Set hardware count clear	Select a hardware source for clearing count operation with the GTCSR register, and wait for count clear by the hardware source. In Figure 21.109, GTCSR.CSELCB = 1.
9	Set hardware source operation	Set operation of the hardware source selected in the GTSSR, GTPSR, or GTCSR registers, and start, stop, or clear counting. In Figure 21.109, ELC_GPTA input and ELC_GPTB input are set.

21.3.8.3 Synchronous Clear Operation by Inter Channel Cooperation

The counters of other channels can be cleared at the same time with the counter clear of some channel caused by the compare match, input capture, saw wave up-count overflow, saw wave down-count underflow, and the GTIOCnA / GTIOCnB pin input selected in the GTCSR register.

The counter clear caused by GTCLR register, external trigger input and the ELC input can perform as synchronous clear when the same counter clear factor is set to target channels of synchronous clear. Therefore, these factors are not prepared for the synchronous clear operation by inter channel cooperation.

Set the channel that generates the synchronization clear source and the channel that is synchronized clear in the same synchronous set/clear group with the GTCR.SSCGRP[1:0] bits.

Similar to the synchronous operation in section 21.3.8.1. Synchronized Operation by Software, if the count clock selected by the GTCR.TPCS [3:0] bits is different for each channel, the synchronous clear operation cannot be performed at exact same timing. Similar to the example of simultaneous clearing operation by software in Figure 21.108, if the count clock is different for each channel, the synchronous clear factor is synchronized with the count clock of each channel before counter clearing.

When either the SSCE bit or the SSCD bit of the GTSECR register is set to 1, the GTCR.SSCEN bits of the channels that selected on the GTSECSR register are set to 0 or 1 and the GTCNT synchronous set/clear function of multiple channels are enabled or disabled at the same time.

Figure 21.110 shows an example of synchronous clear operation by inter channel cooperation and Table 21.50 shows an example for setting synchronous clear operation by inter channel cooperation.

Table 21.49 通过硬件源同时启动的示例设置(2of2)

No.	步骤名称	Description
7	设置硬件计数停止	使用GTPSR寄存器选择停止计数操作的硬件源，并等待硬件源停止计数。在图21.109中，GTPSR.PSELCB=1。
8	设置硬件计数清除	通过GTCSR寄存器选择清除计数操作的硬件源，并等待硬件源清除计数。在图21.109中，GTCSR.CSELCB=1。
9	设置硬件源操作	设置在GTSSR、GTPSR或GTCSR寄存器中选择的硬件源的操作，以及开始、停止或清除计数。在图21.109中，设置了ELC_GPTA输入和ELC_GPTB输入。

21.3.8.3 跨渠道合作同步清关

由于比较匹配、输入捕捉、锯齿波向上计数溢出、锯齿波向下计数下溢以及选择的GTIOCnAGTIOCnB引脚输入，其他通道的计数器可以同时清零。GTCSR寄存器。

GTCLR寄存器、外部触发输入和ELC输入引起的计数器清零，当同步清零的目标通道设置相同的清零因子时，可以作为同步清零。因此，这些因素没有为通道间协作的同步清除操作做好准备。

通过GTCR.SSCGRP[1:0]位将产生同步清除源的通道和同步清除的通道设置在同一个同步设置清除组中。

类似于第21.3.8.1节中的同步操作。软件同步操作，如果GTCR.TPCS[3:0]位选择的计数时钟对于每个通道不同，同步清除操作不能在完全相同的时序执行。与图21.108中软件同时清零操作的示例类似，如果每个通道的计数时钟不同，则同步清零因子与计数器清零前的每个通道的计数时钟同步。

当GTSECR寄存器的SSCE位或SSCD位设置为1时，在GTSECSR寄存器上选择的通道的GTCR.SSCEN位设置为0或1，并启用多通道的GTCNT同步设置清除功能或同时禁用。

图21.110显示了通道间协作的同步清除操作示例，表21.50显示了通道间协作设置同步清除操作的示例。

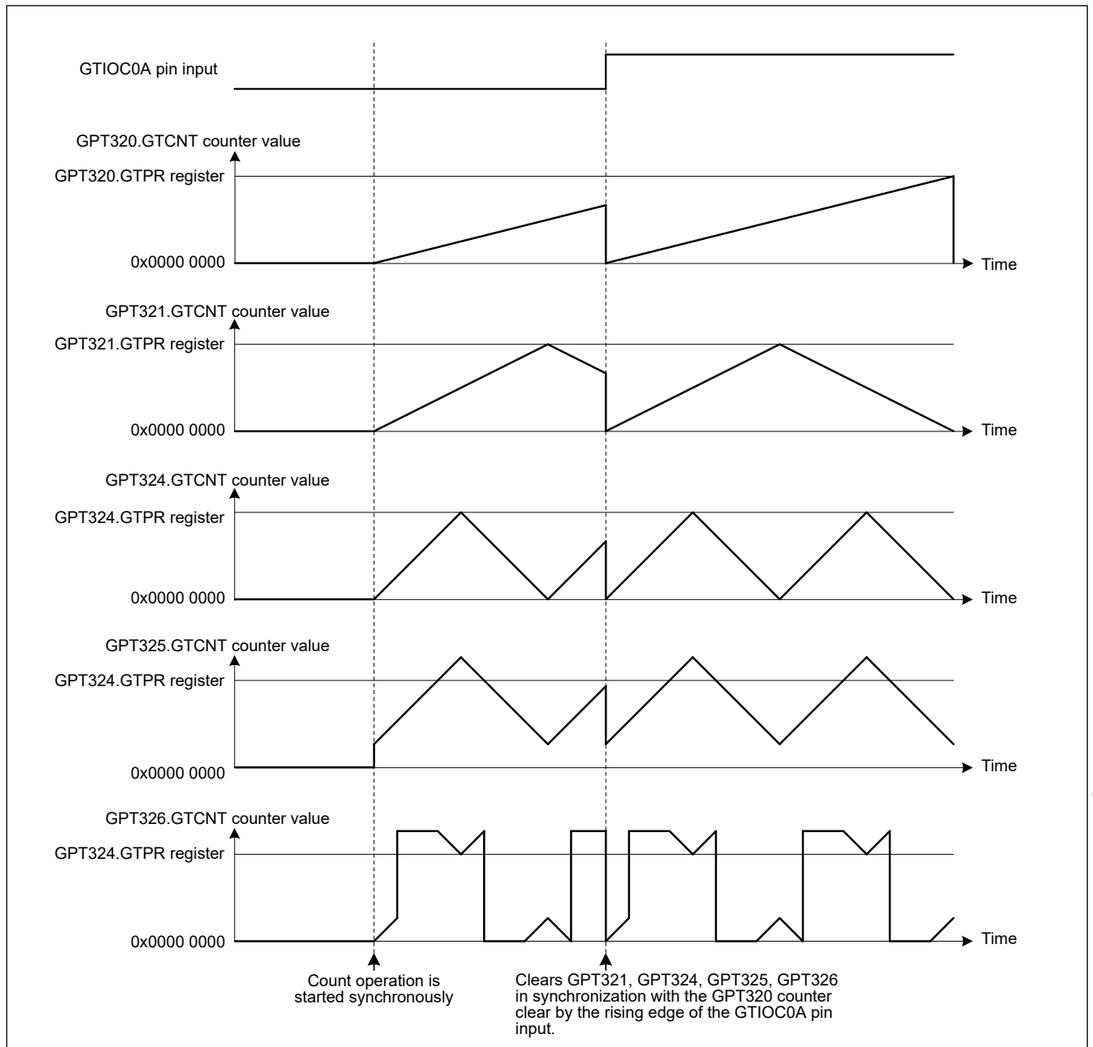


Figure 21.110 Example of Synchronous Clear Operation by Inter Channel Cooperation (GPT320 is saw-wave and counter is cleared by the rising edge of the GTIOC0A, GPT321 is triangle wave, GPT324,5,6 are complementary PWM mode. GPT320,1,4,5,6 are the same synchronous set/clear group)

Table 21.50 Example for Setting Synchronous Clear Operation by Inter Channel Cooperation (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0] or GTCR.MD[3:0]. In Figure 21.110, 000b (saw-wave PWM mode 1) is set to GPT320. 100b (triangle-wave PWM mode 1) is set to GPT321. 1100b (complementary PWM mode 1) is set to GPT324(GPT325,6).
2	Set count direction	Select the count direction (up or down) with GTUDDTYC. In Figure 21.110, for GPT320 and GPT321, lower 2 bits of GTUDDTYC is set to 11b, and then lower 2 bits of GTUDDTYC is set to 01b (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits of the corresponding channel.
4	Set cycle	Set the cycle in GTPR of the corresponding channel. When complementary PWM mode, set the cycle in GTPR of the master channel.

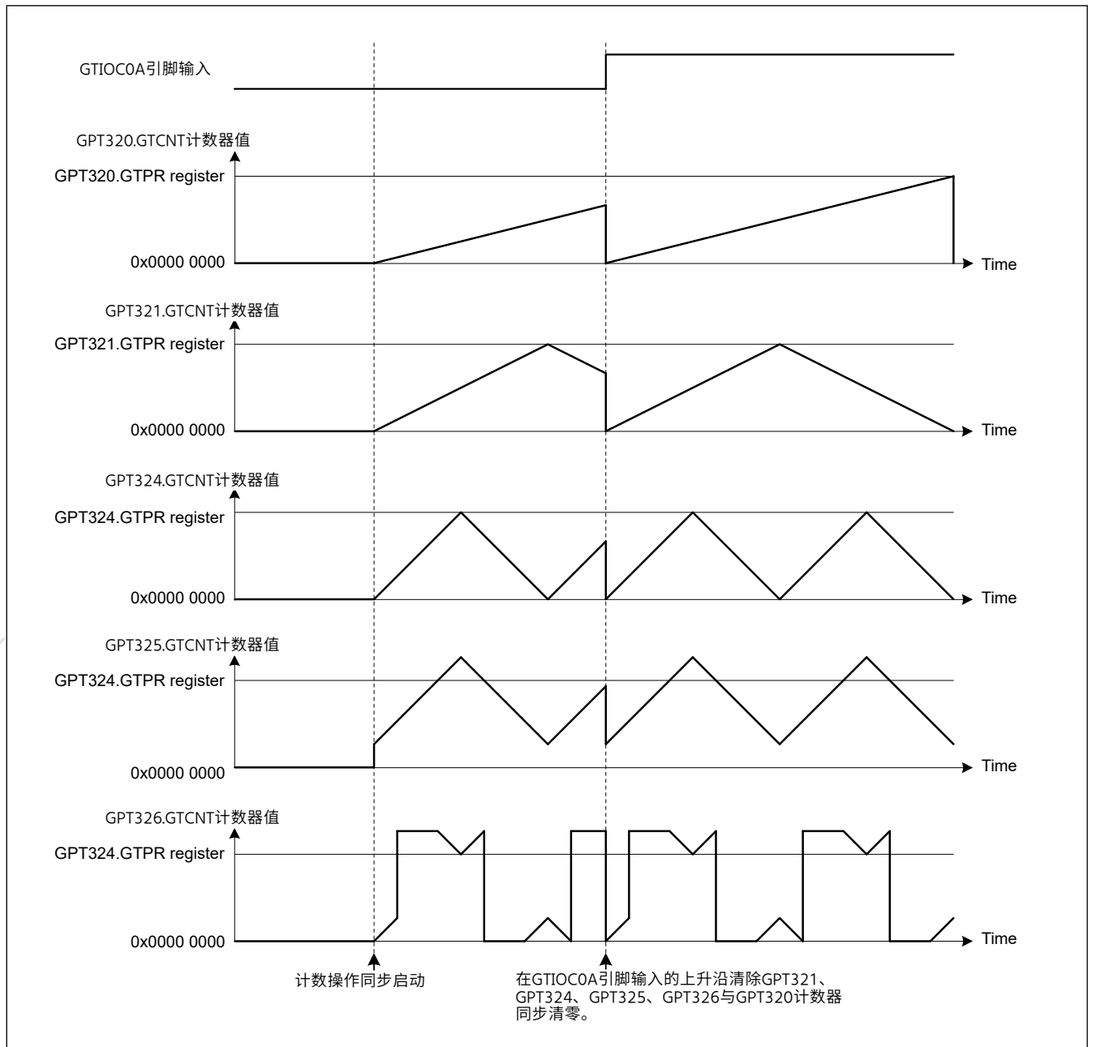


图21.110通道间协作同步清零操作示例（GPT320为锯齿波，计数器由GTIOC0A的上升沿清零，GPT321为三角波，GPT324 5 6为互补PWM模式。GPT320 1 4 5 6是同一个同步组清组）

Table 21.50 通过通道间协作设置同步清除操作的示例(1of2)

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]或GTCR.MD[3:0]设置操作模式。 在图21.110中，000b（锯齿波PWM模式1）设置为GPT320。100b（三角波PWM模式1）设置为GPT321。1100b（互补PWM模式1）设置为GPT324(GPT325 6)。
2	设置计数方向	使用GTUDDTYC选择计数方向（向上或向下）。 在图21.110中，对于GPT320和GPT321，将GTUDDTYC的低2位设置为11b，然后将GTUDDTYC的低2位设置为01b（向上计数）。
3	选择计数时钟	用相应通道的GTCR.TPCS[3:0]位选择计数时钟。
4	设置周期	在相应通道的GTPR中设置循环。 互补PWM模式时，在主通道的GTPR中设置周期。

Table 21.50 Example for Setting Synchronous Clear Operation by Inter Channel Cooperation (2 of 2)

No.	Step Name	Description
5	Set initial value for counter	Set the initial value in the GTCNT counter of the corresponding channel.
6	Inter channel cooperation synchronous clear setting (Source channel)	Set the GTINTAD register and GTCR.SCGTIOC bit in the source channel of inter channel cooperation synchronous clear to enable synchronous clear. When complementary PWM mode, set GTINTAD of the master channel. In Figure 21.110, GPT320.GTCR.SCGTIOC bit is 1.
7	Inter channel cooperation synchronous clear setting (Cleared channels)	Set GTCSR.CSCMSC[2:0] bits in the cleared channels of inter channel cooperation synchronous clear to select the counter clear by synchronous counter clearing group. When complementary PWM mode, set GTCSR of the master channel. In Figure 21.110, GTCSR.CSCMSC[2:0] bits of GPT321 and GPT324 is 111b.
8	Set group of inter channel cooperation synchronous clear	Set the same value to GTCR.SSCGRP[1:0] bits in the source channel and cleared channels of inter channel cooperation synchronous clear and set them in the same synchronous set/clear group. When complementary PWM mode, set GTCR of the master channel.
9	Enable inter channel cooperation synchronous clear	Set GTCR.SSCEN bits in the source channel and cleared channels of inter channel cooperation synchronous clear to enable synchronous clear.

21.3.9 PWM Output Operation Examples

(1) Synchronized PWM output

The GPT outputs 10 × 2 phases of linked PWM waveforms for a maximum of GPT × 10 channels.

Figure 21.111 shows an example in which four channels perform synchronized operation in saw-wave PWM mode 1 and eight phases of PWM waveforms are output. The GTIOCnA is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCnB is set so that it outputs low as the initial value, high at a GTCCRB compare match, and low at the cycle end.

Table 21.50 通过通道间协作设置同步清除操作的示例(2of2)

No.	步骤名称	Description
5	设置计数器的初始值	在相应通道的GTCNT计数器中设置初始值。
6	通道间协作同步清除设置（源通道）	设置通道间协作同步清除源通道中的GTINTAD寄存器和GTCR.SCGTIOC位，使能同步清除。 在互补PWM模式下，设置主通道的GTINTAD。 在图21.110中，GPT320.GTCR.SCGTIOC位为1。
7	通道间协作同步清除设置（已清除通道）	设置通道间协作同步清除清除通道中的GTCSR.CSCMSC[2:0]位，选择同步计数器清除组的计数器清除。互补PWM模式时，设置主通道的GTCSR。 在图21.110中，GPT321和GPT324的GTCSR.CSCMSC[2:0]位为111b。
8	设置组间通道协作同步清零	将源通道和通道间协作同步清除的清除通道中的GTCR.SSCGRP[1:0]位设置为相同的值，并将它们设置在同一个同步设置清除组中。互补PWM模式时，设置主通道的GTCR。
9	启用通道间协作同步清除	设置源通道中的GTCR.SSCEN位和通道间协作同步清除的清除通道，使能同步清除。

21.3.9 PWM输出操作示例

(1) 同步PWM输出

GPT为最多GPT×10个通道输出10×2相链接的PWM波形。

图21.111显示了一个示例，其中四个通道在锯齿波PWM模式1下执行同步操作并输出8相PWM波形。GTIOCnA设置为输出低作为初始值，在GTCCRA比较匹配时输出高，在循环结束时输出低。GTIOCnB设置为输出低作为初始值，高

GTCCRB比较匹配，并在循环结束时为低。

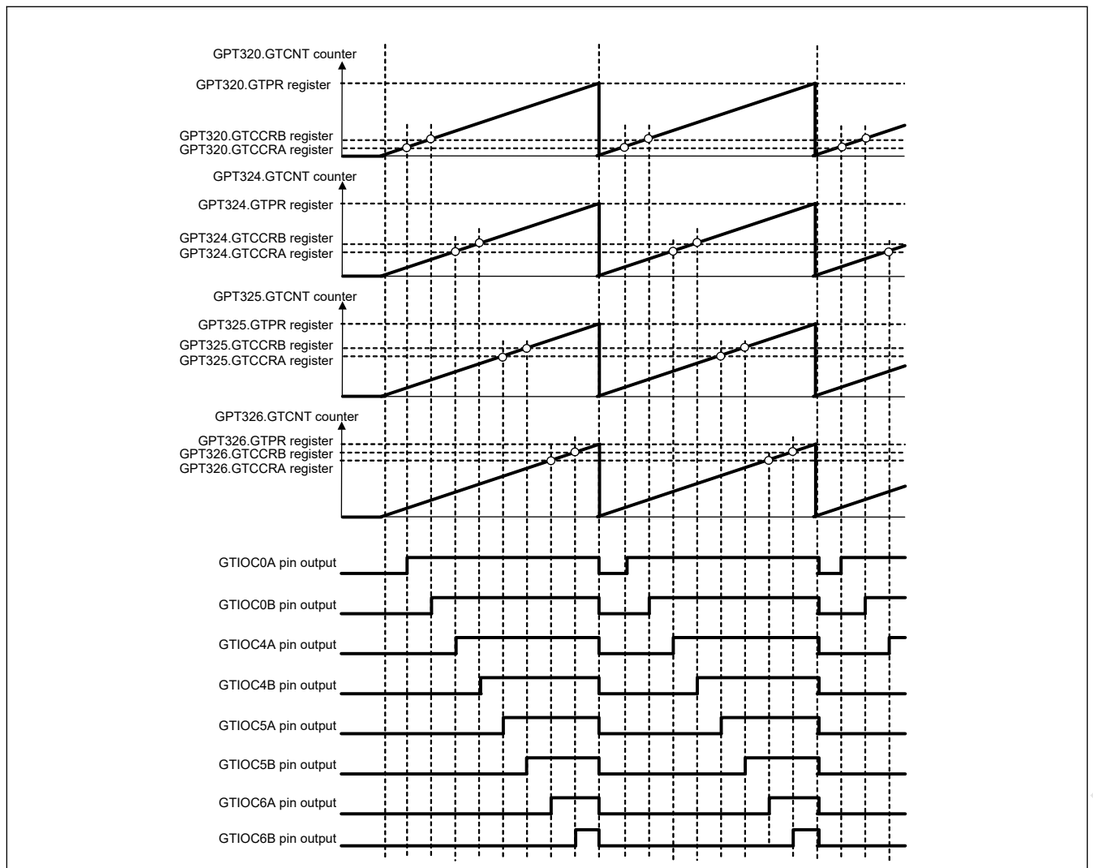


Figure 21.111 Example of synchronized PWM output

(2) 3-phase saw-wave complementary PWM output

Figure 21.112 shows an example in which three channels perform synchronized operation in saw-wave PWM mode 1 and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, low at a GTCCRB compare match, and high at the cycle end.

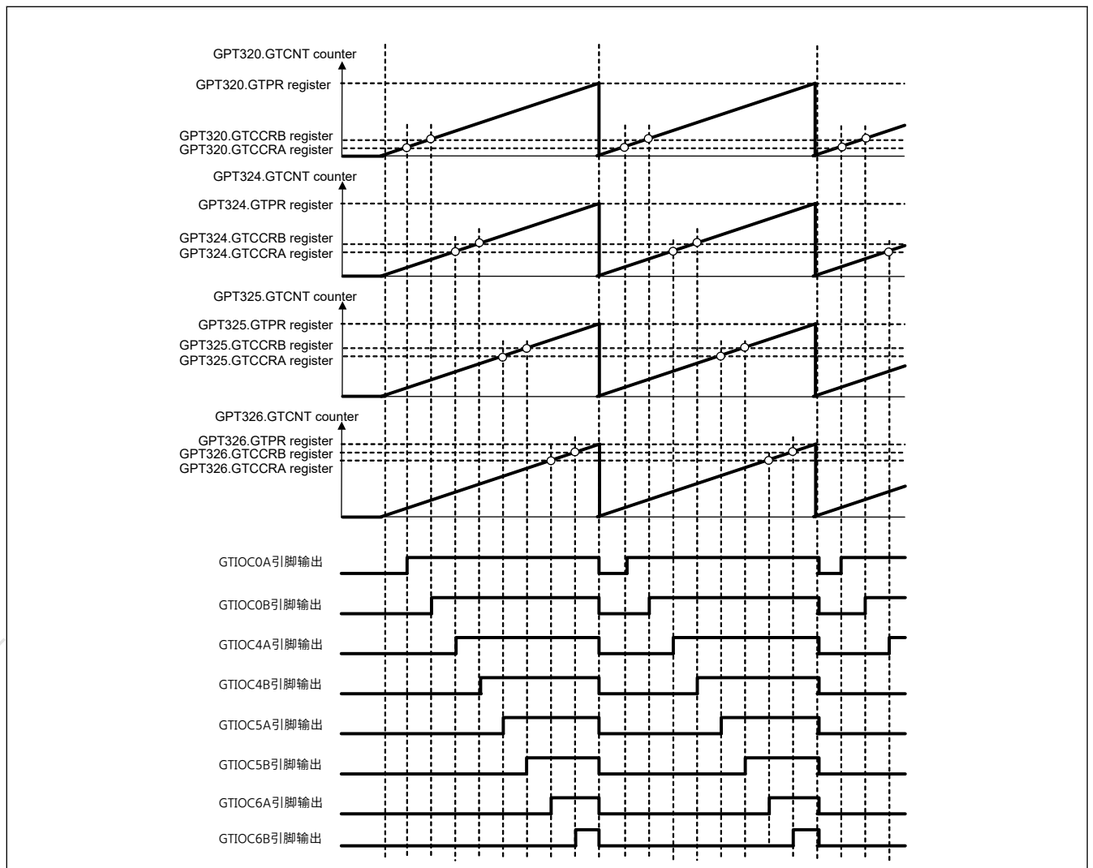


图21.111同步PWM输出示例

(2) 三相锯齿波互补PWM输出

图21.112显示了一个示例，其中三个通道在锯齿波PWM模式1下执行同步操作并输出三相互补PWM波形。GTIOCnA引脚设置为输出低作为初始值，在GTCCRA比较匹配时输出高，在周期结束时输出低。GTIOCnB引脚设置为输出高作为初始值，在GTCCRB比较匹配时输出低，在周期结束时输出高。

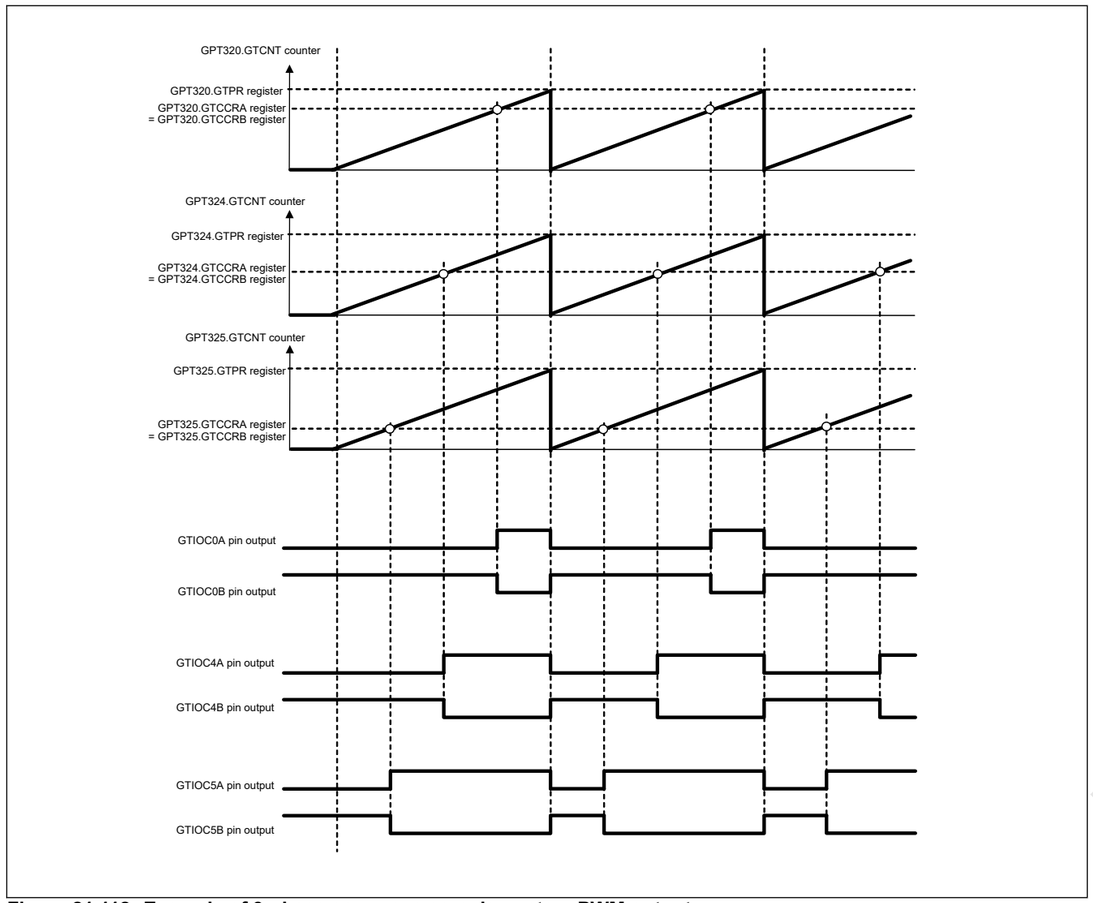


Figure 21.112 Example of 3-phase saw-wave complementary PWM output

(3) 3-phase saw-wave complementary PWM output with automatic dead time setting

Figure 21.113 shows an example in which three channels perform synchronized operation in saw-wave one-shot pulse mode with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTIOCnB compare match, and retains the output at the cycle end.

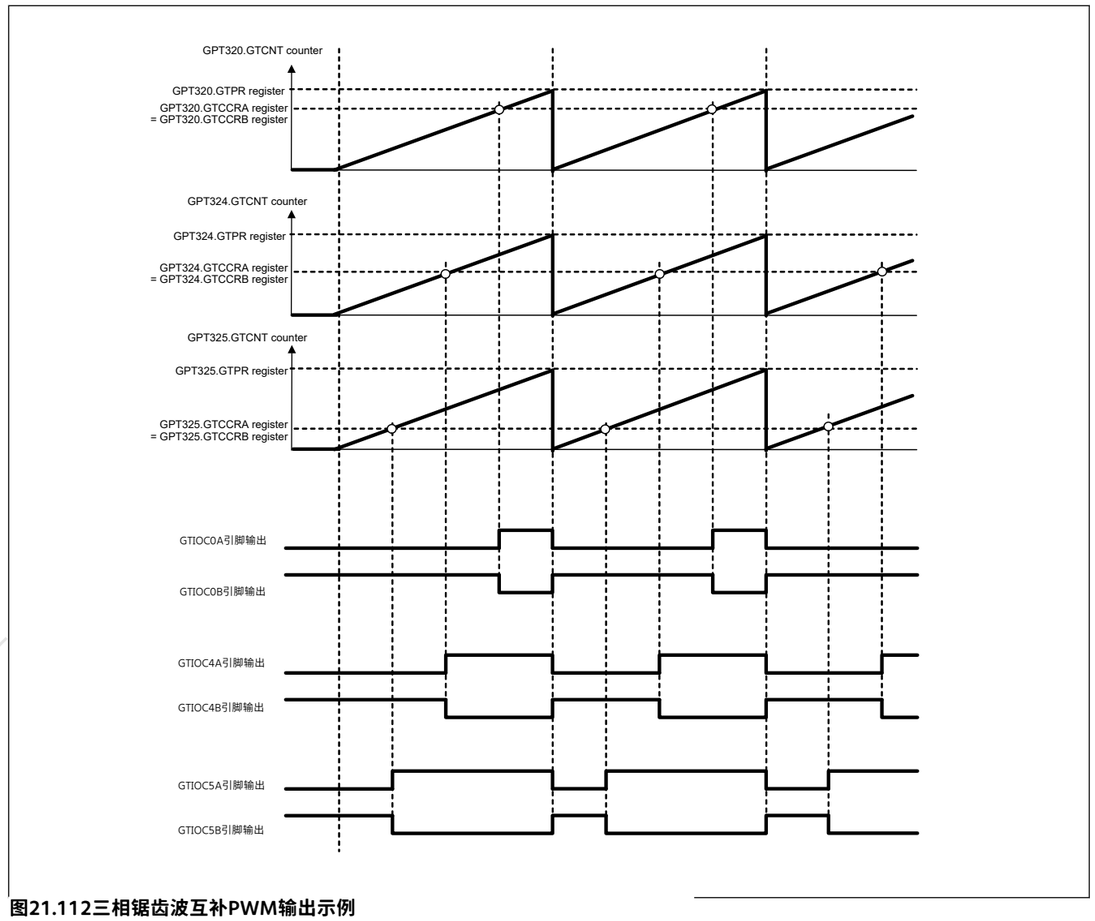


图21.112三相锯齿波互补PWM输出示例

(3) 具有自动死区时间设置的三相锯齿波互补PWM输出

图21.113显示了一个示例，其中三个通道在具有自动死区时间设置的锯齿波一次性脉冲模式下执行同步操作并输出三相互补PWM波形。GTIOCnA引脚设置为输出低电平作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCnB引脚设置为输出高电平作为初始值，在GTIOCnB比较匹配时切换输出，并在周期结束时保持输出。

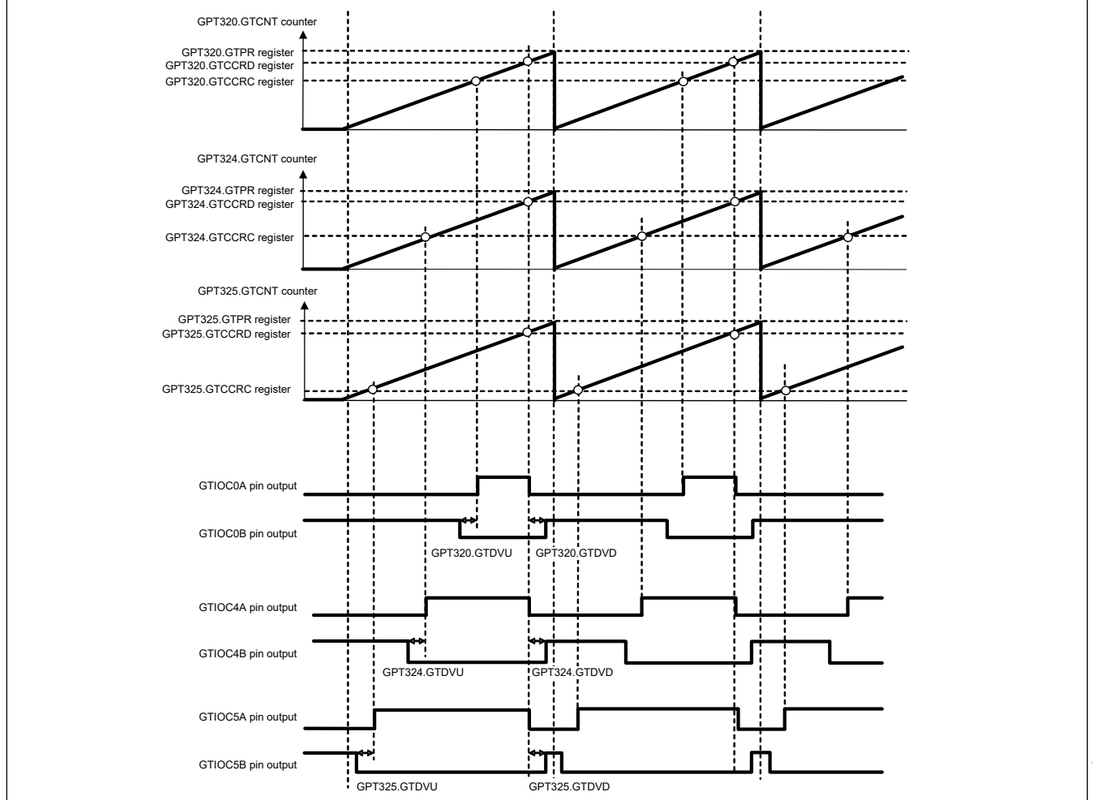


Figure 21.113 Example of 3-phase saw-wave complementary PWM output with automatic dead time setting

(4) 3-phase triangle-wave complementary PWM output

Figure 21.114 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

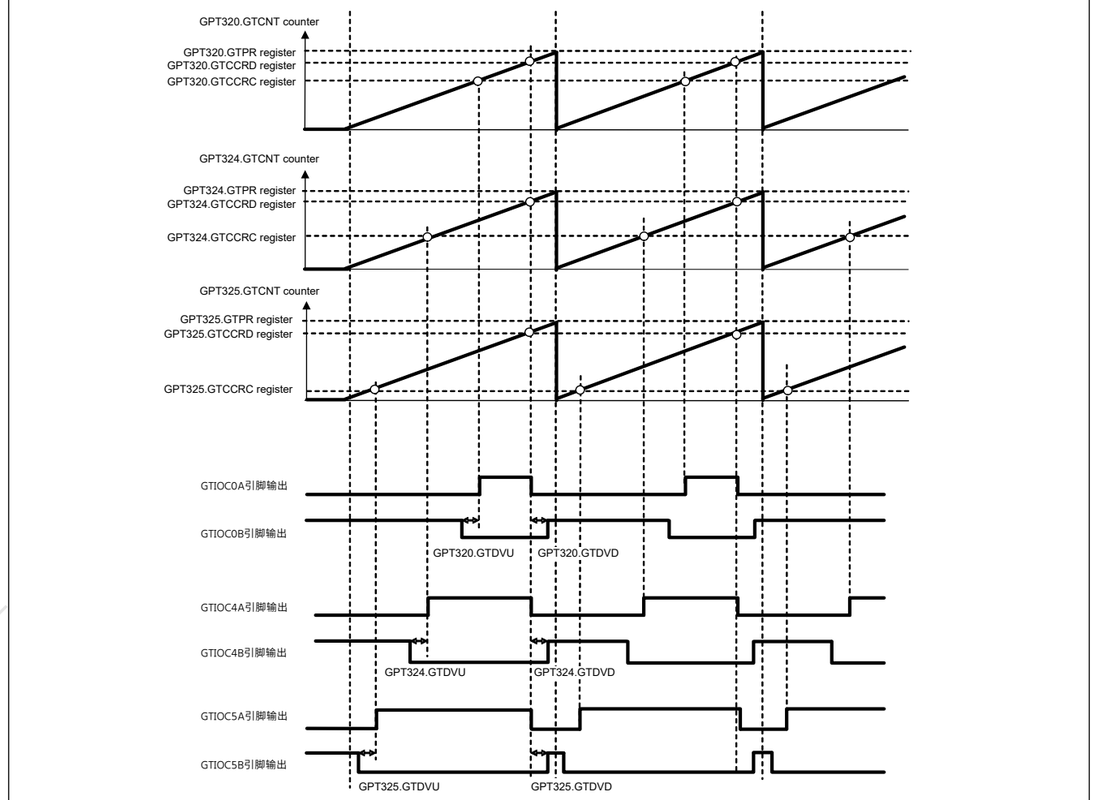


图21.113具有自动死区时间设置的三相锯齿波互补PWM输出示例

(4) 三相三角波互补PWM输出

图21.114显示了一个示例，其中三个通道在三角波PWM模式1中执行同步操作并输出三相互补PWM波形。GTIOCnA引脚设置为输出低电平作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCnB引脚设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在周期结束时保持输出。

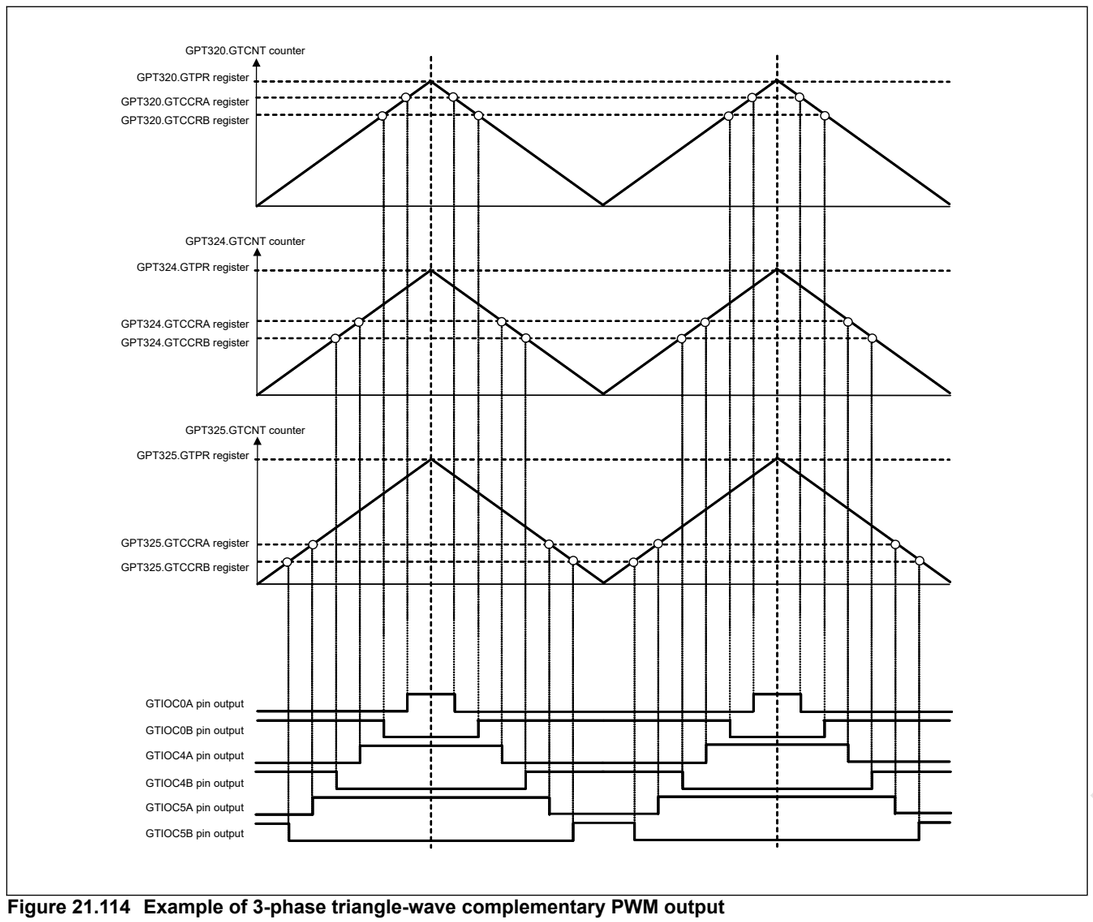


Figure 21.114 Example of 3-phase triangle-wave complementary PWM output

(5) 3-phase triangle-wave complementary PWM output with automatic dead time setting

Figure 21.115 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

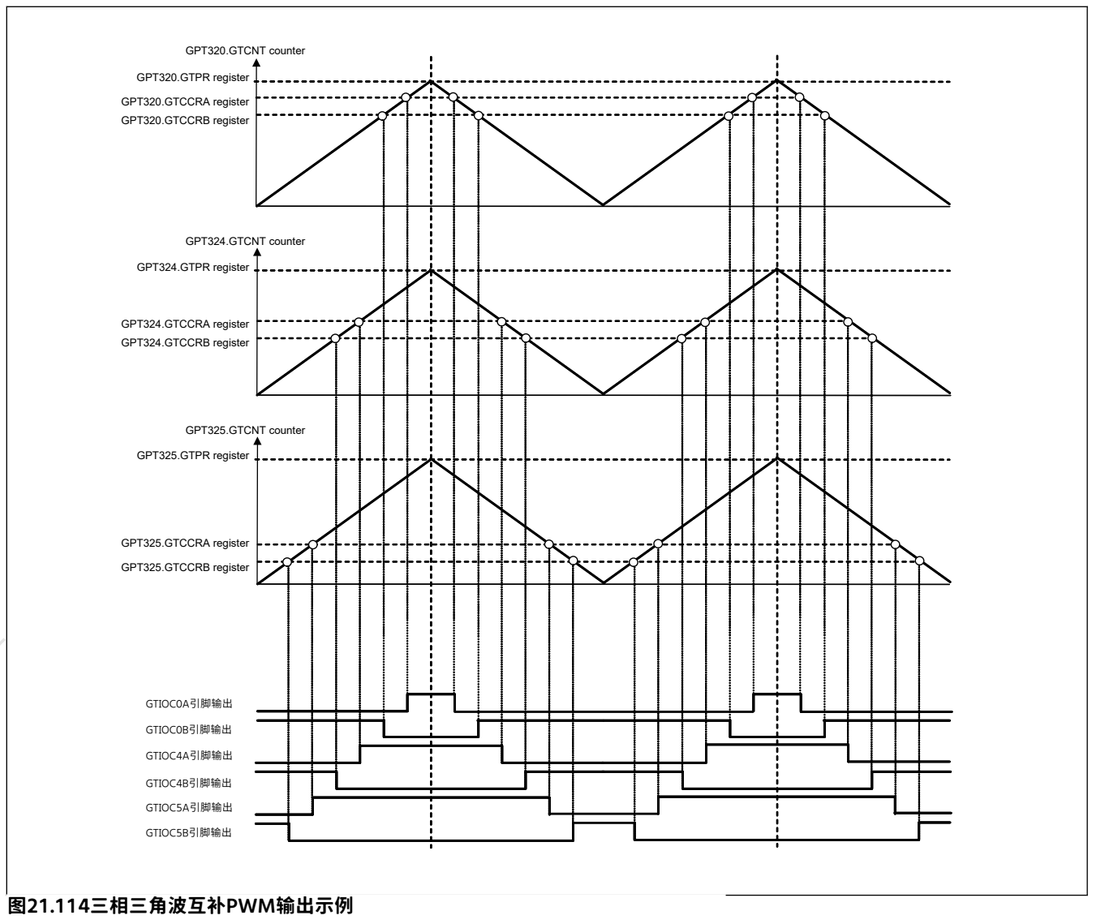


图21.114三相三角波互补PWM输出示例

(5) 具有自动死区时间设置的三相三角波互补PWM输出

图21.115显示了一个示例，其中三个通道在三角波PWM模式1下执行同步操作，自动设置死区时间并输出三相互补PWM波形。GTIOCnA引脚设置为输出低电平作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCnB引脚设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在周期结束时保持输出。

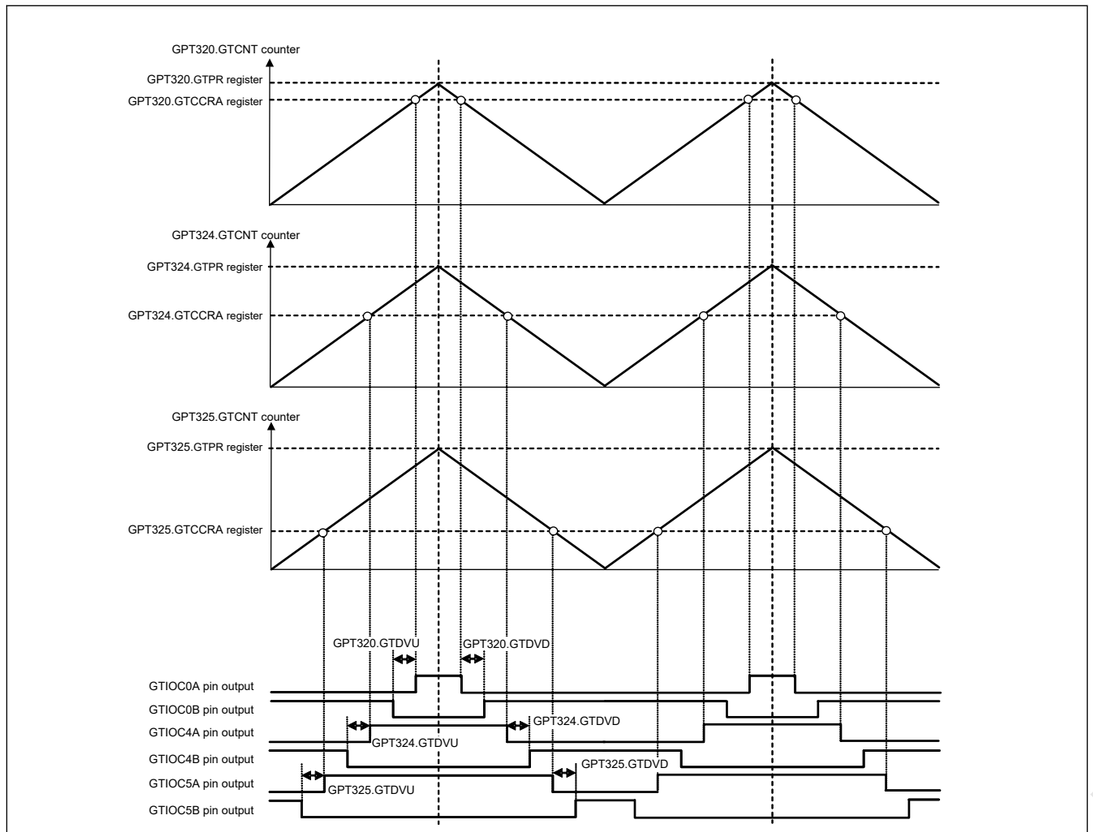


Figure 21.115 Example of 3-phase triangle-wave complementary PWM output with automatic dead time setting

(6) 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

Figure 21.116 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 3 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

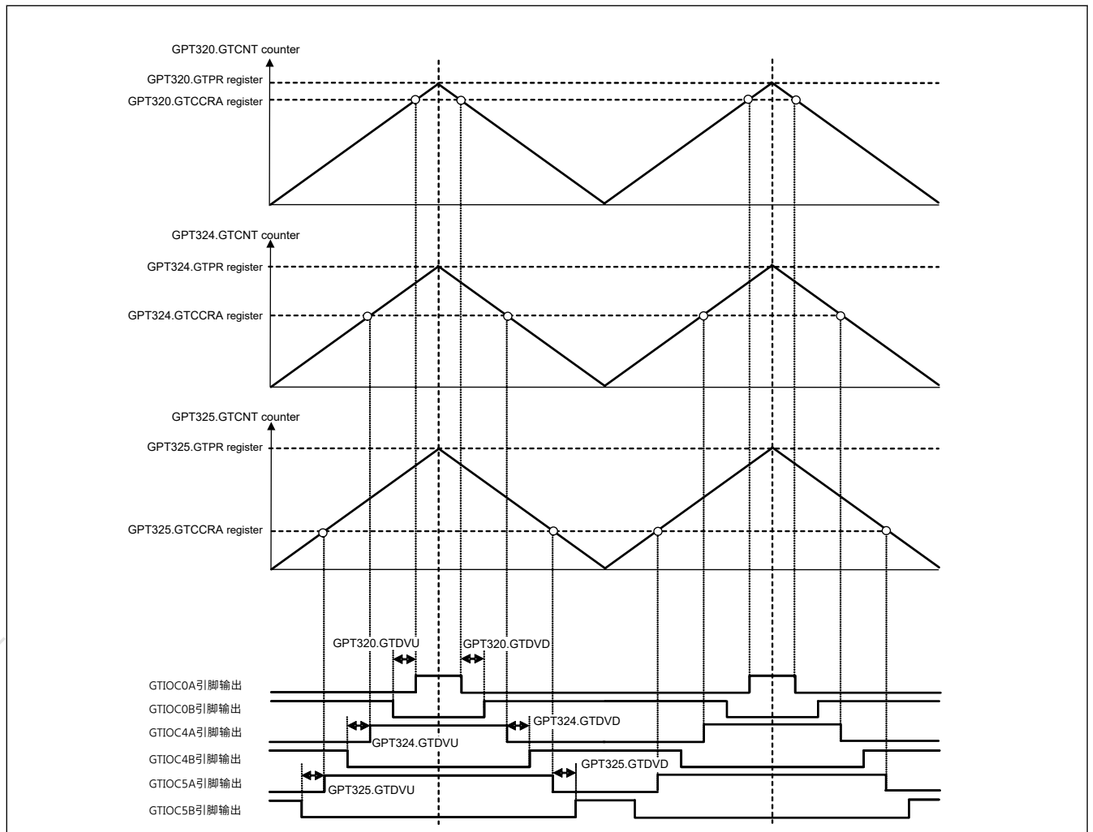


图21.115带自动死区时间设置的三相三角波互补PWM输出示例

(6) 具有自动死区时间设置的三相不对称三角波互补PWM输出

图21.116显示了一个示例，其中三个通道在具有自动死区时间设置的三角波PWM模式3下执行同步操作并输出三相互补PWM波形。GTIOCnA设置为输出低作为初始值，在GTCCRA比较匹配时切换输出，并在循环结束时保留输出。GTIOCnB设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在循环结束时保留输出。

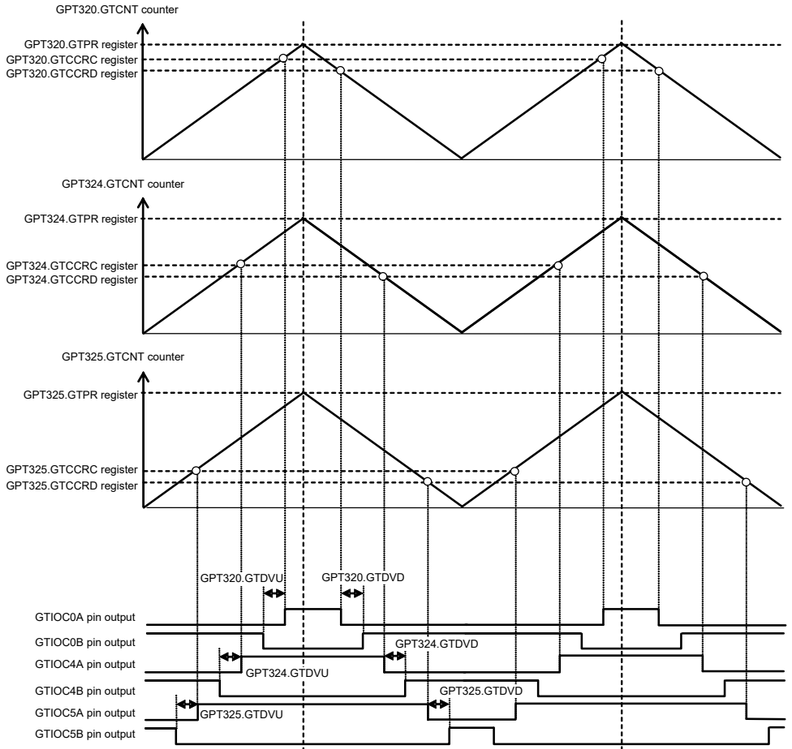


Figure 21.116 Example of 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

21.3.10 Period Count Function

By setting the GTPC register, the end of period can be counted.

The number of period to be counted should be set into the GTPC.PCNT counter when the GTPC.PCEN bit is 0. When the PCEN bit is 1, the PCNT counter can be read, but writing is disabled. When the PCEN bit is 1, down-counting is performed at the end of period. When the PCNT counter is 1 at the end of period, it becomes 0 and counting is stopped to finish the period count function. At that time, the GTST.PCF flag is set, and the period count function finish interrupt request GPTn_PC is generated. When the GTPC.ASTP bit is 1, the GTCNT counter is also stopped at the same time that the period count function is finished.

When the GTCNT counter is stopped while period count function is enabled, the PCNT counter keeps its value. When the GTCNT counter restarts counting and the PCEN bit is 1, the PCNT counter restarts down-counting from the hold value.

When the PCEN bit is changed from 0 to 1 while the PCNT counter is 0 and the ASTP bit is 1, the GTCNT counter is stopped at the count clock immediately after that.

When either GTSECR.SPCE bit or GTSECR.SPCD bit is set to 1, the PCEN bit in the channels set to 1 by the GTSECSR register is simultaneously set the value to enable or disable the period count function for multiple channels.

Figure 21.117 and Figure 21.118 show examples of PWM cycle count function.

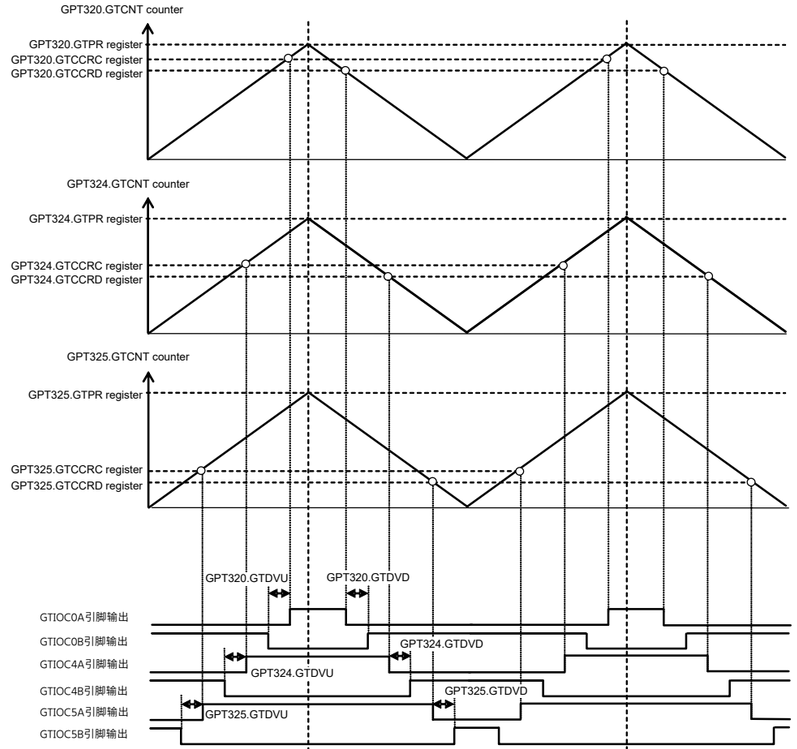


图21.116具有自动死区时间设置的三相不对称三角波互补PWM输出示例

21.3.10 周期计数功能

通过设置GTPC寄存器，可以计算周期结束。

当GTPC.PCEN位为0时，要计数的周期数应设置到GTPC.PCNT计数器中。当PCEN位为1，可以读取PCNT计数器，但禁止写入。当PCEN位为1时，在周期结束时执行递减计数。当PCNT计数器在周期结束时为1时，它变为0并停止计数以完成周期计数功能。此时，GTST.PCF标志置位，产生周期计数功能完成中断请求GPTn_PC。当GTPC.ASTP位为1时，GTCNT计数器也在周期计数功能完成的同时停止。

当GTCNT计数器停止而周期计数功能使能时，PCNT计数器保持其值。当。。。的时候GTCNT计数器重新开始计数且PCEN位为1，PCNT计数器重新从保持值开始向下计数。

当PCEN位从0变为1且PCNT计数器为0且ASTP位为1时，GTCNT计数器立即在计数时钟处停止。

当GTSECR.SPCE位或GTSECR.SPCD位设置为1时，通过GTSECSR寄存器设置为1的通道中的PCEN位同时设置该值以启用或禁用多个通道的周期计数功能。

图21.117和图21.118显示了PWM周期计数功能的示例。

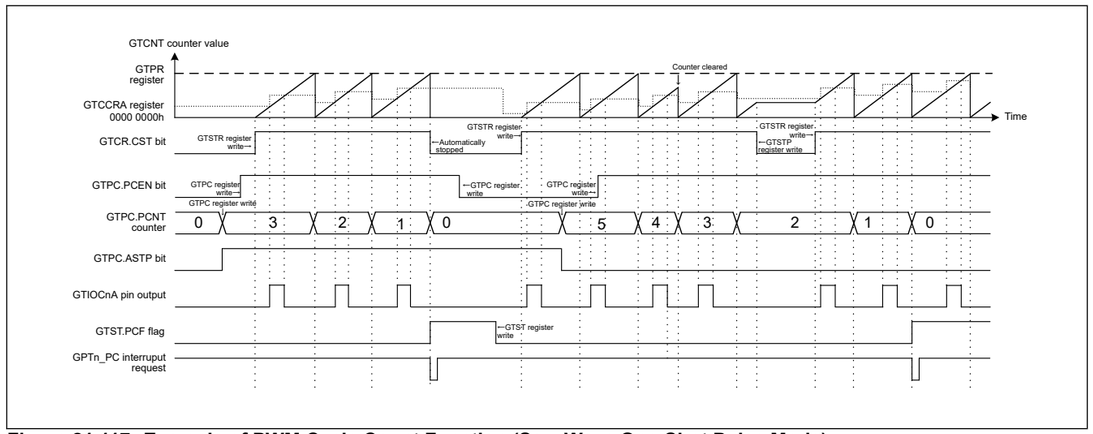


Figure 21.117 Example of PWM Cycle Count Function (Saw-Wave One-Shot Pulse Mode)

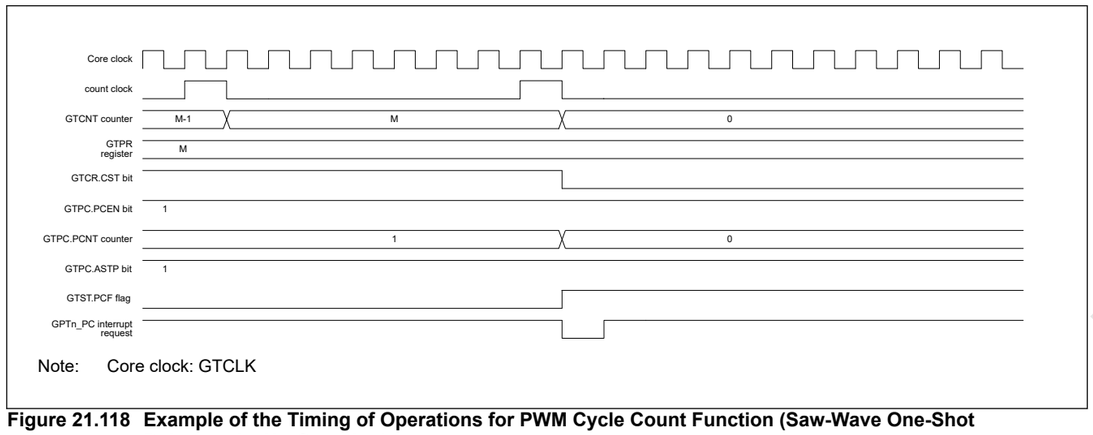


Figure 21.118 Example of the Timing of Operations for PWM Cycle Count Function (Saw-Wave One-Shot Pulse mode, Up-Counting)

21.3.11 Phase Counting Function

The phase difference between the GTIOCnA and GTIOCnB pin (n = 0 to 3) inputs is detected and the associated GTCNT counts up or counts down. The detectable phase difference is available in any combination with the relationship between the edge and the level of GTIOCnA and GTIOCnB pin inputs being set in the GTUPSR and GTDNSR registers. For details on count operation, see section 21.3.1.1. Counter operation.

Figure 21.119 to Figure 21.128 show an example of phase counting modes 1 to 5 operation when the GTIOCnA, GTIOCnB pins are used. Table 21.51 to Table 21.60 show conditions of up-counting or down-counting and list settings for the GTUPSR and GTDNSR registers which is corresponding to Figure 21.119 to Figure 21.128.

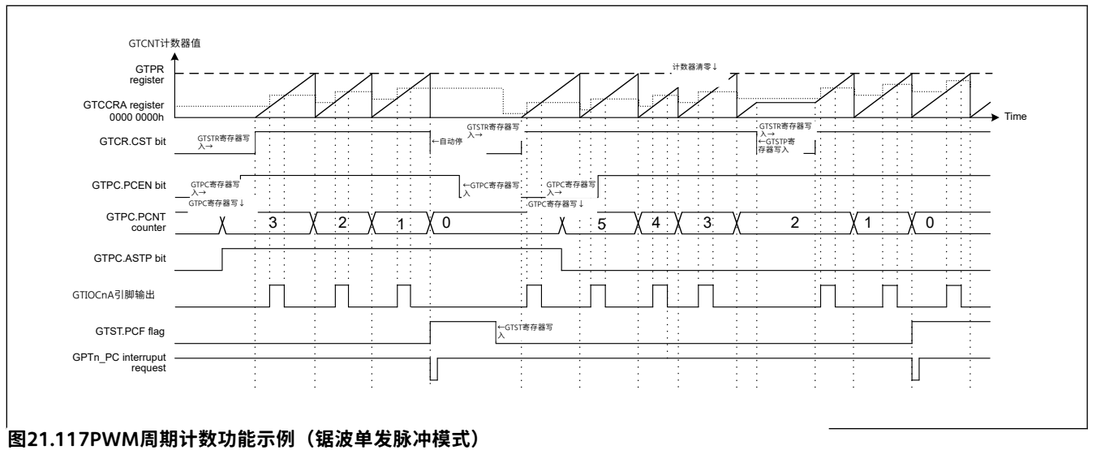


图21.117PWM周期计数功能示例（锯波单发脉冲模式）

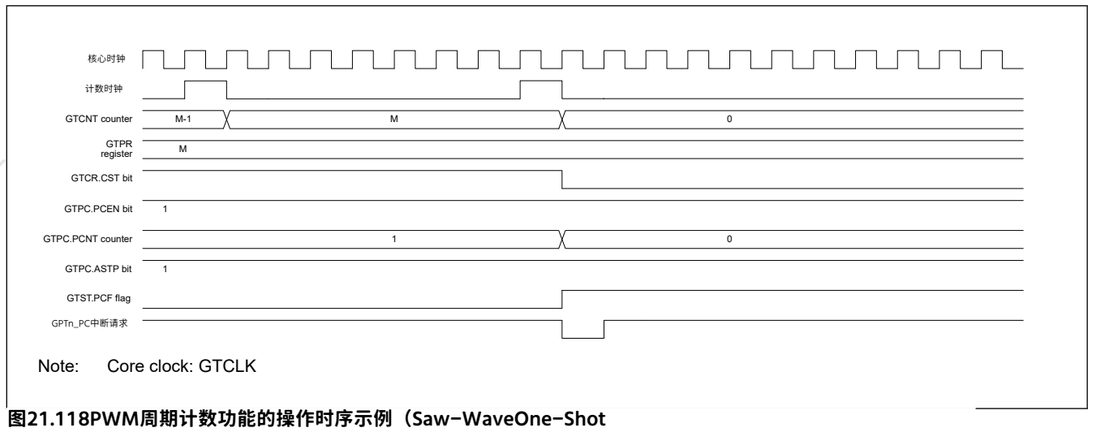


图21.118PWM周期计数功能的操作时序示例（Saw-WaveOne-Shot脉冲模式，向上计数）

21.3.11 相位计数功能

检测到GTIOCnA和GTIOCnB引脚（n=0到3）输入之间的相位差，并且相关的GTCNT向上计数或向下计数。可检测的相位差可与在GTUPSR和GTDNSR寄存器中设置的GTIOCnA和GTIOCnB引脚输入的边沿和电平之间的关系进行任何组合。有关计数操作的详细信息，请参阅第21.3.1.1节。柜台操作。

图21.119至图21.128显示了使用GTIOCnA、GTIOCnB引脚时相位计数模式1至5操作的示例。表21.51至表21.60显示了向上计数或向下计数的条件，并列出了GTUPSR和GTDNSR寄存器的设置，对应于图21.119至图21.128。

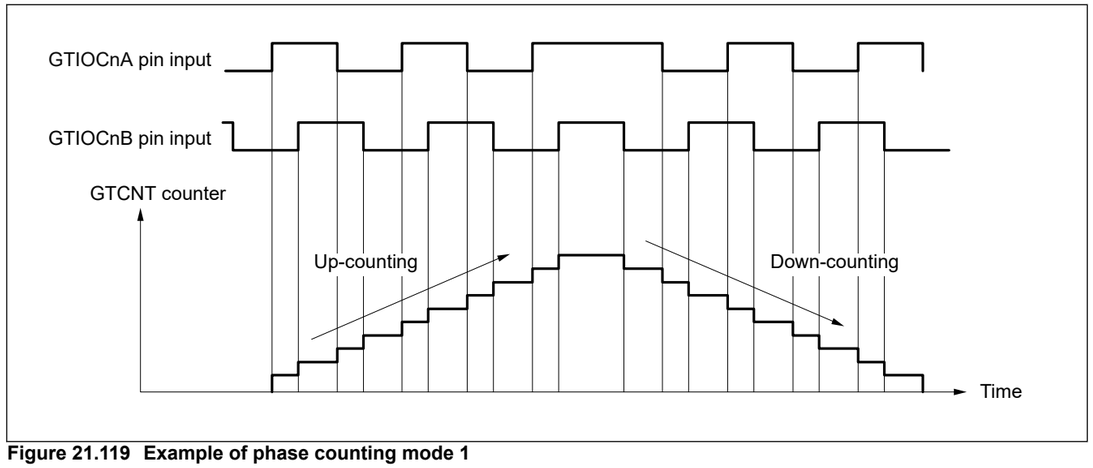


Figure 21.119 Example of phase counting mode 1

Table 21.51 Conditions of up-counting/down-counting in phase counting mode 1

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 0x00006900 GTDNSR = 0x00009600
Low	↓		
↑	Low		
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High		
↓	Low		

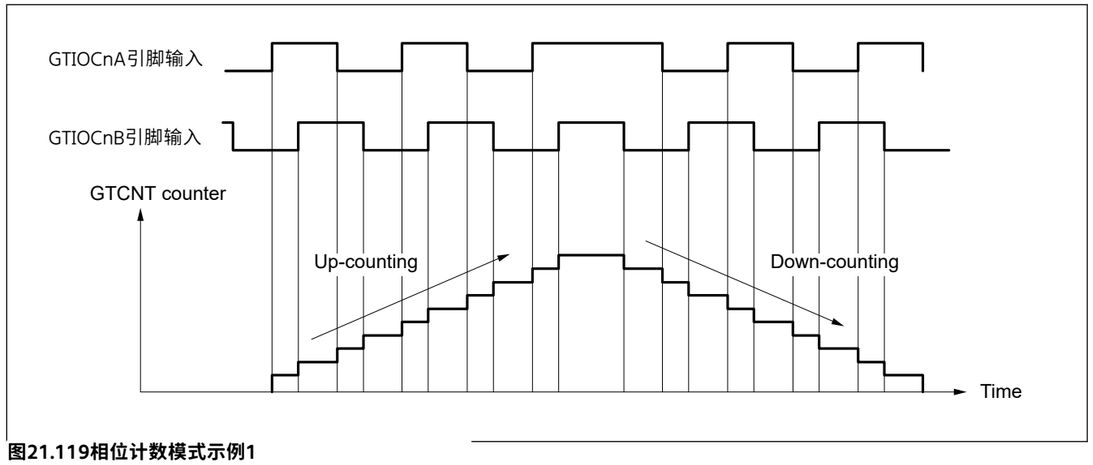


图21.119相位计数模式示例1

Table 21.51 相位计数模式加减计数条件1

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	Up-counting	GTUPSR = 0x00006900 GTDNSR = 0x00009600
Low	↓		
↑	Low		
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High		
↓	Low		

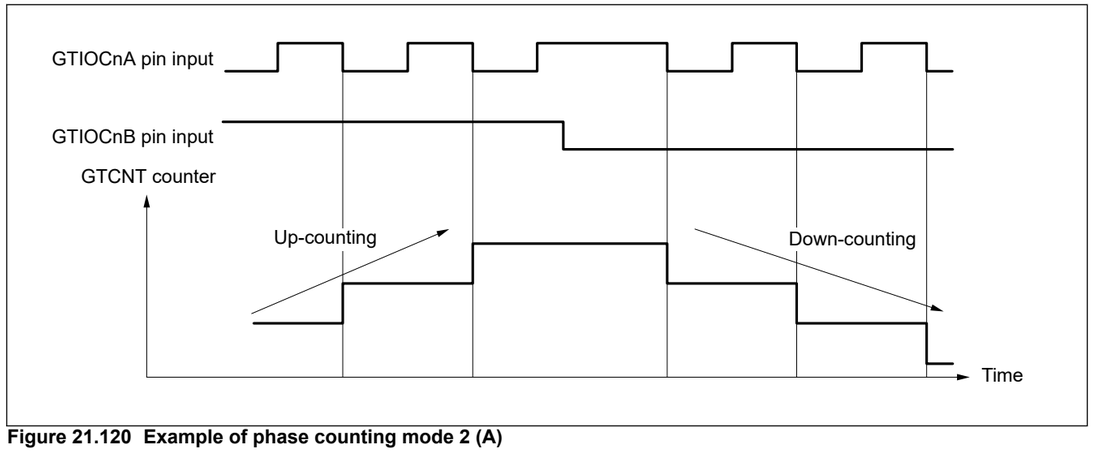


Figure 21.120 Example of phase counting mode 2 (A)

Table 21.52 Conditions of up-counting/down-counting in phase counting mode 2 (A)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000800 GTDNSR = 0x00000400
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Not counting	
Low	↑		
↑	High		
↓	Low	Down-counting	

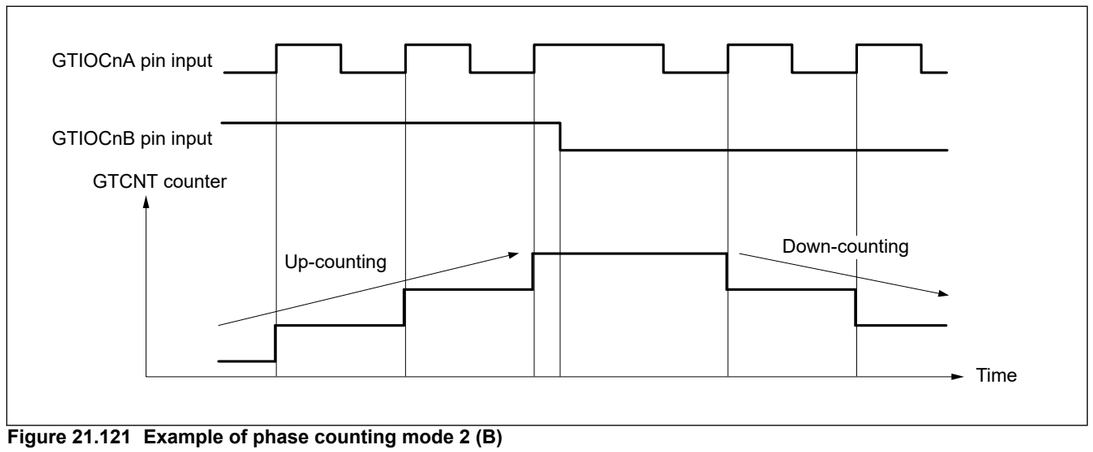


Figure 21.121 Example of phase counting mode 2 (B)

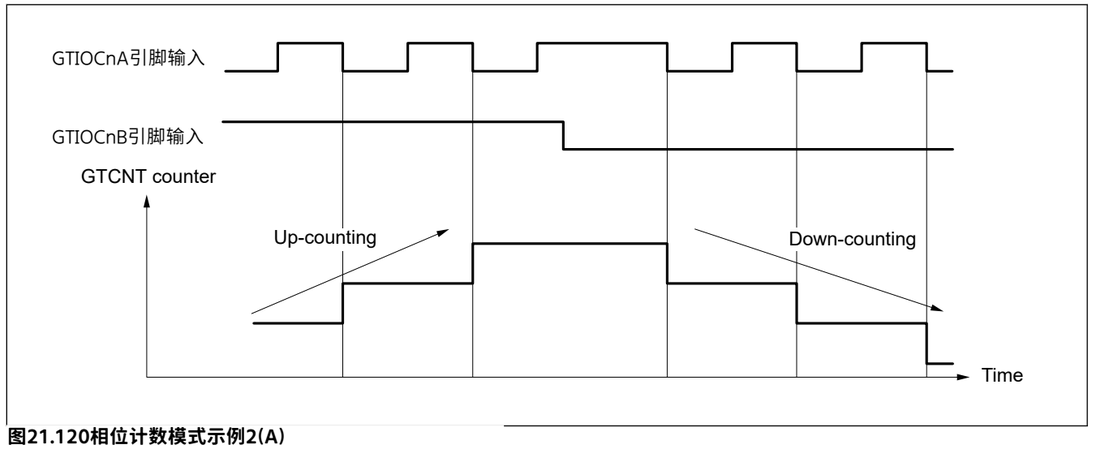


图21.120相位计数模式示例2(A)

Table 21.52 相位计数模式2(A)加减计数条件

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x00000800 GTDNSR = 0x00000400
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	不算数	
Low	↑		
↑	High		
↓	Low	Down-counting	

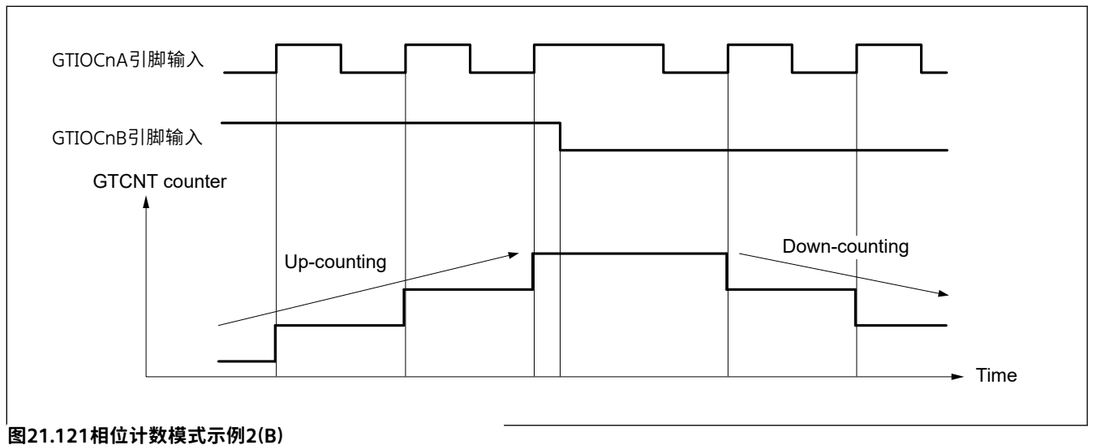


图21.121相位计数模式示例2(B)

Table 21.53 Conditions of up-counting/down-counting in phase counting mode 2 (B)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000200 GTDNSR = 0x00000100
Low	↓		
↑	Low	Down-counting	
↓	High	Not counting	
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Not counting	

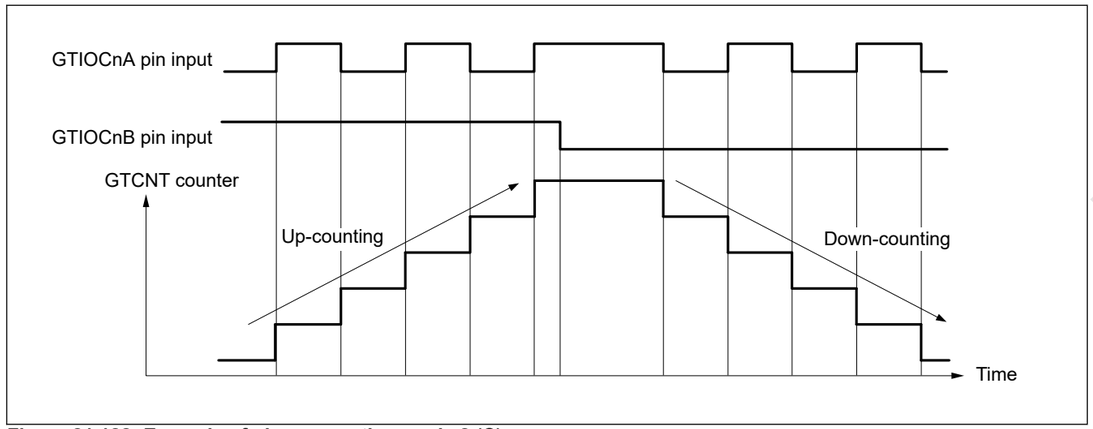


Figure 21.122 Example of phase counting mode 2 (C)

Table 21.53 相位计数模式2(B)加减计数条件

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x00000200 GTDNSR = 0x00000100
Low	↓		
↑	Low	Down-counting	
↓	High	不算数	
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	不算数	

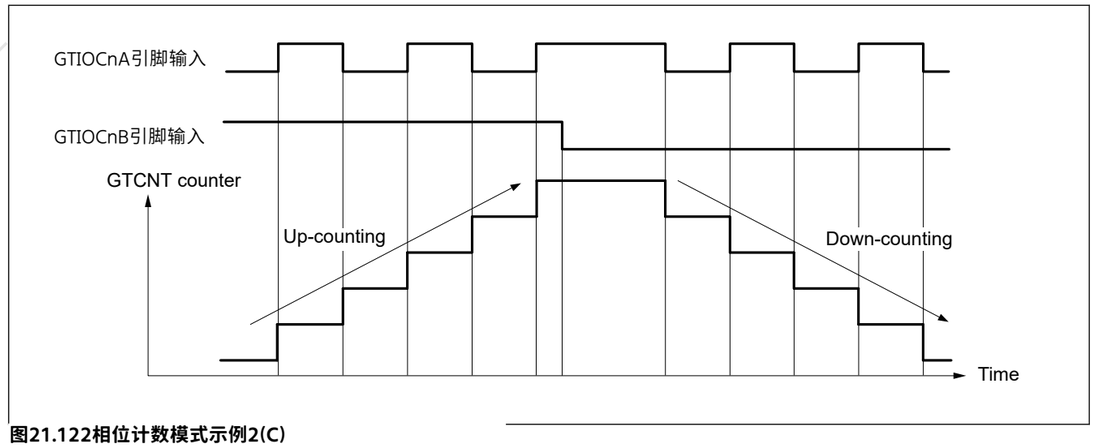


图21.122相位计数模式示例2(C)

Table 21.54 Conditions of up-counting/down-counting in phase counting mode 2 (C)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000A00 GTDNSR = 0x00000500
Low	↓		
↑	Low	Down-counting	
↓	High	Up-counting	
High	↓	Not counting	
Low	↑		
↑	High	Up-counting	
↓	Low	Down-counting	

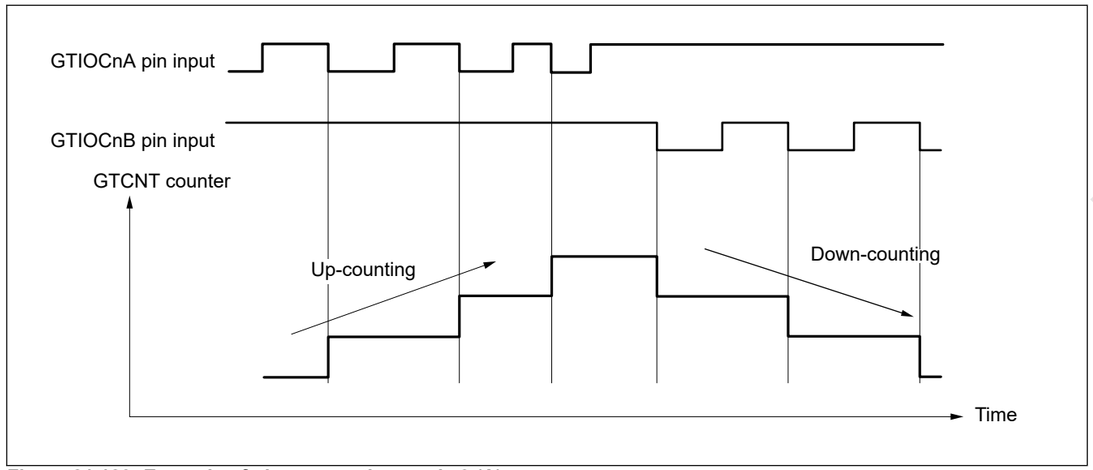


Figure 21.123 Example of phase counting mode 3 (A)

Table 21.54 相位计数模式2(C)加减计数条件

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x00000A00 GTDNSR = 0x00000500
Low	↓		
↑	Low	Down-counting	
↓	High	Up-counting	
High	↓	不算数	
Low	↑		
↑	High	Up-counting	
↓	Low	Down-counting	

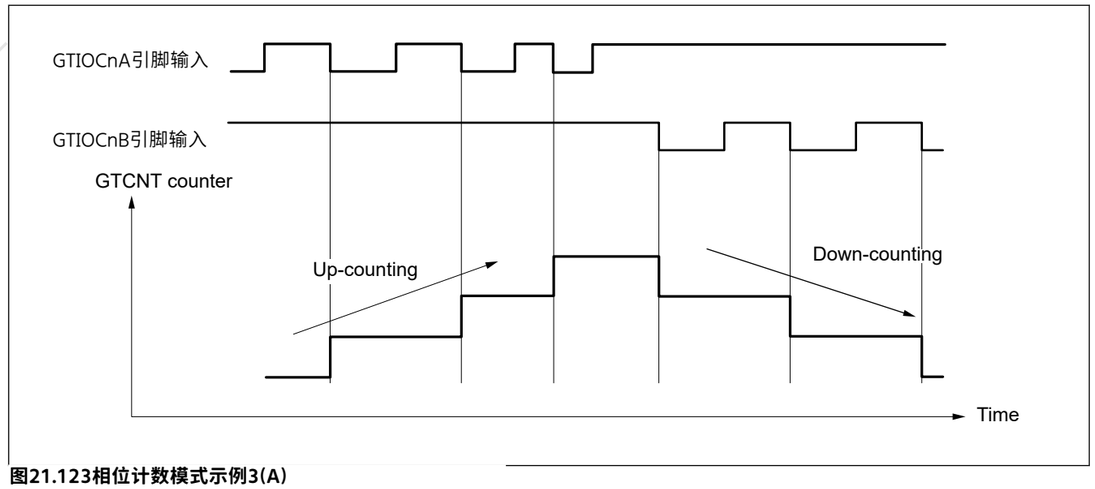


图21.123相位计数模式示例3(A)

Table 21.55 Conditions of up-counting/down-counting in phase counting mode 3 (A)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000800 GTDNSR = 0x00008000
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Not counting	
↑	High		
↓	Low		

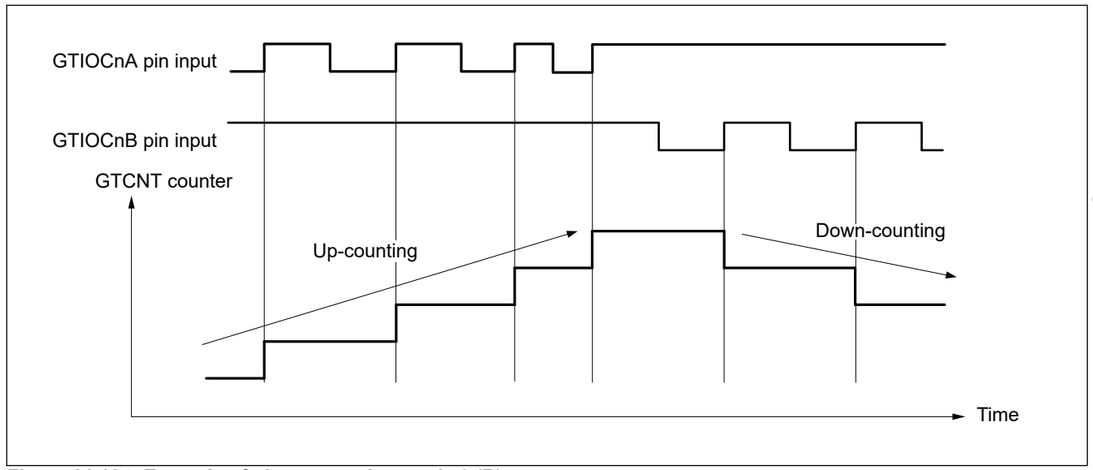


Figure 21.124 Example of phase counting mode 3 (B)

Table 21.55 相位计数模式3(A)加减计数条件

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x00000800 GTDNSR = 0x00008000
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	不算数	
↑	High		
↓	Low		

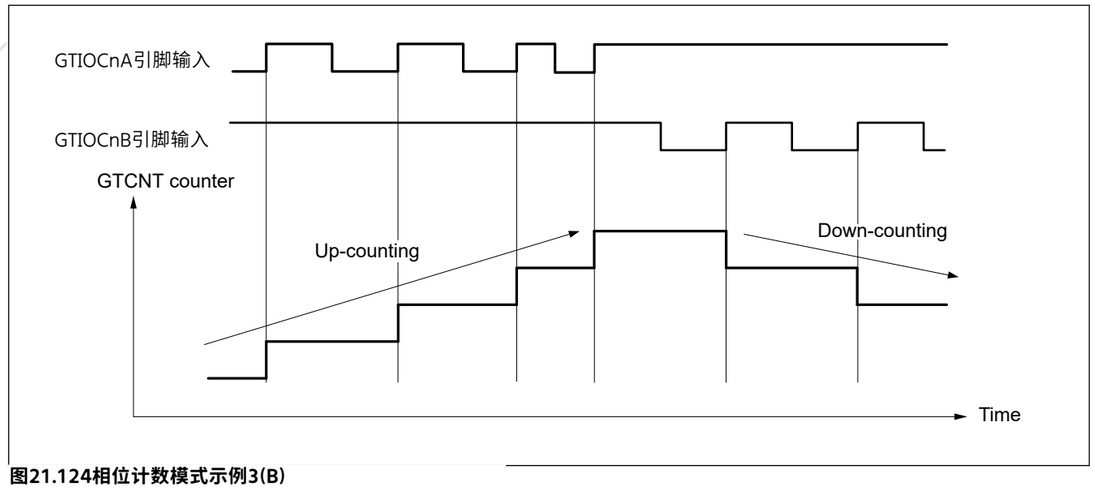


图21.124相位计数模式示例3(B)

Table 21.56 Conditions of up-counting/down-counting in phase counting mode 3 (B)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 0x00000200 GTDNSR = 0x00002000
Low	↓	Not counting	
↑	Low		
↓	High		
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Not counting	

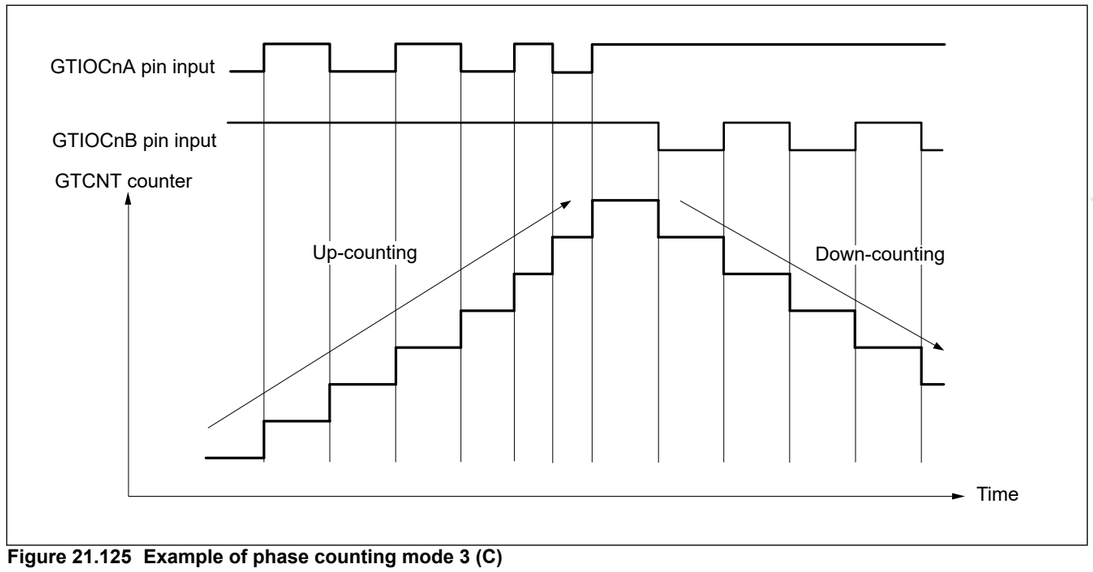


Figure 21.125 Example of phase counting mode 3 (C)

Table 21.56 相位计数模式3(B)加减计数条件

↑ :上升沿

↓ :下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	Down-counting	GTUPSR = 0x00000200 GTDNSR = 0x00002000
Low	↓	不算数	
↑	Low		
↓	High		
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	不算数	

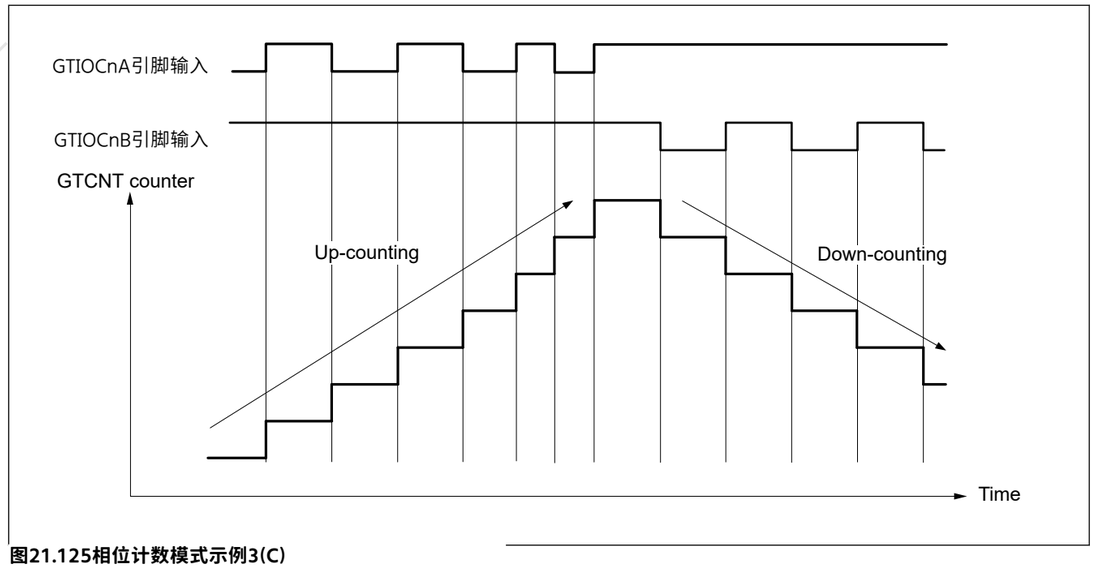


图21.125相位计数模式示例3(C)

Table 21.57 Conditions of up-counting/down-counting in phase counting mode 3 (C)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 0x00000A00 GTDNSR = 0x0000A000
Low	↓	Not counting	
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Not counting	
↑	High	Up-counting	
↓	Low	Not counting	

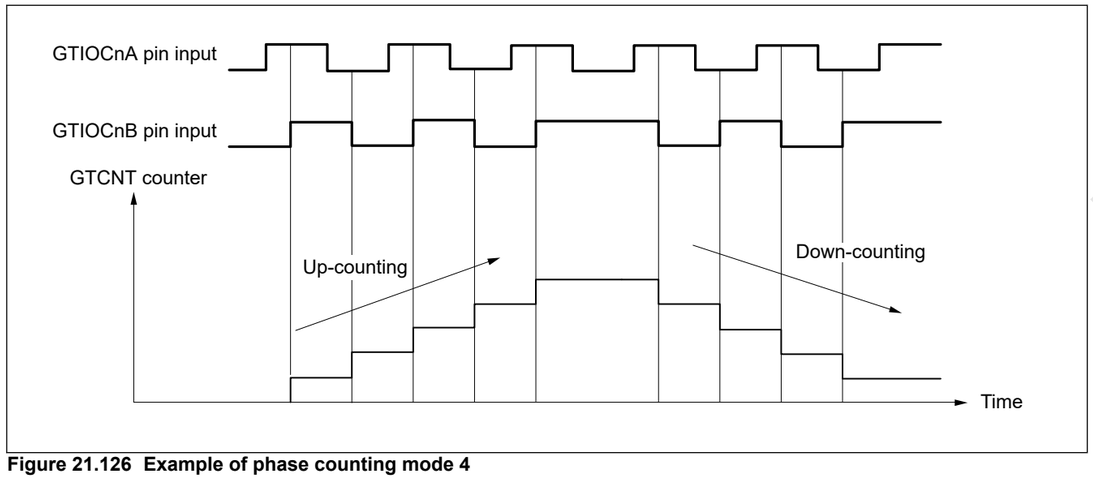


Figure 21.126 Example of phase counting mode 4

Table 21.57 相位计数模式3(C)加减计数条件

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	Down-counting	GTUPSR = 0x00000A00 GTDNSR = 0x0000A000
Low	↓	不算数	
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	不算数	
↑	High	Up-counting	
↓	Low	不算数	

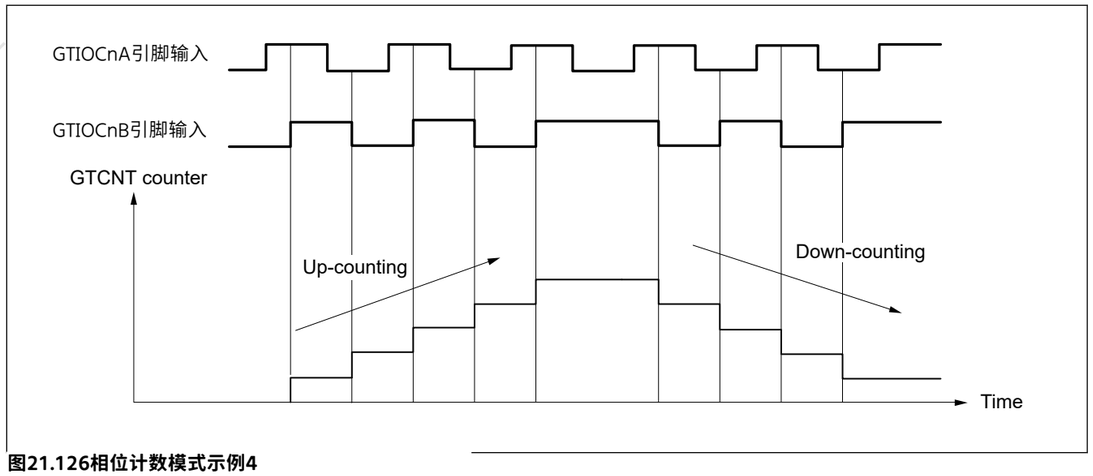


图21.126相位计数模式示例4

Table 21.58 Conditions of up-counting/down-counting in phase counting mode 4

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 0x00006000 GTDNSR = 0x00009000
Low	↓		
↑	Low	Not counting	
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High	Not counting	
↓	Low		

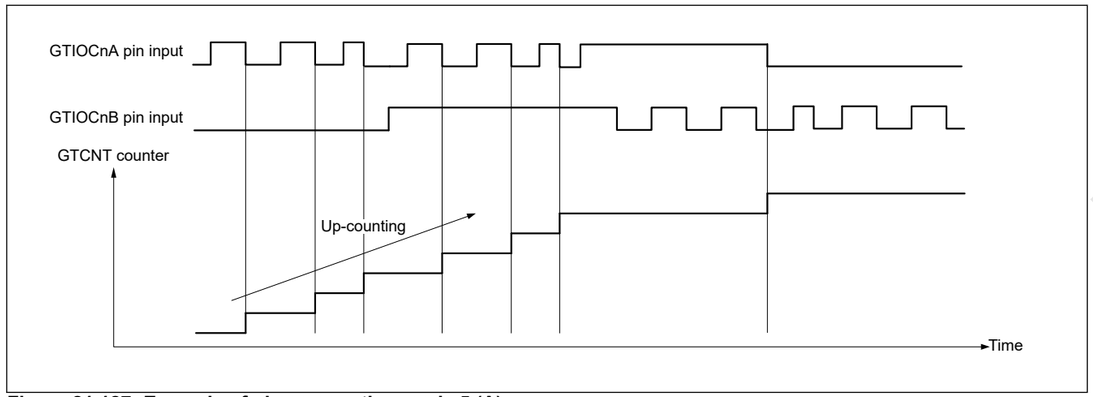


Figure 21.127 Example of phase counting mode 5 (A)

Table 21.58 相位计数方式4加减计数条件

↑ :上升沿

↓ :下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	Up-counting	GTUPSR = 0x00006000 GTDNSR = 0x00009000
Low	↓		
↑	Low	不算数	
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High	不算数	
↓	Low		

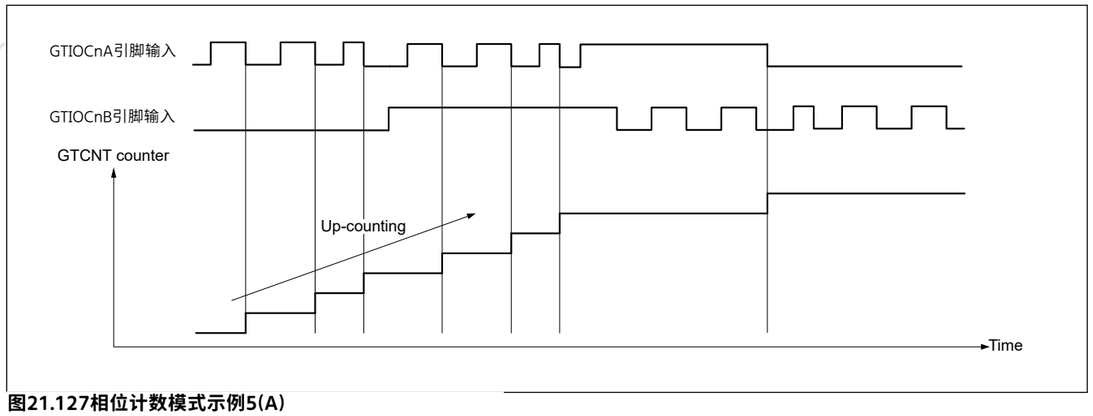


图21.127相位计数模式示例5(A)

Table 21.59 Conditions of up-counting/down-counting in phase counting mode 5 (A)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000C00 GTDNSR = 0x00000000
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Not counting	
Low	↑		
↑	High		
↓	Low	Up-counting	

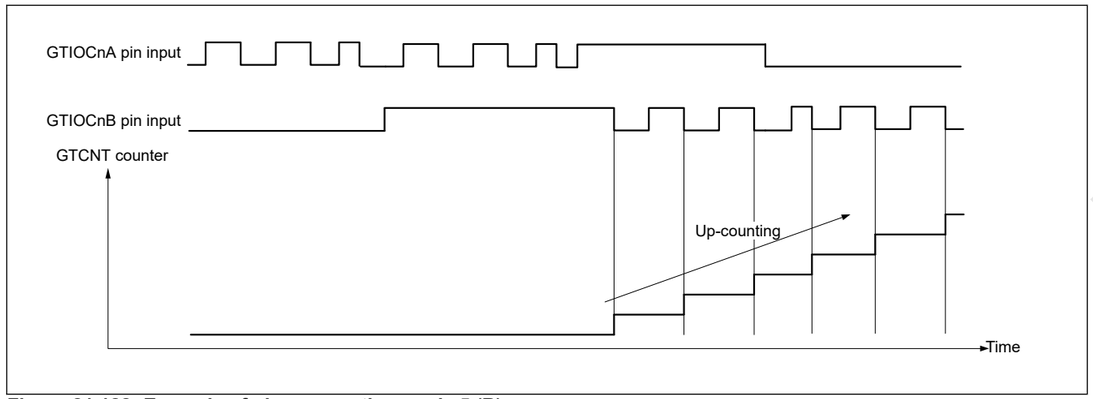


Figure 21.128 Example of phase counting mode 5 (B)

Table 21.59 相位计数模式下加减计数条件5（A）

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x00000C00 GTDNSR = 0x00000000
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	不算数	
Low	↑		
↑	High		
↓	Low	Up-counting	

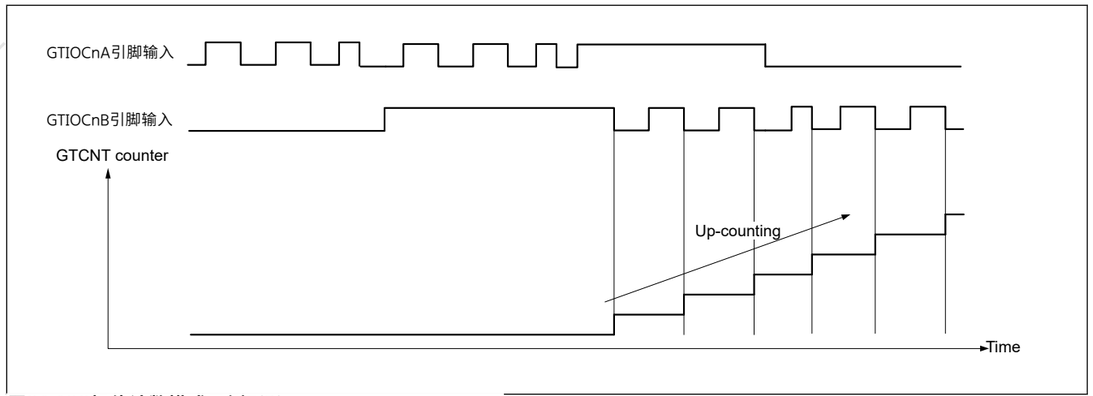


图21.128相位计数模式示例5(B)

Table 21.60 Conditions of up-counting/down-counting in phase counting mode 5 (B)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High		Not counting	GTUPSR = 0x0000C000 GTDNSR = 0x00000000
Low		Up-counting	
	Low	Not counting	
	High		
High		Up-counting	
Low		Not counting	
	High		
	Low		

21.3.12 External pulse width measuring function

The pulse width of GTIOCnA pin input (n = 0 to 3), GTIOCnB pin input, and GTETRGA / GTETRGB / GTETRGC / GTETRGD pin inputs can be measured.

The setting to enable or disable count-up of the GTCNT counter and the input pin and level which measured pulse width are selected by the USILVL[3:0] bits of the GTUPSR register.

The setting to enable or disable count-down of the GTCNT counter and the input pin and level which measured pulse width are selected by the DSILVL[3:0] bits of the GTDNSR register.

The setting to enable both count-up and count-down of the GTCNT counter at the same time is prohibited.

The counting operation performs periodic counting with the period of the GTPR register.

If the phase counting function and the pulse width measuring function are enabled at the same time, the pulse width measuring function does not work and the phase counting function works.

Figure 21.129, Figure 21.130 show examples of external pulse width measuring function and Table 21.61 shows example for setting external pulse width measuring function.

Table 21.60 相位计数模式下加减计数条件5(B)

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High		不算数	GTUPSR = 0x0000C000 GTDNSR = 0x00000000
Low		Up-counting	
	Low	不算数	
	High		
High		Up-counting	
Low		不算数	
	High		
	Low		

21.3.12 外部脉宽测量功能

GTIOCnA引脚输入（n=0至3）、GTIOCnB引脚输入和GTETRGAGTETRGBGTETRGC的脉冲宽度可以测量GTETRGD引脚输入。

通过GTUPSR寄存器的USILVL[3:0]位选择启用或禁用GTCNT计数器的计数以及测量脉冲宽度的输入引脚和电平的设置。

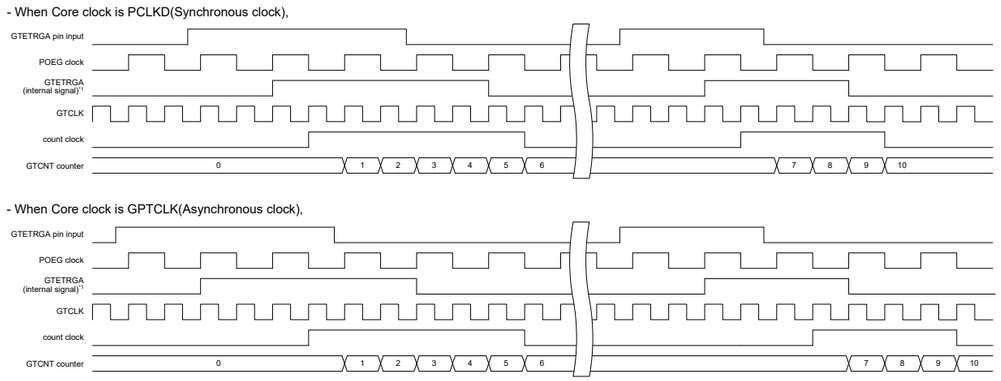
通过GTDNSR寄存器的DSILVL[3:0]位选择启用或禁用GTCNT计数器的倒数计数以及测量脉冲宽度的输入引脚和电平。

禁止同时启用GTCNT计数器的加计数和减计数的设置。

计数操作以GTPR寄存器的周期进行周期性计数。

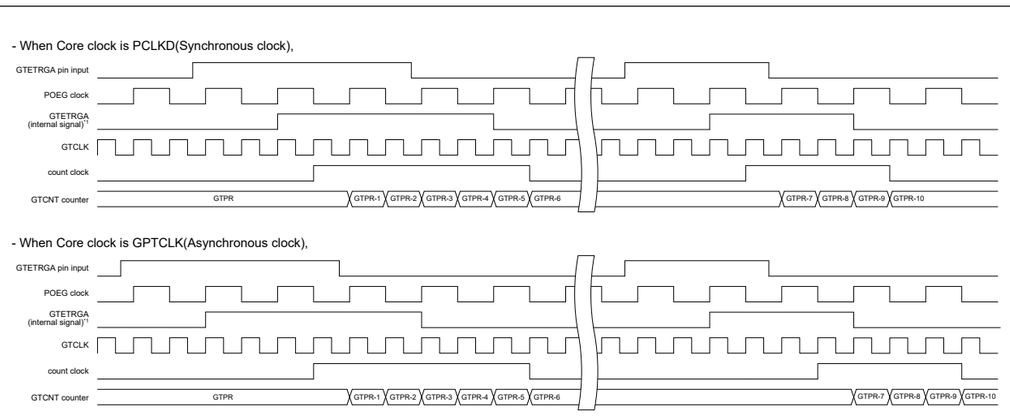
如果同时开启相位计数功能和脉宽测量功能，则脉宽测量功能不起作用，相位计数功能起作用。

图21.129、图21.130显示了外部脉冲宽度测量功能的示例，表21.61显示了设置外部脉冲宽度测量功能的示例。



Note: POEG clock: PCLKB
Note 1. The input signal to GPT when the digital noise filter of GTETRGA pin is not used in POEG is shown.

Figure 21.129 Example of External pulse width measuring function(Up-counting)

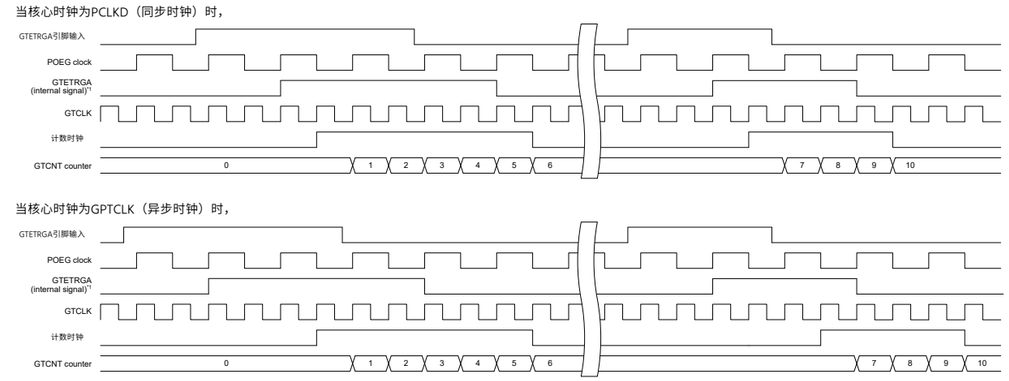


Note: POEG clock: PCLKB
Note 1. The input signal to GPT when the digital noise filter of GTETRGA pin is not used in POEG is shown.

Figure 21.130 Example of External pulse width measuring function(Down-counting)

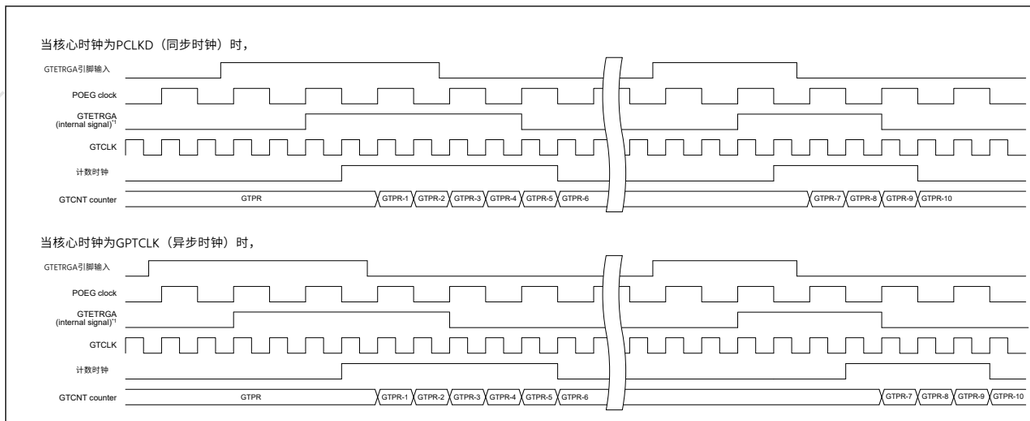
Table 21.61 Example for Setting External pulse width measuring function

No.	Step Name	Description
1	Set external pulse width measuring function	Enable external pulse width measuring function with the GTUPSR.USILVL[3:0] bits for up-counting operation and the GTDNSR.DSILVL[3:0] bits for down-counting operation and select the input pin and level to measure. In Figure 21.129, GTUPSR.USILVL[3:0] = 1001b (count up when GTETRGA pin is 1), In Figure 21.130, GTDNSR.DSILVL[3:0] = 1001b (count down when GTETRGA pin is 1)
2	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits of the corresponding channel.
3	Set cycle	Set the cycle in GTPR of the corresponding channel.
4	Set initial value for counter	Set the initial value in the GTCNT counter of the corresponding channel. In Figure 21.129, 0000 0000h is set. In Figure 21.130, the GTPR register value is set.
5	Start count operation	Input a pulse to the input pin to be measured to start count operation.



Note: POEG clock: PCLKB
注1.显示在POEG中未使用GTETRGA引脚的数字噪声滤波器时GPT的输入信号。

图21.129外部脉冲宽度测量功能示例（递增计数）



Note: POEG clock: PCLKB
注1.显示在POEG中未使用GTETRGA引脚的数字噪声滤波器时GPT的输入信号。

图21.130外部脉冲宽度测量功能示例（递减计数）

Table 21.61 设置外部脉冲宽度测量功能示例

No.	步骤名称	Description
1	设置外部脉宽测量功能	使用GTUPSR.USILVL[3:0]位启用外部脉冲宽度测量功能进行向上计数操作和GTDNSR.DSILVL[3:0]位进行向下计数操作，并选择要测量的输入引脚和电平。在图21.129中，GTUPSR.USILVL[3:0]=1001b（GTETRGA引脚为1时向上计数）， 在图21.130中，GTDNSR.DSILVL[3:0]=1001b（GTETRGA引脚为1时倒计时）
2	选择计数时钟	用相应通道的GTCR.TPCS[3:0]位选择计数时钟。
3	设置周期	在相应通道的GTPR中设置循环。
4	设置计数器的初始值	在相应通道的GTCNT计数器中设置初始值。 在图21.129中，设置了00000000h。在图21.130中，设置了GTPR寄存器值。
5	开始计数操作	向要测量的输入引脚输入一个脉冲以开始计数操作。

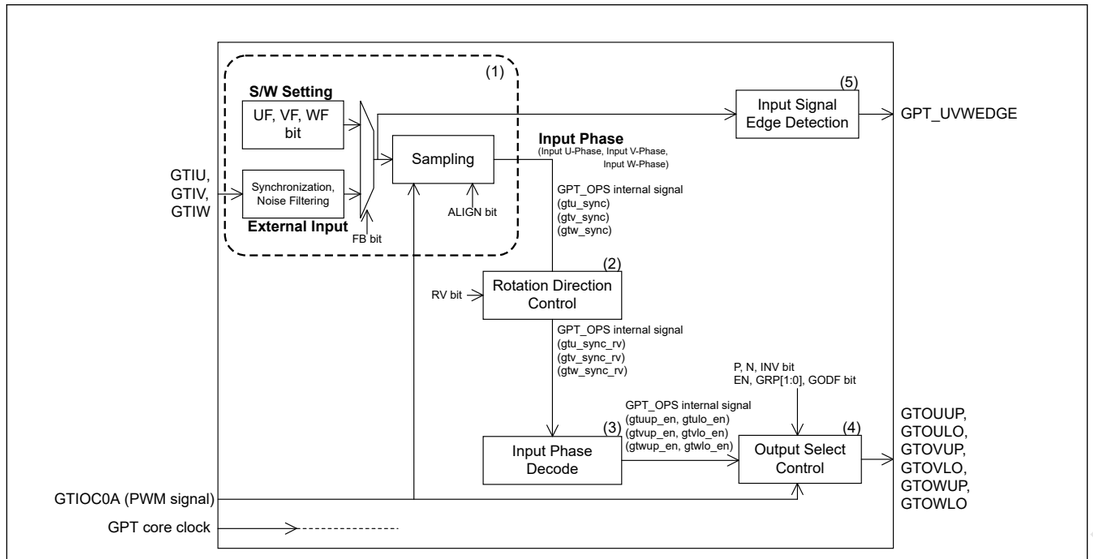
21.3.13 Output Phase Switching (GPT_OPS)

GPT_OPS can easily control Brushless DC motor using Output Phase Switching Control Register (OPSCR).

GPT_OPS uses S/W setting value (OPSCR.UF, VF, WF bits) or external signals detected by the Hall element as input signals. GPT_OPS outputs either level signals or chopped signals by GPT320's PWM as the 6-phase (U-positive phase / negative phase, V-positive phase / negative phase, W-positive phase / negative phase) signals to control motor.

Figure 21.131 shows the block diagram of GPT_OPS.

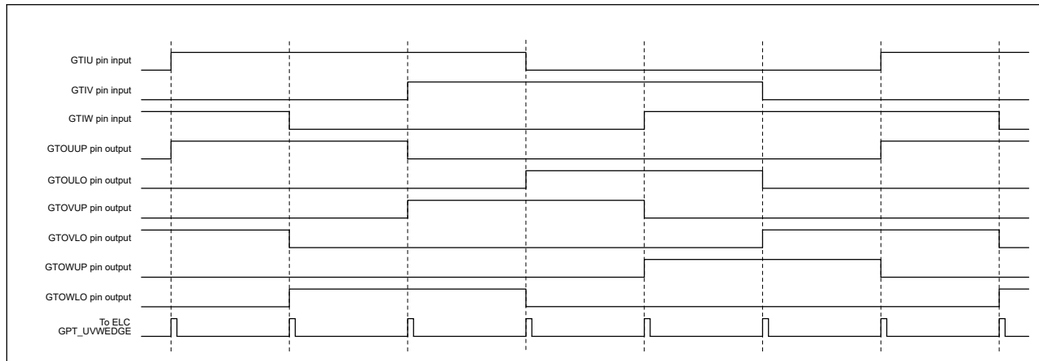
The GPT_UVWEDGE signal is output signal to ELC generated by detecting the edge of input signal.



Note: GPT core clock: GTCLK (PCLKD or GPTCLK)

Figure 21.131 GPT_OPS Block Diagram

Figure 21.132 and Figure 21.133 show examples of GPT_OPS level output operation.



Note: Register settings: OPSCR.FB = 0, OPSCR.RV = 0, OPSCR.P = 0, OPSCR.N = 0, OPSCR.INV = 0

Figure 21.132 Example of GPT_OPS Level Output Operation (Forward Rotation)

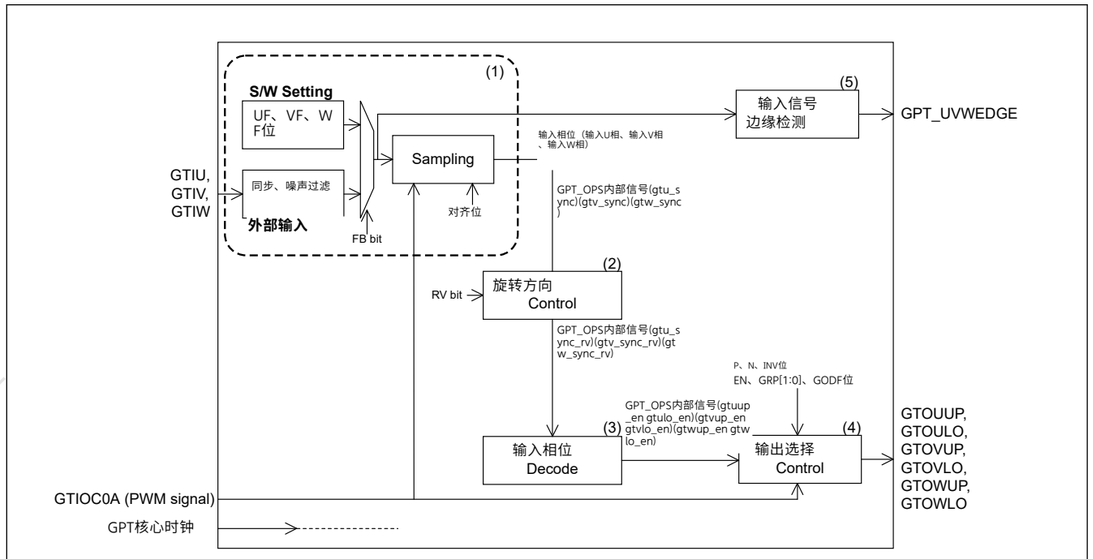
21.3.13 输出相位切换(GPT_OPS)

GPT_OPS可以使用输出相位切换控制寄存器(OPSCR)轻松控制无刷直流电机。

GPT_OPS使用SW设置值（OPSCR.UF、VF、WF位）或霍尔元件检测到的外部信号作为输入信号。GPT_OPS通过GPT320的PWM输出电平信号或斩波信号作为6相（U正相负相，V正相负相，W正相负相）信号来控制电机。

图21.131显示了GPT_OPS的框图。

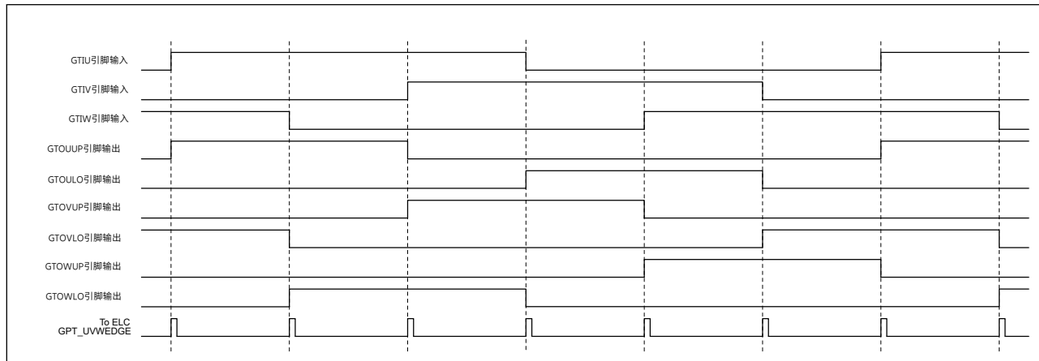
GPT_UVWEDGE信号是对ELC的输出信号，通过检测输入信号的边沿产生。



Note: GPT内核时钟：GTCLK（PCLKD或GPTCLK）

图21.131GPT_OPS框图

图21.132和图21.133显示了GPT_OPS级别输出操作的示例。



Note: Register settings: OPSCR.FB = 0, OPSCR.RV = 0, OPSCR.P = 0, OPSCR.N = 0, OPSCR.INV = 0

图21.132GPT_OPS电平输出操作示例（正向旋转）

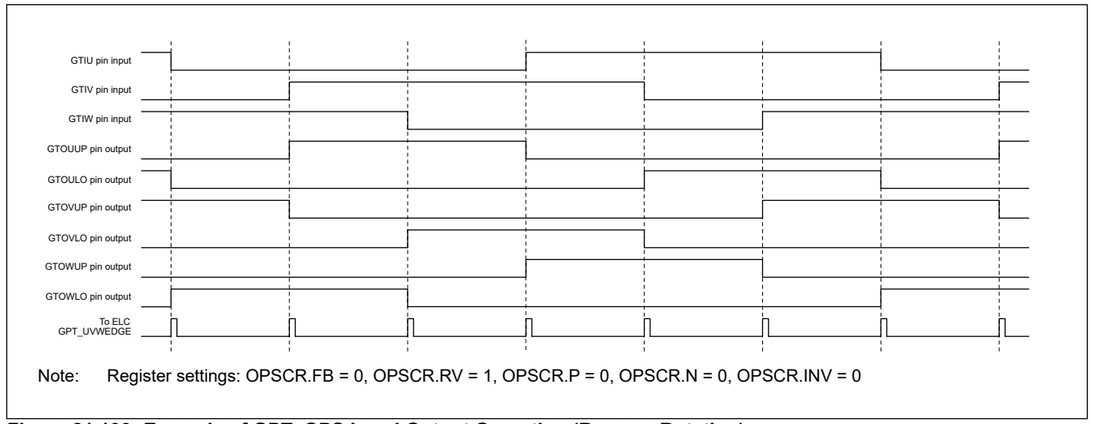


Figure 21.133 Example of GPT_OPS Level Output Operation (Reverse Rotation)

Figure 21.134 and Figure 21.135 show examples of GPT_OPS chopped output operation.

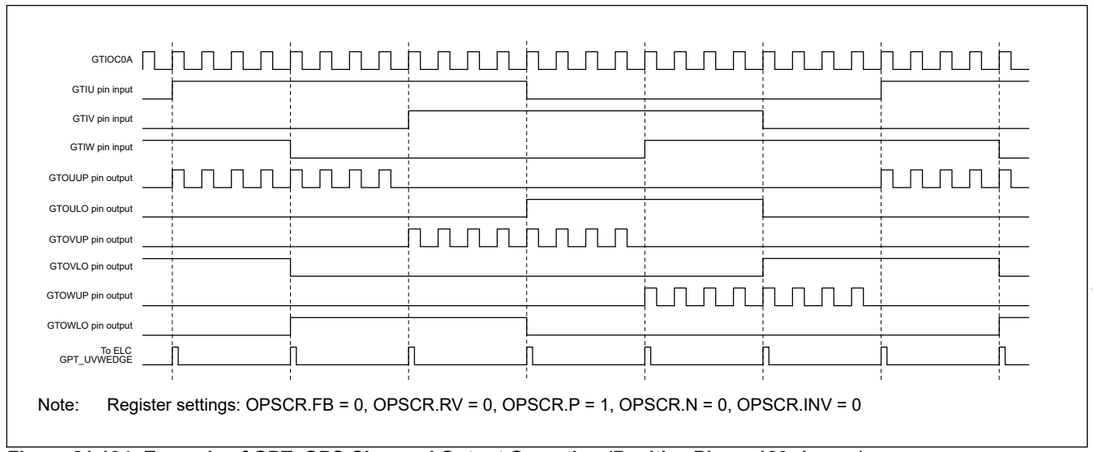


Figure 21.134 Example of GPT_OPS Chopped Output Operation (Positive Phase 120-degree)

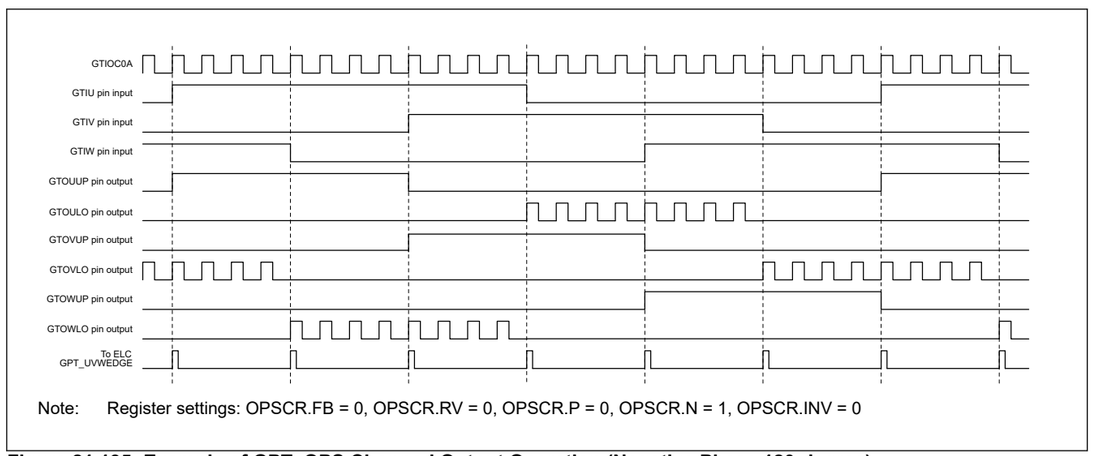


Figure 21.135 Example of GPT_OPS Chopped Output Operation (Negative Phase 120-degree)

Figure 21.136 shows an example of GPT_OPS output disable control operation.

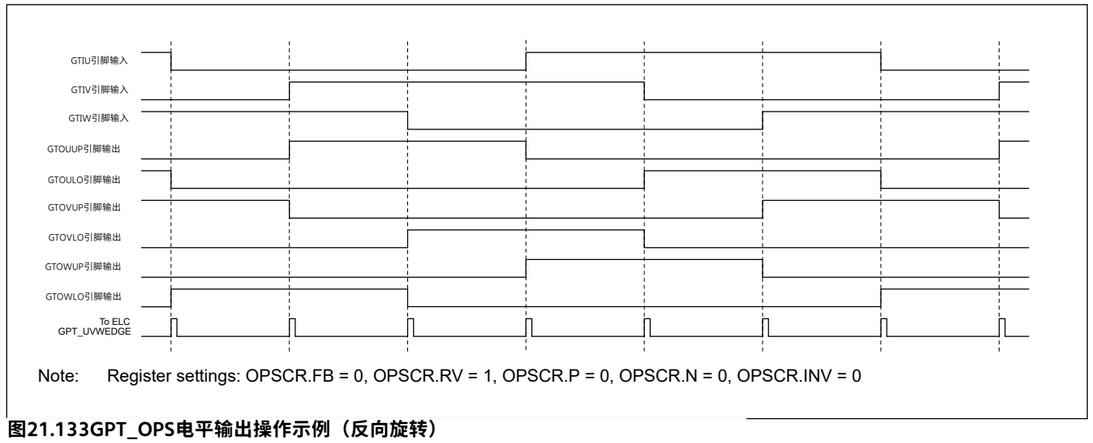


图21.133GPT_OPS电平输出操作示例（反向旋转）

图21.134和图21.135显示了GPT_OPS斩波输出操作的示例。

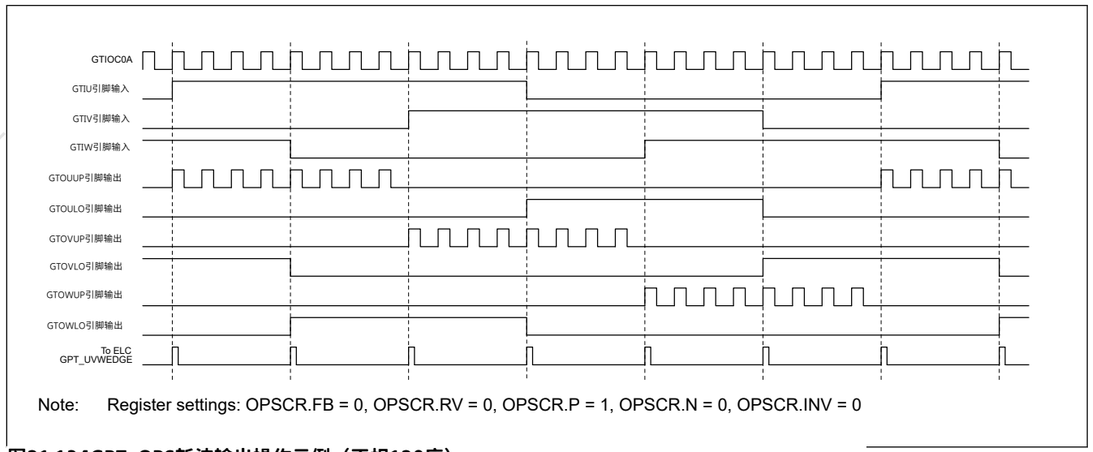


图21.134GPT_OPS斩波输出操作示例（正相120度）

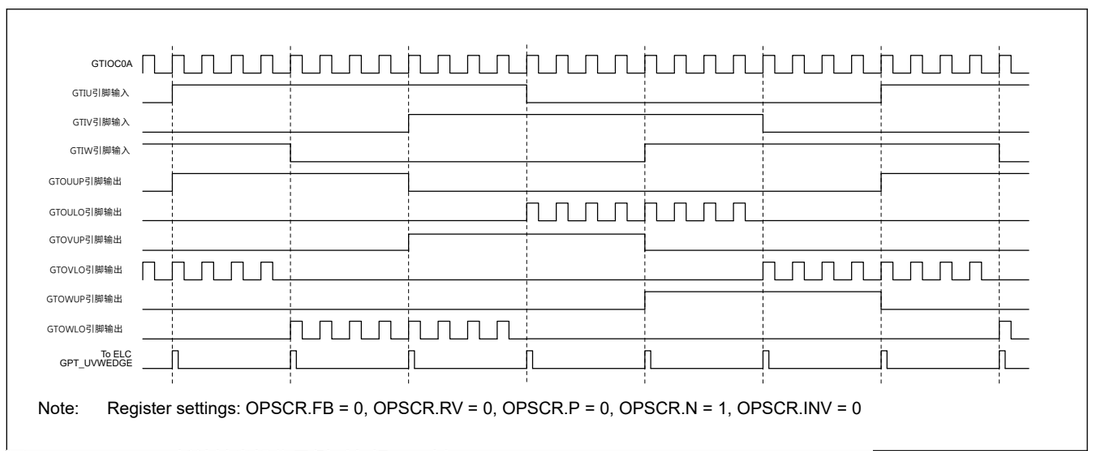


图21.135GPT_OPS斩波输出操作示例（负相120度）

图21.136显示了GPT_OPS输出禁用控制操作的示例。

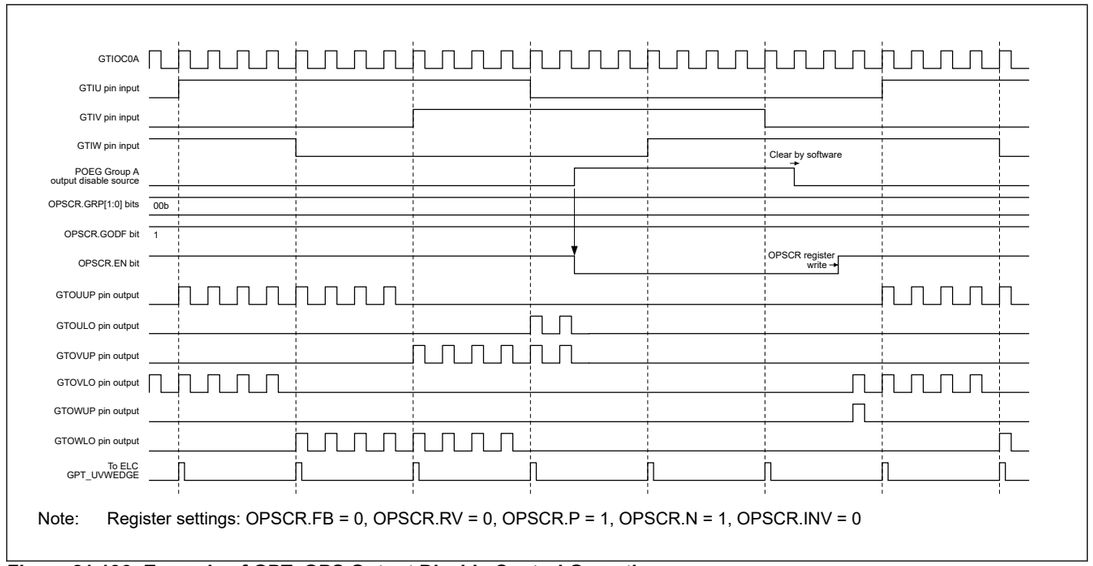


Figure 21.136 Example of GPT_OPS Output Disable Control Operation

21.3.13.1 Input Selection and Sampling

The FB bit selects either the software setting value or external input for the input signal.

When the FB bit is 0, the GTIU, GTIV, GTIW external input are selected for the input signal to GPT_OPS after synchronization with the GPT core clock (GTCLK) and noise filtering.

When the FB bit is 1, the software setting value (UF,VF,WF bits) are selected for the input signal to GPT_OPS.

The selected input signals are sampled by the method selected by the ALIGN bit, and they are treated as input phase of GPT_OPS.

When the ALIGN bit is 0, the input signals are sampled by GTCLK.

When the ALIGN bit is 1, the input signals are sampled by the falling edge of GTIOC0A pin output.

The signals after sampling can be read by the U, V, W bits.

Table 21.62 shows the input selection by the FB bit and sampling method by the ALIGN bit.

Table 21.62 Input Selection and Sampling Method

OPSCR Register		Input Selection Sampling Method	Input Phase (GPT_OPS internal signal)
FB bit	ALIGN bit		
0	0	GTIU, GTIV, GTIW external input GTCLK sampling	Input U-phase (gtu_sync) Input V-phase (gtv_sync) Input W-phase (gtw_sync)
	1	GTIU, GTIV, GTIW external input GTIOC0A falling edge sampling	
1	0	Software setting value UF, VF, WF bits GTCLK sampling	
	1	Software setting value UF, VF, WF bits GTIOC0A falling edge sampling	

21.3.13.2 Rotation Direction Control

When the rotation direction is reverse (RV bit = 1), the input phase is inverted.

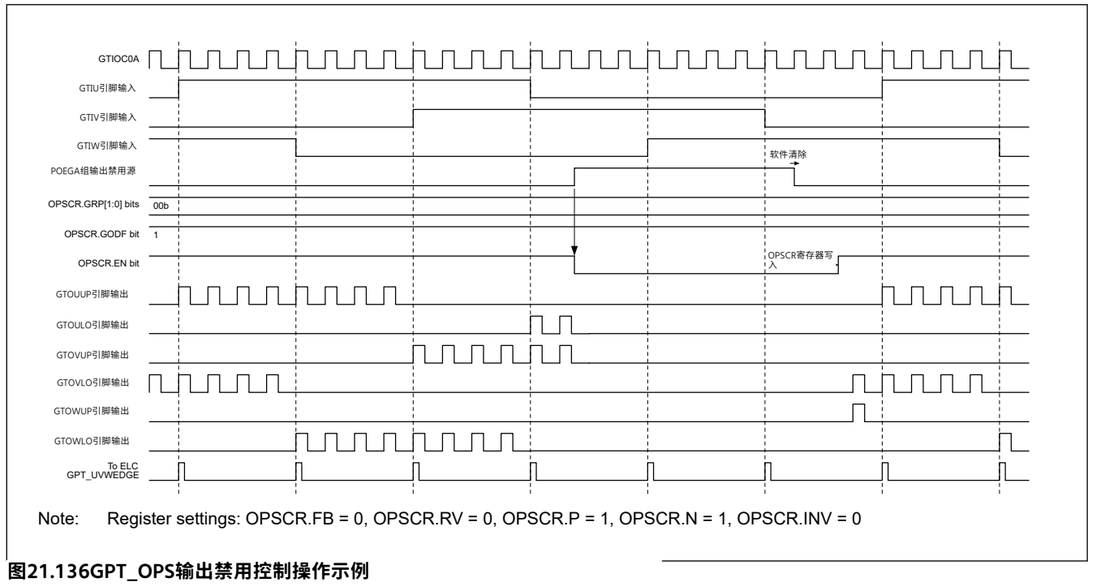


图21.136GPT_OPS输出禁用控制操作示例

21.3.13.1 输入选择和采样

FB位选择输入信号的软件设置值或外部输入。

当FB位为0时，在与GPT内核时钟(GTCLK)同步和噪声过滤后，选择GTIU、GTIV、GTIW外部输入作为GPT_OPS的输入信号。

当FB位为1时，为GPT_OPS的输入信号选择软件设置值（UF、VF、WF位）。

选择的输入信号按照ALIGN位选择的方法进行采样，并将它们视为输入相位GPT_OPS.

当ALIGN位为0时，输入信号由GTCLK采样。

当ALIGN位为1时，输入信号在GTIOC0A引脚输出的下降沿采样。

采样后的信号可以通过U、V、W位读取。

表21.62显示了FB位的输入选择和ALIGN位的采样方法。

Table 21.62 输入选择和采样方法

OPSCR Register		输入选择 抽样方法	输入相位（GPT_OPS内部信号）
FB bit	对齐位		
0	0	GTIU、GTIV、GTIW外部输入 GTCLK sampling	Input U-phase (gtu_sync) Input V-phase (gtv_sync) Input W-phase (gtw_sync)
	1	GTIU、GTIV、GTIW外部输入GTIOC0A下降沿采样	
1	0	软件设定值UF、VF、WF位 GTCLK sampling	
	1	软件设定值UF、VF、WF位 GTIOC0A下降沿采样	

21.3.13.2 旋转方向控制

当旋转方向为反向时（RV位=1），输入相位反转。

21.3.13.3 Input phase decode

The 6-phase signals by decoding input phase after rotation direction control are generated.

Table 21.63 and Table 21.64 show the decode tables of input phase to rotate motor in forward (RV = 0) and reverse (RV = 1).

Table 21.63 The Decode Table of Input Phase (Forward Rotation)

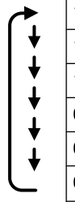
	Input Phase			Input Phase after Rotation Direction Control			6-Phase Signals					
	U Phase	V Phase	W Phase	U Phase	V Phase	W Phase	U Positive Phase	U Negative Phase	V Positive Phase	V Negative Phase	W Positive Phase	W Negative Phase
	gtu_sync	gtv_sync	gtw_sync	gtu_sync_rv	gtv_sync_rv	gtw_sync_rv	gtuup_en	gtulo_en	gtvup_en	gtvlo_en	gtwup_en	gtwlo_en
	1	0	1	1	0	1	1	0	0	1	0	0
	1	0	0	1	0	0	1	0	0	0	0	1
	1	1	0	1	1	0	0	0	1	0	0	1
	0	1	0	0	1	0	0	1	1	0	0	0
	0	1	1	0	1	1	0	1	0	0	1	0
	0	0	1	0	0	1	0	0	0	1	1	0
	0	0	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	0	0	0	0	0	0

Table 21.64 The Decode Table of Input Phase (Reverse Rotation)

	Input Phase			Input Phase after Rotation Direction Control			6-Phase Signals					
	U Phase	V Phase	W Phase	U Phase	V Phase	W Phase	U Positive Phase	U Negative Phase	V Positive Phase	V Negative Phase	W Positive Phase	W Negative Phase
	gtu_sync	gtv_sync	gtw_sync	gtu_sync_rv	gtv_sync_rv	gtw_sync_rv	gtuup_en	gtulo_en	gtvup_en	gtvlo_en	gtwup_en	gtwlo_en
	1	0	1	0	1	0	0	1	1	0	0	0
	1	0	0	0	1	1	0	1	0	0	1	0
	1	1	0	0	0	1	0	0	0	1	1	0
	0	1	0	1	0	1	1	0	0	1	0	0
	0	1	1	1	0	0	1	0	0	0	0	1
	0	0	1	1	1	0	0	0	1	0	0	1
	0	0	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	0	0	0	0	0	0

21.3.13.4 Output selection control

The EN, P, N, INV bits select the output wave.

The EN bit enables output of the 6-phase output. When the EN bit is 1, output of the 6-phase output is enabled. When the EN bit is 0, the external pin output is Hi-Z.

The P, N bits select whether chopping positive and negative phase are performed or not. When P, N bits are 1, chopping is performed by GTIOC0A pin output.

When the chopping is performed, there are cases where the PWM width of output is shorter than the width of the PWM used to chop just before or after switching of output phase, depending on the phase difference between the phase output switch timing and the phase of PWM.

The INV bit selects the polarity (either positive logic or negative logic) of phase output.

21.3.13.3 输入相位解码

旋转方向控制后通过解码输入相位生成6相信号。

表21.63和表21.64显示了电机正转(RV=0)和反转(RV=1)的输入相位解码表。

Table 21.63 输入相位解码表（正向旋转）

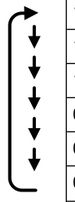
	输入相位			旋转后的输入相位方向控制			6-Phase Signals					
	U Phase	V Phase	W Phase	U Phase	V Phase	W Phase	U Positive Phase	U Negative Phase	V Positive Phase	V Negative Phase	W Positive Phase	W Negative Phase
	gtu_sync	gtv_sync	gtw_sync	gtu_sync_rv	gtv_sync_rv	gtw_sync_rv	gtuup_en	gtulo_en	gtvup_en	gtvlo_en	gtwup_en	gtwlo_en
	1	0	1	1	0	1	1	0	0	1	0	0
	1	0	0	1	0	0	1	0	0	0	0	1
	1	1	0	1	1	0	0	0	1	0	0	1
	0	1	0	0	1	0	0	1	1	0	0	0
	0	1	1	0	1	1	0	1	0	0	1	0
	0	0	1	0	0	1	0	0	0	1	1	0
	0	0	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	0	0	0	0	0	0

Table 21.64 输入相位解码表（反转）

	输入相位			旋转后的输入相位方向控制			6-Phase Signals					
	U Phase	V Phase	W Phase	U Phase	V Phase	W Phase	U Positive Phase	U Negative Phase	V Positive Phase	V Negative Phase	W Positive Phase	W Negative Phase
	gtu_sync	gtv_sync	gtw_sync	gtu_sync_rv	gtv_sync_rv	gtw_sync_rv	gtuup_en	gtulo_en	gtvup_en	gtvlo_en	gtwup_en	gtwlo_en
	1	0	1	0	1	0	0	1	1	0	0	0
	1	0	0	0	1	1	0	1	0	0	1	0
	1	1	0	0	0	1	0	0	0	1	1	0
	0	1	0	1	0	1	1	0	0	1	0	0
	0	1	1	1	0	0	1	0	0	0	0	1
	0	0	1	1	1	0	0	0	1	0	0	1
	0	0	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	0	0	0	0	0	0

21.3.13.4 输出选择控制

EN、P、N、INV位选择输出波形。

EN位使能6相输出的输出。EN位为1时，使能6相输出。当。。。的时候
EN位为0，外部引脚输出为Hi-Z。

P、N位选择是否执行斩波正相和反相。当P、N位为1时，由GTIOC0A引脚输出进行斩波。

进行斩波时，输出的PWM宽度有时会比输出相位切换前后的斩波宽度短，这取决于相位输出切换时序和相位之间的相位差。脉宽调制。

INV位选择相位输出的极性（正逻辑或负逻辑）。

Table 21.65 and Table 21.66, show the output selection control method for positive and negative phase output.

Table 21.65 Output Selection Control Method (Positive Phase)

EN bit	P bit	INV bit	GTOUUP / GTOVUP / GTOWUP
0	x	x	0 (External pin output is Hi-Z)
1	0	0	Positive logic level output (gtuup_en) (gtvup_en) (gtwup_en)
1	0	1	Negative logic level output (~gtuup_en) (~gtvup_en) (~gtwup_en)
1	1	0	Positive logic chopped output (GTIOC0A & gtuup_en) (GTIOC0A & gtvup_en) (GTIOC0A & gtwup_en)
1	1	1	Negative logic chopped output (~(GTIOC0A & gtuup_en)) (~(GTIOC0A & gtvup_en)) (~(GTIOC0A & gtwup_en))

Table 21.66 Output Selection Control Method (Negative Phase)

EN bit	N bit	INV bit	GTOULO / GTOVLO / GTOWLO
0	x	x	0 (External pin output is Hi-Z)
1	0	0	Positive logic level output (gtulo_en) (gtvlo_en) (gtwlo_en)
1	0	1	Negative logic level output (~gtulo_en) (~gtvlo_en) (~gtwlo_en)
1	1	0	Positive logic chopped output (GTIOC0A & gtulo_en) (GTIOC0A & gtvlo_en) (GTIOC0A & gtwlo_en)
1	1	1	Negative logic chopped output (~(GTIOC0A & gtulo_en)) (~(GTIOC0A & gtvlo_en)) (~(GTIOC0A & gtwlo_en))

21.3.13.5 Output Selection Control (Group Output Disable Function)

When GODF = 1 and signal value selected by the GRP bit is Hi (Output Disable Request), GPT_OPS's output pins are changed to Hi-Z asynchronously and the OPSCR.EN bit is cleared to 0 by the output disable request signal synchronized with GTCLK.

For the return, after clearing the Output Disable Request by software, please set the EN = 1.

The timing of EN bit cleared to 0 is 3 GTCLK cycles after generating the output disable request. In order to perform the output disable control surely, the output disable request flag in POEG should be cleared in the timing that terminating the output disable request is at least 4 GTCLK cycles after generating the output disable request.

The example of the operation of the group output disable control, please refer to the above-mentioned Figure 21.136.

21.3.13.6 Event Link Controller (ELC) Output

The logical sum of the pulse detected by rising and falling edge of U, V, W phase input is output to the event link controller (ELC). When the high level period of input phase is short, there are cases that the detected edge is not transmitted to the ELC correctly because of the logical sum.

表21.65和表21.66显示了正反相输出的输出选择控制方法。

Table 21.65 输出选择控制方式（正相）

EN位	P bit	INV位	GTOUUP / GTOVUP / GTOWUP
0	x	x	0（外部引脚输出为Hi-Z）
1	0	0	正逻辑电平输出(gtuup_en)(gtvup_en)(gtwup_en)
1	0	1	负逻辑电平输出(~gtuup_en)(~gtvup_en)(~gtwup_en)
1	1	0	正逻辑斩波输出(GTIOC0A&gtuup_en)(GTIOC0A&gtvup_en)(GTIOC0A&gtwup_en)
1	1	1	负逻辑斩波输出(~(GTIOC0A&gtuup_en))(~(GTIOC0A&gtvup_en))(~(GTIOC0A&gtwup_en))

Table 21.66 输出选择控制方式（负相）

EN位	N bit	INV位	GTOULO / GTOVLO / GTOWLO
0	x	x	0（外部引脚输出为Hi-Z）
1	0	0	正逻辑电平输出(gtulo_en)(gtvlo_en)(gtwlo_en)
1	0	1	负逻辑电平输出(~gtulo_en)(~gtvlo_en)(~gtwlo_en)
1	1	0	正逻辑斩波输出(GTIOC0A&gtulo_en)(GTIOC0A&gtvlo_en)(GTIOC0A&gtwlo_en)
1	1	1	负逻辑斩波输出(~(GTIOC0A&gtulo_en))(~(GTIOC0A&gtvlo_en))(~(GTIOC0A&gtwlo_en))

21.3.13.5 输出选择控制（组输出禁用功能）

当GODF=1且GRP位选择的信号值为Hi(OutputDisableRequest)时，GPT_OPS的输出引脚异步更改为Hi-Z并且OPSCR.EN位通过与GTCLK同步的输出禁用请求信号清零。

返回时，请在软件清除OutputDisableRequest后，设置EN=1。

EN位清0的时间是产生输出禁止请求后的3个GTCLK周期。为了可靠地执行输出禁用控制，POEG中的输出禁用请求标志应在产生输出禁用请求后至少4个GTCLK周期终止输出禁用请求的时序中清除。

组输出禁用控制的操作示例，请参考上述图21.136。

21.3.13.6 事件链接控制器(ELC)输出

通过U、V、W相输入的上升沿和下降沿检测到的脉冲的逻辑和输出到事件链接控制器(ELC)。当输入相的高电平周期较短时，检测到的边沿有时会因为逻辑和而不能正确传输到ELC。

21.3.13.7 GPT_OPS Start Operation Setting Flow

Table 21.67 Example for Setting of GPT_OPS Start Operation

No.	Step Name	Description
1	Set Operation Mode of GPT320	Set the PWM output operation mode of GPT320. refer to section 21.3.3. PWM Output Operating Mode
2	Start Count Operation of GTP320	Start count operation of GPT320, and outputs PWM waveform.
3	Set GPT_OPS Input Condition	• When the soft setting is selected, set the soft setting values in the UF, VF, WF bits. • When the external input is selected, if necessary, use noise filtering. Select the sampling clock for external input into NFCS[1:0] bits, and set NFEN bit to 1.
4	Select GPT_OPS Input phase and Alignment	Select input phase by FB bit. Select alignment of input phase by ALIGN bit.
5	Set GPT_OPS Output phase Condition	Set the rotation direction by RV bit. Select whether chopping is performed or not by P, N bits. Select the output polarity by INV bit.
6	Set GPT_OPS Output Disable Condition	Select the error group by GRP[1:0] bits Set ON/OFF of the group output disable function by GODF bit.
7	Set GPT_OPS Operation	Set EN bit to 1 to output the 6-phase output to drive the brushless DC motor.

21.3.14 Inter Channel Logical Operation Function

The logical operation function between compare match outputs can be performed.

Figure 21.137 shows the block diagram of inter channel logical operation.

To prevent hazard to the GPT output, the signal after logical operation is latched with GTCLK. After latching, the output disable control is performed.

When the logical operation function which causes the delay of 1 GTCLK is selected, the output enable signal is also delayed with 1 GTCLK and input to the output disable control.

When the same signal (C = A or D = B) to operate logical function AND, OR, EXOR and NOR is selected, C or D is treated as 1. In the case of GTIOCnA pin output, when A of same channel is selected for C, the result of AND is A, the result of OR is 1, the result of EXOR is NOT A, and the result of NOR is 0.

21.3.13.7 GPT_OPS启动操作设置流程

Table 21.67 GPT_OPS启动操作设置示例

No.	步骤名称	Description
1	设置GPT320的操作模式	设置GPT320的PWM输出操作模式。 请参阅第21.3.3节。PWM输出工作模式
2	开始计数操作 GTP320	开始GPT320的计数操作，并输出PWM波形。
3	设置GPT_OPS输入条件	• 选择软设置时，在UF、VF、WF位中设置软设置值。 • Whentheexternalinputisselected ifnecessary usenoisefiltering.选择外部输入的采样时钟到NFCS[1:0]位，并将NFEN位设置为1。
4	选择GPT_OPS输入相位和对齐	通过FB位选择输入相位。通过ALIGN位选择输入相位的对齐方式。
5	设置GPT_OPS输出相位 Condition	通过RV位设置旋转方向。通过P、N位选择是否进行斩波 。 通过INV位选择输出极性。
6	设置GPT_OPS输出禁用 Condition	通过GRP[1:0]位选择错误组 通过GODF位设置组输出禁用功能的ONOFF。
7	设置GPT_OPS操作	将EN位设置为1，输出6相输出以驱动无刷直流电机。

21.3.14 通道间逻辑运算功能

可以执行比较匹配输出之间的逻辑运算功能。

图21.137显示了通道间逻辑操作的框图。

为防止对GPT输出造成危害，逻辑运算后的信号由GTCLK锁存。锁存后，执行输出禁用控制。

Whenthelogicaloperationfunctionwhichcausesthedelayof1GTCLKisselected theoutputenablesignalisalsodelayed with1GTCLKandinputtotheoutputdisablecontrol.

Whenthesamesignal(C=AorD=B)tooperatelogicalfunctionAND OR EXORandNORisselected CorDistreatedas1.Inthe caseofGTIOCnApinoutput whenAofsamechannelisselected对于C，AND的结果是A，OR的结果是1，EXOR的结果是NOTA，NOR的结果是0。

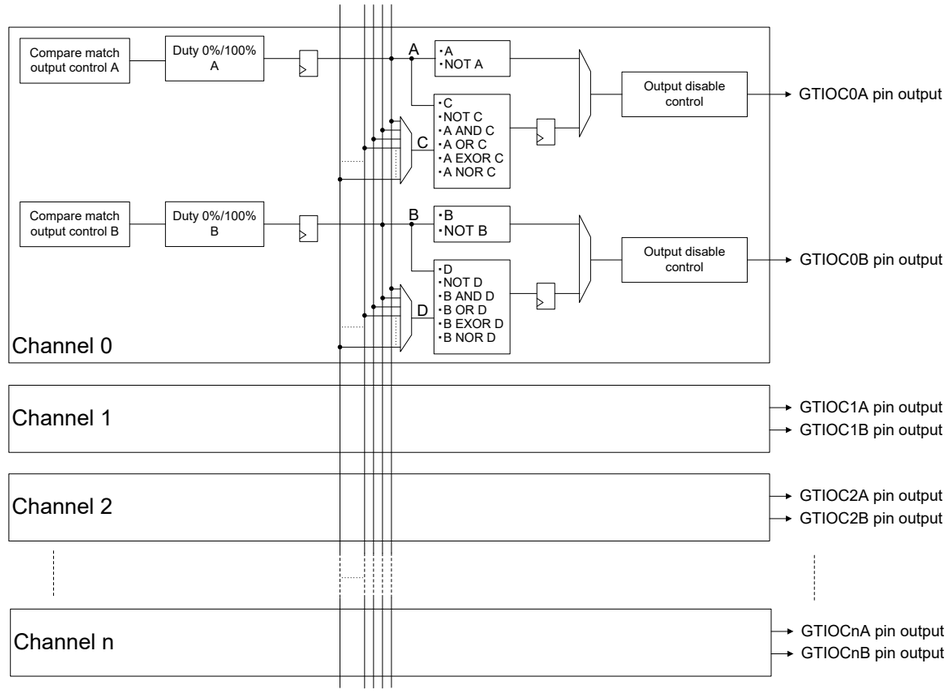


Figure 21.137 Block Diagram of Inter Channel Logical Operation

Figure 21.138 shows an example of inter channel logical operation.

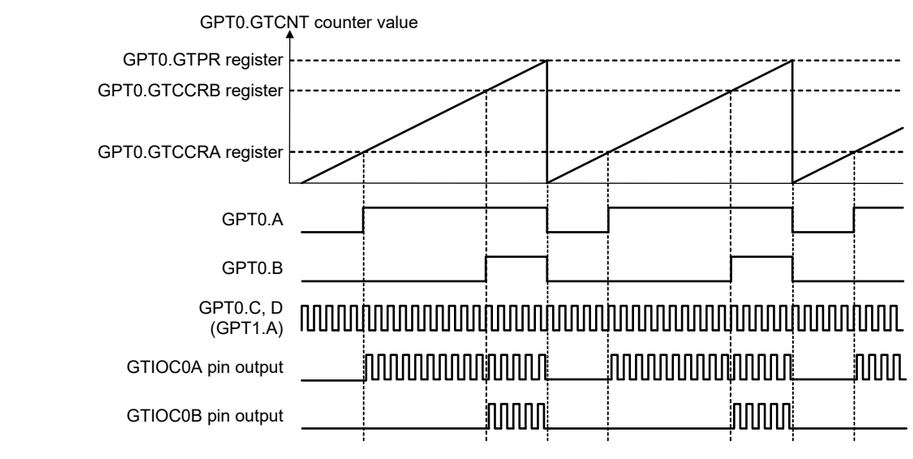


Figure 21.138 Example of Inter Channel Logical Operation

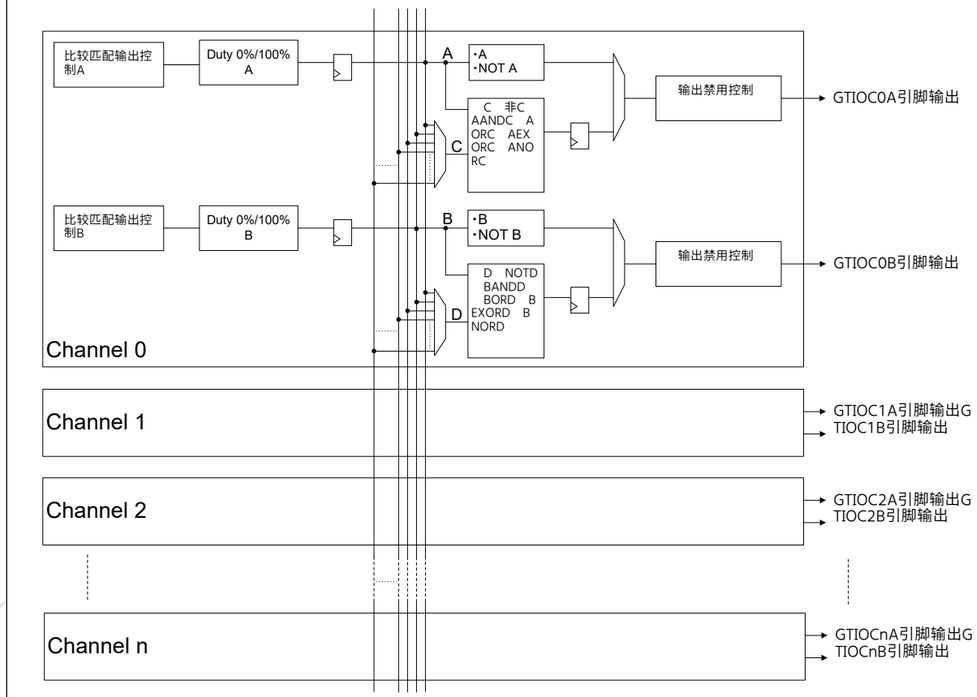


图21.137通道间逻辑操作框图

图21.138显示了通道间逻辑操作的示例。

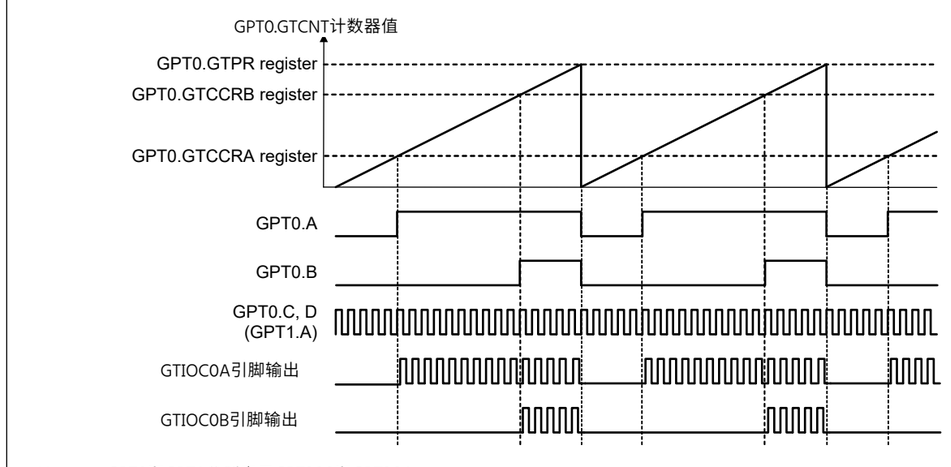


图21.138通道间逻辑操作示例

21.4 Interrupt Sources

21.4.1 Interrupt Sources

The GPT provides the following interrupt sources:

- GTCCR input capture/compare match
- GTADTR compare match
- GTCNT counter overflow (GTPR compare match)/underflow.
- period count function finish

Each interrupt source has its own status flag. When an interrupt source signal is generated, the associated status flag in GTST is set to 1, and an interrupt request is generated. The associated status flag in GTST can be cleared by writing 0. If flag set and flag clear occur at the same time, flag clear takes priority over flag set. These flags are automatically updated by the internal state. The Interrupt Controller Unit can change the relative channel priorities. However, the priority within a channel is fixed. For details, see section 12, Interrupt Controller Unit (ICU).

Table 21.68 lists the GPT interrupt sources.

Table 21.68 Interrupt sources

Channel	Name	Interrupt source	Interrupt flag	DTC activation
n = 0 to 9	GPTn_CCMPA	GPT32n.GTCCRA input capture/compare match	GTST[0] (TCFA)	Possible
	GPTn_CCMPB	GPT32n.GTCCRB input capture/compare match	GTST[1] (TCFB)	Possible
	GPTn_CMPC	GPT32n.GTCCRC compare match	GTST[2] (TCFC)	Possible
	GPTn_CMPD	GPT32n.GTCCRD compare match	GTST[3] (TCFD)	Possible
	GPTn_CMPE	GPT32n.GTCCRE compare match	GTST[4] (TCFE)	Possible
	GPTn_CMPF	GPT32n.GTCCRF compare match	GTST[5] (TCFF)	Possible
	GPTn_OVF	GPT32n.GTCNT overflow (GPT32n.GTPR compare match)	GTST[6] (TCFPO)	Possible
	GPTn_UDF	GPT32n.GTCNT underflow	GTST[7] (TCFPU)	Possible
	GPTn_ADTRGA	GPT32n.GTADTRA compare match	GTST[17:16] (ADTRADF, ADTRAUF)	Possible
	GPTn_ADTRGB	GPT32n.GTADTRB compare match	GTST[19:18] (ADTRBDF, ADTRBUF)	Possible
	GPTn_PC	Period count function finish (n = 0 to 3)	GTST[31] (PCF)	Possible

(1) GPTn_CCMPA interrupt (n = 0 to 9)

An interrupt request is generated under the following conditions:

- When the GTCCRA register functions as a compare match register, the GTCNT counter value (in complementary PWM mode, the GTCNT counter value of master channel) matches with the GTCCRA register
- When the GTCCRA register functions as an input capture register, the input-capture signal causes transfer of the GTCNT counter value to the GTCCRA register. In complementary PWM mode, GTCCRA register does not function as an input capture register.

(2) GPTn_CCMPB interrupt (n = 0 to 9)

An interrupt request is generated under the following conditions:

- When the GTCCRB register functions as a compare match register, the GTCNT counter value matches with the GTCCRB register. In complementary PWM mode, GTCCRB register does not function as a compare match register.
- When the GTCCRB register functions as an input capture register, the input-capture signal causes transfer of the GTCNT counter value to the GTCCRB register. In complementary PWM mode, GTCCRB register does not function as an input capture register.

21.4 中断源

21.4.1 中断源

GPT提供以下中断源：

●GTCCR输入捕捉比较匹配

●GTADTR比较匹配

●GTCNT计数器上溢（GTPR比较匹配）下溢。

●周期计数功能完成

每个中断源都有自己的状态标志。当一个中断源信号产生时，相关的状态标志在GTST设置为1，并产生中断请求。GTST中相关的状态标志可以通过写入0来清除。如果标志设置和标志清除同时发生，标志清除优先于标志设置。这些标志由内部状态自动更新。中断控制器单元可以改变相关的通道优先级。但是，通道内的优先级是固定的。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

表21.68列出了GPT中断源。

Table 21.68 中断源

Channel	Name	中断源	中断标志	DTC activation
n = 0 to 9	GPTn_CCMPA	GPT32n.GTCCRA输入捕捉比较匹配	GTST[0] (TCFA)	Possible
	GPTn_CCMPB	GPT32n.GTCCRB输入捕捉比较匹配	GTST[1] (TCFB)	Possible
	GPTn_CMPC	GPT32n.GTCCRC比较匹配	GTST[2] (TCFC)	Possible
	GPTn_CMPD	GPT32n.GTCCRD比较匹配	GTST[3] (TCFD)	Possible
	GPTn_CMPE	GPT32n.GTCCRE比较匹配	GTST[4] (TCFE)	Possible
	GPTn_CMPF	GPT32n.GTCCRF比较匹配	GTST[5] (TCFF)	Possible
	GPTn_OVF	GPT32n.GTCNT溢出（GPT32n.GTPR比较匹配）	GTST[6] (TCFPO)	Possible
	GPTn_UDF	GPT32n.GTCNT underflow	GTST[7] (TCFPU)	Possible
	GPTn_ADTRGA	GPT32n.GTADTRA比较匹配	GTST[17:16] (ADTRADF, ADTRAUF)	Possible
	GPTn_ADTRGB	GPT32n.GTADTRB比较匹配	GTST[19:18] (ADTRBDF, ADTRBUF)	Possible
	GPTn_PC	周期计数功能完成（n=0到3）	GTST[31] (PCF)	Possible

(1) GPTn_CCMPA中断（n=0到9）

在以下情况下会产生中断请求：

●当GTCCRA寄存器作为比较匹配寄存器时，GTCNT计数器值（互补PWM模式下，主通道的GTCNT计数器值）与GTCCRA寄存器匹配

●当GTCCRA寄存器用作输入捕捉寄存器时，输入捕捉信号会导致传输GTCNT计数器值到GTCCRA寄存器。在互补PWM模式下，GTCCRA寄存器不用作输入捕捉寄存器。

(2) GPTn_CCMPB中断（n=0到9）

在以下情况下会产生中断请求：

●当GTCCRB寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRB寄存器。在互补PWM模式下，GTCCRB寄存器不用作比较匹配寄存器。

●当GTCCRB寄存器用作输入捕捉寄存器时，输入捕捉信号会导致传输GTCNT计数器值到GTCCRB寄存器。在互补PWM模式下，GTCCRB寄存器不用作输入捕捉寄存器。

(3) GPTn_CMPC interrupt (n = 0 to 9)

An interrupt request is generated under the following condition:

- When the GTCCRC register functions as a compare match register, the GTCNT counter value (in complementary PWM mode, GTCNT counter value of master channel) matches with the GTCCRC register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[3:0] = 0001b (saw-wave one-shot pulse mode)
- GTCR.MD[3:0] = 0110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRC register).

(4) GPTn_CMPD interrupt (n = 0 to 9)

An interrupt request is generated under the following condition:

- When the GTCCRD register functions as a compare match register, the GTCNT counter value (in complementary PWM mode, the GTCNT counter value of master channel) matches with the GTCCRD register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[3:0] = 0001b (saw-wave one-shot pulse mode)
- GTCR.MD[3:0] = 0110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (buffer operation with the GTCCRD register).

(5) GPTn_CMPE interrupt (n = 0 to 9)

An interrupt request is generated under the following condition:

- When the GTCCRE register functions as a compare match register, the GTCNT counter value (in complementary PWM mode, the GTCNT counter value of master channel) matches with the GTCCRE register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[3:0] = 0001b (saw-wave one-shot pulse mode)
- GTCR.MD[3:0] = 0110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRE register).

(6) GPTn_CMPF interrupt (n = 0 to 9)

An interrupt request is generated under the following condition:

- When the GTCCRF register functions as a compare match register, the GTCNT counter value (in complementary PWM mode, the GTCNT counter value of master channel) matches with the GTCCRF register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[3:0] = 0001b (saw-wave one-shot pulse mode)
- GTCR.MD[3:0] = 0110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (buffer operation with the GTCCRF register).

(7) GPTn_OVF interrupt (n = 0 to 9)

An interrupt request is generated in the following conditions:

- In saw-wave PWM mode 1 and saw-wave one-shot pulse mode, interrupt requests are enabled at overflows (when the GTCNT counter value changes from GTPR to 0 during up-counting)
- In saw-wave PWM mode 2, interrupt requests are enabled at overflows (GTCNT counter value changes from GTCCRm (m = A to F) register value selected with GTCSR.CSCMSC[2:0] bits to 0) or the time when GTCNT counter value matches GTPR register value.
- In triangle-wave mode, interrupt requests are enabled at crests (the GTCNT changes from GTPR to GTPR-1)

(3) GPTn_CMPC中断（n=0到9）

在以下情况下会产生中断请求：

●当GTCCRC寄存器作为比较匹配寄存器时，GTCNT计数器值（在互补PWM模式下，主通道的GTCNT计数器值）与GTCCRC寄存器匹配。

不执行比较匹配，因此在以下情况下不请求中断：

- GTCR.MD[3:0] = 0001b (saw-wave one-shot pulse mode)
- GTCR.MD[3:0] = 0110b (triangle-wave PWM mode 3)

●GTBER.CCRA[1:0]=01b 10b 11b（使用GTCCRC寄存器进行缓冲操作）。

(4) GPTn_CMPD中断（n=0到9）

在以下情况下会产生中断请求：

●当GTCCRD寄存器作为比较匹配寄存器时，GTCNT计数器值（在互补PWM模式下，主通道的GTCNT计数器值）与GTCCRD寄存器匹配。

不执行比较匹配，因此在以下情况下不请求中断：

- GTCR.MD[3:0] = 0001b (saw-wave one-shot pulse mode)
- GTCR.MD[3:0] = 0110b (triangle-wave PWM mode 3)

●GTBER.CCRA[1:0]=10b 11b（使用GTCCRD寄存器进行缓冲操作）。

(5) GPTn_CMPE中断（n=0到9）

在以下情况下会产生中断请求：

●当GTCCRE寄存器作为比较匹配寄存器时，GTCNT计数器值（在互补PWM模式下，主通道的GTCNT计数器值）与GTCCRE寄存器匹配。

不执行比较匹配，因此在以下情况下不请求中断：

- GTCR.MD[3:0] = 0001b (saw-wave one-shot pulse mode)
- GTCR.MD[3:0] = 0110b (triangle-wave PWM mode 3)

●GTBER.CCRB[1:0]=01b 10b 11b（使用GTCCRE寄存器进行缓冲操作）。

(6) GPTn_CMPF中断（n=0到9）

在以下情况下会产生中断请求：

●当GTCCRF寄存器作为比较匹配寄存器时，GTCNT计数器值（在互补PWM模式下，主通道的GTCNT计数器值）与GTCCRF寄存器匹配。

不执行比较匹配，因此在以下情况下不请求中断：

- GTCR.MD[3:0] = 0001b (saw-wave one-shot pulse mode)
- GTCR.MD[3:0] = 0110b (triangle-wave PWM mode 3)

●GTBER.CCRB[1:0]=10b 11b（使用GTCCRF寄存器进行缓冲操作）。

(7) GPTn_OVF中断（n=0到9）

在以下情况下会产生中断请求：

●在锯齿波PWM模式1和锯齿波单次脉冲模式下，溢出时使能中断请求（当GTCNT计数器值在递增计数期间从GTPR变为0时）

●在锯齿波PWM模式2中，中断请求在溢出（GTCNT计数器值从使用GTCSR.CSCMSC[2:0]位选择的GTCCRm（m=A到F）寄存器值变为0）或GTCNT计数器值与GTPR寄存器值匹配。

●在三角波模式下，在波峰处启用中断请求（GTCNT从GTPR变为GTPR-1）

- In complementary PWM mode, interrupt requests are enabled at crests (GTCNT counter value of master channel changes from GTPR register value to GTPR register value minus 1).
- In counting by hardware sources (include external pulse width measuring function), an overflow (GTCNT changes from GTPR to 0 in up count) has occurred.

(8) GPTn_UDF interrupt (n = 0 to 9)

An interrupt request is generated in the following conditions.

- In saw-wave PWM mode 1 and saw-wave one-shot pulse mode, interrupt requests are enabled at underflows (when the GTCNT counter value changes from 0 to GTPR during down-counting)
- In triangle-wave mode, interrupt requests are enabled at troughs (the GTCNT changes from 0 to 1)
- In complementary PWM mode, interrupt requests are enabled at troughs (GTCNT counter value of master channel changes from 0 to 1).
- In counting by hardware sources (include external pulse width measuring function), underflow (GTCNT changes from 0 to GTPR in down count) has occurred.

About Interrupt signals and interrupt status flags, see section 21.2.16. GTST : General PWM Timer Status Register.

(9) GPTn_ADTRGA interrupt (n = 0 to 9)

When the GTCNT counter value matches with GTADTRA, an interrupt request is generated under the following condition.

- In Up-counting, the interrupt enable bit (ADTRAUEN) in GTINTAD is 1.
- In Down-counting, the interrupt enable bit (ADTRADEN) in GTINTAD is 1.
  In event count operation performing, this interrupt request isn't generated.

(10) GPTn_ADTRGB interrupt (n = 0 to 9)

When the GTCNT counter value matches with GTADTRB, an interrupt is generated under the following condition.

- In Up-counting, the interrupt enable bit (ADTRBUEN) in GTINTAD is 1.
- In Down-counting, the interrupt enable bit (ADTRBDEN) in GTINTAD is 1.
  In event count operation performing, this interrupt request isn't generated.

(11) GPTn_PC Interrupt (n = 0 to 3)

When the GTPC.PCEN bit is 1 and the GTPC.PCNT counter is 1, an interrupt request is generated at the end of cycle.

21.4.2 DMAC and DTC Activation

The DMAC and DTC can be activated by the interrupt in each channel. For details, see section 12, Interrupt Controller Unit (ICU), section 15, DMA Controller (DMAC), and section 16, Data Transfer Controller (DTC).

21.4.3 Interrupt and A/D Conversion Start Request Skipping Function

21.4.3.1 Interrupt Skipping Function by GTITC Register

By setting the GTITC register, the GTCNT counter overflow (GTPR register compare match) interrupt (GPTn_OVF) and underflow interrupt (GPTn_UDF) can be skipped. Other interrupts and A/D conversion start request signals can be skipped in coordination with the GPTn_OVF/GPTn_UDF skipping function. When the interrupt is skipped, the updating of relevant status flag is also skipped. The interrupt skipping is continued even if the status flag is set to 1.

The interrupt skipping function is related only to the GTITC register setting, and is not related to setting of the GTINTAD register interrupt enable bit. The interrupt skipping is continued even if the interrupt is disabled with GTINTAD register setting.

When both troughs and crests are counted and skipped in triangle-wave mode, if the number of times of skipping is odd, GPTn_OVF/GPTn_UDF interrupt requests cannot be generated at troughs only or at crests only depending on the skipping counter start timing. Therefore, in order to count both troughs and crests and generate the GPTn_OVF/GPTn_UDF interrupts at troughs only or crests only in triangle-wave mode, the number of times of skipping should be even.

●在互补PWM模式下，中断请求在波峰处使能（主通道的GTCNT计数器值从GTPR寄存器值变为GTPR寄存器值减1）。

●通过硬件源计数（包括外部脉冲宽度测量功能），发生溢出（GTCNT在向上计数时从GTPR变为0）。

(8) GPTn_UDF中断（n=0到9）

在以下情况下会产生中断请求。

●在锯齿波PWM模式1和锯齿波单发脉冲模式下，下溢时（当向下计数期间GTCNT计数器值从0变为GTPR时）使能中断请求

●在三角波模式下，在波谷处启用中断请求（GTCNT由0变为1）

●在互补PWM模式下，中断请求在波谷处启用（主通道的GTCNT计数器值从0变为1）。

●硬件源计数（包括外部脉宽测量功能）发生下溢（向下计数时GTCNT从0变为GTPR）。

关于中断信号和中断状态标志，请参见第21.2.16节。GTST：通用PWM定时器状态寄存器。

(9) GPTn_ADTRGA中断（n=0到9）

当GTCNT计数器值与GTADTRA匹配时，会在以下条件下产生中断请求。

●在向上计数中，GTINTAD中的中断使能位（ADTRAUEN）为1。

●在递减计数中，GTINTAD中的中断使能位(ADTRADEN)为1。在执行事件计数操作时，不产生该中断请求。

(10)GPTn_ADTRGB中断（n=0到9）

当GTCNT计数器值与GTADTRB匹配时，会在以下条件下产生中断。

●在向上计数中，GTINTAD中的中断使能位（ADTRBUEN）为1。

●在递减计数中，GTINTAD中的中断使能位（ADTRBDEN）为1。在执行事件计数操作时，不产生该中断请求。

(11)GPTn_PC中断（n=0到3）

当GTPC.PCEN位为1且GTPC.PCNT计数器为1时，在周期结束时产生中断请求。

21.4.2 DMAC和DTC激活

DMAC和DTC可以通过每个通道中的中断来激活。有关详细信息，请参阅第12节，中断控制器单元(ICU)，第15节，DMA控制器(DMAC)，和第16节，数据传输控制器(DTC)。

21.4.3 中断和AD转换开始请求跳过功能

21.4.3.1 GTITC寄存器的中断跳跃功能

通过设置GTITC寄存器，可以跳过GTCNT计数器溢出（GTPR寄存器比较匹配）中断（GPTn_OVF）和下溢中断（GPTn_UDF）。与GPTn_OVFGPTn_UDF跳过功能配合，可以跳过其他中断和AD转换开始请求信号。当中断被跳过时，相关状态标志的更新也被跳过。即使状态标志设置为1，中断跳过也会继续。

中断跳过功能只与GTITC寄存器的设置有关，与GTINTAD寄存器中断使能位的设置无关。即使通过GTINTAD寄存器设置禁用中断，中断跳过也会继续。

三角波模式下波谷和波峰都计数跳越时，若跳越次数为奇数，
GPTn_OVFGPTn_UDF中断请求不能仅在波谷或波峰产生，具体取决于跳跃计数器的开始时间。因此，为了在三角波模式下同时计算波谷和波峰，并在仅波谷或波峰产生GPTn_OVFGPTn_UDF中断，跳过的次数应该是偶数。

Similarly, in saw-wave mode, when both overflows and underflows are counted and skipped with the count direction changed, GPTn_OVF/GPTn_UDF interrupt requests are sometimes not generated at overflows only or at underflows only. Therefore, in order to count both overflows and underflows with the count direction changed and generate the GPTn_OVF/ GPTn_UDF interrupts at overflows only or underflows only in saw-wave mode, the skipping state should be carefully checked before using.

When changing the skipping count, be sure to release the skipping count setting (GTITC.IVTC[1:0] bits = 00b).

Figure 21.139 to Figure 21.144 show examples of skipping function operation.

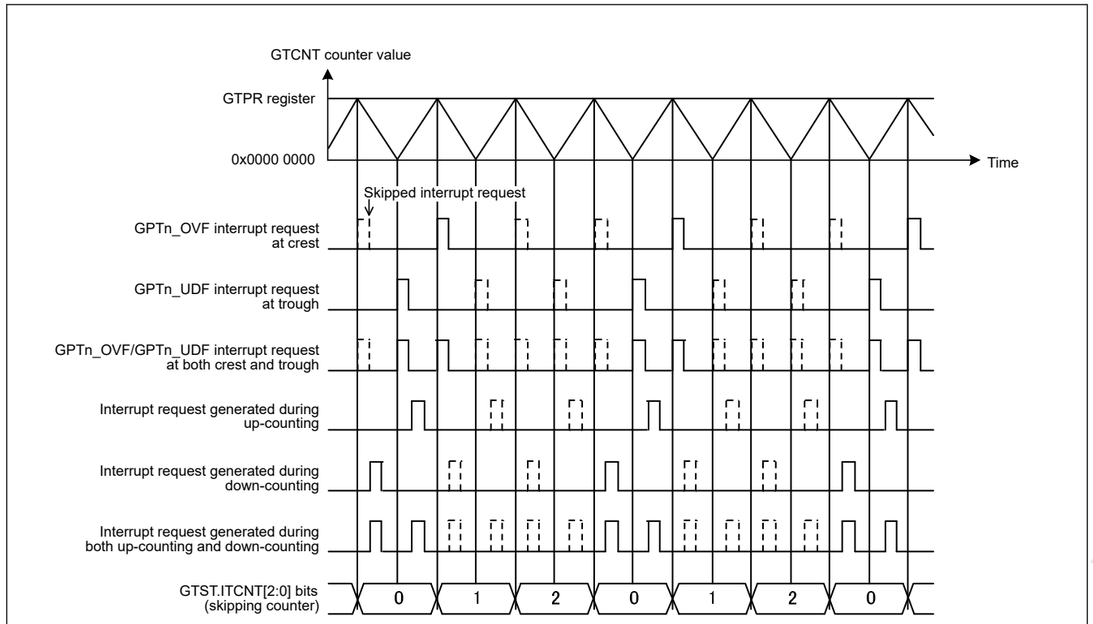


Figure 21.139 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Crests, Skipping Count: 2)

类似地，在锯齿波模式下，当计数方向改变同时计数和跳过上溢和下溢时，GPTn_OVFGPTn_UDF中断请求有时不会仅在上溢或仅在下溢时产生。因此，为了在计数方向改变的情况下计算上溢和下溢并生成GPTn_OVF

GPTn_UDF仅在上溢或仅在锯齿波模式下下溢时中断，使用前应仔细检查跳过状态。

更改跳过计数时，请务必释放跳过计数设置（GTITC.IVTC[1:0]位=00b）。

图21.139至图21.144显示了跳过函数操作的示例。

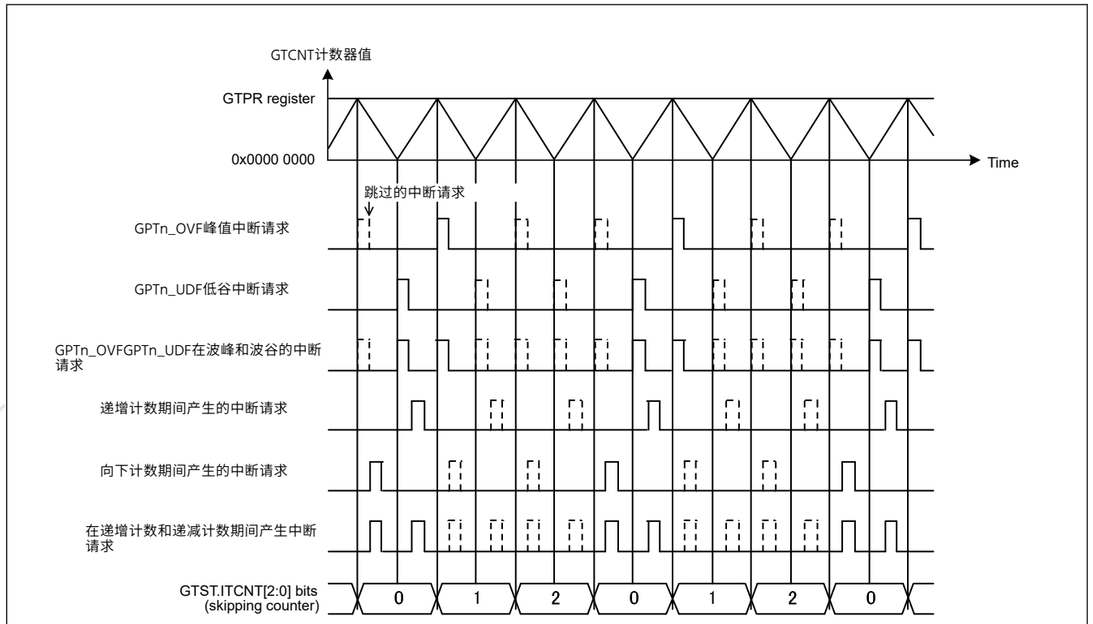


图21.139中断跳跃函数操作示例（三角波、计数和跳跃）波峰，跳过计数：2）

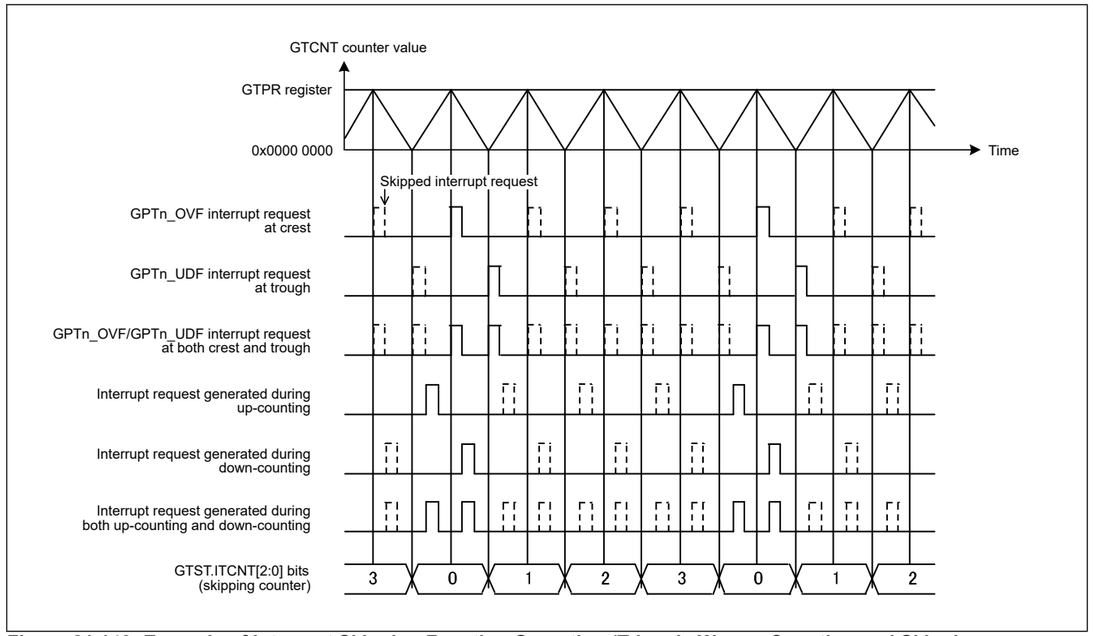


Figure 21.140 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Troughs, Skipping Count: 3)

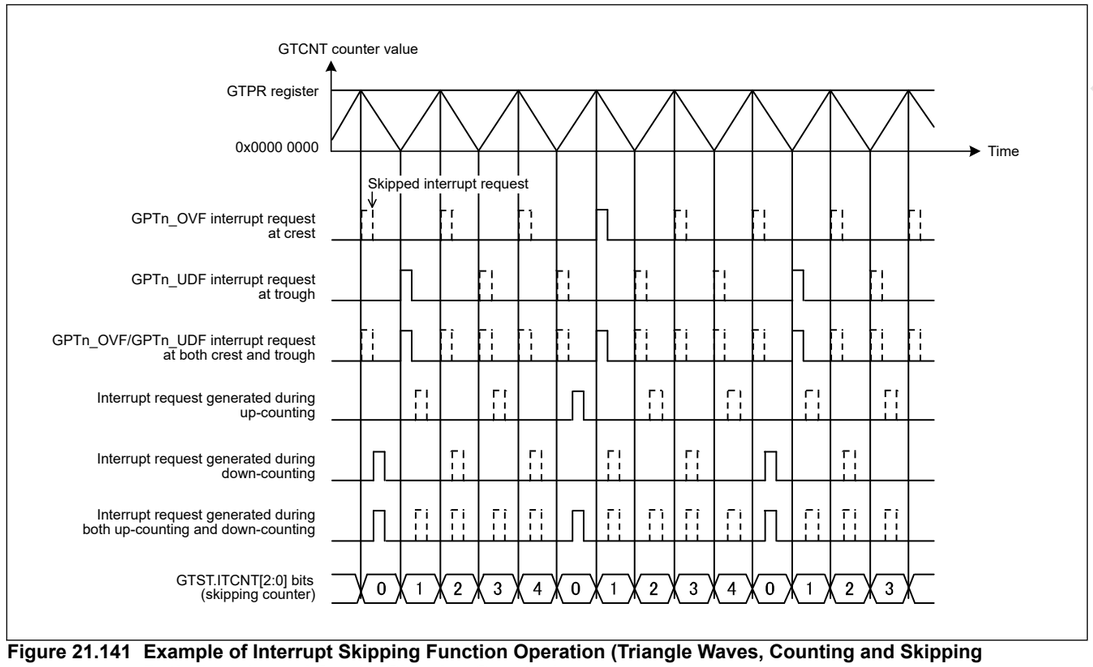


Figure 21.141 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 4)

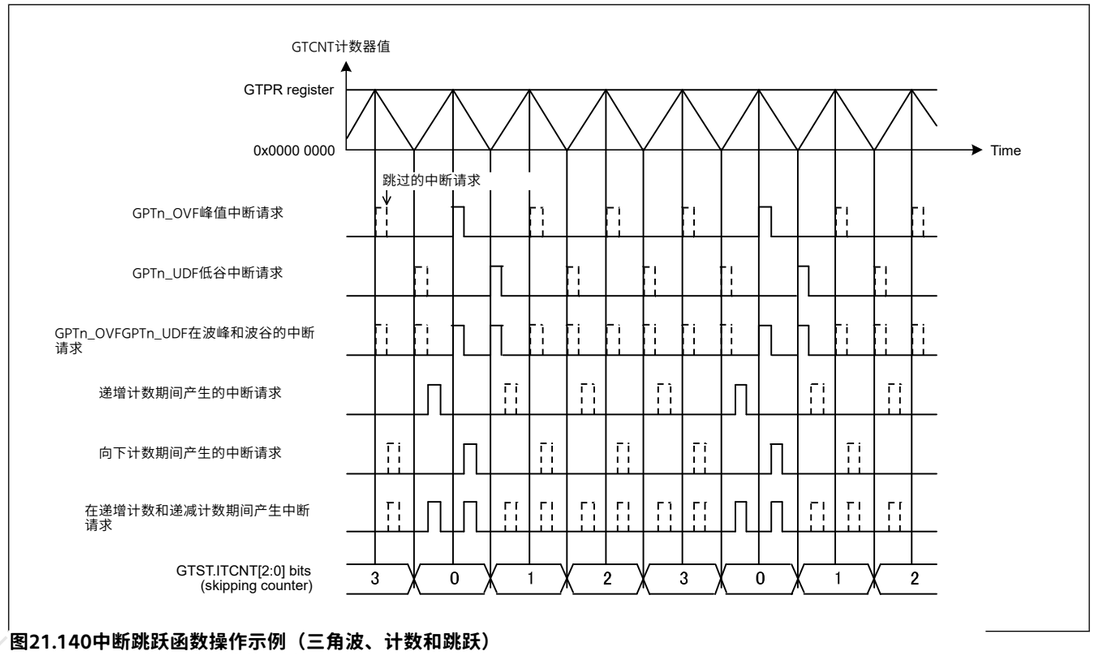


图21.140中断跳跃函数操作示例（三角波、计数和跳跃）槽，跳过计数：3）

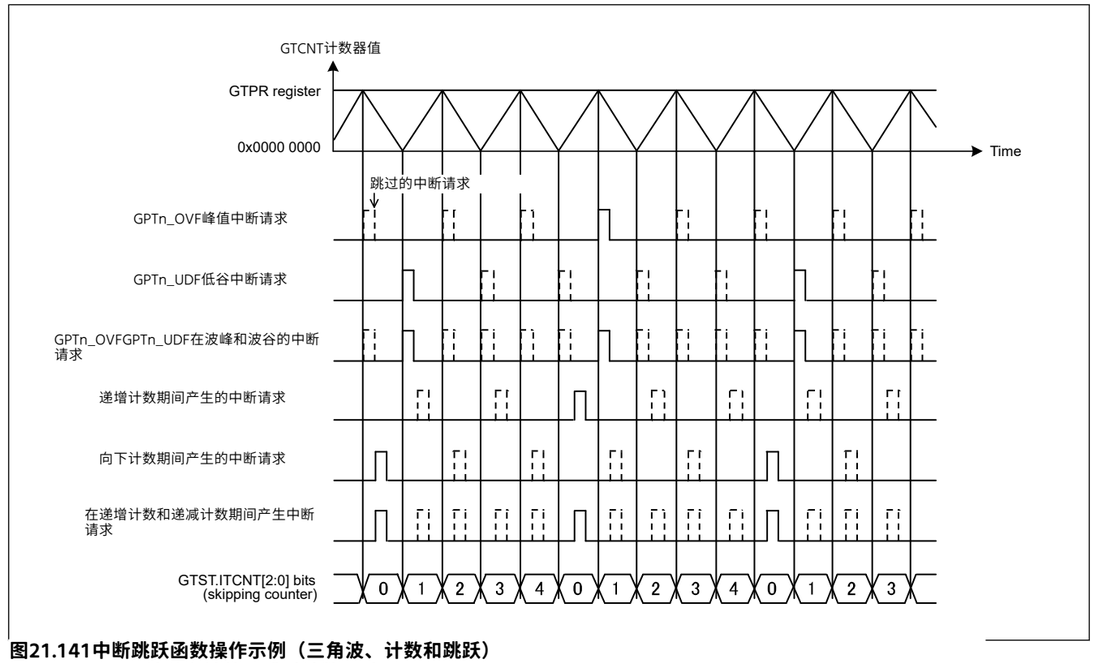


图21.141中断跳跃函数操作示例（三角波、计数和跳跃）波谷和波峰，跳过计数：4）

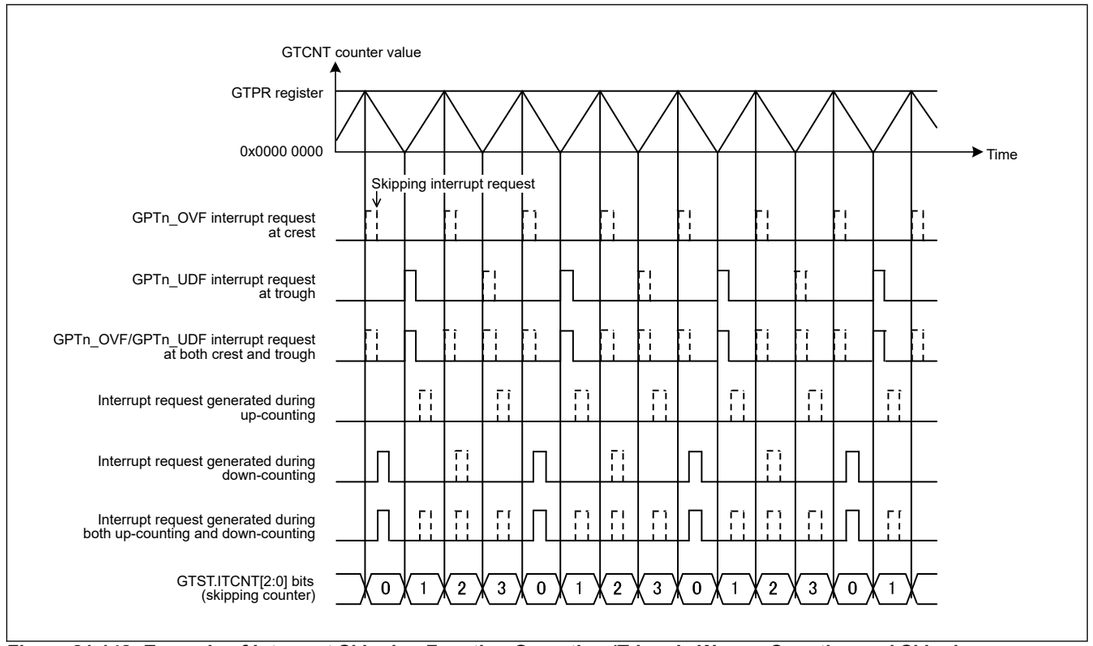


Figure 21.142 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 3, Skipping Started at Up-Counting)

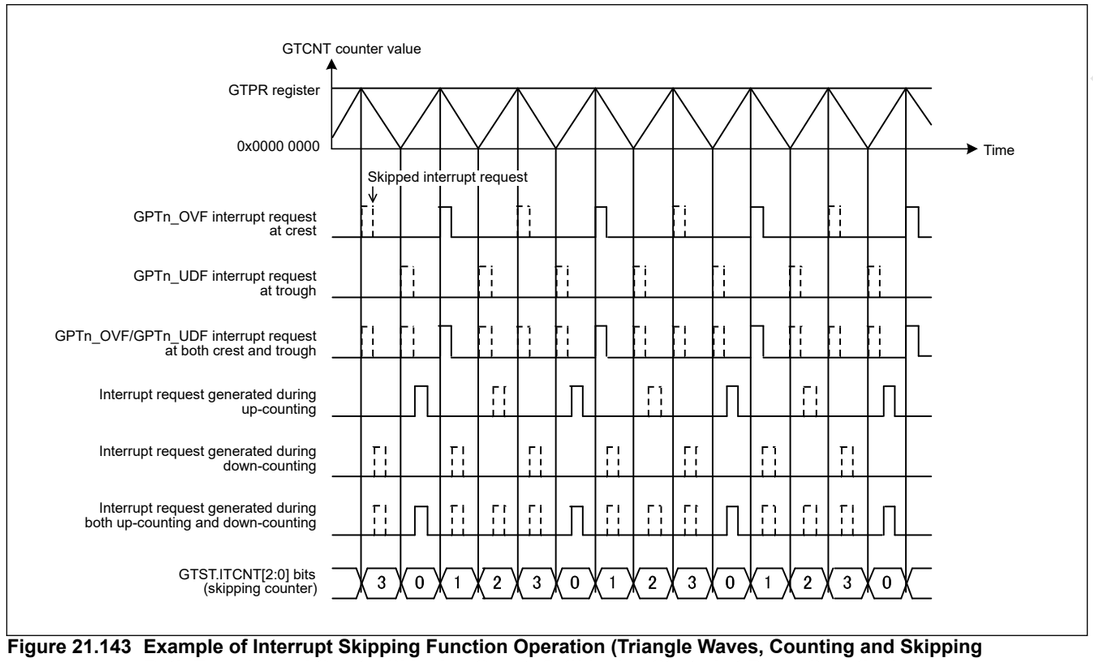


Figure 21.143 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 3, Skipping Started at Down-Counting)

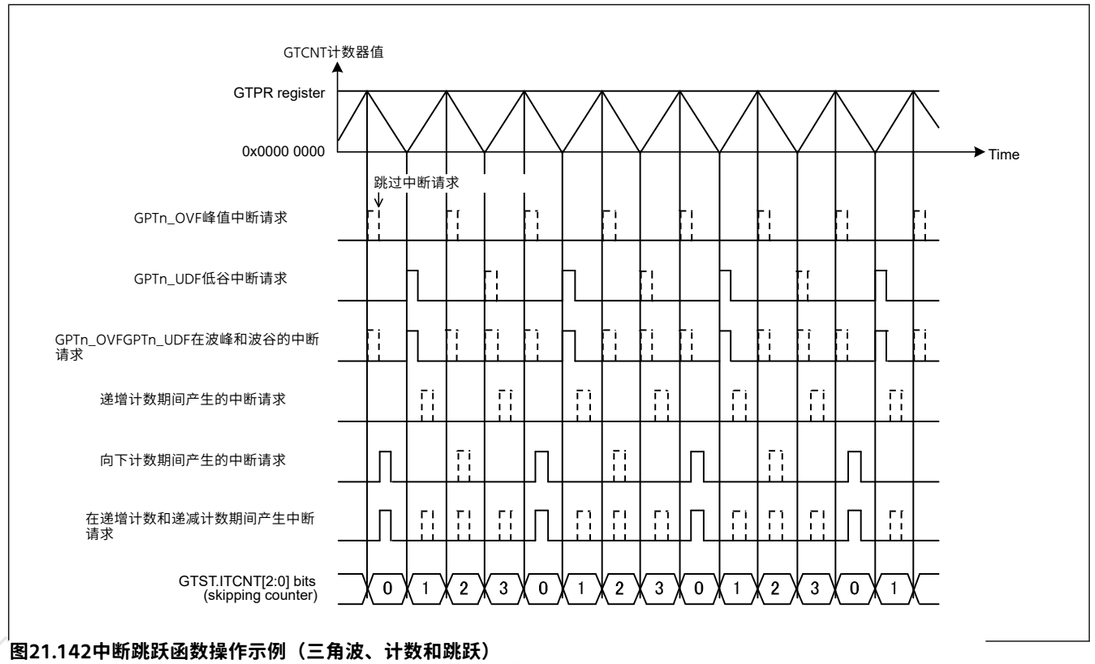


图21.142中断跳跃函数操作示例（三角波、计数和跳跃）波谷和波峰，跳过计数：3，跳过从向上计数开始）

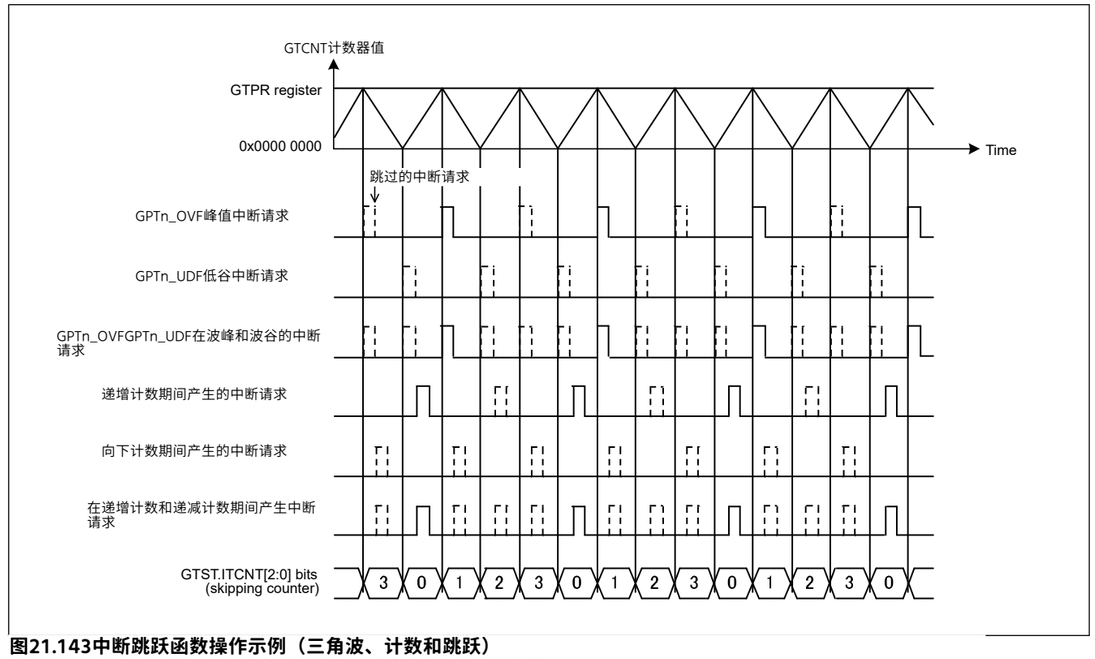


图21.143中断跳跃函数操作示例（三角波、计数和跳跃）波谷和波峰，跳过计数：3，跳过从向下计数开始）

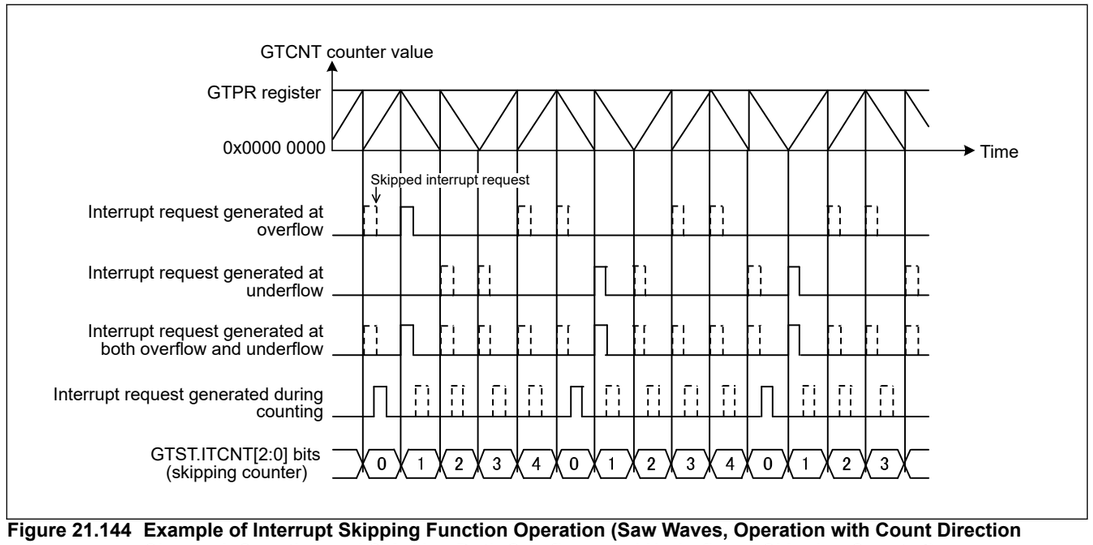


Figure 21.144 Example of Interrupt Skipping Function Operation (Saw Waves, Operation with Count Direction Changed, Counting and Skipping Both Overflows and Underflows, Skipping Count: 4)

21.4.3.2 Extended Interrupt Skipping Function

Overflow/underflow interrupt, compare match/input capture interrupt, A/D conversion start request, and buffer transfer can be skipped by counting the GTCNT counter overflow or underflow based on settings of the GTEITC, GTEITLI1, GTEITLI2 and GTEITLB registers.

Overflow/underflow interrupt, compare match/input capture interrupt, A/D conversion start request, and buffer transfer can individually be set for skipping and the skipping period using the GTEITLI1, GTEITLI2, and GTEITLB registers.

The skipping period is set, related to the operation of the two independent extended interrupt skipping counters (EITCNT1[3:0] and EITCNT2[3:0] bits in the GTEITC registers), as a period that either of the counter value for such skipping counters is other than 0 or other than the skipping count. The skipping period can also be set as a period that the both skipping counters are set as other than 0 or other than the skipping count for the counter value.

Figure 21.145 shows the counter operation for interrupt skipping by the GTITC register and extended interrupt skipping.

The counter operation for extended interrupt skipping is set by the GTEITC register.

The EITCNT1[3:0] bits are set for 0 as initial value and then they count the count source (in Figure 21.145, a crest is selected) selected by the extended interrupt counter 1 count source select bit (GTEITC.EIVTC1[1:0] bits), and repeat the count operation which returns to 0 when the skipping count (in Figure 21.145, count is 2) set by the extended interrupt skipping 1 skipping count setting bit (EIVTT1[3:0] bits) is achieved.

The EITCNT2[3:0] bits can be set for the initial value and they count the count source (in Figure 21.145, a trough is selected) selected by the extended interrupt counter 2 count source select bit (EIVTC2[1:0] bits), and repeat the count operation which return to 0 when the skipping count (in Figure 21.145 count is 2) set by the EIVTT2[3:0] bits is achieved. The initial value is set when the GTEITC register is written by the access of upper 16 bits or 32 bits while the setting for the extended interrupt skipping counter 2 is not counted (EIVTC2[1:0] bits are 00b) and when the write value to the EIVTC2[1:0] bits is other than 00b. When the initial value is set, the write value to the extended interrupt skipping counter 2 initial value bits (EITCNT2IV[3:0] bits) are set as the initial value for the EITCNT2[3:0] bits.

The extended interrupt skipping counter starts up-counting at the first count clock after the setting is modified from not counting to counting.

The interrupt skipping count counter (GTST.ITCNT[2:0] bits) for the interrupt skipping function set by the GTITC register is reset to 000b when the GTCNT counter operation is stopped: however, the EITCNT1[3:0] and EITCNT2[3:0] bits for the extended interrupt skipping function retain the value even after the GTCNT counter operation is stopped, and the counting can be resumed from the value before the counter is stopped. When values for the EITCNT1[3:0] and EITCNT2[3:0] bits are to be reset (0000b), set the EIVTC1[1:0] and EIVTC2[1:0] bits to the setting for not counting (not skipping) (00b).

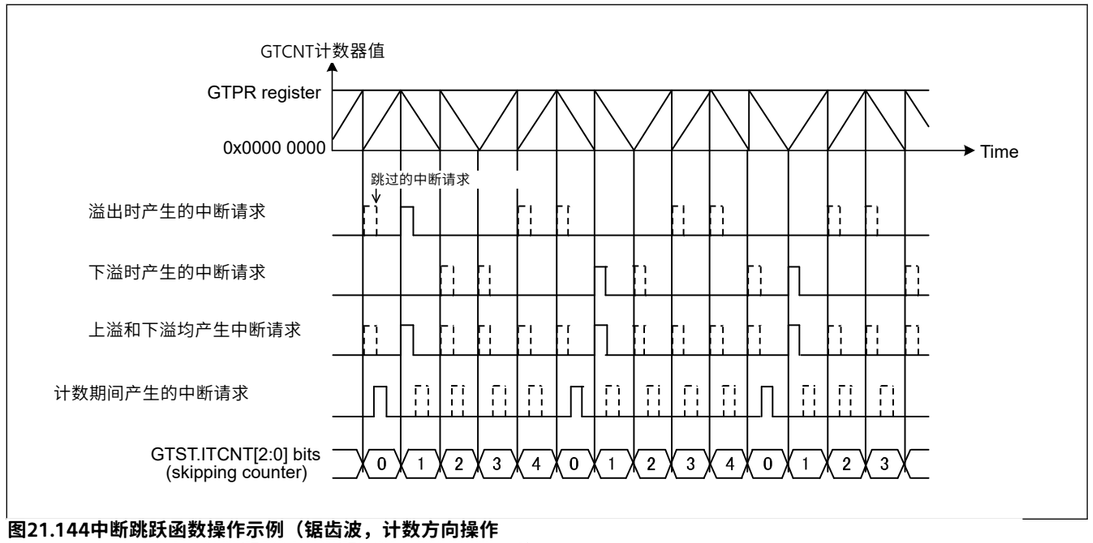


图21.144中断跳跃函数操作示例（锯齿波，计数方向操作更改，计数和跳过上溢和下溢，跳过计数：4）

21.4.3.2 扩展中断跳过功能

根据GTEITC、GTEITLI1、GTEITLI2和GTEITLB寄存器的设置，通过对GTCNT计数器上溢或下溢进行计数，可以跳过上溢下溢中断、比较匹配输入捕捉中断、AD转换开始请求和缓冲区传输。

可以使用GTEITLI1、GTEITLI2和GTEITLB寄存器分别设置上溢下溢中断、比较匹配输入捕捉中断、AD转换开始请求和缓冲区传输以用于跳过和跳过周期。

设置跳过周期，与两个独立的扩展中断跳过计数器（GTEITC寄存器中的EITCNT1[3:0]和EITCNT2[3:0]位）的操作有关，作为此类计数器值中的任何一个的周期跳过计数器不是0或不是跳过计数。也可以将跳过时间段设置为两个跳过计数器设置为0以外的时间段或设置为计数器值的跳过次数以外的时间段。

图21.145显示了通过GTITC寄存器跳过中断和扩展中断跳过的计数器操作。

扩展中断跳过的计数器操作由GTEITC寄存器设置。

EITCNT1[3:0]位设置为0作为初始值，然后对扩展中断计数器1计数源选择位(GTEITC.EIVTC1[1:0]位），并重复计数操作，当达到扩展中断跳过1跳过计数设置位（EIVTT1[3:0]位）设置的跳过计数（在图21.145中，计数为2）时返回0。

EITCNT2[3:0]位可设置为初始值，并对扩展中断计数器2计数源选择位(EIVTC2[1:0]位)，并重复计数操作，当达到EIVTT2[3:0]位设置的跳过计数（在图21.145中计数为2）时返回0。当通过高16位或32位访问写入GTEITC寄存器时设置初始值，而扩展中断跳过计数器2的设置不计数（EIVTC2[1:0]位为00b）以及写入值时到EIVTC2[1:0]位不是00b。设置初始值时，将写入扩展中断跳过计数器2个初始值位（EITCNT2IV[3:0]位）的值设置为EITCNT2[3:0]位的初始值。

扩展中断跳过计数器在设置从不计数修改为计数后的第一个计数时钟开始向上计数。

由GTITC寄存器设置的中断跳过功能的中断跳过计数计数器（GTST.ITCNT[2:0]位）在GTCNT计数器操作停止时复位为000b：但是，EITCNT1[3:0]和EITCNT2[3:0]扩展中断跳过功能位即使在GTCNT计数器操作停止后仍保持该值，并且可以从计数器停止之前的值重新开始计数。当EITCNT1[3:0]和EITCNT2[3:0]位的值要复位(0000b)时，将EIVTC1[1:0]和EIVTC2[1:0]位设置为不计数的设置（不跳过）（00b）。

When the skipping count is to be changed, change the count after stopping the skipping counter operation (set either of the EIVTC1[1:0] bit or the EIVTC2[1:0] bit to 00b).

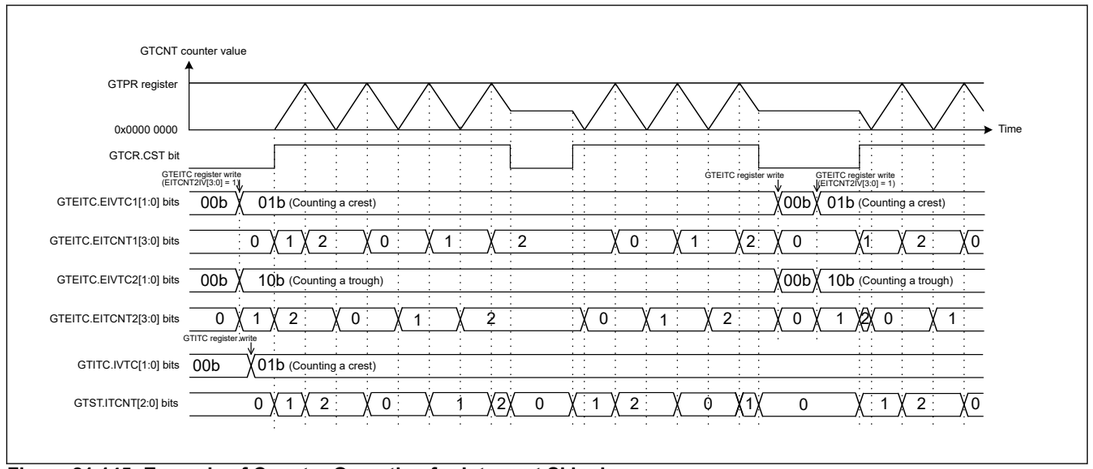


Figure 21.145 Example of Counter Operation for Interrupt Skipping

Interrupt skipping by the GTEITL1 register and A/D conversion start request skipping by the GTEITLI2 register can be performed simultaneously with skipping by the GTITC register or GTADCMSC register. A skipping period in this case is represented by OR-ed skipping periods of respective registers.

Figure 21.146 shows corresponding interrupt skipping operations by different registers are performed simultaneously.

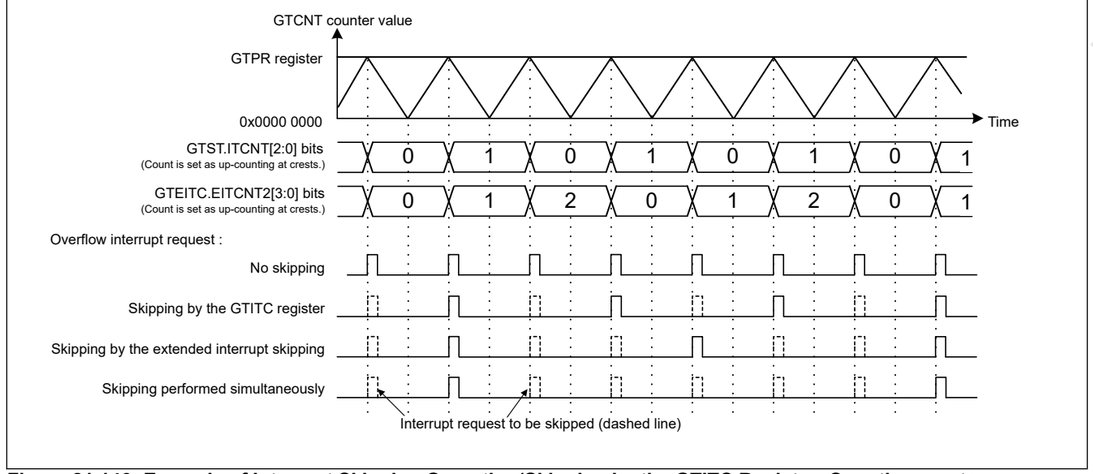


Figure 21.146 Example of Interrupt Skipping Operation(Skipping by the GTITC Register: Counting crests, Extended Interrupt Skipping: EIVTC1[1:0] bits = 00b, EIVTC2[1:0] bits = 01b, EITLV[2:0] bits = 010b)

When the extended interrupt skipping selected by GTEITLI1 is performed, the relevant status flag is also skipped. The skipping function is continued even if the status flag is set to 1.

When A/D conversion start request skipping selected by GTEITLI2 is performed, the relevant status flag is also skipped. The skipping function is continued even if the status flag is set to 1.

Skipping of updating of status flag and ELC event source outputs corresponding to A/D conversion start request for which skipping can be set up in the GTEITLI2 register is only based on the settings of the GTITC register and the extended interrupt skipping register, and has no connection with the setting of A/D conversion start request enable bit in the

如果要更改跳跃计数，请在停止跳跃计数器操作后更改计数（设置任一EIVTC1[1:0]位或EIVTC2[1:0]位到00b）。

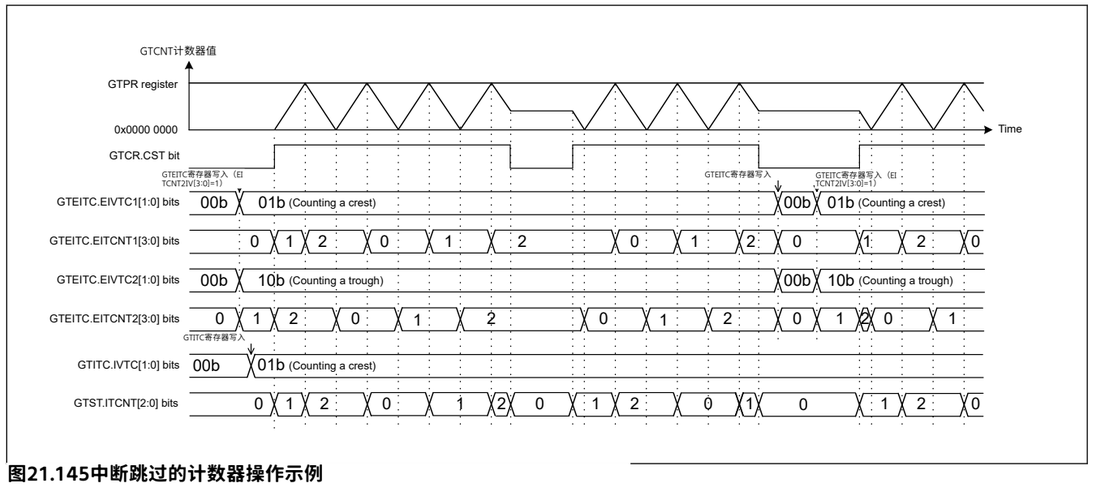


图21.145中断跳过的计数器操作示例

GTEITL1寄存器的中断跳跃和GTEITLI2寄存器的AD转换开始请求跳跃可以与GTITC寄存器或GTADCMSC寄存器的跳跃同时执行。这种情况下的跳跃周期由各个寄存器的或运算跳跃周期表示。

图21.146显示了不同寄存器同时执行相应的中断跳过操作。

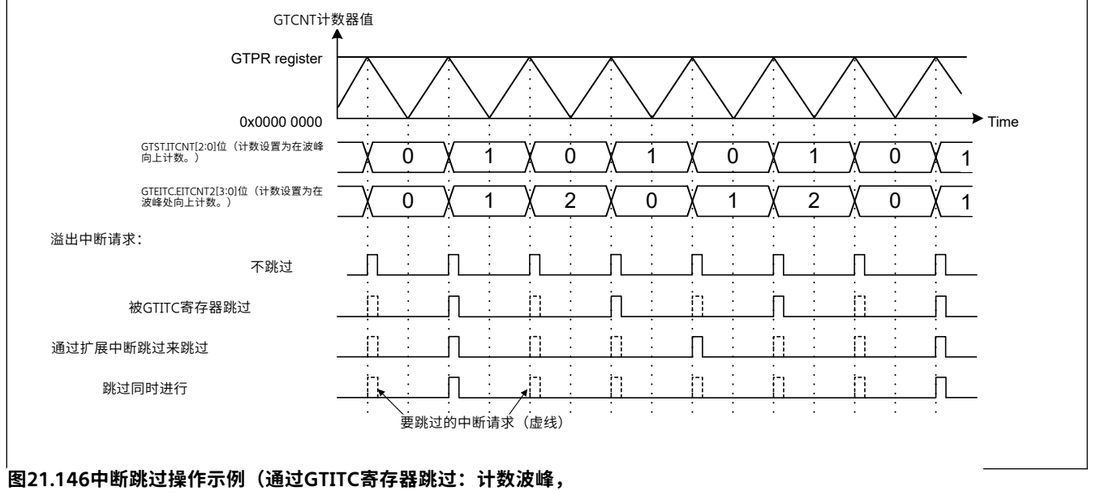


图21.146中断跳过操作示例（通过GTITC寄存器跳过：计数波峰，扩展中断跳过：EIVTC1[1:0]位=00b，EIVTC2[1:0]位=01b，EITLV[2:0]位=010b）

当执行GTEITLI1选择的扩展中断跳过时，相关的状态标志也被跳过。即使状态标志设置为1，跳过功能也会继续。

当执行GTEITLI2选择的AD转换开始请求跳过时，相关状态标志也被跳过。
即使状态标志设置为1，跳过功能也会继续。

跳过可在GTEITLI2寄存器中设置跳过的AD转换开始请求对应的状态标志更新和ELC事件源输出的跳过仅基于GTITC寄存器和扩展中断跳过寄存器的设置，与在AD转换开始请求使能位的设置

GTINTAD register. The A/D conversion start request enable bit is used only for A/D conversion start request output(ELC event source output) after skipping.

A buffer transfer skipping by the GTEITLB register is performed in all of buffer operation which is enabled in the GTBER and GTDTCR registers and GTBER2 register, or all buffer operations performed by saw-wave one-shot pulse mode or triangle-wave PWM mode 3 or complementary PWM mode(excludes buffer transfer from GTCCRC, GTCCRE to GTCCRA).

An interrupt skipping and a buffer transfer skipping are operated individually. An interrupt output without performing a buffer transfer and performing a buffer transfer without an interrupt output can also be operated.

Figure 21.147 to Figure 21.154 show examples of extended skipping function operation.

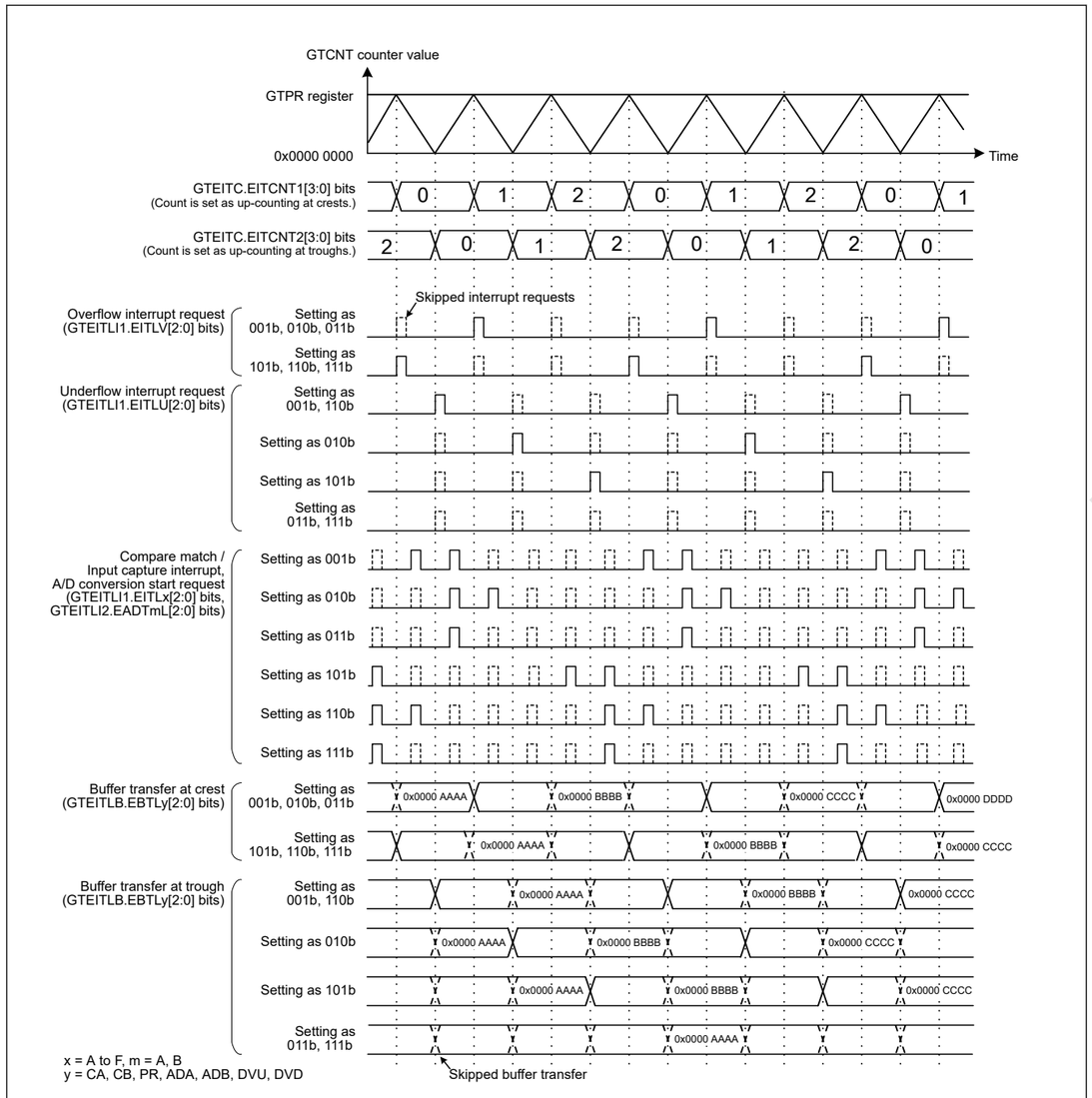


Figure 21.147 Example of Extended Interrupt Skipping Function (Triangle wave, Counting Crests, Extended Interrupt Skipping 1 Skipping Count: 2, Counting Troughs, Extended Interrupt Skipping 2 Skipping Count: 2, Extended Interrupt Skipping Counter 2 Initial Value: 0)

GTINTAD寄存器。AD转换开始请求使能位仅用于跳过后的AD转换开始请求输出（ELC事件源输出）。

在GTBER和GTDTCR寄存器和GTBER2寄存器中使能的所有缓冲区操作，或锯波单次脉冲模式或三角波PWM模式3或互补PWM模式（不包括从GTCCRC、GTCCRE到GTCCRA的缓冲区传输）。

中断跳过和缓冲区传输跳过是单独操作的。也可以操作不执行缓冲传送的中断输出和不执行中断输出的缓冲传送。

图21.147至图21.154显示了扩展跳过功能操作的示例。

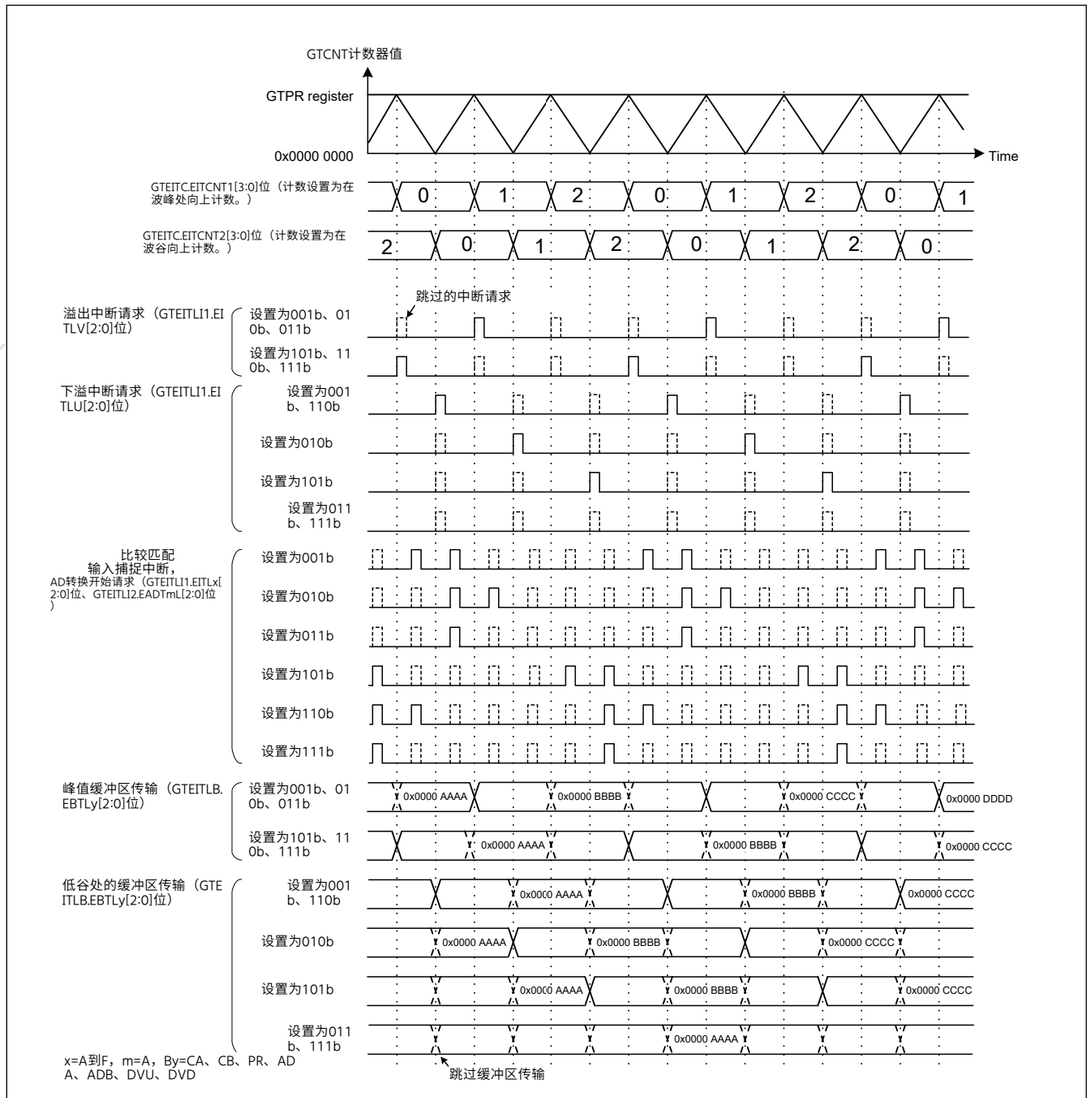


图21.147扩展中断跳过功能示例（三角波、计数波峰、扩展中断跳过1跳过计数：2，计数波谷，扩展中断跳过2跳过计数：2，扩展中断跳过计数器2初始值：0）

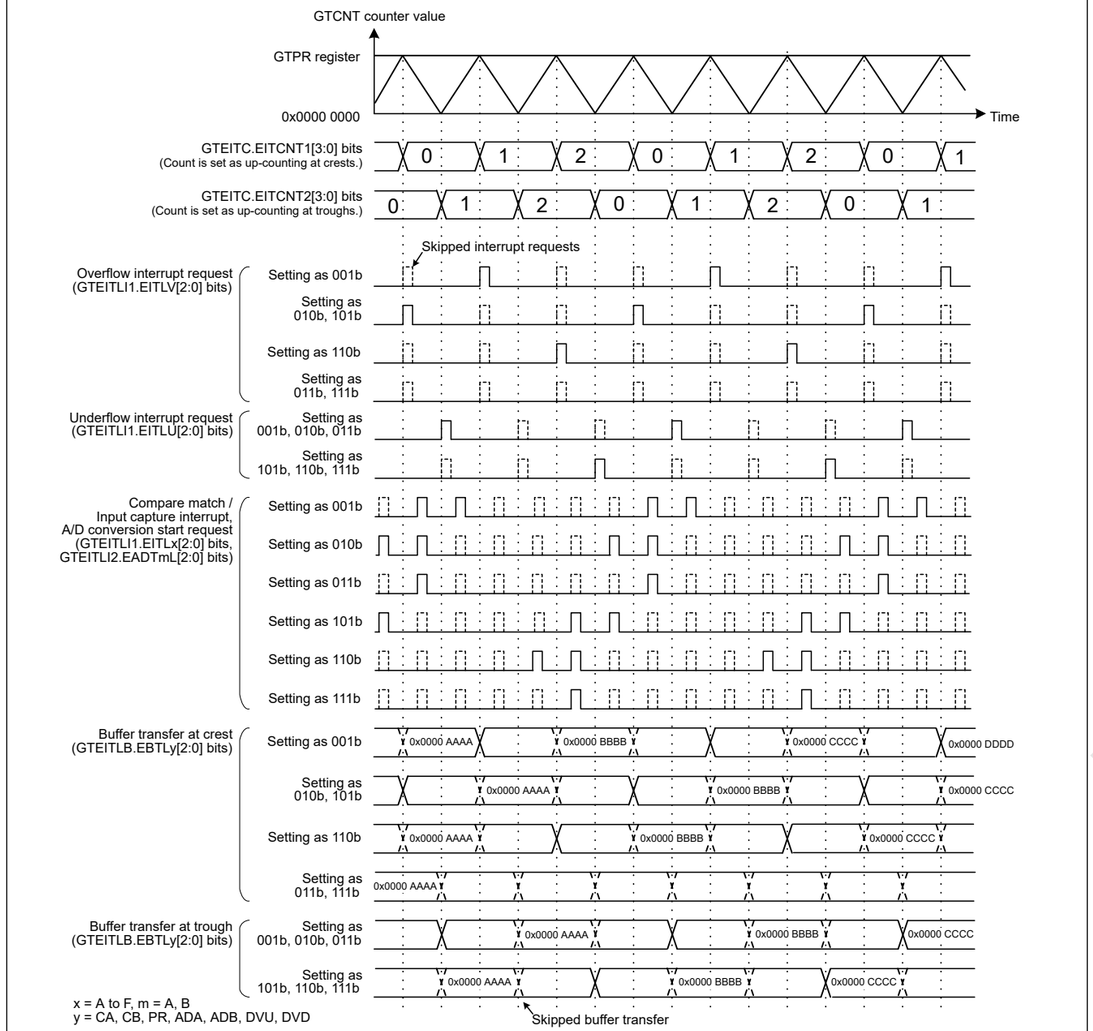


Figure 21.148 Example of Extended Interrupt Skipping Function (Triangle Waves, Count Crests by the Extended Interrupt Skipping 1 with Skipping Count: 2, Count Troughs by the Extended Interrupt Skipping 2 with Skipping Count: 2, Extended Interrupt Skipping Counter 2 Initial Value: 1)

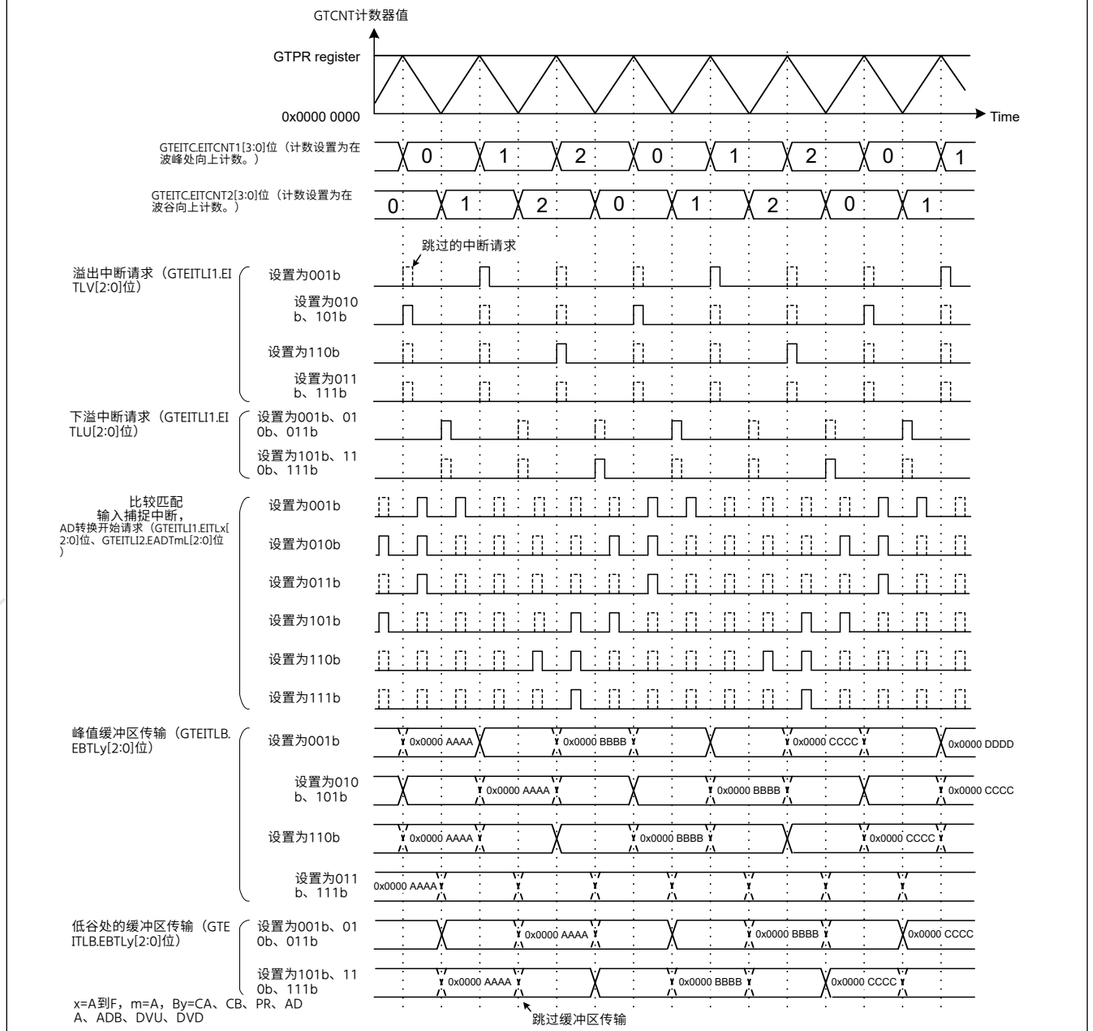


图21.148扩展中断跳过功能示例（三角波，由ExtendedInterruptSkipping1withSkippingCount:2 CountTroughsbytheExtended带有跳过计数的中断跳过2：2，扩展中断跳过计数器2初始Value: 1)

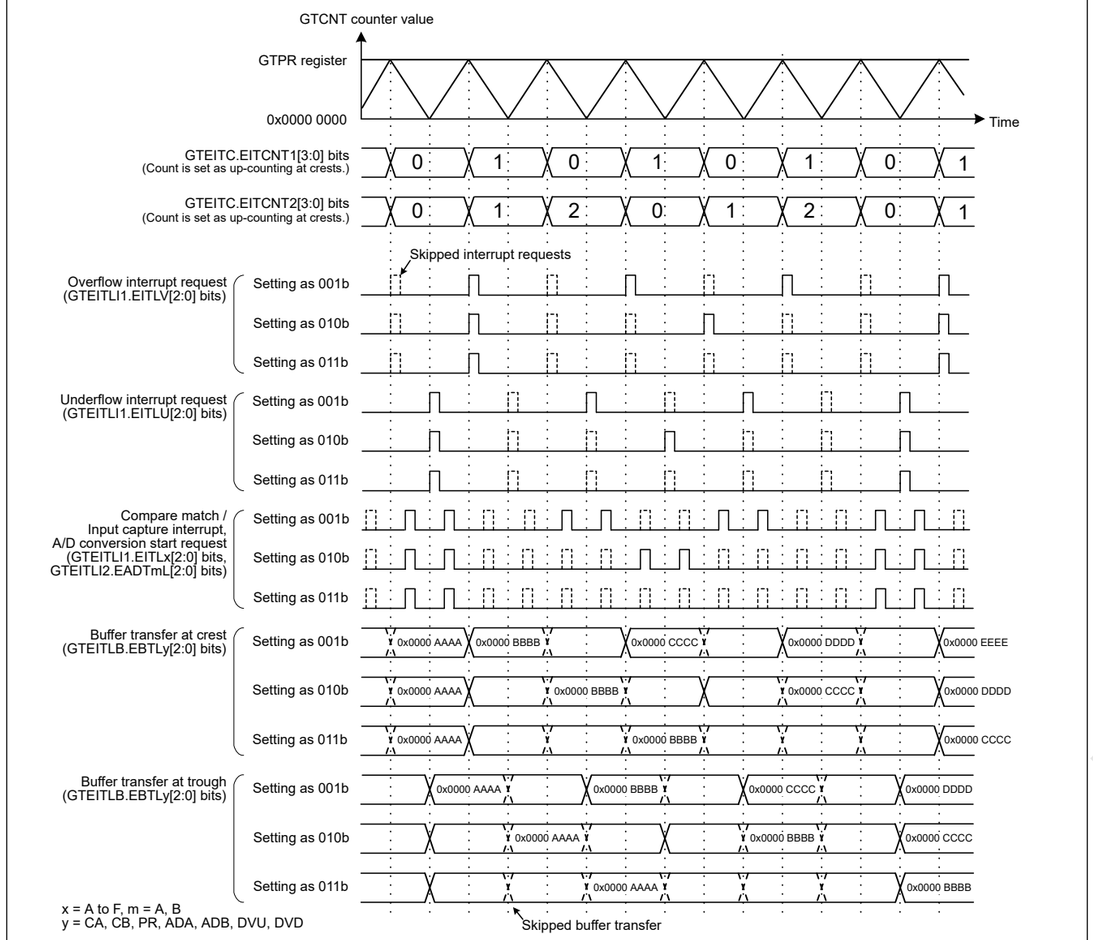


Figure 21.149 Example of Extended Interrupt Skipping Function Operation (Triangle Waves, Counting Crests, Extended Interrupt Skipping 1 Skipping Count: 1, Counting Crests, Extended Interrupt Skipping 2 Skipping Count: 2, Extended Interrupt Skipping Counter 2 Initial Value: 0, Skipped in the Period other than GTEITC.EITCNTk bits (k = 1, 2) as 0)

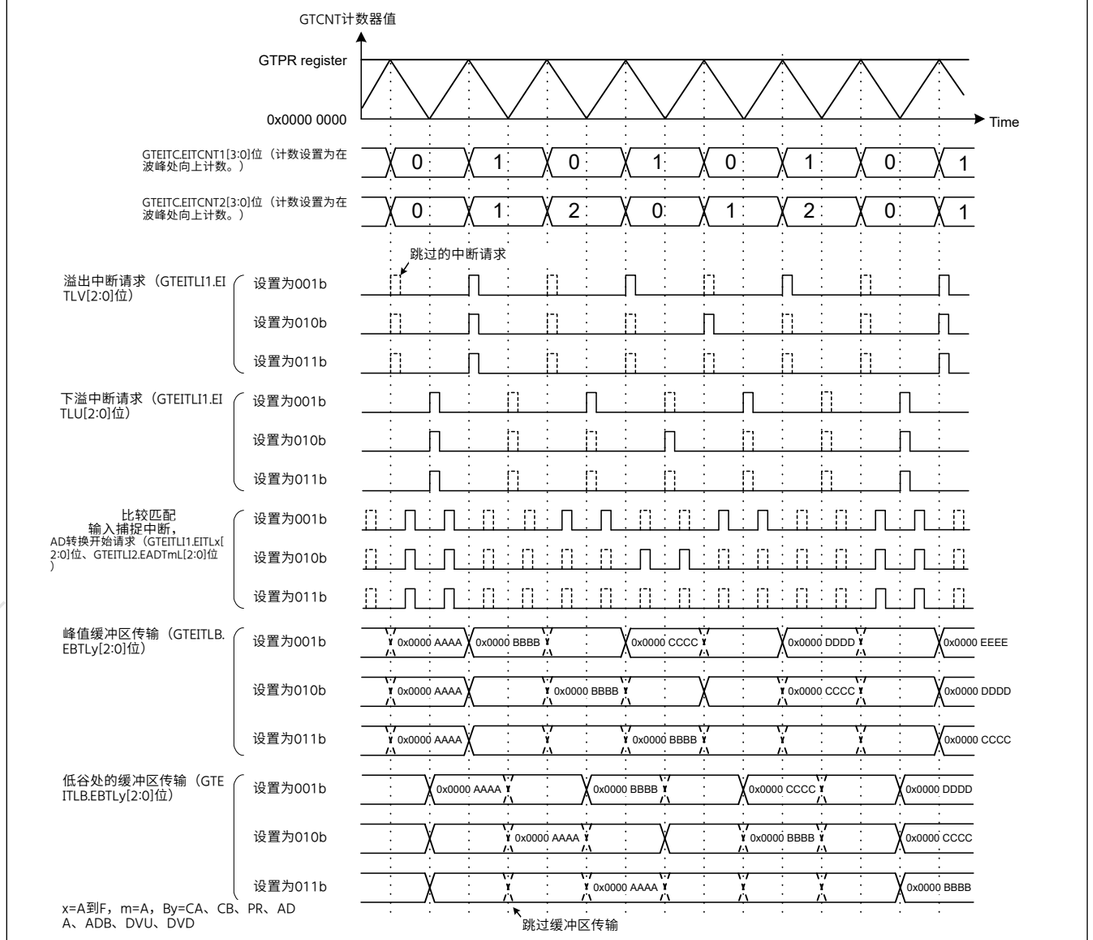


图21.149扩展中断跳过功能操作示例（三角波、计数波峰、ExtendedInterruptSkipping1SkippingCount:1 CountingCrests ExtendedInterrupt跳过2跳过计数：2，扩展中断跳过计数器2初始值：0，在GTEITC.EITCNTk位(k=1 2)以外的周期中跳过为0）

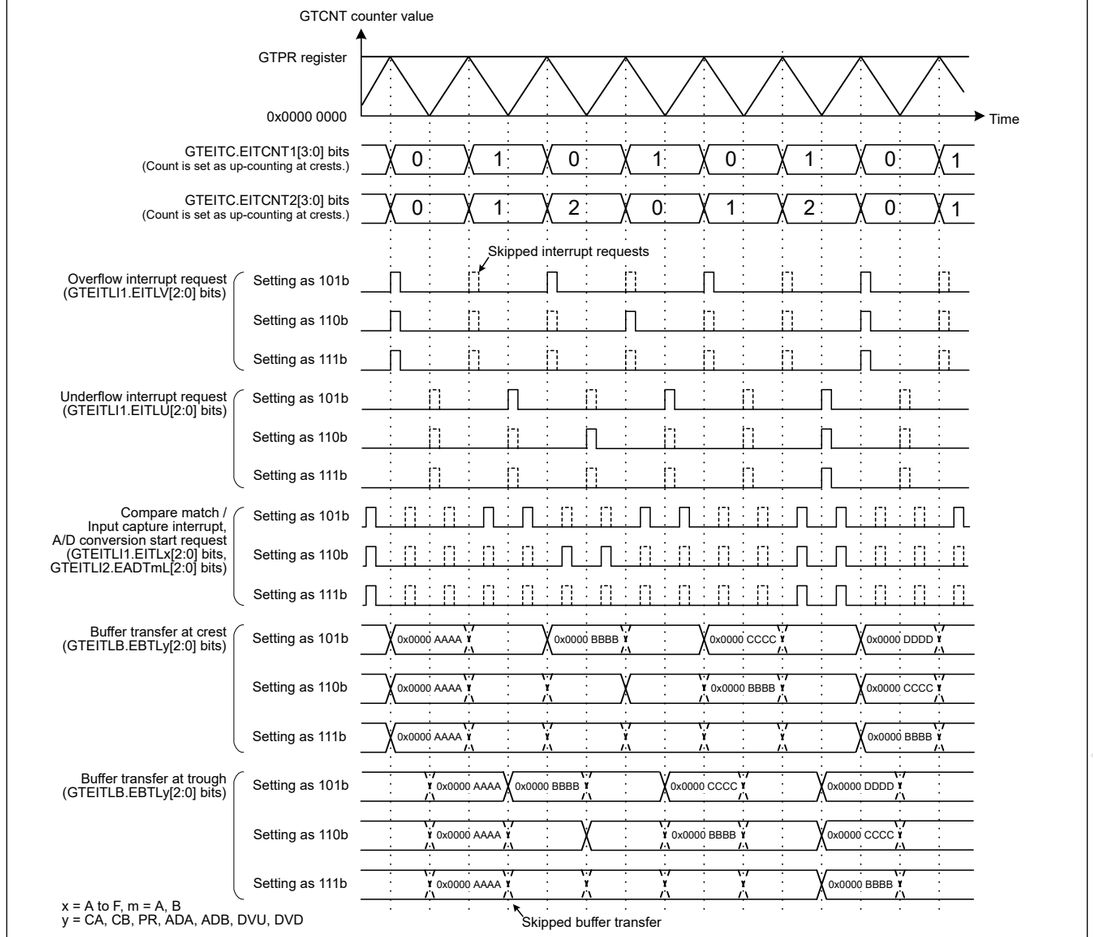


Figure 21.150 Example of Extended Interrupt Skipping Function Operation (Triangle Waves, Counting Crests, Extended Interrupt Skipping 1 Skipping Count: 1, Counting Crests, Extended Interrupt Skipping 2 Skipping Count: 2, Extended Interrupt Skipping Counter 2 Initial Value: 0, Skipped in the Period other than GTEITC.EITCNTk bits (k = 1, 2) as GTEITC.EIVTTk bits.)

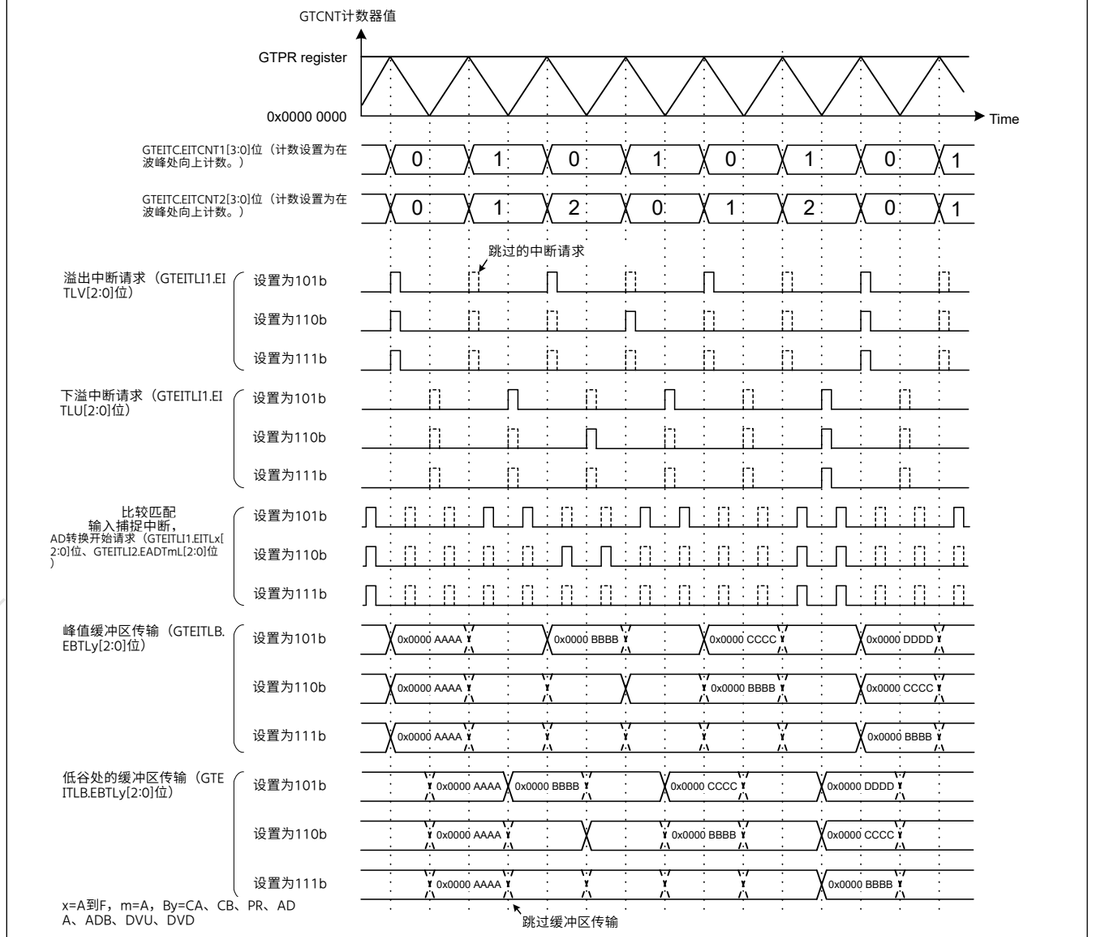


图21.150扩展中断跳过功能操作示例（三角波、计数波峰、ExtendedInterruptSkipping1SkippingCount:1 CountingCrests ExtendedInterrupt跳过2跳过计数：2，扩展中断跳过计数器2初始值：0，在GTEITC.EITCNTk位(k=1 2)以外的周期中作为GTEITC.EIVTTk位跳过。）

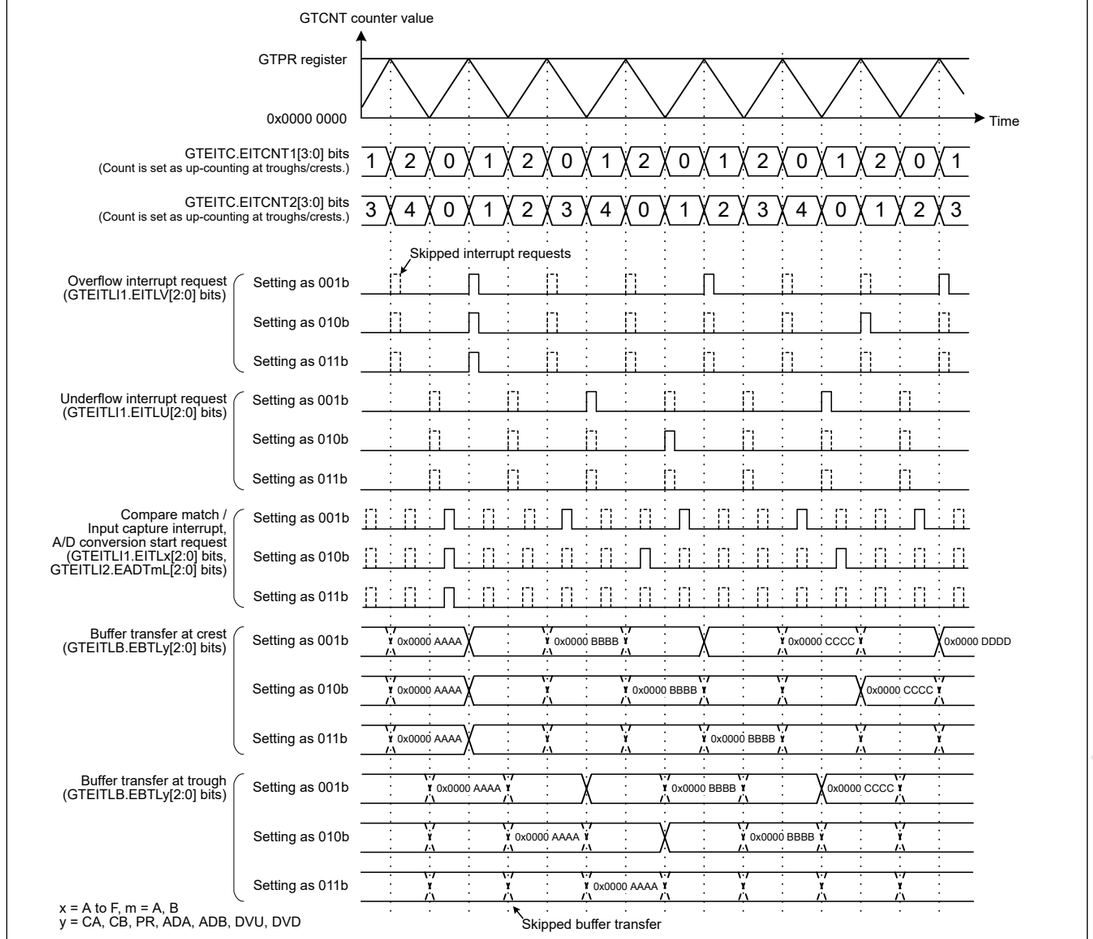


Figure 21.151 Example of Extended Interrupt Skipping Function Operation (Triangle Waves, Counting both Crests and Troughs, Extended Interrupt Skipping 1 Skipping Count: 2, Counting both Crests and Troughs, Extended Interrupt Skipping 2 Skipping Count: 4, Extended Interrupt Skipping Counter 2 Initial Value: 0, Skipped in the Period other than GTEITC.EITCNTk bits (k = 1, 2) as 0)

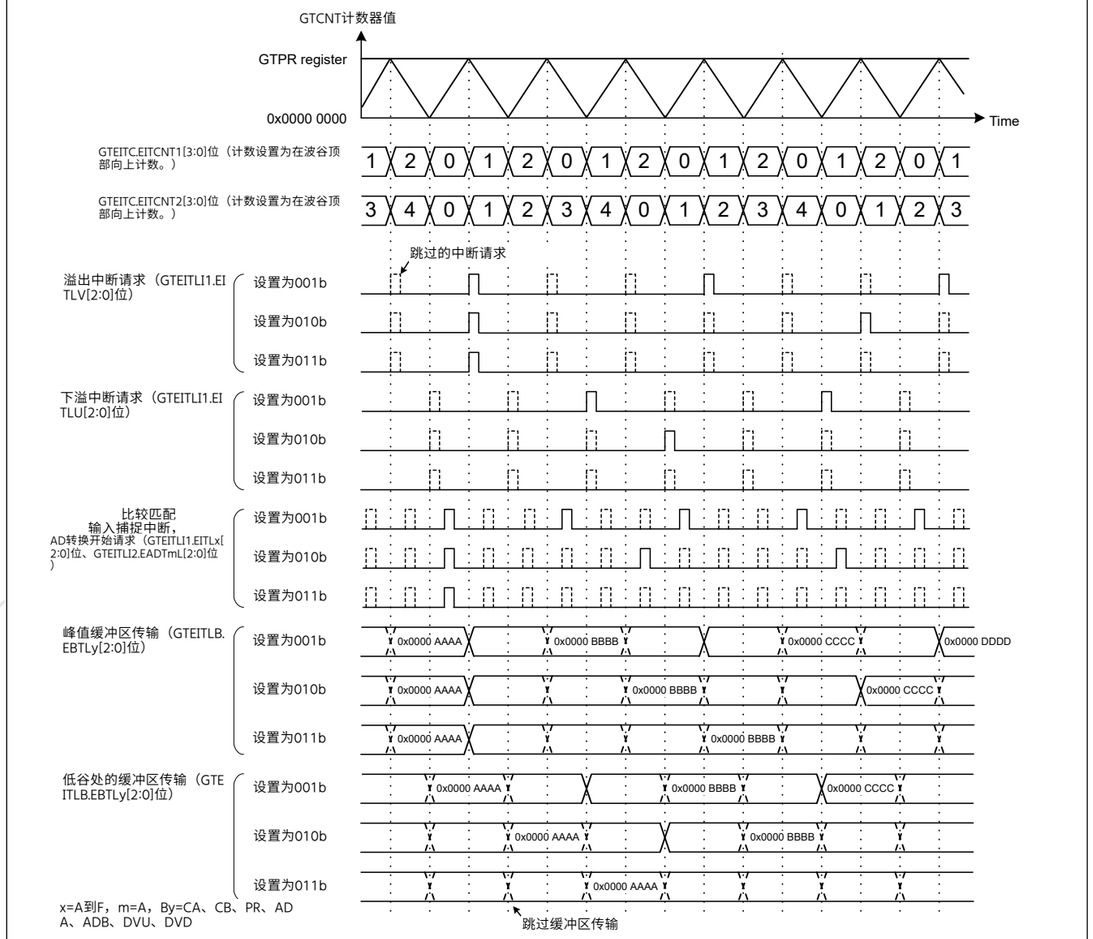


图21.151扩展中断跳过函数操作示例（三角波，同时计数波峰和波谷，扩展中断跳跃1跳跃计数：2，波峰和波谷计数，扩展中断跳跃2跳跃计数：4，扩展中断跳跃计数器2初始值：0，在GTEITC.EITCNTk位（k=1 2)作为0）

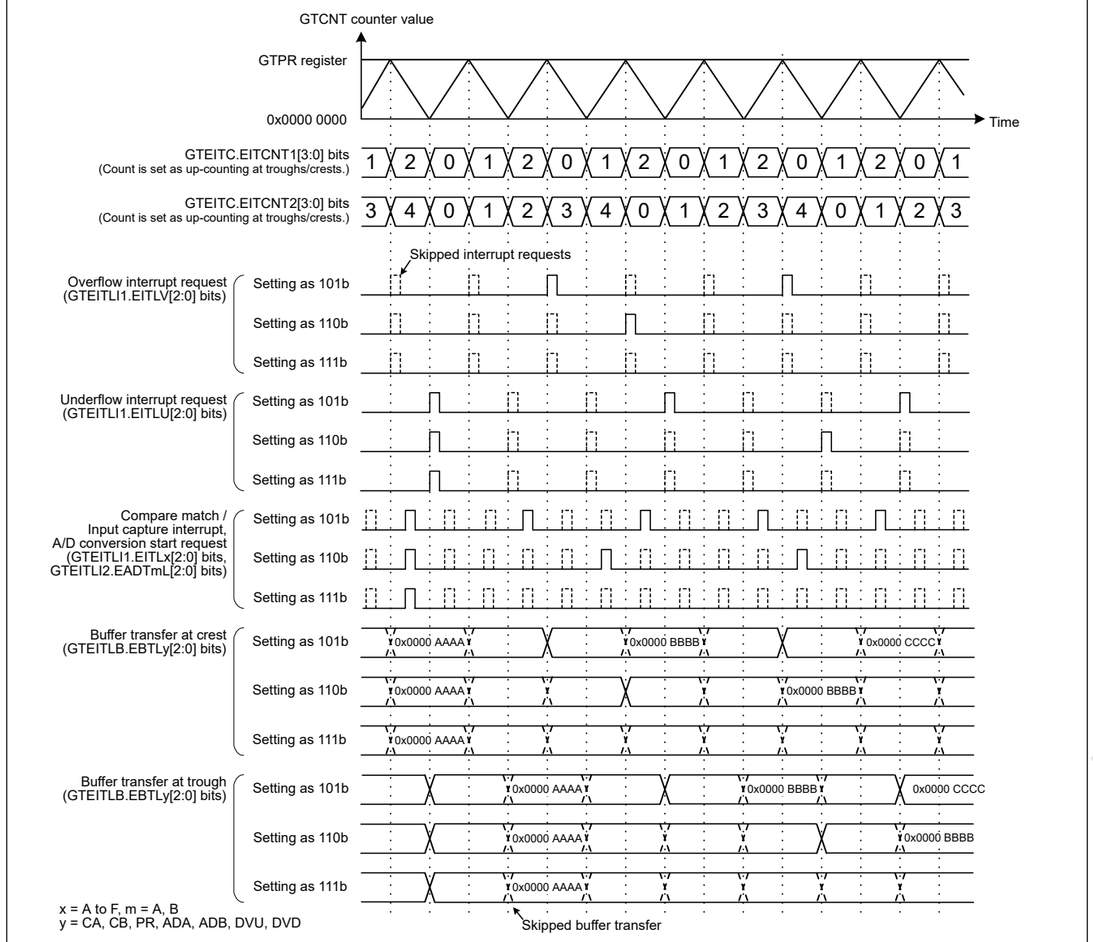


Figure 21.152 Example of Extended Interrupt Skipping Function Operation (Triangle Waves, Counting both Crests and Troughs, Extended Interrupt Skipping 1 Skipping Count: 2, Counting both Crests and Troughs, Extended Interrupt Skipping 2 Skipping Count: 4, Extended Interrupt Skipping Counter 2 Initial Value: 0, Skipped in the Period other than GTEITC.EITCNTk bits (k = 1, 2) as GTEITC.EIVTTk bit.)

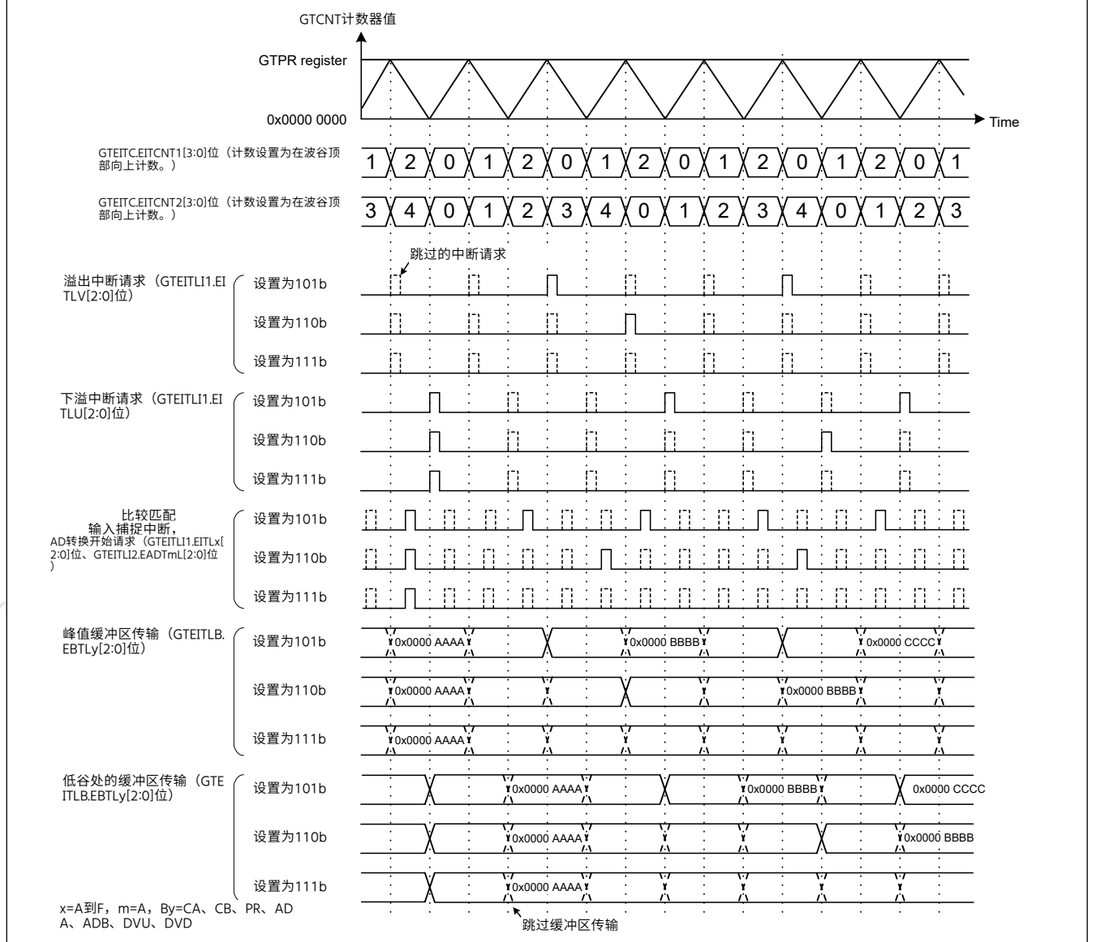


图21.152扩展中断跳过函数操作示例（三角波，同时计数波峰和波谷，扩展中断跳跃1跳跃计数：2，波峰和波谷计数，扩展中断跳跃2跳跃计数：4，扩展中断跳跃计数器2初始值：0，在除GTEITC.EITCNTk位（k=1 2)为GTEITC.EIVTTk bit.)

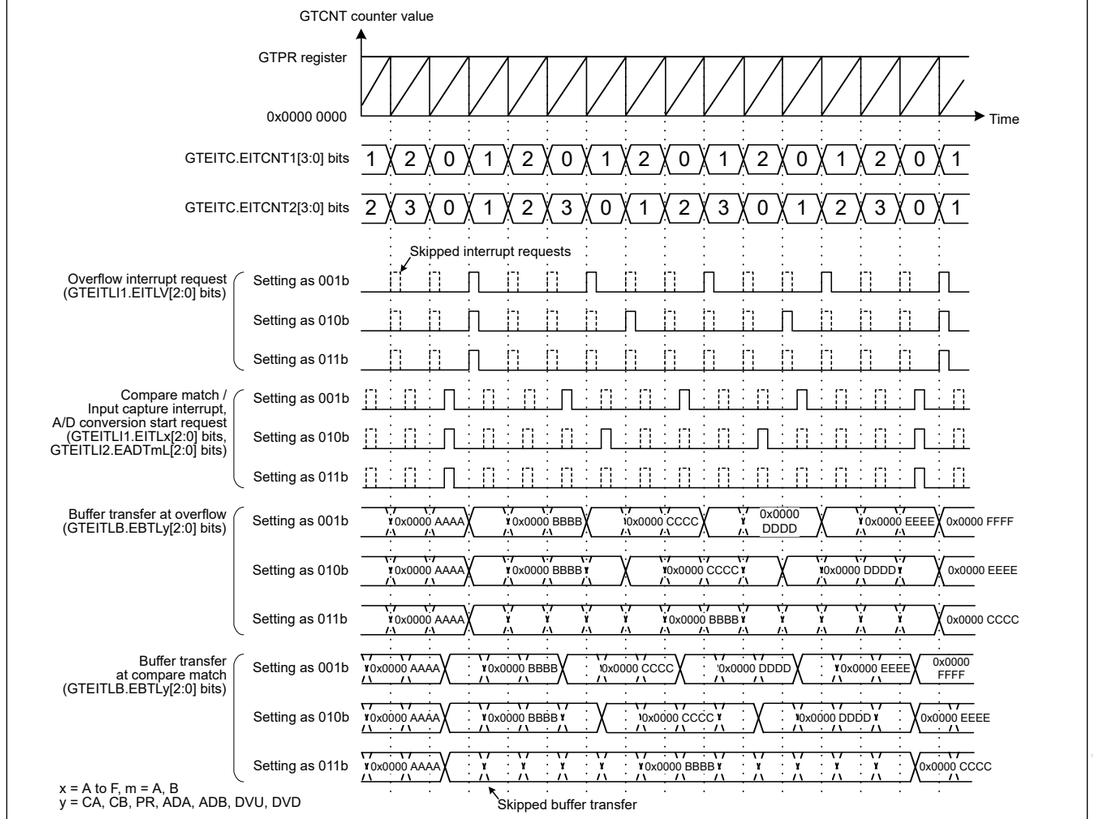


Figure 21.153 Example of Extended Interrupt Skipping Function Operation (Up-Counting in Saw Waves, Counting Overflow, Extended Interrupt Skipping 1 Skipping Count: 2, Counting Overflow, Extended Interrupt Skipping 2 Skipping Count: 3, Extended Interrupt Skipping Counter 2 Initial Value: 0, Skipped in the Period other than GTEITC.EITCNTk bits (k = 1, 2) as 0)

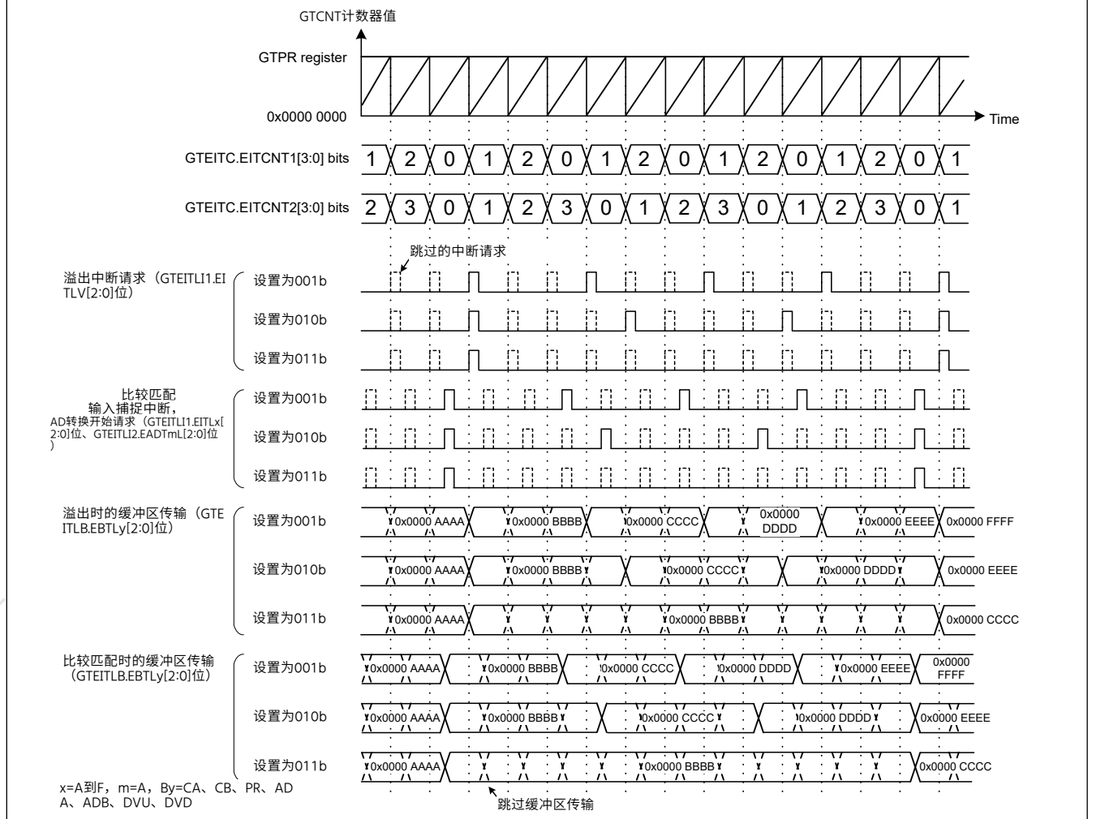


图21.153扩展中断跳过功能操作示例（在锯齿波中向上计数，计数溢出，扩展中断跳过1跳过计数：2，计数溢出，扩展中断跳过2跳过计数：3，扩展中断跳过计数器2初始值：0，在除GTEITC.EITCNTk位（k=1 2）之外的周期中跳过为0）

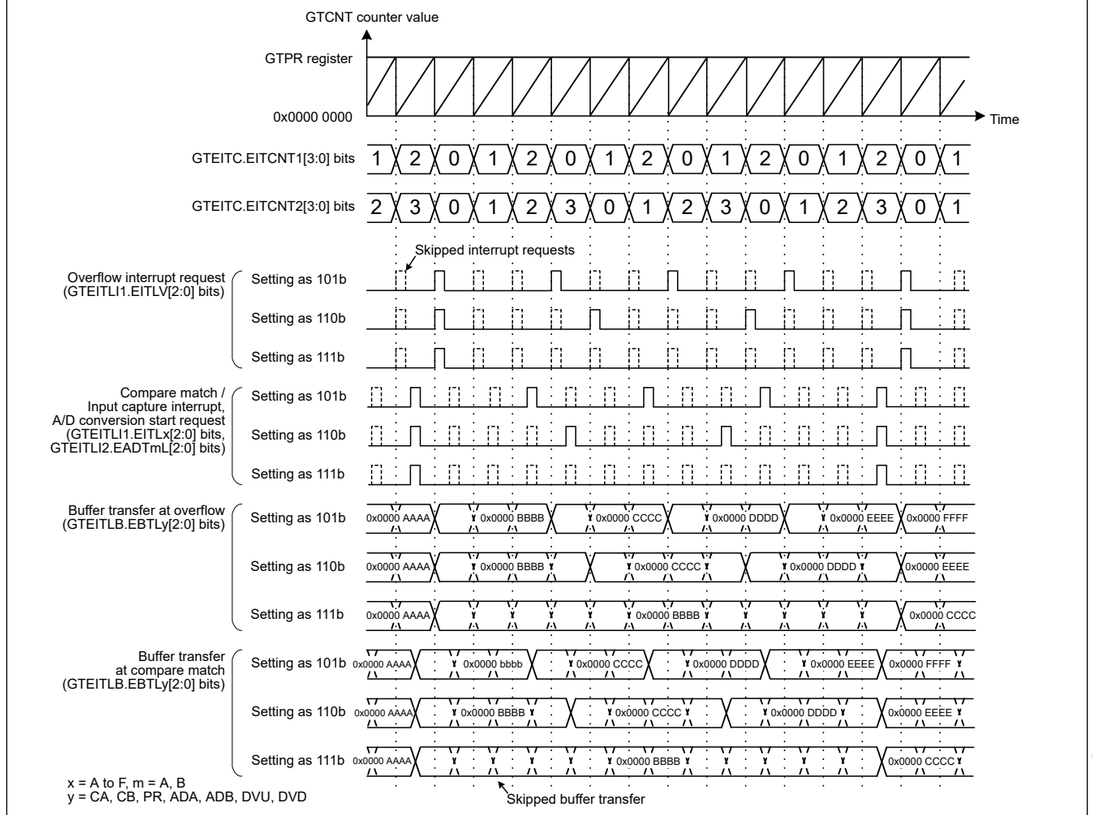


Figure 21.154 Example of Extended Interrupt Skipping Function Operation (Up-Counting Saw Waves, Counting Overflow, Extended Interrupt Skipping 1 Skipping Count: 2, Counting Overflow, Extended Interrupt Skipping 2 Skipping Count: 3, Extended Interrupt Skipping Counter 2 Initial Value: 0, Skipped in the Period other than GTEITC.EITCNTk bits (k = 1, 2) as GTEITC.EIVTTk bits.)

Figure 21.155 shows an example of the extended interrupt skipping operation on the input capture. When the setting is for the input capture operation setting (GTCR.ICDS bit = 0) at count stop of the GTCNT counter, the interrupt by the input capture and the extended skipping on buffer transfer is enabled even at count stop of the GTCNT counter.

When the input capture is generated at count stop of the GTCNT counter by setting the ICDS bit as 0, an interrupt and a buffer transfer are skipped if the skipping counter value is the same with the skipping period set in a corresponding interrupt skipping function select bit.

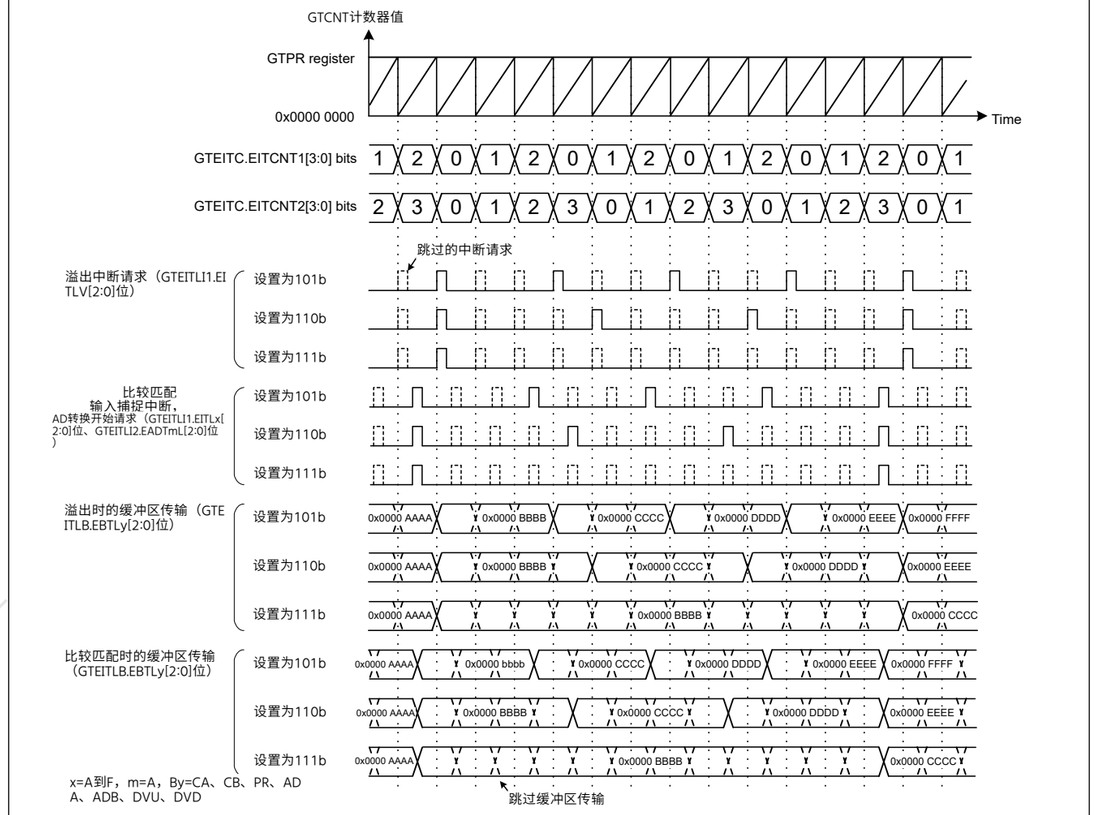


图21.154扩展中断跳过功能操作示例（向上计数锯齿波，计数溢出，扩展中断跳过1跳过计数：2，计数溢出，扩展中断跳过2跳过计数：3，扩展中断跳过计数器2初始值：0，在GTEITC.EITCNTk位(k=1 2)以外的周期中作为GTEITC.EIVTTk位跳过。）

图21.155显示了输入捕捉的扩展中断跳过操作示例。当设置为GTCNT计数器的计数停止时的输入捕捉操作设置（GTCR.ICDS位=0）时，即使在GTCNT计数器的计数停止时，输入捕捉的中断和缓冲区传输的扩展跳过也会使能。

当通过将ICDS位设置为0在GTCNT计数器的计数停止时产生输入捕捉时，如果跳过计数器值与相应中断跳过功能选择位中设置的跳过周期相同，则跳过中断和缓冲区传输.

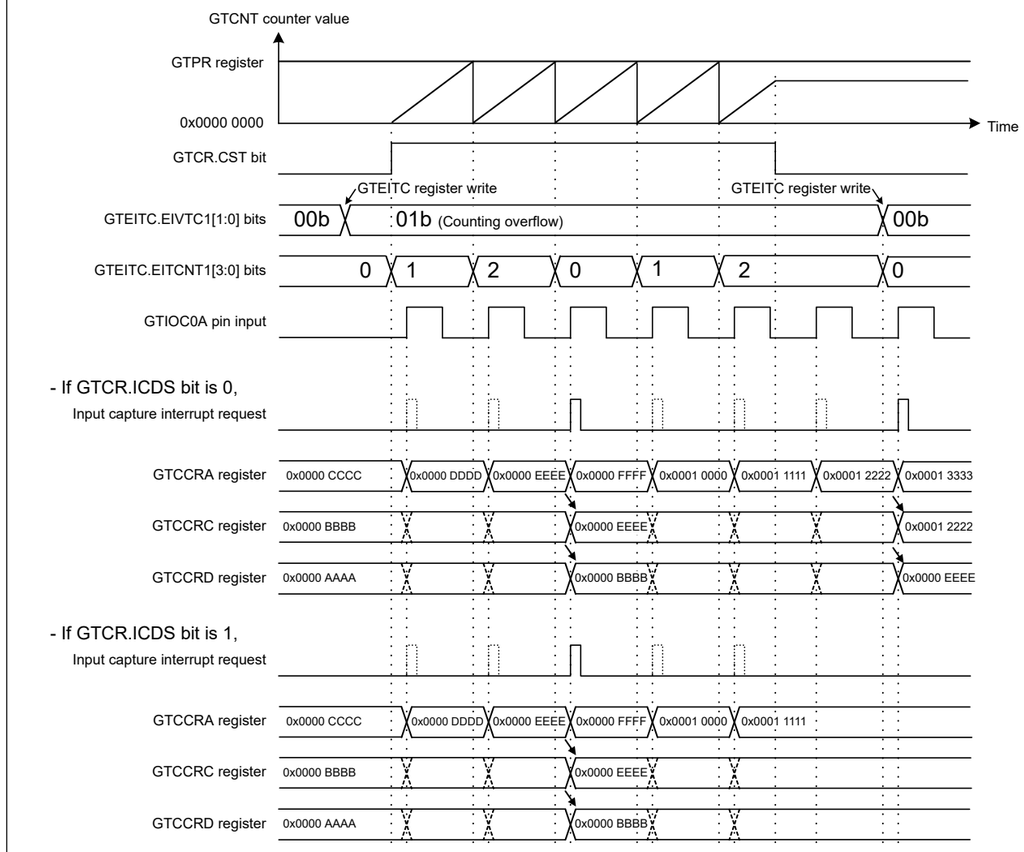


Figure 21.155 Example of Input Capture Operation in the Extended Interrupt Skipping Function Operation (Up-Counting Saw Waves, Counting Overflow, Extended Interrupt Skipping 1 Skipping Count: 2, Skipped in the Period other than the EITCNT1 as 0, Input Capture at the Input Rising)

Table 21.69 shows an example of setting the extended interrupt skipping.

The extended interrupt skipping counter 2 initial value is set by the written value to the ETICNT2IV[3:0] bits which is applied to change the setting from not counting the extended interrupt skipping counter 2 count source (GTEITC.EIVTC2[1:0] bits = 00b) to counting (EIVTC2[1:0] bits = other than 00b). Writing to the extended interrupt skipping counter 2 initial value bit (ETICNT2IV[3:0] bits) is performed only when the setting of the above mentioned extended interrupt skipping counter 2 initial value is written.

Table 21.69 Example for Setting the Extended Interrupt Skipping (1 of 2)

No.	Step Name	Description
1	Set GTCNT counter operation, Set buffer operation, Set compare match value	Refer to section 21.3.2. Buffer Operation, section 21.3.3. PWM Output Operating Mode, and so on.
2	Set the extended interrupt skipping function	Select the skipping counter used for skipping and the skipping period with the skipping function select bit for the interrupt, for the A/D conversion start request, and for a buffer transfer, all which are to be skipped, in the GTEITLI1, GTEITLI2, and GTEITLB registers respectively.

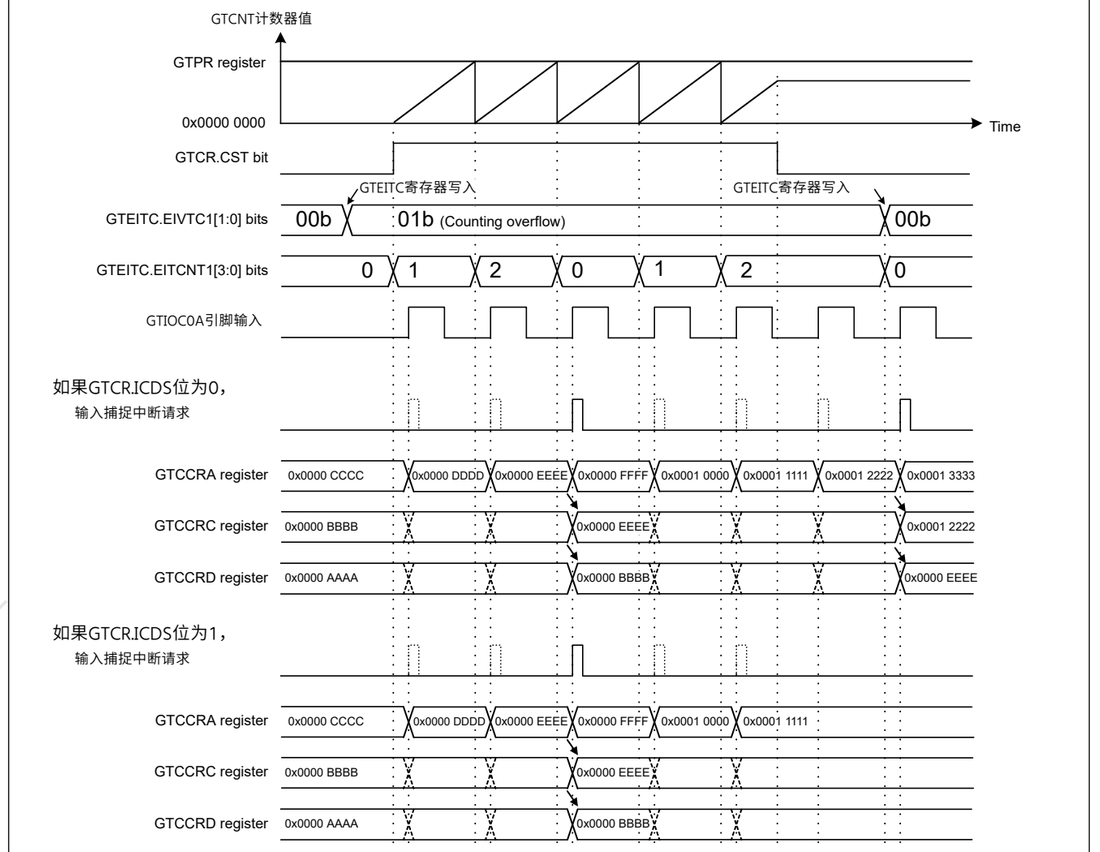


图21.155扩展中断跳过功能操作中的输入捕捉操作示例（向上计数锯齿波、计数溢出、扩展中断跳过1跳过计数：2、在EITCNT1以外的周期中跳过为0、输入上升沿时的输入捕捉）

表21.69显示了设置扩展中断跳过的示例。

扩展中断跳过计数器2的初始值由写入ETICNT2IV[3:0]位的值设置，该值用于将设置从不计算扩展中断跳过计数器2计数源(GTEITC.EIVTC2[1:0]位=00b)到计数（EIVTC2[1:0]位=00b除外）。仅当写入上述扩展中断跳过计数器2初始值的设置时，才会写入扩展中断跳过计数器2初始值位（ETICNT2IV[3:0]位）。

Table 21.69 设置扩展中断跳过的示例(1of2)

No.	步骤名称	Description
1	设置GTCNT计数器操作， 设置缓冲操作， 设置比较匹配值	请参阅第21.3.2节。缓冲区操作，第21.3.3节。PWM输出工作模式等。
2	设置扩展中断跳过功能	在GTEITLI1、GTEITLI2和GTEITLB寄存器中，使用中断、AD转换开始请求和缓冲区传输的跳跃功能选择位选择跳跃计数器和跳跃周期分别。

Table 21.69 Example for Setting the Extended Interrupt Skipping (2 of 2)

No.	Step Name	Description
3	Set the extended skipping counter	With the GTEITC register, set a count source of the skipping counter used for skipping, skipping count, and the skipping counter 2 initial value as the following order. Set EIVTCk[1:0] bits (k = 1,2) as value other than 00b, and set EIVTTk[3:0] bits as value other than 0000b. When the skipping counter 2 is used, change EIVTC2[1:0] bits from 00b to value other than 00b as well as set EITCNT2IV[3:0] bits to the skipping counter 2 initial value.
4	Start count operation	Set GTCR.CST to 1 to start count operation.
5	Set buffer value for each cycle	Refer to section 21.3.2. Buffer Operation, section 21.3.3. PWM Output Operating Mode, and so on.

21.4.3.3 A/D conversion Start Request Compare Match Skipping Function

The A/D conversion start request and GTADTR register buffer transfer can be skipped by counting the compare matches of GTADTRA register and GTADTRB register based on settings of the GTADCMSC register and GTADCMSS register.

The skipping period is set, related to the operation of the two independent A/D conversion start request compare match skipping counters (ADCMSCNT1[3:0] and ADCMSCNT2[3:0] bits in the GTADCMSC register), as a period that either of the counter value for such skipping counters is other than 0 or other than the skipping count. The skipping period can also be set as a period that the both skipping counters are set as other than 0 or other than the skipping count for the counter value.

Figure 21.156 shows the counter operation for A/D conversion start request compare match skipping.

The counter operation for A/D conversion start request compare match skipping is set by the GTADCMSC register.

The ADCMSCNT1[3:0] bits count the count source (in Figure 21.156, a crest is selected) selected by the A/D conversion start request compare match skipping counter 1 count source select bit (GTADCMSC.ADCMSC1[1:0] bits), and repeat the count operation which returns to 0 when the skipping count (in Figure 21.156, count is 2) set by the A/D conversion start request compare match skipping 1 skipping count setting bit (ADCMST1[3:0] bits) is achieved.

The ADCMSCNT2[3:0] bits count the count source (in Figure 21.156, a trough is selected) selected by the A/D conversion start request compare match skipping counter 2 count source select bit (GTADCMSC.ADCMSC2[1:0] bits), and repeat the count operation which returns to 0 when the skipping count (in Figure 21.156, count is 2) set by the A/D conversion start request compare match skipping 2 skipping count setting bit (ADCMST2[3:0] bits) is achieved.

The ADCMSCNTk[3:0] bits (k = 1, 2) can be set for the initial value. The initial value is set when the GTADCMSC register is written by the access of 16 bits or 32 bits while the setting for the A/D conversion start request compare match skipping counter k is not counted (ADCMSCk [1:0] bits are 00b) and the write value to the ADCMSCk[1:0] bits is other than 00b. When the initial value is set, the write value to the A/D conversion start request compare match skipping counter k initial value bits (ADCMSCNTkIV[3:0] bits) are set as the initial value for the ADCMSCNT2[3:0] bits.

The A/D conversion start request compare match skipping counter starts up-counting at the first count clock after the setting is modified from not counting to counting.

The ADCMSCNT1[3:0] and ADCMSCNT2[3:0] bits for the A/D conversion start request compare match skipping function retain the value even after the GTCNT counter operation is stopped, and the counting can be resumed from the value before the counter is stopped. When values for the ADCMSCNT1[3:0] and ADCMSCNT2[3:0] bits are to be reset (0000b), set the ADCMSC1[1:0] and ADCMSC2[1:0] bits to the setting for not counting (not skipping) (00b).

When the skipping count is to be changed, change the count after stopping the skipping counter operation (set either of the ADCMSC1[1:0] bit or the ADCMSC 2[1:0] bit to 00b).

Table 21.69 设置扩展中断跳过的示例(2of2)

No.	步骤名称	Description
3	设置扩展跳过计数器	使用GTEITC寄存器，按以下顺序设置用于跳跃的跳跃计数器的计数源、跳跃计数和跳跃计数器2的初始值。将EIVTCk[1:0]位(k=1 2)设置为00b以外的值，并将EIVTTk[3:0]位设置为0000b以外的值。使用跳跃计数器2时，将EIVTC2[1:0]位从00b更改为00b以外的值，并将EITCNT2IV[3:0]位设置为跳跃计数器2的初始值。
4	开始计数操作	将GTCR.CST设置为1以启动计数操作。
5	为每个周期设置缓冲区值	请参阅第21.3.2节。缓冲区操作，第21.3.3节。PWM输出工作模式等。

21.4.3.3 AD转换开始请求比较匹配跳过功能

AD转换开始请求和GTADTR寄存器缓冲传输可以通过计算比较匹配来跳过
GTADTRA寄存器和GTADTRB寄存器基于GTADCMSC寄存器和GTADCMSS寄存器的设置。

设置跳跃周期，与两个独立的AD转换开始请求比较匹配跳跃计数器（GTADCMSC寄存器中的ADCMSCNT1[3:0]和ADCMSCNT2[3:0]位）的操作有关，作为此类跳过计数器的计数器值不是0或不是跳过计数。也可以将跳过时间段设置为两个跳过计数器设置为0以外的时间段或设置为计数器值的跳过次数以外的时间段。

图21.156显示了AD转换开始请求比较匹配跳过的计数器操作。

AD转换开始请求比较匹配跳过的计数器操作由GTADCMSC寄存器设置。

ADCMSCNT1[3:0]位对由AD转换开始请求比较匹配跳过计数器1计数源选择位（GTADCMSC.ADCMSC1[1:0]位）选择的计数源（在图21.156中，选择一个波峰）进行计数，并重复计数操作，当达到由AD转换开始请求比较匹配跳过1跳过计数设置位（ADCMST1[3:0]位）设置的跳过计数（在图21.156中，计数为2）时，计数操作返回0。

ADCMSCNT2[3:0]位计数由AD转换开始请求比较匹配跳过计数器2计数源选择位（GTADCMSC.ADCMSC2[1:0]位）选择的计数源（在图21.156中，选择了一个波谷），并重复计数操作，当达到由AD转换开始请求比较匹配跳过2跳过计数设置位（ADCMST2[3:0]位）设置的跳过计数（在图21.156中，计数为2）时，计数操作返回0。

ADCMSCNTk[3:0]位(k=1 2)可设置为初始值。当通过16位或32位访问写入GTADCMSC寄存器时设置初始值，同时不计算AD转换开始请求比较匹配跳过计数器k的设置（ADCMSCk[1:0]位为00b）并且向ADCMSCk[1:0]位写入的值不是00b。设置初始值时，将写入AD转换开始请求比较匹配跳过计数器k初始值位（ADCMSCNTkIV[3:0]位）的值设置为ADCMSCNT2[3:0]位的初始值。

AD转换开始请求比较匹配跳过计数器在设置从不计数修改为计数后的第一个计数时钟开始向上计数。

AD转换开始请求比较匹配跳过功能的ADCMSCNT1[3:0]和ADCMSCNT2[3:0]位即使在GTCNT计数器操作停止后仍保持该值，并且可以从计数器之前的值恢复计数停了下来。当ADCMSCNT1[3:0]和ADCMSCNT2[3:0]位的值要复位(0000b)时，将ADCMSC1[1:0]和ADCMSC2[1:0]位设置为不计数的设置（不跳过）（00b）。

如果要更改跳跃计数，请在停止跳跃计数器操作后更改计数（设置任一ADCMSC1[1:0]位或ADCMSC2[1:0]位到00b)。

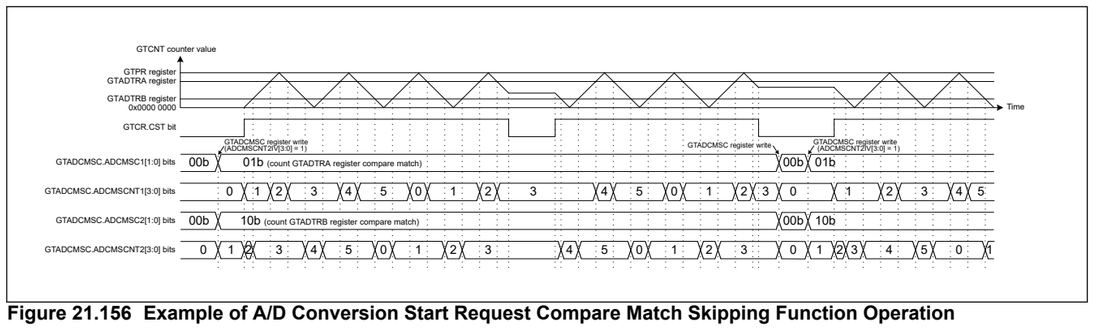


Figure 21.156 Example of A/D Conversion Start Request Compare Match Skipping Function Operation

A/D conversion start request skipping by the ADCMSC register can be performed simultaneously with skipping by the GTITC register or GTEITC register. A skipping period in this case is represented by OR-ed skipping periods of respective registers.

Figure 21.157 shows corresponding interrupt skipping operations and A/D conversion start request skipping operation are performed simultaneously.

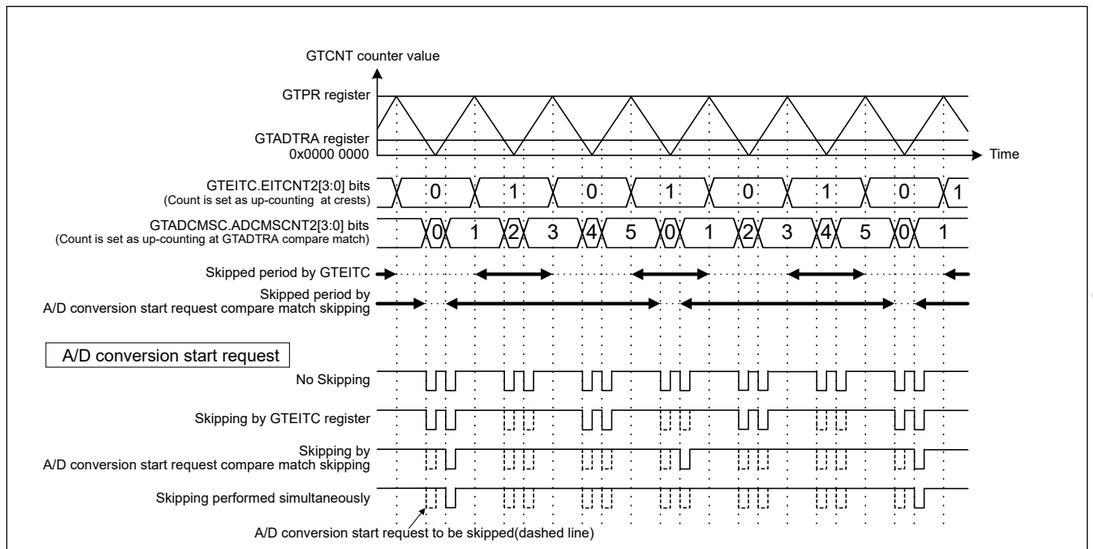


Figure 21.157 Example of A/D Conversion Start Request Compare Match Skipping Function Operation (Extended Interrupt Skipping: EIVTC2[1:0] = 01b, EADTAL[2:0] = 010b, A/D Conversion Start Request Compare Match Skipping: ADCMSC2[1:0] = 01b, ADCMSAL[2:0] = 010b)

When A/D conversion start request skipping which can be set by the GTADCMSS register is performed, updating of status flag and the ELC event output depend on the A/D conversion start request enable bit in the GTINTAD register. All the operations by A/D conversion start request which are set as disable by the GTINTAD register is not performed.

A buffer transfer skipping by the GTADCMSS register is performed in all of buffer operation which is enabled in the GTBER and GTBER2 register, or all buffer operations performed by saw-wave one-shot pulse mode or triangle-wave PWM mode 3 or complementary PWM mode(excludes buffer transfer from GTCCRC, GTCCRE to GTCCRA).

An A/D conversion start request skipping and a buffer transfer skipping are operated individually.

Figure 21.158, Figure 21.159 show examples of extended skipping function operation.

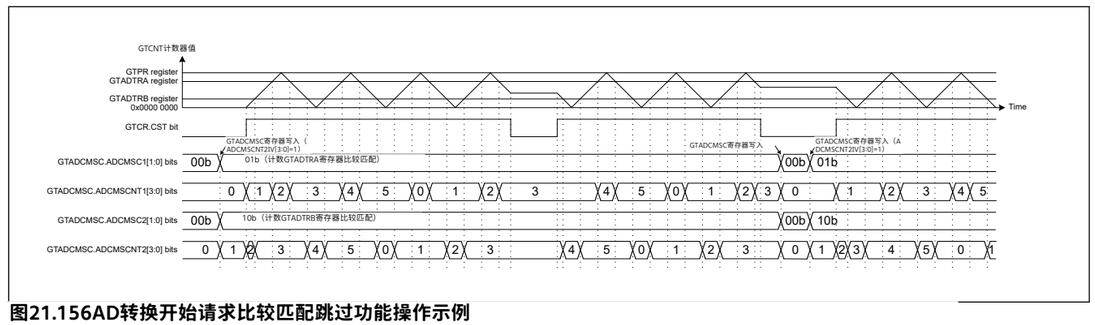


图21.156AD转换开始请求比较匹配跳过功能操作示例

ADCMSC寄存器跳过的D转换开始请求可以与
GTITC寄存器或GTEITC寄存器。这种情况下的跳跃周期由各个寄存器的或运算跳跃周期表示。

图21.157显示了相应的中断跳过操作和AD转换开始请求跳过操作同时执行。

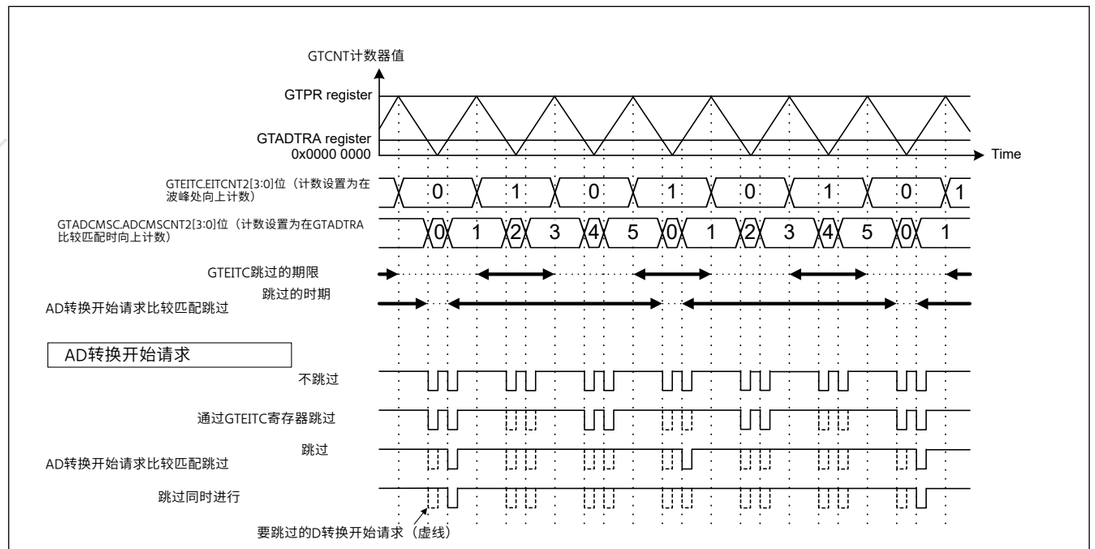


图21.157AD转换开始请求比较匹配跳过功能操作示例（扩展中断跳过：EIVTC2[1:0]=01b，EADTAL[2:0]=010b，AD转换开始请求比较匹配跳过：ADCMSC2[1:0]=01b，ADCMSAL[2:0]=010b）

当执行可由GTADCMSS寄存器设置的AD转换开始请求跳过时，状态标志和ELC事件输出的更新取决于GTINTAD寄存器中的AD转换开始请求使能位。由GTINTAD寄存器设置为禁用的AD转换开始请求的所有操作均不执行。

GTADCMSS寄存器的缓冲区传输跳过在所有缓冲区操作中执行，该操作在GTBER和GTBER2寄存器，或由锯齿波单次脉冲模式或三角波PWM模式3或互补PWM模式执行的所有缓冲区操作（不包括从GTCCRC、GTCCRE到GTCCRA的缓冲区传输）。

AD转换开始请求跳过和缓冲区传送跳过是单独操作的。

图21.158、图21.159显示了扩展跳过功能操作的示例。

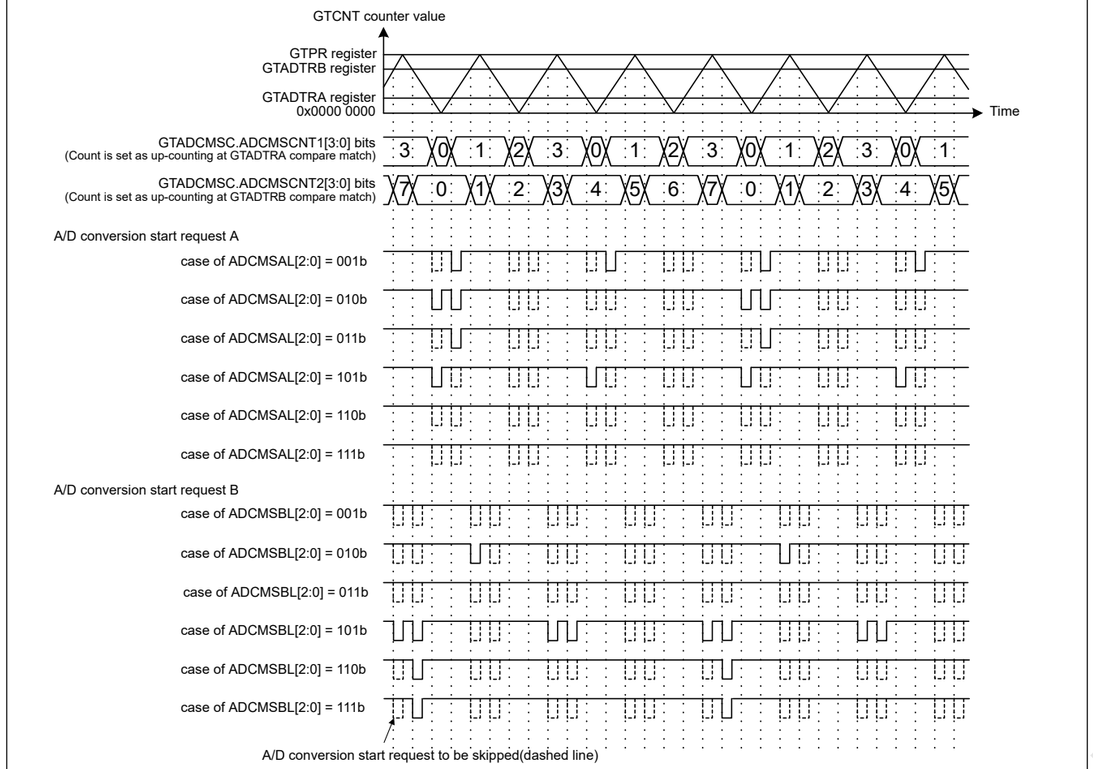


Figure 21.158 Example of A/D Conversion Start Request Compare Match Skipping Function Operation (Triangle wave, A/D Conversion Start Request Compare Match Skipping 1 Skipping Count: 3 Counting GTADTRA compare match, A/D Conversion Start Request Compare Match Skipping 2 Skipping Count: 7 Counting GTADTRB compare match)

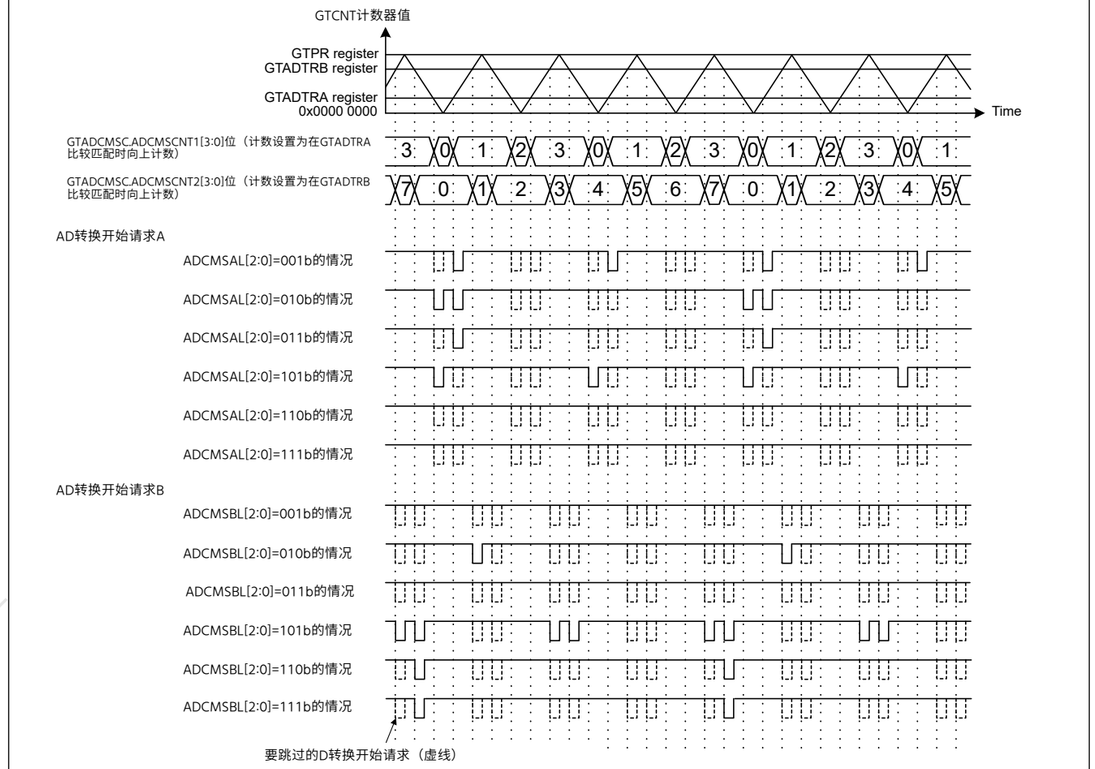


图21.158AD转换开始请求比较匹配跳过功能操作示例
（三角波，AD转换开始请求比较匹配跳过1跳过计数：3计数GTADTRA比较匹配，AD转换开始请求比较匹配跳过2
跳过计数：7计数GTADTRB比较匹配）

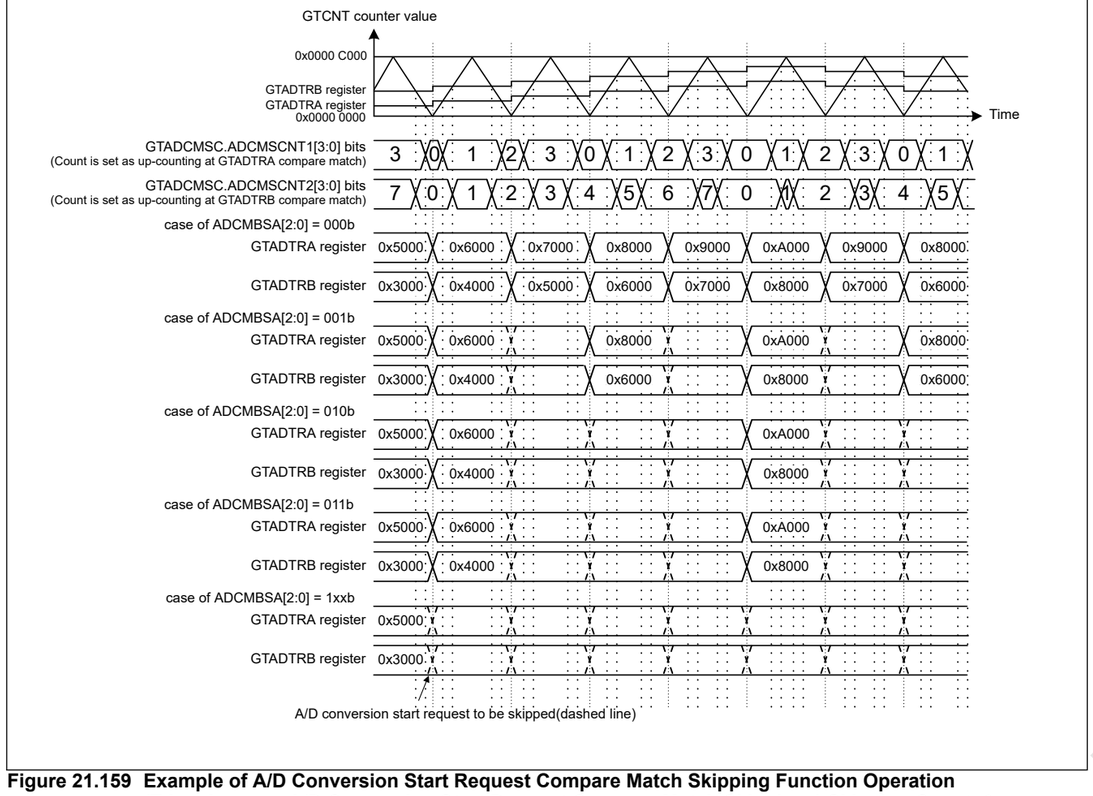


Figure 21.159 Example of A/D Conversion Start Request Compare Match Skipping Function Operation (Triangle wave, A/D Conversion Start Request Compare Match Skipping 1 Skipping Count: 3 Counting GTADTRA compare match, A/D Conversion Start Request Compare Match Skipping 2 Skipping Count: 7 Counting GTADTRB compare match, Buffer transfer of GTADTRA and GTADTRB at trough)

Table 21.70 shows an example of setting the A/D conversion start request compare match skipping.

The A/D conversion start request compare match skipping counter 2 initial value is set by the written value to the ADCMSCNT2IV[3:0] bits which is applied to change the setting from not counting the extended interrupt skipping counter 2 count source (GTADCMSC.ADCMSC2[1:0] bits = 00b) to counting (ADCMSC2[1:0] bits = other than 00b). Writing to the A/D conversion start request compare match skipping counter 2 initial value bit (ADCMSCNT2IV[3:0] bits) is performed only when the setting of the above mentioned A/D conversion start request compare match skipping counter 2 initial value is written.

Table 21.70 Example for Setting the A/D Conversion Start Request Compare Match Skipping (1 of 2)

No.	Step Name	Description
1	Set GTCNT counter operation, Set buffer operation, Set compare match value	Refer to section 21.3.2. Buffer Operation, section 21.3.3. PWM Output Operating Mode, section 21.5. A/D Conversion Start Request, and so on.
2	Set the A/D conversion start request compare match skipping function	Select the skipping counter and the skipping period with the skipping function select bit for the A/D conversion start request or the bit for the buffer transfer to be skipped in the GTADCMSS register.

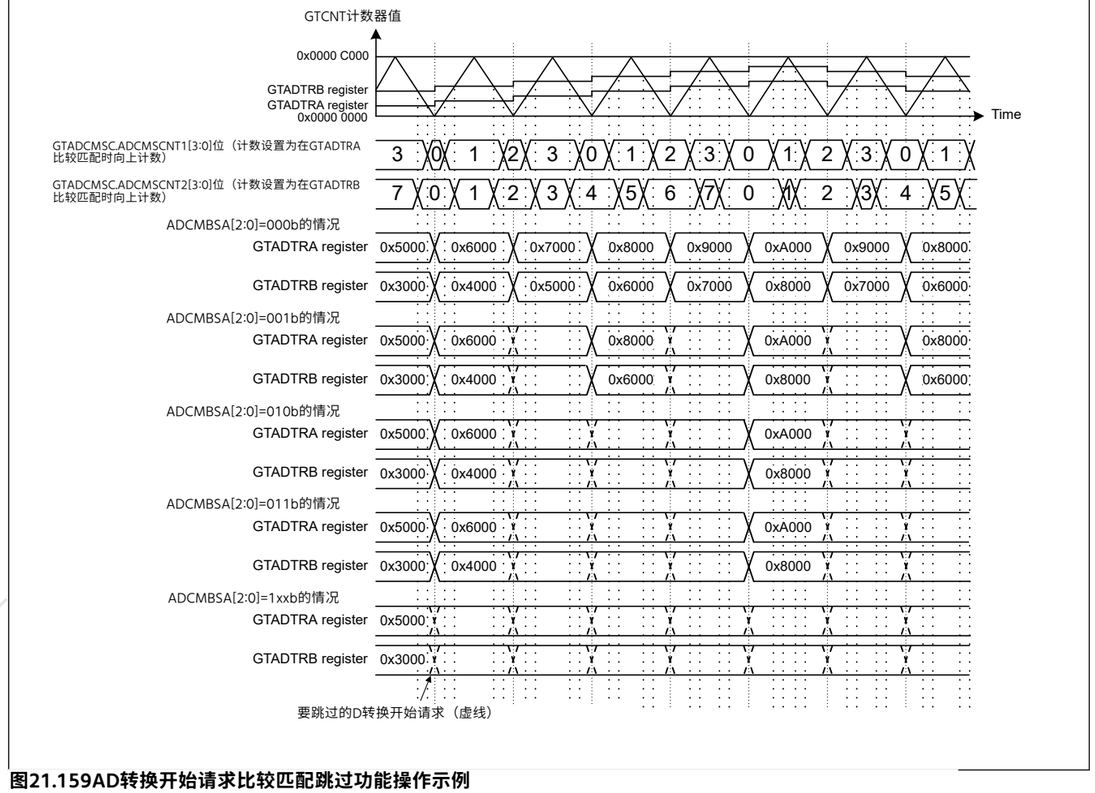


图21.159AD转换开始请求比较匹配跳过功能操作示例
（三角波，AD转换开始请求比较匹配跳过1跳过计数：3计数GTADTRA比较匹配，AD转换开始请求比较匹配跳过2
跳过计数：7计数GTADTRB比较匹配，GTADTRA的缓冲区传输和
GTADTRB at trough)

表21.70显示了设置AD转换开始请求比较匹配跳过的示例。

AD转换开始请求比较匹配跳过计数器2的初始值由写入的值设置到ADCMSCNT2IV[3:0]位用于将设置从不计数扩展中断跳过计数器2计数源(GTADCMSC.ADCMSC2[1:0]位=00b)更改为计数(ADCMSC2[1:0]位=其他大于00b)。仅当写入上述AD转换开始请求比较匹配跳过计数器2初始值的设置时，才会写入AD转换开始请求比较匹配跳过计数器2初始值位（ADCMSCNT2IV[3:0]位）。

Table 21.70 设置AD转换开始请求比较匹配跳过的示例(1of2)

No.	步骤名称	Description
1	设置GTCNT计数器操作， 设置缓冲操作， 设置比较匹配值	请参阅第21.3.2节。缓冲区操作，第21.3.3节。PWM输出操作模式，第21.5节。AD转换开始请求，等等。
2	设置AD转换开始请求比较匹配跳过功能	通过AD转换开始请求的跳跃功能选择位或GTADCMSS寄存器中要跳跃的缓冲区传输位选择跳跃计数器和跳跃周期。

Table 21.70 Example for Setting the A/D Conversion Start Request Compare Match Skipping (2 of 2)

No.	Step Name	Description
3	Set the A/D conversion start request compare match skipping counter k (k = 1, 2)	With the GTADCMSC register, set a count source of the skipping counter, skipping count, and the skipping counter k initial value as the following order. Set the GTADCMSC.ADCMSCk[1:0] bits as value other than 00b, and set the ADCMSTk[3:0] bits as value other than 0000b. Change the ADCMSCk[1:0] bits from 00b to value other than 00b as well as set the ADCMSCNTkIV[3:0] bits to the skipping counter k initial value.
4	Start count operation	Set GTCR.CST to 1 to start count operation.
5	Set buffer value for each cycle	Refer to section 21.3.2. Buffer Operation, section 21.3.3. PWM Output Operating Mode, section 21.5. A/D Conversion Start Request, and so on.

21.5 A/D Conversion Start Request

The A/D conversion start request can be issued at a compare match between the GTCNT counter and the GTADTRA or GTADTRB register. Up-counting only, down-counting only, or both up-counting and down-counting can be specified by setting the GTINTAD register.

In complementary PWM mode, the A/D conversion start request can be issued at a compare match with the GTCNT counter of master channel.

During event count operation, the A/D conversion start request can not be generated.

The A/D conversion start request is output as event signals to ELC.

The GTADTRA and GTADTRB registers each has two buffer registers. Buffer operation with the GTADTRA register used together with the GTADTBRA and GTADTDBRA registers, and buffer operation with the GTADTRB register used together with the GTADTBRB and GTADTDBRB registers can be performed.

The timing of the generation of requests to start A/D conversion can be monitored by an external pin. When the A/D conversion start request signal to be monitored is selected in the GTADSMR.ADSMSk bit (k = 0, 1) and when the output is enabled in the ADSMENk bit, a signal is output synchronized with a cycle frame of the timer used to generate the A/D conversion start request signal, of which the output is driven high at the generation of the A/D conversion start request signal by the GTADSMk pin, or at the end of the cycle of which the output is driven low. When a signal to request the start of A/D conversion is generated at the end of the cycle, the generation of this signal has priority in terms of monitoring output and the output remains at the high level till the end of the next cycle. The registers (GTADTRA and GTADTRB) that are sources of generating the A/D conversion start request signals and their counting directions can be checked by the A/D conversion start request flags (ADTRAUF, ADTRADF, ADTRBUF, and ADTRBDF) in the GTST register. When the output of the same A/D conversion start request signal monitoring output is enabled for multiple channels, ORed signals will be output from the GPT32.

Figure 21.160 shows an example of A/D conversion start request operation, Table 21.71 shows example for setting A/D conversion start request operation.

Table 21.70 设置AD转换开始请求比较匹配跳过的示例(2of2)

No.	步骤名称	Description
3	设置AD转换开始请求比较匹配跳过计数器k(k=1 2)	使用GTADCMSC寄存器，按以下顺序设置跳跃计数器的计数源、跳跃计数和跳跃计数器k初始值。 将GTADCMSC.ADCMSCk[1:0]位设置为00b以外的值，并将ADCMSTk[3:0]位设置为0000b以外的值。将ADCMSCk[1:0]位从00b更改为00b以外的值，并设置 ADCMSCNTkIV[3:0]位到跳跃计数器k的初始值。
4	开始计数操作	将GTCR.CST设置为1以启动计数操作。
5	为每个周期设置缓冲区值	请参阅第21.3.2节。缓冲区操作，第21.3.3节。PWM输出操作模式，第21.5节。AD转换开始请求，等等。

21.5 AD转换开始请求

可以在GTCNT计数器与GTADTRA或GTADTRB寄存器之间的比较匹配时发出AD转换开始请求。通过设置GTINTAD寄存器，可以指定仅递增计数、仅递减计数或同时递增计数和递减计数。

在互补PWM模式下，可以在与主通道的GTCNT计数器比较匹配时发出AD转换开始请求。

在事件计数操作期间，不能产生AD转换开始请求。

AD转换开始请求作为事件信号输出到ELC。

GTADTRA和GTADTRB寄存器各有两个缓冲寄存器。可以使用与GTADTBRA和GTADTDBRA寄存器一起使用的GTADTRA寄存器进行缓冲操作，以及使用与GTADTBRB和GTADTDBRB寄存器一起使用的GTADTRB寄存器进行缓冲操作。

可以通过外部引脚监控开始AD转换的请求的生成时间。当在GTADSMR.ADSMSk位(k=0 1)中选择要监视的AD转换开始请求信号并且在ADSMENk位中使能输出时，将输出与用于定时器的周期帧同步的信号。产生AD转换开始请求信号，其输出在GTADSMk引脚产生AD转换开始请求信号时被驱动为高电平，或者在输出被驱动为低电平的周期结束时被驱动为高电平。当在周期结束时产生请求开始AD转换的信号时，该信号的产生在监视输出方面具有优先权，并且输出保持高电平直到下一个周期结束。可以通过GTST寄存器中的AD转换开始请求标志（ADTRAUF、ADTRADF、ADTRBUF和ADTRBDF）检查作为产生AD转换开始请求信号的源的寄存器（GTADTRA和GTADTRB）及其计数方向。当多个通道的相同AD转换开始请求信号监视输出启用时，将从GPT32输出ORed信号。

图21.160显示了AD转换启动请求操作的示例，表21.71显示了设置AD转换启动请求操作的示例。

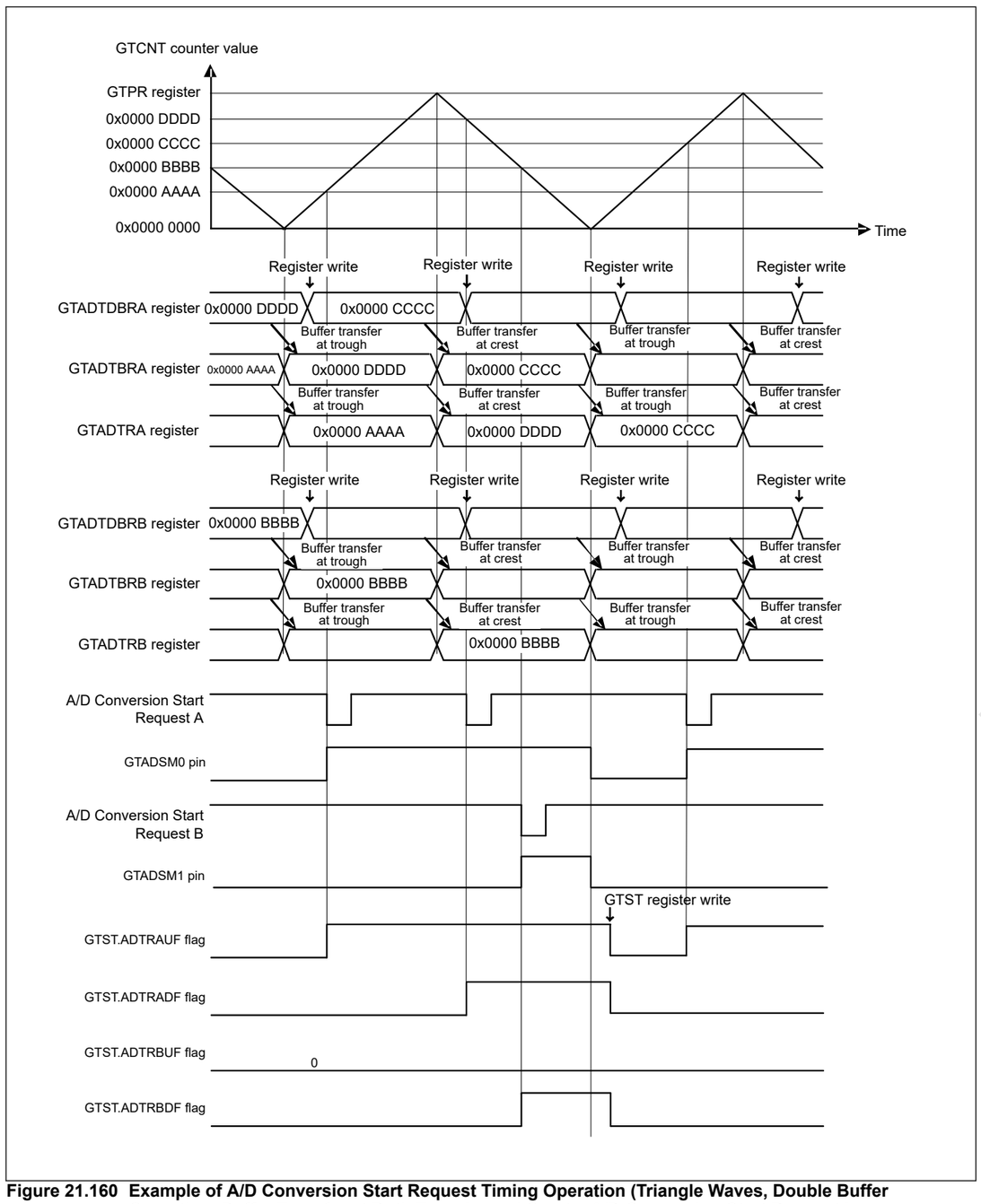


Figure 21.160 Example of A/D Conversion Start Request Timing Operation (Triangle Waves, Double Buffer Operation, Buffer Transfer at Both Troughs and Crests, A/D Conversion Start Request by GTADTRA Register at Both Up-Counting and Down-Counting, A/D Conversion Start Request by GTADTRB Register at Down-Counting, Monitoring of the GTADTRA Register Up-Counting by the GTADSM0 Pin, Monitoring of the GTADTRB Register Down-Counting by the GTADSM1 Pin)

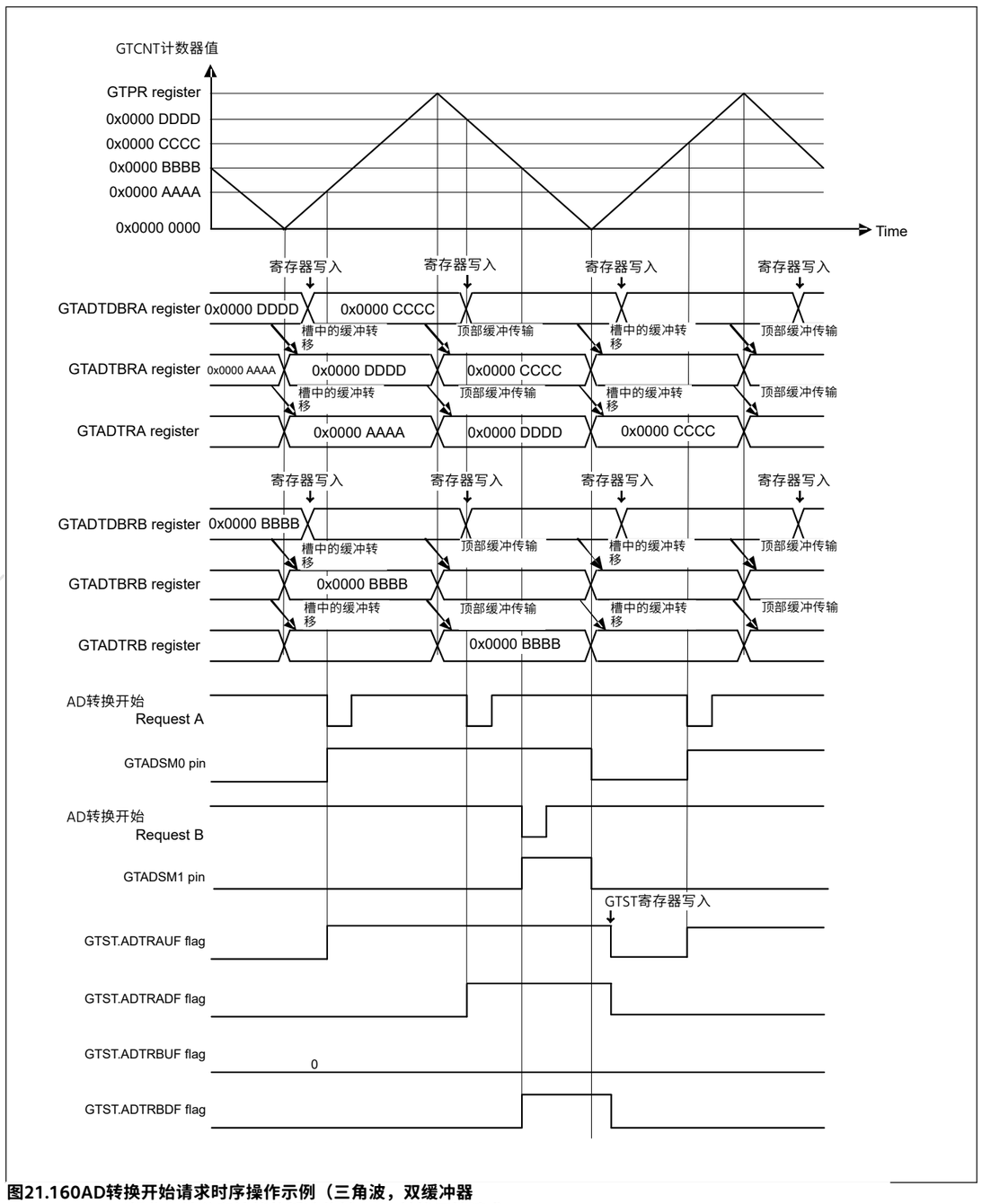


图21.160AD转换开始请求时序操作示例（三角波，双缓冲器操作，波谷和波峰的缓冲传输，AD转换开始请求向上计数和向下计数时的GTADTRA寄存器，向下计数时由GTADTRB寄存器发出的AD转换开始请求，通过GTADSM0引脚监控GTADTRA寄存器向上计数，通过GTADSM1引脚监控GTADTRB寄存器向下计数）

Table 21.71 Example for Setting A/D Conversion Start Request Timing Operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.160, 100b, 101b, or 110b (0100b, 0101b, or 0110b) (triangle-wave PWM mode) is set.
2	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
3	Set cycle	Set the cycle in the GTPR register.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set buffer operation	Set buffer operation with the ADTTA[1:0], ADTTB[1:0], ADTDA, and ADTDB bits in the GTBER register. In Figure 21.160, ADTTA[1:0] = 11b, ADTTB[1:0] = 11b, ADTDA = 1, and ADTDB = 1.
6	Set compare match value	Set the A/D conversion start request point in the GTADTRA and GTADTRB registers.
7	Set buffer value	For buffer operation, set the A/D conversion start request point in one cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTBRA and GTADTBRB registers. For double buffer operation, also set the A/D conversion start request point in two cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or one cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTDBRA and GTADTDBRB registers.
8	Set A/D conversion start request for monitoring	Select the A/D conversion start request signal to be monitored with ADSMS0[1:0] and ADSMS1[1:0] bits in GTADSMR from GTADSM0 and GTADSM1 pins and enable output of the A/D conversion start request signal being monitored to ADSMEN0 and ADSMEN1 bits in GTADSMR. In Figure 21.160, ADSMS0[1:0] = 00b, ADSMS1[1:0] = 11b, ADSMEN0 = 1, and ADSMEN1 = 1.
9	Enable A/D conversion start request	Set to enable A/D conversion start request with the ADTRAUEN, ADTRADEN, ADTRBUEN, and ADTRBDEN bits in the GTINTAD register. In Figure 21.160, ADTRAUEN = 1, ADTRADEN = 1, ADTRBUEN = 0, and ADTRBDEN = 1.
10	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
11	Set buffer value for each cycle	For buffer operation, set the A/D conversion start request point in one cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTBRA and GTADTBRB registers. For double buffer operation, also set the A/D conversion start request point in two cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or one cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTDBRA and GTADTDBRB registers.

Figure 21.161 shows an example for A/D conversion start request timing operation.

This shows an example of the output of A/D conversion start request A by the ELC as start source 0 (ELC_AD00) for the A/D converter. The A/D conversion start request A signal is output by the ELC in response to a match in comparison with the GTADTRA register.

The same timing applies when the A/D conversion start request A signal from GPT is directly input to ADC without going through ELC.

If GPT is operating with PCLKD and ADC is operating with PCLKA, A/D conversion start request A is passed to ELC on the next rising edge of PCLKA.

If GPT is operating with GPTCLK and ADC is also operating with GPTCLK, A/D conversion start request A is passed to ELC without delay.

For all other clock combinations, A/D conversion start request A is synchronized and passed to ELC.

Table 21.71 设置AD转换开始请求时序操作的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]位或GTCR.MD[3:0]位设置操作模式。 在图21.160中，设置了100b、101b或110b（0100b、0101b或0110b）（三角波PWM模式）。
2	选择计数时钟	使用GTCR.TPCS[3:0]位选择计数时钟。
3	设置周期	在GTPR寄存器中设置周期。
4	设置计数器的初始值	在GTCNT计数器中设置初始值。
5	设置缓冲操作	使用GTBER寄存器中的ADTTA[1:0]、ADTTB[1:0]、ADTDA和ADTDB位设置缓冲区操作。在图21.160中，ADTTA[1:0]=11b，ADTTB[1:0]=11b，ADTDA=1，ADTDB=1。
6	设置比较匹配值	在GTADTRA和GTADTRB寄存器中设置AD转换开始请求点。
7	设置缓冲区值	对于缓冲操作，将AD转换开始请求点设置在当前周期后的一个周期（锯齿波模式或三角波模式，在波谷或波峰处缓冲传输）或当前周期后的半个周期（三角波模式GTADTBRA和GTADTBRB寄存器中的波谷和波峰缓冲传输）。 对于双缓冲操作，还要在当前周期后的两个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的一个周期（在三角波模式下）设置AD转换开始请求点GTADTDBRA和GTADTDBRB寄存器中的波谷模式和波峰缓冲传输）。
8	设置监控用AD转换开始请求	使用ADSMS0[1:0]选择要监视的AD转换开始请求信号，然后来自GTADSM0和GTADSM1引脚的GTADSMR中的ADSMS1[1:0]位，并允许将被监视的AD转换开始请求信号输出到GTADSMR中的ADSMEN0和ADSMEN1位。在图21.160中，ADSMS0[1:0]=00b，ADSMS1[1:0]=11b，ADSME0=1，ADSME1=1。
9	启用AD转换启动请求	通过ADTRAUEN、ADTRADEN、ADTRBUEN和GTINTAD寄存器中的ADTRBDEN位。 在图21.160中，ADTRAUEN=1、ADTRADEN=1、ADTRBUEN=0和ADTRBDEN=1。
10	开始计数操作	将GTCR.CST位设置为1以启动计数操作。
11	为每个周期设置缓冲区值	对于缓冲操作，将AD转换开始请求点设置在当前周期后的一个周期（锯齿波模式或三角波模式，在波谷或波峰处缓冲传输）或当前周期后的半个周期（三角波模式GTADTBRA和GTADTBRB寄存器中的波谷和波峰缓冲传输）。 对于双缓冲操作，还要在当前周期后的两个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的一个周期（在三角波模式下）设置AD转换开始请求点GTADTDBRA和GTADTDBRB寄存器中的波谷模式和波峰缓冲传输）。

图21.161显示了AD转换开始请求时序操作的示例。

这显示了ELC作为AD转换器的启动源0(ELC_AD00)输出AD转换启动请求A的示例。AD转换开始请求A信号由ELC输出，以响应与GTADTRA寄存器的比较匹配。

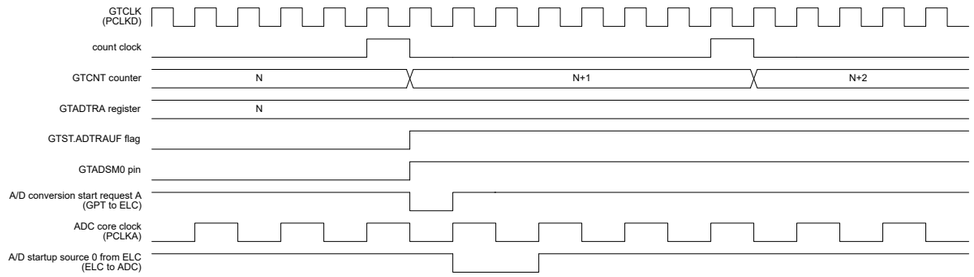
当来自GPT的AD转换开始请求A信号不经过ELC直接输入到ADC时，同样的时序也适用。

如果GPT使用PCLKD运行，而ADC使用PCLKA运行，则AD转换开始请求A在PCLKA的下一个上升沿传递给ELC。

如果GPT使用GPTCLK运行并且ADC也使用GPTCLK运行，则将AD转换启动请求A传递给ELC毫不拖延。

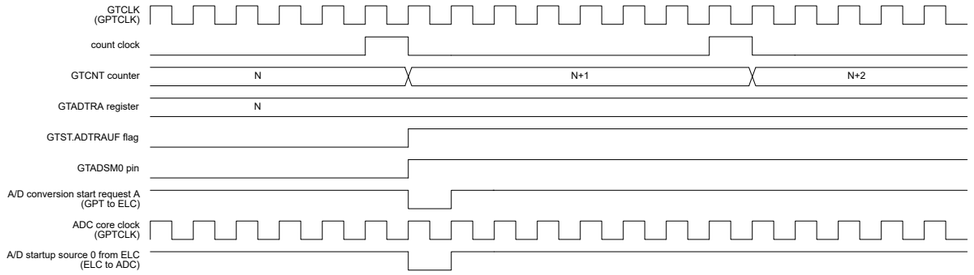
对于所有其他时钟组合，AD转换启动请求A被同步并传递给ELC。

- When GPT core clock is PCLKD and ADC core clock is PCLKA (GPT core clock and ADC core clock are synchronous),



Note: This is an example when the clock ratio is PCLKD:PCLKA= 2:1.

- When GPT core clock is GPTCLK and ADC core clock is GPTCLK (GPT core clock and ADC core clock are the same clock),



- When GPT core clock is PCLKD and ADC core clock is PCLKC (GPT core clock and ADC core clock are asynchronous),

Note: This is an example when the clock ratio is PCLKD:PCLKC= 2:1.

Figure 21.161 Example of A/D Conversion Start Request Timing Operation

For the restriction of A/D Conversion Start Request, see section 17, Event Link Controller (ELC), and section 21.10.6. Interval of interrupt request.

21.6 Operations Linked by ELC

21.6.1 Event Signal Output to ELC

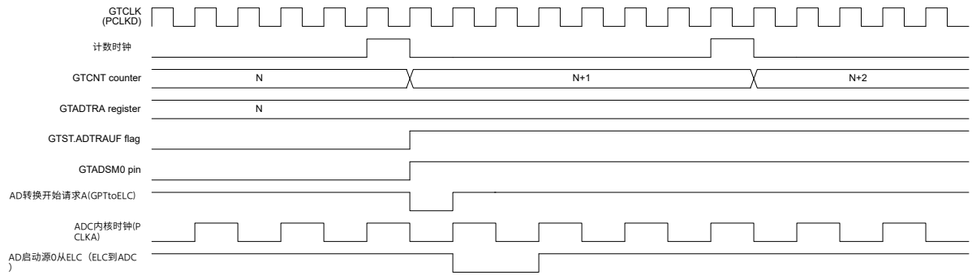
The GPT can perform operation linked with another module set in advance when its interrupt request signal is used as an event signal by the Event Link Controller (ELC).

The A/D conversion start request during up-counting/down-counting can be enabled/disabled individually with the A/D conversion start request enable bit to output events output to ELC.

The GPT has the following ELC event signals:

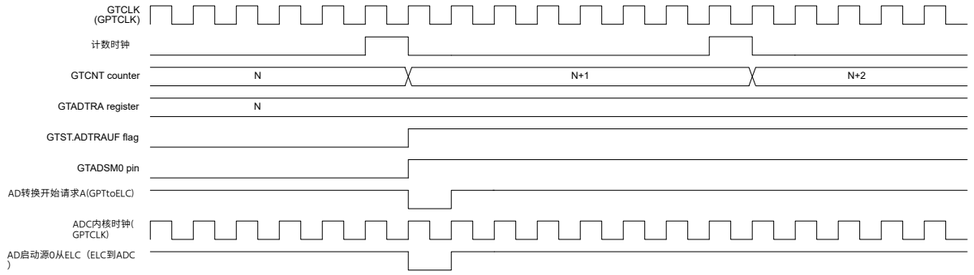
- Generation of compare match and input capture A interrupt (GPTn_CCMPA)
- Generation of compare match and input capture B interrupt (GPTn_CCMPB)

当GPT内核时钟为PCLKD且ADC内核时钟为PCLKA时（GPT内核时钟和ADC内核时钟同步），



注意：这是时钟比率为PCLKD:PCLKA=2:1时的示例。

当GPT内核时钟为GPTCLK且ADC内核时钟为GPTCLK时（GPT内核时钟和ADC内核时钟为同一时钟），



当GPT内核时钟为PCLKD且ADC内核时钟为PCLKC时（GPT内核时钟和ADC内核时钟异步），

注意：这是时钟比率为PCLKD:PCLKC=2:1时的示例。

图21.161AD转换开始请求时序操作示例

关于AD转换开始请求的限制，请参阅第17节，事件链接控制器(ELC)和第21.10.6节。
中断请求的间隔。

21.6 由ELC链接的操作

21.6.1 事件信号输出到ELC

当GPT的中断请求信号被事件链接控制器(ELC)用作事件信号时，GPT可以执行与预先设置的另一个模块链接的操作。

向上计数期间的AD转换开始请求可以通过AD转换开始请求使能位单独禁用，以将事件输出到ELC。

GPT具有以下ELC事件信号：

- ●产生比较匹配和输入捕捉A中断(GPTn_CCMPA)
- ●产生比较匹配和输入捕捉B中断(GPTn_CCMPB)

- Generation of compare match C interrupt (GPTn_CMPC)
- Generation of compare match D interrupt (GPTn_CMPD)
- Generation of compare match E interrupt (GPTn_CMPE)
- Generation of compare match F interrupt (GPTn_CMPF)
- Generation of overflow interrupt (GPTn_OVF)
- Generation of underflow interrupt (GPTn_UDF)
- Generation of A/D conversion start request A (GPTn_ADTRGA)
- Generation of A/D conversion start request B (GPTn_ADTRGB)
- Finish of period count function (GPTm_PC)

Note: n = 0 to 9
m = 0 to 3

21.6.2 Event Signal Inputs from ELC

The GPT can perform the following operations in response to a maximum of 8 events from the ELC:

- Start counting, stop counting, clear counting
- Up-counting, down-counting
- Input capture.

See section 17, Event Link Controller (ELC) for the connection between the ELC and the event signal input.

21.7 Noise Filter Function

Each pin for use in input capture and Hall sensor input to the GPT is equipped with a noise filter. The noise filter samples input signals at the sampling clock and removes the pulses whose length is less than 3 sampling cycles.

The noise filter functionality includes enabling and disabling the noise filter for each pin and setting of the sampling clock for each channel.

Figure 21.162 shows the timing of noise filtering.

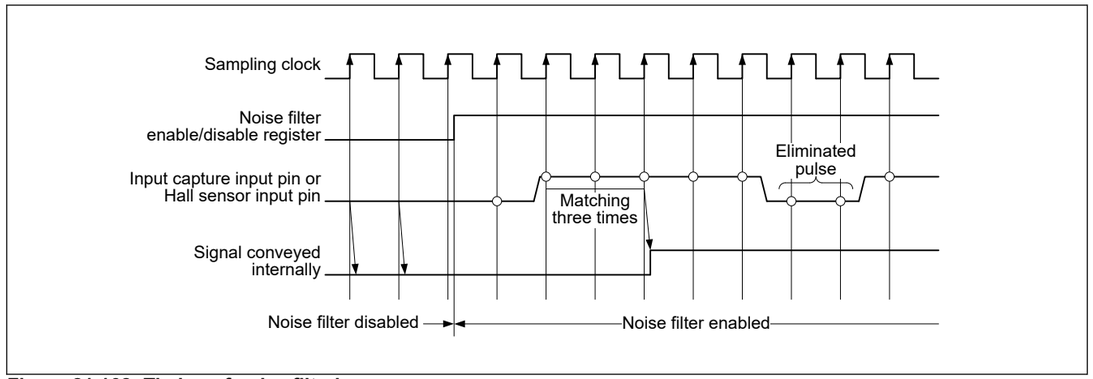


Figure 21.162 Timing of noise filtering

If noise filtering is enabled, the input capture operation or output phase switching operation is performed on the edges of the noise filtered signal after a delay of (sampling interval × 2 + GTCLK) at the shortest. This is due to the noise filtering for the input capture input or hall sensor input.

●产生比较匹配C中断(GPTn_CMPC)
●产生比较匹配D中断(GPTn_CMPD)
●产生比较匹配E中断(GPTn_CMPE)
●产生比较匹配F中断(GPTn_CMPF)
●产生溢出中断（GPTn_OVF）
●产生下溢中断（GPTn_UDF）
●生成AD转换开始请求A(GPTn_ADTRGA)
●生成AD转换开始请求B(GPTn_ADTRGB)
●周期计数功能完成（GPTm_PC）

Note: n = 0 to 9
m = 0 to 3

21.6.2 来自ELC的事件信号输入

GPT可以执行以下操作以响应来自ELC的最多8个事件：

●开始计数、停止计数、清计数
- Up-counting, down-counting
●输入捕捉。

有关ELC和事件信号输入之间的连接，请参见第17节，事件链接控制器(ELC)。

21.7 噪音过滤功能

用于GPT的输入捕捉和霍尔传感器输入的每个引脚都配备了噪声滤波器。噪声滤波器以采样时钟对输入信号进行采样，并去除长度小于3个采样周期的脉冲。

噪声过滤器功能包括为每个引脚启用和禁用噪声过滤器以及为每个通道设置采样时钟。

图21.162显示了噪声过滤的时序。

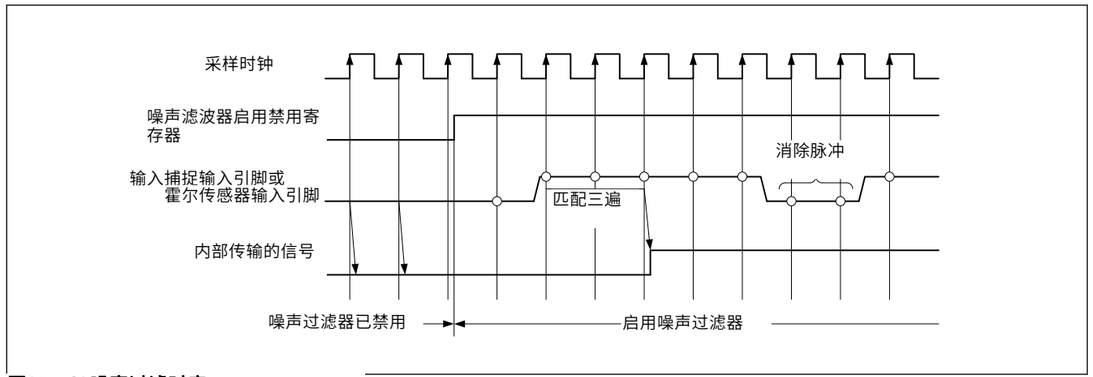


图21.162噪声过滤时序

如果噪声过滤使能，输入捕捉操作或输出相位切换操作在最短延迟（采样间隔×2+GTCLK）后在噪声过滤信号的边缘执行。这是由于输入捕捉输入或霍尔传感器输入的噪声过滤。

21.8 Protection Function

21.8.1 Write-Protection for Registers

To prevent registers from being accidentally modified, registers can be write-protected in channel units by setting GTWP.WP. Write-protection can be set for the following registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU, GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR, GTADSMR, GTEITC, GTEITLI1, GTEITLI2, GTEITLB, GTICLF, GTPC, GTADCMSC, GTADCMSS, GTBER2, GTOLBR, GTICCR.

Every bit in registers GTSTR, GTSTP and GTCLR which can update the corresponding registers in other channels and can be updated by any of the corresponding registers in other channels conversely, can be protected by setting the GTWP.STRWP, STPWP, and CLRWP bits, respectively, per channel.

Likewise, writing to the GTSECSR and GTSECR registers, which can control all channels by writing to the GTSECSR and GTSECR registers of a given channel, can by enabled or disabled by the setting of the GTWP.CMNWP bit.

Protection using the GTWP register is only for write operations by the CPU. This protection does not cover updates to registers that occur in association with CPU writes.

21.8.2 Disabling of Buffer Operation

If the timing of the buffer register write is delayed relative to the timing for the buffer transfer, buffer operation can be suspended with the GTBER.BD[3], BD[2], BD[1] and BD[0] bits settings. Specifically, buffer transfer can be temporarily disabled even though a buffer transfer condition is generated during buffer register write, by setting the BD[3], BD[2], BD[1] and BD[0] bits to 1 (buffer operation disabled) before buffer register write, and setting the bits to 0 (buffer operation enabled) after completion of writing to all the buffer registers.

The BD[3], BD[2], BD[1] and BD[0] bits can be set on channel basis by writing directly to the GTBER register or it can be set to 0 simultaneously by setting the GTSECR register for multiple channels which were set by the GTSECSR register.

Figure 21.163 shows an example of operation for disabling buffer operation by writing to the GTBER register.

21.8 保护功能

21.8.1 寄存器的写保护

为了防止寄存器被意外修改，可以通过设置以通道为单位对寄存器进行写保护
GTWP.WP。可以为以下寄存器设置写保护：

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU, GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR, GTADSMR, GTEITC, GTEITLI1, GTEITLI2, GTEITLB, GTICLF, GTPC, GTADCMSC, GTADCMSS, GTBER2, GTOLBR, GTICCR.

寄存器GTSTR、GTSTP和GTCLR中的每个位可以更新其他通道中的相应寄存器，反之也可以由其他通道中的任何相应寄存器更新，可以分别通过设置GTWP.STRWP、STPWP和CLRWP位来保护 每个频道。

同样，写入GTSECSR和GTSECR寄存器，它们可以通过写入GTSECSR和
给定通道的GTSECR寄存器可以通过设置GTWP.CMNWP位来启用或禁用。

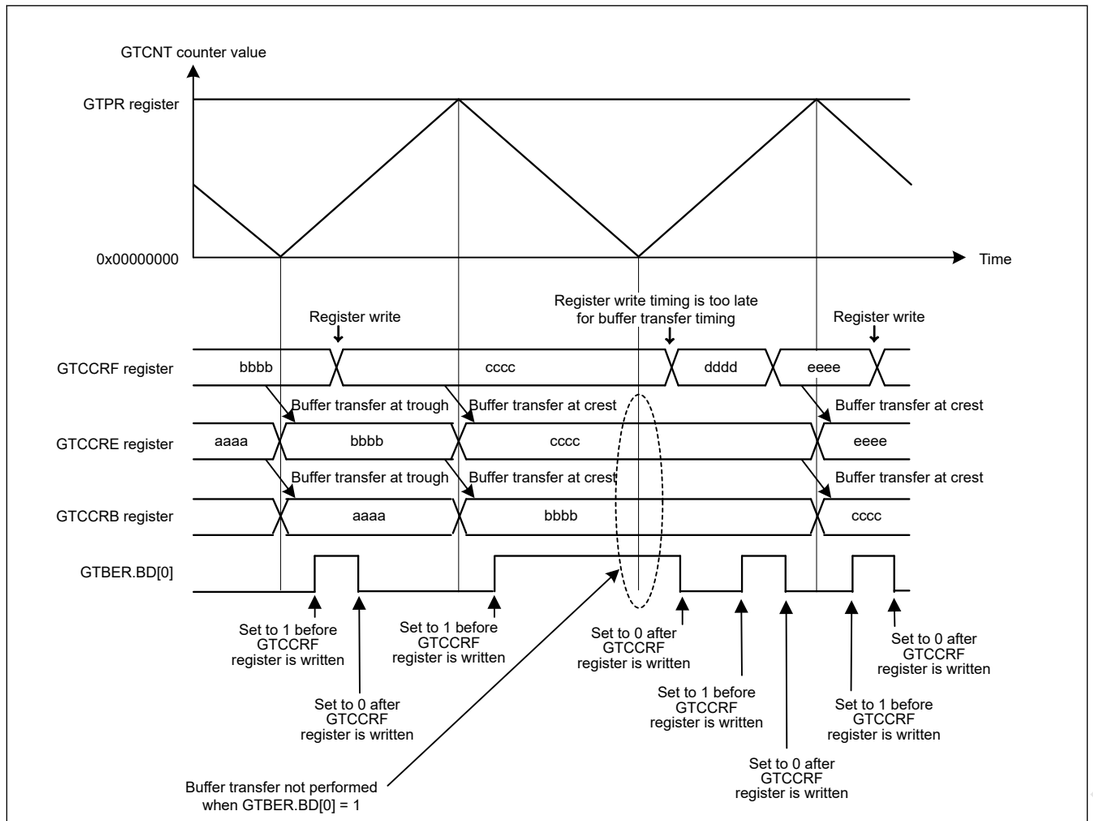
使用GTWP寄存器的保护仅适用于CPU的写操作。此保护不涵盖与CPU写入相关的寄存器更新。

21.8.2 禁用缓冲区操作

如果缓冲寄存器写入的时序相对于缓冲传输的时序延迟，则可以通过GTBER.BD[3]、BD[2]、BD[1]和BD[0]位设置暂停缓冲操作。具体而言，通过将BD[3]、BD[2]、BD[1]和BD[0]位设置为1（禁用缓冲操作)在写入缓冲寄存器之前，并在完成对所有缓冲寄存器的写入后将这些位设置为0（启用缓冲操作）。

BD[3]、BD[2]、BD[1]和BD[0]位可以通过直接写入GTBER寄存器以通道为单位设置，也可以通过为多个通道设置GTSECR寄存器同时设置为0由GTSECSR寄存器设置。

图21.163显示了通过写入GTBER寄存器来禁用缓冲区操作的操作示例。



Note: The base address of registers are the same.

Figure 21.163 Example of operation for disabling buffer operation with triangle waves, double buffer operation, and buffer transfer at both troughs and crests

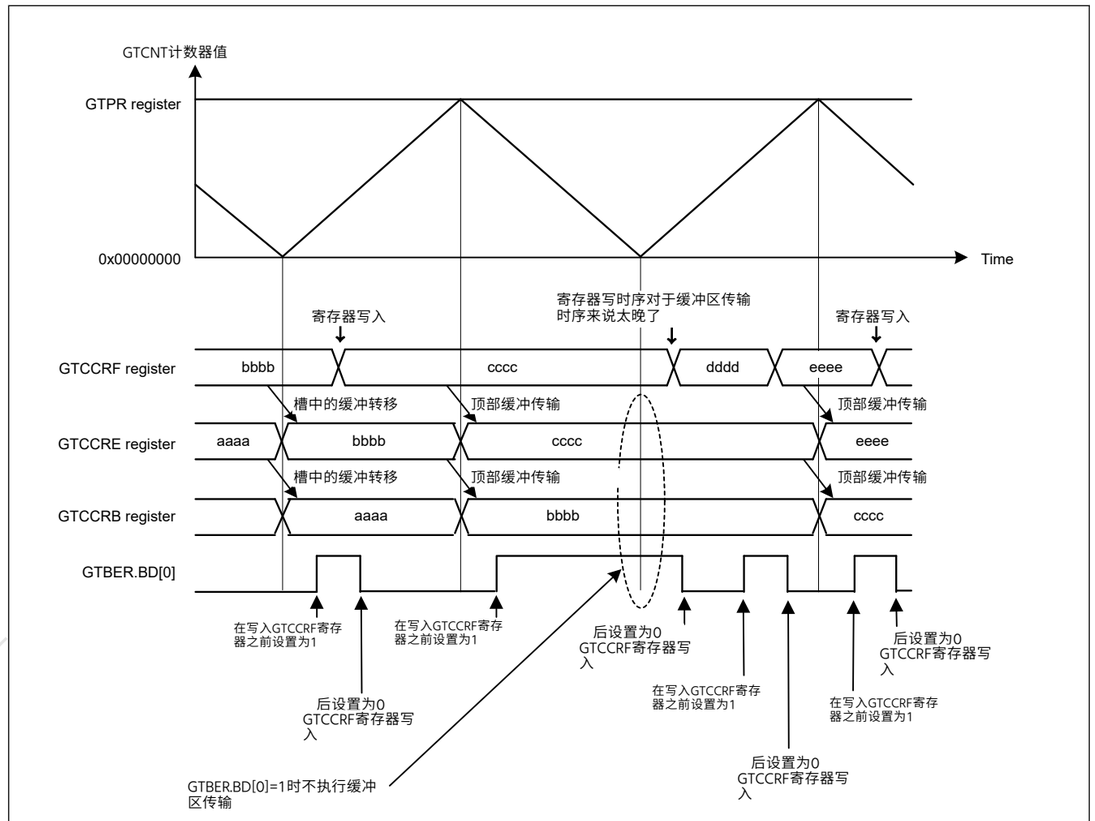
21.8.2.1 Simultaneous Control of Buffer Operations of Multiple Channels

The GTBER.BD bit can be set by writing directly to the GTBER register per channel or by making settings in the GTSECR register for multiple channels that have already set in the GTSECSR register.

Follow the procedure below to simultaneously set the GTBER.BD bits of multiple channels.

1. Select the channels for simultaneously setting by the GTSECSR register
   Set the GTSECSR register so that the values at the bit positions for the corresponding channels for simultaneously setting of the GTBER.BD bits become 1. All GTSECSR registers can be updated by writing to the GTSECSR register of any channel.
2. Simultaneously set the GTBER.BD bits by updating the GTSECR register
   In the GTSECR register, set the operation of the GTBER.BD bits (enabling or disabling of buffer operation) which are to be simultaneously set. Writing to a GTSECR register from any channel updates the GTBER.BD bits in all channels corresponding to the bits set as 1 in the GTSECSR register, in accordance with the value of the GTSECR register.

Figure 21.164 and Figure 21.165 show examples of simultaneously controlling the enabling or disabling of buffer operation for multiple channels.



Note: 寄存器的基地址相同。

图21.163禁用三角波缓冲操作、双缓冲操作和波谷和波峰缓冲传输的操作示例

21.8.2.1 多通道缓冲操作的同时控制

GTBER.BD位可以通过直接写入每个通道的GTBER寄存器或通过在GTSECR寄存器中为已在GTSECSR寄存器中设置的多个通道进行设置来设置。

按照以下步骤同时设置多个通道的GTBER.BD位。

1.通过GTSECSR寄存器选择同时设置的通道
设置GTSECSR寄存器，使用于同时设置GTBER.BD位的相应通道的位位置的值变为1。通过写入任何通道的GTSECSR寄存器，可以更新所有GTSECSR寄存器。

2.通过更新GTSECR寄存器同时设置GTBER.BD位
在GTSECR寄存器中，设置要同时设置的GTBER.BD位的操作（启用或禁用缓冲区操作）。根据GTSECR寄存器的值，从任何通道写入GTSECR寄存器会更新与GTSECSR寄存器中设置为1的位相对应的所有通道中的GTBER.BD位。

图21.164和图21.165显示了同时控制多个通道的缓冲区操作的启用或禁用的示例。

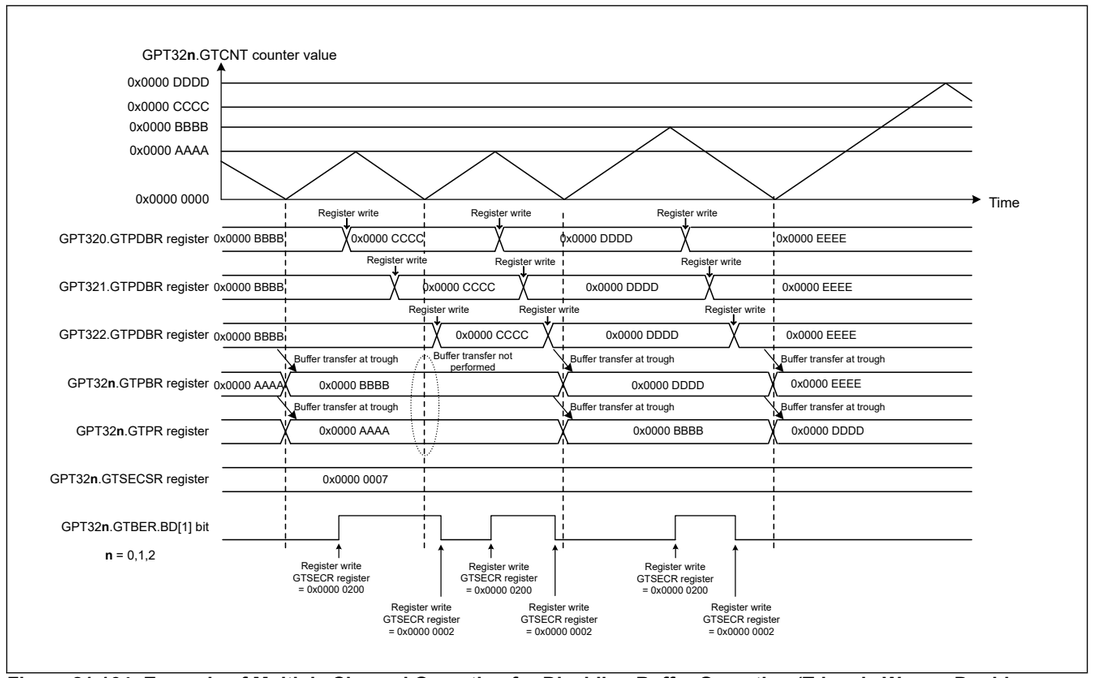


Figure 21.164 Example of Multiple Channel Operation for Disabling Buffer Operation (Triangle Waves, Double Buffer Operation)

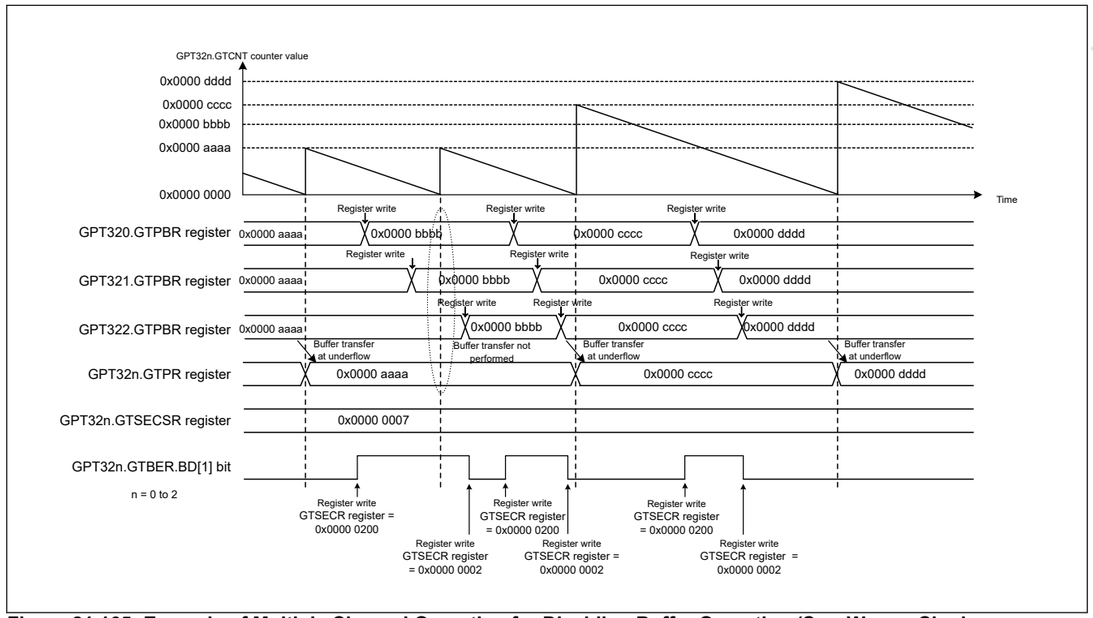


Figure 21.165 Example of Multiple Channel Operation for Disabling Buffer Operation (Saw Waves, Single Buffer Operation)

21.8.2.2 Repeated Double-Buffered Operation When Disabling GTCCR Buffer Transfer

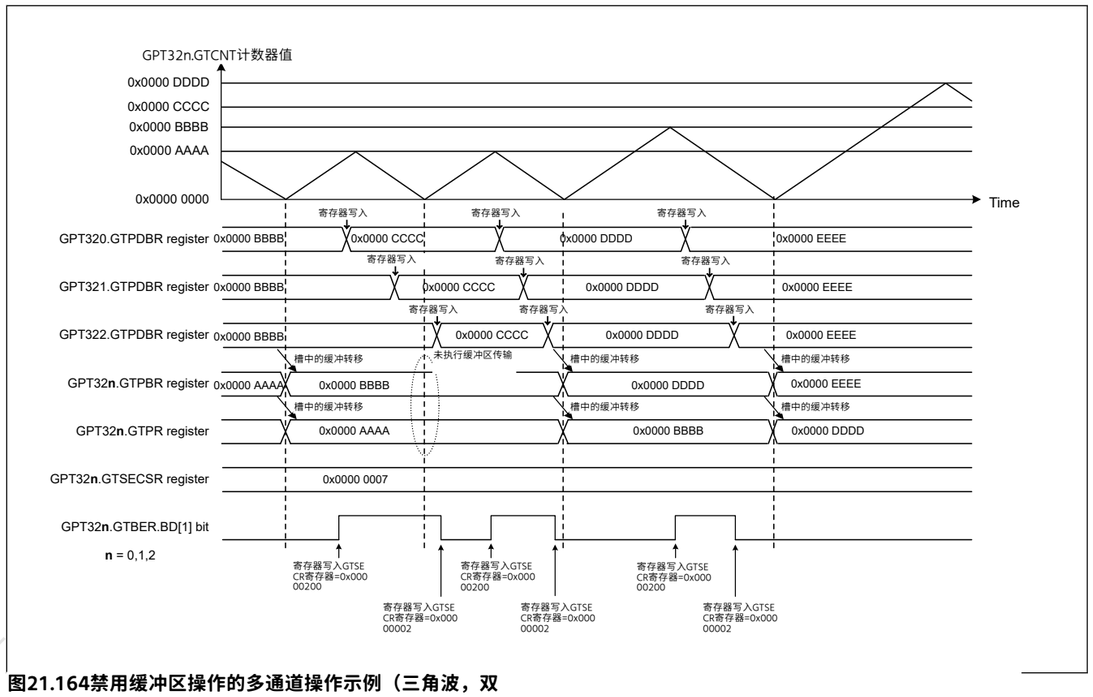


图21.164禁用缓冲区操作的多通道操作示例（三角波，双 Buffer Operation)

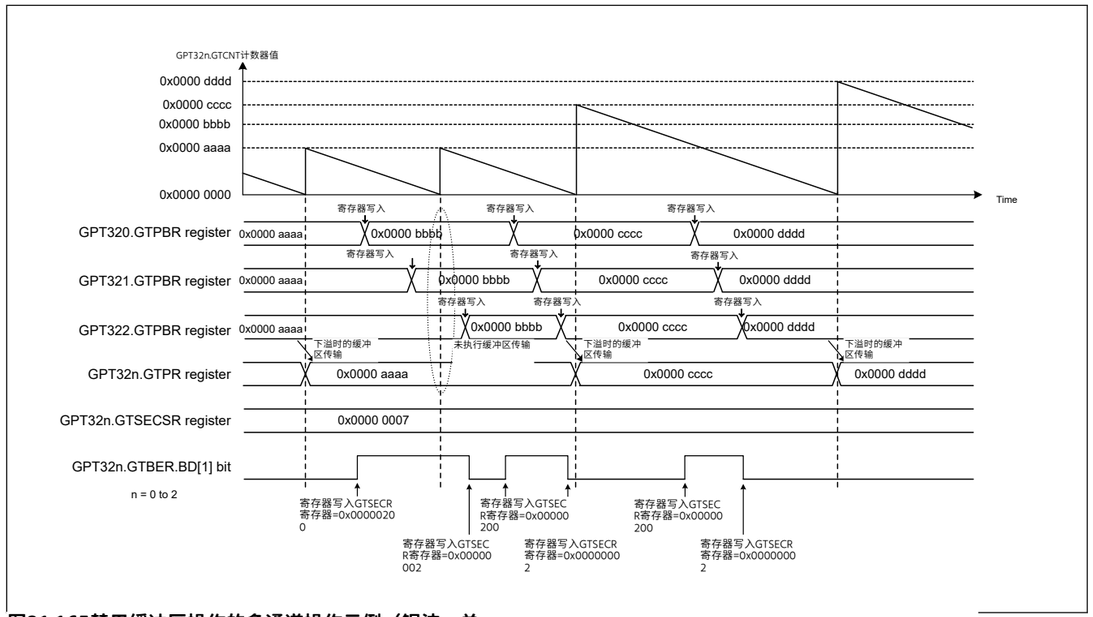


图21.165禁用缓冲区操作的多通道操作示例（锯波，单 Buffer Operation)

21.8.2.2 禁用GTCCR缓冲区传输时重复双缓冲操作

When a GTBER.DBRTECm (m = A, B) bit is set to 1 in saw-wave one-shot pulse mode or triangle-wave PWM mode 3, transfer from the intermediate buffer to the GTCCRm (m = A, B) register is repeated on a cyclic basis even while buffer transfer is disabled by the setting of the GTBER.BD[0] bit or by the buffer transfer extended skipping function.

(1) In saw-wave one-shot pulse mode

In saw-wave one-shot pulse mode, the compare match value for the first half of a waveform is stored in temporary register x (x = C, E) as the intermediate buffer for the GTCCRx (x = C, E) register and the compare match value for the second half of a waveform is stored in temporary register m (m = A, B) as the intermediate buffer for the GTCCRy (y = D, F) register, respectively, for compare match values during repeated buffer operation, and the given values are alternately transferred to the GTCCRm (m = A, B) registers.

Table 21.72 lists the types of buffer transfer of the GTCCR register during counting in saw-wave one-shot pulse mode.

While counting is stopped, the setting of the value in the temporary register is transferred through forcible buffer transfer. In forcible buffer transfer, the values of the GTCCRy (y = D, F) registers are transferred to temporary registers m (m = A, B), and the values of the GTCCRx (x = C, E) are transferred to temporary registers x (x = C, E) when the setting of the corresponding GTBER.DBRTECm (m = A, B) bit is 1, respectively.

When the setting of the GTBER.DBRTECm (m = A, B) bit is 1, values written by the CPU to the GTCCRm (m = A, B) registers are reflected as the values of temporary registers x (x = C, E).

Table 21.72 GTCCR Buffer Transfer Operation in Saw-Wave One Shot Pulse Mode during GTCNT Counting

GTBER.DBRTECm	Buffer Transfer	Timing of transfer				
		GTCCRx ↓ GTCCRm	GTCCRx ↓ Temporary register x	Temporary register x ↓ GTCCRm	GTCCRy ↓ Temporary register m	Temporary register m ↓ GTCCRm
0	Transfer enabled period	Overflow or Underflow	No transfer	No transfer	Overflow or Underflow	GTCCRm compare match
	Transfer disabled period	No transfer	No transfer	No transfer	No transfer	No transfer
1	Transfer enabled period	Overflow or Underflow	Overflow or Underflow	No transfer	Overflow or Underflow	GTCCRm compare match
	Transfer disabled period	No transfer	No transfer	Overflow or Underflow	No transfer	GTCCRm compare match

Note: m = A, B
x = C, E
y = D, F

Figure 21.166 shows the operation of generating transfer-disabled period by extended buffer transfer skipping as an example of repeated double buffer operations when the GTCCR buffer transfer disabled in saw-wave one-shot pulse mode.

Figure 21.167 shows the operation of generating transfer-disabled period by updating the GTBER.BD[0] bit as an example of repeated double-buffer operations when the GTCCR buffer transfer is disabled in saw-wave one-shot pulse mode.

当GTBER.DBRTECm(m=A B)位在锯齿波单次脉冲模式或三角波PWM模式3中设置为1时，从中间缓冲区传输到GTCCRm(m=A B)寄存器即使通过设置GTBER.BD[0]位或通过缓冲区传输扩展跳过功能禁用缓冲区传输，也会循环重复。

(1) 在锯齿波单发脉冲模式下

在锯齿波单次脉冲模式下，波形前半部分的比较匹配值存储在临时寄存器x(x=C E)中，作为GTCCRx(x=C E)寄存器的中间缓冲区和波形后半部分的比较匹配值存储在临时寄存器m(m=A B)中，分别作为GTCCRy(y=D F)寄存器的中间缓冲区，用于在重复缓冲区操作期间比较匹配值 给定值交替传送到GTCCRm(m=A B)寄存器。

表21.72列出了在锯齿波单发脉冲模式下计数期间GTCCR寄存器的缓冲传输类型。

计数停止时，临时寄存器中的值的设置通过强制缓冲传输进行传输。在强制缓冲区传输中，GTCCRy(y=D F)寄存器的值被传输到临时寄存器m(m=A B)，GTCCRx(x=C E)的值被传输到临时寄存器x(x=C E)当相应的GTBER.DBRTECm(m=A B)位的设置分别为1时。

当GTBER.DBRTECm(m=A B)位设置为1时，CPU写入GTCCRm(m=A B)寄存器的值反映为临时寄存器x(x=C E)的值）。

Table 21.72 GTCNT计数期间Saw−WaveOneShotPulse模式下的GTCCR缓冲区传输操作

GTBER.DBRTECm	缓冲传输	转移时间				
		GTCCRx ↓ GTCCRm	GTCCRx ↓临时寄存器x	临时登记册x ↓ GTCCRm	GTCCRy ↓临时寄存器m	临时登记册 ↓ GTCCRm
0	转移启用期	上溢或下溢	无转让	无转让	上溢或下溢	GTCCRm比较匹配
	转让禁用期	无转让	无转让	无转让	无转让	无转让
1	转移启用期	上溢或下溢	上溢或下溢	无转让	上溢或下溢	GTCCRm比较匹配
	转让禁用期	无转让	无转让	上溢或下溢	无转让	GTCCRm比较匹配

Note: m = A, B
x = C, E
y = D, F

图21.166显示了通过扩展缓冲区传输跳过生成传输禁用周期的操作，作为在锯波单次脉冲模式下禁用GTCCR缓冲区传输时重复双缓冲区操作的示例。

图21.167显示了通过更新GTBER.BD[0]位生成传输禁用周期的操作，作为在锯波单次脉冲模式下禁用GTCCR缓冲区传输时重复双缓冲区操作的示例。

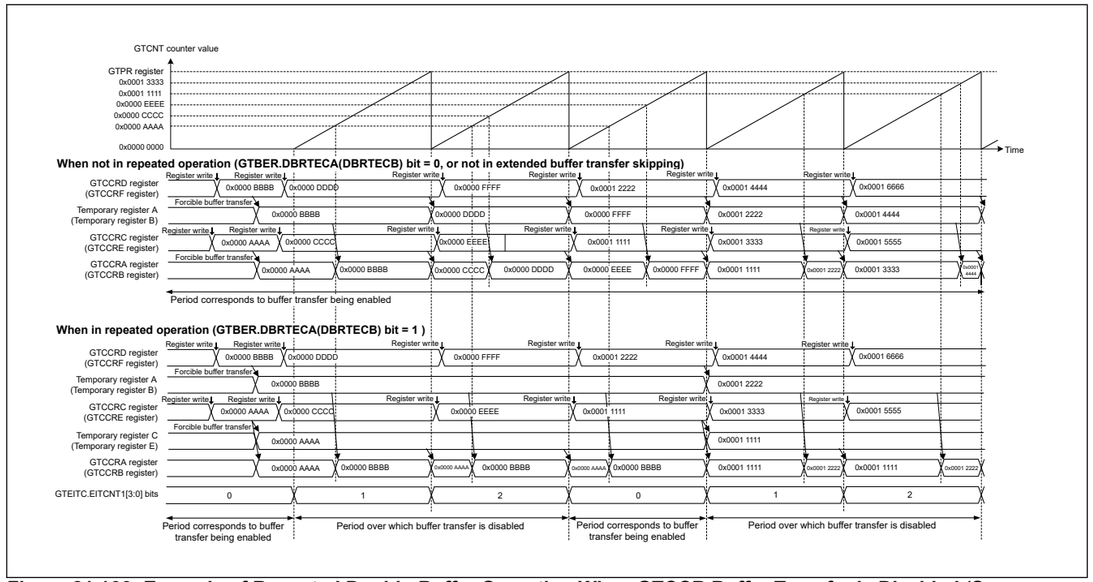


Figure 21.166 Example of Repeated Double-Buffer Operation When GTCCR Buffer Transfer is Disabled (Saw-Wave One-Shot Pulse Mode, Using Extended Buffer Transfer Skipping, GTBER.BD[0] is Constantly 0)

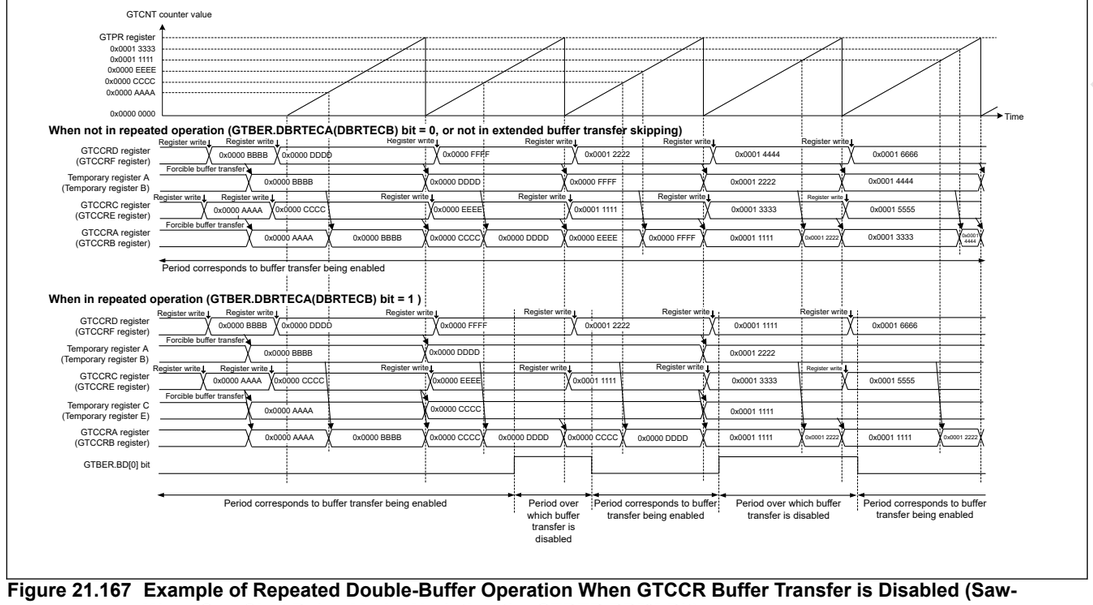


Figure 21.167 Example of Repeated Double-Buffer Operation When GTCCR Buffer Transfer is Disabled (Saw-Wave One-Shot Pulse Mode, Updating the GTBER.BD[0] Bit)

(2) In triangle-wave PWM mode 3

In triangle-wave PWM mode 3, the compare match value for the first half of a waveform is stored in the temporary register x (x = C, E) as the intermediate buffer for the GTCCRx (x = C, E) register and the compare match value for the second half of a waveform is stored in temporary register m (m = A, B) as the intermediate buffer for the GTCCRy (y = D, F) register,

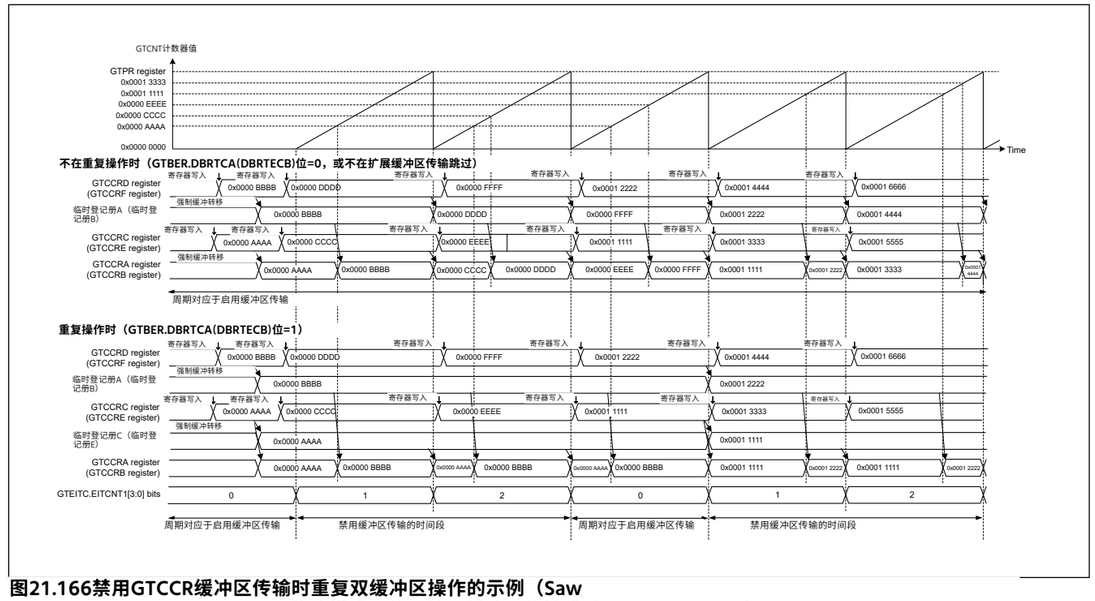


图21.166禁用GTCCR缓冲区传输时重复双缓冲区操作的示例（Saw WaveOne-Shot脉冲模式，使用扩展缓冲区传输跳过，GTBER.BD[0]为Constantly 0)

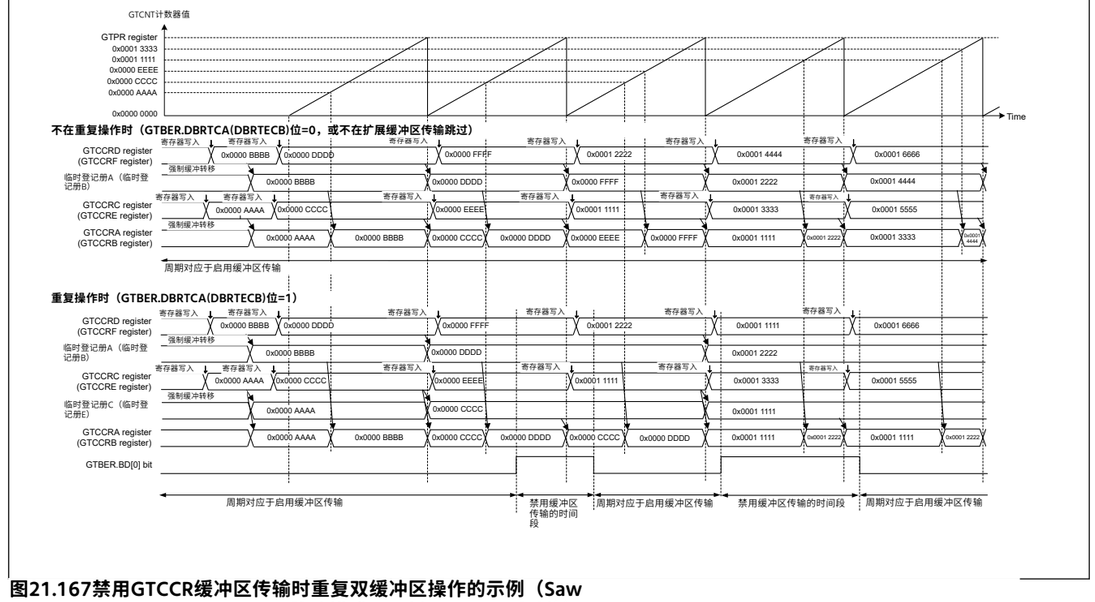


图21.167禁用GTCCR缓冲区传输时重复双缓冲区操作的示例（Saw WaveOne-Shot脉冲模式，更新GTBER.BD[0]位）

(2) 在三角波PWM模式3

在三角波PWM模式3中，波形前半部分的比较匹配值存储在临时寄存器x(x=C E)中，作为GTCCRx(x=C E)寄存器和波形后半部分的比较匹配值存储在临时寄存器m(m=A B)中，作为GTCCRy(y=D F)寄存器的中间缓冲区，

respectively, for compare match values during repeated buffer operation, and the given values are alternately transferred to the GTCCRm (m = A, B) register.

Table 21.73 lists the types of buffer transfer of the GTCCR register during counting operation in triangle-wave PWM mode 3.

While counting is stopped, the setting of the value in the temporary register is transferred through forcible buffer transfer. In forcible buffer transfer, the values of the GTCCRy (y = D, F) registers are transferred to temporary registers m (m = A, B), and the values of the GTCCRx (x = C, E) are transferred to temporary registers x (x = C, E), when the setting of the corresponding GTBER.DBRTECm (m = A, B) bit is 1, respectively.

When the setting of the GTBER.DBRTECm (m = A, B) bit is set to 1, values written by the CPU to the GTCCRm (m = A, B) registers are reflected as the values of temporary registers x (x = C, E).

Table 21.73 GTCCR Buffer Transfer Operation in Triangle-Wave PWM Mode 3 during GTCNT Counting

GTBER.DBRTECm	Buffer Transfer	Timing of transfer				
		GTCCRx ↓ GTCCRm	GTCCRx ↓ Temporary register x	Temporary register x ↓ GTCCRm	GTCCRy ↓ Temporary register m	Temporary register m ↓ GTCCRm
0	Transfer enabled period	Trough	No transfer	No transfer	Trough	Crest
	Transfer disabled period	No transfer	No transfer	No transfer	No transfer	No transfer
1	Transfer enabled period	Trough	Trough	No transfer	Trough	Crest
	Transfer disabled period	No transfer	No transfer	Trough	No transfer	Crest

Note: m = A, B
x = C, E
y = D, F

Figure 21.168 shows the operation of generating transfer-disabled period by extended buffer transfer skipping as an example of repeated double buffer operations when the GTCCR buffer transfer disabled in triangle-wave PWM mode 3.

Figure 21.169 shows the operation of generating transfer-disabled period by updating the GTBER.BD[0] bit as an example of repeated double-buffer operations when the GTCCR buffer transfer is disabled in triangle-wave PWM mode 3.

分别用于在重复缓冲区操作期间比较匹配值，并将给定值交替传送到GTCCRm(m=A B)寄存器。

表21.73列出了三角波PWM模式3计数操作期间GTCCR寄存器的缓冲传输类型。

计数停止时，临时寄存器中的值的设置通过强制缓冲传输进行传输。在强制缓冲区传输中，GTCCRy(y=D F)寄存器的值被传输到临时寄存器m(m=A B)，GTCCRx(x=C E)的值被传输到临时寄存器x(x=C E)，当相应的GTBER.DBRTECm(m=A B)位的设置分别为1时。

当GTBER.DBRTECm(m=A B)位设置为1时，CPU写入GTCCRm(m=A B)寄存器反映为临时寄存器x(x=C E)的值。

Table 21.73 GTCNT计数期间三角波PWM模式3中的GTCCR缓冲区传输操作

GTBER.DBRTECm	缓冲传输	转移时间				
		GTCCRx ↓ GTCCRm	GTCCRx ↓临时寄存器x	临时登记册x ↓ GTCCRm	GTCCRy ↓临时寄存器m	临时登记册 ↓ GTCCRm
0	转移启用期	Trough	无转让	无转让	Trough	Crest
	转让禁用期	无转让	无转让	无转让	无转让	无转让
1	转移启用期	Trough	Trough	无转让	Trough	Crest
	转让禁用期	无转让	无转让	Trough	无转让	Crest

Note: m = A, B
x = C, E
y = D, F

图21.168显示了在三角波PWM模式3中禁用GTCCR缓冲区传输时，通过扩展缓冲区传输跳过生成传输禁用周期的操作作为重复双缓冲区操作的示例。

图21.169显示了通过更新GTBER.BD[0]位生成传输禁用周期的操作，作为在三角波PWM模式3中禁用GTCCR缓冲区传输时重复双缓冲区操作的示例。

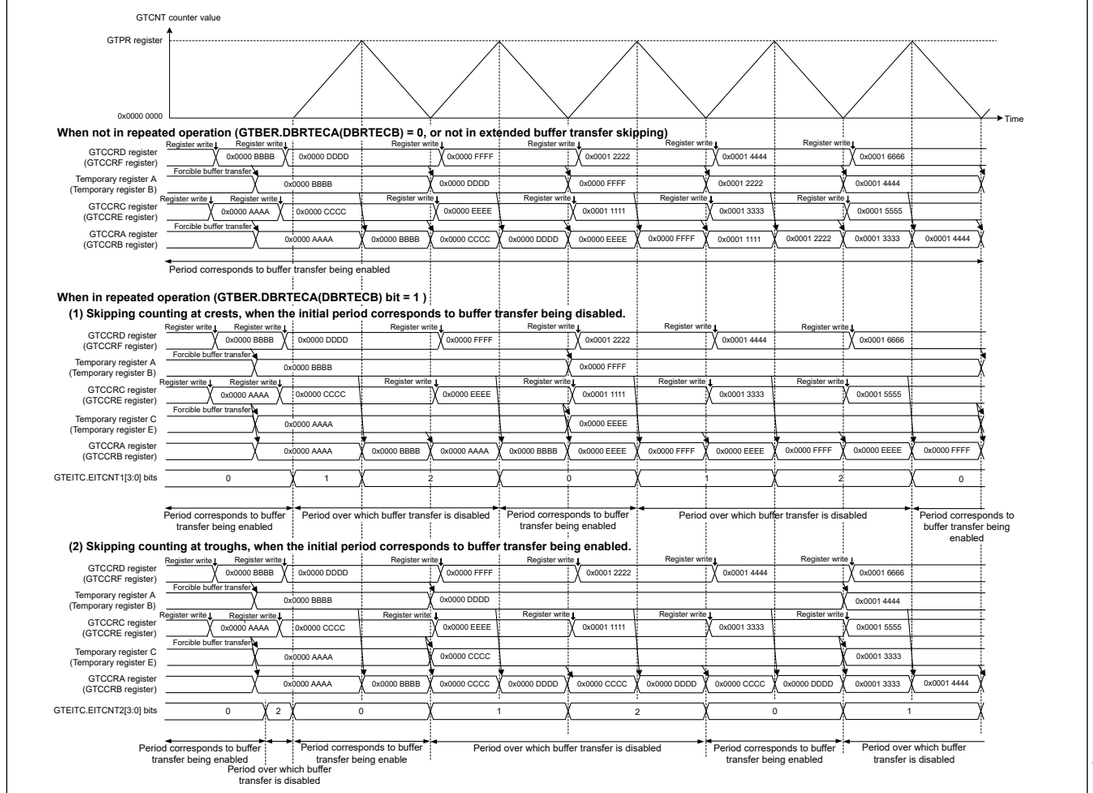


Figure 21.168 Example of Repeated Double-Buffer Operation When GTCCR Buffer Transfer is Disabled (Triangle-Wave PWM Mode 3, Using Extended Buffer Transfer Skipping, GTBER.BD[0] is Constantly 0)

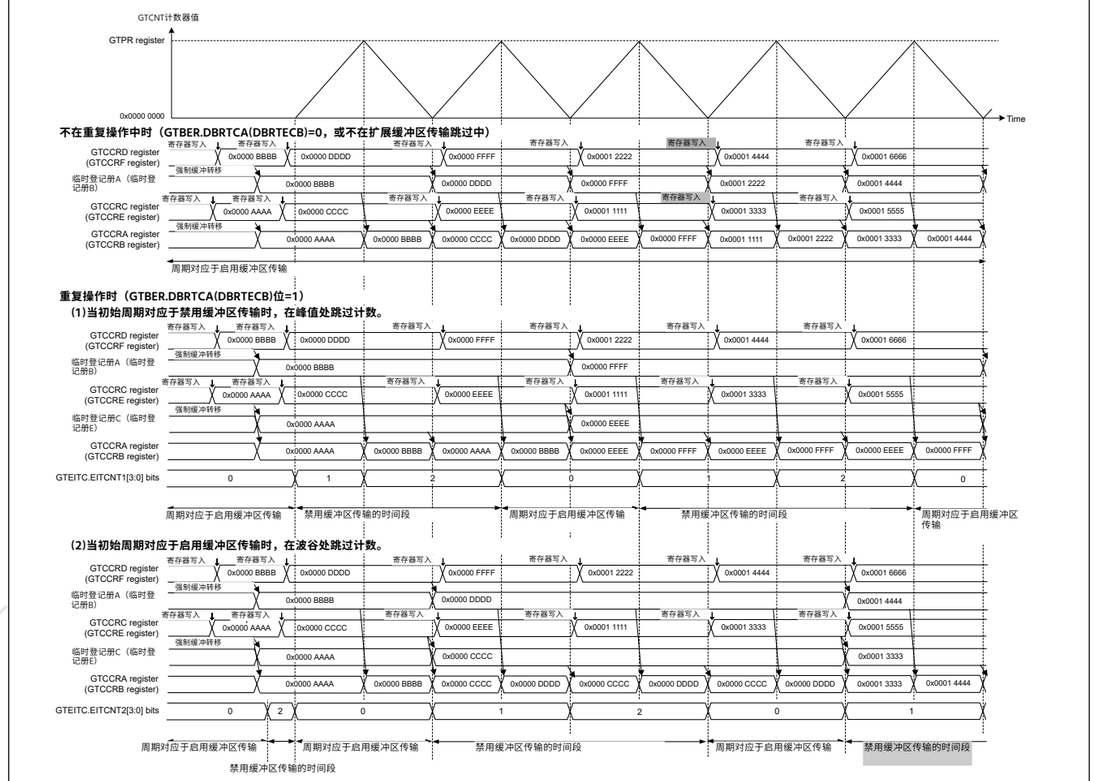


图21.168禁用GTCCR缓冲区传输时重复双缓冲区操作的示例（三角波PWM模式3，使用扩展缓冲区传输跳过，GTBER.BD[0]始终为0）

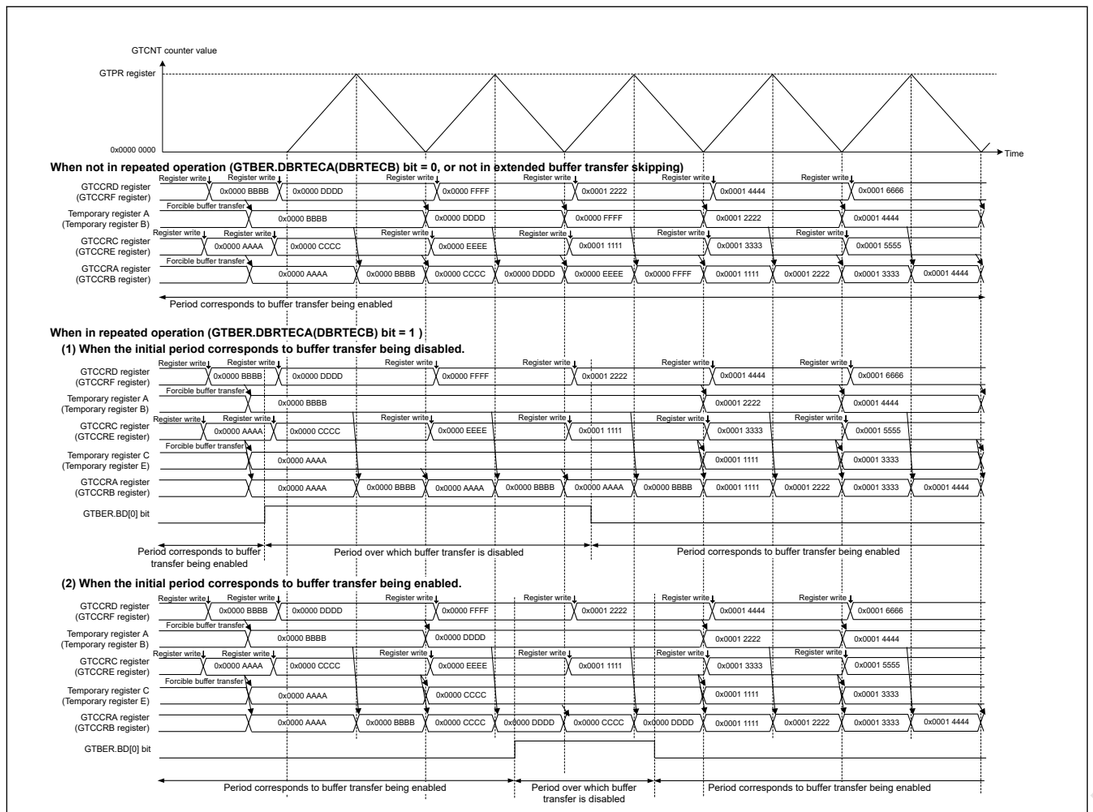


Figure 21.169 Example of Repeated Double-Buffer Operation When GTCCR Buffer Transfer is Disabled (Triangle-Wave PWM Mode 3, Updating the GTBER.BD[0] Bit)

21.8.3 GTIOCnm Pin Output Negate Control (n = 0 to 9, m = A, B)

For protection from system failure, the output disable control that changes the GTIOCnm pin output value forcibly is provided for GTIOCnm pin output by the request of output disable from POEG. Output protection is required when a dead time error or the same output level being on the GTIOCnA and GTIOCnB pins is detected. GPT detects this condition and generates output disable requests to POEG according to the setting of the output disable request permission bits, such as GTINTAD.GRPDTE, GTINTAD.GRPABH, GTINTAD.GRPABL. After the POEG performs the logical OR of the output disable request from each channel and the output disable request from the external input, the POEG generates output disable requests to GPT.

One output disable signal (representing the shared output disable request signal of the GTIOCnA pin and the GTIOCnB pin) out of 4 output disable requests generated by the POEG is selected by setting GTINTAD.GRP[1:0]. The status of the selected disable output request is monitored by reading the GTST.ODF bit. The output level during output disable is set based on the GTIOR.OADF[1:0] bits for the GTIOCnA pin and the GTIOR.OBDF[1:0] setting for the GTIOCnB pin.

The change to the output disable state is performed asynchronously by generating the output disable request from the POEG. The release of the output disable state is performed at end of cycle by terminating the output disable request. It is after 3 GTCLK at shortest when the output disable condition is released after the output disable request becomes no longer satisfied. To reliably control output disabling, clear the flag of POEG for which the condition for the request to disable the output is no longer satisfied after 4 cycles of GTCLK.

When event count is performed or when the operating mode is saw-wave PWM mode 2 or when the output disable state should be released immediately without waiting for end of cycle, GTIOR.OADF[1:0] should be set to 00b (for GTIOCnA pin) or GTIOR.OBDF[1:0] should be set to 00b (for the GTIOCnB pin).

Figure 21.170 shows an example of the GTIOCnm pin output disable control operation. (n = 0 to 9, m = A, B)

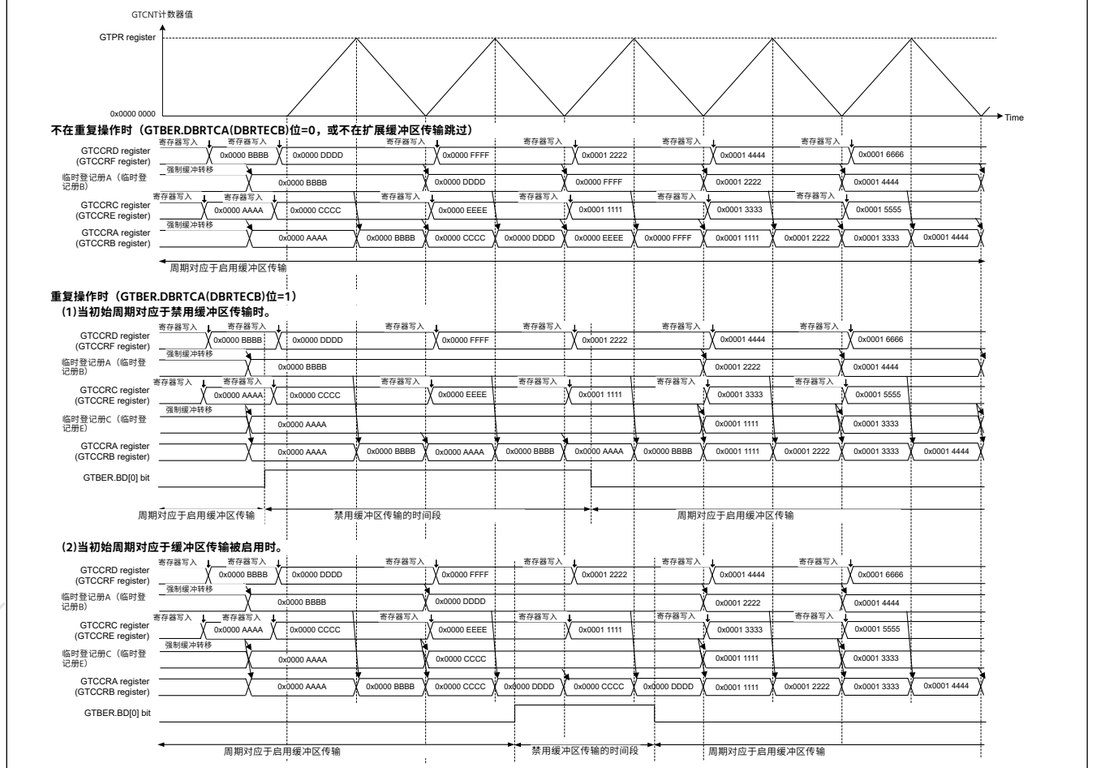


图21.169禁用GTCCR缓冲区传输时重复双缓冲区操作的示例（三角波PWM模式3，更新GTBER.BD[0]位）

21.8.3 GTIOCnm引脚输出负控制（n=0到9，m=A，B）

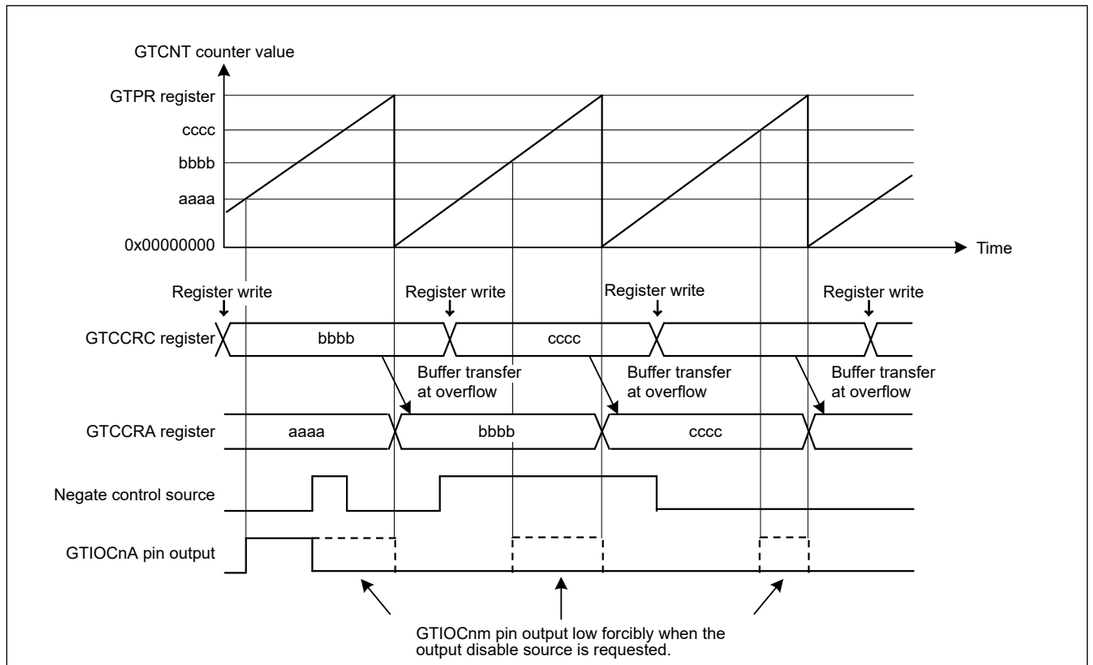
为防止系统故障，根据POEG的输出禁用请求，为GTIOCnm引脚输出提供强制改变GTIOCnm引脚输出值的输出禁用控制。当检测到死区错误或GTIOCnA和GTIOCnB引脚上的输出电平相同时，需要输出保护。GPT检测到这种情况并根据输出禁用请求许可位的设置，如GTINTAD.GRPDTE、GTINTAD.GRPABH、GTINTAD.GRPABL向POEG生成输出禁用请求。在POEG对来自每个通道的输出禁止请求和来自外部输入的输出禁止请求进行逻辑或运算后，POEG向GPT生成输出禁止请求。

通过设置GTINTAD.GRP[1:0]，在POEG产生的4个输出禁止请求中选择一个输出禁止信号（代表GTIOCnA引脚和GTIOCnB引脚的共享输出禁止请求信号）。通过读取GTST.ODF位来监控所选禁用输出请求的状态。输出禁用期间的输出电平根据GTIOCnA引脚的GTIOR.OADF[1:0]位和GTIOCnB引脚的GTIOR.OBDF[1:0]设置来设置。

对输出禁用状态的更改是通过从
POEG。通过终止输出禁用请求，在循环结束时执行输出禁用状态的释放。输出禁止请求不再满足后，输出禁止条件解除的时间最短为3GTCLK之后。为了可靠地控制输出禁用，在4个GTCLK周期后，清除不再满足禁用输出请求的条件的POEG标志。

当执行事件计数或工作模式为锯齿波PWM模式2或输出禁用状态应立即释放而无需等待周期结束时，GTIOR.OADF[1:0]应设置为00b（对于GTIOCnA引脚）或GTIOR.OBDF[1:0]应设置为00b（对于GTIOCnB引脚）。

图21.170显示了GTIOCnm引脚输出禁用控制操作的示例。(n=0到9 m=A B)



Note: The base address of registers are the same.

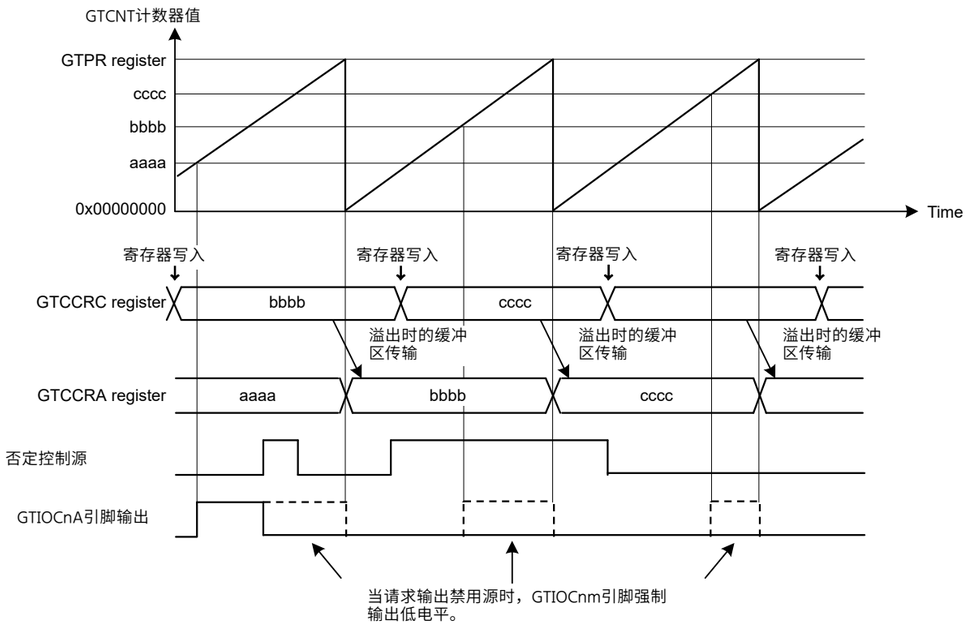
Figure 21.170 Example of GTIOCnm pin output disable control operation in saw-wave up-counting, buffer operation, active level 1, high output at GTCCRA compare match, low output at cycle end, and low output at output disable (n = 0 to 9, m = A, B)

21.8.4 Output Protection Function for GTIOCnm Pin Output (n = 0 to 9; m = A, B)

To prepare for a case when an incorrect value (0x0000 0000 or a value greater than or equal to the GTPR register value) is set in the GTCCRA register, the output protection function for the GTIOCnm pin output (disabling function) is activated when the automatic dead time is set (GTDTCR.TDE bit = 1) in triangle-wave PWM mode.

The status of the output protection function can be read from the GTSOS.SOS[1:0] bits.

Figure 21.171 shows the output protection function state transition.



Note: 寄存器的基地址相同。

图21.170GTIOCnm引脚输出禁用控制操作示例在锯齿波递增计数，缓冲器操作，有效电平1，GTCCRA比较匹配时输出高，周期结束时输出低，输出禁用时输出低（n=0到9，m=A，B）

21.8.4 GTIOCnm引脚输出的输出保护功能（n=0至9；m=A、B）

为防止在GTCCRA寄存器中设置了不正确的值（0x00000000或大于或等于GTPR寄存器值）的情况，当自动在三角波PWM模式下设置死区时间（GTDTCR.TDE位=1）。

可以从GTSOS.SOS[1:0]位读取输出保护功能的状态。

图21.171显示了输出保护功能状态转换。

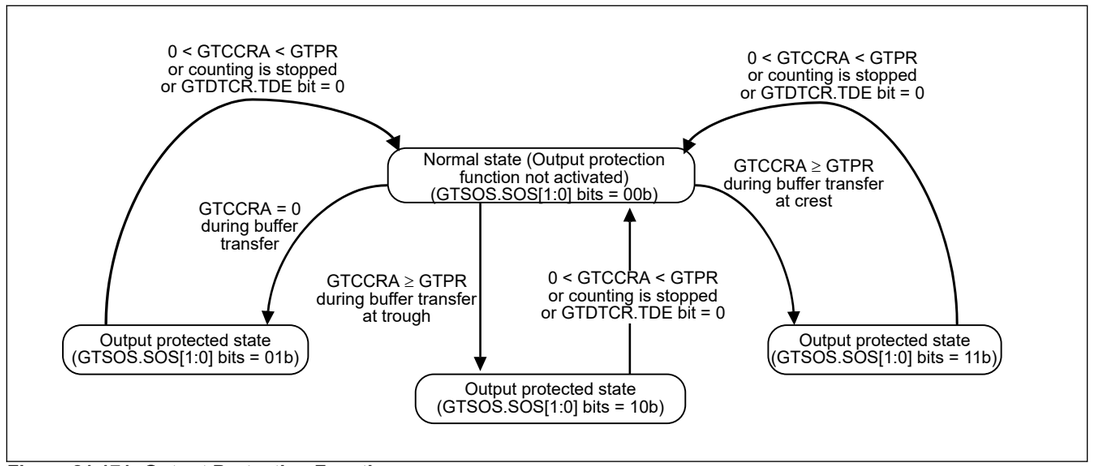
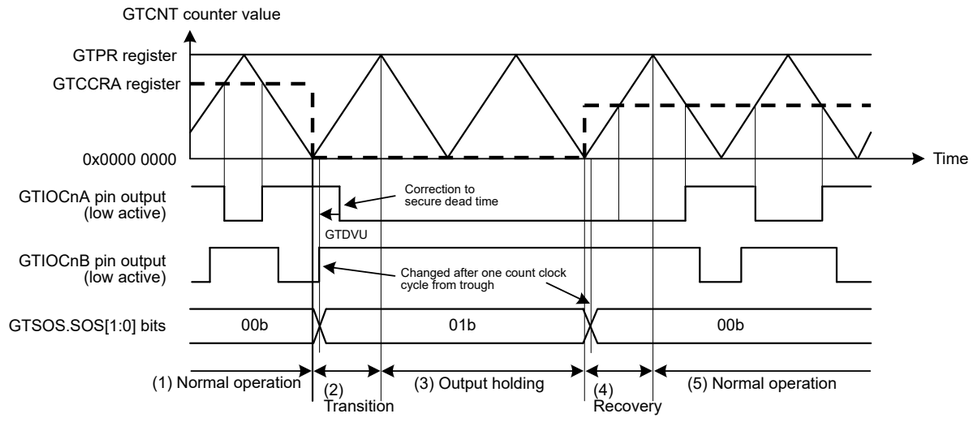


Figure 21.171 Output Protection Function

(1) Output Protection Function When the GTCCRA Register is Set to 0x0000 0000 during Buffer Transfer

Figure 21.172 and Figure 21.173 show examples of output protection function operation when the GTCCRA register is set to 0x0000 0000 during buffer transfer at troughs, and Figure 21.174 and Figure 21.175 show examples when the GTCCRA register is set to 0x0000 0000 during buffer transfer at crests.



(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Transition period : When GTCCRA = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period : The output is held while GTCCRA = 0.
(4) Recovery period : When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period : Toggle output due to a compare match is performed normally.

Figure 21.172 Example of Output Protection Function Operation When GTCCRA is Set to 0x0000 0000 during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low) (n = 0 to 9)

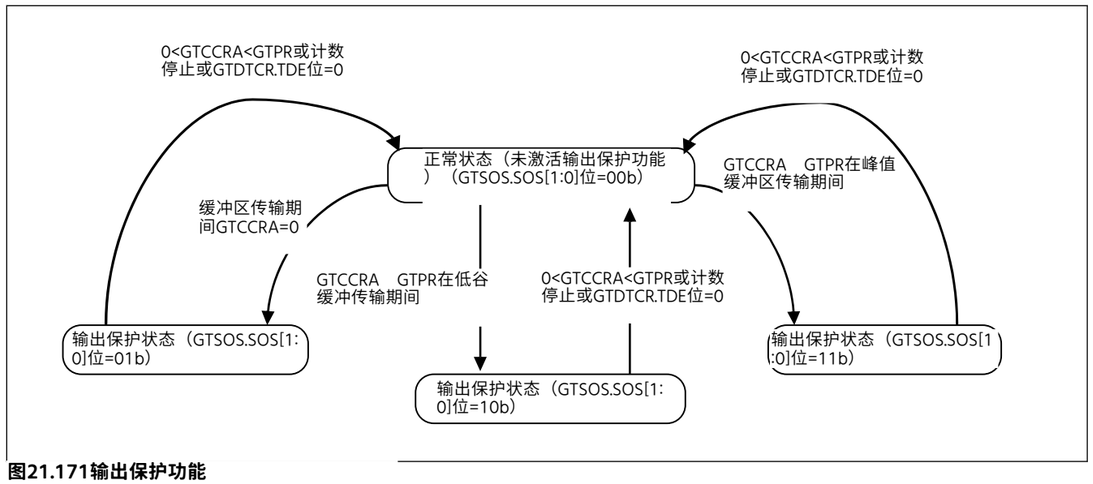
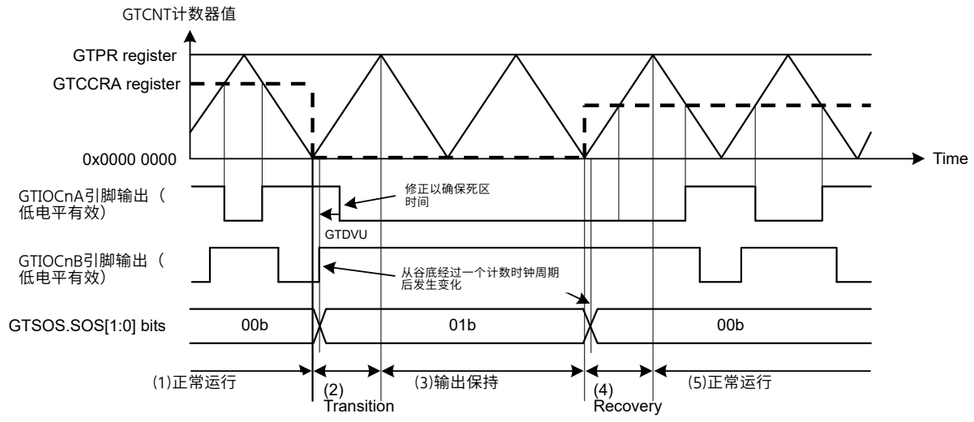


图21.171输出保护功能

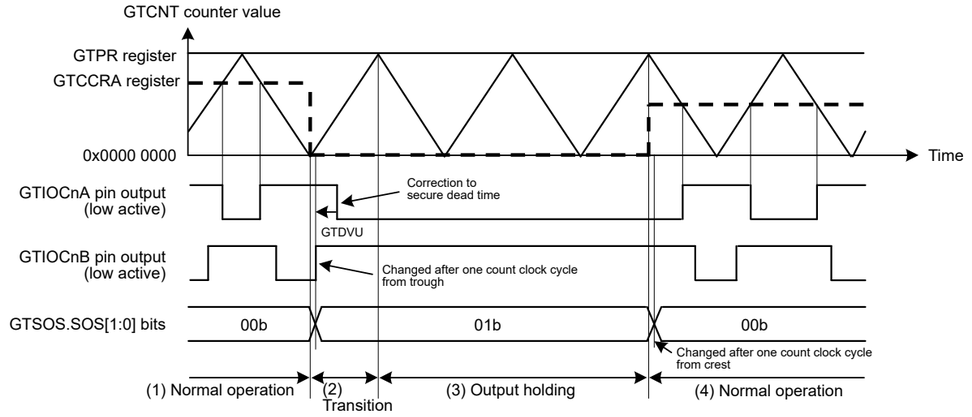
(1) 缓冲期间GTCCRA寄存器设置为0x00000000时的输出保护功能 Transfer

图21.172和图21.173显示了在波谷缓冲区传输期间GTCCRA寄存器设置为0x00000000时的输出保护功能操作示例，图21.174和图21.175显示了在波峰缓冲区传输期间GTCCRA寄存器设置为0x00000000的示例。



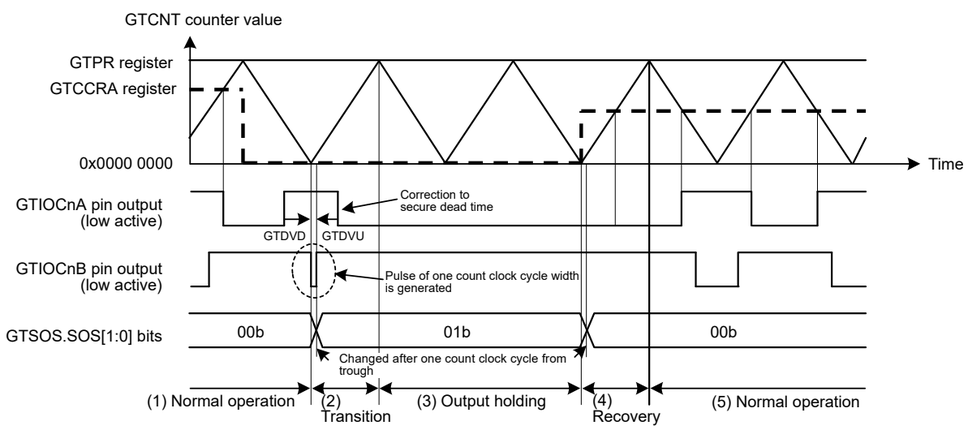
(1)正常运营期： 由于比较匹配而切换输出正常执行。
(2)过渡期： 当谷底检测到GTCCRA=0时，输出保护状态变为GTSOS.SOS[1:0]位=01b，并且切换输出持续到下一个波峰。
(3)输出保持期： 在GTCCRA=0时保持输出。
(4)恢复期： 当波谷检测到0<GTCCRA<GTPR时，输出保护状态变为GTSOS.SOS[1:0]位=00b，保持输出保持到下一个波峰。
(5)正常运营期： 由于比较匹配而切换输出正常执行。

图21.172GTCCRA设置为0x00000000时的输出保护功能操作示例 低谷处的缓冲区传输（在缓冲区传输期间恢复为0<GTCCRA<GTPR 低谷，活跃水平：低）（n=0到9）



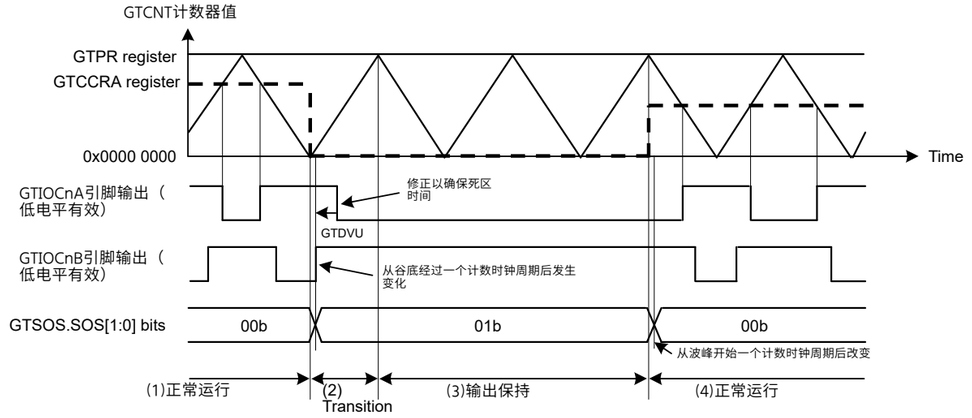
(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Transition period : When GTCCRA = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period : The output is held while GTCCRA = 0.
(4) Normal operation period : When 0 < GTCCRA < GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 21.173 Example of Output Protection Function Operation When GTCCRA is Set to 0x0000 0000 during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low) (n = 0 to 9)



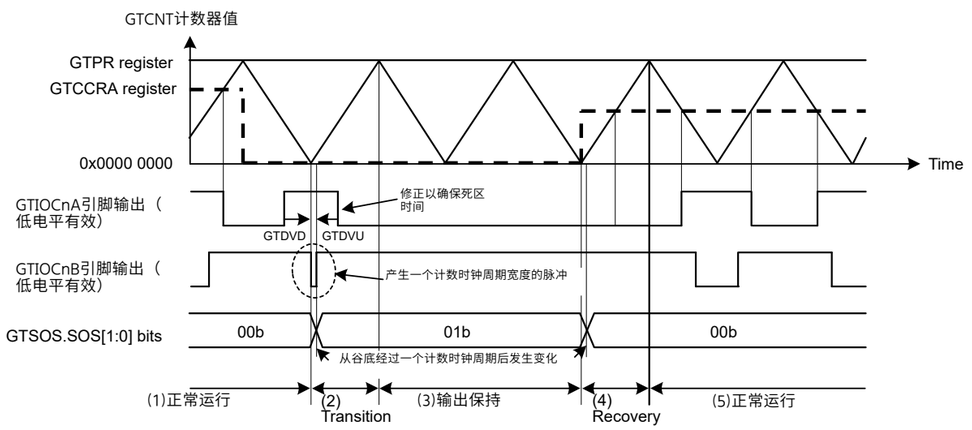
(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Transition period : When GTCCRA = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding : The output is held while GTCCRA = 0.
(4) Recovery period : When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period : Toggle output due to a compare match is performed normally.

Figure 21.174 Example of Output Protection Function Operation When GTCCRA is Set to 0x0000 0000 during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low) (n = 0 to 9)



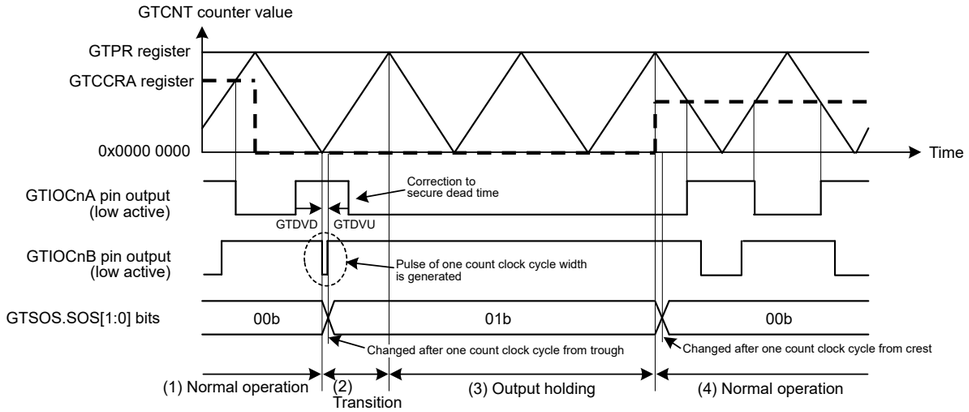
(1)正常运营期： 由于比较匹配而切换输出正常执行。
(2)过渡期： 当谷底检测到GTCCRA=0时，输出保护状态变为GTSOS.SOS[1:0]位=01b，并且切换输出持续到下一个波峰。
(3)输出保持期： 在GTCCRA=0时保持输出。
(4)正常运营期： 当波峰检测到0<GTCCRA<GTPR时，输出保护状态变为GTSOS.SOS[1:0]位=00b，并且由于比较匹配而正常执行切换输出。

图21.173GTCCRA设置为0x00000000时的输出保护功能操作示例 波谷缓冲转移（在波峰缓冲转移期间恢复为0<GTCCRA<GTPR，活动电平：低）（n=0到9）



(1)正常运营期： 由于比较匹配而切换输出正常执行。
(2)过渡期： 当谷底检测到GTCCRA=0时，输出保护状态变为GTSOS.SOS[1:0]位=01b，并且切换输出持续到下一个波峰。
(3)输出保持期： 在GTCCRA=0时保持输出。
(4)恢复期： 当波谷检测到0<GTCCRA<GTPR时，输出保护状态变为GTSOS.SOS[1:0]位=00b，保持输出保持到下一个波峰。
(5)正常运营期： 由于比较匹配而切换输出正常执行。

图21.174GTCCRA设置为0x00000000时的输出保护功能操作示例 波峰缓冲转移（在波谷缓冲转移期间恢复为0<GTCCRA<GTPR，活动电平：低）（n=0到9）

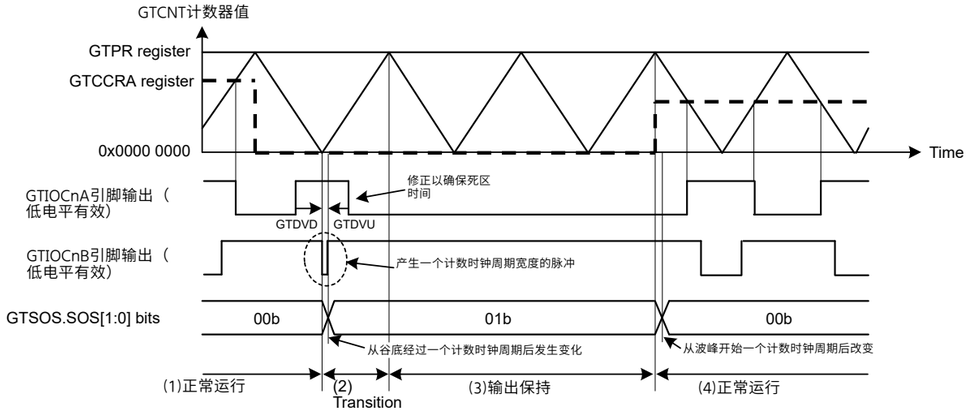


(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Transition period : When GTCCRA = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period : The output is held while GTCCRA = 0.
(4) Normal operation period : When 0 < GTCCRA < GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 21.175 Example of Output Protection Function Operation When the GTCCRA is Set to 0x0000 0000 during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low) (n = 0 to 9)

(2) Output Protection Function When GTCCRA Register ≥ GTPR Register is Set during Buffer Transfer at Troughs

Figure 21.176 and Figure 21.177 show examples of output protection function operation when GTCCRA register ≥ GTPR register is set during buffer transfer at troughs.

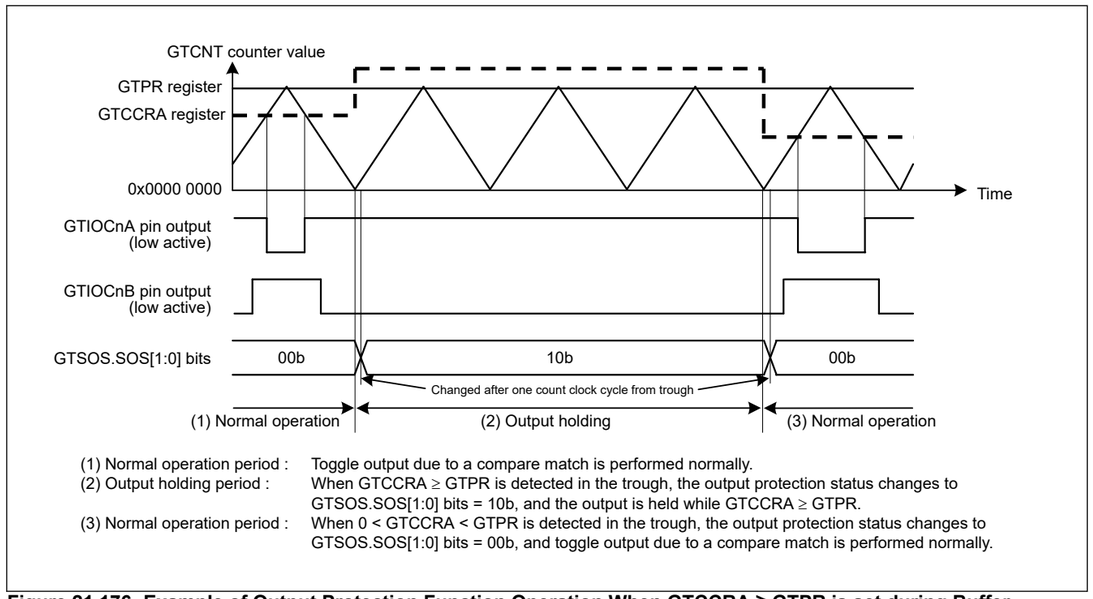


(1)正常运营期： 由于比较匹配而切换输出正常执行。
(2)过渡期： 当谷底检测到GTCCRA=0时，输出保护状态变为GTSOS.SOS[1:0]位=01b，并且切换输出持续到下一个波峰。
(3)输出保持期： 在GTCCRA=0时保持输出。
(4)正常运营期： 当波峰检测到0<GTCCRA<GTPR时，输出保护状态变为GTSOS.SOS[1:0]位=00b，并且由于比较匹配而正常执行切换输出。

图21.175峰值缓冲区传输期间GTCCRA设置为0x00000000时的输出保护功能操作示例（在峰值缓冲区传输期间恢复为0<GTCCRA<GTPR，有效 电平：低）（n=0至9）

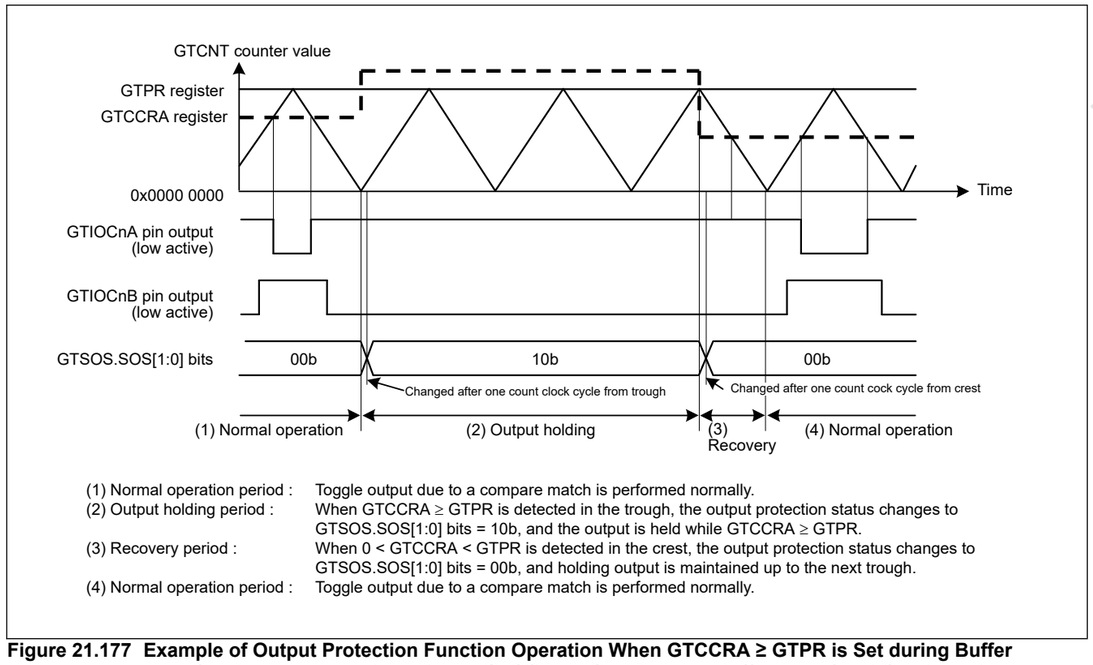
(2) 缓冲期间GTCCRA寄存器≥GTPR寄存器置位时的输出保护功能在低谷转移

图21.176和图21.177显示了在谷底缓冲区传输期间设置GTCCRA寄存器≥GTPR寄存器时的输出保护功能操作示例。



(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Output holding period : When GTCCRA ≥ GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 10b, and the output is held while GTCCRA ≥ GTPR.
(3) Normal operation period : When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 21.176 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is set during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low) (n = 0 to 9)

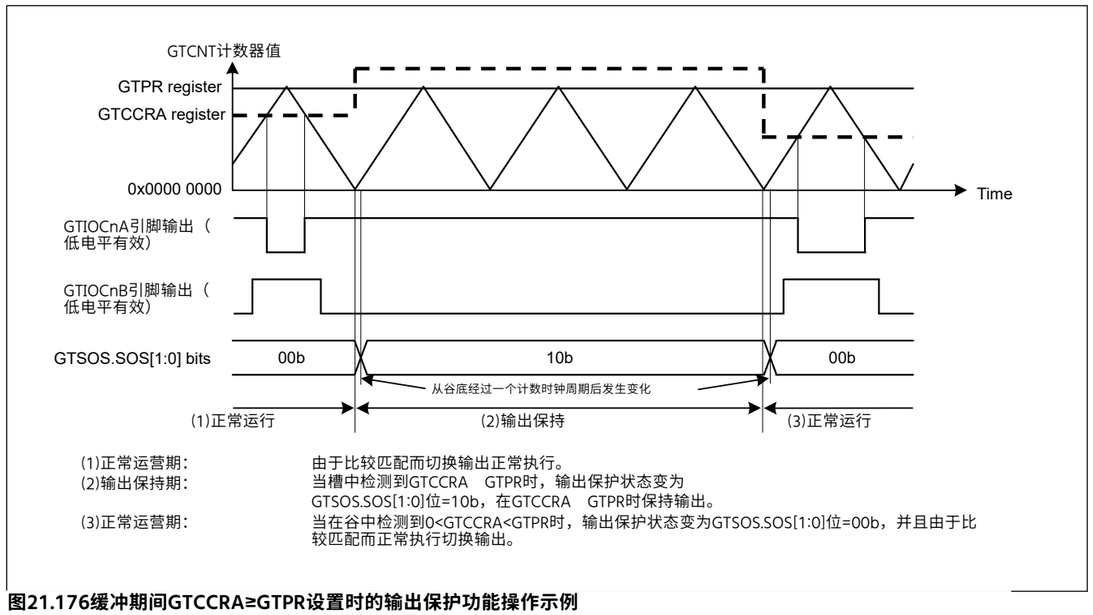


(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Output holding period : When GTCCRA ≥ GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 10b, and the output is held while GTCCRA ≥ GTPR.
(3) Recovery period : When 0 < GTCCRA < GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next trough.
(4) Normal operation period : Toggle output due to a compare match is performed normally.

Figure 21.177 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low) (n = 0 to 9)

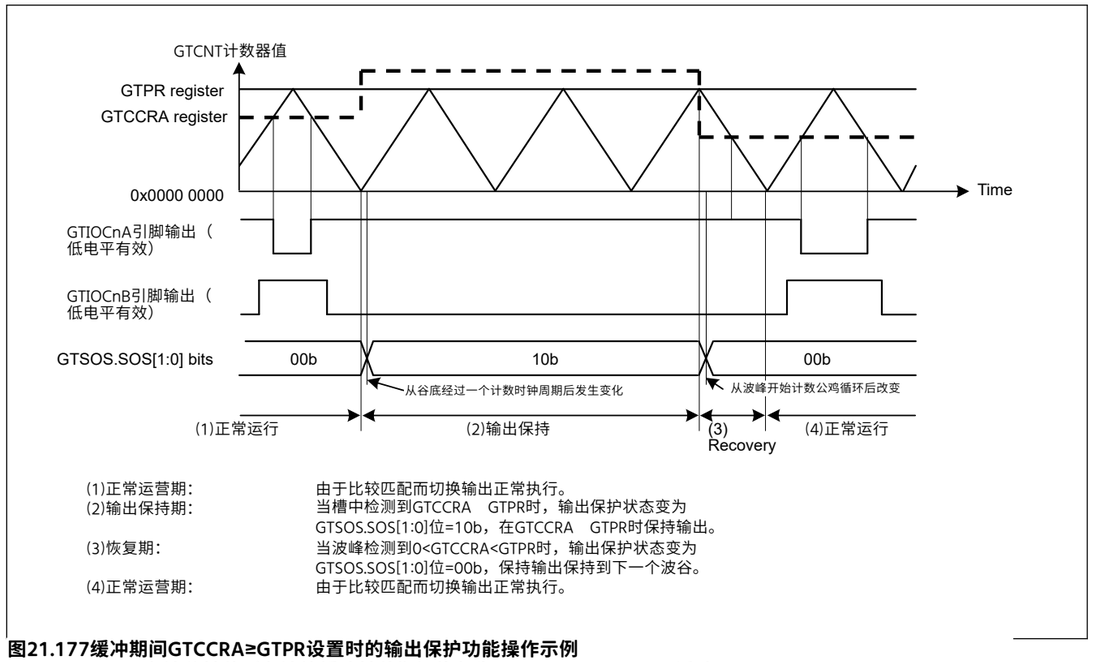
(3) Output Protection Function When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests

Figure 21.178 and Figure 21.179 show examples of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at crests.



(1)正常运营期： 由于比较匹配而切换输出正常执行。
(2)输出保持期： 当槽中检测到GTCCRA GTPR时，输出保护状态变为GTSOS.SOS[1:0]位=10b，在GTCCRA GTPR时保持输出。
(3)正常运营期： 当在谷中检测到0<GTCCRA<GTPR时，输出保护状态变为GTSOS.SOS[1:0]位=00b，并且由于比较匹配而正常执行切换输出。

图21.176缓冲期间GTCCRA≥GTPR设置时的输出保护功能操作示例 谷底转移（在谷底缓冲转移期间恢复为0<GTCCRA<GTPR，活动电平：低）（n=0到9）

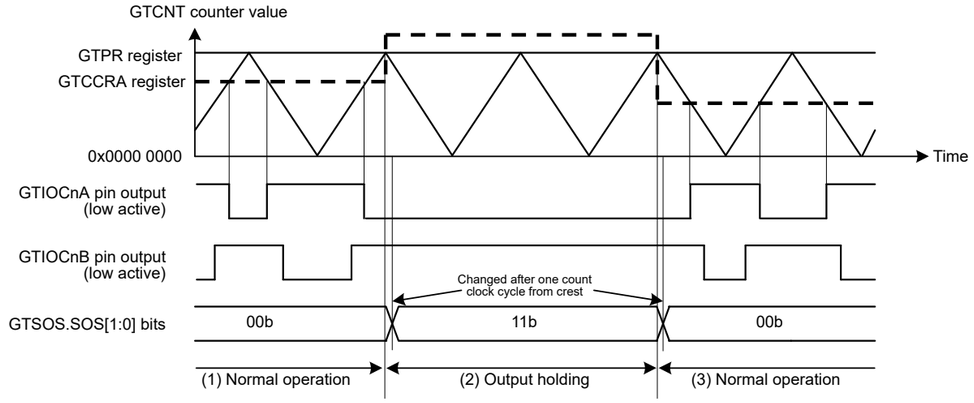


(1)正常运营期： 由于比较匹配而切换输出正常执行。
(2)输出保持期： 当槽中检测到GTCCRA GTPR时，输出保护状态变为GTSOS.SOS[1:0]位=10b，在GTCCRA GTPR时保持输出。
(3)恢复期： 当波峰检测到0<GTCCRA<GTPR时，输出保护状态变为GTSOS.SOS[1:0]位=00b，保持输出保持到下一个波谷。
(4)正常运营期： 由于比较匹配而切换输出正常执行。

图21.177缓冲期间GTCCRA≥GTPR设置时的输出保护功能操作示例 在波谷转移（在波峰缓冲转移期间恢复为0<GTCCRA<GTPR，活动 Level: Low) (n = 0 to 9)

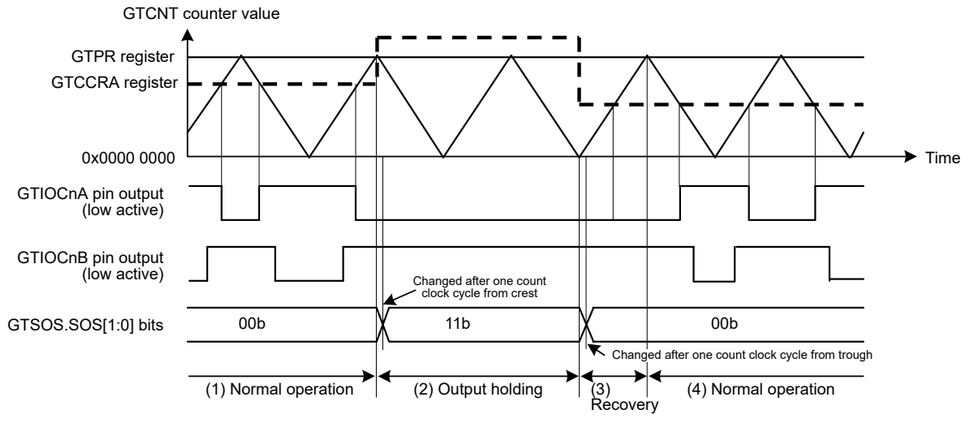
(3) 在峰值缓冲传输期间设置GTCCRA≥GTPR时的输出保护功能

图21.178和图21.179显示了在峰值缓冲区传输期间设置GTCCRA≥GTPR时输出保护功能操作的示例。



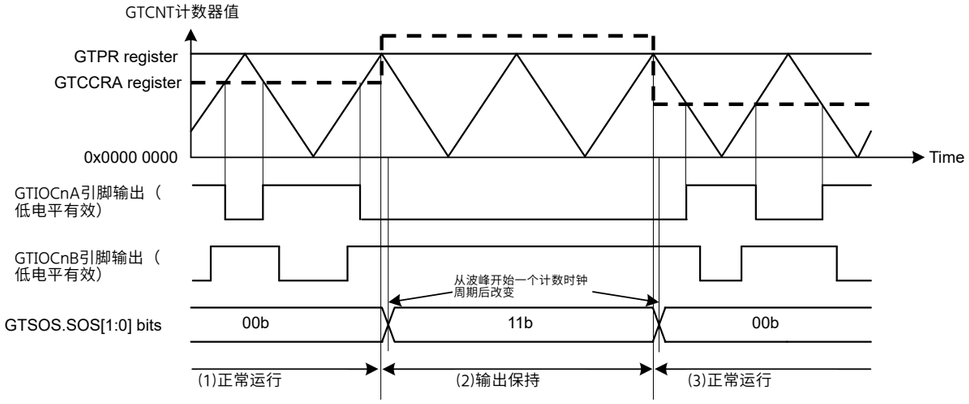
(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Output holding period : When GTCCRA ≥ GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 11b, and the output is held while GTCCRA ≥ GTPR.
(3) Normal operation period : When 0 < GTCCRA < GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 21.178 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low) (n = 0 to 9)



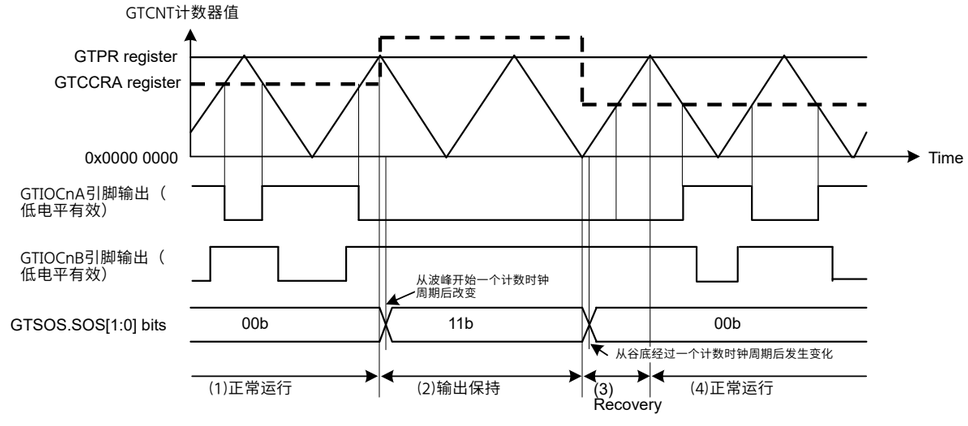
(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Output holding period : When GTCCRA ≥ GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] = 11b, and the output is held while GTCCRA ≥ GTPR.
(3) Recovery period : When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] = 00b, and holding output is maintained up to the next crest.
(4) Normal operation period : Toggle output due to a compare match is performed normally.

Figure 21.179 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low) (n = 0 to 9)



(1)正常运营期： 由于比较匹配而切换输出正常执行。
(2)输出保持期： 当波峰检测到GTCCRA GTPR时，输出保护状态变为GTSOS.SOS[1:0]位=11b，在GTCCRA GTPR时保持输出。
(3)正常运营期： 当波峰检测到0<GTCCRA<GTPR时，输出保护状态变为GTSOS.SOS[1:0]位=00b，并且由于比较匹配而正常执行切换输出。

图21.178缓冲期间GTCCRA≥GTPR设置时的输出保护功能操作示例 在波峰传输（在波峰缓冲传输期间恢复为0<GTCCRA<GTPR，活动 Level: Low) (n = 0 to 9)



(1)正常运营期： 由于比较匹配而切换输出正常执行。
(2)输出保持期： 当波峰检测到GTCCRA GTPR时，输出保护状态变为GTSOS.SOS[1:0]=11b，在GTCCRA GTPR时保持输出。
(3)恢复期： 当波谷检测到0<GTCCRA<GTPR时，输出保护状态变为GTSOS.SOS[1:0]=00b，保持输出保持到下一个波峰。
(4)正常运营期： 由于比较匹配而切换输出正常执行。

图21.179缓冲期间GTCCRA≥GTPR设置时的输出保护功能操作示例 在波峰转移（在波谷缓冲转移期间恢复为0<GTCCRA<GTPR，活动 Level: Low) (n = 0 to 9)

(4) Restricted Specification of Output Protection Function

Even if an incorrect value (0x0000 0000 or a value greater than or equal to the GTPR register value) is set in the GTCCRA register during count operation, the output protection functions in a specific way such that one of the positive- and negative-phase outputs becomes non-active. However, if the following condition is not satisfied, the output protection does not operate normally.

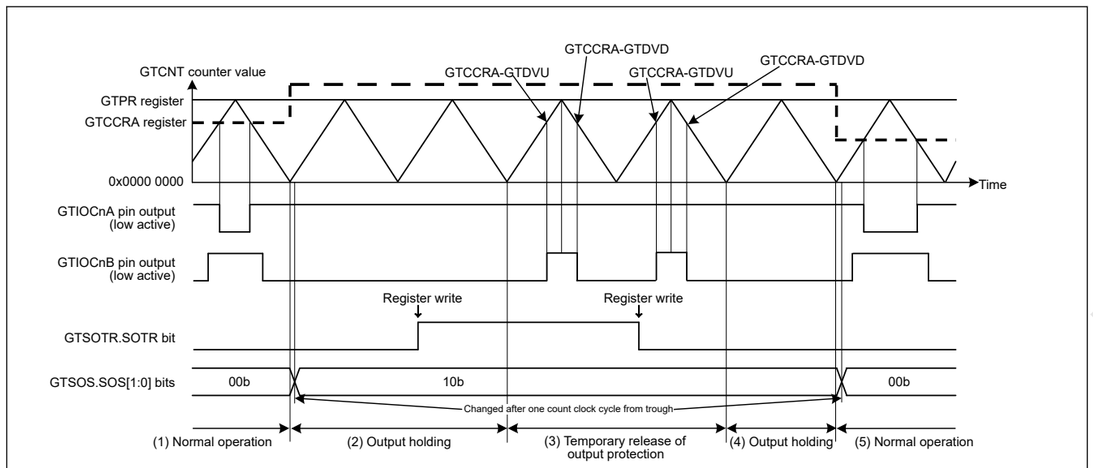
- When the GTCCRA register value at the start of count operation is greater than 0x0000 0000, and less than the setting value of the GTPR register

(5) Temporary Release of Output Protection Function

When the GTSOS.SOS[1:0] bits = 10b (protected state in which GTCCRA register ≥ GTPR register has occurred during transfer at trough), the protected state of the GTIOCnB pin output can be temporarily released by setting the GTSOTR.SOTR bit to 1. The SOS[1:0] bits retain 10b even if the output protection function is released.

When the SOTR bit is set to 0, the GTIOCnB pin output protection can be restarted.

Figure 21.180 shows examples of the operation of temporary release of output protection when the setting of the GTCCRA register ≥ GTPR register during buffer transfer at troughs.



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 10b, and the output is held while GTCCRA ≥ GTPR.
Even when the GTSOTR.SOTR bit is set to 1 during the output holding period, the GTIOCnB pin output is held until the first trough after the setting.
(3) Output protection temporary release period: After GTSOTR.SOTR bit is set to 1, the GTIOCnB pin output is performed normally from the first trough after the setting.
Even when the GTSOTR.SOTR bit is set to 0 during the output protection releasing period, the GTIOCnB pin output is held until the first trough after the setting.
(4) Output holding period: The output is held until 0 < GTCCRA < GTPR is detected in the trough.
(5) Normal operation period: When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 21.180 Example of Temporary Release of Output Protection When the Setting of the GTCCRA ≥ GTPR during Buffer Transfer at Trough s (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low) (n = 0 to 9)

21.9 Initialization Method of Output Pins

21.9.1 Pin Settings after Reset

The GPT registers are initialized at a reset. Start counting after selecting the port pin function with the PmnPFS register, setting GTIOR.OAE and GTIOR.OBE bits, and outputting the GPT function to external pins.

(4) 输出保护功能限制规格

即使在计数操作期间在GTCCRA寄存器中设置了不正确的值（0x00000000或大于或等于GTPR寄存器值的值），输出保护也会以特定方式起作用，使得正相和负相输出之一变为非积极的。但是，如果不满足以下条件，则输出保护不能正常动作。

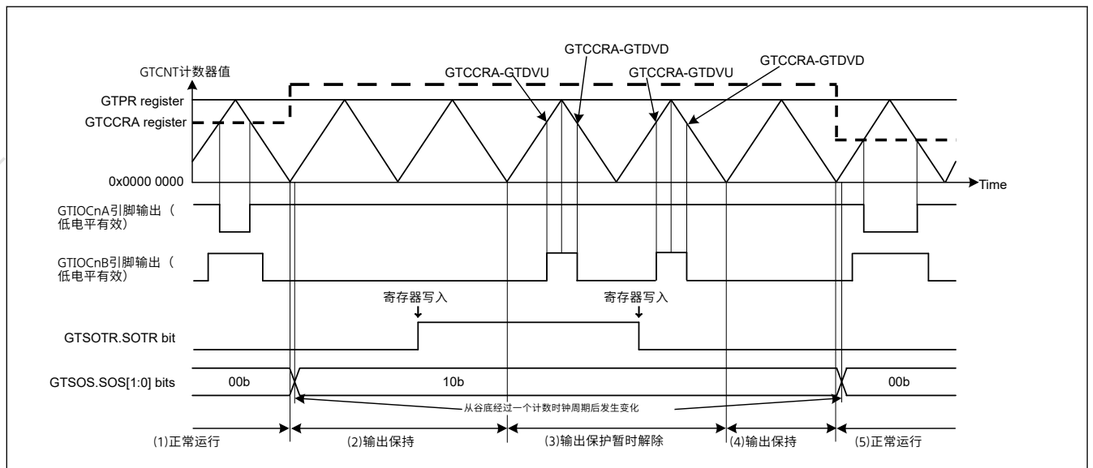
●当计数操作开始时GTCCRA寄存器值大于0x00000000，且小于GTPR寄存器的设置值时

(5) 输出保护功能暂时解除

当GTSOS.SOS[1:0]位=10b时（在低谷传输期间发生GTCCRA寄存器≥GTPR寄存器的保护状态），通过设置GTSOTR.SOTR位可以暂时解除GTIOCnB引脚输出的保护状态为1。即使输出保护功能解除，SOS[1:0]位仍保持10b。

当SOTR位设置为0时，可以重新启动GTIOCnB引脚输出保护。

图21.180显示了在谷底缓冲传输期间，当GTCCRA寄存器的设置≥GTPR寄存器时，输出保护的临时解除操作示例。



(1)正常运营期：由于比较匹配而切换输出正常执行。
(2)输出保持周期：当检测到GTCCRA GTPR处于波谷时，输出保护状态变为GTSOS.SOS[1:0]bits=10b，输出保持同时GTCCRA GTPR。即使在输出保持期间GTSOTR.SOTR位设置为1，GTIOCnB引脚输出也会保持到设置后的第一个波谷。(3)输出保护临时解除周期：GTSOTR.SOTR位设置为1后，GTIOCnB引脚输出从设置后的第一个波谷开始正常进行。即使在输出保护解除期间将GTSOTR.SOTR位设置为0，GTIOCnB引脚输出也会保持到设置后的第一个波谷。

(4)输出保持期：保持输出直到在波谷中检测到0<GTCCRA<GTPR。
(5)正常运营期：当在谷中检测到0<GTCCRA<GTPR时，输出保护状态变为GTSOS.SOS[1:0]位=00b，并且由于比较匹配而正常执行切换输出。

图21.180谷s缓冲转移期间GTCCRA≥GTPR的设置时输出保护的临时解除示例（在谷s缓冲转移期间恢复为0<GTCCRA<GTPR，有效 电平：低）（n=0至9）

21.9 输出管脚的初始化方法

21.9.1 复位后的引脚设置

GPT寄存器在复位时被初始化。通过PmnPFS寄存器选择端口引脚功能，设置GTIOR.OAE和GTIOR.OBE位，并将GPT功能输出到外部引脚后开始计数。

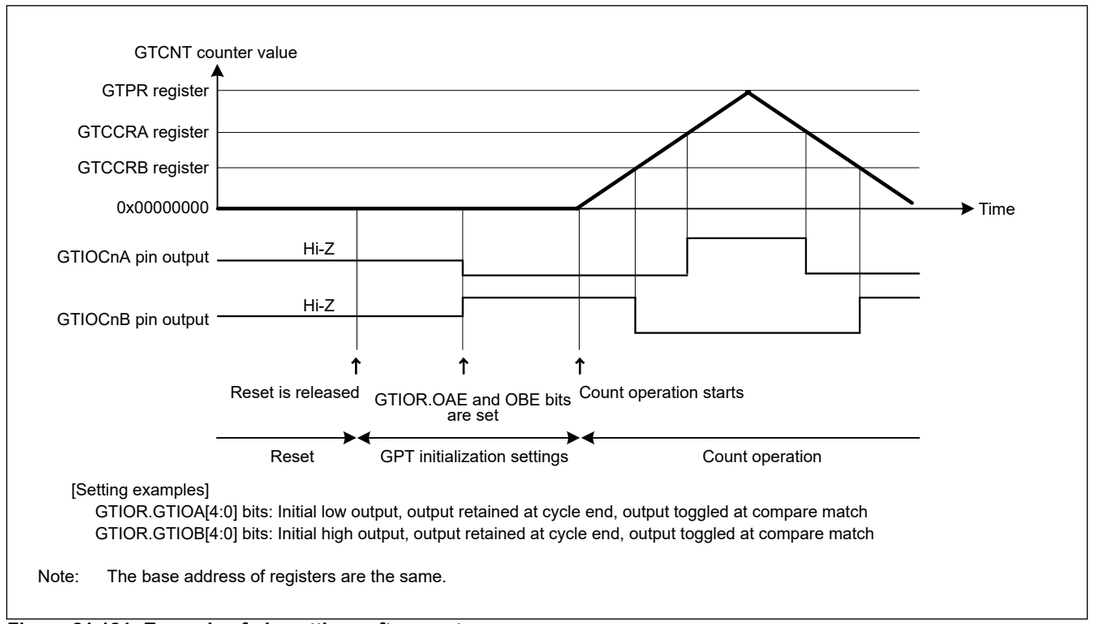


Figure 21.181 Example of pin settings after reset

21.9.2 Pin Initialization Due to Error during Operation

If an error occurs during GPT operation, the following four types of pin control can be performed before pin initialization:

- Set the OAHLD and OBHLD bits in GTIOR to 1 and retain the outputs at count stop
- Set the OAHLD and OBHLD bits in GTIOR to 0, specify arbitrary output values at OADFLT and OBDFLT in GTIOR, and output the arbitrary values at count stop
- Set the pin to output an arbitrary value as a general output port by setting the PDR, PODR registers and PmnPFS.PMR bit of the I/O port in advance. Set the OAE and OBE bits in GTIOR to 0, and the control bit associated with the pin in the PMR to 0 to allow arbitrary values to be output from the pin set as a general output port when an error occurs.
- Drive the output to a high impedance state using the POEG function.

If the automatic dead time setting is made, clear the GTDTCR.TDE bit to 0 after counting stops. When counting stops, only the values of registers that are changed by a GPT external source change. If counting is resumed, operation continues from where it stopped. If counting is stopped, the registers must be initialized before counting starts.

21.10 Usage Notes

21.10.1 Module-Stop Function Setting

The Module Stop Control Register can enable or disable GPT operation. The GPT is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

Set GTCLKCR register before releasing the module-stop state.

21.10.2 GTCCRn Settings during Compare Match Operation (n = A to F)

(1) When automatic dead time setting is made in triangle-wave PWM mode

The GTCCRA register must satisfy all of the following conditions:

- GTDVU < GTCCRA
- GTCCRA > GTDVD
- 0 < GTCCRA < GTPR

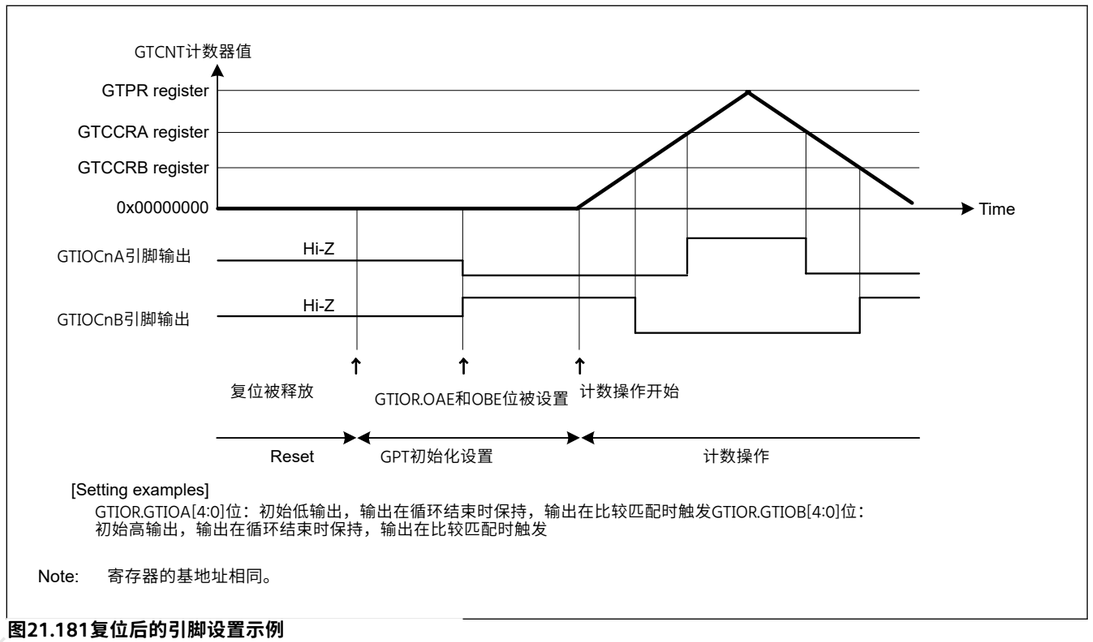


图21.181复位后的引脚设置示例

21.9.2 由于操作过程中的错误而导致的引脚初始化

如果在GPT操作过程中发生错误，可以在引脚初始化之前进行以下四种引脚控制：

●将GTIOR中的OAHLD和OBHLD位设置为1，并在计数停止时保留输出

●将GTIOR中的OAHLD和OBHLD位设置为0，在GTIOR中的OADFLT和OBDFLT指定任意输出值，并在计数停止时输出任意值

●通过预先设置IO端口的PDR、PODR寄存器和PmnPFS.PMR位，将引脚设置为输出任意值作为通用输出端口。将GTIOR中的OAE和OBE位设置为0，并将与PMR中的引脚相关的控制位设置为0，以允许在发生错误时从设置为通用输出端口的引脚输出任意值。

●使用POEG功能将输出驱动为高阻抗状态。

如果进行了自动死区时间设置，则在计数停止后将GTDTCR.TDE位清零。当计数停止时，只有被GPT外部源改变的寄存器的值会改变。如果重新开始计数，则从停止处继续操作。如果停止计数，则必须在计数开始前初始化寄存器。

21.10 使用说明

21.10.1 模块停止功能设置

模块停止控制寄存器可以启用或禁用GPT操作。GPT在重置后最初停止。
释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

在释放模块停止状态之前设置GTCLKCR寄存器。

21.10.2 比较匹配操作期间的GTCCRn设置（n=A到F）

(1) 在三角波PWM模式下进行自动死区时间设置时

GTCCRA寄存器必须满足以下所有条件：

- GTDVU < GTCCRA
- GTCCRA > GTDVD
- 0 < GTCCRA < GTPR

When the setting of GTCCRA = 0 or GTCCRA ≥ GTPR is made for the GTCCRA register during count operation, the output protection function is activated. However, if the following condition is not satisfied, the output protection function does not work normally:

- The value of the GTCCRA register at the start of counting is larger than 0 and less than GTPR.

For details, see section 21.8.4. Output Protection Function for GTIOCnm Pin Output (n = 0 to 9; m = A, B)

(2) When automatic dead time setting is not made in triangle-wave PWM mode

The GTCCRA register must be set within the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. When GTCCRA > GTPR, no compare match occurs.

Similarly, GTCCRB must be set within the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB is 0 or GTCCRB = GTPR is satisfied. When GTCCRB > GTPR, no compare match occurs.

(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, the correct output waveforms with secured dead time may not be obtained.

- In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVD
- In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR - GTDVU, GTCCRD > GTDVD

(4) When automatic dead time setting is not made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRC < GTCCRD < GTPR
- In down-counting: GTPR > GTCCRC > GTCCRD > 0

Similarly, GTCCRE and GTCCRF must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRE < GTCCRF < GTPR
- In down-counting: GTPR > GTCCRE > GTCCRF > 0.

(5) In saw-wave PWM mode

The GTCCRA register must be set with the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. If GTCCRA > GTPR is set, no compare match occurs.

Similarly, GTCCRB must be set with the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. If GTCCRB > GTPR is set, no compare match occurs.

(6) In Complementary PWM mode 1, 2, 3

The GTCCRn register must be set with the range of 0 ≤ GTCCRn ≤ GTPR + GTDVU.

(7) In Complementary PWM mode 4

In single buffer operation, the GTCCRn register must be set with the range of 0 ≤ GTCCRn ≤ GTPR + GTDVU.

In double buffer operation, the GTCCRn register must be set with the range of GTDVU < GTCCRn < GTPR.

21.10.3 Setting Range for GTCNT Counter

Other than the Saw-wave PWM mode 2 and Complementary PWM mode, the GTCNT counter register must be set with the range of 0 ≤ GTCNT ≤ GTPR.

当在计数操作期间对GTCCRA寄存器设置GTCCRA=0或GTCCRA≥GTPR时，输出保护功能被激活。但是，如果不满足以下条件，则输出保护功能不能正常工作：

●计数开始时GTCCRA寄存器的值大于0小于GTPR。

详见21.8.4节。GTIOCnm引脚输出的输出保护功能（n=0至9；m=A、B）

(2) 在三角波PWM模式下未进行自动死区时间设置时

GTCCRA寄存器必须设置在0<GTCCRA<GTPR的范围内。如果设置了GTCCRA=0或GTCCRA=GTPR，则仅当满足GTCCRA=0或GTCCRA=GTPR时，才会在周期内发生比较匹配。当GTCCRA>GTPR时，不发生比较匹配。

同样，GTCCRB必须设置在0<GTCCRB<GTPR的范围内。如果设置了GTCCRB=0或GTCCRB=GTPR，则仅当GTCCRB为0或GTCCRB=GTPR满足时，才会在周期内发生比较匹配。当GTCCRB>GTPR时，不发生比较匹配。

(3) 在锯波单发脉冲模式下进行自动死区时间设置时

GTCCRC和GTCCRD寄存器必须设置为满足以下限制。如果不满足这些限制，则可能无法获得具有安全死区时间的正确输出波形。

- In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVD
- In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR - GTDVU, GTCCRD > GTDVD

(4) 在锯波单发脉冲模式下未进行自动死区时间设置时

GTCCRC和GTCCRD寄存器必须设置为满足以下限制。如果不满足限制，则不会发生两个比较匹配，并且无法执行脉冲输出。

- In up-counting: 0 < GTCCRC < GTCCRD < GTPR
- In down-counting: GTPR > GTCCRC > GTCCRD > 0

同样，必须设置GTCCRE和GTCCRF以满足以下限制。如果不满足限制，则不会发生两个比较匹配，并且无法执行脉冲输出。

- In up-counting: 0 < GTCCRE < GTCCRF < GTPR
- In down-counting: GTPR > GTCCRE > GTCCRF > 0.

(5) 在锯齿波PWM模式下

GTCCRA寄存器必须设置为0<GTCCRA<GTPR。如果设置了GTCCRA=0或GTCCRA=GTPR，则仅当满足GTCCRA=0或GTCCRA=GTPR时，才会在周期内发生比较匹配。如果设置了GTCCRA>GTPR，则不会发生比较匹配。

类似地，GTCCRB必须设置在0<GTCCRB<GTPR的范围内。如果设置了GTCCRB=0或GTCCRB=GTPR，则仅当满足GTCCRB=0或GTCCRB=GTPR时，才会在周期内发生比较匹配。如果设置了GTCCRB>GTPR，则不会发生比较匹配。

(6) 在互补PWM模式1、2、3

GTCCRn寄存器的设置范围必须为0≤GTCCRn≤GTPR+GTDVU。

(7) 在互补PWM模式4

在单缓冲操作中，GTCCRn寄存器必须设置在0≤GTCCRn≤GTPR+GTDVU的范围内。

在双缓冲操作中，GTCCRn寄存器必须设置为GTDVU<GTCCRn<GTPR。

21.10.3 GTCNT计数器的设置范围

除了Saw-wavePWM模式2和互补PWM模式，GTCNT计数器寄存器必须设置为0≤GTCNT≤GTPR的范围。

21.10.4 Starting and Stopping the GTCNT Counter

The control timing of starting and stopping the GTCNT counter by the GTCR.CST bit synchronizes the count clock that is selected in GTCR.TPCS[3:0]. When GTCR.CST is updated, the GTCNT counter starts/stops after a count clock that is selected in GTCR.TPCS[3:0]. Therefore, an event generated before the GTCNT counter actually starts is ignored, resulting in situations in which an event is accepted or an interrupt occurs after GTCR.CST is set to 0.

21.10.5 Priority Order of Each Event

(1) GTCNT register

Table 21.74 shows a priority order of events updating the GTCNT register.

Table 21.74 Priority order of sources updating GTCNT

Source updating GTCNT	Priority order
Writing by CPU (writing to GTCNT/GTCLR)	High
Clear by hardware sources set in GTCSR	↑
Count up or down by hardware sources set in GTUPSR/GTDNSR	↑
Count operation	Low

If up-counting and down-counting by hardware sources occur at the same time, the GTCNT counter value does not change.
When there is a conflict between updating the GTCNT register and reading by the CPU, pre-update data is read.

(2) GTCR.CST bit

When there is a conflict between starting/stopping by hardware sources set in the GTSSR/GTPSR registers and writing by the CPU (writing to GTCR/GTSTR/GTSTP registers), the writing by CPU has priority over the starting/stopping by hardware sources.

In case that stop by the period count function conflicts with start by the CPU writing (GTCR register writing/GTSTR register writing), the period count function is finished with setting the GTST.PCF flag. The CST bit is not changed and the GTCNT continues to count.

When there is a conflict between starting by hardware sources set in the GTSSR register and stopping by hardware sources set in GTPSR register, the GTCR.CST bit value does not change. When there is a conflict between updating the GTCR.CST bit and reading by the CPU (reading from GTCR/GTSTR/GTSTP registers), pre-update data is read.

(3) GTCCRm registers (m = A to F)

When there is a conflict between input capture/buffer transfer operation and writing to the GTCCRm registers, the writing to GTCCRm registers has priority over input capture/buffer transfer operation. When there is a conflict between input capture and writing to the counter register by the CPU or updating the counter register by hardware sources, the pre-update counter value is captured. When there is a conflict between updating the GTCCRm registers and reading by the CPU, pre-update data is read.

(4) GTPR register

When there is a conflict between buffer transfer operation and writing to the GTPR register, writing to GTPR register has priority over buffer transfer operation. When there is a conflict between updating GTPR register and reading by the CPU, pre-update data is read.

(5) GTADTRm registers (m = A, B)

When there is a conflict between buffer transfer operation and writing to GTADTRm register, writing to GTADTRm register has priority over buffer transfer operation.

When there is a conflict between updating the GTADTRm register and reading by the CPU, pre-update data is read.

(6) GTDVm registers (m = U, D)

When there is a conflict between buffer transfer operation and writing to GTDVm register, writing to GTDVm register has priority over buffer transfer operation.

21.10.4 启动和停止GTCNT计数器

通过GTCR.CST位启动和停止GTCNT计数器的控制时序与在GTCR.TPCS[3:0]中选择的计数时钟同步。当GTCR.CST更新时，GTCNT计数器在GTCR.TPCS[3:0]中选择的计数时钟后开始停止。因此，在GTCNT计数器实际启动之前产生的事件将被忽略，从而导致在GTCR.CST设置为0之后接受事件或发生中断的情况。

21.10.5 每个事件的优先顺序

(1) GTCNT register

表21.74显示了更新GTCNT寄存器的事件的优先级顺序。

Table 21.74 更新GTCNT的源的优先顺序

源更新GTCNT	优先顺序
CPU写入（写入GTCNTGTCLR）	High
由GTCSR中设置的硬件源清除	↑
通过GTUPSRGTDNSR中设置的硬件源进行向上或向下计数	↑
计数操作	Low

如果硬件源的递增计数和递减计数同时发生，GTCNT计数器值不会改变。
当更新GTCNT寄存器和CPU读取之间存在冲突时，会读取更新前的数据。

(2) GTCR.CST bit

当GTSSRGTPSR寄存器中设置的硬件源启动停止与CPU写入（写入GTCRGTSTRGTSTP寄存器）发生冲突时，CPU写入优先于硬件源启动停止。

如果周期计数功能停止与CPU写入启动（GTCR寄存器写入GTSTR寄存器写入）发生冲突，则周期计数功能通过设置GTST.PCF标志结束。CST位不变，GTCNT继续计数。

当GTSSR寄存器中设置的硬件源启动和GTPSR寄存器中设置的硬件源停止之间存在冲突时，GTCR.CST位的值不会改变。当更新GTCR.CST位与CPU读取（从GTCRGTSTRGTSTP寄存器读取）之间存在冲突时，将读取更新前数据。

(3) GTCCRm寄存器（m=A到F）

当输入捕捉缓冲区传输操作与写入GTCCRm寄存器之间存在冲突时，写入GTCCRm寄存器优先于输入捕捉缓冲区传输操作。当输入捕获与CPU写入计数器寄存器或硬件源更新计数器寄存器之间存在冲突时，将捕获更新前的计数器值。当更新GTCCRm寄存器和CPU读取之间存在冲突时，会读取更新前的数据。

(4) GTPR register

当缓冲区传输操作与写入GTPR寄存器之间存在冲突时，写入GTPR寄存器优先于缓冲区传输操作。当更新GTPR寄存器与CPU读取发生冲突时，读取更新前的数据。

(5) GTADTRm registers (m = A, B)

当缓冲区传输操作和写入GTADTRm寄存器之间存在冲突时，写入GTADTRm寄存器优先于缓冲区传输操作。

当更新GTADTRm寄存器与CPU读取之间存在冲突时，会读取更新前的数据。

(6) GTDVm registers (m = U, D)

当缓冲区传输操作与写入GTDVm寄存器发生冲突时，写入GTDVm寄存器优先于缓冲区传输操作。

When there is a conflict between updating the GTDVm register and reading by the CPU, pre-update data is read.

(7) GTIOR.GTIOm registers (m = A, B)

When there is a conflict between buffer transfer operation and writing to GTIOR.GTIOm register, writing to GTIOR.GTIOm register has priority over buffer transfer operation.

When there is a conflict between updating the GTIOR.GTIOm and reading by the CPU, pre-update data is read.

21.10.6 Interval of interrupt request

When the core clock of GPT is GPTCLK, interrupt may be lost if the interval between the same interrupt signal is shorter than the following value. However, this restriction does not apply to different interrupt signals.

Interrupt_Interval [ns] = Period_of_GPTCLK [ns] * 6 + Period_of_PCLKA [ns] * 4

For the restriction of event signal, see section 17, Event Link Controller (ELC).

Also, ADC can receive the A/D conversion start request from GPT without going through ELC by setting ADTRGGPTx register (x = 0 to 8).

Again, when the clocks of GPT and ADC are combined as shown in Table 21.75, the A/D conversion start request may be lost if the interval between one A/D conversion start request and the next is less than the following value for the same A/D conversion start request.

However, this restriction does not apply to different A/D conversion start request.

Event_Interval [ns] = Period_of_GPT_core_clock [ns] * 6 + Period_of_ADC_core_clock [ns] * 4

Table 21.75 Combination of clocks with the restricted Event Interval

GPT core clock	ADC core clock
GPTCLK	PCLKA or PCLKC
PCLKD	PCLKC or GPTCLK

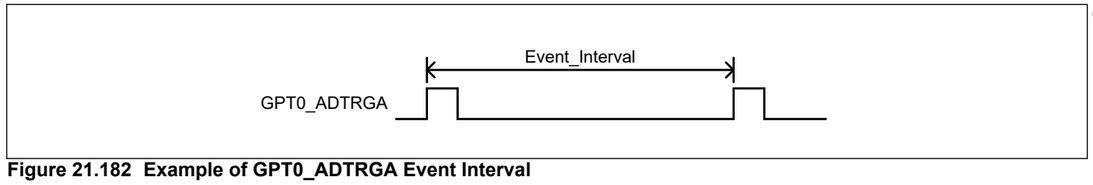


Figure 21.182 Example of GPT0_ADTRGA Event Interval

21.10.7 Notes on the GTIOCnm signal input to PWM Delay Generation Circuit (n = 0 to 3, m = A, B)

When controlling the delay of PWM waveform in PWM Delay Generation Circuit, the following limitations exist.

- In saw-wave mode, It is prohibited to change the GTIOCnm signal during the three clock cycles immediately before overflow or underflow.
- In saw-wave mode, it is prohibited to clear the GTCNT register by GTCSR during counting operation.
- In triangle-wave mode, It is prohibited to change the GTIOCnm signal during the three clock cycles immediately before trough.

If the above limitations are not followed, the edge of signal waveform output from PWM Delay Generation Circuit may disappear.

Figure 21.183 shows an example of the change timing of an unacceptable GTIOCnm signal.

当更新GTDVm寄存器与CPU读取之间存在冲突时，会读取更新前的数据。

(7) GTIOR.GTIOm registers (m = A, B)

当缓冲区传输操作和写入GTIOR.GTIOm寄存器之间存在冲突时，写入GTIOR.GTIOm寄存器优先于缓冲区传输操作。

当更新GTIOR.GTIOm和CPU读取之间存在冲突时，读取更新前的数据。

21.10.6 中断请求的间隔

当GPT的核心时钟为GPTCLK时，如果同一中断信号之间的间隔小于以下值，则可能会丢失中断。但是，此限制不适用于不同的中断信号。

Interrupt_Interval [ns] = Period_of_GPTCLK [ns] * 6 + Period_of_PCLKA [ns] * 4

有关事件信号的限制，请参见第17节，事件链接控制器(ELC)。

此外，通过设置ADTRGGPTx寄存器（x=0到8），ADC可以接收来自GPT的AD转换开始请求，而无需通过ELC。

同样，当GPT和ADC的时钟如表21.75所示组合时，如果一个AD转换开始请求和下一个AD转换开始请求之间的间隔小于相同AD转换开始请求的以下值，则可能会丢失AD转换开始请求.

但是，此限制不适用于不同的AD转换启动请求。

Event_Interval [ns] = Period_of_GPT_core_clock [ns] * 6 + Period_of_ADC_core_clock [ns] * 4

Table 21.75 时钟与受限事件间隔的组合

GPT核心时钟	ADC内核时钟
GPTCLK	PCLKA or PCLKC
PCLKD	PCLKC or GPTCLK

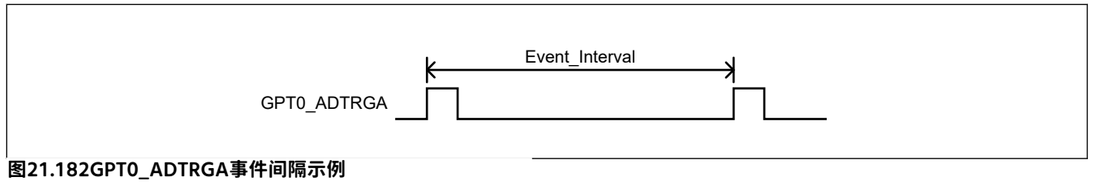


图21.182GPT0_ADTRGA事件间隔示例

21.10.7 GTIOCnm信号输入到PWM延迟发生电路的注意事项（n=0到3，m=A，B）

在PWM延迟发生电路中控制PWM波形的延迟时，存在以下限制。

●在锯齿波模式下，在上溢或下溢之前的三个时钟周期内禁止改变GTIOCnm信号。

●在锯齿波模式下，计数操作期间禁止通过GTCSR清除GTCNT寄存器。

●在三角波模式下，在波谷之前的三个时钟周期内禁止改变GTIOCnm信号。

如果不遵守上述限制，PWM延迟产生电路输出的信号波形边沿可能会消失。

图21.183显示了一个不可接受的GTIOCnm信号的变化时序示例。

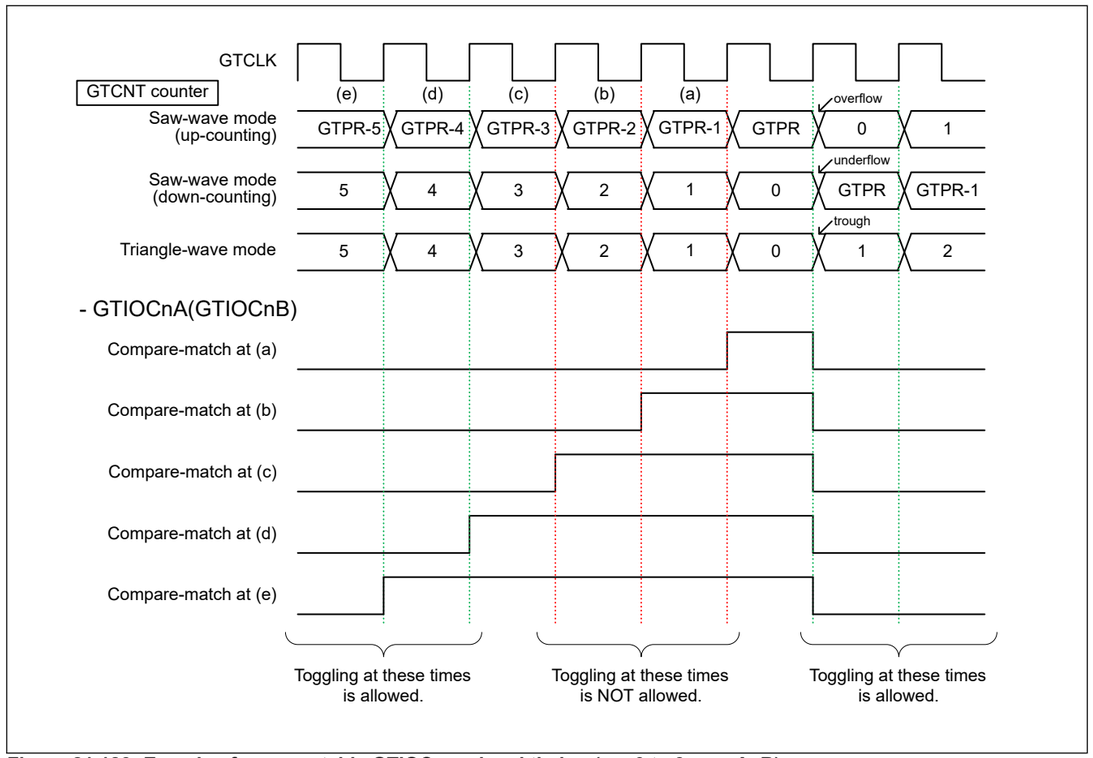


Figure 21.183 Eample of unacceptable GTIOCnm signal timing (n = 0 to 3, m = A, B)

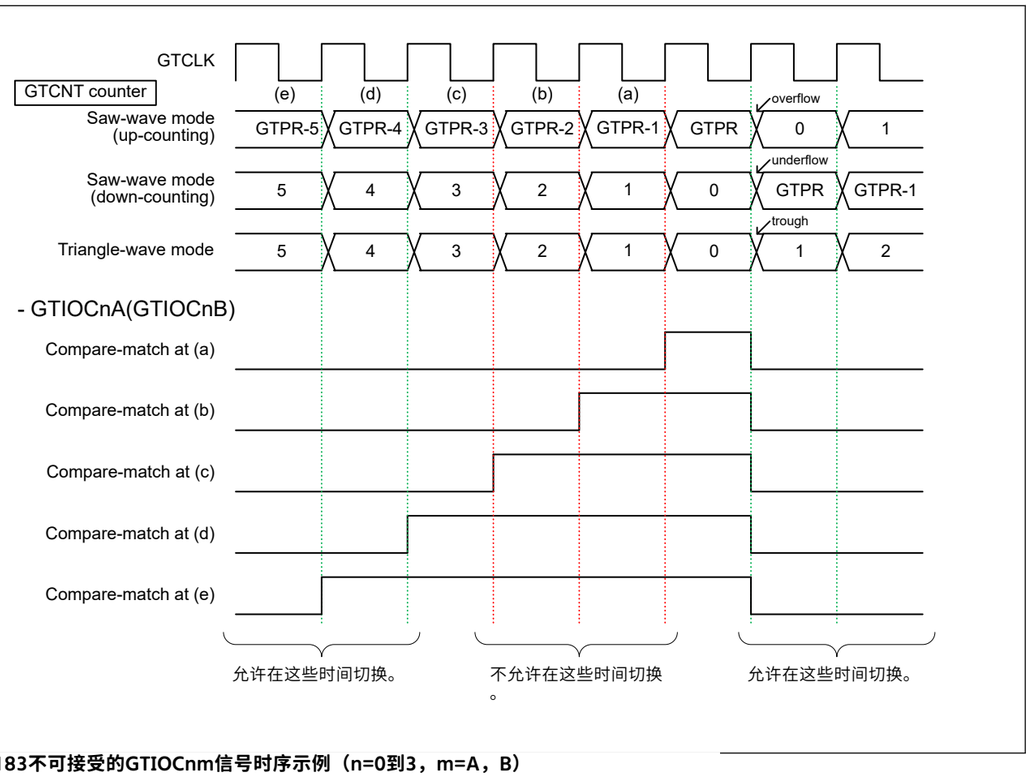


图21.183不可接受的GTIOCnm信号时序示例（n=0到3，m=A，B）

22. PWM Delay Generation Circuit (PDG)

22.1 Overview

The PWM Delay Generation circuit (PDG) has 4 channels delay circuits that can connect to the GPT. The PDG can control the rise and fall edge timing with which the PWM output for the GPT320 through the GPT323.

Table 22.1 lists the specifications for the PWM Delay Generation Circuit, Figure 22.1 shows a block diagram, and Table 22.2 lists the I/O pins.

Table 22.1 Specifications of the PWM Delay Generation Circuit

Parameter	Specifications
Function	The circuit can control the timing with which signals on the two PWM output pins for channel 0/1/2/3 rise and fall to an accuracy of up to 1/32 times the period of the GPT core clock (GTCLK). The GPT core clock (GTCLK) can be selected from PCLKD or GPTCLK.

22. PWM延迟产生电路(PDG)

22.1 Overview

PWM延迟生成电路(PDG)有4个通道延迟电路，可以连接到GPT。PDG可以通过GPT323控制GPT320的PWM输出的上升沿和下降沿时序。

表22.1列出了PWM延迟产生电路的规格，图22.1显示了框图，表22.2列出了IO引脚。

Table 22.1 PWM延迟发生电路的规格

Parameter	Specifications
Function	该电路可以控制通道0123的两个PWM输出引脚上的信号上升和下降的时序，精度高达GPT内核时钟(GTCLK)周期的132倍。GPT内核时钟(GTCLK)可以从PCLKD或GPTCLK中选择。

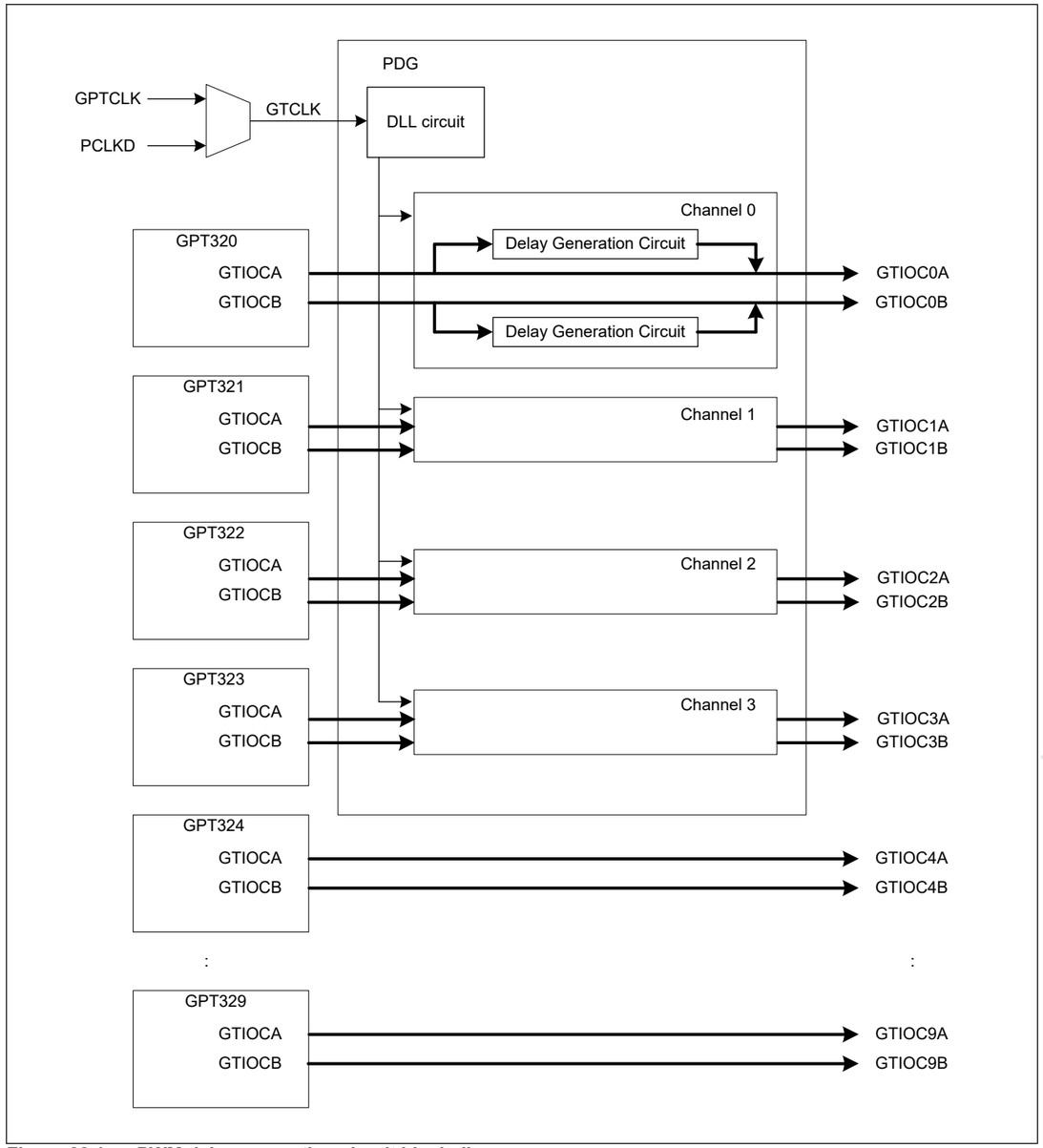


Figure 22.1 PWM delay generation circuit block diagram

Table 22.2 PWM delay generation circuit I/O pins (1 of 2)

I/O pin	I/O	Function
GTIOC0A	Output	Delayed output of GTIOCA pin of GPT channel 0
GTIOC0B	Output	Delayed output of GTIOCB pin of GPT channel 0
GTIOC1A	Output	Delayed output of GTIOCA pin of GPT channel 1
GTIOC1B	Output	Delayed output of GTIOCB pin of GPT channel 1
GTIOC2A	Output	Delayed output of GTIOCA pin of GPT channel 2

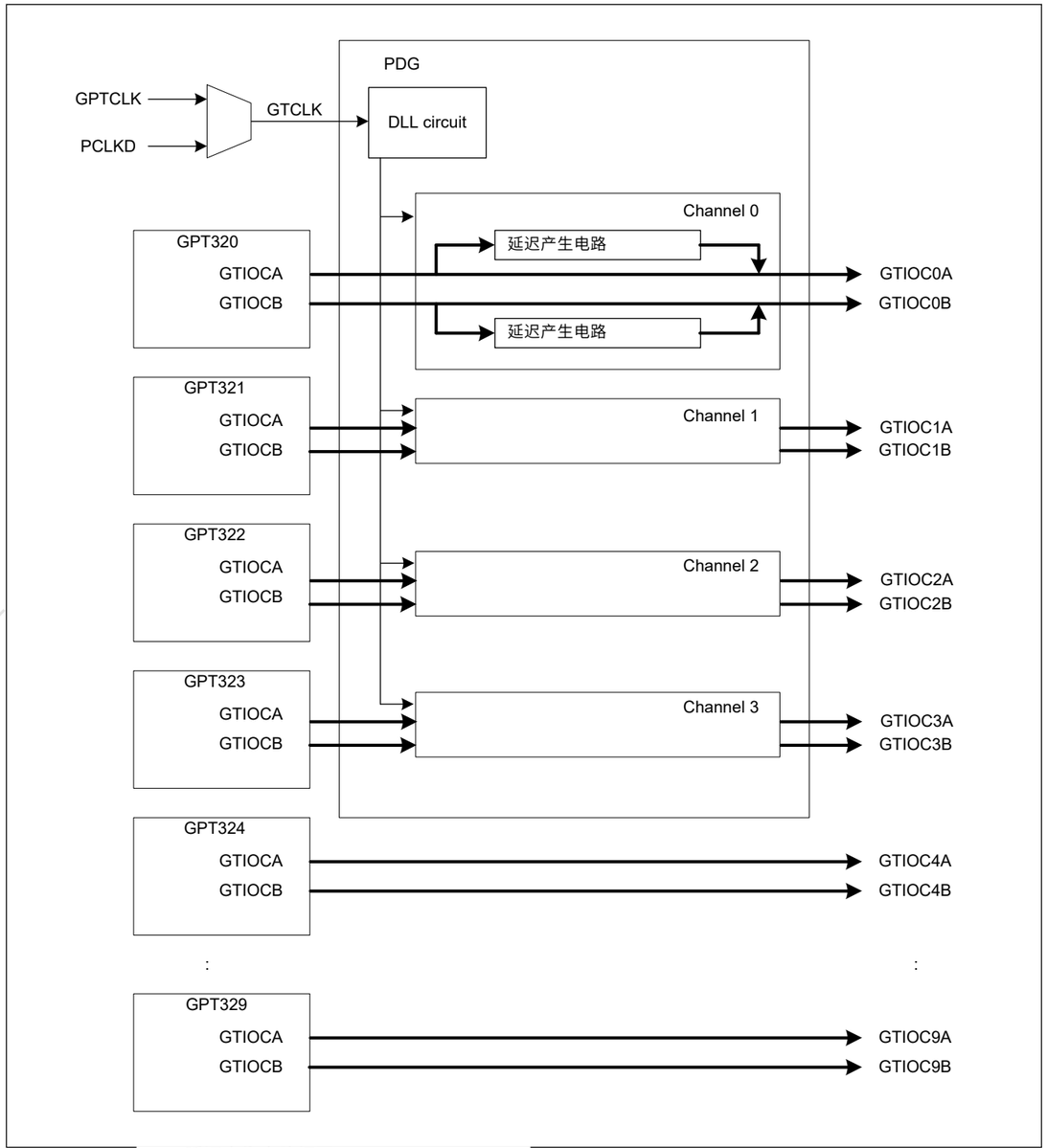


Figure 22.1 PWM延迟产生电路框图

Table 22.2 PWM延迟生成电路IO引脚（2个中的1个）

I/O pin	I/O	Function
GTIOC0A	Output	GPT通道0的GTIOCA管脚延迟输出
GTIOC0B	Output	GPT通道0的GTIOCB管脚延迟输出
GTIOC1A	Output	GPT通道1的GTIOCA管脚延迟输出
GTIOC1B	Output	GPT通道1的GTIOCB管脚延迟输出
GTIOC2A	Output	GPT通道2的GTIOCA管脚延迟输出

Table 22.2 PWM delay generation circuit I/O pins (2 of 2)

I/O pin	I/O	Function
GTIOC2B	Output	Delayed output of GTIOCB pin of GPT channel 2
GTIOC3A	Output	Delayed output of GTIOCA pin of GPT channel 3
GTIOC3B	Output	Delayed output of GTIOCB pin of GPT channel 3

22.2 Register Descriptions

22.2.1 GTDLYCR : PWM Output Delay Control Register

Base address: PDG = 0x4016_A000

Offset address: 0x0000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FRANGE	—	—	—	—	—	—	DLYRST	DLLEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLLEN	DLL Operation Enable 0: DLL operation disabled 1: DLL operation enabled	R/W
1	DLYRST	PWM Delay Generation Circuit Reset 0: Normal operation 1: Reset	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	FRANGE	GPT core clock Frequency Range 0: GPT core clock frequency is 115 MHz to 200 MHz 1: GPT core clock frequency is 80 MHz to 120 MHz	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

The GTDLYCR register controls the PWM delay generation circuit, which applies delays to the PWM outputs. GTDLYCR register can be written when register write protection is disabled (GPT320.GTWP.WP = 0).

When changing GTDLYCR after changing the value of GPT320.GTWP.WP bit, be sure to read back the value of GTWP register before changing the value of GTDLYCR.

DLLEN bit (DLL Operation Enable)

The DLLEN bit selects whether the on-chip DLL in the PWM delay generation circuit is activated or not.

DLYRST bit (PWM Delay Generation Circuit Reset)

The DLYRST bit resets the internal state of the PWM delay generation circuit.

FRANGE bit (GPT core clock Frequency Range)

The FRANGE bit sets the frequency range of the GPT core clock.

Set the FRANGE bit only when the DLLEN bit is 0.

Table 22.2 PWM延迟产生电路IO引脚(2of2)

I/O pin	I/O	Function
GTIOC2B	Output	GPT通道2的GTIOCB管脚延迟输出
GTIOC3A	Output	GPT通道3的GTIOCA管脚延迟输出
GTIOC3B	Output	GPT通道3的GTIOCB管脚延迟输出

22.2 注册说明

22.2.1 GTDLYCR:PWM输出延迟控制寄存器

Base address: PDG = 0x4016_A000

Offset address: 0x0000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	法兰西	—	—	—	—	—	—	DLYRST	DLLEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLLEN	DLL操作启用 0：禁用DLL操作1：启用DLL操作	R/W
1	DLYRST	PWM延迟产生电路复位 0：正常运行1：复位	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
8	FRANGE	GPT内核时钟频率范围 0：GPT内核时钟频率为115MHz至200MHz1：GPT内核时钟频率为80MHz至120MHz	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

GTDLYCR寄存器控制PWM延迟生成电路，该电路将延迟应用于PWM输出。当寄存器写保护被禁用时（GPT320.GTWP.WP=0），可以写入GTDLYCR寄存器。

在更改GPT320.GTWP.WP位的值后更改GTDLYCR时，务必在更改GTDLYCR的值之前回读GTWP寄存器的值。

DLLEN位（DLL操作使能）

DLLEN位选择是否激活PWM延迟产生电路中的片上DLL。

DLYRST位（PWM延迟产生电路复位）

DLYRST位复位PWM延迟产生电路的内部状态。

FRANGE位（GPT内核时钟频率范围）

FRANGE位设置GPT内核时钟的频率范围。

仅当DLLEN位为0时设置FRANGE位。

22.2.2 GTDLYCR2 : PWM Output Delay Control Register 2

Base address: PDG = 0x4016_A000

Offset address: 0x0002

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	DLYEN3	DLYEN2	DLYEN1	DLYEN0	—	—	—	—	DLYBS3	DLYBS2	DLYBS1	DLYBS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLYBS0	PWM Delay Generation Circuit bypass for channel 0 0: Delay generation circuit of channel 0 bypassed 1: Delay generation circuit of channel 0 not bypassed	R/W
1	DLYBS1	PWM Delay Generation Circuit bypass for channel 1 0: Delay generation circuit of channel 1 bypassed 1: Delay generation circuit of channel 1 not bypassed	R/W
2	DLYBS2	PWM Delay Generation Circuit bypass for channel 2 0: Delay generation circuit of channel 2 bypassed 1: Delay generation circuit of channel 2 not bypassed	R/W
3	DLYBS3	PWM Delay Generation Circuit bypass for channel 3 0: Delay generation circuit of channel 3 bypassed 1: Delay generation circuit of channel 3 not bypassed	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	DLYEN0	PWM Delay Generation Circuit enable for channel 0 0: Delay generation circuit of channel 0 enabled 1: Delay generation circuit of channel 0 disabled	R/W
9	DLYEN1	PWM Delay Generation Circuit enable for channel 1 0: Delay generation circuit of channel 1 enabled 1: Delay generation circuit of channel 1 disabled	R/W
10	DLYEN2	PWM Delay Generation Circuit enable for channel 2 0: Delay generation circuit of channel 2 enabled 1: Delay generation circuit of channel 2 disabled	R/W
11	DLYEN3	PWM Delay Generation Circuit enable for channel 3 0: Delay generation circuit of channel 3 enabled 1: Delay generation circuit of channel 3 disabled	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W

The GTDLYCR2 register controls each channel of PWM delay generation circuit. GTDLYCR2 can be written when register write protection is disabled (GPT320.GTWP.WP = 0).

When changing GTDLYCR2 after changing the value of GPT320.GTWP.WP bit, be sure to read back the value of GTWP register before changing the value of GTDLYCR2.

DLYBSn (n = 0 to 3) bit (PWM Delay Generation Circuit Bypass for channel n)

The DLYBSn bit selects whether delays are applied to PWM output signals from the GTIOCnA and GTIOCnB pins (n = 0 to 3) by the PWM delay generation circuit or whether the circuit is bypassed.

A signal delayed in the PWM delay generation circuit is output 3 cycles of GPT core clock (GTCLK) later than if it bypasses the PWM delay generation circuit.

DLYENn (n = 0 to 3) bit (PWM Delay Generation Circuit Enable for channel n)

The DLYENn bit selects whether channel n (n = 0 to 3) of PWM delay generation circuit is power on or off. If channel n of the PWM delay generation circuit is not used, set to 1.

22.2.2 GTDLYCR2：PWM输出延迟控制寄存器2

Base address: PDG = 0x4016_A000

Offset address: 0x0002

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	DLYEN3	DLYEN2	DLYEN1	DLYEN0	—	—	—	—	DLYBS3	DLYBS2	DLYBS1	DLYBS0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLYBS0	通道0的PWM延迟生成电路旁路 0：通道0的延时产生电路被旁路1：通道0的延时产生电路不被旁路	R/W
1	DLYBS1	通道1的PWM延迟生成电路旁路 0：通道1的延迟产生电路被旁路1：通道1的延迟产生电路不被旁路	R/W
2	DLYBS2	通道2的PWM延迟生成电路旁路 0：通道2的延迟产生电路被旁路1：通道2的延迟产生电路不被旁路	R/W
3	DLYBS3	通道3的PWM延迟生成电路旁路 0：通道3的延迟产生电路被旁路1：通道3的延迟产生电路不被旁路	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	DLYEN0	通道0的PWM延迟生成电路使能 0：启用通道0的延迟产生电路1：禁用通道0的延迟产生电路	R/W
9	DLYEN1	通道1的PWM延迟生成电路使能 0：启用通道1的延迟产生电路1：禁用通道1的延迟产生电路	R/W
10	DLYEN2	通道2的PWM延迟生成电路使能 0：启用通道2的延迟产生电路1：禁用通道2的延迟产生电路	R/W
11	DLYEN3	通道3的PWM延迟生成电路使能 0：通道3延迟产生电路有效1：通道3延迟产生电路无效	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W

GTDLYCR2寄存器控制PWM延迟产生电路的每个通道。当寄存器写保护被禁用（GPT320.GTWP.WP=0）时，可以写入GTDLYCR2。

在更改GPT320.GTWP.WP位的值后更改GTDLYCR2时，务必在更改GTDLYCR2的值之前回读GTWP寄存器的值。

DLYBSn（n=0到3）位（通道n的PWM延迟生成电路旁路）

DLYBSn位选择是否通过PWM延迟生成电路对来自GTIOCnA和GTIOCnB引脚（n=0至3）的PWM输出信号施加延迟，或者是否绕过该电路。

在PWM延迟发生电路中延迟的信号比绕过PWM延迟发生电路的信号晚3个GPT内核时钟(GTCLK)周期输出。

DLYENn（n=0到3）位（通道n的PWM延迟生成电路使能）

DLYENn位选择PWM延迟发生电路的通道n（n=0到3）是打开还是关闭。如果不使用PWM延迟发生电路的通道n，则设置为1。

22.2.3 GTDLYRnA : GTIOCnA Rising Output Delay Register (n = 0 to 3)

Base address: PDG = 0x4016_A000

Offset address: 0x018 + 0x4 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DLY[4:0]	GTIOCnA Output Rising Edge Delay Setting 0x00: Delay on rising edges is not applied 0x01: Delay of 1/32 times GTCLK period applied 0x02: Delay of 2/32 times GTCLK period applied 0x03: Delay of 3/32 times GTCLK period applied 0x04: Delay of 4/32 times GTCLK period applied 0x05: Delay of 5/32 times GTCLK period applied 0x06: Delay of 6/32 times GTCLK period applied 0x07: Delay of 7/32 times GTCLK period applied 0x08: Delay of 8/32 times GTCLK period applied 0x09: Delay of 9/32 times GTCLK period applied 0x0A: Delay of 10/32 times GTCLK period applied 0x0B: Delay of 11/32 times GTCLK period applied 0x0C: Delay of 12/32 times GTCLK period applied 0x0D: Delay of 13/32 times GTCLK period applied 0x0E: Delay of 14/32 times GTCLK period applied 0x0F: Delay of 15/32 times GTCLK period applied 0x10: Delay of 16/32 times GTCLK period applied 0x11: Delay of 17/32 times GTCLK period applied 0x12: Delay of 18/32 times GTCLK period applied 0x13: Delay of 19/32 times GTCLK period applied 0x14: Delay of 20/32 times GTCLK period applied 0x15: Delay of 21/32 times GTCLK period applied 0x16: Delay of 22/32 times GTCLK period applied 0x17: Delay of 23/32 times GTCLK period applied 0x18: Delay of 24/32 times GTCLK period applied 0x19: Delay of 25/32 times GTCLK period applied 0x1A: Delay of 26/32 times GTCLK period applied 0x1B: Delay of 27/32 times GTCLK period applied 0x1C: Delay of 28/32 times GTCLK period applied 0x1D: Delay of 29/32 times GTCLK period applied 0x1E: Delay of 30/32 times GTCLK period applied 0x1F: Delay of 31/32 times GTCLK period applied	R/W
15:5	—	These bits are read as 0. The write value should be 0.	R/W

The GTDLYRnA register sets a delay to be applied to rising edges of output signals on the GTIOCnA pin. On the timing for the transfer of settings, see section 22.3.2. Timing for Transfer of GTDLYRnA, GTDLYRnB, GTDLYFnA, and GTDLYFnB Register Settings.

GTDLYRnA can be written when register write protection is disabled (GPT32n.GTWP.WP = 0).

When changing GTDLYRnA after changing the value of GPT32n.GTWP.WP bit, be sure to read back the value of GTWP register before changing the value of GTDLYRnA.

22.2.3 GTDLYRnA:GTIOCnA上升沿输出延迟寄存器(n=0to3)

Base address: PDG = 0x4016_A000

Offset address: 0x018 + 0x4 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DLY[4:0]	GTIOCnA输出上升沿延迟设置 0x00：不应用上升沿延迟0x01：应用延迟132倍GTCLK周期0x02：应用延迟232倍GTCLK周期0x03：延迟3应用32倍GTCLK周期0x04：延迟4应用32倍GTCLK周期0x05:延迟532倍GTCLK周期0x06:延迟632倍GTCLK周期0x07:延迟732倍GTCLK周期0x08:延迟832倍GTCLK周期0x09:延迟932倍GTCLK周期0x0A:延迟1032倍GTCLK周期0x0B:延迟1132倍GTCLK周期0x0C:延迟1232倍GTCLK周期0x0D:延迟1332倍GTCLK周期0x0E:延迟1432倍GTCLK周期0x0F:延迟1532倍GTCLK周期0x10:延迟1632倍GTCLK周期0x11:延迟1732倍GTCLK周期0x12:延迟1832倍GTCLK周期0x13:延迟1932倍GTCLK周期0x14:延迟2032倍GTCLK周期应用0x15:应用2132倍GTCLK周期的延迟0x16：应用2232倍GTCLK周期的延迟0x17：应用2332倍GTCLK周期的延迟0x18：应用2432倍GTCLK周期的延迟0x19：应用2532倍GTCLK周期的延迟0x1A：应用2632倍GTCLK周期的延迟0x1B：应用2732倍GTCLK周期的延迟0x1C：应用2832倍GTCLK周期的延迟0x1D：应用2932倍GTCLK周期的延迟0x1E：应用3032倍GTCLK周期的延迟0x1F：应用3132倍GTCLK周期的延迟	R/W
15:5	—	这些位被读取为0。写入值应为0。	R/W

GTDLYRnA寄存器设置延迟应用于GTIOCnA引脚上输出信号的上升沿。关于设置传送的时间，请参阅第22.3.2节。GTDLYRnA、GTDLYRnB、GTDLYFnA和GTDLYFnB寄存器设置的传输时序。

当寄存器写保护被禁用（GPT32n.GTWP.WP=0）时，可以写入GTDLYRnA。

在更改GPT32n.GTWP.WP位的值后更改GTDLYRnA时，务必在更改GTDLYRnA的值之前读回GTWP寄存器的值。

22.2.4 GTDLYFnA : GTIOCnA Falling Output Delay Register (n = 0 to 3)

Base address: PDG = 0x4016_A000

Offset address: 0x028 + 0x4 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DLY[4:0]	GTIOCnA Output Falling Edge Delay Setting 0x00: Delay on falling edges is not applied 0x01: Delay of 1/32 times GTCLK period applied 0x02: Delay of 2/32 times GTCLK period applied 0x03: Delay of 3/32 times GTCLK period applied 0x04: Delay of 4/32 times GTCLK period applied 0x05: Delay of 5/32 times GTCLK period applied 0x06: Delay of 6/32 times GTCLK period applied 0x07: Delay of 7/32 times GTCLK period applied 0x08: Delay of 8/32 times GTCLK period applied 0x09: Delay of 9/32 times GTCLK period applied 0x0A: Delay of 10/32 times GTCLK period applied 0x0B: Delay of 11/32 times GTCLK period applied 0x0C: Delay of 12/32 times GTCLK period applied 0x0D: Delay of 13/32 times GTCLK period applied 0x0E: Delay of 14/32 times GTCLK period applied 0x0F: Delay of 15/32 times GTCLK period applied 0x10: Delay of 16/32 times GTCLK period applied 0x11: Delay of 17/32 times GTCLK period applied 0x12: Delay of 18/32 times GTCLK period applied 0x13: Delay of 19/32 times GTCLK period applied 0x14: Delay of 20/32 times GTCLK period applied 0x15: Delay of 21/32 times GTCLK period applied 0x16: Delay of 22/32 times GTCLK period applied 0x17: Delay of 23/32 times GTCLK period applied 0x18: Delay of 24/32 times GTCLK period applied 0x19: Delay of 25/32 times GTCLK period applied 0x1A: Delay of 26/32 times GTCLK period applied 0x1B: Delay of 27/32 times GTCLK period applied 0x1C: Delay of 28/32 times GTCLK period applied 0x1D: Delay of 29/32 times GTCLK period applied 0x1E: Delay of 30/32 times GTCLK period applied 0x1F: Delay of 31/32 times GTCLK period applied	R/W
15:5	—	These bits are read as 0. The write value should be 0.	R/W

The GTDLYFnA register sets a delay to be applied to falling edges of output signals on the GTIOCnA pin. On the timing for the transfer of settings, see section 22.3.2. Timing for Transfer of GTDLYRnA, GTDLYRnB, GTDLYFnA, and GTDLYFnB Register Settings.

GTDLYFnA can be written when register write protection is disabled (GPT32n.GTWP.WP = 0).

When changing GTDLYFnA after changing the value of GPT32n.GTWP.WP bit, be sure to read back the value of GTWP register before changing the value of GTDLYFnA.

22.2.4 GTDLYFnA:GTIOCnA下降输出延迟寄存器(n=0to3)

Base address: PDG = 0x4016_A000

Offset address: 0x028 + 0x4 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DLY[4:0]	GTIOCnA输出下降沿延迟设置 0x00：不应用下降沿延迟0x01：应用延迟132倍GTCLK周期0x02：应用延迟232倍GTCLK周期0x03：延迟3应用32倍GTCLK周期0x04：延迟4应用32倍GTCLK周期0x05:延迟532倍GTCLK周期0x06:延迟632倍GTCLK周期0x07:延迟732倍GTCLK周期0x08:延迟832倍GTCLK周期0x09:延迟932倍GTCLK周期0x0A:延迟1032倍GTCLK周期0x0B:延迟1132倍GTCLK周期0x0C:延迟1232倍GTCLK周期0x0D:延迟1332倍GTCLK周期0x0E:延迟1432倍GTCLK周期0x0F:延迟1532倍GTCLK周期0x10:延迟1632倍GTCLK周期0x11:延迟1732倍GTCLK周期0x12:延迟1832倍GTCLK周期0x13:延迟1932倍GTCLK周期0x14:延迟2032倍GTCLK周期应用0x15:应用2132倍GTCLK周期的延迟0x16：应用2232倍GTCLK周期的延迟0x17：应用2332倍GTCLK周期的延迟0x18：应用2432倍GTCLK周期的延迟0x19：应用2532倍GTCLK周期的延迟0x1A：应用2632倍GTCLK周期的延迟0x1B：应用2732倍GTCLK周期的延迟0x1C：应用2832倍GTCLK周期的延迟0x1D：应用2932倍GTCLK周期的延迟0x1E：应用3032倍GTCLK周期的延迟0x1F：应用3132倍GTCLK周期的延迟	R/W
15:5	—	这些位被读取为0。写入值应为0。	R/W

GTDLYFnA寄存器设置延迟应用于GTIOCnA引脚上输出信号的下降沿。关于设置传送的时间，请参阅第22.3.2节。GTDLYRnA、GTDLYRnB、GTDLYFnA和GTDLYFnB寄存器设置的传输时序。

当寄存器写保护被禁用（GPT32n.GTWP.WP=0）时，可以写入GTDLYFnA。

在更改GPT32n.GTWP.WP位的值后更改GTDLYFnA时，务必在更改GTDLYFnA的值之前读回GTWP寄存器的值。

22.2.5 GTDLYRnB : GTIOCnB Rising Output Delay Register (n = 0 to 3)

Base address: PDG = 0x4016_A000

Offset address: 0x01A + 0x4 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DLY[4:0]	GTIOCnB Output Rising Edge Delay Setting 0x00: Delay on rising edges is not applied 0x01: Delay of 1/32 times GTCLK period applied 0x02: Delay of 2/32 times GTCLK period applied 0x03: Delay of 3/32 times GTCLK period applied 0x04: Delay of 4/32 times GTCLK period applied 0x05: Delay of 5/32 times GTCLK period applied 0x06: Delay of 6/32 times GTCLK period applied 0x07: Delay of 7/32 times GTCLK period applied 0x08: Delay of 8/32 times GTCLK period applied 0x09: Delay of 9/32 times GTCLK period applied 0x0A: Delay of 10/32 times GTCLK period applied 0x0B: Delay of 11/32 times GTCLK period applied 0x0C: Delay of 12/32 times GTCLK period applied 0x0D: Delay of 13/32 times GTCLK period applied 0x0E: Delay of 14/32 times GTCLK period applied 0x0F: Delay of 15/32 times GTCLK period applied 0x10: Delay of 16/32 times GTCLK period applied 0x11: Delay of 17/32 times GTCLK period applied 0x12: Delay of 18/32 times GTCLK period applied 0x13: Delay of 19/32 times GTCLK period applied 0x14: Delay of 20/32 times GTCLK period applied 0x15: Delay of 21/32 times GTCLK period applied 0x16: Delay of 22/32 times GTCLK period applied 0x17: Delay of 23/32 times GTCLK period applied 0x18: Delay of 24/32 times GTCLK period applied 0x19: Delay of 25/32 times GTCLK period applied 0x1A: Delay of 26/32 times GTCLK period applied 0x1B: Delay of 27/32 times GTCLK period applied 0x1C: Delay of 28/32 times GTCLK period applied 0x1D: Delay of 29/32 times GTCLK period applied 0x1E: Delay of 30/32 times GTCLK period applied 0x1F: Delay of 31/32 times GTCLK period applied	R/W
15:5	—	These bits are read as 0. The write value should be 0.	R/W

The GTDLYRnB register sets a delay to be applied to rising edges of output signals on the GTIOCnB pin. On the timing for the transfer of settings, see section 22.3.2. Timing for Transfer of GTDLYRnA, GTDLYRnB, GTDLYFnA, and GTDLYFnB Register Settings.

GTDLYRnB can be written when register write protection is disabled (GPT32n.GTWP.WP = 0).

When changing GTDLYRnB after changing the value of GPT32n.GTWP.WP bit, be sure to read back the value of GTWP register before changing the value of GTDLYRnB.

22.2.5 GTDLYRnB:GTIOCnB上升沿输出延迟寄存器(n=0to3)

Base address: PDG = 0x4016_A000

Offset address: 0x01A + 0x4 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DLY[4:0]	GTIOCnB输出上升沿延迟设置 0x00：不应用上升沿延迟0x01：应用延迟132倍GTCLK周期0x02：应用延迟232倍GTCLK周期0x03：延迟3应用32倍GTCLK周期0x04：延迟4应用32倍GTCLK周期0x05:延迟532倍GTCLK周期0x06:延迟632倍GTCLK周期0x07:延迟732倍GTCLK周期0x08:延迟832倍GTCLK周期0x09:延迟932倍GTCLK周期0x0A:延迟1032倍GTCLK周期0x0B:延迟1132倍GTCLK周期0x0C:延迟1232倍GTCLK周期0x0D:延迟1332倍GTCLK周期0x0E:延迟1432倍GTCLK周期0x0F:延迟1532倍GTCLK周期0x10:延迟1632倍GTCLK周期0x11:延迟1732倍GTCLK周期0x12:延迟1832倍GTCLK周期0x13:延迟1932倍GTCLK周期0x14:延迟2032倍GTCLK周期应用0x15:应用2132倍GTCLK周期的延迟0x16：应用2232倍GTCLK周期的延迟0x17：应用2332倍GTCLK周期的延迟0x18：应用2432倍GTCLK周期的延迟0x19：应用2532倍GTCLK周期的延迟0x1A：应用2632倍GTCLK周期的延迟0x1B：应用2732倍GTCLK周期的延迟0x1C：应用2832倍GTCLK周期的延迟0x1D：应用2932倍GTCLK周期的延迟0x1E：应用3032倍GTCLK周期的延迟0x1F：应用3132倍GTCLK周期的延迟	R/W
15:5	—	这些位被读取为0。写入值应为0。	R/W

GTDLYRnB寄存器设置延迟应用于GTIOCnB引脚上输出信号的上升沿。关于设置传送的时间，请参阅第22.3.2节。GTDLYRnA、GTDLYRnB、GTDLYFnA和GTDLYFnB寄存器设置的传输时序。

当寄存器写保护被禁用（GPT32n.GTWP.WP=0）时，可以写入GTDLYRnB。

在更改GPT32n.GTWP.WP位的值后更改GTDLYRnB时，务必在更改GTDLYRnB的值之前读回GTWP寄存器的值。

22.2.6 GTDLYFnB : GTIOCnB Falling Output Delay Register (n = 0 to 3)

Base address: PDG = 0x4016_A000

Offset address: 0x02A + 0x4 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DLY[4:0]	GTIOCnB Output Falling Edge Delay Setting 0x00: Delay on falling edges is not applied 0x01: Delay of 1/32 times GTCLK period applied 0x02: Delay of 2/32 times GTCLK period applied 0x03: Delay of 3/32 times GTCLK period applied 0x04: Delay of 4/32 times GTCLK period applied 0x05: Delay of 5/32 times GTCLK period applied 0x06: Delay of 6/32 times GTCLK period applied 0x07: Delay of 7/32 times GTCLK period applied 0x08: Delay of 8/32 times GTCLK period applied 0x09: Delay of 9/32 times GTCLK period applied 0x0A: Delay of 10/32 times GTCLK period applied 0x0B: Delay of 11/32 times GTCLK period applied 0x0C: Delay of 12/32 times GTCLK period applied 0x0D: Delay of 13/32 times GTCLK period applied 0x0E: Delay of 14/32 times GTCLK period applied 0x0F: Delay of 15/32 times GTCLK period applied 0x10: Delay of 16/32 times GTCLK period applied 0x11: Delay of 17/32 times GTCLK period applied 0x12: Delay of 18/32 times GTCLK period applied 0x13: Delay of 19/32 times GTCLK period applied 0x14: Delay of 20/32 times GTCLK period applied 0x15: Delay of 21/32 times GTCLK period applied 0x16: Delay of 22/32 times GTCLK period applied 0x17: Delay of 23/32 times GTCLK period applied 0x18: Delay of 24/32 times GTCLK period applied 0x19: Delay of 25/32 times GTCLK period applied 0x1A: Delay of 26/32 times GTCLK period applied 0x1B: Delay of 27/32 times GTCLK period applied 0x1C: Delay of 28/32 times GTCLK period applied 0x1D: Delay of 29/32 times GTCLK period applied 0x1E: Delay of 30/32 times GTCLK period applied 0x1F: Delay of 31/32 times GTCLK period applied	R/W
15:5	—	These bits are read as 0. The write value should be 0.	R/W

The GTDLYFnB register sets a delay to be applied to falling edges of output signals on the GTIOCnB pin. On the timing for the transfer of settings, see section 22.3.2. Timing for Transfer of GTDLYRnA, GTDLYRnB, GTDLYFnA, and GTDLYFnB Register Settings.

GTDLYFnB can be written when register write protection is disabled (GPT32n.GTWP.WP = 0).

When changing GTDLYFnB after changing the value of GPT32n.GTWP.WP bit, be sure to read back the value of GTWP register before changing the value of GTDLYFnB.

22.3 Operation

22.3.1 Adjustments to the Timing of Rising and Falling Edges in PWM Waveforms

The timing of rising and falling edges in PWM waveforms which are output from the GTIOCnA and GTIOCnB pins, where n = channel number, can be delayed to an accuracy of 1/32 of the GPT core clock (GTCLK) period.

If the timing of rising or falling edges in PWM waveforms output from the GTIOCnA and GTIOCnB pins must be adjusted, initialize the PWM generation circuit as shown in the procedure in Figure 22.2.

22.2.6 GTDLYFnB:GTIOCnB下降输出延迟寄存器(n=0to3)

Base address: PDG = 0x4016_A000

Offset address: 0x02A + 0x4 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DLY[4:0]	GTIOCnB输出下降沿延迟设置 0x00：不应用下降沿延迟0x01：应用延迟132倍GTCLK周期0x02：应用延迟232倍GTCLK周期0x03：延迟3应用32倍GTCLK周期0x04：延迟4应用32倍GTCLK周期0x05:延迟532倍GTCLK周期0x06:延迟632倍GTCLK周期0x07:延迟732倍GTCLK周期0x08:延迟832倍GTCLK周期0x09:延迟932倍GTCLK周期0x0A:延迟1032倍GTCLK周期0x0B:延迟1132倍GTCLK周期0x0C:延迟1232倍GTCLK周期0x0D:延迟1332倍GTCLK周期0x0E:延迟1432倍GTCLK周期0x0F:延迟1532倍GTCLK周期0x10:延迟1632倍GTCLK周期0x11:延迟1732倍GTCLK周期0x12:延迟1832倍GTCLK周期0x13:延迟1932倍GTCLK周期0x14:延迟2032倍GTCLK周期应用0x15:应用2132倍GTCLK周期的延迟0x16：应用2232倍GTCLK周期的延迟0x17：应用2332倍GTCLK周期的延迟0x18：应用2432倍GTCLK周期的延迟0x19：应用2532倍GTCLK周期的延迟0x1A：应用2632倍GTCLK周期的延迟0x1B：应用2732倍GTCLK周期的延迟0x1C：应用2832倍GTCLK周期的延迟0x1D：应用2932倍GTCLK周期的延迟0x1E：应用3032倍GTCLK周期的延迟0x1F：应用3132倍GTCLK周期的延迟	R/W
15:5	—	这些位被读取为0。写入值应为0。	R/W

GTDLYFnB寄存器设置延迟应用于GTIOCnB引脚上输出信号的下降沿。关于设置传送的时间，请参阅第22.3.2节。GTDLYRnA、GTDLYRnB、GTDLYFnA和GTDLYFnB寄存器设置的传输时序。

当寄存器写保护被禁用（GPT32n.GTWP.WP=0）时，可以写入GTDLYFnB。

在更改GPT32n.GTWP.WP位的值后更改GTDLYFnB时，请务必在更改GTDLYFnB的值之前回读GTWP寄存器的值。

22.3 Operation

22.3.1 PWM波形上升沿和下降沿时序的调整

从GTIOCnA和GTIOCnB引脚输出的PWM波形的上升沿和下降沿时序（其中n=通道数）可以延迟到GPT内核时钟(GTCLK)周期的1×32的精度。

如果必须调整GTIOCnA和GTIOCnB引脚输出的PWM波形的上升沿或下降沿时序，请按照图22.2中的步骤初始化PWM生成电路。

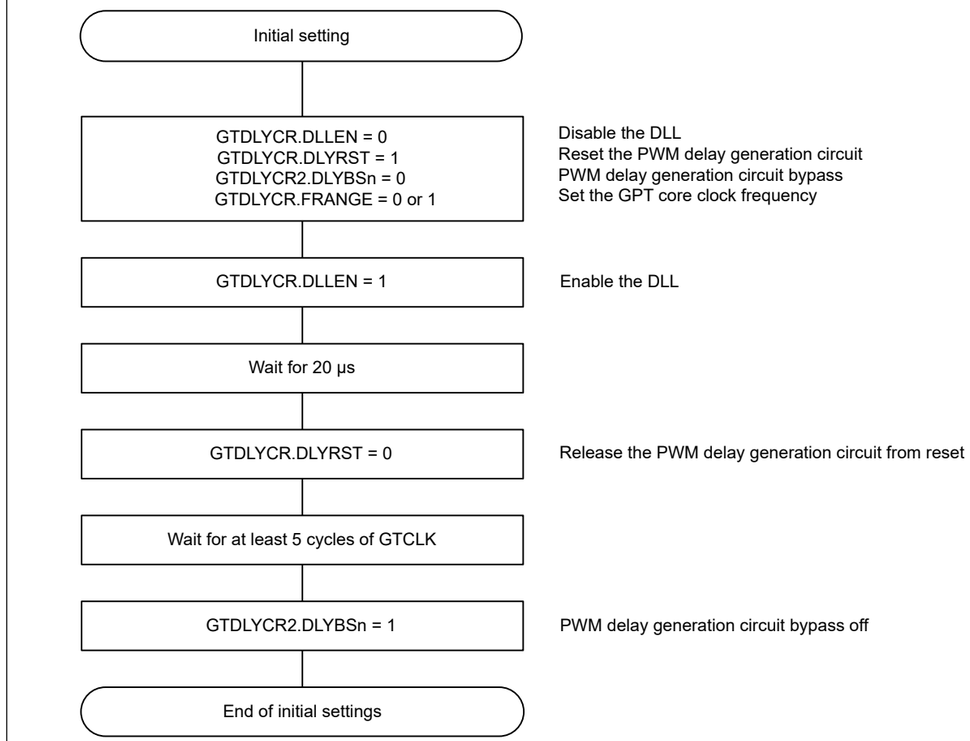


Figure 22.2 Example of initialization flow for the PWM delay generation circuit

In the PWM delay generation circuit, delay can be applied to rising and falling edges of the PWM output to an accuracy of 1/32 of the period of the GPT core clock (GTCLK). This is described in section 21.3.3. PWM Output Operating Mode. Delays associated with the settings are reflected in the PWM output with the timing described in section 22.3.2. Timing for Transfer of GTDLYRnA, GTDLYRnB, GTDLYFnA, and GTDLYFnB Register Settings. Table 22.3 shows the association between the GTDLYRnA, GTDLYRnB, GTDLYFnA, and GTDLYFnB registers and the PWM outputs.

Table 22.3 Association between PWM output pins and delay setting registers

PWM output pin	Rising-edge delay setting register	Falling-edge delay setting register
GTIOC0A	GTDLYR0A	GTDLYF0A
GTIOC0B	GTDLYR0B	GTDLYF0B
GTIOC1A	GTDLYR1A	GTDLYF1A
GTIOC1B	GTDLYR1B	GTDLYF1B
GTIOC2A	GTDLYR2A	GTDLYF2A
GTIOC2B	GTDLYR2B	GTDLYF2B
GTIOC3A	GTDLYR3A	GTDLYF3A
GTIOC3B	GTDLYR3B	GTDLYF3B

When the PWM delay generation circuit is in use, the timing with which a PWM output signal rises and falls can be controlled to an accuracy of 1/32 of the period of the GPT core clock (GTCLK). When this option is not in use, the period of the PWM output waveform is controlled to an accuracy of one period of the input clock for the timer counter, which is GTCLK. With the PWM delay generation circuit, the output can be controlled to an accuracy 32 times better. Additionally,

Figure 22.2 PWM延迟产生电路的初始化流程示例

在PWM延迟生成电路中，可以将延迟应用于PWM输出的上升沿和下降沿，精度为GPT内核时钟(GTCLK)周期的1 32。这在第21.3.3节中进行了描述。PWM输出工作模式。与设置相关的延迟反映在PWM输出中，时序在第22.3. 2节中描述。GTDLYRnA、GTDLYRnB、GTDLYFnA和GTDLYFnB寄存器设置的传输时序。表22.3显示了GTDLYRnA 、GTDLYRnB、GTDLYFnA和GTDLYFnB寄存器与PWM输出之间的关联。

Table 22.3 PWM输出引脚和延迟设置寄存器之间的关联

PWM输出引脚	上升沿延迟设置寄存器	下降沿延迟设置寄存器
GTIOC0A	GTDLYR0A	GTDLYF0A
GTIOC0B	GTDLYR0B	GTDLYF0B
GTIOC1A	GTDLYR1A	GTDLYF1A
GTIOC1B	GTDLYR1B	GTDLYF1B
GTIOC2A	GTDLYR2A	GTDLYF2A
GTIOC2B	GTDLYR2B	GTDLYF2B
GTIOC3A	GTDLYR3A	GTDLYF3A
GTIOC3B	GTDLYR3B	GTDLYF3B

当使用PWM延迟产生电路时，PWM输出信号上升和下降的时序可以控制在GPT内核时钟(GTCLK)周期的1×32精度。不使用此选项时，PWM输出波形的周期被控制为定时器计数器输入时钟的一个周期的精度，即GTCLK。使用PWM延迟产生电路，可以将输出控制精度提高32倍。此外，

the delay settings also control the periods at high and low level for the PWM waveform to the given accuracy. PWM delay generation circuit channels can be individually enabled or disabled.

22.3.2 Timing for Transfer of GTDLYRnA, GTDLYRnB, GTDLYFnA, and GTDLYFnB Register Settings

Settings for the GTDLYRnA, GTDLYRnB, GTDLYFnA, and GTDLYFnB registers are initially transferred to temporary registers, and then reflected in the delay on the GTIOCnA and GTIOCnB (n = 0 to 3) outputs. Transfer of the settings takes place on overflows (in up-counting) or underflows (in down-counting) for saw waves, and in the troughs of triangle waves.

Figure 22.3 and Figure 22.4 show examples of the operation of the GTDLYR0A and GTDLYF0A registers.

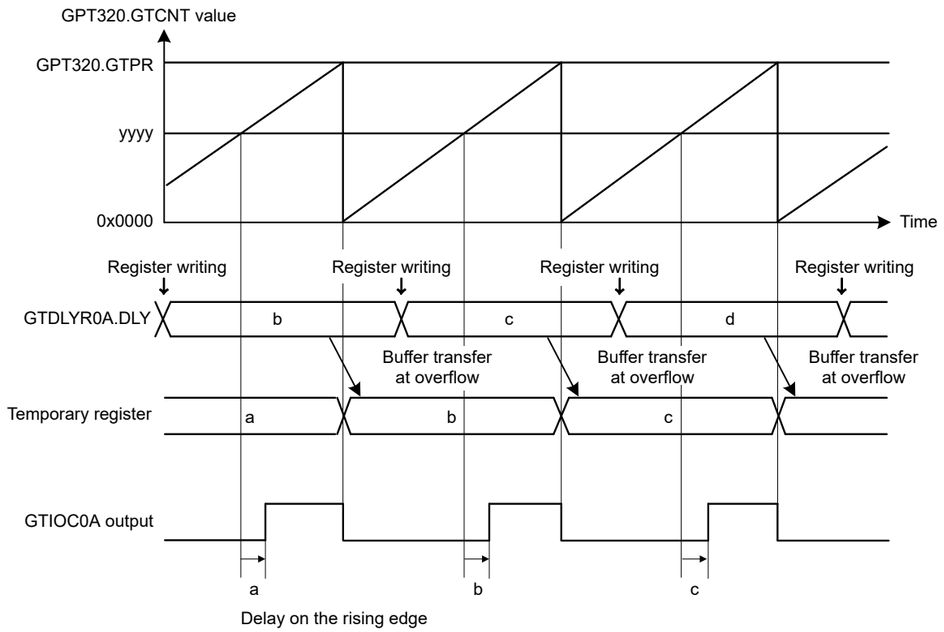


Figure 22.3 Example of GTDLYR0A register operation with PWM saw-wave generation

延迟设置还控制PWM波形的高电平和低电平周期，以达到给定的精度。PWM延迟生成电路通道可以单独启用或禁用。

22.3.2 GTDLYRnA、GTDLYRnB、GTDLYFnA和GTDLYFnB的传输时间注册设置

GTDLYRnA、GTDLYRnB、GTDLYFnA和GTDLYFnB寄存器的设置最初传送到临时寄存器，然后反映在GTIOCnA和GTIOCnB（n=0到3）输出的延迟中。设置的传输发生在锯齿波的上溢（向上计数）或下溢（向下计数）以及三角波的波谷中。

图22.3和图22.4显示了GTDLYR0A和GTDLYF0A寄存器的操作示例。

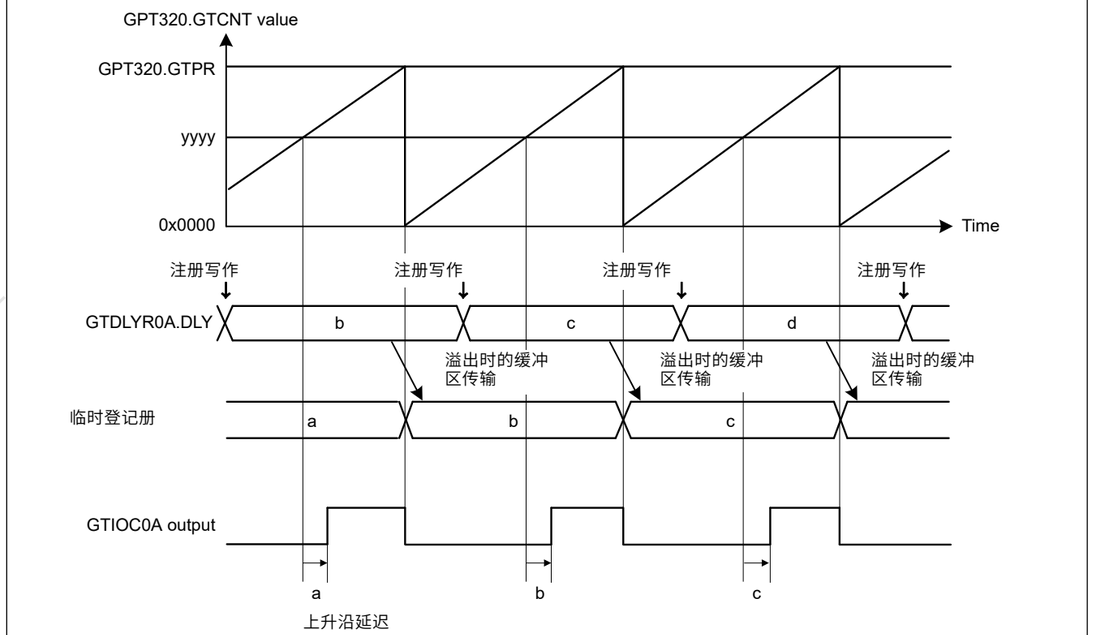


Figure 22.3 GTDLYR0A寄存器操作示例，带PWM锯齿波生成

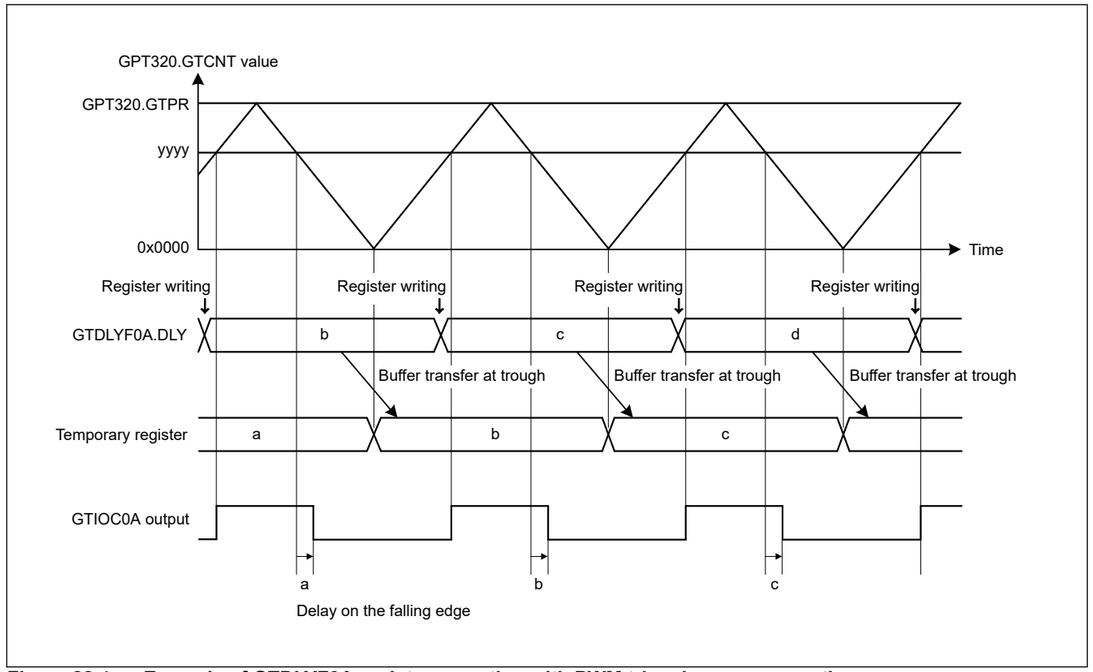


Figure 22.4 Example of GTDLYF0A register operation with PWM triangle-wave generation

22.4 Usage Notes

22.4.1 Settings for the Module-Stop Function

The Module Stop Control Register D (MSTPCRD) can enable or disable operation of the PWM delay generation circuit. The PWM delay generation circuit is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

22.4.2 Notes on Delay Settings for PWM Delay Generation Circuit

When the PWM delay generation circuit generates delays for a PWM output waveform and the waveform is toggled in response to compare-matches, do not change the settings for delay while the compare-match value is within the ranges listed in Table 22.4. This constraint applies to the GTDLYFnA, GTDLYRnA, GTDLYFnB, and GTDLYRnB registers.

Table 22.4 Constraints on delay settings

Mode	Direction of counting	Compare-match value
Saw-wave mode	Up	GTPR - 2 or above
	Down	2 or below
Triangle-wave mode	Down	2 or below

Figure 22.5 shows an example of how the constraints apply to the timing of setting GTDLYFnA in saw-wave waveform one-shot pulse mode (counting up). Do not change the value set in GTDLYFnA while GTCCRD ≥ GTPR - 2.

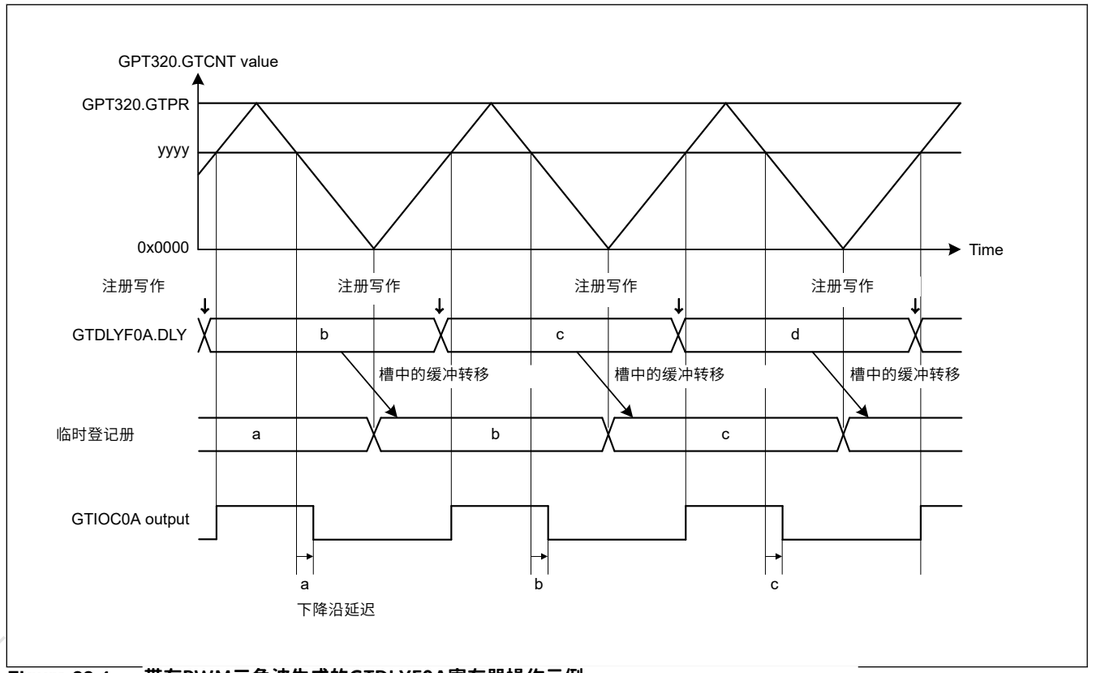


Figure 22.4 带有PWM三角波生成的GTDLYF0A寄存器操作示例

22.4 使用说明

22.4.1 模块停止功能的设置

模块停止控制寄存器D(MSTPCRD)可以启用或禁用PWM延迟生成电路的操作。
PWM延迟产生电路在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

22.4.2 PWM延迟产生电路的延迟设置注意事项

当PWM延迟生成电路为PWM输出波形产生延迟并且波形响应比较匹配而切换时，当比较匹配值在表22.4中列出的范围内时，请勿更改延迟设置。此约束适用于GTDLYFnA、GTDLYRnA、GTDLYFnB和GTDLYRnB寄存器。

Table 22.4 延迟设置的限制

Mode	计数方向	Compare-match value
Saw-wave mode	Up	GTPR2或以上
	Down	2或以下
Triangle-wave mode	Down	2或以下

图22.5显示了约束如何应用于在锯波波形单次脉冲模式（向上计数）中设置GTDLYFnA的时序的示例。当GTCCRD≥GTPR2时，请勿更改GTDLYFnA中设置的值。

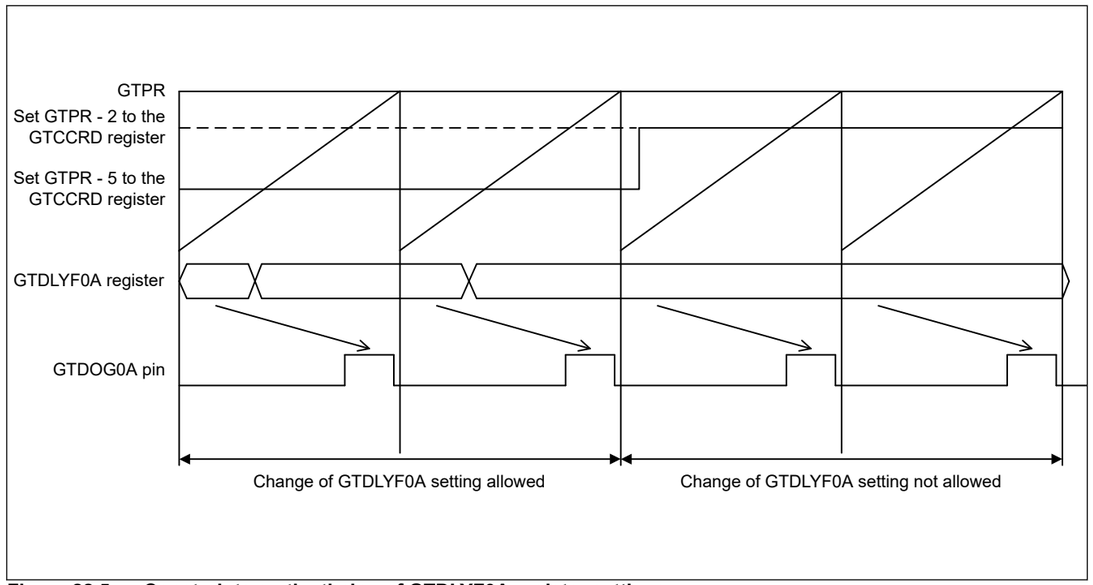


Figure 22.5 Constraints on the timing of GTDLYF0A register settings

Changing the values in the GTDLYFnA, GTDLYRnA, GTDLYFnB, and GTDLYRnB registers during periods where changes to settings are not allowed, might lead to faulty output waveforms such as shifts in the timing of output waveform transitions from the expected values.

22.4.3 Register Write Interval

When GPT core clock is GPTCLK, the writing value may not be reflected if the interval between writing to the GTDLYRnA/GTDLYFnA/GTDLYRnB/GTDLYFnA register is shorter than the following interval time. This restriction only applies to successive writes to the same register.

Write_Interval [ns] = Period_of_PCLKA [ns] × 6 + Period_of_GPTCLK [ns] × 4

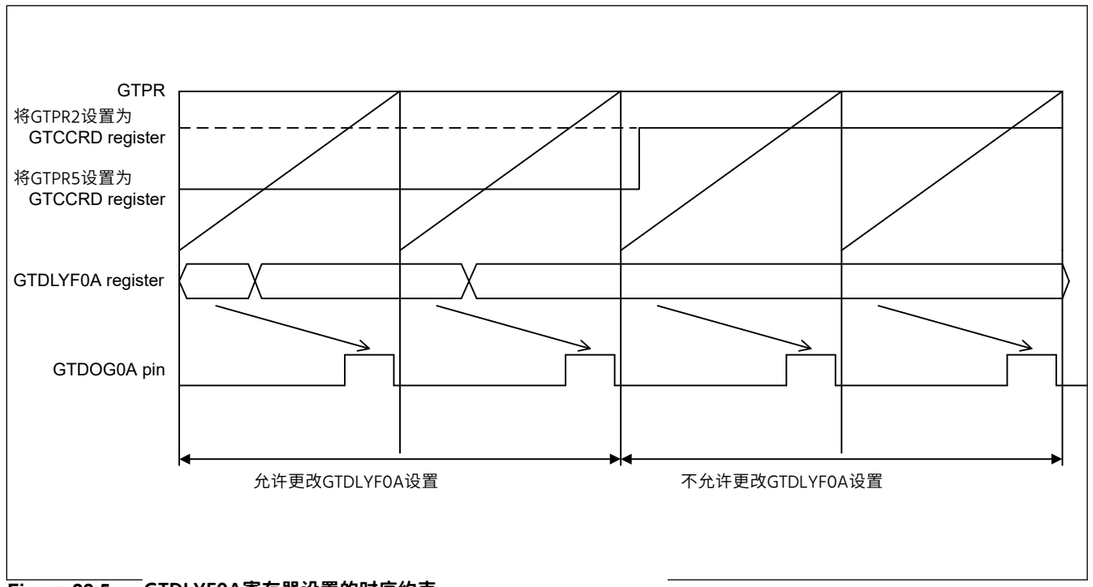


Figure 22.5 GTDLYF0A寄存器设置的时序约束

在不允许更改设置的期间更改GTDLYFnA、GTDLYRnA、GTDLYFnB和GTDLYRnB寄存器中的值可能会导致错误的输出波形，例如输出波形转换的时序偏离预期值。

22.4.3 寄存器写入间隔

当GPT内核时钟为GPTCLK时，如果写入到GTDLYRnAGTDLYFnAGTDLYRnBGTDLYFnA寄存器比以下间隔时间短。此限制仅适用于对同一寄存器的连续写入。

Write_Interval [ns] = Period_of_PCLKA [ns] × 6 + Period_of_GPTCLK [ns] × 4

23. Low Power Asynchronous General Purpose Timer (AGTW)

This is the AGTW_B version of the AGTW peripheral module.

AGTW_B is referred to as AGTW in this chapter.

23.1 Overview

The low power Asynchronous General Purpose Timer (AGT) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.

Table 23.1 lists the AGTW specifications, Figure 23.1 shows a block diagram, and Table 23.2 lists the I/O pins.

Table 23.1 AGTW specifications

Parameter		Description
Operating modes	Timer mode	The count source is counted
	Pulse output mode	The count source is counted and the output is inverted at each timer underflow
	Event counter mode	An external event is counted
	Pulse width measurement mode	An external pulse width is measured
	Pulse period measurement mode	An external pulse period is measured
Number of Channels		32 bits × 2 channels (AGTWn (n = 0, 1))
Count source (operating clock)*2	Timer mode	PCLKB, PCLKB/2, PCLKB/8, AGTLCLK/d (d = 1, 2, 4, 8, 16, 32, 64, or 128), or underflow signal of AGTW0 selectable.*1
	Pulse output mode	
	Pulse width measurement mode	
	Pulse period measurement mode	
	Event counting mode	External event input
Interrupt and Event Link function		• Underflow event signal or measurement complete event signal – When the counter underflows – When the measurement of the active width of the external input pin (AGTWIOn) completes in pulse width measurement mode – When the set edge of the external input pin (AGTWIOn) is input in pulse period measurement mode. • Compare match A event signal – When the values of AGT register and AGTCMA register matched (compare match A function enabled). • Compare match B event signal – When the values of AGT and AGTCMB registers matched (compare match B function enabled). • Return from Snooze mode or Software Standby mode can be performed with AGT1_AGTI, AGT1_AGTCMAI, or AGT1_AGTCMBI*3
Selectable functions		• Compare match function One or two of the AGT Compare Match A register and AGT Compare Match B register is selectable.
TrustZone Filter		Security attribution can be set for each channels

Note 1. AGTW0 cannot use underflow signal. AGTW1 connects directly with the underflow event signal from the AGTW0 timer.
Note 2. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ the frequency of the count source clock.
Note 3. In details, see section 10, Low Power Modes.

23. 低功耗异步通用定时器(AGTW)

这是AGTW外设模块的AGTW_B版本。

AGTW_B在本章中称为AGTW。

23.1 Overview

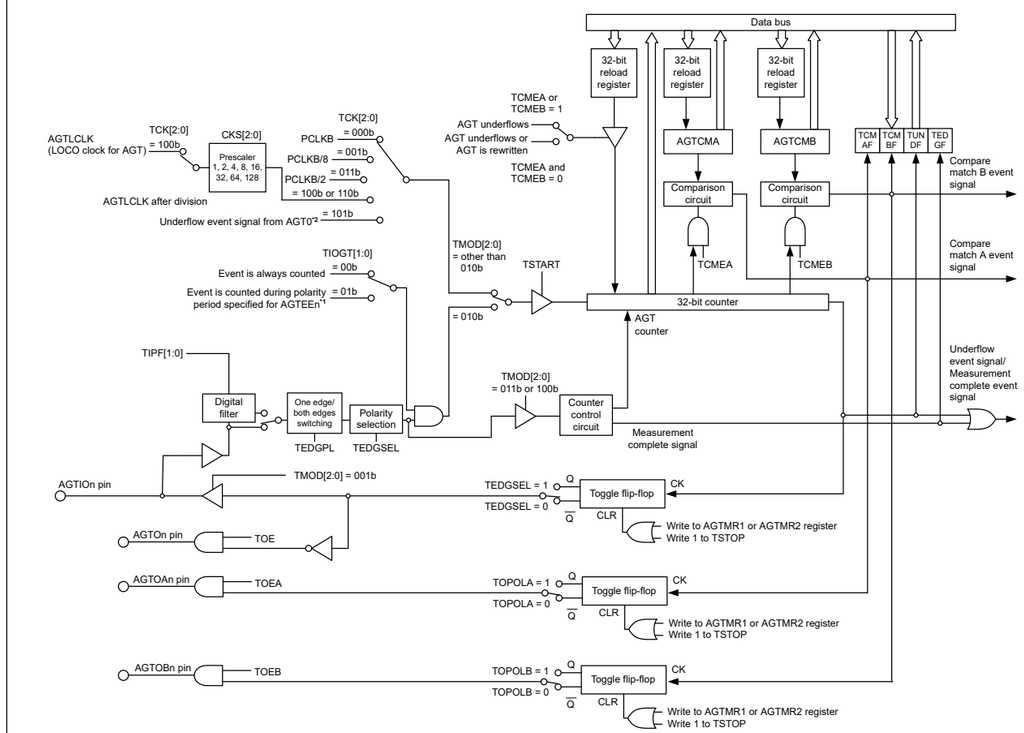
低功耗异步通用定时器(AGT)是一个32位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。该定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配到同一个地址，可以通过AGT寄存器访问。

表23.1列出了AGTW规范，图23.1显示了框图，表23.2列出了IO引脚。

Table 23.1 AGTW specifications

Parameter		Description
操作模式	定时器模式	计数源被计数
	脉冲输出方式	计数源被计数并在每次定时器下溢时反转输出
	事件计数器模式	计算外部事件
	脉宽测量模式	测量外部脉冲宽度
	脉冲周期测量模式	测量外部脉冲周　　期
通道数		32位×2通道(AGTWn(n=0 1))
计数源（工作时钟）*2	定时器模式	PCLKB、PCLKB2、PCLKB8、AGTLCLKd（d=1、2、4、8、16、32、64或128）或AGTW0的下溢信号可选。*1
	脉冲输出方式	
	脉宽测量模式	
	脉冲周期测量模式	
	事件计数模式	外部事件输入
中断和事件链接功能		• 下溢事件信号或测量完成事件信号 – 当计数器下溢时 – 在脉冲宽度测量模式下，外部输入引脚(AGTWION)的有效宽度测量完成时 – 在脉冲周期测量模式下输入外部输入引脚(AGTWION)的设置边沿时。 • 比较匹配A事件信号 – 当AGT寄存器和AGTCMA寄存器的值匹配时（比较匹配A功能启用）。 • 比较匹配B事件信号 – 当AGT和AGTCMB寄存器的值匹配时（比较匹配B功能启用）。 • 从贪睡模式或软件待机模式返回可以通过AGT1_AGTI, AGT1_AGTCMAI, or AGT1_AGTCMBI*3
可选择的功能		• 比较匹配功能AGT比较匹配A寄存器和AGT比较匹配中的一个或两个B寄存器是可选的。
TrustZone Filter		可以为每个通道设置安全属性

注1.AGTW0不能使用下溢信号。AGTW1直接连接来自AGTW0定时器的下溢事件信号。
注2.满足外设模块时钟（PCLKB）的频率≥计数源时钟的频率。
注3.详细信息请参见第10节，低功耗模式。



Note 1. The polarity can be selected by the EEPS bit in the AGTISR register.
Note 2. AGTW0 cannot use AGTW0 underflow event. AGTW1 uses the underflow of AGTW0.

Figure 23.1 AGTW block diagram

Table 23.2 AGTW I/O pins

Pin name	I/O	Function
AGTEEn	Input	External event input enable for AGTW
AGTIOn	Input/output	External event input and pulse output for AGTW
AGTOn	Output	Pulse output for AGTW
AGTOAn	Output	Compare match A output for AGTW
AGTOBn	Output	Compare match B output for AGTW

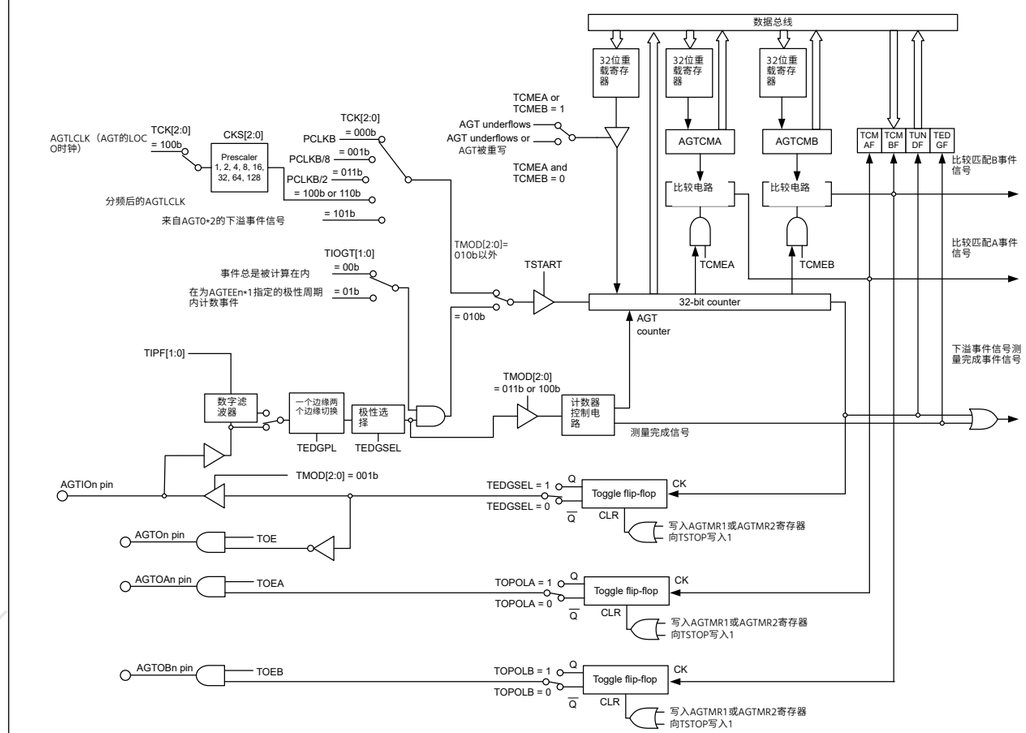
Note: Channel number: n = 0, 1

23.2 Register Descriptions

23.2.1 AGT : AGT Counter Register

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)
Offset address: 0x00

Bit position:	31																												0
Bit field:																													
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1



注1.可以通过AGTISR寄存器中的EEPS位选择极性。
注2.AGTW0不能使用AGTW0下溢事件。AGTW1使用AGTW0的下溢。

Figure 23.1 AGTW框图

Table 23.2 AGTW I/O pins

引脚名称	I/O	Function
AGTEEn	Input	AGTW的外部事件输入使能
AGTIOn	Input/output	AGTW的外部事件输入和脉冲输出
AGTOn	Output	AGTW的脉冲输出
AGTOAn	Output	比较AGTW的匹配A输出
AGTOBn	Output	比较AGTW的匹配B输出

Note: Channel number: n = 0, 1

23.2 注册说明

23.2.1 AGT:AGT计数器寄存器

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)
Offset address: 0x00

Bit position:	31																												0
Bit field:																													
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	32-bit counter and reload register Setting range : 0x00000000 to 0xFFFFFFFF	R/W

AGTWn.AGT is a 32-bit register. The write value is written to the reload register and the read value is read from the counter.

The states of the reload register and the counter change according to the TSTART bit in the AGTCR register and TCMEA/TCMEB bit in the AGTCMSR register. For details, see section 23.3.1. Reload Register and Counter Rewrite Operation.

When 1 is written to the TSTOP bit in the AGTCR register, AGT counter is forcibly stopped and set to 0xFFFFFFFF.

When the TCK[2:0] bits setting in the AGTMR1 register are a value other than 001b (PCLKB/8) or 011b (PCLKB/2), if the AGT register is set to 0x00000000, a request signal to the ICU, the DTC, the DMAC, and the ELC is generated once immediately after the count starts. The and AGTWOn, AGTWIOn pin output are toggled.

When the AGT register is set to 0x00000000 in event counter mode, regardless of the value of TCK[2:0] bits, a request signal to the ICU, the DTC, the DMAC, and the ELC is generated once immediately after the count starts.

In addition, the AGTWOn pin output is toggled even during a period other than the specified count period. When the AGT register is set to 0x00000001 or more, a request signal is generated each time AGT underflows.

23.2.2 AGTCMA : AGT Compare Match A Register

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x04

Bit position: 31 … 0

Bit field:

Value after reset: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bit	Symbol	Function	R/W
31:0	n/a	32-bit compare match A data is stored.*1 Setting range : 0x00000000 to 0xFFFFFFFF	R/W

Note 1. Set the AGTCMA register to 0xFFFFFFFF when compare match A is not used.

The AGTCMA register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and compare register A change according to the TSTART bit in the AGTCR register. For details, see section 23.3.2. Reload Register and AGT Compare Match A/B Register Rewrite Operation.

23.2.3 AGTCMB : AGT Compare Match B Register

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x08

Bit position: 31 … 0

Bit field:

Value after reset: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bit	Symbol	Function	R/W
31:0	n/a	32-bit compare match B data is stored.*1 Setting range : 0x00000000 to 0xFFFFFFFF	R/W

Note 1. Set the AGTCMB register to 0xFFFFFFFF when compare match B is not used.

The AGTCMB register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and compare register B change according to the TSTART bit in the AGTCR register. For details, see section 23.3.2. Reload Register and AGT Compare Match A/B Register Rewrite Operation.

Bit	Symbol	Function	R/W
31:0	n/a	32位计数器和重载寄存器设置范围：0x0000 0000到0xFFFFFFFF	R/W

AGTWn.AGT是一个32位寄存器。写入值写入重载寄存器，读取值从计数器中读取。

重载寄存器和计数器的状态根据AGTCR寄存器和TCMEA中的TSTART位改变
AGTCMSR寄存器中的TCMEB位。详见23.3.1节。重载寄存器和计数器重写操作。

当AGTCR寄存器的TSTOP位写入1时，AGT计数器被强制停止并设置为0xFFFFFFFF。

当AGTMR1寄存器中的TCK[2:0]位设置为001b(PCLKB8)或011b(PCLKB2)以外的值时，如果AGT寄存器设置为0x00000000，计数开始后立即生成一次对ICU、DTC、DMAC和ELC的请求信号。和AGTWOn、AGTWOn引脚输出被切换。

当AGT寄存器在事件计数器模式下设置为0x00000000时，无论TCK[2:0]位的值如何，都会在计数开始后立即生成一次对ICU、DTC、DMAC和ELC的请求信号.

此外，即使在指定计数周期以外的周期内，AGTWOn引脚输出也会切换。当AGT寄存器设置为0x00000001或更大时，每次AGT下溢时都会产生一个请求信号。

23.2.2 AGTCMA:AGT比较匹配A寄存器

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x04

Bit position: 31 … 0

Bit field:

重置后的值: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bit	Symbol	Function	R/W
31:0	n/a	存储32位比较匹配A数据。*1 设置范围：0x00000000至0xFFFFFFFF	R/W

注1.不使用比较匹配A时，将AGTCMA寄存器设置为0xFFFFFFFF。

AGTCMA寄存器是一个读写寄存器，用于设置与AGT计数器比较匹配的值。重载寄存器和比较寄存器A的状态根据AGTCR寄存器中的TSTART位而改变。详见23.3.2节。重载寄存器和AGT比较匹配AB寄存器重写操作。

23.2.3 AGTCMB:AGT比较匹配B寄存器

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x08

Bit position: 31 … 0

Bit field:

重置后的值: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bit	Symbol	Function	R/W
31:0	n/a	存储32位比较匹配B数据。*1 设置范围：0x00000000至0xFFFFFFFF	R/W

注1.不使用比较匹配B时，将AGTCMB寄存器设置为0xFFFFFFFF。

AGTCMB寄存器是一个读写寄存器，用于设置与AGT计数器比较匹配的值。重载寄存器和比较寄存器B的状态根据AGTCR寄存器中的TSTART位而改变。详见23.3.2节。重载寄存器和AGT比较匹配AB寄存器重写操作。

23.2.4 AGTCR : AGT Control Register

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TCMBF	TCMAF	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSTART	AGT Count Start*2 0: Count stops 1: Count starts	R/W
1	TCSTF	AGT Count Status Flag*2 0: Count stopped 1: Count in progress	R
2	TSTOP	AGT Count Forced Stop*1 0: Writing is invalid 1: The count is forcibly stopped	W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	TEDGF	Active Edge Judgment Flag 0: No active edge received 1: Active edge received	R/(W)*3
5	TUNDF	Underflow Flag 0: No underflow 1: Underflow	R/(W)*3
6	TCMAF	Compare Match A Flag 0: No match 1: Match	R/(W)*3
7	TCMBF	Compare Match B Flag 0: No match 1: Match	R/(W)*3

Note 1. When 1 (count is forcibly stopped) is written to the TSTOP bit, the TSTART bit and TCSTF flag are initialized at the same time. The pulse output level is also initialized. The read value is 0.
Note 2. For information on using the TSTART bit and TCSTF flag, see section 23.4.1. Count Operation Start and Stop Control.
Note 3. Only 0 can be written to clear the flag.

TSTART bit (AGT Count Start)

The count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When the TSTART bit is set to 1 (count starts), the TCSTF flag is set to 1 (count in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF flag is set to 0 (count stops) in synchronization with the count source. For details, see section 23.4.1. Count Operation Start and Stop Control.

TCSTF flag (AGT Count Status Flag)

The TCSTF flag indicates the AGT count status.

[Setting condition]

- When 1 is written to the TSTART bit (the TCSTF flag is set to 1 in synchronization with the count source).

[Clearing conditions]

- When 0 is written to the TSTART bit (the TCSTF flag is set to 0 in synchronization with the count source)
- When 1 is written to the TSTOP bit.

TSTOP bit (AGT Count Forced Stop)

When 1 is written to the TSTOP bit, the count is forcibly stopped. The read value is 0.

23.2.4 AGTCR:AGT控制寄存器

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TCMBF	TCMAF	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSTART	AGT计数开始*2 0：计数停止1 ：计数开始	R/W
1	TCSTF	AGT计数状态标志*2 0：计数停止1：计数中	R
2	TSTOP	AGTCount强制停止*1 0：写入无效1：强制停止计数	W
3	—	该位读取为0。写入值应为0。	R/W
4	TEDGF	主动边缘判断标志 0：未收到有效边沿1：收到有效边沿	R/(W)*3
5	TUNDF	Underflow Flag 0: No underflow 1: Underflow	R/(W)*3
6	TCMAF	比较匹配标志 0：不匹配1 ：匹配	R/(W)*3
7	TCMBF	比较匹配B标志 0：不匹配1 ：匹配	R/(W)*3

注1.当1（强制停止计数）写入TSTOP位时，TSTART位和TCSTF标志同时初始化。脉冲输出电平也被初始化。读取值为0。

注2.有关使用TSTART位和TCSTF标志的信息，请参阅第23.4.1节。计数操作启动和停止控制。
注3.只能写入0来清除标志。

TSTART位（AGT计数开始）

通过向TSTART位写入1开始计数操作，通过写入0停止计数操作。当TSTART位设置为1（计数开始）时，TCSTF标志设置为1（计数进行中）与计数源同步。此外，在TSTART位写入0后，TCSTF标志与计数源同步设置为0（计数停止）。详见23.4.1节。计数操作启动和停止控制。

TCSTF标志（AGT计数状态标志）

TCSTF标志指示AGT计数状态。

[Setting condition]

●当TSTART位写入1时（TCSTF标志设置为1，与计数源同步）。

[Clearing conditions]

●TSTART位写入0时（TCSTF标志设置为0与计数源同步）

●TSTOP位写入1时。

TSTOP位（AGT计数强制停止）

向TSTOP位写入1时，强制停止计数。读取值为0。

TEDGF flag (Active Edge Judgment Flag)

The TEDGF flag indicates that an active edge was detected.

[Setting condition]

- When the measurement of the active width of the external input pin (AGTWIOn) is complete in pulse width measurement mode
- When the set edge of the external input pin (AGTWIOn) is input in pulse period measurement mode.

[Clearing condition]

- When 0 is written to this flag by software.

TUNDF flag (Underflow Flag)

The TUNDF flag indicates that the counter underflowed.

[Setting condition]

- When the counter underflows.

[Clearing condition]

- When 0 is written to this flag by software.

TCMAF flag (Compare Match A Flag)

The TCMAF flag indicates that compare match A was detected.

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMA register.

[Clearing condition]

- When 0 is written to this flag by software.

TCMBF flag (Compare Match B Flag)

The TCMBF flag indicates that compare match B was detected.

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMB register.

[Clearing condition]

- When 0 is written to this flag by software.

23.2.5 AGTMR1 : AGT Mode Register 1

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TCK[2:0]			TEDGPL	TMOD[2:0]		
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	TMOD[2:0]	Operating Mode*3 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode Others: Setting prohibited	R/W

TEDGF标志（活动边缘判断标志）

TEDGF标志表示检测到有效边沿。

[Setting condition]

●在脉冲宽度测量模式下，外部输入引脚(AGTWION)的有效宽度测量完成时

●在脉冲周期测量模式下输入外部输入引脚(AGTWION)的设置边沿时。

[Clearing condition]

●当软件向该标志写入0时。

TUNDF flag (Underflow Flag)

TUNDF标志指示计数器下溢。

[Setting condition]

●当计数器下溢时。

[Clearing condition]

●当软件向该标志写入0时。

TCMAF标志（比较匹配A标志）

TCMAF标志表示检测到比较匹配A。

[Setting condition]

●当AGT寄存器中的值与AGTCMA寄存器中的值匹配时。

[Clearing condition]

●当软件向该标志写入0时。

TCMBF标志（比较匹配B标志）

TCMBF标志表示检测到比较匹配B。

[Setting condition]

●当AGT寄存器中的值与AGTCMB寄存器中的值匹配时。

[Clearing condition]

●当软件向该标志写入0时。

23.2.5 AGTMR1：AGT模式寄存器1

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TCK[2:0]			TEDGPL	TMOD[2:0]		
重置后的值：	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	TMOD[2:0]	操作模式*3 000：定时器模式001：脉冲输出模式01 0：事件计数器模式011：脉冲宽度测量 模式100：脉冲周期测量模式 其他：禁止设置	R/W

Bit	Symbol	Function	R/W
3	TEDGPL	Edge Polarity*4 0: Single-edge 1: Both-edge	R/W
6:4	TCK[2:0]	Count Source*1 *2 *5 *7 0 0 0: PCLKB 0 0 1: PCLKB/8 0 1 1: PCLKB/2 1 0 0: Divided clock AGTLCLK specified by CKS[2:0] bits in the AGTMR2 register 1 0 1: Underflow event signal from AGTW0*6 1 1 0: Setting prohibited Others: Setting prohibited	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Note: Write access to the AGTMR1 register initializes the output from the AGTWOn, AGTWIOn, AGTWOAn, and AGTWOBn pins. For details on the output level at initialization, see section 23.2.7. AGTIOC : AGT I/O Control Register.
Note 1. When event counter mode is selected, the external input pin (AGTWIOn) is selected as the count source regardless of the setting of TCK[2:0] bits.
Note 2. Do not switch count sources during count operation. Only switch count sources when both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count stops).
Note 3. The operating mode can only be changed when the count is stopped while both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count is stopped). Do not change the operating mode during count operation.
Note 4. The TEDGPL bit is enabled only in event counter mode.
Note 5. To run AGT in Software Standby mode, select AGTLCLK (TCK[2:0] = 100b).
Note 6. AGTW0 cannot use AGTW0 underflow (setting prohibited). AGTW1 uses the AGTW0 underflow.
Note 7. Do not change the TCK[2:0] bits when the CKS[2:0] bits in the AGTMR2 register is not 000b. First, change the CKS[2:0] bits in the AGTMR2 register to 000b. Then change the TCK[2:0] bits and wait for one cycle of the count source.

23.2.6 AGTMR2 : AGT Mode Register 2

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)
Offset address: 0x0E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPM	—	—	—	—	CKS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CKS[2:0]	AGTLCLK Count Source Clock Frequency Division Ratio*1 *2 *3 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/4 0 1 1: 1/8 1 0 0: 1/16 1 0 1: 1/32 1 1 0: 1/64 1 1 1: 1/128	R/W
6:3	—	These bits are read as 0. The write value should be 0.	R/W
7	LPM	Low Power Mode 0: Normal mode 1: Low power mode	R/W

Note 1. Do not rewrite the CKS[2:0] bits during count operation. Only rewrite the CKS[2:0] bits when both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count stops).
Note 2. When count source is AGTLCLK, the switch of CKS[2:0] bits is valid.
Note 3. Do not switch the TCK[2:0] bits in the AGTMR1 register when CKS[2:0] bits are not 000b. Switch the TCK[2:0] bits in the AGTMR1 register after CKS[2:0] bits are set to 000b, and wait for 1 cycle of the count source.

CKS[2:0] bit (AGTLCLK Count Source Clock Frequency Division Ratio)

CKS[2:0] bits select the Count Source Clock Frequency Division Ratio for AGTLCLK.

Bit	Symbol	Function	R/W
3	TEDGPL	边缘极性*4 0: Single-edge 1: Both-edge	R/W
6:4	TCK[2:0]	计数源*1*2*5*7 000：PCLKB001：PCLKB8011：PCLKB2100：分频时钟AGTLCLK由AGTMR2寄存器中的CKS[2:0]位指定101：来自AGTW0的下溢事件信号*6 110：禁止设定 其他：禁止设置	R/W
7	—	该位读取为0。写入值应为0。	R/W

Note: 对AGTMR1寄存器的写访问初始化来自AGTWOn、AGTWOn、AGTWOAn和AGTWOBn引脚的输出。有关初始化时的输出电平的详细信息，请参阅第23.2.7节。AGTIOC：AGTIO控制寄存器。
注意1.选择事件计数器模式时，无论设置如何
TCK[2:0] bits.
注2.在计数操作期间不要切换计数源。只有当TSTART位和TCSTF标志都在
AGTCR寄存器设置为0（计数停止）。
注3.只有在AGTCR寄存器中的TSTART位和TCSTF标志都设置为0（计数停止）时停止计数才能更改操作模式。请勿在计数操作期间更改操作模式。
注4.TEDGPL位仅在事件计数器模式下启用。
注5.要在软件待机模式下运行AGT，请选择AGTLCLK(TCK[2:0]=100b)。
注6.AGTW0不能使用AGTW0下溢（禁止设置）。AGTW1使用AGTW0下溢。
注7.当AGTMR2寄存器中的CKS[2:0]位不是000b时，不要更改TCK[2:0]位。首先，更改CKS[2:0]位
AGTMR2寄存器到000b。然后改变TCK[2:0]位并等待计数源的一个周期。

23.2.6 AGTMR2:AGT模式寄存器2

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)
Offset address: 0x0E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPM	—	—	—	—	CKS[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CKS[2:0]	AGTLCLK计数源时钟分频比*1*2*3 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/4 0 1 1: 1/8 1 0 0: 1/16 1 0 1: 1/32 1 1 0: 1/64 1 1 1: 1/128	R/W
6:3	—	这些位被读取为0。写入值应为0。	R/W
7	LPM	低功耗模式 0：正常模式1：低功耗模式	R/W

注1.在计数操作期间不要重写CKS[2:0]位。仅当AGTCR寄存器中的TSTART位和TCSTF标志都设置为0（计数停止）时才重写CKS[2:0]位。

注2.当计数源为AGTLCLK时，CKS[2:0]位的切换有效。
注3.当CKS[2:0]位不是000b时，不要切换AGTMR1寄存器中的TCK[2:0]位。在CKS[2:0]位设置为000b后，切换AGTMR1寄存器中的TCK[2:0]位，并等待计数源的1个周期。

CKS[2:0]位（AGTLCLK计数源时钟分频比）

CKS[2:0]位选择AGTLCLK的计数源时钟分频比。

LPM bit (Low Power Mode)

The LPM bit sets the low power operation, which impacts access to certain AGT registers. Set this bit to 1 to operate in low power.

When this bit is 1, access to the following registers is prohibited:

- AGT/AGTCMA/AGTCMB/AGTCR.

After this bit is switched from 1 to 0, the first access to the register is constrained as follows:

- When reading from the AGT register, read AGT register twice. Only the second reading of data is valid.
- When writing to the AGT, AGTCMA, AGTCMB, and AGTCR register, allow at least 2 cycles of the count source clock when writing to the register.
- When confirm the value written to the AGT, AGTCMA, AGTCMB, and AGTCR registers.
  - When the count operation is stopped; after writing data, it can be read in the next cycle.
  - When the count operation is operating; after writing data, it can be written 4 cycles after the count source clock.

Figure 23.2 shows the flow of how to write LPM bit

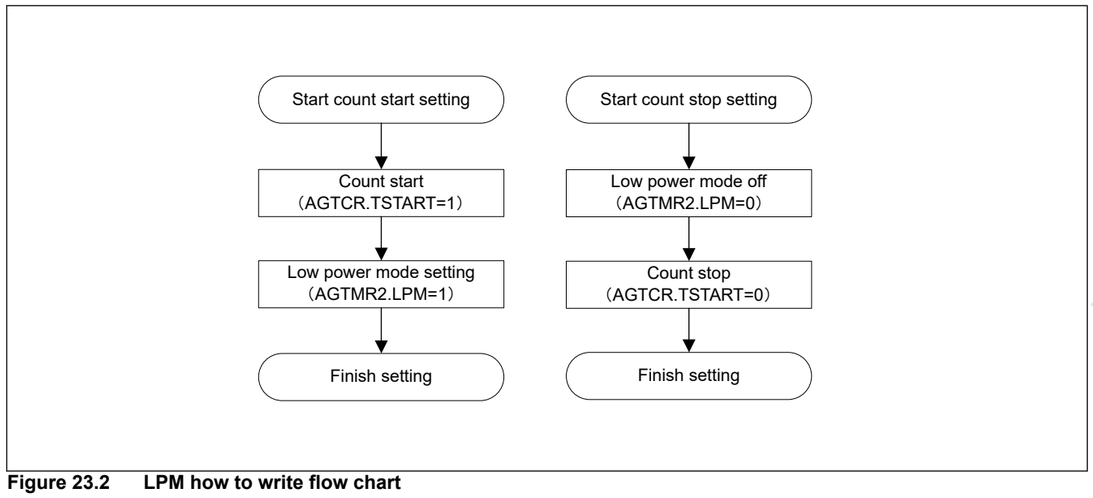


Figure 23.2 LPM how to write flow chart

23.2.7 AGTIOC : AGT I/O Control Register

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIOGT[1:0]		TIPF[1:0]		—	TOE	—	TEDG SEL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TEDGSEL	I/O Polarity Switch Function varies depending on the operating mode (see Table 23.3 and Table 23.4).	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W
2	TOE	AGTWOn pin Output Enable 0: AGTWOn pin output disabled 1: AGTWOn pin output enabled	R/W

LPM位（低功耗模式）

LPM位设置低功耗操作，这会影响对某些AGT寄存器的访问。将此位设置为1以在低功耗下工作。

该位为1时，禁止访问以下寄存器：

- AGT/AGTCMA/AGTCMB/AGTCR.

该位由1变为0后，对寄存器的第一次访问受到如下约束：

●读取AGT寄存器时，读取AGT寄存器两次。只有第二次读取数据是有效的。

●写入AGT、AGTCMA、AGTCMB和AGTCR寄存器时，写入寄存器时至少允许计数源时钟的2个周期。

●确认写入AGT、AGTCMA、AGTCMB、AGTCR寄存器的值时。

当计数操作停止时；写入数据后，可以在下一个周期读取。

当计数操作正在运行时；写入数据后，可在计数源时钟后4个周期写入。

图23.2显示如何写入LPM位的流程

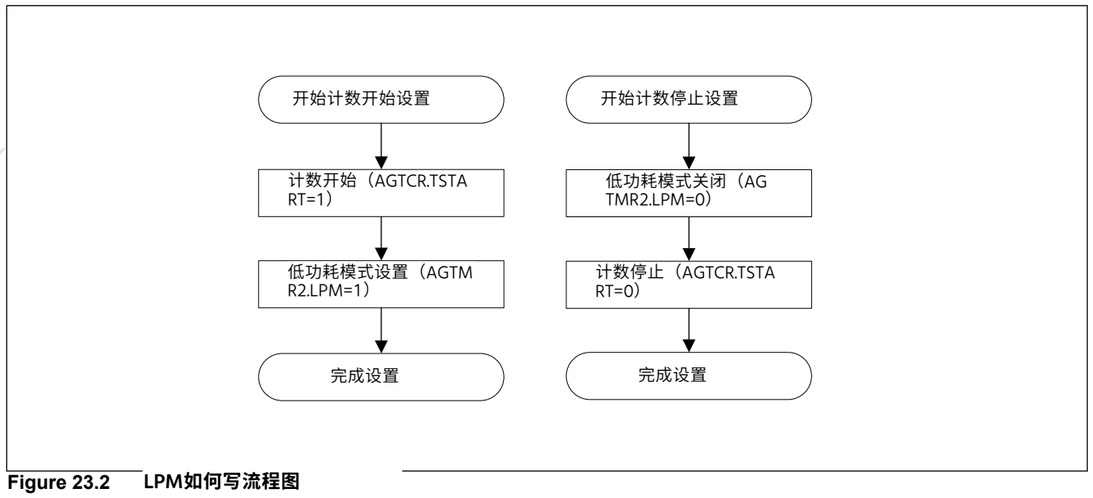


Figure 23.2 LPM如何写流程图

23.2.7 AGTIOC:AGTIO控制寄存器

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIOGT[1:0]		TIPF[1:0]		—	TOE	—	TEDG SEL
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TEDGSEL	IO极性开关 功能因操作模式而异（见表23.3和表23.4）。	R/W
1	—	该位读取为0。写入值应为0。	R/W
2	TOE	AGTWOn引脚输出使能 0：禁止AGTWOn引脚输出1：使能AGTWOn引脚输出	R/W

Bit	Symbol	Function	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
5:4	TIPF[1:0]	Input Filter*3 These bits specifies the sampling frequency of the filter for the AGTWIOn input. If the input to the AGTWIOn pin is sampled and the value matches three successive times, that value is taken as the input value. 0 0: No filter 0 1: Filter sampled at PCLKB 1 0: Filter sampled at PCLKB/8 1 1: Filter sampled at PCLKB/32	R/W
7:6	TIOGT[1:0]	Count Control*1 *2 0 0: Event is always counted 0 1: Event is counted during polarity period specified for AGTWEEn pin Others: Setting prohibited	R/W

Note 1. When AGTWEEn pin is used, the polarity to count an event can be selected with the EEPS bit in the AGTISR register.
Note 2. TIOGT[1:0] bits are enabled only in event counter mode.
Note 3. When event counter mode operation is performed during Software Standby mode, the digital filter function cannot be used.

TEDGSEL bit (I/O Polarity Switch)

The TEDGSEL bit switches the AGTWOn pin output polarity and the AGTWIOn pin input/output edge and polarity.

In pulse output mode, it only controls polarity of the AGTWOn pin output and AGTWIOn pin output. AGTWOn pin output and AGTWIOn pin output are initialized when the AGTMR1 register is written or the TSTOP bit in the AGTCR register is written with 1.

TOE bit (AGTWOn pin Output Enable)

The TOE bit selects whether the AGTOn pin output is disabled or enabled.

TIPF[1:0] bits (Input Filter)

The TIPF[1:0] bits specify the sampling frequency of the AGTIOn pin input filter. When the input to the AGTIOn pin is sampled and the values match three times in succession, the value is regarded as the input value.

TIOGT[1:0] bits (Count Control)

The TIOGT[1:0] bits control the event count.

Table 23.3 AGTWIOn pin I/O edge and polarity switching

Operating mode	Function
Timer mode	Not used
Pulse output mode	0: Output is started at high (initialization level: high) i.e. inverted output 1: Output is started at low (initialization level: low). i.e. normal output
Event counter mode	0: Count on rising edge 1: Count on falling edge.
Pulse width measurement mode	0: Low-level width is measured 1: High-level width is measured.
Pulse period measurement mode	0: Measure from one rising edge to the next rising edge 1: Measure from one falling edge to the next falling edge.

Table 23.4 AGTWOn pin output polarity switching

Operating mode	Function
All modes	0: Output is started at low (initial level: low): Normal output 1: Output is started at high (initial level: high): Inverted output

Bit	Symbol	Function	R/W
3	—	该位读取为0。写入值应为0。	R/W
5:4	TIPF[1:0]	输入滤波器*3 这些位指定AGTWIOn输入的滤波器采样频率。如果对AGTWIOn引脚的输入进行采样并且该值连续匹配3次，则将该值作为输入值。 00：无滤波器01：滤波器在PCLK B1采样0：滤波器在PCLKB8采样 11：滤波器在PCLKB32采样	R/W
7:6	TIOGT[1:0]	计数控制*1*2 00：始终计数事件01：在为AGTWEEn引脚指定的极性周期内计数事件 其他：禁止设置	R/W

注1.当使用AGTWEEn引脚时，可以通过AGTISR寄存器中的EEPS位选择计数事件的极性。
注2.TIOGT[1:0]位仅在事件计数器模式下启用。
注3.在软件待机模式下执行事件计数器模式操作时，不能使用数字滤波器功能。

TEDGSEL位（IO极性开关）

TEDGSEL位切换AGTWOn引脚输出极性和AGTWIOn引脚输入输出边沿和极性。

在脉冲输出模式下，它只控制AGTWOn引脚输出和AGTWIOn引脚输出的极性。AGTWOn引脚输出和AGTWIOn引脚输出在写入AGTMR1寄存器或AGTCR寄存器的TSTOP位写入1时初始化。

TOE位（AGTWOn引脚输出使能）

TOE位选择是禁用还是启用AGTOn引脚输出。

TIPF[1:0] bits (Input Filter)

TIPF[1:0]位指定AGTIOn引脚输入滤波器的采样频率。当AGTIOn引脚的输入被采样并且值连续匹配3次时，该值被认为是输入值。

TIOGT[1:0] bits (Count Control)

TIOGT[1:0]位控制事件计数。

Table 23.3 AGTWIOn引脚IO边沿和极性切换

操作模式	Function
定时器模式	不曾用过
脉冲输出方式	0：输出从高开始（初始化电平：高），即反相输出1：输出从低开始（初始化电平：低）。即正常输出
事件计数器模式	0：上升沿计数1：下降沿计数。
脉宽测量模式	0：测量低电平宽度1：测量高电平宽度。
脉冲周期测量模式	0：从一个上升沿测量到下一个上升沿1：从一个下降沿测量到下一个下降沿。

Table 23.4 AGTWOn引脚输出极性切换

操作模式	Function
所有模式	0：低电平开始输出（初始电平：低电平）：正常输出1：高电平开始输出（初始电平：高电平）：反相输出

23.2.8 AGTISR : AGT Event Pin Select Register

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x11

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	EEPS	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 0. The write value should be 0.	R/W
2	EEPS	AGTWEEn Polarity Selection 0: An event is counted during the low-level period 1: An event is counted during the high-level period	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

EEPS bit (AGTWEEn Polarity Selection)

The EEPS bit selects the polarity of events to be counted.

23.2.9 AGTCMSR : AGT Compare Match Function Select Register

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TOPOLB	TOEB	TCMEB	—	TOPOLA	TOEA	TCMEA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCMEA	AGT Compare Match A Register Enable*1 *2 *3 0: AGT Compare match A register disabled 1: AGT Compare match A register enabled	R/W
1	TOEA	AGTWOAn Pin Output Enable*1 *2 0: AGTWOAn pin output disabled 1: AGTWOAn pin output enabled	R/W
2	TOPOLA	AGTWOAn Pin Polarity Select*1 *2 0: AGTWOAn pin output is started on low. i.e. normal output 1: AGTWOAn pin output is started on high. i.e. inverted output	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	TCMEB	AGT Compare Match B Register Enable*1 *2 *3 0: Compare match B register disabled 1: Compare match B register enabled	R/W
5	TOEB	AGTWOBn Pin Output Enable*1 *2 0: AGTWOBn pin output disabled 1: AGTWOBn pin output enabled	R/W
6	TOPOLB	AGTWOBn Pin Polarity Select*1 *2 0: AGTWOBn pin output is started on low. i.e. normal output 1: AGTWOBn pin output is started on high. i.e. inverted output	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. Do not rewrite the AGTCMSR register during a count operation. Only rewrite the AGTCMSR register when both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count stops).
Note 2. Do not set 1 when in pulse width measurement mode or pulse period measurement mode.
Note 3. When 1 is written to the TSTOP bit in the AGTCR register, TCMEA and TCMEB is forcibly stopped and set to 0.

23.2.8 AGTISR:AGT事件引脚选择寄存器

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x11

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	EEPS	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	这些位被读取为0。写入值应为0。	R/W
2	EEPS	AGTWEEn极性选择 0：在低电平期间计数一个事件1：在高电平期间计数一个事件	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

EEPS位（AGTWEEn极性选择）

EEPS位选择要计数的事件的极性。

23.2.9 AGTCMSR:AGT比较匹配功能选择寄存器

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TOPOLB	TOEB	TCMEB	—	TOPOLA	TOEA	TCMEA
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCMEA	AGT比较匹配A寄存器使能*1*2*3 0：禁用AGT比较匹配A寄存器1：启用AGT比较匹配A寄存器	R/W
1	TOEA	AGTWOAn引脚输出使能*1*2 0：禁止AGTWOAn引脚输出1：使能AGTWOAn引脚输出	R/W
2	TOPOLA	AGTWOAn引脚极性选择*1*2 0：AGTWAn引脚输出低电平启动。即正常输出1：AGTWAn引脚输出以高电平启动。即反相输出	R/W
3	—	该位读取为0。写入值应为0。	R/W
4	TCMEB	AGT比较匹配B寄存器使能*1*2*3 0：比较匹配B寄存器禁用1：比较匹配B寄存器启用	R/W
5	TOEB	AGTWOBn引脚输出使能*1*2 0：禁止AGTWOBn引脚输出1：使能AGTWOBn引脚输出	R/W
6	TOPOLB	AGTWOBn引脚极性选择*1*2 0：AGTWOBn引脚输出从低电平开始。即正常输出1：AGTWOBn引脚输出以高电平启动。即反相输出	R/W
7	—	该位读取为0。写入值应为0。	R/W

注1.在计数操作期间不要重写AGCTMSR寄存器。只有在TSTART位和AGTCR寄存器中的TCSTF标志设置为0（计数停止）。
注2.在脉冲宽度测量模式或脉冲周期测量模式下不要设置为1。
注3.当AGTCR寄存器的TSTOP位写入1时，TCMEA和TCMEB被强制停止并设置为0。

23.2.10 AGTIOSEL : AGT Pin Select Register

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TIES	—	—	—	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
4	TIES	AGTWIOn Pin Input Enable 0: External event input is disabled during Software Standby mode 1: External event input is enabled during Software Standby mode	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

The AGTIOSEL register sets the AGTWIOn pin when using the AGTWIOn pin in Software Standby mode.

TIES bit (AGTWIOn Pin Input Enable)

The TIES bit enables or disables an external event input.

23.3 Operation

23.3.1 Reload Register and Counter Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and the counter differs depending on the value of the TSTART bit in the AGTCR register and of the TCMEA or TCMEB bit in the AGTCMSR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and the counter. When the TSTART bit is 1 (count starts) and the TCMEA bit and TCMEB bit are 0 (AGT compare match A/B register are invalid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the next count source. When the TSTART bit is 1 (count starts) and the TCMEA bit or the TCMEB bit is 1 (AGT compare match A register or compare match B register is valid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the underflow of the counter.

Figure 23.3 and Figure 23.4 show the timing of rewrite operation with TSTART bit value and TCMEA/TCMEB bit value.

23.2.10 AGTIOSEL:AGT引脚选择寄存器

Base address: AGTW_Bn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TIES	—	—	—	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	这些位被读取为0。写入值应为0。	R/W
4	TIES	AGTWIOn引脚输入使能 0：在软件待机模式下禁用外部事件输入1：在软件待机模式下启用外部事件输入	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

当在软件待机模式下使用AGTWIOn引脚时，AGTIOSEL寄存器设置AGTWIOn引脚。

TIES位（AGTWION引脚输入使能）

TIES位启用或禁用外部事件输入。

23.3 Operation

23.3.1 重载寄存器和计数器重写操作

无论何种操作模式，对重载寄存器和计数器的重写操作的时序根据AGTCR寄存器中的TSTART位和AGTCMSR寄存器中的TCMEA或TCMEB位的值而有所不同。当TSTART位为0（计数停止）时，计数值直接写入重载寄存器和计数器。当TSTART位为1（计数开始）且TCMEA位和TCMEB位为0（AGT比较匹配AB寄存器无效）时，该值与计数源同步写入重载寄存器，然后写入计数器与下一个计数源同步。当TSTART位为1（计数开始）且TCMEA位或TCMEB位为1（AGT比较匹配A寄存器或比较匹配B寄存器有效）时，值与计数源同步写入重载寄存器，然后与计数器的下溢同步到计数器。

图23.3和图23.4显示了使用TSTART位值和TCMEATCMEB位值进行重写操作的时序。

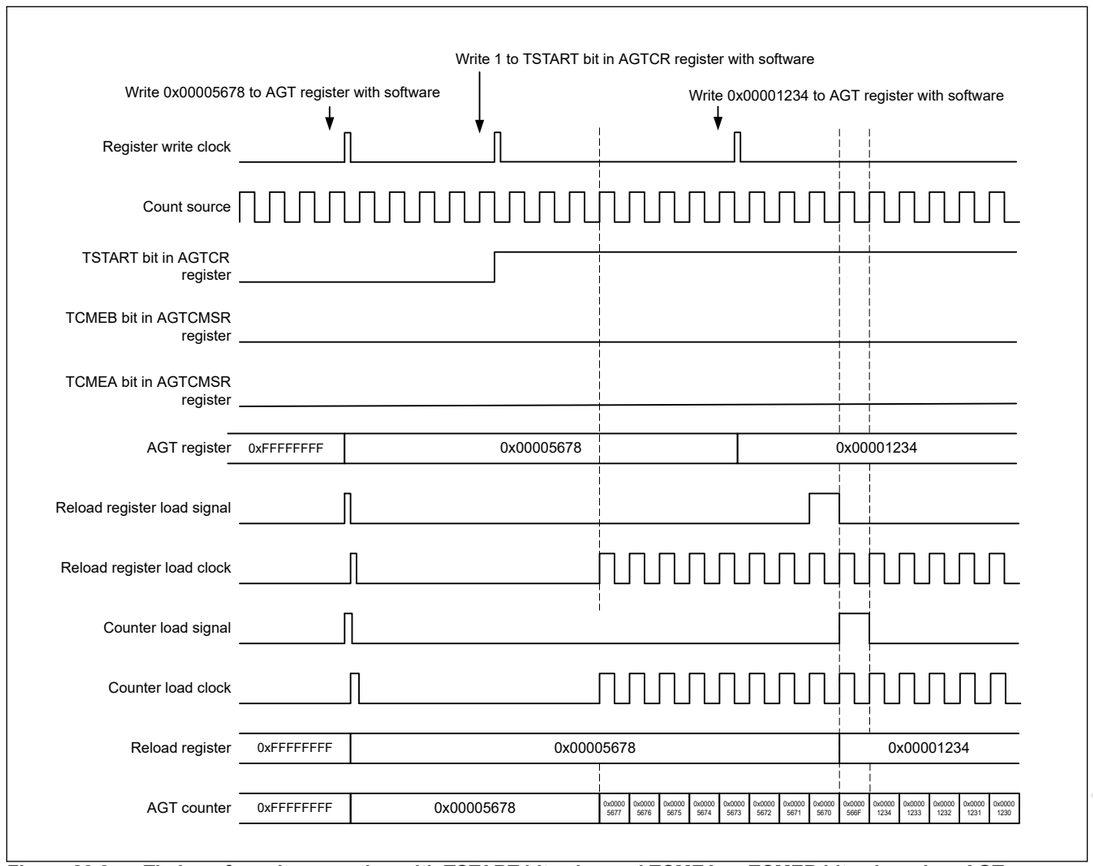


Figure 23.3 Timing of rewrite operation with TSTART bit value and TCMEA or TCMEB bit value when AGT compare match A register or AGT compare match B register is invalid

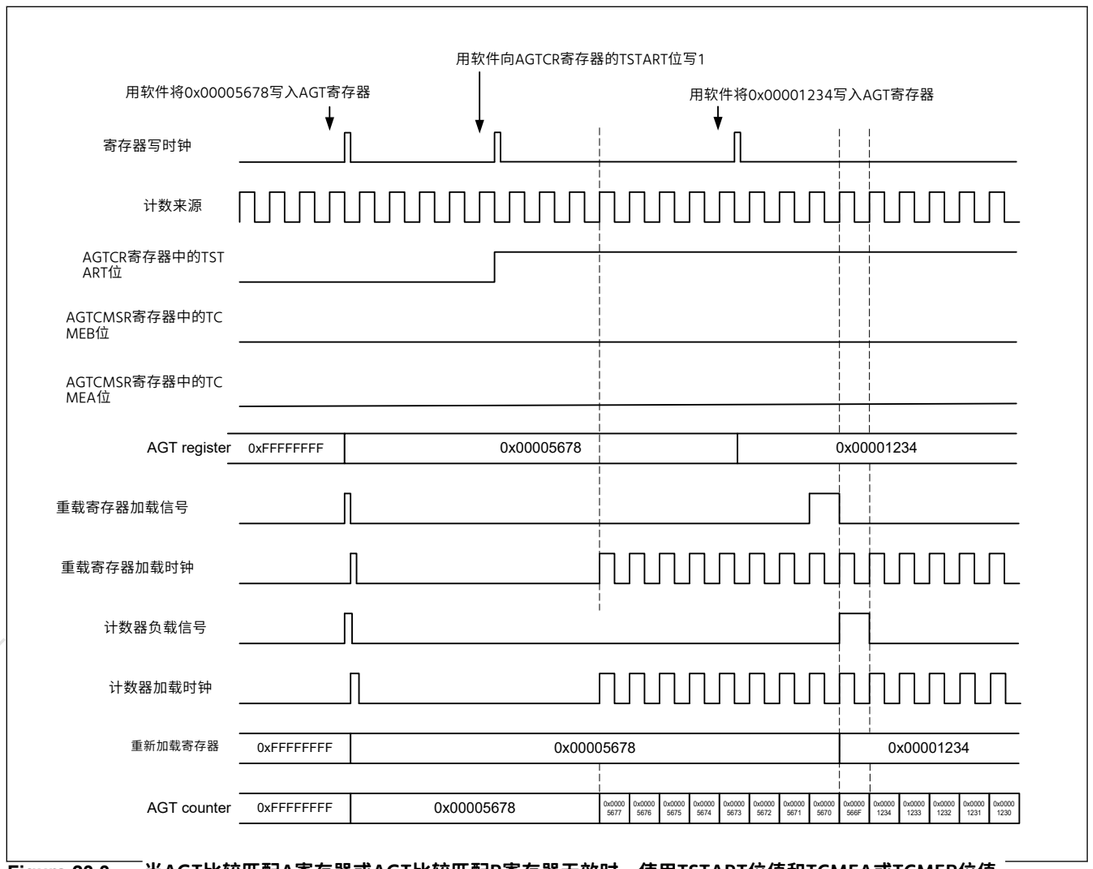


Figure 23.3 当AGT比较匹配A寄存器或AGT比较匹配B寄存器无效时，使用TSTART位值和TCMEA或TCMEB位值进行重写操作的时序

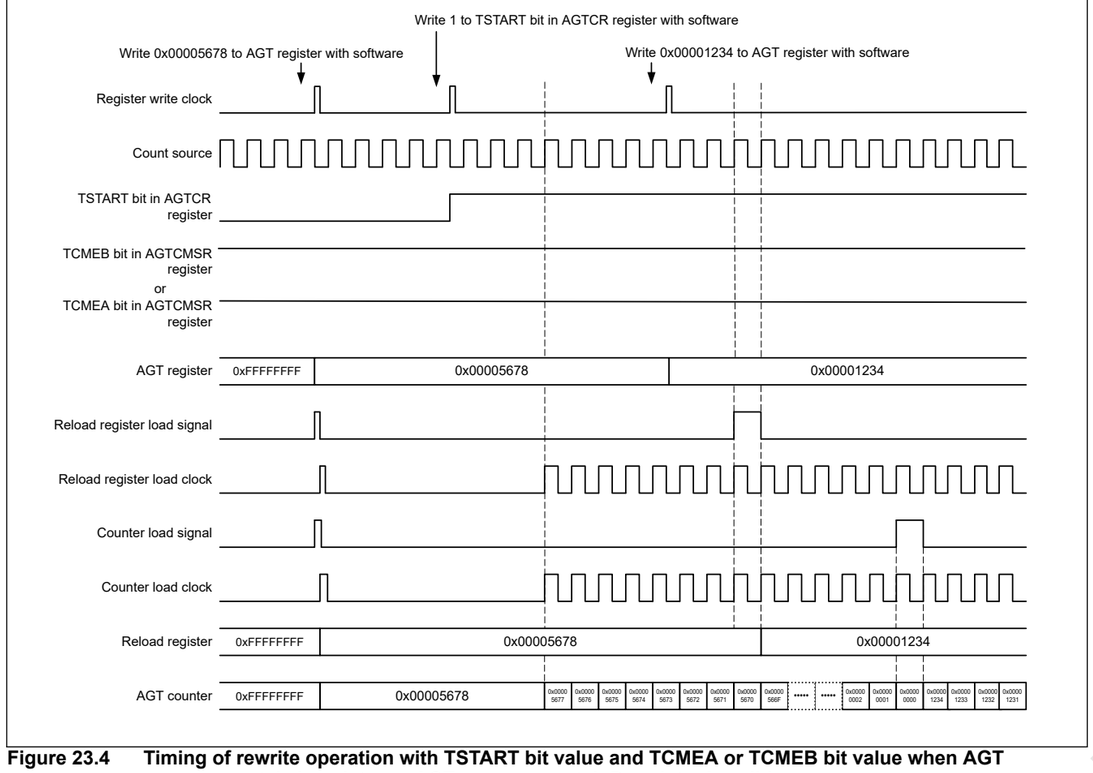


Figure 23.4 Timing of rewrite operation with TSTART bit value and TCMEA or TCMEB bit value when AGT compare match A register or AGT compare match B register is valid

23.3.2 Reload Register and AGT Compare Match A/B Register Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and AGT compare register A/B depends on the value of the TSTART bit in the AGTCR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and AGT compare register A/B. When the TSTART bit is 1 (count starts), the value is written to the reload register in synchronization with the count source, and then to the compare register in synchronization with the underflow of the counter.

Figure 23.5 shows the timing of rewrite operation with TSTART bit value for compare register A. AGT Compare register B is of the same timing as AGT compare register A.

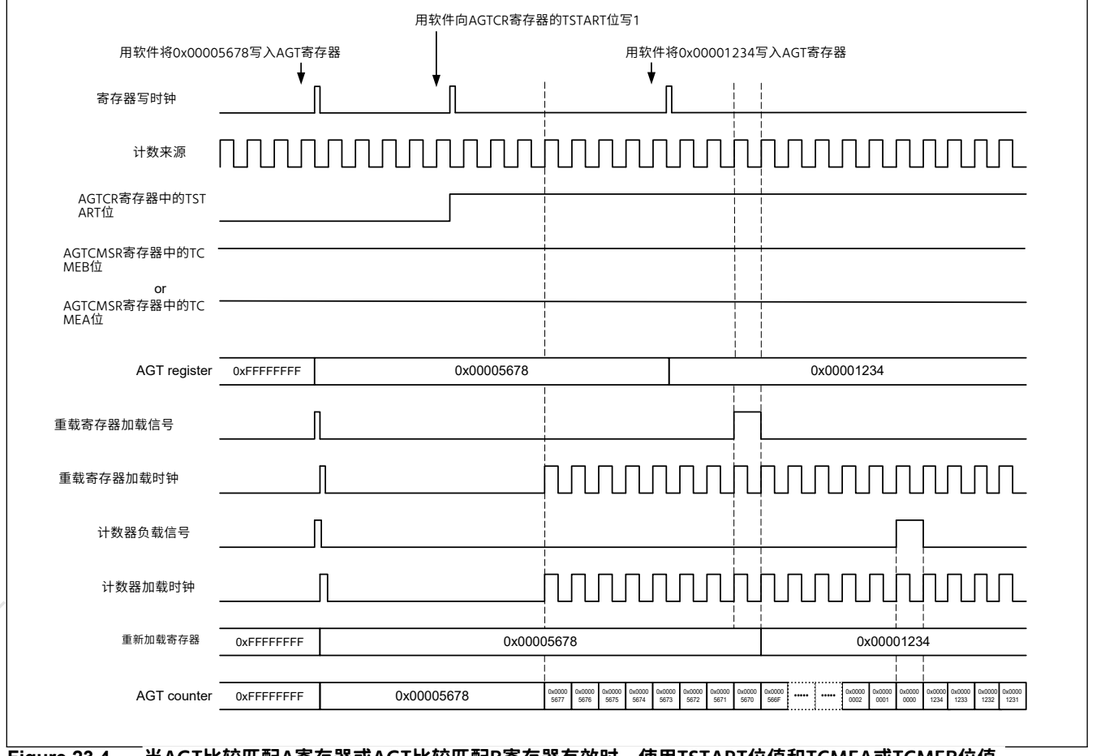


Figure 23.4 当AGT比较匹配A寄存器或AGT比较匹配B寄存器有效时，使用TSTART位值和TCMEA或TCMEB位值进行重写操作的时序

23.3.2 重载寄存器和AGT比较匹配AB寄存器重写操作

不管操作模式如何，对重载寄存器和AGT比较寄存器AB的重写操作的时序取决于AGTCR寄存器中TSTART位的值。当TSTART位为0（计数停止）时，计数值直接写入重载寄存器和AGT比较寄存器AB。当TSTART位为1（计数开始）时，该值同步写入重载寄存器计数源，然后与计数器的下溢同步到比较寄存器。

图23.5显示了比较寄存器A的TSTART位值的重写操作时序。AGT比较寄存器B与AGT比较寄存器A的时序相同。

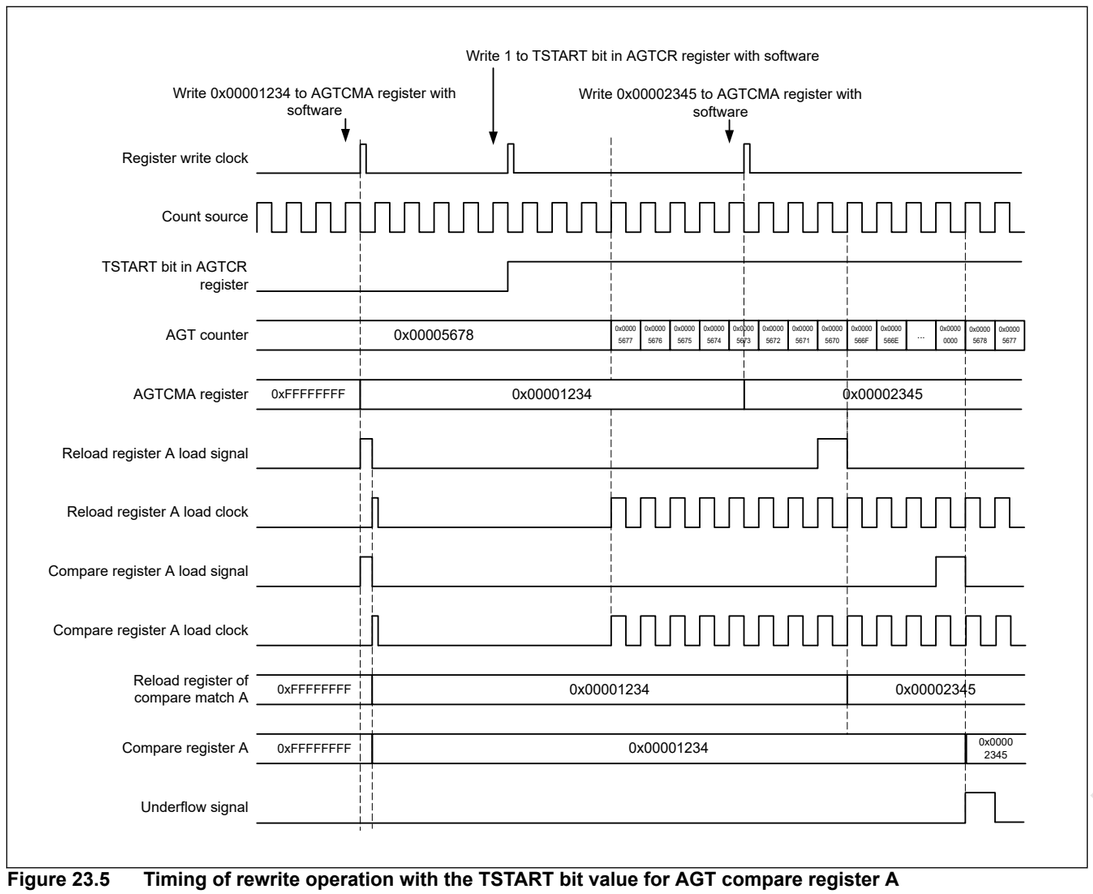


Figure 23.5 Timing of rewrite operation with the TSTART bit value for AGT compare register A

23.3.3 Timer Mode

In this mode, the AGT counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register. In timer mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0x00000000 and the next count source is input, an underflow occurs and an interrupt request is generated.

Figure 23.6 shows the operation example in timer mode.

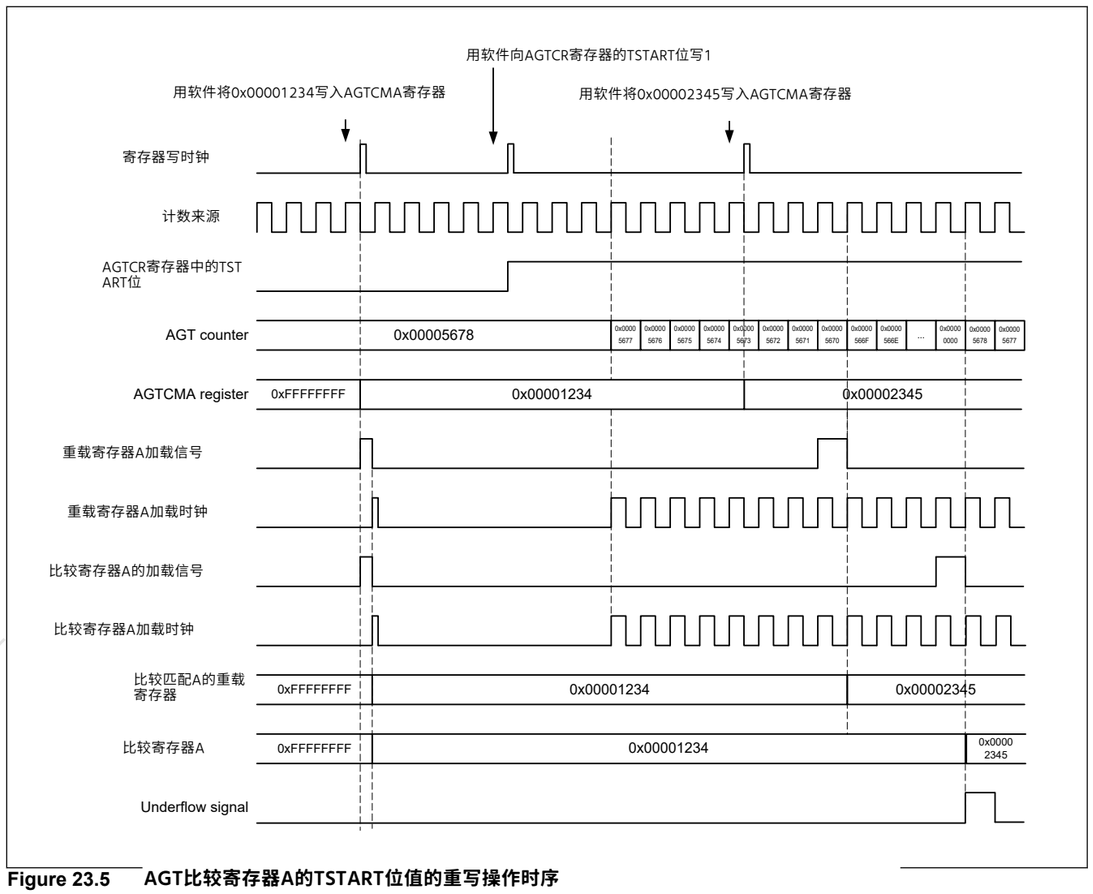


Figure 23.5 AGT比较寄存器A的TSTART位值的重写操作时序

23.3.3 定时器模式

在此模式下，AGT计数器按AGTMR1寄存器中的TCK[2:0]位选择的计数源递减。
在定时器模式下，计数值在计数源的每个上升沿减1。当计数值达到0x00000000并输入下一个计数源时，发生下溢并产生中断请求。

图23.6显示了定时器模式下的操作示例。

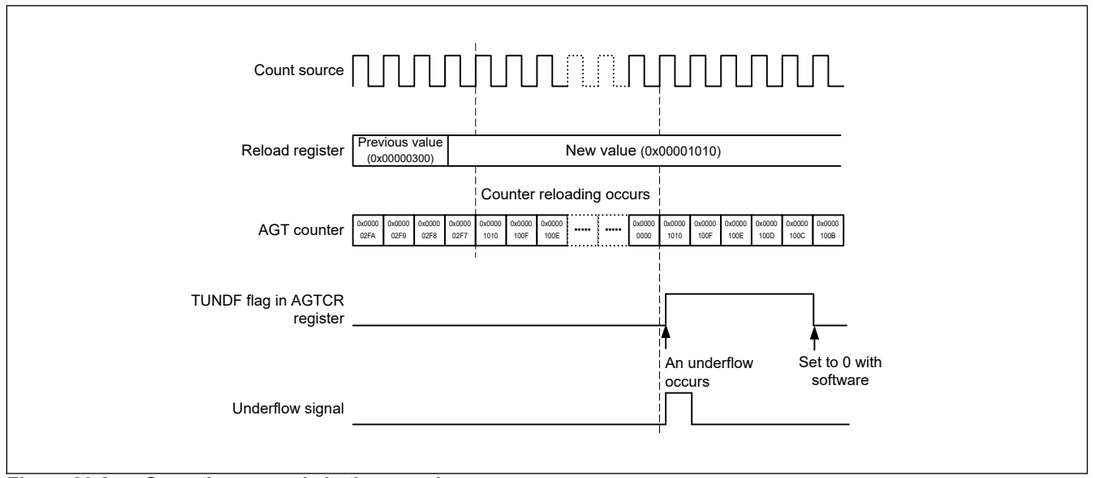


Figure 23.6 Operation example in timer mode

23.3.4 Pulse Output Mode

In pulse output mode, the counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register, and the output level of the AGTWIOn and AGTOn pins inverted each time an underflow occurs.

In pulse output mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0x00000000 and the next count source is input, an underflow occurs and an interrupt request is generated. In addition, a pulse can be output from the AGTWIOn and AGTOn pins. The output level is inverted each time an underflow occurs. The pulse output from the AGTWOn pin can be stopped with the TOE bit in the AGTIOC register. The output level can be selected with the TEDGSEL bit in the AGTIOC register.

Figure 23.7 shows the operation example in pulse output mode.

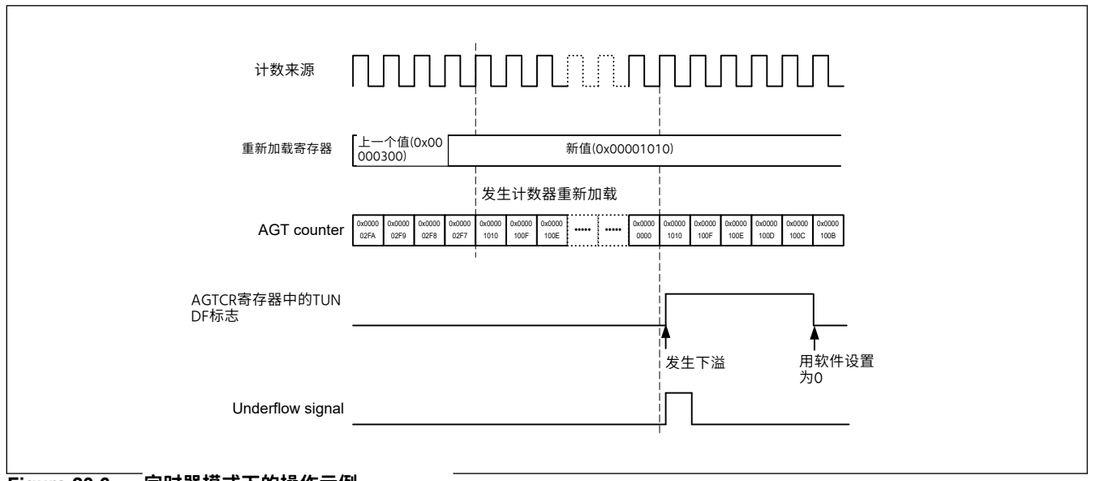


Figure 23.6 定时器模式下的操作示例

23.3.4 脉冲输出方式

在脉冲输出模式下，计数器由AGTMR1寄存器中的TCK[2:0]位选择的计数源递减，每次发生下溢时AGTWIOn和AGTOn引脚的输出电平反转。

在脉冲输出模式下，计数值在计数源的每个上升沿减1。当计数值达到0x00000000并输入下一个计数源时，发生下溢并产生中断请求。此外，可以从AGTWIOn和AGTOn引脚输出脉冲。每次发生下溢时，输出电平都会反转。AGTWOn引脚的脉冲输出可通过AGTIOC寄存器中的TOE位停止。可以通过AGTIOC寄存器中的TEDGSEL位选择输出电平。

图23.7显示了脉冲输出模式下的操作示例。

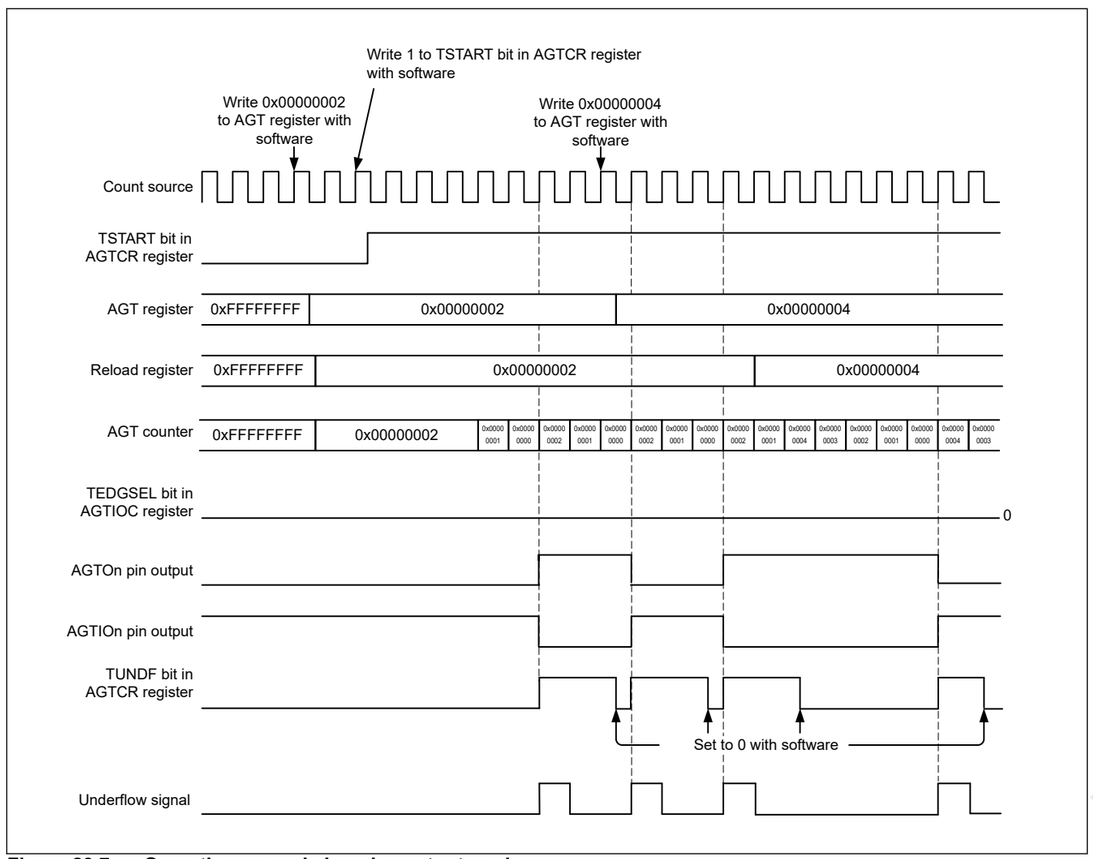


Figure 23.7 Operation example in pulse output mode

23.3.5 Event Counter Mode

In event counter mode, the counter is decremented by an external event signal (count source) input to the AGTWIOn pin. Various periods for counting events can be set with the TIOGT[1:0] bits in the AGTIOC register and AGTISR registers. In addition, the filter function for the AGTWIOn pin input can be specified with bits TIPF[1:0] in the AGTIOC register. The output from the AGTWOn pin can be toggled even in event counter mode.

Figure 23.8 shows the operation example in event counter mode.

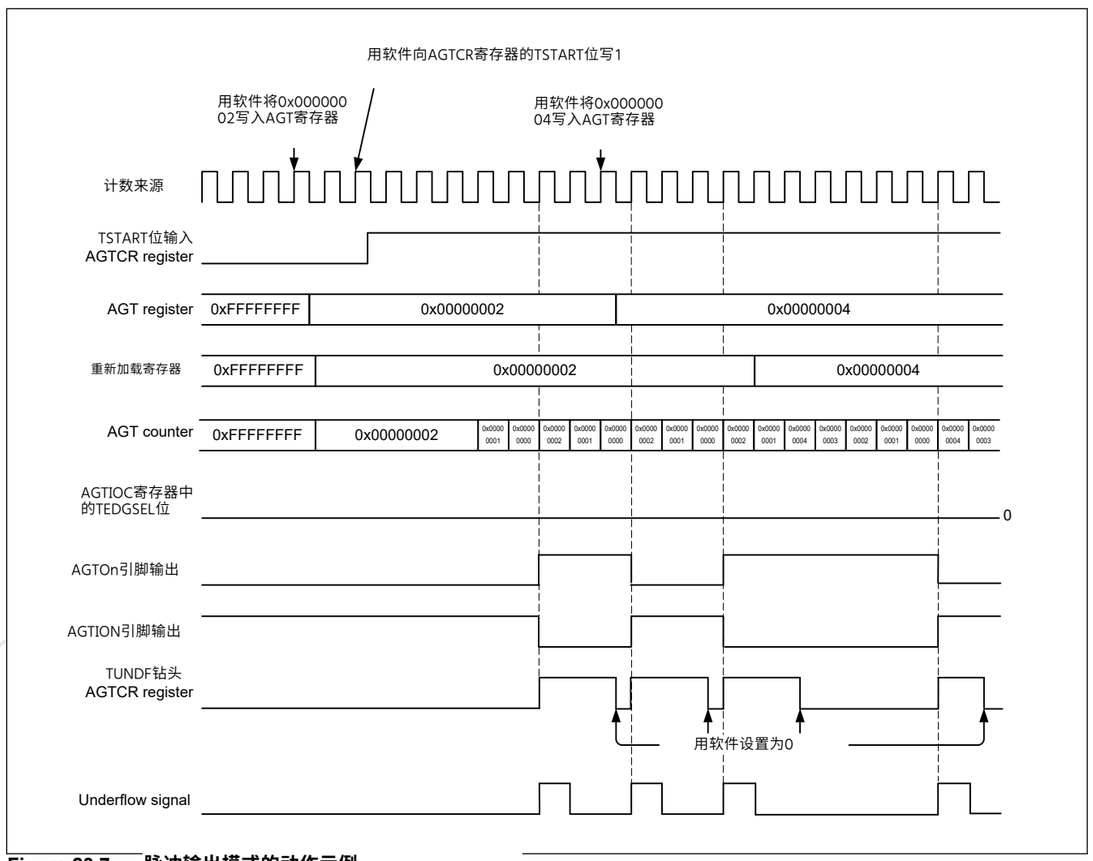


Figure 23.7 脉冲输出模式的动作示例

23.3.5 事件计数器模式

在事件计数器模式下，计数器由输入到AGTWIOn引脚的外部事件信号（计数源）递减。可以使用AGTIOC寄存器和AGTISR寄存器中的TIOGT[1:0]位设置计数事件的各种周期。此外，可以通过AGTIOC寄存器中的位TIPF[1:0]指定AGTWIOn引脚输入的过滤器功能。即使在事件计数器模式下，也可以切换AGTWOn引脚的输出。

图23.8显示了事件计数器模式下的操作示例。

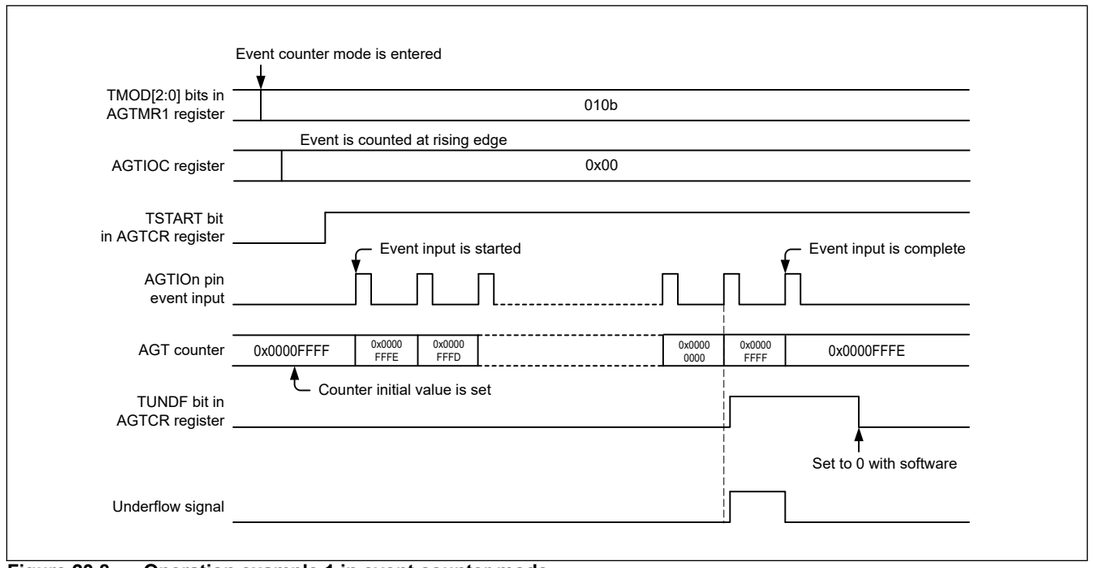
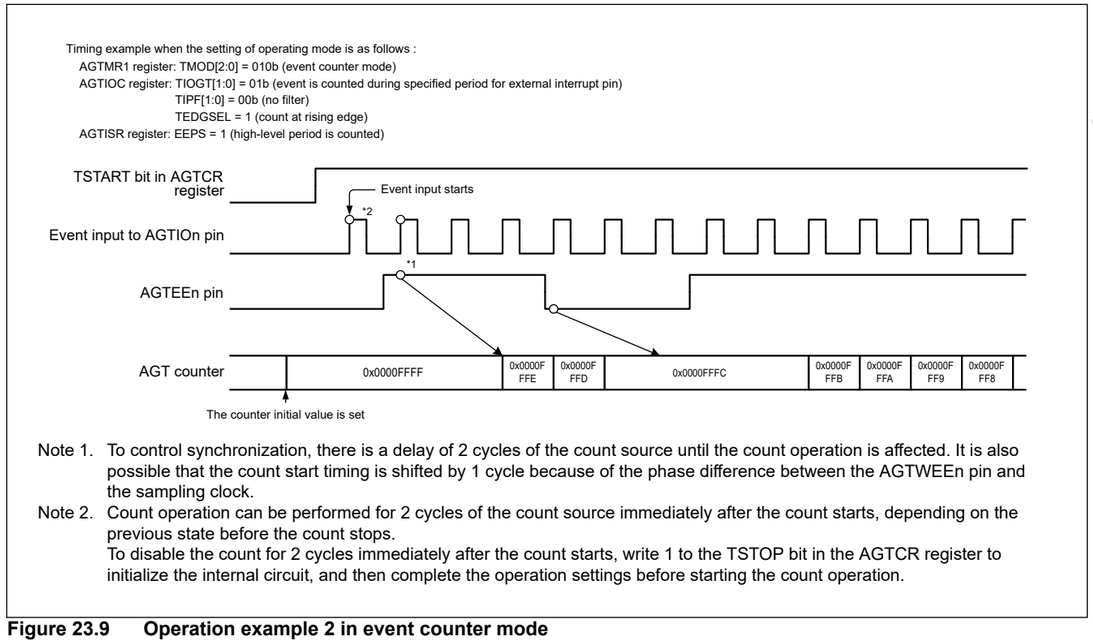


Figure 23.8 Operation example 1 in event counter mode

Figure 23.9 shows an operation example for counting during the specified period in event counter mode (TIOGT[1:0] bits in the AGTIOC register are set to 01b).



Note 1. To control synchronization, there is a delay of 2 cycles of the count source until the count operation is affected. It is also possible that the count start timing is shifted by 1 cycle because of the phase difference between the AGTWEEn pin and the sampling clock.

Note 2. Count operation can be performed for 2 cycles of the count source immediately after the count starts, depending on the previous state before the count stops.
To disable the count for 2 cycles immediately after the count starts, write 1 to the TSTOP bit in the AGTCR register to initialize the internal circuit, and then complete the operation settings before starting the count operation.

Figure 23.9 Operation example 2 in event counter mode

23.3.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the AGTWIOn pin is measured. When the level specified by the TEDGSEL bit in the AGTIOC register is input to the AGTWIOn pin, the counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register. When the specified level on the AGTWIOn pin ends, the counter is stopped, the TEDGF bit in the AGTCR register is set to 1 (active edge received), and an interrupt request is generated. The measurement of pulse width data is performed by reading the count value while the counter is

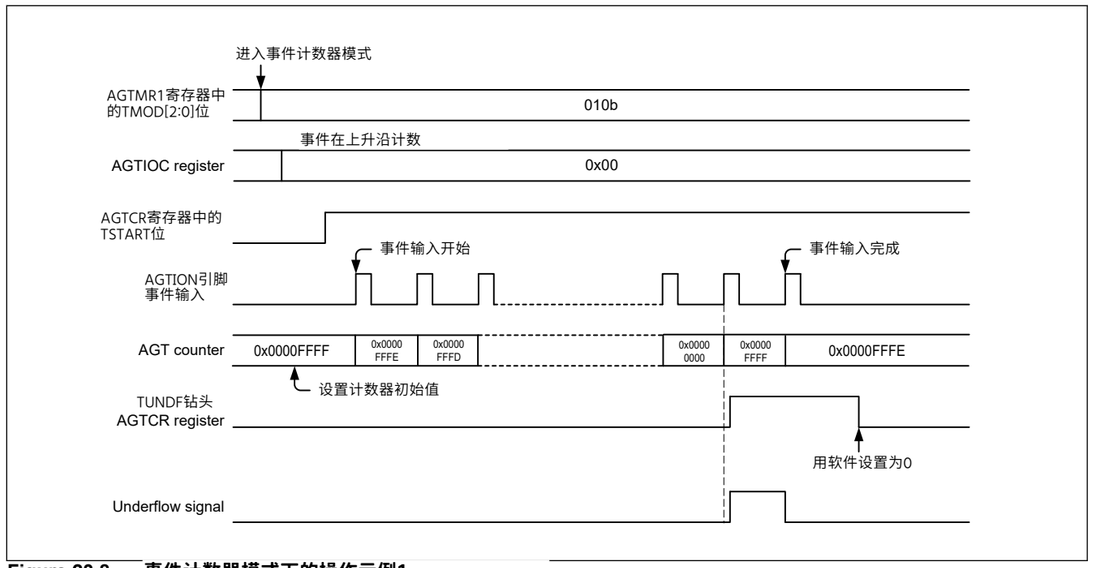
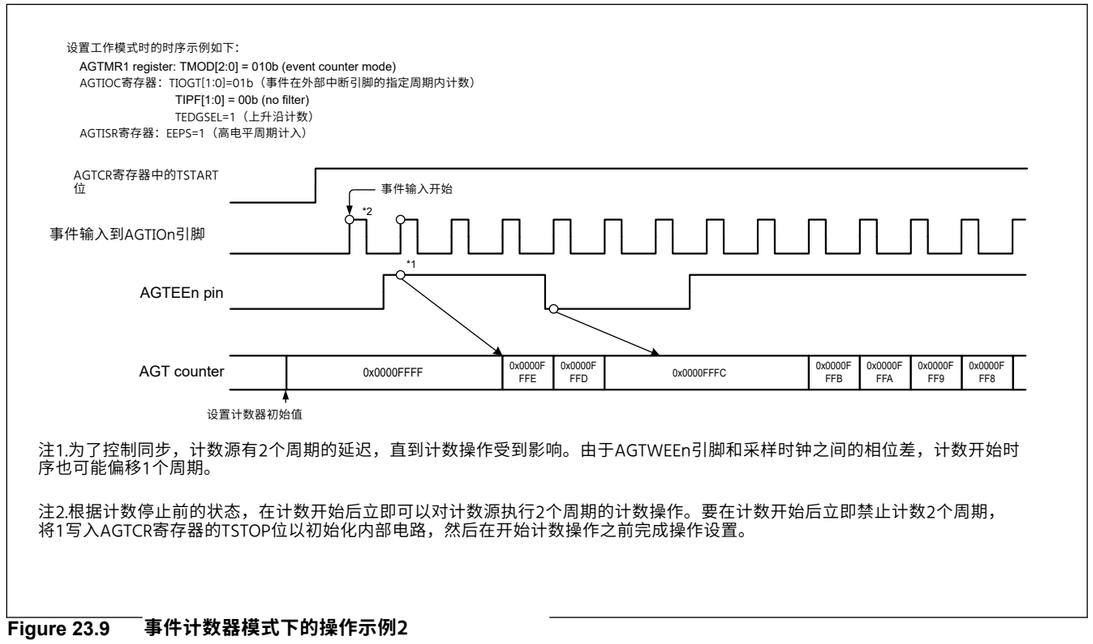


Figure 23.8 事件计数器模式下的操作示例1

图23.9显示了在事件计数器模式下在指定周期内进行计数的操作示例（AGTIOC寄存器中的TIOGT[1:0]位设置为01b）。



注1.为了控制同步，计数源有2个周期的延迟，直到计数操作受到影响。由于AGTWEEn引脚和采样时钟之间的相位差，计数开始时序也可能偏移1个周期。

注2.根据计数停止前的状态，在计数开始后立即可以对计数源执行2个周期的计数操作。要在计数开始后立即禁止计数2个周期，将1写入AGTCR寄存器的TSTOP位以初始化内部电路，然后在开始计数操作之前完成操作设置。

Figure 23.9 事件计数器模式下的操作示例2

23.3.6 脉冲宽度测量模式

在脉冲宽度测量模式下，测量输入到AGTWIOn引脚的外部信号的脉冲宽度。当AGTIOC寄存器中的TEDGSEL位指定的电平输入到AGTWIOn引脚时，计数器会根据AGTMR1寄存器中的TCK[2:0]位选择的计数源递减。当AGTWIOn引脚上的指定电平结束时，计数器停止，AGTCR寄存器中的TEDGF位设置为1（接收到有效沿），并产生中断请求。脉冲宽度数据的测量是通过在计数器运行时读取计数值来执行的。

stopped. Also, when the counter underflows during measurement, the TUNDF bit in the AGTCR register is set to 1 and an interrupt request is generated.

Figure 23.10 shows the operation example in pulse width measurement mode.

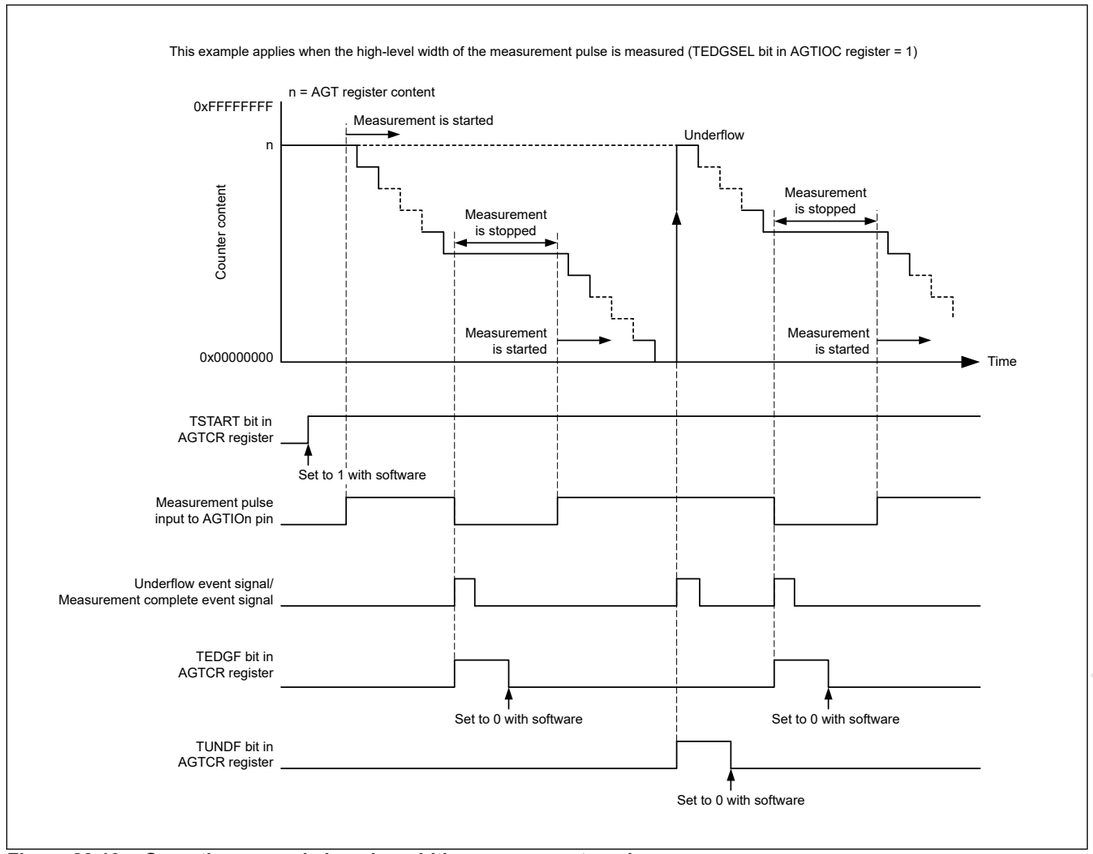


Figure 23.10 Operation example in pulse width measurement mode

23.3.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the AGTWIOn pin is measured. The counter is decremented by the count source selected with TCK[2:0] bits in the AGTMR1 register. When a pulse with the period specified by the TEDGSEL bit in the AGTIOC register is input to the AGTWIOn pin, the count value is transferred to the read-out buffer on the rising edge of the count source. The value in the reload register is loaded to the counter at the next rising edge. Simultaneously, the TEDGF flag in the AGTCR register is set to 1 (active edge received) and an interrupt request is generated. The read-out buffer (AGT register) is read at this time and the difference from the reload value (see section 23.4.6. How to Calculate Event Number, Pulse Width, and Pulse Period) is the period data of the input pulse. The period data is retained until the read-out buffer is read. When the counter underflows, the TUNDF flag in the AGTCR register is set to 1 (underflow) and an interrupt request is generated.

Figure 23.11 shows the operation example in pulse period measurement mode.

Only input pulses with a period longer than twice the period of the count source are measured. Also, the low-level and high-level widths must both be longer than the period of the count source. If a pulse period shorter than these conditions is input, the input might be ignored.

停了下来。此外，当测量期间计数器下溢时，AGTCR寄存器中的TUNDF位设置为1，并产生中断请求。

图23.10显示了脉宽测量模式下的操作示例。

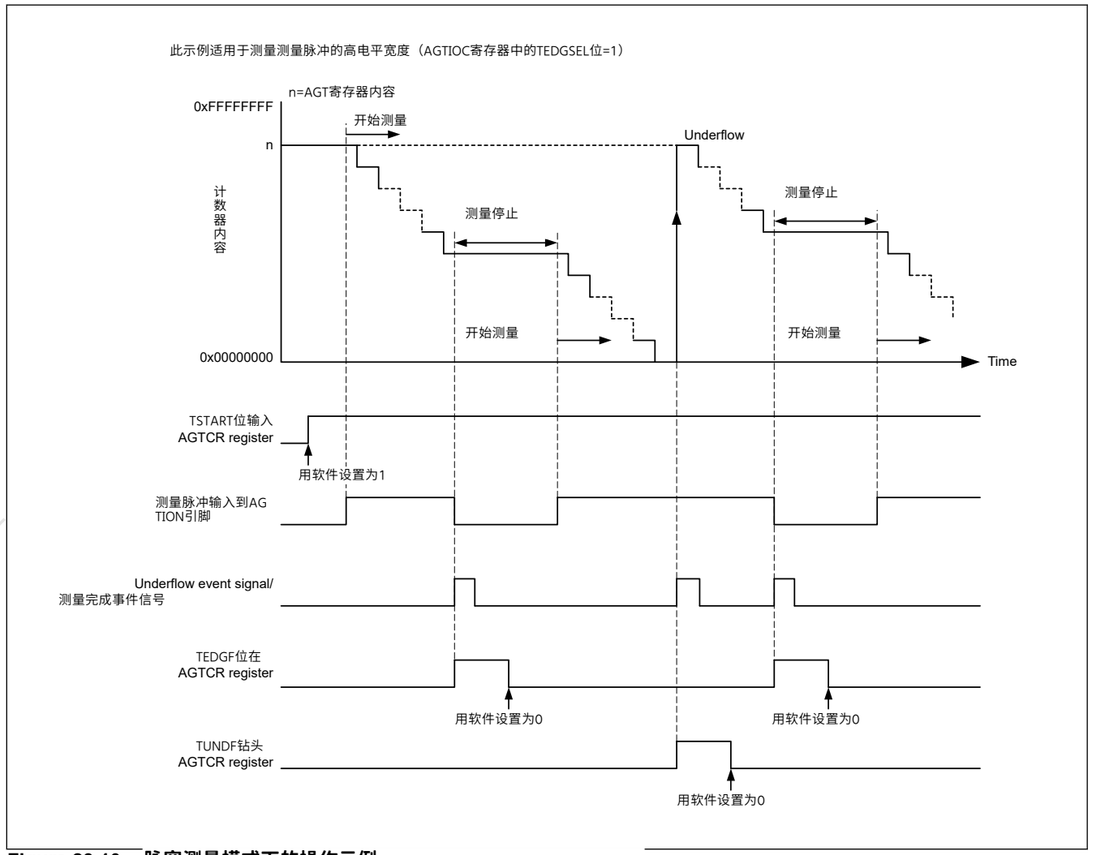


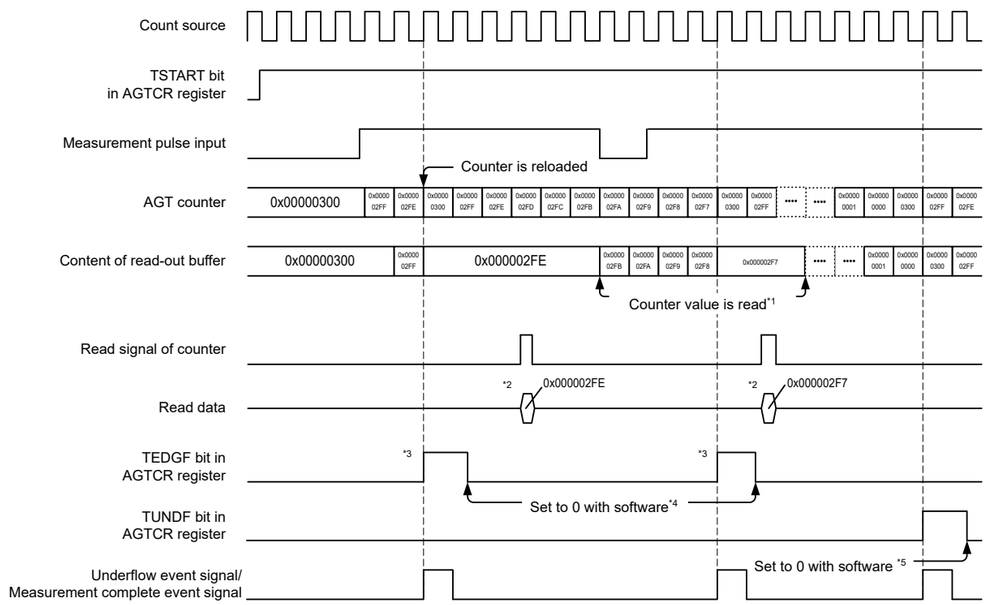
Figure 23.10 脉宽测量模式下的操作示例

23.3.7 脉冲周期测量模式

在脉冲周期测量模式下，测量输入到AGTWIOn引脚的外部信号的脉冲周期。计数器由AGTMR1寄存器中的TCK[2:0]位选择的计数源递减。当AGTIOC寄存器中的TEDGSEL位指定周期的脉冲输入到AGTWIOn引脚时，计数值在计数源的上升沿传送到读出缓冲器。重载寄存器中的值在下一个上升沿加载到计数器。同时，AGTCR寄存器中的TEDGF标志设置为1（接收到有效沿）并产生中断请求。此时会读取读出缓冲区（AGT寄存器），与重载值的差值（见23.4.6节。如何计算事件数、脉冲宽度和脉冲周期）是输入脉冲的周期数据。周期数据被保留，直到读出缓冲器被读取。当计数器下溢时，AGTCR寄存器中的TUNDF标志设置为1（下溢）并产生中断请求。

图23.11显示了脉冲周期测量模式下的操作示例。

仅测量周期长于计数源周期两倍的输入脉冲。此外，低电平和高电平宽度都必须长于计数源的周期。如果输入比这些条件短的脉冲周期，输入可能会被忽略。



This example applies when the initial value of the AGT register is set to A, the TEDGSEL bit in the AGTIOC register is set to 0, and the period from one rising edge to the next edge of the measurement pulse is measured.

Note 1. Reading from the AGT register must be performed during the period from when the TEDGF flag is set to 1 (active edge received) until the next active edge is input. The content of the read-out buffer is retained until the AGT register is read. If it is not read before the active edge is input, the measurement result of the previous period is retained.
Note 2. When the AGT register is read in pulse period measurement mode, the content of the read-out buffer is read.
Note 3. When the active edge of the measurement pulse is input and then the set edge of an external pulse is input, the TEDGF flag in the AGTCR register is set to 1 (active edge received).
Note 4. To set to 0 with software, write 0 to the TEDGF flag in the AGTCR register with an 8-bit memory manipulation instruction.
Note 5. To set to 0 with software, write 0 to the TUNDF flag in the AGTCR register with an 8-bit memory manipulation instruction.

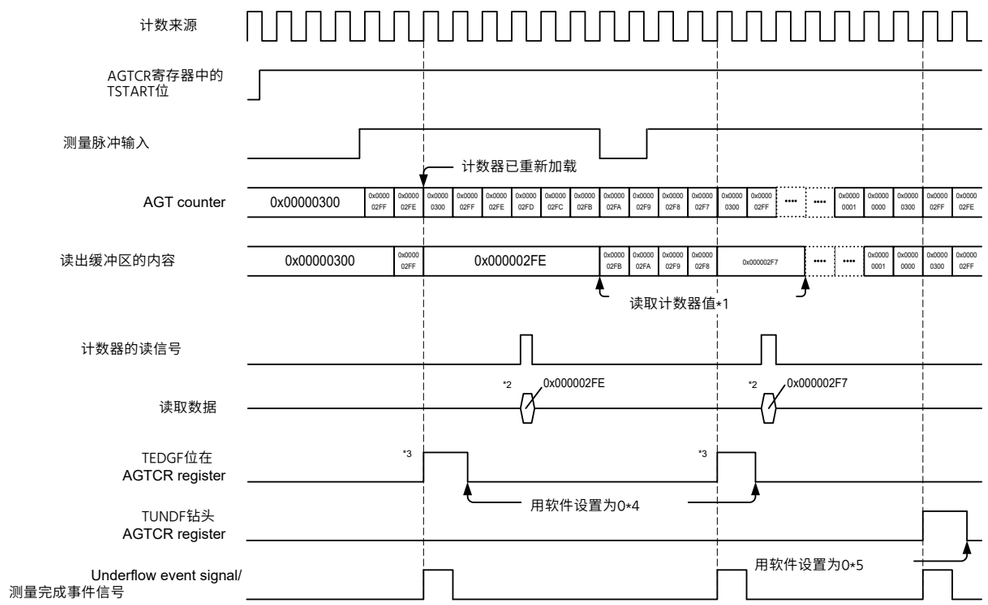
Figure 23.11 Operation example in pulse period measurement mode

23.3.8 Compare Match function

The compare match function detects matches (compare match) between the content of the AGTCMA or AGTCMB register and the content of the AGT register. This function is enabled when the TCMEA or TCMEB bit in the AGTCMSR register is 1 (compare match A register or compare match B register is valid). The counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register, and when the values of AGT and AGTCMA or AGTCMB match, the TCMAF/TCMBF flag in the AGTCR register is set to 1 (match), and an interrupt request is generated.

When the compare match function is enabled, the timing of the rewrite operation to the reload register and the counter differs. See section 23.3.1. Reload Register and Counter Rewrite Operation for details. In addition, the output level of the AGTWOAn, AGTWOBn pins is inverted by the match and by the underflow. The output level can be selected with the TOPOLA or TOPOLB bit in the AGTCMSR register.

Figure 23.12 shows the operation example in compare match mode.



此示例适用于将AGT寄存器的初始值设置为A，将AGTIOC寄存器中的TEDGSEL位设置为0，并测量从一个上升沿到下一个测量脉冲沿的周期的情况。

注1.从TEDGF标志设置为1（接收到有效边沿）到输入下一个有效边沿期间，必须执行从AGT寄存器的读取。读出缓冲器的内容一直保留到AGT寄存器被读取。如果在输入有效边沿之前未读取，则保留前一周期的测量结果。

注2.在脉冲周期测量模式下读取AGT寄存器时，会读取读出缓冲区的内容。
注3.当输入测量脉冲的有效边沿，然后输入外部脉冲的设置边沿时，AGTCR寄存器中的TEDGF标志设置为1（接收到有效边沿）。

注4.要使用软件设置为0，请使用8位存储器操作指令将0写入AGTCR寄存器中的TEDGF标志。注5.要通过软件设置为0，请使用8位存储器操作指令将0写入AGTCR寄存器中的TUNDF标志。

Figure 23.11 脉冲周期测量模式下的操作示例

23.3.8 比较匹配功能

比较匹配功能检测AGTCMA或AGTCMB寄存器的内容与AGT寄存器的内容之间的匹配（比较匹配）。该功能在AGTCMSR寄存器中的TCMEA或TCMEB位为1时使能（比较匹配A寄存器或比较匹配B寄存器有效）。计数器按AGTMR1寄存器中TCK[2:0]位选择的计数源递减，当AGT和AGTCMA或AGTCMB的值匹配时，AGTCR寄存器中的TCMAFTCMBF标志设置为1（匹配），并产生中断请求。

当比较匹配功能启用时，对重载寄存器和计数器的重写操作的时序不同。请参阅第23.3.1节。重载寄存器和计数器重写操作了解详情。此外，AGTWOAn、AGTWOBn引脚的输出电平通过匹配和下溢反转。输出电平可以选择与

AGTCMSR寄存器中的TOPOLA或TOPOLB位。

图23.12显示了比较匹配模式下的操作示例。

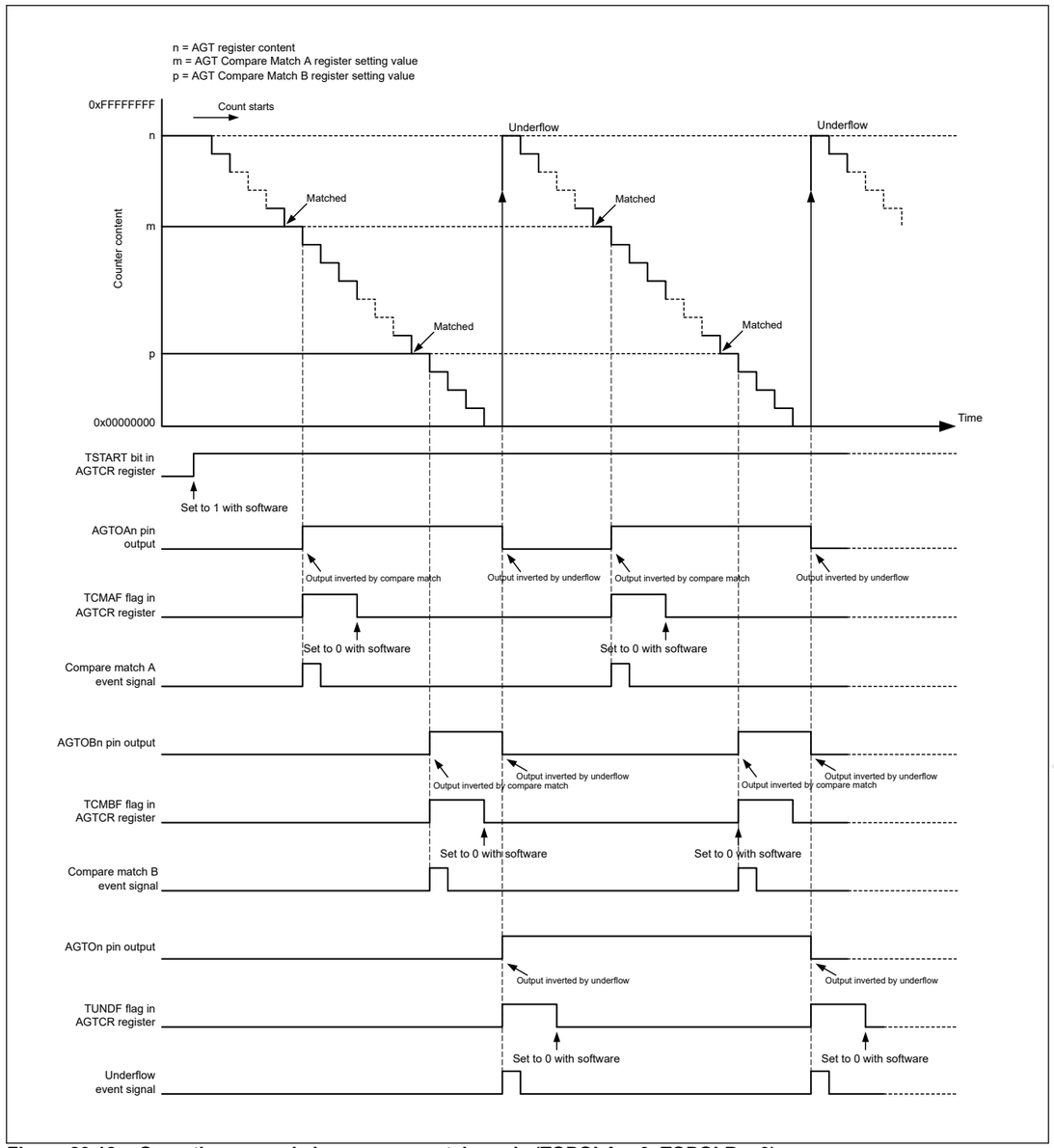


Figure 23.12 Operation example in compare match mode (TOPOLA = 0, TOPOLB = 0)

23.3.9 Output Settings for Each Mode

Table 23.5 to Table 23.8 list the states of pins AGTWOn, AGTWIOn, AGTWOAn, and AGTWOBn pins in each mode.

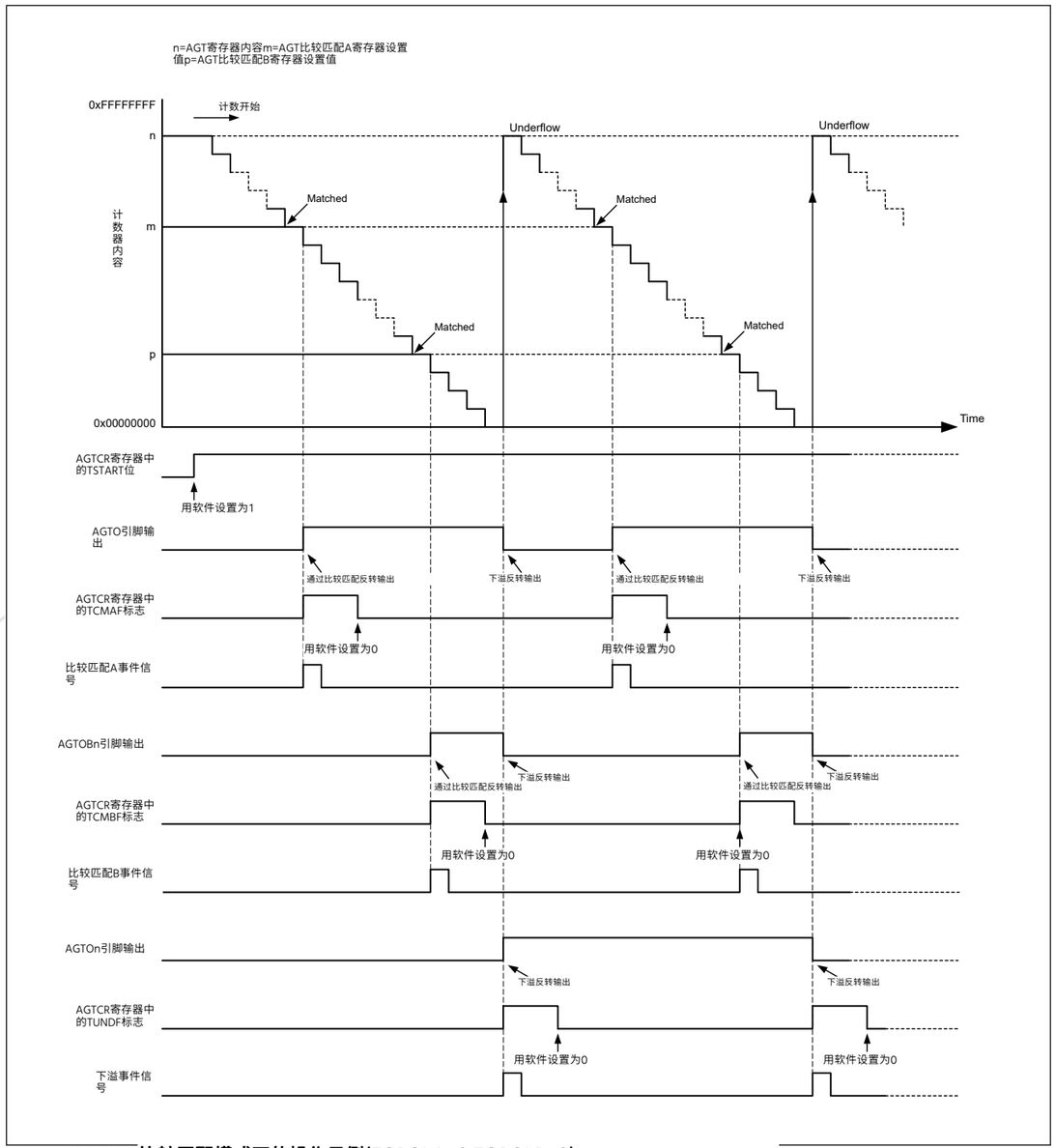


Figure 23.12 比较匹配模式下的操作示例(TOPOLA=0 TOPOLB=0)

23.3.9 每种模式的输出设置

表23.5至表23.8列出了引脚AGTWOn、AGTWOn、AGTWOAn和AGTWOBn引脚在每种模式下的状态。

Table 23.5 AGTWOn pin setting

Operating mode	AGTIOC register		AGTWOn pin output
	TOE bit	TEDGSEL bit	
All modes	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled

Table 23.6 AGTWIOn pin setting

Operating mode	AGTIOC register	AGTWIOn pin I/O
	TEDGSEL bit	
Timer mode	0 or 1	Input (not used)
Pulse output mode	1	Normal output
	0	Inverted output
Event counter mode	0 or 1	Input
Pulse width measurement mode		
Pulse period measurement mode		

Table 23.7 AGTWOAn pin setting

Operating mode	AGTCMSR register		AGTWOAn pin output
	TOEA bit	TOPOLA bit	
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

Table 23.8 AGTWOBn pin setting (1 of 2)

Operating mode	AGTCMSR register		AGTWOBn pin output
	TOEB bit	TOPOLB bit	
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)

Table 23.5 AGTWOn引脚设置

操作模式	AGTIOC register		AGTWOn引脚输出
	脚趾位	TEDGSEL bit	
所有模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用

Table 23.6 AGTWIOn引脚设置

操作模式	AGTIOC register	AGTWIOn pin I/O
	TEDGSEL bit	
定时器模式	0 or 1	Input (not used)
脉冲输出方式	1	正常输出
	0	反相输出
事件计数器模式	0 or 1	Input
脉宽测量模式		
脉冲周期测量模式		

Table 23.7 AGTWO引脚设置

操作模式	AGTCMSR register		AGTWO引脚输出
	TOEA bit	TOPOLA bit	
定时器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉冲输出方式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
事件计数器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉宽测量模式	0	0	Prohibited
脉冲周期测量模式			

Table 23.8 AGTWOBn引脚设置(1of2)

操作模式	AGTCMSR register		AGTWOBn引脚输出
	TOEB bit	TOPOLB bit	
定时器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉冲输出方式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
事件计数器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）

Table 23.8 AGTWOBn pin setting (2 of 2)

Operating mode	AGTCMSR register		AGTWOBn pin output
	TOEB bit	TOPOLB bit	
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

23.3.10 Standby Mode

The AGT can operate in Software Standby mode. Set it to Software Standby mode with count operation start (TSTART = 1, TCSTF = 1).

Table 23.9 and Table 23.10 show the setting that can be used in Software Standby mode.

Table 23.9 Usable settings in Software Standby mode (AGTW0)

Operating mode	AGTMR1.TCK[2:0]	Operating clock	Resurgence factor of CPU
Timer mode	100b	AGTLCLK	—
Pulse output mode	100b	AGTLCLK	—
Event counter mode	—	AGTWIOn*1	—
Pulse width measurement mode	100b	AGTLCLK	—
Pulse period measurement mode	100b	AGTLCLK	—

Note: —: invalid
Note 1. When using the AGTWIOn pin for external event input in Software Standby mode, set AGTIOSEL.TIES = 1.

Table 23.10 Usable settings in Software Standby mode (AGTW1)

Operating mode	AGTMR1.TCK[2:0]	Operating clock	Resurgence factor of CPU
Timer mode	100b or 101b*1	AGTLCLK or AGTW0 underflow	• Underflow • Compare match A/B
Pulse output mode	100b or 101b*1	AGTLCLK or AGTW0 underflow	• Underflow • Compare match A/B
Event counter mode	—	AGTWIOn*2	• Underflow • Compare match A/B
Pulse width measurement mode	100b or 101b*1	AGTLCLK or AGTW0 underflow	• Underflow • Active edge
Pulse period measurement mode	100b or 101b*1	AGTLCLK or AGTW0 underflow	• Underflow • Active edge

Note: —: invalid
Note: Release of Software Standby mode is only AGT1.
Note: Compare match A/B is resurgence factor of CPU from Software Standby mode.
Note 1. Only when AGTW0 operates in Table 23.9
Note 2. When using the AGTWIOn pin for external event input in Software Standby mode, set AGTIOSEL.TIES = 1.

23.3.11 Interrupt Sources

The AGTWn has three interrupt sources as listed in Table 23.11.

Table 23.11 AGTW interrupt sources

Name	Interrupt source	DMAC/DTC activation
AGTn_AGTI	• When the counter underflows • When measurement of the active width of the external input pin (AGTWIOn) is complete in pulse width measurement mode • When the set edge of the external input pin (AGTWIOn) is input in pulse period measurement mode.	Possible
AGTn_AGTCMAI	• When the values of AGT register and AGTCMA register match	Possible
AGTn_AGTCMBI	• When the values of AGT register and AGTCMB register match	Possible

Note: Channel number (n = 0, 1)

Table 23.8 AGTWOBn引脚设置(2of2)

操作模式	AGTCMSR register		AGTWOBn引脚输出
	TOEB bit	TOPOLB bit	
脉宽测量模式	0	0	Prohibited
脉冲周期测量模式			

23.3.10 待机模式

AGT可以在软件待机模式下运行。将其设置为软件待机模式，计数操作开始（TSTART=1，TCSTF = 1).

表23.9和表23.10显示了可以在软件待机模式下使用的设置。

Table 23.9 软件待机模式下的可用设置(AGTW0)

操作模式	AGTMR1.TCK[2:0]	工作时钟	CPU的中兴系数
定时器模式	100b	AGTLCLK	—
脉冲输出方式	100b	AGTLCLK	—
事件计数器模式	—	AGTWIOn*1	—
脉宽测量模式	100b	AGTLCLK	—
脉冲周期测量模式	100b	AGTLCLK	—

Note: —: invalid
注1.在软件待机模式下将AGTWIOn引脚用于外部事件输入时，设置AGTIOSEL.TIES=1。

Table 23.10 软件待机模式下的可用设置(AGTW1)

操作模式	AGTMR1.TCK[2:0]	工作时钟	CPU的中兴系数
定时器模式	100b or 101b*1	AGTLCLK or AGTW0 underflow	• Underflow • 比较匹配AB
脉冲输出方式	100b or 101b*1	AGTLCLK or AGTW0 underflow	• Underflow • 比较匹配AB
事件计数器模式	—	AGTWIOn*2	• Underflow • 比较匹配AB
脉宽测量模式	100b or 101b*1	AGTLCLK or AGTW0 underflow	• Underflow • 主动边缘
脉冲周期测量模式	100b or 101b*1	AGTLCLK or AGTW0 underflow	• Underflow • 主动边缘

Note: —: invalid
Note: 软件待机模式的释放只有AGT1。
Note: 比较匹配AB是CPU从软件待机模式中恢复的因素。
注1.仅当AGTW0在表23.9中运行时
注2.在软件待机模式下将AGTWIOn引脚用于外部事件输入时，设置AGTIOSEL.TIES=1。

23.3.11 中断源

AGTWn有表23.11中列出的三个中断源。

Table 23.11 AGTW中断源

Name	中断源	DMAC/DTC activation
AGTn_AGTI	• 当计数器下溢时 • 在脉冲宽度测量模式下，外部输入引脚(AGTWION)的有效宽度测量完成时 • 在脉冲周期测量模式下输入外部输入引脚(AGTWION)的设置边沿时。	Possible
AGTn_AGTCMAI	• 当AGT寄存器和AGTCMA寄存器的值匹配时	Possible
AGTn_AGTCMBI	• 当AGT寄存器和AGTCMB寄存器的值匹配时	Possible

Note: 通道号(n=0 1)

23.3.12 Event Signal Output to ELC

The AGTWn (n = 0, 1) uses the Event Link Controller (ELC) to perform a link operation to a specified module using the interrupt request signal as the event signal. The AGTWn (n = 0, 1) outputs compare match A, compare match B, and underflow/measurement complete signals as event signals. For details, see section 17, Event Link Controller (ELC).

23.4 Usage Notes

23.4.1 Count Operation Start and Stop Control

- When the operating mode (see Table 23.1) is set to other than the event counter mode, or the count source is set to other than AGTWn underflow event signal (TCK[2:0] = 101b):
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count is stopped, the TCSTF flag in the AGTCR register remains 0 (count stops) for 3 cycles of the count source. Do not access the registers associated with AGTW other than the TCSTF flag until this bit is set to 1 (count in progress).
  - After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF flag remains 1 for 3 cycles of the count source. When the TCSTF flag is set to 0, the count is stopped. Do not access the registers associated with AGTW. Other than the TCSTF flag until this bit is set to 0.
- When the operating mode (see Table 23.1) is set to event counter mode, or the count source is set to AGTW1 underflow event signal (TCK[2:0] = 101b):
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count is stopped, the TCSTF flag in the AGTCR register remains 0 (count stops) for 2 PCLKB cycles. Do not access the registers associated with AGTW other than the TCSTF flag until this bit is set to 1 (count in progress).
  - After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF flag remains 1 for 2 PCLKB cycles. When the TCSTF flag is set to 0, the count is stopped. Do not access the registers associated with AGTW other than the TCSTF flag until this bit is set to 0.

23.4.2 Access to Counter Register

When the TSTART bit and TCSTF flag in the AGTCR register are both 1 (count starts), allow at least 3 cycles of the count source clock between writes when writing to the AGT register successively.

23.4.3 When Changing Mode

The registers associated with AGT operating mode (AGTMR1, AGTMR2, AGTIOC, AGTISR, AGTCMSR and AGTIOC) can be changed only when the count is stopped with both the TSTART bit and TCSTF flag set to 0 (count stops). Do not change these registers during count operation.

When the registers associated with AGT operating mode are changed, the values of TEDGF, TUNDF, TCMAF, and TCMBF flags are undefined. Before starting the count, write 0 to the following flags:

- TEDGF (no active edge received)
- TUNDF (no underflow)
- TCMAF (no match)
- TCMBF (no match).

23.4.4 Output pin setting

When using the AGTWOn, AGTWIOn, AGTWOAn, or AGTWOBn as an output pin, set up the Operation and determine the initial output values. Then set an output mode in the port register.

When using the AGTWIOn as an input pin in pulse width measurement mode or pulse period measurement mode, set up the Operation and start count operation. Then start to enter external events from the AGTWIOn pin. Invalidate the first measurement and validate the second and later completed measurements.

23.3.12 事件信号输出到ELC

AGTWn(n=0 1)使用事件链接控制器(ELC)使用中断请求信号作为事件信号执行到指定模块的链接操作。AGTWn (n=0 1)输出比较匹配A、比较匹配B和下溢测量完成信号作为事件信号。有关详细信息，请参阅第17节，事件链接控制器(ELC)。

23.4 使用说明

23.4.1 计数操作启动和停止控制

●当操作模式（见表23.1）设置为非事件计数器模式，或计数源设置为非AGTWn下溢事件信号（TCK[2:0]=101b）时：

在计数停止期间将1（计数开始）写入AGTCR寄存器中的TSTART位后，AGTCR寄存器中的TCSTF标志在计数源的3个周期内保持为0（计数停止）。在此位设置为1（正在进行计数）之前，不要访问与AGTW相关的寄存器，而不是TCSTF标志。

在计数操作期间将0（计数停止）写入TSTART位后，TCSTF标志在计数源的3个周期内保持为1。当TCSTF标志设置为0时，停止计数。不要访问与AGTW关联的寄存器。除TCSTF标志外，直到该位设置为0。

●当工作模式（见表23.1）设置为事件计数器模式，或计数源设置为AGTW1下溢事件信号（TCK[2:0]=101b）时：

在停止计数时将1（计数开始）写入AGTCR寄存器中的TSTART位后，AGTCR寄存器中的TCSTF标志在2个PCLKB周期内保持为0（计数停止）。在此位设置为1（正在进行计数）之前，不要访问与AGTW相关的寄存器，而不是TCSTF标志。

在计数操作期间将0（计数停止）写入TSTART位后，TCSTF标志保持1持续2
PCLKB周期。当TCSTF标志设置为0时，停止计数。不要访问与相关的寄存器
AGTW不是TCSTF标志，直到该位设置为0。

23.4.2 访问计数器寄存器

当AGTCR寄存器中的TSTART位和TCSTF标志都为1（计数开始）时，连续写入AGT寄存器时，在两次写入之间至少允许计数源时钟的3个周期。

23.4.3 更改模式时

与AGT操作模式相关的寄存器（AGTMR1、AGTMR2、AGTIOC、AGTISR、AGTCMSR和AGTIOC）只有在TSTART位和TCSTF标志都设置为0（计数停止）时停止计数时才能更改。在计数操作期间不要更改这些寄存器。

当与AGT工作模式相关的寄存器发生变化时，TEDGF、TUNDF、TCMAF和
TCMBF标志未定义。在开始计数之前，将0写入以下标志：

●TEDGF（未收到有效边沿）

- TUNDF (no underflow)
- TCMAF (no match)
- TCMBF (no match).

23.4.4 输出引脚设置

使用AGTWOn、AGTWOn、AGTWOAn或AGTWOBn作为输出引脚时，设置操作并确定初始输出值。然后在端口寄存器中设置一个输出模式。

在脉冲宽度测量模式或脉冲周期测量模式下使用AGTWIOn作为输入引脚时，设置
操作并开始计数操作。然后开始从AGTWIOn引脚输入外部事件。使第一次测量无效并验证第二次和以后
完成的测量。

23.4.5 Digital Filter

When using the digital filter, do not start the timer operation for 5 cycles of the digital filter clock after setting TIPF[1:0] bits and when the TEDGSEL bit in the AGTIOC register changes.

23.4.6 How to Calculate Event Number, Pulse Width, and Pulse Period

- In event counter mode, event number is expressed mathematically as follows:
  Event number = initial value of counter [AGT register] - counter value of active event end
- In pulse width measurement mode, pulse width is expressed mathematically as follows:
  Pulse width = counter value of stopping measurement - counter value of next stopping measurement
- In pulse period measurement mode, input pulse period is expressed mathematically as follows:
  Period of input pulse = (initial value of counter [AGT register] - reading value of the read-out buffer) + 1.

23.4.7 When Count is Forcibly Stopped by TSTOP Bit

After the counter is forcibly stopped by the TSTOP bit in the AGTCR register, do not access the following I/O registers for 1 cycle of the count source:

- AGT
- AGTCMA
- AGTCMB
- AGTCR
- AGTMR1
- AGTMR2.

23.4.8 When Selecting AGTW0 Underflow as the Count Source

Operate according to the following procedures described in this section when selecting the underflow event signal as the count source.

(1) Procedure for starting operation

1. Set AGTW.
2. Start the count operation of AGTW1.
3. Start the count operation of AGTW0.

(2) Procedure for stopping operation

1. Stop the count operation of AGTW0.
2. Stop the count operation of AGTW1.
3. Stop the count source clock of AGTW1 (write 000b in the AGTMR1.TCK[2:0] bits).

23.4.9 Module-stop function

AGTW operation can be disabled or enabled using Module Stop Control Register D (MSTPCRD). The AGTW module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes

23.4.10 When Switching Source Clock

When switching a clock source by changing SCKSCR.CKSEL[2:0], the clock output from the selector stops for 4 cycles of the switched clock. Therefore, when using the AGTWIOn, AGTWEEn, or both input as external event input, the clock source should not be switched. If switching the clock source while using the external event input, extend the input pulse width by 4 clock cycles of the switched source clock cycles.

23.4.5 数字滤波器

使用数字滤波器时，在设置TIPF[1:0]位后以及AGTIOC寄存器中的TEDGSEL位发生变化时，在数字滤波器时钟的5个周期内不要启动定时器操作。

23.4.6 如何计算事件编号、脉冲宽度和脉冲周期

●在事件计数器模式下，事件编号以数学方式表示如下：
事件编号=计数器的初始值[AGT寄存器]活动事件结束的计数器值

●在脉冲宽度测量模式下，脉冲宽度以数学方式表示如下：
脉冲宽度=停止测量的计数器值下一个停止测量的计数器值

●在脉冲周期测量模式下，输入脉冲周期的数学表达式如下：
输入脉冲周期=（计数器初始值[AGT寄存器]读出缓冲器的读取值）+1。

23.4.7 当计数被TSTOP位强制停止时

计数器被AGTCR寄存器中的TSTOP位强制停止后，在计数源的1个周期内不要访问以下IO寄存器：

- AGT
- AGTCMA
- AGTCMB
- AGTCR
- AGTMR1
- AGTMR2.

23.4.8 选择AGTW0下溢作为计数源时

选择下溢事件信号作为计数源时，请按照本节所述的以下步骤进行操作。

(1) 开始运行的步骤

1. Set AGTW.

2.启动AGTW1的计数操作。

3.启动AGTW0的计数操作。

(2) 停止运行的步骤

1.停止AGTW0的计数操作。

2.停止AGTW1的计数操作。

3.停止AGTW1的计数源时钟（将000b写入AGTMR1.TCK[2:0]位）。

23.4.9 Module-stop function

可以使用模块停止控制寄存器D(MSTPCRD)禁用或启用AGTW操作。AGTW模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式

23.4.10 切换源时钟时

当通过改变SCKSCR.CKSEL[2:0]来切换时钟源时，选择器的时钟输出在切换时钟的4个周期内停止。因此，当使用AGTWIOn、AGTWEn或两者输入作为外部事件输入时，不应切换时钟源。如果在使用外部事件输入时切换时钟源，请将输入脉冲宽度延长4个切换源时钟周期的时钟周期。

24. Watchdog Timer (WDT)

24.1 Overview

The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.

Table 24.1 lists the WDT specifications and Figure 24.1 shows a block diagram.

Table 24.1 WDT specifications

Parameter	Specifications
Count source*1	Peripheral clock (PCLKB)
Clock division ratio	Division by 4, 64, 128, 512, 2048, or 8192
Counter operation	Counting down using a 14-bit down-counter
Condition for starting the counter	• Auto start mode: Counting automatically starts after a reset or after an underflow or refresh error occurs • Register start mode: Counting is started with a refresh by writing to the WDTRR register • Only secure developer can select Auto-start mode or Register-start mode
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Watchdog timer reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading of the counter value	The down-counter value can be read by the WDTSR register
Event link function (output)	• Down-counter underflow event output • Refresh error event output
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep-mode count stop control output
TrustZone Filter	Security attribution can be set

Note 1. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

24. 看门狗定时器(WDT)

24.1 Overview

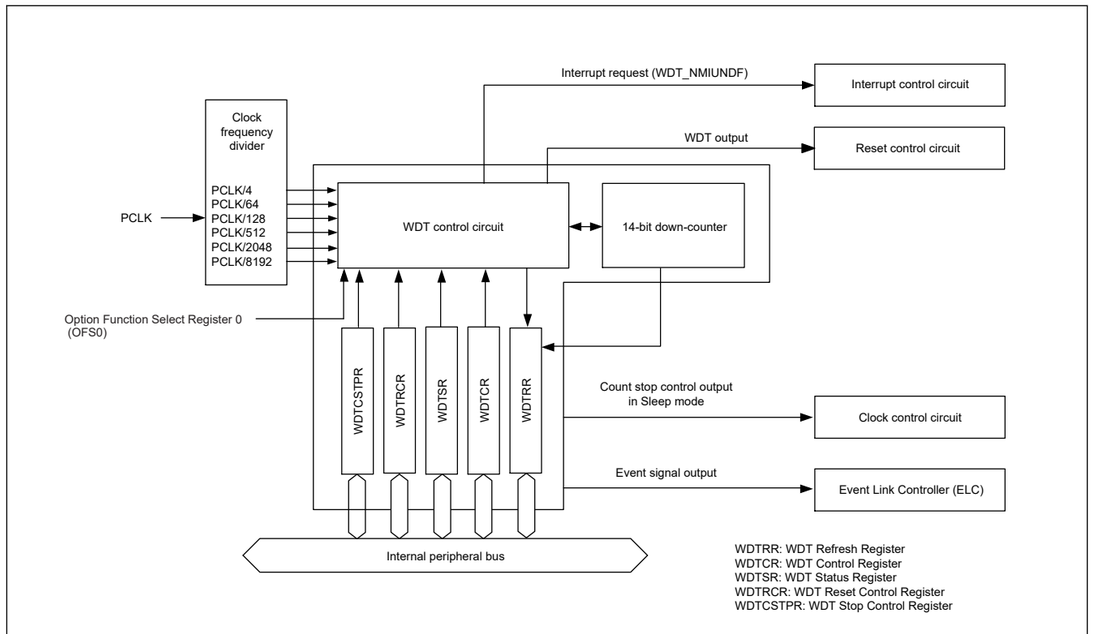
看门狗定时器(WDT)是一个14位递减计数器，可用于在计数器下溢时复位MCU，因为系统已失控且无法刷新WDT。此外，WDT可用于产生不可屏蔽中断或下溢中断。

表24.1列出了WDT规范，图24.1显示了框图。

Table 24.1 WDT specifications

Parameter	Specifications
计数来源*1	外设时钟(PCLKB)
时钟分频比	除以4、64、128、512、2048或8192
计数器操作	使用14位递减计数器进行递减计数
启动计数器的条件	• 自动启动模式：复位后或发生下溢或刷新错误后自动开始计数 • 寄存器启动模式：通过写入WDTRR寄存器以刷新开始计数 • 只有安全的开发人员可以选择自动启动模式或注册启动模式
停止计数器的条件	• 复位（递减计数器和其他寄存器恢复初始值） • 计数器下溢或产生刷新错误
窗口功能	可以指定窗口开始和结束位置（允许刷新和禁止刷新期间）
看门狗定时器复位源	• Down-counter underflows • 刷新允许时间之外的刷新（刷新错误）
Non-maskable interrupt/interrupt sources	• Down-counter underflows • 刷新允许时间之外的刷新（刷新错误）
读取计数器值	递减计数器的值可以通过WDTSR寄存器读取
事件链接功能（输出）	• 递减计数器下溢事件输出 • 刷新错误事件输出
输出信号（内部信号）	• 复位输出 • 中断请求输出 • 休眠模式计数停止控制输出
TrustZone Filter	可设置安全属性

注1.满足外设模块时钟（PCLKB）的频率≥4×（分频后的计数时钟源的频率）。



Note: PCLK = PCLKB

Figure 24.1 WDT block diagram

24.2 Register Descriptions

24.2.1 WDTRR : WDT Refresh Register

Base address: WDT = 0x4008_3400

Offset address: 0x00

Bit position:	7							0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

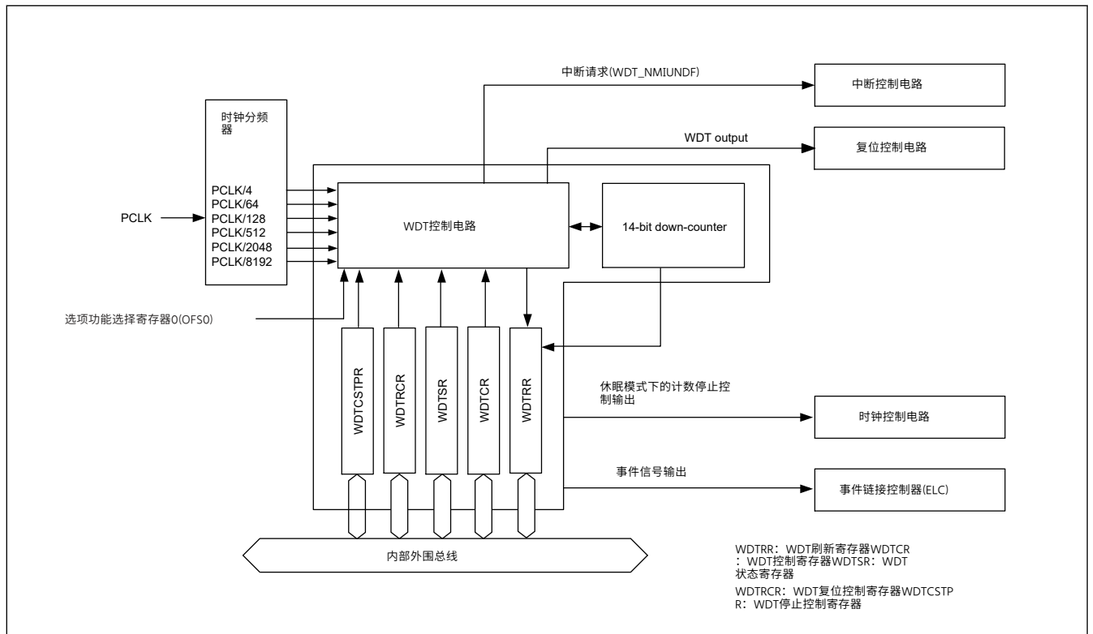
Bit	Symbol	Function	R/W
7:0	n/a	The down-counter is refreshed by writing 0x00 and then writing 0xFF to this register.	R/W

The WDTRR register refreshes the down-counter of the WDT.

The down-counter of the WDT is refreshed by writing 0x00 and then writing 0xFF to WDTRR register (refresh operation) within the refresh-permitted period.

After the down-counter is refreshed, it starts counting down from the value selected by setting the WDT Timeout Period Select bits (OFS0.WDTTOPS[1:0]) in the Option Function Select Register 0 in auto start mode. In register start mode, counting down starts from the value selected by setting the Timeout Period Select bits (WDTCR.TOPS[1:0]) in the WDT Control Register.

When 0x00 is written, the read value is 0x00. When a value other than 0x00 is written, the read value is 0xFF. For details of the refresh operation, see section 24.3.3. Refresh Operation.



Note: PCLK = PCLKB

Figure 24.1 看门狗框图

24.2 注册说明

24.2.1 WDTRR:WDT刷新寄存器

Base address: WDT = 0x4008_3400

Offset address: 0x00

Bit position:	7							0
Bit field:								
重置后的值：	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	通过写入0x00然后将0xFF写入该寄存器来刷新递减计数器。	R/W

WDTRR寄存器刷新WDT的递减计数器。

WDT的递减计数器通过在允许刷新期间内写入0x00然后将0xFF写入WDTRR寄存器（刷新操作）来刷新。

递减计数器刷新后，在自动启动模式下，它从通过设置选项功能选择寄存器0中的WDT超时周期选择位(OFS0.WDTTOPS[1:0])选择的值开始递减计数。在寄存器启动模式下，倒计时从通过设置WDT控制寄存器中的超时周期选择位(WDTCR.TOPS[1:0])选择的值开始。

写入0x00时，读取值为0x00。写入0x00以外的值时，读取的值为0xFF。有关刷新操作的详细信息，请参阅第24.3.3节。刷新操作。

24.2.2 WDTCR : WDT Control Register

Base address: WDT = 0x4008_3400

Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
Value after reset:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Function	R/W
1:0	TOPS[1:0]	Timeout Period Select 0 0: 1024 cycles (0x03FF) 0 1: 4096 cycles (0x0FFF) 1 0: 8192 cycles (0x1FFF) 1 1: 16384 cycles (0x3FFF)	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
7:4	CKS[3:0]	Clock Division Ratio Select 0x1: PCLKB/4 0x4: PCLKB/64 0xF: PCLKB/128 0x6: PCLKB/512 0x7: PCLKB/2048 0x8: PCLKB/8192 Others: Setting prohibited	R/W
9:8	RPES[1:0]	Window End Position Select 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (do not specify window end position).	R/W
11:10	—	These bits are read as 0. The write value should be 0.	R/W
13:12	RPSS[1:0]	Window Start Position Select 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (do not specify window start position).	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

The WDTCR register is used to set the clock division ratio, and window start and end positions for refresh, and the timeout period until the down-counter underflows in register start mode.

Some constraints apply to writes to the WDTCR register. For details, see section 24.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the settings in the WDTCR register are disabled, and the settings in the Option Function Select Register 0 (OFS0) are enabled. The settings for the WDTCR register can also be made in the OFS0 register. For details, see section 24.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

TOPS[1:0] bits (Timeout Period Select)

The TOPS[1:0] bits select the timeout period, the period until the down-counter underflows, from 1024, 4096, 8192, and 16384 cycles, taking the divided clock specified in the CKS[3:0] bits as 1 cycle. After the down-counter is refreshed, the combination of the CKS[3:0] and TOPS[1:0] bits determines the number of PCLKB cycles until the counter underflows.

Table 24.2 lists the relationship between the CKS[3:0] and TOPS[1:0] bit settings, the timeout period, and the number of PCLKB cycles.

24.2.2 WDTCR:WDT控制寄存器

Base address: WDT = 0x4008_3400

Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
重置后的值：	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Function	R/W
1:0	TOPS[1:0]	超时时间选择 0 0: 1024 cycles (0x03FF) 0 1: 4096 cycles (0x0FFF) 1 0: 8192 cycles (0x1FFF) 1 1: 16384 cycles (0x3FFF)	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
7:4	CKS[3:0]	时钟分频比选择 0x1: PCLKB/4 0x4: PCLKB/64 0xF: PCLKB/128 0x6: PCLKB/512 0x7: PCLKB/2048 0x8: PCLKB/8192 其他：禁止设置	R/W
9:8	RPES[1:0]	窗口结束位置选择 00：75%01：50%10：25%11：0%（不指定 窗口结束位置）。	R/W
11:10	—	这些位被读取为0。写入值应为0。	R/W
13:12	RPSS[1:0]	窗口起始位置选择 00：25%01：50%10：75%11：100%（不指定 窗口起始位置）。	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W

WDTCR寄存器用于设置时钟分频比、刷新的窗口开始和结束位置，以及在寄存器开始模式下直到递减计数器下溢的超时时间。

一些限制适用于写入WDTCR寄存器。详见24.3.2节。控制对WDTCR的写入，WDTRCR和WDTCSTPR寄存器。

在自动启动模式下，禁用WDTCR寄存器中的设置，启用选项功能选择寄存器0(OFS0)中的设置。WDTCR寄存器的设置也可以在OFS0寄存器中进行。详见24.3.8节。选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

TOPS[1:0]位（超时周期选择）

TOPS[1:0]位从1024、4096、8192和16384个周期中选择超时周期，即递减计数器下溢之前的周期，将CKS[3:0]位中指定的分频时钟作为1个周期.向下计数器刷新后，CKS[3:0]和TOPS[1:0]位的组合决定了PCLKB周期数，直到计数器下溢。

表24.2列出了CKS[3:0]和TOPS[1:0]位设置、超时时间和
PCLKB cycles.

Table 24.2 Timeout period settings

CKS[3:0] bits	TOPS[1:0] bits	Clock division ratio	Timeout period (number of cycles)	PCLKB clock cycles
0x1	00b	PCLKB/4	1024	4096
	01b		4096	16384
	10b		8192	32768
	11b		16384	65536
0x4	00b	PCLKB/64	1024	65536
	01b		4096	262144
	10b		8192	524288
	11b		16384	1048576
0xF	00b	PCLKB/128	1024	131072
	01b		4096	524288
	10b		8192	1048576
	11b		16384	2097152
0x6	00b	PCLKB/512	1024	524288
	01b		4096	2097152
	10b		8192	4194304
	11b		16384	8388608
0x7	00b	PCLKB/2048	1024	2097152
	01b		4096	8388608
	10b		8192	16777216
	11b		16384	33554432
0x8	00b	PCLKB/8192	1024	8388608
	01b		4096	33554432
	10b		8192	67108864
	11b		16384	134217728

CKS[3:0] bits (Clock Division Ratio Select)

The CKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the PCLKB divided by 4, 64, 128, 512, 2048, and 8192. Combined with the TOPS[1:0] bit setting, this allows the WDT to be configured to a count period between 4096 and 134217728 PCLKB clock cycles.

RPES[1:0] bits (Window End Position Select)

The RPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. Set the window end position to a value less than the value for the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is enabled.

RPSS[1:0] bits (Window Start Position Select)

The RPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window start position. Set the window start position to a value greater than the value for the window end position. If the window start position is set to a value less than or equal to the window end position, the window end position is set to 0%.

Table 24.3 lists the counter values for the window start and end positions, and Figure 24.2 shows the refresh-permitted period set in the RPSS[1:0], RPES[1:0], and TOPS[1:0] bits.

Table 24.2 超时时间设置

CKS[3:0] bits	TOPS[1:0] bits	时钟分频比	超时时间（周期数）	PCLKB时钟周期
0x1	00b	PCLKB/4	1024	4096
	01b		4096	16384
	10b		8192	32768
	11b		16384	65536
0x4	00b	PCLKB/64	1024	65536
	01b		4096	262144
	10b		8192	524288
	11b		16384	1048576
0xF	00b	PCLKB/128	1024	131072
	01b		4096	524288
	10b		8192	1048576
	11b		16384	2097152
0x6	00b	PCLKB/512	1024	524288
	01b		4096	2097152
	10b		8192	4194304
	11b		16384	8388608
0x7	00b	PCLKB/2048	1024	2097152
	01b		4096	8388608
	10b		8192	16777216
	11b		16384	33554432
0x8	00b	PCLKB/8192	1024	8388608
	01b		4096	33554432
	10b		8192	67108864
	11b		16384	134217728

CKS[3:0]位（时钟分频比选择）

CKS[3:0]位指定用于递减计数器的时钟的分频比。分频比可以从PCLKB除以4、64、128、512、2048和8192中选择。结合TOPS[1:0]位设置，这允许将WDT配置为4096和134217728个PCLKB时钟周期。

RPES[1:0]位（窗口结束位置选择）

RPES[1:0]位指定指示刷新允许周期的窗口结束位置。可以为窗口结束位置选择75%、50%、25%或0%的超时时间。将窗口结束位置设置为小于窗口起始位置的值（窗口起始位置>窗口结束位置）。如果窗口结束位置大于窗口起始位置，则仅启用窗口起始位置设置。

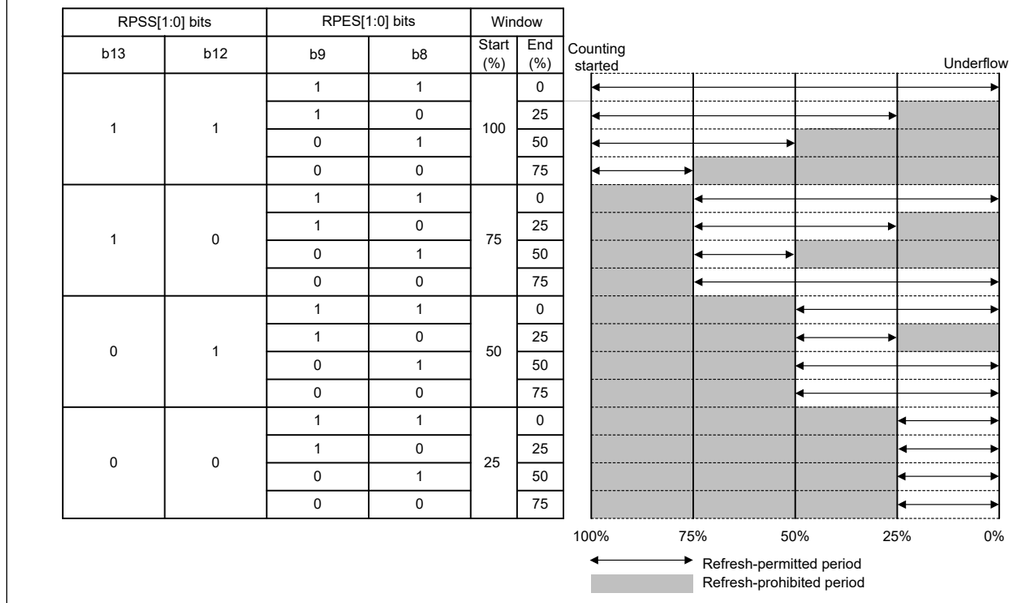
RPSS[1:0]位（窗口起始位置选择）

RPSS[1:0]位指定指示允许刷新周期的窗口起始位置。窗口起始位置可选择100%、75%、50%或25%的超时时间。将窗口开始位置设置为大于窗口结束位置的值。如果窗口开始位置设置为小于或等于窗口结束位置的值，则窗口结束位置设置为0%。

表24.3列出了窗口开始和结束位置的计数器值，图24.2显示了在RPSS[1:0]、RPES[1:0]和TOPS[1:0]位中设置的允许刷新周期。

Table 24.3 Relationship between the timeout period and window start and end counter values

TOPS[1:0]	Timeout period		Window start and end counter value			
	Cycles	Counter value	100%	75%	50%	25%
00b	1024	0x03FF	0x03FF	0x02FF	0x01FF	0x00FF
01b	4096	0x0FFF	0x0FFF	0x0BFF	0x07FF	0x03FF
10b	8192	0x1FFF	0x1FFF	0x17FF	0x0FFF	0x07FF
11b	16384	0x3FFF	0x3FFF	0x2FFF	0x1FFF	0x0FFF



Note: If window end setting ≥ window start setting, the window end setting is set to 0%.

Figure 24.2 RPSS[1:0] and RPES[1:0] bits setting and refresh-permitted period

24.2.3 WDTSR : WDT Status Register

Base address: WDT = 0x4008_3400

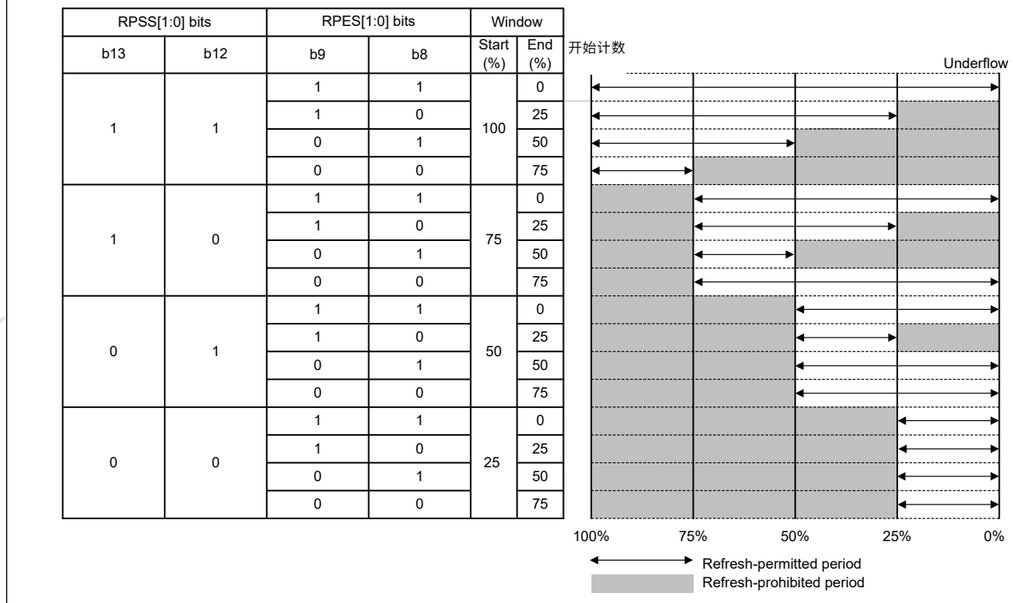
Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	REFEF	UNDF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CNTVAL[13:0]	Down-Counter Value Value counted by the down-counter	R
14	UNDFF	Underflow Flag 0: No underflow occurred 1: Underflow occurred	R/W*1

Table 24.3 超时时间与窗口开始和结束计数器值之间的关系

TOPS[1:0]	超时时间		窗口开始和结束计数器值			
	Cycles	计数器值	100%	75%	50%	25%
00b	1024	0x03FF	0x03FF	0x02FF	0x01FF	0x00FF
01b	4096	0x0FFF	0x0FFF	0x0BFF	0x07FF	0x03FF
10b	8192	0x1FFF	0x1FFF	0x17FF	0x0FFF	0x07FF
11b	16384	0x3FFF	0x3FFF	0x2FFF	0x1FFF	0x0FFF



Note: 如果窗口结束设置≥窗口开始设置，则窗口结束设置设置为0%。

Figure 24.2 RPSS[1:0]和RPES[1:0]位设置和允许刷新周期

24.2.3 WDTSR:WDT状态寄存器

Base address: WDT = 0x4008_3400

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	REFEF	UNDF	CNTVAL[13:0]													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CNTVAL[13:0]	Down-Counter Value 递减计数器计数的值	R
14	UNDFF	Underflow Flag 0：未发生下溢1：发生下溢	R/W*1

Bit	Symbol	Function	R/W
15	REFEF	Refresh Error Flag 0: No refresh error occurred 1: Refresh error occurred	R/W*1

Note 1. Only 0 can be written to clear the flag.

The WDTSR register indicates the counter value of the down-counter and the status of whether an underflow or refresh error occurred in the down-counter.

CNTVAL[13:0] bits (Down-Counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the counter. A value of 1 indicates that the down counter underflowed. Write 0 to the flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N+1) PCLKB cycles. In addition, clearing of the flag is ignored for (N+1) PCLKB cycles after an underflow. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0x1, N = 4
- When WDTCR.CKS[3:0] = 0x4, N = 64
- When WDTCR.CKS[3:0] = 0xF, N = 128
- When WDTCR.CKS[3:0] = 0x6, N = 512
- When WDTCR.CKS[3:0] = 0x7, N = 2048
- When WDTCR.CKS[3:0] = 0x8, N = 8192

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred, indicating that a refresh operation was performed during a prohibited period. A value of 1 indicates that a refresh error occurred. Write 0 to the flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N+1) PCLKB cycles. In addition, clearing of the flag is ignored for (N+1) PCLKB cycles after a refresh error. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0x1, N = 4
- When WDTCR.CKS[3:0] = 0x4, N = 64
- When WDTCR.CKS[3:0] = 0xF, N = 128
- When WDTCR.CKS[3:0] = 0x6, N = 512
- When WDTCR.CKS[3:0] = 0x7, N = 2048
- When WDTCR.CKS[3:0] = 0x8, N = 8192

24.2.4 WDTRCR : WDT Reset Control Register

Base address: WDT = 0x4008_3400

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RSTIRQS	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
15	REFEF	刷新错误标志 0：未发生刷新错误1：发生刷新错误	R/W*1

注1.只能写入0来清除标志。

WDTSR寄存器指示递减计数器的计数值以及递减计数器是否发生下溢或刷新错误的状态。

CNTVAL[13:0] bits (Down-Counter Value)

读取CNTVAL[13:0]位以确认递减计数器的值。读取的值可能与实际计数相差1。

UNDFF flag (Underflow Flag)

读取UNDFF标志以确认计数器是否发生下溢。值1表示递减计数器下溢。将0写入标志以将值设置为0。写入1无效。

清除UNDFF标志需要(N+1)个PCLKB周期。此外，在下溢后的(N+1)个PCLKB周期内忽略标志的清除。N在WDTCR.CKS[3:0]位中指定如下：

- When WDTCR.CKS[3:0] = 0x1, N = 4
- When WDTCR.CKS[3:0] = 0x4, N = 64
- When WDTCR.CKS[3:0] = 0xF, N = 128
- When WDTCR.CKS[3:0] = 0x6, N = 512
- When WDTCR.CKS[3:0] = 0x7, N = 2048
- When WDTCR.CKS[3:0] = 0x8, N = 8192

REFEF标志（刷新错误标志）

读取REFEF标志，确认是否发生刷新错误，表示在禁止期间进行了刷新操作。值1表示发生了刷新错误。将0写入标志以将值设置为0。写入1无效。

清除REFEF标志需要(N+1)个PCLKB周期。此外，在刷新错误后的(N+1)个PCLKB周期内，标志的清除将被忽略。N在WDTCR.CKS[3:0]位中指定如下：

- When WDTCR.CKS[3:0] = 0x1, N = 4
- When WDTCR.CKS[3:0] = 0x4, N = 64
- When WDTCR.CKS[3:0] = 0xF, N = 128
- When WDTCR.CKS[3:0] = 0x6, N = 512
- When WDTCR.CKS[3:0] = 0x7, N = 2048
- When WDTCR.CKS[3:0] = 0x8, N = 8192

24.2.4 WDTRCR:WDT复位控制寄存器

Base address: WDT = 0x4008_3400

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RSTIRQS	—	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
7	RSTIRQS	Reset Interrupt Request Select 0: Enable non-maskable interrupt request or interrupt request output 1: Enable reset output	R/W

The WDTRCR register controls reset output by a WDT down-counter underflow or interrupt request output.

Some constraints apply to writes to the WDTRCR register. For details, see section 24.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTRCR register settings are disabled, and the settings in the Option Function Select register 0 (OFS0) are enabled. The settings for the WDTRCR register can also be made for the OFS0 register. For details, see section 24.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

24.2.5 WDTCSTPR : WDT Count Stop Control Register

Base address: WDT = 0x4008_3400

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SLCSTP	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	SLCSTP	WDT Count Stop Control Register 0: Disable count stop 1: Stop count on transition to Sleep mode	R/W

The WDTCSTPR register controls whether to stop the WDT counter in a low power mode. Some constraints apply to writes to the WDTCSTPR register. For details, see section 24.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTCSTPR register settings are disabled, and the settings in the Option Function Select register 0 (OFS0) are enabled. The settings for the WDTCSTPR register can also be made for the OFS0 register. For details, see section 24.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

SLCSTP bit (WDT Count Stop Control Register)

The SLCSTP bit selects whether to stop counting on transition to Sleep mode, Snooze, or Software Standby mode.

24.2.6 Option Function Select Register 0 (OFS0)

For information on the OFS0 register, see section 24.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

24.3 Operation

24.3.1 Count Operation in each Start Mode

The WDT has two start modes:

- Auto start mode, in which counting automatically starts after a release from the reset state
- Register start mode, in which counting starts with a refresh by writing to the register.

In auto start mode, counting automatically starts after a release from the reset state according to the settings in the Option Function Select register 0 (OFS0) in the flash.

In register start mode, counting starts with a refresh by writing to the WDTRR register after the respective registers are set after a a release from the reset state.

Bit	Symbol	Function	R/W
7	RSTIRQS	复位中断请求选择 0：使能不可屏蔽中断请求或中断请求输出1：使能复位输出	R/W

WDTRCR寄存器通过WDT递减计数器下溢或中断请求输出控制复位输出。

一些限制适用于写入WDTRCR寄存器。详见24.3.2节。控制写入WDTCR、WDTRCR和WDTCSTPR寄存器。

在自动启动模式下，WDTRCR寄存器设置被禁用，而选项功能选择寄存器0(OFS0)中的设置被启用。WDTRCR寄存器的设置也可以对OFS0寄存器进行。详见24.3.8节。选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

24.2.5 WDTCSTPR:WDT计数停止控制寄存器

Base address: WDT = 0x4008_3400

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SLCSTP	—	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	这些位被读取为0。写入值应为0。	R/W
7	SLCSTP	WDT计数停止控制寄存器 0：禁用计数停止1：转换到睡眠模式时停止计数	R/W

WDTCSTPR寄存器控制是否在低功耗模式下停止WDT计数器。一些限制适用于写入WDTCSTPR寄存器。详见24.3.2节。控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入。

在自动启动模式下，WDTCSTPR寄存器设置被禁用，而选项功能选择寄存器0(OFS0)中的设置被启用。也可以对OFS0寄存器进行WDTCSTPR寄存器的设置。详见24.3.8节。选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

SLCSTP位（WDT计数停止控制寄存器）

SLCSTP位选择在转换到休眠模式、贪睡或软件待机模式时是否停止计数。

24.2.6 选项功能选择寄存器0(OFS0)

有关OFS0寄存器的信息，请参见第24.3.8节。选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

24.3 Operation

24.3.1 每种启动模式下的计数操作

WDT有两种启动模式：

●自动启动模式，从复位状态释放后自动开始计数

●寄存器启动模式，通过写入寄存器，从刷新开始计数。

在自动启动模式下，根据选项中的设置从复位状态释放后自动开始计数
功能选择闪存中的寄存器0(OFS0)。

在寄存器启动模式下，在从复位状态释放后，在设置各个寄存器后，通过写入WDTRR寄存器，从刷新开始计数。

Select auto start mode or register start mode by setting the WDT Start Mode Select bit (OFS0.WDTSTRT) in the OFS0 register.

When the auto start mode is selected, the settings in the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled while the settings in the OFS0 register are enabled.

When the register start mode is selected, the setting for the OFS0 register is disabled while the settings for the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

24.3.1.1 Register start mode

When the WDT Start Mode Select bit (OFS0.WDTSTRT) is 1, register start mode is selected and the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

After the reset state is released, set the following to Sleep mode in the WDTCSTPR register:

- Clock division ratio
- Window start and end positions
- Timeout period in the WDTCR register
- Reset output or interrupt request output in the WDTRCR register
- Counter stop control during transitions to Sleep mode in the WDTCSTPR register

Refresh the down-counter to start counting down from the value set in the Timeout Period Selection bits (WDTCR.TOPS[1:0]).

Thereafter, as long as the counter is refreshed in the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and counting down continues. The WDT does not output the reset signal as long as counting continues. However, if the down-counter underflows because the down-counter cannot be refreshed due to a program runaway, or if a refresh error occurs because the counter was refreshed outside the refresh-permitted period, the WDT outputs the reset signal or a non-maskable interrupt request/interrupt request (WDT_NMIUNDF). Reset output or interrupt request output can be selected in the WDT Reset Interrupt Request Select bit (WDTRCR.RSTIRQS). Non-maskable interrupt requests or interrupt requests can be selected in the WDT Underflow/Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 24.3 shows an example of operation under the following conditions:

- Register start mode (OFS0.WDTSTRT = 1)
- Reset output is enabled (WDTRCR.RSTIRQS = 1)
- The window start position is 75% (WDTCR.RPSS[1:0] = 10b)
- The window end position is 25% (WDTCR.RPES[1:0] = 10b)

通过设置OFS0寄存器中的WDT启动模式选择位(OFS0.WDTSTRT)来选择自动启动模式或寄存器启动模式。

选择自动启动模式后，WDT控制寄存器（WDTCR）中的设置，WDTRESET控制寄存器（WDTRCR）和WDT计数停止控制寄存器（WDTCSTPR）在启用OFS0寄存器中的设置时被禁用。

选择寄存器启动模式时，在WDT控件的设置时禁用OFS0寄存器的设置
使能寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)和WDT计数停止控制寄存器(WDTCSTPR)。

24.3.1.1 注册启动模式

当WDT启动模式选择位(OFS0.WDTSTRT)为1时，选择寄存器启动模式并启用WDT控制寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)和WDT计数停止控制寄存器(WDTCSTPR)。

释放复位状态后，在WDTCSTPR寄存器中将以下内容设置为休眠模式：

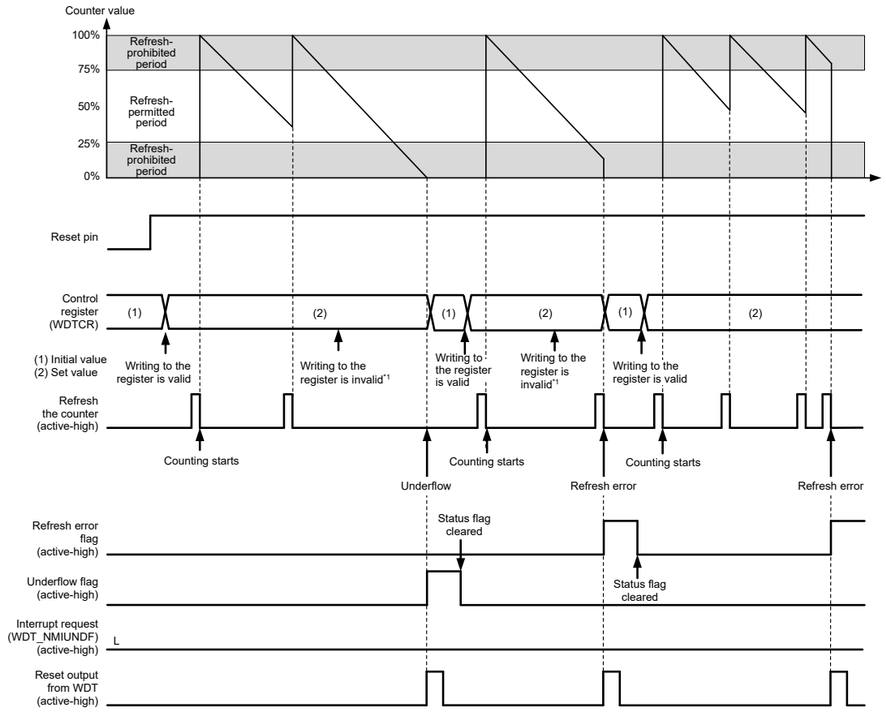
- ●时钟分频比
- ●窗口开始和结束位置
- ●WDTCR寄存器中的超时时间
- ●WDTRCR寄存器中的复位输出或中断请求输出
- ●WDTCSTPR寄存器中转换到休眠模式期间的计数器停止控制

刷新递减计数器以从超时周期选择位(WDTCR.TOPS[1:0])中设置的值开始递减计数。

此后，只要在可刷新期间刷新了计数器，则每次刷新计数器时都会重置计数器中的值，并继续递减计数。只要继续计数，WDT就不会输出复位信号。但是，如果由于程序失控导致递减计数器无法刷新而导致递减计数器下溢，或者由于计数器在刷新允许时间之外刷新而发生刷新错误，则WDT输出复位信号或非可屏蔽中断请求中断请求(WDT_NMIUNDF)。可以在WDT复位中断请求选择位(WDTRCR.RSTIRQS)中选择复位输出或中断请求输出。可以在WDT下溢刷新错误中断 允许位(NMIER.WDTEN)中选择不可屏蔽的中断请求或中断请求。

图24.3显示了以下条件下的操作示例：

- ●寄存器启动模式（OFS0.WDSTSTRT=1）
- ●启用复位输出(WDTRCR.RSTIRQS=1)
- ●窗口起始位置为75%(WDTCR.RPSS[1:0]=10b)
- ●窗口结束位置为25%(WDTCR.RPES[1:0]=10b)



Note: See section 24.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.
Reset pin = RES

Figure 24.3 Operation example in register start mode

24.3.1.2 Auto start mode

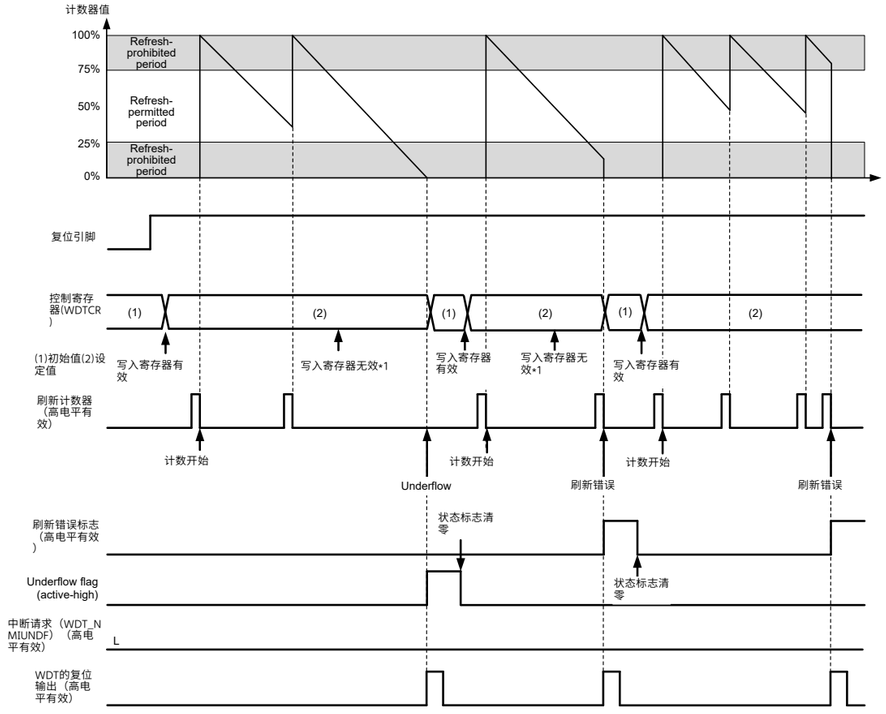
When the WDT Start Mode Select bit (OFS0.WDTSTRT) in the Option Function Select Register 0 (OFS0) is 0, auto start mode is selected, the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled, and the settings in the OFS0 register are enabled.

Within the reset state, the setting values for the following in the Option Function Select Register 0 (OFS0) are set in the WDT registers:

- Clock division ratio
- Window start and end positions
- Timeout period
- Reset output or interrupt request
- Counter stop control during transition to Sleep mode

When the reset state is released, the down-counter automatically starts counting down from the value set in the WDT Timeout Period Select bits (OFS0.WDTTOPS[1:0]).

Thereafter, as long as the counter is refreshed in the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and counting down continues. The WDT does not output the reset signal as long as the counting continues. However, if the down-counter underflows because refreshing of the down-counter is not possible due to a



Note: 请参阅第24.3.2节。控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入。
复位引脚=RES

Figure 24.3 寄存器启动模式下的操作示例

24.3.1.2 自动启动模式

当WDT启动模式选择位置（OFS0.WDTSTSTRT）中的选项功能选择寄存器0（OFS0）为0时，选择了自动启动模式，WDT控制寄存器（WDTCR）（WDTCR），WDTRESETRESETCONTROMCONTROL寄存器（WDTRCR）和WDTCountCountCountCountCount停止控制寄存器(WDTCSTPR)被禁用，而OFS0寄存器中的设置被启用。

在复位状态下，选项功能选择寄存器0(OFS0)中的以下设置值在
WDT registers:

- ●时钟分频比
- ●窗口开始和结束位置
- ●超时时间
- ●复位输出或中断请求
- ●转换到睡眠模式期间的计数器停止控制

当复位状态解除时，递减计数器自动从WDT中设置的值开始递减计数
超时周期选择位(OFS0.WDTTOPS[1:0])。

此后，只要在可刷新期间刷新了计数器，则每次刷新计数器时都会重置计数器中的值，并继续递减计数。只要继续计数，WDT就不会输出复位信号。但是，如果递减计数器下溢，因为递减计数器的刷新是不可能的，因为

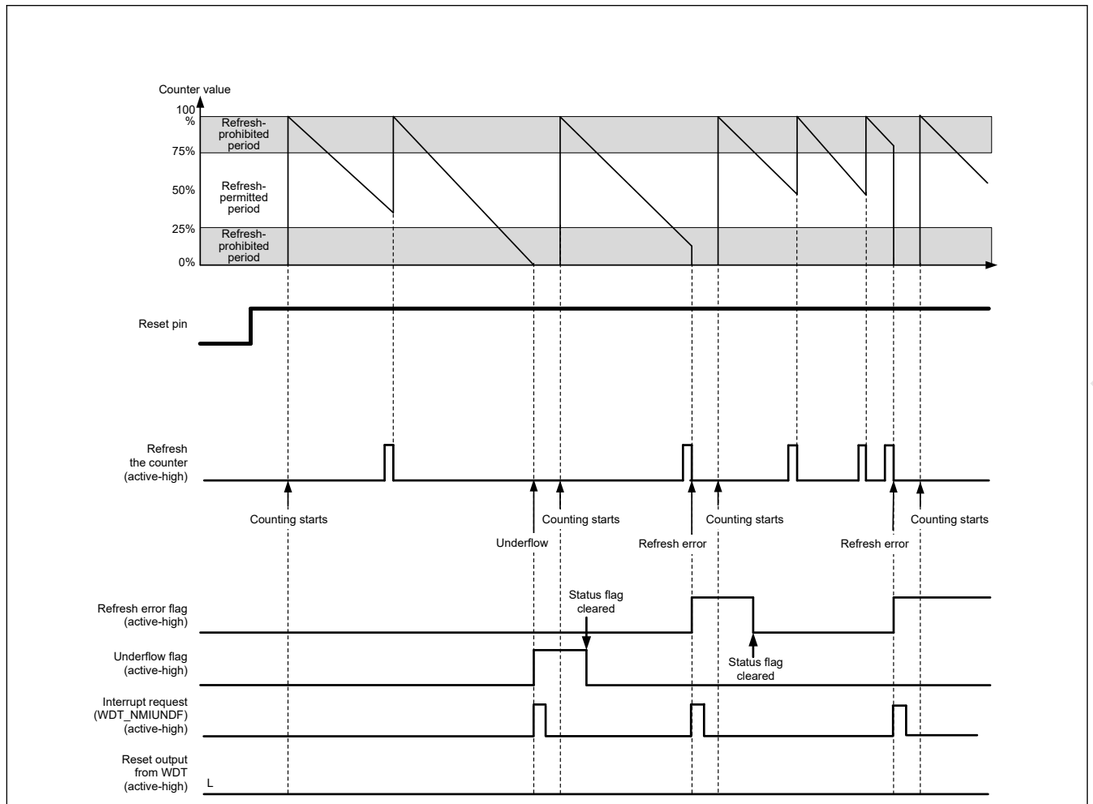
runaway program or if a refresh error occurs due to refreshing outside the refresh-permitted period, the WDT outputs the reset signal or non-maskable interrupt request/interrupt request (WDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle. The value of the timeout period is set in the down-counter and counting restarts.

Reset output or interrupt request output can be selected by setting the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS). Non-maskable interrupt request or interrupt request can be selected in the WDT Underflow/ Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 24.4 shows an example of operation (non-maskable interrupt) under the following conditions:

- Auto start mode (OFS0.WDTSTRT = 0)
- Non-maskable interrupt request output is enabled (OFS0.WDTRSTIRQS = 0)
- The window start position is 75% (OFS0.WDTRPSS[1:0] = 10b)
- The window end position is 25% (OFS0.WDTRPES[1:0] = 10b)



Note: Reset pin = RES

Figure 24.4 Operation example in auto start mode

24.3.2 Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers

Writing to the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), or WDT Count Stop Control Register (WDTCSTPR) is possible once between the release from the reset state and the first refresh operation.

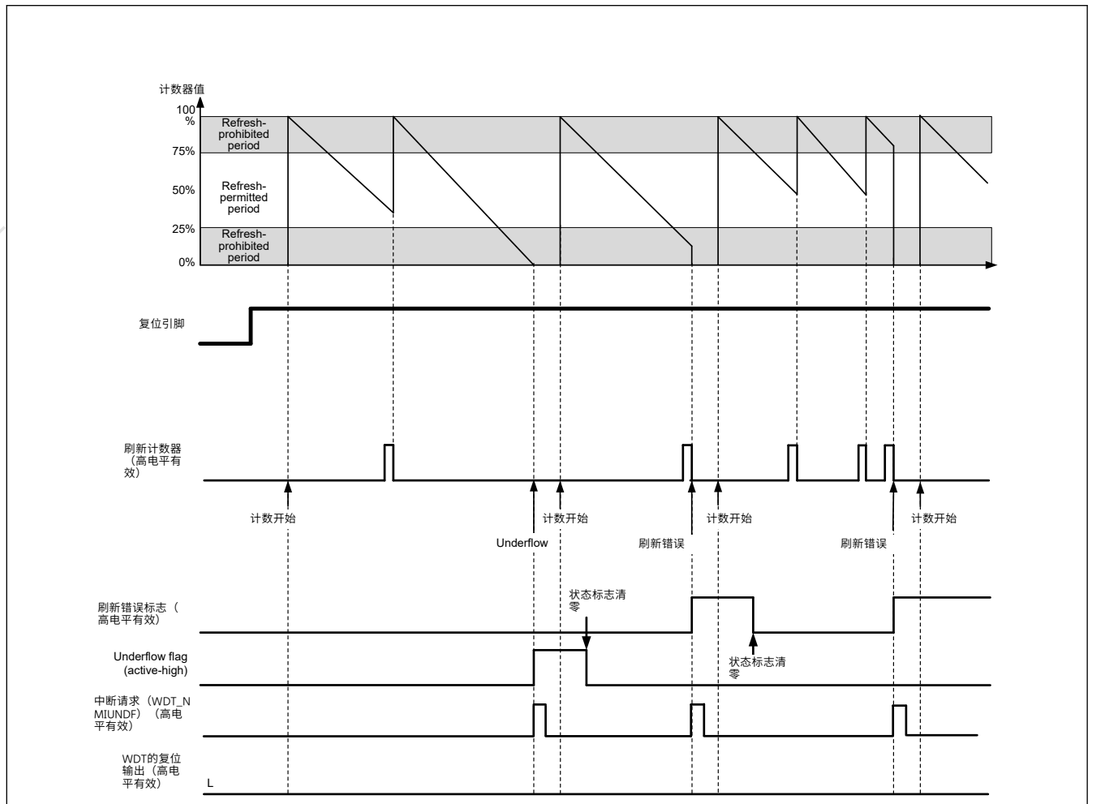
如果程序失控或由于刷新允许刷新期间之外发生刷新错误，则WDT输出复位信号或不可屏蔽中断请求中断请求(WDT_NMIUNDF)。

复位信号或不可屏蔽中断请求中断请求产生后，计数器在计数1个周期后重新加载超时周期。超时时间的值在递减计数器中设置并重新开始计数。

通过设置WDT复位中断请求选择位(OFS0.WDTRSTIRQS)可以选择复位输出或中断请求输出。可以在WDT下溢刷新错误中断 允许位(NMIER.WDTEN)中选择不可屏蔽的中断请求或中断请求。

图24.4显示了以下条件下的操作示例（不可屏蔽中断）：

- ●自动启动模式（OFS0.WDTSTRT=0）
- ●使能不可屏蔽中断请求输出（OFS0.WDTRSTIRQS=0）
- ●窗口起始位置为75%(OFS0.WDTRPSS[1:0]=10b)
- ●窗口结束位置为25%(OFS0.WDTRPES[1:0]=10b)



Note: 复位引脚=RES

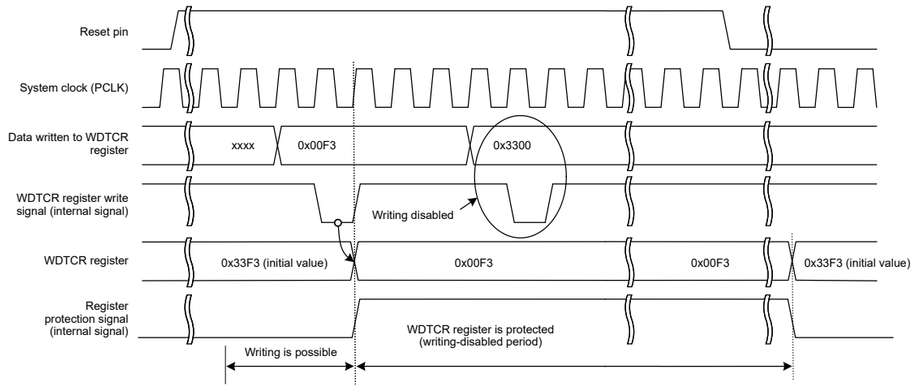
Figure 24.4 自动启动模式下的操作示例

24.3.2 控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入

写入WDT控制寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)或WDT计数停止控制在从复位状态释放到第一次刷新操作之间，寄存器(WDTCSTPR)是可能的。

After a refresh (counting starts) or a write to WDTCR, WDTRCR or WDTCSTPR register, the protection signal in the WDT becomes 1 to protect WDTCR, WDTRCR and WDTCSTPR register against subsequent write attempts. This protection is released by the reset source of the WDT. With other reset sources, the protection is not released.

Figure 24.5 shows control waveforms produced in response to writing to the WDTCR.



Note: PCLK = PCLKB
Reset pin = RES

Figure 24.5 Control waveforms produced in response to writes to the WDTCR register

24.3.3 Refresh Operation

The down-counter is refreshed and starts counting operation on a write of the values 0x00 and 0xFF to the WDT Refresh Register (WDTRR). If a value other than 0xFF is written after 0x00, the down-counter is not refreshed. If an invalid value is written, correct refreshing resumes on a write of 0x00 and 0xFF to the WDTRR register.

Correct refreshing is also performed when a register other than WDTRR is accessed or WDTRR is read between writing 0x00 and writing 0xFF to WDTRR. Writes to refresh the counter must be made within the refresh-permitted period, and this is determined by the 0xFF write. For this reason, correct refreshing is performed even when 0x00 is written outside the refresh-permitted period.

[Example write sequences that are valid for refreshing the counter]

- 0x00 → 0xFF
- 0x00 ((n–1)th time) → 0x00 (nth time) → 0xFF
- 0x00 → access to another register or read from WDTRR → 0xFF

[Example write sequences that are invalid for refreshing the counter]

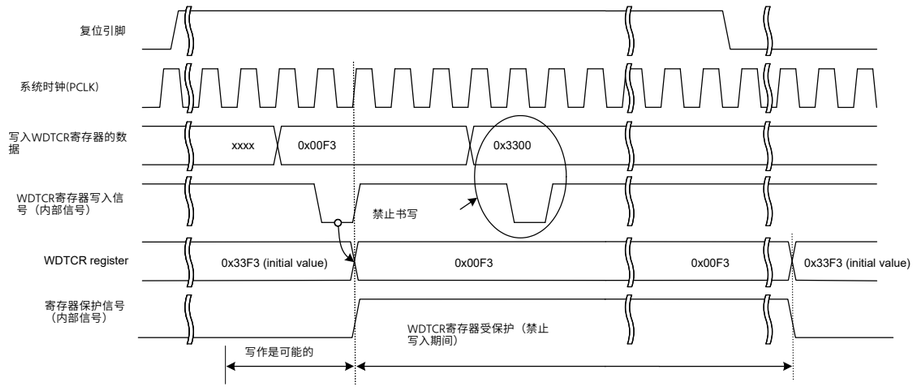
- 0x23 (a value other than 0x00) → 0xFF
- 0x00 → 0x54 (a value other than 0xFF)
- 0x00 → 0xAA (0x00 and a value other than 0xFF) → 0xFF

After 0xFF is written to the WDT Refresh Register (WDTRR), refreshing the down-counter requires up to 4 cycles of the signal for counting. To meet this requirement, complete writing 0xFF to WDTRR 4 count cycles before the down-counter underflows.

Figure 24.6 shows the WDT refresh-operation waveforms when the clock division ratio is PCLKB/64.

在刷新（计数开始）或写入WDTCR、WDTRCR或WDTCSTPR寄存器后，WDT变为1以保护WDTCR、WDTRCR和WDTCSTPR寄存器免受后续写入尝试。该保护由WDT的复位源解除。使用其他复位源时，不会解除保护。

图24.5显示了响应写入WDTCR产生的控制波形。



Note: PCLK=PCLKB复位引脚=RES

Figure 24.5 响应写入WDTCR寄存器而产生的控制波形

24.3.3 刷新操作

向下计数器刷新并在将值0x00和0xFF写入WDT刷新时开始计数操作寄存器(WDTRR)。如果在0x00之后写入0xFF以外的值，则不刷新递减计数器。如果写入无效值，则在向WDTRR寄存器写入0x00和0xFF时会恢复正确刷新。

在写入0x00和写入0xFF到WDTRR之间访问WDTRR以外的寄存器或读取WDTRR时，也会执行正确刷新。刷新计数器的写入必须在允许刷新的周期内进行，这由0xFF写入决定。因此，即使在可刷新期间外写入0x00，也会执行正确的刷新。

[对刷新计数器有效的示例写入序列]

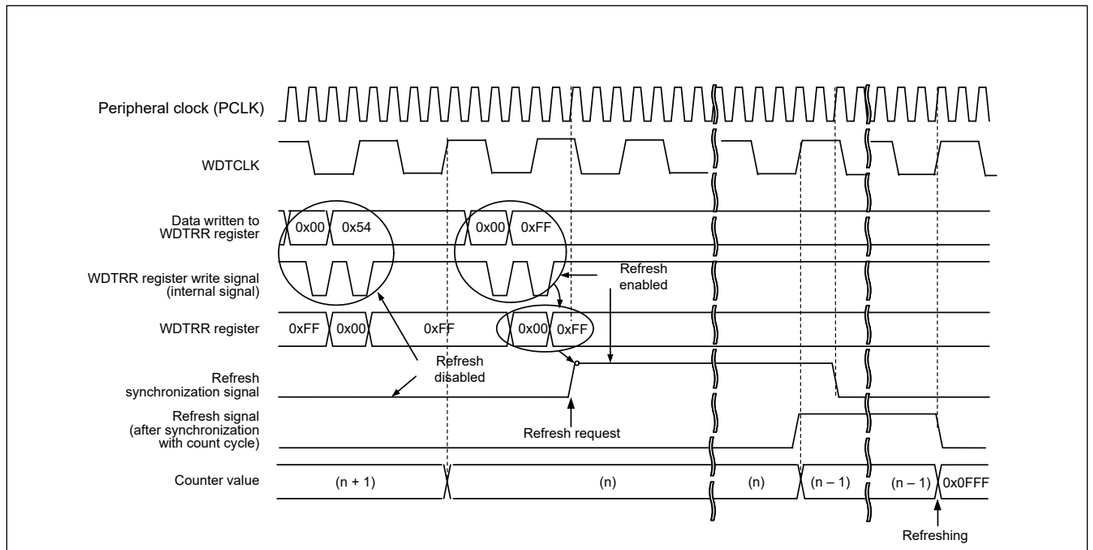
- 0x00 → 0xFF
- 0x00 ((n–1)th time) → 0x00 (nth time) → 0xFF
- ●0x00→访问另一个寄存器或从WDTRR读取→0xFF

[对刷新计数器无效的示例写入序列]

- ●0x23（0x00以外的值）→0xFF
- ●0x00→0x54（0xFF以外的值）
- ●0x00→0xAA（0x00和0xFF以外的值）→0xFF

将0xFF写入WDT刷新寄存器(WDTRR)后，刷新递减计数器最多需要4个信号周期进行计数。为满足此要求，请在递减计数器下溢之前的4个计数周期内将0xFF写入WDTRR。

图24.6显示了时钟分频比为PCLKB64时的WDT刷新操作波形。



Note: PCLK = PCLKB

Figure 24.6 WDT refresh operation waveforms when WDTCR.CKS[3:0] = 0x4 and WDTCR.TOPS[1:0] = 01b

Note: When setting the refresh time, consider the oscillation accuracy of the clock sources of the PCLKB and WDTCLK. Set values which ensure that refreshing is possible even when the frequency varies in the range of error of the oscillation accuracy.

24.3.4 Status Flags

The refresh error (WDTSR.REFEF) and underflow (WDTSR.UNDFF) flags retain the source of the interrupt request from the WDT. After a release from the interrupt request generation, read the WDTSR.REFEF and WDTSR.UNDFF flags to check for the interrupt source. For each flag, writing 0 clears the bit. Writing 1 has no effect. Leaving the status flags unchanged does not affect operation. If the flags are not cleared at the next interrupt request from the WDT, the earlier interrupt source is cleared and the new interrupt source is written. For the time period between when 0 is written in each flag and when its value is reflected, see section 24.2.3. WDTSR : WDT Status Register.

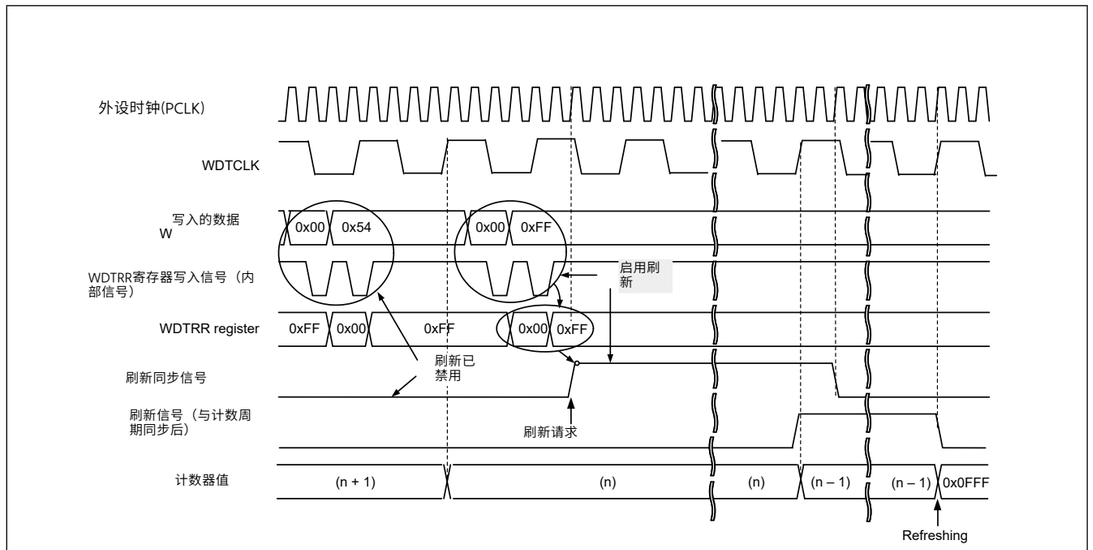
24.3.5 Reset Output

When the Reset Interrupt Select bit (WDTRCR.RSTIRQS) is set to 1 in register start mode, or when the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1 in auto start mode, a reset signal is output for 1 cycle count when an underflow in the down-counter or a refresh error occurs.

In register start mode, the down-counter is initialized (all bits set to 0) and stopped in that state after output of a reset signal. After the reset state is released and the program is restarted, the counter is set up again and counting down starts again with a refresh. In auto start mode, counting down starts automatically after the reset state is released.

24.3.6 Interrupt Sources

When the Reset Interrupt Select bit (WDTRCR.RSTIRQS) is set to 0 in register start mode or when the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 0 in auto start mode, an interrupt (WDT_NMIUNDF) signal is generated when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 12, Interrupt Controller Unit (ICU).



Note: PCLK = PCLKB

Figure 24.6 WDTCR.CKS[3:0]=0x4和WDTCR.TOPS[1:0]=01b时的WDT刷新操作波形

Note: 设置刷新时间时，要考虑PCLKB和WDTCLK时钟源的振荡精度。设定即使频率在振荡精度的误差范围内变化也能进行刷新的值。

24.3.4 状态标志

刷新错误(WDTSR.REFEF)和下溢(WDTSR.UNDFF)标志保留来自WDT的中断请求源。释放中断请求生成后，读取WDTSR.REFEF和WDTSR.UNDFF标志以检查中断源。对于每个标志，写入0会清除该位。写1无效。保持状态标志不变不会影响操作。如果在WDT发出下一个中断请求时未清除标志，则清除较早的中断源并写入新的中断源。关于从各标志写入0到反映其值的时间段，请参阅第24.2.3节。WDTSR：WDT状态寄存器。

24.3.5 复位输出

当复位中断选择位(WDTRCR.RSTIRQS)在寄存器启动模式下设置为1时，或当WDT复位时在自动启动模式下，选项功能选择寄存器0(OFS0)中的中断请求选择位(OFS0.WDTRSTIRQS)设置为1，当递减计数器中的下溢或刷新错误发生时，在1个周期计数内输出复位信号.

在寄存器启动模式下，递减计数器被初始化（所有位设置为0）并在输出复位信号后停止在该状态。复位状态解除并重新启动程序后，再次设置计数器，并通过刷新再次开始倒计时。在自动启动模式下，复位状态解除后自动开始倒计时。

24.3.6 中断源

当在寄存器启动模式下复位中断选择位(WDTRCR.RSTIRQS)设置为0或WDT复位时在自动启动模式下，选项功能选择寄存器0(OFS0)中的中断请求选择位(OFS0.WDTRSTIRQS)设置为0，当计数器下溢或发生刷新错误时，将产生中断(WDT_NMIUNDF)信号。此中断可用作不可屏蔽中断或中断。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

Table 24.4 WDT interrupt source

Name	Interrupt source	Interrupt to CPU	Start DMAC or DTC
WDT_NMIUNDF	• Down-counter underflow • Refresh error	Possible	Not possible

24.3.7 Reading the Down-Counter Value

The WDT stores the counter value in the down-counter value bits (WDTSR.CNTVAL[13:0]) of the WDT Status Register. Check these bits to obtain the counter value. The read value of the down-counter might differ from the actual count by one.

Figure 24.7 shows the processing for reading the WDT down-counter value when the clock division ratio is PCLKB/64.

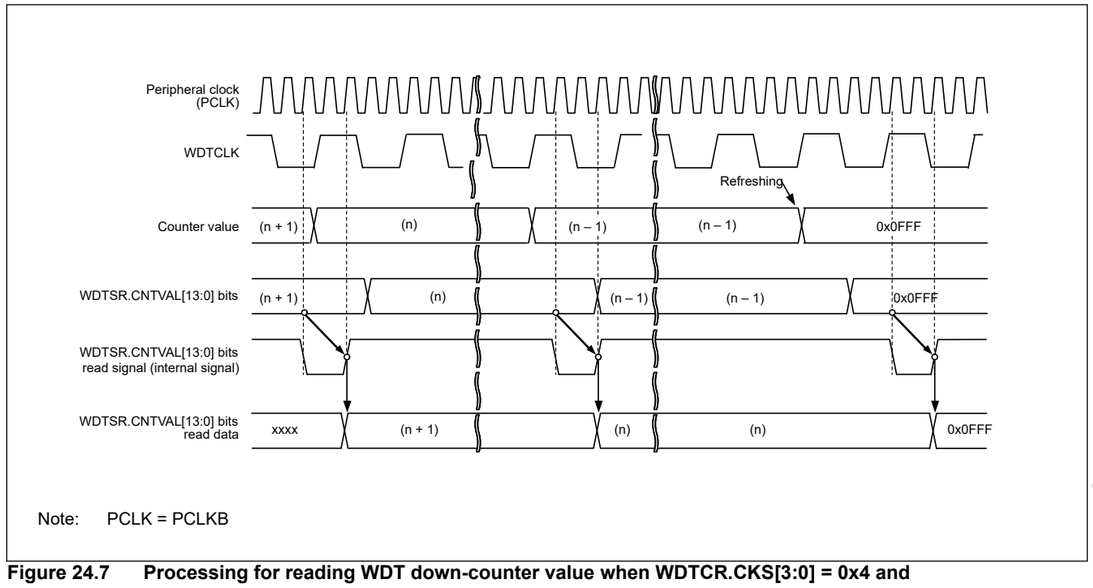


Figure 24.7 Processing for reading WDT down-counter value when WDTCR.CKS[3:0] = 0x4 and WDTCR.TOPS[1:0] = 01b

24.3.8 Association between Option Function Select Register 0 (OFS0) and WDT Registers

Table 24.5 lists the association between the Option Function Select Register 0 (OFS0) used in auto start mode, and the registers used in register start mode. For details on the Option Function Select Register 0 (OFS0), see section 6.2.1. OFS0 : Option Function Select Register 0.

Table 24.5 Association between Option Function Select Register 0 (OFS0) and the WDT registers

Control target	Function	OFS0 register (enabled in auto start mode) OFS0.WDTSTRT = 0	WDT registers (enabled in register start mode) OFS0.WDTSTRT = 1
Down-counter	Timeout period selection	OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]
	Clock division ratio selection	OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]
	Window start position selection	OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]
	Window end position selection	OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]
Reset output or interrupt request output	Reset output or interrupt request output selection	OFS0.WDTRSTIRQS	WDTRCR.RSTIRQS
Count stop	Sleep or Snooze mode count stop control	OFS0.WDTSTPCTL	WDTCSTPR.SLCSTP

Table 24.4 WDT中断源

Name	中断源	对CPU的中断	启动DMAC或DTC
WDT_NMIUNDF	• Down-counter underflow • 刷新错误	Possible	不可能

24.3.7 读取递减计数器值

WDT将计数器值存储在WDT状态寄存器的递减计数器值位(WDTSR.CNTVAL[13:0])中。检查这些位以获得计数器值。递减计数器的读取值可能与实际计数相差1。

图24.7显示了在时钟分频比为PCLKB64时读取WDT递减计数器值的处理。

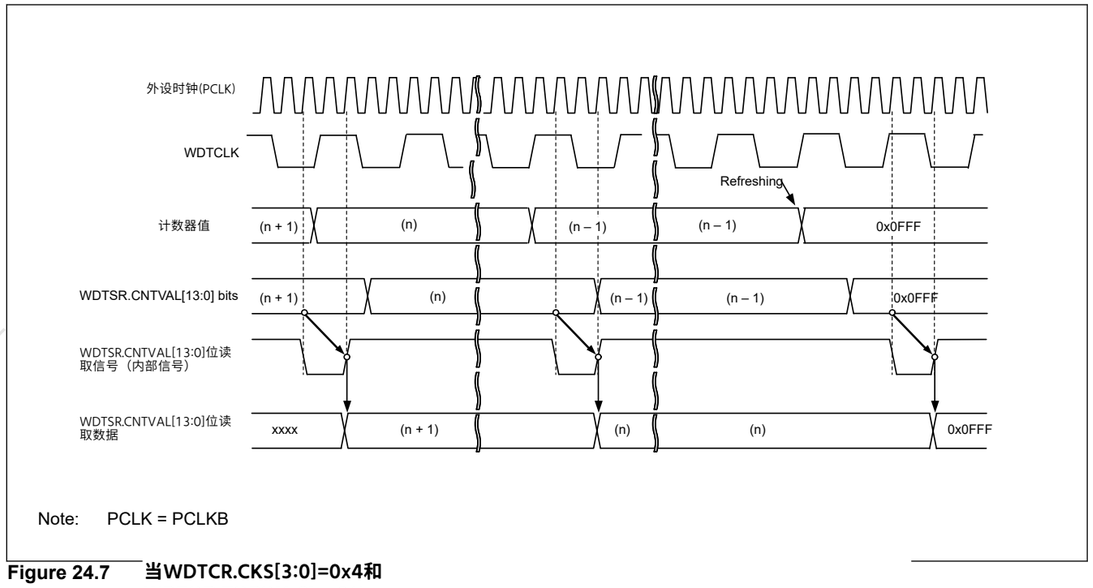


Figure 24.7 当WDTCR.CKS[3:0]=0x4和WDTCR.TOPS[1:0] = 01b

24.3.8 选项功能选择寄存器0(OFS0)和WDT之间的关联 Registers

表24.5列出了用于自动启动模式的选项功能选择寄存器0(OFS0)和用于寄存器启动模式的寄存器之间的关联。有关选项功能选择寄存器0(OFS0)的详细信息，请参见第6.2.1节。OFS0：选项功能选择寄存器0。

Table 24.5 选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联

控制目标	Function	OFS0寄存器（在自动启动模式下启用）OFS0.WDTSTRT=0	WDT寄存器（在寄存器启动模式下启用）OFS0.WDTSTRT=1
Down-counter	超时时间选择	OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]
	时钟分频比选择	OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]
	窗口起始位置选择	OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]
	窗口结束位置选择	OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]
复位输出或中断请求输出	复位输出或中断请求输出选择	OFS0.WDTRSTIRQS	WDTRCR.RSTIRQS
计数停止	睡眠或贪睡模式计数停止控制	OFS0.WDTSTPCTL	WDTCSTPR.SLCSTP

24.4 Output to the Event Link Controller (ELC)

The WDT is capable of a link operation for the previously specified module when interrupt request signal is used as an event signal by the ELC. The event signal is output by the counter underflow and refresh error. An event signal is output regardless of the setting of the Reset Interrupt Request Select bit (WDTRCR.RSTIRQS) in register start mode or auto start mode. An event signal can also be output when the next interrupt source is generated while the Refresh Error flag (WDTSR.REFEF) or Underflow flag (WDTSR.UNDFF) is 1. For details, see section 17, Event Link Controller (ELC).

24.5 Usage Notes

24.5.1 ICU Event Link Setting Register n (IELSRn) Setting

Setting 0x53 to ICU Event Link Setting Register n (ICU.IELSRn) is prohibited when enabling the WDT reset assertion (OFS0.WDTRSTIRQS = 0 or WDTRCR.RSTIRQS = 0) or when enabling event link operation (ELSRn.ELS[8:0] = 0x53).

24.4 输出到事件链接控制器(ELC)

当ELC将中断请求信号用作事件信号时，WDT能够对先前指定的模块进行链接操作。事件信号由计数器下溢和刷新错误输出。在寄存器启动模式或自动启动模式下，无论复位中断请求选择位(WDTRCR.RSTIRQS)的设置如何，都会输出事件信号。当刷新错误标志(WDTSR.REFEF)或下溢标志(WDTSR.UNDFF)为1时，也可以在产生下一个中断源时输出事件信号。有关详细信息，请参阅第17节，事件链接控制器(ELC)。

24.5 使用说明

24.5.1 ICU事件链接设置寄存器n(IELSRn)设置

当启用WDT复位断言(OFS0.WDTRSTIRQS=0或WDTRCR.RSTIRQS=0)或启用事件链接操作(ELSRn.ELS[8:0])时，禁止将0x53设置为ICU事件链接设置寄存器n(ICU.IELSRn)=0x53)。

25. Independent Watchdog Timer (IWDT)

25.1 Overview

The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

The IWDT functions differ from those of the WDT in the following respects:

- The divided IWDT-dedicated clock (IWDTCLK) is used as the count source (not affected by PCLKB)
- IWDT does not support register start mode

Table 25.1 lists the IWDT specifications and Figure 25.1 shows a block diagram.

Table 25.1 IWDT specifications

Parameter	Description
Count source*1	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter
Condition for starting the counter	• Counting automatically starts after a reset • Only secure developer can start the IWDT
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated (counting restarts automatically).
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Reading the counter value	The down-counter value can be read by the IWDTSR register
Event link function	• Down-counter underflow event output • Refresh error event output.
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep-mode count stop control output.
Auto start mode	Configurable to the following triggers: • Clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Timeout period of the Independent Watchdog Timer (OFS0.IWDTTOPS[1:0] bits) • Window start position in the Independent Watchdog Timer (OFS0.IWDTRPSS[1:0] bits) • Window end position in the Independent Watchdog Timer (OFS0.IWDTRPES[1:0] bits) • Reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Down-count stop function at transition to Sleep, Snooze, or Software Standby mode (OFS0.IWDTSTPCTL bit).
TrustZone Filter	Security attribution can be set

Note 1. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

The bus interface and registers operate with PCLKB, and the 14-bit counter and control circuits operate with IWDTCLK.

25. 独立看门狗定时器(IWDT)

25.1 Overview

独立看门狗定时器(IWDT)包含一个14位递减计数器，必须定期对其进行服务以防止计数器下溢。IWDT提供复位MCU或生成不可屏蔽中断或下溢中断的功能。由于定时器使用独立的专用时钟源运行，因此当系统失控时，它在将MCU作为故障安全机制返回到已知状态时特别有用。IWDT可以通过复位、下溢、刷新错误或寄存器中的计数值的刷新来自动触发。

IWDT的功能与WDT的功能有以下不同：

●分频IWDT专用时钟（IWDTCLK）用作计数源（不受PCLKB影响）

●IWDT不支持寄存器启动方式

表25.1列出了IWDT规范，图25.1显示了框图。

Table 25.1 IWDT specifications

Parameter	Description
计数来源*1	IWDT-dedicated clock (IWDTCLK)
时钟分频比	除以1、16、32、64、128或256
计数器操作	使用14位递减计数器进行递减计数
启动计数器的条件	• 复位后自动开始计数 • 只有安全的开发人员才能启动IWDT
停止计数器的条件	• 复位（递减计数器和其他寄存器恢复初始值） • 计数器下溢或产生刷新错误（计数自动重新开始）。
窗口功能	可以指定窗口开始和结束位置（允许刷新和禁止刷新期间）
重置输出源	• Down-counter underflows • 在允许刷新的期限之外刷新（刷新错误）。
Non-maskable interrupt/interrupt sources	• Down-counter underflows • 在允许刷新的期限之外刷新（刷新错误）。
读取计数器值	递减计数器的值可以通过IWDTSR寄存器读取
事件链接功能	• 递减计数器下溢事件输出 • 刷新错误事件输出。
输出信号（内部信号）	• 复位输出 • 中断请求输出 • 休眠模式计数停止控制输出。
自动启动模式	可配置为以下触发器：● 复位后的时钟分频比（OFS0.IWDTCKS[3:0]位） • 独立看门狗定时器的超时周期（OFS0.IWDTTOPS[1:0]位） • 独立看门狗定时器中的窗口起始位置（OFS0.IWDTRPSS[1:0]位） • 独立看门狗定时器中的窗口结束位置（OFS0.IWDTRPES[1:0]位） • 复位输出或中断请求输出（OFS0.IWDTRSTIRQS位） • 转换到休眠、贪睡或软件待机模式时的减计数停止功能（OFS0.IWDTSTPCL位）。
TrustZone Filter	可设置安全属性

注1.满足外设模块时钟（PCLKB）的频率≥4×（分频后的计数时钟源的频率）。

总线接口和寄存器使用PCLKB运行，14位计数器和控制电路使用IWDTCLK运行。

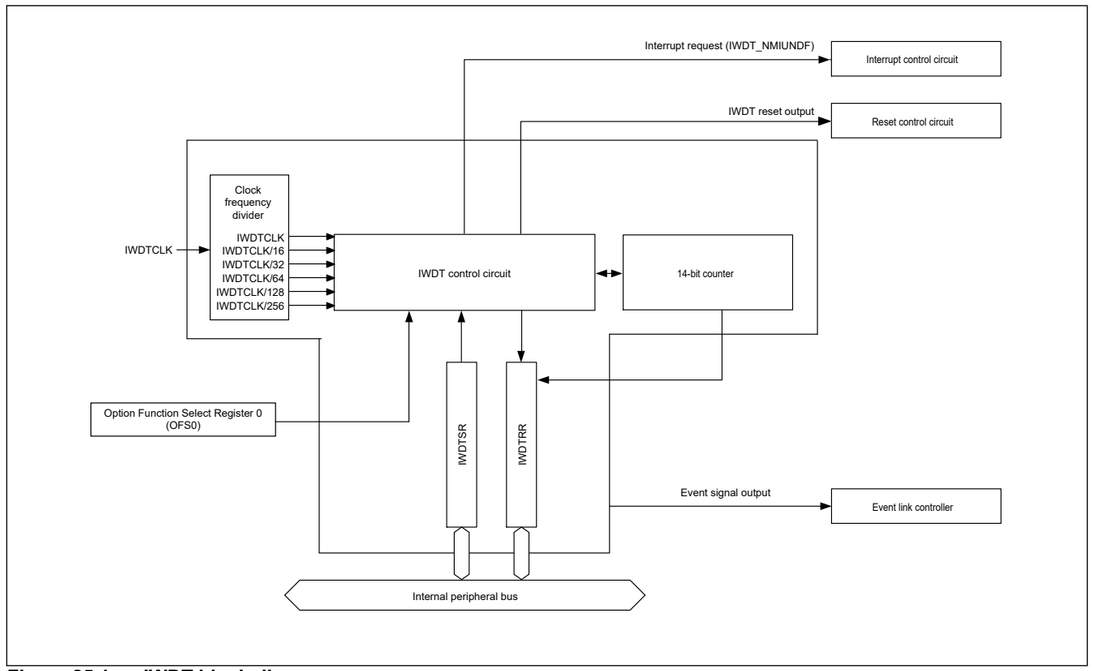


Figure 25.1 IWDT block diagram

25.2 Register Descriptions

25.2.1 IWDTRR : IWDT Refresh Register

Base address: IWDT = 0x4008_3200

Offset address: 0x00

Bit position:	7							0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	The down-counter is refreshed by writing 0x00 and then writing 0xFF to this register	R/W

The IWDTRR register refreshes the down-counter of the IWDT. The down-counter of the IWDT is refreshed by writing 0x00 and then writing 0xFF to IWDTRR (refresh operation) within the refresh-permitted period. After the down-counter is refreshed, it starts counting down from the value selected in the IWDT Timeout Period Select bits (OFS0.IWDTTOPS[1:0]) in the Option Function Select Register 0 (OFS0).

When 0x00 is written, the read value is 0x00. When a value other than 0x00 is written, the read value is 0xFF. For details of the refresh operation, see section 25.3.2. Refresh Operation.

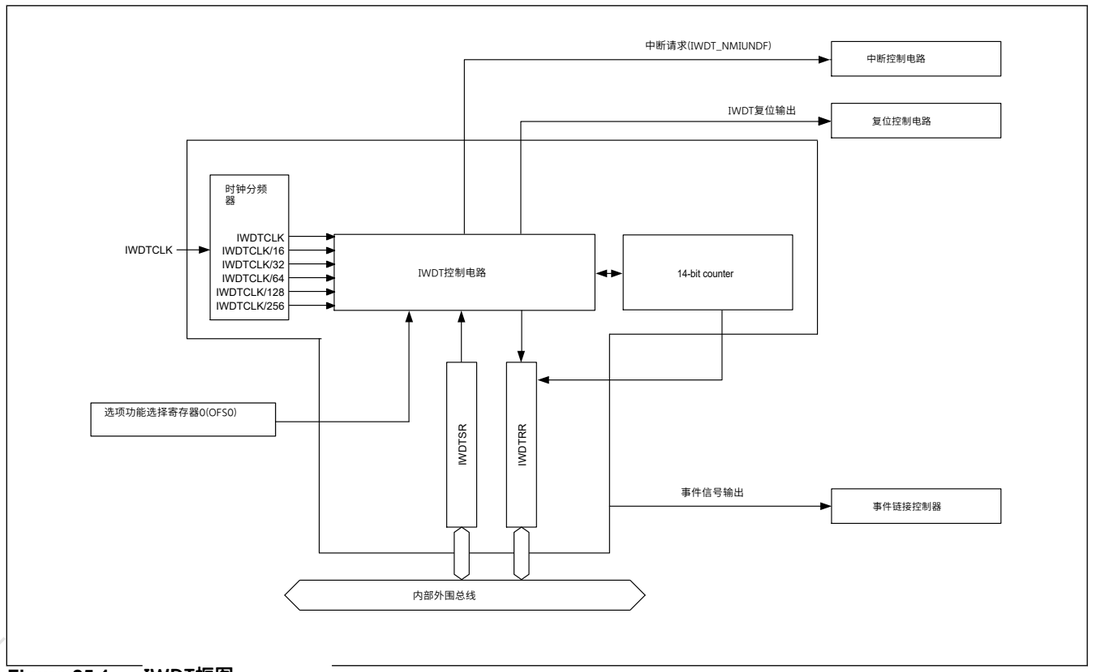


Figure 25.1 IWDT框图

25.2 注册说明

25.2.1 IWDTRR:IWDT刷新寄存器

Base address: IWDT = 0x4008_3200

Offset address: 0x00

Bit position:	7							0
Bit field:								
重置后的值:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	通过写入0x00然后将0xFF写入该寄存器来刷新递减计数器	R/W

IWDTRR寄存器刷新IWDT的递减计数器。IWDT的递减计数器通过在允许刷新的周期内写入0x00然后将0xFF写入IWDTRR（刷新操作）来刷新。递减计数器刷新后，它从选项功能选择寄存器0(OFS0)的IWDT超时周期选择位(OFS0.IWDTTOPS[1:0])中选择的值开始递减计数。

写入0x00时，读取值为0x00。写入0x00以外的值时，读取的值为0xFF。有关刷新操作的详细信息，请参阅第25.3.2节。刷新操作。

25.2.2 IWDTSR : IWDT Status Register

Base address: IWDT = 0x4008_3200

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CNTVAL[13:0]	Down-counter Value Value counted by the down-counter	R
14	UNDFF	Underflow Flag 0: No underflow occurred 1: Underflow occurred	R/W*1
15	REFEF	Refresh Error Flag 0: No refresh error occurred 1: Refresh error occurred	R/W*1

Note 1. Only 0 can be written to clear the flag.

The IWDTSR register indicates the counter value of the down-counter and whether an underflow or refresh error occurred in the down-counter.

CNTVAL[13:0] bits (Down-counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the down-counter. The value 1 indicates that the down-counter underflowed. Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N + 2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of this flag is ignored for (N + 2) IWDTCLK cycles after an underflow. N is specified in the IWDTCKS[3:0] bits as follows:

- When OFS0.IWDTCKS[3:0] = 0x0, N = 1
- When OFS0.IWDTCKS[3:0] = 0x2, N = 16
- When OFS0.IWDTCKS[3:0] = 0x3, N = 32
- When OFS0.IWDTCKS[3:0] = 0x4, N = 64
- When OFS0.IWDTCKS[3:0] = 0xF, N = 128
- When OFS0.IWDTCKS[3:0] = 0x5, N = 256.

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred. This indicates that a refresh operation was performed during a prohibited period. The value 1 indicates that a refresh error occurred. Write 0 to the REFEF flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N + 2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of this flag is ignored for (N + 2) IWDTCLK cycles following a refresh error. N is specified in the IWDTCKS[3:0] bits as follows:

- When OFS0.IWDTCKS[3:0] = 0x0, N = 1
- When OFS0.IWDTCKS[3:0] = 0x2, N = 16
- When OFS0.IWDTCKS[3:0] = 0x3, N = 32
- When OFS0.IWDTCKS[3:0] = 0x4, N = 64
- When OFS0.IWDTCKS[3:0] = 0xF, N = 128
- When OFS0.IWDTCKS[3:0] = 0x5, N = 256.

25.2.2 IWDTSR:IWDT状态寄存器

Base address: IWDT = 0x4008_3200

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	REFEF	UNDFF	CNTVAL[13:0]													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CNTVAL[13:0]	Down-counter Value 递减计数器计数的值	R
14	UNDFF	Underflow Flag 0：未发生下溢1：发生下溢	R/W*1
15	REFEF	刷新错误标志 0：未发生刷新错误1：发生刷新错误	R/W*1

注1.只能写入0来清除标志。

IWDTSR寄存器指示递减计数器的计数值以及递减计数器是否发生下溢或刷新错误。

CNTVAL[13:0] bits (Down-counter Value)

读取CNTVAL[13:0]位以确认递减计数器的值。读取的值可能与实际计数相差1。

UNDFF flag (Underflow Flag)

读取UNDFF标志以确认递减计数器中是否发生下溢。值1表示递减计数器下溢。将0写入UNDFF标志以将值设置为0。写入1无效。

清除UNDFF标志需要(N+2)个IWDTCLK周期和2个PCLKB周期。此外，在下溢后的(N+2)个IWDTCLK周期内，该标志的清除将被忽略。N在IWDTCKS[3:0]位中指定如下：

- When OFS0.IWDTCKS[3:0] = 0x0, N = 1
- When OFS0.IWDTCKS[3:0] = 0x2, N = 16
- When OFS0.IWDTCKS[3:0] = 0x3, N = 32
- When OFS0.IWDTCKS[3:0] = 0x4, N = 64
- When OFS0.IWDTCKS[3:0] = 0xF, N = 128
- When OFS0.IWDTCKS[3:0] = 0x5, N = 256.

REFEF标志（刷新错误标志）

读取REFEF标志以确认是否发生刷新错误。这表示在禁止期间执行了刷新操作。值1表示发生了刷新错误。将0写入REFEF标志以将值设置为0。写入1无效。

清除REFEF标志需要(N+2)个IWDTCLK周期和2个PCLKB周期。此外，在刷新错误后的(N+2)个IWDTCLK周期内，该标志的清除将被忽略。N在IWDTCKS[3:0]位中指定如下：

- When OFS0.IWDTCKS[3:0] = 0x0, N = 1
- When OFS0.IWDTCKS[3:0] = 0x2, N = 16
- When OFS0.IWDTCKS[3:0] = 0x3, N = 32
- When OFS0.IWDTCKS[3:0] = 0x4, N = 64
- When OFS0.IWDTCKS[3:0] = 0xF, N = 128
- When OFS0.IWDTCKS[3:0] = 0x5, N = 256.

25.2.3 OFS0 : Option Function Select Register 0

For information on the Option Function Select Register 0 (OFS0), see section 6.2.1. OFS0 : Option Function Select Register 0.

IWDTTOPS[1:0] bits (IWDT Timeout Period Select)

The IWDTTOPS[1:0] bits select the timeout period, that is, the period until the down-counter underflows, from 128, 512, 1024, or 2048 cycles, taking the divided clock specified in the IWDTCKS[3:0] bits as 1 cycle.

After the down-counter is refreshed, the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits determines the number of IWDTCLK cycles until the counter underflows.

Table 25.2 lists the relationship between the IWDTCKS[3:0] and IWDTTOPS[1:0] bit settings, the timeout period, and the number of IWDTCLK cycles.

Table 25.2 Timeout period settings

IWDTCKS[3:0] bits				IWDTTOPS[1:0] bits		Clock division ratio	Timeout period (number of cycles)	IWDTCLK cycles
b7	b6	b5	b4	b1	b0			
0	0	0	0	0	0	IWDTCLK	128	128
				0	1		512	512
				1	0		1024	1024
				1	1		2048	2048
0	0	1	0	0	0	IWDTCLK/16	128	2048
				0	1		512	8192
				1	0		1024	16384
				1	1		2048	32768
0	0	1	1	0	0	IWDTCLK/32	128	4096
				0	1		512	16384
				1	0		1024	32768
				1	1		2048	65536
0	1	0	0	0	0	IWDTCLK/64	128	8192
				0	1		512	32768
				1	0		1024	65536
				1	1		2048	131072
1	1	1	1	0	0	IWDTCLK/128	128	16384
				0	1		512	65536
				1	0		1024	131072
				1	1		2048	262144
0	1	0	1	0	0	IWDTCLK/256	128	32768
				0	1		512	131072
				1	0		1024	262144
				1	1		2048	524288

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the IWDT-dedicated clock (IWDTCLK) divided by 1, 16, 32, 64, 128, and 256. Combined with the IWDTTOPS[1:0] bit setting, the IWDT can be configured to a count period between 128 and 524,288 IWDTCLK cycles.

25.2.3 OFS0：选项功能选择寄存器0

有关选项功能选择寄存器0(OFS0)的信息，请参见第6.2.1节。OFS0：选项功能选择寄存器0。

IWDTTOPS[1:0]位（IWDT超时周期选择）

IWDTTOPS[1:0]位选择超时周期，即从128、512、1024或2048个周期开始，直到递减计数器下溢的周期，采用IWDTCKS[3:0]位中指定的分频时钟作为1个周期。

向下计数器刷新后，IWDTCKS[3:0]和IWDTTOPS[1:0]位的组合决定了在计数器下溢之前的IWDTCLK周期数。

表25.2列出了IWDTCKS[3:0]和IWDTTOPS[1:0]位设置、超时周期和IWDTCLK周期数之间的关系。

Table 25.2 超时时间设置

IWDTCKS[3:0] bits				IWDTTOPS[1:0] bits		时钟分频比	超时时间（周期数）	IWDTCLK cycles
b7	b6	b5	b4	b1	b0			
0	0	0	0	0	0	IWDTCLK	128	128
				0	1		512	512
				1	0		1024	1024
				1	1		2048	2048
0	0	1	0	0	0	IWDTCLK/16	128	2048
				0	1		512	8192
				1	0		1024	16384
				1	1		2048	32768
0	0	1	1	0	0	IWDTCLK/32	128	4096
				0	1		512	16384
				1	0		1024	32768
				1	1		2048	65536
0	1	0	0	0	0	IWDTCLK/64	128	8192
				0	1		512	32768
				1	0		1024	65536
				1	1		2048	131072
1	1	1	1	0	0	IWDTCLK/128	128	16384
				0	1		512	65536
				1	0		1024	131072
				1	1		2048	262144
0	1	0	1	0	0	IWDTCLK/256	128	32768
				0	1		512	131072
				1	0		1024	262144
				1	1		2048	524288

IWDTCKS[3:0]位（IWDT专用时钟分频比选择）

IWDTCKS[3:0]位指定用于递减计数器的时钟分频比。分频比可以从IWDT专用时钟(IWDTCLK)除以1、16、32、64、128和256中选择。结合IWDTTOPS[1:0]位设置，可以将IWDT配置为计数128到524 288个IWDTCLK周期之间的周期。

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. Set the window end position to a value less than the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is enabled.

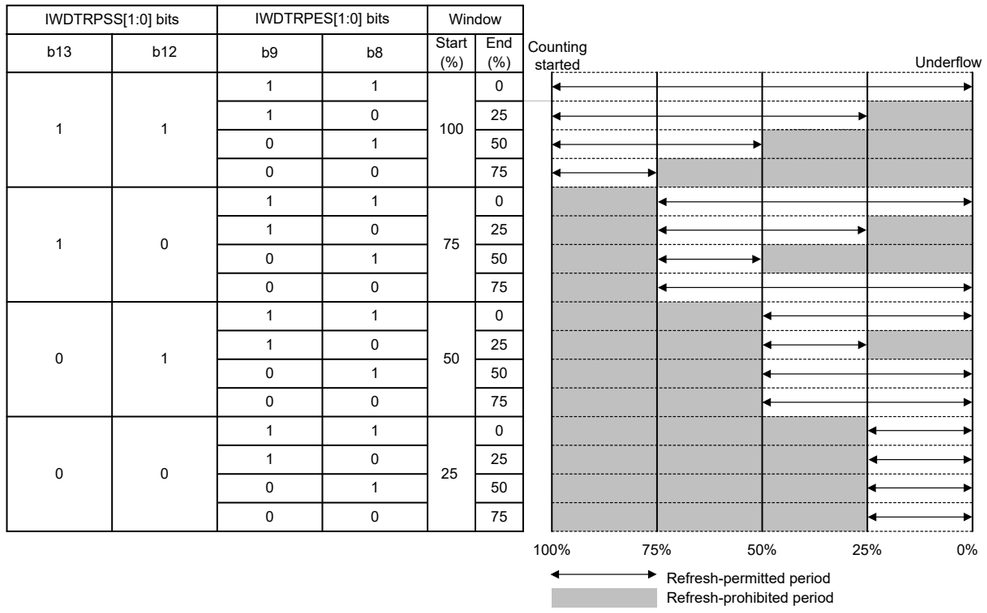
IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window start position. Set the window start position to a value greater than the window end position. If the window start position is less than or equal to the window end position, the window end position is set to 0%.

Table 25.3 lists the counter values for the window start and end positions, and Figure 25.2 shows the refresh-permitted period set in the IWDTRPSS[1:0], IWDTRPES[1:0], and IWDTTOPS[1:0] bits.

Table 25.3 Relationship between the timeout period and window start and end counter values

IWDTTOPS[1:0] bits		Timeout period		Window start and end counter value			
b1	b0	Cycles	Counter value	100%	75%	50%	25%
0	0	128	0x007F	0x007F	0x005F	0x003F	0x001F
0	1	512	0x01FF	0x01FF	0x017F	0x00FF	0x007F
1	0	1024	0x03FF	0x03FF	0x02FF	0x01FF	0x00FF
1	1	2048	0x07FF	0x07FF	0x05FF	0x03FF	0x01FF



Note: If window end setting ≥ window start setting, the window end setting is set to 0%.

Figure 25.2 IWDTRPSS[1:0] and IWDTRPES[1:0] bit settings and refresh-permitted period

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit specifies the behavior when an underflow or a refresh error occurs. Setting 1 selects reset output. Setting 0 selects non-maskable interrupt or interrupt.

IWDTRPES[1:0]位（IWDT窗口结束位置选择）

IWDTRPES[1:0]位指定指示刷新允许周期的窗口结束位置。可以为窗口结束位置选择75%、50%、25%或0%的超时时间。将窗口结束位置设置为小于窗口开始位置的值（窗口开始位置>窗口结束位置）。如果窗口结束位置大于窗口起始位置，则仅启用窗口起始位置设置。

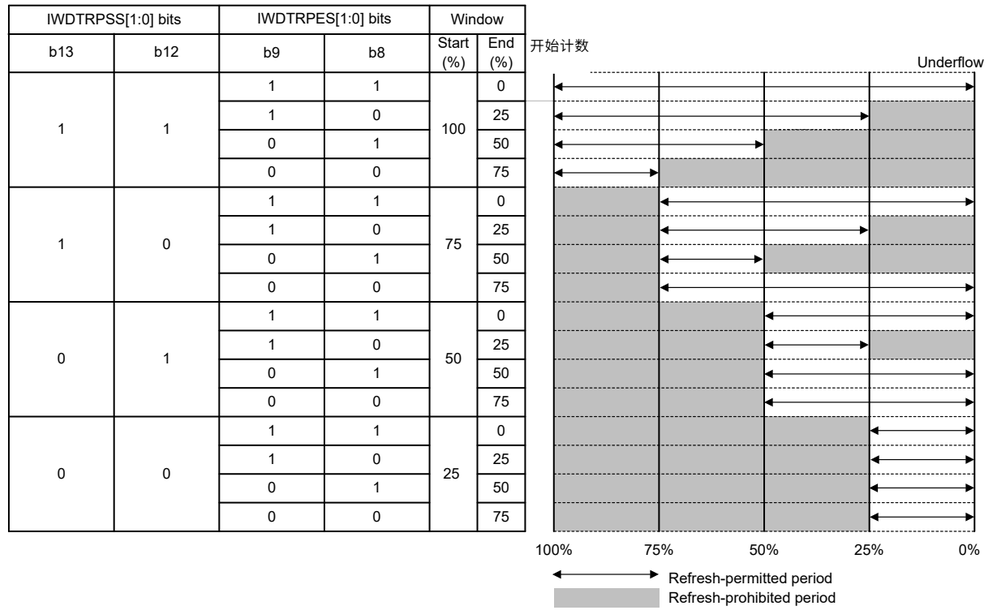
IWDTRPSS[1:0]位（IWDT窗口起始位置选择）

IWDTRPSS[1:0]位指定指示刷新允许周期的窗口起始位置。窗口起始位置可选择100%、75%、50%或25%的超时时间。将窗口开始位置设置为大于窗口结束位置的值。如果窗口开始位置小于或等于窗口结束位置，则窗口结束位置设置为0%。

表25.3列出了窗口开始和结束位置的计数器值，图25.2显示了在IWDTRPSS[1:0]、IWDTRPES[1:0]和IWDTTOPS[1:0]位中设置的允许刷新周期。

Table 25.3 超时时间与窗口开始和结束计数器值之间的关系

IWDTTOPS[1:0] bits		超时时间		窗口开始和结束计数器值			
b1	b0	Cycles	计数器值	100%	75%	50%	25%
0	0	128	0x007F	0x007F	0x005F	0x003F	0x001F
0	1	512	0x01FF	0x01FF	0x017F	0x00FF	0x007F
1	0	1024	0x03FF	0x03FF	0x02FF	0x01FF	0x00FF
1	1	2048	0x07FF	0x07FF	0x05FF	0x03FF	0x01FF



Note: 如果窗口结束设置≥窗口开始设置，则窗口结束设置设置为0%。

Figure 25.2 IWDTRPSS[1:0]和IWDTRPES[1:0]位设置和允许刷新周期

IWDTRSTIRQS位（IWDT复位中断请求选择）

IWDTRSTIRQS位指定发生下溢或刷新错误时的行为。设置1选择复位输出。
设置0选择不可屏蔽中断或中断。

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit selects whether to stop counting on transition to Sleep, Snooze, or Software Standby mode.

25.3 Operation

25.3.1 Auto Start Mode

When the IWDT Start Mode Select bit (OFS0.IWDTSTRT) in the Option Function Select Register 0 is 0, auto start mode is selected, otherwise the IWDT is disabled.

Within the reset state, the setting values for the following in the Option Function Select Register 0 (OFS0) are set in the IWDT registers:

- Clock division ratio (OFS0.IWDTCKS[3:0])
- Window start and end positions (OFS0.IWDTRPSS[1:0], OFS0.IWDTRPES[1:0])
- Timeout period (OFS0.IWDTTOPS[1:0])
- Reset output or interrupt request (OFS0.IWDTRSTIRQS)

When the reset state is released, the counter automatically starts counting down from the value selected in the IWDT Timeout Period Select bits (OFS0.IWDTTOPS[1:0]).

After that, as long as the program continues normal operation and the counter is refreshed within the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and down-counting continues. The IWDT does not output the reset signal as long as this procedure continues. However, if the counter underflows because the program crashed or because a refresh error occurred when an attempt is made to refresh outside the refresh-permitted period, the IWDT asserts the reset signal or non-maskable interrupt request/interrupt request (IWDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle, the value of the timeout period is set in the down-counter and counting starts. The reset output or interrupt request output can be selected with the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS). Non-maskable interrupt request or interrupt request can be selected with the IWDT Underflow/Refresh Error Interrupt Enable bit (NMIER.IWDTEN).

Figure 25.3 shows an example of operation under the following conditions:

- Auto start mode (OFS0.IWDTSTRT = 0)
- Non-maskable interrupt request output is enabled (OFS0.IWDTRSTIRQS = 0)
- The window start position is 75% (OFS0.IWDTRPSS[1:0] = 10b)
- The window end position is 25% (OFS0.IWDTRPES[1:0] = 10b).

IWDTSTPCTL位（IWDT停止控制）

IWDTSTPCTL位选择在转换到休眠、贪睡或软件待机模式时是否停止计数。

25.3 Operation

25.3.1 自动启动模式

当IWDT启动模式选择位置（OFS0.IWDTSTRT）中的选项函数选择寄存器0为0时，选择了自动启动模式，否则IWDT将被禁用。

在复位状态下，选项功能选择寄存器0(OFS0)中的以下设置值在
IWDT registers:

- ●时钟分频比（OFS0.IWDTCKS[3:0]）
- ●窗口开始和结束位置（OFS0.IWDTRPSS[1:0]、OFS0.IWDTRPES[1:0]）
- ●超时周期（OFS0.IWDTOPS[1:0]）
- ●复位输出或中断请求（OFS0.IWDTRSTIRQS）

解除复位状态后，计数器自动从IWDT中选择的值开始倒计时
超时周期选择位(OFS0.IWDTOPS[1:0])。

之后，只要程序继续正常运行，并且在允许刷新的时间内刷新计数器，每次刷新计数器并继续递减计数时，计数器中的值都会被复位。只要此过程继续，IWDT就不会输出复位信号。但是，如果由于程序崩溃或在刷新允许周期之外尝试刷新时发生刷新错误而导致计数器下溢，则IWDT将置位复位信号或不可屏蔽中断请求中断请求(IWDT_NMIUNDF)。

复位信号或不可屏蔽中断请求中断请求产生后，计数器在计数1个周期后重新加载超时周期，超时周期的值设置在递减计数器中并开始计数。可以通过IWDT复位中断请求选择位(OFS0.IWDTRSTIRQS)选择复位输出或中断请求输出。可以使用IWDT下溢刷新错误中断　　允许位(NMIER.IWDTEN)选择不可屏蔽的中断请求或中断请求。

图25.3显示了以下条件下的操作示例：

- ●自动启动模式（OFS0.IWDTSTRT=0）
- ●使能不可屏蔽中断请求输出（OFS0.IWDTRSTIRQS=0）
- ●窗口起始位置为75%(OFS0.IWDTRPSS[1:0]=10b)
- ●窗口结束位置为25%(OFS0.IWDTRPES[1:0]=10b)。

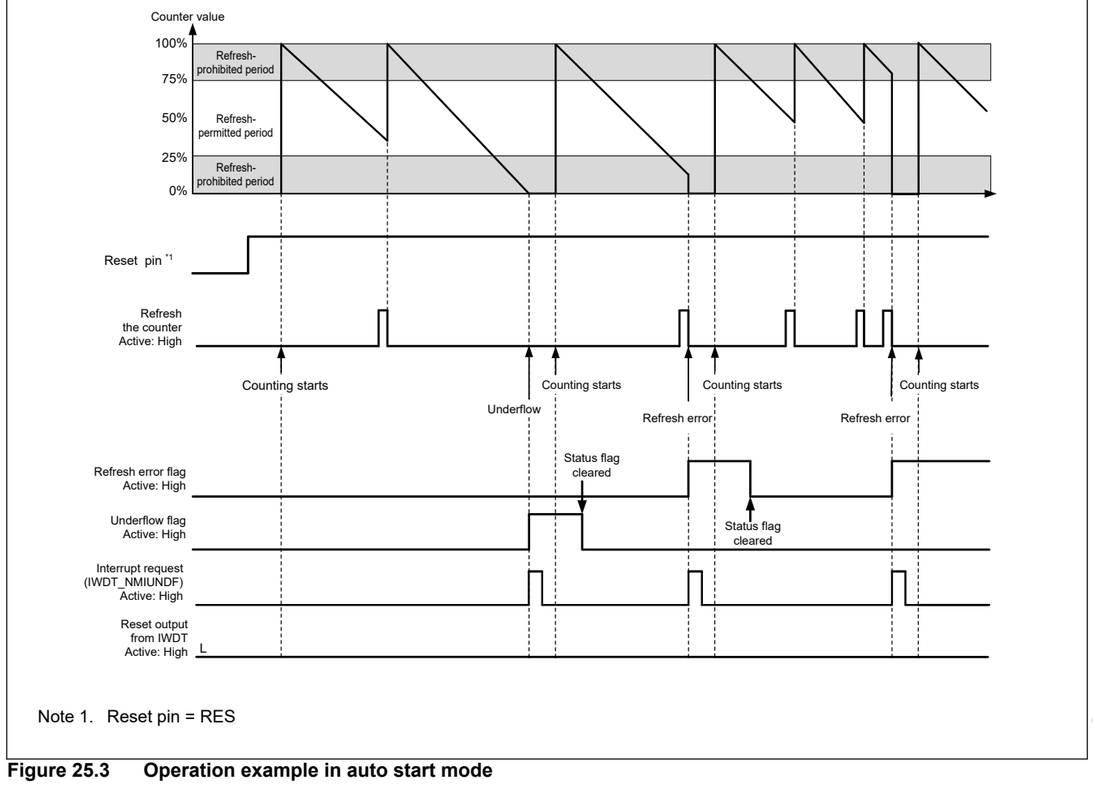


Figure 25.3 Operation example in auto start mode

25.3.2 Refresh Operation

The down-counter is refreshed and operation starts (counting is started by refreshing) by writing the values 0x00 and 0xFF to the IWDT Refresh Register (IWDTRR). If a value other than 0xFF is written after 0x00, the down-counter is not refreshed. If an invalid value is written, correct refreshing resumes on a write of 0x00 and 0xFF to the IWDTRR.

When writes are made in the order of 0x00 (first time) → 0x00 (second time), and if 0xFF is written after that, the writing order 0x00 → 0xFF is satisfied. Writing 0x00 ((n - 1)th time) →0x00 (nth time) → 0xFF is valid, and the refresh is performed correctly. Even when the first value written before 0x00 is not 0x00, correct refreshing is performed as long as the operation contains the write sequence of 0x00 → 0xFF.

Correct refreshing is also performed regardless of whether a register other than IWDTRR is accessed or IWDTRR is read between writing 0x00 and writing 0xFF to IWDTRR. Writes to refresh the counter must be made within the refresh-permitted period. Whether writing is done within the refresh-permitted period is determined when 0xFF is written. For this reason, correct refreshing is performed even when 0x00 is written outside the refresh-permitted period.

[Example write sequences that are valid to refresh the counter]

- 0x00 → 0xFF
- 0x00 ((n - 1)th time) → 0x00 (nth time) → 0xFF
- 0x00 → access to another register or read from IWDTRR → 0xFF.

[Example write sequences that are not valid to refresh the counter]

- 0x23 (a value other than 0x00) → 0xFF
- 0x00 → 0x54 (a value other than 0xFF)

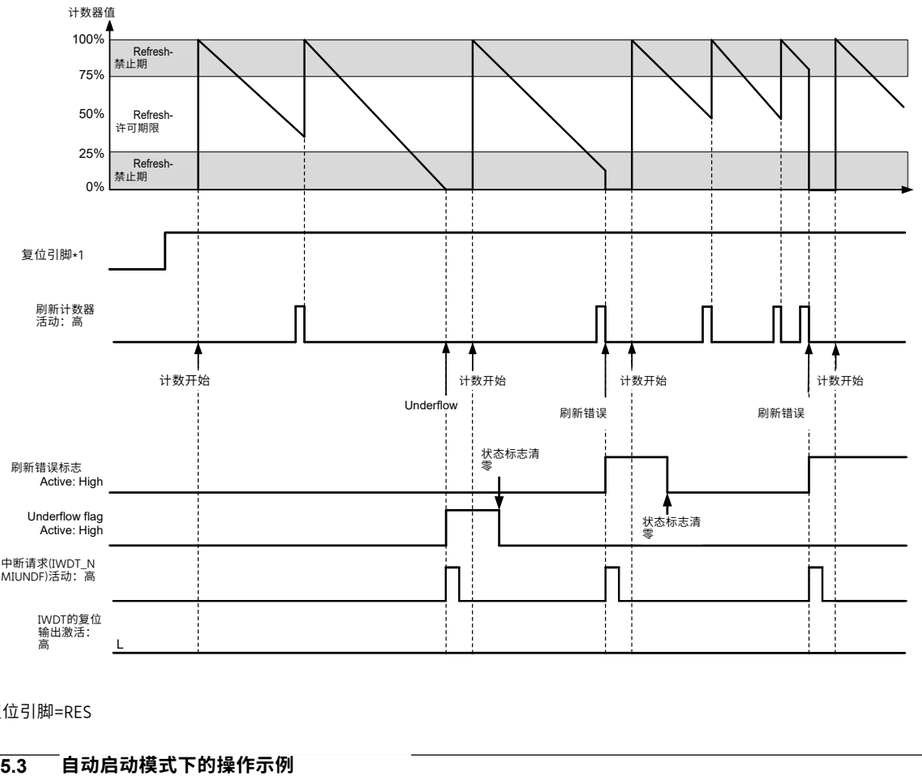


Figure 25.3 自动启动模式下的操作示例

25.3.2 刷新操作

通过将值0x00和0xFF写入IWDT刷新寄存器(IWDTRR)来刷新递减计数器并开始操作（通过刷新开始计数）。如果在0x00之后写入0xFF以外的值，则不刷新递减计数器。如果写入无效值，则在向IWDTRR写入0x00和0xFF时会恢复正确刷新。

当以0x00（第一次）→0x00（第二次）的顺序进行写入时，如果在此之后写入0xFF，则满足写入顺序0x00→0xFF。写入0x00((n1)次)→0x00(n次)→0xFF有效，刷新正确。即使在0x00之前写入的第一个值不是0x00时，只要操作包含0x00→0xFF的写入序列，就会执行正确的刷新。

无论在写入0x00和写入0xFF到IWDTRR之间是否访问IWDTRR以外的寄存器或读取IWDTRR，也会执行正确刷新。刷新计数器的写入必须在允许刷新的期限内进行。在写入0xFF时确定是否在可刷新周期内完成写入。因此，即使在可刷新期间外写入0x00，也会执行正确的刷新。

[对刷新计数器有效的示例写入序列]

- 0x00 → 0xFF
- 0x00 ((n - 1)th time) → 0x00 (nth time) → 0xFF
- ●0x00→访问另一个寄存器或从IWDTRR读取→0xFF。

[对刷新计数器无效的示例写入序列]

- ●0x23（0x00以外的值）→0xFF
- ●0x00→0x54（0xFF以外的值）

- 0x00 → 0xAA (0x00 and a value other than 0xFF) → 0xFF.

After 0xFF is written to the IWDTRR register, refreshing the counter requires up to 4 cycles of the signal for counting (the IWDT-Dedicated Clock Frequency Division Ratio Select bits (OFS0.IWDTCKS[3:0]) to determine how many cycles of the IWDT-dedicated clock (IWDTCLK) make up 1 cycle for counting. To meet this requirement, writing 0xFF to the IWDTRR must be completed 4 count cycles before the end of the refresh-permitted period or a down-counter underflow. The value of the counter can be checked with the counter bits (IWDTSR.CNTVAL[13:0]).

[Example refreshing timings]

- When the window start position is set to 0x1FFF, even if 0x00 is written to IWDTRR before 0x1FFF is reached at (0x2002, for example), refreshing occurs if 0xFF is written to IWDTRR after the value of the IWDTSR.CNTVAL[13:0] bits reaches 0x1FFF
- When the window end position is set to 0x1FFF, refreshing occurs if 0x2003 (4 count cycles before 0x1FFF) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 0x00 → 0xFF to IWDTRR
- When the refresh-permitted period continues until count 0x0000, refreshing can be performed immediately before an underflow. In this case, if 0x0003 (4 count cycles before an underflow) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 0x00 → 0xFF to IWDTRR, no underflow occurs and refreshing is performed.

Figure 25.4 shows the IWDT refresh-operation waveforms when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

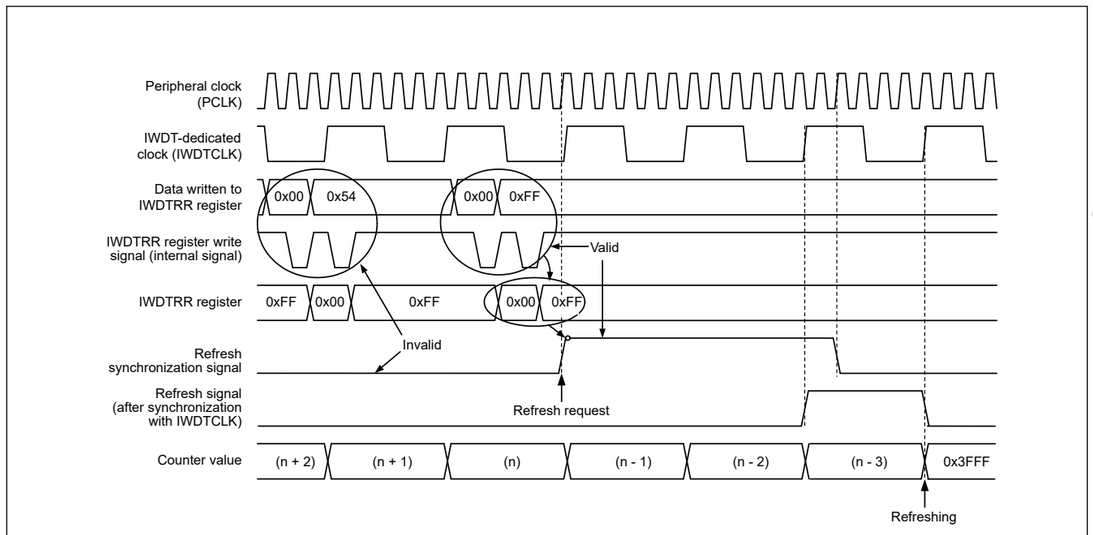


Figure 25.4 IWDT refresh operation waveforms when OFS0.IWDTCKS[3:0] = 0000b, OFS0.IWDTTOPS[1:0] = 11b

25.3.3 Status Flags

The refresh error (IWDTSR.REFEF) and underflow (IWDTSR.UNDFF) flags retain the source of the interrupt request from the IWDT. Therefore, after a release from the interrupt request generation, read the IWDTSR.REFEF and UNDFF flags to check for the interrupt source. For each flag, writing 0 clears the bit and writing 1 has no effect.

Leaving the status flags unchanged does not affect operation. If the flags are not cleared at the time of the next interrupt request from the IWDT, the earlier interrupt source is cleared and the new interrupt source is written. For the time period between when 0 is written in each flag and when its value is reflected, see section 25.2.2. IWDTSR : IWDT Status Register.

●0x00→0xAA（0x00和0xFF以外的值）→0xFF。

将0xFF写入IWDTRR寄存器后，刷新计数器需要最多4个周期的信号计数（IWDT专用时钟分频比选择位（OFS0.IWDTCKS[3:0]）来确定IWDT专用时钟(IWDTCLK)占1个周期用于计数。为满足此要求，必须在刷新允许周期结束或递减计数器下溢之前4个计数周期完成向IWDTRR写入0xFF。可以使用计数器位(IWDTSR.CNTVAL[13:0])检查计数器。

[Example refreshing timings]

●当窗口起始位置设置为0x1FFF时，即使在到达0x1FFF之前将0x00写入IWDTRR（例如0x2002），如果在IWDTSR.CNTVAL[13:0]位的值达到0x1FFF后将0xFF写入IWDTRR，则会发生刷新

●当窗口结束位置设置为0x1FFF时，如果在将0x00→0xFF写入IWDTRR后立即从IWDTSR.CNTVAL[13:0]位读取0x2003（0x1FFF之前的4个计数周期）或更大的值，则会发生刷新

●当刷新允许周期持续到计数0x0000时，可以在下溢之前立即执行刷新。在这种情况下，如果在将0x00→0xFF写入IWDTRR后立即从IWDTSR.CNTVAL[13:0]位读取0x0003（下溢前的4个计数周期）或更大的值，则不会发生下溢并执行刷新。

图25.4显示了当PCLKB>IWDTCLK且时钟分频比为时的IWDT刷新操作波形
IWDTCLK.

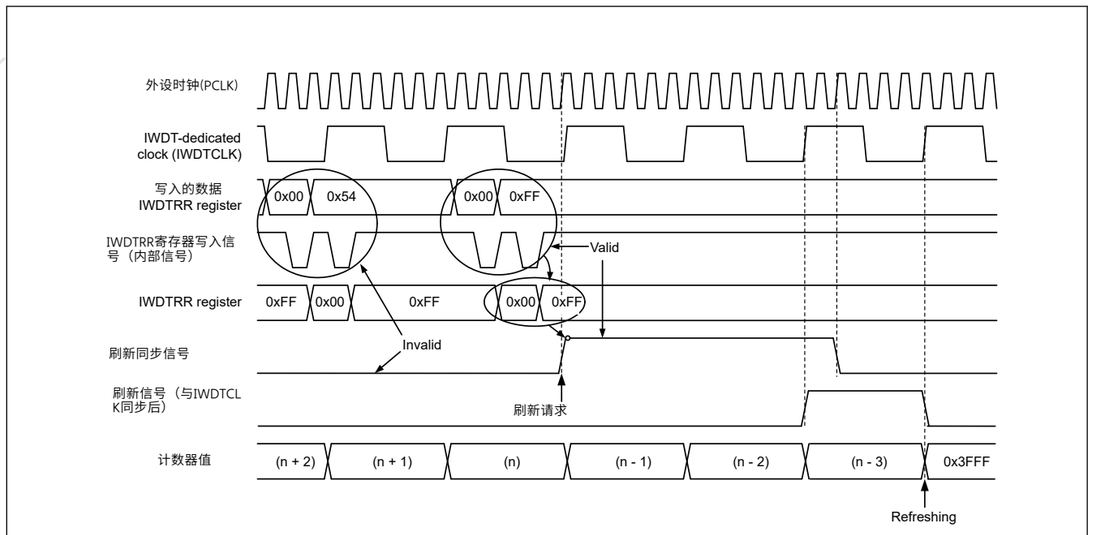


Figure 25.4 OFS0.IWDTCKS[3:0]=0000b OFS0.IWDTCKS[1:0]=11b时的IWDT刷新操作波形

25.3.3 状态标志

刷新错误(IWDTSR.REFEF)和下溢(IWDTSR.UNDFF)标志保留来自IWDT的中断请求源。因此，在中断请求生成释放后，读取IWDTSR.REFEF和UNDFF标志以检查中断源。对于每个标志，写入0清除该位，写入1无效。

保持状态标志不变不会影响操作。如果在IWDT发出下一个中断请求时未清除标志，则清除较早的中断源并写入新的中断源。关于从各标志写入0到反映其值的时间段，请参阅第25.2.2节。IWDTSR：IWDT状态寄存器。

25.3.4 Reset Output

When the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1, a reset signal is output when an underflow in the counter or a refresh error occurs. Counting down automatically starts after the reset output.

25.3.5 Interrupt Sources

When the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 0, an interrupt (IWDT_NMIUNDF) signal occurs when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 12, Interrupt Controller Unit (ICU).

Table 25.4 IWDT interrupt source

Name	Interrupt source	Interrupt to CPU	Start DMAC or DTC
IWDT_NMIUNDF	• Down-counter underflow • Refresh error	Possible	Not possible

25.3.6 Reading the Down-Counter Value

As the counter is a IWDT-dedicated clock (IWDTCLK), the counter value cannot be read directly. The IWDT synchronizes the counter value with the peripheral clock (PCLKB) and stores it in the down-counter value bits (IWDTSR.CNTVAL[13:0]) of the IWDT Status Register. Check these bits to obtain the counter value indirectly.

Reading the counter value requires multiple PCLKB clock cycles (up to 4 clock cycles), and the read counter value might differ from the actual counter value by a value of one count.

Figure 25.5 shows the processing for reading the IWDT counter value when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

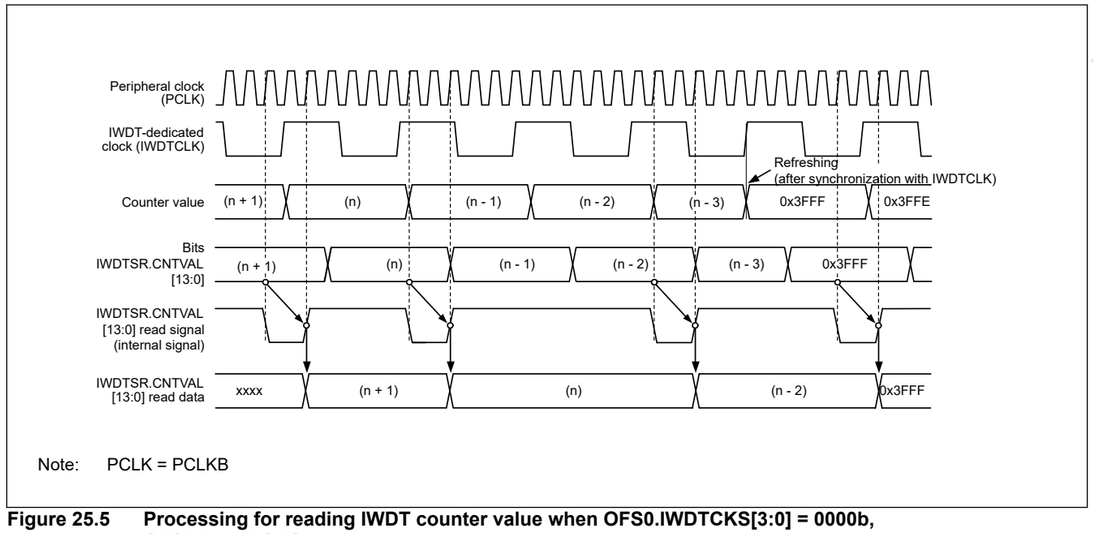


Figure 25.5 Processing for reading IWDT counter value when OFS0.IWDTCKS[3:0] = 0000b, OFS0.IWDTTOPS[1:0] = 11b

25.4 Output to the Event Link Controller (ELC)

The IWDT is capable of link operation for a specified module when the interrupt request signal is used as an event signal by the event link controller (ELC). The event signal is output by the counter underflow or refresh error.

An event signal is output regardless of the setting of the OFS0.IWDTRSTIRQS bit. An event signal can also be output at generation of the next interrupt source while the Refresh Error flag (IWDTSR.REFEF) or Underflow flag (IWDTSR.UNDFF) is 1. For details, see section 17, Event Link Controller (ELC).

25.3.4 复位输出

当IWDT重置中断请求选择位置（OFS0.IWDTRSTIRQS）中的选项函数选择寄存器0（OFS0）的位置为1时，当计数器中的下流或刷新错误发生时，将输出重置信号。复位输出后自动开始倒计时。

25.3.5 中断源

当IWDT重置中断请求选择位置（OFS0.IWDTRSTIRQS）中的选项函数选择寄存器0（OFS0）设置为0时，当计数器中的下流或刷新错误发生时，会发生中断（IWDT_NMIUNDF）信号。此中断可用作不可屏蔽中断或中断。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

Table 25.4 IWDT中断源

Name	中断源	对CPU的中断	启动DMAC或DTC
IWDT_NMIUNDF	• Down-counter underflow • 刷新错误	Possible	不可能

25.3.6 读取递减计数器值

由于计数器是IWDT专用时钟(IWDTCLK)，因此无法直接读取计数器值。IWDT将计数器值与外设时钟(PCLKB)同步，并将其存储在IWDT状态寄存器的递减计数器值位(IWDTSR.CNTVAL[13:0])中。检查这些位以间接获得计数器值。

读取计数器值需要多个PCLKB时钟周期（最多4个时钟周期），读取的计数器值可能与实际计数器值相差一个计数值。

图25.5显示了当PCLKB>IWDTCLK且时钟分频比为IWDTCLK时读取IWDT计数器值的处理。

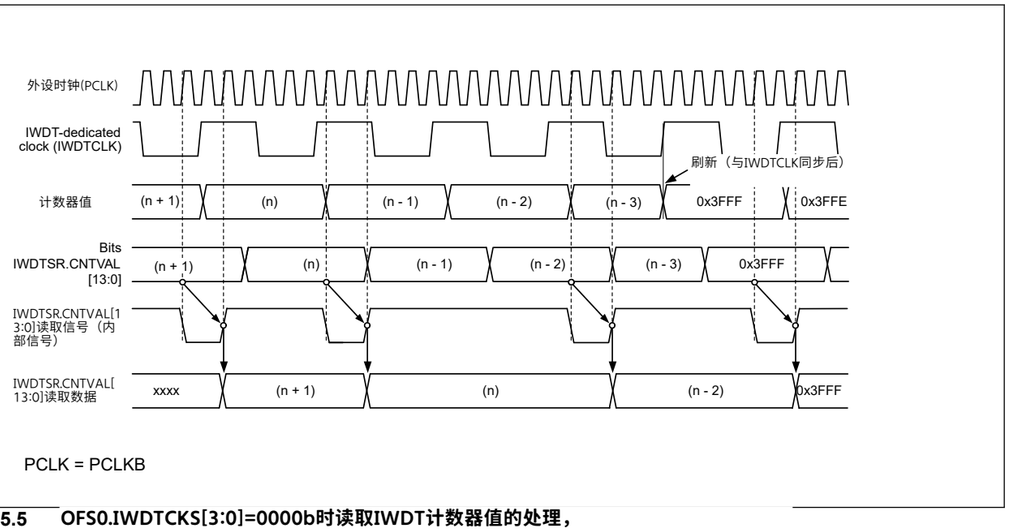


Figure 25.5 OFS0.IWDTCKS[3:0]=0000b时读取IWDT计数器值的处理，OFS0.IWDTTOPS[1:0] = 11b

25.4 输出到事件链接控制器(ELC)

当中断请求信号被事件链接控制器(ELC)用作事件信号时，IWDT能够对指定模块进行链接操作。事件信号由计数器下溢或刷新错误输出。

无论OFS0.IWDTRSTIRQS位的设置如何，都会输出事件信号。当刷新错误标志(IWDTSR.REFEF)或下溢标志(IWDTSR.UNDFF)为1时，也可以在生成下一个中断源时输出事件信号。有关详细信息，请参阅第17节，事件链接控制器(ELC)。

25.5 Usage Notes

25.5.1 Refresh Operations

While configuring the refresh time, consider variations in the range of errors given the accuracy of PCLKB and IWDTCLK. Set values that ensure refreshing is possible.

25.5.2 Clock Division Ratio Setting

Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

25.5.3 Constraints on the ICU Event Link Setting Register n (IELSRn) Setting

Setting 0x52 to ICU Event Link Setting Register n (IELSRn.IELS[8:0]) is prohibited when enabling the IWDT reset assertion (OFS0.IWDTRSTIRQS = 0) or when enabling event link operation (ELSRn.ELS[8:0] = 0x52).

25.5 使用说明

25.5.1 刷新操作

在配置刷新时间时，请考虑给定PCLKB和IWDTCLK精度的误差范围的变化。
设置确保可以刷新的值。

25.5.2 时钟分频比设置

满足外设模块时钟（PCLKB）的频率≥4×（分频后的计数时钟源的频率）。

25.5.3 ICU事件链接设置寄存器n(IELSRn)设置的约束

当启用IWDT复位断言(OFS0.IWDTRSTIRQS=0)或启用事件链接操作(ELSRn.ELS[8:0]=0x52）。

26. Serial Communications Interface (SCI)

This is the SCI_B version of the SCI peripheral module.

SCI_B is referred to as SCI in this chapter.

26.1 Overview

The Serial Communications Interface (SCI) × 6 channels have asynchronous and synchronous serial interfaces:

- Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))
- 8-bit clock synchronous interface
- Simple IIC (master-only)
- Simple SPI
- Simple LIN
- Smart card interface
- Manchester interface

The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0 to 4, 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.

In this section, PCLK refers to PCLKA, TCLK refers to SCITCLK.

Table 26.1 lists the SCI specifications, Figure 26.1 shows a block diagram of SCI, and Table 26.2 lists the I/O pins.

Table 26.1 SCI specifications (1 of 4)

Parameter		Specifications
Number of modules		6 (SCIn (n = 0 to 4, 9))
Serial communication modes		• Asynchronous • Clock synchronous • Simple IIC • Simple SPI • Simple LIN • Smart card interface • Manchester interface
Transfer speed		Bit rate specifiable with the on-chip baud rate generator
Full-duplex communications		• Transmitter: Continuous transmission possible using double-buffering • Receiver: Continuous reception possible using double-buffering
Half-duplex communications		Half-duplex communication is possible by using only TXDn pins
Data transfer		Selectable as LSB-first or MSB-first transfer
Inverter for communication terminals (RXDn, TXDn)		Selectable inverter for each terminals (RXDn, TXDn)
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, receive data ready, address match. Break Field detection/output, Bus collision detection, Active edge detection. Completion of generation of a start condition, restart condition, or stop condition. (for simple IIC mode)
Loop Back function		Self-diagnosis of communication function by IP internal transmission / reception is possible
Synchronizer Bypass function		Ability to bypass synchronization circuit between bus clock and operation clock (TCLK)
Module-stop function		Module-stop state can be set for each channel
Snooze end request		SCI0 address mismatch (SCI0_DCUF)
Clock synchronous mode	Data length	8 bits
	Adjustment of receive sampling timing	Adjustable receive sampling timing after the default timing in master mode only when using internal clock

26. 串行通信接口(SCI)

这是SCI外设模块的SCI_B版本。

SCI_B在本章中称为SCI。

26.1 Overview

串行通信接口(SCI)×6通道具有异步和同步串行接口：

●异步接口（UART和异步通信接口适配器(ACIA)）

●8位时钟同步接口

- Simple IIC (master-only)

●简单的SPI

●简单的LIN

●智能卡接口

●曼彻斯特接口

智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。SCIn(n=0到4 9)具有FIFO缓冲区以实现连续和全双工通信，并且可以使用片上波特率发生器独立配置数据传输速度。

本节中，PCLK指PCLKA，TCLK指SCITCLK。

表26.1列出了SCI规格，图26.1显示了SCI的框图，表26.2列出了IO引脚。

Table 26.1 SCI规范(1of4)

Parameter		Specifications
模块数量		6 (SCIn (n = 0 to 4, 9))
串行通信模式		• Asynchronous • 时钟同步 • Simple IIC • 简单的SPI • 简单的LIN • 智能卡接口 • 曼彻斯特界面
传输速度		可通过片上波特率发生器指定比特率
Full-duplex communications		• 发送器：可使用双缓冲进行连续传输 • 接收器：使用双缓冲可以连续接收
Half-duplex communications		仅使用TXDn引脚即可实现半双工通信
数据传输		可选择LSB优先或MSB优先传输
通信终端用变频器（RXDn、TXDn）		每个端子可选逆变器（RXDn，TXDn）
中断源		发送结束、发送数据空、接收数据满、接收错误、接收数据就绪、地址匹配。BreakField检测输出，总线碰撞检测，主动边缘检测。 完成启动条件、重新启动条件或停止条件的生成。（对于简单IIC模式）
环回功能		可通过IP内部发送接收进行通信功能的自我诊断
同步器旁路功能		能够绕过总线时钟和操作时钟(TCLK)之间的同步电路
Module-stop function		每个通道可设置模块停止状态
暂停结束请求		SCI0地址不匹配(SCI0_DCUF)
时钟同步模式	数据长度	8 bits
	接收采样时序的调整	仅当使用内部时钟时，主模式下默认时序后可调整接收采样时序

Table 26.1 SCI specifications (2 of 4)

Parameter		Specifications
	Receive error detection	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)
	Double-speed mode	Baud rate generator double-speed mode is selectable
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins
	Transmission and reception	Selectable to 1-stage register or 16-stage FIFO
Asynchronous mode	Data length	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits
	Adjustment of receive sampling timing	Adjustable receive sampling timing before/after the default timing
	Adjustment of transmit timing	Adjustable edge timing of transmit waveform controlled by the setting value of registers.
	Parity	Even parity, odd parity, or no parity
	Receive error detection	• Parity error • Overrun error • Framing error
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pin and CTSn pin
	Transmission and reception	Selectable to 1-stage register or 16-stage FIFO
	Address match	Interrupt request/event output can be issued upon detecting a match between received data and the value in the compare match register
	Address mismatch (SCI0 only) receive data	Snooze end request can be issued when detecting a mismatch between the received data and the value in the compare match register
	Start-bit detection	Selectable to low level or falling edge detection
	Break detection	Breaks from framing errors detectable by read from CSR register
	Clock source	Selectable to internal or external clock
	Double-speed mode	Baud rate generator double-speed mode is selectable
	Multi-processor communications function	Serial communication enabled among multiple processors
	RS-485 driver control function	Output DEn signal to enable external transceiver transmit mode
	Noise cancellation	Digital noise filters included on signal paths from the RXDn pin inputs
Smart card interface mode	Error processing	Error signal can be automatically transmitted upon detecting a parity error during reception
		Data can be automatically retransmitted upon receiving an error signal during transmission
	Data type	Both direct and inverse convention supported
Manchester mode	Communication format	Manchester code with the preface and the Start Bit added
	Data length	7,8, or 9 bits
	Transmission stop bit	1 or 2 bits
	Parity function	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, framing, Manchester errors
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pin and CTSn pin
	Clock source	Only internal clock can be used.
	Double-speed mode	Baud rate generator double-speed mode is selectable

Table 26.1 SCI规范(2of4)

Parameter		Specifications
	接收错误检测	溢出错误
	时钟源	可选择内部时钟（主模式）或外部时钟（从模式）
	Double-speed mode	波特率发生器双速模式可选
	硬件流控制	可通过CTSn_RTSn引脚控制发送和接收
	传输和接收	可选择1级寄存器或16级FIFO
异步模式	数据长度	7、8或9位
	传输停止位	1或2位
	接收采样时序的调整	默认时序后可调接收采样时序
	发射时序的调整	由寄存器的设定值控制的可调整的发送波形边沿时序。
	Parity	偶校验、奇校验或无校验
	接收错误检测	• 奇偶校验错误 • 溢出错误 • 构图错误
	硬件流控制	可通过CTSn_RTSn引脚和CTSn引脚控制发送和接收
	传输和接收	可选择1级寄存器或16级FIFO
	地址匹配	检测到接收数据与比较匹配寄存器中的值匹配时，可以发出中断请求事件输出
	地址不匹配（仅SCI0）接收数据	当检测到接收到的数据与比较匹配寄存器中的值不匹配时，可以发出贪睡结束请求
	Start-bit detection	可选择低电平或下降沿检测
	断线检测	通过从CSR寄存器读取可检测到的帧错误中断
	时钟源	可选择内部或外部时钟
	Double-speed mode	波特率发生器双速模式可选
	多处理器通讯功能	在多个处理器之间启用串行通信
	RS-485驱动控制功能	输出DEn信号以启用外部收发器发送模式
	噪音消除	来自RXDn引脚输入的信号路径上包含数字噪声滤波器
智能卡接口方式	错误处理	在接收过程中检测到奇偶校验错误时可以自动发送错误信号
		传输过程中接收到错误信号可自动重传数据
	数据类型	支持直接和反向约定
曼彻斯特模式	通讯格式	添加了前言和起始位的曼彻斯特代码
	数据长度	7 8或9位
	传输停止位	1或2位
	奇偶校验函数	偶校验、奇校验或无校验
	接收错误检测	奇偶校验、超限、成帧、曼彻斯特错误
	硬件流控制	可通过CTSn_RTSn引脚和CTSn引脚控制发送和接收
	时钟源	只能使用内部时钟。
	Double-speed mode	波特率发生器双速模式可选

Table 26.1 SCI specifications (3 of 4)

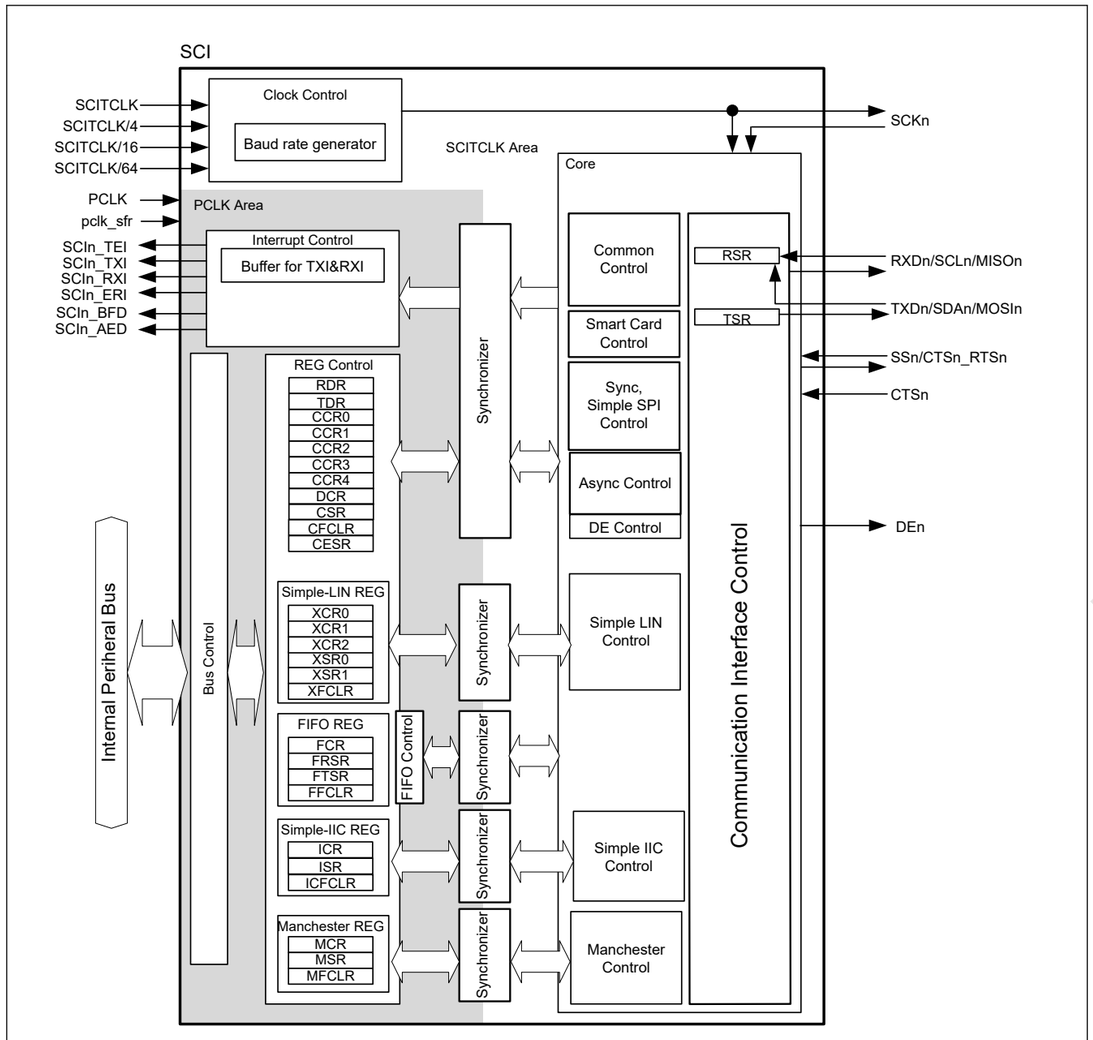
Parameter		Specifications
	Multi-processor communication function	Serial communication among multiple processors
	Manchester encoding / decoding function	Function to perform Manchester encoding / decoding of transmission / reception data and communicate using Manchester code
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters
	Preface setting / detection function	The function outputs the configured the preface pattern and detects it.
	Start Bit setting / detection function	The function outputs the configured the Start Bit pattern and detects it.
	Reception retiming function	Timing correction is performed for each bit of the received signal
Simple IIC mode	Transfer format	I^2C bus format (MSB-first only)
	Operating mode	Master (single-master operation only)
	Transfer rate	Up to 400 kbps
	Noise cancellation	The signal paths from input on the SCLn and SDAn pins incorporate digital noise filters and provide an adjustable interval for noise cancellation
Simple SPI mode	Data length	8 bits
	Error detection	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)
	Double-speed mode	Baud rate generator double-speed mode is selectable
	Transmission / Reception	Selectable either 1 stage register or 16-stage FIFO
	Adjustment of receive sampling timing	Adjustable receive sampling timing after the default timing in master mode only when using internal clock
	SSn input pin function	High impedance state can be invoked on the output pins by driving the SSn pin high.
	Clock settings	Configurable among four clock phase and clock polarity settings
Simple LIN	Start Frame Transmission	• Break Field output possible, Break Field output complete interrupt output possible • Bus collision detection possible, bus collision detection interrupt output possible
	Start Frame Reception	• Break Field detectable, Break Field detected interrupt output possible • Control Field 0/1 data comparison function • Control Field 1 can set two types of comparison data of primary and secondary • Priority interrupt bit can be set in Control Field 1 • Handling of Start Frames that do not include a Break Field • Handling of Start Frames that do not include a Control Field 0 • Bit rate measurement function
	Input/Output control function	• Selectable polarity for TXDn and RXDn signals • Selection of a digital filter for the RXDn signal • Half-duplex operation employing RXDn and TXDn signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDn
Bit rate modulation function		Error reduction through correction of outputs from the on-chip baud rate generator
Event link function		Error event output for receive error or error signal detection (SCIn_ERI) (n = 0 to 4, 9)
		Receive data full event output (SCIn_RXI) (n = 0 to 4, 9)
		Transmit data empty event output (SCIn_TXI) (n = 0 to 4, 9)
		Address match event output (SCIn_AM) (n = 0 to 4, 9)
		Active edge detection event output (SCIn_AED) (n = 0 to 4, 9)

Table 26.1 SCI规范(3of4)

Parameter		Specifications
	多处理器通讯功能	多个处理器之间的串行通信
	曼彻斯特编码解码功能	对发送接收数据进行曼彻斯特编码解码并使用曼彻斯特码进行通信的功能
	噪音消除	来自RXDn引脚输入的信号路径包含数字噪声滤波器
	前言设定检测功能	该函数输出配置的序言模式并检测它。
	起始位设置检测功能	该函数输出配置的起始位模式并检测它。
	接收重定时功能	对接收信号的每一位进行定时校正
简单IIC模式	传输格式	I2C总线格式（仅MSB优先）
	操作模式	主机（仅限单主机操作）
	传输率	高达400kbps
	噪音消除	来自SCLn和SDAn引脚输入的信号路径包含数字噪声滤波器，并提供可调节的噪声消除间隔
简单SPI模式	数据长度	8 bits
	错误检测	溢出错误
	时钟源	可选择内部时钟（主模式）或外部时钟（从模式）
	Double-speed mode	波特率发生器双速模式可选
	传输接收	可选择1级寄存器或16级FIFO
	接收采样时序的调整	仅当使用内部时钟时，主模式下默认时序后可调整接收采样时序
	SSn输入引脚功能	通过将SSn引脚驱动为高电平，可以在输出引脚上调用高阻抗状态。
	时钟设置	可在四个时钟相位和时钟极性设置之间进行配置
简单的LIN	开始帧传输	• 可中断场输出，可中断场输出完成中断输出 • 可进行总线碰撞检测，可进行总线碰撞检测中断输出
	开始帧接收	• 可检测断场，可检测断场中断输出 • ControlField01数据比较功能 • ControlField1可设置主次两种比较数据 • 可以在控制字段1中设置优先级中断位 • 处理不包含中断字段的起始帧 • 不包含控制字段0的起始帧的处理 • 比特率测量功能
	输入输出控制功能	• TXDn和RXDn信号的可选极性 • 为RXDn信号选择数字滤波器 • 采用在同一引脚上复用的RXDn和TXDn信号的半双工操作 • 通过RXDn接收的数据采样的可选时序
比特率调制功能		通过校正片上波特率发生器的输出来减少错误
事件链接功能		接收错误或错误信号检测的错误事件输出(SCIn_ERI)(n=0到4 9)
		接收数据满事件输出(SCIn_RXI)(n=0to4 9)
		发送数据空事件输出(SCIn_TXI)(n=0to4 9)
		地址匹配事件输出(SCIn_AM)(n=0to4 9)
		有效边沿检测事件输出(SCIn_AED)(n=0to4 9)

Table 26.1 SCI specifications (4 of 4)

Parameter	Specifications
	Transmit end event output (SCIn_TEI) (n = 0 to 4, 9)
TrustZone Filter	Security attribution can be set for each channels

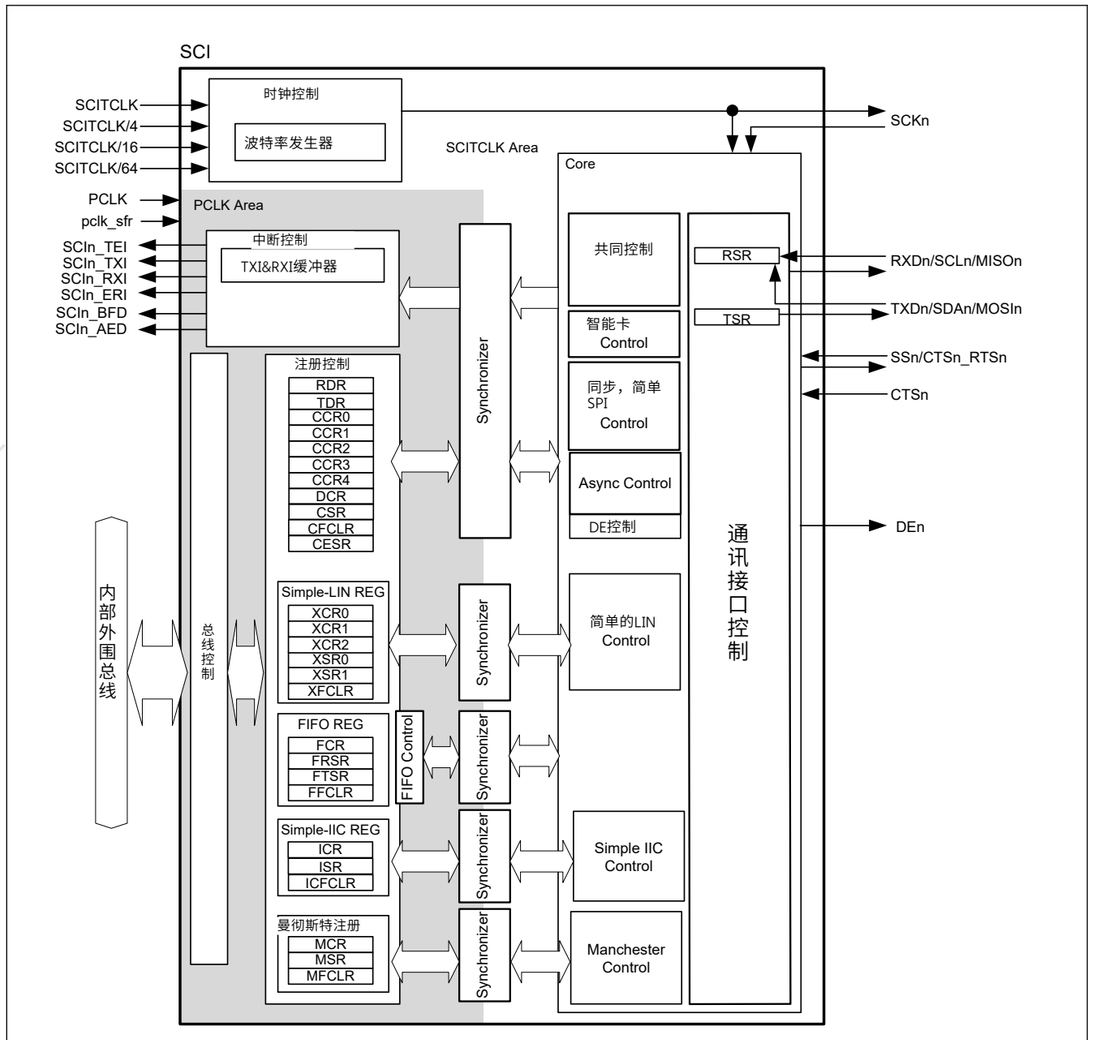


Note: n = 0 to 4, 9

Figure 26.1 SCI block diagram

Table 26.1 SCI规范（4个中的4个）

Parameter	Specifications
	发送结束事件输出(SCIn_TEI)(n=0to4 9)
TrustZone Filter	可以为每个通道设置安全属性



Note: n = 0 to 4, 9

Figure 26.1 SCI框图

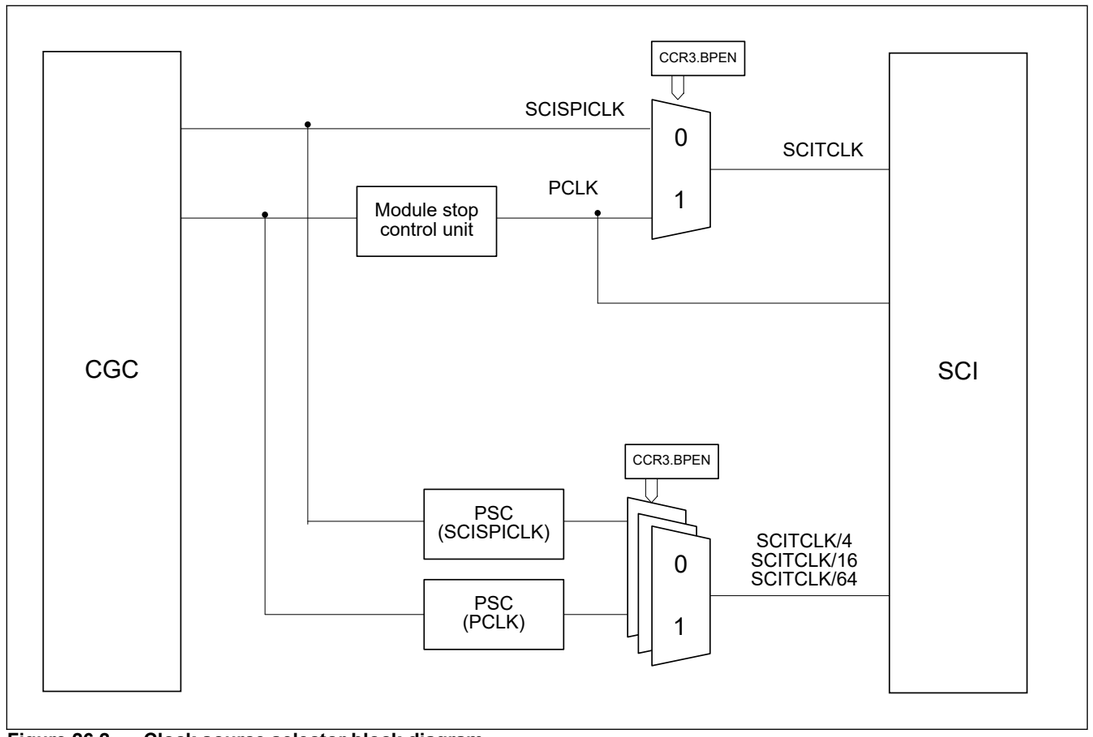


Figure 26.2 Clock source selector block diagram

Table 26.2 SCI I/O pins

Function	Pin name	Input/ Output	Description
SCIn (n = 0 to 4, 9)	RXDn/SCLn/MISOn	Input/ Output	SCIn receive data input SCIn I^2C clock input/output SCIn slave transmit data input/output
	TXDn/SDAn/MOSIn	Input/ Output	SCIn transmit data output SCIn I^2C data input/output SCIn master transmit data input/output
	SSn/CTSn_RTSn	Input/ Output	SCIn chip select input, active-low SCIn transfer start control input/output, active-low
	CTSn	Input	SCIn transfer start control input, active-low
	DEn	Output	Driver Enable signal output
	SCKn	Input/ Output	SCIn clock input/output

26.2 Register Descriptions

26.2.1 RSR : Receive Shift Register

RSR is a shift register that receives serial data input from the RXDn pin and converts it into parallel data. When one frame of data is received, the data is automatically transferred to the RDR register. The RSR register cannot be directly accessed by the CPU.

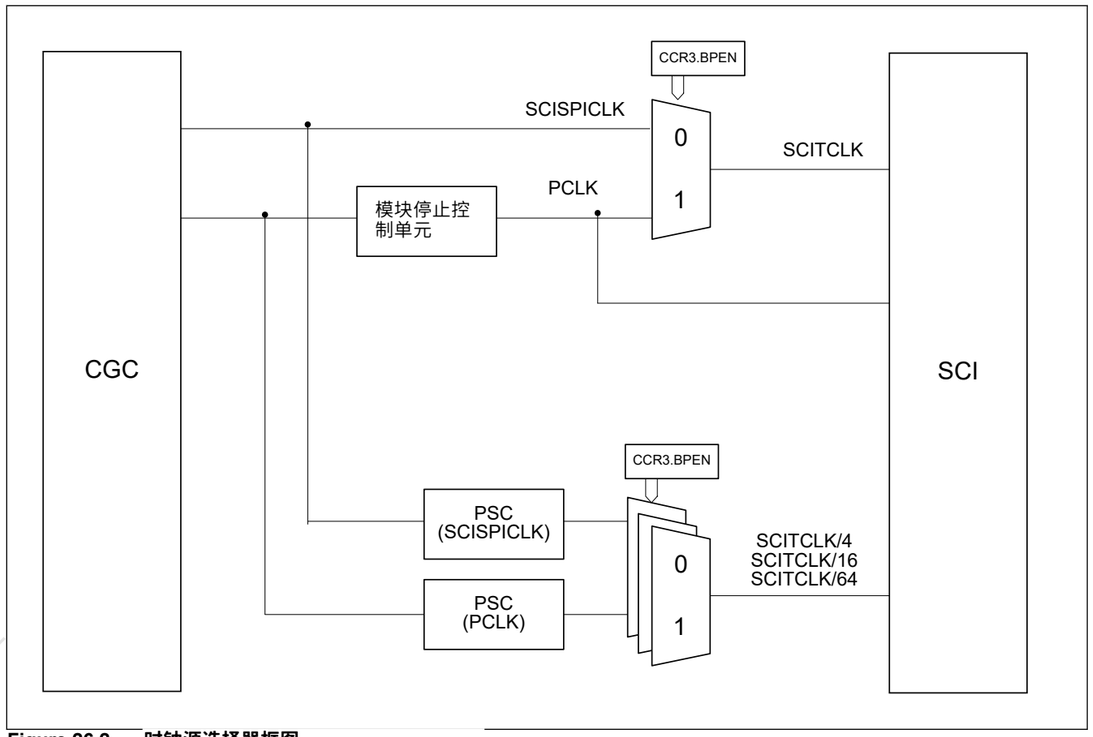


Figure 26.2 时钟源选择器框图

Table 26.2 SCIIO引脚

Function	引脚名称	Input/ Output	Description
SCIn (n = 0 to 4, 9)	RXDn/SCLn/MISOn	Input/ Output	SCIn接收数据输入 SCIn I^2C clock input/output SCIn从机发送数据输入输出
	TXDn/SDAn/MOSIn	Input/ Output	SCIn发送数据输出SCInI2C 数据输入输出 SCIn主机发送数据输入输出
	SSn/CTSn_RTSn	Input/ Output	SCIn片选输入，低电平有效 SCIn传输开始控制输入输出，低电平有效
	CTSn	Input	SCIn传输开始控制输入，低电平有效
	DEn	Output	驱动使能信号输出
	SCKn	Input/ Output	SCIn clock input/output

26.2 注册说明

26.2.1 RSR:接收移位寄存器

RSR是一个移位寄存器，它接收从RXDn引脚输入的串行数据并将其转换为并行数据。当接收到一帧数据时，数据会自动传输到RDR寄存器。CPU不能直接访问RSR寄存器。

26.2.2 RDR : Receive Data Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	FER	PER	—	—	ORER	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	FFER	FPER	DR	MPB	RDAT[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	Serial receive data RDAT is a 9-bit register for storing received data. Received data is stored in [6:0] when 7-bit data is selected, in [7:0] when 8-bit data is selected, and in [8:0] when 9-bit data is selected. And 0 is stored in the unused bit.	R
9	MPB	Multi-processor flag 0: Data transmission cycles 1: ID transmission cycles	R
10	DR	Receive data ready flag FRSR.DR can be read.	R
11	FPER	FIFO parity error flag Valid only in Asynchronous mode 0: There is no parity error in the data read from the receive-FIFO 1: There is parity error in the data read from the receive-FIFO	R
12	FFER	FIFO framing error flag Valid only in Asynchronous mode 0: There is no framing error in the data read from the receive-FIFO 1: There is framing error in the data read from the receive-FIFO	R
23:13	—	These bits are read as 0.	R
24	ORER	Overrun Error flag CSR.ORER can be read.	R
26:25	—	These bits are read as 0.	R
27	PER	Parity error flag CSR.PER can be read.	R
28	FER	Framing error flag CSR.FER can be read.	R
31:29	—	These bits are read as 0.	R

In FIFO mode (CCR3.FM = 1), this register is 16-stage FIFO buffer configuration.

RDAT[8:0] bit (Serial receive data)

After one frame of data is received, the received data is transferred from the RSR register to this register, thus allowing the RSR register to receive the next data.

The RSR and RDR registers have a double-buffered construction to enable continuous reception.

For Non-FIFO mode, read RDR only once when a receive data full interrupt (SCIn_RXI) request is issued. Without reading received data from RDR, if the next one frame is received, an overrun error occurs.

For FIFO mode, continuous reception is executed until 16 stages are stored. If data is read when there is no received data in the receive-FIFO(RDR), the value is undefined. When the receive-FIFO (RDR) are full of received data, subsequent serial receive data is lost.

The CPU cannot write to RDR.

26.2.2 RDR:接收数据寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	FER	PER	—	—	ORER	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	FFER	FPER	DR	MPB	RDAT[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	串口接收数据 RDAT是一个9位寄存器，用于存储接收到的数据。 选择7位数据时，接收数据存储在[6:0]中，选择8位数据时存储在[7:0]中，选择9位数据时存储在[8:0]中。0存储在未使用的位中。	R
9	MPB	Multi-processor flag 0：数据传输周期1：ID传输周期	R
10	DR	可以读取接收数据就绪 标志FRSR.DR。	R
11	FPER	FIFO奇偶校验错误标志 仅在异步模式下有效 0：从接收FIFO读取的数据没有奇偶校验错误1：从接收FIFO读取的数据有奇偶校验错误	R
12	FFER	FIFO成帧错误标志 仅在异步模式下有效 0：从接收FIFO读取的数据没有帧错误1：从接收FIFO读取的数据有帧错误	R
23:13	—	这些位读为0。	R
24	ORER	溢出错误标志 可以读取CSR.ORER。	R
26:25	—	这些位读为0。	R
27	PER	奇偶校验错误标志 可以读取CSR.PER。	R
28	FER	帧错误标志 可以读取CSR.FER。	R
31:29	—	这些位读为0。	R

在FIFO模式（CCR3.FM=1）下，该寄存器为16级FIFO缓冲器配置。

RDAT[8:0]位（串行接收数据）

接收到一帧数据后，将接收到的数据从RSR寄存器传送到该寄存器，从而允许RSR寄存器接收下一个数据。

RSR和RDR寄存器具有双缓冲结构以实现连续接收。

对于非FIFO模式，在发出接收数据完整中断(SCIn_RXI)请求时仅读取一次RDR。如果不从RDR读取接收到的数据，如果接收到下一帧，则会发生溢出错误。

对于FIFO模式，执行连续接收直到存储16个阶段。如果在接收FIFO(RDR)中没有接收到数据时读取数据，则该值未定义。当接收FIFO(RDR)充满接收数据时，后续串行接收数据将丢失。

CPU无法写入RDR。

0 is stored in the bit position which isn't received (RDR.bit8 or RDR.bit7) at the time of 7bit or 8bit communication of Asynchronous and Manchester mode.

MPB bit (Multi-processor flag)

In Asynchronous mode and Manchester mode, during multi-processor communication (CCR3.MP = 1), the value of the multi-processor bit corresponding to the received data (RDAT[8:0]) can be read.

FPER bit (FIFO parity error flag)

Indicates whether the data read from the receive-FIFO has a parity error.

0 is stored for non-FIFO mode.

FFER bit (FIFO framing error flag)

Indicates whether the data read from receive-FIFO has a framing error.

0 is stored for non-FIFO mode.

26.2.3 TDR : Transmit Data Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TSYNC	—	—	MPBT	TDAT[8:0]								
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	Serial transmit data TDAT is a 9-bit register for setting transmit data. Transmit data is set in [6:0] when 7-bit data is selected, in [7:0] when 8-bit data is selected, and in [8:0] when 9-bit data is selected. When byte access, write TDR [15:8] and then write TDR [7:0].	R/W
9	MPBT	Multi-processor transfer bit flag Value of the multi-processor bit in the transmission frame. This bit is use in Asynchronous and Manchester mode. When writing to this bit when not used, write the initial value. 0: Data transmission cycles 1: ID transmission cycles	R/W
11:10	—	These bits are read as 1. The write value should be 1.	R/W
12	TSYNC	Transmit SYNC data It is valid when MCR.SBSEL = 1 and MCR.SYNSEL = 1 in Manchester mode. When this bit is not used, write the initial value. 0: The Start Bit is transmitted as DATA SYNC. 1: The Start Bit is transmitted as COMMAND SYNC.	R/W
31:13	—	These bits are read as 1. The write value should be 1.	R/W

In FIFO mode (CCR3.FM = 1), this register is 16-stage FIFO buffer configuration.

TDAT[8:0] bit (Serial transmit data)

The TDR is a 9-bit register for storing transmit data.

When empty space is detected in the TSR register, the transmit data stored in the TDR registers is transferred to TSR, and transmitting is started.

0存储在异步和曼彻斯特模式的7位或8位通信时未接收到的位位置（RDR.bit8或RDR.bit7）。

MPB bit (Multi-processor flag)

在异步模式和曼彻斯特模式下，在多处理器通信期间（CCR3.MP=1），可以读取接收到的数据对应的多处理器位（RDAT[8:0]）的值。

FPER位（FIFO奇偶校验错误标志）

指示从接收FIFO读取的数据是否有奇偶校验错误。

0存储为非FIFO模式。

FFER位（FIFO帧错误标志）

指示从接收FIFO读取的数据是否有帧错误。

0存储为非FIFO模式。

26.2.3 TDR：发送数据寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TSYNC	—	—	MPBT	TDAT[8:0]								
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	串行传输数据 TDAT是一个9位寄存器，用于设置发送数据。 Transmitdataissetin[6:0]when7-bitdataisselected in[7:0]when8-bitdataisselected andin[8:0]when9-bitdataisselected.字节访问时，先写入TDR[15:8]，再写入TDR[7:0]。	R/W
9	MPBT	多处理器传输位标志 传输帧中多处理器位的值。该位用于异步和曼彻斯特模式。不使用时写入该位时，写入初始值。 0：数据传输周期1：ID传输周期	R/W
11:10	—	这些位被读取为1。写入值应为1。	R/W
12	TSYNC	传输同步数据 在曼彻斯特模式下，当MCR.SBSEL=1且MCR.SYNSEL=1时有效。不使用该位时，写入初始值。 0：起始位作为DATASYNC发送。1：起始位作为COMMANDSYNC发送。	R/W
31:13	—	这些位被读取为1。写入值应为1。	R/W

在FIFO模式（CCR3.FM=1）下，该寄存器为16级FIFO缓冲器配置。

TDAT[8:0]位（串行发送数据）

TDR是一个9位寄存器，用于存储发送数据。

当在TSR寄存器中检测到空空间时，存储在TDR寄存器中的发送数据被传送到TSR，并开始发送。

The TSR and TDR registers have a double-buffered construction to realize continuous reception. When the next data to be transmitted is stored in TDR after one frame of data has been transmitted, the transmitting operation is continued by transfer to the TSR register.

When the SCI detects that the transmit shift register (TSR) is empty, it transmits data written in the transmit-FIFO (TDR) into TSR and starts serial transmission. Continuous serial transmission is executed until there is no transmit data left in the transmit-FIFO (TDR).

For non-FIFO mode, when a transmit data empty interrupt (SCIn_TXI) request is issued and CCR0.TE is 1, write transmit data to the TDR only once.

For FIFO mode, when transmit-FIFO is full of transmit data 16 frames, no more data can be written. If writing of new data is attempted, the data is ignored.

The TDR register can always be read / written from the CPU. And when byte access, write TDR[15:8] and then write TDR[7:0].

MPBT bit (Multi-processor transfer bit flag)

Selects the multi processor bit of transmit frame.

TSYNC bit (Transmit SYNC data)

When Manchester mode and MCR.SBSEL = 1 and MCR.SYNSEL = 1, the type of SYNC selected according to this bit becomes the Start Bit of the transmission frame.

26.2.4 TSR : Transmit Shift Register

TSR is a shift register that transmits serial data. To perform serial data transmission, the SCI first automatically transfers transmit data from TDR to TSR, then sends the data to the TXDn pin. The CPU cannot directly access the TSR.

26.2.5 CCR0 : Common Control Register 0

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	SSE	—	—	TEIE	TIE	—	—	—	RIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IDSEL	DCME	MPIE	—	—	—	TE	—	—	—	RE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RE	Receive Enable 0: Serial reception is disabled 1: Serial reception is enabled	R/W*1 *3
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	TE	Transmit Enable 0: Serial transmission is disabled 1: Serial transmission is enabled	R/W*1
7:5	—	These bits are read as 0. The write value should be 0.	R/W

TSR和TDR寄存器具有双缓冲结构以实现连续接收。在发送一帧数据后，当下一个要发送的数据存储在TDR中时，通过传输到TSR寄存器继续发送操作。

当SCI检测到发送移位寄存器(TSR)为空时，它将写入发送FIFO(TDR)的数据发送到TSR并开始串行发送。执行连续串行传输，直到传输FIFO(TDR)中没有传输数据。

对于非FIFO模式，当发出发送数据空中断(SCIn_TXI)请求且CCR0.TE为1时，仅将发送数据写入TDR一次。

对于FIFO模式，当传输FIFO充满传输数据16帧时，不能再写入数据。如果尝试写入新数据，则忽略该数据。

TDR寄存器总是可以从CPU读取写入。并且当字节访问时，写入TDR[15:8]然后写入TDR[7:0].

MPBT位（多处理器传输位标志）

选择发送帧的多处理器位。

TSYNC位（发送SYNC数据）

当曼彻斯特模式和MCR.SBSEL=1且MCR.SYNSEL=1时，根据该位选择的SYNC类型成为传输帧的起始位。

26.2.4 TSR：发送移位寄存器

TSR是传送串行数据的移位寄存器。为了进行串行数据传输，SCI首先自动将发送数据从TDR传输到TSR，然后将数据发送到TXDn引脚。CPU不能直接访问TSR。

26.2.5 CCR0:公共控制寄存器0

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	SSE	—	—	TEIE	TIE	—	—	—	RIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IDSEL	DCME	MPIE	—	—	—	TE	—	—	—	RE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RE	接收启用 0：禁止串行接收1：允许串行接收	R/W*1 *3
3:1	—	这些位被读取为0。写入值应为0。	R/W
4	TE	发送启用 0：禁止串行传输1：允许串行传输	R/W*1
7:5	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
8	MPIE	Multi-Processor Interrupt Enable Valid in Asynchronous mode and Manchester mode when CCR3.MP is 1. This bit should set 0 in smart card interface mode. 0: Non-Multi-Processor reception 1: Multi -Processor reception When the data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags to 1 is disabled. When the data with the multiprocessor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and non-multi-processor reception is resumed. If you want to continue receiving operation using the multiprocessor function, set this bit to 1 sufficiently earlier than receiving the STOP bit of the next received frame. (Consider the synchronization delay time.)	R/W*2
9	DCME	Data Compare Match Enable Valid only in Asynchronous mode 0: Address match function is disabled 1: Address match function is enabled	R/W*2
10	IDSEL	ID frame select Valid only in Asynchronous mode with multi-processor 0: It's always compared data in spite of the value of the MPB bit. 1: It's compared data when the MPB bit is 1 (ID frame) only.	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W
16	RIE	Receive Interrupt Enable 0: SCIn_RXI and SCIn_ERI interrupt requests are disabled 1: SCIn_RXI and SCIn_ERI interrupt requests are enabled	R/W
19:17	—	These bits are read as 0. The write value should be 0.	R/W
20	TIE	Transmit Interrupt Enable 0: SCIn_TXI interrupt request is disabled 1: SCIn_TXI interrupt request is enabled	R/W
21	TEIE	Transmit End Interrupt Enable This bit should set 0 in smart card interface mode. 0: SCIn_TEI interrupt request is disabled 1: SCIn_TEI interrupt request is enabled	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W
24	SSE	SSn Pin Function Enable Valid in Simple SPI mode. In slave mode (CCR3.CKE[1:0] = 1x), set 1 to this bit. 0: SSn pin function is disabled. 1: SSn pin function is enabled.	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. In clock-synchronous mode (CCR3.MOD[2:0] = 010b), Simple SPI mode (CCR3.MOD[2:0] = 011b), and Simple IIC mode (CCR3.MOD[2:0] = 100b), 1 can be written only when TE = 0 and RE = 0. After setting TE or RE to 1, only 0 can be written in TE and RE In other mode, writing is enabled under any condition.

Note 2. This bit is a bit that is cleared by hardware. Note that writing to a bit other than this bit with a bit manipulation instruction may cause this bit to be unintentionally set to 1 by a read-modify-write operation.

Note 3. In clock synchronous mode and Simple SPI mode, receive only setting is prohibited in the internal clock (master mode) (TE = 0 and RE = 1 setting prohibited).

RE bit (Receive Enable)

Enables or disables serial receive operation.

When this bit is set to 1, serial reception becomes possible after the synchronization delay time has elapsed in asynchronous mode or the synchronous clock input in clock synchronous mode or the neg-edge of RXDn in manchester mode or start bit in smart-card-interface-mode.

Note that CCR3 should be set prior to setting the RE bit to 1 in order to designate the reception format.

Except smart-card-interface-mode, even if reception is halted by setting the RE bit to 0, the CSR. RDRF, FER, PER, ORER, MSR.MER, SBER, SYER, PFER, FRSR. DR flags are not affected, and the previous values is retained. In smart-card-interface-mode, even if reception is halted by setting the RE bit to 0, the CSR.FER, PER, ORER flags are not affected and the previous value is retained. Also, to stop the reception operation, synchronization delay time will be required from when the RE bit is set to 0 until the reception operation is stopped.

Bit	Symbol	Function	R/W
8	MPIE	多处理器中断使能 当CCR3.MP为1时，在异步模式和曼彻斯特模式下有效。 该位在智能卡接口模式下应设置为0。 0：非多处理器接收1：多处理器接收 当接收到多处理器位设置为0的数据时，不读取数据，并且将状态标志设置为1被禁用。当接收到多处理器位设置为1的数据时，MPIE位自动清0，恢复非多处理器接收。如果要继续使用多处理器功能进行接收操作，请在接收到下一接收帧的STOP位之前将该位设置为1。（考虑同步延迟时间。）	R/W*2
9	DCME	数据比较匹配启用 仅在异步模式下有效 0：地址匹配功能关闭1：地址匹配功能打开	R/W*2
10	IDSEL	身份证框选择 仅在多处理器异步模式下有效 0：不管MPB位的值如何，总是比较数据。1：仅当MPB位为1（ID帧）时比较数据。	R/W
15:11	—	这些位被读取为0。写入值应为0。	R/W
16	RIE	接收中断使能 0：禁止SCIn_RXI和SCIn_ERI中断请求1：使能SCIn_RXI和SCIn_ERI中断请求	R/W
19:17	—	这些位被读取为0。写入值应为0。	R/W
20	TIE	发送中断使能 0：禁止SCIn_TXI中断请求1：使能SCIn_TXI中断请求	R/W
21	TEIE	发送结束中断使能 该位在智能卡接口模式下应设置为0。 0：禁止SCIn_TEI中断请求1：使能SCIn_TEI中断请求	R/W
23:22	—	这些位被读取为0。写入值应为0。	R/W
24	SSE	SSn引脚功能使能在简单SPI模式下有效。 在从机模式下（CCR3.CKE[1:0]=1x），将该位设置为1。 0：禁用SSn引脚功能。1：SSn引脚功能使能。	R/W
31:25	—	这些位被读取为0。写入值应为0。	R/W

注1.在时钟同步模式(CCR3.MOD[2:0]=010b)、简单SPI模式(CCR3.MOD[2:0]=011b)和简单IIC模式下(CCR3.MOD[2:0]=100b)，只有TE=0和RE=0时才能写1。设置TE或RE为1后，TE和RE只能写0，其他模式下，写为在任何条件下启用。

注2.该位由硬件清零。请注意，使用位操作指令写入该位以外的位可能会导致该位被读取-修改-写入操作无意中设置为1。

注3.在时钟同步模式和简单SPI模式下，内部时钟（主机模式）（TE=0和RE=1禁止设置）。

RE位（接收使能）

启用或禁用串行接收操作。

当此位设置为1时，在异步模式下经过同步延迟时间或时钟同步模式下同步时钟输入或曼彻斯特模式下RXDn的下降沿或智能卡接口中的起始位之后，串行接收变为可能-模式。

请注意，为了指定接收格式，应在将RE位设置为1之前设置CCR3。

除了智能卡接口模式，即使通过将RE位设置为0来停止接收，CSR。RDRF、FER、PER、ORER、MSR.MER、SBER、SYER、PFER、FRSR。DR标志不受影响，并且保留以前的值。在智能卡接口模式下，即使通过将RE位设置为0来停止接收，CSR.FER、PER、ORER标志也不受影响，并且保留之前的值。此外，为了停止接收操作，从RE位设置为0到停止接收操作需要同步延迟时间。

TE bit (Transmit Enable)

Enables or disables serial transmission.

When this bit is set to 1, serial transmission becomes possible after the synchronization delay time has elapsed. After the synchronization delay time, transmission is started by writing transmit data to TDR. Note that CCR3 should be set prior to setting the TE bit to 1 in order to designate the transmission format. In addition, the synchronization delay time is required until the transmission control circuit is stopped after the TE bit is set to 0.

MPIE bit (Multi-Processor Interrupt Enable)

When this bit is set to 1 and the data with the multi-processor bit set to 0 is received, the data is not read and setting the status flags (CSR.RDRF, ORER, FER, FRSR, DR, MSR.MER, SYER, PFER, SBER) are disabled.

When the data with the multi-processor bit set to 1 is received, the MPIE is automatically cleared to 0, and normal reception is resumed. For details, refer to section 26.4. Multi-Processor Communication Function. If you want to continue receiving operation using the multiprocessor function, set this bit to 1 sufficiently earlier than receiving the STOP bit of the next received frame.

When the receive data includes the MPB bit set to 0, the receive data is not transferred from the RSR to the RDR, a receive error is not detected, and setting the flags ORER, FER, MER, SYER, PFER, and SBER to 1 is disabled.

When the receive data includes the MPB bit set to 1, the MPB bit is set to 1, the MPIE bit is automatically cleared to 0, the SCIn_RXI and SCIn_ERI interrupt requests are enabled (if CCR0.RIE is set to 1), and setting the flags ORER, FER, MER, SYER, PFER, and SBER to 1 is enabled.

MPIE should be set to 0 if multi-processor communications function is not to be used.

DCME bit (Data Compare Match Enable)

It can select whether the Address match function (data compare match function) uses or not.

When DCME is 1, if SCI detects the match to the comparison data (CCR4.CMPD) with receive data, DCME is cleared automatically, and after that, SCI operation mode will be receive mode without data compare match function.

Refer to section 26.3.6. Address Match (Receive Data Match Detection) Function.

The write value should be 0 other than asynchronous mode.

IDSEL bit (ID frame select)

It can select whether it is compared in spite of the value of MPB bit or it's compared only the data of MPB bit = 1 (ID frame) when the Address match function is valid. Please set at the same time as DCME.

RIE bit (Receive Interrupt Enable)

Enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

SCIn_RXI and SCIn_ERI interrupt request is disabled by setting the RIE bit to 0.

An SCIn_ERI interrupt request can be canceled by reading 1 from the CSR.ORER, FER, or PER and then setting the flag to 0 or setting the RIE bit to 0.

In the case of Manchester mode, the MER, SYER, PFER and SBER flags are also the cause of SCIn_ERI interrupt request, so the same processing is necessary. For details of these flags, see section 26.2.12. MCR : Manchester Control Register and section 26.2.21. MSR : Manchester Status Register.

TIE bit (Transmit Interrupt Enable)

Enables or disables SCIn_TXI interrupt request.

An SCIn_TXI interrupt request is disabled by setting the TIE bit to 0. At the beginning of transmission, set 1 to CCR0.TE and CCR0.TIE simultaneously. Then the SCIn_TXI interrupt request is generated.

TEIE bit (Transmit End Interrupt Enable)

Enables or disables a SCIn_TEI interrupt request. A SCIn_TEI interrupt request is disabled by setting the TEIE bit to 0.

In simple IIC mode, the SCIn_TEI is allocated to the interrupt on completion of issuing a start, restart, or stop condition (STIn). In this case, the TEIE bit can be used to enable or disable the STIn.

TE位（发送使能）

启用或禁用串行传输。

当该位设置为1时，经过同步延迟时间后可以进行串行传输。在同步延迟时间之后，通过将发送数据写入TDR开始发送。请注意，为了指定传输格式，应在将TE位设置为1之前设置CCR3。此外，在将TE位设置为0后，直到传输控制电路停止为止需要同步延迟时间。

MPIE位（多处理器中断允许）

当该位设置为1并且接收到多处理器位设置为0的数据时，不读取数据并设置状态标志（CSR.RDRF、ORER、FER、FRSR、DR、MSR.MER、SYER PFER SBER)被禁用。

当接收到多处理器位设置为1的数据时，MPIE自动清零，恢复正常接收。详情请参阅26.4节。多处理器通信功能。如果要继续使用多处理器功能进行接收操作，请在接收到下一接收帧的STOP位之前将该位设置为1。

当接收数据包括MPB位设置为0时，接收数据不从RSR传输到RDR，未检测到接收错误，并将标志ORER、FER、MER、SYER、PFER和SBER设置为1被禁用。

当接收数据包括MPB位设置为1时，MPB位设置为1，MPIE位自动清为0，启用SCIn_RXI和SCIn_ERI中断请求（如果CCR0.RIE设置为1），并设置标志ORER、FER、MER，
启用SYER、PFER和SBER为1。

如果不使用多处理器通信功能，则MPIE应设置为0。

DCME位（数据比较匹配使能）

可以选择是否使用地址匹配功能（数据比较匹配功能）。

当DCME为1时，如果SCI检测到比较数据（CCR4.CMPD）与接收数据匹配，则DCME自动清零，之后SCI操作模式将变为无数据比较匹配功能的接收模式。

请参阅第26.3.6节。地址匹配（接收数据匹配检测）功能。

除异步模式外，写入值应为0。

IDSEL位（ID帧选择）

当地址匹配功能有效时，可以选择不管MPB位的值是比较还是只比较MPB位=1（ID帧）的数据。请与DCME同时设置。

RIE位（接收中断允许）

启用或禁用SCIn_RXI和SCIn_ERI中断请求。

通过将RIE位设置为0来禁用SCIn_RXI和SCIn_ERI中断请求。

SCIn_ERI中断请求可以通过从CSR.ORER、FER或PER读取1然后将标志设置为0或将RIE位设置为0来取消。

在曼彻斯特模式的情况下，MER、SYER、PFER和SBER标志也是SCIn_ERI中断请求的原因，因此需要进行相同的处理。有关这些标志的详细信息，请参阅第26.2.12节。MCR：曼彻斯特控制寄存器和第26.2.21节。MSR：曼彻斯特状态寄存器。

TIE位（发送中断允许）

启用或禁用SCIn_TXI中断请求。

通过将TIE位设置为0来禁用SCIn_TXI中断请求。在传输开始时，同时将CCR0.TE和CCR0.TIE设置为1。然后产生SCIn_TXI中断请求。

TEIE位（发送结束中断允许）

启用或禁用SCIn_TEI中断请求。通过将TEIE位设置为0来禁用SCIn_TEI中断请求。

在简单IIC模式下，SCIn_TEI在完成发出启动、重启或停止条件(STIn)时分配给中断。在这种情况下，TEIE位可用于启用或禁用STIn。

SSE bit (SSn Pin Function Enable)

Set this bit to 1 if the SSn pin is to be used in control of transmission and reception (in simple SPI mode).

Set this bit to 0 in any other mode. Do not set both the SSE and CTSE bits to enabled (even if this setting is made, operation is the same as that when these bits are set to 0).

In the slave mode (CCR3.CKE[1:0] = 10 or 11), SSE should be set 1.

In the master mode (CCR3.CKE[1:0] = 00 or 01) and single-master, the SSn pin on the master side is not required to control reception and transmission, so SSE should be set 0.

26.2.6 CCR1 : Common Control Register 1

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	NFEN	—	NFCS[2:0]			—	—	—	SHARPS	—	—	—	SPLP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	RINV	TINV	—	—	PM	PE	—	—	SPB2IO	SPB2DT	—	—	CTSPEN	CTSE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
0	CTSE	CTS Enable 0: CTS function is disabled (RTS output function is enabled). 1: CTS function is enabled.	R/W
1	CTSPEN	CTS external pin Enable 0: Alternate setting to use CTS and RTS functions as either one terminal 1: Dedicated setting for separately using CTS and RTS functions with 2 terminals	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	SPB2DT	Serial port break data select The output level of TXDn terminal is selected when CCR0.TE = 0 and SPB2IO = 1.*1 0: When TINV is 0, Low level is output in TXDn terminal. When TINV is 1, High level is output in TXDn terminal. 1: When TINV is 0, High level is output in TXDn terminal. When TINV is 1, Low level is output in TXDn terminal.	R/W
5	SPB2IO	Serial port break I/O It's selected whether the value of SPB2DT is output to TXDn terminal when CCR0.TE = 0.*1 0: The value of SPB2DT bit isn't output in TXDn terminal. 1: The value of SPB2DT bit is output in TXDn terminal.	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
8	PE	Parity Enable Valid only in Asynchronous mode and Manchester mode. In Smart Card Interface mode, set 1 to this bit. 0: When transmitting: Do not add parity bit When receiving: Do not check parity bit 1: When transmitting: Add parity bit When receiving: Check parity bit	R/W
9	PM	Parity Mode Valid only when the PE bit is 1 0: Selects even parity 1: Selects odd parity	R/W
11:10	—	These bits are read as 0. The write value should be 0.	R/W

SSE位（SSn引脚功能使能）

如果SSn引脚用于控制发送和接收（在简单SPI模式下），则将该位设置为1。

在任何其他模式下将此位设置为0。不要将SSE和CTSE位都设置为使能（即使进行了此设置，操作与这些位设置为0时的操作相同）。

在从机模式下（CCR3.CKE[1:0]=10或11），SSE应设置为1。

在主机模式（CCR3.CKE[1:0]=00或01）和单主机下，主机侧的SSn引脚不需要控制接收和发送，因此SSE应设置为0。

26.2.6 CCR1：公共控制寄存器1

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	NFEN	—	NFCS[2:0]			—	—	—	SHARPS	—	—	—	SPLP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	RINV	TINV	—	—	PM	PE	—	—	SPB2IO	SPB2DT	—	—	CTSPEN	CTSE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
0	CTSE	CTS Enable 0：禁用CTS功能（启用RTS输出功能）。1：CTS功能使能。	R/W
1	CTSPEN	CTS外部引脚使能 0：将CTS和RTS功能作为一个端子使用的交替设置1：单独使用2个端子的CTS和RTS功能的专用设置	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	SPB2DT	串口中断数据选择 当CCR0.TE=0且SPB2IO=1时选择TXDn端子的输出电平。*1 0：当TINV为0时，TXDn端输出低电平。当TINV为1时，TXDn端输出高电平。 1：当TINV为0时，TXDn端输出高电平。当TINV为1时，TXDn端输出低电平。	R/W
5	SPB2IO	串口中断IO 选择当CCR0.TE=0时SPB2DT的值是否输出到TXDn端子。*1 0：TXDn端不输出SPB2DT位的值。1：SPB2DT位的值在TXDn端输出。	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
8	PE	奇偶校验使能 仅在异步模式和曼彻斯特模式下有效。在智能卡接口模式下，将此位设置为1。 0：发送时：不加校验位接收时：不校验校验位 1：发送时：添加校验位接收时：校验校验位	R/W
9	PM	奇偶校验模式 仅当PE位为1时有效 0：选择偶校验1：选择奇校验	R/W
11:10	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
12	TINV	TXD invert 0: Transmit data is not inverted and output to TXDn.*2 1: Transmit data is inverted and output to TXDn.	R/W
13	RINV	RXD invert 0: Received data from RXDn is not inverted and input.*2 1: Received data from RXDn is inverted and input.	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W
16	SPLP	Loopback Control It can be used when internal clock operation in asynchronous mode, internal mode operation in Manchester mode, internal clock operation in clock synchronous mode. 0: Normal mode 1: Loopback mode	R/W
19:17	—	These bits are read as 0. The write value should be 0.	R/W
20	SHARPS	Half-duplex communication select In the Simple IIC mode, in the Smart Card Interface Mode or in the Simple SPI mode, this bit should be set 0. 0: TXDn terminal, RXDn terminal independent 1: TXDn / RXDn terminal combination use (Half-duplex communication using TXDn pin)	R/W
23:21	—	These bits are read as 0. The write value should be 0.	R/W
26:24	NFCS[2:0]	Noise Filter Clock Select Valid in Asynchronous mode and Manchester mode, Simple LIN mode, and Simple IIC mode. In Simple IIC mode, 000 setting is prohibited. The on-chip baud rate generator source clock means the clock selected by CCR2.CKS [1:0]. Select for the noise filter's clock source. 0 0 0: The base clock signal divided by 1. 0 0 1: The on-chip baud rate generator source clock divided by 1. 0 1 0: The on-chip baud rate generator source clock divided by 2. 0 1 1: The on-chip baud rate generator source clock divided by 4. 1 0 0: The on-chip baud rate generator source clock divided by 8. others: Setting prohibited.	R/W
27	—	These bits are read as 0. The write value should be 0.	R/W
28	NFEN	Digital Noise Filter Function Enable Valid in Asynchronous mode, manchester mode, Simple LIN mode and Simple IIC mode 0: In Asynchronous, Manchester, Simple LIN mode: Disable noise cancellation function for RXDn input signal In Simple IIC mode: Disable noise cancellation function for SCLn and SDAn input signals 1: In Asynchronous, Manchester, Simple LIN mode: Enable noise cancellation function for RXDn input signal In Simple IIC mode: Enable noise cancellation function for SCLn and SDAn input signals	R/W
31:29	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Please use this bit in asynchronous mode and manchester mode only. Movement by other mode isn't guaranteed.
Note 2. RINV/TINV should be set 0 in smart card interface mode and simple IIC mode.

CTSE bit (CTS Enable)

Set this bit to 1 if the SSn pin is to be used for inputting of the CTSn control signal to control of transmission and reception. The RTSn signal is output when this bit is set to 0. Set this bit to 0 in smart card interface mode, simple SPI mode, Simple LIN mode, and simple IIC mode. Do not set both the CTSE and SSE bits to enabled (even if this setting is made, operation is the same as that when these bits are set to 0).

CTSPEN bit (CTS external pin Enable)

When CTSE is 1, select the terminals usage method when using the CTS and RTS functions. Set this bit to 1 when assigning the CTS/RTS function to 2 terminals and using them at the same time. Set it to 0 except in Asynchronous and Manchester modes.

Bit	Symbol	Function	R/W
12	TINV	TXD invert 0：发送数据不反相并输出到TXDn。*2 1：发送数据反转并输出到TXDn。	R/W
13	RINV	RXD invert 0：从RXDn接收的数据不反相输入。*2 1：从RXDn接收到的数据被反转并输入。	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W
16	SPLP	Loopback Control 它可以用于异步模式下的内部时钟操作、曼彻斯特模式下的内部模式操作、时钟同步模式下的内部时钟操作。 0：正常模式1：环回模式	R/W
19:17	—	这些位被读取为0。写入值应为0。	R/W
20	SHARPS	半双工通讯选择 在简单IIC模式、智能卡接口模式或简单SPI模式下，该位应设置为0。 0：TXDn端子、RXDn端子独立1：TXDnRXDn端子组合使用 （使用TXDn引脚的半双工通信）	R/W
23:21	—	这些位被读取为0。写入值应为0。	R/W
26:24	NFCS[2:0]	噪声滤波器时钟选择 在异步模式和曼彻斯特模式、简单LIN模式和简单IIC模式下有效。在SimpleIIC模式下，禁止000设置。 片内波特率发生器源时钟是指由CCR2.CKS[1:0]选择的时钟。选择噪声滤波器的时钟源。 000：基本时钟信号除以1。001：片内波特率发生器源时钟除以1。010：片内波特率发生器源时钟除以2。011：片内波特率发生器源时钟除以4。100：片内波特率发生器源时钟除以8。 其他：禁止设置。	R/W
27	—	这些位被读取为0。写入值应为0。	R/W
28	NFEN	数字噪声滤波器功能启用 在异步模式、曼彻斯特模式、简单LIN模式和简单IIC模式下有效 0：在异步、曼彻斯特、简单LIN模式下：禁用RXDn输入信号的噪声消除功能在简单IIC模式下：禁用SCLn和SDAn输入信号的噪声消除功能 1：在Asynchronous、Manchester、SimpleLIN模式下：使能RXDn输入信号的噪声消除功能在SimpleIIC模式下：使能SCLn和SDAn输入信号的噪声消除功能	R/W
31:29	—	这些位被读取为0。写入值应为0。	R/W

注1.请仅在异步模式和曼彻斯特模式下使用该位。不能保证通过其他模式移动。
注2.RINVTINV在智能卡接口模式和简单IIC模式下应设置为0。

CTSE bit (CTS Enable)

如果SSn引脚用于输入CTSn控制信号以控制发送和接收，则将该位设置为1。当该位设置为0时输出RTSn信号。在智能卡接口模式、简单SPI模式、简单LIN模式和简单IIC模式下将该位设置为0。不要将CTSE和SSE位都设置为使能（即使进行了此设置，操作与将这些位设置为0时的操作相同）。

CTSPEN位（CTS外部引脚使能）

CTSE为1时，选择使用CTS和RTS功能时的终端使用方式。当将CTSRTS功能分配给2个端子并同时使用它们时，将此位设置为1。除异步和曼彻斯特模式外，将其设置为0。

Table 26.3 shows the relationship between the CTSE bit and CTSPEN bit settings and the functions of the CTSn_RTSn pin and CTSn pin.

Table 26.3 CTSE bit and CTSPEN bit settings and pin functions

CTSE bit	CTSPEN bit	CTSn_RTSn pin	CTSn pin
0	0	RTSn signal output	Not use
1	0	CTSn signal input	Not use
1	1	RTSn signal output	CTSn signal input

Note: Please set CTSPEN bit = 0 when CTSE bit = 0.

SPB2DT bit (Serial port break data select), SPB2IO bit (Serial port break I/O)

The TXDn terminal status decided by combination of CCR0.TE bit, CCR1.SPB2IO bit and CCR1.SPB2DT bit is indicated in Table 26.4.

Table 26.4 TXDn terminal status

The value of CCR0.TE	The value of CCR1.SPB2IO	The value of CCR1.SPB2DT	TXDn terminal status (When TINV is 0.)
0	0	—	Hi-Z (initial value)
0	1	0	Low level output
0	1	1	High level output
1	—	—	Serial transmission data is output.

Note: —: Don't care

PE bit (Parity Enable)

When PE bit to 1, the parity bit is added to transmit data before transmission, and the parity bit is checked in reception. In the multiprocessor format, the parity bit is not added or checked regardless of this bit setting.

PM bit (Parity Mode)

Selects the parity mode for transmission and reception (even or odd). In multi-processor mode, this bit is invalid.

For details on the usage of this bit in smart card interface mode, refer to section 26.7.2. Data Format (Except in Block Transfer Mode).

TINV bit (TXD invert), RINV bit (RXD invert)

The data of RDR is controlled by RINV and CCR3.SINV. And the data from TXDn terminal is controlled by TINV and CCR3.SINV. The control by RINV/TINV are done to communication terminals (RXDn / TXDn), so they can control not only data-bits but also other bits (start bit, stop bit, parity bit). Please refer to Figure 26.3 in detail.

During half-duplex communication and slave operation in simple SPI mode, use the TXDn pin for reception, so set the inversion control of the received data with the TINV bit.

Note: Sentences and a timing chart of the IP operation explanation are mentioned by TINV = 0 and RINV = 0 when TINV's value and RINV's value are not specified.

表26.3显示了CTSE位和CTSPEN位设置之间的关系以及CTSn_RTSn引脚和CTSn引脚的功能。

Table 26.3 CTSE位和CTSPEN位设置和引脚功能

CTSE bit	CTSPEN bit	CTSn_RTSn pin	CTSn pin
0	0	RTSn信号输出	不使用
1	0	CTSn信号输入	不使用
1	1	RTSn信号输出	CTSn信号输入

Note: 当CTSE位=0时，请设置CTSPEN位=0。

SPB2DT位（串口断点数据选择）、SPB2IO位（串口断点IO）

由CCR0.TE位、CCR1.SPB2IO位和CCR1.SPB2DT位组合决定的TXDn端子状态如表26.4所示。

Table 26.4 TXDn终端状态

CCR0.TE的值	的价值 CCR1.SPB2IO	的价值 CCR1.SPB2DT	TXDn终端状态（当TINV为0时。）
0	0	—	Hi-Z (initial value)
0	1	0	低电平输出
0	1	1	高电平输出
1	—	—	输出串行传输数据。

Note: —: Don't care

PE位（奇偶校验使能）

当PE位为1时，发送数据前添加奇偶校验位，接收时校验奇偶校验位。

在多处理器格式中，无论此位设置如何，都不会添加或检查奇偶校验位。

PM bit (Parity Mode)

选择发送和接收的奇偶校验模式（偶数或奇数）。在多处理器模式下，该位无效。

关于该位在智能卡接口模式下的使用详情，请参阅第26.7.2节。数据格式（块中除外 Transfer Mode).

TINV bit (TXD invert), RINV bit (RXD invert)

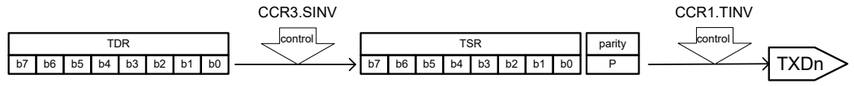
RDR的数据由RINV和CCR3.SINV控制。来自TXDn端的数据由TINV和CCR3.SINV控制。RINVTINV的控制是对通信终端（RXDnTXDn）进行的，因此它们不仅可以控制数据位，还可以控制其他位（起始位、停止位、奇偶校验位）。详细请参考图26.3。

在简单SPI模式下的半双工通信和从机操作期间，使用TXDn引脚进行接收，因此通过TINV位设置接收数据的反转控制。

Note: 当没有指定TINV的值和RINV的值时，TINV=0和RINV=0提到了IP操作说明的语句和时序图。

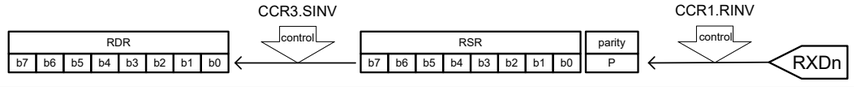
The receive/transmit data control (Data size = 8bits, Even parity, MSB first)

The transmit data is controlled by CCR1.TINV and CCR3.SINV.



CCR3. SINV	CCR1. TINV	TDR	TSR	parity (even)	TXDn waveform
0	0	0xBE	0xBE	0	1 2 3 4 5 6 7 8 9 10 11 12 13 S b7 b6 b5 b4 b3 b2 b1 b0 P
0	1	0xBE	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
1	0	0xBE	0x41	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
1	1	0xBE	0x41	0	S b7 b6 b5 b4 b3 b2 b1 b0 P

The received data is controlled by CCR1.RINV and CCR3.SINV.



CCR3. SINV	CCR1. TINV	RDR	RSR	parity (even)	RXDn waveform
0	0	0xBE	0xBE	0	1 2 3 4 5 6 7 8 9 10 11 12 13 S b7 b6 b5 b4 b3 b2 b1 b0 P
1	0	0x41	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
0	1	0xBE	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
1	1	0x41	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P

Figure 26.3 Example of the receive or transmit data control

SPLP bit (Loopback Control)

When this bit is 1, SCI blocks the input path from RXDn and connects the output path to TXDn to the reception data register.

Transmit data can be inverted and received by combining it with TINV bit.

Clock synchronous mode at slave operation, Asynchronous mode when using an external clock, and Simple LIN mode, set this bit to 0.

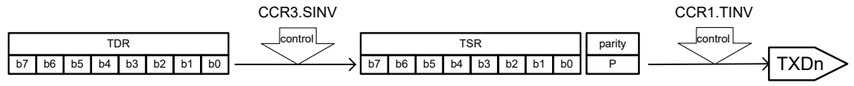
SHARPS bit (Half-duplex communication select)

Setting this bit to 1 enables half-duplex communication using the TXDn pin. However, it cannot be used in Simple SPI mode, Simple IIC mode and Smart Card Interface mode.

If this bit is set to 1 and CCR0.TE = 1, CCR0.RE = 0, the TXDn pin becomes communication output. If this bit is set to 1 and CCR0.TE = 0, CCR0.RE = 1, the TXDn pin becomes the communication input. For details, see section 26.18. Half-Duplex communication Function.

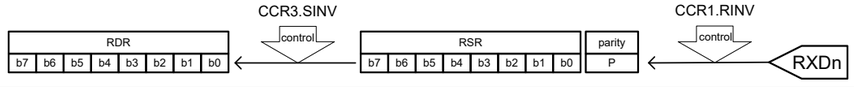
接收发送数据控制（数据大小=8bits，偶校验，MSB在前）

发送数据由CCR1.TINV和CCR3.SINV控制。



CCR3. SINV	CCR1. TINV	TDR	TSR	parity (even)	TXDn waveform
0	0	0xBE	0xBE	0	1 2 3 4 5 6 7 8 9 10 11 12 13 S b7 b6 b5 b4 b3 b2 b1 b0 P
0	1	0xBE	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
1	0	0xBE	0x41	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
1	1	0xBE	0x41	0	S b7 b6 b5 b4 b3 b2 b1 b0 P

接收的数据由CCR1.RINV和CCR3.SINV控制。



CCR3. SINV	CCR1. TINV	RDR	RSR	parity (even)	RXDn waveform
0	0	0xBE	0xBE	0	1 2 3 4 5 6 7 8 9 10 11 12 13 S b7 b6 b5 b4 b3 b2 b1 b0 P
1	0	0x41	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
0	1	0xBE	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
1	1	0x41	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P

Figure 26.3 接收或发送数据控制示例

SPLP bit (Loopback Control)

当该位为1时，SCI阻塞来自RXDn的输入路径，并将输出路径连接到TXDn和接收数据寄存器。

发送数据可以通过与TINV位组合来反转和接收。

从机操作时的时钟同步模式、使用外部时钟时的异步模式和简单LIN模式，将此位设置为0。

SHARPS位（半双工通信选择）

将该位设置为1启用使用TXDn引脚的半双工通信。但是，它不能用于简单SPI模式、简单IIC模式和智能卡接口模式。

如果该位设置为1且CCR0.TE=1，CCR0.RE=0，则TXDn引脚变为通信输出。如果该位设置为1且CCR0.TE=0，CCR0.RE=1，则TXDn引脚变为通信输入。有关详细信息，请参阅第26.18节。半双工通信功能。

NFCS[2:0] bit (Noise Filter Clock Select)

These bits select the sampling clock for the digital noise filter.

To use the noise filter in asynchronous mode, manchester mode and Simple LIN mode set these bits from 000b to 100b. In simple IIC mode, set the bits to a value in the range from 001b to 100b.

NFEN bit (Digital Noise Filter Function Enable)

This bit enables or disables the digital noise filter function. When the function is enabled, noise cancellation is applied to the RXDn input signal in asynchronous mode, manchester mode, Simple LIN mode, and noise cancellation is applied to the SDAn and SCLn input signals in simple IIC mode. In any mode other than above, set the NFEN bit to 0 to disable the digital noise filter function. When the function is disabled, input signals are transferred as is, as internal signals.

26.2.7 CCR2 : Common Control Register 2

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MDDR[7:0]								—	—	CKS[1:0]		—	—	—	BRME
Value after reset:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BRR[7:0]								—	ABCSE	ABCS	BGDM	—	BCP[2:0]		
Value after reset:	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
2:0	BCP[2:0]	Base Clock Pulse Selects the number of base clock cycles in smart card interface mode. 0 0 0: 93 clock cycles (S = 93)*1 0 0 1: 128 clock cycles (S = 128)*1 0 1 0: 186 clock cycles (S = 186)*1 0 1 1: 512 clock cycles (S = 512)*1 1 0 0: 32 clock cycles (S = 32)*1 (Initial value) 1 0 1: 64 clock cycles (S = 64)*1 1 1 0: 372 clock cycles (S = 372)*1 1 1 1: 256 clock cycles (S = 256)*1	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	BGDM	Baud Rate Generator Double-Speed Mode Select Valid in asynchronous/Manchester/clock-synchronous/Simple SPI mode and CCR3.CKE[1] = 0. 0: Baud rate generator outputs the clock with single frequency. 1: Baud rate generator outputs the clock with doubled frequency.	R/W
5	ABCS	Asynchronous Mode Base Clock Select Valid only in Asynchronous mode, Manchester mode and Simple LIN mode 0: Selects 16 base clock cycles for 1-bit period. 1: Selects 8 base clock cycles for 1-bit period.	R/W
6	ABCSE	Asynchronous Mode Extended Base Clock Select Valid only in Asynchronous mode and CCR3.CKE[1] = 0 0: Clock cycles for 1-bit period is decided with combination be-tween CCR2.BGDM and CCR2.ABCS. 1: Baud rate is 6 base clock cycles for 1-bit period and the clock of a double frequency is output from the baud rate generator.	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
15:8	BRR[7:0]	Bit rate setting BRR is an 8-bit register that adjusts the bit rate.	R/W

NFCS[2:0]位（噪声滤波器时钟选择）

这些位选择数字噪声滤波器的采样时钟。

要在异步模式、曼彻斯特模式和简单LIN模式下使用噪声滤波器，将这些位设置为从000b到100b。在简单IIC模式下，将位设置为001b到100b范围内的值。

NFEN位（数字噪声滤波器功能使能）

该位启用或禁用数字噪声滤波器功能。启用该功能后，噪声消除将应用于
异步模式、曼彻斯特模式、简单LIN模式和噪声消除中的RXDn输入信号应用于
SDAn和SCLn在简单IIC模式下输入信号。在上述以外的任何模式下，将NFEN位设置为0以禁用数字噪声滤波器功能。禁用该功能时，输入信号按原样作为内部信号传输。

26.2.7 CCR2：公共控制寄存器2

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MDDR[7:0]								—	—	CKS[1:0]		—	—	—	BRME
重置后的值：	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BRR[7:0]								—	ABCSE	ABCS	BGDM	—	BCP[2:0]		
重置后的值：	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
2:0	BCP[2:0]	基本时钟脉冲 选择智能卡接口模式下的基本时钟周期数。 000：93个时钟周期(S=93)*1 001：128个时钟周期(S=128)*1 010：186个时钟周期(S=186)*1 011：512个时钟周期(S=512)*1 100:32个时钟周期(S=32)*1(初始值)101:64个时钟周期(S=64)*1 110：372个时钟周期(S=372)*1 111：256个时钟周期(S=256)*1	R/W
3	—	该位读取为0。写入值应为0。	R/W
4	BGDM	波特率发生器双速模式选择 在异步曼彻斯特时钟同步简单SPI模式和CCR3.CKE[1]=0下有效。 0：波特率发生器输出单频时钟。1：波特率发生器输出倍频时钟。	R/W
5	ABCS	异步模式基本时钟选择 仅在异步模式、曼彻斯特模式和简单LIN模式下有效 0：为1位周期选择16个基本时钟周期。1：为1位周期选择8个基本时钟周期。	R/W
6	ABCSE	异步模式扩展基本时钟选择 仅在异步模式和CCR3.CKE[1]=0下有效 0：1位周期的时钟周期由CCR2.BGDM和CCR2.ABCS之间的组合决定。 1：波特率为1位周期的6个基本时钟周期，从波特率发生器输出双频时钟。	R/W
7	—	该位读取为0。写入值应为0。	R/W
15:8	BRR[7:0]	比特率设置 BRR是一个8位寄存器，用于调整比特率。	R/W

Bit	Symbol	Function	R/W
16	BRME	Bit Modulation Enable 0: Bit rate modulation function is disabled. 1: Bit rate modulation function is enabled.	R/W
19:17	—	These bits are read as 0. The write value should be 0.	R/W
21:20	CKS[1:0]	Clock Select 0 0: TCLK clock (n = 0)*2 0 1: TCLK/4 clock (n = 1)*2 1 0: TCLK/16 clock (n = 2)*2 1 1: TCLK/64 clock (n = 3)*2	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W
31:24	MDDR[7:0]	Modulation Duty Setting MDDR corrects the bit rate adjusted by the BRR[7:0] bits.	R/W

Note 1. S is the value of S in BRR[7:0] bits explanation.
Note 2. n is the decimal notation of the value of n in BRR[7:0] bits explanation.

BCP[2:0] bit (Base Clock Pulse)

These bits select the number of base clock cycles in a 1-bit data transfer time in smart card interface mode.

For details, refer to section 26.7.4. Receive Data Sampling Timing and Reception Margin.

BGDM bit (Baud Rate Generator Double-Speed Mode Select)

This bit is valid when the on-chip baud rate generator is selected as the clock source (CCR3.CKE[1] = 0) in asynchronous mode, Manchester mode, clock synchronous mode, Simple SPI mode. When external clock is selected (CCR3.CKE[1] = 1), set it to 0. For the clock output from the baud rate generator, either single or doubled frequency can be selected. The base clock is generated by the clock output from the baud rate generator. When the BGDM bit is set to 1, the base clock cycle is halved, and the bit rate is doubled.

Set this bit to 0 in modes other than asynchronous mode or Manchester mode or clock synchronous mode or Simple SPI mode.

ABCS bit (Asynchronous Mode Base Clock Select)

Selects the clock cycles for 1-bit period.

Set it to 0 in modes other than Asynchronous mode, Manchester mode and Simple LIN mode.

ABCSE bit (Asynchronous Mode Extended Base Clock Select)

The pulse number for a base clock at 1-bit period is 6 and the clock of a double frequency is output from baud rate generator. Only when the bit rate is set to 6 dividing frequency of the bus clock, please use this bit and set CCR2.CKS [1:0] = 00b and BRR[7:0] = 0x00.

Set it to 0 in modes other than asynchronous mode. Even in asynchronous mode, set it to 0 when using external clock.

Table 26.5 Base clock cycle number per 1-bit

ABCSE	ABCS	BGDM	The base clock cycles /1bit	The frequency of the baud rate generator
0	0	0	16	×1
0	0	1	16	×2
0	1	0	8	×1
0	1	1	8	×2
1	— (don't care)	— (don't care)	6	×2

BRR[7:0] bit (Bit rate setting)

BRR is an 8-bit register that adjusts the bit rate.

SCI has independent baud rate generator control, different bit rates can be set for each. Table 26.6 shows the relation-ship between the setting (N) in the BRR and the bit rate (B) for asynchronous mode, multiprocessor transfer, Manchester mode, clock synchronous mode, smart card interface mode, simple SPI mode, and simple IIC mode.

Bit	Symbol	Function	R/W
16	BRME	位调制使能 0：比特率调制功能关闭。1：比特率调制功能使能。	R/W
19:17	—	这些位被读取为0。写入值应为0。	R/W
21:20	CKS[1:0]	时钟选择 0 0: TCLK clock (n = 0)*2 0 1: TCLK/4 clock (n = 1)*2 1 0: TCLK/16 clock (n = 2)*2 1 1: TCLK/64 clock (n = 3)*2	R/W
23:22	—	这些位被读取为0。写入值应为0。	R/W
31:24	MDDR[7:0]	调制占空比设置 MDDR校正由BRR[7:0]位调整的比特率。	R/W

注1.S是BRR[7:0]位解释中S的值。
注2.n是BRR[7:0]位解释中n值的十进制表示法。

BCP[2:0]位（基本时钟脉冲）

这些位选择智能卡接口模式下1位数据传输时间内的基本时钟周期数。

详情请参阅26.7.4节。接收数据采样时序和接收余量。

BGDM位（波特率发生器双速模式选择）

在异步模式、曼彻斯特模式、时钟同步模式、简单SPI模式选择片内波特率发生器作为时钟源（CCR3.CKE[1]=0）时，该位有效。Whenexternalclockisselected(CCR3.CKE[1]=1) setitto0.Fortheclockoutputfromthebaudrategenerator eithersingleordoubledfrequencycanbeselected.基本时钟由波特率发生器的时钟输出生成。当BGDM位设置为1时，基本时钟周期减半，比特率加倍。

在异步模式或曼彻斯特模式或时钟同步模式或简单SPI模式以外的模式下将此位设置为0。

ABCS位（异步模式基本时钟选择）

选择1位周期的时钟周期。

在异步模式、曼彻斯特模式和简单LIN模式以外的模式下将其设置为0。

ABCSE位（异步模式扩展基本时钟选择）

1位周期的基本时钟脉冲数为6，从波特率发生器输出双频时钟。只有当比特率设置为总线时钟的6分频时，请使用该位并设置CCR2.CKS[1:0]=00b和BRR[7:0]=0x00。

在异步模式以外的模式下将其设置为0。即使在异步模式下，使用外部时钟时也将其设置为0。

Table 26.5 每1位的基本时钟周期数

ABCSE	ABCS	BGDM	基本时钟周期1bit	波特率发生器的频率
0	0	0	16	×1
0	0	1	16	×2
0	1	0	8	×1
0	1	1	8	×2
1	— (don't care)	— (don't care)	6	×2

BRR[7:0]位（比特率设置）

BRR是一个8位寄存器，用于调整比特率。

SCI具有独立的波特率发生器控制，可分别设置不同的比特率。表26.6显示了BRR中的设置(N)与异步模式、多处理器传输、曼彻斯特模式、时钟同步模式、智能卡接口模式、简单SPI模式和简单IIC模式的比特率(B)之间的关系.

Table 26.6 Relationship between N Setting in BRR and Bit Rate B

Mode	CCR2 settings BGDM bit	ABCS bit	ABCS E bit	BRR[7:0] setting	Error
Asynchronous, multi-processor, Manchester, Simple-LIN*3	0	0	0	$N = \frac{TCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	1	0	0	$N = \frac{TCLK \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{TCLK \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	Don't care	Don't care	1*2	$N = \frac{TCLK \times 10^6}{12 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
Clock synchronous, simple SPI				$N = \frac{TCLK \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	—
Smart card interface				$N = \frac{TCLK \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\right\} \times 100$
Simple IIC*1				$N = \frac{TCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	—

Note: B: Bit rate (bps)
N: BRR setting for on-chip baud rate generator (0 ≤ N ≤ 255)
TCLK: Operating frequency (MHz)
n and S: Determined by the settings of the CCR2 registers as listed in the Table 26.8 and Table 26.9. Please be careful about $2^{(2n+1)}$ is used in the expression for Smart card interface, $2^{(2n-1)}$ is used in other mode.
Note 1. Adjust the bit rate so that the widths at high and low level of the SCL output in simple IIC mode satisfy the IIC standard.
Note 2. In Manchester mode, only ABCSE = 0 can be selected.
Note 3. In Simple LIN mode, BGDM = 0 and ABCSE = 0 can be selected.

Table 26.7 Calculating Widths at High and Low Level for SCL

Mode	SCLn	Formula (result in seconds)
IIC	Width at high level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 7 \times \frac{1}{TCLK \times 10^6}$
	Width at low level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 8 \times \frac{1}{TCLK \times 10^6}$

Table 26.8 Clock Source Settings

CCR2 setting CKS[1:0] bit	Clock source	n
00	TCLK clock	0
01	TCLK/4 clock	1
10	TCLK/16 clock	2
11	TCLK/64 clock	3

Table 26.9 Base Clock Settings in Smart Card Interface Mode (1 of 2)

CCR2 setting BCP[2:0] setting	Base clock cycles for 1-bit period	S
0 0 0	93 clock cycles	93
0 0 1	128 clock cycles	128
0 1 0	186 clock cycles	186

Table 26.6 BRR中的N设置与比特率B的关系

Mode	CCR2 settings BGDM bit	ABCS 位	ABCS E位	BRR[7:0] setting	Error
异步、多处理器、曼彻斯特、Simple-LIN*3	0	0	0	$N = \frac{TCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	1	0	0	$N = \frac{TCLK \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{TCLK \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	Don't care	Don't care	1*2	$N = \frac{TCLK \times 10^6}{12 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
时钟同步，简单的SPI				$N = \frac{TCLK \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	
智能卡接口				$N = \frac{TCLK \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\right\} \times 100$
*1				$N = \frac{TCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	—

Note: B：比特率（bps）
N：片内波特率发生器的BRR设置（0≤N≤255）
TCLK：工作频率(MHz)n和S：由表26.8和表26.9中列出的CCR2寄存器的设置决定。请注意2（2n
+1)用于智能卡接口的表达式，2(2n-1)用于其他模式。
注1.调整码率，使简单IIC模式下SCL输出的高低电平宽度满足IIC标准。
注2.在曼彻斯特模式下，只能选择ABCSE=0。
注3.在简单LIN模式下，可以选择BGDM=0和ABCSE=0。

Table 26.7 计算SCL的高低电平宽度

Mode	SCLn	公式（以秒为单位的结果）
IIC	高电平宽度（最小值）	$(N+1) \times 4 \times 2^{2n-1} \times 7 \times \frac{1}{TCLK \times 10^6}$
	低电平宽度（最小值）	$(N+1) \times 4 \times 2^{2n-1} \times 8 \times \frac{1}{TCLK \times 10^6}$

Table 26.8 时钟源设置

CCR2 setting CKS[1:0] bit	时钟源	n
00	TCLK clock	0
01	TCLK/4 clock	1
10	TCLK/16 clock	2
11	TCLK/64 clock	3

Table 26.9 智能卡接口模式下的基本时钟设置（1of2）

CCR2 setting BCP[2:0] setting	1位周期的基本时钟周期	S
0 0 0	93个时钟周期	93
0 0 1	128个时钟周期	128
0 1 0	186个时钟周期	186

Table 26.9 Base Clock Settings in Smart Card Interface Mode (2 of 2)

CCR2 setting		
BCP[2:0] setting	Base clock cycles for 1-bit period	S
0 1 1	512 clock cycles	512
1 0 0	32 clock cycles	32
1 0 1	64 clock cycles	64
1 1 0	372 clock cycles	372
1 1 1	256 clock cycles	256

Table 26.10 and Table 26.11 list examples of N settings in BRR in asynchronous mode and Manchester mode. Table 26.12 lists the maximum bit rate settable for each operating frequency. Examples of BRR (N) settings in clock synchronous mode and simple SPI mode are listed in Table 26.15. Examples of BRR (N) settings in smart card interface mode are listed in Table 26.17. Examples of BRR (N) settings in simple IIC mode are listed in Table 26.19. In smart card interface mode, the number of base clock cycles S in a 1-bit data transfer time can be selected. For details, refer to section 26.7.4. Receive Data Sampling Timing and Reception Margin. Table 26.14 and Table 26.16 list the maximum bit rates with external clock input.

When either the asynchronous mode base clock select bit (ABCS) or the baud rate generator double-speed mode select bit (BGDM) is set to 1 in asynchronous mode and manchester mode, the bit rate becomes twice that listed in Table 26.10 and Table 26.11. When both of those registers are set to 1, the bit rate becomes four times the listed value.

Table 26.10 Examples of BRR Settings for various Bit Rates (Asynchronous Mode and Manchester Mode) (1) (1 of 3)

Bit rate (bps)	Operating Frequency TCLK (MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	–0.26	2	177	–0.25	2	212	0.03	2	217	0.08
150	2	103	0.16	2	127	0	2	129	0.16	2	155	0.16	2	159	0
300	1	207	0.16	1	255	0	2	64	0.16	2	77	0.16	2	79	0
600	1	103	0.16	1	127	0	1	129	0.16	1	155	0.16	1	159	0
1200	0	207	0.16	0	255	0	1	64	0.16	1	77	0.16	1	79	0
2400	0	103	0.16	0	127	0	0	129	0.16	0	155	0.16	0	159	0
4800	0	51	0.16	0	63	0	0	64	0.16	0	77	0.16	0	79	0
9600	0	25	0.16	0	31	0	0	32	–1.36	0	38	0.16	0	39	0
19200	0	12	0.16	0	15	0	0	15	1.73	0	19	–2.34	0	19	0
31250	0	7	0	0	9	–1.7	0	9	0	0	11	0	0	11	2.4
38400	—	—	—	0	7	0	0	7	1.73	0	9	–2.34	0	9	0

Table 26.10 Examples of BRR Settings for various Bit Rates (Asynchronous Mode and Manchester Mode) (1) (2 of 3)

Bit rate (bps)	Operating Frequency TCLK (MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	–0.17	3	70	0.03	3	75	0.48	3	79	–0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0	2	233	0.16	2	255	0
300	2	90	0.16	2	103	0.16	2	111	0	2	116	0.16	2	127	0
600	1	181	0.16	1	207	0.16	1	223	0	1	233	0.16	1	255	0
1200	1	90	0.16	1	103	0.16	1	111	0	1	116	0.16	1	127	0
2400	0	181	0.16	0	207	0.16	0	223	0	0	233	0.16	0	255	0
4800	0	90	0.16	0	103	0.16	0	111	0	0	116	0.16	0	127	0

Table 26.9 智能卡接口模式下的基本时钟设置(2of2)

CCR2 setting		
BCP[2:0] setting	1位周期的基本时钟周期	S
0 1 1	512个时钟周期	512
1 0 0	32个时钟周期	32
1 0 1	64个时钟周期	64
1 1 0	372个时钟周期	372
1 1 1	256个时钟周期	256

表26.10和表26.11列出了BRR在异步模式和曼彻斯特模式下的N设置示例。表26.12列出了每个工作频率可设置的最大比特率。表26.15列出了时钟同步模式和简单SPI模式下的BRR(N)设置示例。智能卡接口模式下的BRR(N)设置示例在表26.17中列出。简单IIC模式下的BRR(N)设置示例如表26.19所示。在智能卡接口模式下，可以选择1位数据传输时间内的基本时钟周期数S。详情请参阅26.7.4节。接收数据采样时序和接收余量。表26.14和表26.16列出了外部时钟输入的最大比特率。

在异步模式和曼彻斯特模式下，当异步模式基本时钟选择位(ABCS)或波特率发生器双速模式选择位(BGDM)设置为1时，比特率变为表26.10和表26.11中列出的两倍.当这两个寄存器都设置为1时，比特率变为所列值的四倍。

Table 26.10 各种比特率（异步模式和曼彻斯特模式）的BRR设置示例(1)(1of3)

比特率(bps)	工作频率TCLK(MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	–0.26	2	177	–0.25	2	212	0.03	2	217	0.08
150	2	103	0.16	2	127	0	2	129	0.16	2	155	0.16	2	159	0
300	1	207	0.16	1	255	0	2	64	0.16	2	77	0.16	2	79	0
600	1	103	0.16	1	127	0	1	129	0.16	1	155	0.16	1	159	0
1200	0	207	0.16	0	255	0	1	64	0.16	1	77	0.16	1	79	0
2400	0	103	0.16	0	127	0	0	129	0.16	0	155	0.16	0	159	0
4800	0	51	0.16	0	63	0	0	64	0.16	0	77	0.16	0	79	0
9600	0	25	0.16	0	31	0	0	32	–1.36	0	38	0.16	0	39	0
19200	0	12	0.16	0	15	0	0	15	1.73	0	19	–2.34	0	19	0
31250	0	7	0	0	9	–1.7	0	9	0	0	11	0	0	11	2.4
38400	—	—	—	0	7	0	0	7	1.73	0	9	–2.34	0	9	0

Table 26.10 各种比特率（异步模式和曼彻斯特模式）的BRR设置示例(1)(2of3)

比特率(bps)	工作频率TCLK(MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	–0.17	3	70	0.03	3	75	0.48	3	79	–0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0	2	233	0.16	2	255	0
300	2	90	0.16	2	103	0.16	2	111	0	2	116	0.16	2	127	0
600	1	181	0.16	1	207	0.16	1	223	0	1	233	0.16	1	255	0
1200	1	90	0.16	1	103	0.16	1	111	0	1	116	0.16	1	127	0
2400	0	181	0.16	0	207	0.16	0	223	0	0	233	0.16	0	255	0
4800	0	90	0.16	0	103	0.16	0	111	0	0	116	0.16	0	127	0

Table 26.10 Examples of BRR Settings for various Bit Rates (Asynchronous Mode and Manchester Mode) (1) (3 of 3)

Bit rate (bps)	Operating Frequency TCLK (MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	45	–0.93	0	51	0.16	0	55	0	0	58	–0.69	0	63	0
19200	0	22	–0.93	0	25	0.16	0	27	0	0	28	1.02	0	31	0
31250	0	13	0	0	15	0	0	16	1.2	0	17	0	0	19	–1.7
38400	—	—	—	0	12	0.16	0	13	0	0	14	–2.34	0	15	0

Note: This is an example when the CCR2.ABCS = 0, CCR2.BGDM = 0 and CCR2.ABCSE = 0.
When either ABCS bit or BGDM bit is set to 1, the bit rate doubles.
When both ABCS = 1 and BGDM = 1, the bit rate increases four times.

Table 26.11 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode and Manchester Mode) (2) (1 of 2)

Bit rate (bps)	Operating frequency TCLK (MHz)														
	20			25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	88	–0.25	3	110	–0.02	3	132	0.13	3	145	0.33	3	177	–0.25
150	3	64	0.16	3	80	0.47	3	97	–0.35	3	106	0.39	3	129	0.16
300	2	129	0.16	2	162	–0.15	2	194	0.16	2	214	–0.07	3	64	0.16
600	2	64	0.16	2	80	0.47	2	97	–0.35	2	106	0.39	2	129	0.16
1200	1	129	0.16	1	162	–0.15	1	194	0.16	1	214	–0.07	2	64	0.16
2400	1	64	0.16	1	80	0.47	1	97	–0.35	1	106	0.39	1	129	0.16
4800	0	129	0.16	0	162	–0.15	0	194	0.16	0	214	–0.07	1	64	0.16
9600	0	64	0.16	0	80	0.47	0	97	–0.35	0	106	0.39	0	129	0.16
19200	0	32	–1.36	0	40	–0.76	0	48	–0.35	0	53	–0.54	0	64	0.16
31250	0	19	0	0	24	0	0	29	0	0	32	0	0	39	0
38400	0	15	1.73	0	19	1.73	0	23	1.73	0	26	–0.54	0	32	–1.36

Table 26.11 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode and Manchester Mode) (2) (2 of 2)

Bit rate (bps)	Operating frequency TCLK (MHz)														
	50			60			100			120			160		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	221	–0.02	—	—	—	—	—	—	—	—	—	—	—	—
150	3	162	–0.15	3	194	0.16	—	—	—	—	—	—	—	—	—
300	3	80	0.47	3	97	–0.35	3	162	–0.15	3	194	0.16	—	—	—
600	2	162	–0.15	2	194	0.16	3	80	0.47	3	97	–0.35	3	129	0.16
1200	2	80	0.47	2	97	–0.35	2	162	–0.15	2	194	0.16	3	64	0.16
2400	1	162	–0.15	1	194	0.16	2	80	0.47	2	97	–0.35	2	129	0.16
4800	1	80	0.47	1	97	–0.35	1	162	–0.15	1	194	0.16	2	64	0.16
9600	0	162	–0.15	0	194	0.16	1	80	0.47	1	97	–0.35	1	129	0.16
19200	0	80	0.47	0	97	–0.35	0	162	–0.15	0	194	0.16	1	64	0.16
31250	0	49	0	0	59	0	1	24	0	0	119	0	0	159	0
38400	0	40	–0.76	0	48	–0.35	0	80	0.47	0	97	–0.35	0	129	0.16

Note: This is an example when the CCR2.ABCS = 0, CCR2.BGDM = 0 and CCR2.ABCSE = 0.

Table 26.10 各种比特率（异步模式和曼彻斯特模式）的BRR设置示例(1)(3of3)

比特率(bps)	工作频率TCLK(MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	45	–0.93	0	51	0.16	0	55	0	0	58	–0.69	0	63	0
19200	0	22	–0.93	0	25	0.16	0	27	0	0	28	1.02	0	31	0
31250	0	13	0	0	15	0	0	16	1.2	0	17	0	0	19	–1.7
38400	—	—	—	0	12	0.16	0	13	0	0	14	–2.34	0	15	0

Note: 这是CCR2.ABCS=0、CCR2.BGDM=0和CCR2.ABCSE=0时的示例。
当ABCS位或BGDM位设置为1时，比特率加倍。
当ABCS=1和BGDM=1时，比特率增加四倍。

Table 26.11 各种比特率（异步模式和曼彻斯特模式）的BRR设置示例(2)(1of2)

比特率(bps)	工作频率TCLK(MHz)														
	20			25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	88	–0.25	3	110	–0.02	3	132	0.13	3	145	0.33	3	177	–0.25
150	3	64	0.16	3	80	0.47	3	97	–0.35	3	106	0.39	3	129	0.16
300	2	129	0.16	2	162	–0.15	2	194	0.16	2	214	–0.07	3	64	0.16
600	2	64	0.16	2	80	0.47	2	97	–0.35	2	106	0.39	2	129	0.16
1200	1	129	0.16	1	162	–0.15	1	194	0.16	1	214	–0.07	2	64	0.16
2400	1	64	0.16	1	80	0.47	1	97	–0.35	1	106	0.39	1	129	0.16
4800	0	129	0.16	0	162	–0.15	0	194	0.16	0	214	–0.07	1	64	0.16
9600	0	64	0.16	0	80	0.47	0	97	–0.35	0	106	0.39	0	129	0.16
19200	0	32	–1.36	0	40	–0.76	0	48	–0.35	0	53	–0.54	0	64	0.16
31250	0	19	0	0	24	0	0	29	0	0	32	0	0	39	0
38400	0	15	1.73	0	19	1.73	0	23	1.73	0	26	–0.54	0	32	–1.36

Table 26.11 各种比特率（异步模式和曼彻斯特模式）的BRR设置示例(2)(2of2)

比特率(bps)	工作频率TCLK(MHz)														
	50			60			100			120			160		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	221	–0.02	—	—	—	—	—	—	—	—	—	—	—	—
150	3	162	–0.15	3	194	0.16	—	—	—	—	—	—	—	—	—
300	3	80	0.47	3	97	–0.35	3	162	–0.15	3	194	0.16	—	—	—
600	2	162	–0.15	2	194	0.16	3	80	0.47	3	97	–0.35	3	129	0.16
1200	2	80	0.47	2	97	–0.35	2	162	–0.15	2	194	0.16	3	64	0.16
2400	1	162	–0.15	1	194	0.16	2	80	0.47	2	97	–0.35	2	129	0.16
4800	1	80	0.47	1	97	–0.35	1	162	–0.15	1	194	0.16	2	64	0.16
9600	0	162	–0.15	0	194	0.16	1	80	0.47	1	97	–0.35	1	129	0.16
19200	0	80	0.47	0	97	–0.35	0	162	–0.15	0	194	0.16	1	64	0.16
31250	0	49	0	0	59	0	1	24	0	0	119	0	0	159	0
38400	0	40	–0.76	0	48	–0.35	0	80	0.47	0	97	–0.35	0	129	0.16

Note: 这是CCR2.ABCS=0、CCR2.BGDM=0和CCR2.ABCSE=0时的示例。

When either ABCS bit or BGDM bit is set to 1, the bit rate doubles.
When both ABCS = 1 and BGDM = 1, the bit rate increases four times.

Table 26.12 Maximum Bit Rate for Each Operating Frequency (Asynchronous Mode and Manchester mode) (1)

TCLK (MHz)	CCR2 settings					Maximum bit rate (bps)	TCLK (MHz)	CCR2 settings					Maximum bit rate (bps)
	BGDM	ABCS	ABCSE	n	N			BGDM	ABCS	ABCSE	n	N	
8	0	0	0	0	0	250000	16	0	0	0	0	0	500000
		1	0	0	0	500000			1	0	0	0	1000000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1000000			1	0	0	0	2000000
	Don't care	Don't care	1	0	0	1333333		Don't care	Don't care	1	0	0	2666666
9.8304	0	0	0	0	0	307200	17.2032	0	0	0	0	0	537600
		1	0	0	0	614400			1	0	0	0	1075200
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1228800			1	0	0	0	2150400
	Don't care	Don't care	1	0	0	1638400		Don't care	Don't care	1	0	0	2867200
10	0	0	0	0	0	312500	18	0	0	0	0	0	562500
		1	0	0	0	625000			1	0	0	0	1125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1250000			1	0	0	0	2250000
	Don't care	Don't care	1	0	0	1666666		Don't care	Don't care	1	0	0	3000000
12	0	0	0	0	0	375000	19.6608	0	0	0	0	0	614400
		1	0	0	0	750000			1	0	0	0	1228800
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1500000			1	0	0	0	2457600
	Don't care	Don't care	1	0	0	2000000		Don't care	Don't care	1	0	0	3276800
12.288	0	0	0	0	0	384000	20	0	0	0	0	0	625000
		1	0	0	0	768000			1	0	0	0	1250000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1536000			1	0	0	0	2500000
	Don't care	Don't care	1	0	0	2048000		Don't care	Don't care	1	0	0	3333333
14	0	0	0	0	0	437500	25	0	0	0	0	0	781250
		1	0	0	0	875000			1	0	0	0	1562500
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1750000			1	0	0	0	3125000
	Don't care	Don't care	1	0	0	2333333		Don't care	Don't care	1	0	0	4166666

当ABCS位或BGDM位设置为1时，比特率加倍。
当ABCS=1和BGDM=1时，比特率增加四倍。

Table 26.12 每个工作频率的最大比特率（异步模式和曼彻斯特模式）(1)

TCLK (MHz)	CCR2 settings					最大比特率(bps)	TCLK (MHz)	CCR2 settings					最大比特率(bps)
	BGDM	ABCS	ABCSE	n	N			BGDM	ABCS	ABCSE	n	N	
8	0	0	0	0	0	250000	16	0	0	0	0	0	500000
		1	0	0	0	500000			1	0	0	0	1000000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1000000			1	0	0	0	2000000
	Don't care	Don't care	1	0	0	1333333		Don't care	Don't care	1	0	0	2666666
9.8304	0	0	0	0	0	307200	17.2032	0	0	0	0	0	537600
		1	0	0	0	614400			1	0	0	0	1075200
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1228800			1	0	0	0	2150400
	Don't care	Don't care	1	0	0	1638400		Don't care	Don't care	1	0	0	2867200
10	0	0	0	0	0	312500	18	0	0	0	0	0	562500
		1	0	0	0	625000			1	0	0	0	1125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1250000			1	0	0	0	2250000
	Don't care	Don't care	1	0	0	1666666		Don't care	Don't care	1	0	0	3000000
12	0	0	0	0	0	375000	19.6608	0	0	0	0	0	614400
		1	0	0	0	750000			1	0	0	0	1228800
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1500000			1	0	0	0	2457600
	Don't care	Don't care	1	0	0	2000000		Don't care	Don't care	1	0	0	3276800
12.288	0	0	0	0	0	384000	20	0	0	0	0	0	625000
		1	0	0	0	768000			1	0	0	0	1250000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1536000			1	0	0	0	2500000
	Don't care	Don't care	1	0	0	2048000		Don't care	Don't care	1	0	0	3333333
14	0	0	0	0	0	437500	25	0	0	0	0	0	781250
		1	0	0	0	875000			1	0	0	0	1562500
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1750000			1	0	0	0	3125000
	Don't care	Don't care	1	0	0	2333333		Don't care	Don't care	1	0	0	4166666

Table 26.13 Maximum Bit Rate for Each Operating Frequency (Asynchronous Mode and Manchester mode) (2)

TCLK (MHz)	CCR2 settings					Maximum bit rate (bps)	TCLK (MHz)	CCR2 settings					Maximum bit rate (bps)
	BGDM	ABCS	ABCSE	n	N			BGDM	ABCS	ABCSE	n	N	
30	0	0	0	0	0	937500	50	0	0	0	0	0	1562500
		1	0	0	0	1875000			1	0	0	0	3125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	3750000			1	0	0	0	6250000
	Don't care	Don't care	1	0	0	5000000		Don't care	Don't care	1	0	0	8333333
33	0	0	0	0	0	1031250	60	0	0	0	0	0	1875000
		1	0	0	0	2062500			1	0	0	0	3750000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	4125000			1	0	0	0	7500000
	Don't care	Don't care	1	0	0	5500000		Don't care	Don't care	1	0	0	10000000
40	0	0	0	0	0	1250000	120	0	0	0	0	0	3750000
		1	0	0	0	2500000			1	0	0	0	7500000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	5000000			1	0	0	0	15000000
	Don't care	Don't care	1	0	0	6666666		Don't care	Don't care	1	0	0	20000000
							160	0	0	0	0	0	5000000
									1	0	0	0	10000000
								1	0	0	0	0	
									1	0	0	0	20000000
								Don't care	Don't care	1	0	0	26666666

Table 26.14 Maximum Bit Rate with External Clock Input (Asynchronous Mode)

TCLK(MHz)	External clock (MHz)	Maximum bit rate (bps)		TCLK(MHz)	External clock (MHz)	Maximum bit rate (bps)	
		CCR2.ABCS bit = 0	CCR2.ABCS bit = 1			CCR2.ABCS bit = 0	CCR2.ABCS bit = 1
8	2	125000	250000	25	6.25	390625	781250
9.8304	2.4576	153600	307200	30	7.5	468750	937500
10	2.5	156250	312500	33	8.25	515625	1031250
12	3	187500	375000	40	10	625000	1250000
12.288	3.072	192000	384000	50	12.5	781250	1562500
14	3.5	218750	437500	60	15	937500	1875000
16	4	250000	500000	120	30	1875000	3750000
17.2032	4.3008	268800	537600	160	40	2500000	5000000
18	4.5	281250	562500				
19.6608	4.9152	307200	614400				
20	5	312500	625000				

Table 26.13 每个工作频率的最大比特率（异步模式和曼彻斯特模式）(2)

TCLK (MHz)	CCR2 settings					最大比特率(bps)	TCLK (MHz)	CCR2 settings					最大比特率(bps)
	BGDM	ABCS	ABCSE	n	N			BGDM	ABCS	ABCSE	n	N	
30	0	0	0	0	0	937500	50	0	0	0	0	0	1562500
		1	0	0	0	1875000			1	0	0	0	3125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	3750000			1	0	0	0	6250000
	Don't care	Don't care	1	0	0	5000000		Don't care	Don't care	1	0	0	8333333
33	0	0	0	0	0	1031250	60	0	0	0	0	0	1875000
		1	0	0	0	2062500			1	0	0	0	3750000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	4125000			1	0	0	0	7500000
	Don't care	Don't care	1	0	0	5500000		Don't care	Don't care	1	0	0	10000000
40	0	0	0	0	0	1250000	120	0	0	0	0	0	3750000
		1	0	0	0	2500000			1	0	0	0	7500000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	5000000			1	0	0	0	15000000
	Don't care	Don't care	1	0	0	6666666		Don't care	Don't care	1	0	0	20000000
							160	0	0	0	0	0	5000000
									1	0	0	0	10000000
								1	0	0	0	0	
									1	0	0	0	20000000
								Don't care	Don't care	1	0	0	26666666

Table 26.14 外部时钟输入的最大比特率（异步模式）

TCLK(MHz)	外部时钟(MHz)	最大比特率(bps)		TCLK(MHz)	外部时钟(MHz)	最大比特率(bps)	
		CCR2.ABCS bit = 0	CCR2.ABCS bit = 1			CCR2.ABCS bit = 0	CCR2.ABCS bit = 1
8	2	125000	250000	25	6.25	390625	781250
9.8304	2.4576	153600	307200	30	7.5	468750	937500
10	2.5	156250	312500	33	8.25	515625	1031250
12	3	187500	375000	40	10	625000	1250000
12.288	3.072	192000	384000	50	12.5	781250	1562500
14	3.5	218750	437500	60	15	937500	1875000
16	4	250000	500000	120	30	1875000	3750000
17.2032	4.3008	268800	537600	160	40	2500000	5000000
18	4.5	281250	562500				
19.6608	4.9152	307200	614400				
20	5	312500	625000				

Table 26.15 BRR Settings for Various Bit Rates (Clock Synchronous Mode, Simple SPI Mode)

Bit rate (bps)	Operating frequency TCLK (MHz)																	
	8			10			30			60			120			160		
	BGDM	n	N	BGDM	n	N	BGDM	n	N	BGDM	n	N	BGDM	n	N	BGDM	n	N
250	0	3	124	0	3	177	—	—	—	—	—	—	—	—	—	—	—	—
500	0	2	249	0	3	77	0	3	233	—	—	—	—	—	—	—	—	—
1k	0	2	124	0	3	38	0	3	116	0	3	233	—	—	—	—	—	—
2.5k	0	2	49	0	1	249	0	3	46	0	3	93	0	3	187	0	3	249
5k	0	2	24	0	1	124	0	2	93	0	3	46	0	3	93	0	3	124
10k	0	1	49	0	0	249	0	2	46	0	2	93	0	3	46	0	2	249
25k	0	2	4	0	1	24	0	1	74	0	1	149	0	2	74	0	3	24
50k	0	1	9	0	0	49	0	0	149	0	1	74	0	1	149	0	2	49
100k	0	1	4	0	0	24	0	0	74	0	0	149	0	1	74	0	2	24
250k	0	1	1	0	0	9	0	0	29	0	1	14	0	1	29	0	2	9
500k	0	1	0	0	0	4	0	0	14	0	0	29	0	1	14	0	2	4
1M	0	0	1	1	0	4	1	0	14	0	0	14	0	0	29	0	1	9
2.5M	—	—	—	0	0	0	0	0	2	0	0	5	0	1	2	0	2	0
5M	—	—	—	1	0	0	1	0	2	0	0	2	0	0	5	0	1	1
7.5M	—	—	—	—	—	—	0	0	0	0	0	1	1	1	0	1	0	10
60M	—	—	—	—	—	—	—	—	—	—	—	—	1	0	0	—	—	—

Note: —: Can be set, but an error over 10% will occur.

Table 26.16 Maximum Bit Rate with External Clock Input (Clock Synchronous Mode, Simple SPI Mode)

TCLK (MHz)	External clock (MHz)	MAX Bit rate (Mbps)	TCLK (MHz)	External clock (MHz)	MAX Bit rate (Mbps)
8	4	4	25	12.5	12.5
10	5	5	30	15	15
12	6	6	33	16.5	16.5
14	7	7	40	20	20
16	8	8	50	25	25
18	9	9	60	30	30
20	10	10	120	60	60

Table 26.17 BRR Settings for Various Bit Rates (Smart Card Interface Mode, n = 0, S = 372) (1 of 4)

Bit rate (bps)	Operating frequency TCLK (MHz)											
	7.1424			10.00			10.7136			13.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	0	0.00	0	1	–30	0	1	–25	0	1	–8.99

Table 26.17 BRR Settings for Various Bit Rates (Smart Card Interface Mode, n = 0, S = 372) (2 of 4)

Bit rate (bps)	Operating frequency TCLK (MHz)											
	14.2848			16.00			18.00			20.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	0.00	0	1	12.01	0	2	–15.99	0	2	–6.66

Table 26.15 各种比特率的BRR设置（时钟同步模式、简单SPI模式）

比特率(bps)	工作频率TCLK(MHz)																	
	8			10			30			60			120			160		
	BGDM	n	N	BGDM	n	N	BGDM	n	N	BGDM	n	N	BGDM	n	N	BGDM	n	N
250	0	3	124	0	3	177	—	—	—	—	—	—	—	—	—	—	—	—
500	0	2	249	0	3	77	0	3	233	—	—	—	—	—	—	—	—	—
1k	0	2	124	0	3	38	0	3	116	0	3	233	—	—	—	—	—	—
2.5k	0	2	49	0	1	249	0	3	46	0	3	93	0	3	187	0	3	249
5k	0	2	24	0	1	124	0	2	93	0	3	46	0	3	93	0	3	124
10k	0	1	49	0	0	249	0	2	46	0	2	93	0	3	46	0	2	249
25k	0	2	4	0	1	24	0	1	74	0	1	149	0	2	74	0	3	24
50k	0	1	9	0	0	49	0	0	149	0	1	74	0	1	149	0	2	49
100k	0	1	4	0	0	24	0	0	74	0	0	149	0	1	74	0	2	24
250k	0	1	1	0	0	9	0	0	29	0	1	14	0	1	29	0	2	9
500k	0	1	0	0	0	4	0	0	14	0	0	29	0	1	14	0	2	4
1M	0	0	1	1	0	4	1	0	14	0	0	14	0	0	29	0	1	9
2.5M	—	—	—	0	0	0	0	0	2	0	0	5	0	1	2	0	2	0
5M	—	—	—	1	0	0	1	0	2	0	0	2	0	0	5	0	1	1
7.5M	—	—	—	—	—	—	0	0	0	0	0	1	1	1	0	1	0	10
60M	—	—	—	—	—	—	—	—	—	—	—	—	1	0	0	—	—	—

Note: —：可设置，但会出现10%以上的误差。

Table 26.16 外部时钟输入的最大比特率（时钟同步模式，简单SPI模式）

TCLK (MHz)	外部时钟(MHz)	最大比特率(Mbps)	TCLK (MHz)	外部时钟(MHz)	最大比特率(Mbps)
8	4	4	25	12.5	12.5
10	5	5	30	15	15
12	6	6	33	16.5	16.5
14	7	7	40	20	20
16	8	8	50	25	25
18	9	9	60	30	30
20	10	10	120	60	60

Table 26.17 各种比特率的BRR设置（智能卡接口模式，n=0，S=372）（1of4）

比特率(bps)	工作频率TCLK(MHz)											
	7.1424			10.00			10.7136			13.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	0	0.00	0	1	–30	0	1	–25	0	1	–8.99

Table 26.17 各种比特率的BRR设置（智能卡接口模式，n=0，S=372）（2of4）

比特率(bps)	工作频率TCLK(MHz)											
	14.2848			16.00			18.00			20.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	0.00	0	1	12.01	0	2	–15.99	0	2	–6.66

Table 26.17 BRR Settings for Various Bit Rates (Smart Card Interface Mode, n = 0, S = 372) (3 of 4)

Bit rate (bps)	Operating frequency TCLK (MHz)											
	25.00			30.00			33.00			40.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	3	–12.49	0	3	5.01	0	4	–7.59	0	5	–6.66

Table 26.17 BRR Settings for Various Bit Rates (Smart Card Interface Mode, n = 0, S = 372) (4 of 4)

Bit rate (bps)	Operating frequency TCLK (MHz)											
	50.00			60.00			120.00			160.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	6	0.01	0	7	5.01	0	16	–1.17	0	21	1.82

Table 26.18 Maximum Bit Rate for Each Operating Frequency (Smart Card Interface Mode, S = 32)

TCLK (MHz)	MAX Bit rate (bps)	n	N	TCLK (MHz)	MAX Bit rate (bps)	n	N
10	156250	0	0	30	468750	0	0
10.7136	167400	0	0	33	515625	0	0
13	203125	0	0	40	625000	0	0
16	250000	0	0	50	781250	0	0
18	281250	0	0	60	937500	0	0
20	312500	0	0	120	1875000	0	0
25	390625	0	0	160	2500000	0	0

Table 26.19 BRR Settings for Various Bit Rates (Simple IIC Mode) (1 of 4)

Bit rate (bps)	Operating frequency TCLK (MHz)											
	8			10			16			20		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10k	0	24	0	0	31	–2.3	1	12	–3.8	1	15	–2.3
25k	0	9	0	0	12	–3.8	1	4	0	1	6	–10.7
50k	0	4	0	0	6	–10.7	1	2	–16.7	1	3	–21.9
100k	0	2	–16.7	0	3	–21.9	0	4	0	0	6	–10.7
250k	0	0	0	0	1	–37.5	0	1	0	0	2	–16.7
350k										0	1	–10.7
400k										0	1	–21.9

Table 26.19 BRR Settings for Various Bit Rates (Simple IIC Mode) (2 of 4)

Bit rate (bps)	Operating frequency TCLK (MHz)											
	25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10k	1	19	–2.3	1	23	–2.3	1	25	–0.8	0	124	0
25k	1	7	–2.3	1	9	–6.3	1	10	–6.3	0	40	0
50k	1	3	–2.3	1	4	–6.3	1	5	–14.1	0	24	0
100k	1	1	–2.3	1	2	–21.9	1	2	–14.1	0	12	–3.85

Table 26.17 各种比特率的BRR设置（智能卡接口模式，n=0，S=372）（3of4）

比特率(bps)	工作频率TCLK(MHz)											
	25.00			30.00			33.00			40.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	3	–12.49	0	3	5.01	0	4	–7.59	0	5	–6.66

Table 26.17 各种比特率的BRR设置（智能卡接口模式，n=0，S=372）（4of4）

比特率(bps)	工作频率TCLK(MHz)											
	50.00			60.00			120.00			160.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	6	0.01	0	7	5.01	0	16	–1.17	0	21	1.82

Table 26.18 每个工作频率的最大比特率（智能卡接口模式，S=32）

TCLK (MHz)	最大比特率(bps)	n	N	TCLK (MHz)	最大比特率(bps)	n	N
10	156250	0	0	30	468750	0	0
10.7136	167400	0	0	33	515625	0	0
13	203125	0	0	40	625000	0	0
16	250000	0	0	50	781250	0	0
18	281250	0	0	60	937500	0	0
20	312500	0	0	120	1875000	0	0
25	390625	0	0	160	2500000	0	0

Table 26.19 各种比特率的BRR设置（简单IIC模式）（1of4）

比特率(bps)	工作频率TCLK(MHz)											
	8			10			16			20		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10k	0	24	0	0	31	–2.3	1	12	–3.8	1	15	–2.3
25k	0	9	0	0	12	–3.8	1	4	0	1	6	–10.7
50k	0	4	0	0	6	–10.7	1	2	–16.7	1	3	–21.9
100k	0	2	–16.7	0	3	–21.9	0	4	0	0	6	–10.7
250k	0	0	0	0	1	–37.5	0	1	0	0	2	–16.7
350k										0	1	–10.7
400k										0	1	–21.9

Table 26.19 各种比特率的BRR设置（简单IIC模式）（2of4）

比特率(bps)	工作频率TCLK(MHz)											
	25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10k	1	19	–2.3	1	23	–2.3	1	25	–0.8	0	124	0
25k	1	7	–2.3	1	9	–6.3	1	10	–6.3	0	40	0
50k	1	3	–2.3	1	4	–6.3	1	5	–14.1	0	24	0
100k	1	1	–2.3	1	2	–21.9	1	2	–14.1	0	12	–3.85

Table 26.19 BRR Settings for Various Bit Rates (Simple IIC Mode) (3 of 4)

Bit rate (bps)	Operating frequency TCLK (MHz)											
	25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
250k	0	3	–21.9	0	3	–6.3	0	4	–17.5	0	4	0
350k	0	2	–25.6	0	2	–10.7	0	2	–1.8	0	3	–10.71
400k	0	1	–2.3	0	1	17.2	0	2	–14.1	0	2	4.17

Table 26.19 BRR Settings for Various Bit Rates (Simple IIC Mode) (4 of 4)

Bit rate (bps)	Operating frequency TCLK (MHz)											
	50			60			120			160		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10k	2	9	–2.3	1	46	–0.27	1	93	–0.27	1	124	0
25k	2	3	–2.3	0	74	0	0	149	0	0	199	0
50k	2	1	–2.3	0	37	–1.32	0	74	0	0	99	0
100k	1	3	–2.3	0	18	–1.32	0	37	–1.31	0	49	0
250k	0	6	–10.7	0	7	–6.25	0	14	0	0	19	0
350k	0	4	–10.7	0	4	7.14	0	10	–2.6	0	13	2.04
400k	0	3	–2.34	0	4	–6.25	0	8	4.17	0	12	–3.85

Table 26.20 Minimum Widths at High and Low Level for SCL at Various Bit Rates (Simple IIC Mode) (1 of 3)

Bit rate (bps)	Operating frequency TCLK (MHz)											
	8			10			16			20		
	n	N	Minimum width of High/Low Level (µs)	n	N	Minimum width of High/Low Level (µs)	n	N	Minimum width of High/Low Level (µs)	n	N	Minimum width of High/Low Level (µs)
10k	0	24	43.75 / 50.00	0	31	44.80 / 51.20	1	12	45.50 / 52.00	1	15	44.80 / 51.20
25k	0	9	17.50 / 20.00	0	12	18.20 / 20.80	1	4	17.50 / 20.00	1	6	19.60 / 22.40
50k	0	4	8.75 / 10.00	0	6	9.80 / 11.20	1	2	10.50 / 12.00	1	3	11.20 / 12.80
100k	0	2	5.25 / 6.00	0	3	5.60 / 6.40	0	4	4.37 / 5.00	0	6	4.90 / 5.60
250k	0	0	1.75 / 2.00	0	1	2.80 / 3.20	0	1	1.75 / 2.00	0	2	2.10 / 2.40
350k										0	1	1.40 / 1.60
400k										0	1	1.40 / 1.60

Table 26.19 各种比特率的BRR设置（简单IIC模式）（3of4）

比特率(bps)	工作频率TCLK(MHz)											
	25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
250k	0	3	–21.9	0	3	–6.3	0	4	–17.5	0	4	0
350k	0	2	–25.6	0	2	–10.7	0	2	–1.8	0	3	–10.71
400k	0	1	–2.3	0	1	17.2	0	2	–14.1	0	2	4.17

Table 26.19 各种比特率的BRR设置（简单IIC模式）（4之4）

比特率(bps)	工作频率TCLK(MHz)											
	50			60			120			160		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10k	2	9	–2.3	1	46	–0.27	1	93	–0.27	1	124	0
25k	2	3	–2.3	0	74	0	0	149	0	0	199	0
50k	2	1	–2.3	0	37	–1.32	0	74	0	0	99	0
100k	1	3	–2.3	0	18	–1.32	0	37	–1.31	0	49	0
250k	0	6	–10.7	0	7	–6.25	0	14	0	0	19	0
350k	0	4	–10.7	0	4	7.14	0	10	–2.6	0	13	2.04
400k	0	3	–2.34	0	4	–6.25	0	8	4.17	0	12	–3.85

Table 26.20 各种比特率下SCL的高电平和低电平最小宽度（简单IIC模式）（1of3）

比特率(bps)	工作频率TCLK(MHz)											
	8			10			16			20		
	n	N	高低电平的最小宽度(µs)	n	N	高低电平的最小宽度(µs)	n	N	高低电平的最小宽度(µs)	n	N	高低电平的最小宽度(µs)
10k	0	24	43.75 / 50.00	0	31	44.80 / 51.20	1	12	45.50 / 52.00	1	15	44.80 / 51.20
25k	0	9	17.50 / 20.00	0	12	18.20 / 20.80	1	4	17.50 / 20.00	1	6	19.60 / 22.40
50k	0	4	8.75 / 10.00	0	6	9.80 / 11.20	1	2	10.50 / 12.00	1	3	11.20 / 12.80
100k	0	2	5.25 / 6.00	0	3	5.60 / 6.40	0	4	4.37 / 5.00	0	6	4.90 / 5.60
250k	0	0	1.75 / 2.00	0	1	2.80 / 3.20	0	1	1.75 / 2.00	0	2	2.10 / 2.40
350k										0	1	1.40 / 1.60
400k										0	1	1.40 / 1.60

Table 26.20 Minimum Widths at High and Low Level for SCL at Various Bit Rates (Simple IIC Mode) (2 of 3)

Bit rate (bps)	Operating frequency TCLK (MHz)											
	25			30			33			40		
	n	N	Minimum width of High/Low Level (µs)	n	N	Minimum width of High/Low Level (µs)	n	N	Minimum width of High/Low Level (µs)	n	N	Minimum width of High/Low Level (µs)
10k	1	19	44.80 / 51.20	1	23	44.80 / 51.20	1	25	44.12 / 50.42	1	32	46.20 / 52.80
25k	1	7	17.92 / 20.48	1	9	18.66 / 21.33	1	10	18.66 / 21.33	1	12	18.20 / 20.80
50k	1	3	8.96 / 10.24	1	4	9.33 / 10.66	1	5	10.18 / 11.63	1	6	9.80 / 11.20
100k	1	1	4.48 / 5.12	1	2	5.60 / 6.40	1	2	5.09 / 5.81	0	13	4.90 / 5.60
250k	0	3	2.24 / 2.56	0	3	1.86 / 2.13	0	4	2.12 / 2.42	0	4	1.75 / 2.00
350k	0	2	1.68 / 1.92	0	2	1.40 / 1.60	0	2	1.27 / 1.45	0	3	1.40 / 1.60
400k	0	1	1.12 / 1.28	0	1	0.93 / 1.07	0	2	1.27 / 1.45	0	2	1.05 / 1.20

Table 26.20 Minimum Widths at High and Low Level for SCL at Various Bit Rates (Simple IIC Mode) (3 of 3)

Bit rate (bps)	Operating frequency TCLK (MHz)											
	50			60			120			160		
	n	N	Minimum width of High/Low Level (µs)	n	N	Minimum width of High/Low Level (µs)	n	N	Minimum width of High/Low Level (µs)	n	N	Minimum width of High/Low Level (µs)
10k	2	9	44.80 / 51.20	1	47	44.80 / 51.20	1	93	43.87 / 50.13	1	124	43.75 / 50
25k	2	3	17.92 / 20.48	0	74	17.50 / 20.00	0	149	17.50 / 20.00	0	199	17.50 / 20.00
50k	2	1	8.96 / 10.24	0	37	8.87 / 10.13	0	74	8.75 / 10.00	0	99	8.75 / 10.00
100k	1	3	4.48 / 5.12	0	18	4.43 / 5.07	0	37	4.43 / 5.07	0	49	4.38 / 5.00
250k	0	6	1.96 / 2.24	0	7	1.87 / 2.13	0	15	1.87 / 2.13	0	49	1.75 / 2.00
350k	0	4	1.40 / 1.60	0	5	1.40 / 1.60	0	10	1.28 / 1.47	0	19	1.23 / 1.40
400k	0	3	1.12 / 1.28	0	4	1.17 / 1.33	0	9	1.17 / 1.33	0	12	1.14 / 1.30

BRME bit (Bit Modulation Enable)

Enables and disables the bit rate modulation function. The bit rate generated by on-chip baud rate generator is evenly corrected when this function is enabled.

Set to 0 in Clock-synchronous mode, Simple SPI mode, Smart Card Interface mode, Manchester mode and Simple LIN mode.

CKS[1:0] bit (Clock Select)

These bits select the clock source for the on-chip baud rate generator.

For the relationship between the settings of these bits and the baud rate, refer to BRR[7:0] bits explanation.

MDDR[7:0] bit (Modulation Duty Setting)

When the BRME bit is set to 1, the bit rate generated by the on-chip baud rate generator is evenly corrected according to the settings of MDDR (M/256). The relationship between the MDDR setting (M) and the bit rate (B) is given in Table 26.21.

The initial value of MDDR is FFh. Bit 7 in this register is fixed to 1.

Table 26.20 不同比特率下SCL的高电平和低电平最小宽度（简单IIC模式）（2of3）

比特率(bps)工作频率TCLK(MHz)												
	25			30			33			40		
	n	N	最小宽度 High/Low Level (µs)	n	N	最小宽度 High/Low Level (µs)	n	N	最小宽度 High/Low Level (µs)	n	N	最小宽度 High/Low Level (µs)
10k	1	19	44.80 / 51.20	1	23	44.80 / 51.20	1	25	44.12 / 50.42	1	32	46.20 / 52.80
25k	1	7	17.92 / 20.48	1	9	18.66 / 21.33	1	10	18.66 / 21.33	1	12	18.20 / 20.80
50k	1	3	8.96 / 10.24	1	4	9.33 / 10.66	1	5	10.18 / 11.63	1	6	9.80 / 11.20
100k	1	1	4.48 / 5.12	1	2	5.60 / 6.40	1	2	5.09 / 5.81	0	13	4.90 / 5.60
250k	0	3	2.24 / 2.56	0	3	1.86 / 2.13	0	4	2.12 / 2.42	0	4	1.75 / 2.00
350k	0	2	1.68 / 1.92	0	2	1.40 / 1.60	0	2	1.27 / 1.45	0	3	1.40 / 1.60
400k	0	1	1.12 / 1.28	0	1	0.93 / 1.07	0	2	1.27 / 1.45	0	2	1.05 / 1.20

Table 26.20 各种比特率下SCL的高电平和低电平最小宽度（简单IIC模式）（3之3）

比特率(bps)工作频率TCLK(MHz)												
	50			60			120			160		
	n	N	高低电平的最小宽度(µs)	n	N	最小宽度 High/Low Level (µs)	n	N	最小宽度 High/Low Level (µs)	n	N	最小宽度 High/Low Level (µs)
10k	2	9	44.80 / 51.20	1	47	44.80 / 51.20	1	93	43.87 / 50.13	1	124	43.75 / 50
25k	2	3	17.92 / 20.48	0	74	17.50 / 20.00	0	149	17.50 / 20.00	0	199	17.50 / 20.00
50k	2	1	8.96 / 10.24	0	37	8.87 / 10.13	0	74	8.75 / 10.00	0	99	8.75 / 10.00
100k	1	3	4.48 / 5.12	0	18	4.43 / 5.07	0	37	4.43 / 5.07	0	49	4.38 / 5.00
250k	0	6	1.96 / 2.24	0	7	1.87 / 2.13	0	15	1.87 / 2.13	0	49	1.75 / 2.00
350k	0	4	1.40 / 1.60	0	5	1.40 / 1.60	0	10	1.28 / 1.47	0	19	1.23 / 1.40
400k	0	3	1.12 / 1.28	0	4	1.17 / 1.33	0	9	1.17 / 1.33	0	12	1.14 / 1.30

BRME位（位调制使能）

启用和禁用比特率调制功能。该功能使能时，片内波特率发生器产生的比特率得到均匀校正。

在时钟同步模式、简单SPI模式、智能卡接口模式、曼彻斯特模式和简单LIN模式下设置为0。

CKS[1:0] bit (Clock Select)

这些位选择片内波特率发生器的时钟源。

这些位的设置与波特率的关系请参考BRR[7:0]位说明。

MDDR[7:0]位（调制占空比设置）

当BRME位设置为1时，片内波特率发生器产生的比特率根据MDDR(M256)的设置进行均匀校正。MDDR设置(M)和比特率(B)之间的关系在表26.21中给出。

MDDR的初始值为FFh。该寄存器的第7位固定为1。

Table 26.21 Relationship between MDDR Setting (M) and Bit Rate (B) When Bit Rate Modulation Function is Used

Mode*1	CCR2 settings			BRR setting	Error
	BGDM bit	ABCS bit	ABCSE bit		
Asynchronous, Multiprocessor transger	0	0	0	$N = \frac{TCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
	1	0	0	$N = \frac{TCLK \times 10^6}{32 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{TCLK \times 10^6}{16 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
	x (Arbitrarily)	x (Arbitrarily)	1*2	$N = \frac{TCLK \times 10^6}{12 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
Simple IIC*2	$N = \frac{TCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$				

Note: B: Bit rate (bps)
M: MDDR setting (128 ≤ M ≤ 255)
N: BRR setting for bound rate generator (0 ≤ N ≤ 255)
TCLK: Operating frequency (MHz)
n: Determined by the settings of the CKS[1:0] as listed in Table 26.8.

Note 1. Do not use this function in Clock-synchronous mode, Simple SPI mode, Smart card Interface mode, Manchester mode and Simple LIN mode.

Note 2. Adjust the bit rate so that the widths at high and low level of the SCL output in simple IIC mode satisfy the I2C standard.

Table 26.22 and Table 26.23 list examples of N settings in BRR and M settings in MDDR in asynchronous mode.

Table 26.22 Examples of BRR and MDDR Settings for Various Bit Rates (Asynchronous Mode) (1) (1 of 3)

Bit rate (bps)	Operating frequency TCLK (MHz)														
	8					9.8304					10				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	5	236	0	0.03	0	7	(256) *1	0	0	0	10	173	1	–0.01
57600	0	3	236	0	0.03	0	4	240	0	0	0	4	236	0	0.03
115200	0	1	236	0	0.03	0	1	192	0	0	0	4	236	1	0.03
230400	0	0	236	0	0.03	0	0	192	0	0	0	1	189	1	0.14
460800	0	0	236	1	0.03	0	0	192	1	0	0	0	189	1	0.14

Table 26.22 Examples of BRR and MDDR Settings for Various Bit Rates (Asynchronous Mode) (1) (2 of 3)

Bit rate (bps)	Operating frequency TCLK (MHz)														
	12					12.288					14				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	8	236	0	0.03	0	9	(256) *1	0	0	0	16	191	1	0
57600	0	5	236	0	0.03	0	4	192	0	0	0	13	236	1	0.03
115200	0	2	236	0	0.03	0	4	192	1	0	0	6	236	1	0.03
230400	0	2	236	1	0.03	0	2	230	1	–0.17	0	2	202	1	–0.11
460800	0	0	157	1	–0.18	0	0	154	1	0.26	0	0	135	1	0.14

Table 26.21 使用比特率调制功能时MDDR设置(M)和比特率(B)的关系

Mode*1	CCR2 settings			BRR setting	Error
	BGDM bit	ABCS位	ABCSE位		
异步、多处理器或传输器	0	0	0	$N = \frac{TCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
	1	0	0	$N = \frac{TCLK \times 10^6}{32 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{TCLK \times 10^6}{16 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
	x (Arbitrarily)	x (Arbitrarily)	1*2	$N = \frac{TCLK \times 10^6}{12 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \left\{\frac{TCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
Simple IIC*2	$N = \frac{TCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$				

Note: B：比特率（bps）
M：MDDR设置(128≤M≤255)N：绑定速率生成器的BR
R设置(0≤N≤255)
TCLK：工作频率(MHz)n：由CKS[1:0]的设置决定，如表26.8中所列。

注1.不要在时钟同步模式、简单SPI模式、智能卡接口模式、曼彻斯特模式和简单模式下使用此功能
LIN模式。
注2.调整比特率，使简单IIC模式下SCL输出的高低电平宽度满足I2C标准。

表26.22和表26.23列出了异步模式下BRR中的N设置和MDDR中的M设置的示例。

Table 26.22 各种比特率（异步模式）的BRR和MDDR设置示例(1)(1of3)

比特率(bps)	工作频率TCLK(MHz)														
	8					9.8304					10				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	5	236	0	0.03	0	7	(256) *1	0	0	0	10	173	1	–0.01
57600	0	3	236	0	0.03	0	4	240	0	0	0	4	236	0	0.03
115200	0	1	236	0	0.03	0	1	192	0	0	0	4	236	1	0.03
230400	0	0	236	0	0.03	0	0	192	0	0	0	1	189	1	0.14
460800	0	0	236	1	0.03	0	0	192	1	0	0	0	189	1	0.14

Table 26.22 各种比特率（异步模式）的BRR和MDDR设置示例(1)(2of3)

比特率(bps)	工作频率TCLK(MHz)														
	12					12.288					14				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	8	236	0	0.03	0	9	(256) *1	0	0	0	16	191	1	0
57600	0	5	236	0	0.03	0	4	192	0	0	0	13	236	1	0.03
115200	0	2	236	0	0.03	0	4	192	1	0	0	6	236	1	0.03
230400	0	2	236	1	0.03	0	2	230	1	–0.17	0	2	202	1	–0.11
460800	0	0	157	1	–0.18	0	0	154	1	0.26	0	0	135	1	0.14

Table 26.22 Examples of BRR and MDDR Settings for Various Bit Rates (Asynchronous Mode) (1) (3 of 3)

Bit rate (bps)	Operating frequency TCLK (MHz)														
	16					17.2032					18				
	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)
38400	0	11	236	0	0.03	0	13	(256) *1	0	0	0	18	166	1	–0.01
57600	0	7	236	0	0.03	0	6	192	0	0	0	18	249	1	–0.01
115200	0	3	236	0	0.03	0	6	192	1	0	0	8	236	1	0.03
230400	0	1	236	0	0.03	0	3	219	1	–0.2	0	1	210	0	0.14
460800	0	1	236	1	0.03	0	1	219	1	–0.2	0	0	210	0	0.14

Note: This is an example when the CCR2.ABCS = 0 and CCR2.ABCSE = 0.
Note 1. It means that the bit rate modulation function is disable. (CCR2.BRME = 0, M = 256)

Table 26.23 Examples of BRR and MDDR Settings for Various Bit Rates (Asynchronous Mode) (2) (1 of 4)

Bit rate (bps)	Operating frequency TCLK (MHz)														
	19.6608					20					25				
	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)
38400	0	15	(256) *1	0	0	0	10	173	0	–0.01	0	11	151	0	0
57600	0	9	240	0	0	0	9	236	0	0.03	0	7	151	0	0
115200	0	4	240	0	0	0	4	236	0	0.03	0	3	151	0	0
230400	0	1	192	0	0	0	4	236	1	0.03	0	1	151	0	0
460800	0	0	192	0	0	0	0	189	0	0.14	0	0	151	0	0

Table 26.23 Examples of BRR and MDDR Settings for Various Bit Rates (Asynchronous Mode) (2) (2 of 4)

Bit rate (bps)	Operating frequency TCLK (MHz)														
	30					33					40				
	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)
38400	0	36	194	1	0.01	0	14	143	0	0.01	0	21	173	0	–0.01
57600	0	10	173	0	–0.01	0	9	143	0	0.01	0	38	230	1	–0.01
115200	0	10	173	1	–0.01	0	4	143	0	0.01	0	9	236	0	0.03
230400	0	6	220	1	–0.09	0	4	143	1	0.01	0	4	236	0	0.03
460800	0	3	252	1	0.14	0	1	229	0	0.1	0	4	236	1	0.03

Table 26.23 Examples of BRR and MDDR Settings for Various Bit Rates (Asynchronous Mode) (2) (3 of 4)

Bit rate (bps)	Operating frequency TCLK (MHz)														
	50					60					120				
	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)
38400	0	23	151	0	0	0	36	194	0	0.01	0	73	194	0	0.01
57600	0	15	151	0	0	0	21	173	0	–0.01	0	58	232	0	0
115200	0	7	151	0	0	0	10	173	0	–0.01	0	21	173	0	–0.01
230400	0	3	151	0	0	0	10	173	1	–0.01	0	10	173	0	–0.01
460800	0	1	151	0	0	0	6	220	1	–0.09	0	10	173	1	–0.01

Table 26.22 各种比特率（异步模式）的BRR和MDDR设置示例(1)(3of3)

比特率(bps)	工作频率TCLK(MHz)														
	16					17.2032					18				
	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)
38400	0	11	236	0	0.03	0	13	(256) *1	0	0	0	18	166	1	–0.01
57600	0	7	236	0	0.03	0	6	192	0	0	0	18	249	1	–0.01
115200	0	3	236	0	0.03	0	6	192	1	0	0	8	236	1	0.03
230400	0	1	236	0	0.03	0	3	219	1	–0.2	0	1	210	0	0.14
460800	0	1	236	1	0.03	0	1	219	1	–0.2	0	0	210	0	0.14

Note: 这是CCR2.ABCS=0和CCR2.ABCSE=0时的示例。
注1.表示码率调制功能关闭。（CCR2.BRME=0，M=256）

Table 26.23 各种比特率（异步模式）的BRR和MDDR设置示例(2)(1of4)

比特率(bps)	工作频率TCLK(MHz)														
	19.6608					20					25				
	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)
38400	0	15	(256) *1	0	0	0	10	173	0	–0.01	0	11	151	0	0
57600	0	9	240	0	0	0	9	236	0	0.03	0	7	151	0	0
115200	0	4	240	0	0	0	4	236	0	0.03	0	3	151	0	0
230400	0	1	192	0	0	0	4	236	1	0.03	0	1	151	0	0
460800	0	0	192	0	0	0	0	189	0	0.14	0	0	151	0	0

Table 26.23 各种比特率（异步模式）的BRR和MDDR设置示例(2)(2of4)

比特率(bps)	工作频率TCLK(MHz)														
	30					33					40				
	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)
38400	0	36	194	1	0.01	0	14	143	0	0.01	0	21	173	0	–0.01
57600	0	10	173	0	–0.01	0	9	143	0	0.01	0	38	230	1	–0.01
115200	0	10	173	1	–0.01	0	4	143	0	0.01	0	9	236	0	0.03
230400	0	6	220	1	–0.09	0	4	143	1	0.01	0	4	236	0	0.03
460800	0	3	252	1	0.14	0	1	229	0	0.1	0	4	236	1	0.03

Table 26.23 各种比特率（异步模式）的BRR和MDDR设置示例(2)(3of4)

比特率(bps)	工作频率TCLK(MHz)														
	50					60					120				
	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)	n	N	M	BGD M bit	Error (%)
38400	0	23	151	0	0	0	36	194	0	0.01	0	73	194	0	0.01
57600	0	15	151	0	0	0	21	173	0	–0.01	0	58	232	0	0
115200	0	7	151	0	0	0	10	173	0	–0.01	0	21	173	0	–0.01
230400	0	3	151	0	0	0	10	173	1	–0.01	0	10	173	0	–0.01
460800	0	1	151	0	0	0	6	220	1	–0.09	0	10	173	1	–0.01

Table 26.23 Examples of BRR and MDDR Settings for Various Bit Rates (Asynchronous Mode) (2) (4 of 4)

Bit rate (bps)	Operating frequency TCLK (MHz)				
	160				
	n	N	M	BGDM bit	Error (%)
38400	0	117	232	0	0
57600	0	58	174	0	0
115200	1	58	174	0	0
230400	1	38	230	0	–0.01
460800	0	9	236	0	0.03

Note: This is an example when the CCR2.ABCS = 0 and CCR2.ABCSE = 0.
Note 1. It means that the bit rate modulation function is disable. (CCR2.BRME = 0, M = 256)

26.2.8 CCR3 : Common Control Register 3

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	BLK	GM	—	—	CKE[1:0]		—	—	DEN	FM	MP	MOD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RXDESEL	STP	SINV	LSBF	—	—	CHR[1:0]		BPEN	—	—	—	—	—	CPOL	CPHA
Value after reset:	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	CPHA	Clock Phase Select Valid in Cock-synchronous mode and Simple SPI mode. Set this bit only when CCR0.TE = 0 and RE = 0. 0: Data is sampled at an odd edge and changes at an even edge. (Clock is delayed.) 1: Data changes at an odd edge and is sampled at an even edge. (Clock is not delayed)	R/W
1	CPOL	Clock Polarity Select Valid in Cock-synchronous mode and Simple SPI mode. Set this bit only when CCR0.TE = 0 and RE = 0. 0: SCKn in idle state is 0. 1: SCKn in idle state is 1.	R/W
6:2	—	These bits are read as 0. The write value should be 0.	R/W
7	BPEN	Synchronizer bypass enable This bit controls whether to bypass the synchronizer circuit between the bus clock and operation clock. 0: Synchronizer circuit is not bypassed. 1: Synchronizer circuit is bypassed.	R/W
9:8	CHR[1:0]	Character Length Valid in Asynchronous mode and Manchester mode*1 Select the data length for transmission and reception. 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length*2	R/W
11:10	—	These bits are read as 0. The write value should be 0.	R/W

Table 26.23 各种比特率（异步模式）的BRR和MDDR设置示例(2)(4of4)

比特率(bps)	工作频率TCLK(MHz)				
	160				
	n	N	M	BGDM bit	Error (%)
38400	0	117	232	0	0
57600	0	58	174	0	0
115200	1	58	174	0	0
230400	1	38	230	0	–0.01
460800	0	9	236	0	0.03

Note: 这是CCR2.ABCS=0和CCR2.ABCSE=0时的示例。
注1.表示码率调制功能关闭。（CCR2.BRME=0，M=256）

26.2.8 CCR3:公共控制寄存器3

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	BLK	GM	—	—	CKE[1:0]		—	—	DEN	FM	MP	MOD[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RXDESEL	STP	SINV	LSBF	—	—	CHR[1:0]		BPEN	—	—	—	—	—	CPOL	CPHA
重置后的值:	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	CPHA	时钟相位选择 在Cock同步模式和简单SPI模式下有效。仅当CCR0.TE=0且RE=0时设置该位。 0：数据在奇数边沿采样，在偶数边沿变化。（时钟延迟。）1：数据在奇边沿变化，在偶边沿采样。（时钟不延迟）	R/W
1	CPOL	时钟极性选择 在Cock同步模式和简单SPI模式下有效。仅当CCR0.TE=0且RE=0时设置该位。 0：空闲状态的SCKn为0。 1：空闲状态的SCKn为1。	R/W
6:2	—	这些位被读取为0。写入值应为0。	R/W
7	BPEN	同步器旁路使能 该位控制是否绕过总线时钟和操作时钟之间的同步器电路。 0：同步器电路不被旁路。1：同步器电路被旁路。	R/W
9:8	CHR[1:0]	字符长度 在异步模式和曼彻斯特模式下有效*1 选择发送和接收的数据长度。 00：发送接收9位数据长度01：发送接收9位数据长度1 0：发送接收8位数据长度（初始值）11：发送接收7位数据长度*2	R/W
11:10	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
12	LSBF	LSB First select Set this bit to 0 in simple IIC mode. Set this bit to 1 in simple LIN mode. 0: MSB first 1: LSB first	R/W
13	SINV	Transmitted/Received Data Invert Set this bit to 0 in Simple IIC mode. The level of communication terminals (RXDn/TXDn) are controlled by combination of this bit and CCR1.TINV/RINV. Please refer to Figure 26.3 in details. 0: TDR contents are transmitted to TSR as they are. RSR contents are stored to RDR as they are. 1: TDR contents are inverted before being transmitted to TSR. RSR contents are inverted and stored to RDR.	R/W
14	STP	Stop Bit Length Valid in Asynchronous mode, Manchester mode, Simple LIN mode 0: 1 stop bit / Break Delimiter length is 1bit 1: 2 stop bits / Break Delimiter length is 2bits	R/W
15	RXDESEL	Asynchronous Start Bit Edge Detection Select Valid only in asynchronous mode Set this bit to 1 in simple LIN mode. 0: The low level on the RXDn pin is detected as the start bit. 1: A falling edge on the RXDn pin is detected as the start bit.	R/W
18:16	MOD[2:0]	Communication mode select Select the SCI communication mode. 0 0 0: Asynchronous mode (Multi-processor mode) 0 0 1: Smart card interface mode 0 1 0: Clock synchronous mode 0 1 1: Simple SPI mode 1 0 0: Simple IIC mode 1 0 1: Manchester mode 1 1 0: Simple LIN mode 1 1 1: Setting prohibited	R/W
19	MP	Multi-Processor Mode Valid in Asynchronous mode, Manchester mode 0: Multi-processor communications function is disabled 1: Multi-processor communications function is enabled	R/W
20	FM	FIFO Mode select Valid in Asynchronous mode (including multi-processor mode), Clock synchronous mode, Simple SPI mode 0: TDR register, RDR register is non-FIFO buffer configuration 1: TDR register, RDR register is FIFO buffer configuration	R/W
21	DEN	Driver enable 0: RS-485 Driver control function disable. 1: RS-485 Driver control function enable.	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
12	LSBF	LSB优先选择 在简单IIC模式下将此位设置为0。 在简单LIN模式下将此位设置为1。 0: MSB first 1: LSB first	R/W
13	SINV	发送接收数据反转 在SimpleIIC模式下将此位设置为0。 通讯终端的电平（RXDnTXDn）由该位和CCR1.TINVRINV组合控制。详见图26.3。 0：TDR内容按原样发送到TSR。RSR内容按原样存储到RDR。 1：TDR内容在发送到TSR之前被反转。RSR内容被反转并存储到RDR。	R/W
14	STP	停止位长度 在异步模式、曼彻斯特模式、简单LIN模式下有效 0：1个停止位BreakDelimiter长度为1bit1：2个停止位BreakDelimiter长度为2bits	R/W
15	RXDESEL	异步起始位边沿检测选择 仅在异步模式下有效 在简单LIN模式下将此位设置为1。 0：RXDn引脚的低电平被检测为起始位。1：RXDn引脚的下降沿被检测为起始位。	R/W
18:16	MOD[2:0]	通讯方式选择 选择SCI通信模式。 000：异步模式（多处理器模式）001：智能卡接口模式010：时钟同步模式011：简单SPI模式100：简单IIC模式101：曼彻斯特模式110：简单LIN模式111：禁止设置	R/W
19	MP	Multi-Processor Mode 在异步模式、曼彻斯特模式下有效 0：禁用多机通讯功能1：启用多机通讯功能	R/W
20	FM	FIFO模式选择在异步模式（包括多处理器模式）、时钟同步模式下有效， 简单SPI模式 0：TDR寄存器，RDR寄存器为非FIFO缓冲配置1：TDR寄存器，RDR寄存器为FIFO缓冲配置	R/W
21	DEN	驱动程序启用 0：RS-485驱动控制功能禁用。1：RS-485驱动控制功能使能。	R/W
23:22	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
25:24	CKE[1:0]	Clock enable 0 0: In the case of Asynchronous mode On-chip baud rate generator The SCKn pin is available for use as an I/O port in accord with the I/O port settings. In the case of Manchester mode and Simple LIN mode On-chip baud rate generator The SCKn pin functions as I/O port. In the case of Clock synchronous mode, Simple SPI mode Internal clock (Master operation) The SCKn pin functions as the clock output pin. In the case of Smart card interface mode and CCR3.GM = 0 Output disabled (The SCKn pin is available for use as an I/O port in accord with the I/O port settings.) In the case of Smart card interface mode and CCR3.GM = 1 Output fixed low 0 1: In the case of Asynchronous mode On-chip baud rate generator The clock with the same frequency as the bit rate is output from the SCKn pin. In the case of Manchester mode and Simple LIN mode Prohibited In the case of Clock synchronous mode, Simple SPI mode Internal clock (Master operation) The SCKn pin functions as the clock output pin. In the case of Smart card interface mode and CCR3.GM = 0 Clock output In the case of Smart card interface mode and CCR3.GM = 1 Clock output 1 0: In the case of Asynchronous mode External clock • When using the external clock 16 times the bit rate should be input from the SCKn pin when CCR2.ABCS bit is 0. Input a clock signal with a frequency 8 times the bit rate when the CCR2.ABCS bit is 1. In the case of Manchester mode and Simple LIN mode Prohibited In the case of Clock synchronous mode, Simple SPI mode External clock (Slave operation) The SCKn pin functions as the clock input pin. In the case of Smart card interface mode and CCR3.GM = 0 Prohibited In the case of Smart card interface mode and CCR3.GM = 1 Output fixed high 1 1: In the case of Asynchronous mode External clock • When using the external clock 16 times the bit rate should be input from the SCKn pin when CCR2.ABCS bit is 0. Input a clock signal with a frequency 8 times the bit rate when the CCR2.ABCS bit is 1. In the case of Manchester mode and Simple LIN mode Prohibited In the case of Clock synchronous mode, Simple SPI mode External clock (Slave operation) The SCKn pin functions as the clock input pin. In the case of Smart card interface mode and CCR3.GM = 0 Prohibited In the case of Smart card interface mode and CCR3.GM = 1 Clock output	R/W
27:26	—	These bits are read as 0. The write value should be 0.	R/W
28	GM	GSM Mode Valid only in Smart card interface mode 0: Non-GSM mode operation 1: GSM mode operation	R/W

Bit	Symbol	Function	R/W
25:24	CKE[1:0]	时钟使能 00：异步模式情况下片内波特率发生器 根据IO端口设置，SCKn引脚可用作IO端口。在曼彻斯特模式和简单LIN模式的情况下 片上波特率发生器 SCKn引脚用作IO端口。 在时钟同步模式的情况下，简单SPI模式 内部时钟（主机操作） SCKn引脚用作时钟输出引脚。 在智能卡接口模式和CCR3.GM=0的情况下 输出禁用（根据IO端口设置，SCKn引脚可用作IO端口。）在智能卡接口模式和CCR3.GM=1的情况下 输出固定低 01：异步模式下片内波特率发生器 从SCKn引脚输出与比特率相同频率的时钟。在曼彻斯特模式和简单LIN模式的情况下 Prohibited 在时钟同步模式的情况下，简单SPI模式 内部时钟（主机操作） SCKn引脚用作时钟输出引脚。 在智能卡接口模式和CCR3.GM=0的情况下时钟输出在智能卡接口模式和CCR3.GM=1的情况下 时钟输出 10：异步模式时外部时钟● 使用外部时钟时，应在CCR2.ABCS位为0时从SCKn引脚输入16倍比特率。当CCR2.ABCS位为1时，输入频率为8倍比特率的时钟信号。曼彻斯特模式和简单LIN模式 Prohibited 在时钟同步模式的情况下，简单SPI模式 外部时钟（从机操作） SCKn引脚用作时钟输入引脚。 在智能卡接口模式和CCR3.GM=0的情况下禁止 在智能卡接口模式和CCR3.GM=1的情况下 输出固定高 11：异步模式下外部时钟● 使用外部时钟时，应在CCR2.ABCS位为0时从SCKn引脚输入16倍比特率。当CCR2.ABCS位为1时，输入频率为8倍比特率的时钟信号。曼彻斯特模式和简单LIN模式 Prohibited 在时钟同步模式的情况下，简单SPI模式 外部时钟（从机操作） SCKn引脚用作时钟输入引脚。 在智能卡接口模式和CCR3.GM=0的情况下禁止 在智能卡接口模式和CCR3.GM=1的情况下 时钟输出	R/W
27:26	—	这些位被读取为0。写入值应为0。	R/W
28	GM	GSM Mode 仅在智能卡接口模式下有效 0：非GSM模式操作1：GSM模式操作	R/W

Bit	Symbol	Function	R/W
29	BLK	Block Transfer Mode Valid only in Smart card interface mode 0: Non-block transfer mode operation 1: Block transfer mode operation	R/W
31:30	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. In other than asynchronous mode and manchester mode, this bit setting is invalid and a fixed data length of 8 bits is used. In the Simple LIN mode, only the data length of 8 bits can be used, so set it to the initial value.
Note 2. LSB first is fixed and the MSB (bit 7) in TDR is not transmitted in transmission.

CPHA bit (Clock Phase Select)

This bit selects the phase of the clock signal output through the SCKn pin. Refer to Figure 26.97 in details.

Set the bit to 1 in other than simple SPI mode and clock synchronous mode.

CPOL bit (Clock Polarity Select)

This bit selects the polarity of the clock signal output through the SCKn pin. Refer to Figure 26.97 in details.

Set the bit to 1 in other than simple SPI mode and clock synchronous mode.

BPEN bit (Synchronizer bypass enable)

The synchronization circuit can be bypassed by this bit only when the same clock is input to the bus clock and the operation clock (TCLK). Refer to section 26.19. Synchronizer Bypass Function in details.

Usage Notes about this bit setting, please refers to section 26.20.17. Notes on CCR3.BPEN bit setting for more detail.

CHR[1:0] bit (Character Length)

Selects the data length for transmission and reception.

Except of asynchronous mode and manchester mode, a fixed data length of 8 bits is used.

LSBF bit (LSB First select)

Select whether to transmit/receive data in MSB first or LSB first.

SINV bit (Transmitted/Received Data Invert)

SINV can invert the transmit data-bit from TDR to TSR, and can invert the received data from RSR to RDR. This bit does not affect the logic level of the parity bit. To invert the parity bit, invert the CCR1.PM.

STP bit (Stop Bit Length)

Selects the stop bit length in transmission.

In reception, only the first stop bit is checked regardless of this bit setting. If the second stop bit is 0, it is treated as the start bit of the next transmit frame.

In addition, it is used as Break Delimiter length setting when sending Start Frame in simple LIN mode.

RXDESEL bit (Asynchronous Start Bit Edge Detection Select)

Selects the detection method of the start bit for reception in asynchronous mode. When a break occurs, data receiving operation depends on the settings of this bit. Set this bit to 1 when reception should be stopped while a break occurs or when reception should be started without retaining the RXDn pin input at high level for the period of one data frame or longer after completion of the break.

Set this bit to 1 in Simple LIN mode. Set this bit to 0 in modes except of asynchronous mode and Simple LIN mode.

MOD[2:0] bit (Communication mode select)

Selects the SCI communication mode.

Bit	Symbol	Function	R/W
29	BLK	块传输模式 仅在智能卡接口模式下有效 0：非块传输模式操作1：块传输模式 操作	R/W
31:30	—	这些位被读取为0。写入值应为0。	R/W

注1.除异步模式和曼彻斯特模式外，该位设置无效，使用8位固定数据长度。在里面
简易LIN模式，只能使用8位的数据长度，所以设置为初始值。
注2.LSB在前是固定的，TDR中的MSB（第7位）在传输中不传输。

CPHA位（时钟相位选择）

该位选择通过SCKn引脚输出的时钟信号的相位。详见图26.97。

在简单SPI模式和时钟同步模式以外的情况下将该位设置为1。

CPOL位（时钟极性选择）

该位选择通过SCKn引脚输出的时钟信号的极性。详见图26.97。

在简单SPI模式和时钟同步模式以外的情况下将该位设置为1。

BPEN位（同步器旁路使能）

只有当总线时钟和操作时钟（TCLK）输入相同的时钟时，该位才能绕过同步电路。请参阅第26.19节。详细同步器旁路功能。

关于此位设置的使用说明，请参阅第26.20.17节。有关CCR3.BPEN位设置的注释以获取更多详细信息。

CHR[1:0] bit (Character Length)

选择发送和接收的数据长度。

除异步模式和曼彻斯特模式外，使用8位的固定数据长度。

LSBF位（LSB优先选择）

选择是以MSB先还是LSB先发送接收数据。

SINV位（发送接收数据反转）

SINV可以将发送数据位从TDR反转到TSR，并且可以将接收到的数据从RSR反转到RDR。该位不影响奇偶校验位的逻辑电平。要反转奇偶校验位，请反转CCR1.PM。

STP bit (Stop Bit Length)

选择传输中的停止位长度。

在接收中，无论该位设置如何，都只检查第一个停止位。如果第二个停止位为0，则将其视为下一个发送帧的起始位。

此外，在简单LIN模式下发送StartFrame时，它 用作BreakDelimiter长度设置。

RXDESEL位（异步起始位边沿检测选择）

选择异步模式下接收起始位的检测方法。发生中断时，数据接收操作取决于该位的设置。在发生中断时应停止接收或应在中断完成后不将RXDn引脚输入保持在高电平一个数据帧或更长时间的情况下开始接收时，将该位设置为1。

在简单LIN模式下将此位设置为1。在异步模式和简单LIN模式以外的模式下，将此位设置为0。

MOD[2:0]位（通讯模式选择）

选择SCI通信模式。

Table 26.24 Relationship between communication mode selection bits (MOD[2:0]), other operation mode setting bits

Communication mode	Asynchronous								Smart Card Interface	Clock synchronous	Simple SPI				Simple IIC	Manchester		Simple LIN
CCR3.MOD[2:0]	000b								001b	010b	011b				100b	101b		110b
CCR3.MP	0				1				—	—	—				—	0	1	—
CCR3.FM	0		1		0		1		—	0	1	0		1	—	—		—
CCR3.DEN	0	1	0	1	0	1	0	1	—	—	—				—	—		—
CCR0.SSE	—								—		0	1	0	1	—	—		—

Note: — is Prohibited setting.

MP bit (Multi-Processor Mode)

Disables/enables the multi-processor communications function. The settings of the PE bit and PM bit are invalid in multi-processor mode.

FM bit (FIFO Mode select)

When the FM bit is set to 1, the TDR register / RDR register switches to FIFO configuration, and transmit FIFO (TDR register) / receive FIFO (RDR register) can be used for serial transmission / reception.

DEN bit (Driver enable)

Select RS-485 Driver control function disable or enable.

CKE[1:0] bit (Clock enable)

These bits select the clock source and SCKn pin function.

In smart card interface mode, these bits control the clock output from the SCKn pin.

In GSM mode, clock output can be dynamically switched. For details, refer to section 26.7.8. Clock Output Control.

GM bit (GSM Mode)

Setting this bit to 1 allows GSM mode operation.

In GSM mode, the CSR.TEND flag set timing is put forward to 11.0 etu (elementary time unit = 1-bit transfer time) from the start and the clock output control function is appended. For details, refer to section 26.7.6. Serial Data Transmission (Except in Block Transfer Mode), section 26.7.8. Clock Output Control.

BLK bit (Block Transfer Mode)

Setting this bit to 1 allows block transfer mode operation.

For details, refer to section 26.7.3. Block Transfer Mode.

26.2.9 CCR4 : Common Control Register 4

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	AET	ATT[2:0]			AJD	AST[2:0]			—	—	—	—	—	—	ATEN	ASEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPD[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 26.24 通信模式选择位(MOD[2:0])与其他操作模式设置位之间的关系

通讯方式	Asynchronous								智能卡 Interface	时钟同步	简单的SPI				Simple IIC	Manchester		Simple LIN
CCR3.MOD[2:0]	000b								001b	010b	011b				100b	101b		110b
CCR3.MP	0				1				—	—	—				—	0	1	—
CCR3.FM	0		1		0		1		—	0	1	0		1	—	—		—
CCR3.DEN	0	1	0	1	0	1	0	1	—	—	—				—	—		—
CCR0.SSE	—								—		0	1	0	1	—	—		—

Note: —是禁止设置。

MP bit (Multi-Processor Mode)

Disables启用多处理器通信功能。PE位和PM位的设置在多处理器模式下无效。

FM位（FIFO模式选择）

当FM位设置为1时，TDR寄存器RDR寄存器切换为FIFO配置，发送FIFO（TDR寄存器）接收FIFO（RDR寄存器）可用于串行发送接收。

DEN位（驱动器使能）

选择禁用或启用RS-485驱动器控制功能。

CKE[1:0] bit (Clock enable)

这些位选择时钟源和SCKn引脚功能。

在智能卡接口模式下，这些位控制SCKn引脚的时钟输出。

在GSM模式下，时钟输出可以动态切换。有关详细信息，请参阅第26.7.8节。时钟输出控制。

GM bit (GSM Mode)

将此位设置为1允许GSM模式操作。

在GSM模式下，CSR.TEND标志置位时序从一开始就提出了11.0etu（基本时间单位=1位传输时间），并附加了时钟输出控制功能。详情请参阅26.7.6节。串行数据传输（块传输模式除外），第26.7.8节。时钟输出控制。

BLK位（块传输模式）

将此位设置为1允许块传输模式操作。

详情请参阅26.7.3节。块传输模式。

26.2.9 CCR4:公共控制寄存器4

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	AET	ATT[2:0]			AJD	AST[2:0]			—	—	—	—	—	—	ATEN	ASEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPD[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	CMPD[8:0]	Compare Match Data Valid only in Asynchronous mode Set the compare data pattern for address match wake-up function	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	ASEN	Adjust receive sampling timing enable Valid in Asynchronous mode using internal clock, Simple LIN mode using internal clock, Clock-synchronous mode operating as master, Simple SPI mode operating as master 0: Adjust sampling timing disable. 1: Adjust sampling timing enable.	R/W
17	ATEN	Adjust transmit timing enable Valid only in Asynchronous mode using internal clock 0: Adjust transmit timing disable. 1: Adjust transmit timing enable.	R/W
23:18	—	These bits are read as 0. The write value should be 0.	R/W
26:24	AST[2:0]	Adjustment value for receive Sampling Timing This bit enables only when ASEN is 1. in Asynchronous mode and Simple LIN mode using internal clock The sampling timing of RXDn terminal is adjusted from the middle of bit by the following formula. Adjustment sampling timing = base clock * the setting value of AST[2:0]. In Clock-synchronous mode and Simple SPI mode using internal clock The RXDn sampling timing can be adjusted by delaying 1 to 4 TCLK 0 0 0: 1TCLK delay 0 0 1: 2TCLK delay 0 1 0: 3TCLK delay 0 1 1: 4TCLK delay Others: Setting prohibited	R/W
27	AJD	Adjustment Direction for receive sampling timing Valid in Asynchronous mode using internal clock, Simple LIN mode using internal clock This bit enables only when ASEN is 1. Adjustment direction for RXDn receive sampling timing is determined by this bit. Refer to section 26.3.10. The function of adjust receive sampling timing (Asynchronous Mode) in details. 0: The sampling timing is adjusted backward to the middle of bit. 1: The sampling timing is adjusted forward to the middle of bit.	R/W
30:28	ATT[2:0]	Adjustment value for Transmit timing Valid in Asynchronous mode using internal clock, Simple LIN mode using internal clock This bit enables only when ATEN is 1. The selected edge timing of TXDn is adjusted by the following formula. Adjustment edge timing = base clock * the setting value of ATT[2:0] This setting timing is limited by setting the base clock cycles. Refer to section 26.3.11. The function of adjust transmit timing (Asynchronous Mode) in details.	R/W
31	AET	Adjustment edge for transmit timing Valid in Asynchronous mode using internal clock, Simple LIN mode using internal clock The adjustable edge is set by this bit. This bit enables only when ATEN is 1. Refer to section 26.3.11. The function of adjust transmit timing (Asynchronous Mode) in details. 0: When CCR1.TINV is 0, adjust the rising edge timing. When CCR1.TINV is 1, adjust the falling edge timing. 1: When CCR1.TINV is 0, adjust the falling edge timing. When CCR1.TINV is 1, adjust the rising edge timing.	R/W

CMPD[8:0] bit (Compare Match Data)

Set the comparison data for receive data when Address match function is enabled (CCR0.DCME = 1). CCR4.CMPD[8:0] should be written while CCR0.DCME is 0.

For the comparison data, it can select length from 3 types, they are CMPD[6:0] with 7bit length enable, CMPD[7:0] with 8bit, and CMPD[8:0] with 9bit length.

Bit	Symbol	Function	R/W
8:0	CMPD[8:0]	比较匹配数据 仅在异步模式下有效 设置地址匹配唤醒功能的比较数据模式	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
16	ASEN	调整接收采样时序使能 在使用内部时钟的异步模式、使用内部时钟的简单LIN模式下有效， 时钟同步模式作为主机运行，简单SPI模式作为主机运行 0：调整采样时序禁用。1：调整采样时序使能。	R/W
17	ATEN	调整发送时序使能 仅在使用内部时钟的异步模式下有效 0：调整发送时序禁用。1：调整发送时序使能。	R/W
23:18	—	这些位被读取为0。写入值应为0。	R/W
26:24	AST[2:0]	接收采样时序的调整值 该位仅在ASEN为1时使能。在使用内部时钟的异步模式和简单LIN模式下RXDn端子的采样时序通过以下公式从位中间调整。调整采样时序=基准时钟*AST[2:0]的设置值。在时钟同步模式和使用内部时钟的简单SPI模式下 可以通过延迟1到4个TCLK来调整RXDn采样时序 0 0 0: 1TCLK delay 0 0 1: 2TCLK delay 0 1 0: 3TCLK delay 0 1 1: 4TCLK delay 其他：禁止设置	R/W
27	AJD	接收采样时序调整方向 在使用内部时钟的异步模式、使用内部时钟的简单LIN模式下有效 该位仅在ASEN为1时使能。 RXDn接收采样时序的调整方向由该位决定。请参阅第26.3.10节。详细调整接收采样时间（异步模式）的功能。 0：采样定时向后调整到位中间。1：采样定时向前调整到位中间。	R/W
30:28	ATT[2:0]	发送时序的调整值在使用内部时钟的异步模式、使用内部时钟的简单LIN模式下有效 该位仅在ATEN为1时启用。 TXDn的选定边沿时序通过以下公式进行调整。 调整边沿时序=基准时钟*ATT[2:0]的设置值此设置时序受基准时钟周期设置的限制。请参阅第26.3.11节。详细调整发送时间（异步模式）的功能。	R/W
31	AET	发送定时的调整边沿 在使用内部时钟的异步模式下有效，在使用内部时钟的简单LIN模式下有效可调边沿由该位设置。该位仅在ATEN为1时启用。请参阅第26.3.11节。详细调整发送时间（异步模式）的功能。 0：当CCR1.TINV为0时，调整上升沿时序。当CCR1.TINV为1时，调整下降沿时序。 1：当CCR1.TINV为0时，调整下降沿时序。当CCR1.TINV为1时，调整上升沿时序。	R/W

CMPD[8:0]位（比较匹配数据）

当地址匹配功能启用时（CCR0.DCME=1）设置接收数据的比较数据。当CCR0.DCME为0时，应写入CCR4.CMPD[8:0]。

对于比较数据，它可以从3种长度中选择，它们是7bit长度使能的CMPD[6:0]、8bit的CMPD[7:0]和9bit长度的CMPD[8:0]。

Note: If the description in this document and the timing chart do not specify the ASEN / ATEN setting value, it means that the reception sampling adjustment function / transmission timing adjustment function are OFF (CCR4.ASEN = 0, CCR4.ATEN = 0).

ASEN bit (Adjust receive sampling timing enable)

When this bit is 1, the receive sampling timing adjustment function is enabled. Control is different in Asynchronous mode, Simple LIN mode, Clock-synchronous mode, and Simple SPI mode.

In Asynchronous mode using internal clock, refer to section 26.6.7. Reception Sampling Timing Adjustment Function in Clock Synchronous Mode with internal clock used in details. The operation when the Simple LIN mode internal clock is selected is the same as when the Asynchronous mode internal clock is selected.

In Clock-synchronous mode as master, Simple SPI mode operating as master, refer to section 26.6.6. Simultaneous Serial Data Transmission and Reception in Clock Synchronous Mode in details. Only the digital delay of the master mode receive sampling clock (MRCLK) can be controlled by this bit. MRCLK analog delay cannot be controlled.

ATEN bit (Adjust transmit timing enable)

When this bit is 1, the transmission timing adjustment function is enabled. The transmission timing adjustment function can adjust the edge timing of the waveform output from the TXDn pin. Refer to section 26.3.11. The function of adjust transmit timing (Asynchronous Mode) in details.

AST[2:0] bit (Adjustment value for receive Sampling Timing)

When the ASEN bit is 1, the receive sampling timing can be adjusted according to this bit setting value.

In Asynchronous mode and Simple LIN mode using internal clock.

The sampling timing of RXDn terminal is adjusted from the middle of bit by the following formula. This setting value is limited by setting the base clock cycles. Refer to section 26.3.10. The function of adjust receive sampling timing (Asynchronous Mode) in details.

Adjustment sampling timing = base clock * the setting value of AST[2:0].

In Clock-synchronous mode and Simple SPI mode using internal clock

The sampling timing of RXDn terminal can be adjusted by delaying 1 to 4 TCLK. Refer to section 26.6.7. Reception Sampling Timing Adjustment Function in Clock Synchronous Mode with internal clock used in details.

000: 1TCLK delay

001: 2TCLK delay

010: 3TCLK delay

011: 4TCLK delay

1xx: Setting prohibited

AJD bit (Adjustment Direction for receive sampling timing)

Set the RXDn pin sampling timing adjustment direction from the bit center to the rear or front. Refer to section 26.3.10. The function of adjust receive sampling timing (Asynchronous Mode) for details.

ATT[2:0] bit (Adjustment value for Transmit timing)

The edge timing of the TXDn pin specified by the AET bit is adjusted by the base clock × ATT[2:0] setting value. The upper limit of the adjustment time that can be set is limited by the number of base clock cycles. Refer to section 26.3.11. The function of adjust transmit timing (Asynchronous Mode) for details.

AET bit (Adjustment edge for transmit timing)

Set the TXDn terminal edge for timing adjustment. Refer to section 26.3.11. The function of adjust transmit timing (Asynchronous Mode) for details.

Note: 如果本文档的说明和时序图中没有指定ASENATEN设置值，则表示接收采样调整功能发送时序调整功能关闭（CCR4.ASEN=0，CCR4.ATEN=0）。

ASEN位（调整接收采样时序使能）

该位为1时，使能接收采样时序调整功能。异步模式下的控制不同，
简单LIN模式、时钟同步模式和简单SPI模式。

在使用内部时钟的异步模式下，请参阅第26.6.7节。详细使用内部时钟的时钟同步模式下的接收采样定时调整功能。选择简单LIN模式内部时钟时的操作与选择异步模式内部时钟时的操作相同。

在时钟同步模式作为主机，简单SPI模式作为主机运行，请参阅第26.6.6节。同时串行
详细介绍时钟同步模式下的数据传输和接收。该位只能控制主模式接收采样时钟（MRCLK）的数字延迟。MRCLK模拟延迟无法控制。

ATEN位（调整发送时序使能）

该位为1时，使能发送时序调整功能。发送时序调整功能可以调整从TXDn引脚输出的波形的边沿时序。请参阅第26.3.11节。详细调整发送时间（异步模式）的功能。

AST[2:0]位（接收采样时序的调整值）

当ASEN位为1时，可以根据该位设置值调整接收采样时序。

在异步模式和简单LIN模式下使用内部时钟。

RXDn端的采样时序由下式从位中间开始调整。此设置值受设置基本时钟周期的限制。请参阅第26.3.10节。详细调整接收采样时间（异步模式）的功能。

调整采样时序=基准时钟*AST[2:0]的设置值。

在时钟同步模式和使用内部时钟的简单SPI模式下

RXDn端的采样时序可以通过延迟1到4个TCLK来调整。请参阅第26.6.7节。接待
详细使用内部时钟的时钟同步模式下的采样定时调整功能。

000: 1TCLK delay

001: 2TCLK delay

010: 3TCLK delay

011: 4TCLK delay

1xx：禁止设置

AJD位（接收采样时序的调整方向）

将RXDn引脚采样时序调整方向设置为从位中心到后或前。请参阅第26.3.10节。调整接收采样时序（异步模式）的功能详见。

ATT[2:0]位（发送时序的调整值）

AET位指定的TXDn引脚的边沿时序由基本时钟×ATT[2:0]设置值调整。可设置的调整时间上限受基准时钟周期数的限制。请参阅第26.3.11节。调整发送时间的功能（异步模式）详情。

AET位（发送时序的调整边沿）

设置TXDn终端边沿以进行时序调整。请参阅第26.3.11节。调整发送时间的功能（异步模式）详情。

26.2.10 ICR : Simple IIC Control Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	IICSCLS[1:0]		IICSDAS[1:0]		—	IICSTPREQ	IICRSTAREQ	IICSTAREQ
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	IICACKT	—	—	—	IICCSC	IICINTM	—	—	—	IICDL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	IICDL[4:0]	SDA Delay Output Select Cycles below are of the clock signal from the on-chip baud rate generator. 0x00: No output delay 0x01: 0 to 1 cycle 0x02: 1 to 2 cycles 0x03: 2 to 3 cycles 0x04: 3 to 4 cycles 0x05: 4 to 5 cycles ⋮ 0x1E: 29 to 30 cycles 0x1F: 30 to 31 cycles	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
8	IICINTM	IIC Interrupt Mode Select 0: Use ACK/NACK interrupts. 1: Use reception and transmission interrupts	R/W
9	IICCSC	Clock Synchronization 0: No synchronization with the clock signal 1: Synchronization with the clock signal	R/W
12:10	—	These bits are read as 0. The write value should be 0.	R/W
13	IICACKT	ACK Transmission Data 0: ACK transmission 1: NACK transmission and reception of ACK/NACK	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W
16	IICSTAREQ	Start Condition Generation 0: A start condition is not generated 1: A start condition is generated. *1 *3 *4 *5	R/W
17	IICRSTAREQ	Restart Condition Generation 0: A restart condition is not generated. 1: A restart condition is generated. *2 *3 *4 *5	R/W
18	IICSTPREQ	Stop Condition Generation 0: A stop condition is not generated. 1: A stop condition is generated *2 *3 *4 *5	R/W
19	—	This bit is read as 0. The write value should be 0.	R/W
21:20	IICSDAS[1:0]	SDA Output Select 0 0: Serial data output 0 1: Generate a start, restart, or stop condition. 1 0: Output the low level on the SDAn pin. 1 1: Place the SDAn pin in the high-impedance state.	R/W

26.2.10 ICR:简单的IIC控制寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	IICSCLS[1:0]		IICSDAS[1:0]		—	IICSTPREQ	IICRSTAREQ	IICSTAREQ
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	IICACKT	—	—	—	IICCSC	IICINTM	—	—	—	IICDL[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	IICDL[4:0]	SDA延迟输出选择 下面的周期是来自片上波特率发生器的时钟信号。 0x00：无输出延迟0x0 1：0到1个周期0x02： 1到2个周期0x03：2到 3个周期0x04：3到4个 周期0x05：4到5个周 期 ⋮ 0x1E：29到30个周期 0x1F：30到31个周期	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
8	IICINTM	IIC中断模式选择 0：使用ACKNACK中断。1：使用接收和发送 中断	R/W
9	IICCSC	时钟同步 0：与时钟信号不同步1：与时钟信号同步	R/W
12:10	—	这些位被读取为0。写入值应为0。	R/W
13	IICACKT	ACK传输数据 0：ACK发送1：NACK发送和接收ACKNACK	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W
16	IICSTAREQ	开始条件生成 0：不产生启动条件1：产生启动条件。*1* 3*4*5	R/W
17	IICRSTAREQ	重启条件生成 0：不产生重启条件。1：产生重启条件。*2* 3*4*5	R/W
18	IICSTPREQ	停止条件生成 0：不产生停止条件。1：产生停止条件*2* 3*4*5	R/W
19	—	该位读取为0。写入值应为0。	R/W
21:20	IICSDAS[1:0]	SDA输出选择 00：串行数据输出01：产生启动、重启或停止条件。 10：SDAn引脚输出低电平。11：将SDAn引脚置于高 阻状态。	R/W

Bit	Symbol	Function	R/W
23:22	IICSCLS[1:0]	SCL Output Select 0 0: Serial clock output 0 1: Generate a start, restart, or stop condition. 1 0: Output the low level on the SCLn pin. 1 1: Place the SCLn pin in the high-impedance state.	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. In the bus free state, perform the start condition generation.
Note 2. In the bus busy state, perform restart or stop condition generation when the SCLn pin after acknowledgment described in Figure 26.84 and Figure 26.85 is low level.
Note 3. Do not set more than one from among the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits to 1 at a given time.
Note 4. Execute the generation of a condition after the value of the IICSTIF flag is 0.
Note 5. Do not write 0 to this bit while it is 1. Generation of a condition is suspended by writing 0 to this bit while it is 1.

IICDL[4:0] bit (SDA Delay Output Select)

These bits are used to set a delay for output on the SDAn pin relative to the falling edge of the output on the SCLn pin. The available delay settings range from no delay to 31 cycles, with the clock signal from the on-chip baud rate generators the base. The signal obtained by frequency-dividing TCLK by the divisor set in CCR2.CKS[1:0] is supplied as the clock signal from the on-chip baud rate generator.

Set these bits to 00000b unless operation is in simple IIC mode. In simple IIC mode, set the bits to a value in the range from 00001b to 11111b.

IICINTM bit (IIC Interrupt Mode Select)

This bit selects the sources of interrupt requests in Simple IIC mode.

IICCSC bit (Clock Synchronization)

Set the IICCSC bit to 1 if the internally generated SCLn clock signal is to be synchronized when the SCLn pin has been placed at the low level in the case of a wait inserted by the other device, etc.

The SCLn clock signal is not synchronized if the IICCSC bit is 0. The SCLn clock signal is generated in accord with the rate selected in the BRR regardless of the level being input on the SCLn pin.

Set the IICCSC bit to 1 except during debugging.

IICACKT bit (ACK Transmission Data)

Transmitted data contains ACK bits. Set this bit to 1 when ACK and NACK bits are received.

IICSTAREQ bit (Start Condition Generation)

When a start condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b as well as setting the IICSTAREQ bit to 1.

If you want to generate the start condition after generating the stop condition, start the generation of the start condition with a half cycle period of the bit rate from the stop condition generation interrupt (STI) request output.

[Setting condition]

- Writing 1 to the bit

[Clearing condition]

- Completion of generation of the start condition

IICRSTAREQ bit (Restart Condition Generation)

When a restart condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b as well as setting the IICRSTAREQ bit to 1.

[Setting condition]

- Writing 1 to the bit

[Clearing condition]

- Completion of generation of the restart condition

Bit	Symbol	Function	R/W
23:22	IICSCLS[1:0]	SCL输出选择 00：串行时钟输出01：产生启动、重启或停止条件。 10：SCLn引脚输出低电平。11：将SCLn引脚置于高阻状态。	R/W
31:24	—	这些位被读取为0。写入值应为0。	R/W

注1.在总线空闲状态下，执行启动条件生成。
注2.在总线繁忙状态下，当图26.84和图26.85中描述的确认后SCLn引脚为低电平时，执行重新启动或停止条件生成。

注3.在给定时间，不要将IICSTAREQ、IICRSTAREQ和IICSTPREQ位中的一个以上设置为1。
注4.在IICSTIF标志的值为0后执行条件生成。
注5.请勿在该位为1时向其写入0。在该位为1时向该位写入0可暂停条件的产生。

IICDL[4:0]位（SDA延迟输出选择）

这些位用于设置SDAn引脚输出相对于SCLn引脚输出下降沿的延迟。可用的延迟设置范围从无延迟到31个周期，以来自片上波特率发生器的时钟信号为基准。通过在CCR2.CKS[1:0]中设置的除数对TCLK进行分频获得的信号作为来自片上波特率发生器的时钟信号提供。

除非在简单IIC模式下操作，否则将这些位设置为00000b。在简单IIC模式下，将位设置为00001b到11111b范围内的值。

IICINTM位（IIC中断模式选择）

该位选择SimpleIIC模式下的中断请求源。

IICCSC bit (Clock Synchronization)

如果在其他设备插入等待等情况下SCLn引脚已置于低电平时内部生成的SCLn时钟信号要同步，则将IICCSC位设置为1。

如果IICCSC位为0，则SCLn时钟信号不同步。无论SCLn引脚上输入的电平如何，SCLn时钟信号都按照在BRR中选择的速率生成。

除调试期间外，将IICCSC位设置为1。

IICACKT位（ACK传输数据）

传输的数据包含ACK位。当收到ACK和NACK位时，将该位设置为1。

IICSTAREQ位（开始条件生成）

当要产生一个开始条件时，将IICSDAS[1:0]和IICSCLS[1:0]位都设置为01b并设置IICSTAREQ位为1。

如果要在生成停止条件后生成开始条件，请从停止条件生成中断(STI)请求输出开始以比特率的半个周期周期开始生成开始条件。

[设定条件]

●向位写入1

[结算条件]

●开始条件的生成完成

IICRSTAREQ位（重启条件生成）

当要产生重启条件时，将IICSDAS[1:0]和IICSCLS[1:0]位都设置为01b以及将IICRSTAREQ位为1。

[设定条件]

●向位写入1

[结算条件]

●重启条件生成完成

IICSTPREQ bit (Stop Condition Generation)

When a stop condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b as well as setting the IICSTPREQ bit to 1.

[Setting condition]

- Writing 1 to the bit

[Clearing condition]

- Completion of generation of the stop condition

IICSDAS[1:0] bit (SDA Output Select)

These bits control output from the SDAn pin.

IICSCLS[1:0] bit (SCL Output Select)

These bits control output from the SCLn pin.

26.2.11 FCR : FIFO Control Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x24

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	RSTRG[4:0]					RFRST	—	—	RTRG[4:0]				
Value after reset:	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TFRST	—	—	TTRG[4:0]					—	—	—	—	—	—	—	DRES
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DRES	Receive data ready error select bit Valid in Asynchronous mode This bit select the interrupt request for a reception data ready detection. 0: reception data full interrupt (SCIn_RXI) 1: receive error interrupt (SCIn_ERI)	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
12:8	TTRG[4:0]	Transmit FIFO data trigger number Valid in Asynchronous mode (including multi processor mode), Clock-synchronous mode, Simple SPI mode Trigger number must be set to 15 or less number. 0x00: Trigger number 0 ⋮ 0x1F: Trigger number 31	R/W
14:13	—	These bits are read as 0. The write value should be 0.	R/W
15	TFRST	Transmit FIFO Data Register Reset This bit enables only when CCR3.FM is 1. The read value is always 0. 0: It is invalid. It does not affect the operation. 1: The number of data stored in Transmit-FIFO (TDR register) are made 0	W
20:16	RTRG[4:0]	Receive FIFO data trigger number Valid in Asynchronous mode (including multi processor mode), Clock-synchronous mode, Simple SPI mode Trigger number must be set to 15 or less number. 0x00: Trigger number 0 ⋮ 0x1F: Trigger number 31	R/W

IICSTPREQ位（停止条件生成）

当要产生停止条件时，将IICSDAS[1:0]和IICSCLS[1:0]位都设置为01b，并将IICSTPREQ位为1。

[设定条件]

●向位写入1

[结算条件]

●停止条件生成完成

IICSDAS[1:0]位（SDA输出选择）

这些位控制SDAn引脚的输出。

IICSCLS[1:0]位（SCL输出选择）

这些位控制SCLn引脚的输出。

26.2.11 FCR：先进先出控制寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x24

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	RSTRG[4:0]					RFRST	—	—	RTRG[4:0]				
重置后的值:	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TFRST	—	—	TTRG[4:0]					—	—	—	—	—	—	—	DRES
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DRES	接收数据就绪错误选择位 在异步模式下有效 该位选择接收数据就绪检测的中断请求。 0：接收数据满中断（SCIn_RXI）1：接收错误中断（SCIn_ERI）	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
12:8	TTRG[4:0]	发送FIFO数据触发数 在异步模式（包括多处理器模式）、时钟同步模式、简单SPI模式 触发器编号必须设置为15或更少的数字。 0x00：触发数0 ⋮ 0x1F：触发器编号31	R/W
14:13	—	这些位被读取为0。写入值应为0。	R/W
15	TFRST	发送FIFO数据寄存器复位 该位仅在CCR3.FM为1时启用。 读取值始终为0。 0：无效。它不影响操作。1：将Transmit-FIFO（TDR寄存器）中存储的数据数设为0	W
20:16	RTRG[4:0]	接收FIFO数据触发数 在异步模式（包括多处理器模式）、时钟同步模式、简单SPI模式 触发器编号必须设置为15或更少的数字。 0x00：触发数0 ⋮ 0x1F：触发器编号31	R/W

Bit	Symbol	Function	R/W
22:21	—	These bits are read as 0. The write value should be 0.	R/W
23	RFRST	Receive FIFO Data Register Reset This bit enables only when CCR3.FM is 1. The read value is always 0. 0: It is invalid. It does not affect the operation. 1: The number of data stored in Receive-FIFO(RDR register) are made 0	W
28:24	RSTRG[4:0]	RTS Output Active Trigger Number Select Valid in Asynchronous mode (including multi processor mode), Clock-synchronous mode This bit enables only when CCR3.FM = 1 and CCR1.CTSE = 0 and CCR0.SSE = 0. Trigger number must be set to 15 or less number. 0x00: Trigger number 0 ⋮ 0x1F: Trigger number 31	R/W
31:29	—	These bits are read as 0. The write value should be 0.	R/W

DRES bit (Receive data ready error select bit)

Select whether the detection of receive data ready (FRSR.DR flag = 1) is the cause of SCIn_RXI interrupt request or the cause of SCIn_ERI interrupt request.

TTRG[4:0] bit (Transmit FIFO data trigger number)

The TDFE flag is set to 1 when the quantity of transmit data in the transmit-FIFO(TDR register) is equal to or less than the specified transmit triggering number. If SCR.TIE = 1, SCIn_TXI interrupt request is occurred.

Note: Trigger number have to be set 15. In case the trigger number is set 16 or more, unexpected SCIn_TXI interrupt will occur.

TFRST bit (Transmit FIFO Data Register Reset)

When the TFRST bit is set to 1, the number of the transmission data stored in Transmit-FIFO(TDR register) is made 0.

RTRG[4:0] bit (Receive FIFO data trigger number)

The CSR.RDRF flag is set to 1 when the quantity of receive data in the receive-FIFO(RDR register) is equal to or greater than the specified receive triggering number. If CCR0.RIE = 1, SCIn_RXI interrupt request is occurred. When FCR.RTRG is set to 0, RDRF bit is set if the quantity of data in receive-FIFO is greater than or equal to 1.

Note: Trigger number have to be set to 15. In case the trigger number is set to 16 or more, unexpected SCIn_RXI interrupt will occur.

RFRST bit (Receive FIFO Data Register Reset)

When the RFRST bit is set to 1, the number of the reception data stored in Receive-FIFO(RDR register) is made 0.

RSTRG[4:0] bit (RTS Output Active Trigger Number Select)

When the quantity of receive data stored in the receive-FIFO (RDR register) is equal to or greater than this number, the RTSn signal is in the High state. When FCR.RSTRG is set to 0, RTSn is in the high state if the quantity of data in reveive FIFO is greater than or equal to 1.

Note: Trigger number have to be set 15. In case the trigger number is set 16 or more, RTSn will go to High state at unexpected timing.

Bit	Symbol	Function	R/W
22:21	—	这些位被读取为0。写入值应为0。	R/W
23	RFRST	接收FIFO数据寄存器复位 该位仅在CCR3.FM为1时启用。 读取值始终为0。 0：无效。它不影响操作。1：Receive-FIFO(RDRregister)中存储的数据个数为0	W
28:24	RSTRG[4:0]	RTS输出有源触发数选择 在异步模式（包括多处理器模式）、时钟同步模式下有效 该位仅在CCR3.FM=1且CCR1.CTSE=0且CCR0.SSE=0时启用。 触发器编号必须设置为15或更少的数字。 0x00：触发数0 ⋮ 0x1F：触发器编号31	R/W
31:29	—	这些位被读取为0。写入值应为0。	R/W

DRES位（接收数据就绪错误选择位）

选择检测到接收数据就绪（FRSR.DR标志=1）是SCIn_RXI中断请求的原因还是SCIn_ERI中断请求的原因。

TTRG[4:0]位（发送FIFO数据触发数）

当发送FIFO（TDR寄存器）中的发送数据量等于或小于指定的发送触发数时，TDFE标志设置为1。如果SCR.TIE=1，则发生SCIn_TXI中断请求。

Note: 触发数必须设置为15。如果触发数设置为16或更多，则会发生意外的SCIn_TXI中断。

TFRST位（发送FIFO数据寄存器复位）

当TFRST位设置为1时，存储在Transmit-FIFO（TDR寄存器）中的传输数据数量为0。

RTRG[4:0]位（接收FIFO数据触发数）

当接收FIFO（RDR寄存器）中的接收数据量等于或大于指定的接收触发数时，CSR.RDRF标志设置为1。如果CCR0.RIE=1，则产生SCIn_RXI中断请求。当FCR.RTRG设置为0时，如果接收FIFO中的数据量大于或等于1，则设置RDRF位。

Note: 触发数必须设置为15。如果触发数设置为16或更多，则会发生意外的SCIn_RXI中断。

RFRST位（接收FIFO数据寄存器复位）

当RFRST位设置为1时，存储在Receive-FIFO（RDR寄存器）中的接收数据数量为0。

RSTRG[4:0]位（RTS输出有效触发数选择）

当存储在接收FIFO（RDR寄存器）中的接收数据数量等于或大于该数量时，
RTSn信号处于高电平状态。当FCR.RSTRG设置为0时，如果接收到的数据量大，则RTSn处于高电平状态
FIFO大于或等于1。

Note: 触发数必须设置为15。如果触发数设置为16或更多，RTSn将在意外时间进入高状态。

26.2.12 MCR : Manchester Control Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	SBERE N	SYERE N	PFERE N	—	—	RPPAT[1:0]		RPLEN[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TPPAT[1:0]		TPLEN[3:0]				—	SBSEL	SYNSEL	SYNVAL	—	ERTEN	TMPOL	RMPOL
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RMPOL	Polarity of Received Manchester Code Sets the polarity of the received Manchester code 0: Logic 0 is coded as a zero-to-one transition in Manchester code Logic 1 is coded as a one-to-zero transition in Manchester code 1: Logic 0 is coded as a one-to-zero transition in Manchester code Logic 1 is coded as a zero-to-one transition in Manchester code	R/W
1	TMPOL	Polarity of Transmit Manchester Code Sets the polarity of the transmit Manchester code 0: Logic 0 is coded as a zero-to-one transition in Manchester code Logic 1 is coded as a one-to-zero transition in Manchester code 1: Logic 0 is coded as a one-to-zero transition in Manchester code Logic 1 is coded as a zero-to-one transition in Manchester code	R/W
2	ERTEN	Manchester Edge Retiming Enable Sets the receive retiming function 0: Disables the receive retiming function 1: Enables the receive retiming function	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	SYNVAL	SYNC value Setting Sets the SYNC type of the start bit(s) in the Manchester code When the start bit area consists of one bit. (SBSEL = 0) • when transmitting 0: The start bit is added as a zero-to-one transition. 1: The start bit is added as a one-to-zero transition. • when receiving 0: Only when the start bit is a zero-to-one transition, the data is received. The other cases are judged as an error. 1: Only when the start bit is a one-to-zero transition, the data is received. The other cases are judged as an error. When the start bit area consists of three bits. (SBSEL = 1) • when transmitting 0: The start bits are added as a zero-to-one transition. (DATA SYNC) 1: The start bits are coded as a one-to-zero transition. (COMMAND SYNC) • when receiving When the start bit area consists of three bits, data is received regardless of the value of this bit.	R/W
5	SYNSEL	SYNC Select 0: The start bit pattern is set with the SYNVAL bit 1: The start bit pattern is set with the TSYNC bit.	R/W
6	SBSEL	Start Bit Select 0: The start bit area consists of one bit. 1: The start bit area consists of three bits (COMMAND SYNC or DATA SYNC)	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

26.2.12 MCR:曼彻斯特控制寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	SBERE N	SYERE N	PFERE N	—	—	RPPAT[1:0]		RPLEN[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TPPAT[1:0]		TPLEN[3:0]				—	SBSEL	SYNSEL	SYNVAL	—	ERTEN	TMPOL	RMPOL
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RMPOL	接收到的曼彻斯特码的极性 设置接收到的曼彻斯特码的极性 0：逻辑0编码为曼彻斯特码中的零到一转换逻辑1编码为曼彻斯特码中的一到零转换 1：逻辑0被编码为曼彻斯特码中的1到零转换逻辑1被编码为曼彻斯特码中的0到1转换	R/W
1	TMPOL	发送曼彻斯特码的极性 设置发送曼彻斯特码的极性 0：逻辑0编码为曼彻斯特码中的零到一转换逻辑1编码为曼彻斯特码中的一到零转换 1：逻辑0被编码为曼彻斯特码中的1到零转换逻辑1被编码为曼彻斯特码中的0到1转换	R/W
2	ERTEN	曼彻斯特边缘重定时启用 设置接收重定时功能 0：关闭接收重定时功能1：打开接收重定时功能	R/W
3	—	该位读取为0。写入值应为0。	R/W
4	SYNVAL	SYNC值设置 设置曼彻斯特代码中起始位的SYNC类型 当起始位区域由一位组成时。(SBSEL=0) • 传输时 0：添加起始位作为从零到一的转换。1：添加起始位作为1到零的转换。 • 接收时 0：仅当起始位为0到1转换时，才接收数据。其他情况判断为错误。 1：仅当起始位为1到零跳变时，才接收数据。其他情况判断为错误。 当起始位区域由三位组成时。(SBSEL=1) • 传输时 0：添加起始位作为零到一的转换。(DATASYNC)1：起始位被编码为一个从一到零的转换。（命令同步） ●接收时当起始位区域由三位组成时，无论该位的值如何，都将接收数据。	R/W
5	SYNSEL	同步选择 0：使用SYNVAL位设置起始位模式1：使用TSYNC位设置起始位模式。	R/W
6	SBSEL	起始位选择 0：起始位区域由一位组成。1：起始位区域由三位组成（COMMANDSYNC或DATA SYNC）	R/W
7	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
11:8	TPLEN[3:0]	Transmit preface length Set the preface length of the transmit data in Manchester mode 0x0: Disables the transmit preface generation Others: Transmit preface length (bit length)	R/W
13:12	TPPAT[1:0]	Transmit preface pattern Set the preface pattern of the transmit data 0 0: ALL ZERO 0 1: ZERO ONE 1 0: ONE ZERO 1 1: ALL ONE	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W
19:16	RPLEN[3:0]	Receive Preface Length Set the preface length in received frames when Manchester mode is enabled 0x0: Disables the receive preface generation Others: Receive preface length (bit length)	R/W
21:20	RPPAT[1:0]	Receive Preface Pattern Set the preface pattern of received frames 0 0: ALL ZERO 0 1: ZERO ONE 1 0: ONE ZERO 1 1: ALL ONE	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W
24	PFEREN	Preface Error Enable Specifies whether to handle a preface error as an interrupt source 0: Does not handle a preface error as an interrupt source 1: Handles a preface error as an interrupt source	R/W
25	SYEREN	Receive SYNC Error Enable Specifies whether to handle a receive SYNC error as an interrupt source 0: Does not handle a receive SYNC error as an interrupt source 1: Handles a receive SYNC error as an interrupt source	R/W
26	SBEREN	Start Bit Error Enable Specifies whether to handle a start bit error as an interrupt source 0: Does not handle a start bit error as an interrupt source 1: Handles a start bit error as an interrupt source	R/W
31:27	—	These bits are read as 0. The write value should be 0.	R/W

RMPOL bit (Polarity of Received Manchester Code)

This bit sets the polarity of the received Manchester code. For details, see section 26.5.7. Serial Data Reception in Manchester Mode.

TMPOL bit (Polarity of Transmit Manchester Code)

This bit sets the polarity of the transmit Manchester code. For details, see section 26.5.6. Serial data transmission in Manchester mode.

ERTEN bit (Manchester Edge Retiming Enable)

This bit sets the receive retiming function in Manchester mode.

For information on the receive retiming function, see section 26.5.9. Receive Retiming.

SYNVAL bit (SYNC value Setting)

This bit is valid when the SYNSEL bit of this register is set to 0.

The SYNC type can be set by combining this bit and the SBSEL bit.

For the start bit area determined by the combination of this bit and the SBSEL bit, see Figure 26.52 and Figure 26.53.

SYNSEL bit (SYNC Select)

This bit is valid when the SBSEL bit of this register is set to 1. This bit determines the destination to be referred to for setting the SYNC type of the start bit area added to Manchester frames.

Bit	Symbol	Function	R/W
11:8	TPLEN[3:0]	传输前言长度 设置曼彻斯特模式下发送数据的前言长度 0x0：禁用发送前言生成 其他：传输前言长度（位长）	R/W
13:12	TPPAT[1:0]	传输前言模式 设置发送数据的前言模式 00：全零01：零 一10：一个零11 ：全一	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W
19:16	RPLEN[3:0]	接收序言长度 启用曼彻斯特模式时设置接收帧中的前言长度 0x0：禁用接收前言生成 其他：接收前言长度（位长）	R/W
21:20	RPPAT[1:0]	接收前言模式 设置接收帧的前言模式 00：全零01：零 一10：一个零11 ：全一	R/W
23:22	—	这些位被读取为0。写入值应为0。	R/W
24	PFEREN	前言错误启用 指定是否将序言错误作为中断源处理 0：不将序言错误作为中断源处理1：将序言错误作为中断源处理	R/W
25	SYEREN	接收同步错误启用 指定是否将接收SYNC错误作为中断源处理 0：不将接收同步错误作为中断源处理1：将接收同步错误作为中断源处理	R/W
26	SBEREN	启动位错误启用 指定是否将起始位错误作为中断源处理 0：不将起始位错误作为中断源处理1：将起始位错误作为中断源处理	R/W
31:27	—	这些位被读取为0。写入值应为0。	R/W

RMPOL位（接收曼彻斯特码的极性）

该位设置接收到的曼彻斯特码的极性。详见26.5.7节。串行数据接收曼彻斯特模式。

TMPOL位（发送曼彻斯特码的极性）

该位设置发送曼彻斯特码的极性。详见26.5.6节。串行数据传输曼彻斯特模式。

ERTEN位（曼彻斯特边沿重定时使能）

该位设置曼彻斯特模式下的接收重定时功能。

有关接收重定时功能的信息，请参见第26.5.9节。接收重定时。

SYNVAL位（SYNC值设置）

当该寄存器的SYNSEL位设置为0时，该位有效。

SYNC类型可以通过组合该位和SBSEL位来设置。

由该位和SBSEL位组合决定的起始位区域见图26.52和图26.53。

SYNSEL bit (SYNC Select)

当该寄存器的SBSEL位设置为1时，该位有效。该位决定了设置添加到曼彻斯特帧的起始位区域的SYNC类型的目标。

When this bit is set to 0, the SYNVAL bit of this register is referred to.

When this bit is set to 1, the TSYNC bit in the TDR register is referred to.

SBSEL bit (Start Bit Select)

This bit sets the start bit area in Manchester frames.

When this bit is set to 1, the start bit area added to each frame consists of three bits, and the SYNSEL and SYNVAL bits in this register are valid.

When this bit is set to 0, the start bit area added to each frame consists of one bit.

TPLEN[3:0] bit (Transmit preface length)

These bits set the preface bit length of the transmit data in Manchester mode.

The settable range is 0x0 to 0xF (0d to 15d). 0h disables the transmit preface, which is not added.

TPPAT[1:0] bit (Transmit preface pattern)

These bits set one of the four preface patterns in Manchester mode. For the transmit data when the TPPAT[1:0] bits are set, see Figure 26.51.

When these bits are set to 00b, the preface area is set to all zeros.

When these bits are set to 01b, the preface area is set to the zero-one-zero-one pattern.

When these bits are set to 10b, the preface area is set to the one-zero-one-zero pattern.

When these bits are set to 11b, the preface area is set to all ones.

RPLEN[3:0] bit (Receive Preface Length)

These bits set the preface bit length of the received frames in Manchester mode.

The settable range is 0x0 to 0xF (0d to 15d). 0x0 disables the receive preface, which is not added. When 0x1 to 0xF is set, the set value is handled as the receive preface bit length.

RPPAT[1:0] bit (Receive Preface Pattern)

These bits set one of the four preface patterns in Manchester mode. For the transmit and receive data when the TPPAT[1:0] bits are set, see Figure 26.51.

When these bits are set to 00b, the preface area is handled as all zeros.

When these bits are set to 01b, the preface area is handled as the zero-one-zero-one pattern.

When these bits are set to 10b, the preface area is handled as the one-zero-one-zero pattern.

When these bits are set to 11b, the preface area is handled as all ones.

PFEREN bit (Preface Error Enable)

This bit specifies whether to handle a preface error as an interrupt source.

When it is set to 0, a preface error is not handled as an interrupt source. When it is set to 1, a preface error is handled as an interrupt source.

SYEREN bit (Receive SYNC Error Enable)

This bit specifies whether to handle a receive SYNC error as an interrupt source.

When it is set to 0, a receive SYNC error is not handled as an interrupt source. When it is set to 1, a receive SYNC error is handled as an interrupt source.

SBEREN bit (Start Bit Error Enable)

This bit specifies whether to handle a start bit error as an interrupt source.

When it is set to 0, a start bit error is not handled as an interrupt source. When it is set to 1, a start bit error is handled as an interrupt source.

当该位设置为0时，引用该寄存器的SYNVAL位。

当该位设置为1时，参考TDR寄存器中的TSYNC位。

SBSEL bit (Start Bit Select)

该位设置曼彻斯特帧中的起始位区域。

当该位设置为1时，添加到每帧的起始位区域由3位组成，该寄存器中的SYNSEL和SYNVAL位有效。

当该位设置为0时，添加到每一帧的起始位区域由一位组成。

TPLEN[3:0]位（发送前言长度）

这些位设置曼彻斯特模式下发送数据的前言位长度。

可设置范围为0x0到0xF（0d到15d）。0h禁用未添加的发送前言。

TPPAT[1:0]位（发送前言模式）

这些位设置曼彻斯特模式中的四个前言模式之一。对于设置TPPAT[1:0]位时的发送数据，请参见图26.51。

当这些位设置为00b时，前言区域设置为全零。

当这些位设置为01b时，前言区域设置为零一零一模式。

当这些位设置为10b时，前言区域设置为一零一零模式。

当这些位设置为11b时，前言区域设置为全1。

RPLEN[3:0]位（接收前言长度）

这些位设置曼彻斯特模式下接收帧的前言位长度。

可设置范围为0x0到0xF（0d到15d）。0x0禁用接收前言，未添加。当设置0x1到0xF时，设置值作为接收前言位长度处理。

RPPAT[1:0]位（接收前言模式）

这些位设置曼彻斯特模式中的四个前言模式之一。对于设置TPPAT[1:0]位时的发送和接收数据，请参见图26.51。

当这些位设置为00b时，前言区域被处理为全零。

当这些位设置为01b时，前言区域作为零一零一模式处理。

当这些位设置为10b时，前言区域作为一零一零模式处理。

当这些位被设置为11b时，前言区域被当作全1处理。

PFEREN位（前言错误使能）

该位指定是否将序言错误作为中断源处理。

当它设置为0时，前言错误不作为中断源处理。当它设置为1时，前言错误作为中断源处理。

SYEREN位（接收同步错误使能）

该位指定是否将接收同步错误作为中断源处理。

当它设置为0时，接收SYNC错误不作为中断源处理。当它设置为1时，接收SYNC错误作为中断源处理。

SBEREN位（启动位错误启用）

该位指定是否将起始位错误作为中断源处理。

当它设置为0时，起始位错误不作为中断源处理。当它设置为1时，起始位错误作为中断源处理。

26.2.13 DCR : Driver Control Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DENGT[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DEAST[4:0]					—	—	—	—	—	—	—	DEPOL
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DEPOL	Driver effective polarity select Valid only in Asynchronous mode 0: The DEn signal is active high. 1: The DEn signal is active low.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
12:8	DEAST[4:0]	Driver Assertion Time Valid only in Asynchronous mode Set the driver assertion time. When DEN = 1, the driver assertion time is inserted in addition to the normal transmission waiting time. Setting DEAST[4:0] = 5'H00 is prohibited.	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W
20:16	DENGT[4:0]	Driver negate time Valid only in Asynchronous mode Set the driver negation time. When DEN = 1, the driver negate time is inserted after STOP bit transmission end. Setting DENGT[4:0] = 5'H00 is prohibited.	R/W
31:21	—	These bits are read as 0. The write value should be 0.	R/W

DEPOL bit (Driver effective polarity select)

Select the active level of the DEn signal.

DEAST[4:0] bit (Driver Assertion Time)

Set the driver assertion time (= time from the activation of the DEn (Driver Enable) signal to the start of the start bit). It is expressed in base clock period.

Driver assertion time

= DEAST [4:0] set value × base clock period + transmission waiting time

DENGT[4:0] bit (Driver negate time)

Set the driver negation time (= time from the end of the last stop bit of the transmitted message until the DEn (Driver Enable) signal is disabled). It is expressed in base clock period.

Driver negate time

= DENGT[4:0] set value × base clock period

If the transmission data is written during the driver negate time, transmit starting operation is different depends on the writing timing. (The DEn signal remains valid, and transmission of the start bit may start after the transmission wait time has elapsed. Also, the DEn signal may become invalid once, and start bit transmission may start after the Driver assertion time has elapsed.)

26.2.13 DCR:驱动控制寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DENGT[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DEAST[4:0]					—	—	—	—	—	—	—	DEPOL
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DEPOL	驱动器有效极性选择 仅在异步模式下有效 0：DEn信号高电平有效。1：DEn信号低电平有效。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
12:8	DEAST[4:0]	驱动程序断言时间 仅在异步模式下有效 设置驱动程序断言时间。当DEN=1时，除了正常的传输等待时间外，还会插入驱动程序断言时间。禁止设置DEAST[4:0]=5'H00。	R/W
15:13	—	这些位被读取为0。写入值应为0。	R/W
20:16	DENGT[4:0]	司机否定时间 仅在异步模式下有效 设置驱动器否定时间。当DEN=1时，在STOP位发送结束后插入驱动器取反时间。禁止设置DENGT[4:0]=5'H00。	R/W
31:21	—	这些位被读取为0。写入值应为0。	R/W

DEPOL位（驱动器有效极性选择）

选择DEn信号的有效电平。

DEAST[4:0]位（驱动器断言时间）

设置驱动器断言时间（=从激活DEn（驱动器使能）信号到开始位开始的时间）。它以基本时钟周期表示。

驱动断言时间

=DEAST[4:0]设定值×基本时钟周期+传输等待时间

DENGT[4:0]位（驱动器取反时间）

设置驱动程序否定时间（=从发送消息的最后一个停止位结束到DEn（驱动程序启用）信号被禁用）。它以基本时钟周期表示。

司机否定时间

=DENGT[4:0]设定值×基本时钟周期

如果在驱动器取反期间写入传输数据，则传输开始操作会因写入时序而异。（DEn信号保持有效，在传输等待时间过去后可能会开始传输起始位。此外，DEn信号可能会变为无效一次，并且可能会在驱动器断言时间过去后开始传输开始位。）

26.2.14 XCR0 : Simple LIN Control Register 0

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	BCCS[1:0]		—	AEDIE	COFIE	BFDIE	—	—	BCDIE	BFOIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PIBS[2:0]			PIBE	CF1DS[1:0]		CF0RE	BFE	—	—	—	—	—	—	TCSS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	TCSS[1:0]	Timer count clock source selection (Valid in Simple LIN mode) Select the clock source of the timer in the LIN module. 0 1: TCLK/4 1 0: TCLK/16 1 1: TCLK/64	R/W*1
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	BFE	Break Field enable Set the presence or absence of Break Field of Start Frame. 0: No Break Field 1: With Break Field	R/W*3
9	CF0RE	Control Field 0 enable Set the presence or absence of Control Field 0 of Start Frame 0: No Control Field 0 1: With Control Field 0	R/W*3
11:10	CF1DS[1:0]	Control Field1 compare data select Select the compare data for Control Field 1 0 0: Select XCR1.PCF1D[7:0] as the compare data 0 1: Select XCR1.SCF1D[7:0] as the compare data 1 0: Select both XCR1.PCF1D[7:0] and XCR1.SCF1D[7:0] as the compare data 1 1: Setting prohibited	R/W*3
12	PIBE	Priority interrupt bit enable 0: Priority interrupt bit disable 1: Priority interrupt bit enable	R/W*3
15:13	PIBS[2:0]	Priority interrupt bit select Specify one of bits 0 to 7 of Control Field 1 as the priority interrupt bit. 0 0 0: bit 0 of Control Field 1 0 0 1: bit 1 of Control Field 1 0 1 0: bit 2 of Control Field 1 0 1 1: bit 3 of Control Field 1 1 0 0: bit 4 of Control Field 1 1 0 1: bit 5 of Control Field 1 1 1 0: bit 6 of Control Field 1 1 1 1: bit 7 of Control Field 1	R/W*3
16	BFOIE	Break Field output completion interrupt enable Select whether to include Break Field output completion as a SCIn_TXI interrupt factor. 0: Break Field output completion is not included in SCIn_TXI interrupt factor 1: Break Field output completion is included in SCIn_TXI interrupt factor	R/W
17	BCDIE	Bus conflict detection interrupt enable Select whether to output an SCIn_ERI interrupt when a bus collision is detected. 0: Bus conflict detection is not included in SCIn_ERI interrupt factor 1: Bus conflict detection is included in SCIn_ERI interrupt factor	R/W
19:18	—	These bits are read as 0. The write value should be 0.	R/W

26.2.14 XCR0:简单LIN控制寄存器0

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	BCCS[1:0]		—	AEDIE	COFIE	BFDIE	—	—	BCDIE	BFOIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PIBS[2:0]			PIBE	CF1DS[1:0]		CF0RE	BFE	—	—	—	—	—	—	TCSS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	TCSS[1:0]	定时器计数时钟源选择（SimpleLIN模式下有效）选择LIN模块中定时器的时钟源。 0 1: TCLK/4 1 0: TCLK/16 1 1: TCLK/64	R/W*1
7:2	—	这些位被读取为0。写入值应为0。	R/W
8	BFE	中断字段启用 设置起始帧的中断字段的存在或不存在。 0：无中断字段1： 有中断字段	R/W*3
9	CF0RE	控制字段0启用 设置StartFrame的ControlField0的有无 0：无控制字段01：有 控制字段0	R/W*3
11:10	CF1DS[1:0]	控制Field1比较数据选择 选择控制字段1的比较数据 00：选择XCR1.PCF1D[7:0]作为比较数据01：选择XCR1.SCF1D[7:0]作为比较数据 10：同时选择XCR1.PCF1D[7:0]和XCR1.SCF1D[7:0]作为比较数据11：禁止设置	R/W*3
12	PIBE	优先中断位使能 0：优先中断位禁止1：优先中 断位使能	R/W*3
15:13	PIBS[2:0]	优先中断位选择 指定控制字段1的位0到7之一作为优先中断位。 000：控制字段1的第0位001 ：控制字段1的第1位010：控 制字段1的第2位011：控制字 段1的第3位100：控制字段1 的第4位101：控制字段1的第 5位110：控制字段1的第6位 111：控制字段1的第7位	R/W*3
16	BFOIE	BreakField输出完成中断使能 选择是否将BreakField输出完成作为SCIn_TXI中断因素包括在内。 0：BreakField输出完成不包含在SCIn_TXI中断因素中1：BreakField输出完成 包含在SCIn_TXI中断因素中	R/W
17	BCDIE	总线冲突检测中断使能 选择检测到总线冲突时是否输出SCIn_ERI中断。 0：总线冲突检测不包含在SCIn_ERI中断因子中1：总线冲突检测包含 在SCIn_ERI中断因子中	R/W
19:18	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
20	BFDIE	Break Field detection interrupt enable Select whether to output a SCIn_BFD interrupt when a Break Field is detected. 0: Break Field detection interrupt disable 1: Break Field detection interrupt enable	R/W
21	COFIE	Counter overflow interrupt enable Select whether to include counter overflow as an SCIn_ERI interrupt factor. 0: Counter overflow is not included in SCIn_ERI interrupt factor 1: Counter overflow is included in SCIn_ERI interrupt factor	R/W
22	AEDIE	Active edge detection interrupt enable Select whether to output an SCIn_AED interrupt when a valid edge is detected. 0: Active edge detection interrupt disable 1: Active edge detection interrupt enable	R/W
23	—	This bit is read as 0. The write value should be 0.	R/W
25:24	BCCS[1:0]	Bus conflict detection clock selection Select the sampling clock for the bus conflict detection circuit. When CCR2.ABCS = 1, setting BCCS[1:0] = 1x is prohibited. 0 0: Base clock*2 0 1: Base clock/2 1 0: Base clock/4 1 1: Setting prohibited	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. You can rewrite TCSS[1:0] only when the timer is stopped (TCST = 0 and SDST = 0 and BMEN = 0)
Note 2. Base clock: 1/16 period of 1 bit period when CCR2.ABCS = 0, 1/8 period of 1 bit period when CCR2.ABCS = 1.
Note 3. This bit is a setting bit required for Start Frame reception operation. Rewrite this bit when Start Frame reception or transmission is not in progress (XCR1.SDST = 0 and XCR1.TCST = 0).

TCSS[1:0] bit (Timer count clock source selection)

Select clock source of timer in Simple LIN module.

BFE bit (Break Field enable)

Set the presence or absence of Break Field of Start Frame.

CF0RE bit (Control Field 0 enable)

Set the presence or absence of Control Field 0 of Start Frame.

CF1DS[1:0] bit (Control Field1 compare data select)

Select the compare data for Control Field 1.

PIBE bit (Priority interrupt bit enable)

Select whether to enable priority interrupt bit comparison of Control Field 1. When this bit is 1, regardless of the XCR1.CF1CE [7:0] setting value, the bit specified in PIBS [2:0] is compared with the primary comparison data for Control Field 1 (XCR1.PCF1D [7:0]).

PIBS[2:0] bit (Priority interrupt bit select)

Specify bit N (N = 0-7) of Control Field 1 as the priority interrupt bit.

BFOIE bit (Break Field output completion interrupt enable)

Select whether to include Break Field output completion as a SCIn_TXI interrupt factor. Set CCR0.TIE = 1 and CCR3.MOD [1: 0] = 110b, to output SCIn_TXI upon completion of Break Field output.

BCDIE bit (Bus conflict detection interrupt enable)

Select whether to output an SCIn_ERI interrupt when a bus collision is detected. In Simple LIN mode (CCR3.MOD [1:0] = 110b), SCIn_ERI output control is performed with this bit. When CCR3.MOD [1:0] = 110b and BCDIE = 1, an SCIn_ERI interrupt is issued when a bus collision is detected even if CCR0.RIE = 0.

Bit	Symbol	Function	R/W
20	BFDIE	断场检测中断使能 选择检测到BreakField时是否输出SCIn_BFD中断。 0：BreakField检测中断禁止1：BreakField检测中断使能	R/W
21	COFIE	计数器溢出中断使能 选择是否将计数器溢出作为SCIn_ERI中断因素。 0：计数器溢出不包含在SCIn_ERI中断因子中1：计数器溢出包含在SCIn_ERI中断因子中	R/W
22	AEDIE	有效边沿检测中断使能 选择检测到有效边沿时是否输出SCIn_AED中断。 0：有效边沿检测中断禁止1：有效边沿检测中断使能	R/W
23	—	该位读取为0。写入值应为0。	R/W
25:24	BCCS[1:0]	总线冲突检测时钟选择 选择总线冲突检测电路的采样时钟。当CCR2.ABCS=1时，禁止设置BCCS[1:0]=1x。 00：基本时钟*2 01：基准时钟210：基准时钟411：禁止设置	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

注1.只有在定时器停止时（TCST=0和SDST=0和BMEN=0）才能重写TCSS[1:0]
注2.基本时钟：当CCR2.ABCS=0时，1位周期的116周期，当CCR2.ABCS=1时，1位周期的18周期。
注3.该位是开始帧接收操作所需的设置位。当开始帧接收或发送不在进行中时（XCR1.SDST=0和XCR1.TCST=0）重写该位。

TCSS[1:0]位（定时器计数时钟源选择）

在SimpleLIN模块中选择定时器的时钟源。

BFE位（BreakField使能）

设置起始帧的中断字段的存在或不存在。

CF0RE位（控制字段0使能）

设置起始帧的控制字段0的存在或不存在。

CF1DS[1:0]位（控制字段1比较数据选择）

选择控制字段1的比较数据。

PIBE位（优先中断位使能）

选择是否启用控制域1的优先中断位比较。当该位为1时，无论XCR1.CF1CE[7:0]设置值，PIBS[2:0]中指定的位与Control的主要比较数据进行比较Field 1 (XCR1.PCF1D [7:0]).

PIBS[2:0]位（优先中断位选择）

将控制字段1的位N(N=0-7)指定为优先中断位。

BFOIE位（BreakField输出完成中断使能）

选择是否将BreakField输出完成作为SCIn_TXI中断因素包括在内。设置CCR0.TIE=1和CCR3.MOD[1:0]=110b，在BreakField输出完成后输出SCIn_TXI。

BCDIE位（总线冲突检测中断使能）

选择检测到总线冲突时是否输出SCIn_ERI中断。在简单LIN模式下(CCR3.MOD[1:0]=110b)，SCIn_ERI输出控制通过该位执行。当CCR3.MOD[1:0]=110b且BCDIE=1时，即使CCR0.RIE=0，当检测到总线冲突时也会发出SCIn_ERI中断。

COFIE bit (Counter overflow interrupt enable)

Select whether to include counter overflow as an SCIn_ERI interrupt factor. Set CCR0.RIE = 1 and CCR3.MOD [1:0] = 110b are required to output SCIn_ERI upon counter overflow.

AEDIE bit (Active edge detection interrupt enable)

Select whether to output an SCIn_AED interrupt when a valid edge is detected. To output SCIn_AED with valid edge detection, XCR1.BMEN = 1 and CCR3.MOD [1:0] = 110b must be set.

BCCS[1:0] bit (Bus conflict detection clock selection)

Select the sampling clock for the bus conflict detection circuit.

26.2.15 XCR1 : Simple LIN Control Register 1

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CF1CE[7:0]								SCF1D[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PCF1D[7:0]								—	—	BMEN	SDST	—	—	—	TCST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCST	Break Field output timer count start trigger 0: Break Field output timer count stopped 1: Break Field output timer count start	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	SDST	Start Frame detection enable 0: Start Frame/Break Field detection disabled 1: Start Frame/Break Field detection enabled Do not set this bit and TCST bit to 1 at the same time.	R/W
5	BMEN	Bit rate measurement enable Set this bit to 1 simultaneously with the SDST bit. When this bit is set to 0, it can be set to 0 at any timing. 0: Bit rate measurement disabled 1: Bit rate measurement enabled	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
15:8	PCF1D[7:0]	Priority compare data for Control Field 1 The priority compare data for Control Field 1	R/W
23:16	SCF1D[7:0]	Secondary compare data for Control Field 1 The secondary compare data for Control Field 1	R/W
31:24	CF1CE[7:0]	Control Field 1 compare bit enable Select whether to compare bit N of Control Field 1. (N = 0 -7) 0: Control Field 1 bit N compare disabled 1: Control Field 1 bit N compare enabled	R/W

TCST bit (Break Field output timer count start trigger)

[Clearing condition]

- When 0 is written to TCST. Break Field output timer count is stopped and TXDn output becomes idle level.
- When Break Field output for the period set in XCR2.BFLW [15: 0] is completed.

[Setting condition]

COFIE位（计数器溢出中断使能）

选择是否将计数器溢出作为SCIn_ERI中断因素。设置CCR0.RIE=1和CCR3.MOD[1:0]=110b需要在计数器溢出时输出SCIn_ERI。

AEDIE位（有效边沿检测中断使能）

选择检测到有效边沿时是否输出SCIn_AED中断。要输出带有有效边沿检测的SCIn_AED，必须设置XCR1.BMEN=1和CCR3.MOD[1:0]=110b。

BCCS[1:0]位（总线冲突检测时钟选择）

选择总线冲突检测电路的采样时钟。

26.2.15 XCR1：简单LIN控制寄存器1

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CF1CE[7:0]								SCF1D[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PCF1D[7:0]								—	—	BMEN	SDST	—	—	—	TCST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCST	BreakField输出定时器计数开始触发 0：BreakField输出定时器计数停止1：BreakField输出定时器计数开始	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
4	SDST	启动帧检测使能 0：禁止开始帧中断字段检测1：使能开始帧中断字段检测 不要将此位和TCST位同时设置为1。	R/W
5	BMEN	比特率测量启用 将此位与SDST位同时设置为1。当该位设置为0时，可以在任何时间设置为0。 0：禁用比特率测量1：启用比特率测量	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
15:8	PCF1D[7:0]	控制字段1的优先比较数据 控制字段1的优先级比较数据	R/W
23:16	SCF1D[7:0]	控制字段1的辅助比较数据 控制字段1的辅助比较数据	R/W
31:24	CF1CE[7:0]	控制字段1比较位使能 选择是否比较控制字段1的位N。（N=0-7） 0：禁止控制字段1位N比较1：使能控制字段1位N比较	R/W

TCST位（BreakField输出定时器计数开始触发）

[Clearing condition]

●当0写入TCST时。BreakField输出定时器计数停止，TXDn输出变为空闲电平。

●当XCR2.BFLW[15:0]中设置的周期的中断字段输出完成时。

[Setting condition]

- When 1 is written to TCST. Start Break Field output from TXDn. Holds 1 during Break Field output.

SDST bit (Start Frame detection enable)

When 1 is written to this bit, Start Frame detection starts. When XCR0.BFE = 1 is set, Break Field can be detected during Start Frame is detected and after Start frame is detected. When XCR0.BFE = 0 is set, Break Field is not detected.

When 0 is written to this bit, Start Frame detection and Break Field detection are stopped. However, if XSR0.RXDSF = 0 at the time of stop, it is not possible to stop data reception of the SCI core with this bit. Write 0 to CCR0.RE to stop the reception operation or perform reception completion processing (CSR.RDRF clear or RDR read) after reception is completed.

BMEN bit (Bit rate measurement enable)

Set this bit to 1 simultaneously with the SDST bit. When this bit is set to 1, the valid edge interval of Control Field 0 and Control Field 1 data is measured.

PCF1D[7:0] bit (Priority compare data for Control Field 1)

Set the priority compare data for Control Field 1.

SCF1D[7:0] bit (Secondary compare data for Control Field 1)

Set the secondary compare data for Control Field 1.

CF1CE[7:0] bit (Control Field 1 compare bit enable)

Select whether to compare bit N of Control Field 1. (N = 0 - 7)

When all of these bits are set to 0 (CF1CE[7:0] = 8'h00), it is always judged that Control Field 1 matches when reception is completed, and XSR0.CF1MF is set. This bit is a comparison enable with PCF1D[7:0] or SCF1D[7:0], and it is not a priority interrupt bit comparison enable.

26.2.16 XCR2 : Simple LIN Control Register 2

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x3C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BFLW[15:0]															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CF0CE[7:0]								CF0D[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CF0D[7:0]	Control Field 0 compare data The compare data for Control Field 0	R/W
15:8	CF0CE[7:0]	Control Field 0 compare bit enable Select whether to compare bit N of Control Field 0. (N = 0 - 7) 0: Control Field 0 bit N compare disabled 1: Control Field 0 bit N compare enabled	R/W
31:16	BFLW[15:0]	Break Field length setting This register sets the Break Field length. The Break Field length is (BFLW [15:0] setting value + 1) × clock of the timer. The upper limit for setting this register is 0xFFFE. (Setting prohibited for 0xFFFF)	R/W

CF0D[7:0] bit (Control Field 0 compare data)

The compare data for Control Field 0.

●当1写入TCST时。从TXDn开始中断字段输出。在BreakField输出期间保持1。

SDST位（起始帧检测使能）

当向该位写入1时，开始帧检测。当XCR0.BFE=1被设置时，BreakField可以被检测到
检测到起始帧并在检测到起始帧之后。当设置XCR0.BFE=0时，不检测中断字段。

当向该位写入0时，开始帧检测和中断字段检测停止。但是，如果停止时XSR0.RXDSF=0，则无法通过该位停止SCI内核的数据接收。将0写入CCR0.RE以停止接收操作或在接收完成后执行接收完成处理（CSR.RDRF清除或RDR读取）。

BMEN位（比特率测量使能）

将此位与SDST位同时设置为1。当该位设置为1时，控制字段0的有效边沿间隔和
测量控制字段1数据。

PCF1D[7:0]位（控制字段1的优先比较数据）

设置控制字段1的优先比较数据。

SCF1D[7:0]位（控制字段1的辅助比较数据）

设置控制字段1的辅助比较数据。

CF1CE[7:0]位（控制字段1比较位使能）

选择是否比较控制字段1的位N。(N=07)

当所有这些位都设置为0(CF1CE[7:0]=8'h00)时，在接收完成时总是判断控制字段1匹配，并设置XSR0.CF1MF。该位是与PCF1D[7:0]或SCF1D[7:0]的比较使能，不是优先中断位比较使能。

26.2.16 XCR2：简单LIN控制寄存器2

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x3C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BFLW[15:0]															
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CF0CE[7:0]								CF0D[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CF0D[7:0]	控制字段0比较数据 控制字段0的比较数据	R/W
15:8	CF0CE[7:0]	控制字段0比较位使能 选择是否比较控制字段0的位N。（N=07） 0：禁用控制字段0位N比较1：启用控制字段0位N比较	R/W
31:16	BFLW[15:0]	中断字段长度设置 该寄存器设置中断字段长度。 BreakField长度为(BFLW[15:0]设置值+1)×定时器时钟。 设置该寄存器的上限为0xFFFE。（0xFFFF禁止设置）	R/W

CF0D[7:0]位（控制字段0比较数据）

控制字段0的比较数据。

CF0CE[7:0] bit (Control Field 0 compare bit enable)

Select whether to compare bit N of Control Field 0. (N = 0 - 7)

When all of these bits are set to 0 (CF0CE[7:0] = 8'h00), it is always judged that Control Field 0 matches when reception is completed, and XSR0.CF0MF is set.

BFLW[15:0] bit (Break Field length setting)

BFLW[15:0] are 16-bit Break Field length setting bits and the initial value is 0xFFFE.

Set the Break Field length to 1 frame or more. The LIN standard stipulates that the Break Field length is 13 bits or more.

When the Break Field sending. Writing 1 to TCST, SCI starts output the Break Field on TXDn. Up-counting is performed with the clock of the timer selected by XCR0.TCSS[1:0]. When the count value matches the value set in this register, up-counting is stopped and Break Field output from TXDn is also stopped.

When the Break Field receiving. Writing 1 to SDST, Start-Frame detection is enabled. SCI starts counting from the negative edge of RXDn. The clock of the timer is selected by XCR0.TCSS[1:0].

When the count value matches the value set in this register, it is determined that a Break Field has been detected. Up-counting continues until the next valid edge or counter overflow.

26.2.17 CSR : Common Status Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x48

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	RDRF	TEND	TDRE	FER	PER	MFF	—	ORER	—	—	—	—	—	DFER	DPER	DCMF
Value after reset:	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RXDMON	—	—	—	—	—	—	—	—	—	—	ERS	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0.	R
4	ERS	Error Signal Status Flag Valid only in Smart card interface mode 0: Error signal Low not responded 1: Error signal Low responded	R
14:5	—	These bits are read as 0.	R
15	RXDMON	Serial input data monitor bit The state of the RXDn terminal without synchronizing by bus clock is shown. 0: When RINV is 0, RXDn terminal is the low level. When RINV is 1, RXDn terminal is the High level. 1: When RINV is 0, RXDn terminal is the High level. When RINV is 1, RXDn terminal is the Low level.	R
16	DCMF	Data Compare Match Flag Valid only in Asynchronous mode 0: No matched 1: Matched	R
17	DPER	Data Compare Match Parity Error Flag Valid only in Asynchronous mode 0: No parity error occurred at address match detection 1: A parity error has occurred at address match detection	R

CF0CE[7:0]位（控制字段0比较位使能）

选择是否比较控制字段0的位N。（N=07）

当所有这些位都设置为0(CF0CE[7:0]=8'h00)时，当接收完成时总是判断控制字段0匹配，并设置XSR0.CF0MF。

BFLW[15:0]位（BreakField长度设置）

BFLW[15:0]是16位间隔字段长度设置位，初始值为0xFFFE。

将中断字段长度设置为1帧或更多。LIN标准规定BreakField长度为13位或更多。

当BreakField发送时。将1写入TCST，SCI开始在TXDn上输出BreakField。通过XCR0.TCSS[1:0]选择的定时器时钟执行递增计数。当计数值与该寄存器中设置的值匹配时，停止向上计数，并且也停止从TXDn输出中断字段。

当BreakField接收时。向SDST写入1，启动帧检测。SCI从RXDn的下降沿开始计数。定时器的时钟由XCR0.TCSS[1:0]选择。

当计数值与此寄存器中设置的值匹配时，确定已检测到中断字段。向上计数一直持续到下一个有效边沿或计数器溢出。

26.2.17 CSR：通用状态寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x48

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	RDRF	TEND	TDRE	FER	PER	MFF	—	ORER	—	—	—	—	—	DFER	DPER	DCMF
重置后的值：	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RXDMON	—	—	—	—	—	—	—	—	—	—	ERS	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	这些位读为0。	R
4	ERS	错误信号状态标志 仅在智能卡接口模式下有效 0：错误信号低电平未响应1：错误信号低电平响应	R
14:5	—	这些位读为0。	R
15	RXDMON	串行输入数据监控位 显示了没有通过总线时钟同步的RXDn端子的状态。 0：当RINV为0时，RXDn端为低电平。当RINV为1时，RXDn端为高电平。 1：当RINV为0时，RXDn端为高电平。当RINV为1时，RXDn端为低电平。	R
16	DCMF	数据比较匹配标志 仅在异步模式下有效 0：不匹配1：匹配	R
17	DPER	数据比较匹配奇偶校验错误标志 仅在异步模式下有效 0：地址匹配检测时未发生奇偶校验错误1：地址匹配检测时发生奇偶校验错误	R

Bit	Symbol	Function	R/W
18	DFER	Data Compare Match Framing Error Flag Valid only in Asynchronous mode 0: No framing error occurred at address match detection 1: A framing error has occurred at address match detection	R
23:19	—	These bits are read as 0.	R
24	ORER	Overrun Error Flag 0: No overrun error occurred 1: An overrun error has occurred	R
25	—	This bit is read as 0.	R
26	MFF	Mode Fault Flag Valid only in Simple SPI mode. 0: No mode fault error 1: Mode fault error	R
27	PER	Parity Error Flag 0: Non-FIFO selected (CCR3.FM = 0): No parity error occurred FIFO selected (CCR3.FM = 1): No parity error in all received data in receive-FIFO 1: Non-FIFO selected (CCR3.FM = 0): A parity error has occurred FIFO selected (CCR3.FM = 1): One or more parity errors occurred in received data in receive-FIFO	R
28	FER	Framing Error Flag 0: Non-FIFO selected (CCR3.FM = 0): No framing error occurred FIFO selected (CCR3.FM = 1): No framing error in all received data in receive-FIFO 1: Non-FIFO selected (CCR3.FM = 0): A framing error has occurred FIFO selected (CCR3.FM = 1): One or more framing errors occurred in received data in receive-FIFO	R
29	TDRE	Transmit Data Empty Flag 0: Non-FIFO selected (CCR3.FM = 0): Transmit data is in TDR register FIFO selected (CCR3.FM = 1): The quantity of transmit data written in transmit-FIFO exceeds the specified transmit triggering number. 1: Non-FIFO selected (CCR3.FM = 0): No transmit data is in TDR register FIFO selected (CCR3.FM = 1): The quantity of transmit data written in transmit-FIFO is equal to or less than the specified transmit triggering number.	R
30	TEND	Transmit End Flag 0: A character is being transmitted or standing by for transmission. 1: Character transfer has been completed, or sending Break Field.	R
31	RDRF	Receive Data Full Flag 0: Non-FIFO selected (CCR3.FM = 0): No received data is in RDR register FIFO selected (CCR3.FM = 1): The quantity of receive data written in receive-FIFO falls below the specified receive triggering number. 1: Non-FIFO selected (CCR3.FM = 0): Received data is in RDR register FIFO selected (CCR3.FM = 1): The quantity of receive data written in receive-FIFO is equal to or greater than the specified receive triggering number.	R

ERS bit (Error Signal Status Flag)

[Setting condition]

- When an error signal LOW is sampled.

[Clearing condition]

- When write 1 to CFCLR.ERSC.

DCMF bit (Data Compare Match Flag)

The DCMF bit indicates that SCI detects the match to the comparison data (CCR4.CMPD) with receive data.

Clearing the CCR0.RE bit to 0 does not affect the DCMF flag, which retains its previous state.

[Setting condition]

- Matched to the comparison data (CCR4.CMPD) with receive data, while CCR0.DCME = 1.

Bit	Symbol	Function	R/W
18	DFER	数据比较匹配帧错误标志 仅在异步模式下有效 0：地址匹配检测时未发生帧错误1：地址匹配检测时发生帧错误	R
23:19	—	这些位读为0。	R
24	ORER	溢出错误标志 0：未发生溢出错误1：发生溢出错误	R
25	—	该位读为0。	R
26	MFF	模式故障标志 仅在简单SPI模式下有效。 0：无模式故障错误1 ：模式故障错误	R
27	PER	奇偶校验错误标志 0：选择非FIFO（CCR3.FM=0）：未发生奇偶校验错误 已选择FIFO(CCR3.FM=1)：接收FIFO中所有接收数据均无奇偶校验错误 1：选择非FIFO（CCR3.FM=0）：发生奇偶校验错误 FIFO已选择（CCR3.FM=1）：接收FIFO中的接收数据发生一个或多个奇偶校验错误	R
28	FER	成帧错误标志 0：选择非FIFO（CCR3.FM=0）：未发生帧错误 选择FIFO(CCR3.FM=1)：接收中所有接收到的数据中没有帧错误 FIFO 1：选择非FIFO（CCR3.FM=0）：发生帧错误 FIFO已选择（CCR3.FM=1）：接收FIFO中的接收数据发生一个或多个帧错误	R
29	TDRE	传输数据空标志 0：选择非FIFO（CCR3.FM=0）：发送数据在TDR寄存器中 FIFO选择（CCR3.FM=1）：发送中写入的发送数据量 FIFO超过了指定的发送触发数。 1：选择非FIFO（CCR3.FM=0）：TDR寄存器中没有发送数据 FIFO选择（CCR3.FM=1）：发送中写入的发送数据量 FIFO等于或小于指定的发送触发数。	R
30	TEND	发送结束标志 0：字符正在传输或等待传输。1：字符传输已完成，或发送中断字段。	R
31	RDRF	接收数据满标志 0：选择非FIFO（CCR3.FM=0）：RDR寄存器中没有接收到的数据 FIFOselected(CCR3.FM=1)：接收写入的接收数据数量 FIFO低于指定的接收触发数。 1：选择非FIFO（CCR3.FM=0）：接收到的数据在RDR寄存器中 FIFOselected(CCR3.FM=1)：接收写入的接收数据数量 FIFO等于或大于指定的接收触发数。	R

ERS位（错误信号状态标志）

[Setting condition]

●采样错误信号LOW时。

[Clearing condition]

●CFCLR.ERSC写入1时。

DCMF位（数据比较匹配标志）

DCMF位指示SCI检测到比较数据(CCR4.CMPD)与接收数据的匹配。

将CCR0.RE位清为0不会影响DCMF标志，它保持其先前的状态。

[Setting condition]

●与接收数据匹配的比较数据（CCR4.CMPD），同时CCR0.DCME=1。

[Clearing condition]

- When write 1 to CFCLR.DCMFC.

DPER bit (Data Compare Match Parity Error Flag)

The DPER bit indicates that a parity error occurred at Address Match detection (reception data match detection).

Clearing the CCR0.RE bit to 0 does not affect the DPER flag, which retains its previous state.

[Setting condition]

- When a parity error was detected by the frame in which an address match was detected.

[Clearing condition]

- When write 1 to CFCLR.DPERC.

DFER bit (Data Compare Match Framing Error Flag)

The DFER bit indicates that a framing error occurred at Address Match detection (reception data match detection).

Clearing the CCR0.RE bit to 0 does not affect the DFER flag, which retains its previous state.

[Setting condition]

- When a stop bit of the frame in which an Address Match was detected is 0.
  When it is a 2-stop mode, the 1st bit of stop bit judges only whether it's 1 and doesn't check the 2nd bit of stop bit.

[Clearing condition]

- When write 1 to CFCLR.DFERC.

ORER bit (Overrun Error Flag)

The ORER bit indicates that an overrun error has occurred during reception and the reception ends abnormally.

Clearing the CCR0.RE bit to 0 does not affect the ORER flag, which retains its previous state. In Simple IIC mode, this bit is not use.

[Setting condition with Non-FIFO mode (CCR3.FM = 0)]

- When the next data is received before reading out RDR with no-error reception data stored in RDR.
  In RDR, receive data prior to an overrun error occurrence is retained, but data received after the overrun error occurrence is lost. When the ORER flag is set to 1, reception data isn't forwarded to RDR register.
  Note that, in clock synchronous mode and Simple SPI mode, serial reception will be stop.

[Setting condition with FIFO mode (CCR3.FM = 1)]

- When the next serial reception is completed while the receive FIFO is full of 16receive data.

[Clearing condition]

- When write 1 to CFCLR.ORERC.

MFF bit (Mode Fault Flag)

The MFF bit indicates mode fault errors. In a multi-master configuration, determine the mode fault error occurrence by reading the MFF flag.

[Setting condition]

- Input on the SSn pin being at the low level during master operation (CCR3.CKE[1:0] = 00 or 01) in simple SPI mode.

[Clearing condition]

- When write 1 to CFCLR.MFFC.

PER bit (Parity Error Flag)

The PER bit indicates that a parity error has occurred during reception and the reception ends abnormally.

Clearing the CCR0.RE bit to 0 does not affect the PER flag, which retains its previous state.

[Clearing condition]

●当CFCLR.DCMFC写1时。

DPER位（数据比较匹配奇偶校验错误标志）

DPER位指示在地址匹配检测（接收数据匹配检测）时发生奇偶校验错误。

将CCR0.RE位清除为0不会影响DPER标志，它会保留其先前的状态。

[Setting condition]

●当检测到地址匹配的帧检测到奇偶校验错误时。

[Clearing condition]

●向CFCLR.DPERC写入1时。

DFER位（数据比较匹配帧错误标志）

DFER位指示在地址匹配检测（接收数据匹配检测）时发生帧错误。

将CCR0.RE位清除为0不会影响DFER标志，它保持其先前的状态。

[Setting condition]

●当检测到地址匹配的帧的停止位为0时。
2停止模式时，停止位第1位只判断是否为1，不检查停止位第2位。

[Clearing condition]

●当CFCLR.DFERC写1时。

ORER位（溢出错误标志）

ORER位表示接收过程中发生溢出错误，接收异常结束。

将CCR0.RE位清为0不会影响ORER标志，它保持其先前的状态。在SimpleIIC模式下，该位不使用。

[非FIFO模式的设置条件(CCR3.FM=0)]

●在读取RDR之前接收到下一个数据时，RDR中存储的接收数据无错误。
在RDR中，保留发生溢出错误之前的接收数据，但发生溢出错误之后接收的数据会丢失。当ORER标志设置为1时，接收数据不转发到RDR寄存器。请注意，在时钟同步模式和简单SPI模式下，串行接收将停止。

[FIFO模式的设置条件(CCR3.FM=1)]

●当接收FIFO已满16个接收数据时，下一次串行接收完成时。

[Clearing condition]

●向CFCLR.ORERC写入1时。

MFF位（模式故障标志）

MFF位指示模式故障错误。在多主机配置中，通过读取MFF标志确定模式故障错误发生。

[Setting condition]

●SSn引脚上的输入在简单SPI模式下主机操作期间（CCR3.CKE[1:0]=00或01）为低电平。

[Clearing condition]

●CFCLR.MFFC写1时。

PER位（奇偶校验错误标志）

PER位表示接收过程中发生奇偶校验错误，接收异常结束。

将CCR0.RE位清为0不会影响PER标志，它保持其先前的状态。

In Clock-synchronous mode, Simple SPI mode and Simple IIC mode, this bit not used.

[Setting condition]

- When a parity error is detected during reception. In FIFO select mode, when one or more parity error is detected in receive-FIFO data.
  In non-FIFO mode, although receive data when the parity error occurs is transferred to RDR, no SCIn_RXI interrupt request occurs. Note that when the PER flag is being set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When write 1 to CFCLR.PERC.

FER bit (Framing Error Flag)

The FER bit indicates that a framing error has occurred during reception and the reception ends abnormally.

Clearing the CCR0.RE bit to 0 does not affect the FER flag, which retains its previous state.

In Clock-synchronous mode, Simple SPI mode and Simple IIC mode, this bit not used.

[Setting condition]

- When 0 is sampled as the stop bit during reception. In FIFO select mode, when one or more framing error is detected in receive-FIFO data. In Manchester mode, when both sampling results (1⁄4 and 3⁄4 sampling points) are not 1 for 1 stop bit. In simple LIN mode, even if a condition that changes to 1 occurs when XCR1.SDST = 1, the FER set timing is delayed up to the Break Field judgment timing at the longest, since it may be a Break Field. If an edge is detected on the RXDn signal before the Break Field judgment timing, FER is detected. If no edge is detected in the RXDn signal before the Break Field judgment timing, Break Field is detected.
  In 2-stop-bit mode, only the first stop bit is checked whether it is 1 but the second stop bit is not checked. In non-FIFO mode, although receive data when the framing error occurs is transferred to RDR, no SCIn_RXI interrupt request occurs. In addition, when the FER flag is being set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When write 1 to CFCLR.FERC.

TDRE bit (Transmit Data Empty Flag)

[Non-FIFO selected (CCR3.FM = 0)]

The TDRE bit indicates the presence of transmit data in the TDR register.

The condition of CCR0.TE = 0 has priority over the condition of 0.

If other conditions that become 1 and conditions that become 0 are satisfied at the same time, the TDRE flag is set to 0.

[Setting condition]

- When CCR0.TE is 0.
- When data is transmitted from the TDR register to the TSR register.

[Clearing condition]

- When write 1 to CFCLR.TDREC.
- When the transmission data is written to the TDR register during CCR0.TE = 1.

[FIFO selected (CCR3.FM = 1)]

The TDRE bit indicates that data has been transferred from the transmit-FIFO (TDR) into the transmit shift register (TSR), the quantity of data in transmit-FIFO has fallen below the specified transmit triggering number.

When the condition which becomes 1 and the condition which becomes 0 were formed at the same time, TDRE flag will be 0. After that, when the number of data stored in transmit-FIFO is judged, and if that is same or greater than TTRG value, TDRE is set to 1 after 1 PCLK.

[Setting condition]

- When the quantity of transmit data written in transmit-FIFO is equal to or less than the specified transmit triggering number*1.

在时钟同步模式、简单SPI模式和简单IIC模式下，该位未使用。

[Setting condition]

●在接收过程中检测到奇偶校验错误时。在FIFO选择模式下，当在接收FIFO数据中检测到一个或多个奇偶校验错误时。在非FIFO模式下，虽然发生奇偶校验错误时的接收数据会传输到RDR，但不会发生SCIn_RXI中断请求。请注意，当PER标志设置为1时，后续接收数据不会传输到RDR。

[Clearing condition]

●向CFCLR.PERC写入1时。

FER位（帧错误标志）

FER位表示接收过程中发生了帧错误，接收异常结束。

将CCR0.RE位清除为0不会影响FER标志，它保持其先前的状态。

在时钟同步模式、简单SPI模式和简单IIC模式下，该位未使用。

[Setting condition]

●在接收过程中采样0作为停止位时。在FIFO选择模式下，当在接收FIFO数据中检测到一个或多个帧错误时。在曼彻斯特模式下，当两个采样结果（1 4和3 4采样点）对于1个停止位都不是1时。在简单LIN模式下，即使在XCR1.SDST=1时发生变为1的条件，FER设置时序最长也会延迟到BreakField判断时序，因为它可能是一个BreakField。如果在BreakField判断时序之前检测到RXDn信号的边沿，则检测到FER。如果在BreakField判断时序之前在RXDn信号中没有检测到边沿，则检测到BreakField。在2-stop-bit模式下，只检查第一个停止位是否为1，不检查第二个停止位。在非FIFO模式下，虽然发生帧错误时的接收数据被传输到RDR，但不会发生SCIn_RXI中断请求。此外，当FER标志设置为1时，后续接收数据不会传输到RDR。

[Clearing condition]

●CFCLR.FERC写入1时。

TDRE位（发送数据空标志）

[Non-FIFO selected (CCR3.FM = 0)]

TDRE位指示TDR寄存器中存在发送数据。

CCR0.TE=0的条件优先于0的条件。

如果同时满足其他变为1的条件和变为0的条件，则TDRE标志设置为0。

[Setting condition]

●当CCR0.TE为0时。

●当数据从TDR寄存器传送到TSR寄存器时。

[Clearing condition]

●CFCLR.TDREC写入1时。

●在CCR0.TE=1期间将发送数据写入TDR寄存器时。

[FIFO selected (CCR3.FM = 1)]

TDRE位表示数据已从发送FIFO(TDR)传输到发送移位寄存器(TSR)，发送FIFO中的数据量已低于指定的发送触发数。

当变为1的条件和变为0的条件同时形成时，TDRE标志将为0。之后，当判断存储在发送FIFO中的数据数量时，如果相同或大于TTRG值，TDRE在1个PCLK之后设置为1。

[Setting condition]

●当写入到transmit-FIFO中的发送数据量等于或小于指定的发送触发数*1时。

Note 1. The transmit-FIFO is FIFO register of 16 steps, the maximum number of data that can be written when the TDRE flag is 1 is indicated in 0x10 - FTSR.T[5:0]. Even if data any more is written, data is discarded.

[Clearing condition]

- When write 1 to CFCLR.TDREC.
- When the transmission data is written to transmit-FIFO by the DTC or DMAC (the last block transfer when block transfer).

TEND bit (Transmit End Flag)

[Non-FIFO selected (CCR3.FM = 0), and Not Smart card interface mode (CCR3.MOD[2:0] ≠ 001)]

The TEND bit indicates completion of transmission.

[Setting condition]

- When CCR0.TE is 0.
- When the CCR0.TE bit is changed from 0 to 1, the TEND flag is not affected and retains the value 1.
- When the TDR register is not updated at the time of transmission of the tail-end bit of a character being transmitted.
- When the TDR register is not updated at the end of DE negate time with DE control function enable (CCR3.DEN = 1).
- When Break Field is sending.

[Clearing condition]

- After the synchronization delay time has elapsed since the transmission data was written to the TDR register during CCR0.TE = 1.
- When write 1 to CFCLR.TDREC during CCR0.TE = 1.

[Non-FIFO selected (CCR3.FM = 0), and Smart card interface mode (CCR3.MOD [2:0] = 001)]

With no error signal from the receiving side, this bit is set to 1 when further data for transfer is ready to be transferred to the TDR register.

[Setting condition]

- When CCR0.TE is 0.
- When the CCR0.TE bit is changed from 0 to 1, the TEND flag is not affected and retains the value 1.
- When a specified period has elapsed after the latest transmission of 1 byte, the ERS flag is 0, and the TDR register is not updated. The set timing is determined by register settings as listed below.1
  When GM = 0 and BLK = 0, 12.5etu after the start of transmission
  When GM = 0 and BLK = 1, 11.5etu after the start of transmission
  When GM = 1 and BLK = 0, 11.0etu after the start of transmission
  When GM = 1 and BLK = 1, 11.0etu after the start of transmission

[Clearing condition]

- After the synchronization delay time has elapsed since the transmission data was written to the TDR register during CCR0.TE = 1.
- When write 1 to CFCLR.TDREC during CCR0.TE = 1.

[FIFO selected (CCR3.FM = 1)]

The TEND bit indicates that the transmit-FIFO does not contain valid data when transmitting the last bit of a serial character, so the transmission is halted.

[Setting condition]

- TEND is set to 1 when transmit-FIFO does not contain transmit data when the last bit of a one-byte serial character is transmitted.
- When the TDR register is not updated at the end of DE negate time with DE control function enable (CCR3.DEN = 1).

[Clearing condition]

注1.发送FIFO为16步的FIFO寄存器，TDRE标志为1时可写入的最大数据数在0x10FTSR.T[5:0]中指示。即使再写入数据，也会丢弃数据。

[Clearing condition]

●CFCLR.TDREC写入1时。

●当传输数据被DTC或DMAC写入传输FIFO时（块传输时的最后一个块传输）。

TEND位（发送结束标志）

[选择非FIFO(CCR3.FM=0)，且非智能卡接口模式(CCR3.MOD[2:0]≠001)]

TEND位指示传输完成。

[Setting condition]

●当CCR0.TE为0时。

●当CCR0.TE位由0变为1时，TEND标志不受影响，保持值为1。

●TDR寄存器在发送一个字符的尾端位时没有更新。

●当在DE取反时间结束时TDR寄存器没有更新且DE控制功能使能(CCR3.DEN=1)。

●发送中断字段时。

[Clearing condition]

●在CCR0.TE=1期间，自发送数据写入TDR寄存器起，经过同步延迟时间后。

●在CCR0.TE=1期间向CFCLR.TDREC写入1时。

[选择非FIFO(CCR3.FM=0)和智能卡接口模式(CCR3.MOD[2:0]=001)]

在接收端没有错误信号的情况下，当进一步的传输数据准备好传输到接收端时，该位设置为1
TDR register.

[Setting condition]

●当CCR0.TE为0时。

●当CCR0.TE位由0变为1时，TEND标志不受影响，保持值为1。

●在最后一次发送1个字节后经过指定时间后，ERS标志为0，并且不更新TDR寄存器。设置时序由寄存器设置确定，如下所示。1当GM=0和BLK=0时，发送开始后12.5etu当GM=0和BLK=1时，开始发送后11.5etu当GM=1和BLK=0，传输开始后11.0etu当GM=1且BLK=1，传输开始后11.0etu

[Clearing condition]

●在CCR0.TE=1期间，自发送数据写入TDR寄存器起，经过同步延迟时间后。

●在CCR0.TE=1期间向CFCLR.TDREC写入1时。

[FIFO selected (CCR3.FM = 1)]

TEND位表示在发送串行字符的最后一位时，发送FIFO不包含有效数据，因此暂停发送。

[Setting condition]

●当发送一个字节串行字符的最后一位时，当发送FIFO不包含发送数据时，TEND设置为1。

●当在DE取反时间结束时TDR寄存器没有更新且DE控制功能使能(CCR3.DEN=1)。

[Clearing condition]

- After the synchronization delay time has elapsed since the transmission data was written to the TDR register during CCR0.TE = 1.

RDRF bit (Receive Data Full Flag)

[Non-FIFO selected (CCR3.FM = 0)]

The RDRF bit indicates the presence of receive data in the RDR register.

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register.

[Clearing condition]

- When write 1 to CFCLR.RDRFC.
- When the read data is read from the RDR register.

[FIFO selected (CCR3.FM = 1)]

The RDRF bit indicates that receive data has been transferred to the receive FIFO data register (RDR), and the quantity of data in receive-FIFO is equal to or greater than the specified receive triggering number. When FCR.RTRG is set to 0, RDRF is set if the quantity of data in receive-FIFO is greater than or equal to 1.

[Setting condition]

- RDRF is set to 1 when the quantity of receive data in receive-FIFO is equal to or greater than the specified receive triggering number*1.

Note 1. Since the receive-FIFO is 16 stage FIFO register, the maximum quantity of data that can be read when RDF is 1 is equivalent to the specified receive data count number (FDR.R[5:0]). If an attempt is made to read after all the data in receive-FIFO has been read, the data is undefined.

[Clearing condition]

- When write 1 to CFCLR.RDRFC.
- When the reception data is read form receive-FIFO by the DTC or DMAC (the last block transfer when block transfer).

When the condition which becomes 1 and the condition which becomes 0 were formed at the same time, RDRF flag will be 0. After that, when the number of stored data in receive-FIFO is judged, and if that is same or greater than RTRG value, RDRF is set to 1 behind 1 PCLK.

Note: Except when interruption communication, RDRF and TDRE should not be cleared by CFCLR register.

26.2.18 ISR : Simple IIC Status Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x4C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	IICSTIF	—	—	IICACKR
Value after reset:	0	0	0	0	0	0	0	0	0	0	x	x	0	x	0	0

Bit	Symbol	Function	R/W
0	IICACKR	ACK Reception Data Flag 0: ACK received 1: NACK received	R

●在CCR0.TE=1期间，自发送数据写入TDR寄存器起，经过同步延迟时间后。

RDRF位（接收数据满标志）

[Non-FIFO selected (CCR3.FM = 0)]

RDRF位指示RDR寄存器中存在接收数据。

[Setting condition]

●接收正常结束时，接收数据从RSR寄存器转发到RDR寄存器。

[Clearing condition]

●当CFCLR.RDRFC写1时。

●从RDR寄存器读取读取数据时。

[FIFO selected (CCR3.FM = 1)]

RDRF位表示接收数据已经传送到接收FIFO数据寄存器（RDR），并且接收FIFO中的数据量等于或大于指定的接收触发数。当FCR.RTRG设置为0时，如果接收FIFO中的数据量大于或等于1，则设置RDRF。

[Setting condition]

●当receive-FIFO中接收数据的数量等于或大于指定的接收触发数*1时，RDRF设置为1。

注1.由于接收FIFO为16级FIFO寄存器，当RDF为1时可读取的最大数据量等于指定的接收数据计数(FDR.R[5:0])。如果在接收FIFO中的所有数据都已读取后尝试读取，则数据未定义。

[Clearing condition]

●当CFCLR.RDRFC写1时。

●当接收数据由DTC或DMAC从接收FIFO中读取时（块传输时的最后一个块传输）。

当变为1的条件和变为0的条件同时形成时，RDRF标志将为0。之后，当判断接收FIFO中存储的数据数量时，如果该数量等于或大于RTRG值，RDRF在1个PCLK之后设置为1。

Note: 除中断通信外，RDRF和TDRE不应由CFCLR寄存器清零。

26.2.18 ISR：简单IIC状态寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x4C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	IICSTIF	—	—	IICACKR
重置后的值:	0	0	0	0	0	0	0	0	0	0	x	x	0	x	0	0

Bit	Symbol	Function	R/W
0	IICACKR	ACK接收数据标志 0：收到ACK1：收到NACK	R

Bit	Symbol	Function	R/W
1	—	This bit is read as 0.	R
2	—	The read value is undefined.	R
3	IICSTIF	Issuing of Start, Restart, or Stop Condition Completed Flag 0: There are no requests for generating conditions or a condition is being generated. 1: A start, restart, or stop condition is completely generated.	R
5:4	—	The read value is undefined.	R
31:6	—	These bits are read as 0.	R

IICACKR bit (ACK Reception Data Flag)

Received ACK and NACK bits can be read from this bit.

The IICACKR flag is updated at the rising of SCLn clock for the ACK/NACK receiving bit.

IICSTIF bit (Issuing of Start, Restart, or Stop Condition Completed Flag)

After generating a condition, this bit indicates that the generation is completed. When using the IICSTAREQ, IICRSTAREQ, or IICSTPREQ bit to cause generation of a condition, do so after setting the IICSTIF flag to 0.

When the IICSTIF flag is 1 while an interrupt request is enabled by setting the CCR0.TEIE bit, an STIn request is output.

[Setting condition]

- Completion of the generation of a start, restart, or stop condition (however, in cases where this conflicts with any of the conditions for the flag becoming 0 listed below, the clearing condition takes precedence)

[Clearing condition]

- Writing 1 to CFCLR.IICSTIFC bit
- When operation is not in Simple IIC mode
- Writing 0 to CCR0.TE bit

26.2.19 FRSR : FIFO Receive Status Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	FNUM[5:0]						—	—	PNUM[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	R[5:0]						—	—	—	—	—	—	—	DR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	0

Bit	Symbol	Function	R/W
0	DR	Receive Data Ready flag 0: Receiving is in progress, or no received data has remained in receive-FIFO after normally completed receiving.(receive-FIFO is empty) 1: The following receive data does not come for a fixed period after storing data under the threshold in the receive-FIFO	R
1	—	The read value is undefined.	R
7:2	—	These bits are read as 0.	R

Bit	Symbol	Function	R/W
1	—	该位读为0。	R
2	—	读取值未定义。	R
3	IICSTIF	发出启动、重启或停止条件完成标志 0：没有条件生成请求或正在生成条件。1：完全生成启动、重新启动或停止条件。	R
5:4	—	读取值未定义。	R
31:6	—	这些位读为0。	R

IICACKR位（ACK接收数据标志）

可以从该位读取接收到的ACK和NACK位。

IICACKR标志在ACKNACK接收位的SCLn时钟上升时更新。

IICSTIF位（发出启动、重启或停止条件完成标志）

生成条件后，该位表示生成完成。当使用IICSTAREQ、IICRSTAREQ或IICSTPREQ位来产生条件时，请在将IICSTIF标志设置为0后执行此操作。

当IICSTIF标志为1且通过设置CCR0.TEIE位使能中断请求时，输出STIn请求。

[设定条件]

●启动、重新启动或停止条件的生成完成（但是，如果这与下面列出的标志变为0的任何条件相冲突，则清除条件优先）

[结算条件]

●向CFCLR.IICSTIFC位写入1

●非SimpleIIC模式操作时

●将0写入CCR0.TE位

26.2.19 FRSR:FIFO接收状态寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	FNUM[5:0]						—	—	PNUM[5:0]					
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	R[5:0]						—	—	—	—	—	—	—	DR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	0

Bit	Symbol	Function	R/W
0	DR	接收数据就绪标志 0：接收中，或正常接收完成后receive-FIFO中没有接收到的数据。（receive-FIFO为空） 1：在接收FIFO中存储低于阈值的数据后，随后的接收数据在一个固定的时间内没有到来	R
1	—	读取值未定义。	R
7:2	—	这些位读为0。	R

Bit	Symbol	Function	R/W
13:8	R[5:0]	Receive-FIFO Data Count Valid in Asynchronous mode (including multi-processor), Clock synchronous mode, Simple SPI mode, when FCR.FM is 1. Indicate the quantity of receive data stored in receive-FIFO	R
15:14	—	These bits are read as 0.	R
21:16	PNUM[5:0]	Parity Error Count Valid only in Asynchronous mode Indicates the quantity of data with a parity error among the receive data stored in the receive FIFO data register.	R
23:22	—	These bits are read as 0.	R
29:24	FNUM[5:0]	Framing Error Count Valid only in Asynchronous mode Indicates the quantity of data with a framing error among the receive data stored in the receive FIFO data register.	R
31:30	—	These bits are read as 0.	R

DR bit (Receive Data Ready flag)

The DR bit indicates that the quantity of data stored in the receive FIFO data register (RDR) falls below the specified receive triggering number, and that no next data has been received yet after the elapse of 15 etu from the last stop bit in asynchronous mode. This bit is valid only Asynchronous mode (including multi-processor mode) and FIFO selected. In other mode, this bit does not set to 1.

[Setting conditions]

- DR is set to 1 when the following conditions are met.
  - After receive-FIFO(RDR) receives less data than the specified receive triggering number, no next data has been received yet after the elapse of 15 etu*1 from the last stop bit
  - CSR.FER, PER flags are 0.

Note 1. This is equivalent to one and a half (1.5) frames in the 8-bit format with one stop bit (etu: elementary time unit).

[Clearing conditions]

- When all receive data in the receive FIFO (RDR register) is read and 1 is written to FFCLR.DRC.
- When CCR3.FM bit is 0.

R[5:0] bit (Receive-FIFO Data Count)

The R[5:0] bits indicate the quantity of receive data stored in receive-FIFO.

0x00 means no receive data. 0x10 means receive-FIFO is full.

PNUM[5:0] bit (Parity Error Count)

The value indicates the quantity of data stored in the receive-FIFO registers with a parity error.

FNUM[5:0] bit (Framing Error Count)

The value indicates the quantity of data stored in the receive-FIFO registers with a framing error.

Bit	Symbol	Function	R/W
13:8	R[5:0]	接收FIFO数据计数 在异步模式（包括多处理器）、时钟同步模式、简单模式下有效 SPI模式，当FCR.FM为1时。 表示在receive-FIFO中存储的接收数据的数量	R
15:14	—	这些位读为0。	R
21:16	PNUM[5:0]	奇偶错误计数 仅在异步模式下有效 表示接收FIFO数据寄存器中存储的接收数据中有奇偶校验错误的数据数量。	R
23:22	—	这些位读为0。	R
29:24	FNUM[5:0]	帧错误计数 仅在异步模式下有效 表示接收FIFO数据寄存器中存储的接收数据中存在帧错误的数据数量。	R
31:30	—	这些位读为0。	R

DR位（接收数据就绪标志）

DR位表示存储在接收FIFO数据寄存器（RDR）中的数据量低于指定的接收触发数，并且异步模式下从最后一个停止位经过15个etu后还没有接收到下一个数据.该位仅在异步模式（包括多处理器模式）和选择的FIFO中有效。在其他模式下，该位不设置为1。

[Setting conditions]

●满足以下条件时，DR设置为1。

在receive-FIFO(RDR)接收到的数据少于指定的接收触发数后，从最后一个停止位开始经过15etu*1后还没有接收到下一个数据

CSR.FER、PER标志为0。

注1.这相当于带一个停止位的8位格式的一帧半(1.5)帧（etu：基本时间单位）。

[Clearing conditions]

●当接收FIFO（RDR寄存器）中的所有接收数据被读取并将1写入FFCLR.DRC时。

●当CCR3.FM位为0时。

R[5:0]位（接收FIFO数据计数）

R[5:0]位指示存储在接收FIFO中的接收数据的数量。

0x00表示没有接收数据。0x10表示接收FIFO已满。

PNUM[5:0]位（奇偶错误计数）

该值表示存储在接收FIFO寄存器中的具有奇偶校验错误的数据量。

FNUM[5:0]位（帧错误计数）

该值表示存储在接收FIFO寄存器中的具有帧错误的数据量。

26.2.20 FTSR : FIFO Transmit Status Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x54

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	T[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	T[5:0]	Transmit-FIFO Data Count Valid in Asynchronous mode (including multi-processor), Clock synchronous mode, Simple SPI mode, when FCR.FM is 1. Indicate the quantity of non-transmit data stored in transmit-FIFO	R
31:6	—	These bits are read as 0.	R

T[5:0] bit (Transmit-FIFO Data Count)

The T[5:0] bits indicate the quantity of non-transmitted data stored in transmit-FIFO.

0x00 means no un-transmit data. 0x10 means transmit- FIFO is full.

26.2.21 MSR : Manchester Status Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x58

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	RSYNC	—	MER	—	SBER	SYER	PFER
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PFER	Preface Error flag This bit is set when a preface error (pattern mismatch) is detected 0: No preface error detected 1: Preface error detected	R
1	SYER	SYNC Error flag This bit is set when no edge is detected in the adjustable range during receive retiming 0: No receive SYNC error detected 1: Receive SYNC error detected	R
2	SBER	Start Bit Error flag This bit is set when a pattern mismatch in the start bit area is detected 0: No start bit error detected 1: Start bit error detected	R
3	—	This bit is read as 0.	R

26.2.20 FTSR：FIFO发送状态寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x54

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	T[5:0]					
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	T[5:0]	发送FIFO数据计数 在异步模式（包括多处理器）、时钟同步模式、简单模式下有效 SPI模式，当FCR.FM为1时。 指示存储在发送FIFO中的非发送数据的数量	R
31:6	—	这些位读为0。	R

T[5:0]位（发送FIFO数据计数）

T[5:0]位指示存储在发送FIFO中的未发送数据的数量。

0x00表示没有未传输的数据。0x10表示传输FIFO已满。

26.2.21 MSR:曼彻斯特状态寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x58

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	RSYNC	—	MER	—	SBER	SYER	PFER
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PFER	前言错误标志 当检测到前言错误（模式不匹配）时设置该位 0：未检测到前言错误1：检测到前言错误	R
1	SYER	同步错误标志 当接收重定时期间在可调范围内未检测到边沿时，该位置位 0：未检测到接收同步错误1：检测到接收同步错误	R
2	SBER	起始位错误标志 当检测到起始位区域中的模式不匹配时，设置该位 0：未检测到起始位错误1：检测到起始位错误	R
3	—	该位读为0。	R

Bit	Symbol	Function	R/W
4	MER	Manchester Error Flag Valid for Manchester mode only 0: No Manchester error occurred 1: Manchester error has occurred	R
5	—	This bit is read as 0.	R
6	RSYNC	Receive SYNC data bit It is valid when MCR.SBSEL = 1 in Manchester mode, 0 is read otherwise. 0: The received the Start Bit is DATA SYNC 1: The received the Start Bit is COMMAND SYNC	R
31:7	—	These bits are read as 0.	R

PFER bit (Preface Error flag)

This bit indicates that a preface error was detected when receiving frames in Manchester mode.

Even when the RE bit in CCR0 is set to 0 (serial reception is disabled), the PFER flag is not affected and retains its previous value.

[Setting condition]

- When detecting a preface error when receiving frames in Manchester mode
  The following operations are performed when a preface error occurs.
  - <When MCR.PFEREN = 1>
    The received data is not transferred to the RDR register and no SCIn_RXI interrupt request occurs. Instead, an SCIn_ERI interrupt request occurs. Note that when the PFER flag is being set to 1, the subsequently received data is not transferred to the RDR register.
  - <When MCR.PFEREN = 0>
    The received data is transferred to the RDR register and an SCIn_RXI interrupt request occurs. An SCIn_ERI interrupt request is not generated. The subsequent receive operations are not affected even with the PFER flag being set to 1.

[Clearing condition]

- Write 1 to MFCLR.PFERC.

SYER bit (SYNC Error flag)

This bit indicates that a receive SYNC error was detected when receiving frames in Manchester mode with MCR.ERTEN = 1 (Manchester edge retiming enabled).

Even when the RE bit in CCR0 is set to 0 (serial reception is disabled), the SYER flag is not affected and retains its previous value.

[Setting condition]

- When detecting a receive SYNC error when receiving frames in Manchester mode
  The following operations are performed when a receive SYNC error occurs.
  - <When MCR.SYEREN = 1>
    Although the received data is transferred to the RDR register, no SCIn_RXI interrupt request occurs. Instead, an SCIn_ERI interrupt request occurs. Note that when the SYER flag is being set to 1, the subsequently received data is not transferred to the RDR register.
  - <When MCR.SYEREN = 0>
    The received data is transferred to the RDR register and an SCIn_RXI interrupt request occurs. An SCIn_ERI interrupt request is not generated. The subsequent receive operations are not affected even with the SYER flag being set to 1.

[Clearing condition]

- Write 1 to MFCLR.SYERC.

Bit	Symbol	Function	R/W
4	MER	曼彻斯特错误标志 仅适用于曼彻斯特模式 0：未发生曼彻斯特错误1：发生曼彻斯特错误	R
5	—	该位读为0。	R
6	RSYNC	接收同步数据位 曼彻斯特模式下MCR.SBSEL=1时有效，否则读取0。 0：接收的起始位为DATASYNC1：接收的起始位为COMMANDSYNC	R
31:7	—	这些位读为0。	R

PFER位（前言错误标志）

该位表示在曼彻斯特模式下接收帧时检测到前言错误。

即使将CCR0中的RE位设置为0（禁用串行接收），PFER标志也不受影响并保持其先前的值。

[Setting condition]

●曼彻斯特模式接收帧时检测到前言错误出现前言错误时执行以下操作
。

- <When MCR.PFEREN = 1>
  接收到的数据不会传输到RDR寄存器，也不会发生SCIn_RXI中断请求。相反，一个SCIn_ERI中断请求发生。请注意，当PFER标志设置为1时，随后接收到的数据不会传输到RDR寄存器。
- <When MCR.PFEREN = 0>
  接收到的数据被传送到RDR寄存器并产生SCIn_RXI中断请求。不产生SCIn_ERI中断请求。即使PFER标志设置为1，后续接收操作也不受影响。

[Clearing condition]

●向MFCLR.PFERC写入1。

SYER位（SYNC错误标志）

该位指示在MCR.ERTEN=1（启用曼彻斯特边沿重定时）的曼彻斯特模式下接收帧时检测到接收同步错误。

即使将CCR0中的RE位设置为0（禁用串行接收），SYER标志也不受影响并保持其先前的值。

[Setting condition]

●在曼彻斯特模式下接收帧时检测到接收SYNC错误发生接收SYNC错误时执行以下操作。

- <When MCR.SYEREN = 1>
  虽然接收到的数据被传送到RDR寄存器，但没有SCIn_RXI中断请求发生。相反，一个SCIn_ERI中断请求发生。请注意，当SYER标志设置为1时，随后接收到的数据不会传输到RDR寄存器。
- <When MCR.SYEREN = 0>
  接收到的数据被传送到RDR寄存器并产生SCIn_RXI中断请求。不产生SCIn_ERI中断请求。即使SYER标志设置为1，后续的接收操作也不受影响。

[Clearing condition]

●向MFCLR.SYERC写入1。

SBER bit (Start Bit Error flag)

This bit indicates that a start bit error was detected when receiving frames in Manchester mode.

Even when the RE bit in CCR0 is set to 0 (serial reception is disabled), the SBER flag is not affected and retains its previ-ous value.

[Setting condition]

- When detecting a start bit error when receiving frames in Manchester mode
  The following operations are performed when a start bit error occurs.
  - <When MCR.SBEREN = 1>
    The received data is not transferred to the RDR register and no SCIn_RXI interrupt request occurs. Instead, an SCIn_ERI interrupt request occurs. Note that when the SBER flag is being set to 1, the subsequently received data is not transferred to the RDR register.
  - <When MCR.SBEREN = 0>
    The received data is transferred to the RDR register and an SCIn_RXI interrupt request occurs. An SCIn_ERI interrupt request is not generated. The subsequent receive operations are not affected even with the SBER flag being set to 1.

[Clearing condition]

- Write 1 to MFCLR.SBERC.

MER bit (Manchester Error Flag)

When data is received in Manchester mode, Manchester error is detected, and it is displayed. Even when the RE bit in CCR0 is set to 0 (serial reception is disabled), the MER flag is not affected and retains its previ-ous value.

[Setting conditions]

- When receiving in Manchester mode and detecting Manchester code error in data area of received frame.
  Received data when an error occurs is transferred to the RDR register, but the SCIn_RXI interrupt request is not generated and the SCIn_ERI interrupt request is generated.
  When the Manchester error flag is set to 1, subsequent receive data is not transferred to the RDR register.
  For details on Manchester error, section 26.5.11. Errors in Manchester Mode.

[Clearing condition]

- Write 1 to MFCLR.MERC.

RSYNC bit (Receive SYNC data bit)

When Manchester mode (CCR3.MOD[2:0] = 101b) and MCR.SBSEL = 1, this bit indicates the type of SYNC of the received the Start Bit. For other settings, it is fixed to 0.

26.2.22 XSR0 : Simple LIN Status Register 0

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x5C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CF1RD[7:0]								CF0RD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	AEDF	COF	PIBDF	CF1MF	CF0MF	BFDF	BCDF	BFOF	—	—	—	—	—	—	RXDSF	SFSF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SBER位（起始位错误标志）

该位表示在曼彻斯特模式下接收帧时检测到起始位错误。

即使将CCR0中的RE位设置为0（禁用串行接收），SBER标志也不受影响并保持其先前的值。

[Setting condition]

●在曼彻斯特模式下接收帧时检测到起始位错误发生起始位错误时执行
以下操作。

- <When MCR.SBEREN = 1>
  接收到的数据不会传输到RDR寄存器，也不会发生SCIn_RXI中断请求。相反，一个
  SCIn_ERI中断请求发生。请注意，当SBER标志设置为1时，随后接收到的数据不会传输到RDR寄存器。
- <When MCR.SBEREN = 0>
  接收到的数据被传送到RDR寄存器并产生SCIn_RXI中断请求。不产生SCIn_ERI中断请求。即使SBER标志设置为1，后续接收操作也不受影响。

[Clearing condition]

●向MFCLR.SBERC写入1。

MER位（曼彻斯特错误标志）

在曼彻斯特模式下接收数据时，检测到曼彻斯特错误，并显示出来。即使当RE位在
CCR0设置为0（禁用串行接收），MER标志不受影响并保留其先前的值。

[Setting conditions]

●曼彻斯特模式接收时，检测接收帧数据区的曼彻斯特码错误。
发生错误时接收到的数据被传送到RDR寄存器，但不产生SCIn_RXI中断请求并产生SCIn_ERI中断请求。
当曼彻斯特错误标志设置为1时，后续接收数据不会传输到RDR寄存器。

有关曼彻斯特错误的详细信息，请参阅第26.5.11节。曼彻斯特模式中的错误。

[Clearing condition]

●向MFCLR.MERC写入1。

RSYNC位（接收SYNC数据位）

当曼彻斯特模式(CCR3.MOD[2:0]=101b)且MCR.SBSEL=1时，该位指示接收到的起始位的SYNC类型。对于其他设置，它固定为0。

26.2.22 XSR0：简单LIN状态寄存器0

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x5C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CF1RD[7:0]								CF0RD[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	AEDF	COF	PIBDF	CF1MF	CF0MF	BFDF	BCDF	BFOF	—	—	—	—	—	—	RXDSF	SFSF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SFSF	Start Frame Status flag 0: Start Frame detection disabled or Start Frame detection complete 1: Before Start Frame detection or during detection	R*1
1	RXDSF	RXDn input status flag 0: RXDn input to SCI is enabled 1: RXDn input to SCI is disabled	R*1
7:2	—	These bits are read as 0.	R
8	BFOF	Break Field Output completion flag 0: When Break Field is not output or during output 1: When Break Field output is completed	R
9	BCDF	Bus Conflict detection flag 0: When no Bus Conflict is detected 1: When Bus Conflict is detected	R
10	BFDF	Break Field detection flag 0: When Break Field is not detected 1: When Break Field is detected	R
11	CF0MF	Control Field 0 compare match flag 0: When Control-Field-0 data and the compare data does not match 1: When Control-Field-0 data and the compare data match	R
12	CF1MF	Control Field 1 compare match flag 0: When Control-Field-1 data and the compare data does not match 1: When Control-Field-1 data and the compare data match	R
13	PIBDF	Priority interrupt bit detection flag 0: When Priority interrupt bit is not detected 1: When Priority interrupt bit is detected	R
14	COF	Counter Overflow flag 0: When the counter for Break Field detection does not overflows 1: When the counter for Break Field detection overflows	R
15	AEDF	Active Edge detection flag 0: When Active edge is not detected 1: When Active edge is detected	R
23:16	CF0RD[7:0]	Control Field 0 received data Control Field 0 received data.	R
31:24	CF1RD[7:0]	Control Field 1 received data Control Field 1 received data.	R

Note 1. When PCLK is faster than TCLK, the flag set timing is delayed from the receive data full interrupt (SCIn_RXI) output. To refer to this flag under these conditions, wait at least 1 TCLK cycle after the receive data full interrupt (SCIn_RXI) before reading this register.

SFSF bit (Start Frame Status flag)

Indicates whether detect Start Frame is being detected.

[Setting condition]

- When 1 is written to XCR1.SDST.
- When a Break Field is detected in the Control Field0/Control Field 1/Information Field phase and the transition to the Control Field0 or Control Field1 reception state occurs.

[Clearing condition]

- When XCR1.SDST is 0.
- When Start Frame detection is completed.

RXDSF bit (RXDn input status flag)

Indicates the RXDn input status to the SCI core. When this bit is 1, RXDn input is received only by the simple LIN module and the Break Field is detected and is not input to the SCI core.

Bit	Symbol	Function	R/W
0	SFSF	起始帧状态标志 0：禁止开始帧检测或开始帧检测完成1：开始帧检测之前或检测期间	R*1
1	RXDSF	RXDn输入状态标志 0：启用SCI的RXDn输入1：禁用SCI的RXDn输入	R*1
7:2	—	这些位读为0。	R
8	BFOF	中断字段输出完成标志 0：BreakField不输出时或输出中1：BreakField输出完成时	R
9	BCDF	总线冲突检测标志 0：未检测到总线冲突时1：检测到总线冲突时	R
10	BFDF	中断字段检测标志 0：未检测到中断字段时1：检测到中断字段时	R
11	CF0MF	控制字段0比较匹配标志 0：当Control-Field-0数据和比较数据不匹配时1：当Control-Field-0数据和比较数据匹配时	R
12	CF1MF	控制字段1比较匹配标志 0：当Control-Field-1数据和比较数据不匹配时1：当Control-Field-1数据和比较数据匹配时	R
13	PIBDF	优先中断位检测标志 0：未检测到优先中断位时1：检测到优先中断位时	R
14	COF	计数器溢出标志 0：BreakField检测计数器未溢出时1：BreakField检测计数器溢出时	R
15	AEDF	主动边缘检测标志 0：未检测到有效边沿时1：检测到有效边沿时	R
23:16	CF0RD[7:0]	控制字段0接收数据控制字段 0接收数据。	R
31:24	CF1RD[7:0]	控制字段1接收数据控制字段 1接收数据。	R

注1.当PCLK快于TCLK时，标志设置时序从接收数据完整中断(SCIn_RXI)输出延迟。要在这些条件下引用该标志，请在接收数据完全中断（SCIn_RXI）之后至少等待1个TCLK周期，然后再读取该寄存器。

SFSF位（起始帧状态标志）

指示是否正在检测检测起始帧。

[Setting condition]

●当1写入XCR1.SDST时。

●当在ControlField0ControlField1InformationField阶段检测到一个BreakField并转换到ControlField0或ControlField1接收状态时。

[Clearing condition]

●XCR1.SDST为0时。

●当开始帧检测完成时。

RXDSF位（RXDn输入状态标志）

指示SCI内核的RXDn输入状态。当该位为1时，RXDn输入仅由简单LIN模块接收，并且中断字段被检测到并且不输入到SCI内核。

BFOF bit (Break Field Output completion flag)

Indicates the completion of Break Field output.

This bit can be cleared to 0 by writing 1 to XFCLR.BFOC.

BCDF bit (Bus Conflict detection flag)

Indicates the detection of bus conflict in Simple LIN transmit operation.

This bit can be cleared to 0 by writing 1 to XFCLR.BCDC.

BFDF bit (Break Field detection flag)

Indicates Break Field detection.

This bit can be cleared to 0 by writing 1 to XFCLR.BFDC.

CF0MF bit (Control Field 0 compare match flag)

Indicates compare match of Control Field 0 and compare data.

This bit can be cleared to 0 by writing 1 to XFCLR.CF0MC.

CF1MF bit (Control Field 1 compare match flag)

Indicates compare match detection of Control Field 1 and compare data.

This bit can be cleared to 0 by writing 1 to XFCLR.CF1MC.

PIBDF bit (Priority interrupt bit detection flag)

Indicates compare match detection of Control Field 1 and priority interrupt bit.

This bit can be cleared to 0 by writing 1 to XFCLR.PIBDC.

COF bit (Counter Overflow flag)

Indicates that the 16-bit counter in the simple LIN module has overflowed.

This bit can be cleared to 0 by writing 1 to XFCLR.COFC.

AEDF bit (Active Edge detection flag)

Indicates active edge detection.

This bit can be cleared to 0 by writing 1 to XFCLR.AEDC and when read out XSR1.TCNT[15:0].

CF0RD[7:0] bit (Control Field 0 received data)

Stores the received data with a Control Field 0 match detected.

CF1RD[7:0] bit (Control Field 1 received data)

Stores the received data with a Control Field 1 match detected.

26.2.23 XSR1 : Simple LIN Status Register 1

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x60

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TCNT[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BFOF位（BreakField输出完成标志）

表示中断字段输出完成。

可通过向XFCLR.BFOC写入1将该位清零。

BCDF位（总线冲突检测标志）

指示在简单LIN发送操作中检测到 总线冲突。

可通过向XFCLR.BCDC写入1将该位清零。

BFDF位（BreakField检测标志）

表示中断字段检测。

可通过向XFCLR.BFDC写入1将该位清零。

CF0MF位（控制字段0比较匹配标志）

表示控制字段0的比较匹配和比较数据。

通过向XFCLR.CF0MC写入1可将该位清零。

CF1MF位（控制字段1比较匹配标志）

表示控制字段1的比较匹配检测和比较数据。

该位可通过向XFCLR.CF1MC写入1清零。

PIBDF位（优先中断位检测标志）

表示控制字段1和优先级中断位的比较匹配检测。

可通过向XFCLR.PIBDC写入1将该位清零。

COF位（计数器溢出标志）

表示简单LIN模块中的16位计数器已溢出。

可通过向XFCLR.COFC写入1将该位清零。

AEDF位（有效边沿检测标志）

表示主动边缘检测。

该位可以通过向XFCLR.AEDC写入1以及在读取XSR1.TCNT[15:0]时清除为0。

CF0RD[7:0]位（控制字段0接收数据）

存储接收到的数据与检测到的控制字段0匹配。

CF1RD[7:0]位（控制字段1接收数据）

存储接收到的数据与检测到的控制字段1匹配。

26.2.23 XSR1：简单LIN状态寄存器1

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x60

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TCNT[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TCNT[15:0]	Timer Count Capture value Stores the 16-bit counter capture value. The initial value is 0000.	R
31:16	—	These bits are read as 0.	R

TCNT[15:0] bit (Timer Count Capture value)

Stores the capture value of the 16-bit counter of the Simple LIN module.

- When sending Start Frame
  This register holds the previous value.
- When receiving Start frame with Bit rate measurement disabled
  If a Break Field is detected in the Break Field detection state (refer to Figure 26.79), the Break Field length is captured and held (counter value is captured at the rising edge of RXDn). If a Break Field is detected in a state other than the Break Field detection state, the previous value is retained.
  If the counter overflows, it will not be captured.
- When receiving Start frame with Bit rate measurement enabled
  The count value is captured and held at the valid edge (both RXDn edges). However, in the Break Field detection state, the count value is not captured even if a valid edge occurs. Counter capture value retention is canceled by this register read. Even if a valid edge occurs before reading, the counter value is not captured.

26.2.24 CFCLR : Common Flag Clear Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x68

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	RDRFC	—	TDREC	FERC	PERC	MFFC	—	ORERC	—	—	—	—	—	DFERC	DPERC	DCMFC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	ERSC	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	The write value should be 0.	W
4	ERSC	ERS clear bit Setting this bit to 1 clears the CSR.ERS bit. The read value is always 0.	W
15:5	—	The write value should be 0.	W
16	DCMFC	DCMF clear bit Setting this bit to 1 clears the CSR.DCMF bit. The read value is always 0.	W
17	DPERC	DPER clear bit Setting this bit to 1 clears the CSR.DPER bit. The read value is always 0.	W
18	DFERC	DFER clear bit Setting this bit to 1 clears the CSR.DFER bit. The read value is always 0.	W
23:19	—	The write value should be 0.	W
24	ORERC	ORER clear bit Setting this bit to 1 clears the CSR.ORER bit. The read value is always 0.	W
25	—	The write value should be 0.	W
26	MFFC	MFF clear bit Setting this bit to 1 clears the CSR.MFF bit. The read value is always 0.	W
27	PERC	PER clear bit Setting this bit to 1 clears the CSR.PER bit. The read value is always 0.	W

Bit	Symbol	Function	R/W
15:0	TCNT[15:0]	定时器计数捕获值 存储16位计数器捕获值。初始值为0000。	R
31:16	—	这些位读为0。	R

TCNT[15:0]位（定时器计数捕捉值）

存储SimpleLIN模块的16位计数器的捕获值。

●发送起始帧时
该寄存器保存先前的值。

●接收起始帧且比特率测量禁用时
如果在中断字段检测状态下检测到中断字段（参见图26.79），则会捕获并保持中断字段长度（在RXDn的上升沿捕获计数器值）。如果在中断字段检测状态之外的状态下检测到中断字段，则保留先前的值。

如果计数器溢出，则不会被捕获。

●在启用比特率测量的情况下接收起始帧时
计数值被捕获并保持在有效边沿（两个RXDn边沿）。但是，在BreakField检测状态下，即使出现有效边沿，也不会捕获计数值。计数器捕获值保留被此寄存器读取取消。即使在读取之前出现有效边沿，也不会捕获计数器值。

26.2.24 CFCLR:公共标志清除寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x68

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	RDRFC	—	TDREC	FERC	PERC	MFFC	—	ORERC	—	—	—	—	—	DFERC	DPERC	DCMFC
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	ERSC	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	写入值应为0。	W
4	ERSC	ERS清零位 将此位设置为1会清除CSR.ERS位。读取值始终为0。	W
15:5	—	写入值应为0。	W
16	DCMFC	DCMF清零位 将此位设置为1会清除CSR.DCMF位。读取值始终为0。	W
17	DPERC	DPER清零位 将此位设置为1会清除CSR.DPER位。读取值始终为0。	W
18	DFERC	DFER清零位 将此位设置为1会清除CSR.DFER位。读取值始终为0。	W
23:19	—	写入值应为0。	W
24	ORERC	ORER清零位 将此位设置为1会清除CSR.ORER位。读取值始终为0。	W
25	—	写入值应为0。	W
26	MFFC	MFF清零位 将此位设置为1会清除CSR.MFF位。读取值始终为0。	W
27	PERC	PER清零位 将此位设置为1会清除CSR.PER位。读取值始终为0。	W

Bit	Symbol	Function	R/W
28	FERC	FER clear bit Setting this bit to 1 clears the CSR.FER bit. The read value is always	W
29	TDREC	TDRE clear bit Setting this bit to 1 clears the CSR.TDRE bit. The read value is always 0.	W
30	—	The write value should be 0.	W
31	RDRFC	RDRF clear bit Setting this bit to 1 clears the CSR.RDRF bit. The read value is always 0.	W

26.2.25 ICFCLR : Simple IIC Flag Clear Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x6C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	IICSTIFC	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	—	The write value should be 0.	W
3	IICSTIFC	IICSTIF clear bit Setting this bit to 1 clears the ISR.IICSTIF bit. The read value is always 0.	W
31:4	—	The write value should be 0.	W

26.2.26 FFCLR : FIFO Flag Clear Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x70

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DRC	DR clear bit Setting this bit to 1 clears the FRSR.DR bit. The read value is always 0.	W
31:1	—	The write value should be 0.	W

Bit	Symbol	Function	R/W
28	FERC	FER清除位 将此位设置为1会清除CSR.FER位。读取值始终为	W
29	TDREC	TDRE清零位 将此位设置为1会清除CSR.TDRE位。读取值始终为0。	W
30	—	写入值应为0。	W
31	RDRFC	RDRF清零位 将此位设置为1会清除CSR.RDRF位。读取值始终为0。	W

26.2.25 ICFCLR:简单的IIC标志清除寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x6C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	IICSTIFC	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	—	写入值应为0。	W
3	IICSTIFC	IICSTIF清零位 将此位设置为1会清除ISR.IICSTIF位。读取值始终为0。	W
31:4	—	写入值应为0。	W

26.2.26 FFCLR:FIFO标志清除寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x70

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DRC	DR清零位 将此位设置为1会清除FRSR.DR位。读取值始终为0。	W
31:1	—	写入值应为0。	W

26.2.27 MFCLR : Manchester Flag Clear Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x74

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	MERC	—	SBERC	SYERC	PFERC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PFERC	PFER clear bit Setting this bit to 1 clears the MSR.PFER bit. The read value is always 0.	W
1	SYERC	SYER clear bit Setting this bit to 1 clears the MSR.SYER bit. The read value is always 0.	W
2	SBERC	SBER clear bit Setting this bit to 1 clears the MSR.SBER bit. The read value is always 0.	W
3	—	The write value should be 0.	W
4	MERC	MER clear bit Setting this bit to 1 clears the MSR.MER bit. The read value is always 0.	W
31:5	—	The write value should be 0.	W

26.2.28 XFCLR : Simple LIN Flag Clear Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x78

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	AEDC	COFC	PIBDC	CF1MC	CF0MC	BFDC	BCDC	BFOC	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	The write value should be 0.	W
8	BFOC	BFOF clear bit Setting this bit to 1 clears the XSR0.BFOF bit. The read value is always 0.	W
9	BCDC	BCDF clear bit Setting this bit to 1 clears the XSR0.BCDF bit. The read value is always 0.	W
10	BFDC	BFDF clear bit Setting this bit to 1 clears the XSR0.BFDF bit. The read value is always 0.	W
11	CF0MC	CF0MF clear bit Setting this bit to 1 clears the XSR0.CF0MF bit. The read value is always 0.	W
12	CF1MC	CF1MF clear bit Setting this bit to 1 clears the XSR0.CF1MF bit. The read value is always 0.	W

26.2.27 MFCLR:曼彻斯特标志清除寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x74

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	MERC	—	SBERC	SYERC	PFERC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PFERC	PFER清零位 将此位设置为1会清除MSR.PFER位。读取值始终为0。	W
1	SYERC	SYER清零位 将此位设置为1会清除MSR.SYER位。读取值始终为0。	W
2	SBERC	SBER清零位 将此位设置为1会清除MSR.SBER位。读取值始终为0。	W
3	—	写入值应为0。	W
4	MERC	MER清零位 将此位设置为1会清除MSR.MER位。读取值始终为0。	W
31:5	—	写入值应为0。	W

26.2.28 XFCLR:简单的LIN标志清除寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x78

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	AEDC	COFC	PIBDC	CF1MC	CF0MC	BFDC	BCDC	BFOC	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	写入值应为0。	W
8	BFOC	BFOF清零位 将此位设置为1会清除XSR0.BFOF位。读取值始终为0。	W
9	BCDC	BCDF清零位 将此位设置为1会清除XSR0.BCDF位。读取值始终为0。	W
10	BFDC	BFDF清零位 将此位设置为1会清除XSR0.BFDF位。读取值始终为0。	W
11	CF0MC	CF0MF清零位 将此位设置为1会清除XSR0.CF0MF位。读取值始终为0。	W
12	CF1MC	CF1MF清零位 将此位设置为1会清除XSR0.CF1MF位。读取值始终为0。	W

Bit	Symbol	Function	R/W
13	PIBDC	PIBDF clear bit Setting this bit to 1 clears the XSR0.PIBDF bit. The read value is always 0.	W
14	COFC	COFF clear bit Setting this bit to 1 clears the XSR0.COF bit. The read value is always 0.	W
15	AEDC	AEDF clear bit Setting this bit to 1 clears the XSR0.AEDF bit and cancels holding the XSR1 register. The read value is always 0.	W
31:16	—	The write value should be 0.	W

26.2.29 CESR : Communication Enable Status Register

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TIST	—	—	—	RIST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RIST	RE Internal status 0: RE signal internal state value 0 1: RE signal internal state value 1	R
3:1	—	These bits are read as 0.	R
4	TIST	TE Internal status 0: TE signal internal state value 0 1: TE signal internal state value 1	R
7:5	—	These bits are read as 0.	R

The operation clocks of the communication module and control register can be used asynchronously. Since some control register values are transmitted internally via the synchronization circuit so that they operate correctly even if they are asynchronous, it takes some time for the state to be reflected internally after rewriting the control register.

Communication enable CCR0.TE and CCR0.RE correspond to this register, and when these control bits are set from 1 to 0 to rewrite the control bits for the next communication, the TE and RE signal It is necessary to rewrite the next control bit after the internal state becomes 0. If a very slow clock is used for the communication module clock, the TE and RE bit states will not be reflected slowly internally. At this time, you can check the internal status using this register.

26.3 Operation in Asynchronous Mode

Figure 26.4 shows the general format for asynchronous serial communications. One frame consists of a start bit (low level), transmit or receive data, a parity bit, and stop bits (high level). In asynchronous serial communications, the communications line is usually held in the mark state (high level).

The SCI monitors the communications line. When the SCI detects a start bit, it starts serial communication. The detection condition of the start bit changes according to the CCR3.RXDESEL setting. SCI regards space (Low level) as a start bit when CCR3.RXDESEL is 0. SCI regards a fall edge as a start bit when RXDESEL is 1.

Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communications. Both the transmitter and receiver have a double-buffered structure in addition to FIFO mode, so that data can be read or written during transmission or reception, enabling continuous data transmission and reception.

Bit	Symbol	Function	R/W
13	PIBDC	PIBDF清零位 将此位设置为1会清除XSR0.PIBDF位。读取值始终为0。	W
14	COFC	COFF清零位 将此位设置为1会清除XSR0.COF位。读取值始终为0。	W
15	AEDC	AEDF清零位 将此位设置为1会清除XSR0.AEDF位并取消保持XSR1寄存器。读取值始终为0。	W
31:16	—	写入值应为0。	W

26.2.29 CESR：通信使能状态寄存器

Base address: SCI_Bn = 0x4011_8000 + 0x0100 × n (n = 0 to 4, 9)

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TIST	—	—	—	RIST
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RIST	RE内部状态 0：RE信号内部状态值01：RE信号内部状态值1	R
3:1	—	这些位读为0。	R
4	TIST	TE内部状态 0：TE信号内部状态值01：TE信号内部状态值1	R
7:5	—	这些位读为0。	R

通信模块和控制寄存器的操作时钟可以异步使用。由于一些控制寄存器的值是通过同步电路在内部传输的，因此即使它们是异步的，它们也可以正常工作，因此在重写控制寄存器后，需要一些时间才能在内部反映状态。

通信使能CCR0.TE和CCR0.RE对应这个寄存器，当这些控制位被设置为1到0来改写下一次通信的控制位时，TE和RE信号后需要改写下一个控制位内部状态变为0。如果通信模块时钟使用非常慢的时钟，则TE和RE位状态不会在内部缓慢反映。此时，您可以使用该寄存器检查内部状态。

26.3 异步模式下的操作

图26.4显示了异步串行通信的一般格式。一帧由起始位（低电平）、发送或接收数据、奇偶校验位和停止位（高电平）组成。在异步串行通信中，通信线路通常保持在标记状态（高电平）。

SCI监控通信线路。当SCI检测到一个起始位时，它开始串行通信。起始位的检测条件根据CCR3.RXDESEL设置而变化。当CCR3.RXDESEL为0时，SCI将空格（低电平）作为起始位。当RXDESEL为1时，SCI将下降沿视为起始位。

在SCI内部，发射器和接收器是独立的单元，可实现全双工通信。发送器和接收器除了FIFO模式外，都具有双缓冲结构，以便在发送或接收过程中可以读取或写入数据，从而实现数据的连续发送和接收。

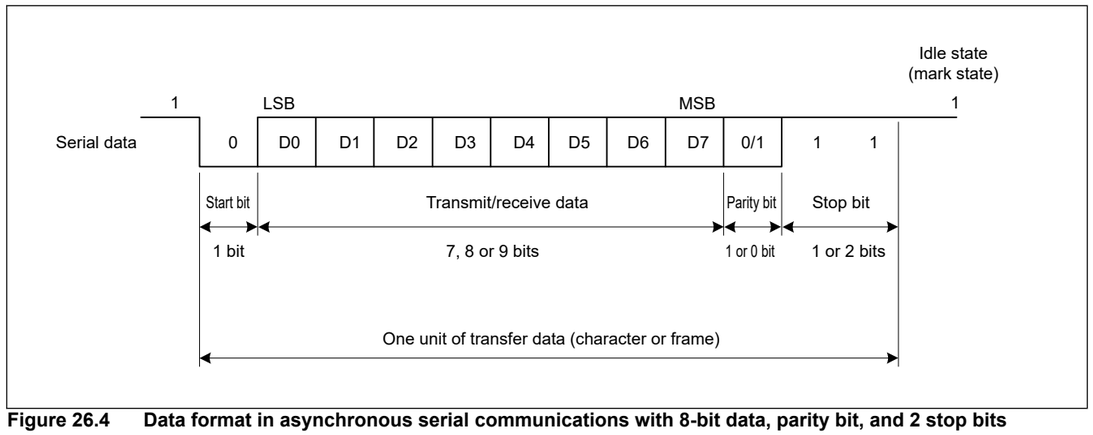


Figure 26.4 Data format in asynchronous serial communications with 8-bit data, parity bit, and 2 stop bits

26.3.1 Serial Data Transfer Format

Table 26.25 lists the serial data transfer formats that can be used in asynchronous mode. Any of 18 transfer formats can be selected with the CCR1 and CCR3 settings. For details on the multi-processor function, see section 26.4. Multi-Processor Communication Function.

Table 26.25 Serial transfer formats in asynchronous mode (1 of 2)

CCR3		CCR1		CCR3	Serial transfer format and frame length
CHR[1:0]		PE	MP	STP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	0	0	0	ST 9-bit data SP
0	0	0	0	1	ST 9-bit data SP SP
0	0	1	0	0	ST 9-bit data P SP
0	0	1	0	1	ST 9-bit data P SP SP
1	0	0	0	0	ST 8-bit data SP
1	0	0	0	1	ST 8-bit data SP SP
1	0	1	0	0	ST 8-bit data P SP
1	0	1	0	1	ST 8-bit data P SP SP
1	1	0	0	0	ST 7-bit data SP
1	1	0	0	1	ST 7-bit data SP SP
1	1	1	0	0	ST 7-bit data P SP
1	1	1	0	1	ST 7-bit data P SP SP

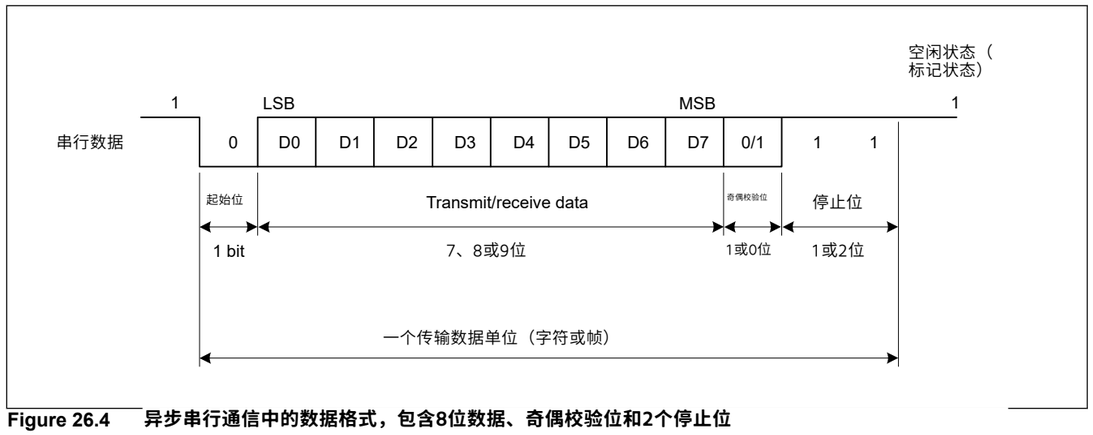


Figure 26.4 异步串行通信中的数据格式，包含8位数据、奇偶校验位和2个停止位

26.3.1 串行数据传输格式

表26.25列出了可以在异步模式下使用的串行数据传输格式。可以使用CCR1和CCR3设置选择18种传输格式中的任何一种。有关多处理器功能的详细信息，请参阅第26.4节。多处理器通信功能。

Table 26.25 异步模式下的串行传输格式（1of2）

CCR3		CCR1		CCR3	串行传输格式和帧长
CHR[1:0]		PE	MP	STP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	0	0	0	ST 9-bit data SP
0	0	0	0	1	ST 9-bit data SP SP
0	0	1	0	0	ST 9-bit data P SP
0	0	1	0	1	ST 9-bit data P SP SP
1	0	0	0	0	ST 8-bit data SP
1	0	0	0	1	ST 8-bit data SP SP
1	0	1	0	0	ST 8-bit data P SP
1	0	1	0	1	ST 8-bit data P SP SP
1	1	0	0	0	ST 7-bit data SP
1	1	0	0	1	ST 7-bit data SP SP
1	1	1	0	0	ST 7-bit data P SP
1	1	1	0	1	ST 7-bit data P SP SP

Table 26.25 Serial transfer formats in asynchronous mode (2 of 2)

CCR3		CCR1		CCR3	Serial transfer format and frame length
CHR[1:0]		PE	MP	STP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	—	1	0	ST 9-bit data MPB SP
0	0	—	1	1	ST 9-bit data MPB SP SP
1	0	—	1	0	ST 8-bit data MPB SP
1	0	—	1	1	ST 8-bit data MPB SP SP
1	1	—	1	0	ST 7-bit data MPB SP
1	1	—	1	1	ST 7-bit data MPB SP SP

ST: Start bit
SP: Stop bit
P: Parity bit
MPB: Multi-processor bit

26.3.2 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI operates on a base clock with a frequency of 16 times*1 the bit rate.

In reception, the SCI samples the falling edge of the start bit using the base clock, and performs internal synchronization.*2

Because receive data is sampled on the rising edge of the 8th pulse*1 of the base clock, data is latched at the middle of each bit (when sampling timing does not adjust (CCR4.ASEN = 0 or CCR4.ASEN = 1 and CCR4.AST[2:0] = 000b)), as shown in Figure 26.5 The reception margin in asynchronous mode is determined by the following formula (1):

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%] \quad \ldots \quad \text{Formula (1)}$$

Note: M: Reception margin
N: Ratio of bit rate to clock
(N = 16 when CCR2.ABCSE = 0 and CCR2.ABCS = 0,
N = 8 when CCR2.ABCSE = 0 and CCR2.ABCS = 1,
N = 6 when CCR2.ABCSE = 1)
D: Duty cycle of clock (D = 0.5 to 1.0)
L: Frame length (L = 9 to 13)
F: Absolute value of clock frequency deviation

Assuming values of F = 0 and D = 0.5 in formula (1), the reception margin is determined using the following formula:
$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\ \%$

This represents the computed value. Renesas recommends a margin of 20% to 30% in system design.

Note 1. In this example, the CCR2.ABCS bit is 0 and the CCR2.ABCSE is 0. When the ABCS bit is 1 and the ABCSE bit is 0, a frequency of 8 times the bit rate is used as a base clock, and receive data is sampled on the rising edge of the 4th pulse of the base clock.
When the ABCSE bit is 1, a sextuple frequency of a bit rate is used as a base clock, and receive data is sampled on the rising edge of the 3rd pulse of the base clock.

Note 2. The determination condition of the start bit is as follows.
The function of adjust sampling timing is OFF (ASEN = 0):

Table 26.25 异步模式下的串行传输格式(2of2)

CCR3		CCR1		CCR3	串行传输格式和帧长
CHR[1:0]		PE	MP	STP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	—	1	0	ST 9-bit data MPB SP
0	0	—	1	1	ST 9-bit data MPB SP SP
1	0	—	1	0	ST 8-bit data MPB SP
1	0	—	1	1	ST 8-bit data MPB SP SP
1	1	—	1	0	ST 7-bit data MPB SP
1	1	—	1	1	ST 7-bit data MPB SP SP

ST: 起始位停
SP: 止位奇偶
P: 校验位
MPB: Multi-processor bit

26.3.2 异步模式下接收数据采样时序和接收余量

在异步模式下，SCI在频率为16倍*1比特率的基本时钟上运行。

在接收时，SCI使用基本时钟对起始位的下降沿进行采样，并执行内部同步。*2

因为接收数据在基本时钟的第8个脉冲*1的上升沿进行采样，所以数据在每个位的中间锁存（当采样时序不调整时（CCR4.ASEN=0或CCR4.ASEN=1和CCR4.AST[2:0]=000b)），如图26.5所示异步模式下的接收余量由下式（1）确定：

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%] \quad \ldots \quad \text{Formula (1)}$$

Note: M：接收余量
N：比特率与时钟的比率
（当CCR2.ABCSE=0和CCR2.ABCS=0时，N=16，
当CCR2.ABCSE=0且CCR2.ABCS=1时，N=8，
N = 6 when CCR2.ABCSE = 1)
D:时钟占空比(D=0.5to1.0)
L：帧长（L=9到13）
F：时钟频率偏差的绝对值

假设公式（1）中的F=0和D=0.5的值，接收裕量使用以下公式确定：
$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\ \%$

这表示计算值。瑞萨建议在系统设计中留出20%到30%的余量。

注1.本例中，CCR2.ABCS位为0，CCR2.ABCSE位为0。当ABCS位为1，ABCSE位为0时，使用8倍比特率的频率作为基准时钟，并在基本时钟的第4个脉冲的上升沿对接收数据进行采样。

当ABCSE位为1时，以比特率的六倍频为基准时钟，在基准时钟的第3个脉冲的上升沿对接收数据进行采样。

注2.起始位的判断条件如下。

调整采样定时功能关闭（ASEN=0）：

The determination condition of a start bit is that Low beyond half bit length continues. It is same as the sampling timing. In Figure 26.5, Low period should be kept over 8-cycles to detect a start bit. If Low period does not keep over 8-cycles, the IP judges this as a noise. So, the IP does not start reception and wait start bit.

The function of adjust sampling timing is ON (ASEN = 1):

The determination condition of a start bit is that Low keeps up until the sampling timing. Adjusting the sampling timing forward (AJD = 1) increases the possibility of erroneously determining a noise as the start bit.

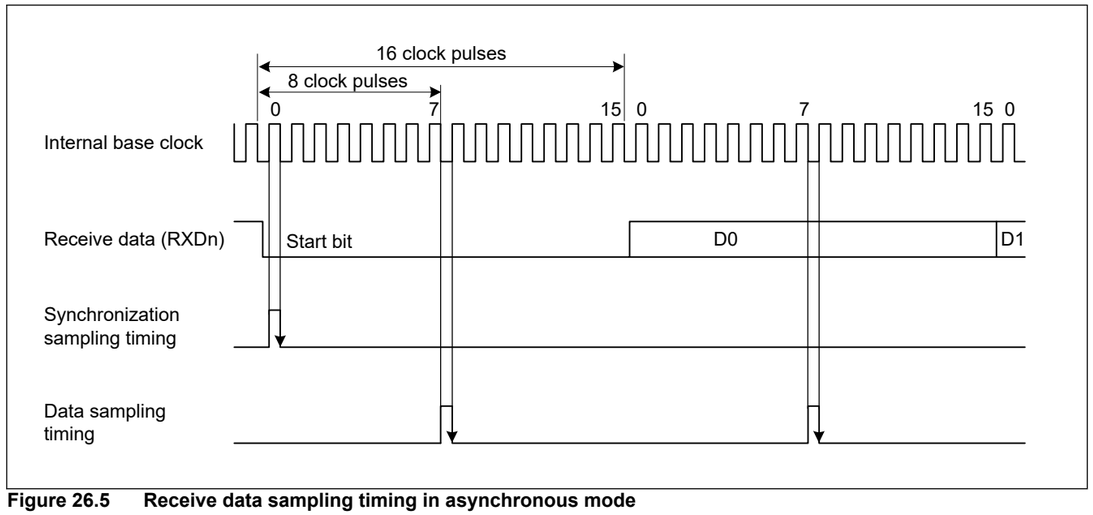


Figure 26.5 Receive data sampling timing in asynchronous mode

26.3.3 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input to the SCKn pin can be selected as the transfer clock of the SCI, based on the CCR3.CKE[1:0] settings.

When an external clock is input to the SCKn pin, the clock frequency must be 16 times the bit rate (when CCR2.ABCS = 0) or 8 times the bit rate (when CCR2.ABCS = 1).

When the SCI uses its internal clock, the clock can be output from the SCKn pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is configured so that the rising edge of the clock is in the middle of the transmit data, as shown in Figure 26.6.

When the internal clock is selected, the SCKn pin is outputted after setting the CCR0.TE or CCR0.RE bit to 1.

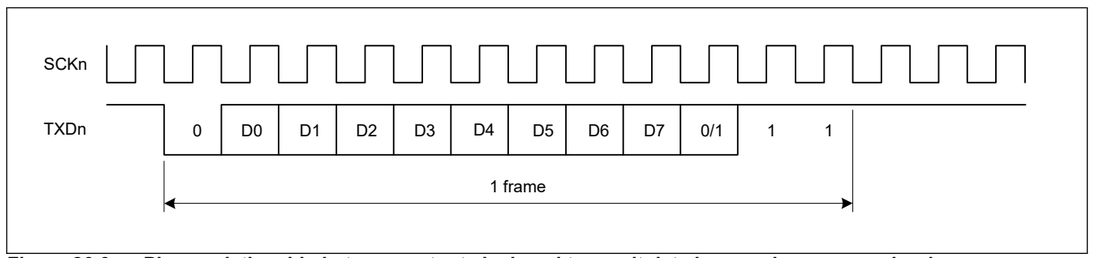


Figure 26.6 Phase relationship between output clock and transmit data in asynchronous mode when CCR1.PE = 1, CCR3.CHR[1:0] = 10b, MP = 0, and STP = 1

26.3.4 Double-Speed Operation and Frequency of 6 Times the Bit Rate

When the CCR2.ABCS bit is set to 1, the SCI operates on the bit rate twice that of when ABCS is set to 0. When the CCR2.BGDM bit is set to 1, the cycle of the base clock is half and the bit rate is double that of when BGDM is set to 0. When the CCR3.CKE[1] bit is set to 0 and the on-chip baud rate generator is selected, setting the ABCS and BGDM bits to 1 allows the SCI to operate at a bit rate four times that when the ABCS and BGDM bits are set to 0.

起始位的确定条件是超过半位长度的Low继续。与采样时间相同。在图26.5中，低电平周期应保持超过8个周期以检测起始位。如果Low周期未保持超过8个周期，则IP将其判断为噪声。因此，IP不开始接收并等待开始位。

调整采样定时功能开启（ASEN=1）：

起始位的确定条件是Low一直保持到采样定时。向前调整采样时序(AJD=1)会增加错误地将噪声确定为起始位的可能性。

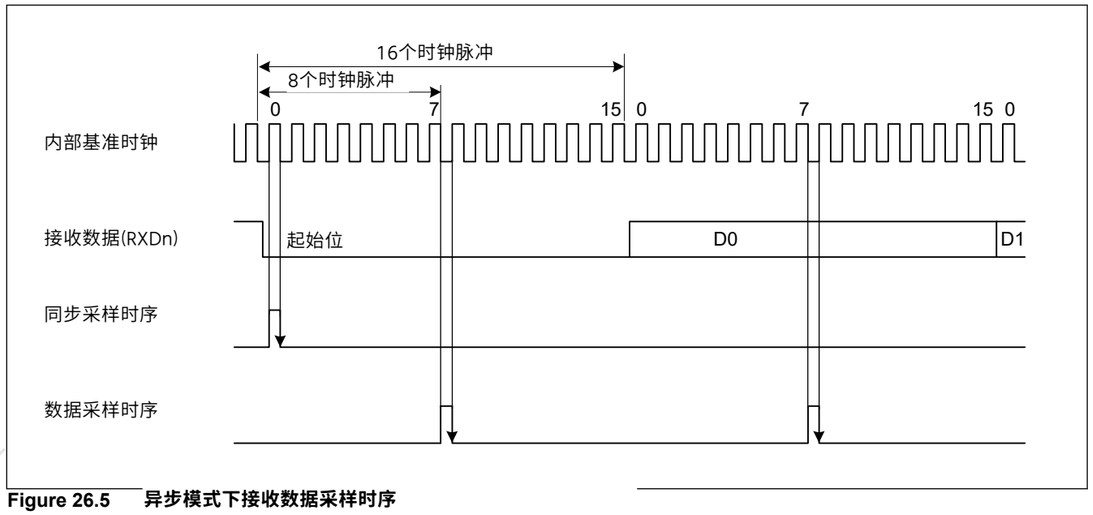


Figure 26.5 异步模式下接收数据采样时序

26.3.3 Clock

根据CCR3.CKE[1:0]的设置，可以选择片内波特率发生器产生的内部时钟或输入到SCKn引脚的外部时钟作为SCI的传输时钟。

当外部时钟输入到SCKn引脚时，时钟频率必须是比特率的16倍（当CCR2.ABCS=0时）或比特率的8倍（当CCR2.ABCS=1时）。

当SCI使用其内部时钟时，时钟可以从SCKn引脚输出。在这种情况下，时钟输出的频率等于比特率，并配置相位，使时钟的上升沿位于发送数据的中间，如图26.6所示。

选择内部时钟时，将CCR0.TE或CCR0.RE位设置为1后输出SCKn引脚。

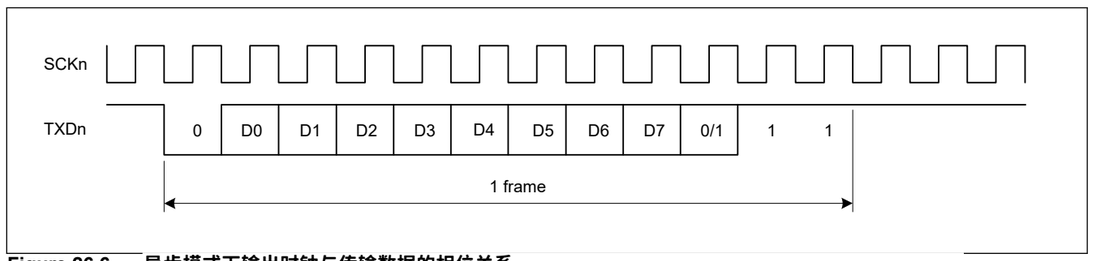


Figure 26.6 异步模式下输出时钟与传输数据的相位关系 CCR1.PE = 1, CCR3.CHR[1:0] = 10b, MP = 0, and STP = 1

26.3.4 双倍速操作和6倍比特率的频率

当CCR2.ABCS位设置为1时，SCI以两倍于ABCS设置为0时的比特率运行。当CCR2.BGDM位设置为1，基本时钟的周期是BGDM设置为0时的一半，比特率是两倍。
当CCR3.CKE[1]位设置为0并选择片内波特率发生器时，将ABCS和BGDM位设置为1允许SCI以四倍于ABCS和BGDM位时的比特率运行设置为0。

When the CCR2.ABCSE bit is set to 1, the number of base clock pulses is 6 during a period of 1 bit, and the base clock frequency is half and the SCI operates at a bit rate 16/3 times that when CCR2.ABCS = 0, CCR2.BGDM = 0, and CCR2.ABCSE = 0.

As shown by Formula (1) in section 26.3.2. Receive Data Sampling Timing and Reception Margin in Asynchronous Mode, the reception margin decreases when the CCR2.ABCS or CCR2.ABCSE bit is set to 1. Therefore, if the target bit rate can be obtained with ABCS or ABCSE set to 0, it is recommended that you use the SCI with ABCS and ABCSE set to 0.

26.3.5 CTS and RTS Functions

The CTS function controls transmission using the CTSn pin input. Setting the CCR1.CTSE bit to 1 enables the CTS function. For the functions of CTS and RTS, you can select the alternate setting to set CTSn_RTSn pin as a multiplexed pin that uses either function with one terminal or the dedicated setting that uses each function independently with two terminals at CTSn pin for CTSn signal and CTSn_RTSn pin for RTSn signal. This setting is done with the CCR1.CTSPEN bit.

When the CTS function is enabled, placing a low level on the CTSn_RTSn pin causes transmission to start.

If FIFO is used and CTSn_RTSn signal is held high before transmission, transmission will not start, so the number of TDR registers written, and the number of data stored are the same (unlike using clock synchronous FIFO).

Driving the CTSn_RTSn pin high while transmission is in progress does not affect transmission of the current frame.

In the RTS function, which uses output on the CTSn_RTSn pin, a low level is output when reception becomes possible. Conditions for output of the low and high levels are shown in this section.

[Conditions for low level output]

Satisfaction of all conditions are listed in this section.

Non-FIFO selected

- The value of the CCR0.RE bit is 1
- When the next reception is possible
  - There are no received data yet to be read and not receiving.
  - CSR.ORER, FER, PER flags are all 0

FIFO selected

- The value of the CCR0.RE bit is 1
- When the next reception is possible
  - When the quantity of receive data written in receive-FIFO(RDR) are less than the setting value of FCR.RSTRG[4:0]
  - CSR.ORER(RDR.ORER) is 0

[Condition for high level output]

- The conditions for low-level output are not satisfied

26.3.6 Address Match (Receive Data Match Detection) Function

The address match function can be used only in asynchronous mode.

If the CCR0.DCME bit is set to 1*2, when one frame of data is received, the SCI compares that received data with the data set in CCR4.CMPD. If the SCI detects a match to the comparison data (CCR4.CMPD*1) with the received data, the SCI can issue the SCIn_RXI interrupt request.

If the CCR3.MP bit is set to 0, comparison occurs only for valid data in receive format. In multi-processor mode (CCR3.MP bit = 1), if the CCR0.IDSEL bit is set to 1, receive data where the MPB bit is 1 is subject to comparison for address match and receive data where the MPB bit is 0 is always treated as a non-match.

If the CCR0.IDSEL bit is set to 0, SCI performs address match detection regardless of the MPB bit value of the received data.

Until SCI detects a match to the comparison data (CCR4.CMPD*1) with receive data, received data is skipped (discarded), and the SCI cannot detect a parity error or framing error.

当CCR2.ABCSE位设置为1时，在1位周期内基本时钟脉冲数为6，基本时钟频率为一半，SCI以16比特率运行，是CCR2.ABCS=时的3倍0，CCR2.BGDM=0，CCR2.ABCSE=0。

如第26.3.2节中的公式（1）所示。异步模式下的接收数据采样时序和接收裕度，当CCR2.ABCS或CCR2.ABCSE位设置为1时，接收裕度减小。因此，如果ABCS或ABCSE设置为0即可获得目标码率，则为建议您使用SCI，ABCS和ABCSE设置为0。

26.3.5 CTS和RTS函数

CTS功能使用CTSn引脚输入控制传输。将CCR1.CTSE位设置为1可启用CTS功能。对于CTS和RTS的功能，您可以选择交替设置，将CTSn_RTSn管脚设置为一个多路复用管脚，使用一个端子的功能或独立使用每个功能的专用设置，在CTSn管脚上为CTSn信号和CTSn_RTSn管脚提供两个端子对于RTSn信号。此设置通过CCR1.CTSPEN位完成。

当CTS功能使能时，将CTSn_RTSn引脚置于低电平会导致传输开始。

如果使用FIFO且CTSn_RTSn信号在发送前保持高电平，则不会开始发送，因此写入的TDR寄存器数量和存储的数据数量相同（与使用时钟同步FIFO不同）。

在传输过程中将CTSn_RTSn引脚驱动为高电平不会影响当前帧的传输。

在使用CTSn_RTSn引脚输出的RTS功能中，当可以接收时输出低电平。
本节显示了低电平和高电平的输出条件。

【低电平输出的条件】

本节列出了所有条件的满足情况。

Non-FIFO selected

●CCR0.RE位的值为1

●下次可以接收时

没有接收到的数据尚未读取且未接收。

CSR.ORER、FER、PER标志均为0

FIFO selected

●CCR0.RE位的值为1

●下次可以接收时

当写入receive-FIFO(RDR)的接收数据量小于FCR.RSTRG[4:0]的设定值时

- CSR.ORER(RDR.ORER) is 0

【高电平输出条件】

●不满足低电平输出条件

26.3.6 地址匹配（接收数据匹配检测）功能

地址匹配功能只能在异步模式下使用。

如果CCR0.DCME位设置为1*2，当接收到一帧数据时，SCI会将接收到的数据与CCR4.CMPD中设置的数据进行比较。如果SCI检测到比较数据(CCR4.CMPD*1)与接收到的数据匹配，则SCI可以发出SCIn_RXI中断请求。

如果CCR3.MP位设置为0，则仅对接收格式的有效数据进行比较。在多处理器模式下（CCR3.MP位=1），如果CCR0.IDSEL位设置为1，则接收MPB位为1的数据进行地址匹配比较，接收MPB位为0的数据始终被视为不匹配。

如果CCR0.IDSEL位设置为0，SCI执行地址匹配检测，而不管接收数据的MPB位值。

在SCI检测到与接收数据的比较数据(CCR4.CMPD*1)匹配之前，将跳过（丢弃）接收到的数据，并且SCI无法检测奇偶校验错误或帧错误。

When SCI detects a match, the CCR0.DCME bit is automatically cleared, and the CSR.DCMF flag is set to 1. If the CCR0.IDSEL bit is set to 1, the CCR0.MPIE bit is automatically cleared. If CCR0.IDSEL is set to 0, the value of the CCR0.MPIE bit is retained. If the CCR0.RIE bit is set to 1, the SCI issues an SCIn_RXI interrupt request.

If the SCI detects a framing error in the receive data for which a match is detected, the CSR.DFER flag is set to 1, and if the SCI detects a parity error in that frame, the CSR.DPER flag is set to 1. The compared receive data and MPB bit is not stored in the RDR register, and CSR.RDRF remains 0.

After the SCI detects a match, and CCR0.DCME is automatically cleared, the SCI receives the next data continuously based on the current register setting.

When the CSR.DFER or CSR.DPER flag is set, the address match is not performed. Before enabling the address match function, set the DCCR.DFER and DCCR.DPER flags to 0.

Examples of the address match function are shown in Figure 26.7 and Figure 26.8.

Note 1. This comparative target can select one length of 3 types: CMPD[6:0] with 7-bit length, CMPD[7:0] with 8-bit length, and CMPD[8:0] with 9-bit length.

Note 2. Set the CCR0.DCME bit to 1 before receiving the start bit of the received frame that performs address matching.

当SCI检测到匹配时，CCR0.DCME位自动清零，CSR.DCMF标志位设置为1。如果CCR0.IDSEL位设置为1，CCR0.MPIE位自动清零。如果CCR0.IDSEL设置为0，则

CCR0.MPIE位被保留。如果CCR0.RIE位设置为1，则SCI发出SCIn_RXI中断请求。

如果SCI在检测到匹配的接收数据中检测到帧错误，则CSR.DFER标志设置为1，如果SCI在该帧中检测到奇偶校验错误，则CSR.DPER标志设置为1。比较的接收数据和MPB位不存储在RDR寄存器中，CSR.RDRF保持为0。

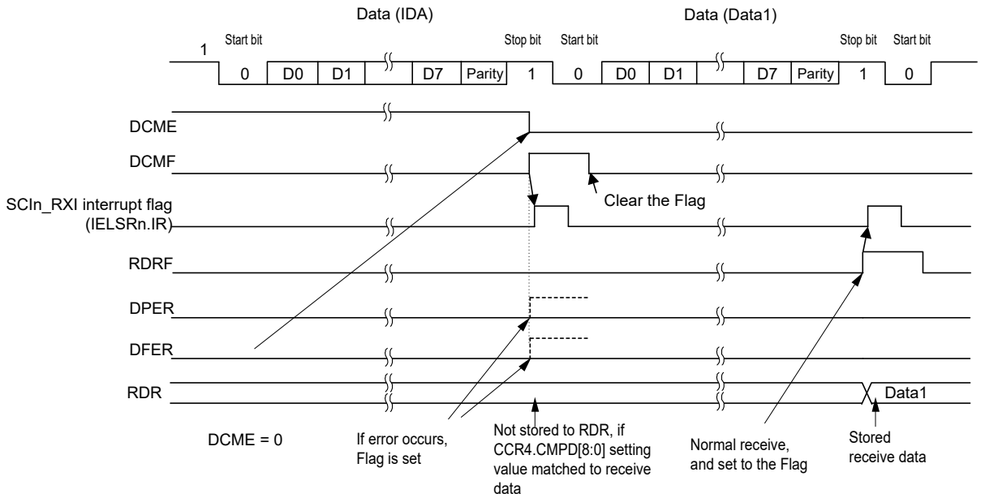
SCI检测到匹配后，CCR0.DCME自动清零，SCI根据当前寄存器设置连续接收下一个数据。

当设置CSR.DFER或CSR.DPER标志时，不执行地址匹配。在启用地址匹配功能之前，将DCCR.DFER和DCCR.DPER标志设置为0。

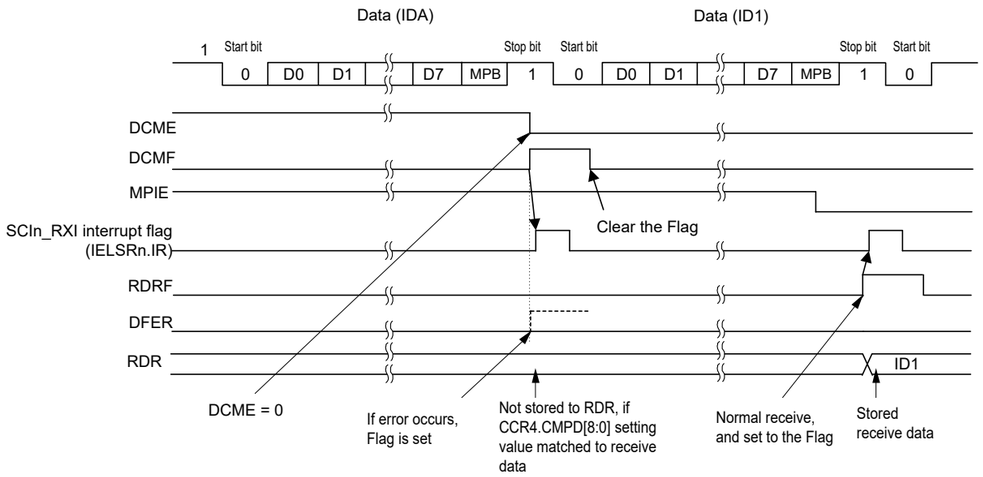
地址匹配函数的例子如图26.7和图26.8所示。

注1.此比较目标可以选择3种长度中的一种：7位长度的CMPD[6:0]、8位长度的CMPD[7:0]和9位长度的CMPD[8:0].

注2.在接收到执行地址匹配的接收帧的起始位之前，将CCR0.DCME位设置为1。

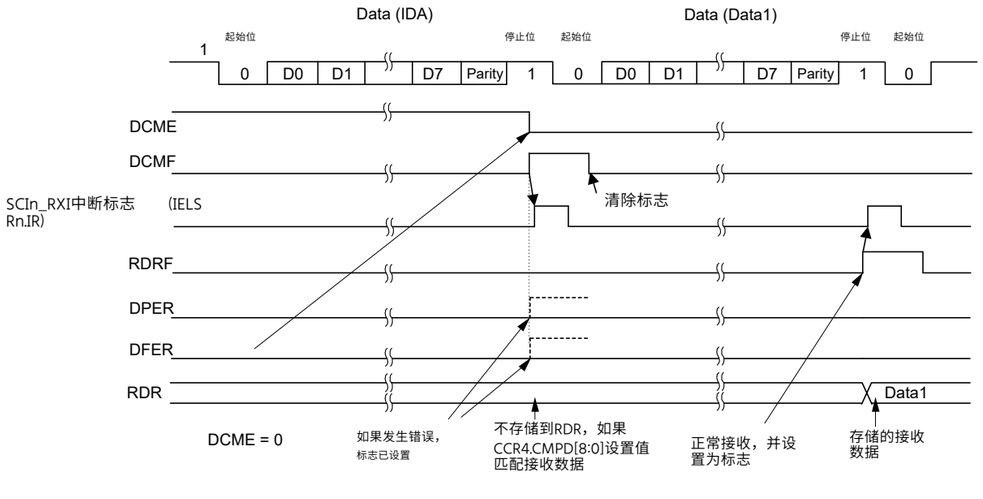


(a) Example of Compare matched between receive data and CCR4.CMPD[8:0] (8bit length/parity/Normal mode)

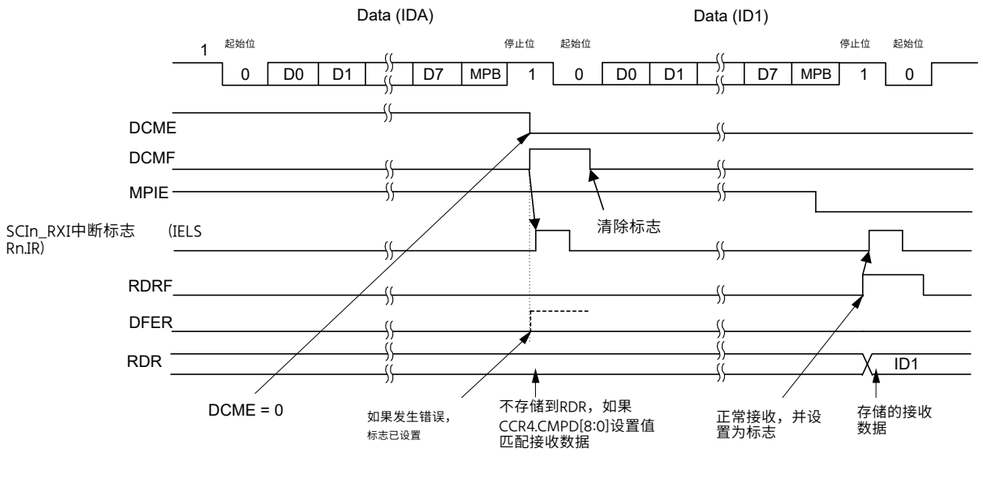


(b) Example of Compare matched between receive data and CCR4.CMPD[8:0] (8bit length/Multi-processor mode)

Figure 26.7 Example of address match (1) normal mode

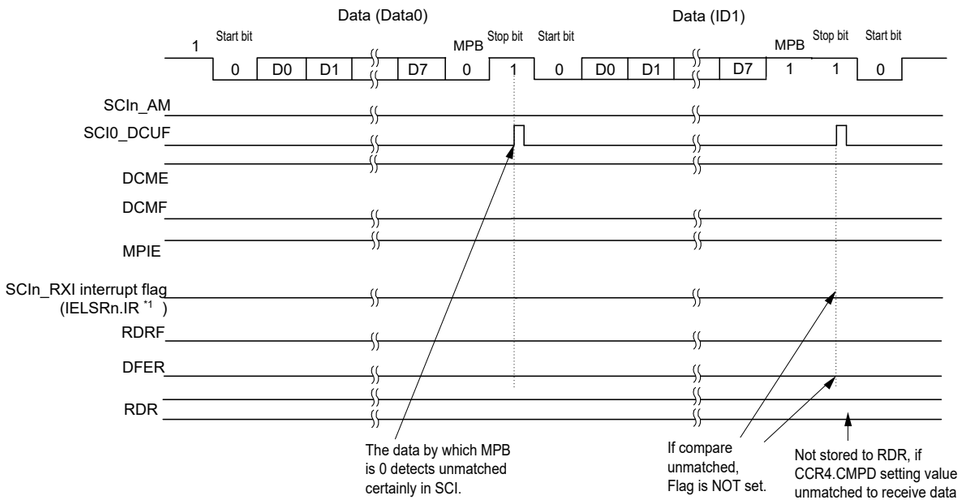


(a)接收数据和CCR4.CMPD[8:0]之间的比较匹配示例（8位长度奇偶校验正常模式）

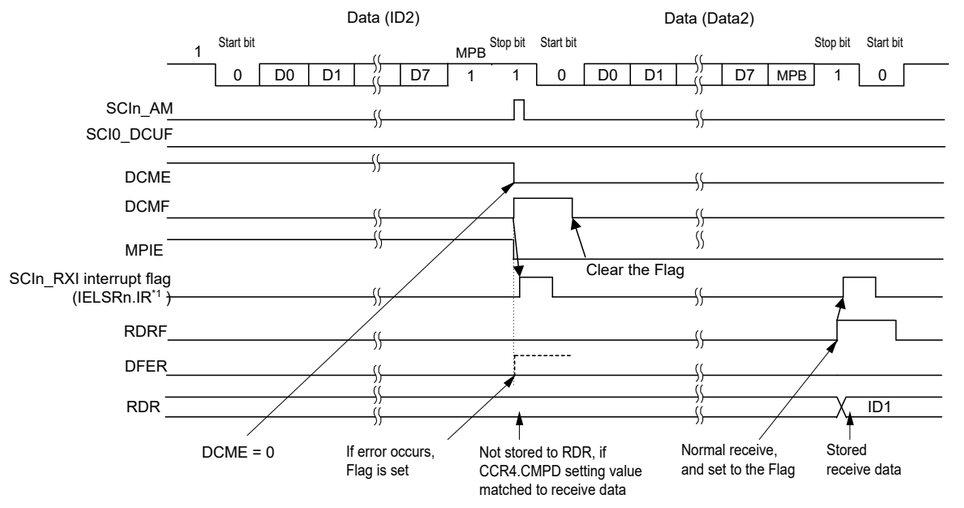


(b)接收数据与CCR4.CMPD[8:0]的比较匹配示例（8位长度多处理器模式）

Figure 26.7 地址匹配示例（一）普通模式



(a) Example of Compare unmatched between receive data and CCR4.CMPD (8bit length/IDSEL = 1/Multi-processor mode)



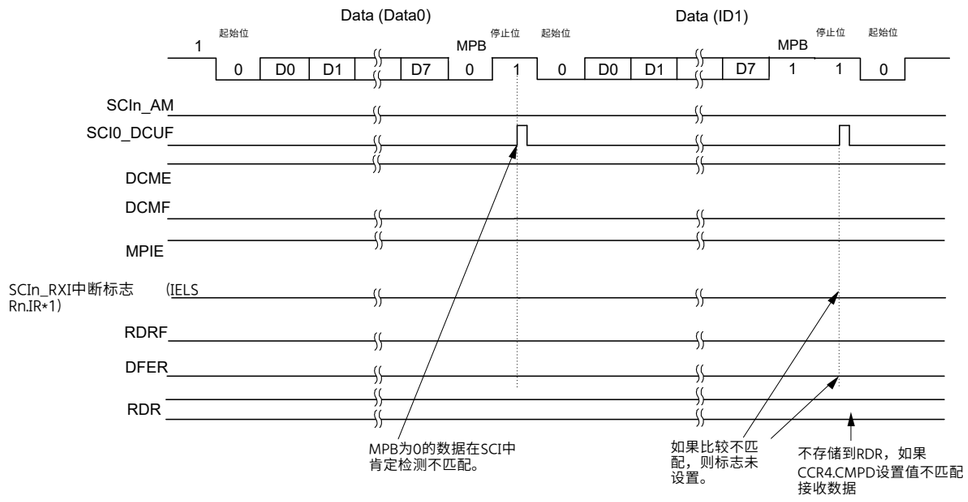
(b) Example of Compare matched between receive data and CCR4.CMPD (8bit length/IDSEL = 1/Multi-processor mode)

Figure 26.8 Example of address match (2) multi-processor mode

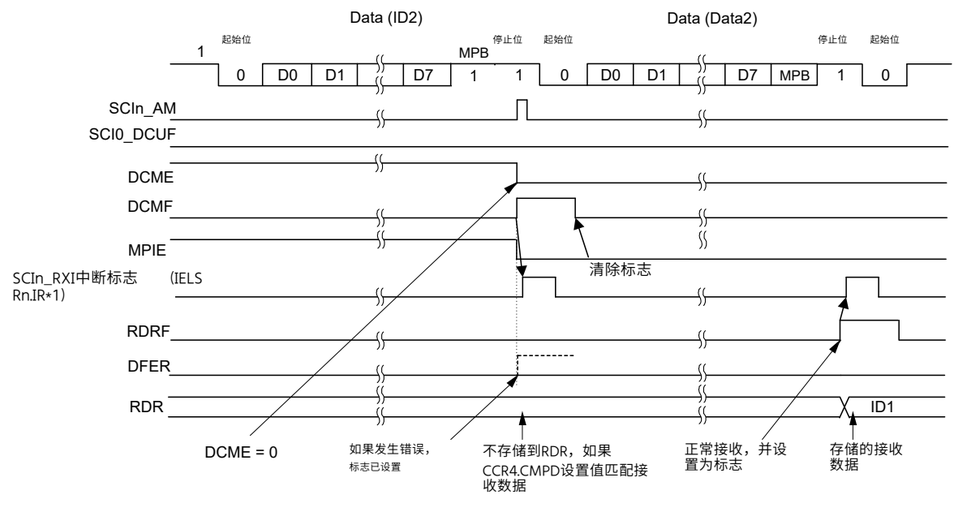
26.3.7 SCI Initialization in Asynchronous Mode

Before transmitting and receiving data, start by writing the initial value 0 to the CCR0.TE and CCR0.RE (or writing the initial value to CCR0), then continue through the SCI initialization procedure (select non-FIFO or FIFO) shown in Table 26.26 and Table 26.27. Whenever the operating mode or transfer format is to be changed, the CCR0.TE and CCR0.RE bits must be initialized before the change is made.

When the external clock is used in asynchronous mode, ensure that the clock signal is supplied during initialization.



(a)接收数据与CCR4.CMPD比较不匹配示例（8位长度IDSEL=1多处理器模式）



(b)接收数据和CCR4.CMPD之间的比较匹配示例（8位长度IDSEL=1多处理器模式）

Figure 26.8 地址匹配示例（二）多处理器模式

26.3.7 异步模式下的SCI初始化

在发送和接收数据之前，首先将初始值0写入CCR0.TE和CCR0.RE（或将初始值写入CCR0），然后继续执行表中所示的SCI初始化程序（选择非FIFO或FIFO）26.26和表26.27。每当要更改操作模式或传输格式时，必须在更改之前初始化CCR0.TE和CCR0.RE位。

在异步模式下使用外部时钟时，请确保在初始化期间提供时钟信号。

Note: Setting the CCR0.RE bit to 0 initializes neither the ORER, FER, RDRF, RDAT, PER, and DR flags in CSR nor RDR. When FIFO selected, even if the TE bit is set as 0, the TEND flag for the selected FIFO buffer is not initialized.

Please be also careful at the time of change in the operation mode.

Note: Switching the value of the CCR0.TE bit from 0 to 1 while the CCR0.TIE bit is 1 leads to the generation of an SCIn_TXI interrupt request.

Table 26.26 Example flow of SCI initialization in asynchronous mode with non-FIFO selected

No.	Step Name	Description
1	Start initialization	—
2	Set CCR0	Set CCR0.TEIE, TIE, RIE, TE, RE to 0. If you have not changed from the initial settings, you can skip this step.
3	Set CCR3	Set up following function and communication mode. Driver control function for RS-485, FIFO no-use, Multi-Processor mode, Communication mode (MOD[2:0] = 000b) Transmission / reception format Clock enable (Leave the initial value when outputting the clock) Leave unused bits at their initial values.
4	Set CCR2	Set up the bit-rate-modulation function*1 *2, select clock, set bit rate*2
5	Set CCR1	Set up the Noise-filter function, the loop-back function, communication terminal status, the parity check function, and the CTSn_RTSn function.
6	Set CCR4	Set up the adjust sampling timing function and the adjust transmit timing function.
7	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
8	Set CCR3	Set clock enable bit (CKE[1:0]) at this step when outputting the clock. After this register setting, the clock pin will be in the output state immediately.
9	Set CFCLR	Write 1 to the following bits and clear the corresponding flag. CFCLR.RDRFC,FERC,PERC,MFFC,ORERC,DFERC,DPERC,DCMFC,ERSC If it's initialization flow after a reset, you can skip this step.
10	Set CCR0	Set the TE or RE bit to 1. To enable interrupts, set the TE bit and TIE bit, and the RE bit and RIE bit to 1 with one instruction at the same time. Setting the TE and RE bits allows TXDn and RXDn to be used.
11	Initialization completed	—

Note 1. If you do not use the bit rate modulation function, you do not need to set it.
Note 2. If you use an external clock, you do not need to set it.

Table 26.27 Example flow of SCI initialization in asynchronous mode with FIFO selected (1 of 2)

No.	Step Name	Description
1	Start initialization	—
2	Set CCR0	Set CCR0.TEIE, TIE, RIE, TE, RE to 0. If you have not changed from the initial settings, you can skip this step.
3	Set CCR3	Set up following function and communication mode. Driver control function for RS-485, FIFO use, Multi-Processor mode, Communication mode (MOD[2:0] = 000b) Transmission / reception format Clock enable (Leave the initial value when outputting the clock) Leave unused bits at their initial values.
4	Set CCR2	Set up the bit-rate-modulation function*1 *2, select clock, set bit rate*2
5	Set CCR1	Set up the Noise-filter function, the loop-back function, communication terminal status, the parity check function, and the CTSn_RTSn function.
6	Set CCR4	Set up the adjust sampling timing function and the adjust transmit timing function.
7	Set FCR	Set the TFRST and RFRST to 1 to empty FIFO. Set the DRES, TTRG[4:0], RTRG[4:0], and RSTRG[4:0] bits
8	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.

Note: 将CCR0.RE位设置为0不会初始化CSR和RDR中的ORER、FER、RDRF、RDAT、PER和DR标志。选择FIFO时，即使TE位设置为0，所选FIFO缓冲区的TEND标志也不会初始化。

在改变操作模式时也请小心。

Note: 当CCR0.TIE位为1时，将CCR0.TE位的值从0切换到1会导致生成SCIn_TXI中断请求。

Table 26.26 选择非FIFO的异步模式下SCI初始化示例流程

No.	步骤名称	Description
1	开始初始化	—
2	Set CCR0	将CCR0.TEIE、TIE、RIE、TE、RE设置为0。如果未更改初始设置，则可以跳过此步骤。
3	Set CCR3	设置跟随功能和通讯方式。 RS-485驱动控制功能，不使用FIFO，多处理器模式，通信模式(MOD[2:0]=000b)发送接收格式 时钟使能（输出时钟时保留初始值） 将未使用的位保留为其初始值。
4	Set CCR2	设置比特率调制功能*1*2，选择时钟，设置比特率*2
5	Set CCR1	设置Noise-filter功能、loop-back功能、通信终端状态、奇偶校验功能和CTSn_RTSn功能。
6	Set CCR4	设置调整采样定时功能和调整发送定时功能。
7	设置IO端口功能	进行IO端口设置以启用TXDn、RXDn和所需的输入和输出功能 SCKn pins.
8	Set CCR3	输出时钟时在此步骤设置时钟使能位（CKE[1:0]）。此寄存器设置后，时钟引脚将立即处于输出状态。
9	Set CFCLR	将1写入以下位并清除相应的标志。 CFCLR.RDRFC FERC PERC MFFC ORERC DFERC DPERC DCMFC ERSC如果是reset后的初始化流程，可以跳过这一步。
10	Set CCR0	将TE或RE位设置为1。要使能中断，请同时将TE位和TIE位以及RE位和RIE位设置为1，同时使用一条指令。设置TE和RE位允许使用TXDn和RXDn。
11	初始化完成	—

注1.如果不使用码率调制功能，则无需设置。
注2.如果使用外部时钟，则无需设置。

Table 26.27 选择FIFO的异步模式下SCI初始化示例流程（1of2）

No.	步骤名称	Description
1	开始初始化	—
2	Set CCR0	将CCR0.TEIE、TIE、RIE、TE、RE设置为0。如果未更改初始设置，则可以跳过此步骤。
3	Set CCR3	设置跟随功能和通讯方式。 RS-485驱动控制功能、FIFO使用、多处理器模式、通信模式(MOD[2:0]=000b)发送接收格式 时钟使能（输出时钟时保留初始值） 将未使用的位保留为其初始值。
4	Set CCR2	设置比特率调制功能*1*2，选择时钟，设置比特率*2
5	Set CCR1	设置Noise-filter功能、loop-back功能、通信终端状态、奇偶校验功能和CTSn_RTSn功能。
6	Set CCR4	设置调整采样定时功能和调整发送定时功能。
7	Set FCR	将TFRST和RFRST设置为1以清空FIFO。设置DRES、TTRG[4:0]、RTRG[4:0]和 RSTRG[4:0] bits
8	设置IO端口功能	进行IO端口设置以启用TXDn、RXDn和所需的输入和输出功能 SCKn pins.

Table 26.27 Example flow of SCI initialization in asynchronous mode with FIFO selected (2 of 2)

No.	Step Name	Description
9	Set CCR3	If you select a clock output in asynchronous mode, set the CKE[1:0] bit here. After setting the register, the clock pin will be in the output state immediately. But the clock operates after setting TE or RE to 1.
10	Set CFCLR	Write 1 to the following bits and clear the corresponding flag. CFCLR.RDRFC, FERC, PERC, MFFC, ORERC, DFERC, DPERC, DCMFC, ERSC If it's initialization flow after a reset, you can skip this step.
11	Set FFCLR	Write 1 to The FFCLR.BRKC,DRC and clear the corresponding flag. If it's initialization flow after a reset, you can skip this step.
12	Set CCR0	Set the TE or RE bit to 1. To enable interrupts, set the TE bit and TIE bit, and the RE bit and RIE bit to 1 with one instruction at the same time. Setting the TE and RE bits allows TXDn and RXDn to be used.
13	Initialization completed	—

Note 1. If you do not use the bit rate modulation function, you do not need to set it.
Note 2. If you use an external clock, you do not need to set it.

Figure 26.9 shows an example of the timing when data is transmitted after reset is released, and SCI is set to asynchronous mode according to Table 26.26 or Table 26.27. As shown in the figure, when the pin function is set to the TXDn pin, the CCR0.TE bit is 0, so the pin is high impedance. When transmit data is written after setting the CCR0.TE bit to 1, data transmission starts. There is a transmission wait time from writing TDR to data transmission starts. In asynchronous mode, TXDn is high during this period.

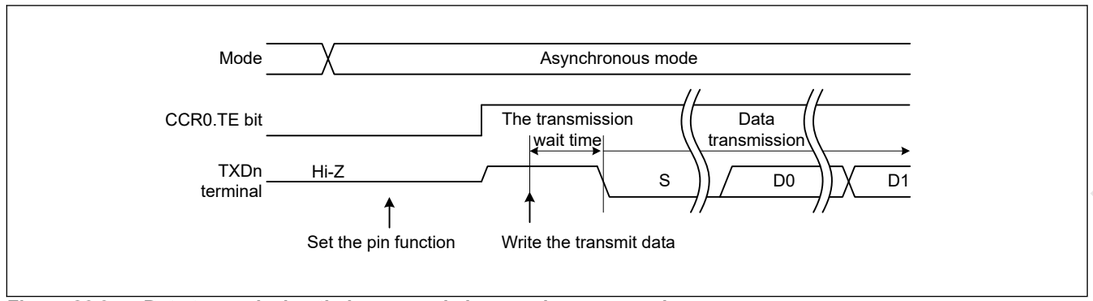


Figure 26.9 Data transmission timing example in asynchronous mode

26.3.8 Serial Data Transmission in Asynchronous Mode

(1) Non-FIFO selected

Figure 26.10, Figure 26.11, Figure 26.12 and Figure 26.13 show examples of serial transmission in asynchronous mode.

In serial transmission, the SCI operates as described in this section.

1. The SCI transfers data from the TDR register to the TSR register when data is written to TDR in the SCIn_TXI interrupt handling routine.
   The SCIn_TXI interrupt request at the beginning of transmission is generated when the CCR0.TE and CCR0.TIE bits are set to 1 simultaneously by a single instruction.
2. Transmission starts after the CCR1.CTSE bit is set to 0 (CTS function is disabled) or a low level on the CTSn_RTSn pin causes data transfer from the TDR register to the TSR register. If the CCR0.TIE bit is 1, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to the TDR register in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set the CCR0.TIE bit to 0 (SCIn_TXI interrupt requests are disabled) and the CCR0.TEIE bit to 1 (an SCIn_TEI interrupt request is enabled) after the last of the data to be transmitted is written to the TDR register from the handling routine for SCIn_TXI requests.
3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data

Table 26.27 选择FIFO的异步模式下SCI初始化示例流程（2个中的2个）

No.	步骤名称	Description
9	Set CCR3	如果选择异步模式下的时钟输出，请在此处设置CKE[1:0]位。设置寄存器后，时钟管脚将立即处于输出状态。但时钟在将TE或RE设置为1后运行。
10	Set CFCLR	将1写入以下位并清除相应的标志。CFCLR.RDRFC、FERC、PERC、MFFC ORERC DFERC DPERC DCMFC ERSC如果是复位后的初始化流程，可以跳过这一步。
11	Set FFCLR	将1写入FFCLR.BRKC DRC并清除相应标志。如果是reset后的初始化流程，可以跳过这一步。
12	Set CCR0	将TE或RE位设置为1。要使能中断，请同时将TE位和TIE位以及RE位和RIE位设置为1，同时使用一条指令。设置TE和RE位允许使用TXDn和RXDn。
13	初始化完成	—

注1.如果不使用码率调制功能，则无需设置。
注2.如果使用外部时钟，则无需设置。

图26.9显示了复位释放后发送数据的时序示例，根据表26.26或表26.27将SCI设置为异步模式。如图所示，当引脚功能设置为TXDn引脚时，CCR0.TE位为0，因此引脚为高阻态。将CCR0.TE位设置为1后写入发送数据时，数据发送开始。从写入TDR到数据传输开始有一个传输等待时间。在异步模式下，TXDn在此期间为高电平。

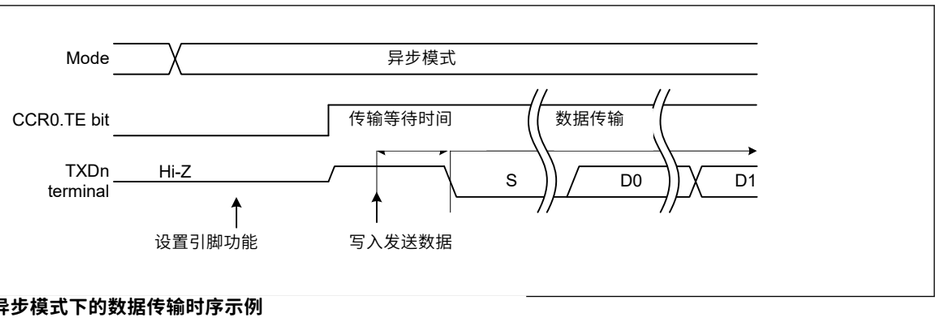


Figure 26.9 异步模式下的数据传输时序示例

26.3.8 异步模式下的串行数据传输

(1)选择非FIFO图26.10、图26.11、图26.12和图26.13显示了异步模式下的串行传输示例。

在串行传输中，SCI的操作如本节所述。

1.当数据在SCIn_TXI中断处理程序中写入TDR时，SCI将数据从TDR寄存器传输到TSR寄存器。当CCR0.TE和CCR0.TIE位通过一条指令同时设置为1时，会在传输开始时产生SCIn_TXI中断请求。

2.CCR1.CTSE位设置为0（禁用CTS功能）或CTSn_RTSn引脚上的低电平导致数据从TDR寄存器传输到TSR寄存器后开始传输。如果CCR0.TIE位为1，则产生SCIn_TXI中断请求。通过在当前发送数据发送完成之前将下一个发送数据写入SCIn_TXI中断处理程序中的TDR寄存器，可以实现连续发送。使用SCIn_TEI中断请求时，在写入要发送的最后一个数据后，将CCR0.TIE位设置为0（禁止SCIn_TXI中断请求）并将CCR0.TEIE位设置为1（启用SCIn_TEI中断请求）从SCIn_TXI请求的处理例程到TDR寄存器。

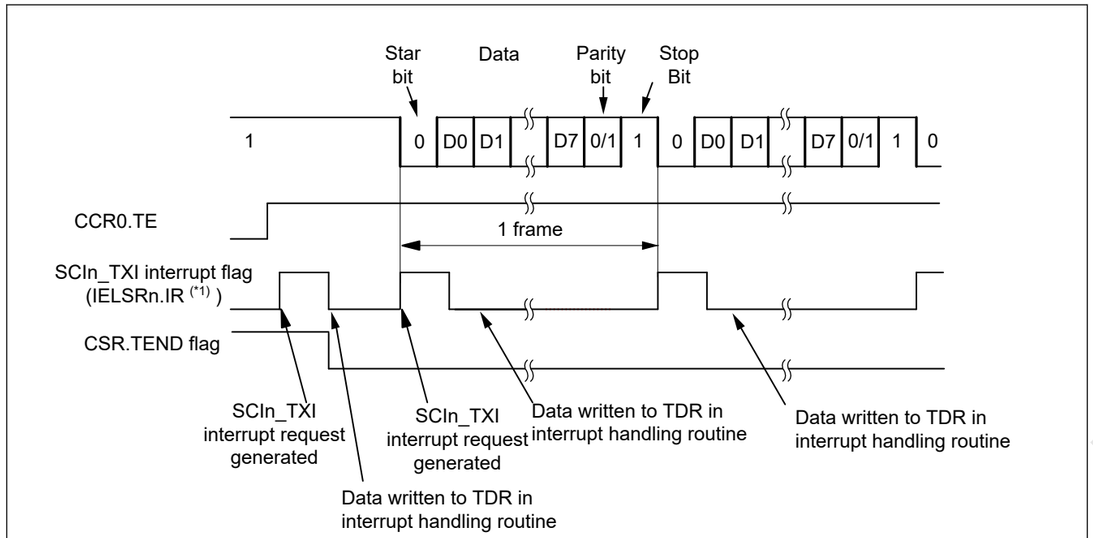
3.数据按以下顺序从TXDn引脚发送：

- 起始位
- 传输数据

- Parity bit or multi-processor bit (can be omitted depending on the format)
- Stop bit

4. The SCI checks for update of the TDR register on output of the stop bit.
5. When the TDR register is updated, setting the CCR1.CTSE bit to 0 (CTS function is disabled) or a low level input on the CTSn_RTSn pin causes transfer of the next transmit data from the TDR register to the TSR register and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If the TDR register is not updated, the CSR.TEND flag is set to 1, the stop bit is sent, and the mark state is entered, in which 1 is output. If the CCR0.TEIE bit is 1, the CSR.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated.

Figure 26.10, Figure 26.11, Figure 26.12 and Figure 26.13 show examples of serial transmission in asynchronous mode.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.10 Example operation for serial transmission in asynchronous mode (1) with 8-bit data, parity bit, 1 stop bit, CTS function not used, and at the beginning of transmission

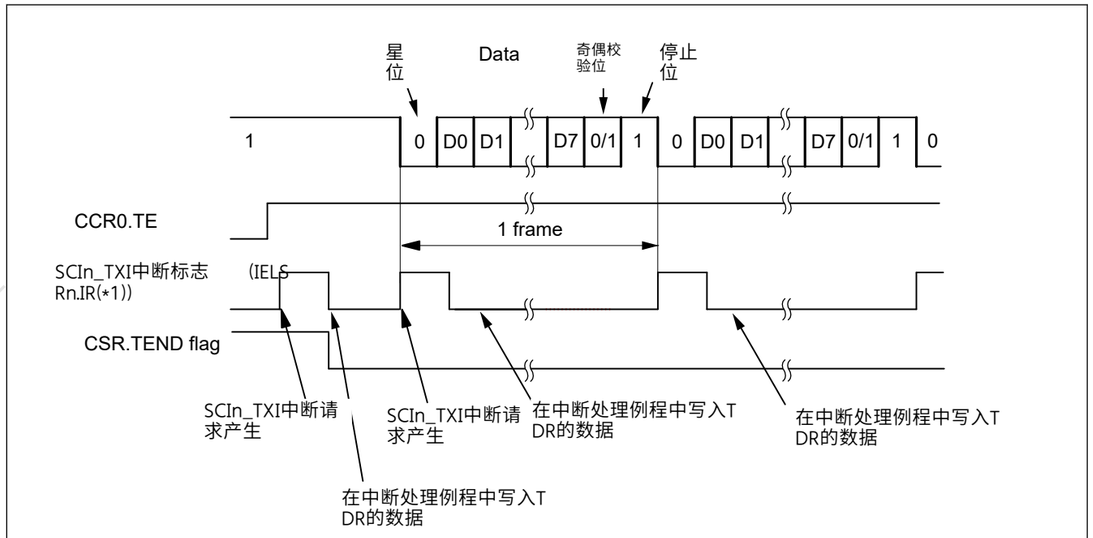
●奇偶校验位或多处理器位（可根据格式省略）
●停止位

4.SCI在停止位输出时检查TDR寄存器的更新。

5.当TDR寄存器更新时，设置CCR1.CTSE位为0（CTS功能被禁用）或低电平输入开启CTSn_RTSn引脚导致下一个发送数据从TDR寄存器传输到TSR寄存器并传输停止位，然后开始下一帧的串行传输。

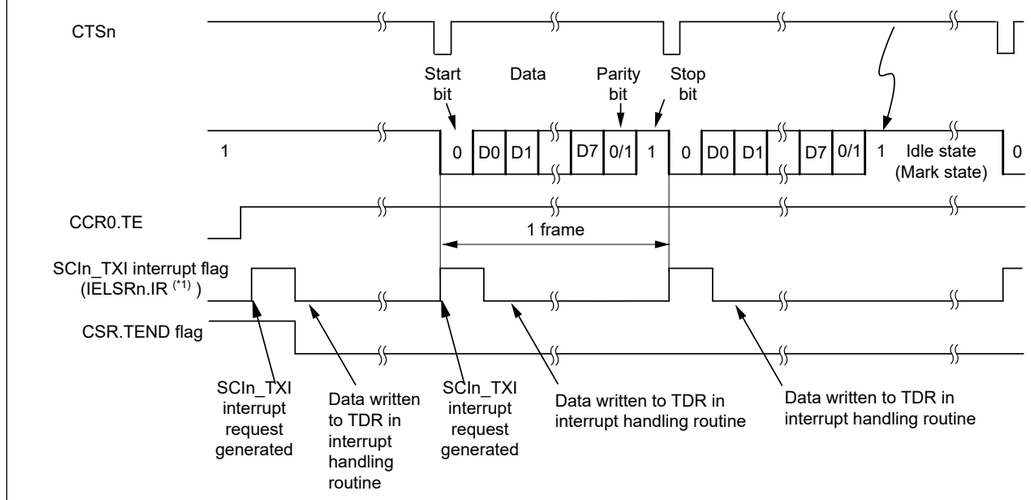
6、如果TDR寄存器没有更新，则CSR.TEND标志置1，发送停止位，进入标记状态，其中输出1。如果CCR0.TEIE位为1，则CSR.TEND标志设置为1，并产生SCIn_TEI中断请求。

图26.10、图26.11、图26.12和图26.13显示了异步模式下的串行传输示例。



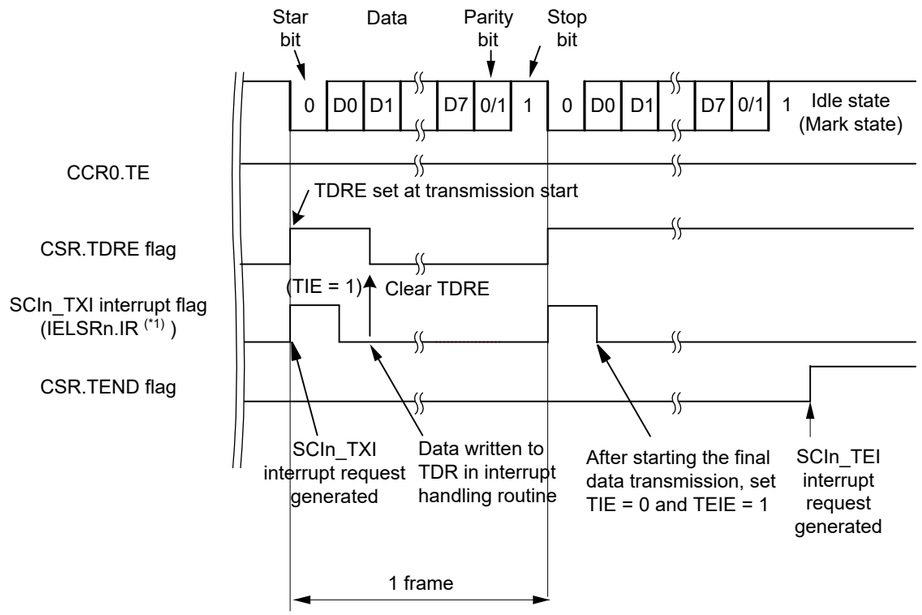
注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.10 异步模式下串行传输的示例操作(1)使用8位数据、奇偶校验位、1个停止位、未使用CTS功能以及传输开始时



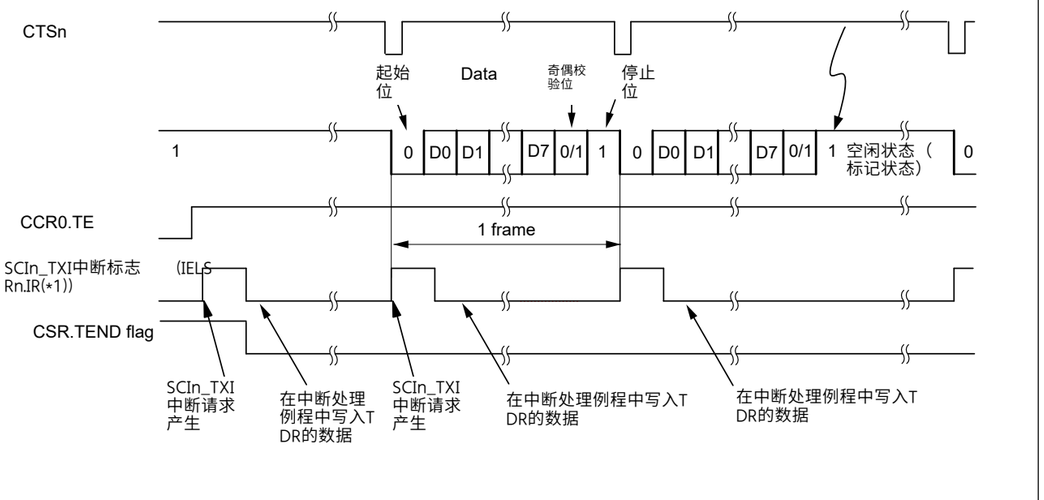
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.11 Example operation for serial transmission in asynchronous mode (2) with 8-bit data, parity bit, one stop bit, CTS function used, and at the beginning of transmission



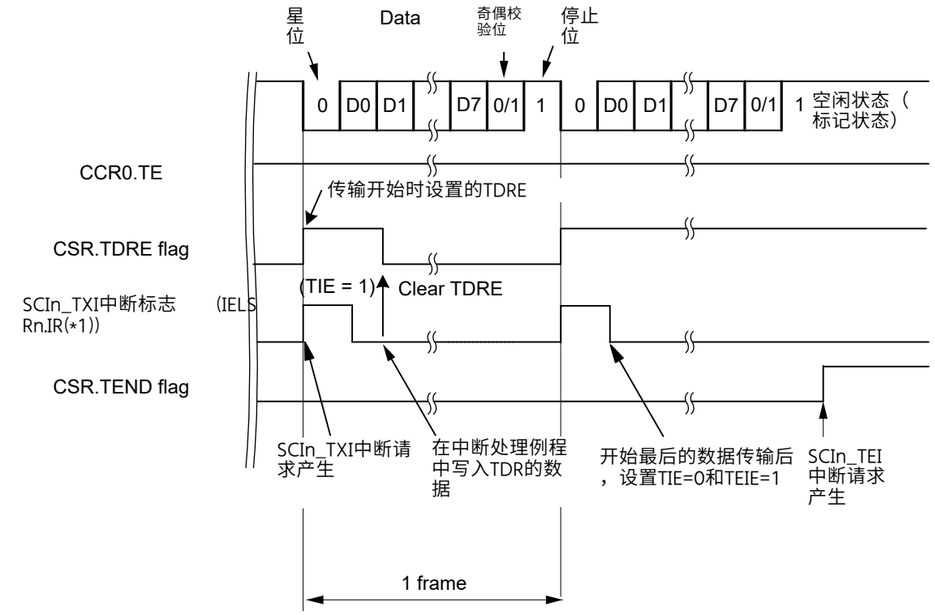
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.12 Example operation for serial transmission in asynchronous mode (3) with 8-bit data, parity bit, one stop bit, CTS function not used, and from the middle of transmission until transmission completion



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.11 异步模式下串行传输的示例操作(2)使用8位数据、奇偶校验位、一个停止位、使用CTS功能以及在传输开始时



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.12 异步模式下串行传输的示例操作(3)使用8位数据、奇偶校验位、一个停止位、未使用CTS功能，以及从传输中间到传输完成

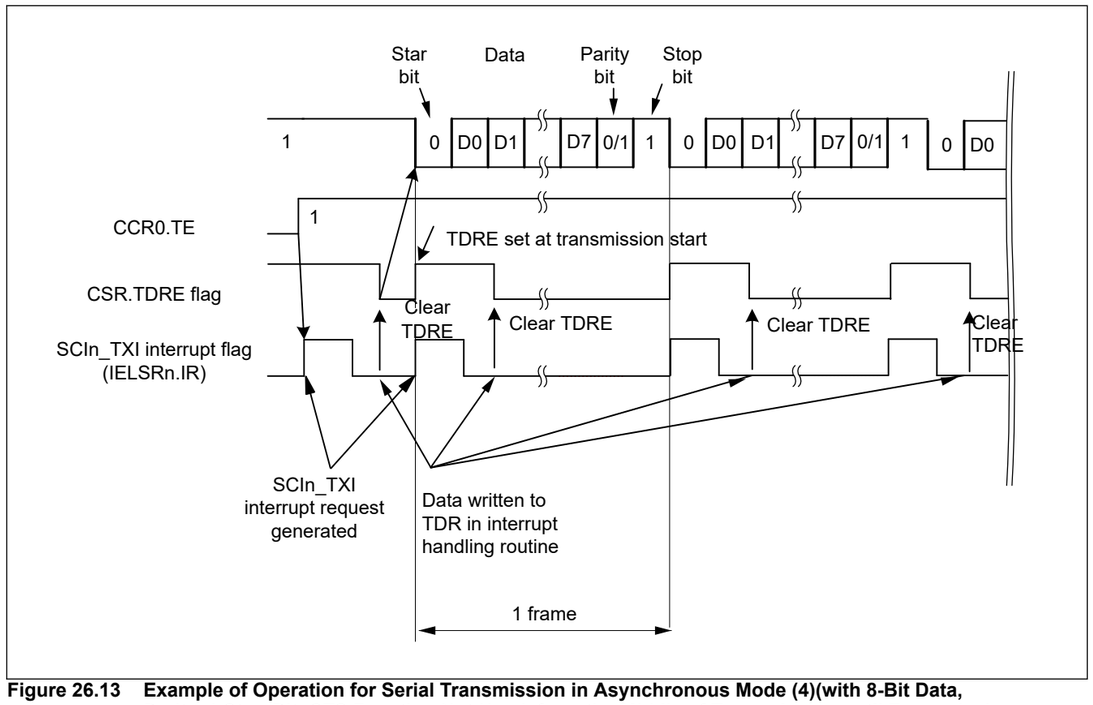


Figure 26.13 Example of Operation for Serial Transmission in Asynchronous Mode (4)(with 8-Bit Data, Parity, 1 Stop Bit, CTS Function Not Used, from the Middle of Transmission until Transmission Completion)

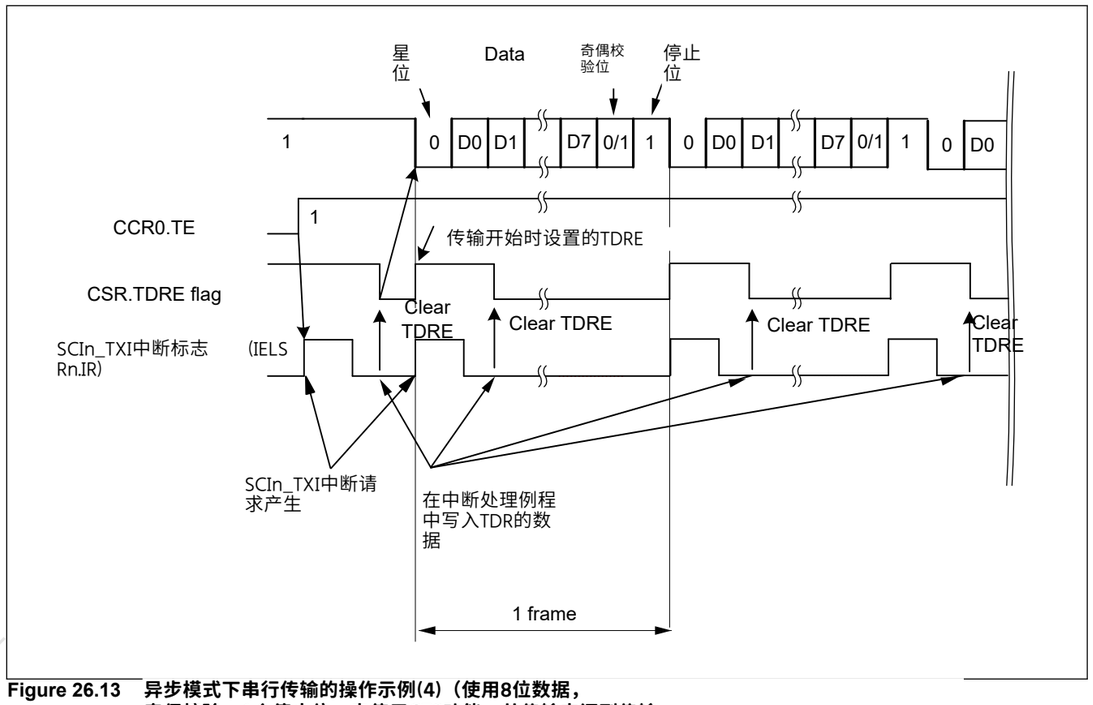
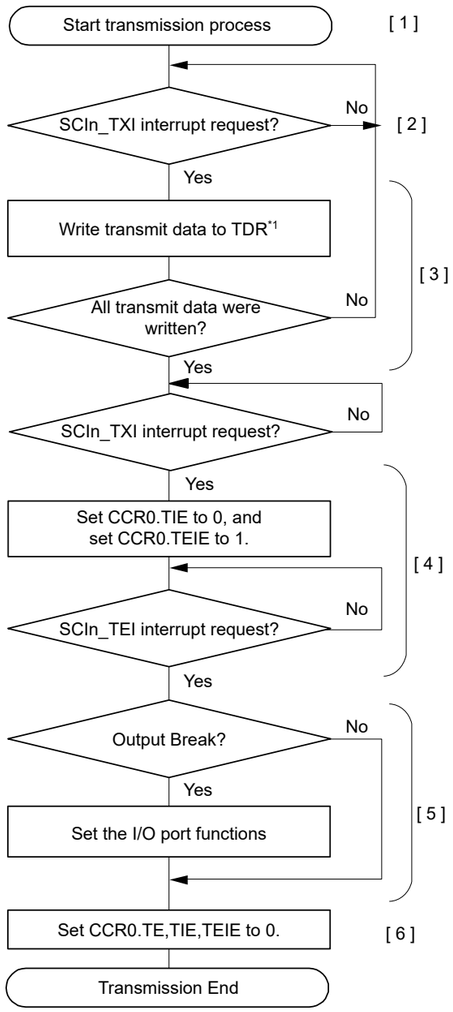


Figure 26.13 异步模式下串行传输的操作示例(4)（使用8位数据，奇偶校验，1个停止位，未使用CTS功能，从传输中间到传输Completion)



[1] Start transmission process

[2] SCIn_TXI interrupt request:
The transmit-data-empty-interrupt(SCIn_TXI) is generated at following conditions.
When set TE and TIE to 0 at same time.
When transmission-data forwards to TSR from TDR.

[3] Serial transmission continuation procedure:
To continue serial transmission write transmit data to TDR*1 once by using a SCIn_TXI.
Transmit data can also be written by activating the DMAC or DTC.

[4] If you use TEI, set TIE = 0 and TEIE = 1 after writing the last-transmit-data to TDR*1 and transmission is started.

[5] Break output at the end of serial transmission:
To output a break, it is necessary to set SPB2IO and SPB2DT, for output status setting when TE is 0.
(If you set these bits at initialization, you can skip this step.)

[6] Set CCR0.TE,TIE,TEIE to 0.

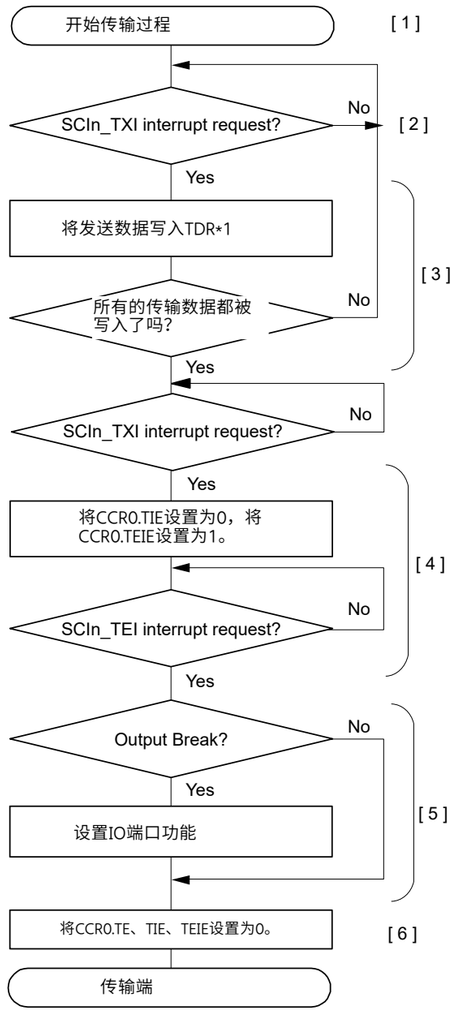
Note 1. In case of byte access with data length 9 bits, write transmit data in order of TDR[15:8] and TDR[7:0].

Figure 26.14 Example flow of serial transmission in asynchronous mode with non-FIFO selected

(2) FIFO selected

Figure 26.15 shows an example of a data format that is written to TDR register in asynchronous mode with FIFO selected.

Data corresponding to the data length is set to TDR[8:0]. Write 0 for unused bits. Write in order from TDR[15:8] to TDR[7:0].



[1]开始传输过程

[2]SCIn_TXI中断请求：发送数据空中断（SCIn_TXI）在以下条件下产生。当同时设置TE和TIE为0时。

当传输数据从TDR转发到TSR时。

[3]串行传输继续过程：要继续串行传输，使用SCIn_TXI将传输数据写入TDR*1一次。也可以通过激活DMAC或DTC来写入传输数据。[4]

如果使用TEI，在将最后发送数据写入TDR*1并开始发送后，设置TIE=0和TEIE=1。

[5]串行传输结束时的Break输出：要输出Break，需要设置SPB2IO和SPB2DT，用于TE为0时的输出状态设置。（如果在初始化时设置了这些位，则可以跳过此步骤。）

[6] 将CCR0.TE、TIE、TEIE设置为0。

注1.在数据长度为9位的字节访问情况下，按照TDR[15:8]和TDR[7:0]的顺序写入发送数据。

Figure 26.14 选择非FIFO的异步模式下串行传输示例流程

(2) FIFO selected

图26.15显示了以异步模式写入TDR寄存器并选择FIFO的数据格式示例。

与数据长度对应的数据设置为TDR[8:0]。为未使用的位写入0。按从TDR[15:8]到TDR[7:0].

Data Length	Register setting		Transmit data in TDR[15:0]															
	CCR3. CHR[1:0]		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bit	1	1	—	—	—	—	—	—	MPBT	—	—	TDAT[6:0]						
8 bit	1	0	—	—	—	—	—	—	MPBT	—	TDAT[7:0]							
9 bit	0	Don't Care	—	—	—	—	—	—	MPBT	TDAT[8:0]								

Note: —: Invalid. The write value should be 0.

Figure 26.15 Data format written to transmit-FIFO(TDR) with FIFO selected

In serial transmission, the SCI operates as described in this section.

1. The SCI transfers data from the TDR register to the TSR register when data is written to TDR in the SCIn_TXI interrupt handling routine. The amount of data that can be written to TDR is 16 minus FTSR.T[5:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the CCR0.TE and CCR0.TIE bits are set to 1 simultaneously by a single instruction.
2. Transmission starts after the CCR1.CTSE bit is set to 0 (CTS function is disabled) or a low level on the CTSn_RTSn pin causes data transfer from the TDR register to the TSR register. When the amount of transmit data written in TDR is equal to or less than the specified transmit triggering number, CSR.TDFE is set to 1. If the CCR0.TIE bit is 1, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to TDR in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set the CCR0.TIE bit to 0 (SCIn_TXI interrupt requests are disabled) and the CCR0.TEIE bit to 1 (an SCIn_TEI interrupt request is enabled) after the last of the data to be transmitted is written to the TDR register from the handling routine for SCIn_TXI requests.
3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data
   - Parity bit or multi-processor bit (can be omitted depending on the format)
   - Stop bit
4. On output of the stop bit, the SCI checks whether non-transmitted data remains in the TDR register.
5. When data is set to transmit-FIFO (TDR), setting the CCR1.CTSE bit to 0 (CTS function is disabled) or a low level input on the CTSn_RTSn pin causes transfer of the next transmit data from TDR to TSR and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If data is not set in transmit-FIFO (TDR), the TEND flag in CSR is set to 1, the stop bit is sent, and the mark state is entered in which 1 is output. If the CCR0.TEIE bit is 1, the CSR.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated.

Figure 26.16 shows an example flow of serial transmission in asynchronous mode with FIFO selected.

数据长度	注册设置		在TDR[15:0]中传输数据															
	CCR3. CHR[1:0]		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bit	1	1	—	—	—	—	—	—	MPBT	—	—	TDAT[6:0]						
8 bit	1	0	—	—	—	—	—	—	MPBT	—	TDAT[7:0]							
9 bit	0	Don't Care	—	—	—	—	—	—	MPBT	TDAT[8:0]								

Note: –：无效的。写入值应为0。

Figure 26.15 在选择FIFO的情况下写入发送FIFO(TDR)的数据格式

在串行传输中，SCI的操作如本节所述。

1.当数据在SCIn_TXI中断处理程序中写入TDR时，SCI将数据从TDR寄存器传输到TSR寄存器。可写入TDR的数据量为16减去FTSR.T[5:0]字节。当CCR0.TE和CCR0.TIE位通过一条指令同时设置为1时，会在传输开始时产生SCIn_TXI中断请求。

2.CCR1.CTSE位设置为0（禁用CTS功能）或CTSn_RTSn引脚上的低电平导致数据从TDR寄存器传输到TSR寄存器后开始传输。当写入TDR的发送数据量等于或小于指定的发送触发数时，CSR.TDFE设置为1。如果CCR0.TIE位为1，则产生SCIn_TXI中断请求。在当前发送数据发送完成之前，通过在SCIn_TXI中断处理例程中将下一个发送数据写入TDR可以实现连续发送。使用SCIn_TEI中断请求时，在写入要发送的最后一个数据后，将CCR0.TIE位设置为0（禁止SCIn_TXI中断请求）并将CCR0.TEIE位设置为1（启用SCIn_TEI中断请求）从SCIn_TXI请求的处理例程到TDR寄存器。

3.数据按以下顺序从TXDn引脚发送：

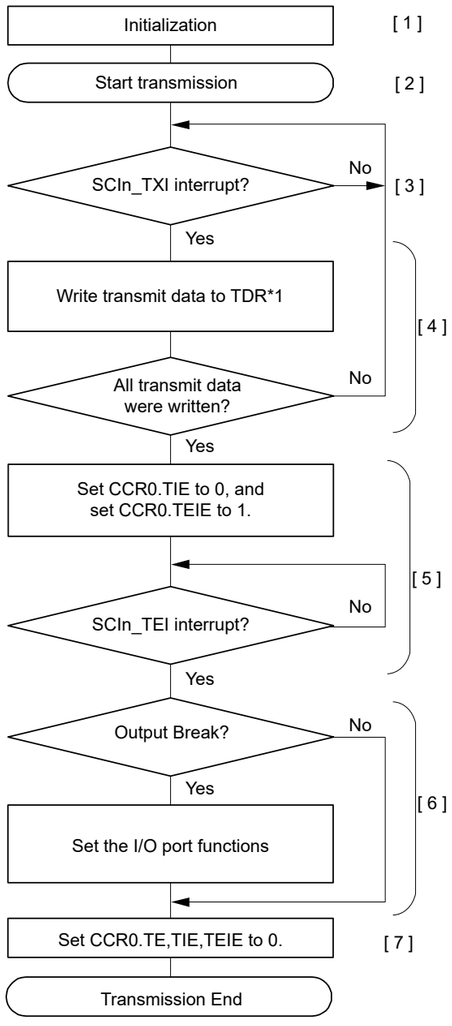
- ●起始位
- ●传输数据
- ●奇偶校验位或多处理器位（可根据格式省略）
- ●停止位

4.在停止位输出时，SCI检查未发送的数据是否保留在TDR寄存器中。

5.当数据设置为发送FIFO（TDR）时，将CCR1.CTSE位设置为0（CTS功能禁用）或低电平CTSn_RTSn引脚上的输入导致下一个传输数据从TDR传输到TSR并传输停止位，然后开始下一帧的串行传输。

6.如果发送FIFO(TDR)中没有设置数据，则CSR中的TEND标志设置为1，发送停止位，进入输出1的标记状态。如果CCR0.TEIE位为1，则CSR.TEND标志设置为1，并产生SCIn_TEI中断请求。

图26.16显示了选择FIFO的异步模式下串行传输的示例流程。



[1] Initialize SCI.
To enable SCIn_TXI interrupt, set TE and TIE to 1 with one instruction at the same time.

[2] Set transmit-data to the transmit-FIFO(TDR).
The number of transmittable data that can be set is16 .

[3] TXI interrupt request:
The transmit-data-empty-interrupt(SCIn_TXI) is generated
when transmission-data forwards to TSR from the transmit-FIFO(TDR) and the number of transmit-data written in the transmit-FIFO is equal to or less than the transmit-FIFO threshold.

[4] Serial transmission continuation procedure:
To continue serial transmission, write all transmit data to the transmit-FIFO(TDR) by using a SCIn_TXI interrupt and clear TDRE flag to 0. (Transmit data can also be written to the transmit- FIFO(TDR) by activating the DMAC or DTC. In this case, the TDRE flag is cleared automatically, so please don't operate the TDRE flag.)
The number of transmission data it's possible to write in is 16 - (the number of stored transmit FIFO data).

[5] If you use SCIn_TEI, set TIE = 0 and TEIE = 1 after writing the last-transmit-data to TDR*1.

[6] Break output at the end of serial transmission:
To output a break, it is necessary to set SPB2IO and SPB2DT, for output status setting when TE is 0.
(If you set these bits at initialization, you can skip this step.)

[7] Set CCR0.TE,TIE,TEIE to 0.

Note 1. In case of byte access with data length 9 bits, write transmit data in order of TDR[15:8] and TDR[7:0].

Figure 26.16 Example flow of serial transmission in asynchronous mode with FIFO selected

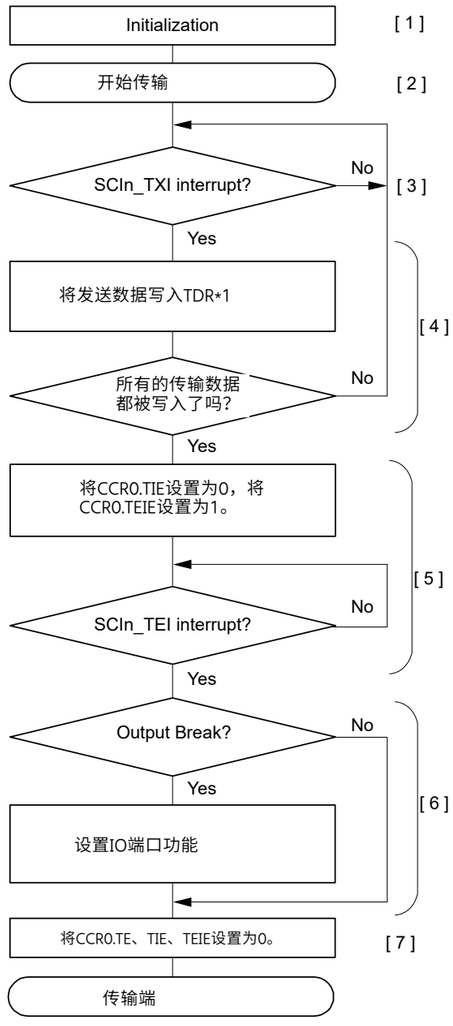
26.3.9 Serial Data Reception in Asynchronous Mode

(1) Non-FIFO selected

Figure 26.17 and Figure 26.18 show an example of the operation for serial data reception in asynchronous mode.

In serial data reception, the SCI operates as follows:

1. When the value of the CCR0.RE bit becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. The SCI monitors the communications line and when it detects a start bit, the SCI performs internal synchronization, stores receive data in RSR, and checks the parity bit and stop bit.
3. If an overrun error occurs, the CSR.ORER flag is set to 1. If the CCR0.RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the RDR register.



[1] 初始化SCI。
要启用SCIn_TXI中断，请同时使用一条指令将TE和TIE设置为1。

[2]将发送数据设置到发送FIFO(TDR)。可设置的可发送数据数为16。

[3]TXI中断请求：当传输数据从传输FIFO(TDR)转发到TSR并且写入传输FIFO的传输数据数量相等时，产生传输数据空中断(SCIn_TXI)到或小于发送FIFO阈值。

[4] 串行传输继续过程：
要继续串行发送，请使用SCIn_TXI中断将所有发送数据写入发送FIFO(TDR)，并将TDRE标志清零。（发送数据也可以通过激活DMAC或DTC写入发送FIFO(TDR)。在在这种情况下，TDRE标志会自动清零，因此请不要操作TDRE标志。）
可写入的传输数据数为16（存储的传输FIFO数据数）。

[5]如果您使用SCIn_TEI，请在将最后传输数据写入TDR*1后设置TIE=0和TEIE=1。

[6]串行传输结束时的中断输出：要输出中断，需要设置SPB2IO和SPB2DT，用于TE为0时的输出状态设置。（如果在初始化时设置了这些位，则可以跳过此步骤。）

[7] 将CCR0.TE、TIE、TEIE设置为0。

注1.在数据长度为9位的字节访问情况下，按照TDR[15:8]和TDR[7:0]的顺序写入发送数据。

Figure 26.16 选择FIFO的异步模式下串行传输示例流程

26.3.9 异步模式下的串行数据接收

(1) Non-FIFO selected

图26.17和图26.18显示了异步模式下串行数据接收操作的示例。

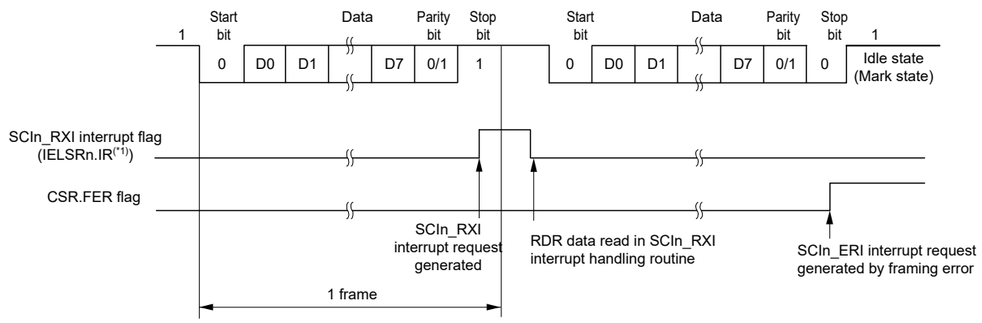
在串行数据接收中，SCI操作如下：

1.当CCR0.RE位的值变为1时，CTSn_RTSn引脚上的输出信号变为低电平。

2.SCI监控通信线路，当检测到起始位时，SCI执行内部同步，将接收数据存储在RSR中，并检查奇偶校验位和停止位。

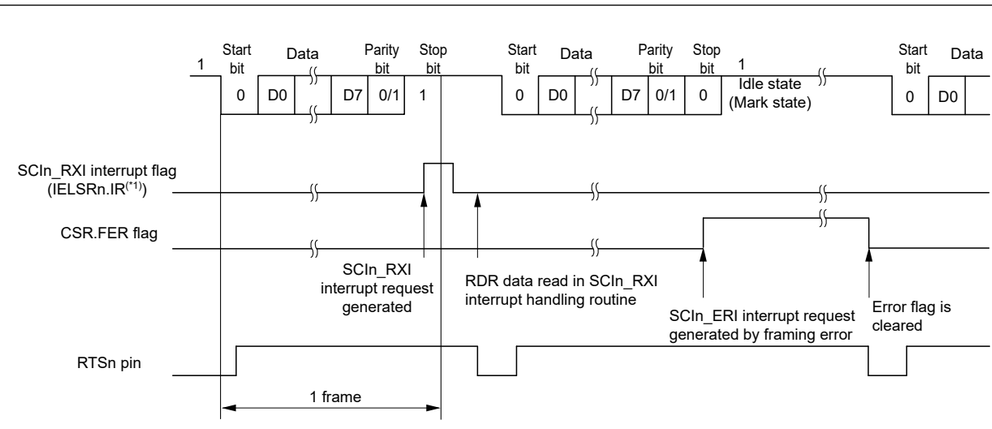
3.如果发生溢出错误，则CSR.ORER标志设置为1。如果CCR0.RIE位为1，则产生SCIn_ERI中断请求。接收数据不传送到RDR寄存器。

4. If a parity error is detected, the CSR.PER flag is set to 1 and receive data is transferred to the RDR register. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated.
5. If a framing error is detected, the CSR.FER flag is set to 1 and receive data is transferred to the RDR register. If the CCR0.RIE bit is 1, an SCIn_ERI interrupt request is generated.
6. When reception finishes successfully, receive data is transferred to the RDR register. If the CCR0.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to the RDR register in the SCIn_RXI interrupt handling routine before reception of the next receive data is complete. Reading the received data that was transferred to the RDR register causes the CTSn_RTSn pin to output low.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.17 Example of SCI operation for serial reception in asynchronous mode (1) when the RTS function is not used, and with 8-bit data, parity bit, and 1 stop bit



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.18 Example of SCI operation for serial reception in asynchronous mode (2) when RTS function is used, and with 8-bit data, parity bit, and 1 stop bit

Table 26.28 lists the states of the flags in the CSR status register and receive data handling when a receive error is detected.

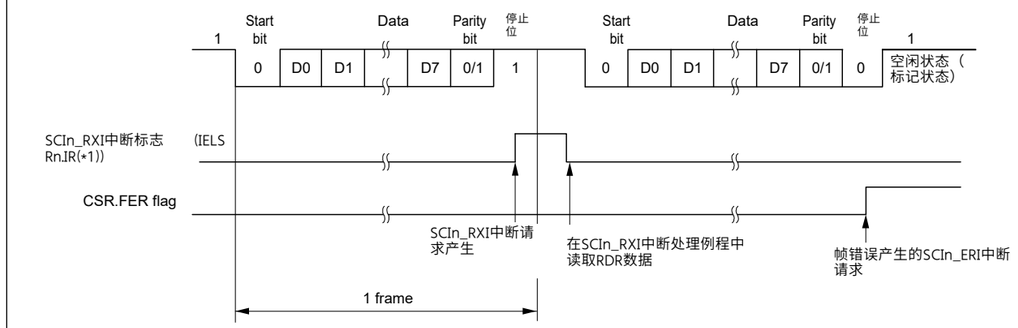
If a receive error is detected, an SCIn_ERI interrupt request is generated but an SCIn_RXI interrupt request is not generated. Data reception cannot be resumed while the receive error flag is 1. Accordingly, set the ORER, FER, and PER bits to 0 before resuming reception. In addition, be sure to read the RDR register during overrun error processing. When a reception is forced to terminate by setting the CCR0.RE bit to 0 during operation, read the RDR register because received data that is not yet read might be left in the RDR.

Figure 26.19 and Figure 26.20 show example flows of serial data reception.

4.如果检测到奇偶校验错误，则将CSR.PER标志设置为1，并将接收数据传输到RDR寄存器。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。

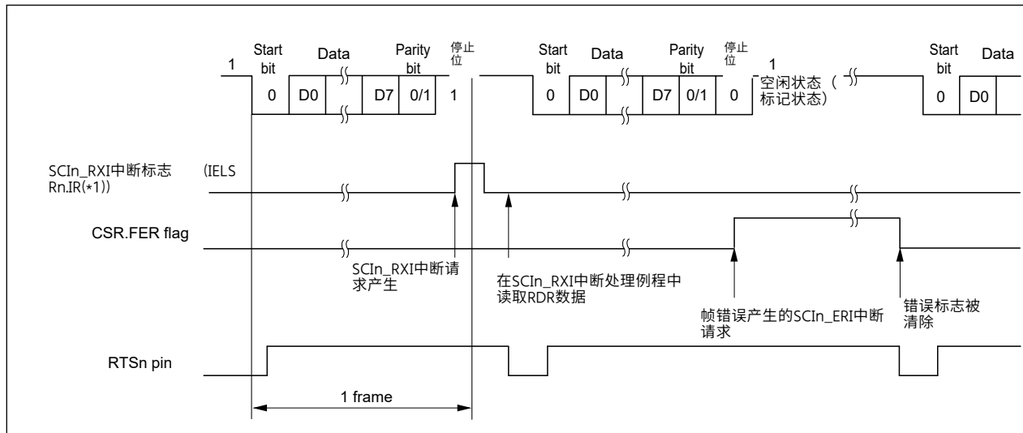
5.如果检测到帧错误，CSR.FER标志设置为1，接收数据被传送到RDR寄存器。如果CCR0.RIE位为1，则产生SCIn_ERI中断请求。

6.接收成功后，接收数据传送到RDR寄存器。如果CCR0.RIE位为1，则
SCIn_RXI中断请求产生。通过读取传输到的接收数据启用连续接收
在接收下一个接收数据完成之前，SCIn_RXI中断处理程序中的RDR寄存器。
读取传输到RDR寄存器的接收数据会导致CTSn_RTSn引脚输出低电平。



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.17 异步模式下串行接收的SCI操作示例(1)不使用RTS功能时，具有8位数据、奇偶校验位和1个停止位



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.18 使用RTS功能，8位数据、奇偶校验位和1个停止位时，异步模式下串行接收的SCI操作示例(2)

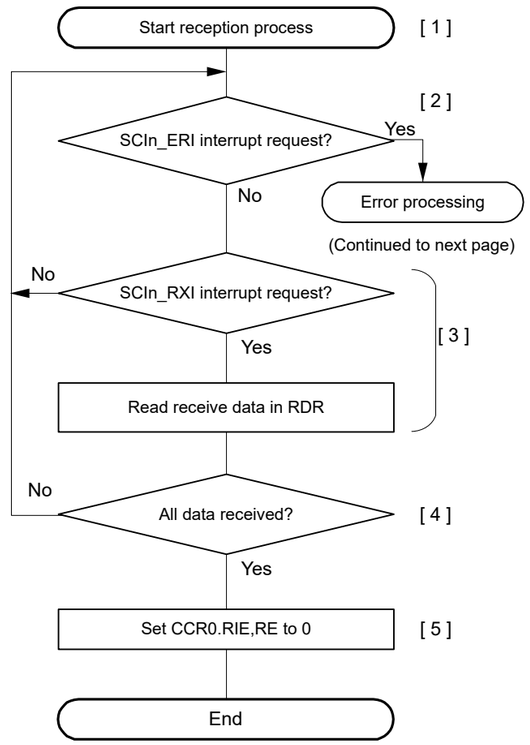
表26.28列出了CSR状态寄存器中标志的状态以及检测到接收错误时的接收数据处理。

如果检测到接收错误，则会产生SCIn_ERI中断请求，但不会产生SCIn_RXI中断请求。
当接收错误标志为1时，无法恢复数据接收。因此，在恢复接收之前，请将ORER、FER和PER位设置为0。此外，请务必在溢出错误处理期间读取RDR寄存器。如果在操作期间通过将CCR0.RE位设置为0来强制终止接收，请读取RDR寄存器，因为尚未读取的接收数据可能会留在RDR中。

图26.19和图26.20显示了串行数据接收的示例流程。

Table 26.28 Flags in CSR Status Register and receive data handling

Flags in the CSR Status Register			Receive data	Receive error type
ORER	FER	PER		
1	0	0	Lost	Overrun error
0	1	0	Transferred to RDR	Framing error
0	0	1	Transferred to RDR	Parity error
1	1	0	Lost	Overrun error + framing error
1	0	1	Lost	Overrun error + parity error
0	1	1	Transferred to RDR	Framing error + parity error
1	1	1	Lost	Overrun error + framing error + parity error



[1] Start reception process

[2] Receive error processing and break detection: If a receive error occurs, an SCIn_ERI interrupt is generated. After performing the appropriate error processing, be sure to set the ORER, PER, and FER flags to 0. Reception cannot be resumed if any of these flags is set to 1. In the case of a framing error, a break can be detected by reading the value of the input port corresponding to the RXDn pin.

[3] Read the receive data in RDR once in the SCIn_RXI interrupt handling routine.

[4] Serial reception continuation procedure: To continue serial reception, before the stop bit of the current frame is received, read data from RDR in the SCIn_RXI interrupt handling routine. The RDR data can also be read by activating the DMAC or DTC.

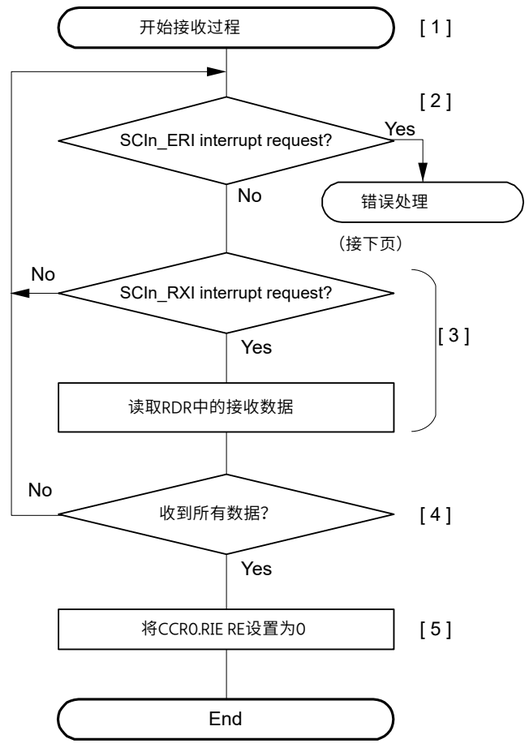
[5] Set CCR0.RIE,RE to 0.

Note 1. Do not set RE to 0 before reading RDR.

Figure 26.19 Example flow of serial reception in asynchronous mode with non-FIFO selected and Address Matching Disabled (1)

Table 26.28 CSR状态寄存器中的标志和接收数据处理

CSR状态寄存器中的标志			接收数据	接收错误类型
ORER	FER	PER		
1	0	0	Lost	溢出错误
0	1	0	转移到RDR	构图错误
0	0	1	转移到RDR	奇偶校验错误
1	1	0	Lost	溢出错误+成帧错误
1	0	1	Lost	溢出错误+奇偶校验错误
0	1	1	转移到RDR	成帧错误+奇偶校验错误
1	1	1	Lost	溢出错误+帧错误+奇偶校验错误



[1]开始接收进程

[2]接收错误处理和中断检测：如果发生接收错误，则产生SCIn_ERI中断。执行适当的错误处理后，请务必将ORER、PER和FER标志设置为0。如果这些标志中的任何一个设置为1，则无法恢复接收。在帧错误的情况下，可以通过以下方式检测中断读取对应于RXDn引脚的输入端口的值。

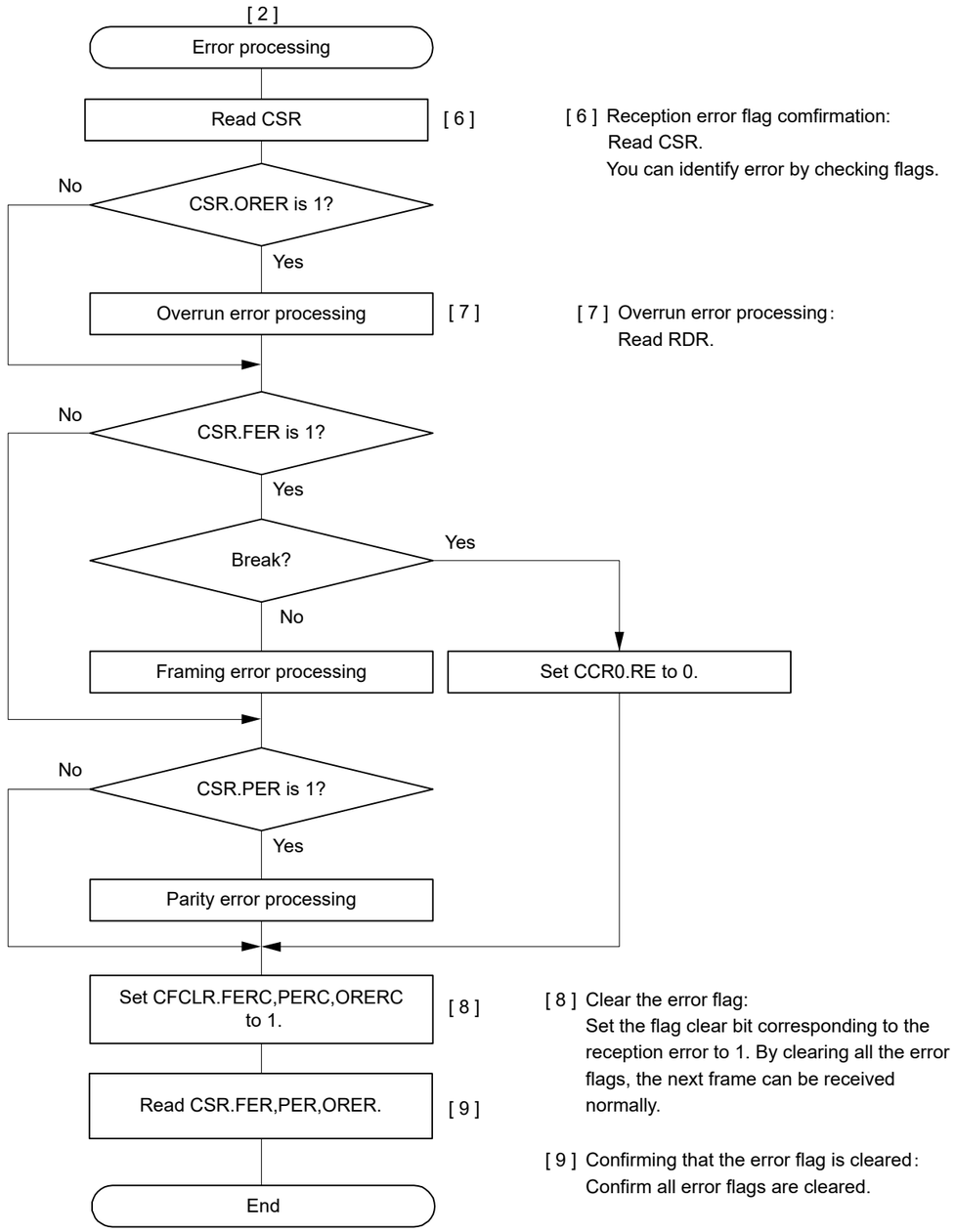
[3]在SCIn_RXI中断处理程序中读取一次RDR中的接收数据。

[4]串行接收继续程序：要继续串行接收，在接收到当前帧的停止位之前，在SCIn_RXI中断处理程序中从RDR读取数据。RDR数据也可以通过激活DMAC或DTC来读取。

[5]将CCR0.RIE RE设置为0。

注1.在读取RDR之前不要将RE设置为0。

Figure 26.19 异步模式下串行接收的示例流程，选择了非FIFO和地址匹配已禁用(1)

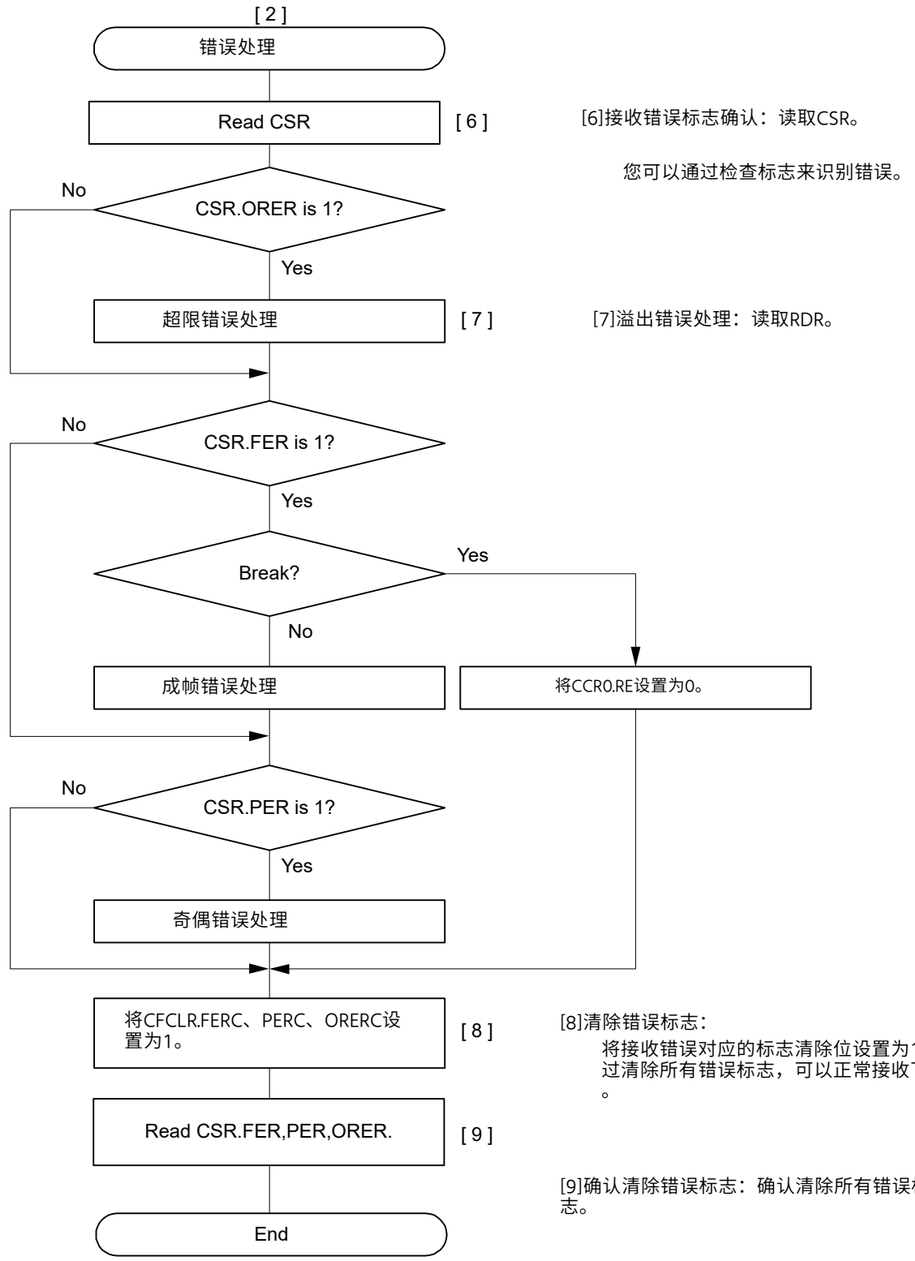


Note: The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 26.20 Example flow of serial reception in asynchronous mode with non-FIFO selected and Address Matching Disabled (2)

(2) FIFO selected

Figure 26.21 shows an example of a data format that is written to Receive-FIFO(RDR) register in asynchronous mode.



Note: 选择9位数据长度时，RDR寄存器成为RDRHL寄存器。

Figure 26.20 异步模式下串行接收的示例流程，选择了非FIFO和地址匹配已禁用(2)

(2) FIFO selected

图26.21显示了在异步模式下写入Receive-FIFO(RDR)寄存器的数据格式示例。

In asynchronous mode, 0 is written to the MPB bit in the RDR register. Data that corresponds to the data length is written to RDR. Unused bits are written as 0. If software reads RDR, the SCI updates FER, PER, and receive data (RDAT[8:0]) in the RDR register with the next data. The flags RDF, ORER, and DR in the RDR register always reflect the associated flags in the CSR register.

Data Length	Register Setting		Receive flag in RDR[31:0], MPB, RDAT[8:0]															
	CCR3.CHR[1:0]		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7bit	1	1	-	-	-	FFER	FPER	DR	MPB	0	0	RDAT[6:0]						
8bit	1	0	-	-	-	FFER	FPER	DR	MPB	0	RDAT[7:0]							
9bit	0	Don't care	-	-	-	FFER	FPER	DR	MPB	RDAT[8:0]								
	CCR3.CHR[1:0]		b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
7bit	1	1	-	-	-	FER	PER	-	-	ORER	-	-	-	-	-	-	-	-
8bit	1	0	-	-	-	FER	PER	-	-	ORER	-	-	-	-	-	-	-	-
9bit	0	Don't care	-	-	-	FER	PER	-	-	ORER	-	-	-	-	-	-	-	-

Note: 0 is always read from the MPB flag (RDR [9] bit).
When a 7-bit data length is selected, 0 is read from the RDAT [8:7] bits.
When 8-bit data length is selected, 0 is read from the RDAT [8] bit.

Figure 26.21 Data format stored in receive-FIFO(RDR) with FIFO selected

Table 26.29 lists the states of the flags in CSR status register and receive data handling when a receive error is detected with FIFO selected. Figure 26.22 and Figure 26.23 show samples of flowcharts for serial data reception with FIFO selected.
In serial data reception, the SCI operates as follows:

1. When the value of the CCR0.RE bit becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. The SCI monitors the communications line and, when it detects a start bit, the SCI performs internal synchronization, stores receive data in the RSR register.
3. If an overrun error occurs during normal communications, the CSR.ORER flag is set to 1. If the CCR0.RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the RDR register.
4. If a parity error is detected, the PER flag and receive data are transferred to the RDR register. If the CCR0.RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
5. If a framing error is detected, the FER flag and receive data are transferred to the RDR register. If the CCR0.RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
6. After a framing error is detected and when SCI detects that the continuous receive data is zero for one frame, reception stops.
7. When the amount of data stored in the RDR register falls below the specified receive triggering number, and the next data is not received after 15 ETUs from the last stop bit in asynchronous mode, the FRSR.DR flag is set to 1. When the CCR0.RIE bit is 1 and the FCR.DRES bit is 0, the SCI generates an SCIn_RXI interrupt request. When the FCR.DRES bit is 1, SCI generates an SCIn_ERI interrupt request.
8. When reception finishes successfully, receive data is transferred to the RDR register. The RDRF bit is set to 1 when the amount of receive data written to RDR is equal to or greater than the specified receive triggering number. If the CCR0.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to the RDR register in the SCIn_RXI interrupt handling routine, before an overrun error occurs. If the received data that is transferred to RDR is less than the RTS trigger number, the CTSn_RTSn pin outputs low.

Table 26.29 Flags in the CSR Status Register and Receive Data Handling (FIFO selected) (1 of 2)

CSR value			Receive-FIFO (RDR)	Receive Error Type
ORER	FER*1	PER*1	RDAT[8:0]	
1	0	0	Lost	Overrun error
0	1	0	Transferred RDR	Framing error
0	0	1	Transferred RDR	Parity error

在异步模式下，0被写入RDR寄存器的MPB位。与数据长度对应的数据被写入RDR。未使用的位写入0。如果软件读取RDR，则SCI更新FER、PER和接收数据（RDAT[8:0]）
RDR注册下一个数据。RDR寄存器中的标志RDF、ORER和DR始终反映CSR寄存器中的相关标志。

数据长度	寄存器设置		RDR[31:0]、MPB、RDAT[8:0]中的接收标志															
	CCR3.CHR[1:0]		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7bit	1	1	-	-	-	FFER	FPER	DR	MPB	0	0	RDAT[6:0]						
8bit	1	0	-	-	-	FFER	FPER	DR	MPB	0	RDAT[7:0]							
9bit	0	Don't care	-	-	-	FFER	FPER	DR	MPB	RDAT[8:0]								
	CCR3.CHR[1:0]		b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
7bit	1	1	-	-	-	FER	PER	-	-	ORER	-	-	-	-	-	-	-	-
8bit	1	0	-	-	-	FER	PER	-	-	ORER	-	-	-	-	-	-	-	-
9bit	0	Don't care	-	-	-	FER	PER	-	-	ORER	-	-	-	-	-	-	-	-

Note: 总是从MPB标志（RDR[9]位）读取0。选择7位数据长度时，从RDAT[8:7]位读取0。
选择8位数据长度时，从RDAT[8]位读取0。

Figure 26.21 数据格式存储在接收FIFO(RDR)中并选择了FIFO

表26.29列出了CSR状态寄存器中标志的状态以及当检测到接收错误时的接收数据处理
选择先进先出。图26.22和图26.23显示了选择FIFO的串行数据接收的流程图示例。
在串行数据接收中，SCI操作如下：

1.当CCR0.RE位的值变为1时，CTSn_RTSn引脚上的输出信号变为低电平。

2.SCI监视通信线路，当它检测到一个起始位时，SCI执行内部同步，将接收数据存储在RSR寄存器中。

3.如果在正常通信过程中发生溢出错误，则CSR.ORER标志设置为1。如果CCR0.RIE位为1，则产生SCIn_ERI中断请求。接收数据不传送到RDR寄存器。

4.如果检测到奇偶校验错误，则将PER标志和接收数据传送到RDR寄存器。如果CCR0.RIE位设置为1，则产生SCIn_ERI中断请求。

5.如果检测到帧错误，则将FER标志和接收数据传送到RDR寄存器。如果CCR0.RIE位设置为1，则产生SCIn_ERI中断请求。

6、检测到帧错误后，当SCI检测到连续接收数据一帧为零时，停止接收。

7.当存储在RDR寄存器中的数据量低于指定的接收触发数，并且在异步模式下从最后一个停止位开始15个ETU后没有接收到下一个数据时，FRSR.DR标志设置为1。CCR0.RIE位为1，FCR.DRES位为0，SCI产生一个SCIn_RXI中断请求。当FCR.DRES位为1时，SCI产生一个SCIn_ERI中断请求。

8.接收成功后，接收数据传送到RDR寄存器。当写入RDR的接收数据量等于或大于指定的接收触发数时，RDRF位设置为1。如果CCR0.RIE位为1，则产生SCIn_RXI中断请求。在发生溢出错误之前，通过在SCIn_RXI中断处理例程中读取传输到RDR寄存器的接收数据来启用连续接收。如果接收到的传输到RDR的数据小于RTS触发数，CTSn_RTSn引脚输出低电平。

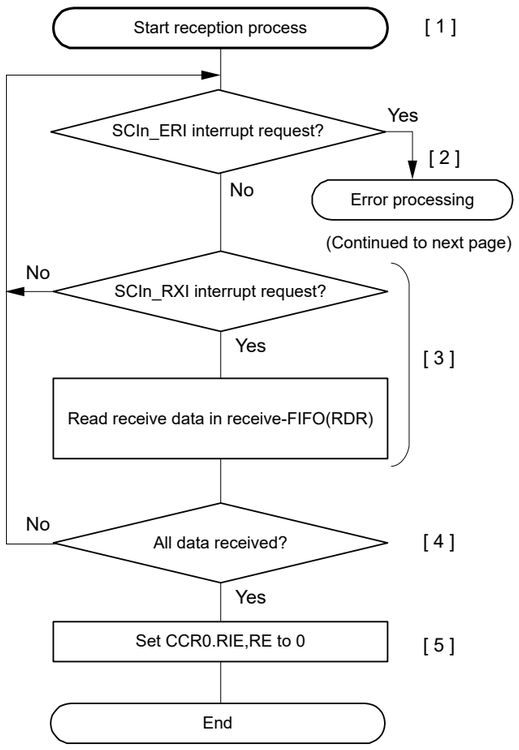
Table 26.29 CSR状态寄存器中的标志和接收数据处理（选择FIFO）（1of2）

CSR value			Receive-FIFO (RDR)	接收错误类型
ORER	FER*1	PER*1	RDAT[8:0]	
1	0	0	Lost	溢出错误
0	1	0	Transferred RDR	构图错误
0	0	1	Transferred RDR	奇偶校验错误

Table 26.29 Flags in the CSR Status Register and Receive Data Handling (FIFO selected) (2 of 2)

CSR value			Receive-FIFO (RDR)	Receive Error Type
ORER	FER*1	PER*1	RDAT[8:0]	
1	1	0	Lost	Overrun error + Framing error
1	0	1	Lost	Overrun error + Parity error
0	1	1	Transferred RDR	Framing error + Parity error
1	0	0	Lost	Overrun error + Framing error + Parity error

Note 1. This flag indicates whether there is an error in received data when reception is completed.



[1] Start reception process

[2] Receive error processing and break detection: If a receive error occurs, an SCIn_ERI interrupt is generated. After performing the appropriate error processing, be sure to set the ORER flags to 0. Reception cannot be resumed if ORER is set to 1. Reception can continue even if PER,FER,DR flags are 1.

[3] Read the receive data in the receive-FIFO(RDR) in the SCIn_RXI interrupt handling routine. The reception data stored in the receive-FIFO(RDR) is read until the number of stored data will be below the FCR.RTRG value at least. You can confirm the number of the reception data in the FIFO by FRSR.R[5:0].

[4] Serial reception continuation procedure: To continue serial reception, before an overrun error occurs, please read data from the receive-FIFO(RDR) in the SCIn_RXI interrupt handling routine and clear CSR.RDRF flag and FRSR.DR flag to 0. The receive-FIFO data can also be read by activating the DMA or DTC. The RDRF flag is cleared automatically in this case, so please don't operate the RDRF flag.

[5] Set CCR0.RIE,RE to 0.

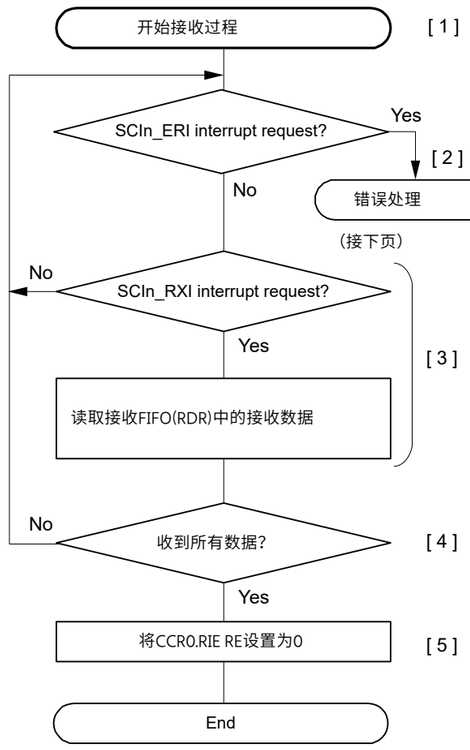
Note 1. Can be read in the RDR.ORER, PER, FER and DR flags.

Figure 26.22 Example flow of serial reception in asynchronous mode with FIFO selected and Address Matching Enabled (1)

Table 26.29 CSR状态寄存器中的标志和接收数据处理（选择FIFO）（2之2）

CSR value			Receive-FIFO (RDR)	接收错误类型
ORER	FER*1	PER*1	RDAT[8:0]	
1	1	0	Lost	溢出错误+成帧错误
1	0	1	Lost	溢出错误+奇偶校验错误
0	1	1	Transferred RDR	成帧错误+奇偶校验错误
1	0	0	Lost	溢出错误+帧错误+奇偶校验错误

注1.该标志表示接收完成时接收数据是否有错误。



[1]开始接收进程

[2]接收错误处理和中断检测：如果发生接收错误，则产生SCIn_ERI中断。执行适当的错误处理后，请务必将ORER标志设置为0。如果ORER设置为1，则无法恢复接收。即使PER、FER、DR标志为1，也可以继续接收。

[3]在receive中读取接收数据

SCIn_RXI中断处理例程中的FIFO(RDR)。读取存储在接收FIFO(RDR)中的接收数据，直到存储的数据数量至少低于FCR.RTRG值。您可以通过FRSR.R[5:0]确认FIFO中接收数据的数量。

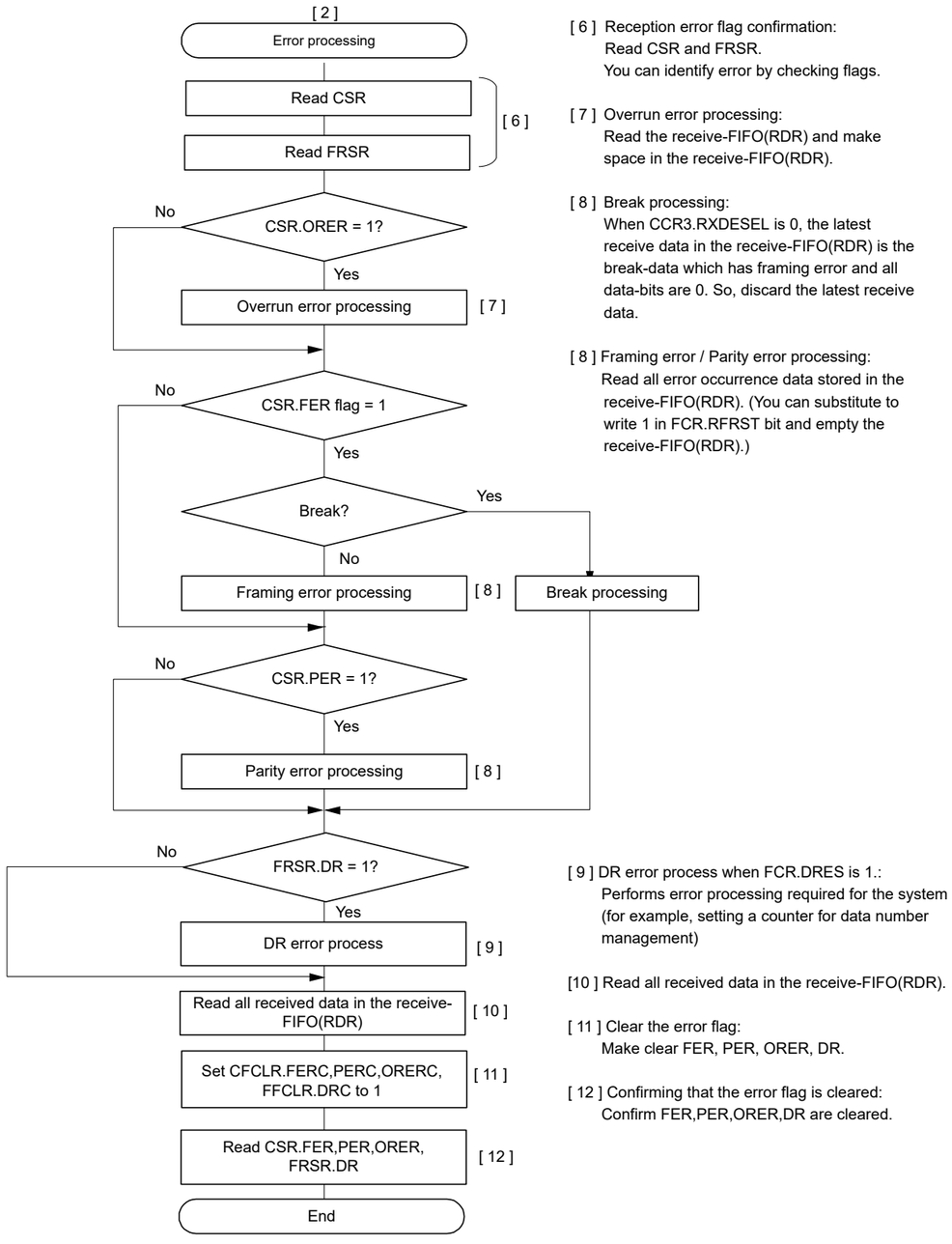
[4]串行接收继续过程：

要继续串行接收，在发生溢出错误之前，请在SCIn_RXI中断处理程序中从接收FIFO(RDR)中读取数据，并将CSR.RDRF标志和FRSR.DR标志清除为0。接收FIFO数据也可以被读取通过激活DMA或DTC。这种情况下RDRF标志会自动清零，因此请不要操作RDRF标志。

[5]将CCR0.RIE RE设置为0。

注1.可以在RDR.ORER、PER、FER和DR标志中读取。

Figure 26.22 选择FIFO和地址的异步模式下串行接收示例流程匹配启用(1)



[6] Reception error flag confirmation:
Read CSR and FRSR.
You can identify error by checking flags.

[7] Overrun error processing:
Read the receive-FIFO(RDR) and make space in the receive-FIFO(RDR).

[8] Break processing:
When CCR3.RXDESEL is 0, the latest receive data in the receive-FIFO(RDR) is the break-data which has framing error and all data-bits are 0. So, discard the latest receive data.

[8] Framing error / Parity error processing:
Read all error occurrence data stored in the receive-FIFO(RDR). (You can substitute to write 1 in FCR.RFRST bit and empty the receive-FIFO(RDR).)

[9] DR error process when FCR.DRES is 1.:
Performs error processing required for the system (for example, setting a counter for data number management)

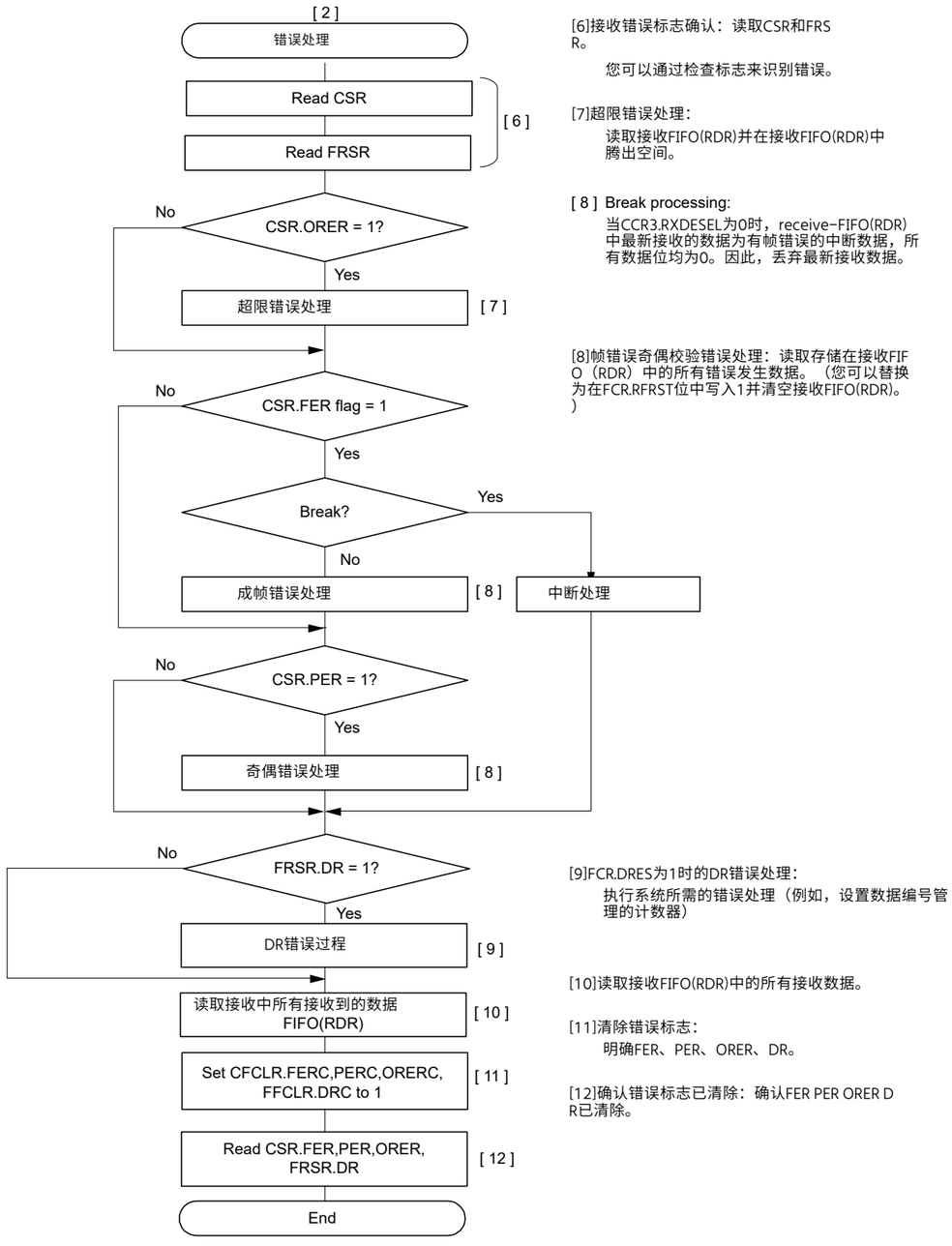
[10] Read all received data in the receive-FIFO(RDR).

[11] Clear the error flag:
Make clear FER, PER, ORER, DR.

[12] Confirming that the error flag is cleared:
Confirm FER,PER,ORER,DR are cleared.

Figure 26.23 Example flow of serial reception in asynchronous mode with FIFO selected Address Matching Disabled (2)

26.3.10 The function of adjust receive sampling timing (Asynchronous Mode)



[6]接收错误标志确认：读取CSR和FRSR。
您可以通过检查标志来识别错误。

[7]超限错误处理：
读取接收FIFO(RDR)并在接收FIFO(RDR)中腾出空间。

[8] Break processing:
当CCR3.RXDESEL为0时，receive-FIFO(RDR)中最新接收的数据为有帧错误的中断数据，所有数据位均为0。因此，丢弃最新接收数据。

[8]帧错误奇偶校验错误处理：读取存储在接收FIFO（RDR）中的所有错误发生数据。（您可以替换为在FCR.RFRST位中写入1并清空接收FIFO(RDR)。）

[9]FCR.DRES为1时的DR错误处理：
执行系统所需的错误处理（例如，设置数据编号管理的计数器）

[10]读取接收FIFO(RDR)中的所有接收数据。

[11]清除错误标志：
明确FER、PER、ORER、DR。

[12]确认错误标志已清除：确认FER PER ORER DR已清除。

Figure 26.23 使用FIFO选择地址匹配的异步模式串行接收示例流程 Disabled (2)

26.3.10 调整接收采样定时功能（异步模式）

When there is the difference between the rising transfer time and the falling transfer time through a photo coupler, the receive sampling timing at middle of bit affects the reception margin. In this case, the receive sampling timing is able to adjust from the middle of bit to the optimum timing by using this function.

The receive sampling timing is adjusted from the middle of bit by following formula. And the adjustable direction is set by CCR4.AJD. You can select forward or backward from the middle of bit. When adjusting backward (CCR4.AJD = 0), substitute AJD = +1 and substitute AJD = -1 when adjusting forward (CCR4.AJD = 1).

Adjusted sampling timing = the middle of bit + AJD * (base clock * the setting value of CCR4.AST[2:0])

The setting timing is limited by base clock cycles per 1 bit. Please refer to Table 26.30 in detail.

An overview of reception operation of the communication through a photo coupler with this function is shown in Figure 26.24, Figure 26.25 and Figure 26.26, the explanation of operation with this function is shown in Figure 26.27.

Please don't use this function when there is no difference between the rising transfer time and the falling transfer time, because there is a possibility of deteriorating the reception margin.

Table 26.30 The acceptable value of CCR4 register (asynchronous mode using internal clock)

CCR2.ABCSE	CCR2.ABCS	The number of base clock cycles/1bit	The acceptable value of CCR4	
			CCR4.AJD	CCR4.AST
1	x	6	0	000b – 010b*1
			1	
0	1	8	0	000b – 011b*1
			1	
0	0	16	0	000b – 111b
			1	

Note: x: Don't care

Note 1. When the value of CCR4.AST exceeds the acceptable value, sampling is done at default timing. (Adjustment of sampling is not done.)

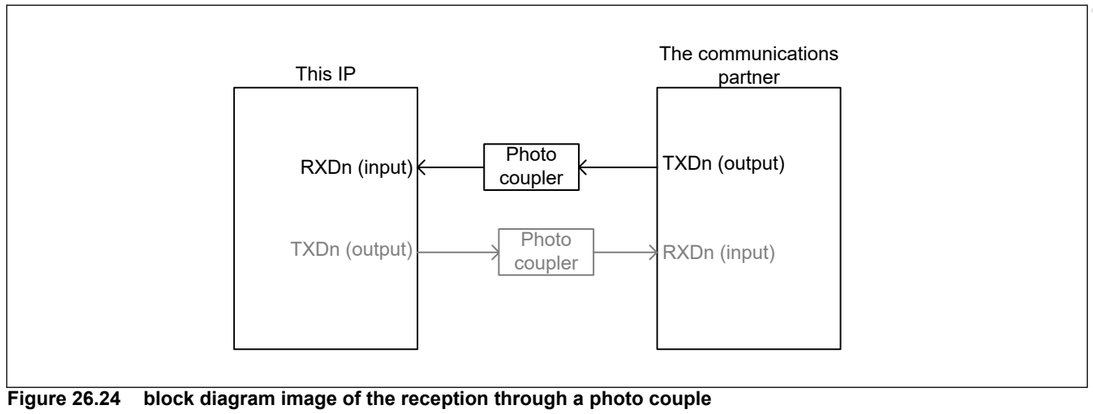


Figure 26.24 block diagram image of the reception through a photo couple

当通过光电耦合器的上升传输时间和下降传输时间之间存在差异时，位中间的接收采样时间会影响接收裕度。在这种情况下，接收采样时序可以通过使用该功能从比特中间调整到最佳时序。

接收采样定时通过以下公式从位中间调整。可调方向由CCR4.AJD。您可以从位的中间选择向前或向后。向后调整时（CCR4.AJD=0），代入AJD=+1，向前调整时代入AJD=-1（CCR4.AJD=1）。

调整后的采样时序=中间位+AJD*（基准时钟*CCR4.AST[2:0]的设置值）

设置时序受限于每1位的基本时钟周期。详见表26.30。

图26.24、图26.25、图26.26所示为使用该功能的光耦合器通信的接收操作概要，使用该功能的操作说明如图26.27所示。

请不要在上升传输时间和下降传输时间没有差异时使用此功能，因为有可能恶化接收余量。

Table 26.30 CCR4寄存器的可接受值（使用内部时钟的异步模式）

CCR2.ABCSE	CCR2.ABCS	基本时钟周期数1bit	CCR4的可接受值	
			CCR4.AJD	CCR4.AST
1	x	6	0	000b – 010b*1
			1	
0	1	8	0	000b – 011b*1
			1	
0	0	16	0	000b – 111b
			1	

Note: x: Don't care

注1.当CCR4.AST的值超过可接受的值时，将在默认时序进行采样。（未进行采样调整。）

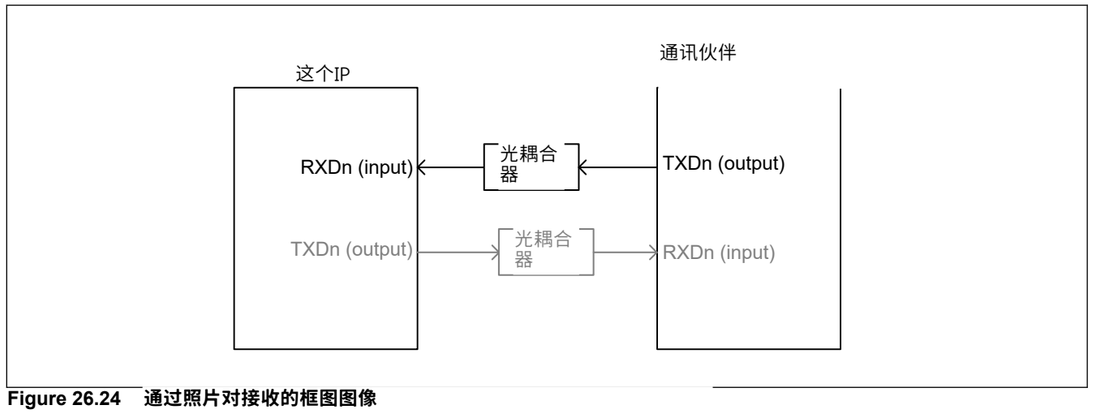
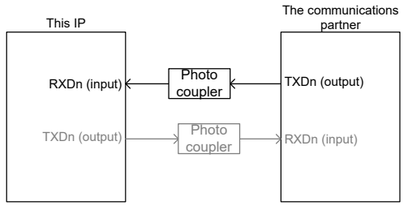
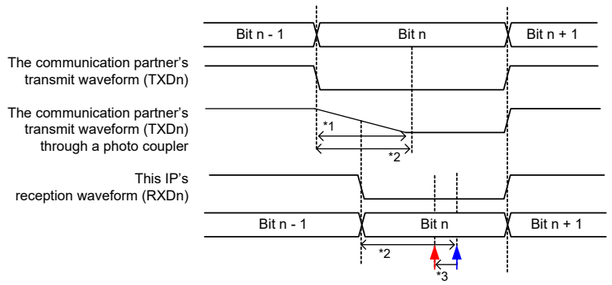


Figure 26.24 通过照片对接收的框图图像



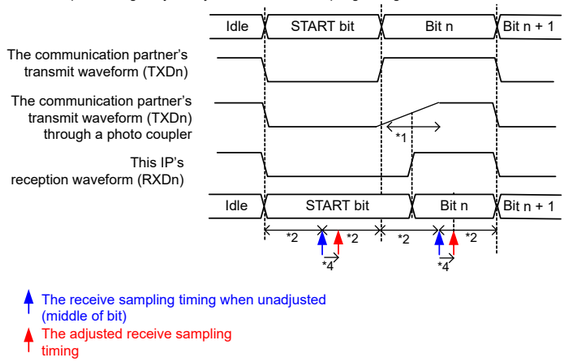
(a) In the case of the falling transfer time >> rising transfer time

The falling edge of reception waveform is made dull like following chart.
In this case, you can sampling at the middle of bit if you adjust the receive sampling timing to forward (AJD = 1).



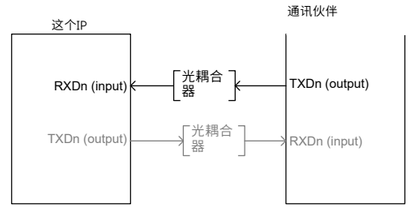
(b) In the case of the falling transfer time << rising transfer time

The rising edge of reception waveform is made dull like following chart.
So, the reception margin of communications partner will be bad. In this case, you can improve the reception margin if you adjust the receive sampling timing to back.



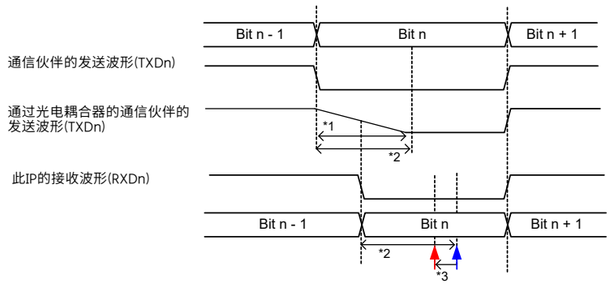
Note: This waveform shows the operation image of adjustment in reception sampling timing.
Note 1. The dull period by a photo coupler
Note 2. Bit center timing at set communication rate
Note 3. When CCR4.AJD is 1, the receive sampling timing is shifted to forward by the setting value of CCR4.AST[2:0].
Note 4. When CCR4.AJD is 0, the Receive sampling timing is shifted to backward by the setting value of CCR4.AST[2:0].

Figure 26.25 Overview of reception operation of the communication through a photo coupler



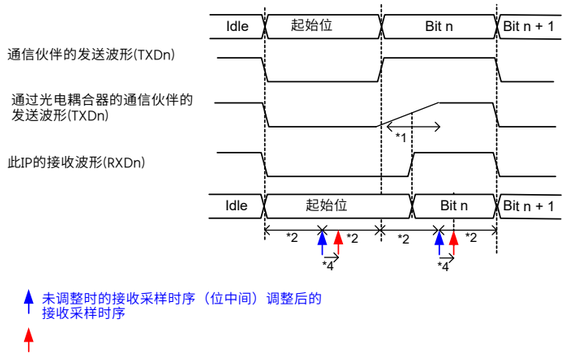
(a)在下降传输时间>>上升传输时间的情况下

接收波形的下降沿变钝，如下图所示。
在这种情况下，如果将接收采样时序调整为正向（AJD=1），则可以在位中间进行采样。



(b)在下降传输时间<<上升传输时间的情况下

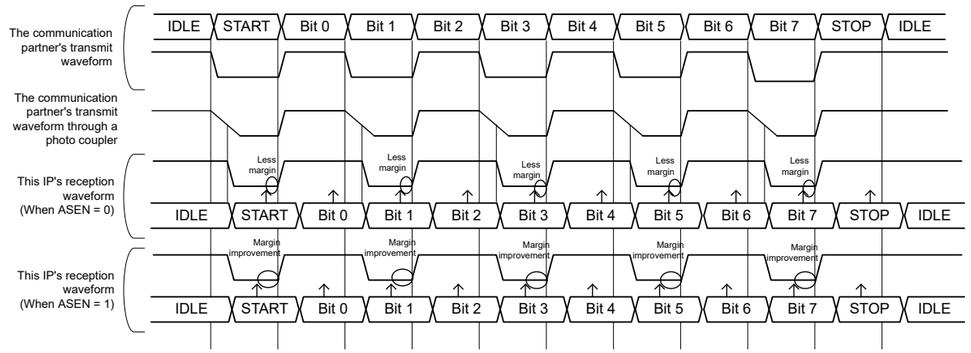
接收波形的上升沿变钝，如下图所示。
因此，通信伙伴的接收幅度会很差。在这种情况下，如果您将接收采样定时向后调整，您可以提高接收裕度。



Note: 该波形显示了接收采样定时调整的操作图像。
注1.光电耦合器的无光泽期
注2.设定通信速率下的位中心时序
注3.当CCR4.AJD为1时，接收采样定时向前移动CCR4.AST[2:0]的设置值。
注4.当CCR4.AJD为0时，接收采样时序向后移动CCR4.AST[2:0]的设置值。

Figure 26.25 通过光电耦合器进行通信的接收操作概述

In the case of the falling transfer time >> the rising transfer time by a photo coupler.



In the case of the falling transfer time << the rising transfer time by a photo coupler.

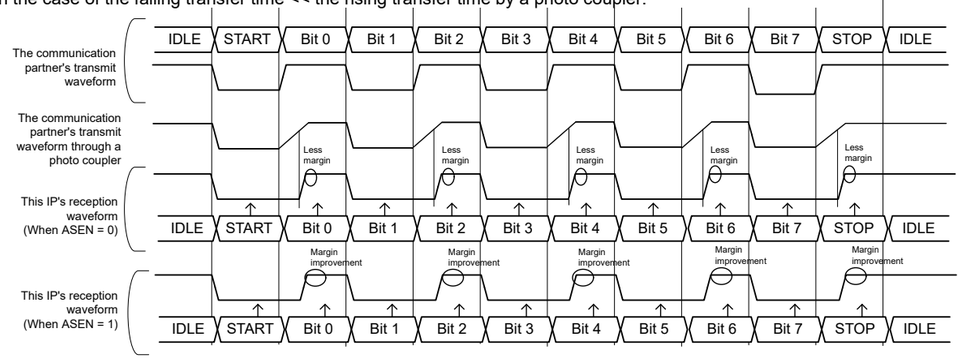
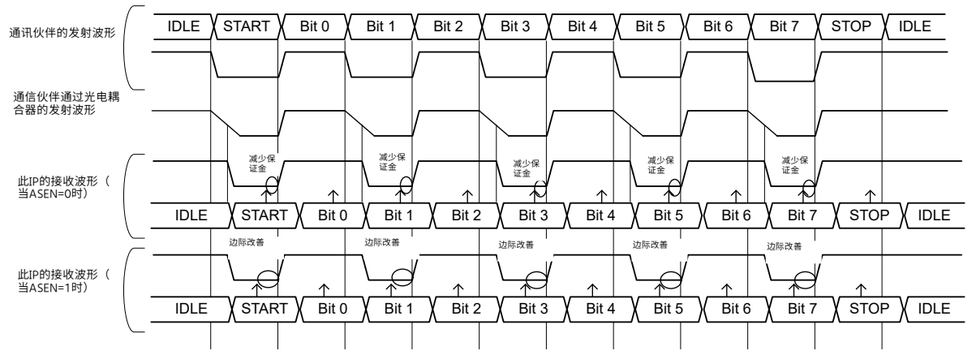


Figure 26.26 Example of improvement in reception margin by the reception sampling timing adjustment function

在下降传输时间的情况下>>光电耦合器的上升传输时间。



在下降传输时间<<光电耦合器的上升传输时间的情况下。

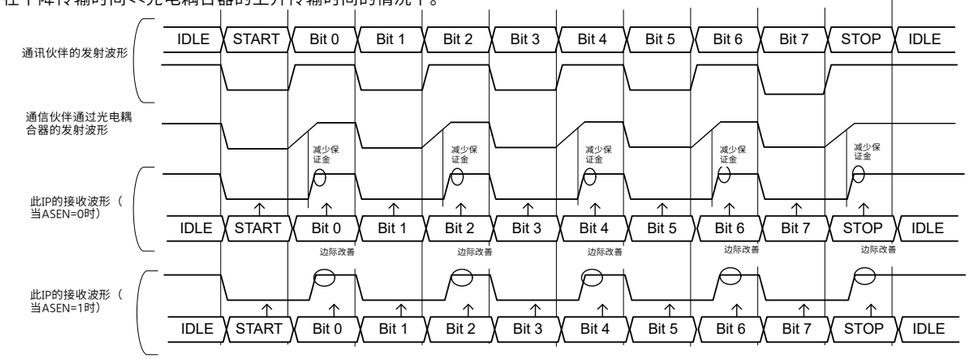


Figure 26.26 通过接收采样定时调整功能提高接收裕量的示例

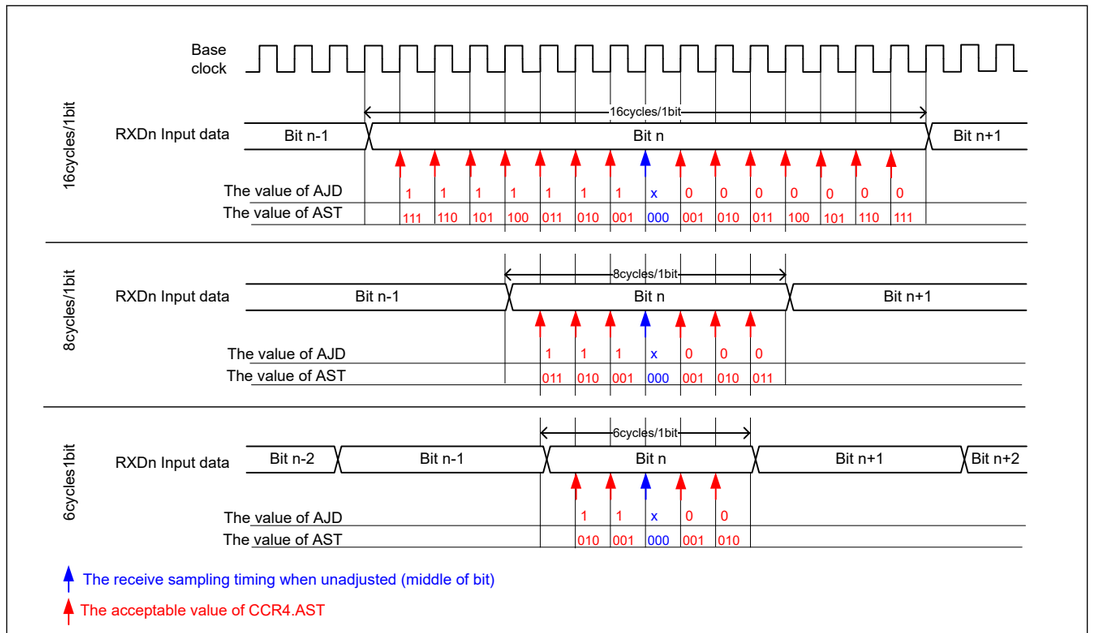


Figure 26.27 Overview of the adjustment operation for the reception sampling timing (asynchronous mode using internal clock)

26.3.11 The function of adjust transmit timing (Asynchronous Mode)

In communication via a photo coupler or the like, when either the rising or falling transition time of the TXDn output signal is long, then a communication partner receive dulled waveform. In this case, the reception margin may be affected.

In these cases, make a communication partner to be sampling at middle of bit using the function of adjust transmit timing.

When CCR4.ATEN is 1, this function can adjust the edge timing at the timing calculated by the following formula for the edge set with CCR4.AET.

The adjustment edge timing = the base clock * CCR4.ATT[2:0]

In addition, the upper limit of the adjustment edge timing is limited by setting the base clock cycles. Refer to Table 26.31 in details.

A transmission movement image figure of the communication through a photo coupler with this function is shown in Figure 26.28, Figure 26.29 and Figure 26.30, the overview of operation with this function is shown in Figure 26.31 and Figure 26.32.

Please don't use this function when there is not the difference between the rising transfer time and the falling transfer time, there is a possibility of deteriorating the reception margin of a communication partner.

Table 26.31 The acceptable value of CCR4.AET and CCR4.ATT (asynchronous mode using internal clock) (1 of 2)

ABCSE	ABCS	The number of base clock cycles/1bit	The acceptable value of CCR4	
			AET	ATT[2:0]
1	x	6	0	000b – 101b
			1	
0	1	8	0	000b – 111b
			1	

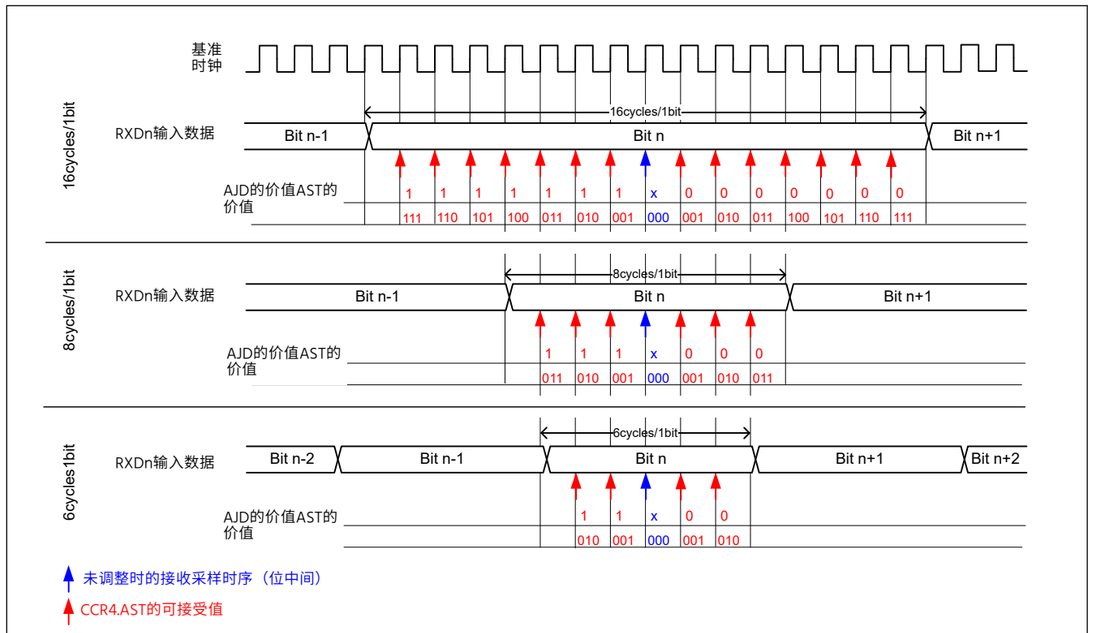


Figure 26.27 接收采样定时调整操作概述（使用内部时钟的异步模式）

26.3.11 调整发送时间的功能（异步模式）

在经由光电耦合器等的通信中，当TXDn输出信号的上升或下降过渡时间较长时，通信伙伴接收到钝化波形。在这种情况下，接收裕量可能会受到影响。

在这些情况下，使用调整发送时间的功能使通信伙伴在位中间进行采样。

当CCR4.ATEN为1时，该功能可以对用CCR4.AET设置的边沿按以下公式计算的时序调整边沿时序。

调整边沿时序=基准时钟*CCR4.ATT[2:0]

另外，调整边沿时序的上限是通过设置基本时钟周期来限制的。详见表26.31。

图26.28、图26.29、图26.30为使用该功能的光耦合器通信的传输动作图，使用该功能的操作概要如图26.31、图26.32所示。

请不要在上升传输时间和下降传输时间之间没有差异时使用此功能，这可能会降低通信伙伴的接收裕度。

Table 26.31 CCR4.AET和CCR4.ATT的可接受值（使用内部时钟的异步模式）（1of2）

ABCSE	ABCS	基本时钟周期数1bit	CCR4的可接受值	
			AET	ATT[2:0]
1	x	6	0	000b – 101b
			1	
0	1	8	0	000b – 111b
			1	

Table 26.31 The acceptable value of CCR4.AET and CCR4.ATT (asynchronous mode using internal clock) (2 of 2)

ABCSE	ABCS	The number of base clock cycles/1bit	The acceptable value of CCR4	
			AET	ATT[2:0]
0	0	16	0	000b – 111b
			1	

Note: x: Don't care
Note: When the value of ACTR.AET/ATT is out of the acceptable value, this SCI module doesn't adjust transmit timing.

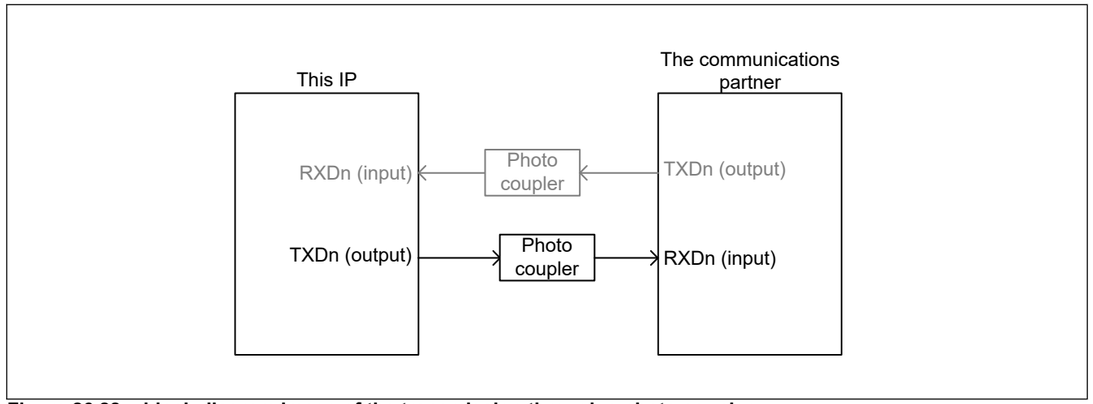


Figure 26.28 block diagram image of the transmission through a photo coupler

Table 26.31 CCR4.AET和CCR4.ATT的可接受值（使用内部时钟的异步模式）(2of2)

ABCSE	ABCS	基本时钟周期数1bit	CCR4的可接受值	
			AET	ATT[2:0]
0	0	16	0	000b – 111b
			1	

Note: x: Don't care
Note: 当ACTR.AETATT的值超出可接受的值时，该SCI模块不调整发送时序。

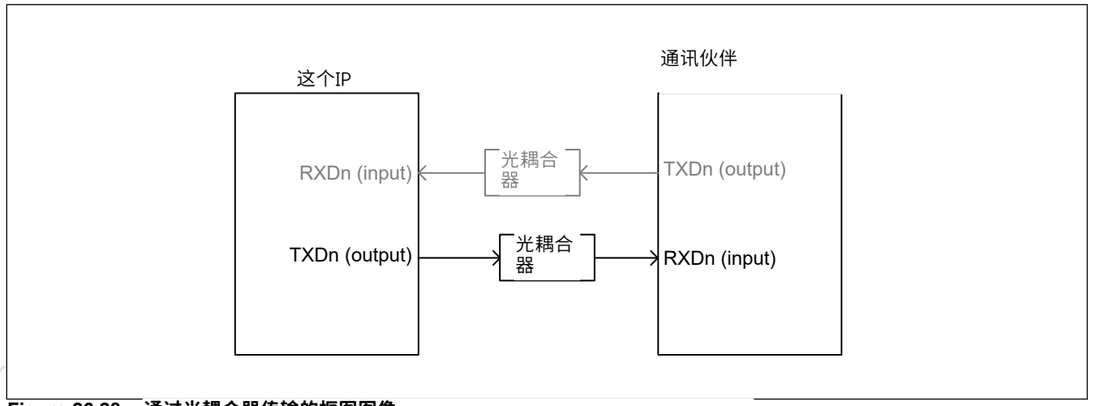
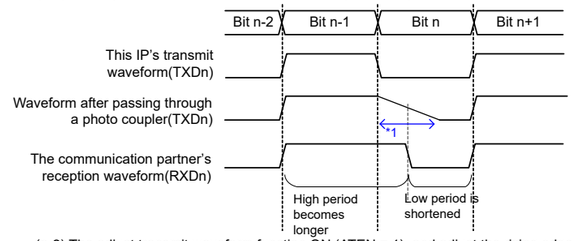


Figure 26.28 通过光耦合器传输的框图图像

(a) In the case of the falling transfer time >> rising transfer time

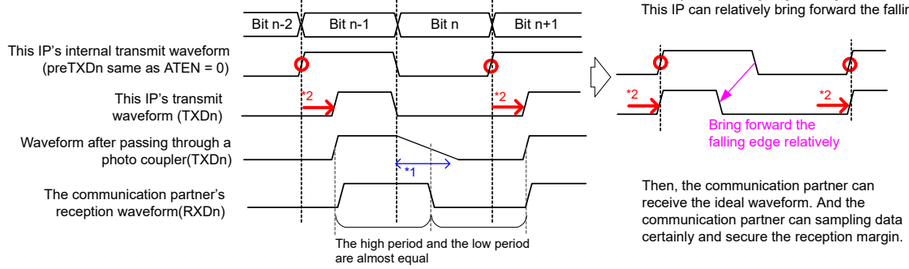
(a-1) The adjust transmit waveform function OFF (ATEN = 0)



The falling edge of Transmission waveform is made dull like the figure on the left.
For the reception waveform of the communication partner, High of Bit n-1 becomes longer and Bit n Low becomes shorter.

As this kind of communication waveform collapses, there is a concern that Low value can not be sampled depending on the sampling timing of the communication partner.

(a-2) The adjust transmit waveform function ON (ATEN = 1), and adjust the rising edge (AET = 0)

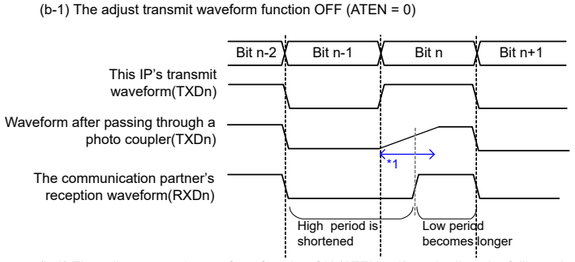


So, adjust the rising edge timing of TXDn waveform.
This IP can relatively bring forward the falling edge.

Then, the communication partner can receive the ideal waveform. And the communication partner can sampling data certainly and secure the reception margin.

(b) In the case of the falling transfer time << rising transfer time

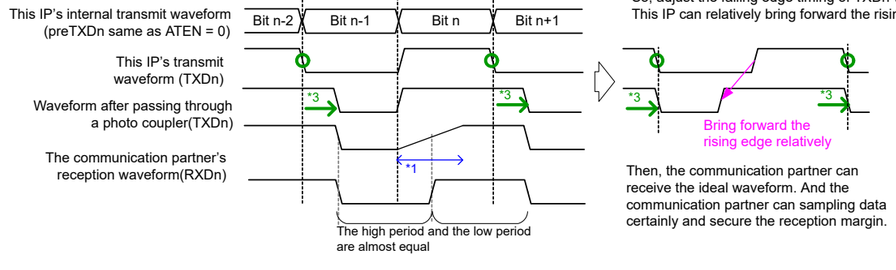
(b-1) The adjust transmit waveform function OFF (ATEN = 0)



The rising edge of transmission waveform is made dull like the figure on the left.
For the reception waveform of the communication partner, Low of Bit n becomes longer and Bit n-1 High becomes shorter.

As this kind of communication waveform collapses, there is a concern that High value can not be sampled depending on the sampling timing of the communication partner.

(b-2) The adjust transmit waveform function ON (ATEN = 1), and adjust the falling edge (AET = 1)



So, adjust the falling edge timing of TXDn waveform.
This IP can relatively bring forward the rising edge.

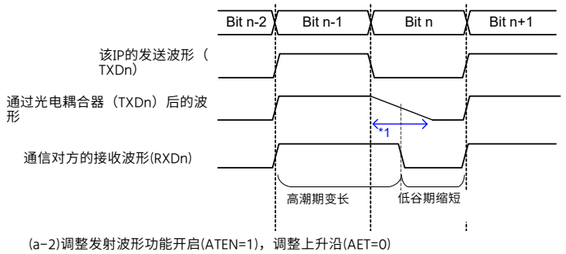
Then, the communication partner can receive the ideal waveform. And the communication partner can sampling data certainly and secure the reception margin.

Note: This waveform shows the operation image of adjustment transmit waveform.
Note 1. The dull period by a photo coupler
Note 2. When CCR4.AET is 0, the rising edge of transmit waveform timing is shifted to back by the setting value of CCR4.ATT[2:0]. This IP transmit waveform bringing forward the falling edge relatively.
Note 3. When CCR4.AET is 1, the falling edge of transmit waveform timing is shifted to back by the setting value of CCR4.ATT[2:0]. This IP transmit waveform bringing forward the rising edge relatively.

Figure 26.29 The overview of transmission operation in the communication through a photo coupler

(a)在下降传输时间>>上升传输时间的情况下

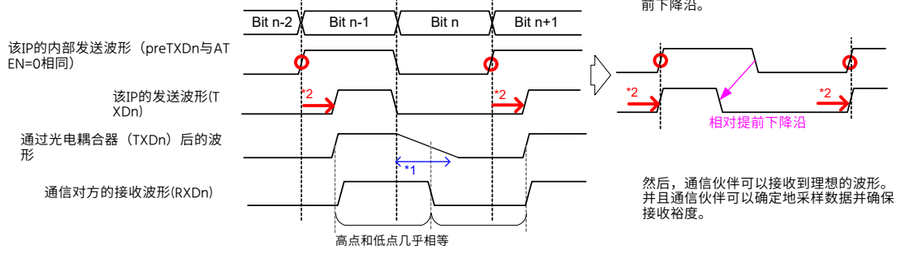
(a-1)调整发射波形功能关闭(ATEN=0)



传输波形的下降沿变暗，如左图。对于通信对方的接收波形，Bitn-1的High变长，BitnLow变短。

由于这种通信波形崩溃，根据通信对方的采样时间，有可能无法采样Low值。

(a-2)调整发射波形功能开启(ATEN=1)，调整上升沿(AET=0)

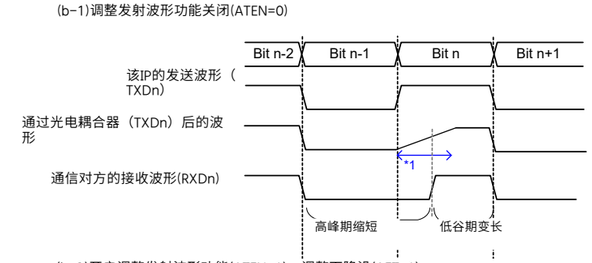


因此，调整TXDn波形的上升沿时序。该IP可以相对提前下降沿。

然后，通信伙伴可以接收到理想的波形。并且通信伙伴可以确定地采样数据并确保接收裕度。

(b)在下降传输时间<<上升传输时间的情况下

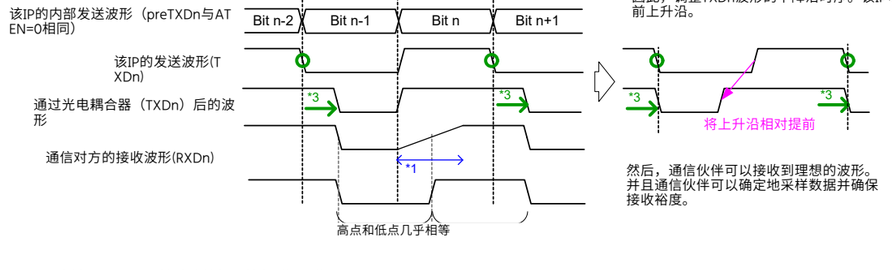
(b-1)调整发射波形功能关闭(ATEN=0)



传输波形的上升沿变暗，如左图。对于通信对方的接收波形，Bitn的Low变长，Bitn-1High变短。

由于这种通信波形崩溃，根据通信对方的采样时间，可能无法采样高值。

(b-2)开启调整发射波形功能(ATEN=1)，调整下降沿(AET=1)



因此，调整TXDn波形的下降沿时序。该IP可以相对提前上升沿。

然后，通信伙伴可以接收到理想的波形。并且通信伙伴可以确定地采样数据并确保接收裕度。

Note: 该波形显示调整发射波形的操作图像。
注1.光电耦合器的无光泽期
注2.当CCR4.AET为0时，发送波形时序的上升沿后移设置值CCR4.ATT[2:0]。该IP传输波形相对提前了下降沿。
注3.当CCR4.AET为1时，发送波形时序的下降沿后移设置值CCR4.ATT[2:0]。该IP传输波形相对提前了上升沿。

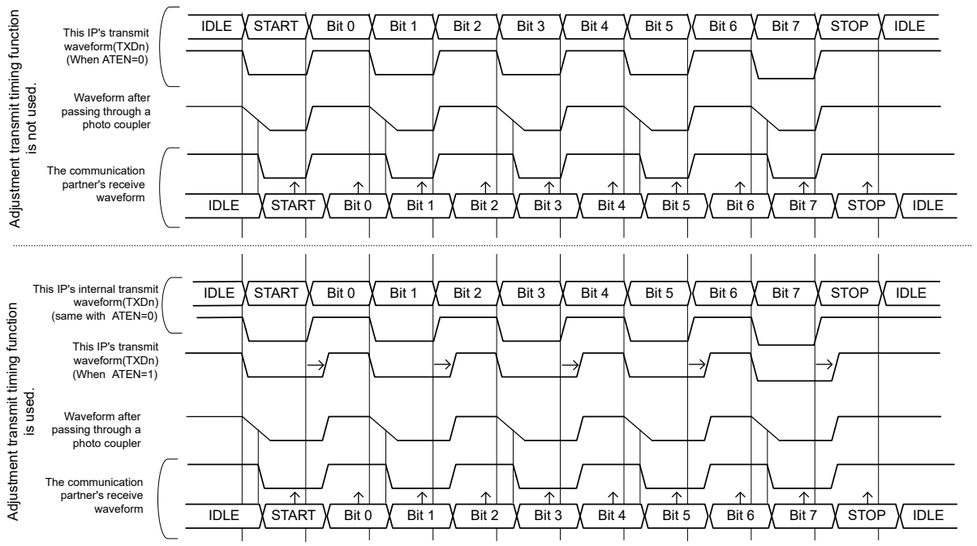
Figure 26.29 光耦合器通信中的传输操作概述

The explanation of transmit waveforms of the communication through a photo coupler using adjust transmit timing function

When using the transmission timing adjustment function, adjust the edge timing of the transmission waveform and correct the reception waveform of the communication partner

The following example is 8 bit long data.

(a) In the case of the falling edge transfer time >> the rising transfer time



(b) In the case of the falling edge transfer time << the rising transfer time

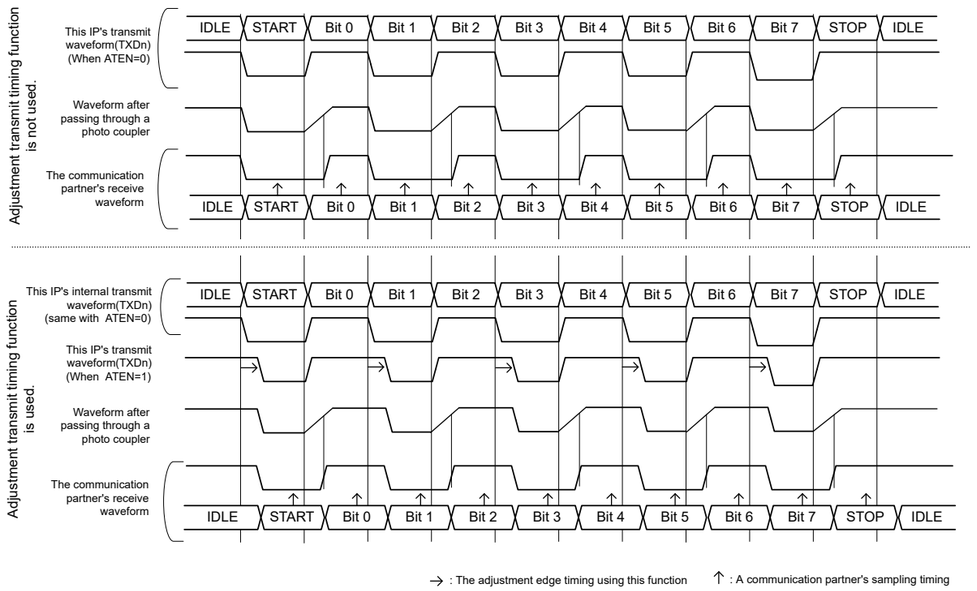
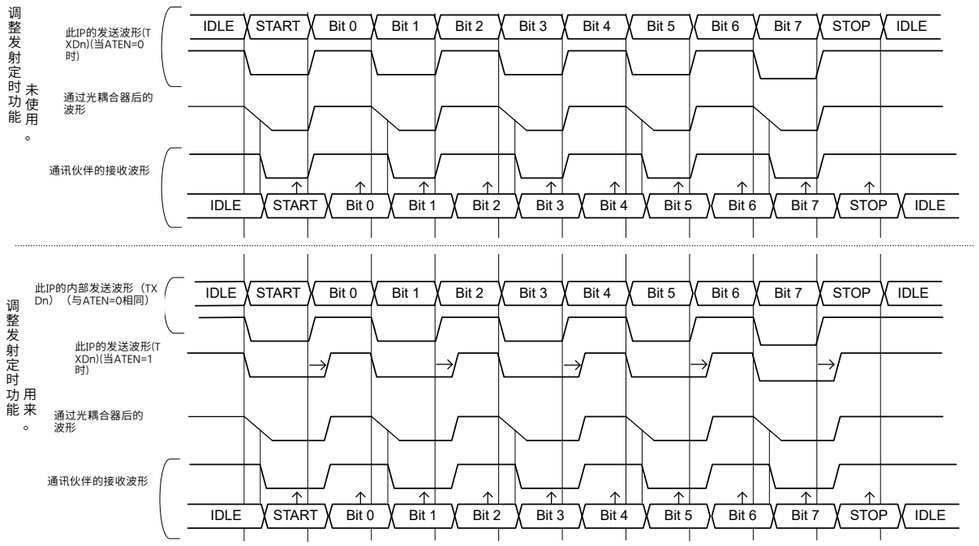


Figure 26.30 The explanation for the transmit waveform through a photo coupler

使用调整发射定时功能通过光电耦合器进行通信的发射波形说明

使用发送定时调整功能时，调整发送波形的边沿定时，修正通信对方的接收波形。下例为8位长的数据。

(a)在下降沿传输时间>>上升沿传输时间的情况下



(b)在下降沿传输时间<<上升沿传输时间的情况下

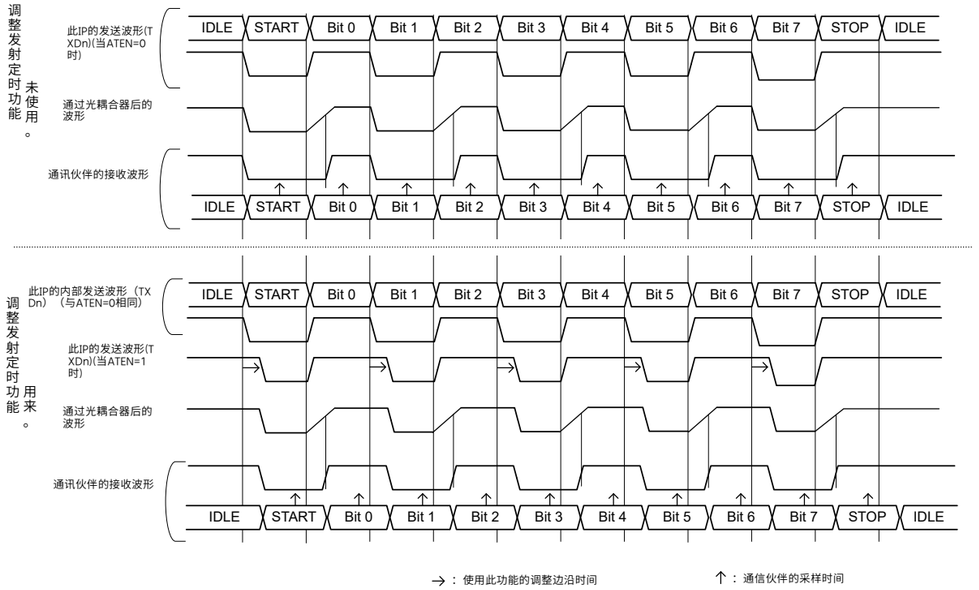
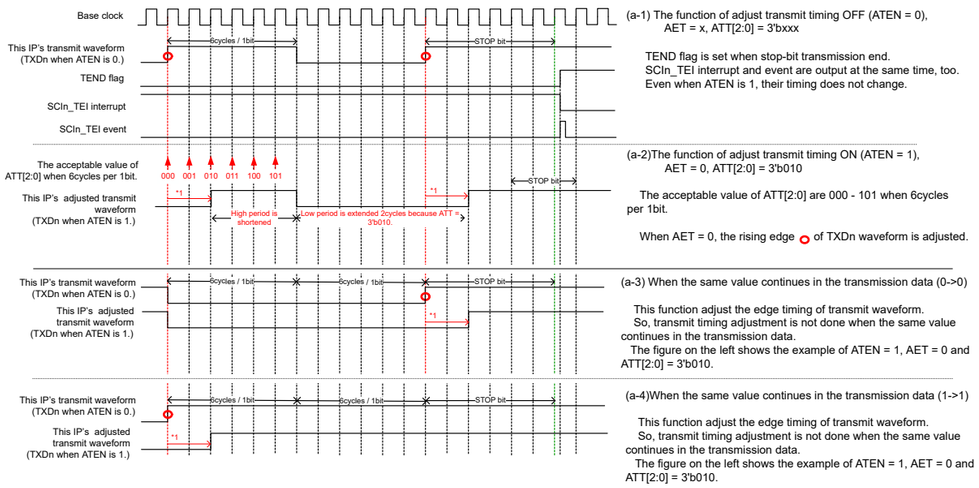


Figure 26.30 通过光电耦合器的发射波形的解释

The operation explanation of adjustment the transmit timing

(a) In the case of the falling transfer time >> rising transfer time
In this case, the high period of a communication partner's reception waveform is made long, and the low period is made short.
Therefore, this IP transmits the waveform with the edge relatively brought forward by adjusting the falling edge timing.
Then adjust value(ATT[2:0]) should be set to make equal the low-period/1bit and high-period/1bit for a communication partner.

This function's operation is explained as an example of 6cycles/1bit.



Note 1. The rising edge of transmit timing is shifted to back by the setting value of CCR4.ATT[2:0].

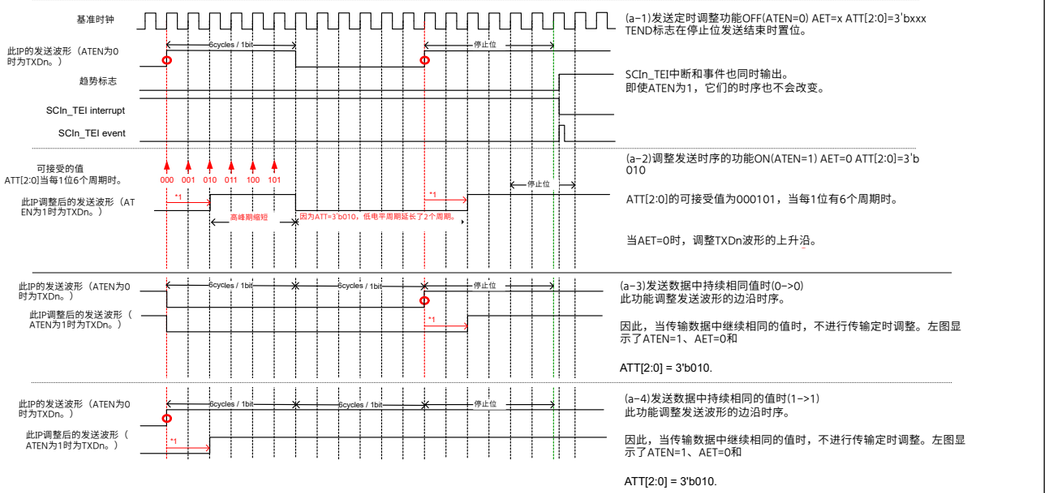
Figure 26.31 The adjustment operation explanation for the transmit timing when AET is 0

调整发送时间的操作说明

(a)在下降传送时间>>上升传送时间的情况下在这种情况下，通信对方的接收波形的高电平周期变长，而低电平周期变短。因此，该IP
通过调整下降沿时序来传输边缘相对提前的波形。

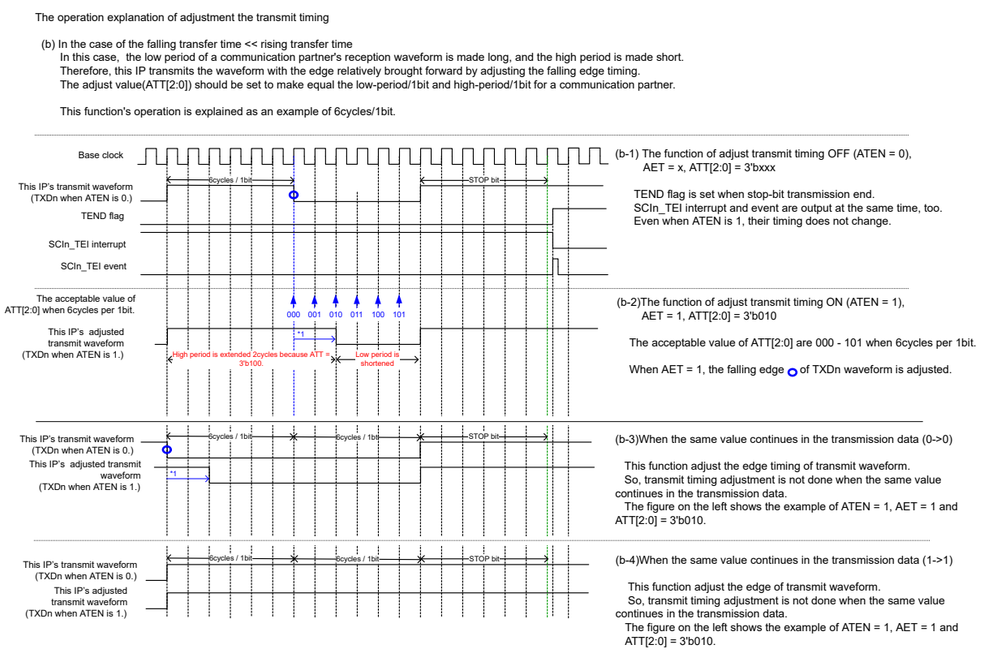
然后调整值（ATT[2:0]）应设置为使通信伙伴的低周期1bit和高周期1bit相等。

该功能的操作以6cycles1bit为例进行说明。



注1.发送时序的上升沿由CCR4.ATT[2:0]的设置值向后移动。

Figure 26.31 AET为0时发射时序调整操作说明



Note 1. The falling edge of transmit timing is shifted to back by the setting value of CCR4.ATT[2:0].

Figure 26.32 The adjustment operation explanation for the transmit timing when AET is 1

26.4 Multi-Processor Communication Function

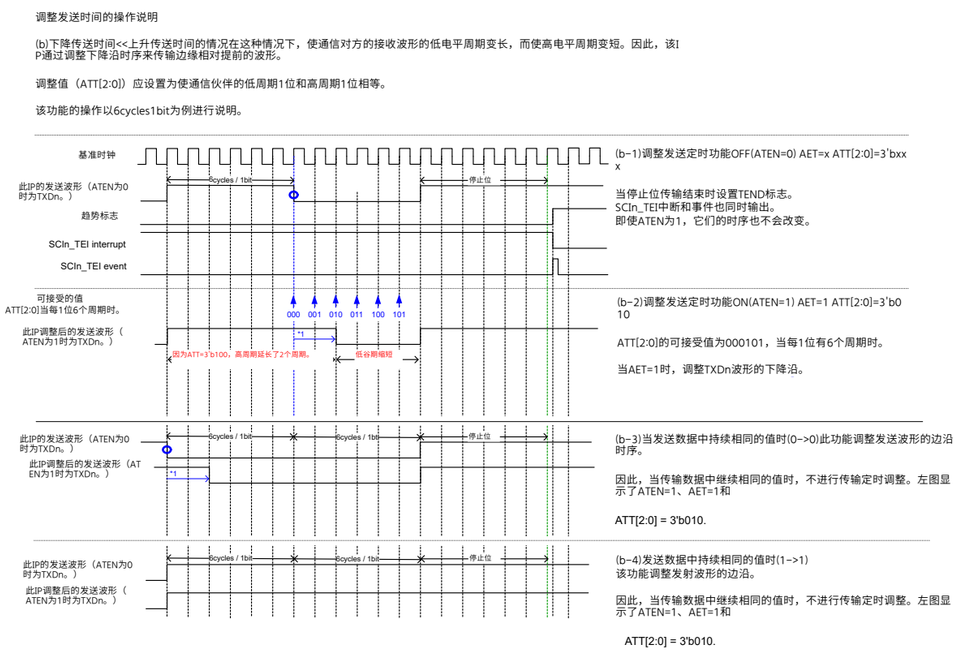
The multi-processor communication function enables the SCI to transmit and receive data between multiple processors by sharing an asynchronous serial communication line that has an added multi-processor bit. In multi-processor communication, a unique ID code is allocated to each receiving station. Serial communication cycles consist of an ID transmission cycle to specify the receiving station and a data transmission cycle to transmit data to the specified receiving station.

The multi-processor bit is used to distinguish between the ID transmission cycle and the data transmission cycle:

- When the multi-processor bit is set to 1, the transmission cycle is the ID transmission cycle
- When the multi-processor bit is set to 0, the transmission cycle is the data transmission cycle

Figure 26.33 shows an example of communication between processors using a multi-processor format. First, a transmitting station transmits communication data in which the multi-processor bit set to 1 is added to the ID code of the receiving station. Next, the transmitting station transmits communication data in which the multi-processor bit set to 0 is added to the transmit data. After receiving communication data with the multi-processor bit set to 1, the receiving station compares the received ID with the ID of the receiving station itself. If the two match, the receiving station receives communication data that is subsequently transmitted. If the received ID does not match with the ID of the receiving station, the receiving station skips the communication data until it receives data in which the multi-processor bit is set to 1.

RTS control cannot be used at the time of multi-processor communication function use because this is a function corresponding to one-to-many communications.



注1.发送时序的下降沿后移CCR4.ATT[2:0]的设置值。

Figure 26.32 AET为1时发射时序调整操作说明

26.4 多处理器通信功能

多处理器通信功能使SCI能够通过共享一条增加了多处理器位的异步串行通信线路在多个处理器之间发送和接收数据。在多处理器通信中，为每个接收站分配一个唯一的ID代码。串行通信周期由指定接收站的ID传输周期和向指定接收站传输数据的数据传输周期组成。

多处理器位用于区分ID传输周期和数据传输周期：

- 当多处理器位设置为1时，传输周期为ID传输周期
- 当多处理器位设置为0时，传输周期为数据传输周期

图26.33显示了使用多处理器格式的处理器之间的通信示例。首先，发送站发送将设置为1的多处理器位添加到接收站的ID码的通信数据。接着，发送站发送在发送数据中附加了多处理器比特为0的通信数据。接收站接收到多处理器位设置为1的通信数据后，将接收到的ID与接收站自身的ID进行比较。如果两者匹配，则接收站接收随后发送的通信数据。如果接收到的ID与接收站的ID不匹配，则接收站跳过通信数据，直到接收到多处理器位设置为1的数据。

在使用多处理器通信功能时，不能使用RTS控制，因为这是一个对应于一对多通信的功能。

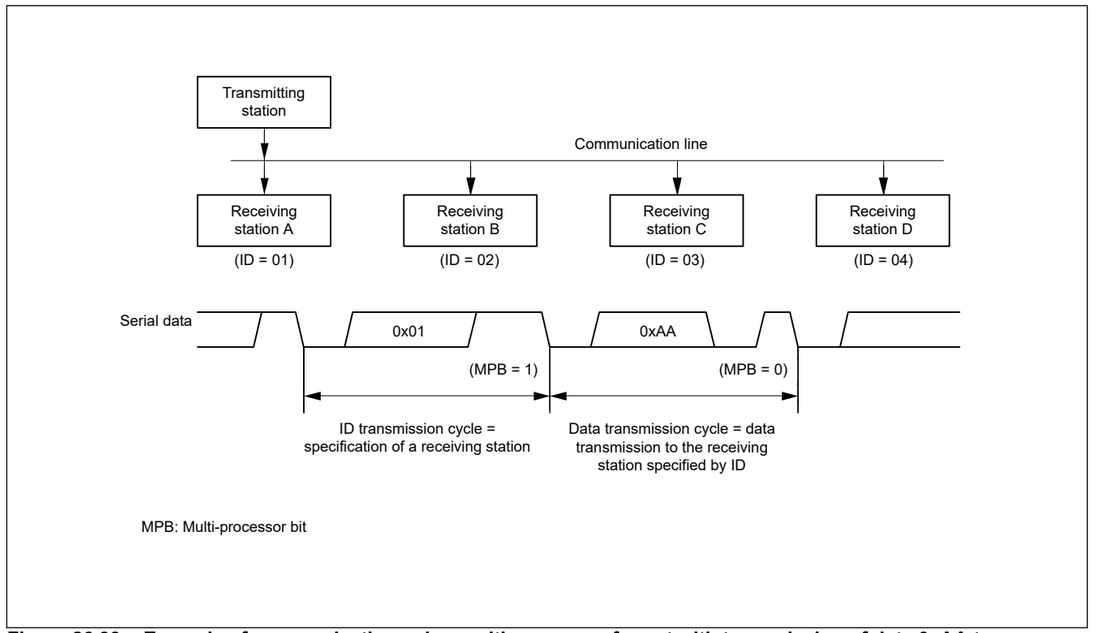


Figure 26.33 Example of communication using multi-processor format with transmission of data 0xAA to receiving station A

(1) Non-FIFO selected

To support this function, the SCI provides the CCR0.MPIE bit. When the MPIE bit is set to 1, the following operations are disabled until the reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from the RSR register to the RDR register
- Detection of a receive error
- Setting of the respective RDRF, ORER, and FER status flags in the CSR register

When the SCI receives a character in which the multi-processor bit is set to 1, the RDR.MPB bit is set to 1 and the CCR0.MPIE bit is automatically cleared, returning the SCI to non-multi-processor reception operation. If the CCR0.RIE bit is set to 1, an SCIn_RXI interrupt is generated.

When the multi-processor format is specified, the parity bit function is disabled. Apart from this, there is no difference from operation in non-multi-processor asynchronous mode. The clock used for the multi-processor communication is the same as the clock used in non-multi-processor asynchronous mode.

(2) FIFO selected

For data transmission, software must write data to TDR.MPBT (Multi-Processor Bit Transfer) that corresponds to transmit data in TDR.TDAT. For data reception, the multi-processor bit that is part of the receive data is written to RDR.MPB and receive data is written to RDR.RDAT.

When the MPIE bit is set to 1, the following operations are disabled until reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from the RSR register to the RDR.RDAT register
- Detection of a receive error
- Detection of DR
- Setting of the respective RDRF, ORER, and FER status flags in the CSR register

When the SCI receives a character in which the multi-processor bit is set to 1, the RDR.MPB bit is set to 1 and receive data is written to receive-FIFO(RDR.RDAT). The CCR0.MPIE bit is automatically cleared, returning the SCI to normal reception operation. If the CCR0.RIE bit is set to 1, an SCIn_RXI interrupt is generated.

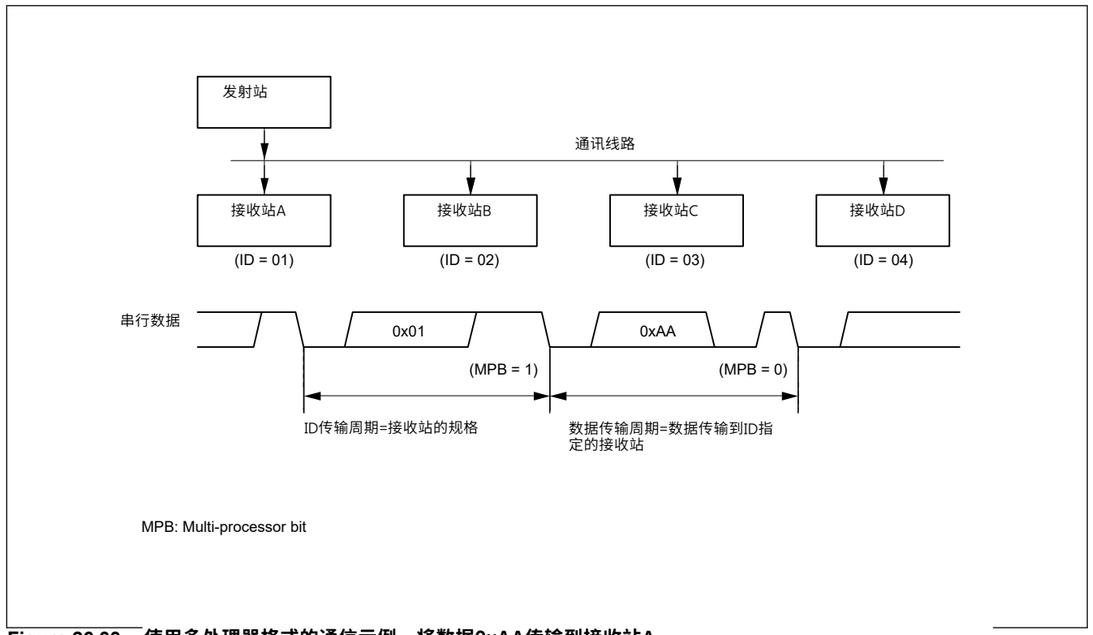


Figure 26.33 使用多处理器格式的通信示例，将数据0xAA传输到接收站A

(1) Non-FIFO selected

为了支持这个功能，SCI提供了CCR0.MPIE位。当MPIE位设置为1时，以下操作被禁止，直到接收到多处理器位设置为1的数据：

- 将接收数据从RSR寄存器传送到RDR寄存器
- 接收错误检测
- 在CSR寄存器中分别设置RDRF、ORER和FER状态标志

当SCI接收到多处理器位设置为1的字符时，RDR.MPB位设置为1，并且
CCR0.MPIE位自动清零，将SCI返回到非多处理器接收操作。如果CCR0.RIE位设置为1，则产生SCIn_RXI中断。

当指定多处理器格式时，奇偶校验位功能被禁用。除此之外，与非多处理器异步模式下的操作没有区别。多处理器通信使用的时钟与非多处理器异步模式使用的时钟相同。

(2) FIFO selected

对于数据传输，软件必须将数据写入对应于TDR.TDAT中传输数据的TDR.MPBT（多处理器位传输）。对于数据接收，作为接收数据一部分的多处理器位写入RDR.MPB，接收数据写入RDR.RDAT。

当MPIE位设置为1时，以下操作被禁止，直到接收到多处理器位设置为1的数据：

- 将接收数据从RSR寄存器传送到RDR.RDAT寄存器
- 接收错误检测
- DR检测
- 在CSR寄存器中分别设置RDRF、ORER和FER状态标志

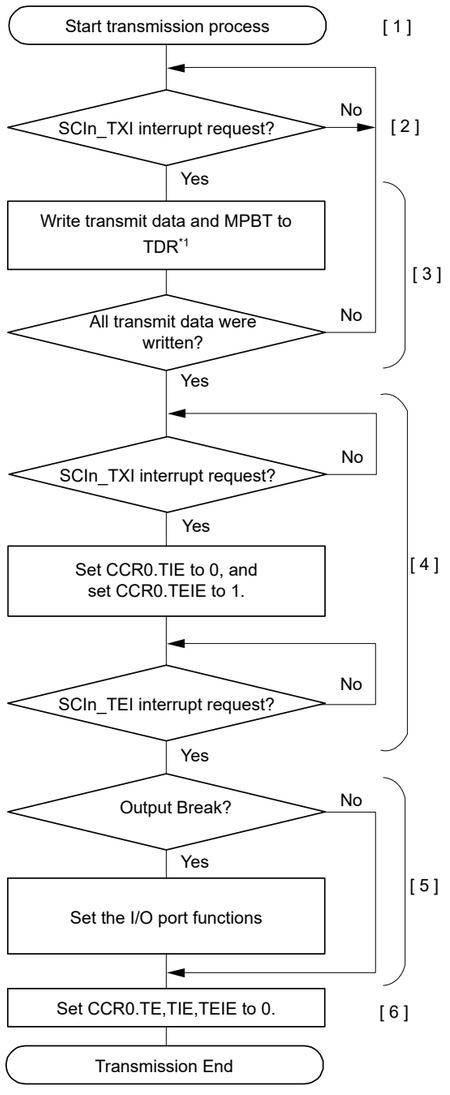
当SCI接收到一个多处理器位设置为1的字符时，RDR.MPB位设置为1，接收数据写入接收FIFO(RDR.RDAT)。CCR0.MPIE位自动清零，使SCI恢复正常接收操作。如果CCR0.RIE位设置为1，则产生SCIn_RXI中断。

When the multi-processor format is specified, the parity bit function is disabled. Apart from this, there is no difference from operation in normal asynchronous mode with FIFO selected.

26.4.1 Multi-Processor Serial Data Transmission

(1) Non-FIFO selected

Figure 26.34 shows an example flow of multi-processor data transmission. In the ID transmission cycle, the ID must be transmitted with the TDR.MPBT bit set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as operations in asynchronous mode.



[1] Start transmission process

[2] SCIn_TXI interrupt request:
The transmit-data-empty-interrupt(SCIn_TXI) is generated at following conditions.
When set TE and TIE to 0 at same time.
When transmission-data forwards to TSR from TDR.

[3] Serial transmission continuation procedure:
To continue serial transmission write transmit data and MPBT setting value to TDR*1 once by using a SCIn_TXI. Transmit data and MPBT setting value can also be written by activating the DMAC or DTC.

[4] If you use SCIn_TEI, set TIE = 0 and TEIE = 1 after writing the last-transmit-data to TDR*1 and transmission is started.

[5] Break output at the end of serial transmission:
To output a break, it is necessary to set SPB2IO and SPB2DT, for output status setting when TE is 0. (If you set these bits at initialization, you can skip this step.)

[6] Set CCR0.TE,TIE,TEIE to 0.

Note 1. In case of byte access with data length 9 bits or to write MPBT bit, write transmit data in order of TDR[15:8] and TDR[7:0].

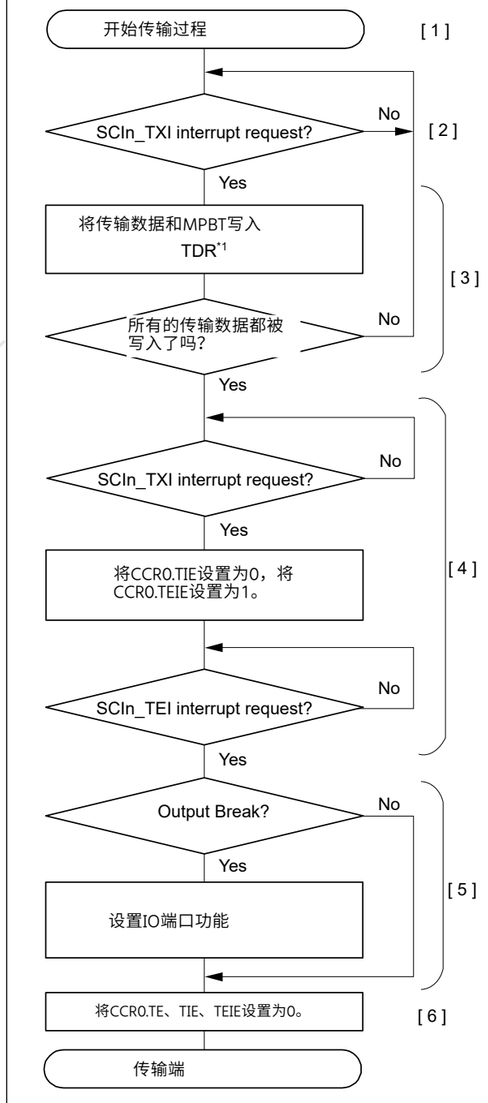
Figure 26.34 Example flow of multi-processor serial transmission with non-FIFO selected

当指定多处理器格式时，奇偶校验位功能被禁用。除此之外，与选择FIFO的正常异步模式下的操作没有区别。

26.4.1 多处理器串行数据传输

(1) Non-FIFO selected

图26.34显示了一个多处理器数据传输的示例流程。在ID传输周期，ID必须在TDR.MPBT位设置为1的情况下传输。在数据传输周期，数据必须在MPBT位设置为0的情况下传输。其余操作与操作相同在异步模式下。



[1]开始传输过程

[2] SCIn_TXI interrupt request:
发送数据空中断(SCIn_TXI)在以下条件下生成。当同时设置TE和TIE为0时。

当传输数据从TDR转发到TSR时。

[3]串行传输继续过程：要继续串行传输，使用SCIn_TXI将传输数据和MPBT设置值写入TDR*1一次。发送数据和MPBT设置值也可以通过激活DMAC或DTC来写入。

[4]如果您使用SCIn_TEI，请在将最后发送数据写入TDR*1并开始发送后设置TIE=0和TEIE=1。

[5]串行传输结束时的中断输出：要输出中断，需要设置SPB2IO和SPB2DT，用于TE为0时的输出状态设置。（如果在初始化时设置了这些位，则可以跳过此步骤。）

[6] 将CCR0.TE、TIE、TEIE设置为0。

注1.在数据长度为9位的字节访问或写入MPBT位的情况下，按照TDR[15:8]的顺序写入发送数据和TDR[7:0].

Figure 26.34 选择非FIFO的多处理器串行传输示例流程

(2) FIFO selected

Figure 26.35 shows an example of data format that is written to transmit-FIFO (TDR) in multi-processor mode. The TDR.MPBT bit is set to 1. Data is set to transmit-FIFO (TDR) with the correct data length. Write 0 for unused bits.

Data Length	Register setting		Transmit data in TDR[15:0]															
	CCR3. CHR[1:0]		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bit	1	1	—	—	—	—	—	—	MPBT	—	—	TDAT[6:0]						
8 bit	1	0	—	—	—	—	—	—	MPBT	—	TDAT[7:0]							
9 bit	0	Don't Care	—	—	—	—	—	—	MPBT	TDAT[8:0]								

Note: —: Invalid. The write value should be 0.

Figure 26.35 Data format written to transmit-FIFO (TDR) in multi-processor mode with FIFO selected

Figure 26.36 shows an example flow of multi-processor serial transmission with FIFO selected. In the ID transmission cycle, the ID must be transmitted with the TDR.MPBT bit set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as operations in asynchronous mode with FIFO selected.

(2) FIFO selected

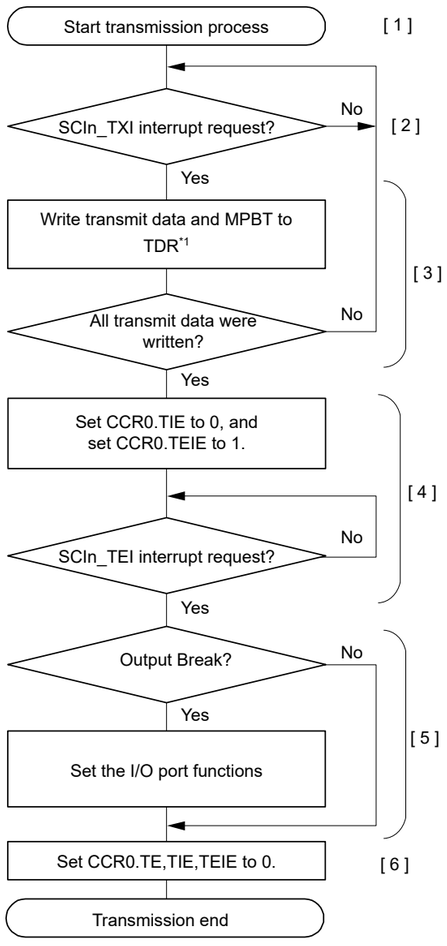
图26.35显示了在多处理器模式下写入发送FIFO(TDR)的数据格式示例。TDR.MPBT位设置为1。数据设置为具有正确数据长度的发送FIFO(TDR)。为未使用的位写入0。

数据长度	注册设置		在TDR[15:0]中传输数据															
	CCR3. CHR[1:0]		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bit	1	1	—	—	—	—	—	—	MPBT	—	—	TDAT[6:0]						
8 bit	1	0	—	—	—	—	—	—	MPBT	—	TDAT[7:0]							
9 bit	0	Don't Care	—	—	—	—	—	—	MPBT	TDAT[8:0]								

Note: —：无效的。写入值应为0。

Figure 26.35 在选择FIFO的多处理器模式下写入发送FIFO(TDR)的数据格式

图26.36显示了选择FIFO的多处理器串行传输示例流程。在ID传输周期，ID必须在TDR.MPBT位设置为1的情况下传输。在数据传输周期，数据必须在MPBT位设置为0的情况下传输。其余操作与操作相同在异步模式下选择FIFO。



[1] Start transmission process
To enable SCIn_TXI interrupt at he start of transmission, set TE and TIE to 1 with one instructions at the same time. And set CCR3.FM,MP to 1.

[2] SCIn_TXI interrupt request:
The transmit-data-empty-interrupt(SCIn_TXI) is generated when transmission-data forwards to TSR from the transmit-FIFO(TDR) and the number of transmit-data written in the transmit-FIFO is equal to or less than the transmit-FIFO threshold.

[3] Serial transmission continuation procedure:
To continue serial transmission, write all transmit data and MPBT setting value to the transmit-FIFO(TDR) by using a SCIn_TXI interrupt. Transmit data and MPBT setting value can also be written to the transmit- FIFO(TDR) by activating the DMAC or DTC.

[4] If you use SCIn_TEI, set TIE = 0 and TEIE = 1 after writing the last-transmit-data to TDR*1.

[5] Break output at the end of serial transmission:
To output a break, it is necessary to set SPB2IO and SPB2DT, for output status setting when TE is 0.
(If you set these bits at initialization, you can skip this step.)

[6] Set CCR0.TE,TIE,TEIE to 0.

Note 1. In case of byte access with data length 9 bits or to write MPBT bit, write transmit data in order of TDR[15:8] and TDR[7:0].

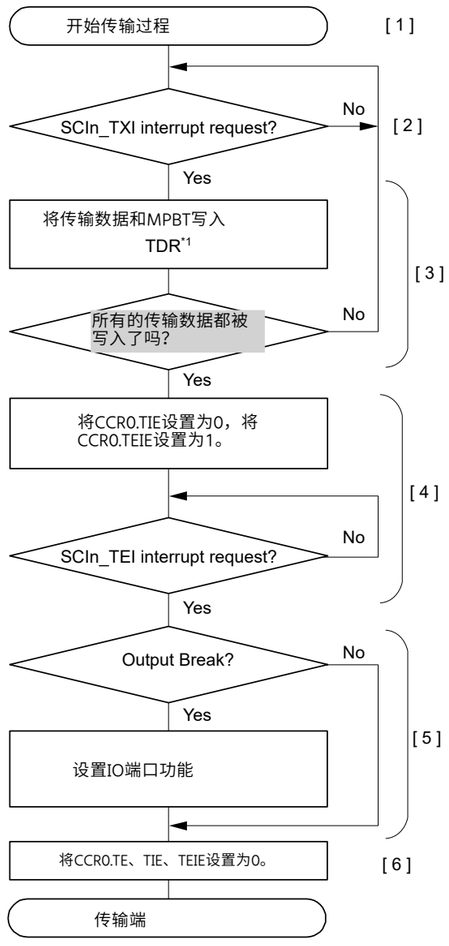
Figure 26.36 Example flow of serial transmission in multi-processor mode with FIFO selected

26.4.2 Multi-Processor Serial Data Reception

(1) Non-FIFO selected

Figure 26.38 and Figure 26.39 are example flows of multi-processor serial reception. When the CCR0.MPIE bit is set to 1, reading communication data is skipped until reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data is transferred to the RDR register, and the SCIn_RXI interrupt request is generated. The rest of the operations are the same as operations in asynchronous mode.

Figure 26.37 shows an example operation for data reception.



[1]开始传输过程要在传输开始时启用SCIn_TXI中断，请将TE和TIE设置为1，同时使用一条指令。并将CCR3.FM MP设置为1。

[2] SCIn_TXI interrupt request:
当传输数据从传输FIFO(TDR)转发到TSR并且写入传输FIFO的传输数据数量等于或小于传输数据时，会产生传输数据空中断(SCIn_TXI)先进先出阈值。

[3] 串行传输继续过程：
要继续串行传输，请使用SCIn_TXI中断将所有传输数据和MPBT设置值写入传输FIFO(TDR)。发送数据和MPBT设置值也可以通过激活DMAC或DTC写入到发送FIFO(TDR)。

[4]如果您使用SCIn_TEI，请在将last-transmit-data写入TDR*1后设置TIE=0和TEIE=1。

[5]串行传输结束时的中断输出：要输出中断，需要设置SPB2IO和SPB2DT，用于TE为0时的输出状态设置。（如果在初始化时设置了这些位，则可以跳过此步骤。）

[6] 将CCR0.TE、TIE、TEIE设置为0。

注1.在数据长度为9位的字节访问或写入MPBT位的情况下，按照TDR[15:8]的顺序写入发送数据和TDR[7:0].

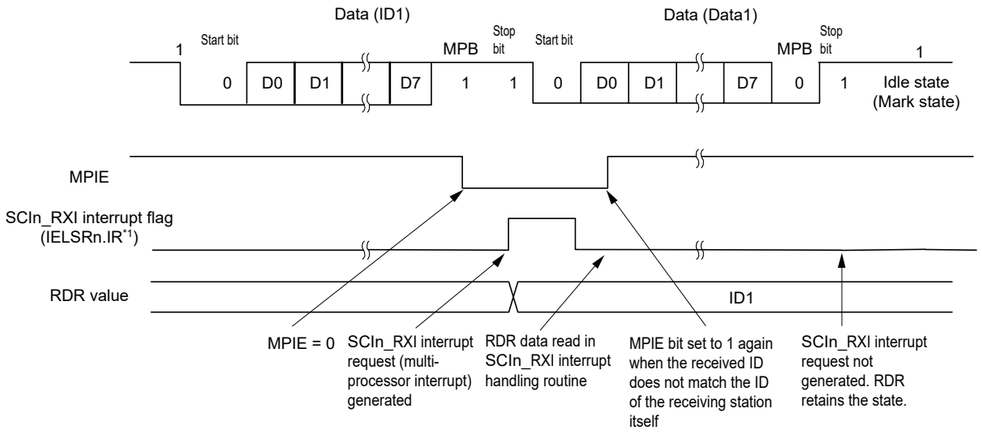
Figure 26.36 选择FIFO的多处理器模式下的串行传输示例流程

26.4.2 多处理器串行数据接收

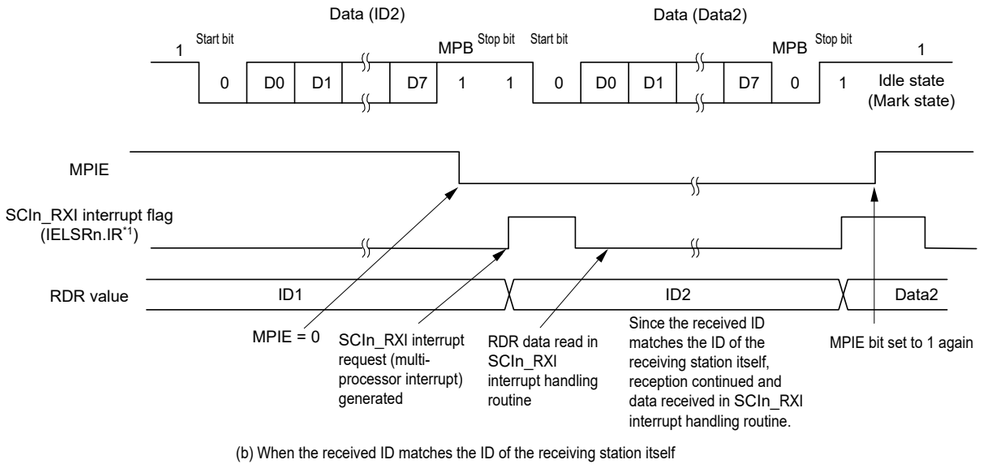
(1) Non-FIFO selected

图26.38和图26.39是多处理器串行接收的示例流程。当CCR0.MPIE位设置为1时，将跳过读取通信数据，直到接收到多处理器位设置为1的通信数据。当接收到多处理器位设置为1的通信数据时，接收到的数据被传送到RDR寄存器，并产生SCIn_RXI中断请求。其余操作与异步模式下的操作相同。

图26.37显示了数据接收的示例操作。



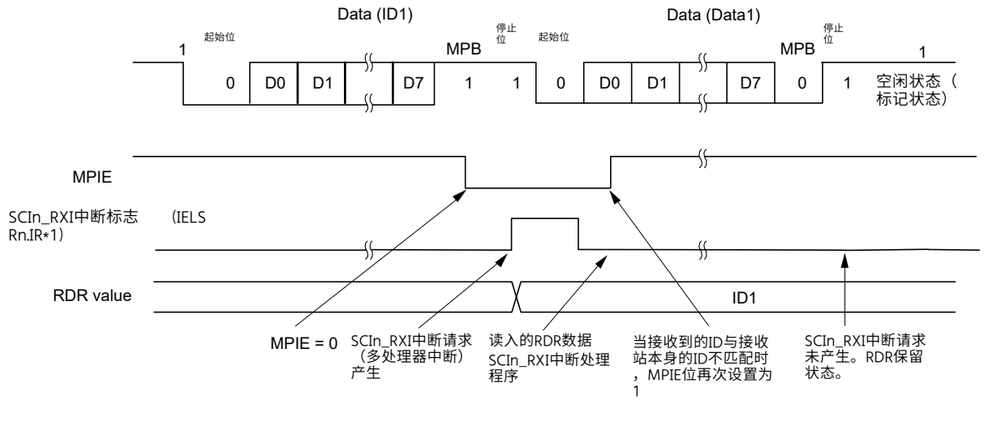
(a) When the received ID does not match the ID of the receiving station itself



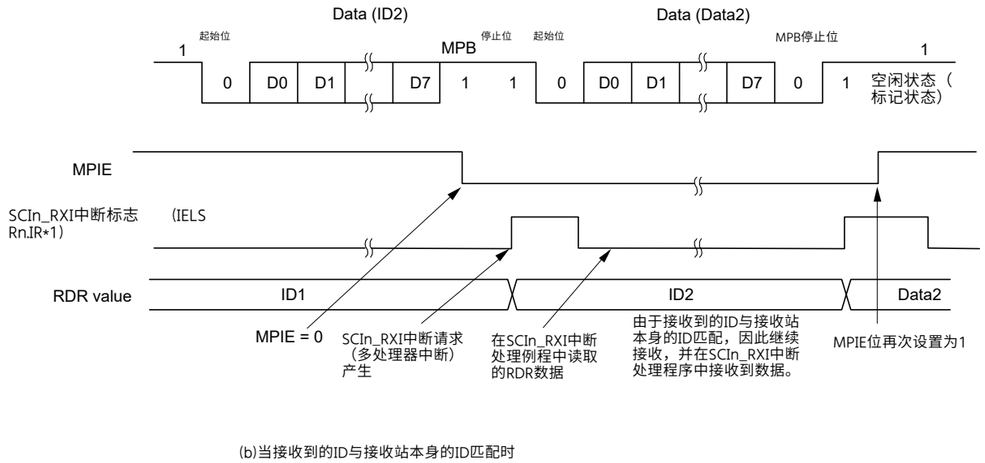
(b) When the received ID matches the ID of the receiving station itself

Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.37 Example of SCI reception with 8-bit data, multi-processor bit, and 1 stop bit



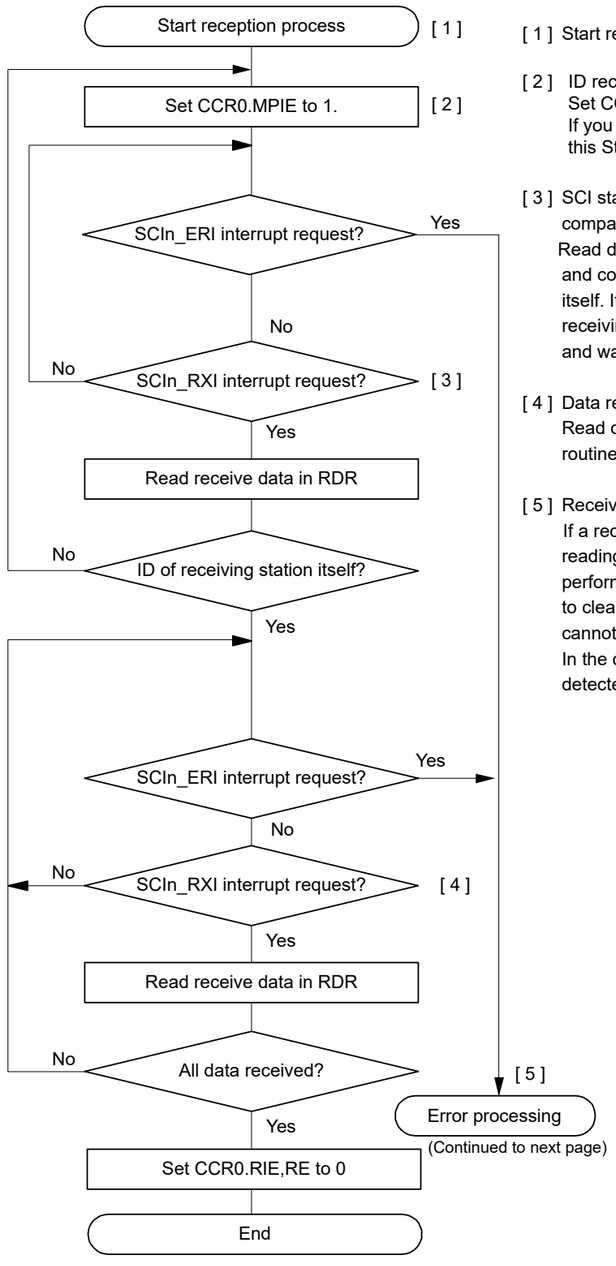
(a)当接收到的ID与接收站本身的ID不匹配时



(b)当接收到的ID与接收站本身的ID匹配时

注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.37 使用8位数据、多处理器位和1个停止位的SCI接收示例



[1] Start reception process

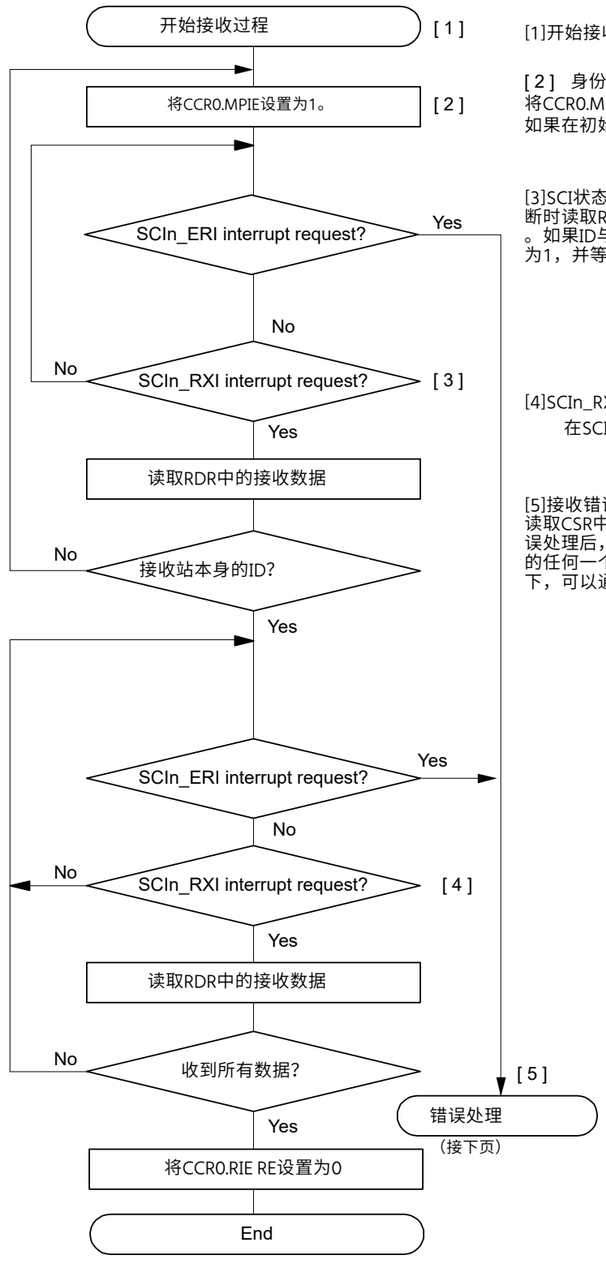
[2] ID reception cycle:
Set CCR0.MPIE to 1. and wait for ID reception.
If you set this bits at initialization([1]), you can skip this Step.

[3] SCI status confirmation and reception and comparison of ID:
Read data in RDR at the first SCIn_RXI interrupt and compare it with the ID of the receiving station itself. If the ID does not match the ID of the receiving station itself, set the MPIE bit to 1 again, and wait for another SCIn_RXI interrupt request.

[4] Data reception at an SCIn_RXI interrupt:
Read data in RDR once in the SCIn_RXI interrupt routine.

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading ORER and FER flags in CSR. After performing the appropriate error processing be sure to clear the ORER and FER flags. Reception cannot be resumed if any of these flags is set to 1. In the case of a framing error, a break can be detected by reading CSR.RXDMON bit.

Figure 26.38 Example flow of multi-processor serial reception with non-FIFO selected (1)



[1]开始接收进程

[2] 身份证接收周期：
将CCR0.MPIE设置为1。并等待ID接收。
如果在初始化时设置此位（[1]），则可以跳过此步骤。

[3]SCI状态确认及ID接收与比较：在第一个SCIn_RXI中断时读取RDR中的数据，并与接收站本身的ID进行比较。如果ID与接收站本身的ID不匹配，再次将MPIE位设置为1，并等待另一个SCIn_RXI中断请求。

[4]SCIn_RXI中断处的数据接收：
在SCIn_RXI中断例程中读取一次RDR中的数据。

[5]接收错误处理和中断检测：如果发生接收错误，则通过读取CSR中的ORER和FER标志来识别错误。执行适当的错误处理后，请务必清除ORER和FER标志。如果这些标志中的任何一个设置为1，则无法恢复接收。在帧错误的情况下，可以通过读取CSR.RXDMON位来检测中断。

Figure 26.38 选择非FIFO的多处理器串行接收示例流程(1)

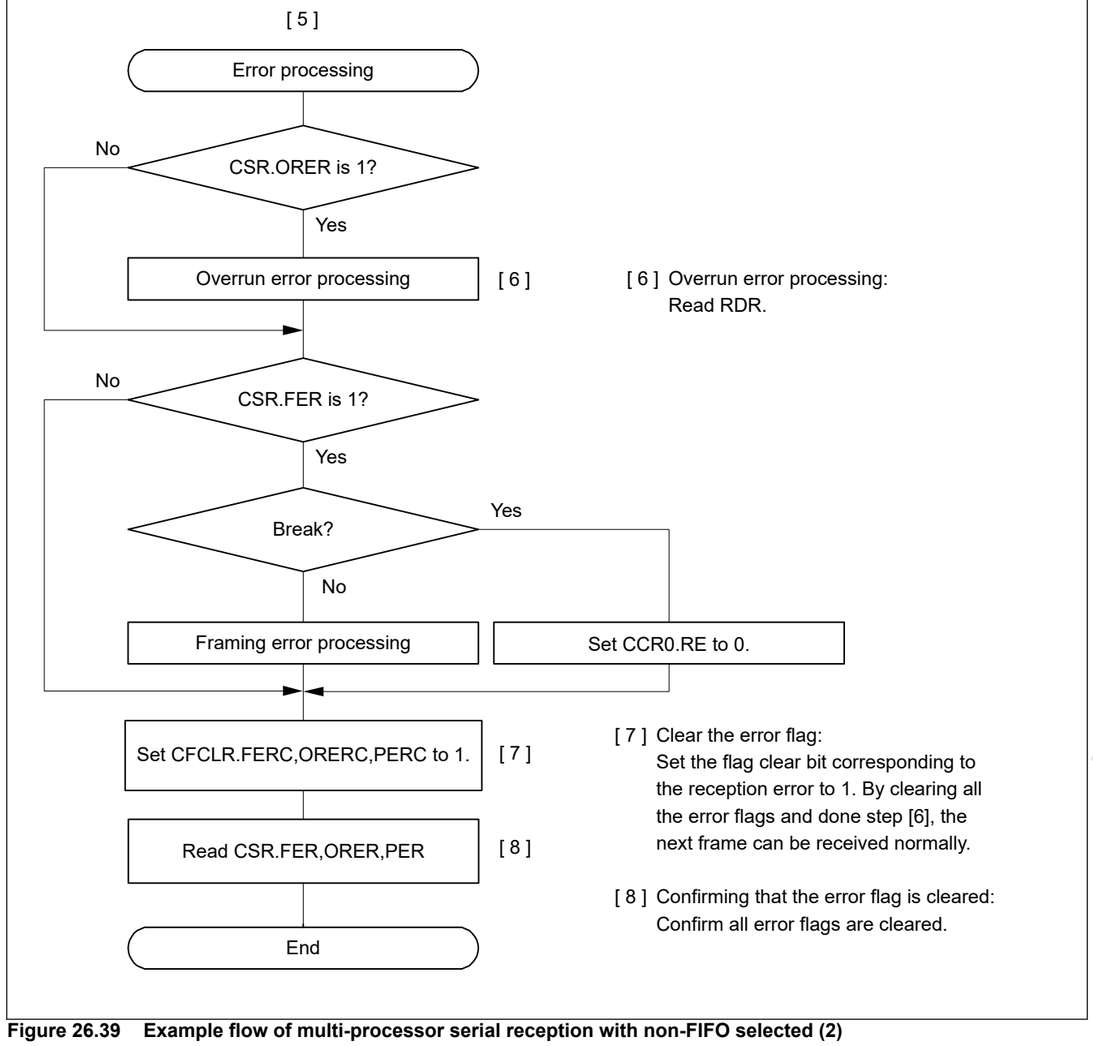


Figure 26.39 Example flow of multi-processor serial reception with non-FIFO selected (2)

(2) FIFO selected

Figure 26.40 shows an example of a data format that is written to receive-FIFO (RDR) in multi-processor mode.

In multi-processor mode, the MPB value that is a part of the receive data is written to the RDR.MPB bit. A value of 0 is written to the RDR.FPER and PER flags. Data is written to receive-FIFO (RDR) with the correct data length. Unused bits are written with 0. When software reads the receive-FIFO (RDR) register, the SCI updates RDR.FFER, FPER, and MPB flags, and receive data (RDAT[8:0]) in receive-FIFO (RDR) with the next data. The FER, PER, and ORER flags in the receive-FIFO (RDR) register always reflect the associated flags in the CSR and FRSR registers.

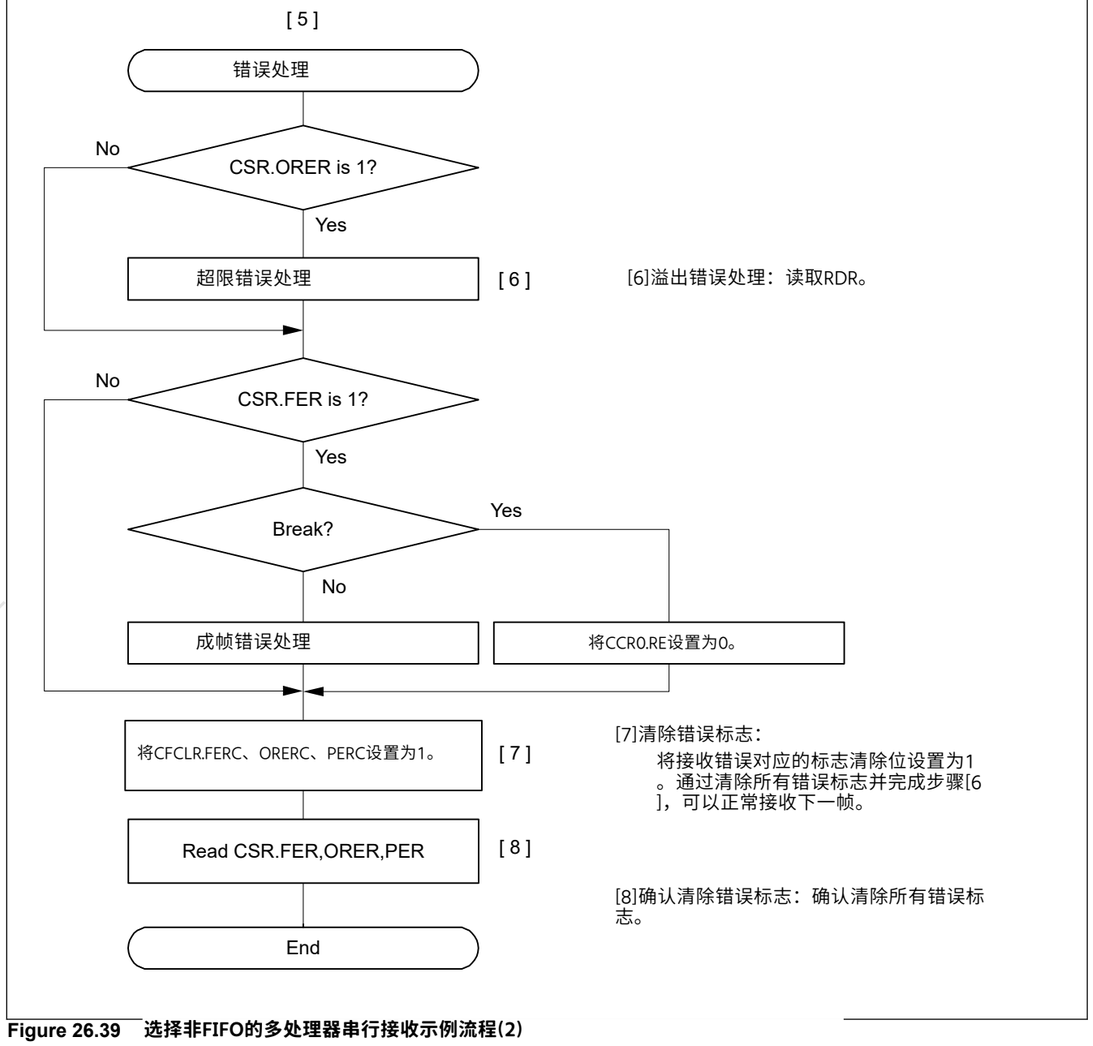


Figure 26.39 选择非FIFO的多处理器串行接收示例流程(2)

(2) FIFO selected

图26.40显示了在多处理器模式下写入接收FIFO(RDR)的数据格式示例。

在多处理器模式下，作为接收数据一部分的MPB值被写入RDR.MPB位。值0写入RDR.FPER和PER标志。数据以正确的数据长度写入接收FIFO(RDR)。未使用的位写入0。当软件读取接收FIFO(RDR)寄存器时，SCI更新RDR.FFER、FPER和MPB标志，并在接收FIFO(RDR)中接收数据(RDAT[8:0])与下一个数据。接收FIFO(RDR)寄存器中的FER、PER和ORER标志始终反映CSR和FRSR寄存器中的相关标志。

Data Length	Register Setting CCR3.CHR[1:0]		Receive data in RDR[31:0] b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7bit	1	1	0	0	0	FFER	FPER	DR	MPB	0	0	RDAT[6:0]						
8bit	1	0	0	0	0	FFER	FPER	DR	MPB	0	RDAT[7:0]							
9bit	0	Don't Care	0	0	0	FFER	FPER	DR	MPB	RDAT[8:0]								
Data Length	CCR3.CHR[1:0]		b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
7bit	1	1	0	0	0	FER	PER	0	0	ORER	0	0	0	0	0	0	0	0
8bit	1	0	0	0	0	FER	PER	0	0	ORER	0	0	0	0	0	0	0	0
9bit	0	Don't Care	0	0	0	FER	PER	0	0	ORER	0	0	0	0	0	0	0	0

Note: When data length is 7bit, it can read always 0 in RDAT[8:7].
When data length is 8bit, it can read always 0 in RDAT[8].

Figure 26.40 Data format stored in receive-FIFO (RDR) in multi-processor mode with FIFO selected

Figure 26.41 shows an example flow of multi-processor data reception with FIFO selected. When the CCR0.MPIE is set to 1, reading communication data is skipped until reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data, MPB and associated errors are transferred to the receive-FIFO (RDR) register. The CCR0.MPIE bit is automatically cleared and normal reception continues.

If a framing error occurs and the CSR.FER flag is set to 1, the SCI continues data reception. The rest of the operations are the same as operations in asynchronous mode with FIFO selected.

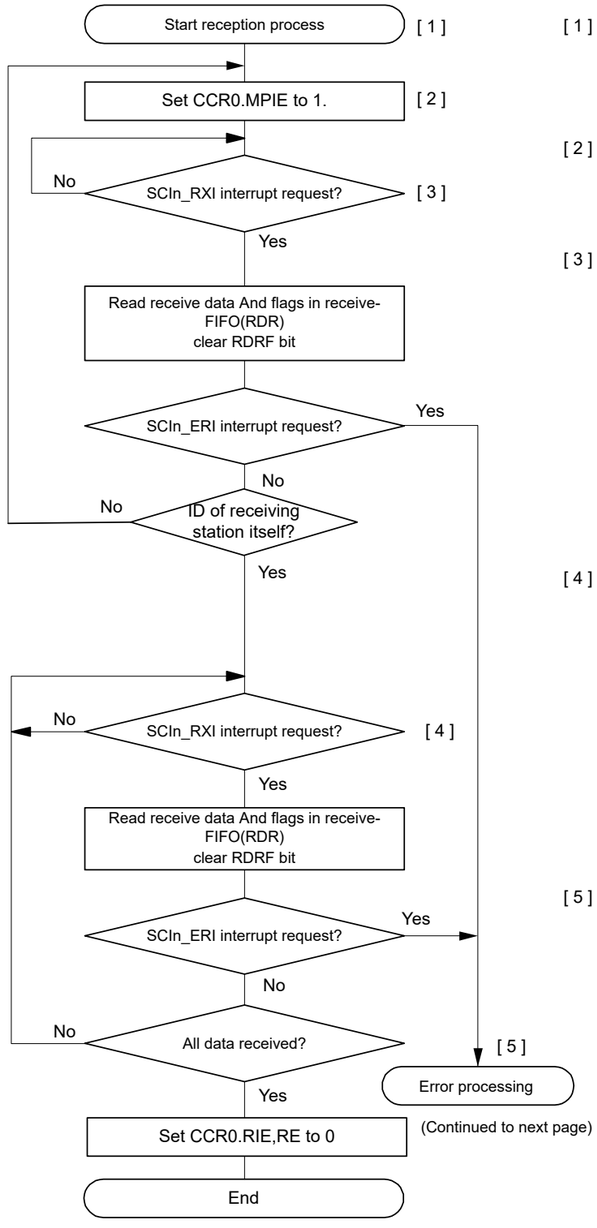
数据长度	CCR3.CHR[1:0]寄存器设置		在RDR[31:0]中接收数据 b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7bit	1	1	0	0	0	FFER	FPER	DR	MPB	0	0	RDAT[6:0]						
8bit	1	0	0	0	0	FFER	FPER	DR	MPB	0	RDAT[7:0]							
9bit	0	Don't Care	0	0	0	FFER	FPER	DR	MPB	RDAT[8:0]								
数据长度	CCR3.CHR[1:0]		b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
7bit	1	1	0	0	0	FER	PER	0	0	ORER	0	0	0	0	0	0	0	0
8bit	1	0	0	0	0	FER	PER	0	0	ORER	0	0	0	0	0	0	0	0
9bit	0	Don't Care	0	0	0	FER	PER	0	0	ORER	0	0	0	0	0	0	0	0

Note: 当数据长度为7bit时，它可以在RDAT[8:7]中读取始终为0。
当数据长度为8bit时，它可以在RDAT[8]中读取始终为0。

Figure 26.40 选择FIFO的多处理器模式下存储在接收FIFO(RDR)中的数据格式

图26.41显示了选择FIFO的多处理器数据接收示例流程。当CCR0.MPIE设置为1时，将跳过读取通信数据，直到接收到多处理器位设置为1的通信数据。当接收到多处理器位设置为1的通信数据时，接收到的数据、MPB和相关错误被传送到接收FIFO(RDR)寄存器。CCR0.MPIE位自动清零，继续正常接收。

如果发生帧错误并且CSR.FER标志设置为1，则SCI继续数据接收。其余操作与选择FIFO的异步模式中的操作相同。



[1] Start reception process
To generate an SCIn_RXI interrupt request with MP detection, please set FCR.RTRG = 1 and FCR.DRES = 0.

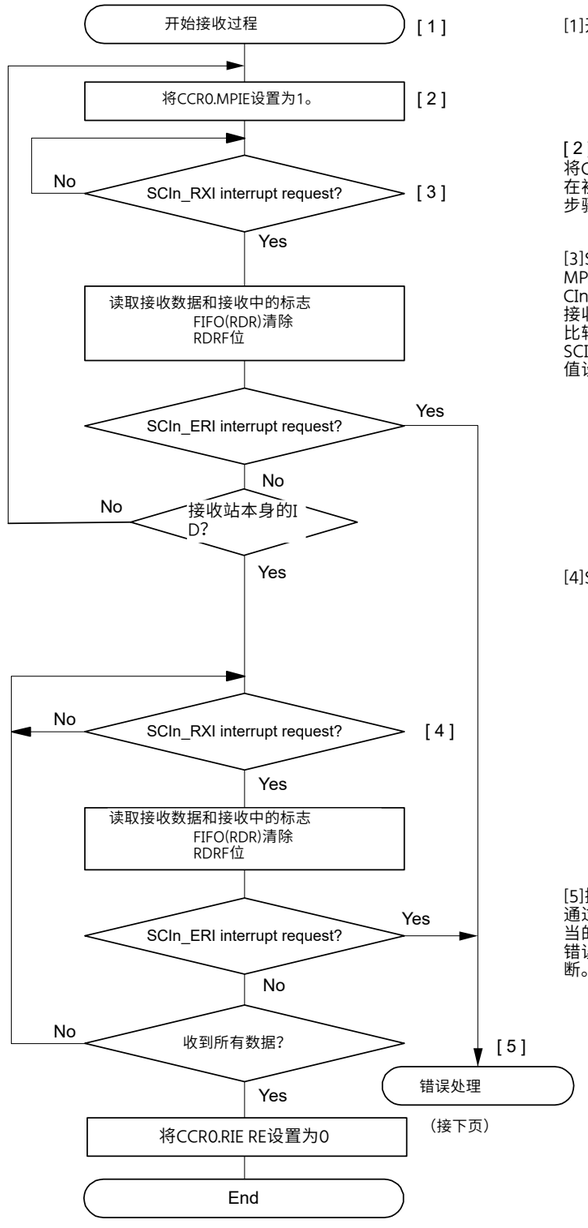
[2] ID reception cycle:
Set CCR0.MPIE to 1. and wait for ID reception. If you set this bits at initialization([1]), you can skip this Step.

[3] SCI status confirmation and reception and comparison of ID:
Skip the communication data until the MPB bit receives data 1. When the MPB bit receives data 1, an SCIn_XRI interrupt request is generated. When an SCIn_RXI interrupt request is received, read the data in the receiving FIFO (RDR register) and compare it to the ID of my station. If it is not my station's ID, set the MPIE bit to 1 again and wait for the SCIn_RXI interrupt request. For my station's ID, set the received FIFO threshold to the necessary value.

[4] Data reception at an SCIn_RXI interrupt:
When the number of received data stored in the received FIFO (RDR register) exceeds the received FIFO threshold, the CSR.RDRF bit becomes 1 and an SCIn_RXI interrupt request is generated. In addition, if the number of received data stored in the received FIFO (RDR register) is 1 or more and less than the received FIFO threshold, the FRSR.DR bit becomes 1 after 15 ETU, and an SCIn_RXI interrupt request is generated. The SCIn_RXI interrupt routine reads the data from the received FIFO (RDR register).

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading ORER and FER flags in CSR. After performing the appropriate error processing be sure to clear the ORER and FER flags. In the case of a framing error, a break can be detected by reading the value of the RXDn pin.

Figure 26.41 Example flow of serial reception in multi-processor mode with FIFO selected



[1]开始接收进程
生成SCIn_RXI中断请求
MP检测，请设置FCR.RTRG=1和
FCR.DRES = 0.

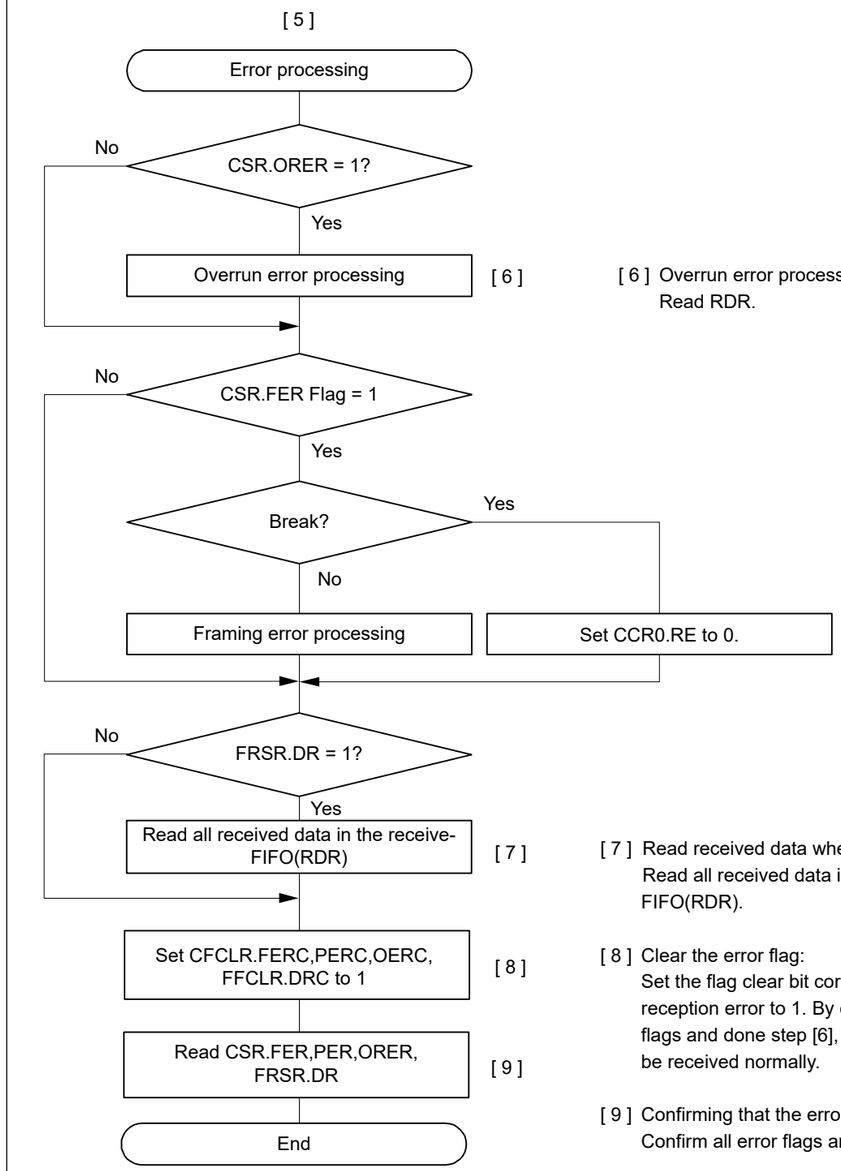
[2] 身份证接收周期：
将CCR0.MPIE设置为1。并等待ID接收。如果在初始化时设置此位（[1]），则可以跳过此步骤。

[3]SCI状态确认及ID接收与比较：跳过通讯数据，直到MPB位接收到数据1。当MPB位接收到数据1时，产生SCIn_XRI中断请求。当收到SCIn_RXI中断请求时，读取接收FIFO（RDR寄存器）中的数据，并与我站的ID进行比较。如果不是我站的ID，重新设置MPIE位为1，等待SCIn_RXI中断请求。对于我站的ID，将接收到的FIFO阈值设置为必要的值。

[4]SCIn_RXI中断处的数据接收：
当接收FIFO（RDR寄存器）中存储的接收数据数量超过接收FIFO阈值时，CSR.RDRF位变为1，并产生SCIn_RXI中断请求。此外，如果接收FIFO（RDR寄存器）中存储的接收数据数量为1或更多且小于接收FIFO阈值，则FRSR.DR位在15个ETU后变为1，并产生SCIn_RXI中断请求。SCIn_RXI中断例程从接收到的FIFO（RDR寄存器）读取数据。

[5]接收错误处理和中断检测：如果发生接收错误，则通过读取CSR中的ORER和FER标志来识别错误。执行适当的错误处理后，请务必清除ORER和FER标志。在帧错误的情况下，可以通过读取RXDn引脚的值来检测中断。

Figure 26.41 选择FIFO的多处理器模式下的串行接收示例流程



[6] Overrun error processing:
Read RDR.

[7] Read received data when FCR.DRES is 1.:
Read all received data in the receive-FIFO(RDR).

[8] Clear the error flag:
Set the flag clear bit corresponding to the reception error to 1. By clearing all the error flags and done step [6], the next frame can be received normally.

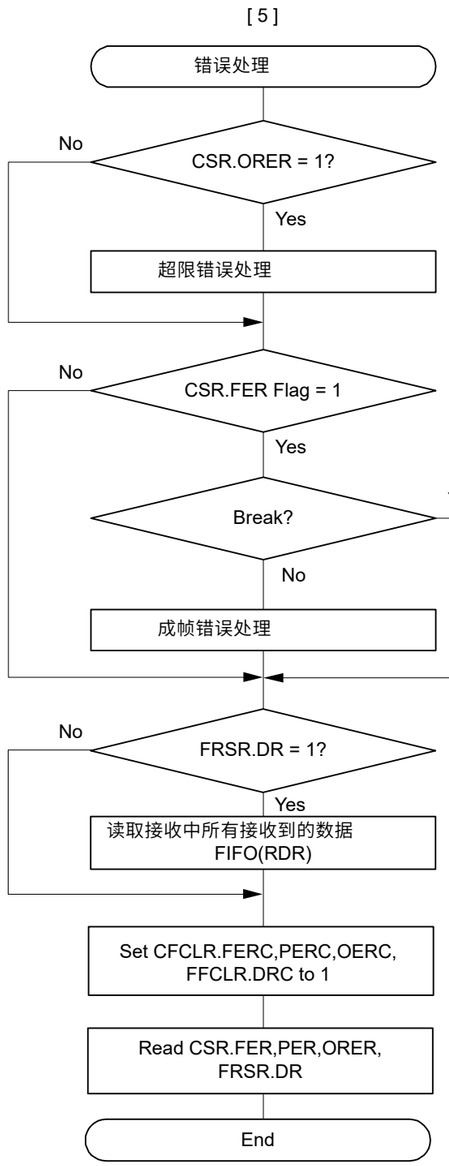
[9] Confirming that the error flag is cleared:
Confirm all error flags are cleared.

Figure 26.42 Example Flowchart of Serial Reception in Multi-Processor Mode (2) (FIFO selected)

26.5 Operation in Manchester mode

In Manchester mode, the transmit or receive serial data is coded in Manchester encoding.

Figure 26.43 shows the conceptual image of Manchester encoding.



[6]溢出错误处理：读取RDR。

[7]FCR.DRES为1时读取接收数据。：读取接收中的所有接收数据
FIFO(RDR).

[8]清除错误标志：
将接收错误对应的标志清除位设置为1。通过清除所有错误标志并完成步骤[6]，可以正常接收下一帧。

[9]确认清除错误标志：确认清除所有错误标志。

Figure 26.42 多处理器模式下串行接收示例流程图（二）（选择FIFO）

26.5 曼彻斯特模式下的操作

在曼彻斯特模式下，发送或接收串行数据以曼彻斯特编码进行编码。

图26.43显示了曼彻斯特编码的概念图。

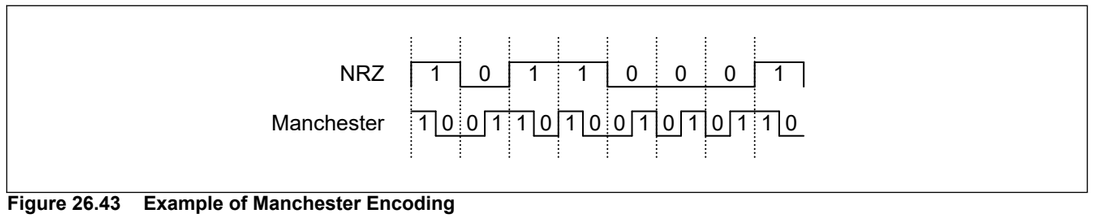


Figure 26.43 Example of Manchester Encoding

In Manchester mode, a preface and a start bit area are added to the transmit data in the register to configure a transmit frame. For transmission, data is encoded in Manchester encoding. When data is received, frames having the same format as transmitted frames are detected and Manchester decoding is performed.

For details on the frame format, see section 26.5.1. Frame Format.

26.5.1 Frame Format

Figure 26.44 shows the frame format in Manchester mode.

In the upper half of the figure, relevant setting registers are shown.

The preface area and the data area are encoded in Manchester encoding.

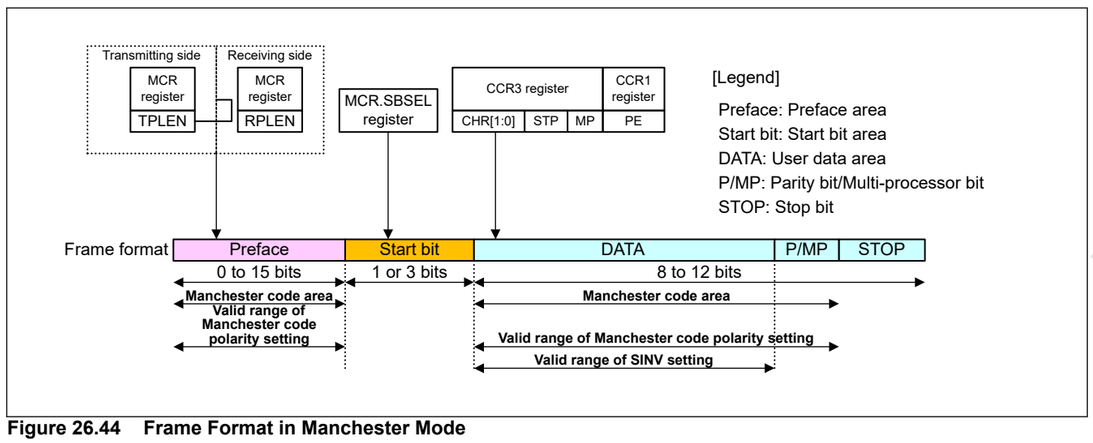


Figure 26.44 Frame Format in Manchester Mode

(1) Preface area

This is a fixed pattern area located at the beginning of each frame.

Different registers are used to set the preface area for transmission and reception. The preface length is determined by setting MCR.TPLEN[3:0] for transmission. It is determined by setting MCR.RPLEN[3:0] for reception.

If it is set to 0, the transmit preface is disabled and is not added.

If it is set to 1d to 15d, a preface whose length is determined by this setting is added.

(For example, if it is set to 1d, a 1-bit preface is added. If it is set to 15d, a 15-bit preface is added.)

The preface pattern is set with MCR.TPPAT[1:0] for transmission and MCR.RPPAT[1:0] for reception, and is selected from four types of patterns.

Figure 26.45 shows how the preface pattern is set. The preface area and the start bit area are added for each communication frame.

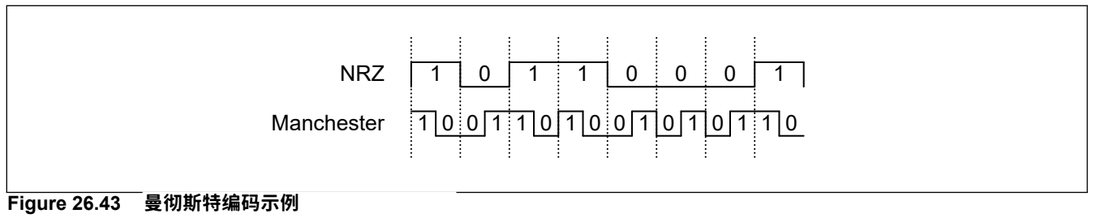


Figure 26.43 曼彻斯特编码示例

在曼彻斯特模式下，前言和起始位区域被添加到寄存器中的发送数据以配置发送帧。对于传输，数据以曼彻斯特编码进行编码。当接收到数据时，检测与传输帧格式相同的帧并执行曼彻斯特解码。

有关帧格式的详细信息，请参见第26.5.1节。帧格式。

26.5.1 帧格式

图26.44显示了曼彻斯特模式下的帧格式。

在图的上半部分，显示了相关的设置寄存器。

前言区和数据区采用曼彻斯特编码。

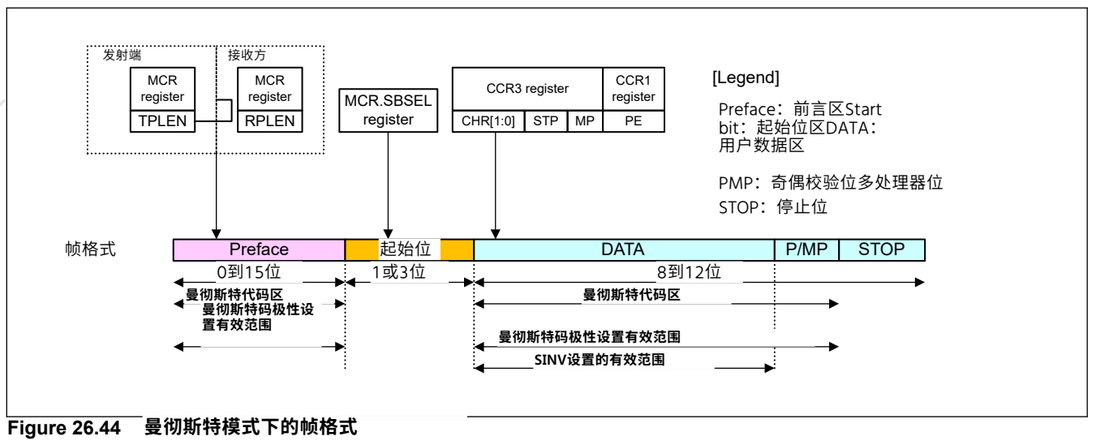


Figure 26.44 曼彻斯特模式下的帧格式

(1) 前言区

这是位于每帧开始处的固定模式区域。

不同的寄存器用于设置发送和接收的前言区域。前言长度通过设置MCR.TPLEN[3:0]来确定传输。通过设置接收的MCR.RPLEN[3:0]来确定。

如果设置为0，则发送前言被禁用且不添加。

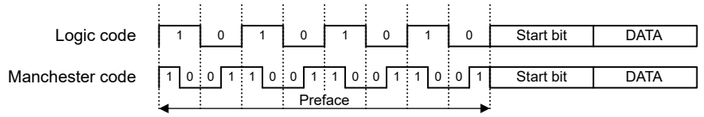
如果设置为1d到15d，则添加一个长度由该设置确定的前言。

（例如，如果设置为1d，则添加1位前言。如果设置为15d，则添加15位前言。）

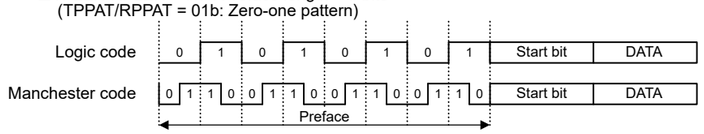
前言模式设置为发送用MCR.TPPAT[1:0]，接收用MCR.RPPAT[1:0]，从四种模式中选择。

图26.45显示了如何设置前言模式。为每个通信帧添加前言区和起始位区。

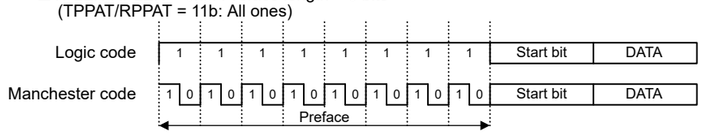
■TPLEN/RPLEN = 0x8: Preface length = 8 bits
(TPPAT/RPPAT = 10b: One-zero pattern)



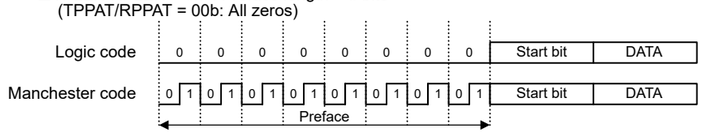
■TPLEN/RPLEN = 0x8: Preface length = 8 bits
(TPPAT/RPPAT = 01b: Zero-one pattern)



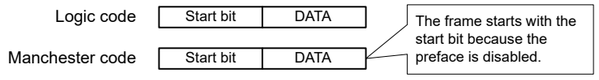
■TPLEN/RPLEN = 0x8: Preface length = 8 bits
(TPPAT/RPPAT = 11b: All ones)



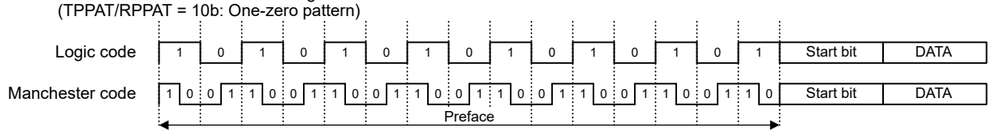
■TPLEN/RPLEN = 0x8: Preface length = 8 bits
(TPPAT/RPPAT = 00b: All zeros)



■TPLEN/RPLEN = 0x0: Preface disabled



■TPLEN/RPLEN = 0xF: Preface length = 15 bits
(TPPAT/RPPAT = 10b: One-zero pattern)



■TPLEN/RPLEN = 0x4: Preface length = 4 bits
(TPPAT/RPPAT = 10b: One-zero pattern)

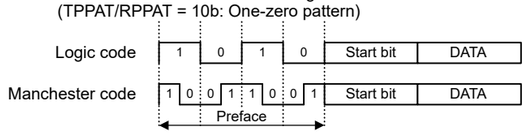


Figure 26.45 Preface Pattern Setting Example

(2) Start bit area

This is an area indicating the start of valid data in a frame. It is added after the preface area.

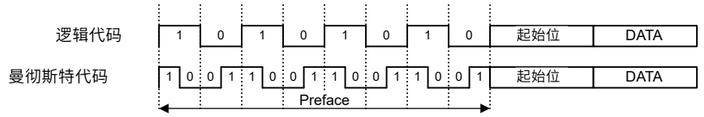
The start bit length is determined by MCR.SBSEL setting. When MCR.SBSEL = “0”, the start bit length is 1 bit.

When MCR.SBSEL = “1”, the start bit length is 3 bits.

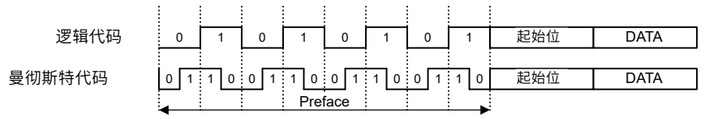
When MCR.SBSEL = “1”, the SYNC type can be selected from command SYNC and data SYNC.

Command SYNC means the three start bits are added as a one-to-zero transition.

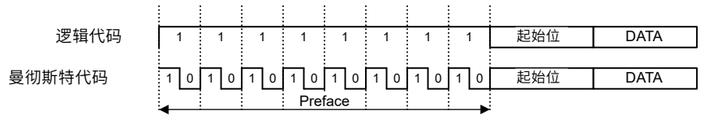
■TPLENRPLEN=0x8：前言长度=8位



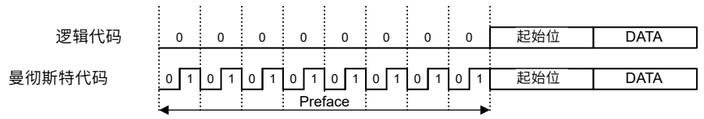
■TPLENRPLEN=0x8：前言长度=8位



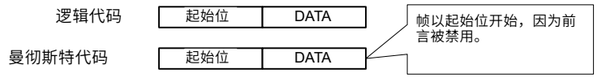
■TPLENRPLEN=0x8：前言长度=8位



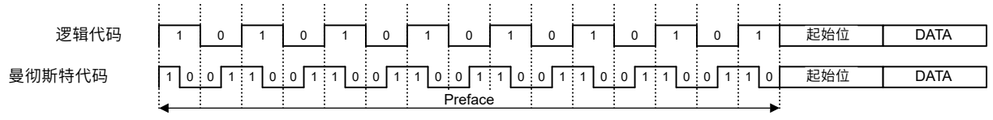
■TPLENRPLEN=0x8：前言长度=8位



■TPLENRPLEN=0x0：前言禁用



（TPPATRPPAT=10b：一零模式）■TPLENRPLEN
=0xF：前言长度=15位



（TPPATRPPAT=10b：一零模式）■TPLENRPLE
N=0x4：前言长度=4位

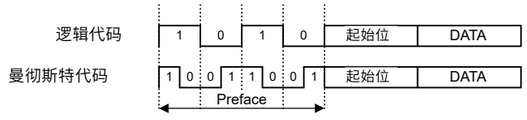


Figure 26.45 前言模式设置示例

(2) 起始位区

这是指示帧中有效数据开始的区域。它添加在前言区域之后。

起始位长度由MCR.SBSEL设置决定。当MCR.SBSEL=“0”时，起始位长度为1位。

当MCR.SBSEL=“1”时，起始位长度为3位。

当MCR.SBSEL=“1”时，SYNC类型可以从命令SYNC和数据SYNC中选择。

命令SYNC意味着三个起始位被添加为一个从1到零的转换。

Data SYNC means the three start bits are added as a zero-to-one transition.

The SYNC type is determined by the MCR.SYNSEL, MCR.SYNVAL and TDR.TSYNC settings.

(When receiving, the received result is applied to MSR.RSYNC.)

When MCR.SBSEL = “0”, the start bit is added as a zero-to-one or one-to-zero transition.

The selection is determined by the MCR.SYNVAL setting.

The MCR.SYNSEL bit specifies the destination to be referred to when setting for transmission.

When the MCR.SYNSEL bit is set to 1, the MCR.SYNVAL setting is referred to. When the MCR.SYNSEL bit is set to 0, the TDR.TSYNC setting is referred to.

Figure 26.46 shows the state of the start bit area according to the settings in the MCR.SYNSEL, MCR.SYNVAL and TDR.TSYNC registers in the case of transmission. Figure 26.47 shows that in the case of reception.

The start bit(s) is not affected by the MCR.TMPOL or MCR.RMPOL setting.

*d.c. = don't care, Preface = preface area, START = start bit area, Data = user data area,
P = parity bit, MP = multi-processor bit, STOP = stop bit

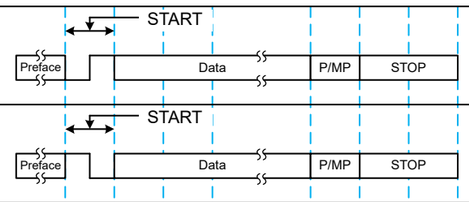
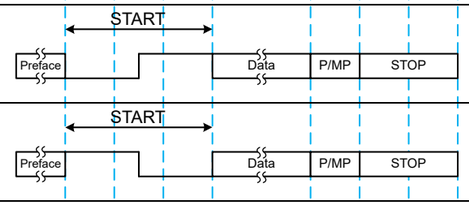
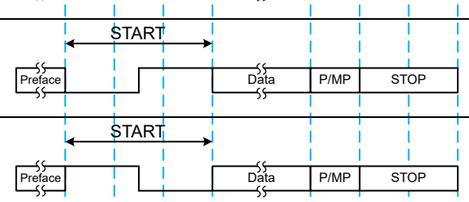
Register setting				Output signal	Output Start bit
MCR			TDR	Output TXDn waveform	
SBSEL	SYNSEL	SYNVAL	TSYNC		
0	d.c.	0	d.c.		1bit 0 to 1 transition
0	d.c.	1	d.c.		1bit 1 to 0 transition
1	0	0	d.c.		3bit 0 to 1 transition (DATA SYNC)
1	0	1	d.c.		3bit 1 to 0 transition (COMMAND SYNC)
1	1	d.c.	0		3bit 0 to 1 transition (DATA SYNC)
1	1	d.c.	1		3bit 1 to 0 transition (COMMAND SYNC)

Figure 26.46 Settings Related to and Format of the Start Bit Area at Transmission

数据同步意味着三个起始位被添加为一个零到一的转换。

SYNC类型由MCR.SYNSEL、MCR.SYNVAL和TDR.TSYNC设置确定。

（接收时，将接收到的结果应用到MSR.RSYNC。）

当MCR.SBSEL=“0”时，添加起始位作为零到一或一到零的转换。

选择由MCR.SYNVAL设置决定。

MCR.SYNSEL位指定设置传输时要参考的目标。

当MCR.SYNSEL位设置为1时，参考MCR.SYNVAL设置。当MCR.SYNSEL位设置为0时，参考TDR.TSYNC设置。

图26.46显示了根据MCR.SYNSEL、MCR.SYNVAL和
TDR.TSYNC寄存器在传输的情况下。图26.47显示了在接收的情况下。

起始位不受MCR.TMPOL或MCR.RMPOL设置的影响。

*直流电=无关，Preface=前言区，START=起始位区，Data=用户数据区，P=奇偶校验位，
MP=多处理器位，STOP=停止位

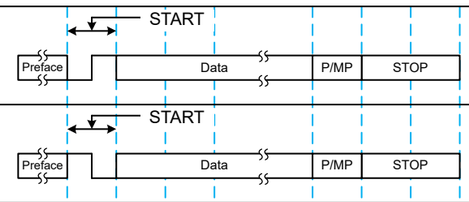
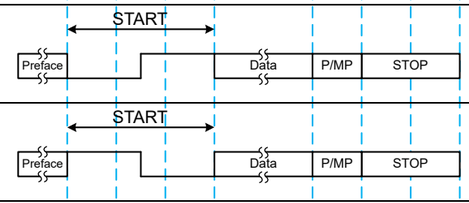
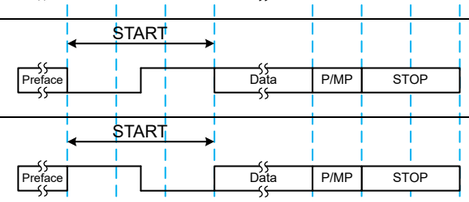
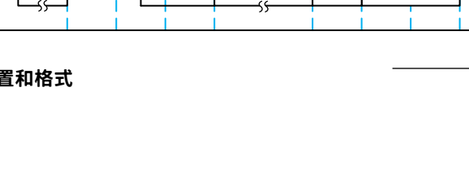
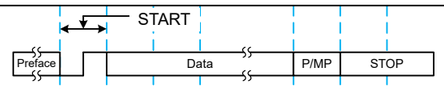
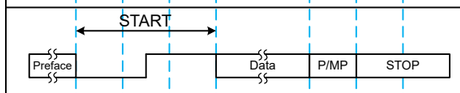
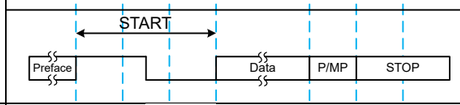
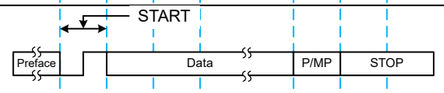
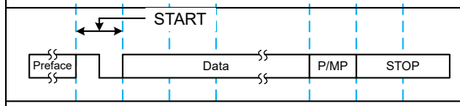
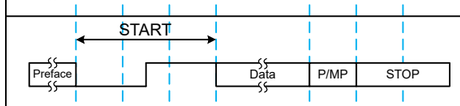
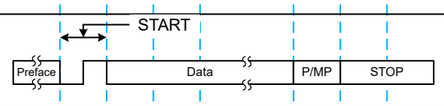
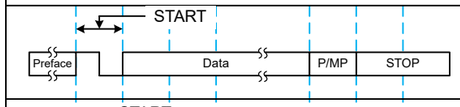
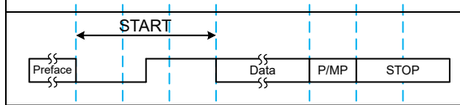
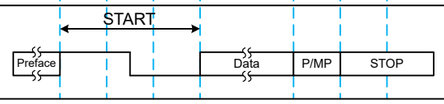
注册设置				输出信号	输出起始位
MCR			TDR	输出TXDn波形	
SBSEL	SYNSEL	SYNVAL	TSYNC		
0	d.c.	0	d.c.		1bit0到1转换
0	d.c.	1	d.c.		1bit1到0转换
1	0	0	d.c.		3bit0到1转换（数据同步）
1	0	1	d.c.		3bit1到0转换(COMMANDSYNC)
1	1	d.c.	0		3bit0到1转换（数据同步）
1	1	d.c.	1		3bit1到0转换(COMMANDSYNC)

Figure 26.46 发送时起始位区域的相关设置和格式

d.c. = don't care, Preface = Preface area, START = Start bit area, Data = Data area
P = Parity bit, MP = Multi-processor bit, STOP = Stop bit

Register setting				Input signal	Start bit detection result*1	Register indication
MCR			TDR	RXDn input waveform		MSR.RSYNC
SBSEL	SYNSEL	SYNVAL	TSYNC			
0	d.c.	0	d.c.		Normal start bit (1 bit: 0-to-1 transition)	0
					Start bit error	0
					Start bit error	0
					Start bit error	0
0	d.c.	1	d.c.		Start bit error	0
					Normal start bit (1 bit: 1-to-0 transition)	0
					Start bit error	0
					Start bit error	0
1	d.c.	d.c.	d.c.		Start bit error	0
					Start bit error	0
					Data SYNC	0
					Command SYNC	1

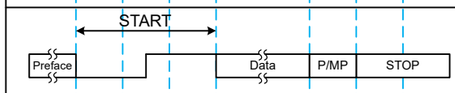
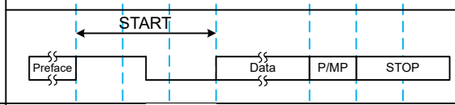
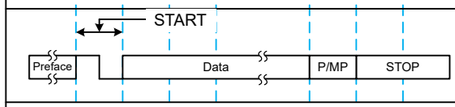
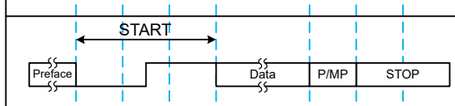
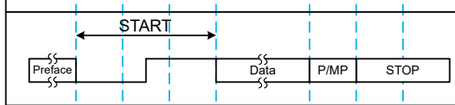
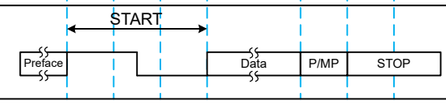
Note 1. Data other than the start bit is assumed to be normal.

Figure 26.47 Settings Related to and Judgment of the Start Bit Area at Reception

(3) DATA

Since the format of the data area is the same as that of the asynchronous mode, see section 26.3.1. Serial Data Transfer Format.

直流电=don'tcare Preface=Prefacearea START=Startbitarea Data=DataareaP=Paritybit
MP=Multi-processorbit STOP=Stopbit

注册设置				输入信号	起始位检测结果*1	登记指示
MCR			TDR	RXDn输入波形		MSR.RSYNC
SBSEL	SYNSEL	SYNVAL	TSYNC			
0	d.c.	0	d.c.		正常起始位（1位：0到1转换）	0
					起始位错误	0
					起始位错误	0
					起始位错误	0
0	d.c.	1	d.c.		起始位错误	0
					正常起始位（1位：1到0转换）	0
					起始位错误	0
					起始位错误	0
1	d.c.	d.c.	d.c.		起始位错误	0
					起始位错误	0
					数据同步	0
					Command SYNC	1

注1.假设起始位以外的数据正常。

Figure 26.47 接收时起始位区域的相关设置和判断

(3) DATA

由于数据区的格式与异步模式相同，见26.3.1节。串行数据传输
Format.

As shown in Figure 26.43, Frame Format in Manchester Mode, the stop bit is not included in the Manchester encoding range.

26.5.2 Clock

As the transfer clock in Manchester mode, the clock generated by the on-chip baud rate generator is used by setting the CCR2.CKS[1:0] bit.

Also it is possible to set the oversampling (transfer rate of one-bit period) by CCR2.ABCS bit.

When the CCR2.ABCS bit is set to 0, oversampling x16 is selected with the one-bit period being 16 cycles of the base clock. When the CCR2.ABCS bit is set to 1, oversampling x8 is selected with the one-bit period being 8 cycles of the base clock.

26.5.3 Initialization of the SCI in Manchester Mode

Before transferring data, write 0 to CCR0.TE and CCR0.RE (or write the initial value to CCR0 register) and initialize the SCI following the example of flowchart shown in Figure 26.48.

Whenever the operating mode or transfer format is changed, the CCR0 register must be initialized before the change is made.

Note that setting the CCR0.RE bit to 0 initializes none of the ORER, FER, PER, RDRF, and RDF flags in the CSR register, the SYER, PFER, MER and SBER flags in the MSR register, and the RDR registers.

Note also that switching the value of CCR0.TE from 0 to 1 when CCR0.TIE is 1 generates a SCIn_TXI interrupt request.

如图26.43，曼彻斯特模式下的帧格式，停止位不包含在曼彻斯特编码范围内。

26.5.2 Clock

作为曼彻斯特模式下的传输时钟，片内波特率发生器产生的时钟用于设置
CCR2.CKS[1:0] bit.

也可以通过CCR2.ABCS位设置过采样（一位周期的传输率）。

当CCR2.ABCS位设置为0时，选择x16过采样，一位周期为基本时钟的16个周期。当CCR2.ABCS位设置为1时，选择x8过采样，一位周期为基本时钟的8个周期。

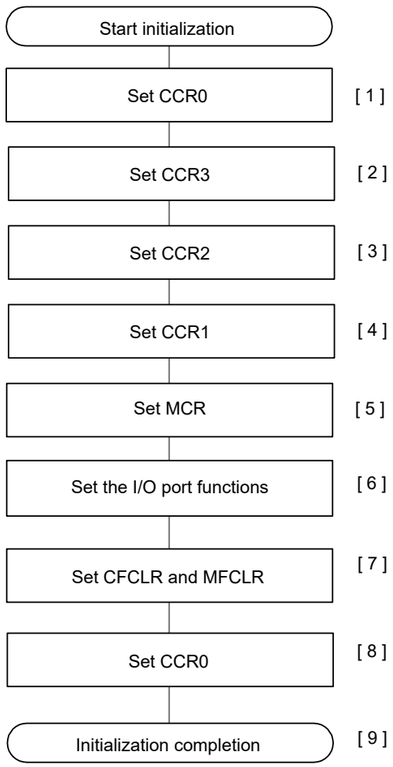
26.5.3 曼彻斯特模式下SCI的初始化

在传输数据之前，将0写入CCR0.TE和CCR0.RE（或将初始值写入CCR0寄存器）并初始化
SCI下面的例子流程图如图26.48所示。

无论何时改变操作模式或传输格式，CCR0寄存器必须在改变之前初始化。

请注意，将CCR0.RE位设置为0不会初始化CSR寄存器中的ORER、FER、PER、RDRF和RDF标志、MSR寄存器中的SYER、PFER、MER和SBER标志以及RDR寄存器。

另请注意，当CCR0.TIE为1时，将CCR0.TE的值从0切换为1会产生SCIn_TXI中断请求。



[1] Set the following bits of CCR0 to 0.
TEIE, TIE, RIE, TE, RE
If you have not changed from the initial settings, you can skip this step.

[2] Set the driver control, Multi-processor communication, the communication mode, transmission/reception format, and Clock enable.
Do not use function bits such as CPOL and CPHA at the initial value.

[3] Set the clock selection, Bit rate setting.
Leave unused function bits at their initial values.(ex. BRME)

[4] Set the noise filter, loopback control, communication terminal status, parity check, and CTS / RTS function.

[5] Set Manchester transmission / reception setting.
Start bit setting, retiming setting, Manchester polarity setting, transmission preface setting, reception preface setting.

[6] Set the I / O port so that the required pin function is valid among the TXDn, RXDn, and SCKn pins.

[7] Set 1 to the following clear bits in the CFCLR and MFCLR registers to clear the target flag.
CFCLR.RDRFC, FERC, PERC, MFC, ORERC, DFERC, DPERC, DCMFC, ERSCMFMFCLR.MERC, SBERC, SYERC, PFERC
This procedure can be omitted for the initial setting after reset.

[9] Set the TE bit or RE bit to 1.
To enable interrupts, set the TE bit and TIE bit, and the RE bit and RIE bit to 1 with one instruction at the same time, and multiprocessor function. The TXDn and RXDn pins can be used by setting the TE and RE bits.

Figure 26.48 SCI Initialization Flow in Manchester Mode

26.5.4 Double-speed operation

When the ABCS bit in CCR2 is set to 1 and eight pulses of the base clock for a 1-bit period is selected, the SCI operates on the bit rate twice that of when ABCS is set to 0.

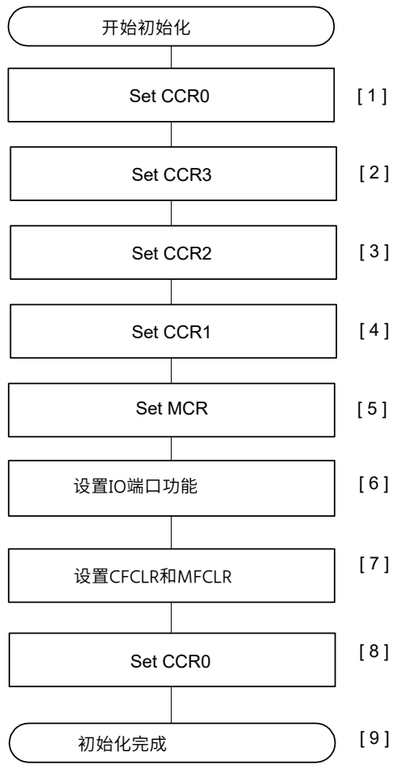
When the BGDM bit in CCR2 is set to 1, the cycle of the base clock is reduced to half and the SCI operates on the bit rate twice that of when ABCS is set to 0.

When the ABCS and the BGDM bits in CCR2 are set to 1, the SCI operates on the bit rate four times that of when the ABCS and the BGDM bits in CCR2 are set to 0.

26.5.5 CTS and RTS functions

The CTS function uses input on the CTSn pin in transmission control. Setting the CTSE bit in CCR1 to 1 enables the CTS function. The CTSn_RTSn pin can be set as a multiplexed pin which allows one pin to be used for either CTS or RTS function, or as dedicated pins with each pin at CTSn pin for CTS function and CTSn_RTSn pin for RTS function. Use the CTSPEN bit in CCR1 for this setting.

When the CTS function is enabled, reception starts only when the CTSn pin is at the low level.



[1]将CCR0的以下位设置为0。
TEIE，领带，RIE，TE，RE
如果您尚未更改初始设置，则可以跳过此步骤。

[2]设置驱动控制、多处理器通信、通信模式、发送接收格式、时钟使能。初始值不要使用CPOL和CPHA等功能位。

[3]设置时钟选择，比特率设置。将未使用的功能位保留为其初始值。（例如BRME）

[4]设置噪声滤波器、环回控制、通信终端状态、奇偶校验、CTSRTS功能。

[5]设置曼彻斯特发射接收设置。起始位设置、重定时设置、曼彻斯特极性设置、发送前言设置、接收前言设置。

[6]设置IO端口，使所需的引脚功能在TXDn、RXDn和SCKn引脚之间有效。

[7]将CFCLR和MFCLR寄存器中的以下清除位设置为1以清除目标标志。CFCLR.RDRFC、FERC、PERC、MFC、ORERC、DFERC、DPERC, DCMFC, ERSCMFMFCLR.MERC, SBERC, SYERC, PFERC
复位后的初始设置可以省略此过程。

[9]将TE位或RE位设置为1。要使能中断，请将TE位和TIE位，以及RE位和RIE位同时设置为1一条指令，以及多处理器功能。通过设置TE和RE位可以使用TXDn和RXDn引脚。

Figure 26.48 曼彻斯特模式下的SCI初始化流程

26.5.4 Double-speed operation

当CCR2中的ABCS位设置为1并选择1位周期的8个基本时钟脉冲时，SCI以ABCS设置为0时的两倍比特率运行。

当CCR2中的BGDM位设置为1时，基本时钟的周期减少到一半，并且SCI以两倍于ABCS设置为0时的比特率运行。

当CCR2中的ABCS和BGDM位设置为1时，SCI以四倍的比特率运行。
CCR2中的ABCS和BGDM位设置为0。

26.5.5 CTS和RTS功能

CTS功能在传输控制中使用CTSn引脚上的输入。将CCR1中的CTSE位设置为1启用CTS功能。CTSn_RTSn引脚可设置为复用引脚，允许一个引脚用于CTS或RTS功能，或作为专用引脚，CTSn引脚用于CTS功能，CTSn_RTSn引脚用于RTS功能。使用CCR1中的CTSPEN位进行此设置。

当CTS功能使能时，只有在CTSn引脚为低电平时才开始接收。

Applying a high level to the CTSn pin after transmission starts does not affect transmission of the current frame, which continues.

The RTS function uses output on the CTSn_RTSn pin to request transmission. When the SCI is ready to receive, it outputs a low level to the CTSn_RTSn pin, Conditions for output of the low level and high level are as follows:

[Conditions for low-level output]

When all conditions listed below are satisfied:

- The value of the RE bit in CCR0 is 1.
- When The SCI is ready to receive next.
  - When there is no received data yet to be read and not receiving
  - All of the following flags are set to 0: CSR.ORER, FER, and PER, MSR.MER, SYER (when SYEREN = 1), PFER (when PFEREN = 1) and SBER flags (when SBEREN = 1).

[Conditions for high-level output]

- When the conditions for low output are not satisfied

26.5.6 Serial data transmission in Manchester mode

The SCI encodes data in Manchester encoding and sends the resultant data in Manchester mode.

When the polarity setting (MCR.TMPOL) set to 0, logic 0 is coded as a zero-to-one transition in Manchester code and logic 1 is coded as a one-to-zero transition in Manchester code.

When the polarity setting (MCR.TMPOL) set to 1, logic 0 is coded as a one-to-zero transition in Manchester code and logic 1 is coded as a zero-to-one transition in Manchester code.

For this reason, a level transition occurs with the Manchester encoded data in the middle of individual logic data. (See Figure 26.43).

The transmitter constructs transmit frames in a specific format by adding a preface area to data and setting the start bit(s) according to the polarity setting and sends resultant serial data.

For details on the frame format, see section 26.5.1. Frame Format.

Figure 26.49 shows the flowchart in transmission. At transmission starts, set the CCR0.TIE and CCR0.TE bits to 1 simultaneously with one instruction. Then, a SCIn_TXI interrupt request is generated. Figure 26.50, Figure 26.51, and Figure 26.52 show examples of the operation for serial transmission in Manchester mode.

传输开始后将高电平施加到CTSn引脚不会影响当前帧的传输，继续传输。

RTS功能使用CTSn_RTSn引脚上的输出来请求传输。当SCI准备好接收时，向CTSn_RTSn管脚输出一个低电平，输出低电平和高电平的条件如下：

[Conditions for low-level output]

当满足下列所有条件时：

●CCR0中RE位的值为1。

●当SCI准备好接收下一个时。

当没有接收到的数据尚未读取且未接收时

以下所有标志都设置为0：CSR.ORER、FER和PER、MSR.MER、SYER（当SYEREN=1时）、PFER（当PFEREN=1时）和SBER标志（当SBEREN=1时）。

[Conditions for high-level output]

●不满足低输出条件时

26.5.6 曼彻斯特模式下的串行数据传输

SCI以曼彻斯特编码对数据进行编码，并以曼彻斯特模式发送结果数据。

当极性设置(MCR.TMPOL)设置为0时，逻辑0被编码为曼彻斯特代码中的零到一转换，逻辑1被编码为曼彻斯特代码中的一到零转换。

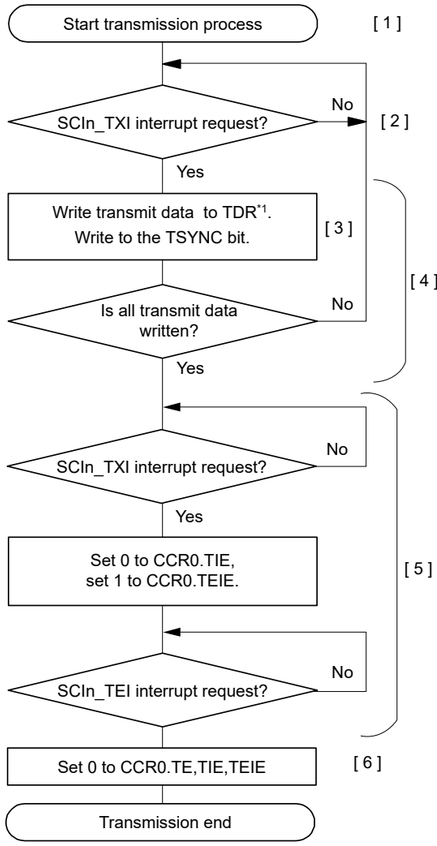
当极性设置(MCR.TMPOL)设置为1时，逻辑0被编码为曼彻斯特代码中的一对零转换，逻辑1被编码为曼彻斯特代码中的零到一转换。

出于这个原因，在各个逻辑数据中间的曼彻斯特编码数据会发生电平转换。（看Figure 26.43）。

发送器通过向数据添加前言区域并根据极性设置设置起始位来构建特定格式的发送帧，并发送结果串行数据。

有关帧格式的详细信息，请参见第26.5.1节。帧格式。

图26.49显示了传输中的流程图。在发送开始时，用一条指令同时将CCR0.TIE和CCR0.TE位设置为1。然后，产生一个SCIn_TXI中断请求。图26.50、图26.51和图26.52显示了曼彻斯特模式下串行传输的操作示例。



[1] Start transmission process

[2] SCIn_TXI interrupt:
A transmit data empty interrupt (SCIn_TXI) request is generated when CCR0.TIE = 1 and TE = 0->1, and when transmit data is transferred from TDR to TSR.

[3] TDR setting:
Write the transmit data to TDR.
When TSYNC is used, also set TDR.TSYNC.

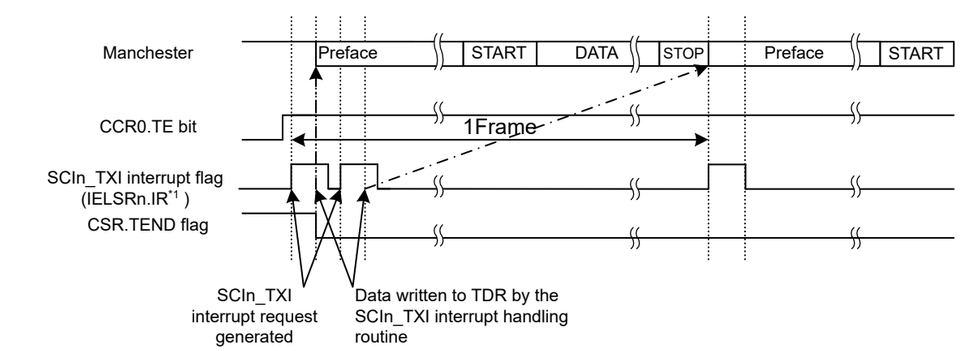
[4] Serial transmission continuation procedure:
To continue serial transmission, write the transmit data to TDR*1 once by using an SCIn_TXI interrupt.
The transmit data can also be written to TDR*1 by activating the DMAC or DTC in the SCIn_TXI interrupt request.

[5] When SCIn_TEI interrupt requests are used, set the CCR0.TIE bit to 0 and the CCR0.TEIE bit to 1 after the last of the data to be transmitted is written to TDR and it' s transmission is started.

[6] Set 0 to CCR0.TE, TIE and TEIE.

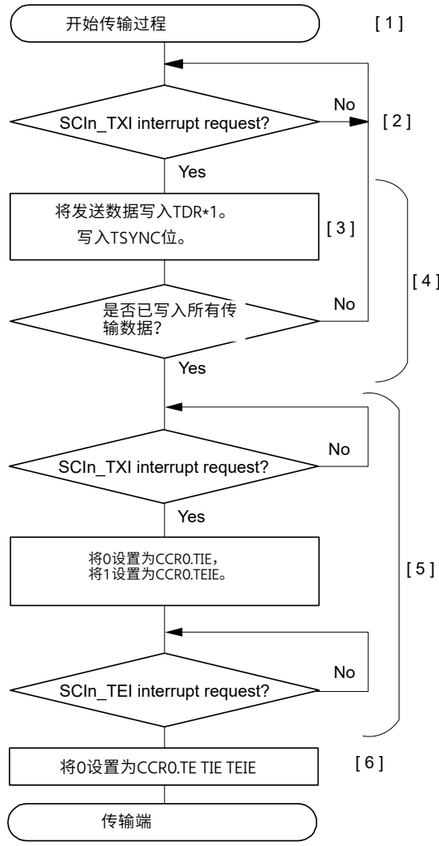
Note 1. If TDR[15:8] requires data write and byte access is required, write the transmit data in the order of TDR [15:8] and TDR [7:0].

Figure 26.49 Example of Serial Transmission Flowchart in Manchester Mode



Note 1. For corresponding interrupt numbers, see section 12, Interrupt Controller Unit (ICU)

Figure 26.50 Example of Start-of-Transmission Operation for Serial Transmission in Manchester mode (with Preface but Without the CTS Function)



[1] 开始传输过程

[2] SCIn_TXI interrupt:
当CCR0.TIE=1且TE=0->1以及发送数据从TDR传输到TSR时，会产生发送数据空中断(SCIn_TXI)请求。

[3] TDR setting:
将发送数据写入TDR。
使用TSYNC时，还要设置TDR.TSYNC。

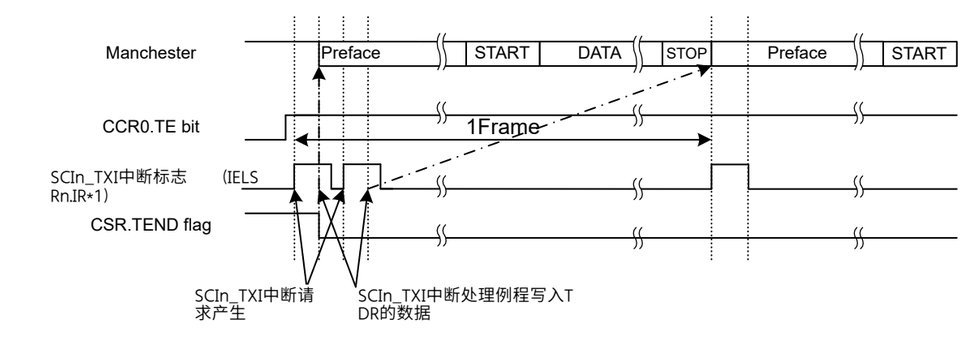
[4]串行传输继续程序：
要继续串行传输，请将传输数据写入TDR*1使用SCIn_TXI中断一次。
发送数据也可以通过激活TDR*1写入SCIn_TXI中断请求中的DMAC或DTC。

[5]当使用SCIn_TEI中断请求时，将要发送的最后一个数据写入TDR并开始发送后，将CCR0.TIE位设置为0，并将CCR0.TEIE位设置为1。

[6] 将0设置为CCR0.TE、TIE和TEIE。

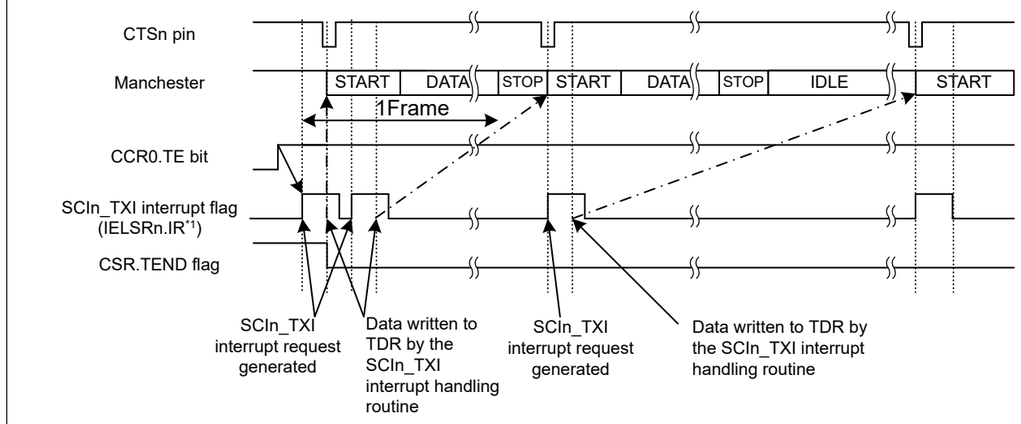
注1.如果TDR[15:8]需要数据写入且需要字节访问，则按照TDR[15:8]和TDR[7:0]的顺序写入发送数据。

Figure 26.49 曼彻斯特模式下的串行传输流程图示例



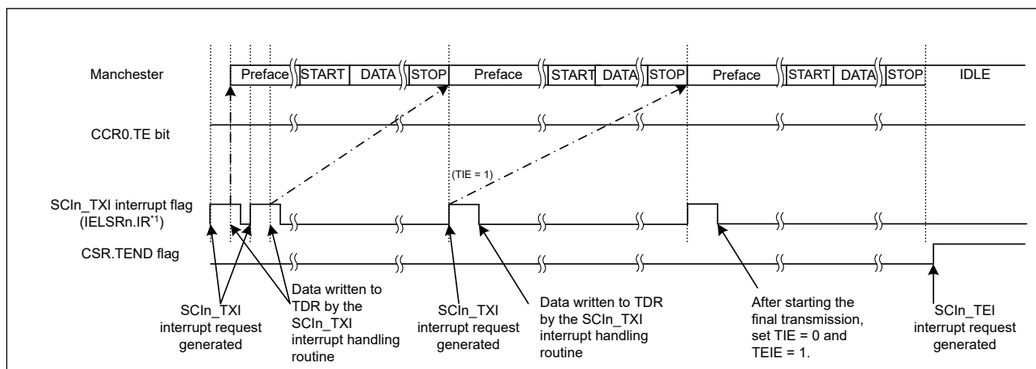
注1.有关相应的中断号，请参阅第12节，中断控制器单元(ICU)

Figure 26.50 曼彻斯特模式下串行传输的传输开始操作示例（使用前言但没有CTS功能）



Note 1. For corresponding interrupt numbers, see section 12, Interrupt Controller Unit (ICU)

Figure 26.51 Example of Start-of-Transmission Operation for Serial Transmission in Manchester Mode (Without Preface but with the CTS Function)



Note 1. For corresponding interrupt numbers, see section 12, Interrupt Controller Unit (ICU)

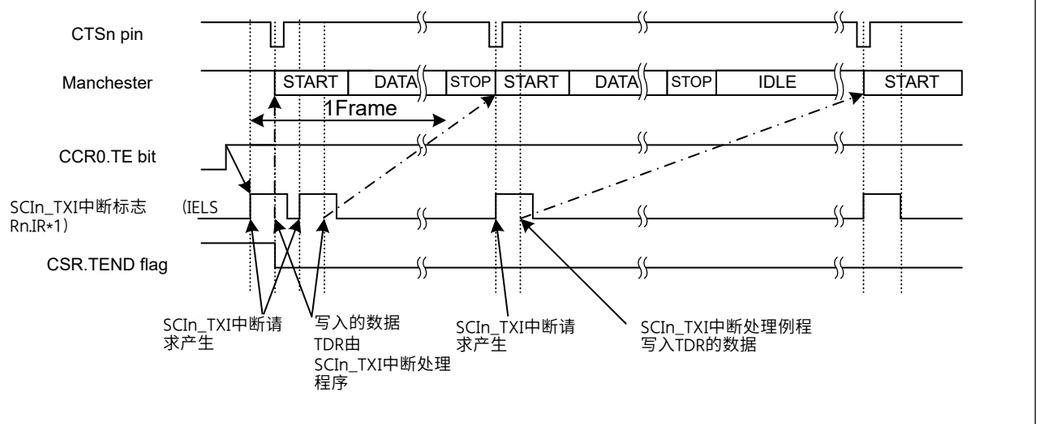
Figure 26.52 Example of End-of-Transmission Operation for Serial Transmission in Manchester Mode (with Preface but Without the CTS Function)

26.5.7 Serial Data Reception in Manchester Mode

In Manchester mode, the SCI operates on a base clock with a frequency of 16 times*1 the bit rate. Reception starts by sampling the falling edges of received data at the base clock. As shown in Figure 26.53, reception starts at a falling edge of the received data and it continues if the received data keeps low for the duration of 1/4 bit. If the received data goes high within the duration of 1/4 bit, the SCI judges it as an error and waits for a falling edge again.

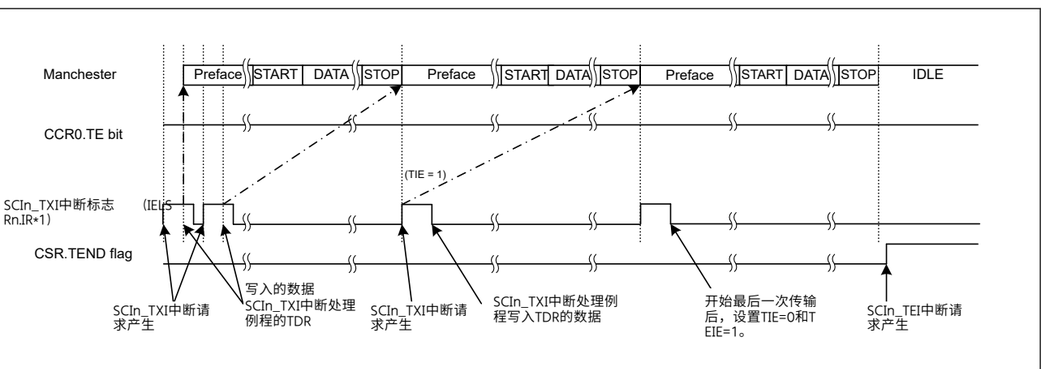
If a high level is expected in the first half of a bit in the received data, the SCI judges a low level that continues for one base clock cycle as an error and ignores the change to the low level.

Note 1. This is the case when CCR2.ABCS = 0. When CCR2.ABCS = 1, the SCI operates on a base clock with a frequency of 8 times the bit rate.



注1.有关相应的中断号，请参阅第12节，中断控制器单元(ICU)

Figure 26.51 曼彻斯特模式下串行传输的传输开始操作示例（无序但具有CTS功能）



注1.有关相应的中断号，请参阅第12节，中断控制器单元(ICU)

Figure 26.52 曼彻斯特模式下串行传输的传输结束操作示例（使用前言但没有CTS功能）

26.5.7 曼彻斯特模式下的串行数据接收

在曼彻斯特模式下，SCI在频率为16倍*1比特率的基本时钟上运行。接收开始于在基本时钟处对接收到的数据的下降沿进行采样。如图26.53所示，接收从接收数据的下降沿开始，如果接收数据保持低电平持续14位，接收将继续。如果接收到的数据在14bit的时间内变高，则SCI判断为错误，再次等待下降沿。

如果在接收数据的前半个比特中预期为高电平，则SCI将持续一个基本时钟周期的低电平判断为错误，并忽略向低电平的变化。

注1.当CCR2.ABCS=0时就是这种情况。当CCR2.ABCS=1时，SCI在频率为比特率8倍的基本时钟上运行。

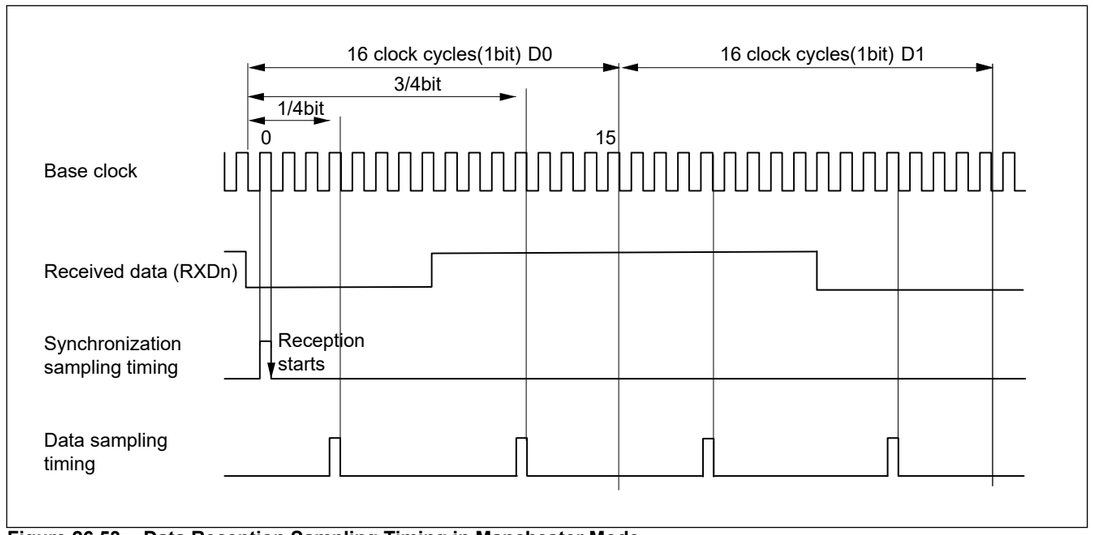


Figure 26.53 Data Reception Sampling Timing in Manchester Mode

In Manchester mode, data reception starts with detection of a preface and start bit area.

The SCI checks the input from the RXDn pin to see whether a preface is added based on the value of MCR.RPLEN.

If the preface is disabled (MCR.RPLEN = 0), it moves on to the detection of a start bit area without detecting a preface.

When a preface is enabled, it identifies a preface pattern setting according to the set value in MCR.RPPAT, and compares it with the RXDn input for a pattern match to detect a preface pattern.

Upon detection of a preface pattern match, it judges it as a normal preface and moves on to the detection of a start bit area.

If detecting a preface pattern mismatch or a Manchester code error in the preface area, it judges it as a preface error and asserts a preface error (PFER).

For start bit detection, the SCI selects an expected value based on the register settings (MCR.SBSEL and SYNVAL), compares it with the RXDn input for a pattern match to detect a start bit area. Upon detection of a start bit pattern match, it judges it as a normal start bit area and moves on to the data processing.

Only when a preface and a start bit area are detected normally, it moves on to the next phase of data reception.

Upon detection of a start bit pattern mismatch, it asserts a start bit error flag (SBER).

In data processing, the SCI shifts the data by the expected received data length based on the register settings (CCR3.CHR[1:0]) through the RSR register. If two sampling points in a bit of the received data are identical, the SCI judges this as a Manchester code error.

For details, see section 26.5.11. Errors in Manchester Mode (4).

When the parity function is disabled (CCR1.PE = 0), the SCI moves on to the next phase of stop bit detection. When the parity function is enabled (CCR1.PE = 1), the SCI performs parity checking. If detecting a parity error, it asserts a parity error flag (PER), and then moves on to stop bit detection.

In stop bit detection, the SCI checks the following in the stop bit area of the received frame:

It has two sampling points in a bit. If both points are at the high level, the bit is recognized as a normal stop bit and the data is stored in the RDR register. At least one low-level point is judged as an abnormal stop bit, causing a framing error flag (FER) to be set. Even when an error is detected, the received data is stored in the RDR register as abnormal data.

Figure 26.54 shows an example of the operation for serial data reception in Manchester mode.

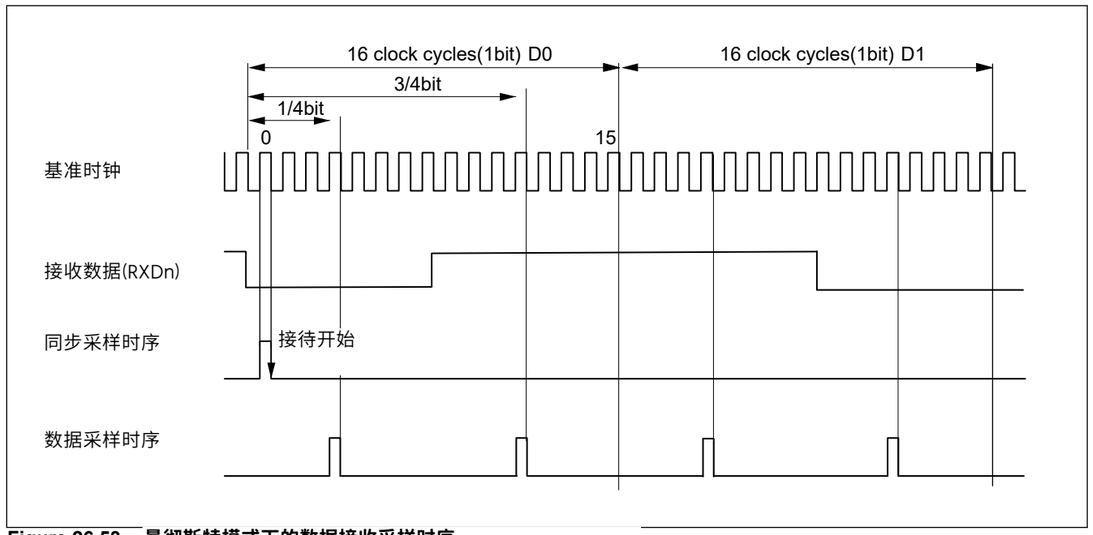


Figure 26.53 曼彻斯特模式下的数据接收采样时序

在曼彻斯特模式下，数据接收从检测前言和起始位区域开始。

SCI检查来自RXDn引脚的输入，以查看是否根据MCR.RPLEN的值添加了前言。

如果前言被禁用（MCR.RPLEN=0），它会继续检测起始位区域而不检测前言。

启用前言时，它根据MCR.RPPAT中的设置值识别前言模式设置，并将其与模式匹配的RXDn输入进行比较，以检测前言模式。

在检测到前言模式匹配时，将其判断为正常前言并继续检测起始位区域。

如果在前言区域检测到前言模式不匹配或曼彻斯特码错误，则将其判断为前言错误并断言前言错误（PFER）。

对于起始位检测，SCI根据寄存器设置（MCR.SBSEL和SYNVAL）选择预期值，将其与模式匹配的RXDn输入进行比较，以检测起始位区域。在检测到起始位模式匹配时，将其判断为正常起始位区域并继续进行数据处理。

只有在正常检测到前言和起始位区域时，才进入下一个数据接收阶段。

在检测到起始位模式不匹配时，它会断言起始位错误标志(SBER)。

在数据处理中，SCI根据寄存器设置(CCR3.CHR[1:0])通过RSR寄存器将数据移位预期的接收数据长度。如果接收到的数据位中的两个采样点相同，则SCI判断为曼彻斯特码错误。

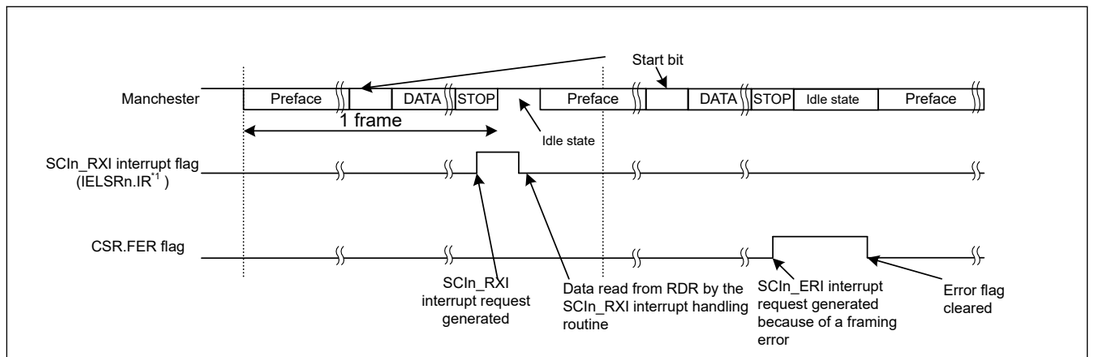
详见26.5.11节。曼彻斯特模式中的错误(4)。

当奇偶校验功能被禁用（CCR1.PE=0）时，SCI进入下一个停止位检测阶段。当启用奇偶校验功能（CCR1.PE=1）时，SCI执行奇偶校验。如果检测到奇偶校验错误，它会置位奇偶校验错误标志(PER)，然后继续进行停止位检测。

在停止位检测中，SCI在接收帧的停止位区域中检查以下内容：

它有两个采样点。如果两个点都处于高电平，则该位被识别为正常停止位，数据存储在RDR寄存器中。至少有一个低电平点被判断为异常停止位，导致设置帧错误标志（FER）。即使检测到错误，接收到的数据也会作为异常数据存储在RDR寄存器中。

图26.54显示了曼彻斯特模式下串行数据接收操作的示例。



Note 1. For corresponding interrupt numbers, see section 12, Interrupt Controller Unit (ICU).

Figure 26.54 Example of Operation for Serial Data Reception in Manchester mode (with a Preface)

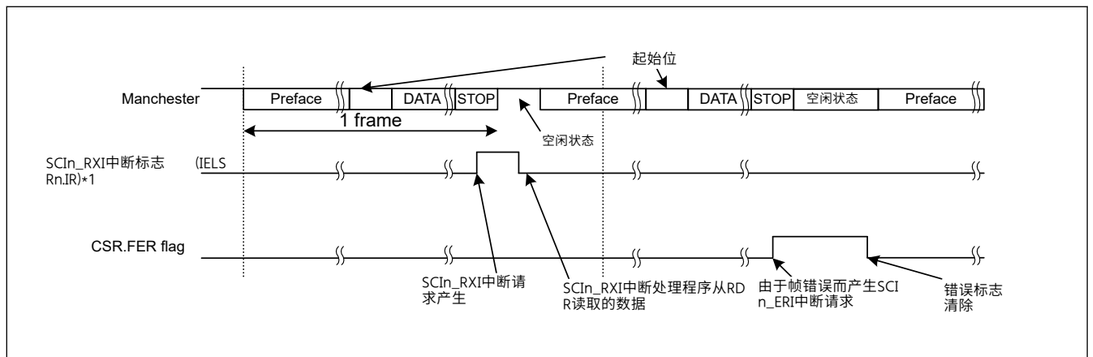
For the state of each status flag in the CCR0 register and RXDn input processing when a receive error is detected, see section 26.5.11. Errors in Manchester Mode.

If a receive error is detected, an SCIn_ERI interrupt request is generated but an SCIn_RXI interrupt request is not generated.

Data reception cannot be resumed while the receive error flag is 1. Accordingly, set the ORER, FER, PER, MER, SYER*1, PFER*1, and SBER*1 flags to 0 before resuming reception. Also, be sure to read the RDR register during overrun error processing. When a reception is forcibly terminated by setting the CCR0.RE bit to 0 during operation, read the RDR register because received data which has not yet been read may be left in the RDR register.

Figure 26.55 and Figure 26.56 show examples of serial data reception flowchart in Manchester mode.

Note 1. Effective when the corresponding bit is enabled.



注1.有关相应的中断号，请参见第12节，中断控制器单元(ICU)。

Figure 26.54 曼彻斯特模式下串行数据接收操作示例（附前言）

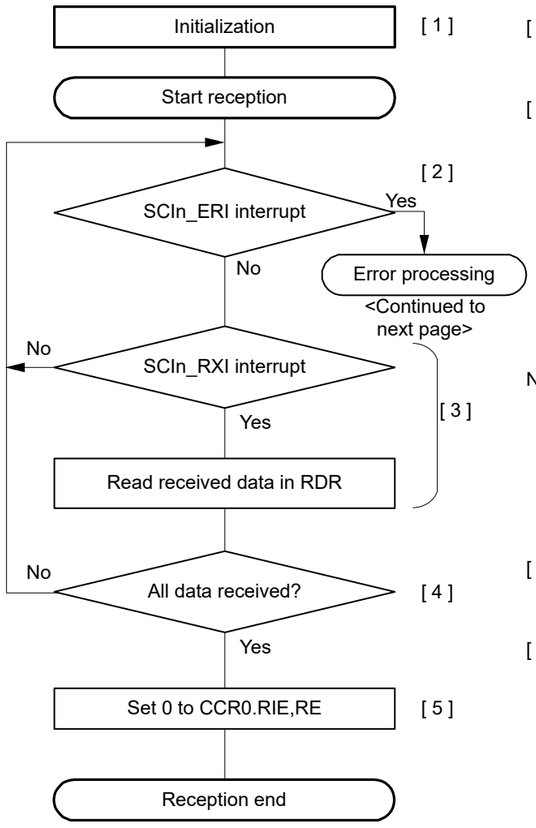
关于检测到接收错误时CCR0寄存器中的每个状态标志的状态和RXDn输入处理，请参阅第26.5.11节。曼彻斯特模式中的错误。

如果检测到接收错误，则会产生SCIn_ERI中断请求，但不会产生SCIn_RXI中断请求。

接收错误标志为1时无法恢复数据接收。因此，请设置ORER、FER、PER、MER、SYER*1，PFER*1和SBER*1在恢复接收之前标志为0。此外，请务必在溢出错误处理期间读取RDR寄存器。如果在操作期间通过将CCR0.RE位设置为0来强制终止接收，请读取RDR寄存器，因为尚未读取的接收数据可能会留在RDR寄存器中。

图26.55和图26.56显示了曼彻斯特模式下的串行数据接收流程图示例。

注1.当相应位使能时有效。



[1] SCI initialization.
(Set CCR0.RE = 1 and RIE = 1)

[2] Receive error processing:
When a receive error occurs, SCI generates an SCIn_ERI interrupt . An error is identified by reading the ORER, PER, FER in CSR and MER, SBER, SYER, PFER in MSR. After performing the appropriate error processing, always set the ORER, PER, FER, MER, SBER, SYER, PFER flags to 0. Reception cannot be resumed if any of these flags is set to 1.

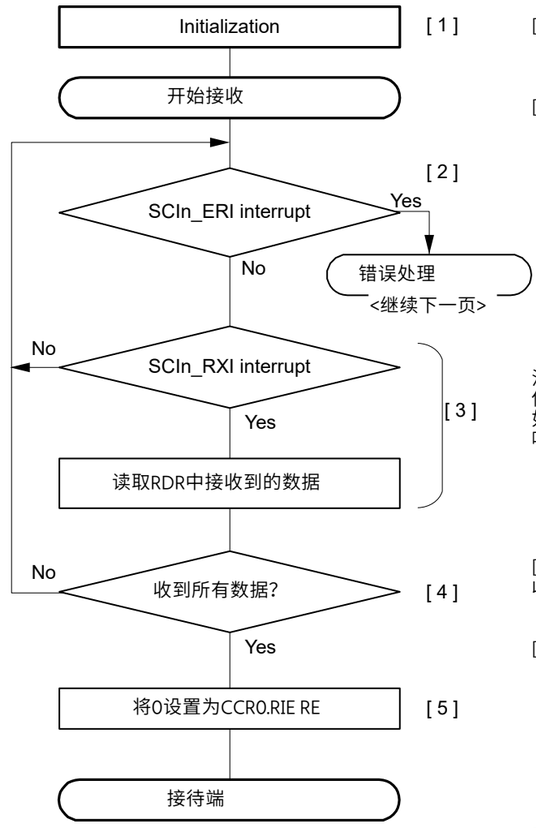
Note: Each of the PFER, SYER, SBER bits in MSR has an enable bit (PFEREN, SYEREN, and SBEREN in MECR). If the corresponding enable bit is set to 0 (disable), the flag value does not affect the communication. Perform error processing as required.

[3] Read the received data in RDR once in the SCIn_RXI interrupt handling routine.

[4] Serial reception continuation procedure:
To continue serial reception, before the stop bit of a frame is received, read data from RDR in the SCIn_RXI interrupt handling routine. The RDR data can also be read by activating the DMAC or DTC.

[5] Write 0 to CCR0.RIE and RE.

Figure 26.55 Example of Serial Data Reception Flowchart in Manchester Mode (Normal Reception)



[1]SCI初始化。
（设置CCR0.RE=1和RIE=1）

[2]接收错误处理：
当接收错误发生时，SCI生成一个
SCIn_ERI中断。通过读取CSR中的ORER、PER、FER和MSR中的MER、SBER、SYER、PFER来识别错误。执行适当的错误处理后，请始终将ORER、PER、FER、MER、SBER、SYER、PFER标志设置为0。如果这些标志中的任何一个设置为1，则无法恢复接收。

注意：MSR中的每个PFER、SYER、SBER位都有一个使能位（MECR中的PFEREN、SYEREN和SBEREN）。如果相应的使能位设置为0（禁用），则标志值不影响通信。根据需要进行错误处理。

[3]在SCIn_RXI中断处理程序中读取一次RDR中接收到的数据。

[4]串行接收继续过程：
要继续串行接收，在接收到帧的停止位之前，在SCIn_RXI中断处理程序中从RDR读取数据。RDR数据也可以通过激活读取

DMAC or DTC.

[5]将0写入CCR0.RIE和RE。

Figure 26.55 曼彻斯特模式下的串行数据接收流程图示例（正常接收）

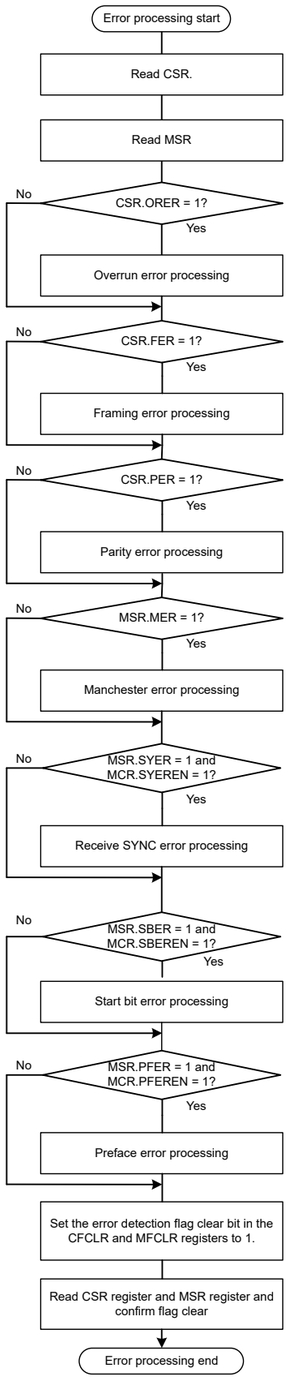


Figure 26.56 Example of Serial Reception Flowchart in Manchester Mode (Error Processing)

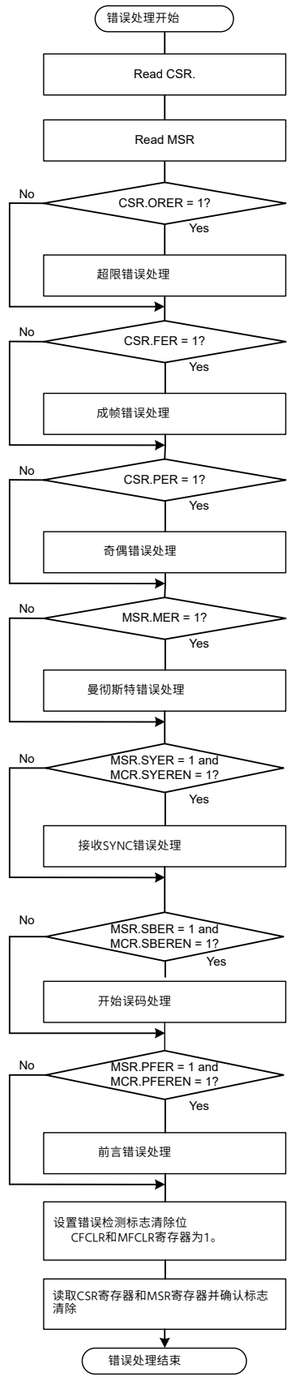


Figure 26.56 曼彻斯特模式下的串行接收流程图示例（错误处理）

26.5.8 Operation When Multi-Processor Bit Is Used

See section 26.4. Multi-Processor Communication Function (1) for the operation in Manchester mode when using multi-processor mode because the operation is the same.

A preface and a start bit area are added to the frame format in Manchester mode. See Figure 26.56 for error processing in Manchester mode for the reception flowchart (Figure 26.39). Refer to Table 26.34 for the operation status when detecting various errors.

26.5.9 Receive Retiming

This function corrects the timing for each central edge of the bit, taking advantage of the fact that each bit has an edge in the center in Manchester code.

The receive retiming function can be turned on or off by setting the ERTEN bit in the MCR register.

When the receive retiming function is turned off (MCR.ERTEN = 0), retiming is not performed, causing misalignment between the internal clock and the RXDn input to be accumulated and the receive margin to be reduced.

When the receive retiming function is turned on (MCR.ERTEN = 1), retiming is performed for the preface area, the start bit area*1, and the data area (excluding the stop bit).

Note 1. Retiming is not performed for the start bit area if the preface length is 0 and the start bit length is 3.

As an example, the receive retiming when oversampling x16 is selected is shown below.

When detecting an RXDn input edge two to four cycles before the expected receive cycle, the receive processing is shortened by one sampling CLK cycle.

When detecting a RXDn input edge two to three cycles after the expected receive cycle, the receive processing is extended by one sampling CLK cycle.

(Even if the clock is misaligned with the data by more than two cycles, one cycle is corrected for each bit.)

Figure 26.57 shows the conceptual image of receive retiming range.

When detecting an edge in the tolerance area in the figure, data is received as is without making correction.

When detecting an edge in the SyncJump area in the figure, data is corrected for reception.

When detecting an edge in the SyncError area in the figure, data is received as abnormal data with no correction made.

For a Manchester code error (data matches at the 1/4-phase and 3/4-phase sampling points), the SCI reports a code error.

26.5.8 使用多处理器位时的操作

请参阅第26.4节。多处理器通信功能(1)曼彻斯特模式下的操作在使用多处理器模式时因为操作是一样的。

曼彻斯特模式的帧格式中添加了前言和起始位区域。接收流程图（图26.39）在曼彻斯特模式下的错误处理见图26.56。检测各种错误时的动作状态见表26.34。

26.5.9 接收重定时

该函数利用曼彻斯特码中每个位在中心的边缘这一事实，校正位的每个中心边沿的时序。

通过设置MCR寄存器中的ERTEN位，可以打开或关闭接收重定时功能。

当接收重定时功能关闭（MCR.ERTEN=0）时，不执行重定时，导致内部时钟和RXDn输入之间的错位被累积，接收裕量减少。

当接收重定时功能打开时（MCR.ERTEN=1），对前言区、起始位区*1和数据区（不包括停止位）执行重定时。

注1.如果序言长度为0且起始位长度为3，则不对起始位区域执行重定时。

例如，选择过采样x16时的接收重定时如下所示。

当在预期接收周期前2到4个周期检测到RXDn输入边沿时，接收处理将缩短1个采样CLK周期。

当在预期接收周期后两到三个周期检测到RXDn输入边沿时，接收处理将延长一个采样CLK周期。

（即使时钟与数据的偏差超过两个周期，也会为每一位校正一个周期。）

图26.57显示了接收重定时范围的概念图。

在图中的公差范围内检测边缘时，直接接收数据而不进行校正。

当在图中的SyncJump区域检测到边缘时，数据被校正以进行接收。

当在图中的SyncError区域检测到边缘时，数据作为异常数据接收，没有进行校正。

对于曼彻斯特编码错误（数据在1个4相和3个4相采样点匹配），SCI报告编码错误。

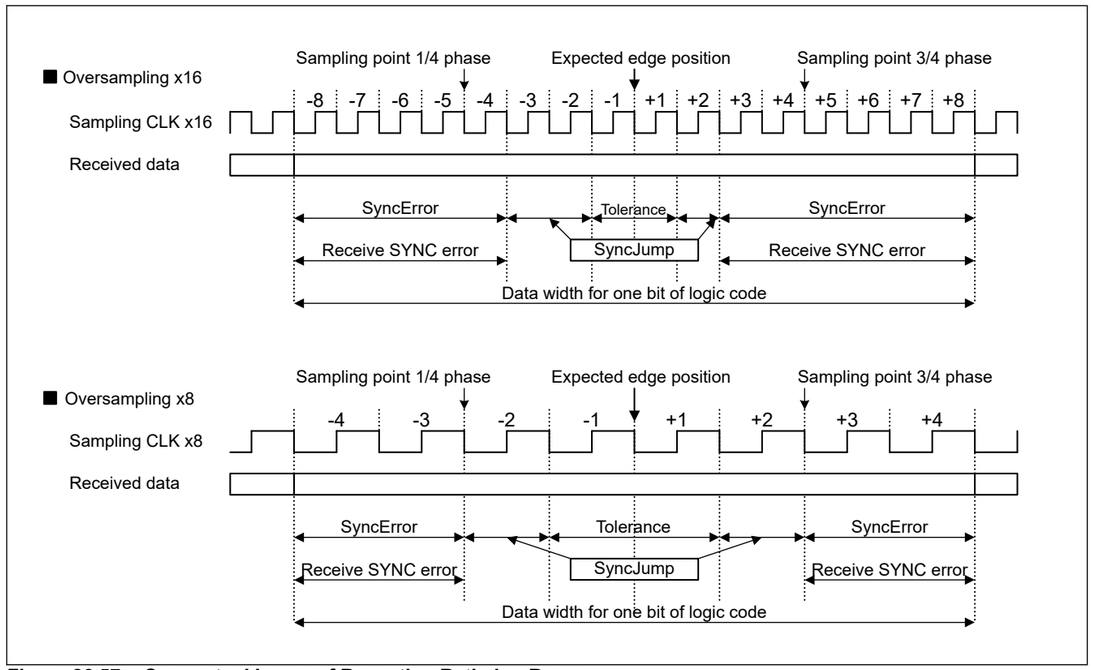


Figure 26.57 Conceptual Image of Reception Retiming Range

26.5.10 Polarity Setting for Manchester Code

The polarity of the Manchester code can be set with the Manchester Control Register (MCR).

It can be set separately for transmission and reception. Use the MCR.TMPOL bit to set the polarity for transmission and the MCR.RMPOL bit to set the polarity for reception.

The Manchester code polarity setting is valid for the preface area, the data area, and the parity or multi-processor area.

When the initial settings (TMPOL/RMPOL = 0) are used for the polarity of Manchester code, logic 0 is encoded as a zero-to-one transition in Manchester code and logic 1 is encoded as a one-to-zero transition in Manchester code. If the settings are changed to TMPOL/RMPOL = 1, logic 0 is encoded as a one-to-zero transition in Manchester code and logic 1 is encoded as a zero-to-one transition in Manchester code. Figure 26.58 shows the conceptual image of the settings and operation.

Separately from the function above, the transmitted and received data in the data area can be inverted by the transmitted/received data inversion function (CCR3.SINV). Since the polarity of Manchester code (MCR.TMPOL/RMPOL) can be set separately from the transmitted/received data invert function (CCR3.SINV), if both are set to inversion (MCR.TMPOL/RMPOL = 1 and CCR3.SINV = 1), the transmitted and received data are set to initial state (inversion + inversion = normal).

The polarity of the start bit area can be set by a register different from the ones mentioned above.

Since a different register is used, the polarity of the start bit area is not affected by the polarity setting for Manchester code mentioned above.

For details on the setting for the start bit area, see section 26.5.1. Frame Format (2).

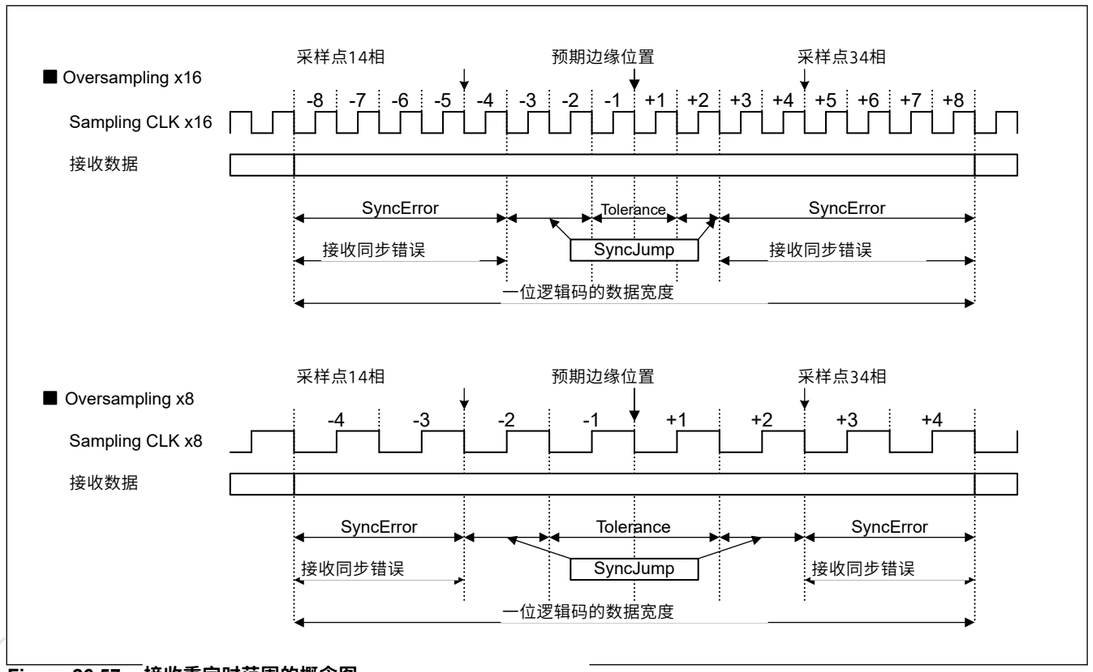


Figure 26.57 接收重定时范围的概念图

26.5.10 曼彻斯特码的极性设置

曼彻斯特码的极性可以通过曼彻斯特控制寄存器(MCR)设置。

可以分别设置发送和接收。使用MCR.TMPOL位设置传输的极性和MCR.RMPOL位设置接收极性。

曼彻斯特码极性设置对前言区、数据区、奇偶校验或多处理器区有效。

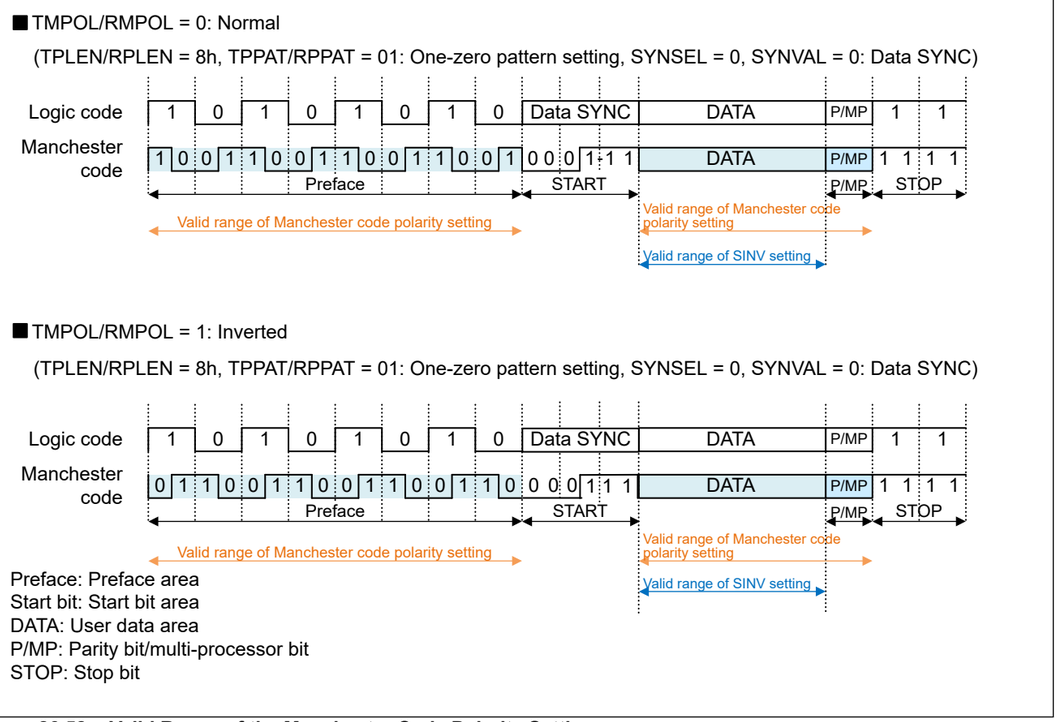
当初始设置(TMPOLRMPOL=0)用于曼彻斯特代码的极性时，逻辑0被编码为曼彻斯特代码中的零到一转换，逻辑1被编码为曼彻斯特代码中的一对零转换。如果设置更改为TMPOLRMPOL=1，则逻辑0被编码为曼彻斯特代码中的一对零转换，逻辑1被编码为曼彻斯特代码中的零到一转换。图26.58显示了设置和操作的概念图。

与上述功能不同，数据区中的发送和接收数据可以通过发送接收数据反转功能(CCR3.SINV)反转。由于曼彻斯特码的极性（MCR.TMPOLRMPOL）可以与发送的接收数据反转功能（CCR3.SINV）分开设置，如果两者都设置为反转（MCR.TMPOLRMPOL=1和CCR3.SINV=1），发送和接收的数据设置为初始状态（反转+反转=正常）。

起始位区域的极性可以通过与上述不同的寄存器来设置。

由于使用了不同的寄存器，因此起始位区域的极性不受上述曼彻斯特码极性设置的影响。

关于起始位区域的设置，请参阅26.5.1节。帧格式(2)。



Preface: Preface area
Start bit: Start bit area
DATA: User data area
P/MP: Parity bit/multi-processor bit
STOP: Stop bit

Figure 26.58 Valid Range of the Manchester Code Polarity Setting

26.5.11 Errors in Manchester Mode

There are the following errors in Manchester mode:

1. Parity error
2. Over run error
3. Framing error
4. Manchester error
5. Preface error
6. Start Bit error
7. Receive SYNC error

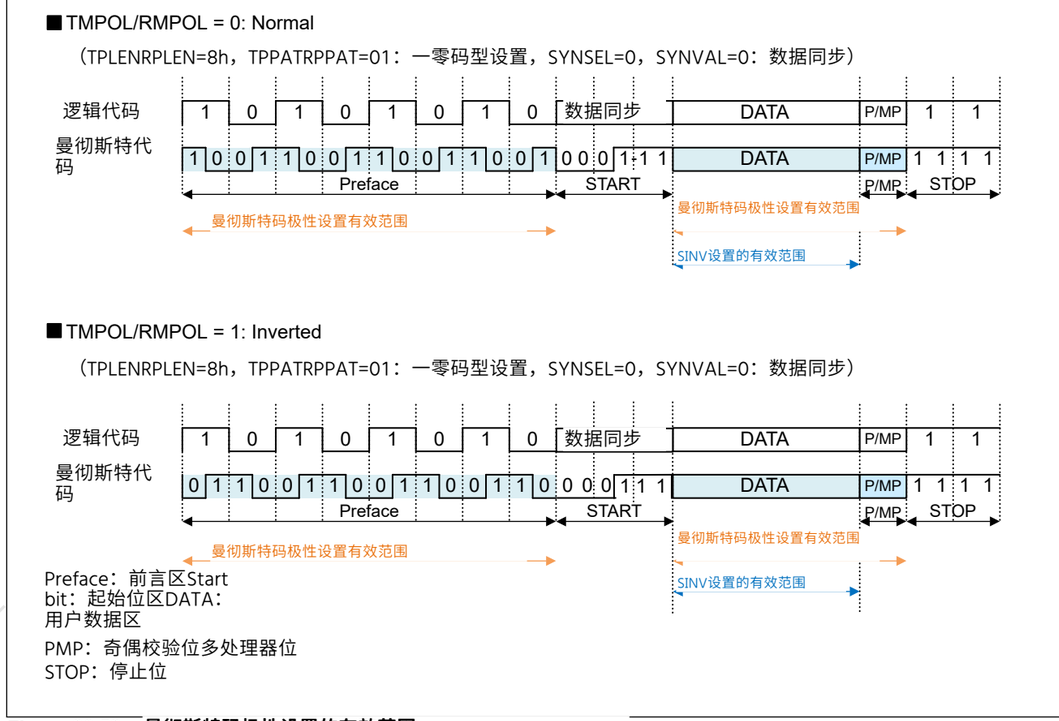
For errors (1) to (3), see section 26.3.9. Serial Data Reception in Asynchronous Mode (1) because they are the same as in asynchronous mode.

Each errors are judged in each area, but they are reflected on flags and operations at the timing of 3/4-bit sampling of the STOP bit area. If a preface error or start bit error is detected, subsequent data will not be received. Therefore, no other error detection is performed, and the error flag holds the previous information.

Table 26.32 lists the states of the serial status register when detecting errors and judgment about whether to store data in the RDR.

Table 26.33 lists the errors that can be detected in each area of a Manchester frame.

If a Preface error or Start bit error is detected, subsequent data will not be received. Therefore, no other error detection is performed, and the error flag holds the result of the previous frame reception. Also, if an error is detected in the previous frame, data will not be received, but errors in the pre-face area and start bit area will update that flag. Table 26.34 shows the flags and actions in this case.



Preface：前言区Start bit：起始位区DATA：用户数据区
PMP：奇偶校验位多处理器位
STOP：停止位

Figure 26.58 曼彻斯特码极性设置的有效范围

26.5.11 曼彻斯特模式中的错误

曼彻斯特模式有以下错误：

1.奇偶校验错误
2.溢出错误
3.构图错误
4.曼彻斯特错误
5.前言错误
6.起始位错误
7.收到SYNC错误

对于错误(1)至(3)，请参阅第26.3.9节。异步模式下的串行数据接收(1)因为它们与异步模式下相同。

在每个区域中判断每个错误，但它们反映在标志和操作上，在3个4位采样的时间
停止位区域。如果检测到前言错误或起始位错误，则不会接收后续数据。因此，不进行其他错误检测，错误标志保存先前的信息。

表26.32列出了串口状态寄存器在检测错误和判断是否存储数据时的状态
RDR.

表26.33列出了可以在曼彻斯特帧的每个区域中检测到的错误。

如果检测到Preface错误或Startbit错误，则不会接收后续数据。因此，不进行其他错误检测，错误标志保存前一帧接收的结果。此外，如果在前一帧中检测到错误，则不会接收数据，但前脸区域和起始位区域中的错误将更新该标志。表26.34显示了这种情况下的标志和操作。

(4) Manchester error

A Manchester error is generated when a Manchester code error is detected.

In Manchester code, there must be an edge (transition) in the center of the bit.

In the data area of a received frame (including the parity/multi-processor bit), the values of the 1/4-bit and 3/4-bit sampling points are checked in each received 1-bit data, and a Manchester code error is determined if these two values match.

If a Manchester code error is detected, the Manchester error flag (MSR.MER) is asserted.

If a Manchester error occurs, it is handled as an interrupt source and event source. If a Manchester error is detected, the next reception is not performed until the corresponding error flag is cleared.

(5) Preface error

A preface error is generated when the preface pattern does not match or a Manchester code error is detected in the preface area. If a preface error is detected, the preface error flag (MSR.PFER) is asserted.

It is possible to set whether to use this error flag as an interrupt source with the setting of the MCR register.

When MCR.PFEREN = 1, a preface error is handled as an interrupt source or event source. If a preface error is detected, the next reception is not performed until the corresponding error flag is cleared.

When MCR.PFEREN = 0, a preface error is not handled as an interrupt source or event source, and the next reception is not halted. However, a preface error is notified to MSR.PFER.

(6) Start bit error

A start bit error is generated when a mismatch is detected between the start bit area in the received frame and the preset start bit pattern. Upon detection of a start bit error, a start bit error flag (MSR.SBER) is asserted.

It is possible to set whether to use the start bit error as an interrupt source with the setting of the MCR register.

When MCR.SBEREN = 1, a start bit error is handled as an interrupt source or event source. If a start bit error is detected, the next reception is not performed until the corresponding error flag is cleared.

When MCR.SBEREN = 0, a start bit error is not handled as an interrupt source or event source, and the next reception is not halted. However, a start bit error is notified to MSR.SBER.

(7) Receive SYNC error

When the receive retiming function described in section 26.5.9. Receive Retiming is enabled, the receive retiming operation is performed.

If no edges are detected within the receive retiming range (SyncError area in Figure 26.57) when receive timing operation is being performed, a receive SYNC error is generated. Upon detection of a receive SYNC error, a receive SYNC error flag (MSR.SYER) is asserted. In areas not subject to retiming, receive SYNC errors are not detected.

The preface area*1, the start bit area*1,*2, and the data area (excluding the stop bit) for which receive retiming operation is performed are checked.

It is possible to set whether to use the receive SYNC error as an interrupt source with the setting of the MCR register.

When MCR.SYEREN = 1, a receive SYNC error is handled as an interrupt source or event source. If a receive SYNC error is detected, the next reception is not performed until the corresponding error flag is cleared.

When MCR.SYEREN = 0, a receive SYNC error is not handled as an interrupt source or event source, and the next reception is not halted. However, a receive SYNC error is notified to MSR.SYER.

Note 1. In the case of a frame that starts with a pattern that expects the first half of the bit to be High, it is excluded from retiming.

Note 2. In the start bit area, when there is no preface length and 3 bit start bit is set, it is not subject to retiming.

Also, the 1st bit and the 2nd bit in the start bit area when 3 bit start bit is set are not subject to retiming.

Table 26.32 Flags in the CSR Register and Receive Data Handling in Manchester Mode (1 of 2)

Flag in the CSR register			Flag in the MRS register				Received data	Received error status (SCIn_ERI interrupt / event generation)
ORER	FER	PER	MER	SBER*1	PFER*1	SYER		
0	0	0	0	0	0	0	transfer to RDR	No error

(4)曼彻斯特错误

当检测到曼彻斯特码错误时，就会产生曼彻斯特错误。

在曼彻斯特码中，位的中心必须有一个边（转换）。

在接收帧的数据区（包括奇偶校验多处理器位），在每个接收的1位数据中检查1个4位和3个4位采样点的值，确定曼彻斯特码错误如果这两个值匹配。

如果检测到曼彻斯特代码错误，则会置位曼彻斯特错误标志(MSR.MER)。

如果发生曼彻斯特错误，则将其作为中断源和事件源进行处理。如果检测到曼彻斯特错误，则在清除相应错误标志之前不会执行下一次接收。

(5)前言错误

当前言模式不匹配或在前言区检测到曼彻斯特码错误时，会产生前言错误。如果检测到前言错误，则断言前言错误标志(MSR.PFER)。

可以通过MCR寄存器的设置来设置是否将此错误标志用作中断源。

当MCR.PFEREN=1时，前言错误作为中断源或事件源处理。如果检测到前言错误，则在相应的错误标志被清除之前不会执行下一次接收。

当MCR.PFEREN=0时，前言错误不会作为中断源或事件源处理，并且不会停止下一次接收。但是，将向MSR.PFER通知前言错误。

(6)起始位错误

当检测到接收帧中的起始位区域与预设的起始位模式不匹配时，会产生起始位错误。在检测到起始位错误时，将置位起始位错误标志(MSR.SBER)。

可以通过MCR寄存器的设置来设置是否使用起始位错误作为中断源。

当MCR.SBEREN=1时，起始位错误作为中断源或事件源处理。如果检测到起始位错误，则在清除相应错误标志之前不会执行下一次接收。

当MCR.SBEREN=0时，不将起始位错误作为中断源或事件源处理，并且不会停止下一次接收。但是，将向MSR.SBER通知起始位错误。

(7)接收同步错误

当接收重定时功能在第26.5.9节中描述。启用接收重定时，执行接收重定时操作。

如果在执行接收定时操作时在接收重定时范围内（图26.57中的SyncError区域）没有检测到边沿，则会产生接收SYNC错误。在检测到接收同步错误时，接收同步错误标志(MSR.SYER)被置位。在不受重定时限制的区域中，不会检测到接收同步错误。

检查执行接收重定时操作的前言区域*1、起始位区域*1、*2和数据区域（不包括停止位）。

可以通过MCR寄存器的设置来设置是否使用接收SYNC错误作为中断源。

当MCR.SYEREN=1时，接收SYNC错误将作为中断源或事件源处理。如果检测到接收SYNC错误，则在清除相应错误标志之前不会执行下一次接收。

当MCR.SYEREN=0时，接收SYNC错误不会作为中断源或事件源处理，并且不会停止下一次接收。但是，接收SYNC错误会通知给MSR.SYER。

注1.对于以预期位的前半部分为高的模式开始的帧，它被排除在重定时之外。

注2.在起始位区域中，当没有序言长度且设置了3位起始位时，不进行重定时。

此外，当设置3位起始位时，起始位区域中的第1位和第2位不受重定时的影响。

Table 26.32 CSR寄存器中的标志和曼彻斯特模式下的接收数据处理(1of2)

CSR寄存器中的标志			MRS寄存器中的标志				接收数据	收到错误状态（SCIn_ERI中断事件产生）
ORER	FER	PER	MER	SBER*1	PFER*1	SYER		
0	0	0	0	0	0	0	转移到RDR	没有错误

Table 26.32 Flags in the CSR Register and Receive Data Handling in Manchester Mode (2 of 2)

Flag in the CSR register			Flag in the MRS register				Received data	Received error status (SCIn_ERI interrupt / event generation)
ORER	FER	PER	MER	SBER*1	PFER*1	SYER		
0	1	0	0	0	0	0	transfer to RDR	Framing error
0	0	1	0	0	0	0	transfer to RDR	Parity error
0	1	1	0	0	0	0	transfer to RDR	Framing error + Parity error
0	0	0	1	0	0	0	transfer to RDR	Manchester error
0	1	0	1	0	0	0	transfer to RDR	Framing error + Manchester error
0	0	1	1	0	0	0	transfer to RDR	Parity error + Manchester error
0	1	1	1	0	0	0	transfer to RDR	Framing error + Parity error + Manchester error
1	0	0	0	0	0	0	Lost	Overrun error
1	1	0	0	0	0	0	Lost	Overrun error + Framing error
1	0	1	0	0	0	0	Lost	Overrun error + Parity error
1	1	1	0	0	0	0	Lost	Overrun error + Framing error + Parity error
1	0	0	1	0	0	0	Lost	Overrun error + Manchester error
1	1	0	1	0	0	0	Lost	Overrun error + Framing error + Manchester error
1	0	1	1	0	0	0	Lost	Overrun error + Parity error + Manchester error
1	1	1	1	0	0	0	Lost	Overrun error + Framing error + Parity error + Manchester error
0	Combination of above			0	0	1	transfer to RDR	Errors above + Receive SYNC error*2
1				0	0	1	Lost	Errors above + Receive SYNC error*2
hold	hold	hold	hold	0	1	0	Lost	Preface error*3
hold	hold	hold	hold	1	0	0	Lost	Start bit error*3
hold	hold	hold	hold	0	1	1	Lost	Preface error*3 + Receive SYNC error*2
hold	hold	hold	hold	1	0	1	Lost	Start bit error*3 + Receive SYNC error*2

Note 1. Start bit error and Preface error never become 1 at the same time.
Note 2. When MCR.SYEREN = 1, SCIn_ERI interrupt / event is generated by SYER factor.
Note 3. If MCR.PFEREN = 1 or MCR.SBEREN = 1, an SCIn_ERI interrupt / event is generated when the corresponding flag is set.

Table 26.33 Errors Detectable in Each Area

	Preface error (PFER)	Start Bit error (SBER)	Manchester error (MER)	Receive SYNC error (SYER)	Parity error (PER)	Framing error (FER)
Preface area	✓	—	—*1	✓*2	—	—
Start Bit area	—	✓	—	✓*2	—	—
Data area	—	—	✓	✓	—	—
Parity area	—	—	✓	✓	✓	—
Multi-processor area	—	—	✓	✓	—	—
Stop Bit area	—	—	—	—	—	✓

Note: ✓: Detected, —: Not detected
Note 1. When an Manchester code error occurs in the preface area, it is defined as a preface error.
Note 2. It may not be subject to Receive SYNC error detection. For details see the text section 26.5.11. Errors in Manchester Mode (7)

Table 26.32 CSR寄存器中的标志和曼彻斯特模式下的接收数据处理(2of2)

CSR寄存器中的标志			MRS寄存器中的标志				接收数据	收到错误状态（SCIn_ERI中断事件产生）
ORER	FER	PER	MER	SBER*1	PFER*1	SYER		
0	1	0	0	0	0	0	转移到RDR	构图错误
0	0	1	0	0	0	0	转移到RDR	奇偶校验错误
0	1	1	0	0	0	0	转移到RDR	成帧错误+奇偶校验错误
0	0	0	1	0	0	0	转移到RDR	曼彻斯特错误
0	1	0	1	0	0	0	转移到RDR	帧错误+曼彻斯特错误
0	0	1	1	0	0	0	转移到RDR	奇偶校验错误+曼彻斯特错误
0	1	1	1	0	0	0	转移到RDR	成帧错误+奇偶校验错误+曼彻斯特错误
1	0	0	0	0	0	0	Lost	溢出错误
1	1	0	0	0	0	0	Lost	溢出错误+成帧错误
1	0	1	0	0	0	0	Lost	溢出错误+奇偶校验错误
1	1	1	0	0	0	0	Lost	溢出错误+帧错误+奇偶校验错误
1	0	0	1	0	0	0	Lost	超限错误+曼彻斯特错误
1	1	0	1	0	0	0	Lost	溢出错误+帧错误+曼彻斯特错误
1	0	1	1	0	0	0	Lost	溢出错误+奇偶校验错误+曼彻斯特错误
1	1	1	1	0	0	0	Lost	溢出错误+成帧错误+奇偶校验错误+曼彻斯特错误
0	以上结合			0	0	1	转移到RDR	上述错误+接收同步错误*2
1				0	0	1	Lost	上述错误+接收同步错误*2
hold	hold	hold	hold	0	1	0	Lost	前言错误*3
hold	hold	hold	hold	1	0	0	Lost	起始位错误*3
hold	hold	hold	hold	0	1	1	Lost	前言错误*3+接收同步错误*2
hold	hold	hold	hold	1	0	1	Lost	起始位错误*3+接收同步错误*2

注1.起始位错误和前言错误永远不会同时变为1。
注2.当MCR.SYEREN=1时，由SYER因素产生SCIn_ERI中断事件。
注3.如果MCR.PFEREN=1或MCR.SBEREN=1，则在设置相应标志时产生SCIn_ERI中断事件。

Table 26.33 每个区域可检测到的错误

	前言错误(PFER)	起始位错误(SBER)	曼彻斯特错误(MER)	接收同步错误(SYER)	奇偶校验错误(PER)	成帧错误(FER)
前言区	✓	—	—*1	✓*2	—	—
起始位区域	—	✓	—	✓*2	—	—
数据区	—	—	✓	✓	—	—
平价区	—	—	✓	✓	✓	—
Multi-processor area	—	—	✓	✓	—	—
停止位区域	—	—	—	—	—	✓

Note: ：检测到，一：未检测到
注1.当序言区出现曼彻斯特码错误时，定义为序言错误。
注2.它可能不受ReceiveSYNC错误检测的影响。有关详细信息，请参阅文本部分26.5.11。曼彻斯特模式中的错误(7)

Table 26.34 Operation status due to presence / absence of error in previous frame and operation status list in multiprocessor mode (1 of 2)

Previous frame	Each area of the Frame					PFERE N	SBERE N	SYERE N	received data	Error flag	Interrupt request	Event signal
	preface	start bit	data	parity	stop							
No Error	PFER No SYER*1	No Error	Don't Care	Don't Care	Don't Care	0	Don't Care	Don't Care	Lost	set PFER*1	not output	not output
						1					output	output
	No Error	SBER No SYER*1	Don't Care	Don't Care	Don't Care	Don't Care	0	Don't Care	Lost	set SBER*1	not output	not output
							1				output	output
	SYER No PFER	No Error	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0	transfer to RDR	set SYER	not output	not output
								1	Lost		output	output
	No Error	SYER No SBER	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0	transfer to RDR	set SYER	not output	not output
								1	Lost		output	output
	No Error	No Error	SYER		No Error	Don't Care	Don't Care	0	transfer to RDR	set SYER	not output	not output
								1			output	output
	No Error	No Error	MER		No Error	Don't Care	Don't Care	Don't Care	transfer to RDR	set MER	output	output
	No Error	No Error	Don't Care	PER	No Error	Don't Care	Don't Care	Don't Care	transfer to RDR	set PER	output	output
	No Error	No Error	Don't Care	Don't Care	FER	Don't Care	Don't Care	Don't Care	transfer to RDR	set FER	output	output
	There is some error ORER					Don't Care	Don't Care	Don't Care	Lost	set some flags*2	output	output
	No Error	No Error	No Error	No Error	No Error ORER	Don't Care	Don't Care	Don't Care	Lost	set ORER	output	output

Table 26.34 由于前一帧中不存在错误而导致的操作状态和多处理器模式下的操作状态列表（1of2）

Previous frame	框架的每个区域					PFERE N	SBERE N	SYERE N	接收数据	错误标志	Interrupt request	事件信号
	preface	起始位	data	parity	stop							
没有错误	PFER No SYER*1	没有错误	不在乎	不在乎	不在乎	0	不在乎	不在乎	Lost	set PFER*1	不输出	不输出
						1					output	output
	没有错误	SBER No SYER*1	不在乎	不在乎	不在乎	不在乎	0	不在乎	Lost	set SBER*1	不输出	不输出
							1				output	output
	SYER No PFER	没有错误	不在乎	不在乎	不在乎	不在乎	不在乎	0	转移到RDR	set SYER	不输出	不输出
								1	Lost		output	output
	没有错误	SYER No SBER	不在乎	不在乎	不在乎	不在乎	不在乎	0	转移到RDR	set SYER	不输出	不输出
								1	Lost		output	output
	没有错误	没有错误	SYER		没有错误	不在乎	不在乎	0	转移到RDR	set SYER	不输出	不输出
								1			output	output
	没有错误	没有错误	MER		没有错误	不在乎	不在乎	不在乎	转移到RDR	设置MER	output	output
	没有错误	没有错误	不在乎	PER	没有错误	不在乎	不在乎	不在乎	转移到RDR	设置PER	output	output
	没有错误	没有错误	不在乎	不在乎	FER	不在乎	不在乎	不在乎	转移到RDR	设置FER	output	output
	有一些错误 ORER					不在乎	不在乎	不在乎	Lost	设置一些标志*2	output	output
	没有错误	没有错误	没有错误	没有错误	没有错误 ORER	不在乎	不在乎	不在乎	Lost	set ORER	output	output

Table 26.34 Operation status due to presence / absence of error in previous frame and operation status list in multiprocessor mode (2 of 2)

Previous frame	Each area of the Frame					PFERE N	SBERE N	SYERE N	received data	Error flag	Interrupt request	Event signal
	preface	start bit	data	parity	stop							
some error*3 *6	PFER No SYER*1	No Error	Don't Care	Don't Care	Don't Care	0	Don't Care	Don't Care	Lost	set PFER*1	output*4	not output*5
						1						
	No Error	SBER No SYER*1	Don't Care	Don't Care	Don't Care	Don't Care	0	Don't Care		set SBER*1		
							1					
	SYER No PFER	No Error	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0		set SYER		
								1				
	No Error	SYER No SBER	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0		set SYER		
								1				
	No Error	No Error	SYER		No Error	Don't Care	Don't Care	0		don't set any flags		
								1				
	No Error	No Error	MER		No Error	Don't Care	Don't Care	Don't Care				
	No Error	No Error	Don't Care	PER	No Error	Don't Care	Don't Care	Don't Care				
	No Error	No Error	Don't Care	Don't Care	FER	Don't Care	Don't Care	Don't Care				
	There is some error ORER					Don't Care	Don't Care	Don't Care				
	No Error	No Error	No Error	No Error	No Error ORER	Don't Care	Don't Care	Don't Care				

Note 1. If SYER is detected, the SYER flag is also set. Other operations are as shown in this table.
Note 2. Other detected error flags including ORER are also set.
Note 3. If all the error flags are cleared before the STOP bit is judged, the operation will be the same as the case where there is no error in the previous frame of this table.
Note 4. Since the SCIn_ERI interrupt request is level output, it remains active due to errors in the previous frame regardless of the presence or absence of error in the relevant frame.
Note 5. Since the error cause is continuously detected, the SCIn_ERI event is not newly output regardless of the presence or absence of errors in the relevant frame.
Note 6. For PFER, SBER, and SYER, when each enable bit is set to disable, it is treated as no error.

Table 26.35 Operation when MPIE = 1 in multi-processor mode (MPIE = 0)

MPB*1	Each area of the frame					PFERE N	SBERE N	SYERE N	received data	Error flag	Interrupt request	Event signal
	preface	start bit	data	parity	stop							
1	No Error	No Error	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	transfer to RDR	set some flags	output*2	output*2
	No PFER	No SBER	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0				
	SYER*3	SYER*3						1	Lost	don't set any flags	not output	not output
	PFER	No Error	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care				
	No Error	SBER	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care					

Note 1. If the received MPB bit us 0, it is not received the frame, and the operation is the same as lost of the reception data of this table.
Note 2. If no error is detected, SCIn_RXI interrupt request or event is output, and if it is detected, SCIn_ERI interrupt request or event is output.

Table 26.34 由于前一帧中不存在错误而导致的操作状态和多处理器模式下的操作状态列表（2of2）

Previous frame	框架的每个区域					PFERE N	SBERE N	SYERE N	接收数据	错误标志	Interrupt request	事件信号
	preface	起始位	data	parity	stop							
一些错误*3*6	PFER No SYER*1	没有错误	不在乎	不在乎	不在乎	0	不在乎	不在乎	Lost	set PFER*1	output*4	不输出*5
						1						
	没有错误	SBER No SYER*1	不在乎	不在乎	不在乎	不在乎	0	不在乎		set SBER*1		
							1					
	SYER No PFER	没有错误	不在乎	不在乎	不在乎	不在乎	不在乎	0		set SYER		
								1				
	没有错误	SYER No SBER	不在乎	不在乎	不在乎	不在乎	不在乎	0		set SYER		
								1				
	没有错误	没有错误	SYER		没有错误	不在乎	不在乎	0		不要设置任何标志		
								1				
	没有错误	没有错误	MER		没有错误	不在乎	不在乎	不在乎				
	没有错误	没有错误	不在乎	PER	没有错误	不在乎	不在乎	不在乎				
	没有错误	没有错误	不在乎	不在乎	FER	不在乎	不在乎	不在乎				
	有一些错误 ORER					不在乎	不在乎	不在乎				
	没有错误	没有错误	没有错误	没有错误	没有错误 ORER	不在乎	不在乎	不在乎				

注1.如果SYER被检测到，SYER标志也被设置。其他操作如本表所示。
注2.还设置了其他检测到的错误标志，包括ORER。
注3.如果在判断STOP位之前清除所有错误标志，则操作将与该表的前一帧没有错误的情况相同。

注4.由于SCIn_ERI中断请求是电平输出，因此无论相关帧中是否存在错误，它都会由于前一帧中的错误而保持有效。

注5.由于不断检测错误原因，因此无论相关帧中是否存在错误，都不会重新输出SCIn_ERI事件。

注6.对于PFER、SBER和SYER，当每个使能位设置为禁用时，它被视为无错误。

Table 26.35 多处理器模式下MPIE=1时的操作(MPIE=0)

MPB*1	框架的每个区域					PFERE N	SBERE N	SYERE N	接收数据	错误标志	Interrupt request	事件信号
	preface	起始位	data	parity	stop							
1	没有错误	没有错误	不在乎	不在乎	不在乎	不在乎	不在乎	不在乎	转移到RDR	设置一些标志	output*2	output*2
	No PFER	No SBER	不在乎	不在乎	不在乎	不在乎	不在乎	0				
	SYER*3	SYER*3						1	Lost	不要设置任何标志	不输出	不输出
	PFER	没有错误	不在乎	不在乎	不在乎	不在乎	不在乎	不在乎				
	没有错误	SBER	不在乎	不在乎	不在乎	不在乎	不在乎					

注1.如果接收到的MPB位我们为0，则不接收该帧，操作与该表的接收数据丢失相同。注2.如果没有检测到错误，则输出SCIn_RXI中断请求或事件，如果检测到，则输出SCIn_ERI中断请求或事件。

Note 3. When SYER is detected in the preface area or the start bit area, the behavior of handling as an error depending on the SYEREN bit changes.

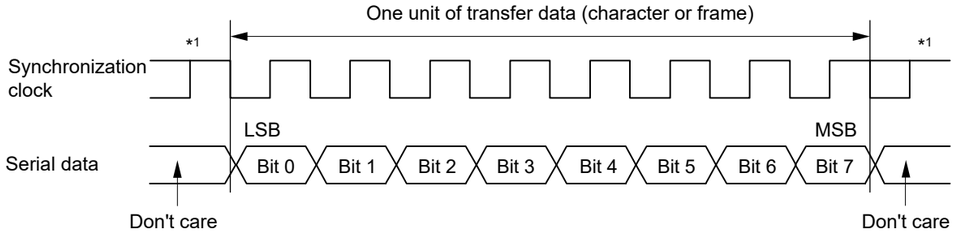
26.6 Operation in Clock Synchronous Mode

Figure 26.59 shows the data format for clock synchronous serial data communications.

In clock synchronous mode, data is transmitted or received in synchronization with clock pulses. For single-character data transfer, data consists of 8-bit. In clock synchronous mode, no parity bit can be added.

In data transmission when CPHA = 1 and CPOL = 1, the SCI outputs data from one falling edge of the synchronization clock to the next falling edge. In data reception, the SCI receives data in synchronization with the rising edge of the synchronization clock. After 8-bit data is output, the transmission line holds the last bit as output state. When the CPHA bit is 0 in slave mode, the transmission line holds the first bit output state.

Within the SCI, the transmitter and receiver are independent units, enabling full-duplex communications by using a shared a communication clock of the transmitter and the receiver. Furthermore, because both the transmitter and the receiver also have a double-buffered structure, so that the next transmit data can be written during transmission or the previous receive data can be read during reception, enabling continuous data transfer.



Note 1. Holds a high level except during continuous transfer.

Figure 26.59 Data format in clock synchronous serial communications with LSB-first order

26.6.1 Clock

If the maximum speed of SCK = 1/2TCLK is set in Clock Synchronous and Simple SPI mode, Do not make PCLK less than half the speed of TCLK. If PCLK is made slower than this, malfunction may occur.

1. When the internal clock is selected
   When the SCI operates on an internal clock (CCR3.CKE[1:0] bits are set to 00b or 01b (master mode)), the synchronization clock is output from the SCKn pin. Eight synchronization clock pulses are output during single-character transmission/reception. When no data transfer is performed, the clock is held at high level.*1 In transmission-only or transmission/reception, the synchronization clock is not output unless transmit data is prepared.
   When the internal clock is selected, the clock with a delay from the SCKn signal is used for the master reception sampling clock. This ensures the data setup time and hold time for high-speed communication.

   Note 1. The signal is held high while (CCR3.CPHA = 0 and CCR3.CPOL = 1) or (CCR3.CPHA = 1 and CCR3.CPOL = 1). It is held low while (CCR3.CPHA = 0 and CCR3.CPOL = 0) or (CCR3.CPHA = 1 and CCR3.CPOL = 0).
2. When the external clock is selected
   When the CCR3.CKE[1:0] bits are set to 10b or 11b (slave mode), data is transmitted and received using the external clock that is input from the SCKn pin.

26.6.2 CTS and RTS Functions

In the CTS function, the CTSn_RTSn pin input controls the start of data reception or transmission when the clock source is the internal clock. Setting the CCR1.CTSE bit to 1 enables the CTS function. When the CTS function is enabled, setting the CTSn_RTSn pin low causes data reception or transmission to start.

Setting the CTSn_RTSn pin high while the data transmission or reception is in progress does not affect transmission or reception of the current frame.

注3.在序言区域或起始位区域中检测到SYER时，根据SYEREN位作为错误处理的行为会发生变化。

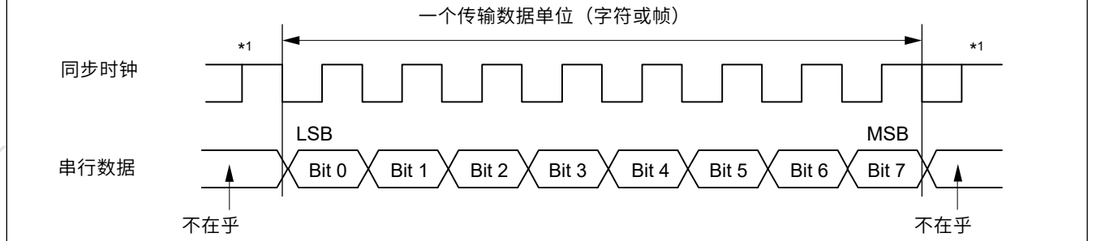
26.6 时钟同步模式下的操作

图26.59显示了时钟同步串行数据通信的数据格式。

在时钟同步模式下，数据的发送或接收与时钟脉冲同步。对于单字符数据传输，数据由8位组成。在时钟同步模式下，不能添加奇偶校验位。

在CPHA=1且CPOL=1时的数据传输中，SCI从同步时钟的一个下降沿到下一个下降沿输出数据。在数据接收中，SCI与同步时钟的上升沿同步接收数据。8位数据输出后，传输线保持最后一位作为输出状态。从机模式下CPHA位为0时，传输线保持第一位输出状态。

在SCI中，发送器和接收器是独立的单元，通过使用发送器和接收器的共享通信时钟来实现全双工通信。此外，由于发送器和接收器都具有双缓冲结构，因此可以在发送过程中写入下一个发送数据，或者在接收过程中读取前一个接收数据，从而实现数据的连续传输。



注1.保持高电平，连续传输期间除外。

Figure 26.59 具有LSB优先顺序的时钟同步串行通信中的数据格式

26.6.1 Clock

如果SCK的最大速度=12TCLK设置在时钟同步和简单SPI模式，不要使PCLK低于TCLK速度的一半。如果PCLK比这慢，可能会发生故障。

1.选择内部时钟时
当SCI在内部时钟上工作时（CCR3.CKE[1:0]位设置为00b或01b（主模式）），同步时钟从SCKn引脚输出。在单字符传输接收期间输出八个同步时钟脉冲。当不进行数据传输时，时钟保持在高电平。*1在仅发送或发送接收中，除非准备好发送数据，否则不会输出同步时钟。选择内部时钟后，将SCKN信号延迟的时钟用于主接收时钟。这确保了高速通信的数据建立时间和保持时间。

注1.当(CCR3.CPHA=0且CCR3.CPOL=1)或(CCR3.CPHA=1且CCR3.CPOL=1)时，信号保持高电平。它在(CCR3.CPHA=0和CCR3.CPOL=0)或(CCR3.CPHA=1和CCR3.CPOL=0)时保持低电平。

2.选择外部时钟时
当CCR3.CKE[1:0]位设置为10b或11b（从模式）时，使用从SCKn引脚输入的外部时钟发送和接收数据。

26.6.2 CTS和RTS函数

在CTS功能中，当时钟源为内部时钟时，CTSn_RTSn引脚输入控制数据接收或发送的开始。将CCR1.CTSE位设置为1可启用CTS功能。当CTS功能使能时，将CTSn_RTSn引脚设置为低电平会导致数据接收或发送开始。

在数据发送或接收过程中将CTSn_RTSn引脚设置为高电平不会影响当前帧的发送或接收。

In the RTS function, the CTSn_RTSn pin output is used to request the start of data reception or transmission when the clock source is an external synchronizing clock. The CTSn_RTSn output goes low when serial communication is enabled. Conditions for output of the CTSn_RTSn low and high are shown as follows:

[Conditions for low output]

Satisfaction of all the following conditions:

Non-FIFO selected when all of the following conditions are satisfied

- The value of the CCR0.RE bit or the CCR0.TE bit is 1
- Next serial communication is enabled.
  - No receive data is present before reading and not receiving. (when CCR0.RE bit = 1)
  - When the transmission data written in TDR is ready for transmission.*1 (when CCR0.TE bit = 1)
- The CSR.ORER flag is 0

Note 1. The CTSn_RTSn pin will be High after starting transmission.

FIFO selected when all of the following conditions are satisfied

- The value of the CCR0.RE bit or the CCR0.TE bit is 1
- Next serial communication is enabled.
  - The number of receive data stored in the receive FIFO (RDR register) is less than the value set in FCR.RSTRG[4:0] (when CCR0.RE bit = 1)
  - When the transmission data written in the transmission FIFO (TDR register) is ready for transmission.*1 (when CCR0.TE bit = 1)
- The CSR.ORER flag is 0

Note 1. The CTSn_RTSn pin will be High after the last data transmission starts.

[Condition for high output]

- The conditions for low output are not satisfied

26.6.3 SCI Initialization in Clock Synchronous Mode

Before transmitting and receiving data, start by writing the initial value 0x00 to the CCR0 register, then continue through the SCI initialization procedure given in the sections describing non-FIFO and FIFO selection in section 26.6.2. CTS and RTS Functions. Anytime the operating mode or transfer format is to be changed, the CCR0.TE and CCR0.RE must write to 0 before the change can be made.

Note: Setting the CCR0.RE bit to 0 initializes neither the ORER, FER, PER, and RDRF flags in CSR nor the RDR register. When the TE bit is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note: Switching the value of the CCR0.TE bit from 1 to 0 when the CCR0.TIE bit is 1 generates an SCIn_TXI interrupt request.

Table 26.36 Example flow of SCI initialization in clock synchronous mode with non-FIFO selected (1 of 2)

No.	Step Name	Description
1	Start initialization	—
2	Set CCR0	Set the CCR0.TEIE, TIE, RIE, TE, and RE bits to 0*1. If you have not changed from the initial settings, you can skip this step.
3	Set FCR	Set the TFRST and RFRST to 1 to empty FIFO. Set the DRES, TTRG[4:0], RTRG[4:0], and RSTRG[4:0] bits.
4	Set CCR3 except MOD[2:0]	Set CCR3 except of communication mode. ● FIFO use/no-use ● Transmission/reception format ● Clock setting ● Leave unused bits (CHR[1:0],STP,RXDSEL,MP,DE, ACS0,GM,BLK) at their initial values.

在RTS功能中，当时钟源为外部同步时钟时，CTSn_RTSn引脚输出用于请求开始数据接收或发送。当串行通信启用时，CTSn_RTSn输出变为低电平。CTSn_RTSn低电平和高电平的输出条件如下所示：

[低输出的条件]

满足以下所有条件：

满足以下所有条件时选择非FIFO

●CCR0.RE位或CCR0.TE位的值为1

●启用下一个串行通信。

在读取和未接收之前不存在接收数据。（当CCR0.RE位=1时）

当写入TDR的传输数据准备好传输时。*1（当CCR0.TE位=1时）

●CSR.ORER标志为0

注1.CTSn_RTSn引脚将在开始发送后为高电平。

满足以下所有条件时选择FIFO

●CCR0.RE位或CCR0.TE位的值为1

●启用下一个串行通信。

接收FIFO（RDR寄存器）中存储的接收数据数量小于FCR.RSTRG[4:0]中设置的值（当CCR0.RE位=1时）

当写入发送FIFO（TDR寄存器）的发送数据准备好发送时。*1（当CCR0.TE位=1时）

●CSR.ORER标志为0

注1.CTSn_RTSn引脚将在最后一次数据传输开始后为高电平。

【高输出条件】

●不满足低输出条件

26.6.3 时钟同步模式下的SCI初始化

在发送和接收数据之前，首先将初始值0x00写入CCR0寄存器，然后继续执行第26.6.2节中描述非FIFO和FIFO选择的部分中给出的SCI初始化过程。CTS和RTS功能。每当要更改操作模式或传输格式时，CCR0.TE和CCR0.RE必须先写入0，然后才能进行更改。

Note: 将CCR0.RE位设置为0既不会初始化CSR中的ORER、FER、PER和RDRF标志，也不会初始化RDR寄存器。当TE位设置为0时，所选FIFO缓冲区的TEND标志未初始化。

Note: 当CCR0.TIE位为1时，将CCR0.TE位的值从1切换为0会产生SCIn_TXI中断请求。

Table 26.36 在时钟同步模式下选择非FIFO的SCI初始化示例流程（1of2）

No.	步骤名称	Description
1	开始初始化	—
2	Set CCR0	将CCR0.TEIE、TIE、RIE、TE和RE位设置为0*1。 如果您尚未更改初始设置，则可以跳过此步骤。
3	Set FCR	将TFRST和RFRST设置为1以清空FIFO。 设置DRES、TTRG[4:0]、RTRG[4:0]和RSTRG[4:0]位。
4	设置CCR3除了MOD[2:0]	设置CCR3通信模式除外。● ● Transmission/reception format ● 时钟设置 ● 将未使用的位(CHR[1:0] STP RXDSEL MP DE ACS0 GM BLK)保留为初始值。

Table 26.36 Example flow of SCI initialization in clock synchronous mode with non-FIFO selected (2 of 2)

No.	Step Name	Description
5	Set CCR3.MOD[2:0]	Set communication mode (MOD[2:0] = 010b)*2.
6	Set CCR2	Select clock, set bit rate *3. Leave unused bits (BCP[2:0],ABCS, ABCSE, BRME,MDDR[7:0]) at their initial values.
7	Set CCR1	Set up the loop-back function, communication terminal status and the CTS/RTS function.
8	Set CCR4	Set up the adjust sampling timing function. Leave unused bits (CMPD[8:0]) at their initial values.
9	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
10	Set CFCLR, FFCLR	Write 1 to the following bits and clear the corresponding flag. CFCLR.RDRFC, FERC, PERC, MFFC, ORERC, DFERC, DPERC, DCMFC, ERSC FFCLR.BRKC, DRC
11	Set CCR0	Set the TE or RE bit to 1.*1 *4 To enable interrupts, set the TE bit and TIE bit, and the RE bit and RIE bit to 1 with one instruction at the same time. Setting the TE and RE bits allows TXDn and RXDn to be used.
12	Initialization completion	—

Note 1. In simultaneous transmit and receive operations, the TE and RE bits in CCR0 should both be to 0 or set to 1 simultaneously.
Note 2. Set CPOL and CPHA before setting the communication mode.
Note 3. If you use an external clock, you do not need to set it.
Note 4. When using the internal clock (master), the setting of reception only is prohibited.

26.6.4 Serial Data Transmission in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 26.60, Figure 26.61, and Figure 26.62 show examples of serial transmission in clock synchronous mode.

In serial data transmission, the SCI operates as follows:

1. The SCI transfers data from the TDR register to the TSR register when data is written to TDR in the SCIn_TXI interrupt handling routine. When starting data transmission, set the CCR0.TIE bit and the CCR0.TE bit to 1 simultaneously by a single instruction. Then a TXI interrupt request is generated.
2. After transferring data from TDR to TSR, the SCI starts transmission. When the CCR0.TIE bit is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to TDR in the SCIn_TXI interrupt handling routine before transmission of the current transmit data finishes. When SCIn_TEI interrupt requests are in use, set the CCR0.TIE bit to 0 and the CCR0.TEIE bit to 1 after the last of the data to be transmitted is written to the TDR register from the handling routine for SCIn_TXI requests.
3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified and in synchronization with the input clock when the use of an external clock is specified. Output of the clock signal is suspended until the input CTS signal is low when the CCR1.CTSE bit is 1 (CTS function enabled).
4. The SCI checks for update to the TDR register on output of the last bit.
5. When the TDR register is updated, the next transmit data is transferred from TDR to TSR, and serial transmission of the next frame starts.
6. If TDR is not updated, the CSR.TEND flag is set to 1. The TXDn pin retains the output state of the last bit. If the CCR0.TEIE bit is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Figure 26.60, Figure 26.61, and Figure 26.62 show examples of serial data transmission.

Table 26.36 在时钟同步模式下选择非FIFO的SCI初始化示例流程（2个中的2个）

No.	步骤名称	Description
5	Set CCR3.MOD[2:0]	设置通信模式(MOD[2:0]=010b)*2。
6	Set CCR2	选择时钟，设置比特率*3。 将未使用的位（BCP[2:0]、ABCS、ABCSE、BRME、MDDR[7:0]）保留为初始值。
7	Set CCR1	设置环回功能、通讯终端状态和CTSRTS功能。
8	Set CCR4	设置调整采样定时功能。将未使用的位(CMPD[8:0])保留为初始值。
9	设置IO端口功能	进行IO端口设置以启用TXDn、RXDn和所需的输入和输出功能 SCKn pins.
10	Set CFCLR, FFCLR	将1写入以下位并清除相应的标志。 CFCLR.RDRFC, FERC, PERC, MFFC, ORERC, DFERC, DPERC, DCMFC, ERSC FFCLR.BRKC, DRC
11	Set CCR0	将TE或RE位设置为1。*1*4要启用中断，请设置TE位和TIE位，以及RE位和 RIE位与一条指令同时为1。 设置TE和RE位允许使用TXDn和RXDn。
12	初始化完成	—

注1.在同时发送和接收操作中，CCR0中的TE和RE位应该都为0或同时设置为1。
注2.在设置通信模式之前设置CPOL和CPHA。
注3.如果使用外部时钟，则无需设置。
注4.使用内部时钟（主时钟）时，禁止仅设置接收。

26.6.4 时钟同步模式下的串行数据传输

(1) Non-FIFO selected

图26.60、图26.61和图26.62显示了时钟同步模式下的串行传输示例。

在串行数据传输中，SCI操作如下：

1.当数据在SCIn_TXI中断处理程序中写入TDR时，SCI将数据从TDR寄存器传输到TSR寄存器。开始数据传输时，通过一条指令同时将CCR0.TIE位和CCR0.TE位设置为1。然后产生一个TXI中断请求。

2.将数据从TDR传输到TSR后，SCI开始传输。当CCR0.TIE位设置为1时，会产生SCIn_TXI中断请求。在当前发送数据发送完成之前，通过在SCIn_TXI中断处理例程中将下一个发送数据写入TDR来启用连续发送。当使用SCIn_TEI中断请求时，在SCIn_TXI请求的处理程序将要发送的最后一个数据写入TDR寄存器后，将CCR0.TIE位设置为0，并将CCR0.TEIE位设置为1。

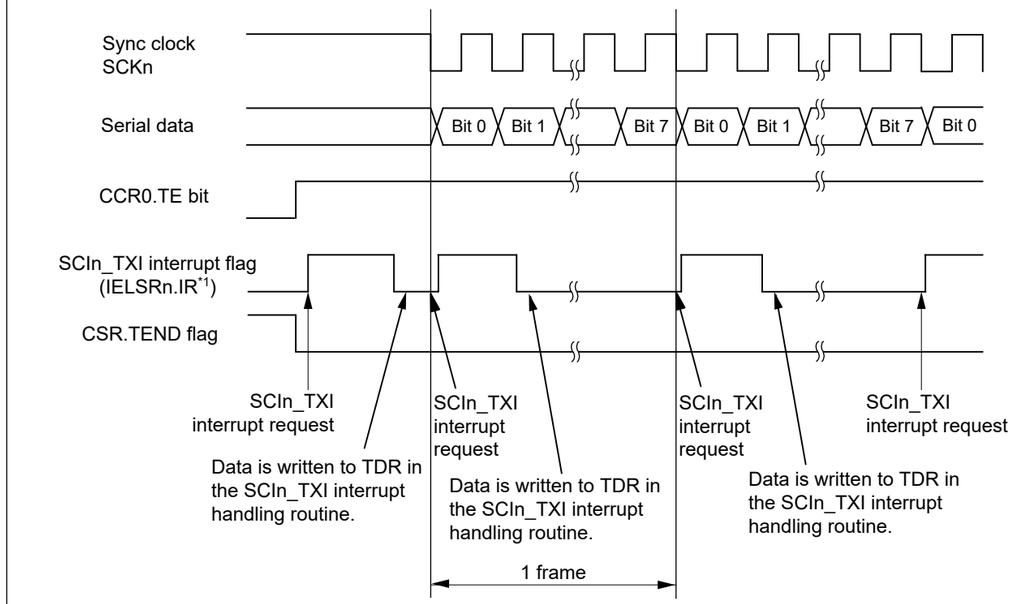
3.指定时钟输出模式时，与输出时钟同步，指定使用外部时钟时，与输入时钟同步，从TXDn引脚发送8位数据。当CCR1.CTSE位为1（CTS功能使能）时，时钟信号的输出被暂停，直到输入CTS信号为低电平。

4.SCI在最后一位输出时检查对TDR寄存器的更新。

5.TDR寄存器更新后，下一个发送数据从TDR传送到TSR，开始下一帧的串行发送。

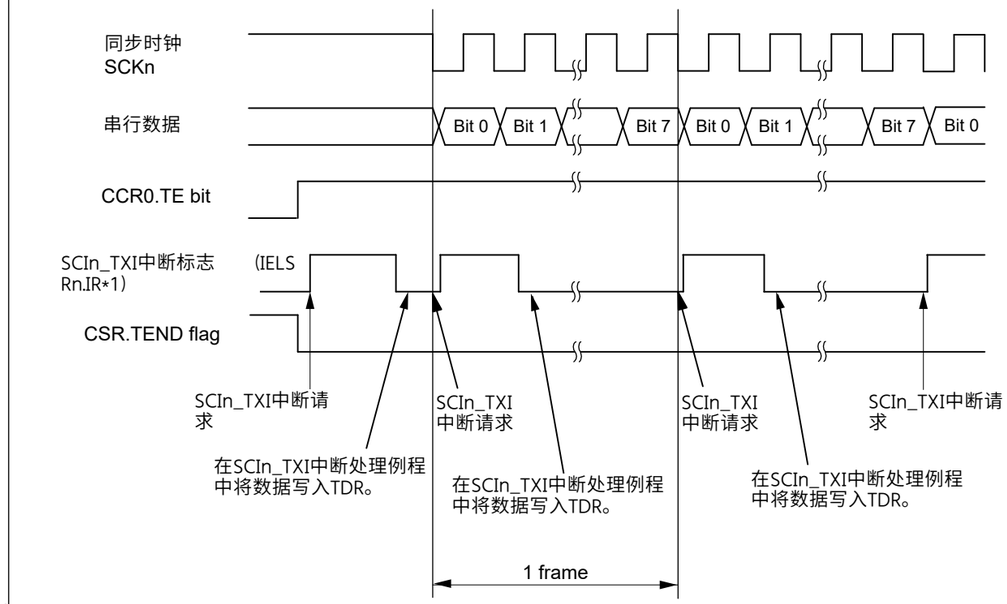
6.如果TDR未更新，则CSR.TEND标志设置为1。TXDn引脚保持最后一位的输出状态。如果CCR0.TEIE位为1，则产生SCIn_TEI中断请求且SCKn引脚保持高电平。

图26.60、图26.61和图26.62显示了串行数据传输的示例。



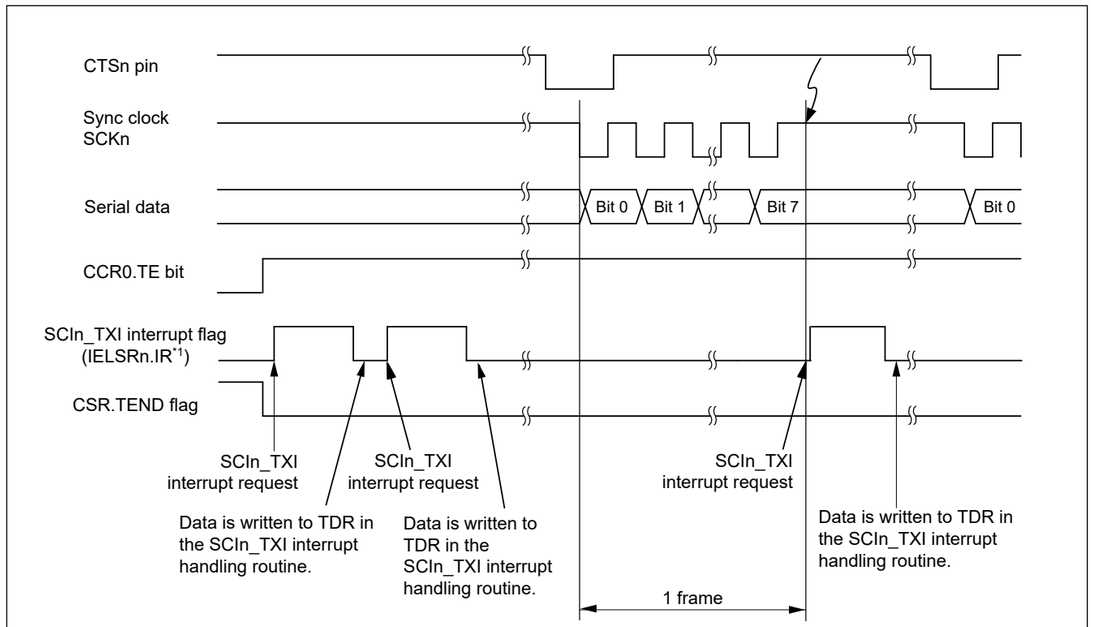
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.60 Example of serial data transmission in clock synchronous mode when the CTS function is not used at the beginning of transmission



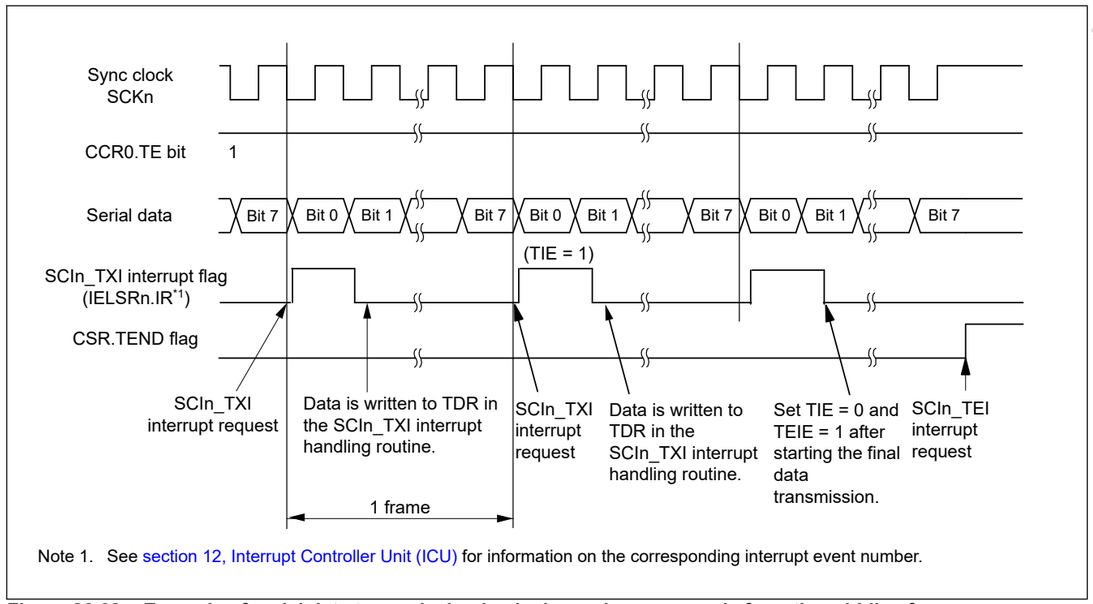
注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.60 传输开始时未使用CTS功能时时钟同步模式下的串行数据传输示例



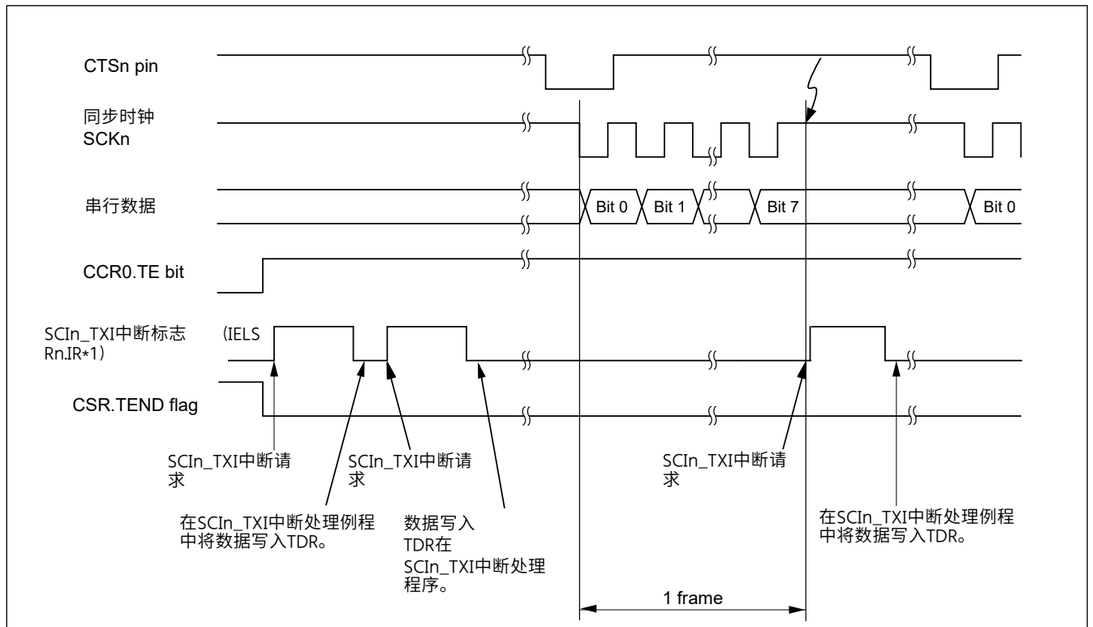
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.61 Example of serial data transmission in clock synchronous mode when the CTS function is used at the beginning of transmission



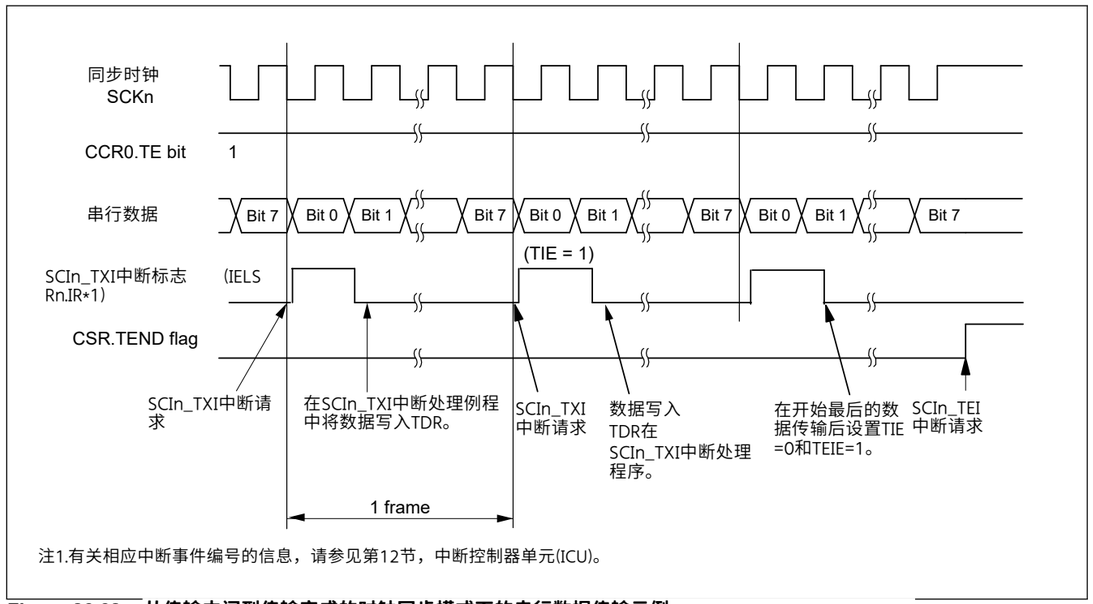
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.62 Example of serial data transmission in clock synchronous mode from the middle of transmission until transmission completion



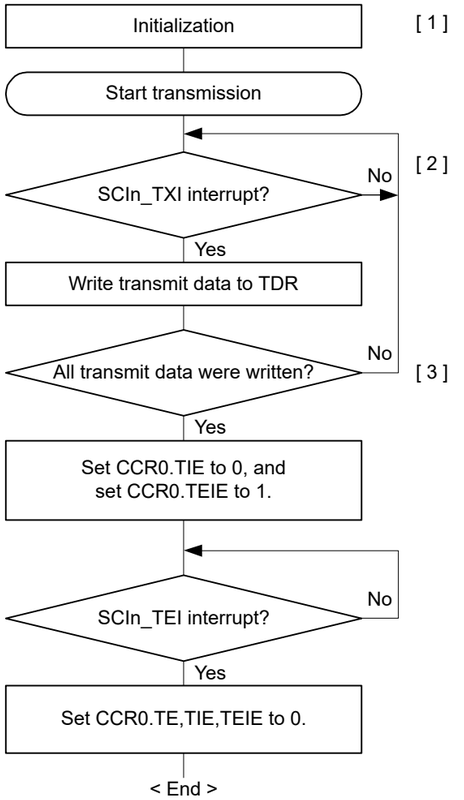
注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.61 传输开始时使用CTS功能时时钟同步模式下的串行数据传输示例



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.62 从传输中间到传输完成的时钟同步模式下的串行数据传输示例



[1] Initialize SCI.
(Set CCR0.TE and TIE to 1.)

[2] Write transmit data to TDR by using SCIn_TXI:
The transmit-data-empty-interrupt(SCIn_TXI) is Generated when transmission-data forwards to TSR from TDR. Write transmit data to TDR once by using a SCIn_TXI.

[3] Serial transmission continuation procedure:
To continue serial transmission write transmit data to TDR by using a SCIn_TXI.
Transmit data can also be written by activating the DMAC or DTC.
If you use SCIn_TEI, set CCR0.TIE = 0 and CCR0.TEIE = 1 after writing the last-transmit-data to TDR.

Note: When the external clock is in use (the value of the CCR3.CKE[1:0] is 10b or 11b), the rising edge on the SCK pin for the last bit sets the CSR.TEND flag to 1. Setting TE to 0 immediately after this, then it may lead to insufficient received data hold time on the receiver side.

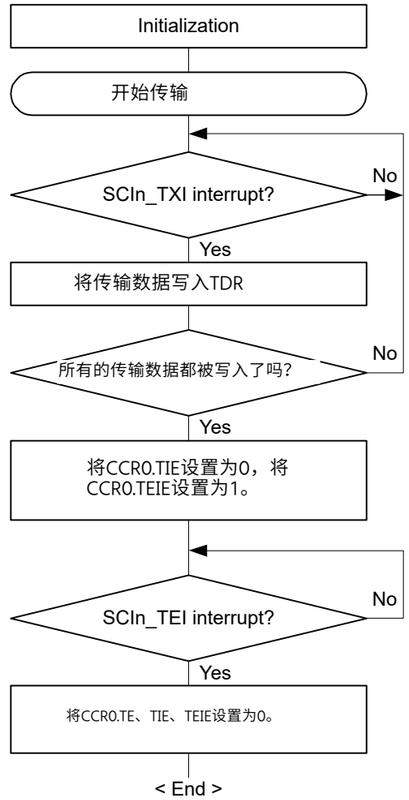
Figure 26.63 Example flow of serial transmission in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 26.64 shows an example of serial transmission in clock synchronous mode with FIFO selected.

In serial data transmission, the SCI operates as follows:

1. The SCI transfers data from the transmit-FIFO (TDR register) to the TSR register when data is written to transmit-FIFO (TDR register) in the SCIn_TXI interrupt handling routine. The amount of data that can be written to transmit-FIFO (TDR register) is 16 - FTSR.T[5:0] bytes. In addition, when starting data transmission, set the CCR0.TIE bit and the CCR0.TE bit to 1 simultaneously by a single instruction. Then a SCIn_TXI interrupt request is generated.
2. After transferring data from transmit-FIFO (TDR register) to TSR, the SCI starts transmission. When the amount of transmit data written in transmit-FIFO (TDR register) is equal to or less than the specified transmit triggering number, the CSR.TDRE is set to 1. When the CCR0.TIE bit is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to transmit-FIFO (TDR register) in the SCIn_TXI interrupt handling routine before transmission of the current transmit data has finished. When SCIn_TEI interrupt requests are in use, set the CCR0.TIE bit to 0 and the CCR0.TEIE bit to 1 after the last of the data to be transmitted is written to the transmit-FIFO (TDR register) from the handling routine for SCIn_TXI requests.
3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified and in synchronization with the input clock when the use of an external clock is specified. Output of the clock signal is suspended until the input CTS signal is low when the CCR1.CTSE bit is 1 (CTS function enabled).
4. The SCI checks whether non-transmitted data remains in transmit-FIFO (TDR register)*1 on output of the stop bit.



[1]初始化SCI。
（将CCR0.TE和TIE设置为1。）

[2]使用SCIn_TXI将发送数据写入TDR：发送数据空中断（SCIn_TXI）是
当传输数据转发到
来自TDR的TSR。使用SCIn_TXI将传输数据写入TDR一次。

[3]串行传输继续程序：要继续串行传输，使用SCIn_TXI将传输数据写入TDR。发送数据也可以通过激活写入
DMAC or DTC.
如果您使用SCIn_TEI，请设置CCR0.TIE=0和CCR0.TEIE=1将最后发送数据写入TDR。

Note: 当使用外部时钟时（CCR3.CKE[1:0]的值为10b或11b），SCK引脚上最后一位的上升沿将CSR.TEND标志设置为1。将TE设置为0在此之后，可能会导致接收端接收数据保持时间不足。

Figure 26.63 选择非FIFO的时钟同步模式下的串行传输示例流程

(2)选择FIFO图26.64显示了在时钟同步模式下选择FIFO的串行传输示例。

在串行数据传输中，SCI操作如下：

1.当数据在SCIn_TXI中断处理程序中写入发送FIFO（TDR寄存器）时，SCI将数据从发送FIFO（TDR寄存器）传输到TSR寄存器。可写入发送FIFO（TDR寄存器）的数据量为16FTSR.T[5:0]字节。此外，在开始数据传输时，通过一条指令同时将CCR0.TIE位和CCR0.TE位设置为1。然后产生一个SCIn_TXI中断请求。

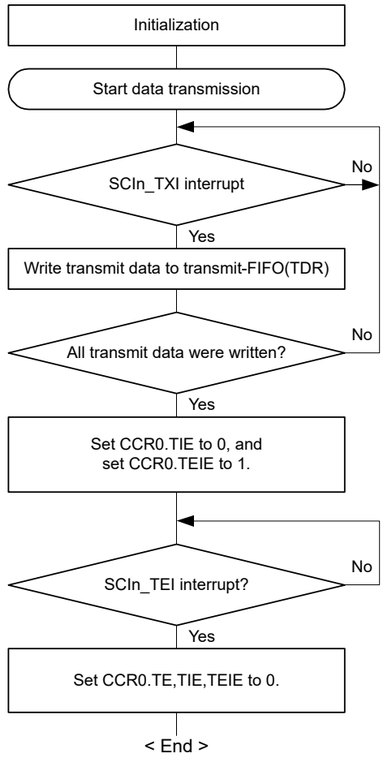
2.将数据从发送FIFO（TDR寄存器）传输到TSR后，SCI开始发送。当写入发送FIFO（TDR寄存器）的发送数据量等于或小于指定的发送触发数时，CSR.TDRE设置为1。当CCR0.TIE位设置为1时，SCIn_TXI中断生成请求。在当前发送数据的发送完成之前，通过在SCIn_TXI中断处理例程中将下一个发送数据写入发送FIFO（TDR寄存器）来启用连续发送。使用SCIn_TEI中断请求时，在SCIn_TXI的处理例程将要发送的最后一个数据写入发送FIFO（TDR寄存器）后，将CCR0.TIE位设置为0并将CCR0.TEIE位设置为1要求。

3.指定时钟输出模式时，与输出时钟同步，指定使用外部时钟时，与输入时钟同步，从TXDn引脚发送8位数据。当CCR1.CTSE位为1（CTS功能使能）时，时钟信号的输出被暂停，直到输入CTS信号为低电平。

4.SCI在停止位输出时检查未发送的数据是否保留在发送FIFO（TDR寄存器）*1中。

5. When data is remaining in the transmit-FIFO (TDR register), the next transmit data is transferred from transmit-FIFO (TDR register) to TSR and serial transmission of the next frame starts.
6. If no data is remaining in the transmit FIFO (TDR register), the CSR.TEND flag is set to 1. The TXDn pin retains the output state of the last bit. If the CCR0.TEIE bit is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Note 1. The number of unsent transmit data stored in the TDR register (transmit FIFO) can be monitored by reading the FTSR.T[5:0] bits.



[1] [1] Initialize SCI.
(Set CCR0.TE and TIE to 1.)

[2] Write transmit data to transmit-FIFO(TDR) by using SCIn_TXI: The transmit-data-empty-interrupt(SCIn_TXI) is generated when transmission-data forwards to TSR from the transmit-FIFO(TDR) and the number of transmit-data written in the transmit-FIFO is equal to or less than the transmit-FIFO threshold.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to the transmit-FIFO(TDR) by using a SCIn_TXI interrupt and clear CSR.TDRE flag to 0. Transmit data can also be written to the transmit- FIFO(TDR) by activating the DMAC or DTC. In this case, the TDRE flag is cleared automatically, so please don't operate the TDRE flag. If you use SCIn_TEI, set CCR0.TIE = 0 and CCR0.TEIE = 1 after writing the last-transmit-data to TDR.

Note: When the external clock is in use (the value of the CCR3.CKE[1:0] is 10b or 11b), the rising edge on the SCK pin for the last bit sets the CSR.TEND flag to 1. Setting CCR0.TE to 0 immediately after this, then it may lead to insufficient received data hold time on the receiver side.

Figure 26.64 Example flow of serial transmission in clock synchronous mode with FIFO selected

26.6.5 Serial Data Reception in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 26.65 and Figure 26.66 show examples of SCI operation for serial reception in clock synchronous mode.

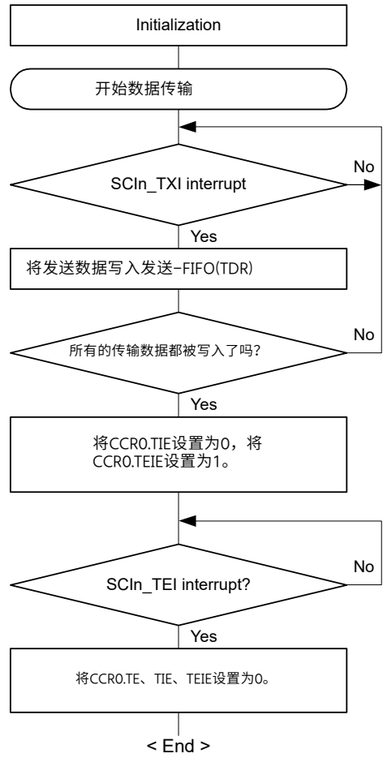
In serial data reception, the SCI operates as follows during serial data reception. Reception-only operation is possible only in slave mode. (In master mode, reception-only operation is prohibited.)

1. When the value of the CCR0.RE bit becomes 1, the CTSn_RTSn pin goes low (when the RTS function is used).
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in the RSR register.

5.当发送FIFO（TDR寄存器）中剩余数据时，下一个发送数据从发送FIFO（TDR寄存器）传送到TSR并开始下一帧的串行发送。

6.如果发送FIFO（TDR寄存器）中没有剩余数据，则CSR.TEND标志设置为1。TXDn引脚保持最后一位的输出状态。如果CCR0.TEIE位为1，则产生SCIn_TEI中断请求且SCKn引脚保持高电平。

注1.存储在TDR寄存器（发送FIFO）中的未发送发送数据的数量可以通过读取
FTSR.T[5:0] bits.



[1] [1]初始化SCI。（将CCR0.TE和TIE设置为1。）

[2]将发送数据写入发送-FIFO(TDR)
通过使用SCIn_TXI：当传输数据从传输FIFO(TDR)转发到TSR并且写入传输FIFO的传输数据数量等于或小于时，产生传输数据空中断(SCIn_TXI)发送FIFO阈值。

[3] 串行传输继续过程：
要继续串行传输，请使用SCIn_TXI中断将传输数据写入传输FIFO(TDR)，并将CSR.TDRE标志清除为0。也可以通过激活DMAC或DTC将传输数据写入传输FIFO(TDR)。在这种情况下，TDRE标志会自动清零，因此请不要操作TDRE标志。如果使用SCIn_TEI，则在将last-transmit-data写入TDR后设置CCR0.TIE=0和CCR0.TEIE=1。

Note: 当使用外部时钟时（CCR3.CKE[1:0]的值为10b或11b），SCK引脚上最后一位的上升沿将CSR.TEND标志设置为1。设置CCR0.TE之后立即为0，则可能导致接收端接收数据保持时间不足。

Figure 26.64 选择FIFO的时钟同步模式下的串行传输示例流程

26.6.5 时钟同步模式下的串行数据接收

(1) Non-FIFO selected

图26.65和图26.66显示了时钟同步模式下串行接收的SCI操作示例。

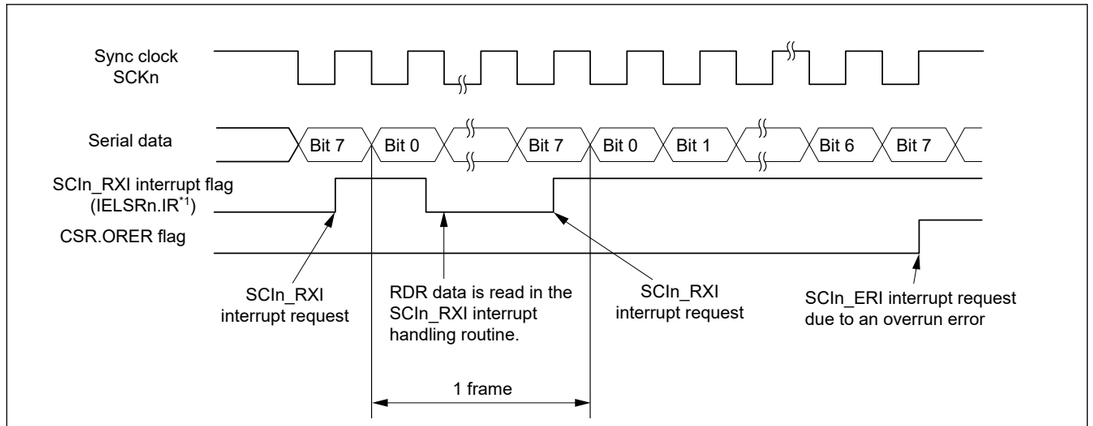
在串行数据接收中，SCI在串行数据接收过程中的操作如下。仅接收操作只能在从模式下进行。（在主模式下，禁止仅接收操作。）

1.当CCR0.RE位的值变为1时，CTSn_RTSn引脚变为低电平（使用RTS功能时）。

2.SCI执行内部初始化，并与同步时钟输入或输出同步开始接收数据，并将接收数据存储在RSR寄存器中。

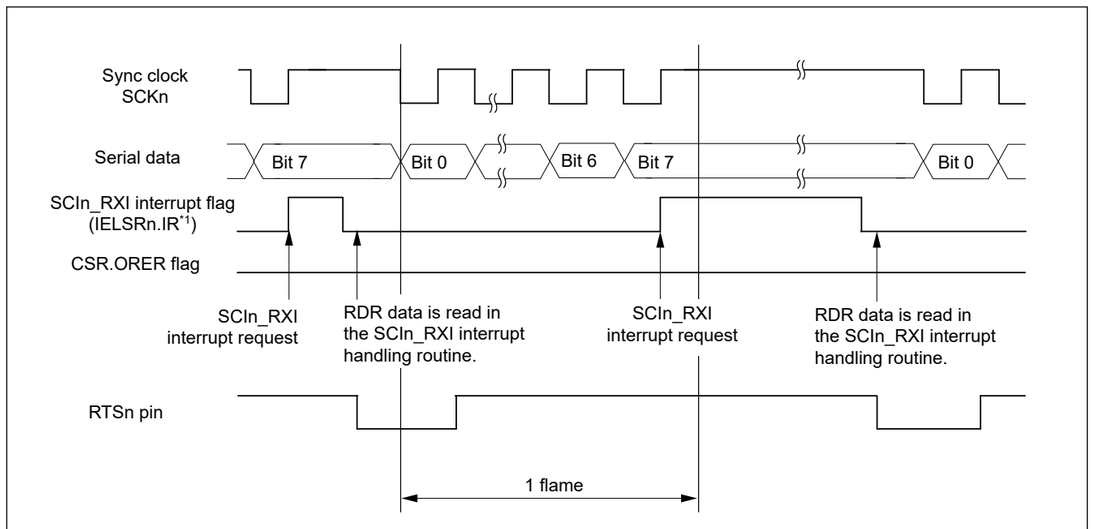
3. If an overrun error occurs, the CSR.ORER flag is set to 1. If the CCR0.RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the RDR register.
4. When reception completes successfully, receive data is transferred to the RDR register. If the CCR0.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the received data transferred to the RDR register in the SCIn_RXI interrupt handling routine before reception of the next receive data completes. Reading the received data that is transferred to RDR causes the CTSn_RTSn pin to output low (when the RTS function is used).

If you want to prevent the CTSn_RTSn pin output from turning low level after the final data is received, clear the CCR0.RE bit to 0 and then read the RDR register.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.65 Example operation for serial reception in clock synchronous mode (1) when the RTS function is not used



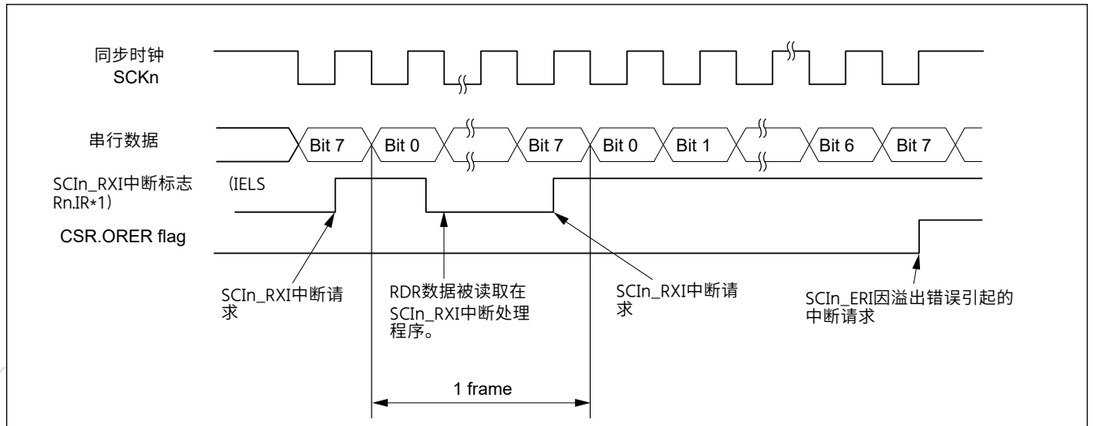
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.66 Example operation for serial reception in clock synchronous mode (2) when RTS function is used

3.如果发生溢出错误，则CSR.ORER标志设置为1。如果CCR0.RIE位为1，则产生SCIn_ERI中断请求。接收数据不传送到RDR寄存器。

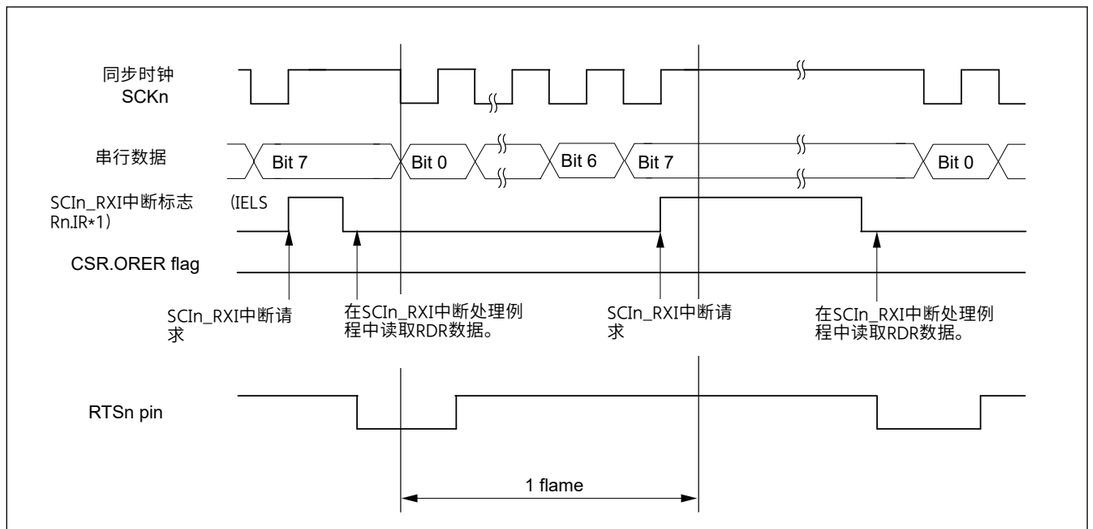
4.当接收成功完成时，接收数据被传送到RDR寄存器。如果CCR0.RIE位为1，则SCIn_RXI中断请求产生。连续接收是通过读取接收到的数据传输到在接收下一个接收数据完成之前，SCIn_RXI中断处理程序中的RDR寄存器。读取传输到RDR的接收数据会导致CTSn_RTSn引脚输出低电平（使用RTS功能时）。

如果要防止CTSn_RTSn引脚输出在收到最终数据后变为低电平，请将CCR0.RE位清零，然后读取RDR寄存器。



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.65 不使用RTS功能时时钟同步模式下串行接收的示例操作(1)

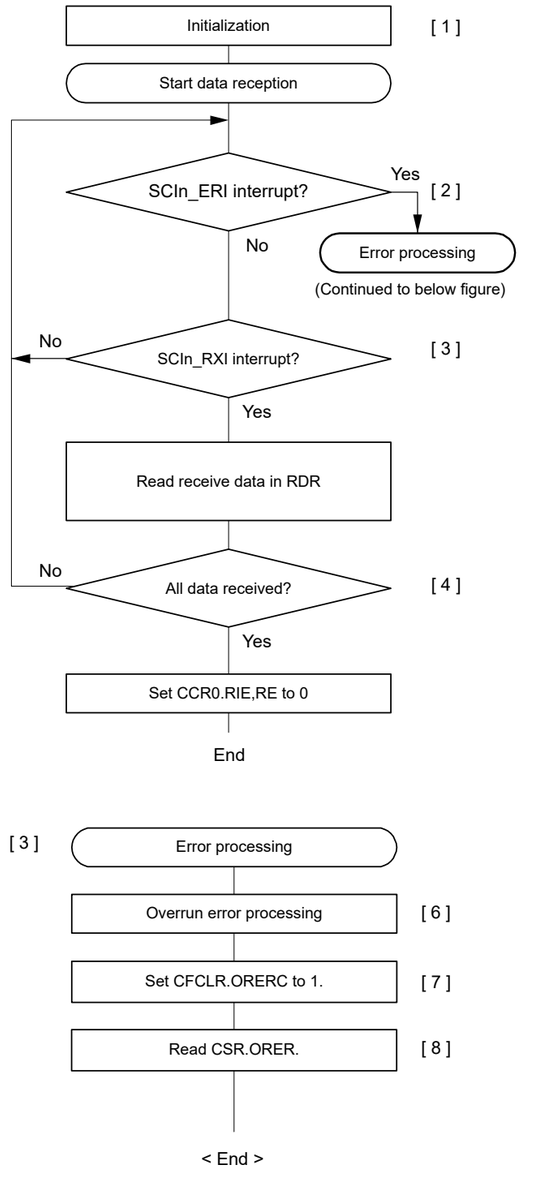


注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.66 使用RTS功能时时钟同步模式下串行接收的示例操作(2)

Data transfer cannot resume while the receive error flag is 1. Therefore, clear the ORER, FER, and PER flags in the CSR register to 0 before resuming data reception. Additionally, always read the RDR register during overrun error processing. When a data reception is forced to terminate by a 0 write to the CCR0.RE bit during operation, read the RDR register because received data that is not yet read might be left in the RDR register.

Figure 26.67 shows an example flow of serial data reception.



[1] Initialize SCI.
(Set CCR0.RE, RIE to 1.)

[2] Receive error processing:
If a receive error occurs, after performing the appropriate error processing, be sure to CSR.ORER is 0. Reception cannot be resumed if ORER is 1.

[3] Read the receive data in RDR once in the SCIn_RXI interrupt handling routine.

[4] Serial reception continuation procedure:
To continue serial reception, before the MSB bit (bit7) of the current frame is received, read data from RDR in the SCIn_RXI interrupt handling routine. The RDR data can also be read by activating the DMAC or DTC.

[6]Overrun error processing:
Read RDR.

[7] Clear the error flag:
Set the flag clear bit corresponding to the reception error to 1. Done this step and step [6], the next frame can be received normally.

[8] Confirming that the error flag is cleared:
Confirm all error flags are cleared.

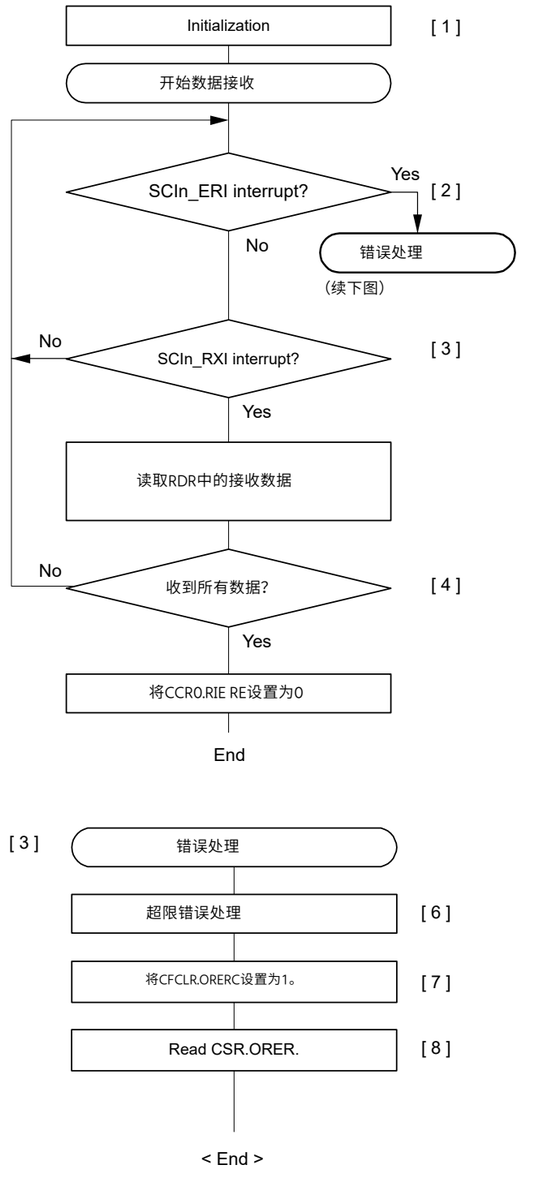
Figure 26.67 Example flow of serial reception in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 26.68 shows an example of serial reception in clock synchronous mode with FIFO selected.

接收错误标志为1时无法恢复数据传输。因此，在恢复数据接收之前，将CSR寄存器中的ORER、FER和PER标志清零。此外，在溢出错误处理期间始终读取RDR寄存器。如果在操作期间通过对CCR0.RE位写入0来强制终止数据接收，请读取RDR寄存器，因为尚未读取的已接收数据可能会留在RDR寄存器中。

图26.67显示了串行数据接收的示例流程。



[1]初始化SCI。
（将CCR0.RE、RIE设置为1。）

[2]接收错误处理：
如果发生接收错误，请在执行适当的错误处理后，确保CSR.ORER为0。如果出现以下情况，则无法恢复接收

ORER为1。[3]在SCIn_RXI中断处理程序中读取一次RDR中的接收数据。

[4]串行接收继续程序：要继续串行接收，在接收到当前帧的MSB位（bit7）之前，在SCIn_RXI中断处理程序中从RDR读取数据。RDR数据也可以通过激活DMAC或DTC来读取。

[6]溢出错误处理：读取RDR。

[7]清除错误标志：
将接收错误对应的标志清除位设置为1。完成此步骤和步骤[6]，可以正常接收下一帧。

[8]确认清除错误标志：确认清除所有错误标志。

Figure 26.67 选择非FIFO的时钟同步模式下的串行接收示例流程

(2)选择FIFO图26.68显示了在时钟同步模式下选择FIFO的串行接收示例。

In serial data reception, the SCI operates as follows during serial data reception. Reception-only operation is possible only in slave mode. (In master mode, reception-only operation is prohibited.)

1. When the value of the CCR0.RE bit becomes 1, the CTSn_RTSn pin goes low (when the RTS function is used).
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and transfers the received data to the receive-FIFO (RDR register).
3. If an overrun error occurs, the CSR.ORER flag is set to 1. If the CCR0.RIE bit is 1, an SCIn_ERI interrupt request is generated. Received data is not transferred to the receive-FIFO (RDR register)*1.
4. When data reception completes successfully, the receive data is transferred to the receive-FIFO (RDR register)*1. The FRSR.RDRF flag is set to 1 when the amount of the receive data stored in receive-FIFO (RDR register) is equal to or greater than the specified receive triggering number. If the CCR0.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous data reception is enabled by reading the receive data transferred to receive-FIFO (RDR register)*1 in the SCIn_RXI interrupt handling routine before an overrun error occurs. If the amount of received data that is transferred to receive-FIFO (RDR register) is less than the specified receive triggering number, the CTSn_RTSn pin goes low (when the RTS function is used).

Note 1. In clock synchronous mode, RDR.RDAT[8] is not used.

在串行数据接收中，SCI在串行数据接收过程中的操作如下。仅接收操作只能在从模式下进行。（在主模式下，禁止仅接收操作。）

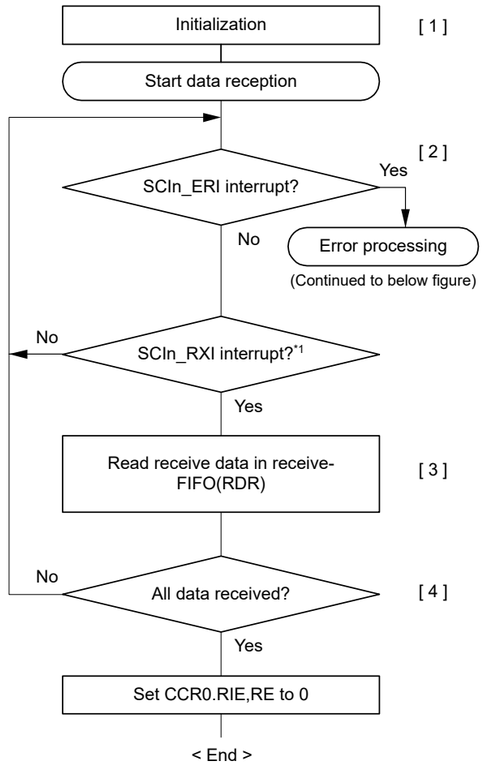
1.当CCR0.RE位的值变为1时，CTSn_RTSn引脚变为低电平（使用RTS功能时）。

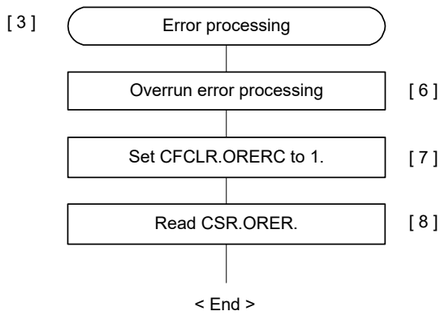
2.SCI执行内部初始化并与同步时钟输入或输出同步开始接收数据，并将接收到的数据传输到接收FIFO（RDR寄存器）。

3.如果发生溢出错误，则CSR.ORER标志设置为1。如果CCR0.RIE位为1，则产生SCIn_ERI中断请求。接收到的数据不传送到接收FIFO（RDR寄存器）*1。

4.当数据接收成功完成时，接收数据被传送到接收FIFO（RDR寄存器）*1。当存储在接收FIFO（RDR寄存器）中的接收数据量等于或大于指定的接收触发数时，FRSR.RDRF标志设置为1。如果CCR0.RIE位为1，则产生SCIn_RXI中断请求。在发生溢出错误之前，通过在SCIn_RXI中断处理例程中读取传输到接收FIFO（RDR寄存器）*1的接收数据来启用连续数据接收。如果传输到接收FIFO（RDR寄存器）的接收数据量小于指定的接收触发数，CTSn_RTSn引脚变为低电平（使用RTS功能时）。

注1.在时钟同步模式下，不使用RDR.RDAT[8]。





[1] Initialize SCI.
(Set CCR0.RE, RIE to 1.)

[2] Receive error processing:
If a receive error occurs, after performing the appropriate error processing, be sure to CSR.ORER is 0. Reception cannot be resumed if ORER is 1.

[3] Read the receive data in the receive-FIFO(RDR) in the SCIn_RXI interrupt handling routine. The reception data stored in the receive-FIFO(RDR) is read until the number of stored data will be below the FCR.RTRG value at least. You can confirm the number of the reception data in the FIFO by FRSR.R[5:0].

[4] Serial reception continuation procedure:
To continue serial reception, before the overrun error occurs, read data from RDR. The RDR data can also be read by activating the DMAC or DTC.

Note1:
Set all received data to an integer multiple of the receive FIFO threshold. If it is not an integral multiple, return to step [2] and it will become an infinite loop, so set a timeout time separately using a timer etc.

[6]Overrun error processing:
Read RDR.

[7] Clear the error flag:
Set the flag clear bit corresponding to the reception error to 1. Done this step and step [6], the next frame can be received normally.

[8] Confirming that the error flag is cleared:
Confirm all error flags are cleared.

Figure 26.68 Example flow of serial reception in clock synchronous mode with FIFO selected

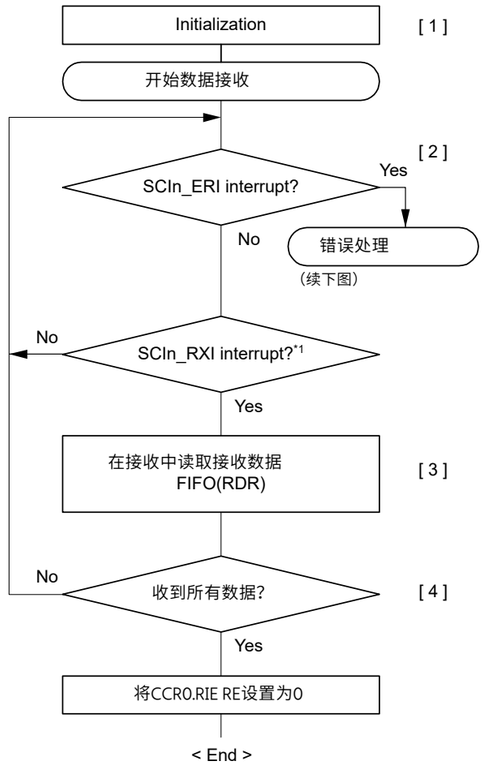
26.6.6 Simultaneous Serial Data Transmission and Reception in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 26.69 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode. After initializing the SCI, use the following procedure for simultaneous serial data transmit and receive operations.

To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data transmission by verifying that the CSR.TEND flag is set to 1.



[1]初始化SCI。
（将CCR0.RE、RIE设置为1。）

[2]接收错误处理：
如果发生接收错误，请在进行适当的错误处理后，确保CSR.ORER为0。如果ORER为1，则无法恢复接收。

[3]在SCIn_RXI中断处理程序中读取接收FIFO(RDR)中的接收数据。读取存储在接收FIFO(RDR)中的接收数据，直到存储的数据数量至少低于FCR.RTRG值。您可以通过FRSR.R[5:0]确认FIFO中接收数据的数量。

[4]串行接收继续过程：要继续串行接收，在溢出错误发生之前，从RDR读取数据。RDR数据也可以通过激活DMAC或DTC来读取。

Note1:
将所有接收到的数据设置为接收FIFO阈值的整数倍。如果不是整数倍，返回步骤[2]会变成死循环，所以用定时器等单独设置超时时间。

[6]溢出错误处理：读取RDR。

[7]清除错误标志：
将接收错误对应的标志清除位设置为1。完成此步骤和步骤[6]，可以正常接收下一帧。

[8]确认清除错误标志：确认清除所有错误标志。

Figure 26.68 选择FIFO的时钟同步模式下的串行接收示例流程

26.6.6 时钟同步的同时串行数据发送和接收 Mode

(1) Non-FIFO selected

图26.69显示了时钟同步模式下同时串行发送和接收操作的示例流程。
初始化SCI后，使用以下程序同时进行串行数据发送和接收操作。

从发送模式切换到同时发送和接收模式：

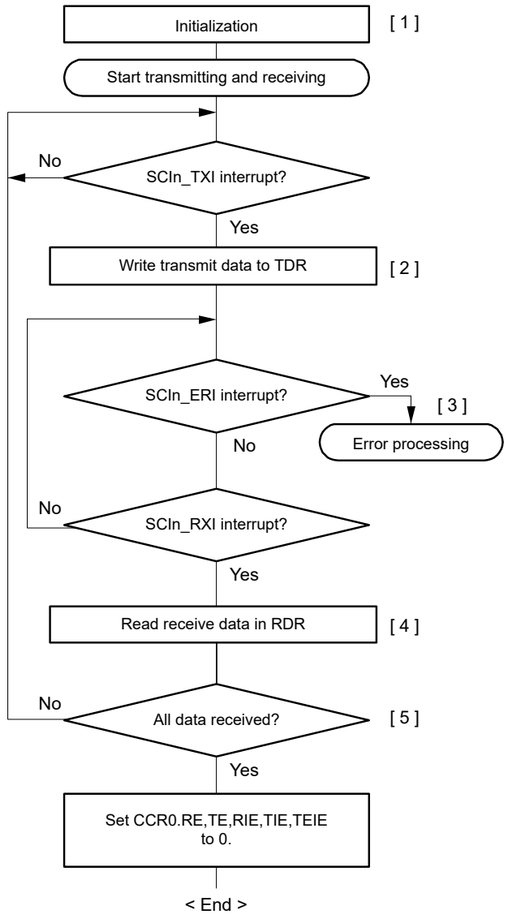
1.通过验证CSR.TEND标志是否设置为1来检查SCI是否完成数据传输。

2. Initialize the CCR0 register, and then set the TIE, RIE, TE, and RE bits in the CCR0 register to 1 simultaneously by a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data reception.
2. Set the CCR0.TE and RE bits to 0, and then check that the receive error flag (ORER, FER, and PER) in the CSR register is 0.
3. Set the TIE, RIE, TE, and RE bits in the CCR0 register to 1 simultaneously by a single instruction.

When the RTS function is used in the concurrent transmission/reception operation, if you want to prevent the CTSn_RTSn pin output from turning to low after the final data is received as in the reception operation, clear the RE and TE bits in CCR0 to 0 simultaneously, and then read the RDR register.



[1] Initialize SCI:
Make the TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to TDR in the SCIn_TXI Interrupt request handling routine.

[3] Receive error processing:
If a receive error occurs, after performing the appropriate error processing, be sure to CSR.ORER is 0. Reception cannot be resumed if ORER is 1.

[4] Reading receive data:
The reception data stored in RDR once in the SCIn_RXI interrupt
request handling routine.

[5] Serial transmission/reception continuation procedure
To continue serial reception, before the MSB bit (bit7) of the current frame is received, read data from RDR in the SCIn_RXI interrupt handling routine. And before the MSB(bit7) of the current frame is transmitted, write transmit data to TDR in the SCIn_TXI interrupt handling. Transmit data can also be written by activating the DMAC or DTC. And the RDR data can also be read by activating the DMAC or DTC.

Figure 26.69 Example flow of simultaneous serial transmission and reception in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 26.70 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode with FIFO selected.

2.初始化CCR0寄存器，然后通过一条指令同时将CCR0寄存器中的TIE、RIE、TE和RE位设置为1。

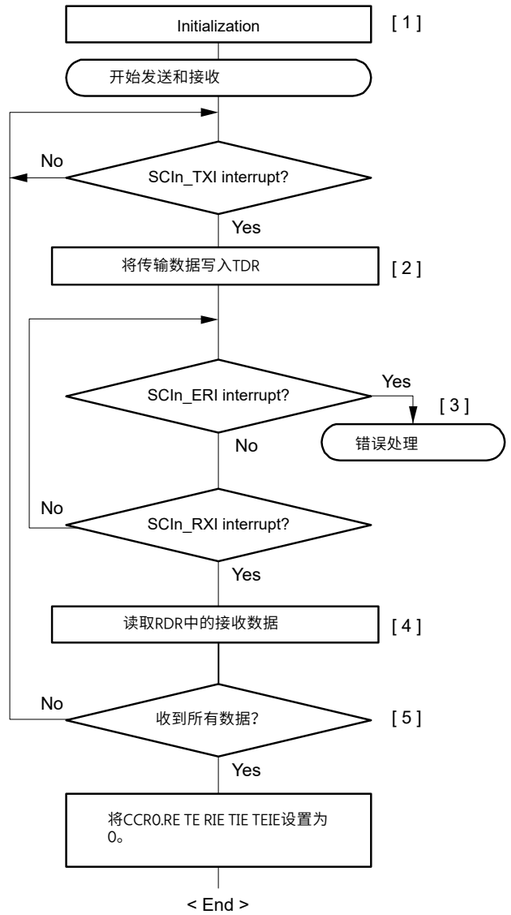
从接收模式切换到同时发送和接收模式：

1.检查SCI是否完成数据接收。

2.将CCR0.TE和RE位设置为0，然后检查CSR寄存器中的接收错误标志（ORER、FER和PER）是否为0。

3.通过一条指令同时将CCR0寄存器中的TIE、RIE、TE和RE位设置为1。

在并发发送接收操作中使用RTS功能时，如果要防止CTSn_RTSn引脚输出在接收操作中一样在接收到最终数据后变为低电平，同时将CCR0中的RE和TE位清零，然后读取RDR寄存器。



[1] Initialize SCI:
使TXDn管脚可以作为发送数据的输出管脚，同时RXDn管脚可以作为接收数据的输入管脚。

[2]发送数据写入：将发送数据写入SCIn_TXI中的TDR
中断请求处理例程。

[3]接收错误处理：
如果发生接收错误，请在执行适当的错误处理后，确保CSR.ORER为0。如果出现以下情况，则无法恢复接收
ORER is 1.

[4]读取接收数据：将接收数据存储在RDR中一次
SCIn_RXI中断请求处理程序
。

[5]串行发送接收继续过程要继续串行接收，在接收到当前帧的MSB位（bit7）之前，在SCIn_RXI中断处理程序中从RDR读取数据。并且在发送当前帧的MSB(bit7)之前，在SCIn_TXI中断处理中将发送数据写入TDR。也可以通过激活DMAC或DTC来写入传输数据。也可以通过激活DMAC或DTC来读取RDR数据。

Figure 26.69 选择非FIFO的时钟同步模式下同时串行发送和接收的示例流程

(2) FIFO selected

图26.70显示了在时钟同步模式下同时串行发送和接收操作的示例流程，其中
FIFO selected.

After initializing the SCI, use the following procedure for simultaneous serial data transmit and receive operations.

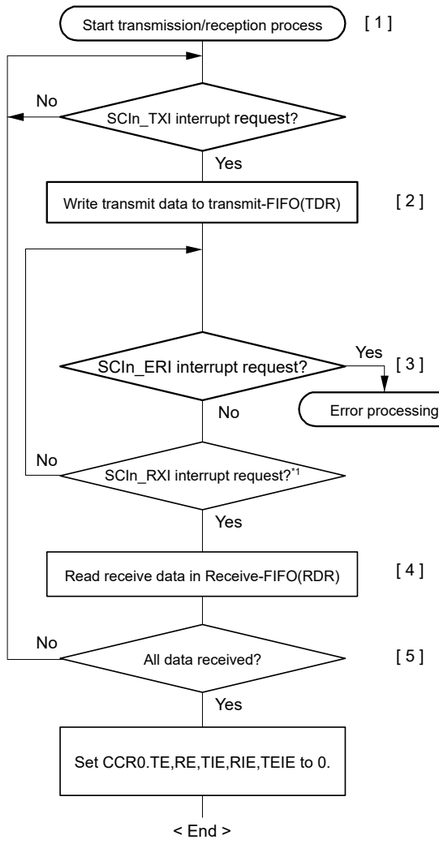
To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the transmission by verifying that the CSR.TEND flag is set to 1.
2. Initialize the CCR0 register, then set the TIE, RIE, TE, and RE bits in the CCR0 register to 1 simultaneously by a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the reception.
2. Set the CCR0.TE and RE bits to 0.
3. Check that the receive error flags (ORER, FER, and PER) in the CSR register are 0, and then set the TIE, RIE, TE, and RE bits in the CCR0 register to 1 simultaneously by a single instruction.

Since clock synchronous communication performs transmission and reception at the same time, make sure that the number of data to be transmitted and received is the same.



[1] Start transmission / reception process

[2] Transmit data write:
Write transmit data to Transmit-FIFO(TDR) in the SCIn_TXI Interrupt request handling routine.
Match the number of transmitted data with the FCR.RTRG.

[3] Receive error processing:
If a receive error occurs, after performing the appropriate error processing (Initialization such as stopping communication, reading all received data, clearing CSR.RDRF, etc.), be sure to ORER is 0. Reception cannot be resumed if ORER is 1.

[4] Read receive data:
Read the received data stored in receive-FIFO(RDR) for the number of the FCR.RTRG in the SCIn_RXI interrupt handling routine.

[5] Serial transmission/reception continuation procedure
To continue serial reception, before the overrun error occurs, read data from RDR and clear CSR.RDRF.
To continue serial transmission, write transmit data to the transmit-FIFO(TDR) by using a SCIn_TXI interrupt and clear TDRE flag to 0.
Transmit data can also be written to the transmit- FIFO(TDR) by activating the DMAC or DTC. And The RDR data can also be read by activating the DMAC or DTC. In this case, the TDRE and RDRF are cleared automatically, so please don't operate the TDRE And RDRF.

Note 1. Set all received data to an integer multiple of the receive FIFO threshold. If it is not an integral multiple, return to step [2] and it will become an infinite loop, so set a timeout time separately using a timer etc.

Figure 26.70 Example flow of simultaneous serial transmission and reception in clock synchronous mode with FIFO selected

初始化SCI后，使用以下程序同时进行串行数据发送和接收操作。

从发送模式切换到同时发送和接收模式：

1.通过验证CSR.TEND标志设置为1来检查SCI是否完成传输。

2.初始化CCR0寄存器，然后通过一条指令同时将CCR0寄存器中的TIE、RIE、TE和RE位设置为1。

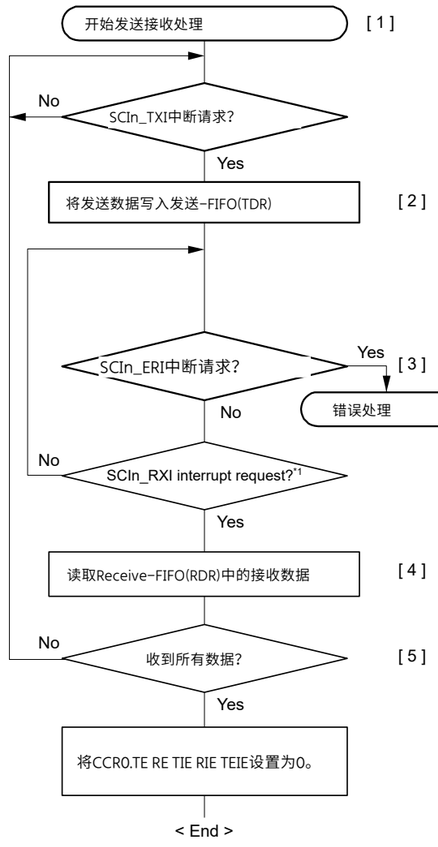
从接收模式切换到同时发送和接收模式：

1.检查SCI是否完成接收。

2.将CCR0.TE和RE位设置为0。

3.检查CSR寄存器中的接收错误标志（ORER、FER和PER）是否为0，然后通过一条指令同时将CCR0寄存器中的TIE、RIE、TE和RE位设置为1。

由于时钟同步通信同时进行发送和接收，请确保要发送和接收的数据数量相同。



[1]开始发送接收处理

[2]发送数据写入：将发送数据写入SCIn_TXI中的Transmit-FIFO(TDR)
中断请求处理例程。
将传输数据的数量与FCR.RTRG匹配。

[3]接收错误处理：
如果发生接收错误，在进行适当的错误处理（如停止通信、读取所有接收数据、清除CSR.RDRF等初始化）后，请确保ORER为0。如果ORER为1，则无法恢复接收。

[4]读取接收数据：在SCIn_RXI中断处理例程中读取存储在接收FIFO(RDR)中的FCR.RTRG编号的接收数据。

[5]串行发送接收继续程序
要继续串行接收，在溢出错误发生之前，从RDR读取数据并清除CSR.RDRF。要继续串行传输，请使用SCIn_TXI中断将传输数据写入传输FIFO(TDR)，并将TDRE标志清零。

发送数据也可以通过激活DMAC或DTC写入发送FIFO(TDR)。并且RDR数据也可以通过激活DMAC或DTC来读取。在这种情况下，TDRE和RDRF会自动清零，所以请不要操作TDRE和RDRF。

注1.将所有接收数据设置为接收FIFO阈值的整数倍。如果不是整数倍，返回步骤[2]会变成死循环，所以用定时器等单独设置超时时间。

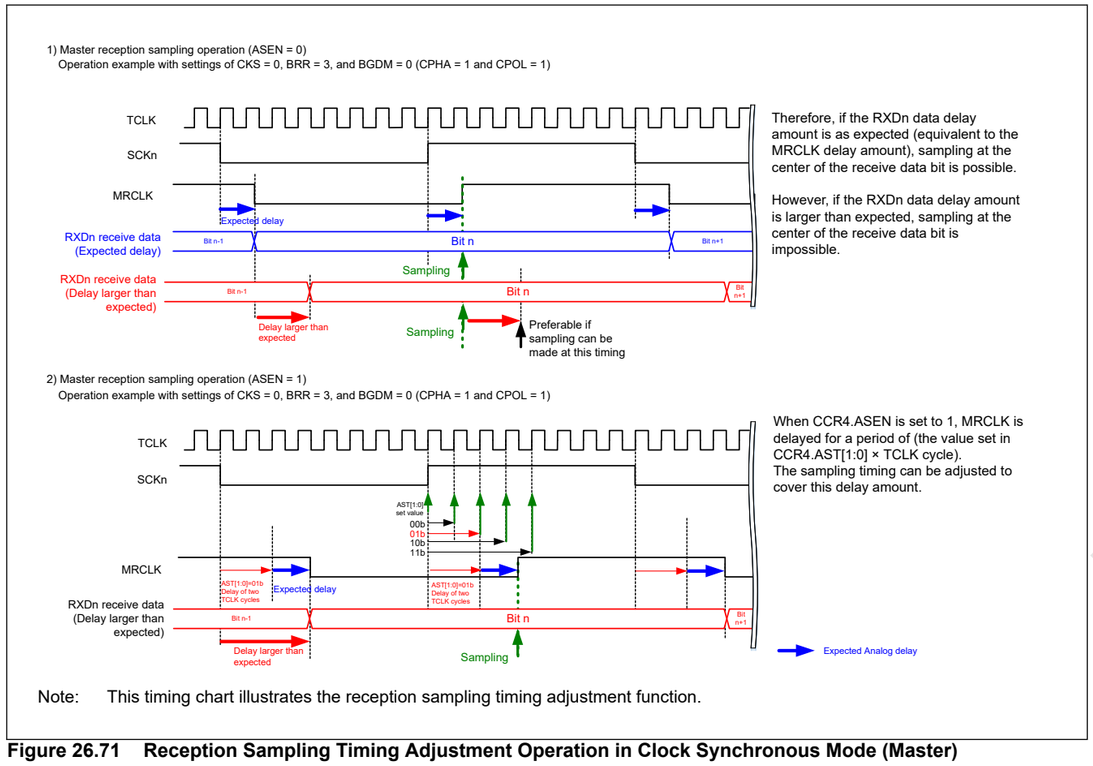
Figure 26.70 选择FIFO的时钟同步模式下同时串行发送和接收的示例流程

26.6.7 Reception Sampling Timing Adjustment Function in Clock Synchronous Mode with internal clock used

When the clock synchronous internal clock is used (master mode), MRCLK is used as a reception sampling clock.

This function adjusts the reception sampling timing by delaying MRCLK by 1 to 4 TCLK and adding a digital delay. MRCLK's analog delay cannot be adjusted by this function.

Setting the CCR4.ASEN bit to 1 enables this function. The delay value is set in CCR4.AST[1:0].



Note: This timing chart illustrates the reception sampling timing adjustment function.

Figure 26.71 Reception Sampling Timing Adjustment Operation in Clock Synchronous Mode (Master)

26.7 Operation in Smart Card Interface Mode

The SCI supports smart card (IC card) interfaces conforming to ISO/IEC 7816-3 (standard for Identification Cards), as an extended function of the SCI.

Smart card interface mode can be selected using the appropriate register.

26.7.1 Example Connection

Figure 26.72 shows an example connection between a smart card (IC card) and the MCU. As shown in Figure 26.72, because the MCU communicates with an IC card using a single transmission line, interconnect the TXDn and RXDn pins and pull up the data transmission line to VCC using a resistor.

Setting the CCR0.TE and CCR0.RE bits to 1 with an IC card disconnected enables closed-loop transmission or reception, allowing self-diagnosis. To supply an IC card with the clock pulses generated by the SCI, input the SCKn pin output to the CLK pin of an IC card.

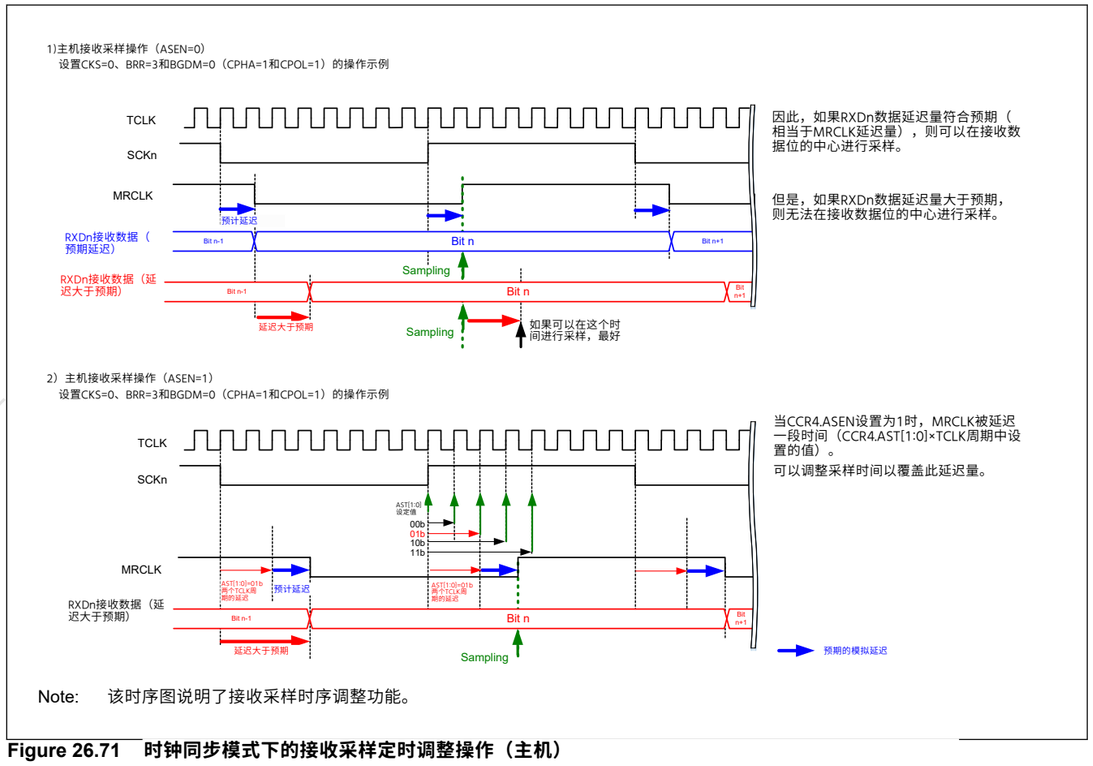
An output port of the MCU can be used to output a reset signal.

26.6.7 使用内部时钟的时钟同步模式下的接收采样定时调整功能

当使用时钟同步内部时钟（主机模式）时，MRCLK用作接收采样时钟。

该函数通过将MRCLK延迟1到4个TCLK并添加数字延迟来调整接收采样时序。
此功能无法调整MRCLK的模拟延迟。

将CCR4.ASEN位设置为1可启用此功能。延迟值在CCR4.AST[1:0]中设置。



Note: 该时序图说明了接收采样时序调整功能。

Figure 26.71 时钟同步模式下的接收采样定时调整操作（主机）

26.7 智能卡接口模式下的操作

SCI支持符合ISOIEC7816-3（识别卡标准）的智能卡（IC卡）接口，作为SCI的扩展功能。

可以使用适当的寄存器选择智能卡接口模式。

26.7.1 示例连接

图26.72显示了智能卡（IC卡）和MCU之间的示例连接。如图26.72所示，由于MCU使用单条传输线与IC卡通信，因此将TXDn和RXDn引脚互连，并使用电阻将数据传输线上拉到VCC。

在断开IC卡的情况下将CCR0.TE和CCR0.RE位设置为1可启用闭环发送或接收，从而实现自诊断。要将SCI产生的时钟脉冲提供给IC卡，请将SCKn引脚输出输入到IC卡的CLK引脚。

MCU的输出端口可用于输出复位信号。

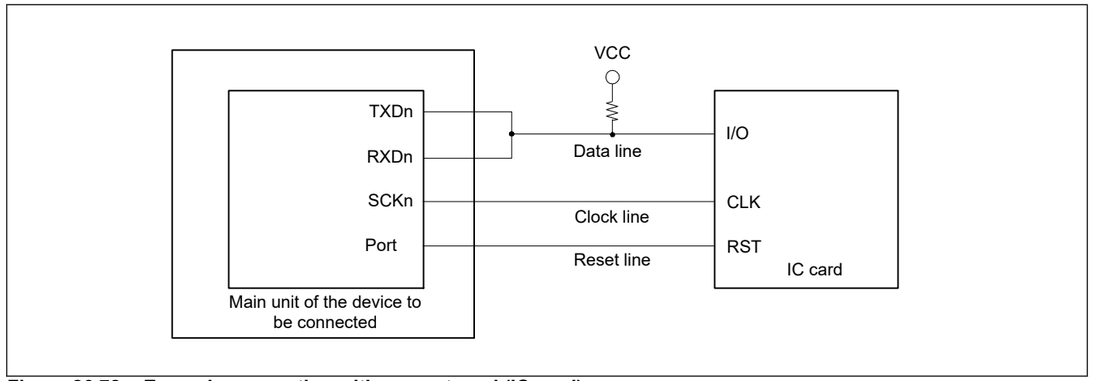


Figure 26.72 Example connection with a smart card (IC card)

26.7.2 Data Format (Except in Block Transfer Mode)

Figure 26.73 shows the data transfer formats in smart card interface mode:

- One frame consists of 8-bit data and a parity bit in asynchronous mode.
- During transmission, at least 2 ETUs (elementary time unit – the time required for transferring 1 bit) is set as a guard time from the end of the parity bit until the start of the next frame.
- If a parity error is detected during reception, a low error signal is output for 1 ETU after 10.5 ETUs elapse from the start bit.
- If an error signal is sampled during transmission, the same data is automatically retransmitted after at least 2 ETUs.

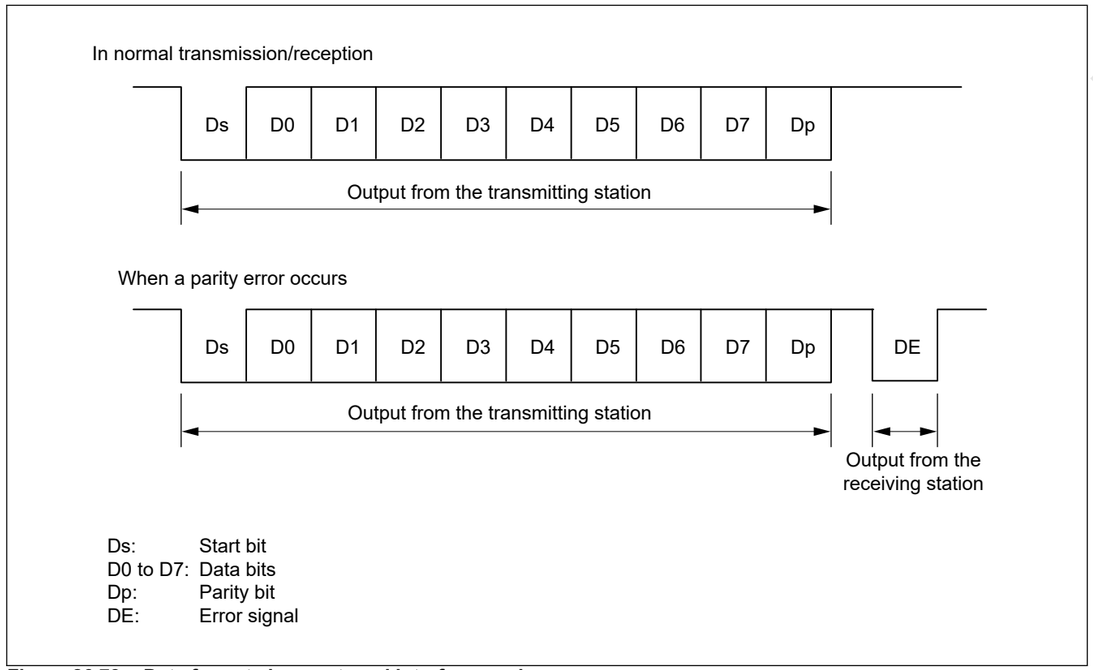


Figure 26.73 Data formats in smart card interface mode

For communications with IC cards of the direct convention type and inverse convention type, follow the procedures in this section.

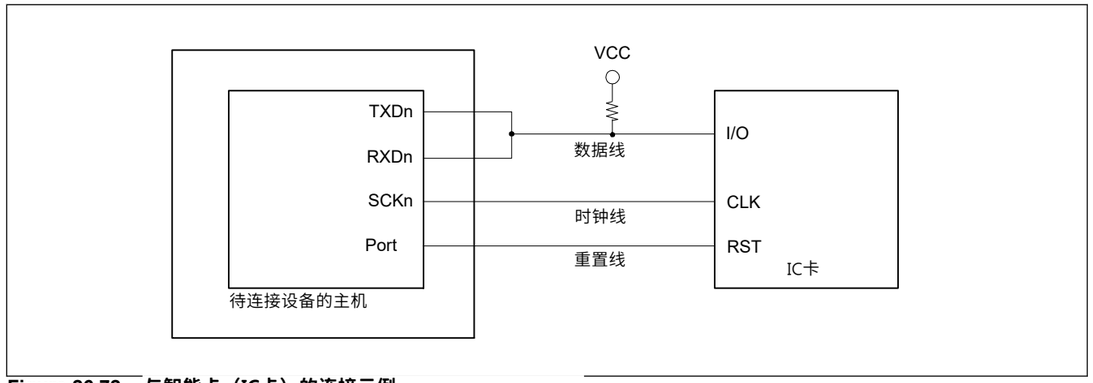


Figure 26.72 与智能卡（IC卡）的连接示例

26.7.2 数据格式（块传输模式除外）

图26.73显示了智能卡接口模式下的数据传输格式：

●一帧由8位数据和一个异步模式的奇偶校验位组成。

●在传输过程中，至少设置2个ETU（基本时间单位——传输1位所需的时间）作为从奇偶校验位结束到下一帧开始的保护时间。

●如果在接收过程中检测到奇偶校验错误，则在从起始位经过10.5ETU后输出1ETU的低错误信号。

●如果在传输过程中对错误信号进行采样，相同的数据会在至少2个ETU后自动重传。

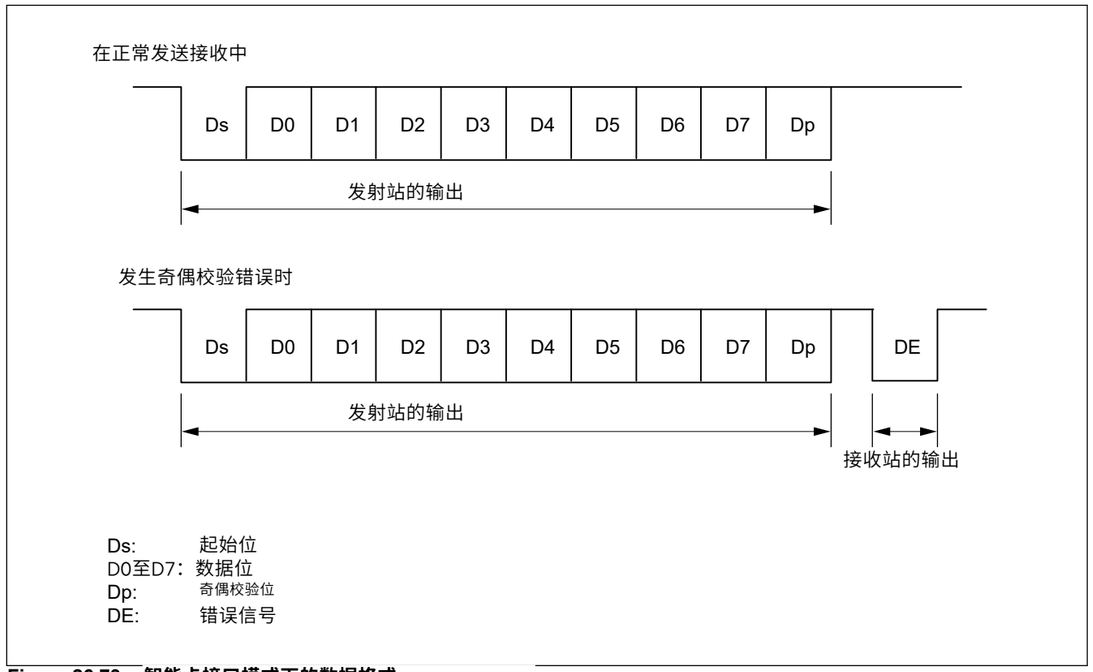


Figure 26.73 智能卡接口模式下的数据格式

与直接约定型和逆约定型IC卡进行通信时，请按照本节的步骤进行。

(1) Direct Convention Type

For the direct convention type, logic levels 1 and 0 indicate the Z and A states, respectively, and data is transferred with LSB-first for the start character, as shown in Figure 26.74. Therefore, data in the start character in the figure is 0x3B.

When using the direct convention type, write 1 to the CCR3.LSBF and write 0 to the CCR3.SINV. Write 0 to the CCR1.PM bit to use even parity, which is prescribed by the smart card standard.

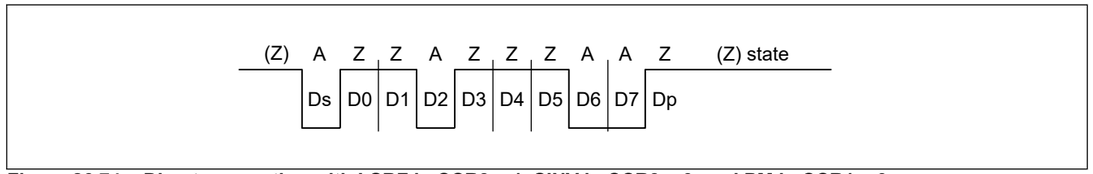


Figure 26.74 Direct convention with LSBF in CCR3 = 1, SINV in CCR3 = 0, and PM in CCR1 = 0

(2) Inverse Convention Type

For the inverse convention type, logic levels 1 and 0 indicate the A and Z states, respectively, and data is transferred with MSB-first for the start character, as shown in Figure 26.75. Therefore, data in the start character in the figure is 0x3F.

When using the inverse convention type, write 0 to the CCR3.LSBF and write 1 to the CCR3.SINV. The parity bit is logic level 0 to produce even parity, which is prescribed by the smart card standard, and corresponds to the Z state. Because the SINV bit of the MCU only inverts data bits D7 to D0, write 1 to the PM bit in CCR1 to invert the parity bit for both transmission and reception.

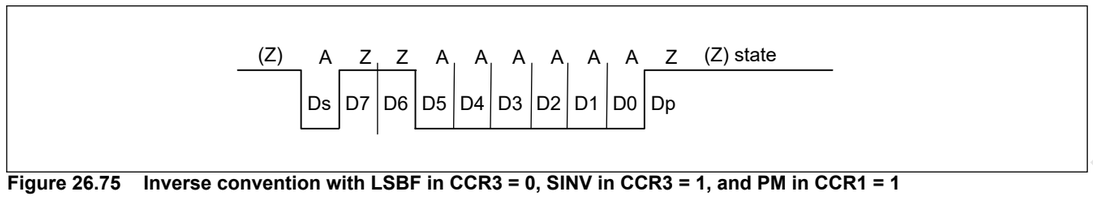


Figure 26.75 Inverse convention with LSBF in CCR3 = 0, SINV in CCR3 = 1, and PM in CCR1 = 1

26.7.3 Block Transfer Mode

Block transfer mode differs from normal smart card interface mode as follows:

- Even if a parity error is detected during reception, no error signal is output. Because the PER flag in CSR is set by error detection, clear the PER flag before receiving the parity bit of the next frame.
- During transmission, at least 1 ETU is set as a guard time from the end of the parity bit until the start of the next frame
- Because the same data is not retransmitted, the TEND flag in CSR is set to 11.5 ETUs after transmission starts
- In block transfer mode, the ERS flag in CSR indicates the error signal status as in normal smart card interface mode, but the flag is read as 0 because no error signal is transferred

26.7.4 Receive Data Sampling Timing and Reception Margin

Only the internal clock generated by the on-chip baud rate generator can be used as a transfer clock in smart card interface mode.

In this mode, the SCI can operate on a base clock with a frequency of 32, 64, 372, 256, 93, 128, 186, or 512 times the bit rate set up in the CCR2.BCP[2:0] bits. The frequency is always 16 times the bit rate in normal asynchronous mode.

For data reception, the falling edge of the start bit is sampled with the base clock to perform internal synchronization.

Receive data is sampled on the 16th, 32nd, 186th, 128th, 46th, 64th, 93rd, and 256th rising edges of the base clock so that it can be latched at the middle of each bit as shown in Figure 26.76. The reception margin is determined by the following formula:

(1) 直接约定型

对于直接约定类型，逻辑电平1和0分别表示Z和A状态，数据通过
LSB-first为起始字符，如图26.74所示。因此，图中起始字符中的数据为0x3B。

使用直接约定类型时，向CCR3.LSBF写入1，向CCR3.SINV写入0。将0写入CCR1.PM位以使用智能卡标准规定的偶校验。

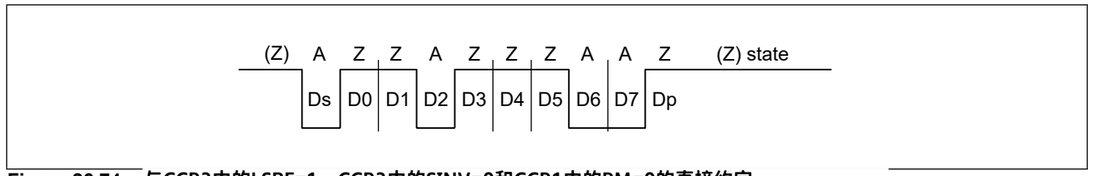


Figure 26.74 与CCR3中的LSBF=1、CCR3中的SINV=0和CCR1中的PM=0的直接约定

(2) 逆约定型

对于逆约定类型，逻辑电平1和0分别表示A和Z状态，数据通过
MSB-first为起始字符，如图26.75所示。因此，图中起始字符中的数据为0x3F。

使用逆约定类型时，向CCR3.LSBF写入0，向CCR3.SINV写入1。奇偶校验位为逻辑电平0，产生偶校验，这是智能卡标准规定的，对应于Z状态。由于MCU的SINV位仅将数据位D7反转为D0，因此向CCR1中的PM位写入1以反转发送和接收的奇偶校验位。

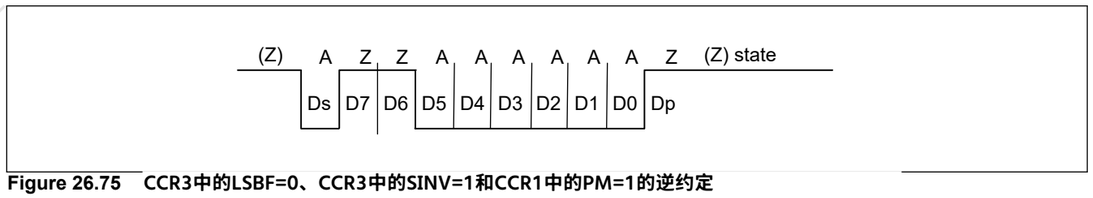


Figure 26.75 CCR3中的LSBF=0、CCR3中的SINV=1和CCR1中的PM=1的逆约定

26.7.3 块传输模式

块传输模式与普通智能卡接口模式的区别如下：

●即使在接收过程中检测到奇偶校验错误，也不会输出错误信号。因为CSR中的PER标志由错误检测设置，所以在接收下一帧的奇偶校验位之前清除PER标志。

●在传输过程中，从奇偶校验位结束到下一帧开始至少设置1个ETU作为保护时间

●由于不重传相同的数据，因此在传输开始后，CSR中的TEND标志设置为11.5ETU

●在块传输模式下，CSR中的ERS 标志指示错误信号状态，与普通智能卡接口模式一样，但该标志被读取为0，因为没有传输错误信号

26.7.4 接收数据采样时序和接收裕量

只有片内波特率发生器产生的内部时钟可以用作智能卡接口模式下的传输时钟。

在这种模式下，SCI可以在频率为CCR2.BCP[2:0]位中设置的比特率的32、64、372、256、93、128、186或512倍的基本时钟上运行。在正常异步模式下，频率始终是比特率的16倍。

对于数据接收，起始位的下降沿用基准时钟进行采样，以进行内部同步。

接收数据在基本时钟的第16、32、186、128、46、64、93和256个上升沿采样，以便在每个位的中间锁存，如图26.76所示。接收余量由以下公式确定：

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%]$$

M: Reception margin (%)

N: Ratio of bit rate to clock ($N = 32, 64, 372, 256$)

D: Duty cycle of clock ($D = 0$ to 1.0)

L: Frame length ($L = 10$)

F: Absolute value of clock frequency deviation

Assuming values of F = 0, D = 0.5, and N = 372 in the specified formula, the reception margin is determined using the following formula:

$M = \{0.5 - 1/(2 \times 372)\} \times 100\ [\%] = 49.866\ \%$

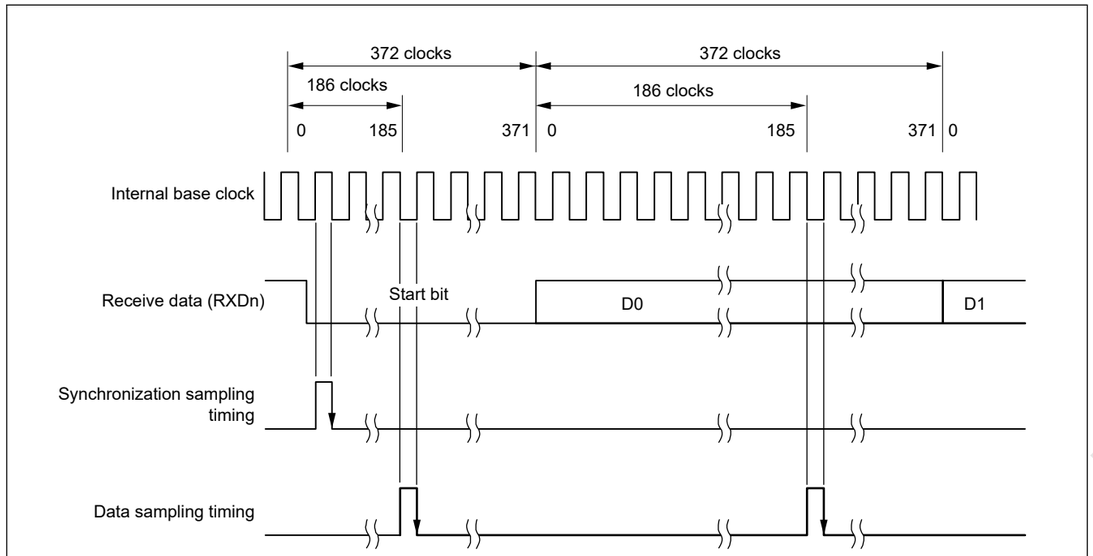


Figure 26.76 Receive data sampling timing in smart card interface mode when the clock frequency is 372 times the bit rate

26.7.5 SCI Initialization (Smart Card Interface Mode)

Before transmitting and receiving data, write the initial value 0x00 in the CCR0 register and initialize the SCI following the example flow shown in Table 26.37.

Always set the initial value in the TIE, RIE, TE, RE, TEIE bits in the CCR0 register before switching from transmission to reception mode or from reception to transmission mode. When CCR0.RE is set to 0, the RDR register is not initialized.

In transmission mode, set 1 to the CCR0.TE bit and CCR0.TIE bit simultaneously, then the SCIn_TXI interrupt request is generated.

To change from reception mode to transmission mode, first check that reception has completed, then initialize the SCI. At the end of initialization, set CCR0.TE = 1 and CCR0.RE = 0. Reception completion can be verified by reading the SCIn_RXI request, ORER, or PER flag in CSR.

To change transmission mode to reception mode, first check that transmission has completed, then initialize the SCI. At the end of initialization, set CCR0.TE = 0 and CCR0.RE = 1. Transmission completion can be verified by reading the TEND flag in CSR.

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%]$$

M：接收余量（%）

N：比特率与时钟的比率（N=32、64、372、256）

D：时钟的占空比（D=0到1.0）

L：帧长（L=10）

F：时钟频率偏差的绝对值

假设指定公式中的F=0、D=0.5和N=372的值，则使用以下公式确定接收余量：

$M = \{0.5 - 1/(2 \times 372)\} \times 100\ [\%] = 49.866\ \%$

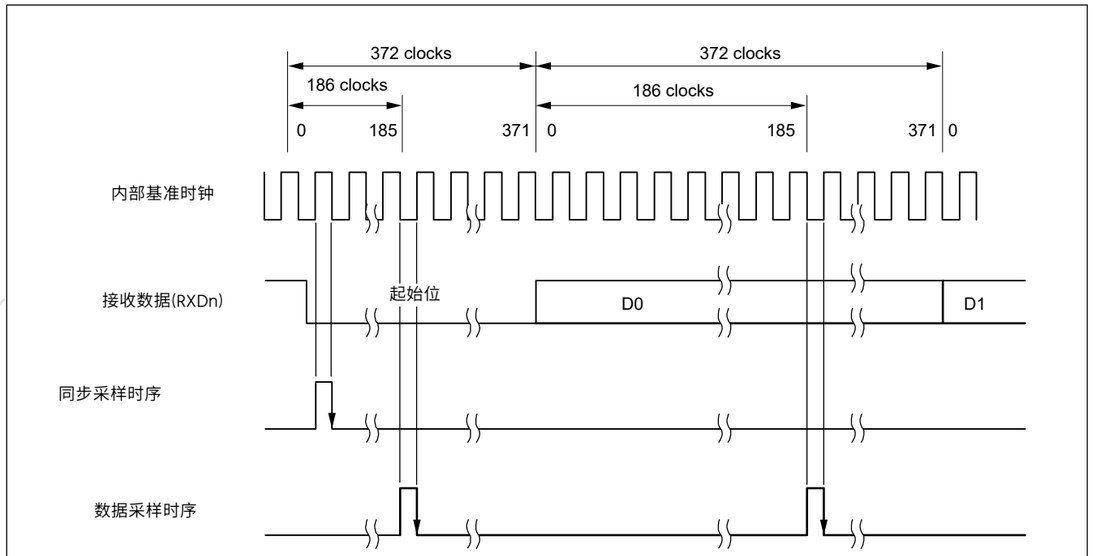


Figure 26.76 时钟频率为372倍比特率时智能卡接口模式下接收数据采样时序

26.7.5 SCI初始化（智能卡接口模式）

在发送和接收数据之前，将初始值0x00写入CCR0寄存器并按照表26.37所示的示例流程初始化SCI。

在从发送模式切换到接收模式或从接收模式切换到发送模式之前，请务必在CCR0寄存器的TIE、RIE、TE、RE、TEIE位中设置初始值。当CCR0.RE设置为0时，RDR寄存器未初始化。

在传输模式下，同时将CCR0.TE位和CCR0.TIE位设置为1，然后产生SCIn_TXI中断请求。

要从接收模式更改为发送模式，首先检查接收是否完成，然后初始化SCI。在初始化结束时，设置CCR0.TE=1和CCR0.RE=0。可以通过读取CSR中的SCIn_RXI请求、ORER或PER标志来验证接收完成。

要将传输模式更改为接收模式，首先检查传输是否完成，然后初始化SCI。在初始化结束时，设置CCR0.TE=0和CCR0.RE=1。可以通过读取CSR中的TEND标志来验证传输完成。

Table 26.37 Example flow of SCI initialization in smart card interface mode

No.	Step Name	Description
1	Start initialization	—
2	Set CCR0	Set CCR0.TEIE, TIE, RIE, TE, RE to 0. If you have not changed from the initial settings, you can skip this step.
3	Set CCR3	Set communication mode (MOD[2:0] = 001b), BLK, GM, and SINV. Leave other bits at their initial values.
4	Set CCR2	Set clock-select and bit-rate. Set BRME to 0.
5	Set CCR1	Set up the loop-back function, communication terminal status. Set NFEN, PE, CTSE to 0 and set PE to 1.
6	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
7	Set CCR3	Set CKE[1:0]. When the CKE[0] bit is set to “1” due on GM setting value, the clock is output from the SCKn pin.
8	Set CFCLR	Write 1 to the following bits and clear the corresponding flag. CFCLR.RDRFC,FERC,PERC,MFFC,ORERC,DFERC,DPERC,DCMFC,ERSC
9	Set CCR0	Set the TE or RE to 1. And set the TIE and RIE. Do not simultaneously set the TE and RE bits to 1 if self-diagnosis in not used.
10	Initialization completed	—

Figure 26.77 is a timing chart when data transmission is performed by making transition to the Smart Card Interface mode according to the above flow chart. The figure shows the case when CCR3.GM bit is 0. As shown in the figure, when the pin function is set to the SCKn pin, the SCKn pin is high impedance because the CCR3.CKE [0] bit is 0. When the TXDn pin is set, the TXDn pin is high impedance because the CCR0.TE bit is 0. Start clock output to the SCKn pin with the clock output setting CCR3.CKE [0] to 1, start data transmission by writing transmit data after setting CCR0.TE to 1.

In the smart card interface mode, even if not communicating at CCR0.TE = 0 and CCR0.RE = 0, the clock is continuously output if the clock output setting is used.

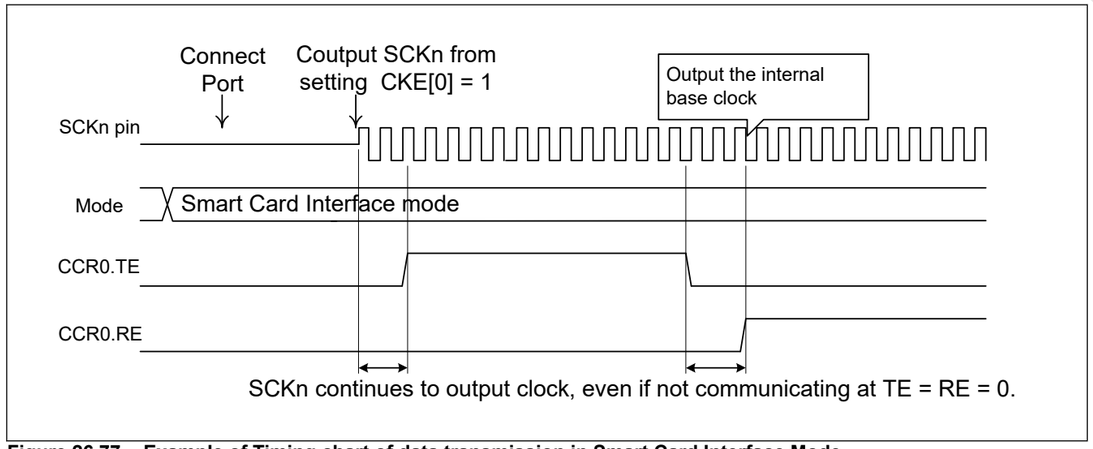


Figure 26.77 Example of Timing chart of data transmission in Smart Card Interface Mode

26.7.6 Serial Data Transmission (Except in Block Transfer Mode)

Serial data transmission in smart card interface mode (except in block transfer mode) is different from that in non-smart card interface mode, in that an error signal is sampled and data can be re-transmitted in smart card mode. Figure 26.78 shows the data re-transfer operation during transmission.

1. When an error signal from the receiver end is sampled after 1-frame data is transmitted, the CSR.ERS flag is set to 1. If the CCR0.RIE bit is 1, an SCIn_ERI interrupt request is generated. Clear the ERS flag to 0 before the next parity bit is sampled.

Table 26.37 智能卡接口模式下SCI初始化流程示例

No.	步骤名称	Description
1	开始初始化	—
2	Set CCR0	将CCR0.TEIE、TIE、RIE、TE、RE设置为0。如果未更改初始设置，则可以跳过此步骤。
3	Set CCR3	设置通信模式(MOD[2:0]=001b)、BLK、GM和SINV。将其他位保留为其初始值。
4	Set CCR2	设置时钟选择和比特率。将BRME设置为0。
5	Set CCR1	设置环回功能，通讯终端状态。将NFEN、PE、CTSE设置为0并设置 PE为1。
6	设置IO端口功能	进行IO端口设置以启用TXDn、RXDn和所需的输入和输出功能 SCKn pins.
7	Set CCR3	设置CKE[1:0]。当CKE[0]位根据GM设置值设置为“1”时，时钟从SCKn引脚输出。
8	Set CFCLR	将1写入以下位并清除相应的标志。 CFCLR.RDRFC,FERC,PERC,MFFC,ORERC,DFERC,DPERC,DCMFC,ERSC
9	Set CCR0	将TE或RE设置为1。并设置TIE和RIE。如果不使用自诊断，请勿同时将TE和RE位设置为1。
10	初始化完成	—

图26.77是按照上述流程图转换到智能卡接口模式进行数据传输时的时序图。图中为CCR3.GM位为0的情况。如图所示，当引脚功能设置为SCKn引脚时，由于CCR3.CKE[0]位为0，SCKn引脚为高阻态。当TXDn引脚置位，TXDn引脚为高阻抗，因为CCR0.TE位为0。时钟输出设置CCR3.CKE[0]为1开始向SCKn引脚输出时钟，设置后通过写入发送数据开始数据传输CCR0.TE为1。

在智能卡接口模式下，即使在CCR0.TE=0和CCR0.RE=0时不通信，如果使用时钟输出设置，时钟也会连续输出。

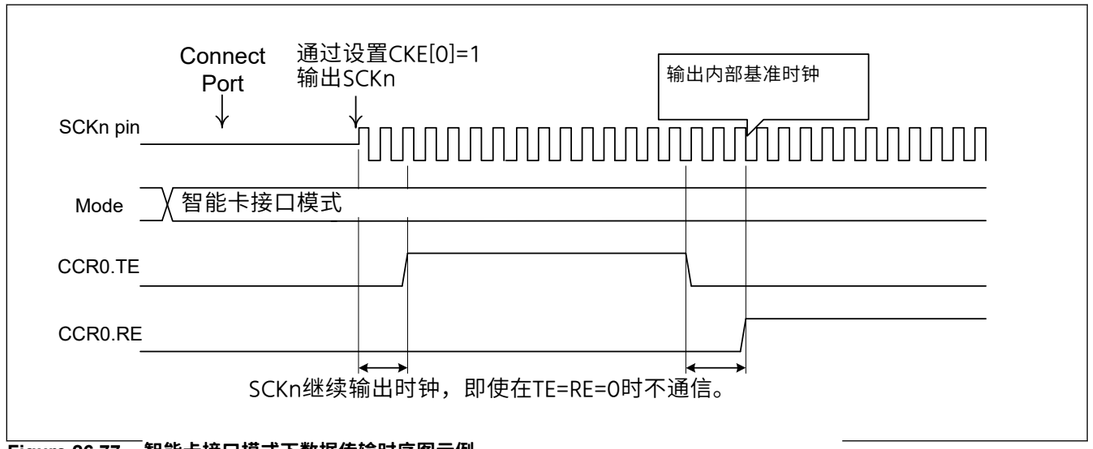


Figure 26.77 智能卡接口模式下数据传输时序图示例

26.7.6 串行数据传输（块传输模式除外）

智能卡接口模式下的串行数据传输（块传输模式除外）与非智能卡接口模式下的串行数据传输不同之处在于，在智能卡模式下对错误信号进行采样，数据可以重新传输。图26.78显示了传输过程中的数据重新传输操作。

1.发送1帧数据后，当从接收端采样到错误信号时，CSR.ERS标志置1。如果CCR0.RIE位为1，则产生SCIn_ERI中断请求。在采样下一个奇偶校验位之前将ERS 标志清零。

2. For a frame in which an error signal is received, the CSR.TEND flag is not set. Data is re-transferred from TDR to TSR, allowing automatic data retransmission.
3. If no error signal is returned from the receiver, the ERS flag is not set to 1.
4. In this case, the SCI determines that transmission of 1-frame data, including the re-transfer, is complete, and the TEND flag is set. If the CCR0.TIE bit is 1, an SCIn_TXI interrupt request is generated. Write transmit data to the TDR to start transmission of the next data.

Figure 26.80 shows an example flow of serial transmission. All the processing steps are automatically performed using an SCIn_TXI interrupt request to activate the DTC or DMAC.

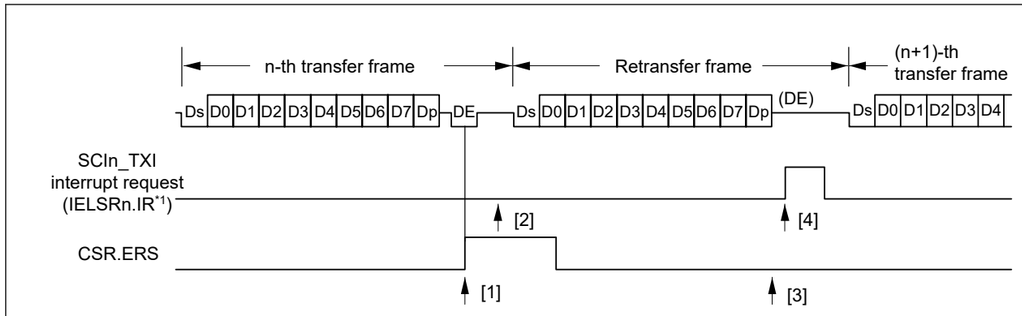
When the CSR.TEND flag is set to 1 in transmission and when the CCR0.TIE bit is 1, an SCIn_TXI interrupt request is generated.

The DTC or DMAC is activated by an SCIn_TXI interrupt request if the SCIn_TXI interrupt request is previously specified as a source of DTC or DMAC activation, allowing the transfer of transmit data. The TEND flag is automatically set to 0 when the DTC or DMAC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During this retransmission, the TEND flag is kept at 0 and the DTC or DMAC is not activated. Therefore, the SCI and DTC or DMAC automatically transmit the specified number of bytes, including retransmission when an error occurs. Because the ERS flag is not automatically cleared, set the RIE bit to 1 before enabling an SCIn_ERI interrupt request to be generated if an error occurs, and clear the ERS flag to 0.

When transmitting or receiving data using the DTC or DMAC, always enable the DTC or DMAC before making the SCI settings.

For DTC or DMAC settings, see section 16, Data Transfer Controller (DTC), section 15, DMA Controller (DMAC).



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.78 Data re-transfer operation in smart card interface transmission mode

The CSR.TEND flag is set at different timings depending on the CCR3.GM bit setting. Figure 26.79 shows the TEND flag generation timing.

2.对于接收到错误信号的帧，不设置CSR.TEND标志。数据从TDR重新传输到TSR，允许自动数据重新传输。

3.如果接收器没有返回错误信号，则ERS 标志不设置为1。

4.在这种情况下，SCI确定1帧数据的传输（包括重新传输）已完成，并设置TEND标志。如果CCR0.TIE位为1，则产生SCIn_TXI中断请求。将传输数据写入TDR以开始传输下一个数据。

图26.80显示了串行传输的示例流程。所有处理步骤都使用一个自动执行SCIn_TXI中断请求以激活DTC或DMAC。

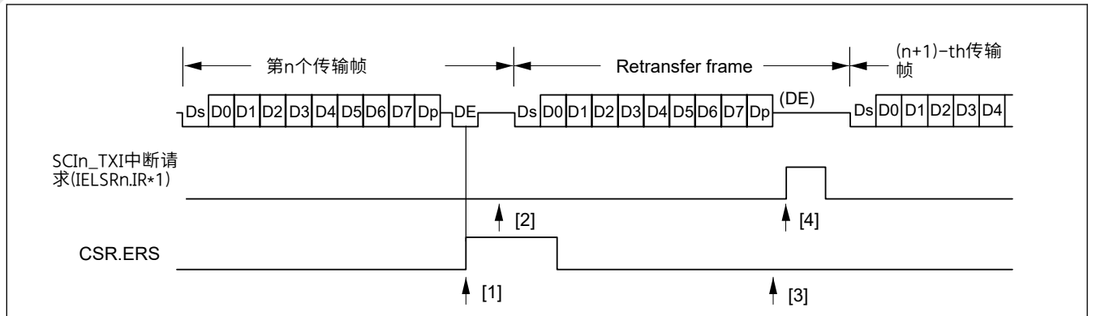
当CSR.TEND标志在传输中设置为1且CCR0.TIE位为1时，将产生SCIn_TXI中断请求。

如果先前将SCIn_TXI中断请求指定为DTC或DMAC激活源，则DTC或DMAC由SCIn_TXI中断请求激活，从而允许传输发送数据。当DTC或DMAC传输数据时，TEND标志自动设置为0。

如果发生错误，SCI会自动重新传输相同的数据。在此重传期间，TEND标志保持为0，并且DTC或DMAC未激活。因此，SCI和DTC或DMAC会自动传输指定的字节数，包括发生错误时的重传。因为ERS 标志不会自动清零，所以如果发生错误，在使能SCIn_ERI中断请求之前将RIE位设置为1，并将ERS 标志清零。

使用DTC或DMAC发送或接收数据时，请务必在进行SCI设置之前启用DTC或DMAC。

对于DTC或DMAC设置，请参阅第16节，数据传输控制器(DTC)，第15节，DMA控制器(DMAC)。



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.78 智能卡接口传输模式下的数据重传操作

CSR.TEND标志根据CCR3.GM位设置在不同的时间设置。图26.79显示了TEND标志生成时序。

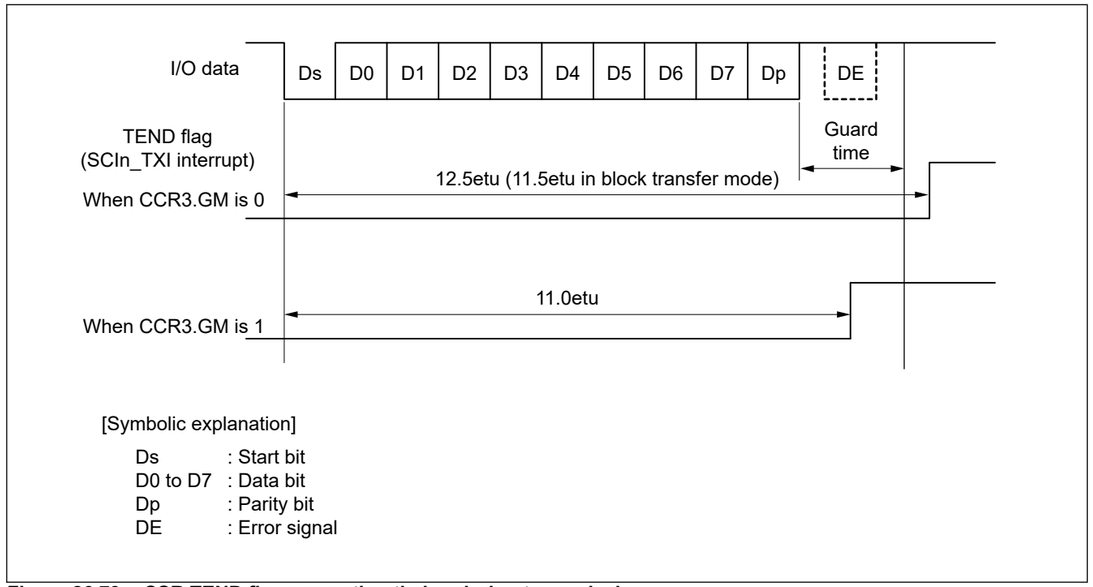


Figure 26.79 CSR.TEND flag generation timing during transmission

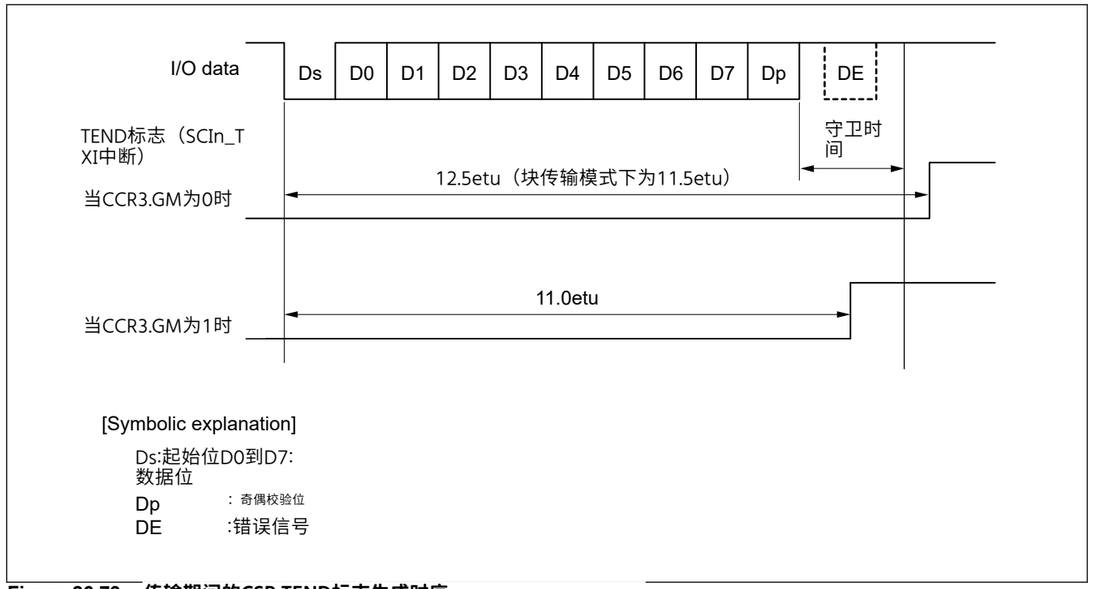


Figure 26.79 传输期间的CSR.TEND标志生成时序

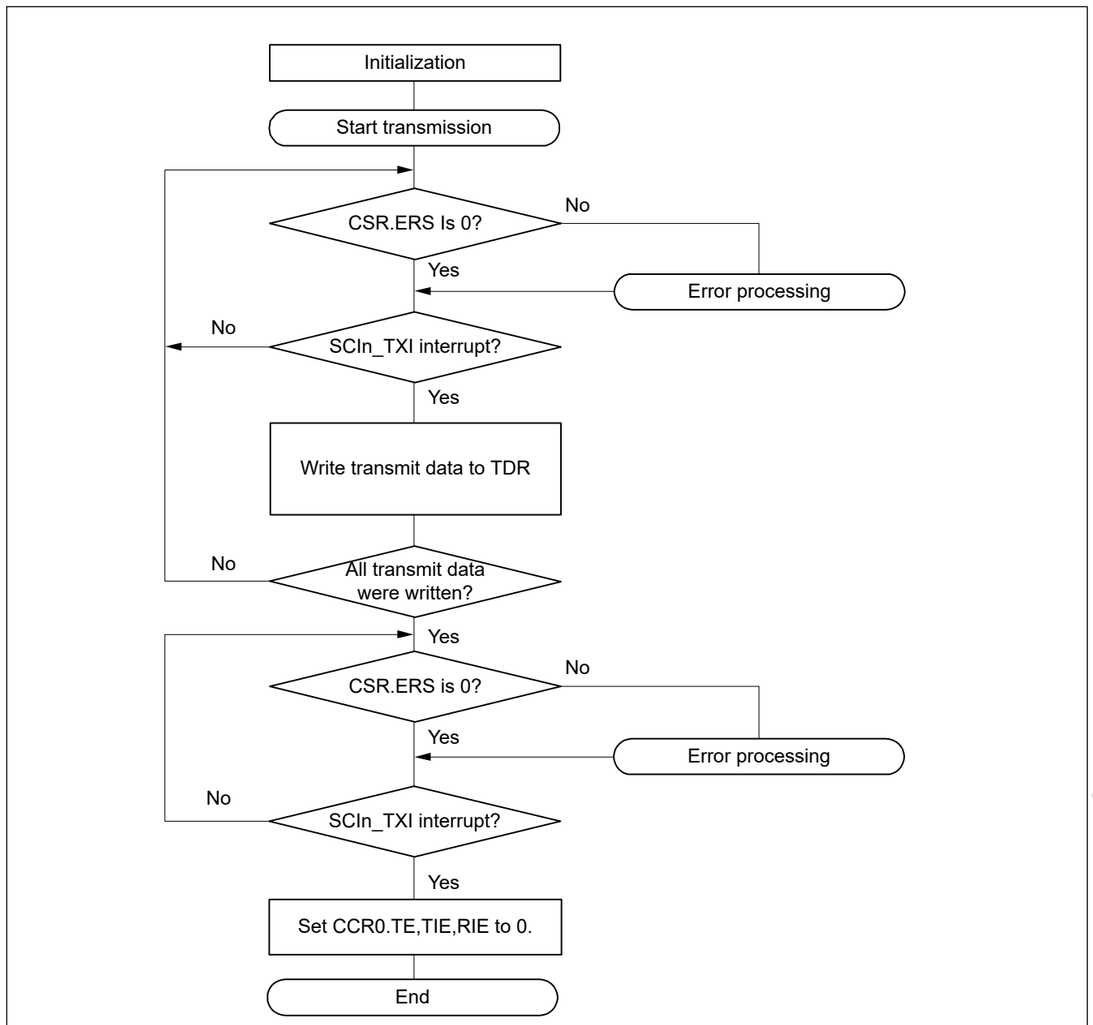


Figure 26.80 Example flow of smart card interface transmission

26.7.7 Serial Data Reception (Except in Block Transfer Mode)

Serial data reception in smart card interface mode is similar to that in non-smart card interface mode. Figure 26.81 shows the data re-transfer operation in reception mode.

1. If a parity error is detected in the receive data, the CSR.PER flag is set to 1. When the CCR0.RIE bit is 1, an SCIn_ERI interrupt request is generated. Clear the PER flag to 0 before the next parity bit is sampled.
2. For a frame in which a parity error is detected, no SCIn_RXI interrupt is generated.
3. When no parity error is detected, the CSR.PER flag is not set to 1.
4. In this case, data is determined to be received successfully. When the CCR0.RIE bit is 1, an SCIn_RXI interrupt request is generated.

Figure 26.82 shows an example flow of serial data reception. All the processing steps are automatically performed using an SCIn_RXI interrupt request to activate the DTC or DMAC.

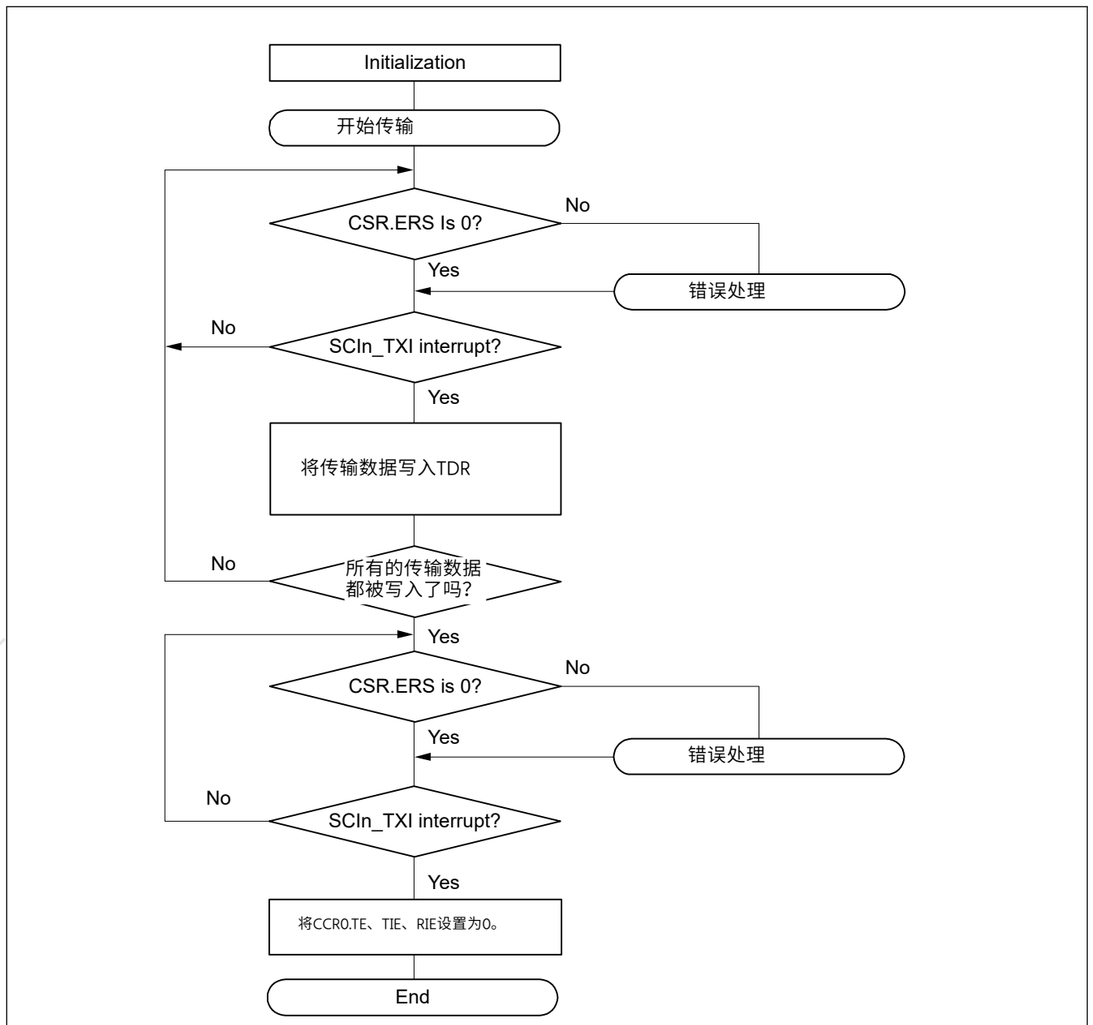


Figure 26.80 智能卡接口传输示例流程

26.7.7 串行数据接收（块传输模式除外）

智能卡接口模式下的串行数据接收与非智能卡接口模式下的串行数据接收类似。图26.81显示了接收模式下的数据重传操作。

1.如果在接收数据中检测到奇偶校验错误，则CSR.PER标志设置为1。当CCR0.RIE位为1时，产生SCIn_ERI中断请求。在采样下一个奇偶校验位之前将PER标志清零。

2.对于检测到奇偶校验错误的帧，不产生SCIn_RXI中断。

3.当没有检测到奇偶校验错误时，CSR.PER标志不设置为1。

4、在这种情况下，确定数据接收成功。当CCR0.RIE位为1时，产生SCIn_RXI中断请求。

图26.82显示了串行数据接收的示例流程。所有处理步骤都使用一个自动执行SCIn_RXI中断请求以激活DTC或DMAC。

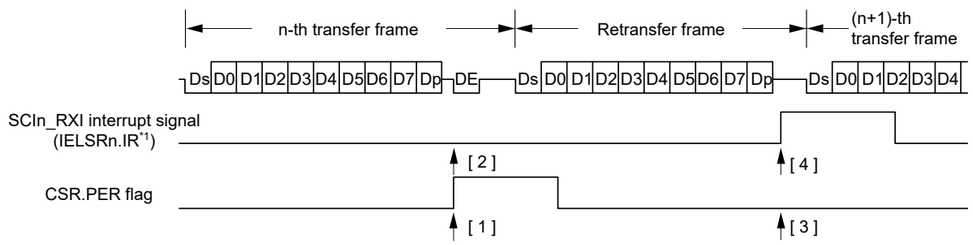
In reception, setting the RIE bit to 1 allows an SCIn_RXI interrupt request to be generated. The DTC or DMAC is activated by an SCIn_RXI interrupt request if the SCIn_RXI interrupt request is previously specified as a source of DTC or DMAC activation, allowing the transfer of receive data.

If an error occurs during reception and either the ORER or PER flag in CSR is set to 1, a receive error interrupt (SCIn_ERI) request is generated. Clear the error flag after the error occurrence. If an error occurs, the DTC or DMAC is not activated and receive data is skipped. Therefore, the number of bytes of receive data specified in the DTC or DMAC is transferred.

If a parity error occurs and the PER flag is set to 1 during reception, the receive data is transferred to RDR, allowing the data to be read.

When a reception is forced to terminate by setting CCR0.RE to 0 during operation, read the RDR register because the received data that is not yet read might be left in the RDR.

Note: For operations in block transfer mode, see section 26.3.9. Serial Data Reception in Asynchronous Mode.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.81 Data re-transfer operation in smart card interface reception mode

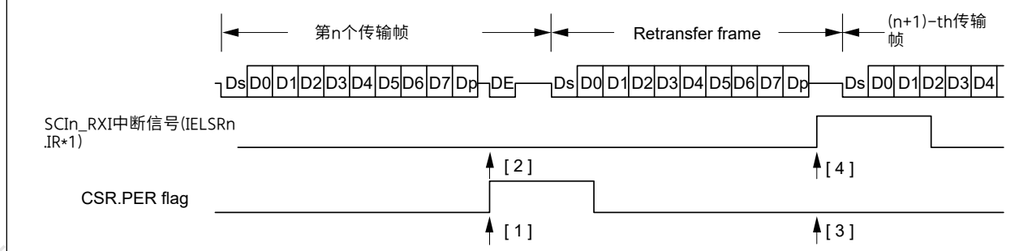
在接收时，将RIE位设置为1允许产生SCIn_RXI中断请求。如果SCIn_RXI中断请求先前被指定为DTC或DMAC激活源，则DTC或DMAC由SCIn_RXI中断请求激活，从而允许传输接收数据。

如果在接收期间发生错误并且CSR中的ORER或PER标志设置为1，则会产生接收错误中断(SCIn_ERI)请求。错误发生后清除错误标志。如果发生错误，则不会激活DTC或DMAC并跳过接收数据。因此，将传输DTC或DMAC中指定的接收数据字节数。

如果在接收过程中发生奇偶校验错误并且PER标志设置为1，则接收数据将传输到RDR，从而可以读取数据。

如果在操作期间通过将CCR0.RE设置为0来强制终止接收，请读取RDR寄存器，因为尚未读取的接收数据可能会留在RDR中。

Note: 关于块传输模式下的操作，请参见第26.3.9节。异步模式下的串行数据接收。



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.81 智能卡接口接收模式下的数据重传操作

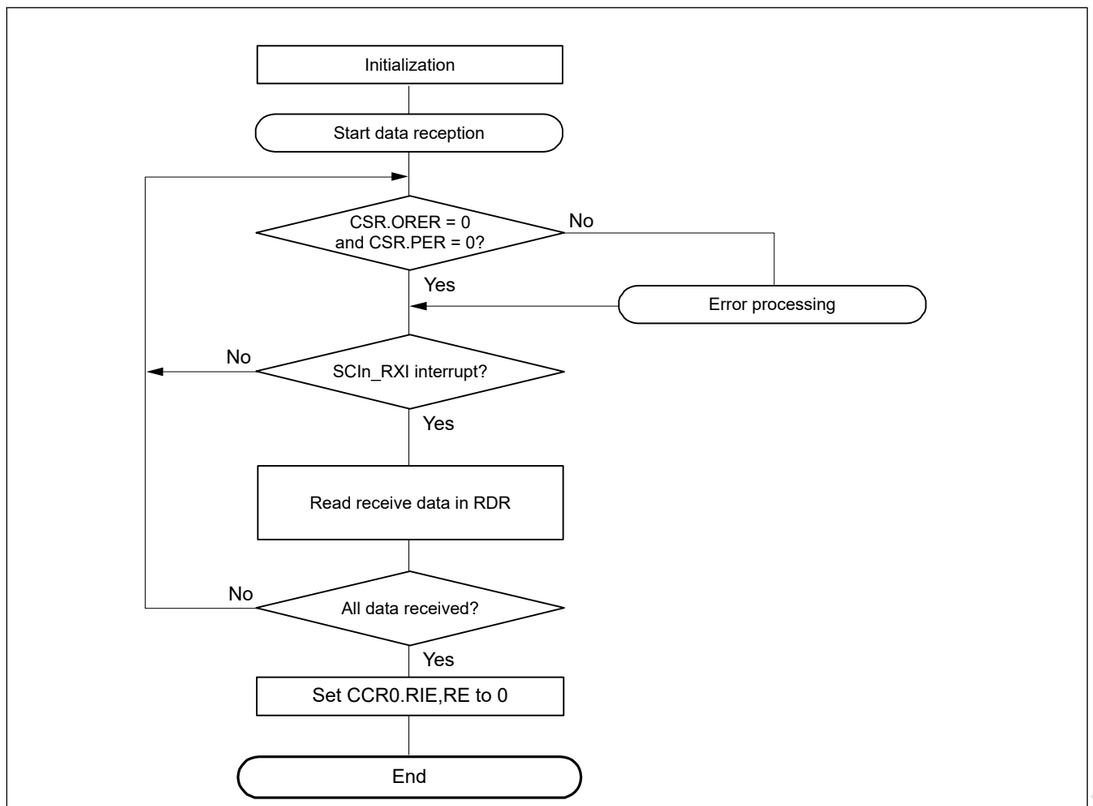


Figure 26.82 Example flow of smart card interface reception

26.7.8 Clock Output Control

When the GM bit in CCR3 is set to 1, the clock output can be controlled by the CKE[1:0] bits in CCR3. For details on the CKE[1:0] bits, see section 26.2.8. CCR3 : Common Control Register 3. When setting the clock output, the base clock described in section 26.7.4. Receive Data Sampling Timing and Reception Margin the bit rate is set by CCR2.CKS, CCR2.BCP[2:0] and BRR[7:0].

Figure 26.83 shows an example timing for the clock output control when the CKE[1] bit in CCR3 is set to 0 and the CKE[0] bit in CCR3 is controlled.

When the GM bit in CCR3 is 0, output control by the CKE[0] bit in CCR3 is immediately reflected on the SCKn pin, so there is a possibility that pulses with an unintended width may be output from the SCKn pin.

When the GM bit in CCR3 is 1, the output pulse control by the CCR3.CKE [0] controls the pulse width set to be based on the state of the base clock.

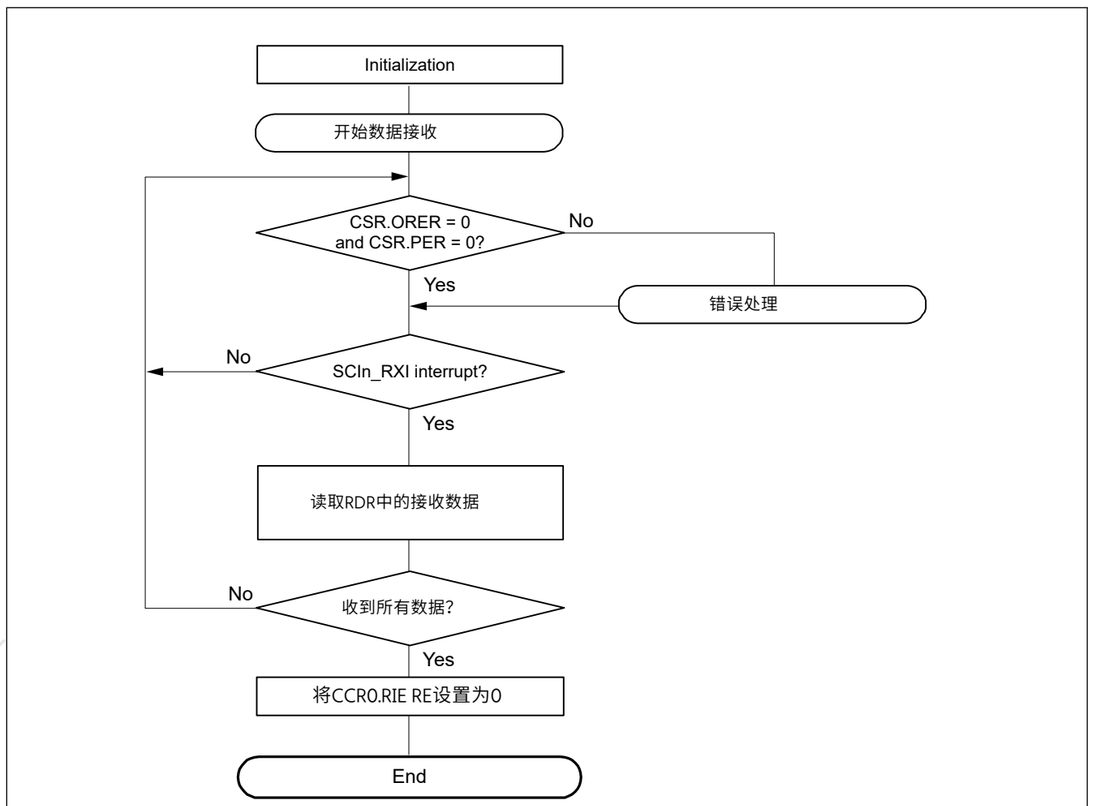


Figure 26.82 智能卡接口接收示例流程

26.7.8 时钟输出控制

当CCR3中的GM位设置为1时，时钟输出可由CCR3中的CKE[1:0]位控制。有关详细信息CKE[1:0]位，参见第26.2.8节。CCR3：公共控制寄存器3。设置时钟输出时，使用第26.7.4节中描述的基本时钟。接收数据采样时序和接收裕度比特率由CCR2.CKS、CCR2.BCP[2:0]和BRR[7:0]设置。

图26.83显示了当CCR3中的CKE[1]位设置为0并控制CCR3中的CKE[0]位时时钟输出控制的示例时序。

当CCR3的GM位为0时，CCR3的CKE[0]位的输出控制立即反映在SCKn引脚上，因此有可能会从SCKn引脚输出不期望宽度的脉冲。

当CCR3中的GM位为1时，由CCR3.CKE[0]控制的输出脉冲控制设置为基于基本时钟状态的脉冲宽度。

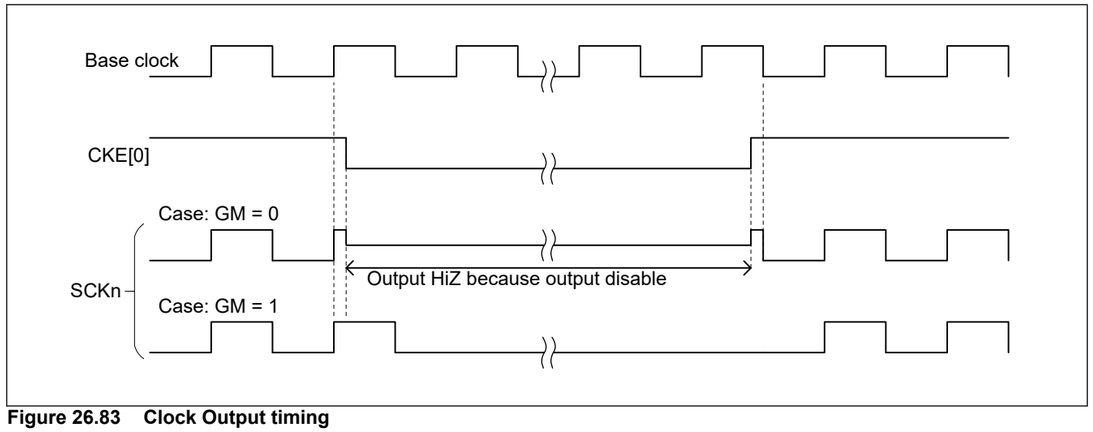


Figure 26.83 Clock Output timing

26.8 Operation in Simple IIC Mode

Simple IIC mode format is composed of 8 data bits and an acknowledge bit. By continuing into a slave-address frame after a start condition or restart condition, a master device can specify a slave device as the partner for communications. The currently specified slave device remains valid until a new slave device is specified or a stop condition is satisfied. The 8 data bits in all frames are transmitted in order from the MSB.

The I^2C bus format and timing of the I^2C bus are shown in Figure 26.84 and Figure 26.85.

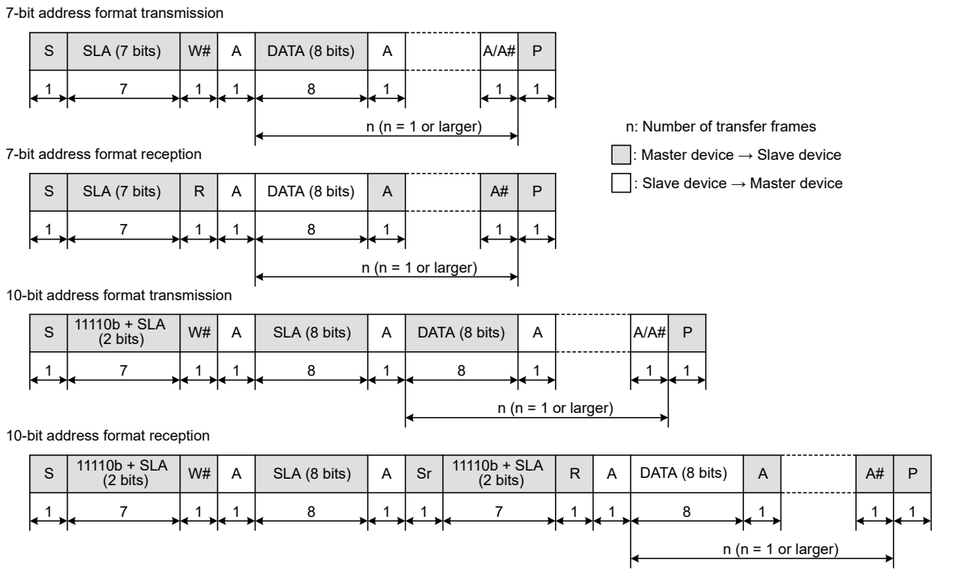


Figure 26.84 I^2C bus format

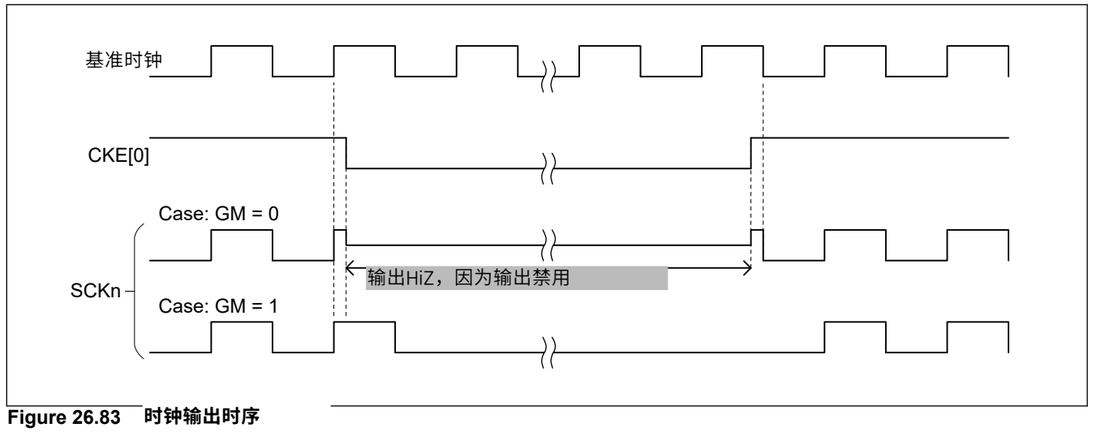


Figure 26.83 时钟输出时序

26.8 简单IIC模式下的操作

简单IIC模式格式由8个数据位和一个确认位组成。通过在启动条件或重新启动条件之后继续进入从地址帧，主设备可以指定从设备作为通信伙伴。当前指定的从设备保持有效，直到指定新的从设备或满足停止条件。所有帧中的8个数据位从MSB开始按顺序传输。

I2C总线格式和I2C总线时序如图26.84和图26.85所示。

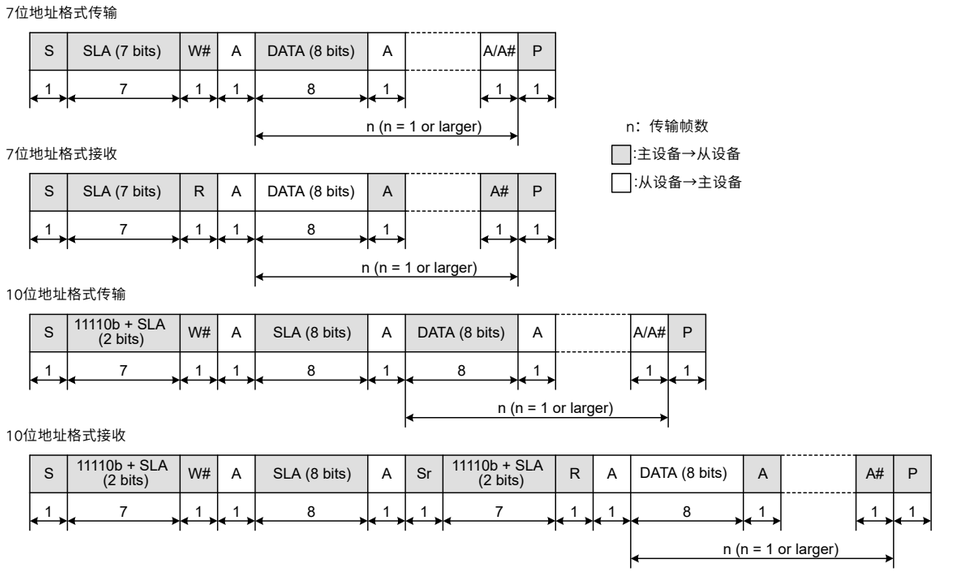


Figure 26.84 I2C总线格式

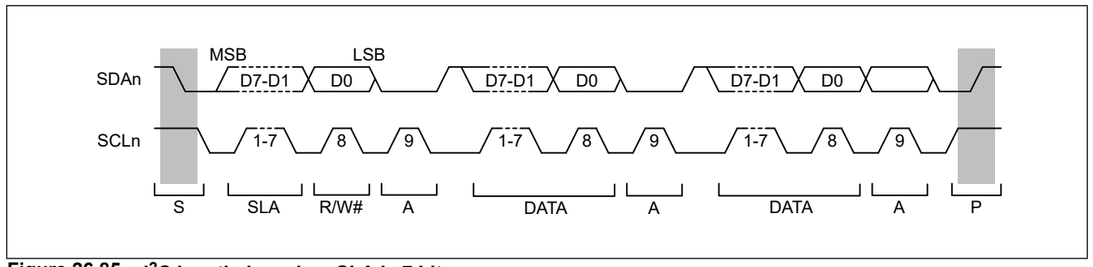


Figure 26.85 I^2C bus timing when SLA is 7 bits

- S: Indicates a start condition, when the master device changes the level on the SDAn line from high to low while the SCLn line is high
- SLA: Indicates a slave address, by which the master device selects a slave device
- R/W#: Indicates the direction of transfer (reception or transmission). The value 1 indicates transfer from the slave device to the master device and 0 indicates transfer from the master device to the slave device.
- A/A#: Indicates an acknowledge bit. This is returned by the slave device for master transmission and by the master device for master reception. Return low indicates ACK and return high indicates NACK.
- Sr: Indicates a restart condition, when the master device changes the level on the SDAn line from high to low while the SCLn line is high and after the setup time elapses
- DATA: Indicates the data being received or transmitted
- P: Indicates a stop condition, when the master device changes the level on the SDAn line from low to high while the SCLn line is high

26.8.1 Generation of Start, Restart, and Stop Conditions

Writing 1 to the ICR.IICSTAREQ bit causes the generation of a start condition. The generation of a start condition proceeds through the following operations:

- The level on the SDAn line falls (from the high level to the low level) and the SCLn line is kept in the released state
- The hold time for the start condition is set as half of a bit period at the bit rate determined by the CCR2.BRR setting
- The level on the SCLn line falls (from the high level to the low level), the IICSTAREQ bit in ICR is set to 0, and a start-condition generated interrupt is output

Writing 1 to the IICRSTAREQ bit in ICR causes the generation of a restart condition. The generation of a restart condition proceeds through the following operations:

- The SDAn line is released and the SCLn line is kept at the low level
- The period at low level for the SCLn line is set as half of a bit period at the bit rate determined by the CCR2.BRR setting
- The SCLn line is released (transition from the low to the high level)
- When a high level is detected on the SCLn line, the setup time for the restart condition is set as half of a bit period at the bit rate determined by the CCR2.BRR setting
- The level on the SDAn line falls (from the high level to the low level)
- The hold time for the restart condition is set as half of a bit period at the bit rate determined by the CCR2.BRR setting
- The level on the SCLn line falls (from the high level to the low level), the ICR.IICRSTAREQ bit is set to 0, and a restart-condition generated interrupt is output

Writing 1 to the ICR.IICSTPREQ bit causes the generation of a stop condition. The generation of a stop condition proceeds through the following operations:

- The level on the SDAn line falls (from the high level to the low level) and the SCLn line is kept at the low level
- The period at low level for the SCLn line is set as half of a bit period at the bit rate determined by the CCR2.BRR setting

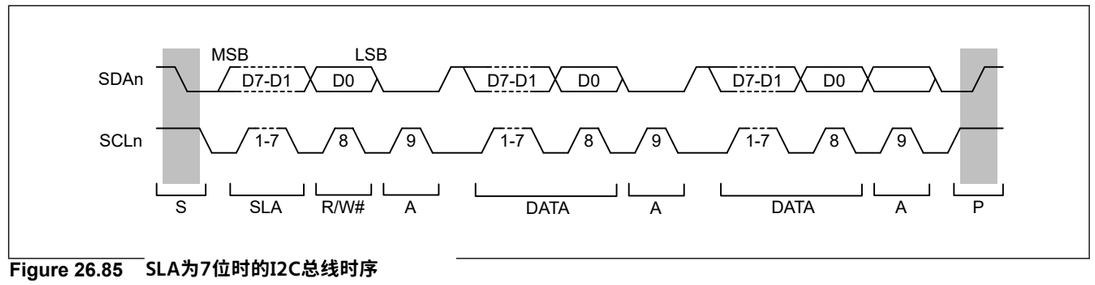


Figure 26.85 SLA为7位时的I2C总线时序

●S：表示启动条件，当主设备在SCLn线为高时将SDAn线上的电平从高电平变为低电平

●SLA：表示从地址，主设备通过该地址选择从设备

●RW#：指示传输方向（接收或传输）。值1表示从从设备传输到主设备，0表示从主设备传输到从设备。

●AA#：表示确认位。这由从设备返回用于主传输，并由主设备返回用于主接收。返回低电平表示ACK，返回高电平表示NACK。

●Sr：表示重启条件，当主设备将SDAn线上的电平从高电平变为低电平，而SCLn线为高电平且经过设置时间后

●DATA：表示正在接收或发送的数据

●P：表示停止条件，当主设备将SDAn线上的电平从低电平变为高电平而SCLn线为高电平时

26.8.1 启动、重启和停止条件的生成

将1写入ICR.IICSTAREQ位会导致产生启动条件。开始条件的生成通过以下操作进行：

●SDAn线上的电平下降（从高电平到低电平），SCLn线保持在释放状态

●开始条件的保持时间设置为比特周期的一半，比特率由CCR2.BRR设置确定

●SCLn线上的电平下降（从高电平到低电平），ICR中的IICSTAREQ位设置为0，并输出一个startcondition产生的中断

将1写入ICR中的IICRSTAREQ位会导致产生重启条件。重新启动条件的生成通过以下操作进行：

●SDAn线释放，SCLn线保持低电平

●SCLn线的低电平周期设置为比特周期的一半，比特率由CCR2.BRR设置确定

●SCLn线被释放（由低电平转变为高电平）

●当在SCLn线上检测到高电平时，重新启动条件的建立时间设置为比特周期的一半，比特率由CCR2.BRR设置确定

●SDAn线上的电平下降（从高电平到低电平）

●重启条件的保持时间设置为比特周期的一半，比特率由CCR2.BRR设置确定

●SCLn线上的电平下降（从高电平变为低电平），ICR.IICRSTAREQ位设置为0，并输出重启条件产生的中断

将1写入ICR.IICSTPREQ位会导致产生停止条件。停止条件的生成通过以下操作进行：

●SDAn线上的电平下降（从高电平到低电平），SCLn线保持在低电平

●SCLn线的低电平周期设置为比特周期的一半，比特率由CCR2.BRR设置确定

- The SCLn line is released (transition from the low to the high level)
- When a high level is detected on the SCLn line, the setup time for the stop condition is set as half of a bit period at the bit rate determined by the CCR2.BRR setting
- The SDAn line is released (transition from the low to the high level), the ICR.IICSTPREQ bit is set to 0, and a stop-condition generated interrupt is output

Figure 26.86 shows the timing of operations in the generation of start, restart, and stop conditions.

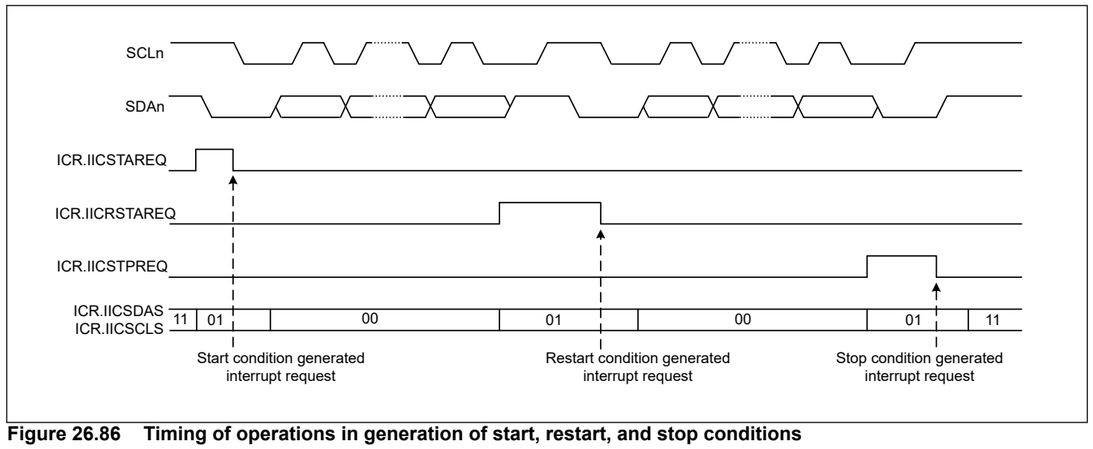


Figure 26.86 Timing of operations in generation of start, restart, and stop conditions

26.8.2 Clock Synchronization

The SCLn line can be driven low if a wait is inserted by a slave device at the other side of the transfer. Setting the ICR.IICCSC bit to 1 applies control to obtain synchronization when a difference arises between the levels of the internal SCLn clock signal and the level being input on the SCLn pin.

When the ICR.IICCSC bit is set to 1, the level of the internal SCLn clock signal changes from low to high. Counting to determine the period at a high level stops while the low level is being input on the SCLn pin. Counting to determine the period at a high level starts after the transition of the input on the SCLn pin to the high level.

The interval from this time until counting to determine the period at high level starts on the transition of the SCLn pin to the high level, is the total time which contains the SCLn input delay, delay for noise filtering of the input on the SCLn pin (2 or 3 cycles of sampling clock for the noise filter), and delay for internal processing (1 or 2 cycles of PCLK). The period at high level of the internal SCLn clock is extended even when other devices do not place the low level on the SCLn line.

If the ICR.IICCSC bit is 1, synchronization is obtained for the transmission and reception of data by taking the logical AND of the input on the SCLn pin and the internal SCLn clock. If the ICR.IICCSC bit is 0, synchronization with the internal SCLn clock is obtained for the transmission and reception of data.

If a slave device inserts a wait period into the interval until the transition of the internal SCLn clock signal from the low to the high level after a request for the generation of a start, restart, or stop condition is issued, the time until generation is prolonged by that period.

If a slave device inserts a wait period after the transition of the internal SCLn clock signal from the low to the high level, although the generation-completed interrupt is issued without stopping the waiting period, generation of the condition itself is not guaranteed.

Figure 26.87 shows an example operation for synchronizing the clocks.

●SCLn线被释放（由低电平转变为高电平）
●当在SCLn线上检测到高电平时，停止条件的建立时间设置为CCR2.BRR设置确定的比特率的半个比特周期

●SDAn线被释放（从低电平转换到高电平），ICR.IICSTPREQ位设置为0，并输出停止条件生成中断

图26.86显示了生成启动、重新启动和停止条件的操作时序。

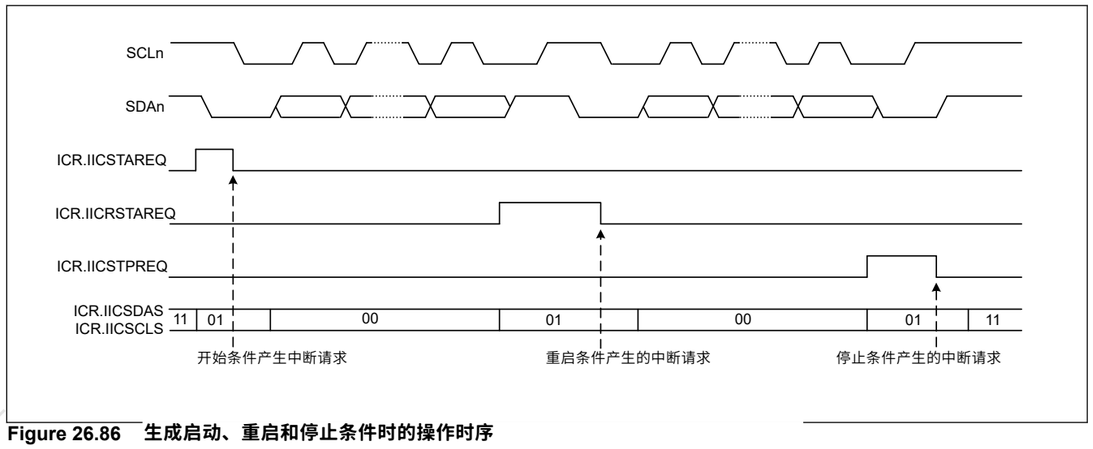


Figure 26.86 生成启动、重启和停止条件时的操作时序

26.8.2 时钟同步

如果从设备在传输的另一侧插入等待，则可以将SCLn线驱动为低电平。设置
当内部电平之间出现差异时，ICR.IICCSC位为1应用控制以获得同步
SCLn时钟信号和输入到SCLn引脚的电平。

当ICR.IICCSC位设置为1时，内部SCLn时钟信号的电平由低变为高。当SCLn引脚输入低电平时，停止计数以确定高电平周期。在SCLn引脚上的输入转换为高电平后，开始计数以确定高电平的周期。

从这个时间到从SCLn引脚转变为高电平开始计数以确定高电平周期的时间间隔是包含SCLn输入延迟、SCLn引脚上输入的噪声过滤延迟的总时间（噪声滤波器的2或3个采样时钟周期）和内部处理的延迟（1或2个PCLK周期）。即使其他设备没有将低电平置于SCLn线上，内部SCLn时钟的高电平周期也会延长。

如果ICR.IICCSC位为1，则通过对SCLn引脚上的输入和内部SCLn时钟进行逻辑与来获得数据发送和接收的同步。如果ICR.IICCSC位为0，则与内部SCLn时钟同步，用于数据的发送和接收。

如果从设备在发出启动、重新启动或停止条件的生成请求后，在内部SCLn时钟信号从低电平转变为高电平之前的间隔中插入一个等待周期，则直到生成的时间为延长了那个时期。

如果从设备在内部SCLn时钟信号从低电平转变为高电平之后插入等待周期，尽管在不停止等待周期的情况下发出生成完成中断，但不能保证条件本身的生成。

图26.87显示了同步时钟的示例操作。

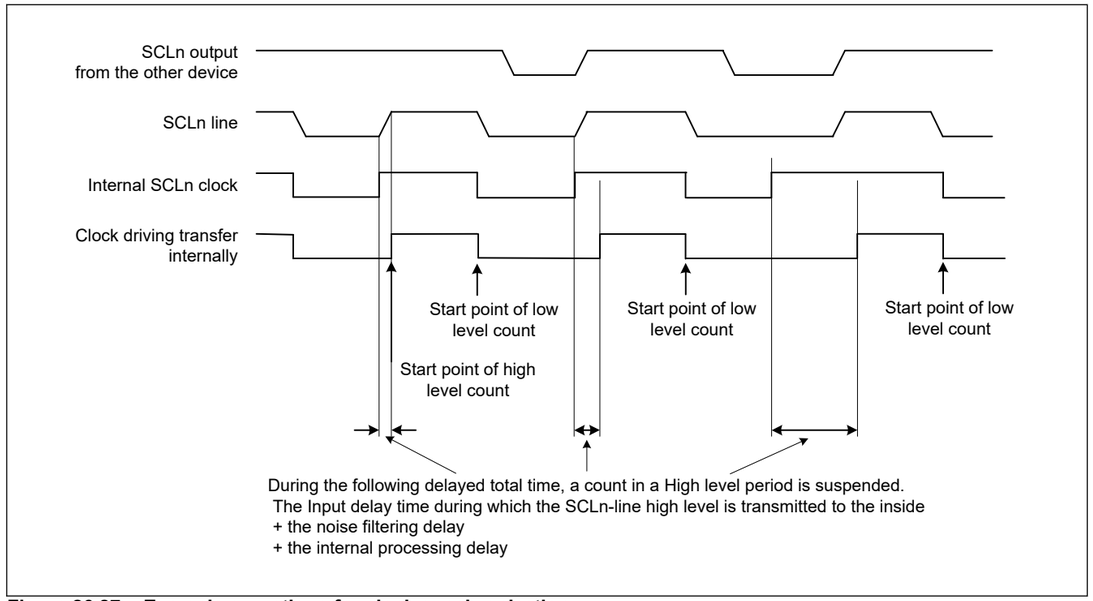


Figure 26.87 Example operations for clock synchronization

26.8.3 SDAn Output Delay

The ICR.IICDL[4:0] bits can be used to set a delay for output on the SDAn pin relative to falling edges of output on the SCLn pin. Delay settings from 0 to 31 are selectable, representing periods of the corresponding numbers of cycles of the clock signal from the on-chip baud rate generator (derived by frequency-dividing the base clock, TCLK, by the divisor selected in the CCR2.CKS[1:0] bits). A delay for output on the SDAn pin applies to the start condition/restart condition/stop condition signal, 8-bit transmit data, and acknowledge bit.

If the SDAn output delay is shorter than the time for the level on the SCLn pin to fall, the change of the output on the SDAn pin starts while the output level on the SCLn pin is falling, creating a possibility of erroneous operation for slave devices. Ensure that settings for the delay of output on the SDAn pin specify times greater than the time output on the SCLn pin takes to fall (300 ns for IIC in normal mode and fast mode).

Figure 26.88 shows the timing of delays in SDAn output.

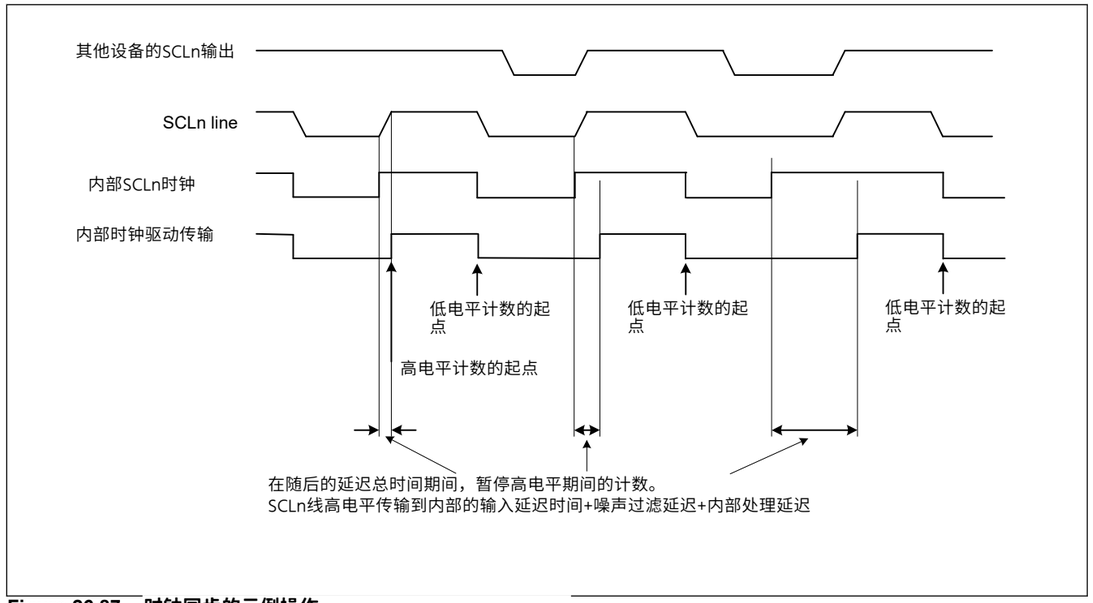


Figure 26.87 时钟同步的示例操作

26.8.3 SDAn输出延迟

ICR.IICDL[4:0]位可用于设置SDAn引脚输出相对于SCLn引脚输出下降沿的延迟。可选择从0到31的延迟设置，表示来自片上波特率发生器的时钟信号的相应周期数的周期（通过将基本时钟TCLK分频得到CCR2.CKS中选择的除数）[1:0]位）。SDAn引脚上的输出延迟适用于启动条件重启条件停止条件信号、8位发送数据和确认位。

如果SDAn输出延迟小于SCLn引脚电平下降的时间，则SDAn引脚上的输出变化会在SCLn引脚上的输出电平下降时开始，从而产生从设备错误操作的可能性.确保SDAn引脚上的输出延迟设置指定的时间大于SCLn引脚上输出的下降时间（IIC在正常模式和快速模式下为300ns）。

图26.88显示了SDAn输出中的延迟时间。

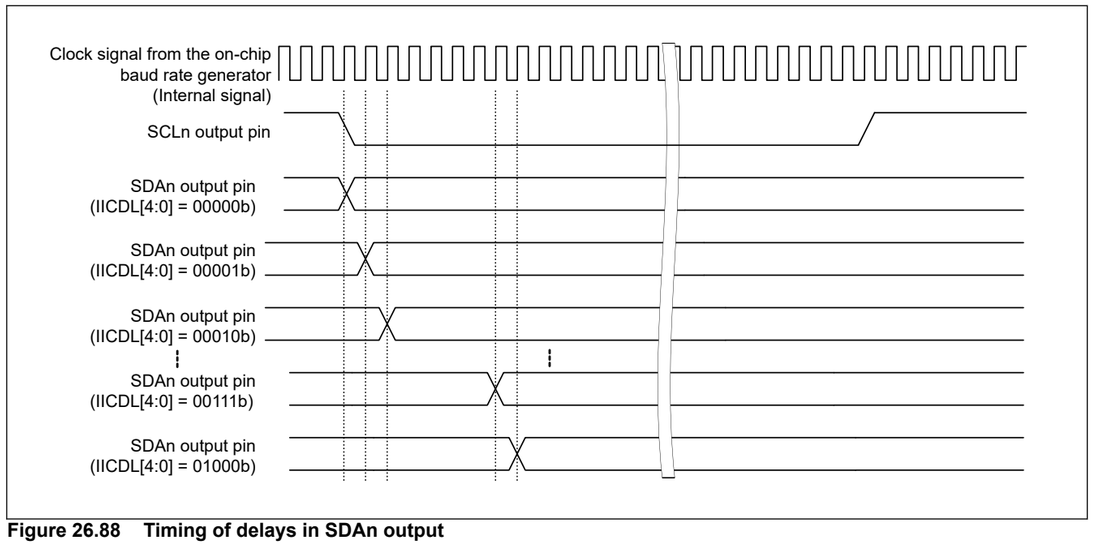


Figure 26.88 Timing of delays in SDAn output

26.8.4 SCI Initialization in Simple IIC Mode

Before transferring data, write the initial value 0x00 to CCR0 and initialize the interface following the example shown in Table 26.38.

Before making any changes to the operating mode or transfer format, be sure to set CCR0 to its initial value. In simple IIC mode, the open-drain setting for the communication ports should be made on the port side.

Table 26.38 Example flow of SCI initialization in simple IIC mode

No.	Step Name	Description
1	Start initialization	—
2	Set CCR0	Set CCR0.TEIE, TIE, RIE, TE, RE to 0. If you have not changed from the initial settings, you can skip this step.
3	Set ICR	Set the IICSDAS[1:0] and IICSCLS[1:0] to 11b. Set the IICDL[4:0] and IICINTM as required. Set the IICACKT and the IICCSC bits to 1.
4	Set CCR3	Set the transmission / reception format as the communication mode (MOD [2:0] = 100b) and CKE [1:0] = 00b.
5	Set CCR2	Set the bit rate modulation function*1, the clock selection, and the bit rate.
6	Set CCR1	Set noise filter, communication pin status, parity check, and CTSn / RTSn function.
7	Set the I/O port functions	Set I/O port settings that allow use (on NMOS open-drain output pins and Hi-Z) of the SCLn and SDAn pin functions.
8	Set CFCLR, ICFCLR	Write 1 to the following bits and clear the corresponding flag. CFCLR.RDRFC, FERC, PERC, MFFC, ORERC, DFERC, DPERC, DCMFC, ERSC ICFCLR.IICSTIFC
9	Set CCR0 (TE, RE, TIE, RIE)	Set the TE and RE bits to 1. To enable interrupts, set the TE, TIE, RE and RIE bits to 1 with one instruction at the same time (for transmission and when the IICINTM bit is 1, clear the RIE bit). Setting the TE and RE bits to 1 makes the SCLn and SDAn pins functions available.
10	Initialization completed	—

Note: Set the CCR0.TE and RE bits to 0 or 1 at the same time.
Note 1. If you do not use the bit rate modulation function, you do not need to set it.

26.8.5 Operation in Master Transmission in Simple IIC Mode

Figure 26.89 and Figure 26.90 show examples of master transmission and Figure 26.91 shows an example flow of data transmission.

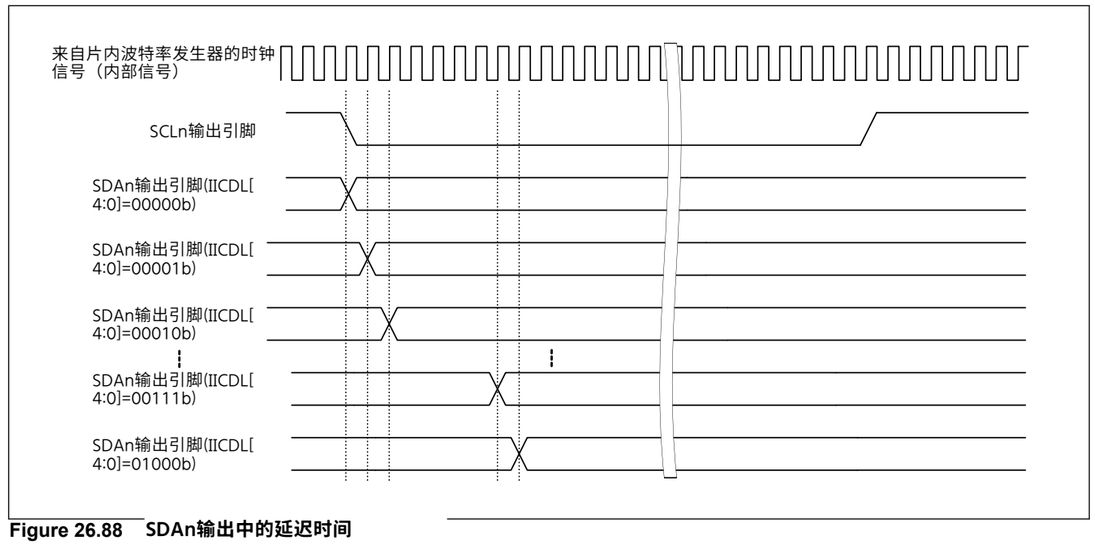


Figure 26.88 SDAn输出中的延迟时间

26.8.4 简单IIC模式下的SCI初始化

在传输数据之前，将初始值0x00写入CCR0并按照中所示的示例初始化接口
Table 26.38.

在对操作模式或传输格式进行任何更改之前，请务必将CCR0设置为其初始值。在简单IIC模式下，通信端口的开漏设置应在端口侧进行。

Table 26.38 简单IIC模式下SCI初始化示例流程

No.	步骤名称	Description
1	开始初始化	—
2	Set CCR0	将CCR0.TEIE、TIE、RIE、TE、RE设置为0。如果未更改初始设置，则可以跳过此步骤。
3	Set ICR	将IICSDAS[1:0]和IICSCLS[1:0]设置为11b。根据需要设置IICDL[4:0]和IICINTM。将IICACKT和IICCSC位设置为1。
4	Set CCR3	将发送接收格式设置为通信模式（MOD[2:0]=100b）和CKE[1:0]=00b。
5	Set CCR2	设置比特率调制功能*1、时钟选择和比特率。
6	Set CCR1	设置噪声滤波器、通信引脚状态、奇偶校验和CTSnRTSn功能。
7	设置IO端口功能	设置允许使用（在NMOS开漏输出引脚和Hi-Z上）SCLn和SDAn引脚功能。
8	Set CFCLR, ICFCLR	将1写入以下位并清除相应的标志。CFCLR.RDRFC、FERC、PERC、MFFC, ORERC, DFERC, DPERC, DCMFC, ERSC ICFCLR.IICSTIFC
9	设置CCR0（TE、RE、TIE、RIE）	将TE和RE位设置为1。要使能中断，请在一条指令同时将TE、TIE、RE和RIE位设置为1（用于传输且当IICINTM位为1时，清除RIE位）。将TE和RE位设置为1使SCLn和SDAn引脚功能可用。
10	初始化完成	—

Note: 同时将CCR0.TE和RE位设置为0或1。
注1.如果不使用码率调制功能，则无需设置。

26.8.5 简单IIC模式下的主传输操作

图26.89和图26.90显示了主机传输的示例，图26.91显示了数据传输的示例流程。

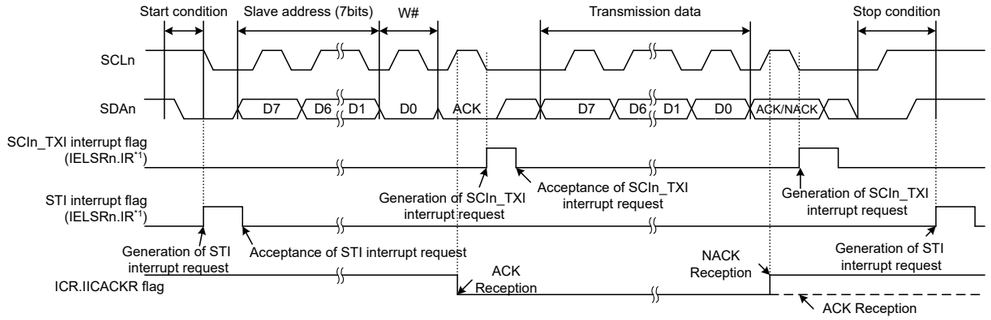
Figure 26.89 shows the operation example when ICR.IICINTM bit is 1 (use reception and transmission interrupts). In this case, you can start DMAC or DTC by SCIn_TXI interrupt. However, if use DMAC or DTC, ACK/NACK can not be confirmed. If you want to confirm ACK/NACK, prepare the transmit data by CPU.

In simple IIC mode, SCIn_TXI interrupt is generated when communication of one frame is completed. And it is not used SCIn_RXI interrupt in master transmission, so the CCR0.RIE set to 0.

See Table 26.43 for more information on the STI interrupt.

Figure 26.91 shows a flow chart in the case of ICR.IICINTM is 1 and address transmission by CPU and data transmission by DTC or DMAC. When 10-bit slave addresses are in use, steps [3] and [4] are repeated twice.

In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the SCIn_TXI interrupt request generation timing during clock synchronous transmission.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.89 Example 1 of operations for master transmission in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts (ICR.IICINTM = 1)

When the ICR.IICINTM bit is set to 0 (use ACK/NACK interrupts) during master transmission, the DTC or DMAC is activated by the ACK interrupt as the trigger and required number of data bytes are transmitted. When the NACK is received, error processing such as transmission stop and retransmission is performed using the NACK interrupt as the trigger.

To restart communication for some reason after writing data in the TDR register, use the following procedure:

1. Set the TE and RE bits in the CCR0 register to 0 to stop communication.
2. Set ICR.IICSCLS[1:0] and ICR.IICSDAS[1:0] bits to 11b, release the I^2C bus, and clear the generation of a condition.
3. If the RDRF flag in the CSR register is set to 1, the RDR register is read by dummy and the RDRF bit is set to 0.
4. Set the TE and RE bits in the CCR0 register to 1 and start the next communication.

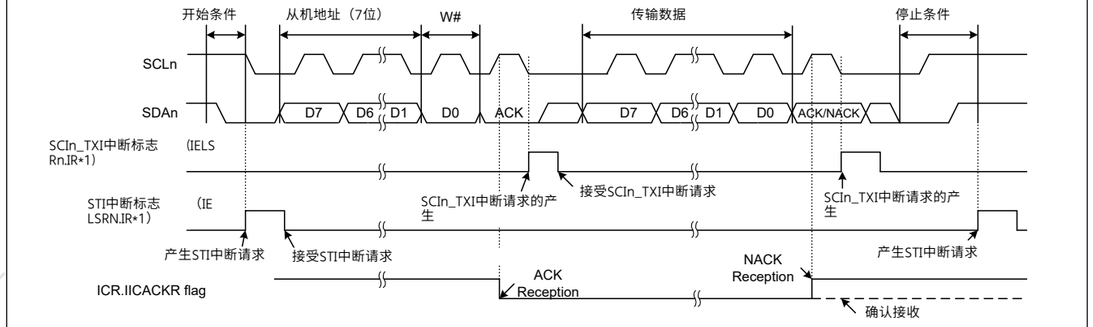
图26.89显示了ICR.IICINTM位为1时的操作示例（使用接收和发送中断）。在这种情况下，您可以通过SCIn_TXI中断启动DMAC或DTC。但是，如果使用DMAC或DTC，则无法确认ACKNACK。如果要确认ACKNACK，请通过CPU准备发送数据。

在简单IIC模式下，SCIn_TXI中断在一帧通信完成时产生。并且没有使用SCIn_RXI在主传输中断，因此CCR0.RIE设置为0。

有关STI中断的更多信息，请参见表26.43。

图26.91是ICR.IICINTM为1，CPU发送地址，DTC或DMAC发送数据时的流程图。当使用10位从地址时，步骤[3]和[4]重复两次。

在简单IIC模式下，与时钟同步传输期间的SCIn_TXI中断请求产生时序不同，当一帧的通信完成时产生发送数据空中断（SCIn_TXI）。



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.89 简单IIC模式下主机发送操作示例1，具有7位从机地址、发送中断和接收中断(ICR.IICINTM =1)

当ICR.IICINTM位在主机传输期间设置为0（使用ACKNACK中断）时，DTC或DMAC由ACK中断作为触发器激活并传输所需的数据字节数。接收到NACK时，以NACK中断为触发进行发送停止、重发等错误处理。

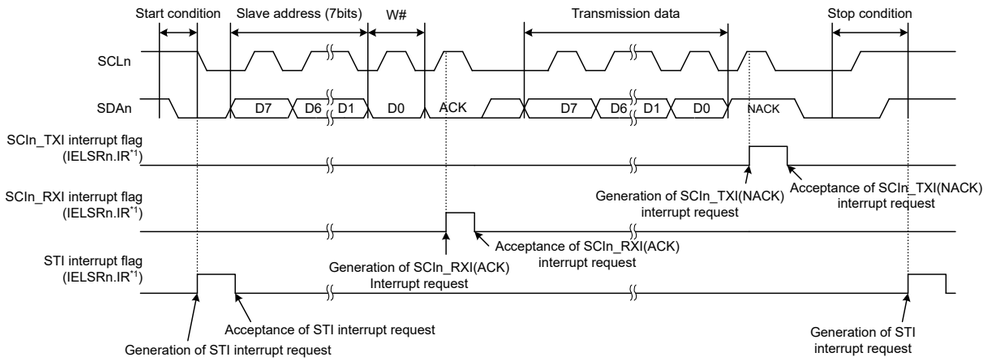
要在将数据写入TDR寄存器后出于某种原因重新启动通信，请使用以下过程：

1.将CCR0寄存器中的TE和RE位设置为0以停止通信。

2.将ICR.IICSCLS[1:0]和ICR.IICSDAS[1:0]位设置为11b，释放I2C总线，并清除条件的产生。

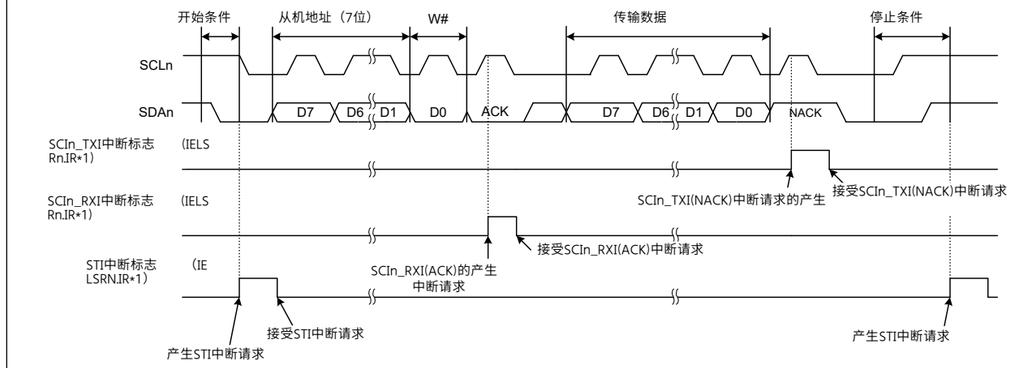
3.如果CSR寄存器中的RDRF标志设置为1，则RDR寄存器被dummy读取并且RDRF位设置为0。

4.将CCR0寄存器中的TE和RE位设置为1，开始下一次通信。



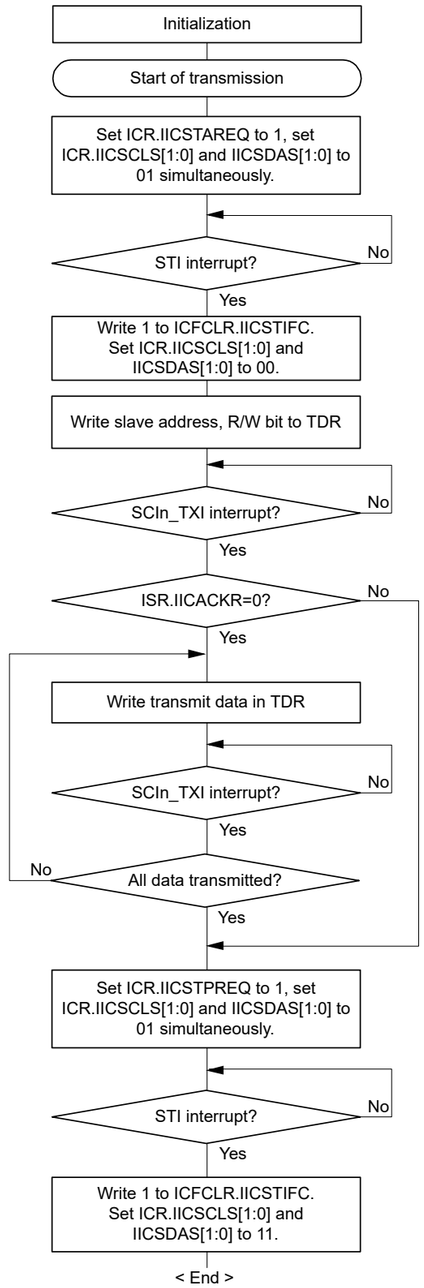
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.90 Example 2 of operations for master transmission in simple IIC mode with 7-bit slave addresses, ACK interrupts, and NACK interrupts (ICR.IICINTM = 0)



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.90 使用7位从地址、ACK中断和NACK中断(ICR.IICINTM=0)的简单IIC模式下主机传输操作示例2

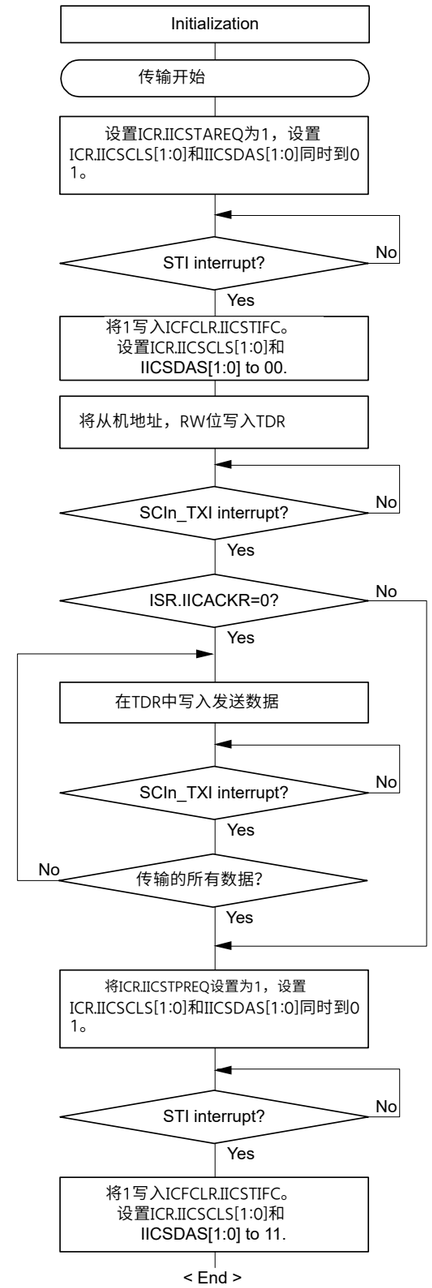


[1] Initialization for simple IIC mode
For transmission, set the CCR0.RIE to 0.
(SCIn_RXI and SCIn_ERI interrupts requests are disabled)
[2] Generate a start condition.
[3] Writing to TDR:
Writing the slave address and value for the R/W bit to TDR.
[4] Confirm ACK response from the slave device:
Check the ISR.IICACKR bit. If its value is 0, it is indicated that the slave device responded with ACK and operations proceed. If its value is 1, it is indicated that there was no response from a slave device so the next transition is to generation of the stop condition.
[5] Steps for continuing with serial transmission:
When transmission is to continue, write further transmit data to TDR. Except for the first data to be transmitted, a SCIn_TXI interrupt request can activate the DMAC or DTC to handle writing of data to TDR.
But it cannot be confirmed status of ACK or NACK in this case.
[6] Generation of a stop condition.

[3] [4] If 10-bits slave address are in use, processing from [3] to [4] is repeated twice.

Note: In simple IIC mode, the SCIn_TXI interrupt request is generated when communication is completed.

Figure 26.91 Example flow of master transmission in simple IIC mode with transmission interrupts and reception interrupts



[1]简单IIC模式的初始化对于传输，将CCR0.RIE设置为0。（SCIn_RXI和SCIn_ERI中断请求被禁用）[2]生成一个开始条件。[3]写入TDR：将RW位的从机地址和值写入到

TDR。[4]确认来自从设备的ACK响应：

检查ISR.IICACKR位。如果其值为0，则表明从设备响应ACK并继续操作。如果其值为1，则表明从设备没有响应，因此下一个转换是生成停止条件。[5]继续串行传输的步骤：

当要继续传输时，将进一步的传输数据写入TDR。除了要发送的第一个数据外，SCIn_TXI中断请求可以激活DMAC或

DTC处理将数据写入TDR。
但是在这种情况下不能确认ACK或NACK的状态。[6]生成停止条件。

[3] [4] 如果使用10位从地址，则从[3]到[4]的处理重复两次。

Note: 在简单IIC模式下，通信完成时会产生SCIn_TXI中断请求。

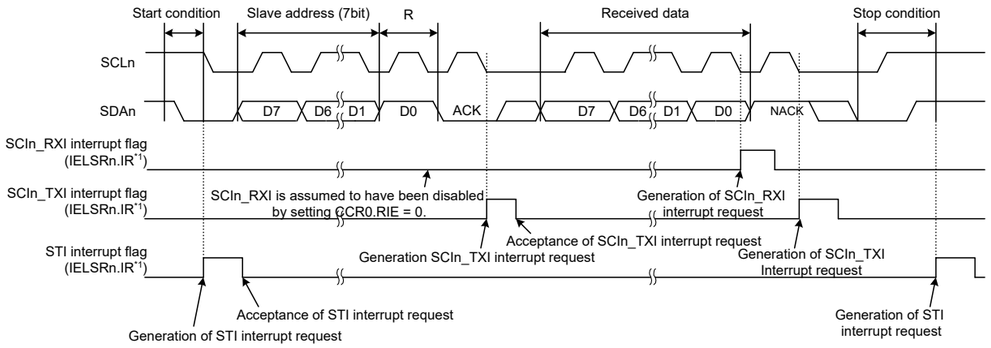
Figure 26.91 带有发送中断和接收中断的简单IIC模式下的主机发送示例流程

26.8.6 Master Reception in Simple IIC Mode

Figure 26.92 shows an example operation in simple IIC mode master reception and Figure 26.94 shows an example flow of master reception.

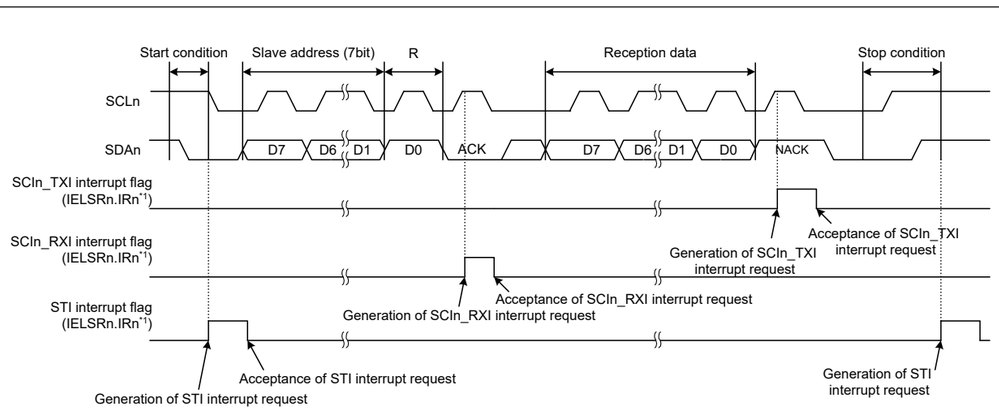
The value of the ICR.IICINTM bit is assumed to be 1 (use reception and transmission interrupts) and 0 (use ACK and NACK interrupts).

In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the SCIn_TXI interrupt request generation timing during clock synchronous transmission.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.92 Example operations for master reception in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts (ICR.IICINTM = 1)



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

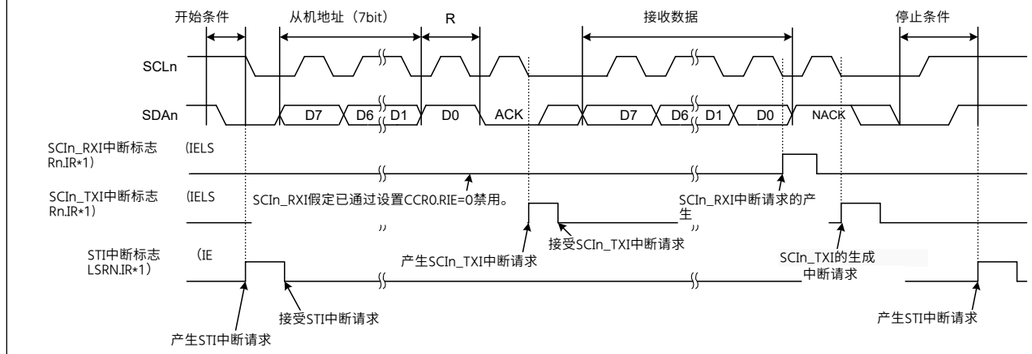
Figure 26.93 Example of Operations for Master Reception in Simple IIC Mode (7bit Slave address, ACK and NACK interrupt in use (ICR.IICINTM = 0))

26.8.6 简单IIC模式下的主接收

图26.92显示了简单IIC模式主机接收的示例操作，图26.94显示了主机接收的示例流程。

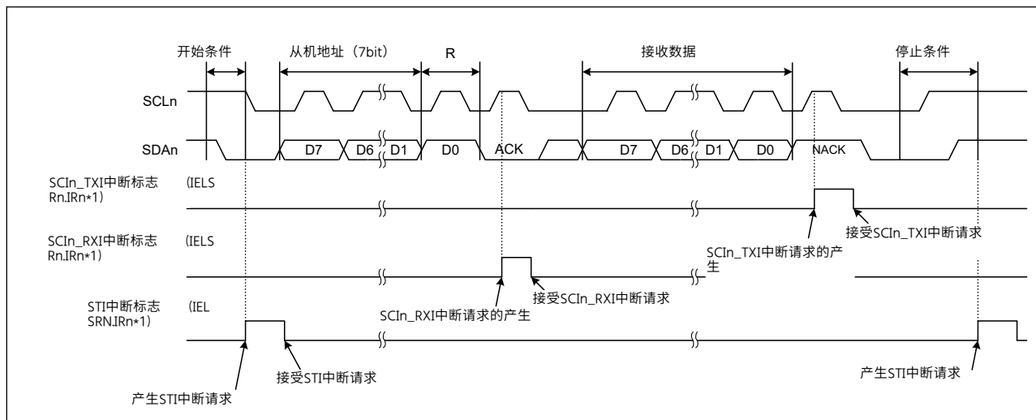
ICR.IICINTM位的值假定为1（使用接收和发送中断）和0（使用ACK和
NACK interrupts).

在简单IIC模式下，与时钟同步传输期间的SCIn_TXI中断请求产生时序不同，当一帧的通信完成时产生发送数据空中断（SCIn_TXI）。



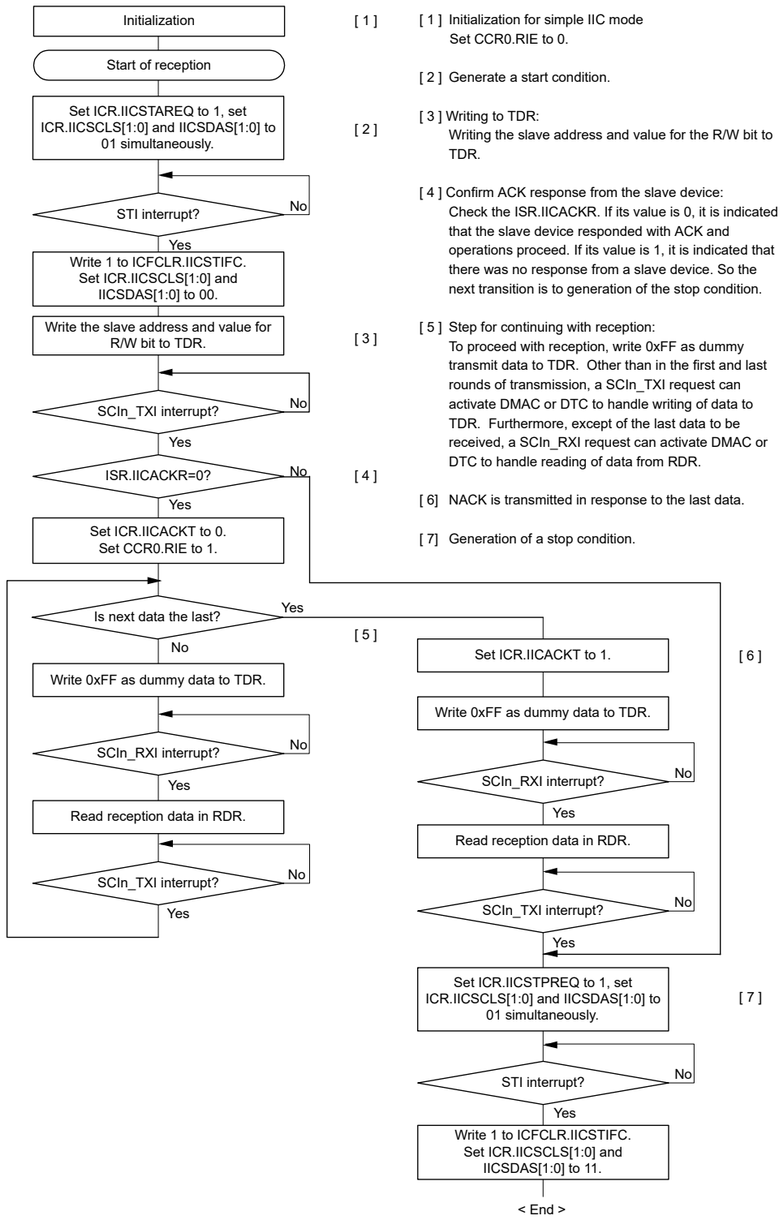
注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.92 简单IIC模式下主机接收的示例操作，具有7位从机地址、发送中断和接收中断(ICR.IICINTM=1)



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 26.93 简单IIC模式下主机接收的操作示例（7位从机地址、ACK和正在使用NACK中断(ICR.IICINTM=0)）



[1] Initialization for simple IIC mode
Set CCR0.RIE to 0.

[2] Generate a start condition.

[3] Writing to TDR:
Writing the slave address and value for the R/W bit to TDR.

[4] Confirm ACK response from the slave device:
Check the ISR.IICACKR. If its value is 0, it is indicated that the slave device responded with ACK and operations proceed. If its value is 1, it is indicated that there was no response from a slave device. So the next transition is to generation of the stop condition.

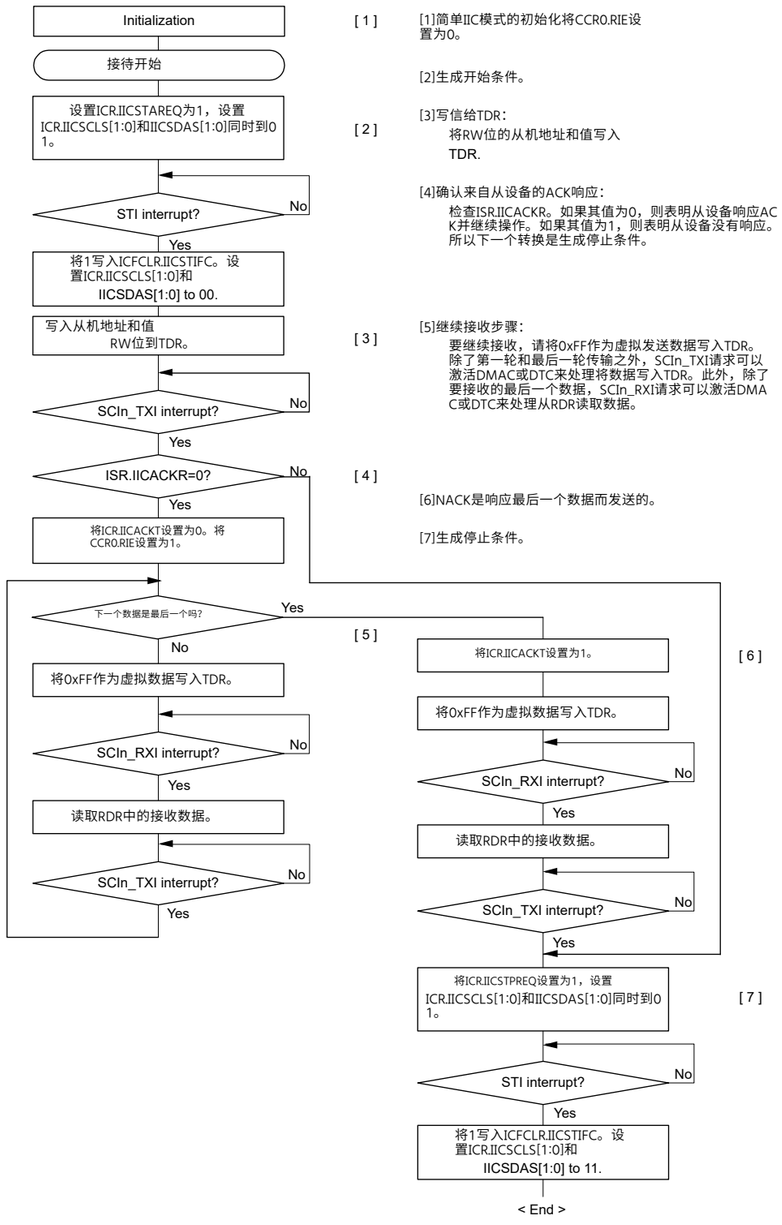
[5] Step for continuing with reception:
To proceed with reception, write 0xFF as dummy transmit data to TDR. Other than in the first and last rounds of transmission, a SCIn_TXI request can activate DMAC or DTC to handle writing of data to TDR. Furthermore, except of the last data to be received, a SCIn_RXI request can activate DMAC or DTC to handle reading of data from RDR.

[6] NACK is transmitted in response to the last data.

[7] Generation of a stop condition.

Note: In simple IIC mode, the SCIn_TXI interrupt request is generated when communication is completed.

Figure 26.94 Example flow of master reception in simple IIC mode with transmission interrupts and reception interrupts (ICR.IICINTM = 1)



[1]简单IIC模式的初始化将CCR0.RIE设置为0。

[2]生成开始条件。

[3]写信给TDR:
将RW位的从机地址和值写入TDR.

[4]确认来自从设备的ACK响应:
检查ISR.IICACKR。如果其值为0，则表明从设备响应ACK并继续操作。如果其值为1，则表明从设备没有响应。所以下一个转换是生成停止条件。

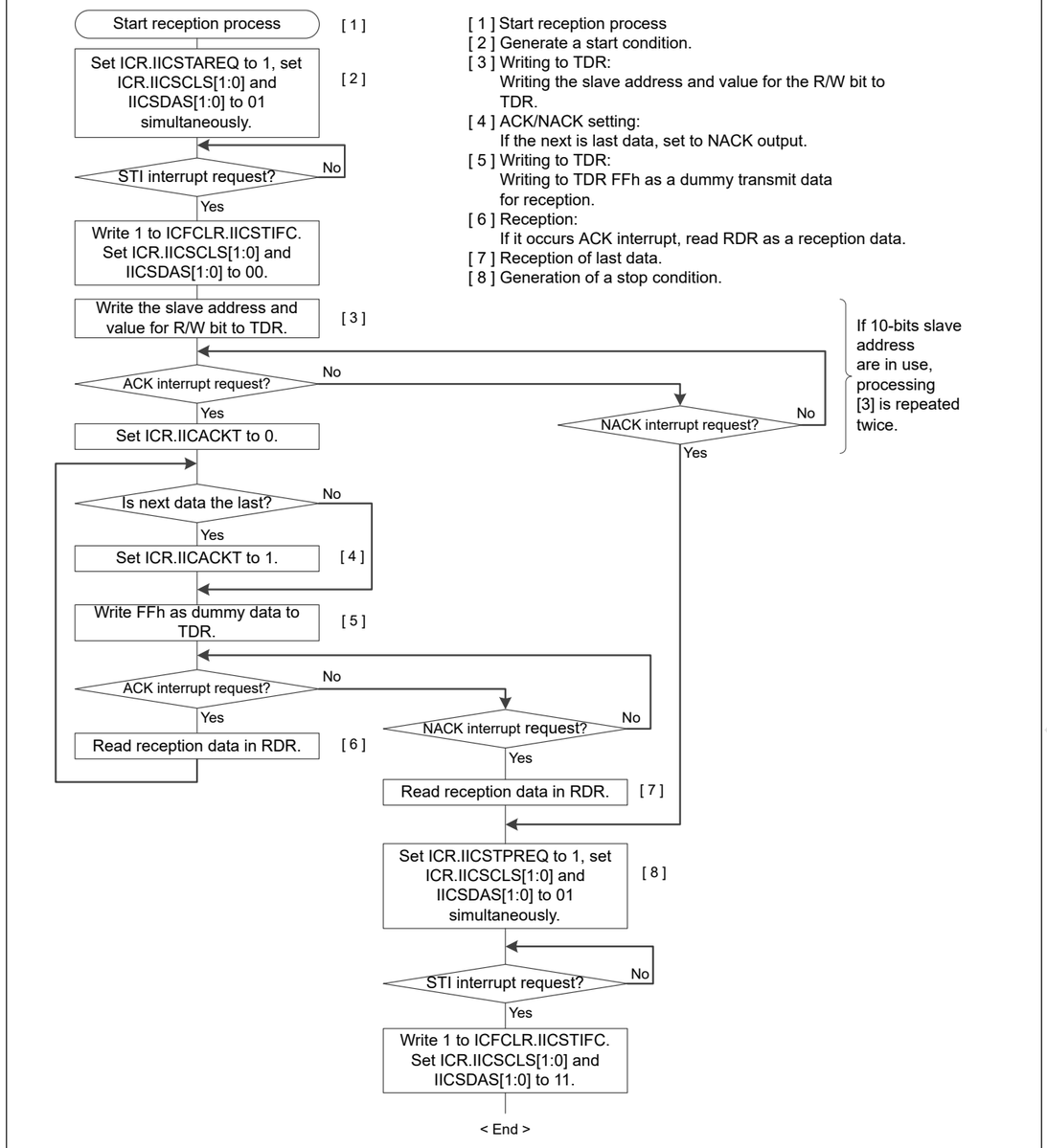
[5]继续接收步骤:
要继续接收，请将0xFF作为虚拟发送数据写入TDR。除了第一轮和最后一轮传输之外，SCIn_TXI请求可以激活DMAC或DTC来处理将数据写入TDR。此外，除了要接收的最后一个数据，SCIn_RXI请求可以激活DMAC或DTC来处理从RDR读取数据。

[6]NACK是响应最后一个数据而发送的。

[7]生成停止条件。

Note: 在简单IIC模式下，通信完成时会产生SCIn_TXI中断请求。

Figure 26.94 带有发送中断和接收中断的简单IIC模式下的主机接收示例流程(ICR.IICINTM=1)



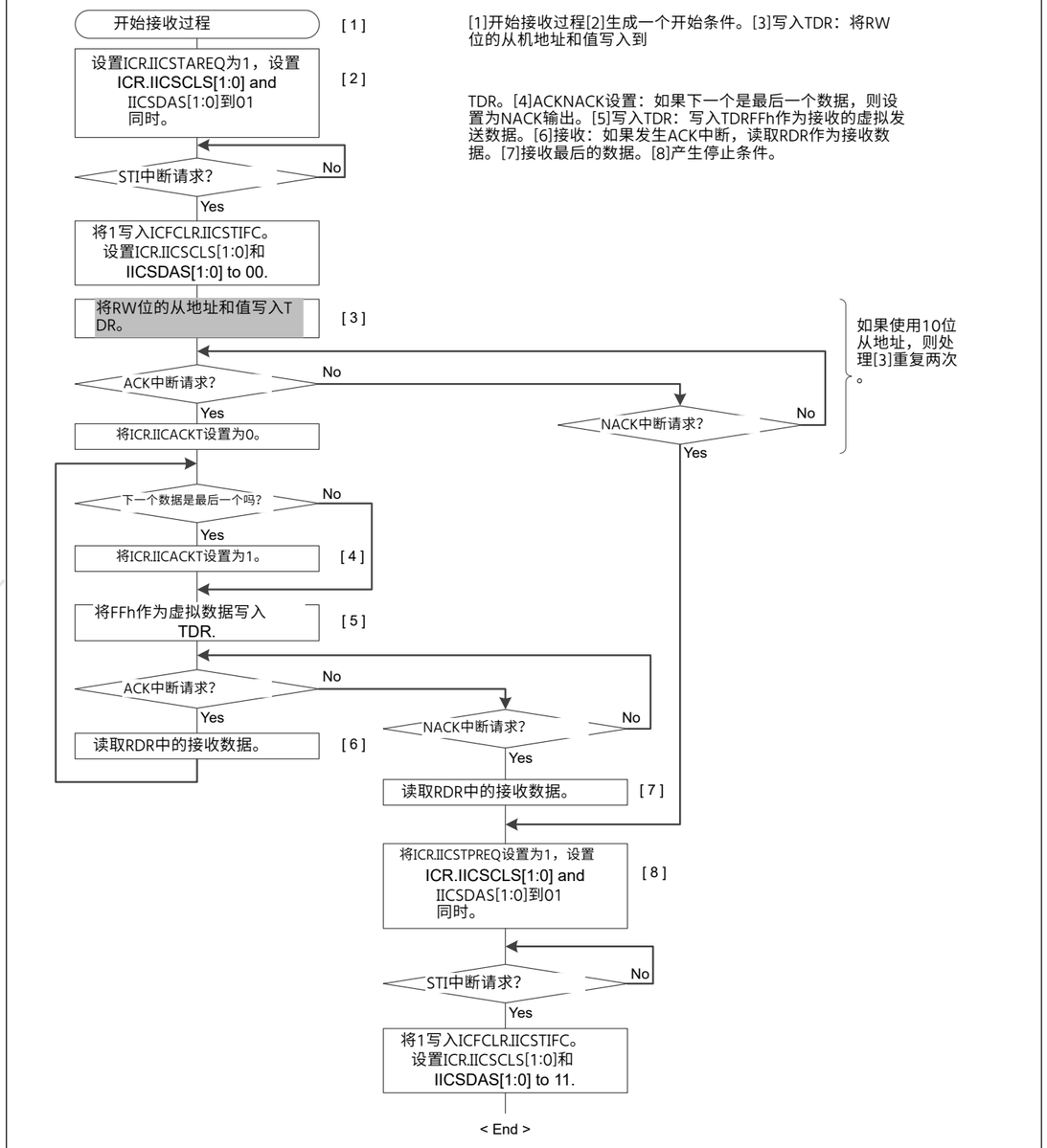
[1] Start reception process
[2] Generate a start condition.
[3] Writing to TDR:
Writing the slave address and value for the R/W bit to TDR.
[4] ACK/NACK setting:
If the next is last data, set to NACK output.
[5] Writing to TDR:
Writing to TDR FFh as a dummy transmit data for reception.
[6] Reception:
If it occurs ACK interrupt, read RDR as a reception data.
[7] Reception of last data.
[8] Generation of a stop condition.

Figure 26.95 Example flow of master reception in simple IIC mode with ACK Interrupts and NACK Interrupts (ICR.IICINTM = 0)

26.9 Operation in Simple SPI Mode

As an extended function, the SCI supports a simple SPI mode that handles transfer among one or multiple master devices and multiple slave devices.

Using the settings for Simple SPI mode setting (CCR3.MOD[2:0] bit = 011b) and setting the CCR0.SSE bit to 1 place the SCI in simple SPI mode. However, the SSn pin function on the master side is not required for connection of the device used



[1]开始接收过程[2]生成一个开始条件。[3]写入TDR：将RW位的从机地址和值写入到

TDR。[4]ACKNACK设置：如果下一个是最后一个数据，则设置为NACK输出。[5]写入TDR：写入TDRFFh作为接收的虚拟发送数据。[6]接收：如果发生ACK中断，读取RDR作为接收数据。[7]接收最后的数据。[8]产生停止条件。

Figure 26.95 带有ACK中断和NACK中断(ICR.IICINTM=0)的简单IIC模式下主机接收示例流程

26.9 简单SPI模式下的操作

作为一项扩展功能，SCI支持简单的SPI模式，可处理一个或多个主设备与多个从设备之间的传输。

使用简单SPI模式设置(CCR3.MOD[2:0]位=011b)并将CCR0.SSE位设置为1，将SCI处于简单SPI模式。但是，主机侧的SSn引脚功能不需要连接所使用的设备

as the master in simple SPI mode when the configuration only has a single master. Therefore, set the CCR0.SSE bit to 0 in such cases.

Figure 26.96 shows an example of connections for simple SPI mode. Control a general port pin to produce the SSn output signal from the master.

In simple SPI mode, data is transferred in synchronization with clock pulses in the same way as in clock synchronous mode. One character of data for transfer consists of 8 bits of data, and parity bits cannot be appended. The data can be inverted by setting the CCR3.SINV bit to 1.

Because the receiver and transmitter are independent of each other within the SCI module, full-duplex communications are possible, with a shared clock signal. Additionally, because both the transmitter and receiver have a buffered structure, writing the next transmit data while transmission is in progress and reading previously received data while reception is in progress are both possible. This enables continuous transfer.

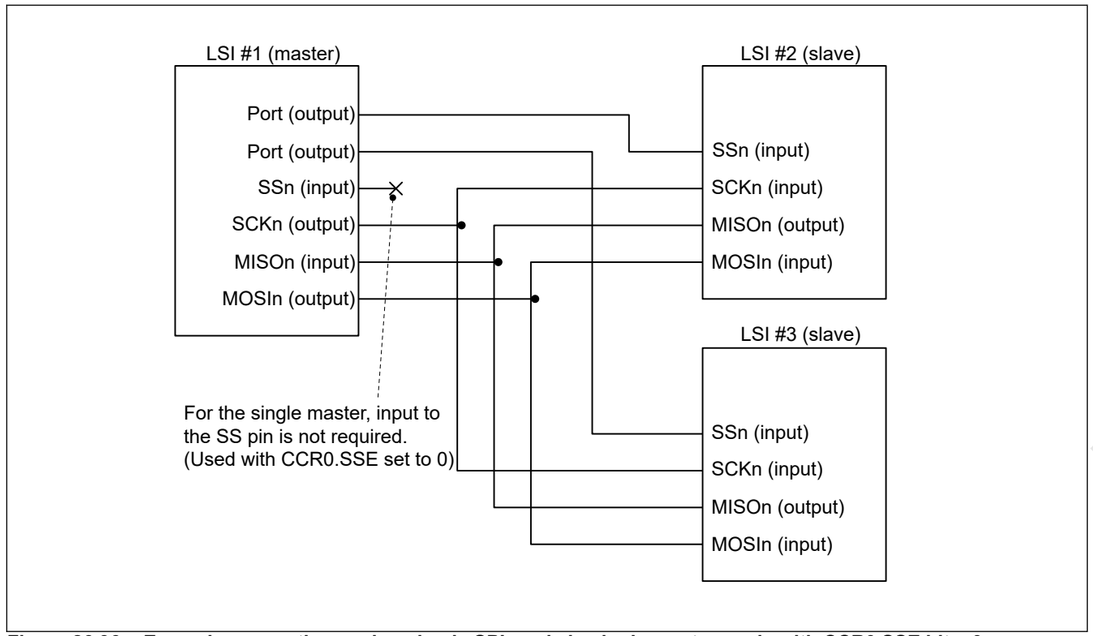


Figure 26.96 Example connections using simple SPI mode in single master mode with CCR0.SSE bit = 0

26.9.1 States of Pins in Master and Slave Modes

The direction (input or output) of pins for the simple SPI mode interface differs according to whether the device is a master (CCR3.CKE[1:0] = 00b or 01b) or slave (CCR3.CKE[1:0] = 10b or 11b).

Table 26.39 lists the relationship between the pin states, mode, and level on the SSn pin.

Table 26.39 States of pins by mode and input level on SSn pin

Mode	Input on SSn pin	State of MOSIn pin	State of MISOn pin	State of SCKn pin
Master mode*1	High level (transfer can proceed)	Output for data transmission*2	Input for received data	Clock output*3
	Low level (transfer cannot proceed)	High-impedance	Input for received data (but disabled)	High-impedance
Slave mode	High level (transfer cannot proceed)	Input for received data (but disabled)	High-impedance	Clock input (but disabled)
	Low level (transfer can proceed)	Input for received data	Output for data transmission	Clock input

Note 1. When there is only a single master (CCR0.SSE = 0), transfer is possible regardless of the input level on the SSn pin. This is equivalent to input of a high level on the SSn pin. The SSn pin is not used and is available for other purposes.

当配置只有一个主机时，作为简单SPI模式的主机。因此，在这种情况下，将CCR0.SSE位设置为0。

图26.96显示了简单SPI模式的连接示例。控制一个通用端口引脚以产生来自主机的SSn输出信号。

在简单SPI模式下，数据与时钟脉冲同步传输，方式与时钟同步模式相同。1个字符的传输数据由8位数据组成，不能附加奇偶校验位。可以通过将CCR3.SINV位设置为1来反转数据。

由于接收器和发送器在SCI模块中彼此独立，因此可以使用共享时钟信号进行全双工通信。此外，由于发送器和接收器都具有缓冲结构，因此在发送过程中写入下一个发送数据和在接收过程中读取先前接收到的数据都是可能的。这使得连续传输成为可能。

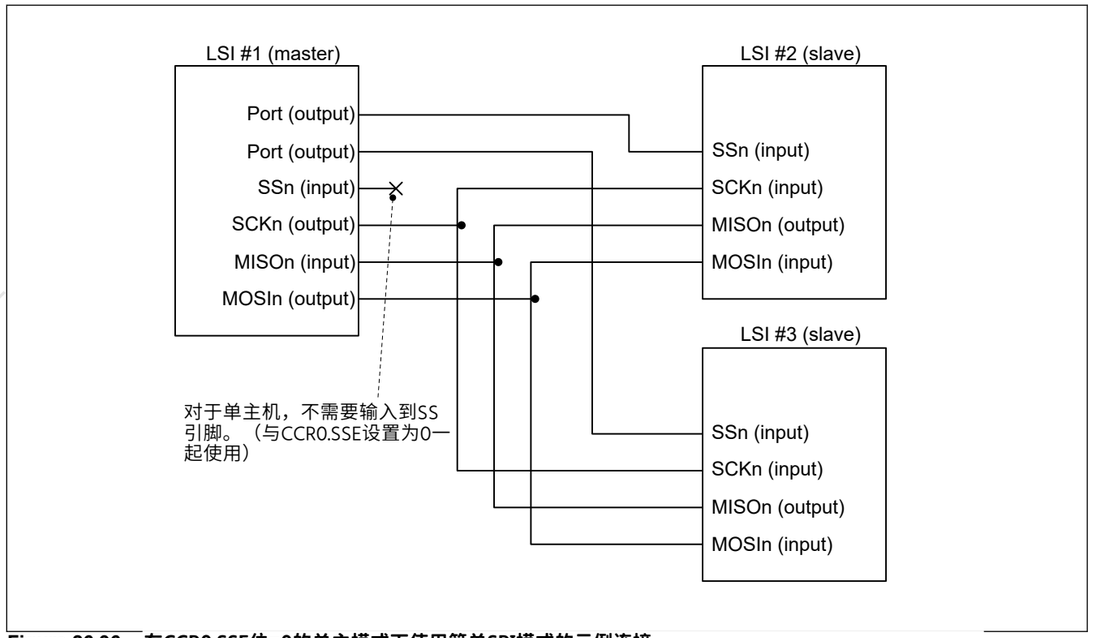


Figure 26.96 在CCR0.SSE位=0的单主模式下使用简单SPI模式的示例连接

26.9.1 主从模式下的引脚状态

简单SPI模式接口的引脚方向（输入或输出）根据设备是主设备（CCR3.CKE[1:0]=00b或01b）还是从设备（CCR3.CKE[1:0]=10b或11b)。

表26.39列出了SSn引脚上的引脚状态、模式和电平之间的关系。

Table 26.39 SSn引脚上的模式和输入电平的引脚状态

Mode	SSn引脚上的输入	MOSIn管脚状态	MISon引脚的状态	SCKn引脚状态
主模式*1	高电平（可以进行转移）	数据传输用输出*2	接收数据的输入	时钟输出*3
	低电平（传输无法进行）	High-impedance	接收数据的输入（但禁用）	High-impedance
从机模式	高电平（传输无法进行）	接收数据的输入（但禁用）	High-impedance	时钟输入（但禁用）
	低电平（可以继续传输）	接收数据的输入	数据传输输出	时钟输入

注1.当只有一个主机(CCR0.SSE=0)时，无论SSn引脚上的输入电平如何，都可以进行传输。这相当于在SSn引脚上输入高电平。SSn引脚未使用，可用于其他用途。

Note 2. The MOSIn pin output is in the high-impedance state when serial transmission is disabled (CCR0.TE bit = 0).
Note 3. The SCKn pin output is in the high-impedance state when serial transmission is disabled (CCR0.TE = 0 and CCR0.RE = 0) in a multi-master configuration (CCR0.SSE = 1).

26.9.2 SS Function in Master Mode

Setting the CKE[1:0] bits in the CCR3 to 00b or 01b selects master mode operation. The SSn pin is not used in single-master configurations (CCR0.SSE = 0), so transmission or reception can proceed regardless of the value of the SSn pin.

When the level on the SSn pin is high in a multi-master configuration (CCR0.SSE = 1), a master device outputs clock signals from the SCKn pin before starting transmission or reception to indicate that there are no other masters or another master is performing reception or transmission.

When the level on the SSn pin is low in a multi-master configuration (CCR0.SSE = 1), there are other masters, and a transmission or reception is in progress. The MOSIn output and SCKn pins are placed in the high-impedance state and starting transmission or reception is not possible. In addition, the value of the CSR.MFF bit is 1, indicating a mode fault error. In a multi-master configuration, start error processing by reading CSR.MFF flag. If a mode fault error occurs while transmission or reception is in progress, transmission or reception does not stop, but the MOSIn and SCKn outputs are in the high-impedance state after completion of the transfer.

When the SSn pin input becomes high level, the SCKn pin outputs a clock signal and the MOSIn outputs data. Even if the SCKn pin and the MOSIn pin are in the high impedance state, internal transmission or reception operation continues, but it stops after transmission or reception of a single character is complete. In this case, any of SCIn_TXI, SCIn_RXI, and SCIn_TEI interrupts occurs.

Use a general port pin to produce the SS output signal from the master.

26.9.3 SS Function in Slave Mode

Setting the CCR3.CKE[1:0] bits to 10b or 11b selects slave operation. When the SSn pin is high, the MISOn output pin is in the high-impedance state and clock input through the SCKn pin is ignored. When the SSn pin is low, clock input through the SCKn pin is valid and transmission or reception can proceed.

If the input on the SSn pin changes from low to high during transmission or reception, the MISOn output pin is placed in the high-impedance state. Transmission / reception operation is immediately suspended. If the transmission is in progress, the CSR.TEND flag will not be set, a transmit end interrupt will not be output, and an abnormal stop status will occur. So, do not negate the SSn pin during slave transmission / reception. If an abnormal stop occurs, set CCR0.RE and CCR0.TE to 0 to stop transmission / reception. To resume transmission / reception, set CCR0.RE and CCR0.TE to 1 after at least TCLK × 3 cycles + PCLK × 3 cycles.

26.9.4 Relationship between Clock and Transmit/Receive Data

The CPOL and CPHA bits in the CCR3 register can be used to set up the clock for use in transmission and reception in four different ways. The relation between the clock signal and the transmission and reception of data is shown in Figure 26.97. The relation is the same for both master and slave operation. This is the same as when the level on the SSn pin is high.

注2.当串行传输被禁用（CCR0.TE位=0）时，MOSIn引脚输出处于高阻抗状态。
注3.在多主机配置(CCR0.SSE=1)中禁用串行传输(CCR0.TE=0和CCR0.RE=0)时，SCKn引脚输出处于高阻抗状态。

26.9.2 主控模式下的SS功能

将CCR3中的CKE[1:0]位设置为00b或01b可选择主模式操作。SSn引脚不用于单主机配置(CCR0.SSE=0)，因此无论SSn引脚的值如何，都可以继续发送或接收。

在多主机配置（CCR0.SSE=1）中，当SSn引脚上的电平为高电平时，主机在开始发送或接收之前从SCKn引脚输出时钟信号，以指示没有其他主机或另一个主机在进行接收或发送。

在多主机配置（CCR0.SSE=1）中，当SSn引脚上的电平为低电平时，存在其他主机，并且正在进行发送或接收。MOSIn输出和SCKn引脚处于高阻状态，无法开始发送或接收。此外，CSR.MFF位的值为1，表示模式故障错误。在多主机配置中，通过读取CSR.MFF标志开始错误处理。如果在发送或接收过程中发生模式故障错误，则发送或接收不会停止，但MOSIn和SCKn输出在传输完成后处于高阻抗状态。

当SSn引脚输入变为高电平时，SCKn引脚输出时钟信号，MOSIn输出数据。即使SCKn引脚和MOSIn引脚处于高阻抗状态，内部发送或接收操作仍继续，但在单个字符的发送或接收完成后停止。在这种情况下，任何SCIn_TXI、SCIn_RXI和SCIn_TEI中断都会发生。

使用通用端口引脚从主机产生SS输出信号。

26.9.3 从模式下的SS功能

将CCR3.CKE[1:0]位设置为10b或11b选择从机操作。当SSn引脚为高电平时，MIOn输出引脚处于高阻状态，通过SCKn引脚输入的时钟被忽略。当SSn引脚为低电平时，通过SCKn引脚输入的时钟有效，可以进行发送或接收。

如果SSn引脚上的输入在发送或接收期间从低电平变为高电平，则MISOn输出引脚处于高阻抗状态。发送接收操作立即暂停。如果正在发送，则不会设置CSR.TEND标志，不会输出发送结束中断，并会出现异常停止状态。因此，在从机发送接收期间不要否定SSn引脚。如果发生异常停止，请将CCR0.RE和CCR0.TE设置为0以停止发送接收。要恢复发送接收，至少在TCLK×3个周期+PCLK×3个周期后将CCR0.RE和CCR0.TE设置为1。

26.9.4 时钟与发送接收数据的关系

CCR3寄存器中的CPOL和CPHA位可用于以四种不同的方式设置用于发送和接收的时钟。时钟信号与数据收发的关系如图26.97所示。主从操作的关系是相同的。这与SSn引脚上的电平为高电平时相同。

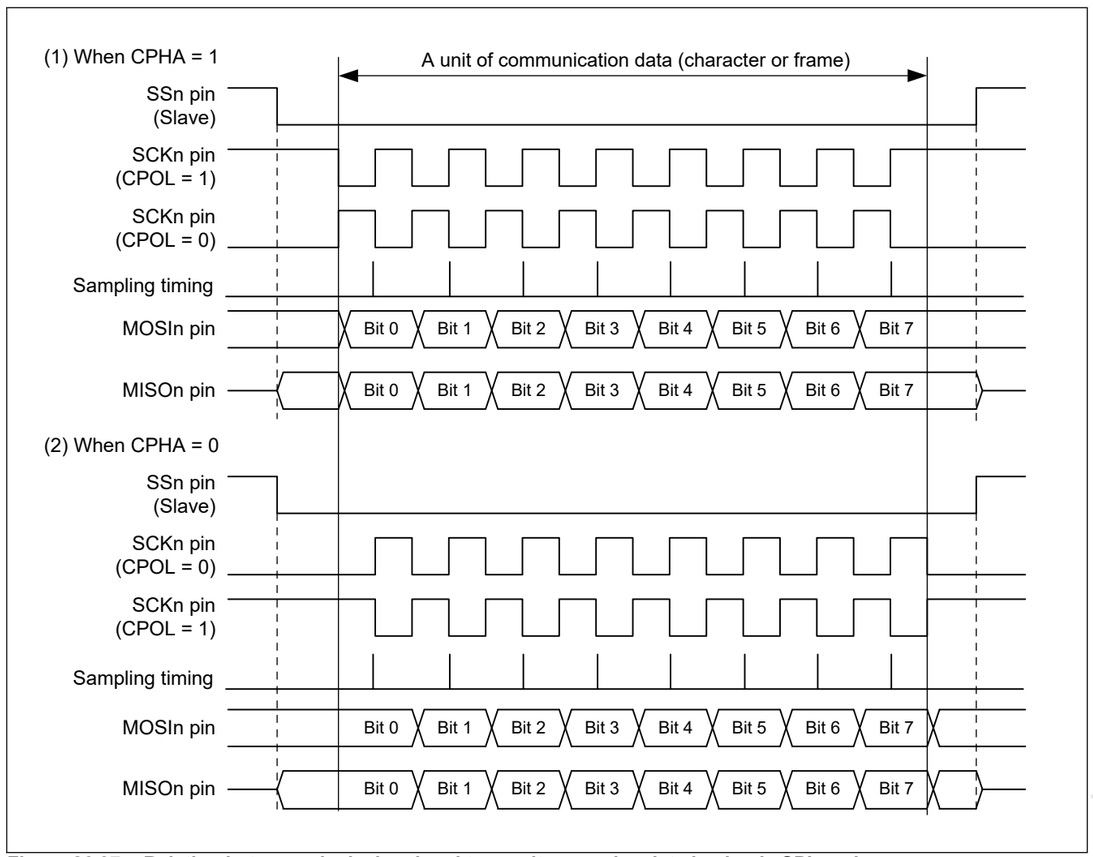


Figure 26.97 Relation between clock signal and transmit or receive data in simple SPI mode

26.9.5 SCI Initialization in Simple SPI Mode

Initialization in simple SPI mode is the same as in clock synchronous mode. See section 26.6.3. SCI Initialization in Clock Synchronous Mode for an example initialization flow. The CPOL and CPHA bits in the CCR3 register must be set to ensure that the clock signal is suitable for both master and slave devices.

Always initialize the CCR0 register before making any changes to the operating mode or transfer format.

Note: Only the RE bit is set to 0. The CSR.ORER, FER, PER, and RDR flags are not initialized.

Changing the value of the TE bit from 1 to 0 or from 0 to 1 when the TIE bit in the CCR0 register is 1 at the same time, leads to the generation of a transmit data empty interrupt (SCIn_TXI).

26.9.6 Transmission and Reception of Serial Data in Simple SPI Mode

In master operation, ensure that the SSn pin of the slave device on the other side of the transfer is at the low level before starting the transfer and at the high level on completion of the transfer. In multiple master operation with CCR0.SSE = 1 even in master mode, a mode fault error will occur if the SSn pin goes low. Therefore, make sure that no mode fault error has occurred before starting communication, and start communication, and make sure that no mode fault error has occurred even after communication ends. If a mode fault error has occurred, communication may be incomplete, so measures such as retransmission are required. Otherwise, the procedures are the same as in clock synchronous mode.

In slave mode, it operates according to the SSn pin input level. Other steps are the same as those of clock synchronous mode.

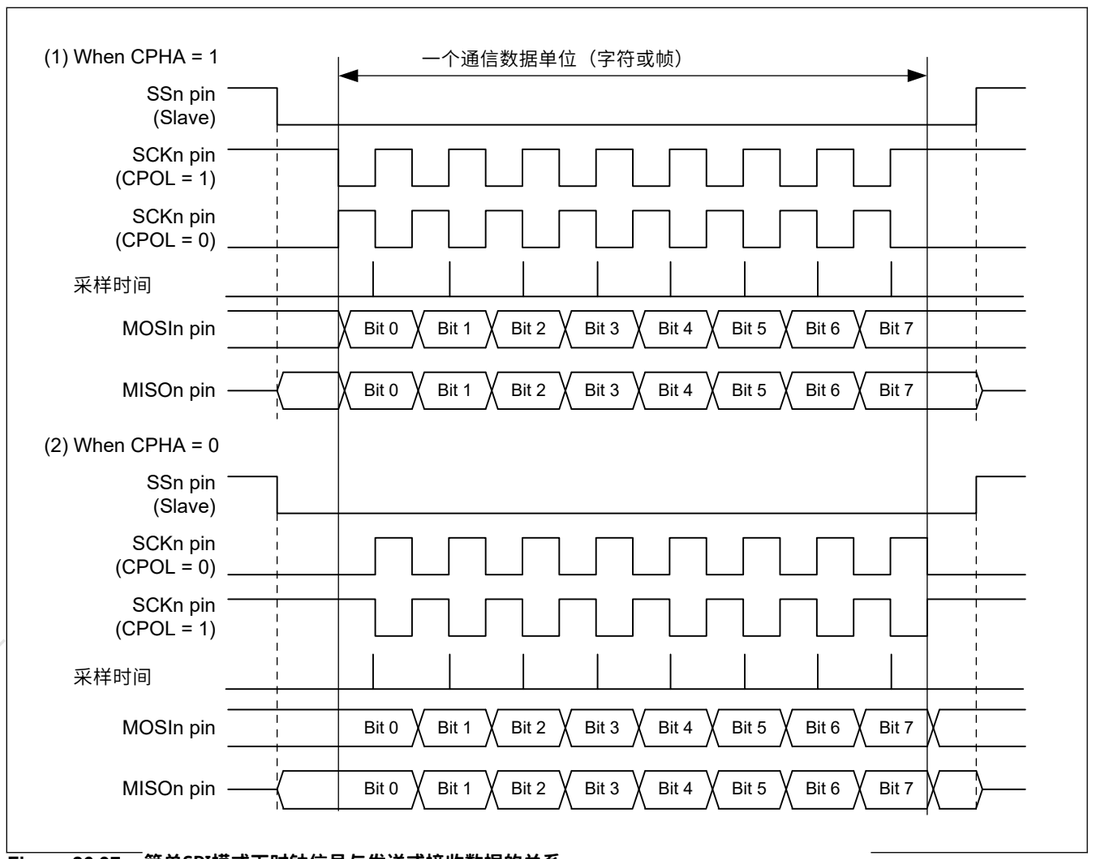


Figure 26.97 简单SPI模式下时钟信号与发送或接收数据的关系

26.9.5 简单SPI模式下的SCI初始化

简单SPI模式的初始化与时钟同步模式相同。请参阅第26.6.3节。时钟中的SCI初始化
示例初始化流程的同步模式。必须设置CCR3寄存器中的CPOL和CPHA位，以确保时钟信号适用于主设备和从设备
。

在对操作模式或传输格式进行任何更改之前，始终初始化CCR0寄存器。

Note: 只有RE位设置为0。CSR.ORER、FER、PER和RDR标志未初始化。

当CCR0寄存器中的TIE位同时为1时，将TE位的值从1更改为0或从0更改为1，会导致产生发送数据空中断（SC
In_TXI）。

26.9.6 简单SPI模式下串行数据的发送和接收

在主机操作中，确保传输另一侧的从设备的SSn管脚在开始传输前为低电平，在传输完成时为高电平。即使在主
机模式下，在CCR0.SSE=1的多主机操作中，如果SSn引脚变为低电平，也会发生模式故障错误。因此，在开始通
讯之前确保没有发生模式故障错误，然后开始通讯，并确保即使在通讯结束后也没有发生模式故障错误。如果发
生模式故障错误，可能会导致通信不完整，因此需要采取重传等措施。否则，过程与时钟同步模式相同。

在从机模式下，它根据SSn引脚输入电平进行操作。其他步骤与时钟同步模式相同。

26.9.7 Reception Sampling Timing Adjustment Function in Simple SPI Mode with internal clock used

The reception sampling timing adjustment function in simple SPI mode is the same as the reception sampling timing adjustment function in clock synchronous mode. For the description of operation, see section 26.6.7. Reception Sampling Timing Adjustment Function in Clock Synchronous Mode with internal clock used.

26.10 Bit Rate Modulation Function

Using the bit rate modulation function, the bit rate can be evenly corrected using the number specified in the MDDR register among 256 clock cycles of internal clocks which is selected by the CKS[1:0] bits in CCR2.

Figure 26.98 shows an example where the PCLK is selected in the CKS[1:0] bits in CCR2, the BRR bit is set to 0, and the MDDR is set to 160 in asynchronous mode. In this example, the cycle of the base clock is evenly corrected (256/160) and the bit rate is also corrected (160/256).

Note: Enabling an internal clock causes bias, and expansion and contraction are generated in the pulse width of the internal base clock.

Do not use this function in clock synchronous mode, simple SPI mode, Smart Card Interface mode, Manchester mode and Simple LIN mode.

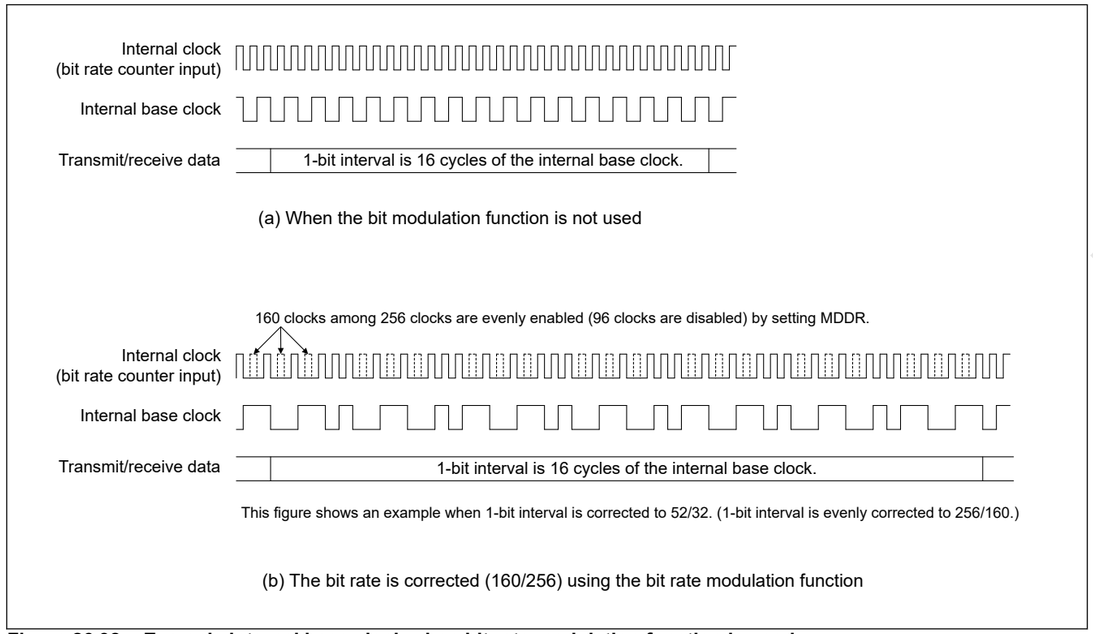


Figure 26.98 Example internal base clock when bit rate modulation function is used

26.11 Simple LIN mode

As an extended function of the SCI, the SCI supports the serial communication protocol (Figure 26.99) consisting of a Start Frame and an Information Frame as Simple LIN. Simple LIN mode is enabled by the CCR3.MOD[2:0] = 110b. Since the simple LIN mode uses the same circuit as the asynchronous mode for transmission / reception control other than Break Field, the basic communication settings required for the asynchronous mode are also required for the simple LIN mode.

(For the setting value when using simple LIN, refer to the explanation in section 26.2. Register Descriptions. In particular, note that CCR3.RXDESEL needs to be changed from the initial value and set to 1.)

The Start Frame consists of a Break Field, Control Field 0, and Control Field 1. The Information Frame can be configured with some Data Fields, a CRC16 Upper Field, and a CRC16 Lower Field.

26.9.7 使用内部时钟的简单SPI模式下的接收采样时序调整功能

简单SPI模式下的接收采样时序调整功能与时钟同步模式下的接收采样时序调整功能相同。操作说明见26.6.7节。使用内部时钟的时钟同步模式下的接收采样定时调整功能。

26.10 比特率调制功能

使用比特率调制功能，可以在由CCR2中的CKS[1:0]位选择的256个内部时钟周期中，使用MDDR寄存器中指定的数量均匀地校正比特率。

图26.98显示了一个示例，其中在CCR2的CKS[1:0]位中选择PCLK，BRR位设置为0，并且在异步模式下MDDR设置为160。在这个例子中，基本时钟的周期被均匀地校正（256160）并且比特率也被校正（160256）。

Note: 启用内部时钟会导致偏差，并且会在内部基本时钟的脉冲宽度中产生扩展和收缩。

不要在时钟同步模式、简单SPI模式、智能卡接口模式、曼彻斯特模式和简单的LIN模式。

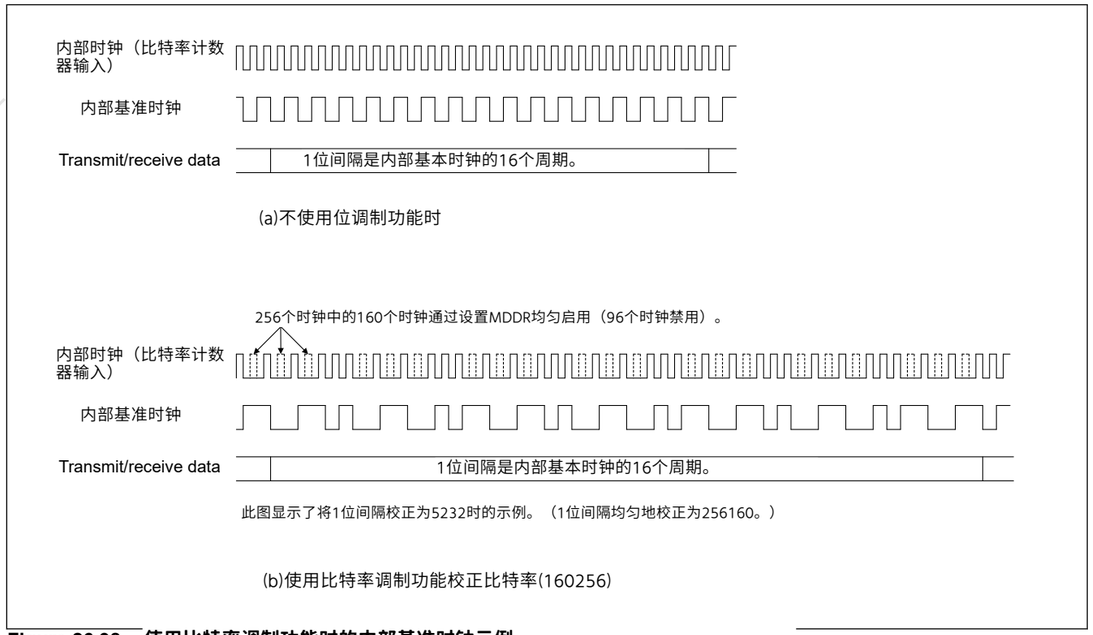


Figure 26.98 使用比特率调制功能时的内部基准时钟示例

26.11 简单LIN模式

作为SCI的扩展功能，SCI支持由Start组成的串行通信协议（图26.99）框架和信息框架作为简单的LIN。简单LIN模式由CCR3.MOD[2:0]=110b启用。由于简单LIN模式使用与异步模式相同的电路进行除BreakField以外的发送接收控制，因此简单LIN模式也需要异步模式所需的基本通信设置。

（使用simpleLIN时的设置值，请参考26.2节寄存器说明。特别注意CCR3.RXDESEL需要从初始值改成1。）

起始帧由中断字段、控制字段0和控制字段1组成。信息帧可以配置一些数据字段、CRC16上字段和CRC16下字段。

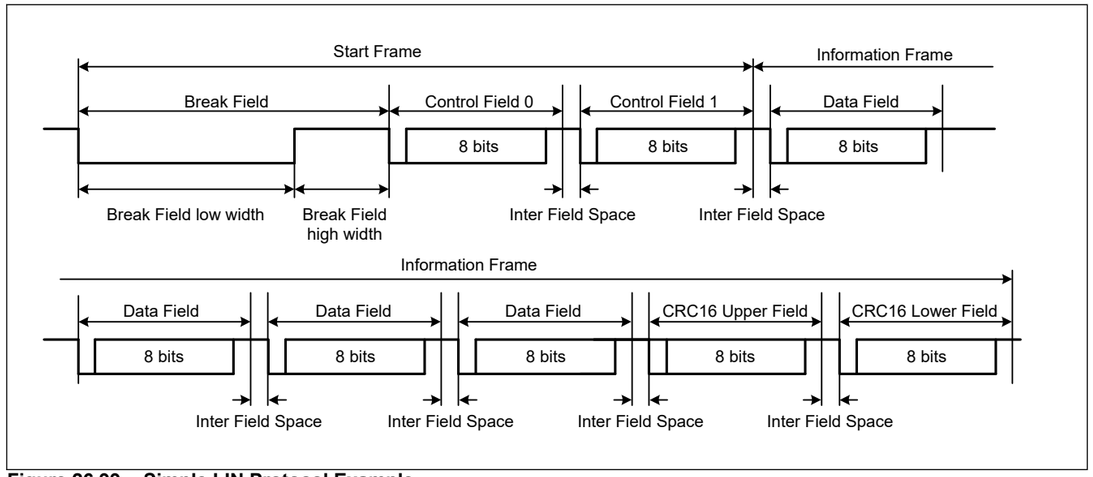


Figure 26.99 Simple LIN Protocol Example

The following describes operations when the Simple LIN is used. In this section, operations are described with the following conditions:

Communication pin (RXDn / TXDn) level inversion function: OFF (RINV = TINV = 0)

When using the simple LIN with the communication pin (RXDn / TXDn) level inversion function enabled, replace the RXDn and TXDn signal levels with their inverted levels.

26.11.1 Simple LIN Start Frame Transmission

Figure 26.100 shows an example of transmission of the Start Frame consisting of a Break Field, Control Field0, and Control Filed1. (Omit Break Field and Control Field0 according to the Start Frame configuration.)

Figure 26.101 shows a flowchart for Start Frame transmission.

The SCI operates as follows during Start Frame transmission.

1. Make the initial settings for the SCI according to the SCI initialization flow (Figure 26.66) in asynchronous mode. In simple LIN mode, do not set CCR0.TE and TIE to 1 at the same time to avoid SCIn_TXI output before the Break Field. Therefore, perform the following two steps sequentially to set the SCI initialization flow (asynchronous mode) procedure [9].
   - Set the bits except CCR0.TIE. (CCR0.TIE = 0, CCR0.TE = 1, and CCR0.RE = 0)
   - Set CCR0.TIE to 1.
2. When 1 is written to TCST, the Break Field output timer starts counting and outputs a low level (Break Field) from the TXDn pin for the period set in XCR2.BFLW[15:0]. A timer count clock source can be selected by XCR0.TCSS[1:0]. Writing 0 to XCR1.TCST suspends output of the Break Field. After the suspension, set CCR0.TE = 0 and turn off the transmission.
3. When the Simple LIN module timer count value matches the set XCR2.BFLW[15:0] value, the timer stops counting and inverts the TXDn pin output level, and the XSR0.BFOF flag is set to 1*1. Furthermore, if XCR0.BFOIE has been set to 1 at this time, a SCIn_TXI interrupt is generated.
4. After the SCIn_TXI interrupt and confirming XSR0.BFOF = 1, write the transmitted data then the Control Field 0 data is transmitted using the SCI*1.

Note: LIN communication requires a Break Delimiter (IDLE period) of 1 bit or more from the end of Break Field output until the next data transmission starts. For this reason, the Break Delimiter length is counted upon completion of Break Field output. If transmit data is written while the Break Delimiter length is being counted, transmission does not start until the Break Delimiter length counting is completed. When transmit data is written after the Break Delimiter length has been counted, transmission starts at the same timing as normal data transmission.
Break Delimiter length count time after Break Field output:
1-bit to 2-bit length (CCR3.STP = 0)

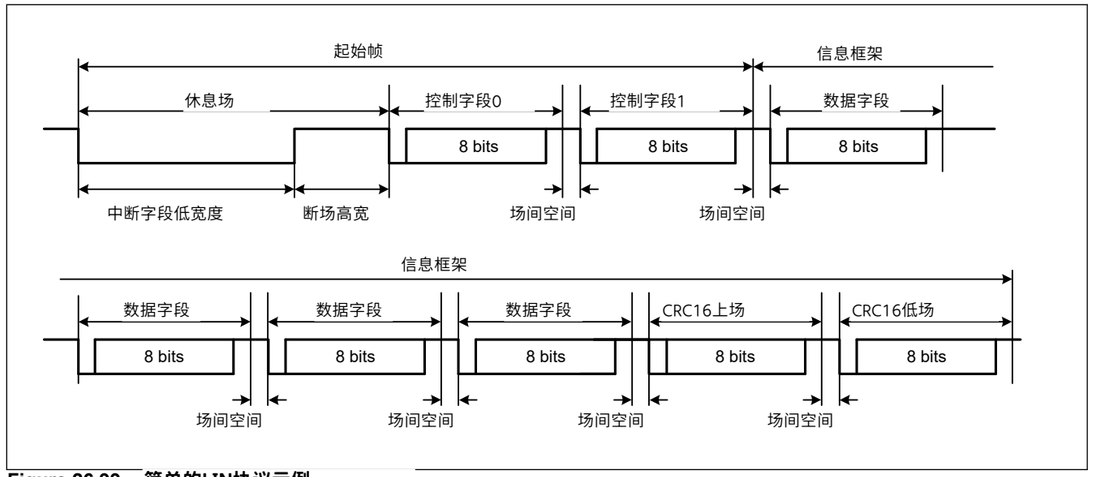


Figure 26.99 简单的LIN协议示例

下面介绍使用SimpleLIN时的操作。在本节中，描述了以下条件的操作：

通讯引脚（RXDnTXDn）电平反转功能：OFF（RINV=TINV=0）

当使用启用了通信引脚（RXDnTXDn）电平反转功能的简单LIN时，更换RXDn和TXDn信号电平及其反相电平。

26.11.1 简单的LIN开始帧传输

图26.100显示了由中断字段、控制字段0和控制组成的起始帧的传输示例归档1。（根据StartFrame配置省略BreakField和ControlField0。）

图26.101显示了起始帧传输的流程图。

SCI在起始帧传输期间操作如下。

1.在异步模式下按照SCI初始化流程（图26.66）对SCI进行初始化设置。在简单LIN模式，不要将CCR0.TE和TIE同时设置为1，以避免在BreakField之前输出SCIn_TXI。因此，依次执行以下两个步骤来设置SCI初始化流程（异步模式）程序[9]。

- ●设置CCR0.TIE以外的位。（CCR0.TIE=0，CCR0.TE=1，CCR0.RE=0）
- ●将CCR0.TIE设置为1。

2.当1写入TCST时，BreakField输出定时器开始计数，并在XCR2.BFLW[15:0]中设置的周期内从TXDn引脚输出低电平（BreakField）。定时器计数时钟源可以通过XCR0.TCSS[1:0]选择。向XCR1.TCST写入0将暂停BreakField的输出。暂停后，设置CCR0.TE=0并关闭传输。

3.当SimpleLIN模块定时器计数值与设置的XCR2.BFLW[15:0]值匹配时，定时器停止计数并反转TXDn引脚输出电平，并将XSR0.BFOF标志设置为1*1。此外，如果此时XCR0.BFOIE已设置为1，则会产生SCIn_TXI中断。

4.SCIn_TXI中断并确认XSR0.BFOF=1后，写入发送的数据，然后使用SCI*1发送控制字段0数据。

Note: LIN通信需要1位或更多的BreakDelimiter（IDLE周期），从BreakField输出结束到下一次数据传输开始。因此，中断分隔符长度在中断字段输出完成时计算。如果在计算间隔分隔符长度时写入发送数据，则在完成间隔分隔符长度计数之前不会开始发送。在计算完间隔分隔符长度后写入发送数据时，发送与正常数据发送的时序相同。

BreakDelimiterlengthcounttimeafterBreakFieldoutput:1位到2位长度(CCR3.STP=0)

2-bit to 3-bit length (CCR3.STP = 1)

5. After the Control Field 0 data has been transmitted, write the Control Field 1 data to TDR. And it is transmitted.
6. After the Control Field 1 data has been transmitted, the Information Frame data is transmitted.

Note 1. After XSR0.BFOF is set to 1, if 1 is written to XCR1.TCST without clearing it, no SCIn_TXI interrupt is output at the end of Break Field transmission. Clear XSR0.BFOF before writing 1 to XCR1.TCST.

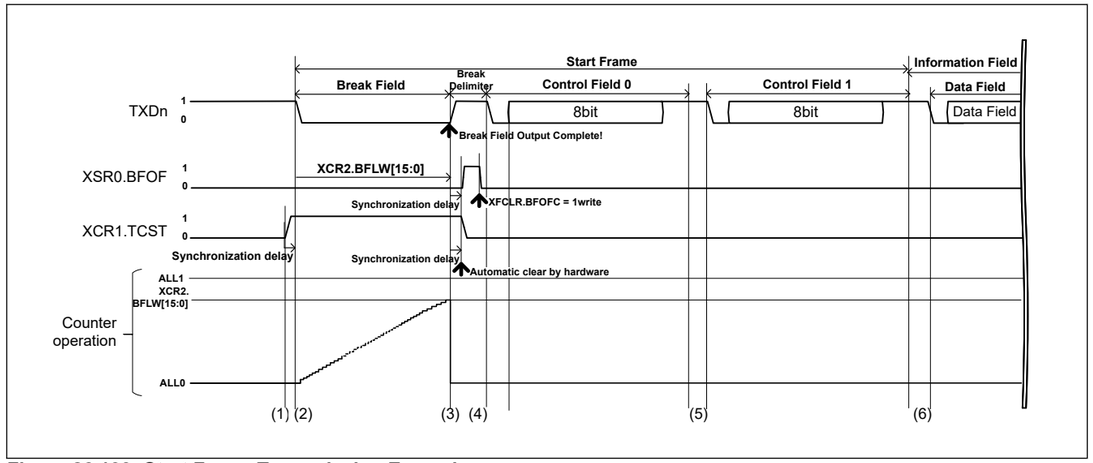


Figure 26.100 Start Frame Transmission Example

2位到3位长度(CCR3.STP=1)

5.控制字段0数据传输完毕后，将控制字段1数据写入TDR。并且被传送。

6.控制字段1数据传输完毕后，信息帧数据被传输。

注1.XSR0.BFOF设置为1后，如果将1写入XCR1.TCST而不清除它，则在BreakField传输结束时不输出SCIn_TXI中断。在将1写入XCR1.TCST之前清除XSR0.BFOF。

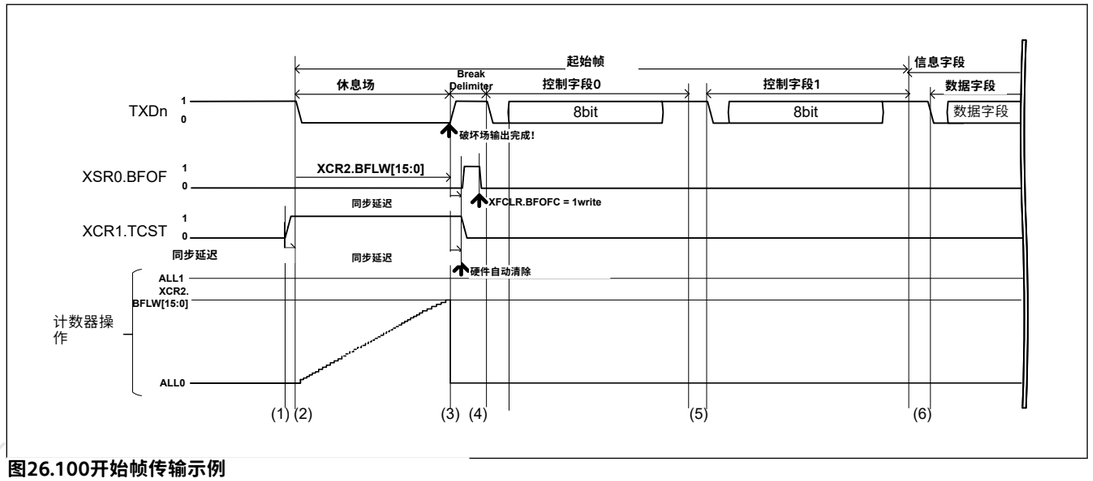


图26.100开始帧传输示例

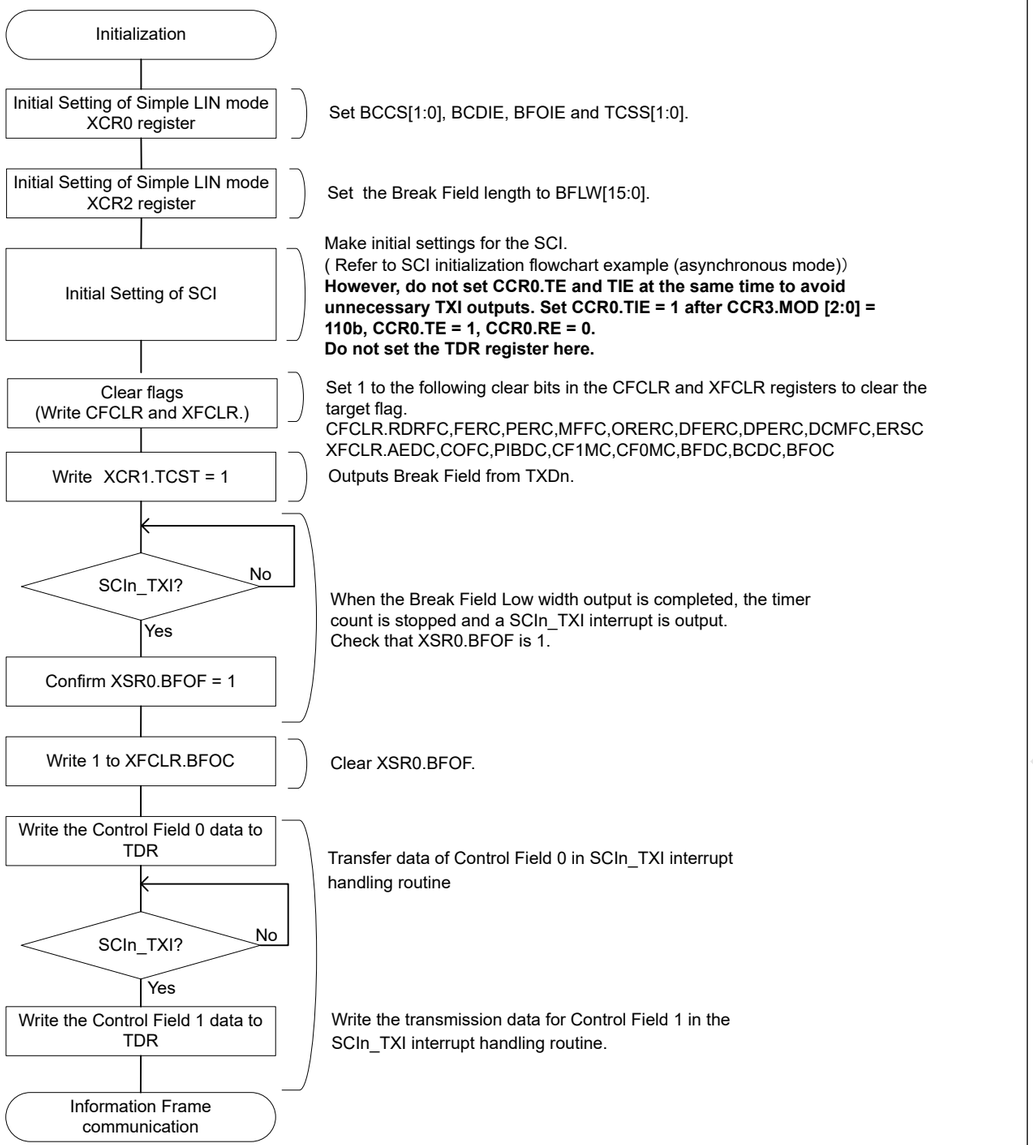


Figure 26.101 Start Frame Transmission Flowchart Example

26.11.2 Simple LIN Start Frame Reception

The SCI can detect Start Frames configured as shown in Figure 26.102.

图26.101起始帧传输流程图示例

26.11.2 简单的LIN开始帧接收

SCI可以检测如图26.102所示配置的起始帧。

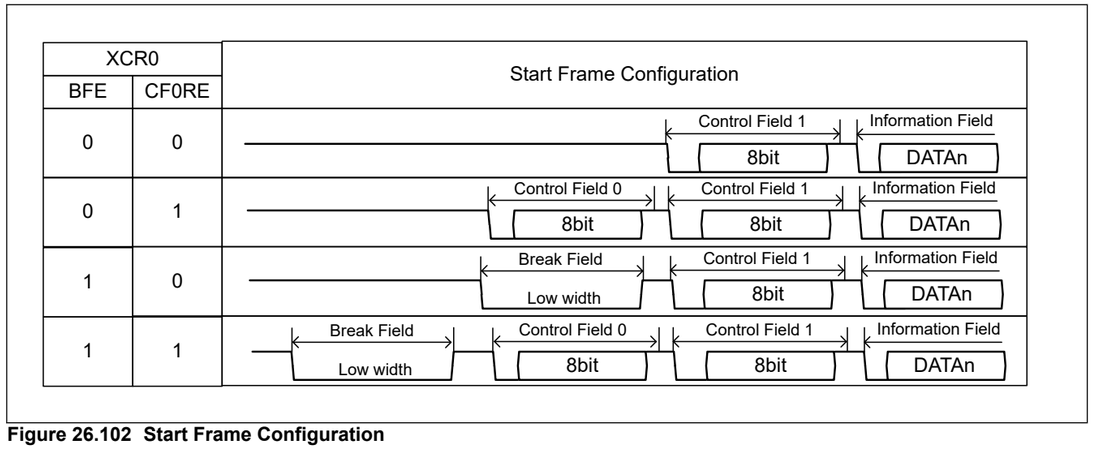


Figure 26.102 Start Frame Configuration

(1) Simple LIN normal reception of Start Frame (PIB not used)

Figure 26.103 shows an example of normal reception of the Start Frame consisting of a Break Field, Control Field0, and Control Field1. Figure 26.104 shows an example of reception to detect the Break Field during Control Field 1. Figure 26.105 shows a flowchart to receive the Start Frame, and Figure 26.106 shows a state transition diagram.

When receiving the Start Frame, the SCI operates as follows. Omit the processing of Break Field and Control Field0 according to the Start Frame configuration.

1. Writing 1 to XCR1.SDST makes it possible to detect the Start Frame. When XCR0.BFE = 1, RXDn input to the SCI core is disabled until the Break Field is detected (because XSR0.RXDSF is set to 1). Once the Break Field is detected, RXDn input can be received to the SCI core (XSR0.RXDSF = 0).
2. When a low level is input from the RXDn pin, the Break Field detection count starts. A timer count clock source can be selected by XCR0.TCSS[1:0].
3. When a low level that is equal to or longer than the period set in XCR2.BFLW[15:0] is input from the RXDn pin, it is determined as Break Field. At this time, XSR0.BFDF is set to 1. If XCR0.BFDIE has been set to 1 at this time, a SCIn_BFD interrupt is generated.
   The timer continues counting until the RXDn rising edge or counter overflow.
4. After the Break Field is detected, when the input level from the RXDn pin becomes high, the count value is captured to XSR1.TCNT[15:0] when BMEN = 0. At this time, XSR0.RXDSF is cleared to 0 and the SCI core starts receiving the RXDn input.
5. The SCI core starts receiving Control Field 0. Because the simple LIN continuously counts the edge interval, it determines a low level that is equal to or longer than the period set in XCR2.BFLW[15:0] as detection of the Break Field. When the Break Field is detected in the Control Field 0 phase, the SCI core waits for reception of Control Field 0 again (Figure 26.104).
6. When Control Field 0 has been received, an SCIn_RXI interrupt is generated and the Control Field 0 data is stored in XSR0.CF0RD[7:0]. When the received data matches the set XCR2.CF0D[7:0] value, XSR0.CF0MF is set to 1. If the received data differs from the set XCR2.CF0D[7:0] value, the SCI transitions to the state before the Break Field is detected.
7. The SCI core starts receiving Control Field 1. When BFE = 1, the Break Field detection function is continuously enabled while SDST = 1 as in the case of Control Field 0. When the Break Field is detected in the Control Field 1 phase, the SCI core waits for reception of Control Field 0 again.
8. When Control Field 1 has been received, an SCIn_RXI interrupt is generated and the Control Field 1 data is stored in XSR0.CF1RD[7:0]. When the received data matches the set XCR1.PCF1D[7:0] value or the set XCR1.SCF1D[7:0] value, XSR0.CF1MF is set to 1. If the received Control Field 1 data matches neither the set XCR1.PCF1D[7:0] value nor the set XCR1.SCF1D[7:0] value, the SCI transitions to the state before the Break Field is detected.
9. The SCI core performs Information Frame communication.
10. When communication is completed, write 0 to XCR1.SDST and 0 to CCR0.RE to stop reception.

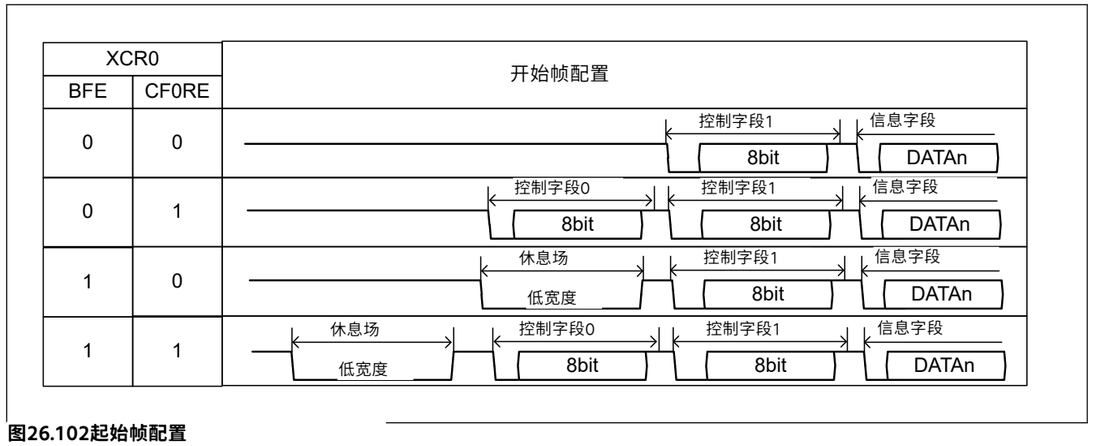


图26.102起始帧配置

(1) 开始帧的简单LIN正常接收（未使用PIB）

图26.103显示了正常接收起始帧的示例，该帧由中断字段、控制字段0和
控制字段1。图26.104显示了在控制域1期间检测中断域的接收示例。图26.105显示了接收起始帧的流程图
，图26.106显示了状态转换图。

当接收到起始帧时，SCI操作如下。根据StartFrame配置省略BreakField和ControlField0的处理。

1.向XCR1.SDST写入1可以检测起始帧。当XCR0.BFE=1时，SCI内核的RXDn输入被禁用，直到检测到中断字段（
因为XSR0.RXDSF设置为1）。一旦检测到中断字段，就可以将RXDn输入接收到SCI内核（XSR0.RXDSF=0）。

2.当从RXDn引脚输入低电平时，BreakField检测计数开始。定时器计数时钟源可以通过XCR0.TCSS[1:0]选择。

3.当等于或长于XCR2.BFLW[15:0]中设置的周期的低电平从RXDn引脚输入时，确定为BreakField。此时，XSR0.B
FDF置1。如果此时XCR0.BFDIE已置1，则产生SCIn_BFD中断。

定时器继续计数，直到RXDn上升沿或计数器溢出。

4.检测到BreakField后，当来自RXDn引脚的输入电平变为高电平时，当BMEN=0时，计数值被捕获到XSR1.TCNT[1
5:0]。此时，XSR0.RXDSF被清除为0和SCI核心开始接收
RXDn input.

5.SCI内核开始接收ControlField0。因为简单的LIN不断地计算边沿间隔，所以它
确定一个等于或长于XCR2.BFLW[15:0]中设置的周期的低电平作为中断字段的检测。当在ControlField0阶段检
测到BreakField时，SCI内核再次等待接收ControlField0（图26.104）。

6.接收到控制字段0后，将产生SCIn_RXI中断，并将控制字段0数据存储在XSR0.CF0RD[7:0]中。当接收到的数据
与设置的XCR2.CF0D[7:0]值匹配时，XSR0.CF0MF设置为1。如果接收到的数据与设置的XCR2.CF0D[7:0]值不同
，则SCI转换到之前的状态检测到中断字段。

7.SCI核开始接收ControlField1，当BFE=1时，BreakField检测功能持续
在SDST=1时启用，与控制字段0的情况一样。当在控制字段1阶段检测到中断字段时，SCI内核再次等待接收控
制字段0。

8.接收到控制字段1后，将产生SCIn_RXI中断，并将控制字段1数据存储在XSR0.CF1RD[7:0]中。当接收到的数据
与设置的XCR1.PCF1D[7:0]值或设置的XCR1.SCF1D[7:0]值匹配时，XSR0.CF1MF设置为1。如果接收到的控制字
段1数据与设置的XCR1都不匹配。PCF1D[7:0]值或设置的XCR1.SCF1D[7:0]值，SCI转换到检测到中断字段之前
的状态。

9.SCI核心执行信息帧通信。

10.通信完成后，向XCR1.SDST写入0，向CCR0.RE写入0，停止接收。

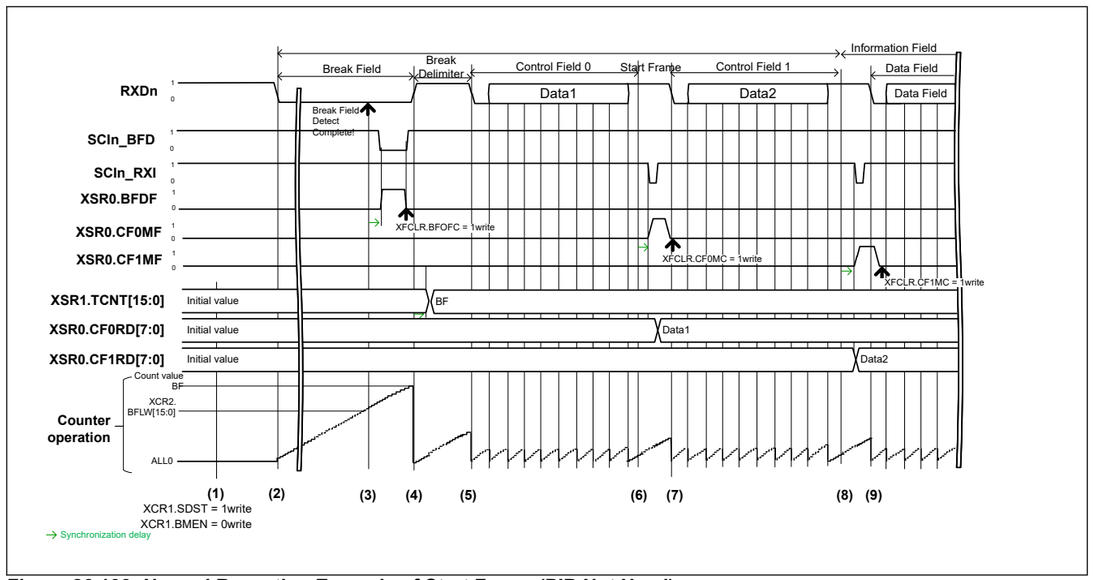


Figure 26.103 Normal Reception Example of Start Frame (PIB Not Used)

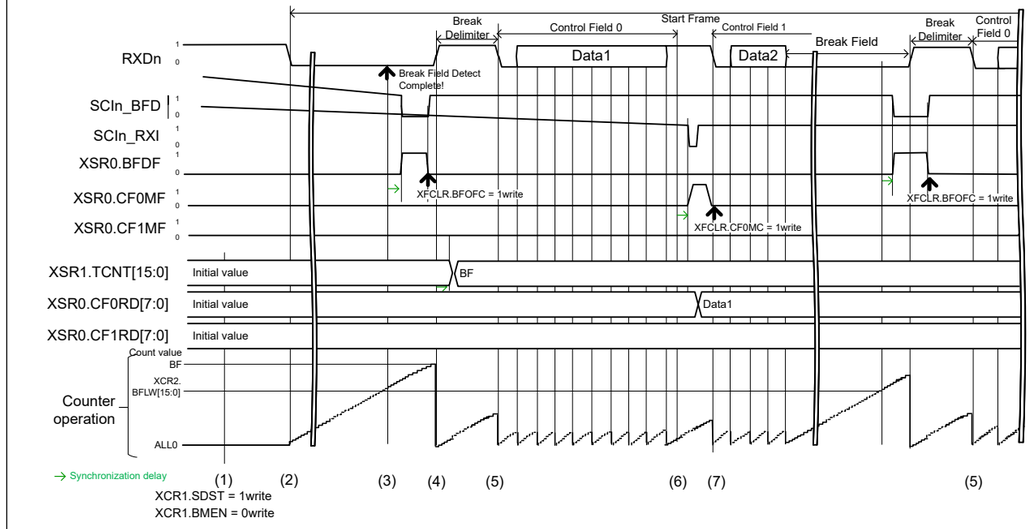


Figure 26.104 Start Frame Reception Example (PIB Not Used) Break Field Detected during Control Field 1

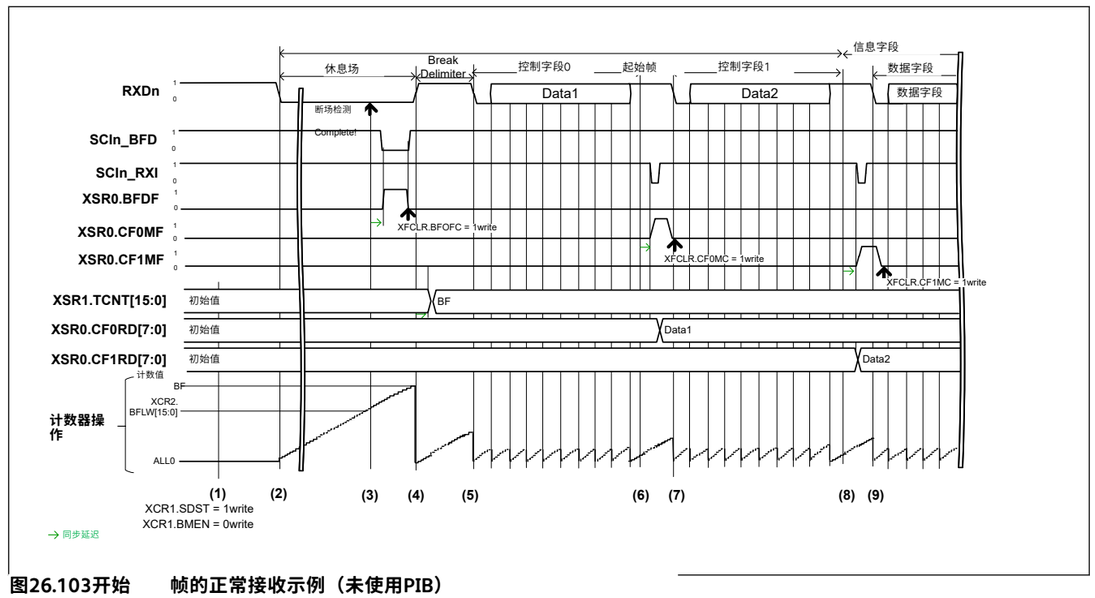


图26.103开始 帧的正常接收示例（未使用PIB）

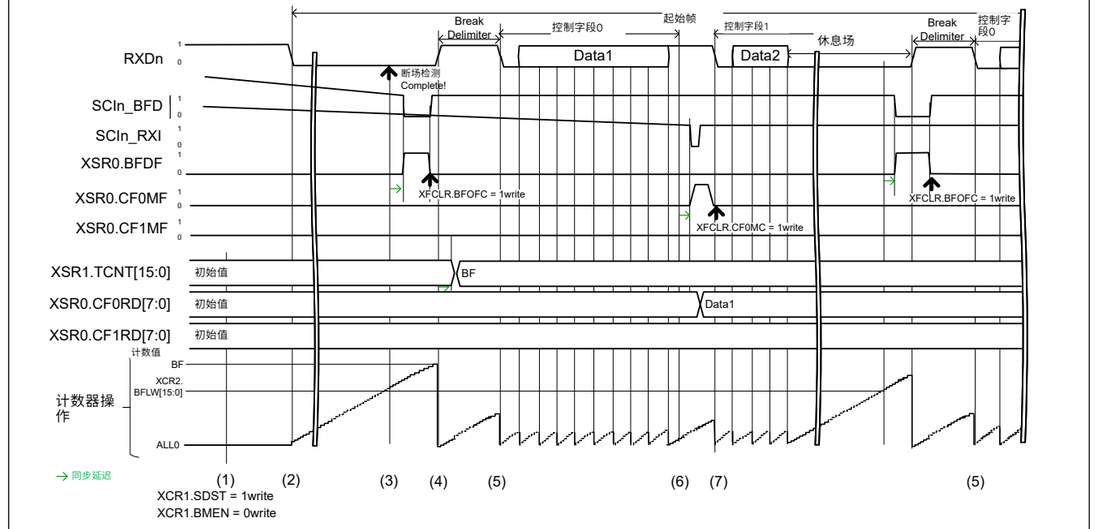


图26.104开始帧接收示例（未使用PIB）在控制字段1期间检测到中断字段

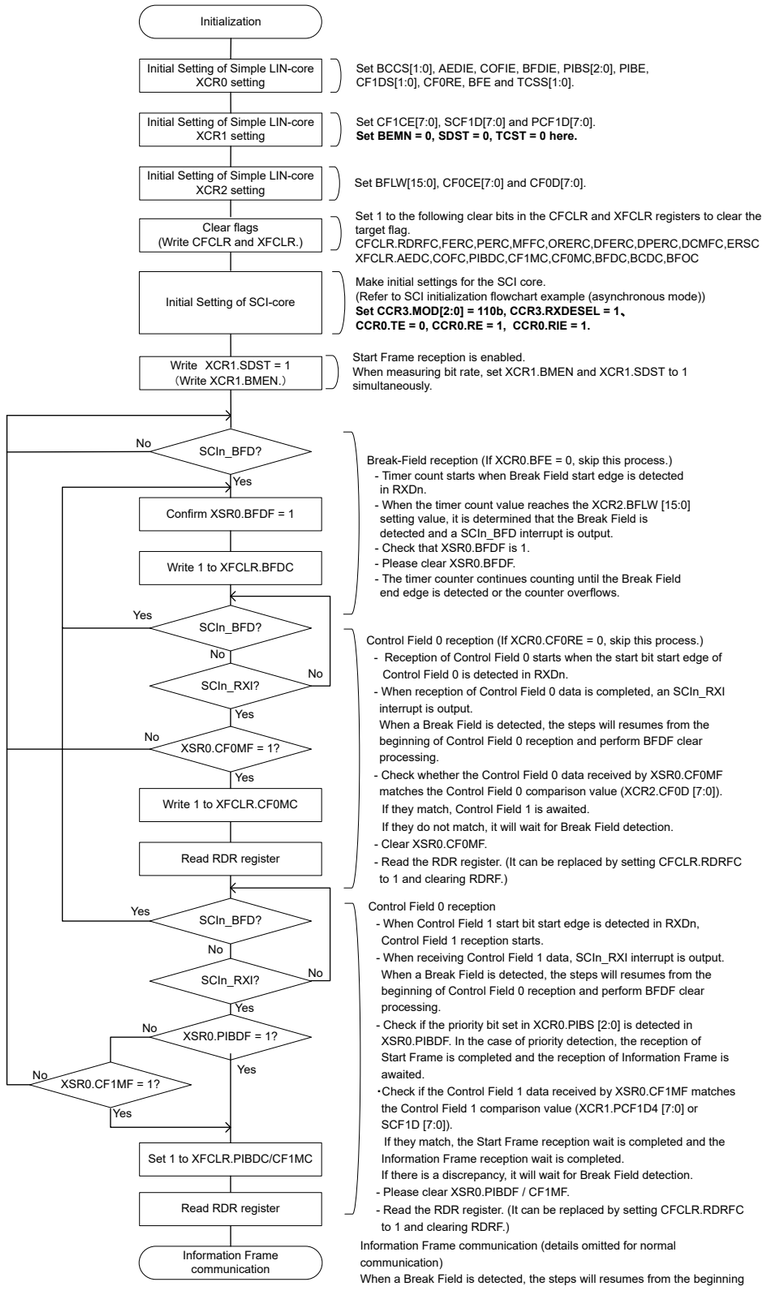


Figure 26.105 Example of Start Frame Reception Flowchart

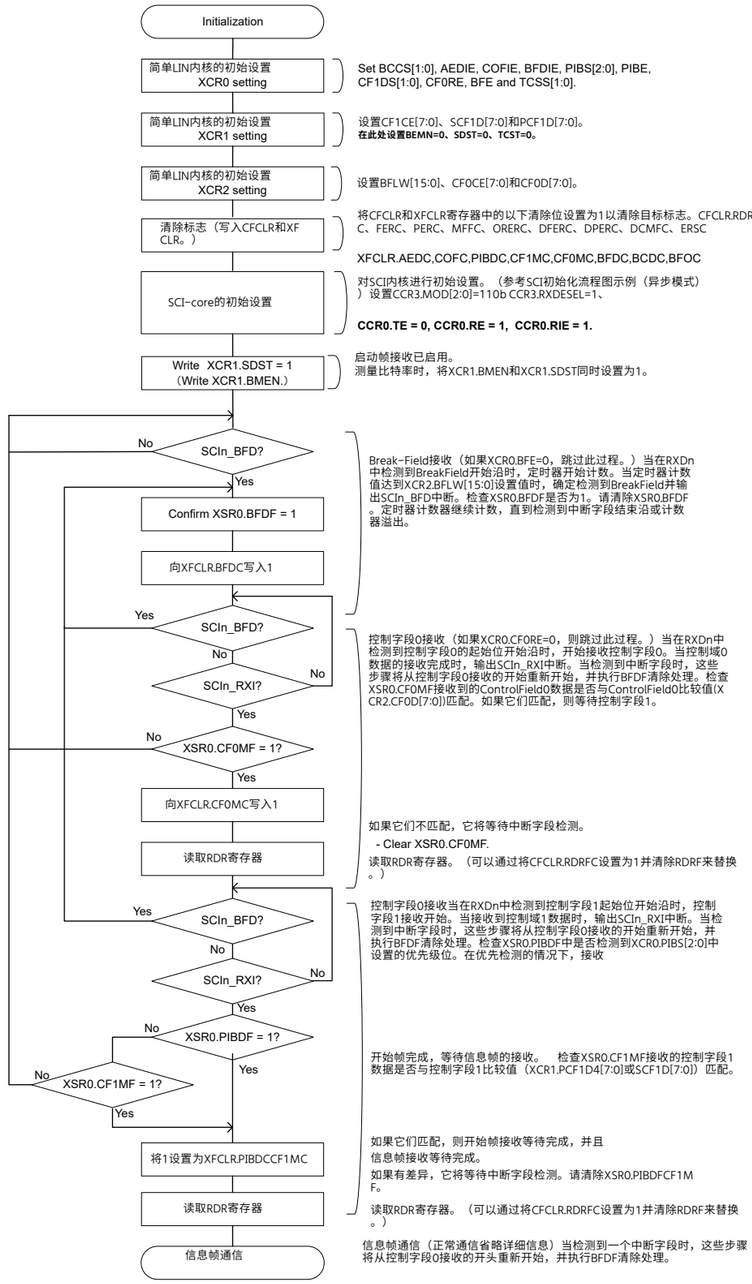


图26.105起始帧接收流程图示例

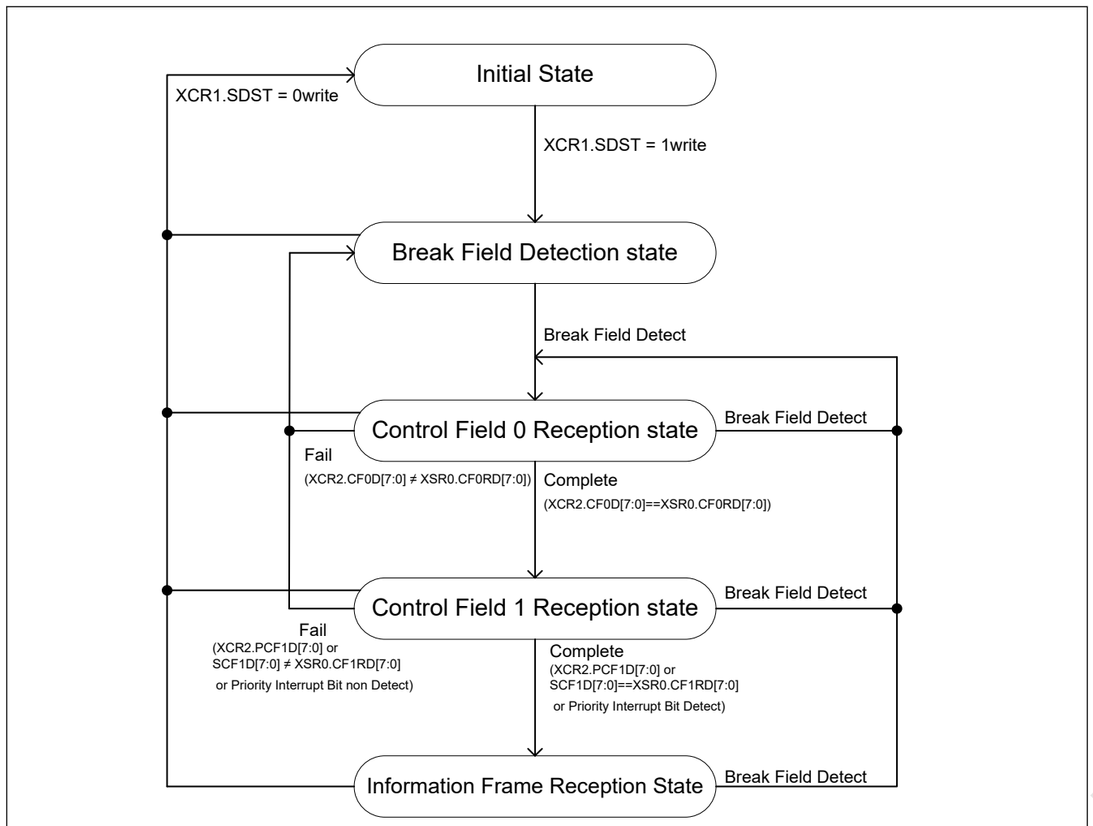


Figure 26.106 State Transition Diagram of Start Frame Reception

(2) Simple LIN Start Frame reception (using the priority interrupt bit)

Figure 26.107 shows an example of Start Frame reception using the priority interrupt bit. The priority interrupt bit is enabled by setting XCR0.PIBE to 1.

The SCI operates as follows during Start Frame reception using the priority interrupt bit.

Steps (1) to (7) are the same as steps (1) to (7) in the Start Frame reception example in Figure 26.103.

(8) When the value specified in the XCR0.PIBS[2:0] bits matches the set XCR1.PCF1D[7:0] value, XSR0.PIBDF is set to 1 and the SCI core performs communication of the Information Frame. If the data received in Control Field 1 matches neither the set XCR1.PCF1D[7:0] value nor the set XCR1.SCF1D[7:0] value and the priority interrupt bit is not detected, the SCI transitions to the state before the Break Field is detected.

(9) Communicate information frame at the SCI core.

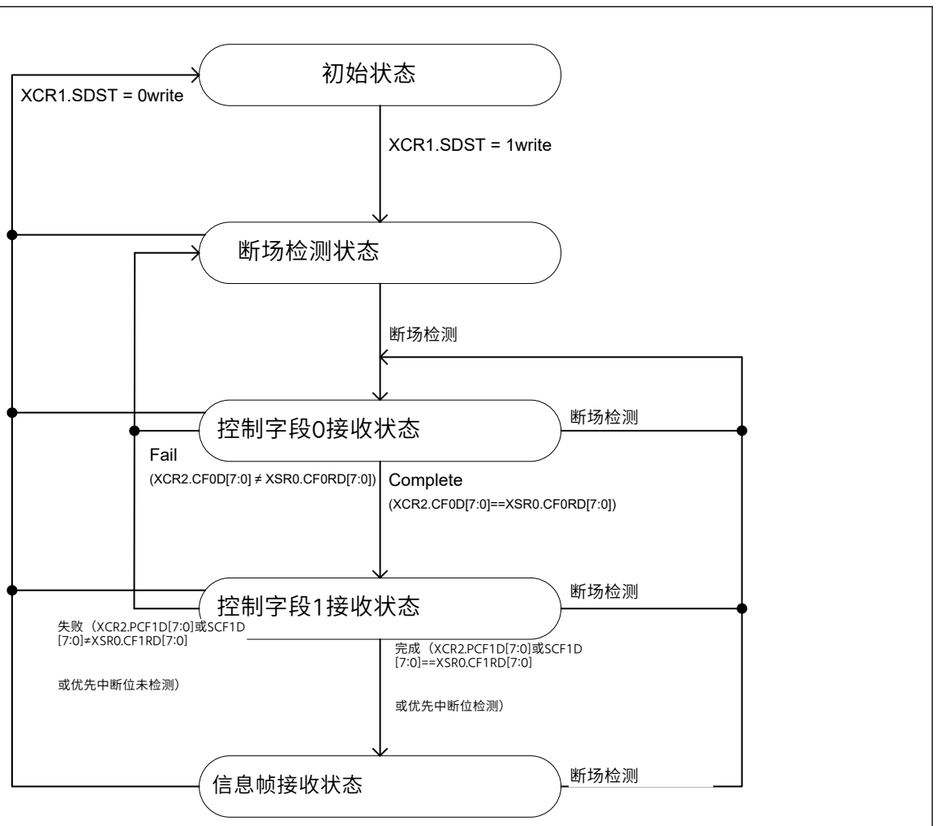


图26.106起始帧接收状态转换图

(2) 简单的LIN开始帧接收（使用优先级中断位）

图26.107显示了使用优先中断位接收起始帧的示例。通过将XCR0.PIBE设置为1来启用优先级中断位。

在使用优先中断位接收起始帧期间，SCI操作如下。

步骤(1)到(7)与图26.103的起始帧接收示例中的步骤(1)到(7)相同。

(8)当XCR0.PIBS[2:0]位中指定的值与设置的XCR1.PCF1D[7:0]值匹配时，XSR0.PIBDF设置为1，SCI内核执行信息帧的通信。如果在控制字段1中接收到的数据既不匹配设置的XCR1.PCF1D[7:0]值也不匹配设置的XCR1.SCF1D[7:0]值并且未检测到优先级中断位，则SCI转换到之前的状态检测到中断字段。

(9)在SCI核心通信信息框架。

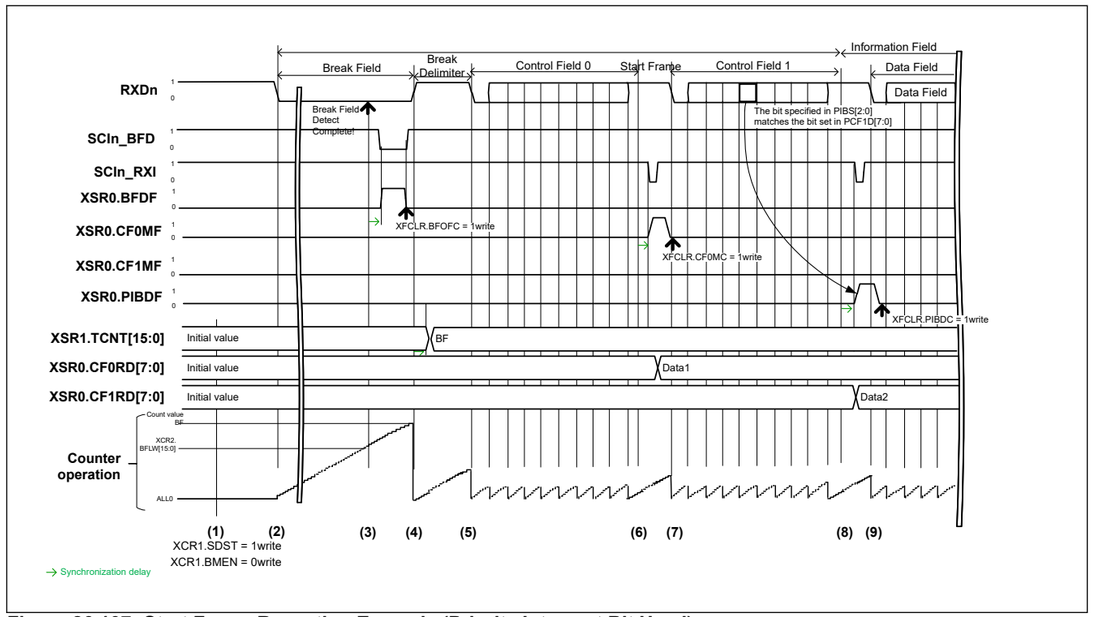


Figure 26.107 Start Frame Reception Example (Priority Interrupt Bit Used)

26.11.3 Simple LIN Bus Conflict Detection Function

In Simple LIN mode (CCR3MOD[2:0] = 110) when TE = 1, the bus conflict detection function works during Break Field output and during data transmission.

Figure 26.108 shows an operation example of the bus conflict detection function. The TXDn pin output and the RXDn pin input are sampled by the bus conflict detection clock set in XCR0.BCCS[1:0]. When a mismatch occurs three times in a row, XSR0.BCDF is set to 1, and if XCR0.BCDIE has been set to 1 at this time, an SCIn_ERI interrupt is generated.

When an SCIn_ERI interrupt is generated, stop transmission according to Figure 26.109. Check the bus state to decide whether to resume transmission.

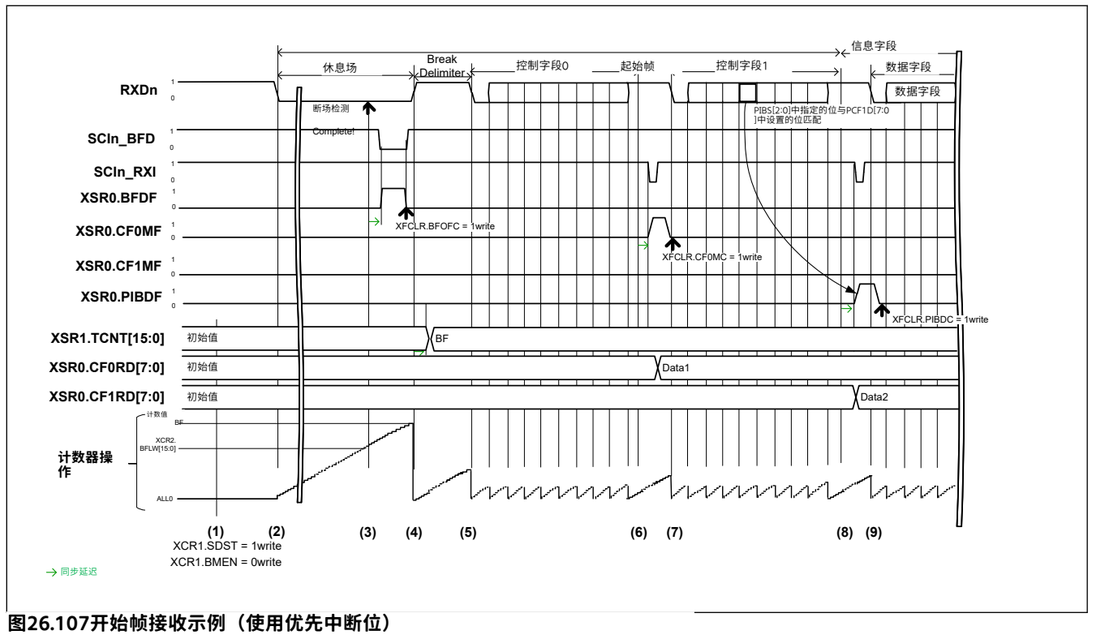


图26.107开始帧接收示例（使用优先中断位）

26.11.3 简单的LIN总线冲突检测功能

在简单LIN模式(CCR3MOD[2:0]=110)中，当TE=1时，总线冲突检测功能在BreakField输出和数据传输期间工作。

图26.108显示了总线冲突检测功能的操作示例。TXDn引脚输出和RXDn引脚输入由XCR0.BCCS[1:0]中设置的总线冲突检测时钟采样。当连续出现3次不匹配时，XSR0.BCDF置1，如果此时XCR0.BCDIE已经置1，则产生SCIn_ERI中断。

当产生SCIn_ERI中断时，根据图26.109停止传输。检查总线状态以决定是否恢复传输。

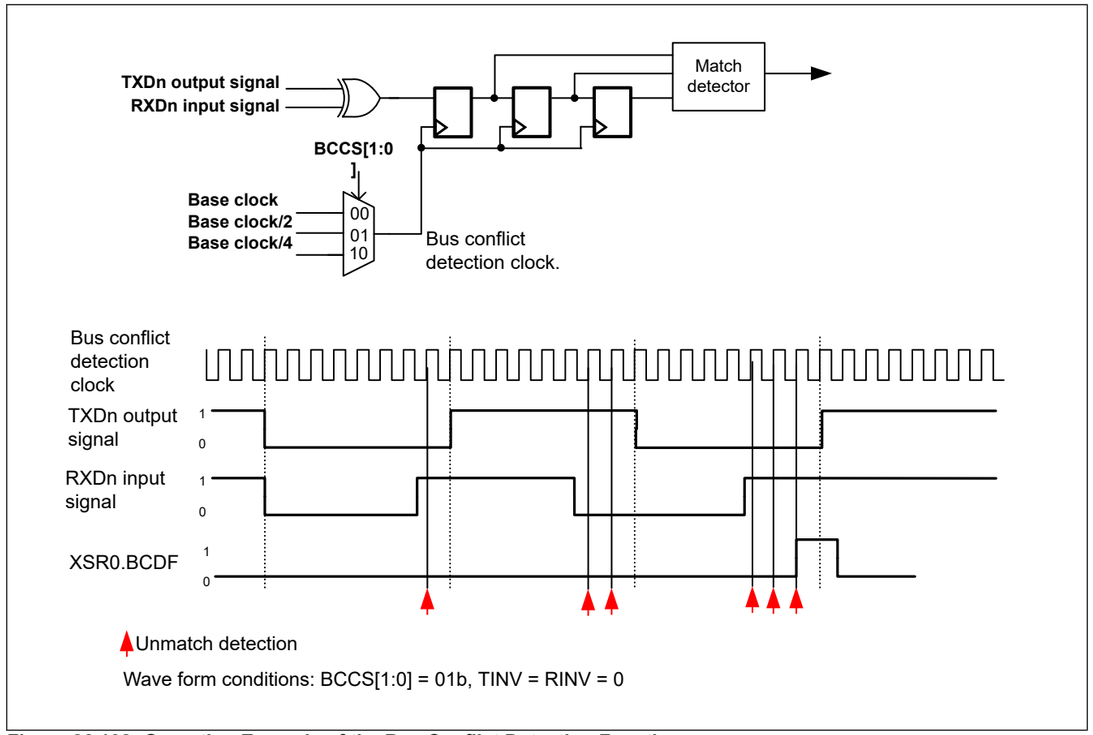


Figure 26.108 Operation Example of the Bus Conflict Detection Function

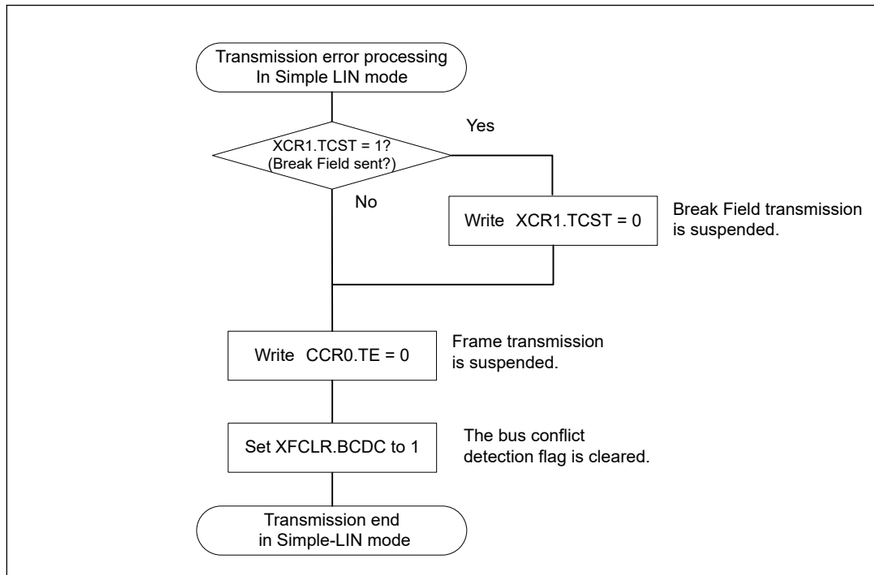


Figure 26.109 SCIn_ERI Interrupt handling flow at transmission in Simple LIN mode

26.11.4 Simple LIN Bit Rate Measurement Function

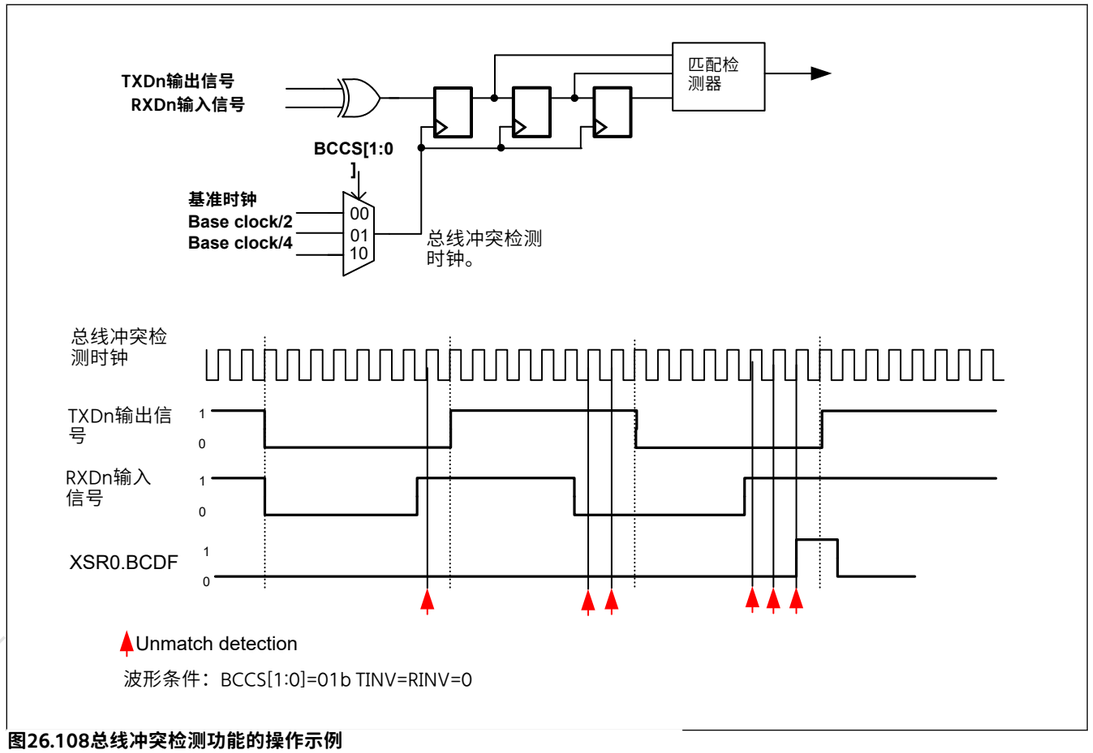


图26.108总线冲突检测功能的操作示例

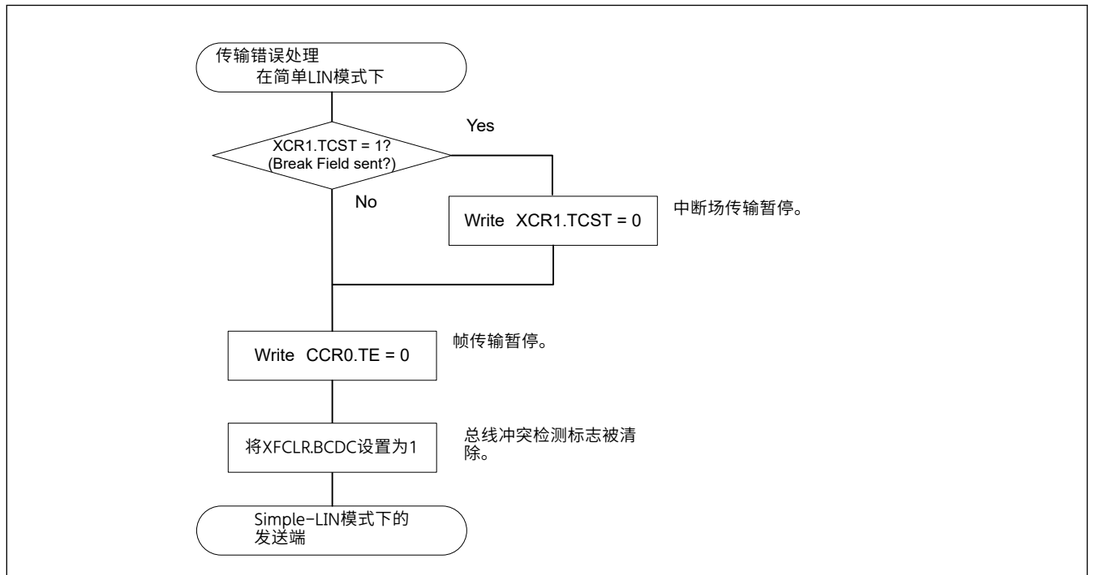


图26.109SCIn_ERI简单LIN模式下传输时的中断处理流程

26.11.4 简单的LIN比特率测量功能

This function measures a bit rate between the effective edges of the input signal from the RXDn pin. Figure 26.110 shows an operation example of the bit rate measurement function.

1. Writing 1 to XCR1.SDST and XCR1.BMEN enables bit rate measurement. When this bit is set to 1, the valid edge interval of Control Field 0 and Control Field 1 data is measured. However, bit rate is not measured between the Break Field and the Break Delimiter. Set XCR1.BMEN and XCR1.SDST to 1 simultaneously, only when measuring bit rate.
2. Because bit rate is not measured in the Break Field, the effective edge detection flag is not set to 1 at the rising edge at the end of the Break Field, and the counter capture value is not stored in XSR1.TCNT[15:0].
3. The counter starts counting from the falling edge of the start bit in Control Field 0. The Break Delimiter count value is not captured in XSR1.TCNT[15:0].
4. The rising edge of the start bit is detected as an effective edge, and then the XSR0.AEDF flag is set to 1. If XCR0.AEDIE has been set to 1 at this time, an SCIn_AED interrupt is output. The start bit count value is stored in XSR1.TCNT[15:0]. The XSR1.TCNT[15:0] value is retained until the effective capture value is read.
5. Even if an effective edge is input from the RXDn input pin, the count value of this effective edge timing is not captured because the XRS1.TCNT[15:0] value has not been read and retention has not been released. In this case, an SCIn_AED interrupt is not output.
6. The XSR1.TCNT[15:0] value is read. Then the retention of XSR1.TCNT[15:0] is released and the XSR0.AEDF flag is cleared by hardware.
7. Because the retention of XSR1.TCNT[15:0] has been released, the count value is captured at the effective edge and is retained. At the same time, the XSR0.AEDF flag is set to 1, and if XCR0.AEDIE has been set to 1, an SCIn_AED interrupt is output. The bit rate can be adjusted by calculating it from the count value between effective edges by software and by changing the SCI settings.
8. To disable bit rate measurement, write 0 to XCR1.BMEN.
9. The XSR0.AEDF value and the XSR1.TCNT[15:0] value remain unchanged at the effective edge timing because the bit rate measurement function is disabled.

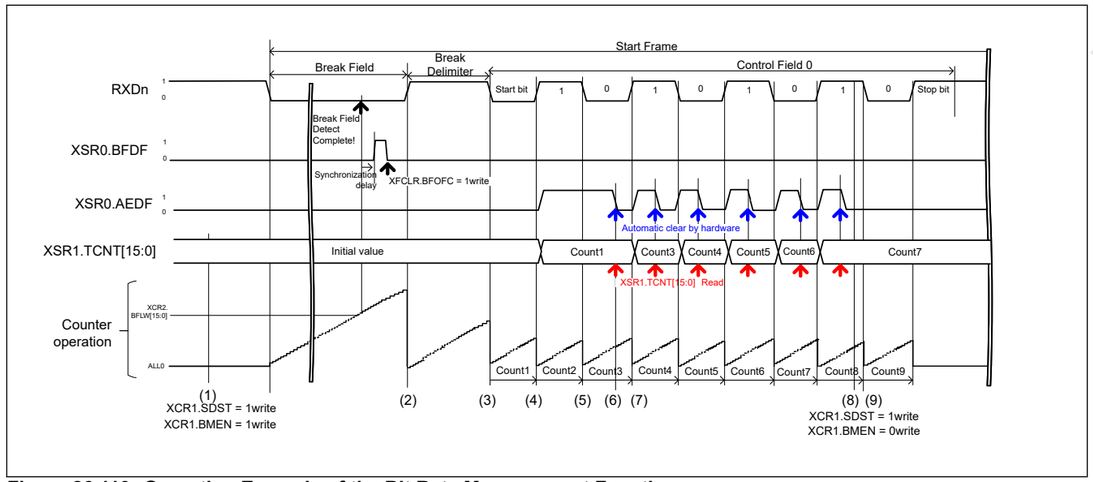


Figure 26.110 Operation Example of the Bit Rate Measurement Function

26.12 Interrupt Sources

26.12.1 Buffer Operation for SCIn_TXI and SCIn_RXI Interrupts

If the conditions for an SCIn_TXI and SCIn_RXI interrupt are satisfied while the interrupt status flag in the ICU is 1, the ICU does not output the interrupt request but saves it internally with a capacity for retention of one request per source.

该功能测量来自RXDn引脚的输入信号的有效边沿之间的比特率。图26.110显示了比特率测量功能的操作示例。

1.将1写入XCR1.SDST和XCR1.BMEN启用比特率测量。当该位设置为1时，有效边沿
测量控制字段0和控制字段1数据的间隔。但是，不测量中断字段和中断定界符之间的比特率。仅在测量比特率时同时将XCR1.BMEN和XCR1.SDST设置为1。

2.因为BreakField中没有测量比特率，所以在BreakField结束的上升沿有效边沿检测标志不设置为1，并且计数器捕获值不存储在XSR1.TCNT[15：0]。

3.计数器从控制字段0中起始位的下降沿开始计数。在XSR1.TCNT[15:0]中不捕获间隔分隔符计数值。

4.检测到起始位的上升沿为有效沿，然后将XSR0.AEDF标志置1。如果
此时XCR0.AEDIE已设置为1，输出SCIn_AED中断。起始位计数值存储在
XSR1.TCNT[15:0]。XSR1.TCNT[15:0]值将一直保留到读取有效捕获值为止。

5.即使从RXDn输入引脚输入有效边沿，由于尚未读取XRS1.TCNT[15:0]值且保留尚未解除，因此不会捕获此有效边沿时序的计数值。在这种情况下，不输出SCIn_AED中断。

6.读取XSR1.TCNT[15:0]值。然后XSR1.TCNT[15:0]的保留被释放，XSR0.AEDF标志被硬件清除。

7.因为XSR1.TCNT[15:0]的保留已经被释放，所以计数值在有效边沿被捕获并被保留。同时，XSR0.AEDF标志置1，如果XCR0.AEDIE已经置1，则输出SCIn_AED中断。可以通过软件从有效边沿之间的计数值计算比特率并通过更改SCI设置来调整比特率。

8.要禁用比特率测量，向XCR1.BMEN写入0。

9.XSR0.AEDF值和XSR1.TCNT[15:0]值在有效边沿时序保持不变，因为比特率测量功能被禁用。

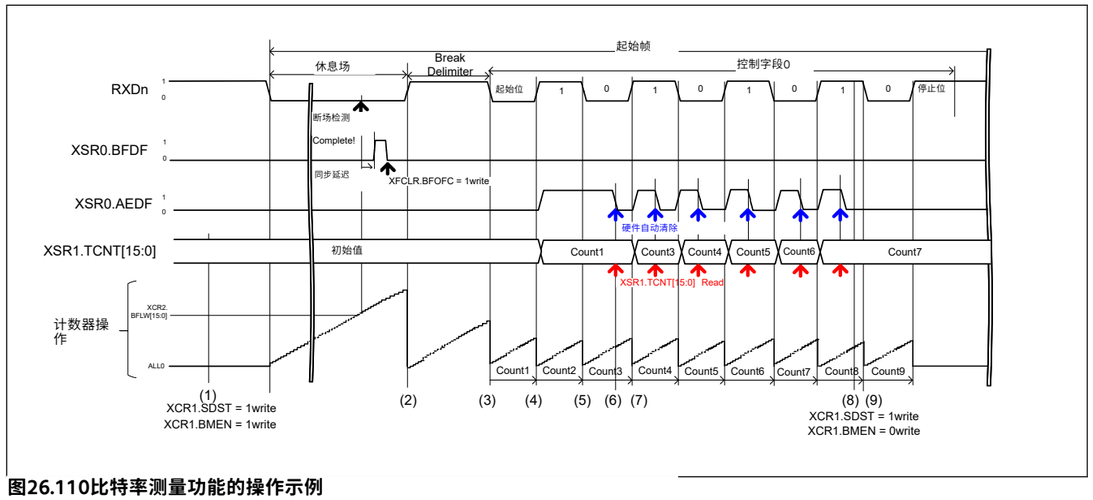


图26.110比特率测量功能的操作示例

26.12 中断源

26.12.1 SCIn_TXI和SCIn_RXI中断的缓冲区操作

如果在ICU中的中断状态标志为1时满足SCIn_TXI和SCIn_RXI中断的条件，则ICU不输出中断请求，而是将其保存在内部，每个源可以保留一个请求。

26.12.2 Interrupts in Asynchronous, Manchester, Clock Synchronous, and Simple SPI Modes

(1) Non-FIFO selected

Table 26.40 lists interrupt sources in asynchronous mode, Manchester mode, clock synchronous mode, and simple SPI mode.

A different interrupt vector can be assigned to each interrupt source. Individual interrupt sources can be enabled or disabled with the enable bits in the CCR0 register.

If the CCR0.TIE bit is 1, an SCIn_TXI interrupt request is generated when transmit data is transferred from the TDR register to the TSR register. An SCIn_TXI interrupt request can also be generated by using a single instruction to set the CCR0.TE and CCR0.TIE bits to 1 at the same time. An SCIn_TXI interrupt request can activate the DTC or DMAC to handle data transfer.

An SCIn_TXI interrupt request is not generated by setting the CCR0.TE bit to 1 when CCR0.TIE is 0 or by setting the CCR0.TIE bit to 1 when the CCR0.TE is 1.*1

When new data is not written by the time of transmission of the last bit of the current transmit data and CCR0.TEIE is 1, the CSR.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated. Additionally, when CCR0.TE is 1, the CSR.TEND flag retains the value 1 until more transmit data is written to the TDR register, and setting CCR0.TEIE to 1 leads to the generation of an SCIn_TEI interrupt request.

Writing data to the TDR register leads to clearing of the CSR.TEND flag and, after a certain time, discarding of the SCIn_TEI interrupt request.

If the CCR0.RIE bit is 1, an SCIn_RXI interrupt request is generated when received data is stored in the RDR register. An SCIn_RXI interrupt request can activate the DTC or DMAC to handle data transfer.

Setting any of the CSR.ORER, FER, PER or MSR.MER*2, SYER*2, PFER*2, and SBER*2 flags to 1 when the CCR0.RIE bit is 1 leads to the generation of an SCIn_ERI interrupt request.

An SCIn_RXI interrupt request is not generated in this case. Clearing all these flags (ORER, FER, PER, MER*2, SYER*2, PFER*2 and SBER*2) leads to discarding of the SCIn_ERI interrupt request.

Note 1. To temporarily prohibit SCIn_TXI interrupts on transmission of the last of the data when a new round of transmission is to be started, after handling the transmission-completed interrupt, control activation of the interrupt by using the interrupt request enable bit in the ICU rather than using the CCR0.TIE bit. This approach can prevent the suppression of SCIn_TXI interrupt requests in the transfer of new data.

Note 2. MER, SYER, PFER, and SBER work as a factor of SCIn_ERI interrupt only in Manchester mode. SYER, PFER, and SBER also only work if its enable bits (SYEREN, PFEREN, SBEREN in MECR) are set to "1".

(2) FIFO selected

Table 26.41 lists interrupt sources in FIFO selected mode.

If the CCR0.TIE bit is 1, an SCIn_TXI interrupt request is generated when the stored amount of data in the transmit-FIFO (TDR) register becomes the threshold value indicated in FCR.TTRG or below. An SCIn_TXI interrupt request can also be generated by using a single instruction to set the CCR0.TIE and CCR0.TE bits to 1 simultaneously or by setting CCR0.TIE to 1 when CCR0.TE is 1.

An SCIn_TXI interrupt request is not generated by setting CCR0.TE to 1 when CCR0.TIE is 0 or by setting the CCR0.TIE bit to 1 while the setting of the CCR0.TE bit is 1.

If CCR0.TEIE is 1 and if the next data is not written to the transmit-FIFO (TDR) register by the time the last bit of the transmit data is sent, the CSR.TEND flag is set to 1 and the SCIn_TEI interrupt request is generated.

If CCR0.RIE is 1, the SCIn_RXI interrupt request is generated when the stored amount of data in the transmit-FIFO (TDR) register is equal to or greater than the threshold value indicated in FCR.RTRG. When RTRG is 0, an SCIn_RXI interrupt does not occur even when the amount of data in the receive FIFO is equal to 0.

If the CCR0.RIE bit is 1, when the CSR.ORER flag is set to 1 or data with a framing error or a parity error is stored in the transmit-FIFO (TDR) register, the SCIn_ERI interrupt request is generated. When the amount of data stored in the transmit-FIFO (TDR) register is at the threshold value or above, the SCIn_RXI interrupt request is also generated. The SCIn_ERI interrupt request can be canceled, in which case CSR.ORER, FER, and PER flags are all cleared.

26.12.2 异步、曼彻斯特、时钟同步和简单SPI中的中断 Modes

(1) Non-FIFO selected

表26.40列出了异步模式、曼彻斯特模式、时钟同步模式和简单SPI模式下的中断源。

可以为每个中断源分配不同的中断向量。可以使用CCR0寄存器中的启用位启用或禁用各个中断源。

如果CCR0.TIE位为1，则当发送数据从TDR寄存器传输到TSR寄存器时，会产生SCIn_TXI中断请求。也可以使用一条指令同时将CCR0.TE和CCR0.TIE位设置为1，从而产生SCIn_TXI中断请求。SCIn_TXI中断请求可以激活DTC或DMAC来处理数据传输。

当CCR0.TIE为0时将CCR0.TE位设置为1或通过设置
当CCR0.TE为1时，CCR0.TIE位为1。*1

当当前发送数据的最后一位发送时未写入新数据且CCR0.TEIE为1，则
CSR.TEND标志设置为1，并产生SCIn_TEI中断请求。此外，当CCR0.TE为1时，
CSR.TEND标志保持值1，直到更多发送数据写入TDR寄存器，将CCR0.TEIE设置为1会导致产生SCIn_TEI中断请求。

将数据写入TDR寄存器会导致CSR.TEND标志清零，并在一定时间后丢弃
SCIn_TEI中断请求。

如果CCR0.RIE位为1，则当接收到的数据存储在RDR寄存器中时会产生SCIn_RXI中断请求。一个
SCIn_RXI中断请求可以激活DTC或DMAC来处理数据传输。

当CCR0.RIE位为1时，将CSR.ORER、FER、PER或MSR.MER*2、SYER*2、PFER*2和SBER*2标志设置为1会导致产生SCIn_ERI中断请求.

在这种情况下不会产生SCIn_RXI中断请求。清除所有这些标志(ORER FER PER MER*2 SYER*2
PFER*2和SBER*2)导致丢弃SCIn_ERI中断请求。

注1.为了在新一轮传输开始时，在最后一个数据传输时暂时禁止SCIn_TXI中断，在处理完传输完成中断后，使用ICU中的中断请求使能位控制中断的激活而不是使用CCR0.TIE位。这种方法可以防止在传输新数据时抑制SCIn_TXI中断请求。

注2.MER、SYER、PFER和SBER仅在曼彻斯特模式下作为SCIn_ERI中断的一个因素起作用。SYER、PFER和
SBER也仅在其启用位（MECR中的SYEREN、PFEREN、SBEREN）设置为“1”时才起作用。

(2) FIFO selected

表26.41列出了FIFO选择模式下的中断源。

如果CCR0.TIE位为1，则当发送FIFO(TDR)寄存器中存储的数据量变为FCR.TTRG中指示的阈值或更低时，将产生SCIn_TXI中断请求。SCIn_TXI中断请求也可以通过使用一条指令同时将CCR0.TIE和CCR0.TE位设置为1或在CCR0.TE为1时将CCR0.TIE设置为1来产生。

当CCR0.TIE为0时将CCR0.TE设置为1或在CCR0.TE位设置为1时将CCR0.TIE位设置为1不会产生SCIn_TXI中断请求。

如果CCR0.TEIE为1，并且如果在发送数据的最后一位发送时下一个数据未写入到发送FIFO(TDR)寄存器，则CSR.TEND标志设置为1，并且SCIn_TEI中断请求生成。

如果CCR0.RIE为1，则当发送FIFO(TDR)寄存器中存储的数据量等于或大于FCR.RTRG中指示的阈值时，将产生SCIn_RXI中断请求。当RTRG为0时，即使接收FIFO中的数据量等于0，也不会发生SCIn_RXI中断。

如果CCR0.RIE位为1，则当CSR.ORER标志设置为1或有帧错误或奇偶校验错误的数据存储在发送FIFO(TDR)寄存器中时，将产生SCIn_ERI中断请求。当存储在发送FIFO（TDR）寄存器中的数据量在阈值或以上时，也会产生SCIn_RXI中断请求。SCIn_ERI中断请求可以被取消，在这种情况下，CSR.ORER、FER和PER标志都被清除。

Table 26.40 SCI interrupt sources with non-FIFO selected

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC or DMAC activation
SCIn_ERI (n = 0 to 4, 9)	Receive error	CSR.ORER, CSR.FER, CSR.PER, CSR.DFER, CSR.DPER, (MSR.MER, MSR.SYER, MSR.PFER, MSR.SBER)*1	CCR0.RIE	Not possible
SCIn_RXI (n = 0 to 4, 9)	Receive data full	CSR.RDRF	CCR0.RIE	Possible
	Address match	CSR.DCMF	CCR0.RIE	Possible
SCIn_TXI (n = 0 to 4, 9)	Transmit data empty	CSR.TDRE	CCR0.TIE	Possible
	TE = 0->1 detection			
SCIn_TEI (n = 0 to 4, 9)	Transmit end	CSR.TEND	CCR0.TEIE	Not possible

Note 1. MER, SYER, PFER, and SBER work as a factor of SCIn_ERI interrupt only in Manchester mode. SYER, PFER, and SBER also only work if its enable bits (SYEREN, PFEREN, SBEREN in MCR) are set to 1.

Table 26.41 SCI interrupt sources with FIFO selected

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC or DMAC activation
SCIn_ERI (n = 0 to 4, 9)	Receive error	CSR.ORER, CSR.FER, CSR.PER, CSR.DFER, CSR.DPER	CCR0.RIE	Not possible
		FRSR.DR (when FCR.DRES = 1)	CCR0.RIE	Not possible
SCIn_RXI (n = 0 to 4, 9)	Receive data full	CSR.RDRF	CCR0.RIE	Possible
	Receive data ready	FRSR.DR (when FCR.DRES = 0)	CCR0.RIE	Possible
	Address match	CSR.DCMF	CCR0.RIE	Possible
SCIn_TXI (n = 0 to 4, 9)	Transmit data empty	CSR.TDFE	CCR0.TIE	Possible
	TE=0->1 detection			
SCIn_TEI (n = 0 to 4, 9)	Transmit end	CSR.TEND	CCR0.TEIE	Not possible

26.12.3 Interrupts in Smart Card Interface Mode

Table 26.42 lists interrupt sources in smart card interface mode. A transmit end interrupt (SCIn_TEI) request and an address match (SCIn_AM) request cannot be used in this mode.

Table 26.42 SCI Interrupt sources in Smart Card Interface Mode

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC or DMAC activation
SCIn_ERI (n = 0 to 4, 9)	Receive error or error signal detection	CSR.ORER, CSR.PER, CSR.ERS	CCR0.RIE	Not possible
SCIn_RXI (n = 0 to 4, 9)	Receive data full	CSR.RDRF	CCR0.RIE	Possible
SCIn_TXI (n = 0 to 4, 9)	Transmit data empty	CSR.TEND	CCR0.TIE	Possible
	When set TE = 0->1			

Data transmission or reception using the DTC or DMAC is also possible in smart card interface mode, similar to normal SCI mode. In transmission, when the CCR0.TEND flag is set to 1, an SCIn_TXI interrupt request is generated. This SCIn_TXI interrupt request activates the DTC or DMAC, allowing transfer of transmit data if the SCIn_TXI request is previously specified as a source of DTC or DMAC activation. The TEND flag is automatically set to 0 when the DTC or DMAC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During the retransmission, the TEND flag is kept at 0 and the DTC or DMAC is not activated. Therefore, the SCI and DTC or DMAC automatically transmit the specified number of bytes, including retransmission after an error occurrence. However, the CSR.ERS flag is not automatically set to

Table 26.40 选择了非FIFO的SCI中断源

Name	中断源	中断标志	中断使能	DTC或DMAC激活
SCIn_ERI (n = 0 to 4, 9)	接收错误	CSR.ORER, CSR.FER, CSR.PER, CSR.DFER, CSR.DPER, (MSR.MER, MSR.SYER, MSR.PFER, MSR.SBER)*1	CCR0.RIE	不可能
SCIn_RXI (n = 0 to 4, 9)	接收数据已满	CSR.RDRF	CCR0.RIE	Possible
	地址匹配	CSR.DCMF	CCR0.RIE	Possible
SCIn_TXI (n = 0 to 4, 9)	传输数据为空	CSR.TDRE	CCR0.TIE	Possible
	TE=0->1检测			
SCIn_TEI (n = 0 to 4, 9)	发射端	CSR.TEND	CCR0.TEIE	不可能

注1.MER、SYER、PFER和SBER仅在曼彻斯特模式下作为SCIn_ERI中断的一个因素起作用。SYER、PFER和SBER也仅在其启用位（MCR中的SYEREN、PFEREN、SBEREN）设置为1时才起作用。

Table 26.41 选择了FIFO的SCI中断源

Name	中断源	中断标志	中断使能	DTC或DMAC激活
SCIn_ERI (n = 0 to 4, 9)	接收错误	CSR.ORER, CSR.FER, CSR.PER, CSR.DFER, CSR.DPER	CCR0.RIE	不可能
		FRSR.DR (when FCR.DRES = 1)	CCR0.RIE	不可能
SCIn_RXI (n = 0 to 4, 9)	接收数据已满	CSR.RDRF	CCR0.RIE	Possible
	接收数据就绪	FRSR.DR (when FCR.DRES = 0)	CCR0.RIE	Possible
	地址匹配	CSR.DCMF	CCR0.RIE	Possible
SCIn_TXI (n = 0 to 4, 9)	传输数据为空	CSR.TDFE	CCR0.TIE	Possible
	TE=0->1 detection			
SCIn_TEI (n = 0 to 4, 9)	发射端	CSR.TEND	CCR0.TEIE	不可能

26.12.3 智能卡接口模式中的中断

表26.42列出了智能卡接口模式下的中断源。在此模式下不能使用发送结束中断(SCIn_TEI)请求和地址匹配(SCIn_AM)请求。

Table 26.42 智能卡接口模式下的SCI中断源

Name	中断源	中断标志	中断使能	DTC或DMAC激活
SCIn_ERI (n = 0 to 4, 9)	接收错误或错误信号检测	CSR.ORER, CSR.PER, CSR.ERS	CCR0.RIE	不可能
SCIn_RXI (n = 0 to 4, 9)	接收数据已满	CSR.RDRF	CCR0.RIE	Possible
SCIn_TXI (n = 0 to 4, 9)	传输数据为空	CSR.TEND	CCR0.TIE	Possible
	当设置TE=0->1			

在智能卡接口模式下也可以使用DTC或DMAC进行数据传输或接收，类似于正常SCI模式。在发送过程中，当CCR0.TEND标志设置为1时，会产生一个SCIn_TXI中断请求。这个SCIn_TXI中断请求激活DTC或DMAC，如果之前将SCIn_TXI请求指定为DTC或DMAC激活源，则允许传输数据。当DTC或DMAC传输数据时，TEND标志自动设置为0。

如果发生错误，SCI会自动重新传输相同的数据。在重传期间，TEND标志保持为0，并且DTC或DMAC不被激活。因此，SCI和DTC或DMAC会自动传输指定的字节数，包括发生错误后的重传。但是，CSR.ERS标志不会自动设置为

0 at error occurrence. Therefore, the ERS flag must be cleared by previously setting the CCR0.RIE bit to 1 to enable an SCIn_ERI interrupt request to be generated at error occurrence.

When transmitting or receiving data using the DTC or DMAC, always enable the DTC or DMAC before making the SCI settings. For DTC or DMAC settings, see section 16, Data Transfer Controller (DTC), section 15, DMA Controller (DMAC).

In reception, an SCIn_RXI interrupt request is generated when receive data is set to the RDR register. This SCIn_RXI interrupt request activates the DTC or DMAC, allowing transfer of the receive data if the SCIn_RXI request is previously specified as a source of DTC or DMAC activation. If an error occurs, the error flag is set. Therefore, the DTC or DMAC is not activated and an SCIn_ERI interrupt request is issued to the CPU instead. The error flag must be cleared.

26.12.4 Interrupts in Simple IIC Mode

Table 26.43 lists the interrupt sources in simple IIC mode. The STI interrupt is allocated to the transmit end interrupt (SCIn_TEI) request. The receive error interrupt (SCIn_ERI) and the address match (SCIn_AM) request cannot be used.

The DTC or DMAC can also be used to handle transfer in simple IIC mode.

When the ICR.IICINTM bit is 1:

- An SCIn_RXI request is generated on the falling edge of the SCLn signal for the 8th bit. If SCIn_RXI is previously set up as an activation source for the DTC or DMAC, the SCIn_RXI request activates the DTC or DMAC to handle transfer of the received data.
- An SCIn_TXI request is generated on the falling edge of the SCLn signal for the 9th bit (acknowledge bit). If SCIn_TXI is previously set up as an activation source for the DTC or DMAC, the SCIn_TXI request activates the DTC or DMAC to handle transfer of the transmit data.

When the ICR.IICINTM bit is 0:

- An SCIn_RXI request (ACK detection) is generated if the input on the SDAn pin is low on the rising edge of the SCLn signal for the 9th bit (acknowledge bit)
- An SCIn_TXI request (NACK detection) is generated if the input on the SDAn pin is high on the rising edge of the SCLn signal for the 9th bit (acknowledge bit)
- If SCIn_RXI is previously set up as an activation source for the DTC or DMAC, the SCIn_RXI request activates the DTC or DMAC to handle transfer of the received data.

If the DTC or DMAC is used for data transfer in reception or transmission, always set up and enable the DTC or DMAC before setting up the SCI.

When the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits in ICR are used to generate a start condition, restart condition, or stop condition, the STI request is issued when generation is complete.

Table 26.43 SCI interrupt sources in Simple IIC Mode

Name	Interrupt source		Interrupt flag	Interrupt enable	DTC or DMAC activation
	ICR.IICINTM = 1	ICR.IICINTM = 0			
SCIn_RXI (n = 0 to 4, 9)	Reception end	—	—	CCR0.RIE	Possible*1
	—	ACK detection	—		Possible
SCIn_TXI (n = 0 to 4, 9)	Transmission end		—	CCR0.TIE	Possible*1
	—	NACK detection	—		Possible
SCIn_TEI(STIn) (n = 0 to 4, 9)	Completion of generation of a start, restart, or stop condition		ICR.IICSTIF	CCR0.TEIE	Not possible

Note 1. If the DMAC or DTC are being used, you can not confirm whether ACK or NACK.

26.12.5 Interrupts in Simple LIN mode

Table 26.44 lists interrupt sources in Simple LIN mode.

发生错误时为0。因此，必须通过预先将CCR0.RIE位设置为1来清除ERS 标志，以使能在错误发生时产生SCIn_ERI中断请求。

使用DTC或DMAC发送或接收数据时，请务必在进行SCI设置之前启用DTC或DMAC。对于DTC或DMAC设置，请参阅第16节，数据传输控制器(DTC)，第15节，DMA控制器(DMAC)。

在接收中，当接收数据设置到RDR寄存器时，会产生SCIn_RXI中断请求。该SCIn_RXI中断请求激活DTC或DMAC，如果先前将SCIn_RXI请求指定为DTC或DMAC激活源，则允许传输接收数据。如果发生错误，则设置错误标志。因此，不会激活DTC或DMAC，而是向CPU发出SCIn_ERI中断请求。必须清除错误标志。

26.12.4 简单IIC模式下的中断

表26.43列出了简单IIC模式下的中断源。STI中断分配给发送结束中断(SCIn_TEI)请求。不能使用接收错误中断(SCIn_ERI)和地址匹配(SCIn_AM)请求。

DTC或DMAC也可用于处理简单IIC模式下的传输。

当ICR.IICINTM位为1时：

●SCIn_RXI请求在第8位的SCLn信号下降沿产生。如果SCIn_RXI先前设置为DTC或DMAC的激活源，则SCIn_RXI请求将激活DTC或DMAC以处理接收数据的传输。

●SCIn_TXI请求在第9位（确认位）的SCLn信号的下降沿产生。如果SCIn_TXI先前设置为DTC或DMAC的激活源，则SCIn_TXI请求将激活DTC或DMAC以处理传输数据的传输。

当ICR.IICINTM位为0时：

●如果SDAn引脚上的输入在第9位（确认位）的SCLn信号的上升沿为低电平，则生成SCIn_RXI请求（ACK检测）

●如果SDAn引脚上的输入在第9位（确认位）的SCLn信号的上升沿为高电平，则生成SCIn_TXI请求（NACK检测）

●如果先前将SCIn_RXI设置为DTC或DMAC的激活源，则SCIn_RXI请求将激活DTC或DMAC以处理接收数据的传输。

如果DTC或DMAC用于接收或传输中的数据传输，请务必在设置SCI之前设置并启用DTC或DMAC。

当ICR中的IICSTAREQ、IICRSTAREQ和IICSTPREQ位用于生成开始条件、重新启动条件或停止条件时，生成完成时会发出STI请求。

Table 26.43 SimpleIIC模式下的SCI中断源

Name	中断源		中断标志	中断使能	DTC或DMAC激活
	ICR.IICINTM = 1	ICR.IICINTM = 0			
SCIn_RXI (n = 0 to 4, 9)	接待端	—	—	CCR0.RIE	Possible*1
	—	确认检测	—		Possible
SCIn_TXI (n = 0 to 4, 9)	传输端		—	CCR0.TIE	Possible*1
	—	NACK检测	—		Possible
SCIn_TEI(STIn) (n = 0 to 4, 9)	完成启动、重新启动或停止条件的生成		ICR.IICSTIF	CCR0.TEIE	不可能

注1.如果正在使用DMAC或DTC，则无法确认是ACK还是NACK。

26.12.5 简单LIN模式下的中断

表26.44列出了简单LIN模式下的中断源。

Table 26.44 SCI interrupt sources in Simple LIN mode

Name	Interrupt Sources	Interrupt Flag	Flag the needs to be confirmed	Interrupt Enable	DTC/DMAC Activation
SCIn_ERI (n = 0 to 4, 9)	Receive error	CSR.ORER, CSR.FER, CSR.PER	—	CCR0.RIE	Not Possible
		XSR0.BCDF		XCR0.BCDIE	
		XSR0.COF		CCR0.RIE, XCR0.COFIE	
SCIn_RXI (n = 0 to 4, 9)	Receive data full flag	CSR.RDRF	XSR0.CF0MF XSR0.CF1MF XSR0.PIBDF	CCR0.RIE	XSR0.SFSF = 0: Possible XSR0.SFSF = 1: Not Possible
SCIn_AED (n = 0 to 4, 9)	Active edge detection	XSR0.AEDF	—	XCR0.AEDIE	Possible
SCIn_TXI (n = 0 to 4, 9)	Transmit data empty interrupt	CSR.TDRE	—	CCR0.TIE	Possible
	When set TE = 0->1				
	Break Field output completion	XSR0.BFOF		CCR0.TIE, XCR0.BFOIE	
SCIn_TEI (n = 0 to 4, 9)	Transmit end	CSR.TEND	—	CCR0.TEIE	Not Possible
SCIn_BFD (n = 0 to 4, 9)	Break Field Detection	XSR0.BFDF	—	XCR0.BFDIE	Not Possible (Unnecessary)

In Simple LIN mode, in addition to reception errors (ORER, FER, PER), an SCIn_ERI interrupt request is output when a bus conflict is detected during transmission, or when a counter overflow of the Simple LIN module occurs. At this time, a SCIn_RXI interrupt request is not output. The SCIn_ERI interrupt request can be canceled by clearing all the flags.

When transmitting Start Frame, if CCR0.TIE = 1 and XCR0.BFOIE = 1, a SCIn_TXI interrupt request is output when Break Field transmission is completed. When Control Field 0 data is written to the TDR register, data transmission starts. Therefore, transmission using DTC or DMAC is possible.

Set CCR0.TEIE = 1 after writing the last transmit data to the TDR register and transmission starts.

During Start Frame reception (XSR0.SFSF = 1), reception using DTC or DMAC by SCIn_RXI interrupt is not possible. Check the CSR register and XSR0 register, check the reception status (See Figure 26.81), and then clear the flag. Also read the RDR register (if you do not need to check the received data value, clear the RDRF flag without reading the RDR register). When reception of Control Field 1 is completed (XSR0.CF1MF = 1), Start Frame detection is disabled (XSR0.SFSF = 0) and reception using DTC or DMAC is possible. Be sure to read the RDR register.

When Start Frame / Break Field detection is enabled (XCR1.SDST = 1), if a Break Field longer than the period set in XCR2.BFLW [15:0] is received, the BFDF flag is set and a SCIn_BFD interrupt request is output. Then SCI becomes the Start Frame reception state. Clear the BFDF flag.

When Start Frame / Break Field detection is enabled (XCR1.SDST = 1) and the bit rate measurement function is enabled (XCR1.BMEN = 1), an SCIn_AED interrupt factor is output when an active edge is detected. Read the timer count capture value (XSR1.TCNT [15:0]).

26.13 Event Linking

By using interrupt request signals as event signals, the SCIn can provide linked operation through the ELC for modules selected in advance.

Event signals can be output regardless of the values of the associated interrupt request enable bits.

(1) Error event output (receive error or error signal detected) (SCIn_ERI, n = 0 to 4, 9)

- Indicates abnormal termination because of a parity error during reception in asynchronous mode
- Indicates abnormal termination because of a framing error during reception in asynchronous mode
- Indicates abnormal termination because of an overrun error during reception

Table 26.44 简单LIN模式下的SCI中断源

Name	中断源	中断标志	标记需要确认的	中断使能	DTC/DMAC Activation
SCIn_ERI (n = 0 to 4, 9)	接收错误	CSR.ORER, CSR.FER, CSR.PER	—	CCR0.RIE	不可能
		XSR0.BCDF		XCR0.BCDIE	
		XSR0.COF		CCR0.RIE, XCR0.COFIE	
SCIn_RXI (n = 0 to 4, 9)	接收数据满标志	CSR.RDRF	XSR0.CF0MF XSR0.CF1MF XSR0.PIBDF	CCR0.RIE	XSR0.SFSF = 0: 可能的XSR0.SFSF=1：不是 Possible
SCIn_AED (n = 0 to 4, 9)	主动边缘检测	XSR0.AEDF	—	XCR0.AEDIE	Possible
SCIn_TXI (n = 0 to 4, 9)	发送数据空中断	CSR.TDRE	—	CCR0.TIE	Possible
	当设置TE=0->1				
	BreakField输出完成	XSR0.BFOF		CCR0.TIE, XCR0.BFOIE	
SCIn_TEI (n = 0 to 4, 9)	发射端	CSR.TEND	—	CCR0.TEIE	不可能
SCIn_BFD (n = 0 to 4, 9)	断场检测	XSR0.BFDF	—	XCR0.BFDIE	不可能（不必要）

在SimpleLIN模式下，除了接收错误（ORER、FER、PER）外，当在传输过程中检测到总线冲突或发生SimpleLIN模块的计数器溢出时，还会输出SCIn_ERI中断请求。此时，不输出SCIn_RXI中断请求。SCIn_ERI中断请求可以通过清除所有标志来取消。

发送StartFrame时，如果CCR0.TIE=1且XCR0.BFOIE=1，Break时输出SCIn_TXI中断请求现场传输完成。当控制字段0数据写入TDR寄存器时，数据传输开始。因此，可以使用DTC或DMAC进行传输。

将最后一个发送数据写入TDR寄存器并开始发送后，设置CCR0.TEIE=1。

在开始帧接收期间（XSR0.SFSF=1），不能通过SCIn_RXI中断使用DTC或DMAC进行接收。检查CSR寄存器和XSR0寄存器，检查接收状态（见图26.81），然后清除标志。还要读取RDR寄存器（如果不需要检查接收到的数据值，请清除RDRF标志而不读取RDR寄存器）。当控制字段1的接收完成时（XSR0.CF1MF=1），开始帧检测被禁用（XSR0.SFSF=0）并且可以使用DTC或DMAC接收。请务必阅读RDR寄存器。

当启用起始帧中断字段检测(XCR1.SDST=1)时，如果中断字段长于设置的周期接收到XCR2.BFLW[15:0]，设置BFDF标志并输出SCIn_BFD中断请求。那么SCI就变成了开始帧接收状态。清除BFDF标志。

当启动帧中断字段检测启用(XCR1.SDST=1)并启用比特率测量功能(XCR1.BMEN=1)时，当检测到有效边沿时输出SCIn_AED中断因子。读取定时器计数捕获值（XSR1.TCNT[15:0]）。

26.13 事件链接

通过使用中断请求信号作为事件信号，SCIn可以通过ELC为预先选择的模块提供链接操作。

无论相关中断请求使能位的值如何，都可以输出事件信号。

(1) 错误事件输出（接收错误或检测到错误信号）（SCIn_ERI，n=0到4、9）

- ●表示异步模式接收时奇偶校验错误导致异常终止
- ●表示异步模式接收时因帧错误而异常终止
- ●表示接收过程中由于溢出错误而异常终止

- Indicates abnormal termination due to a Manchester error during reception (Only in Manchester mode).
- Indicates that a preface error occurred upon reception and abnormal termination occurred (only in Manchester mode and MCR.PFEREN = 1).
- Indicates that a start bit error occurred during reception and abnormal termination occurred (only in Manchester mode and MCR. SBEREN = 1).
- Indicates that a reception sync error occurred during reception and abnormal termination occurred (only in Manchester mode and only when MCR.SYEREN = 1).
- Indicates detection of the error signal during transmission in smart card interface mode
- The CSR.FER and PER flags are 0, and receive data less than the receive FIFO data trigger number is set in a reception FIFO buffer, and it indicates that 15 ETUs elapse when FIFO is selected and the FCR.DRES bit is 1
- In Simple LIN mode, indicates that the 16-bit counter in the Simple LIN module has overflowed.
- In Simple LIN mode, a bus collision is detected during transmission (CCR0.TE = 1).

(2) Receive data full event output (SCIn_RXI, n = 0 to 4, 9)

- Indicates that ACK is detected if the ICR.IICINTM bit is 0 in simple IIC mode
- Indicates that the 8th-bit SCLn falling edge is detected if the ICR.IICINTM bit is 1 in simple IIC mode
- When the ICR.IICINTM bit is 1 during master transmission in simple IIC mode, set the ELC so that receive data full events are not used

Non-FIFO selected

- Indicates that received data is set in the Receive Data Register (RDR).

FIFO selected

- Using this event output is prohibited.

(3) Transmit data empty event output (SCIn_TXI, n = 0 to 4, 9)

- Indicates that the CCR0.TE bit is changed from 0 to 1
- Indicates that transmission is complete in smart card interface mode
- Indicates that NACK is detected if the ICR.IICINTM bit is 0 in simple IIC mode
- Indicates that the 9th-bit SCLn falling edge is detected if the ICR.IICINTM bit is 1 in simple IIC mode
- In Simple LIN mode, indicates that Break Field output is complete.

Non-FIFO selected

- Indicates that transmit data is transferred from the Transmit Data Register (TDR) to the Transmit Shift Register (TSR).

FIFO selected

- Using this event output is prohibited.

(4) Transmit end event output (SCIn_TEI, n = 0 to 4, 9)

- Indicates the completion of transmission
- Indicates that the starting condition, resumption condition, or termination condition is generated in simple IIC mode
- In Smart Card mode, the transmit end event is not output.

Note: When FIFO is selected, using this event output is prohibited

(5) Address match event output (SCIn_AM, n = 0 to 4, 9)

- Indicates a match of the comparison data (CCR4.CMPD) with one frame of receive data when CCR0.DCME is set to 1 in asynchronous mode, including multi-processor mode.

●表示接收过程中由于曼彻斯特错误导致异常终止（仅在曼彻斯特模式下）。
●表示接收时发生前言错误，发生异常终止（仅限曼彻斯特模式和MCR.PFEREN=1）。
●表示接收过程中发生了起始位错误并发生了异常终止（仅在曼彻斯特模式和MCR.SBEREN=1下）。
●表示接收过程中发生接收同步错误并发生异常终止（仅在曼彻斯特模式下且仅当MCR.SYEREN=1时）。
●指示在智能卡接口模式下传输过程中检测到错误信号
●CSR.FER和每个标志为0，并且接收数据少于接收FIFO数据触发器编号，在接收FIFO缓冲区中设置了，这表明选择FIFO时15ETUSETALESE且FCR.DRES位为1
●在SimpleLIN模式下，表示SimpleLIN模块中的16位计数器已溢出。
●在简单LIN模式下，在传输期间检测到总线冲突（CCR0.TE=1）。

(2) 接收数据满事件输出(SCIn_RXI n=0to4 9)

●简单IIC模式下，如果ICR.IICINTM位为0，则表示检测到ACK
●简单IIC模式下，如果ICR.IICINTM位为1，则表示检测到第8位SCLn下降沿
●简单IIC模式下主机发送期间ICR.IICINTM位为1时，设置ELC以便不使用接收数据满事件

Non-FIFO selected

●表示接收数据设置在接收数据寄存器(RDR)中。

FIFO selected

●禁止使用该事件输出。

(3) 发送数据空事件输出（SCIn_TXI n=0to4 9）

●表示CCR0.TE位由0变为1
●表示在智能卡接口模式下传输完成
●简单IIC模式下，如果ICR.IICINTM位为0，则表示检测到NACK
●简单IIC模式下ICR.IICINTM位为1表示检测到第9位SCLn下降沿
●在SimpleLIN模式下，表示BreakField输出完成。

Non-FIFO selected

●表示发送数据从发送数据寄存器(TDR)传送到发送移位寄存器(TSR)。

FIFO selected

●禁止使用该事件输出。

(4) 发送结束事件输出(SCIn_TEI n=0to4 9)

●表示传输完成
●表示在简单IIC模式下产生启动条件、恢复条件或终止条件
●SmartCard模式下，不输出发送结束事件。

Note: 选择FIFO时，禁止使用该事件输出

(5) 地址匹配事件输出(SCIn_AM n=0to4 9)

●在异步模式（包括多处理器模式）下，当CCR0.DCME置1时，表示比较数据（CCR4.CMPD）与一帧接收数据匹配。

(6) Active edge detection event output

- In Simple LIN mode, when CCR1.BMEN is 1, it indicates that a valid edge has been detected in the RXD input signal.

26.14 Address Non-match Event Output (SCI0_DCUF)

SCI0_DCUF indicates the non-match of comparison data (CCR4.CMPD) with receive data that is one frame of the data that is received when CCR0.DCME is set to 1 in asynchronous mode, including multi-processor mode. This event can be used for Snooze end request only. In detail, see section 10, Low Power Modes.

26.15 Noise Cancellation Function

Figure 26.111 shows the configuration of the noise filter used for noise cancellation. The noise filter consists of a 2-stage flip-flop circuit and a match detection circuit. When the input signals of the noise filter and the output signals of the 2- stage flip-flop circuits completely match, the matched level is conveyed as an internal signal. Unless otherwise matched, the previous value is retained. When the same level is retained for 3 cycles or longer on the sampling clock of the noise filter, it is considered as a valid receive signal. A change in pulse for 3 cycles or shorter is considered as noise, not as a receive signal.

In asynchronous mode, Manchester and Simple LIN modes, the noise cancellation function can be applied to the receive signal input to the RXDn pin. The sampling period of the noise filter can be selected from the base clock period and the divided clock of the baud rate generator clock source by CCR1.NFCS[2:0].

- When CCR1.NFCS[2:0] = 000b, CCR2.ABCS = 0 and CCR2.ABCSE = 0, the cycle is 1/16 of a 1-bit period.
- When CCR1.NFCS[2:0] = 000b, CCR2.ABCS = 1 and CCR2.ABCSE = 0, the cycle is 1/8 of a 1-bit period.
- When CCR1.NFCS[2:0] = 000b, CCR2.ABCSE = 1, the cycle is 1/6 of a 1-bit period.

In simple IIC mode, this function can be used for each input on SDAn and SCLn. The sampling clock is selected from divided clock of baud rate generator settings by CCR1.NFCS[2:0].

If the base clock is stopped once with the noise filter enabled and then the base clock input is restarted again, the noise filter operation resumes from the state where the clock was stopped. When CCR0.TE and CCR0.RE are set to 0 during base clock input, all of the noise filter flip-flop values are initialized to 1. Accordingly, if the input data is 1 when reception operation resumes, the function determines that a level match is detected and the result is conveyed as an internal signal. When the level being input corresponds to 0, the initial output of the noise filter is retained until the level matches in three consecutive sampling cycles.

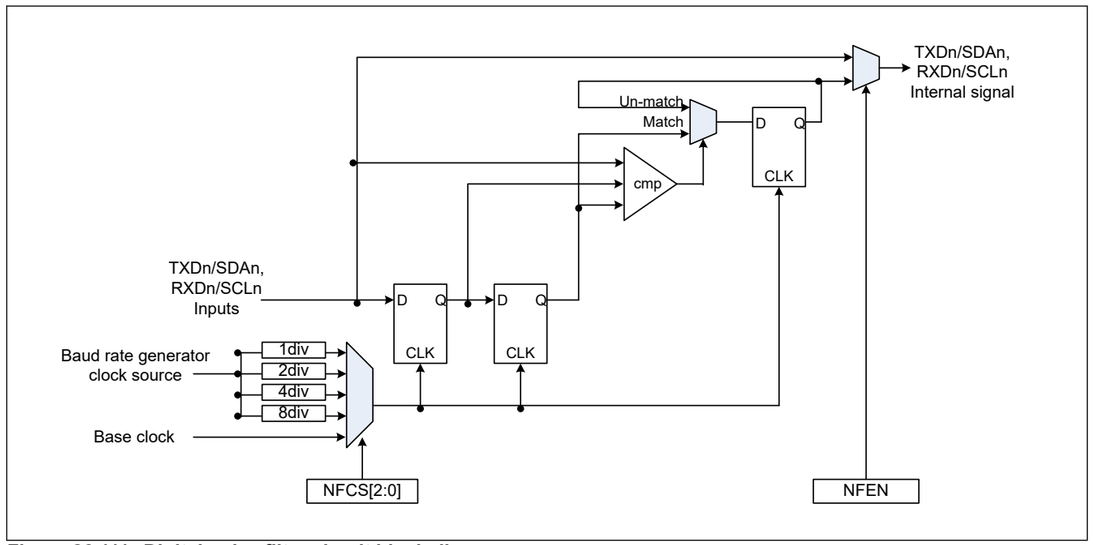


Figure 26.111 Digital noise filter circuit block diagram

(6) 主动边缘检测事件输出

●在SimpleLIN模式下，当CCR1.BMEN为1时，表示在RXD输入信号中检测到有效边沿。

26.14 地址不匹配事件输出(SCI0_DCUF)

SCI0_DCUF表示比较数据（CCR4.CMPD）与接收数据不匹配，接收数据是在异步模式（包括多处理器模式）下CCR0.DCME设置为1时接收到的数据的一帧。此事件仅可用于贪睡结束请求。详细信息，请参见第10节，低功耗模式。

26.15 降噪功能

图26.111显示了用于噪声消除的噪声滤波器的配置。噪声滤波器由一个2级触发器电路和一个匹配检测电路组成。当噪声滤波器的输入信号和2级触发器电路的输出信号完全匹配时，匹配的电平作为内部信号传送。除非另有匹配，否则将保留先前的值。当相同电平在噪声滤波器的采样时钟上保持3个周期或更长时间时，它被认为是有效的接收信号。3个周期或更短的脉冲变化被认为是噪声，而不是接收信号。

在异步模式、曼彻斯特模式和简单LIN模式下，噪声消除功能可应用于输入到RXDn引脚的接收信号。噪声滤波器的采样周期可以通过CCR1.NFCS[2:0]从基础时钟周期和波特率发生器时钟源的分频时钟中选择。

●当CCR1.NFCS[2:0]=000b、CCR2.ABCS=0和CCR2.ABCSE=0时，周期为1位周期的116。
●当CCR1.NFCS[2:0]=000b、CCR2.ABCS=1和CCR2.ABCSE=0时，周期为1位周期的18。
●当CCR1.NFCS[2:0]=000b，CCR2.ABCSE=1时，周期为1位周期的16。

在简单IIC模式下，该功能可用于SDAn和SCLn上的每个输入。采样时钟由CCR1.NFCS[2:0]从波特率发生器设置的分频时钟中选择。

如果在启用噪声滤波器的情况下基准时钟停止一次，然后再次重新启动基准时钟输入，则噪声滤波器操作将从时钟停止的状态恢复。当CCR0.TE和CCR0.RE在基本时钟输入期间设置为0时，所有噪声滤波器触发器值都被初始化为1。因此，如果在接收操作恢复时输入数据为1，则该函数确定一个电平检测到匹配并将结果作为内部信号传送。当输入的电平对应于0时，保留噪声滤波器的初始输出，直到电平在三个连续的采样周期中匹配。

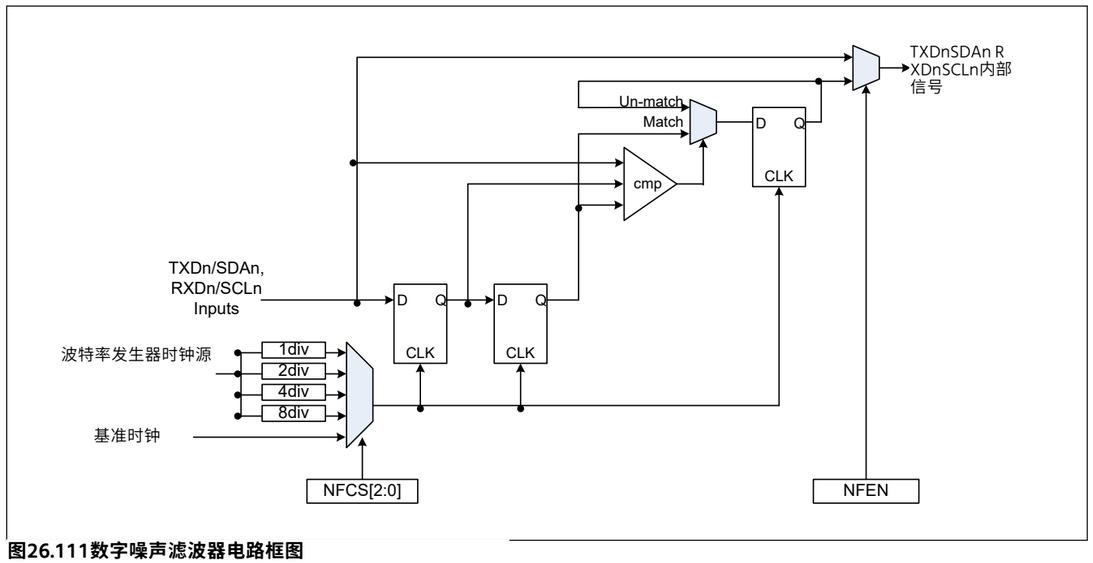


图26.111数字噪声滤波器电路框图

26.16 RS-485 Driver Control Function

Setting the DEN bit in the SCI common control register3 (CCR3) to 1 enables the RS-485 driver control function and generates a DEn (Driver Enable) signal that enables the external transceiver transmission mode. The DEn signal outputs a valid level for the period with driver assertion time and driver negate time added before and after data transmission. The DEn signal valid level is set by the DEPOL bit in the driver control register (DCR).

The driver assertion time is the time from when the DEn signal is valid until the start bit starts. Set by DEAST [4:0] of driver control register (DCR).

The driver negate time is the time from the end of the last stop bit of the transmitted message to the invalidation of the DEn signal. Set with DENGT [4:0] of the driver control register (DCR).

DEAST and DENGT are expressed in base clock period (1/8 or 1/16 bit period). For details, refer to section 26.2.13. DCR : Driver Control Register.

When this function is used (CCR3.DEN = 1), the CSR.TEND set timing and SCIn_TEI interrupt output timing are at the end of the driver negation time.

When transmission is completed and the next transmission data is not written before the DEn signal is negated, the DEn signal is negated once. If the timing for writing the next transmit data is not in time, assert the DEn signal after negating it again, insert the driver assertion time, and transmit the next data. If you want to perform the next transmission with the DEn signal asserted, write the next transmission data to the TDR quickly enough in consideration of the synchronization delay time of the register.

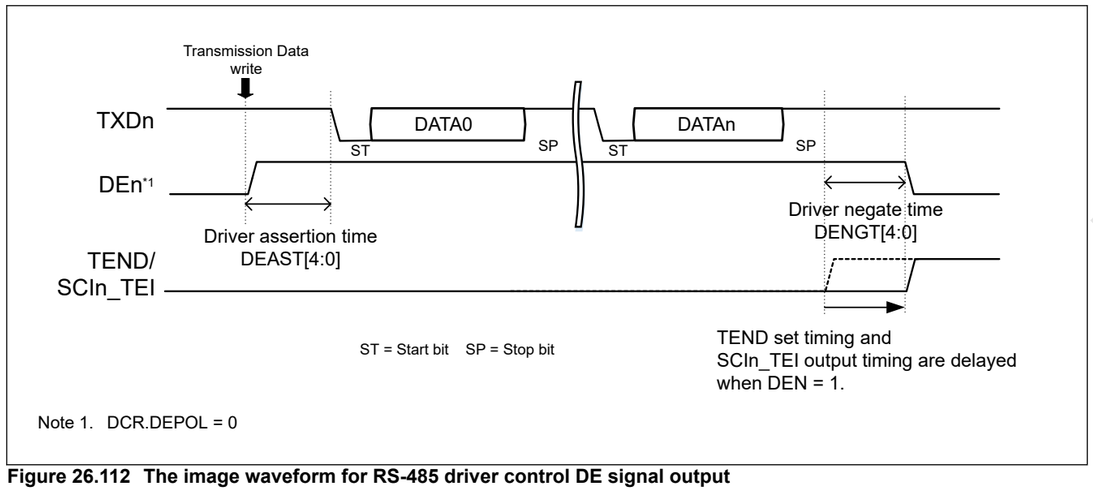


Figure 26.112 The image waveform for RS-485 driver control DE signal output

26.17 Loopback Function

The loopback function can be used in Asynchronous mode with the internal clock, and Manchester mode with the internal clock, and Clock synchronous mode with the internal clock.

When 1 is written to the SPLP bit in the CCR1 register, SCI blocks the external input (RXDn) path and connects the output path of the transmit data register and the input path of the receive data register.

When this function is used with TINV bit = 1, inversion of transmission data becomes reception data. However, this function can be used with TINV = 1 only when operating in clock synchronous mode internal clock.

Table 26.45 shows the relationship between the TINV and SPLP bit settings and the received data.

26.16 RS-485驱动控制功能

将SCI公共控制寄存器3(CCR3)中的DEN位设置为1，启用RS-485驱动器控制功能，并生成启用外部收发器传输模式的DEn(DriverEnable)信号。DEn信号在数据传输前后添加驱动器断言时间和驱动器否定时间的周期内输出有效电平。DEn信号有效电平由驱动控制寄存器(DCR)中的DEPOL位设置。

驱动器断言时间是从DEn信号有效到起始位开始的时间。由驱动控制寄存器(DCR)的DEAST[4:0]设置。

驱动器取反时间是从传输消息的最后一个停止位结束到DEn信号无效的时间。使用驱动控制寄存器(DCR)的DENGT[4:0]设置。

DEAST和DENGT以基本时钟周期（18或116位周期）表示。有关详细信息，请参阅第26.2.13节。直流电阻：驱动程序控制寄存器。

使用此功能时（CCR3.DEN=1），CSR.TEND设置时序和SCIn_TEI中断输出时序在驱动器取反时间结束。

当发送完成并且在DEn信号被取反之前没有写入下一个发送数据时，DEn信号被取反一次。如果写入下一个发送数据的时序不及时，再次取反后置位DEn信号，插入驱动器置位时间，发送下一个数据。如果要在DEn信号置位的情况下执行下一次传输，考虑到寄存器的同步延迟时间，将下一次传输数据足够快地写入TDR。

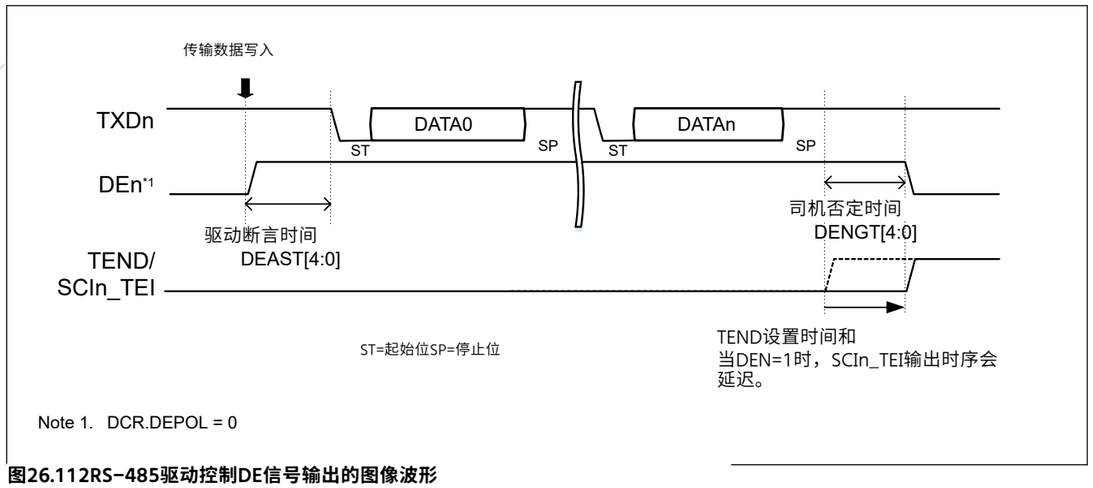


图26.112RS-485驱动控制DE信号输出的图像波形

26.17 Loopback Function

环回功能可用于带内部时钟的异步模式、带内部时钟的曼彻斯特模式和带内部时钟的时钟同步模式。

当向CCR1寄存器中的SPLP位写入1时，SCI会阻塞外部输入(RXDn)路径并连接发送数据寄存器的输出路径和接收数据寄存器的输入路径。

当TINV位=1使用此功能时，发送数据的反相变为接收数据。但是，只有在时钟同步模式内部时钟下运行时，才能在TINV=1时使用此函数。

表26.45显示了TINV和SPLP位设置与接收数据之间的关系。

Table 26.45 TINV and SPLP bit settings and received data

CCR1.TINV	CCR1.SPLP	Receive Data	Communication mode		
			Asynchronous	Manchester	Clock synchronous
			internal clock	internal clock	internal clock
—	0	Receive Data from RXDn terminal	Possible	Possible	Possible
0	1	Transmit Data	Possible	Possible	Possible
1	1	Inverted transmit data	Impossible	Impossible	Possible

Note: —: don't care

Figure 26.113 shows the configuration of the shift register input / output path in loopback mode.

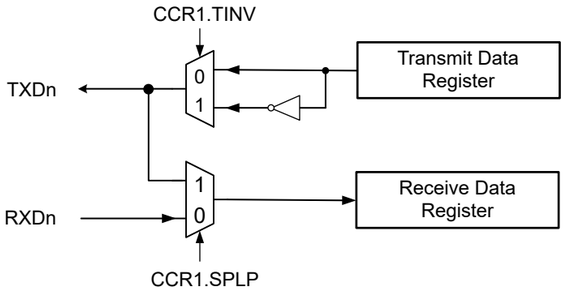


Figure 26.113 Shift register input output configuration image in loopback mode

26.18 Half-Duplex communication Function

Do not use the half-duplex communication function in Simple IIC, Simple SPI and Smart Card Interface modes.

In other communication modes, if the CCR1.SHARPS bit is set to 1, half-duplex communication using the TXDn pin is possible. When half-duplex communication is used, transmission and reception must be performed exclusively. Transmission and reception settings (CCR0.TE = 1 and CCR0.RE = 1) is prohibited.

However, if half-duplex communication is performed as the master reception in clock synchronous mode, perform transmission / reception settings (CCR0.TE = 1 and CCR0.RE = 1) and perform dummy transmission. By dummy transmission (arbitrary transmission data is written to TDR), SCKn is output and reception is enabled. The dummy transmission data is discarded inside the IP and is not actually transmitted.

During half-duplex communication, the only communication port terminal used is the TXDn terminal. Output when CCR0.TE = 1, input when CCR0.TE = 0.

26.19 Synchronizer Bypass Function

The SCI has a bus clock and the operation clock (TCLK). And these have each operating circuit. Therefore, there is a synchronization circuit for signal transfer between different clocks, and synchronization delay time is required for signal propagation between different clocks.

However, the synchronization circuit can be bypassed by the CCR3.BPEN bit only when the same clock is input to the bus clock and the operation clock. In this case, eliminates synchronization delay time and improves responsiveness. Figure 26.114 shows the image waveform of the bypass function.

This IP also has a synchronization circuit between the communication clock (SCKn) and the operation clock (TCLK), but this synchronization circuit cannot be bypassed.

Table 26.45 TINV和SPLP位设置和接收数据

CCR1.TINV	CCR1.SPLP	接收数据	通讯方式		
			Asynchronous	Manchester	时钟同步
			内部时钟	内部时钟	内部时钟
—	0	从RXDn终端接收数据	Possible	Possible	Possible
0	1	传输数据	Possible	Possible	Possible
1	1	反相传输数据	Impossible	Impossible	Possible

Note: ——：不在乎

图26.113显示了环回模式下移位寄存器输入输出路径的配置。

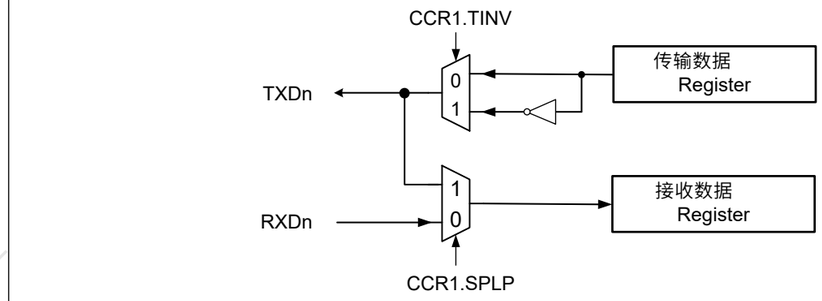


图26.113环回模式下的移位寄存器输入输出配置图

26.18 半双工通信功能

请勿在SimpleIIC、SimpleSPI和SmartCardInterface模式下使用半双工通信功能。

在其他通信模式下，如果CCR1.SHARPS位设置为1，则可以使用TXDn引脚进行半双工通信。当使用半双工通信时，必须专门进行发送和接收。禁止发送和接收设置（CCR0.TE=1和CCR0.RE=1）。

但是，如果在时钟同步模式下作为主机接收执行半双工通信，则执行发送接收设置（CCR0.TE=1和CCR0.RE=1）并执行虚拟发送。通过虚拟传输（将任意传输数据写入TDR），输出SCKn并启用接收。虚拟传输数据在IP内部被丢弃，并不实际传输。

在半双工通信期间，唯一使用的通信端口端子是TXDn端子。输出时CCR0.TE=1，当CCR0.TE=0时输入。

26.19 同步器旁路功能

SCI有一个总线时钟和一个操作时钟（TCLK）。这些都有各自的操作电路。因此，不同时钟之间的信号传输存在同步电路，不同时钟之间的信号传播需要同步延迟时间。

但是，只有在总线时钟和操作时钟输入相同的时钟时，才能通过CCR3.BPEN位绕过同步电路。在这种情况下，消除了同步延迟时间并提高了响应能力。图26.114显示了旁路功能的图像波形。

该IP在通信时钟(SCKn)和操作时钟(TCLK)之间也有一个同步电路，但该同步电路无法绕过。

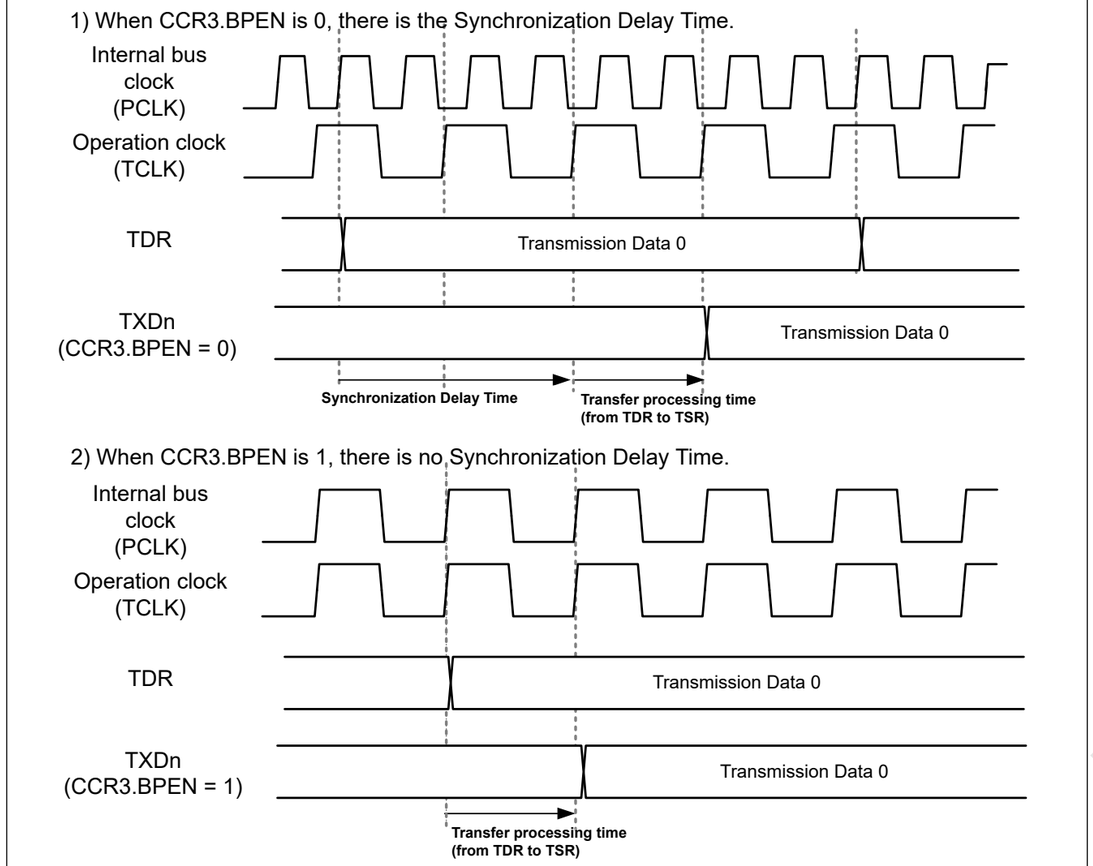


Figure 26.114 Image waveform of Synchronizer bypass function

26.20 Usage Notes

26.20.1 Settings for the Module-Stop Function

The Module Stop Control Register B (MSTPCRB) can enable or disable SCI operation. The SCI is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

26.20.2 SCI Operation during Low Power State

(1) Transmission

Before using the power consumption reduction function to reduce SCI's power consumption, please do the following to confirm transmission end (CSR.TEND = 1):

- Set the output terminal state after transmission operation is stopped by CCR1.SPB2DT, SPB2IO.
- Stop the transmission (CCR0.TIE = 0, TE = 0, TEIE = 0)

When transitions to these states are made during transmission, the data being transmitted become indeterminate.

To transmit data in the same transmission mode after cancellation of the low power consumption state, set the TE bit to 1, read CSR, and write data to TDR sequentially to start data transmission. To transmit data with a different transmission mode, initialize the SCI first.

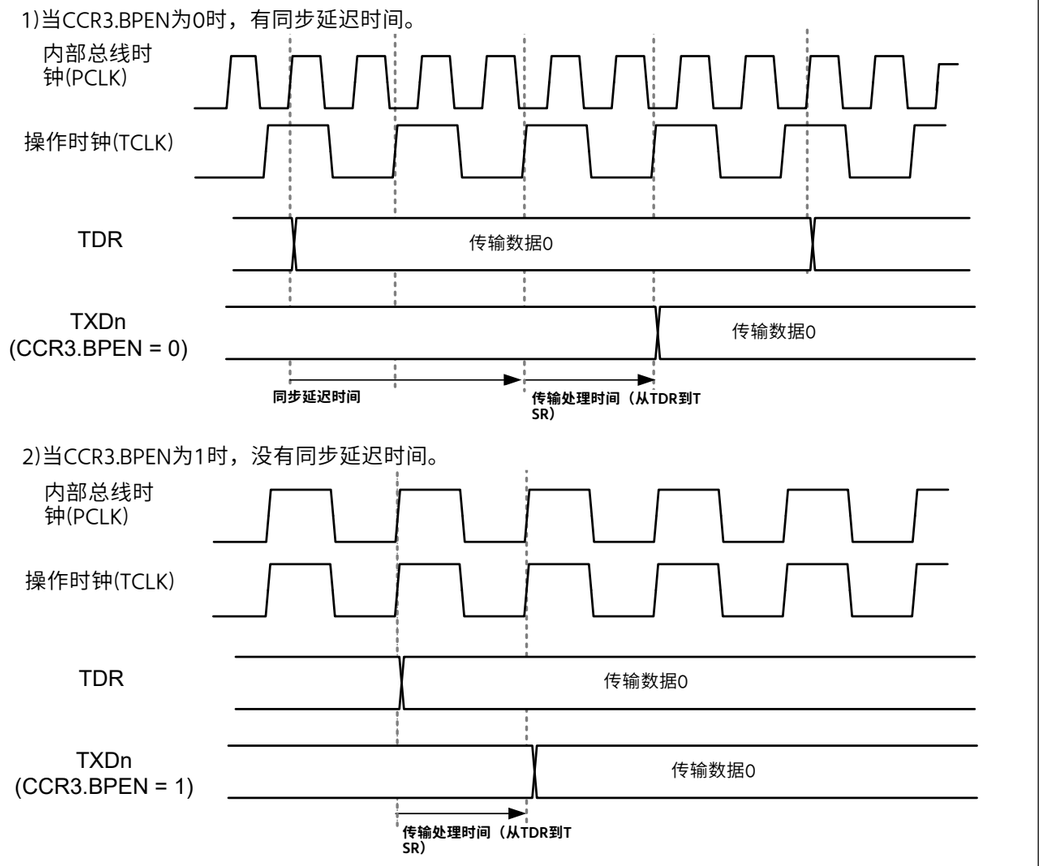


图26.114同步器旁路功能的图像波形

26.20 使用说明

26.20.1 模块停止功能的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用SCI操作。SCI在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

26.20.2 低功耗状态下的SCI操作

(1) Transmission

在使用功耗降低功能降低SCI的功耗之前，请执行以下操作以确认发送结束（CSR.TEND=1）：

●通过CCR1.SPB2DT、SPB2IO设置发送操作停止后的输出端子状态。
●停止传输（CCR0.TIE=0，TE=0，TEIE=0）

在传输过程中转换到这些状态时，正在传输的数据变得不确定。

要在取消低功耗状态后以相同的传输模式传输数据，请将TE位设置为1，读取CSR，然后将数据依次写入TDR以开始数据传输。要以不同的传输模式传输数据，请先初始化SCI。

To start transmission using the DMAC/DTC after cancellation from software standby mode, set the CCR0.TE and CCR0.TIE bit to at the same time. Then SCIn_TXI interrupt flag is generated, which causes the DMAC/DTC to write the transmit data, which starts transmission.

Figure 26.115 shows a sample flowchart for transition to software standby mode during transmission. Figure 26.116 and Figure 26.117 show the port pin states during transition to software standby mode.

(2) Reception

When Address match function is non used as condition of resumption (wake-up)

Before specifying the module stop state or making a transition to software standby mode, stop the receive operations (CCR0.RE = 0). If transition is made during data reception, the data being received will be invalid.

Figure 26.118 shows a sample flowchart for reception to software standby mode during reception.

When Address match function is used as condition of resumption (wake-up)

When using the power consumption reduction function to reduce SCI's power consumption, please do the following:

- Set the operation mode to asynchronous mode, after released
- Set the compare data to CCR4.CMPD and set 1 to CCR0.DCME
- Set the receive operation (CCR0.RE = 1)

Please set CCR3.RXDESEL = 0. Because there is a possibility that a start bit (fall edge of RXDn terminal) can't be detected at the time of low power consumption mode release.

After detecting the falling edge of the RXDn terminal and transitioning from standby mode to snooze mode, the operating clock is supplied to SCI and data is received by SCI. The address match function determines the received data, and if it matches, it transitions from snooze mode to normal mode, and if it does not match, it transitions to standby mode again. This operation behaves as if the standby mode is continued until the communication data matching the CMPD is received, and after the standby mode is released, the normal reception operation is continued.

When using this function, the reception speed must be slow enough because it is necessary to perform the transition from the fall detection of the RXDn terminal to the snooze mode, and from the clock supply to the SCI to the reception.

Figure 26.119 shows a sample flowchart for reception to software standby mode during reception.

要在从软件待机模式取消后使用DMACDTC开始传输，请设置CCR0.TE和CCR0.TIE位同时。然后产生SCIn_TXI中断标志 ，使DMACDTC写入发送数据，开始发送。

图26.115显示了传输期间转换到软件待机模式的示例流程图。图26.116和图26.117显示了转换到软件待机模式期间的端口引脚状态。

(2) Reception

不使用地址匹配功能作为恢复条件时（唤醒）

在指定模块停止状态或转换到软件待机模式之前，停止接收操作(CCR0.RE=0)。如果在数据接收过程中进行转换，正在接收的数据将无效。

图26.118显示了在接收期间接收到软件待机模式的示例流程图。

当地址匹配功能用作恢复条件时（唤醒）

使用功耗降低功能降低SCI的功耗时，请执行以下操作：

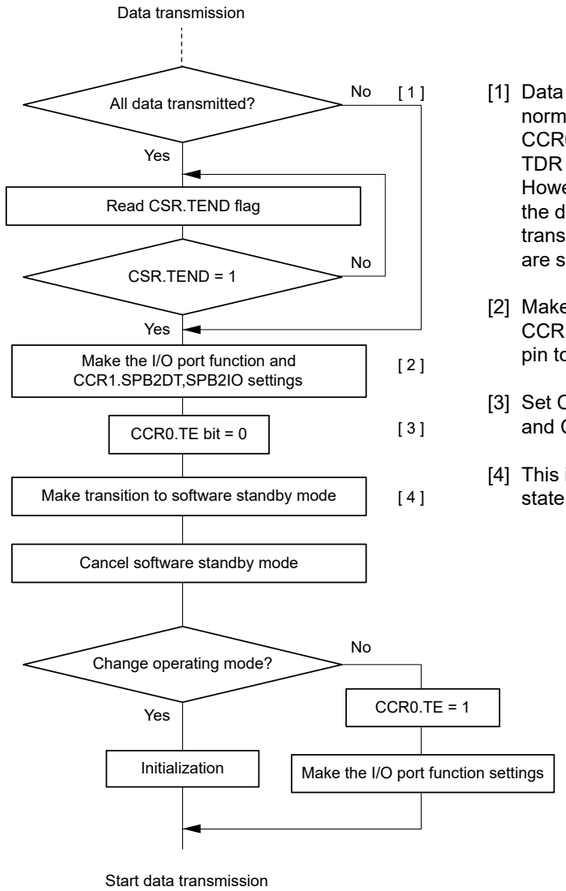
- ●设置操作模式为异步模式，释放后
- ●将比较数据设置为CCR4.CMPD，将1设置为CCR0.DCME
- ●设置接收操作（CCR0.RE=1）

请设置CCR3.RXDESEL=0。因为在低功耗模式释放时可能无法检测到起始位（RXDn端子的下降沿）。

在检测到RXDn端子的下降沿并从待机模式转换到贪睡模式后，工作时钟被提供给SCI，数据由SCI接收。地址匹配功能确定接收到的数据，如果匹配，则从贪睡模式过渡到正常模式，如果不匹配，则再次过渡到待机模式。在接收到与CMPD匹配的通信数据之前，该操作表现为继续待机模式，在解除待机模式后，继续正常接收操作。

使用此功能时，接收速度必须足够慢，因为需要执行从RXDn端子的下降检测到贪睡模式的转换，以及从时钟供应到SCI到接收的转换。

图26.119显示了在接收期间接收到软件待机模式的示例流程图。



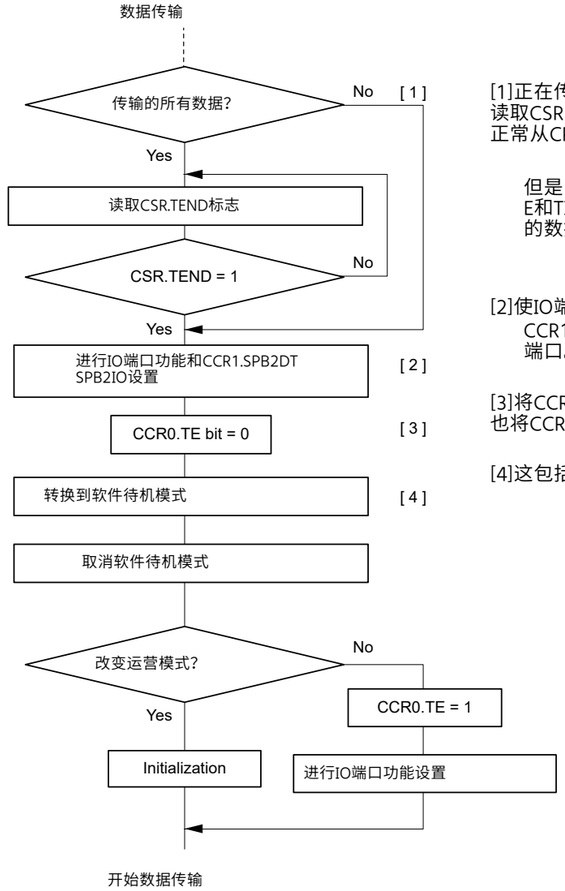
[1] Data being transmitted is lost halfway. Data can be normally transmitted from the CPU by setting the CCR0.TE to “1”, reading CSR, and writing data to TDR after canceling software stand by mode. However, if the DMAC or DTC has been activated, the data remaining in the DMAC or DTC will be transmitted when both the TE and TIE bits in CCR0 are set to “1”.

[2] Make the I/O port function and CCR1.SPB2DT,SPB2IO settings to switch the TxDn pin to operate as a general I/O port.

[3] Set CCR0.TE bit to “0”. Set also 0 to CCR0.TIE and CCR0.TEIE if you set these bits were 1.

[4] This includes the setting for the module stopped state.

Figure 26.115 Example of Flowchart for Transition to Software Standby Mode during Transmission



[1]正在传输的数据中途丢失。通过设置CCR0.TE为“1”，读取CSR，取消软件待机模式后将数据写入TDR，可以正常从CPU传输数据。

但是，如果DMAC或DTC已被激活，则当CCR0中的TE和TIE位都设置为“1”时，将发送DMAC或DTC中剩余的数据。

[2]使IO端口功能和
CCR1.SPB2DT SPB2IO设置将TxDn引脚切换为通用IO端口。

[3]将CCR0.TE位设置为“0”。如果将这些位设置为1，也将CCR0.TIE和CCR0.TEIE设置为0。

[4]这包括模块停止状态的设置。

图26.115传输期间转换到软件待机模式的流程图示例

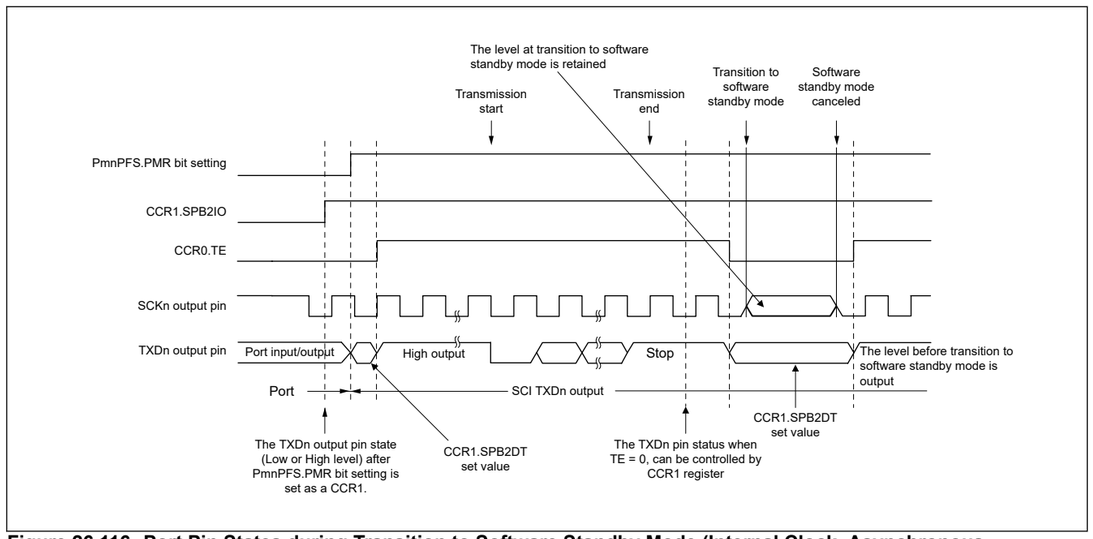


Figure 26.116 Port Pin States during Transition to Software Standby Mode (Internal Clock, Asynchronous Transmission)

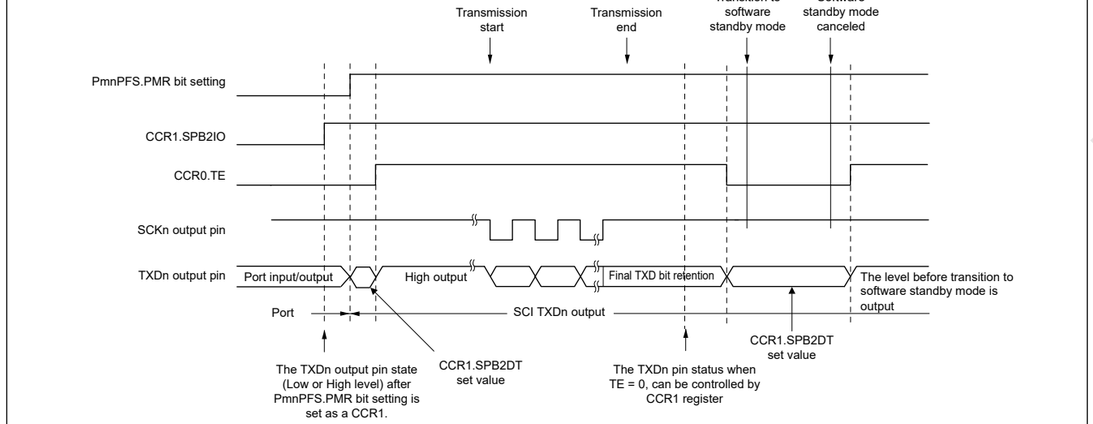


Figure 26.117 Port Pin States during Transition to Software Standby Mode (Internal Clock, Clock Synchronous Transmission)

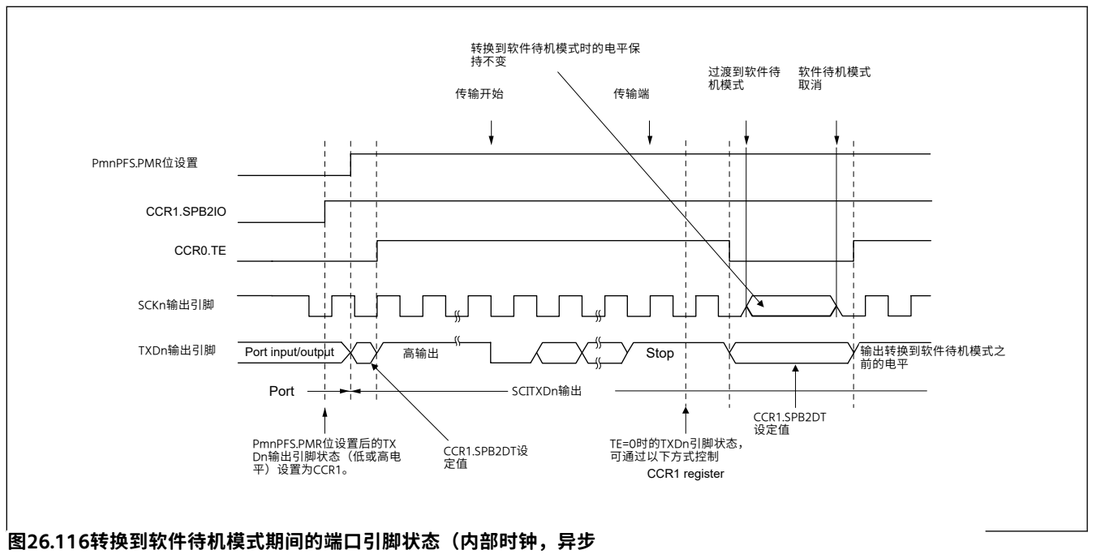


图26.116转换到软件待机模式期间的端口引脚状态（内部时钟，异步 Transmission)

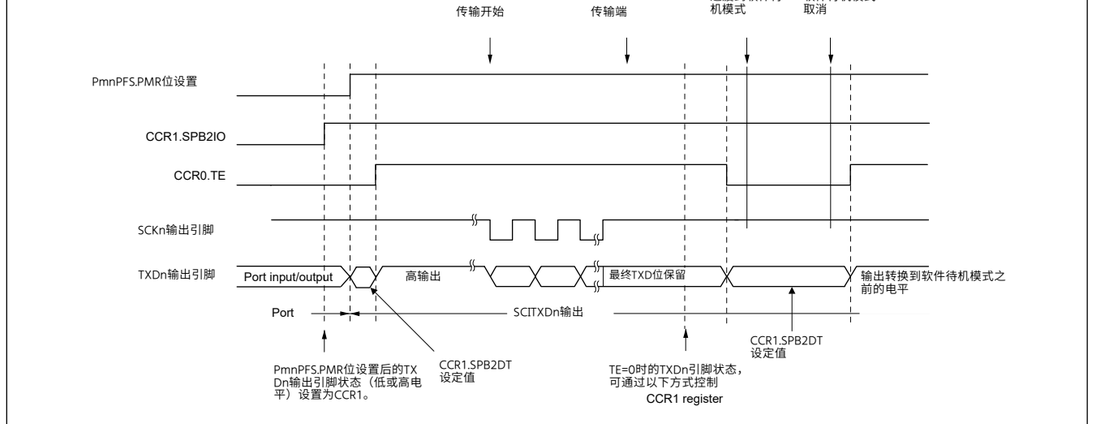
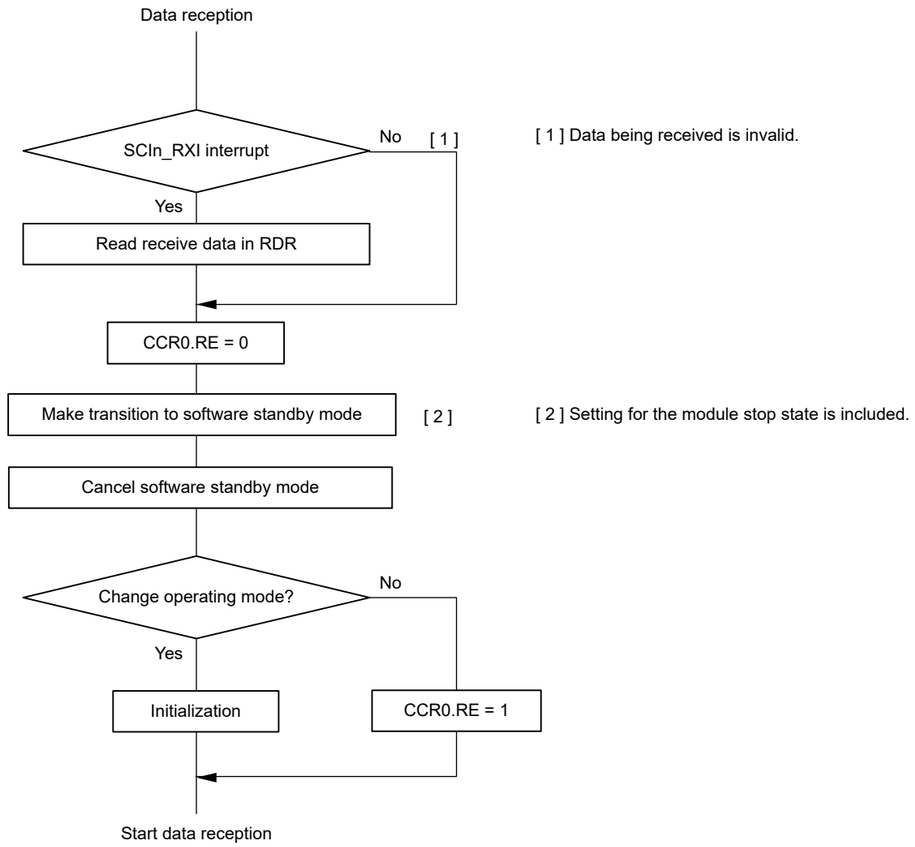


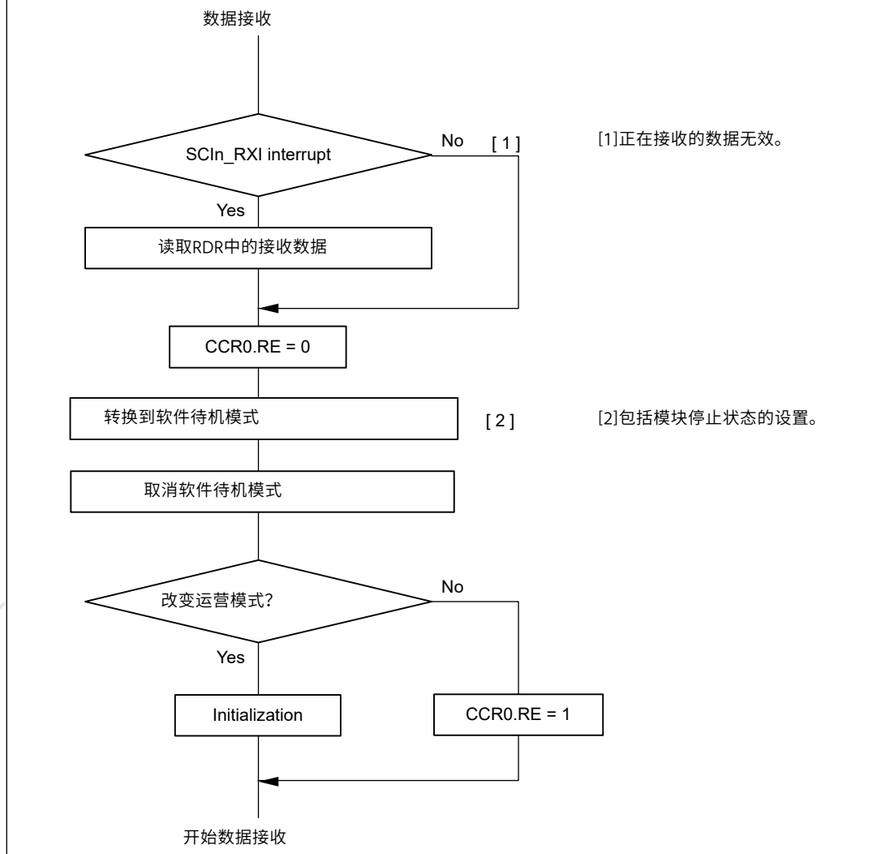
图26.117转换到软件待机模式期间的端口引脚状态（内部时钟、时钟 Synchronous Transmission)



[1] Data being received is invalid.

[2] Setting for the module stop state is included.

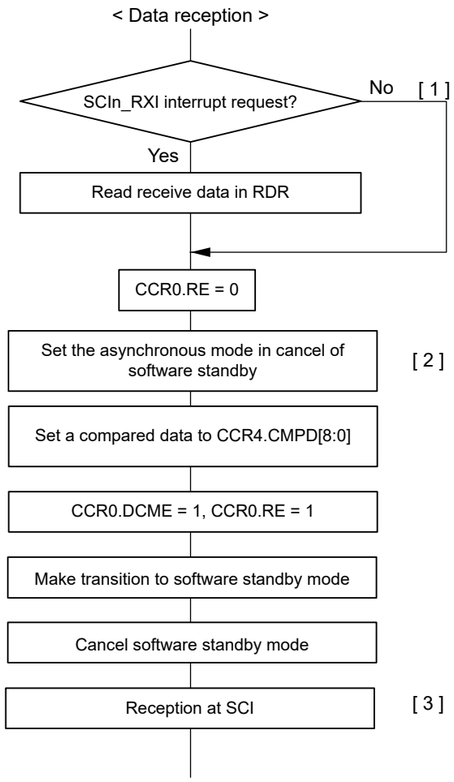
Figure 26.118 Example of Flowchart for Reception to Software Standby Mode during Reception



[1]正在接收的数据无效。

[2]包括模块停止状态的设置。

图26.118接收期间接收到软件待机模式的流程图示例



[1] Data being received is invalid.

[2] The address match feature is only available in asynchronous mode.

[3] The adress match function operates in snooze mode, and when the received data matches the CCR4.CMPD, the standby mode is canceled and the normal reception standby state is set.

Figure 26.119 Example of Flowchart for Reception to Software Standby Mode during Reception with Address match

26.20.3 Break Detection and Processing

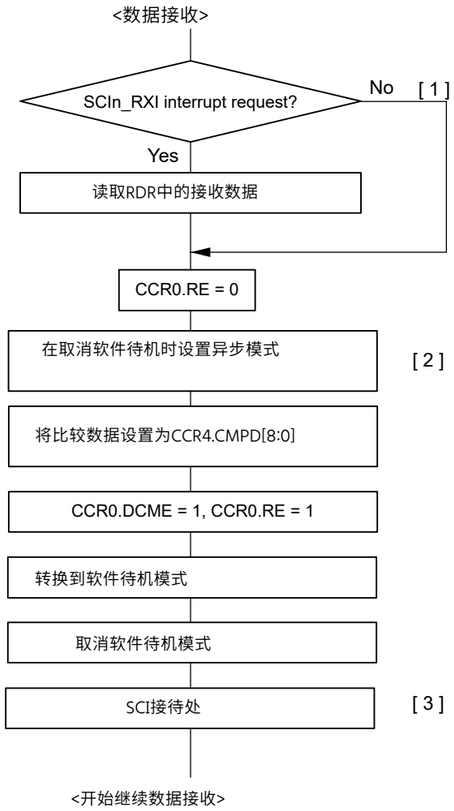
(1) Non-FIFO selected

When a framing error is detected, a break can be detected by reading CSR.RXDMON bit value. In a break, the input from the RXDn pin becomes all 0s, and the CSR.FER flag is set to 1 to indicate a framing error, and the CSR.PER flag might also be set to 1 to indicate a parity error. The SCI continues the receive operation even after a break is received. Therefore, even if the FER flag is 0, indicating that no framing error occurred, it is set to 1 again. When the CCR3.RXDESEL bit is 1, the SCI sets the CSR.FER flag to 1 and stops receiving operations until a start bit of the next data frame is detected. If the CSR.FER flag is set to 0, the CSR.FER flag retains 0 during the break.

When the RXDn pin is set to 1 and the break ends, detecting the beginning of the start bit on the first falling edge of the RXDn pin allows the SCI to start the receiving operation.

(2) FIFO selected

After a framing error is detected and when the SCI detects that continuous receive data is 0 for 1 frame, reception stops. When a framing error is detected, a break can be detected by reading the CSR.RXDMON flag value. After the RXDn signal is in high and the break is finished, data reception to the receive-FIFO (RDR) register resumes.



[1]正在接收的数据无效。

[2]地址匹配功能仅在异步模式。

[3]地址匹配功能在贪睡模式，当接收到的数据与CCR4.CMPD匹配时，取消待机模式并设置正常接收待机状态。

图26.119在地址匹配的接收期间接收到软件待机模式的流程图示例

26.20.3 断裂检测和处理

(1) Non-FIFO selected

当检测到帧错误时，可以通过读取CSR.RXDMON位的值来检测中断。在中断时，来自RXDn引脚的输入变为全0，并且CSR.FER标志设置为1表示帧错误，CSR.PER标志也可能设置为1表示奇偶校验错误。即使在收到中断后，SCI仍继续接收操作。因此，即使FER标志为0，表示没有发生帧错误，它也会再次设置为1。当CCR3.RXDESEL位为1时，SCI将CSR.FER标志设置为1并停止接收操作，直到检测到下一个数据帧的起始位。如果

CSR.FER标志设置为0，CSR.FER标志在中断期间保持0。

当RXDn引脚设置为1且中断结束时，在第一个下降沿检测起始位的开始
RXDn引脚允许SCI开始接收操作。

(2) FIFO selected

检测到帧错误后，当SCI检测到1帧连续接收数据为0时，接收停止。
当检测到帧错误时，可以通过读取CSR.RXDMON标志值来检测中断。在RXDn信号为高电平且中断完成后，接收FIFO(RDR)寄存器的数据接收恢复。

26.20.4 Mark State and Production of Breaks

When the CCR0.TE bit is 0, disabling serial transmission, the state of the TXDn pin can be set using the CCR1.SPB2IO and CCR1.SPB2DT bits. With this approach, a TXDn pin can be placed in the mark state to transmit a break.

Before setting the CCR0.TE bit to 1, enabling serial transmission, set the SPB2IO and SPB2DT bits to put the communication line in the mark state (the state of 1), and change the TXDn pin using I/O port function. To output a break on data transmission, after setting the TXDn pin to output 0 by setting the SPB2IO and SPB2DT bits, change the TXDn pin using the I/O port function and set the CCR0.TE bit to 0. When the CCR0.TE bit is set to 0, the transmitter is initialized regardless of the current state of transmission.

26.20.5 Receive Error Flags and Transmit Operations (Clock Synchronous Mode and Simple SPI Mode)

Transmission can be start by writing transmit-data to TDR even if CSR.ORER is 1. However, reception cannot be started. Note also that the receive error flags cannot be set to 0 even if the CCR0.RE is set to 0 (serial reception is disabled).

26.20.6 Writing Data to TDR

(1) Non-FIFO selected

Data can be written to TDR anytime when CCR0.TE is 1. However, if new data is written to TDR when transmit data is remaining in TDR, the previous data in TDR is lost because it has not been transferred to TSR yet. If you use DTC or DMAC, be sure to write transmit data to TDR in the SCIn_TXI interrupt request handling routine.

(2) FIFO selected

Data can be written to transmit-FIFO(TDR) when CCR0.TE is 1. Check the number of writable data with the FTSR.T [5:0] bit.

26.20.7 Restrictions on Clock Synchronous Transmission (Clock Synchronous Mode and Simple SPI Mode)

When the external clock source is used as a synchronization clock, the following restrictions apply.

(1) Start of transmission

Update TDR by the CPU, DMAC, or DTC and wait at least the following time until the start of the external clock input: (See Figure 26.120)

Time taking into account the output AC spec of the MISO terminal of this product and the input AC spec of the master reception + 1 PCLK cycle + synchronization delay.

(2) Continuous transmission

Write the next transmit data to TDR before the falling edge*1 of the transmit clock for bit 7. Please write the transmit data to TDR in consideration of synchronization delay. If the transmit data cannot be written in time, the previous frame data is resent. (See Figure 26.120)

Note 1. When CCR3.CPOL = 1 and CCR3.CPHA = 0, or CCR3.CPOL = 0 and CCR3.CPHA = 1. In the case of CCR3.CPOL = 0 and CCR3.CPHA = 0, or CCR3.CPOL = 1 and CCR3.CPHA = 1, it's the rising edge.

26.20.4 标记状态和产生的中断

当CCR0.TE位为0时，禁用串行传输，TXDn引脚的状态可以使用CCR1.SPB2IO和CCR1.SPB2DT位。使用这种方法，可以将TXDn引脚置于标记状态以发送中断。

在设置CCR0.TE位为1，使能串行传输之前，设置SPB2IO和SPB2DT位使通信线处于标记状态（状态为1），并使用IO端口功能改变TXDn引脚。要输出数据传输中断，通过设置SPB2IO和SPB2DT位将TXDn引脚设置为输出0后，使用IO端口功能更改TXDn引脚并将CCR0.TE位设置为0。当CCR0.TE位为设置为0，无论当前的传输状态如何，都会初始化发送器。

26.20.5 接收错误标志和发送操作（时钟同步模式和简单SPI模式）

即使CSR.ORER为1，也可以通过将发送数据写入TDR来开始发送。但是，无法开始接收。
另请注意，即使CCR0.RE设置为0（禁用串行接收），也不能将接收错误标志设置为0。

26.20.6 将数据写入TDR

(1) Non-FIFO selected

当CCR0.TE为1时，可以随时将数据写入TDR。但是，如果在TDR中剩余发送数据时将新数据写入TDR，则TDR中的先前数据将丢失，因为它尚未传输到TSR。如果您使用DTC或DMAC，请务必在SCIn_TXI中断请求处理程序中将发送数据写入TDR。

(2) FIFO selected

当CCR0.TE为1时，可以将数据写入发送FIFO(TDR)。使用FTSR.T[5:0]位检查可写入数据的数量。

26.20.7 时钟同步传输的限制（时钟同步模式和简单SPI模式）

当外部时钟源用作同步时钟时，有以下限制。

(1) 传输开始

通过CPU、DMAC或DTC更新TDR，并至少等待以下时间，直到外部时钟输入开始：（参见图26.120）

时间考虑了本产品MISO端子的输出AC规格和主机接收的输入AC规格+1PCLK周期+同步延迟。

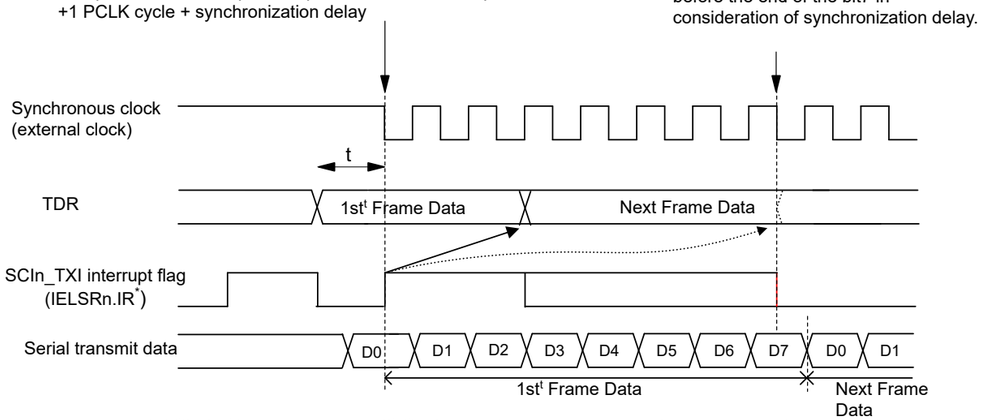
(2) 连续传输

在位7的发送时钟的下降沿*1之前将下一个发送数据写入TDR。请将发送数据写入考虑到同步延迟的TDR。如果发送数据不能及时写入，则重新发送前一帧数据。（见图26.120）

注1.当CCR3.CPOL=1且CCR3.CPHA=0，或CCR3.CPOL=0且CCR3.CPHA=1时。在CCR3.CPOL=0且CCR3.CPHA=0的情况下，或CCR3.CPOL=1且CCR3.CPHA=1，为上升沿。

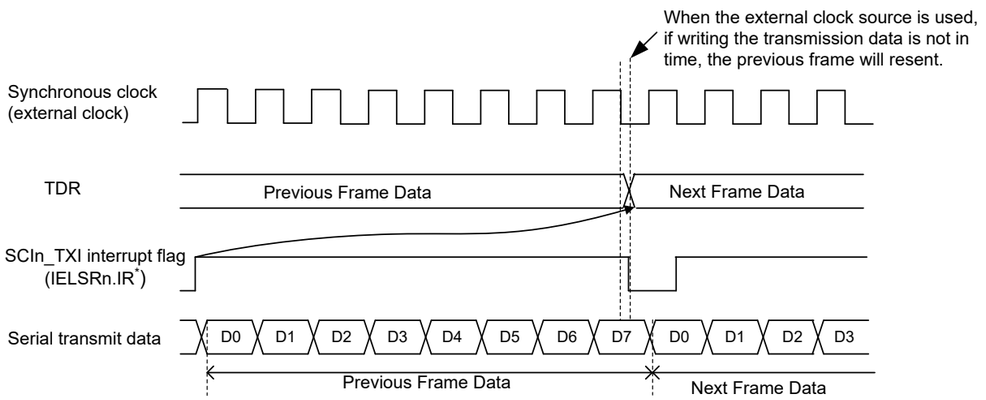
When the external clock source is used, make t more than the following time.
t ≥ Time taking into account the output AC spec of the MISO terminal of this product and the input AC spec of the master reception +1 PCLK cycle + synchronization delay

Write the next transmit data to TDR before the end of the bit7 in consideration of synchronization delay.



(1) Start of transmission and (2) Continuous transmission (When transmission data is in time)

When the external clock source is used, if writing the transmission data is not in time, the previous frame will resent.



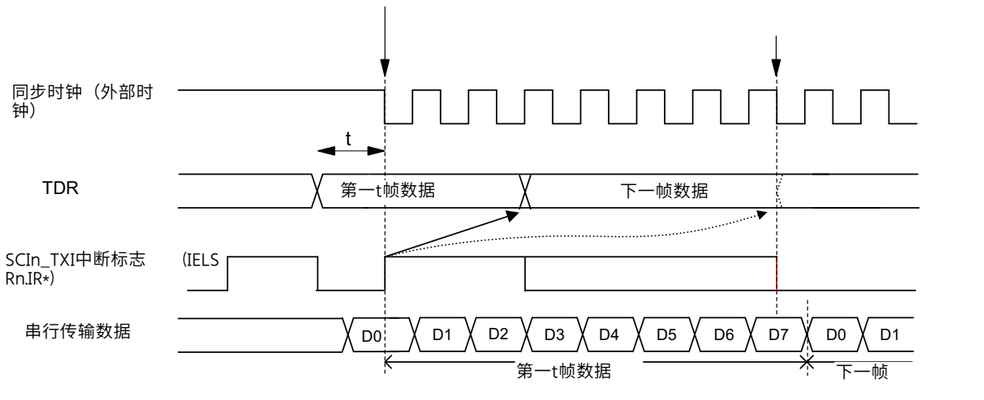
(2) Continuous transmission (When transmission data is not in time)

Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 26.120 Restrictions on Use of External Clock in Clock Synchronous Transmission

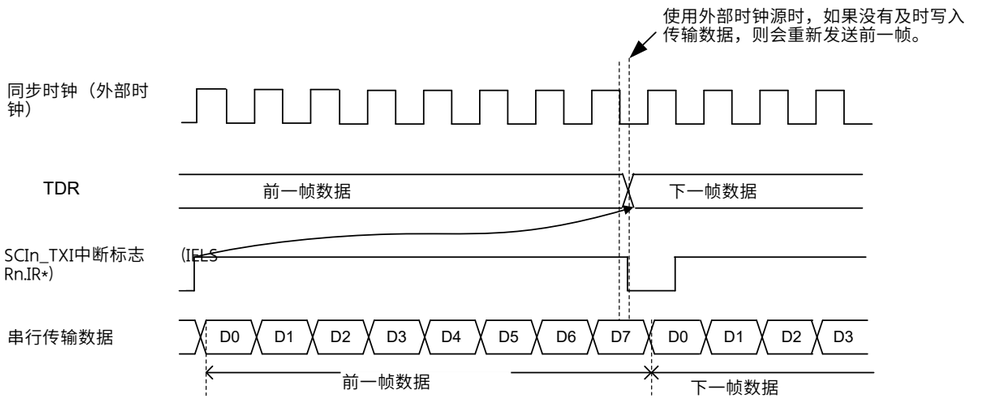
使用外部时钟源时，使t大于以下时间。t≥考虑本产品MISO端子的输出AC规格和主机接收的输入AC规格的时间+1PCLK周期+同步延迟

考虑到同步延迟，在bit7结束之前将下一个发送数据写入TDR。



(1)传输开始和(2)连续传输（传输数据及时）

使用外部时钟源时，如果没有及时写入传输数据，则会重新发送前一帧。



(2)连续传输（传输数据不及时）

注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

图26.120时钟同步传输中使用外部时钟的限制

26.20.8 Restrictions on Using DMAC or DTC

When using the DMAC or DTC to read RDR, be sure to set the receive data full interrupt (SCIn_RXI) as the activation source of the relevant SCI.

During the operation in transmission / reception using the DMAC or DTC, it should not set transfer information of DMAC/DTC.

26.20.8 使用DMAC或DTC的限制

使用DMAC或DTC读取RDR时，务必将接收数据满中断（SCIn_RXI）设置为相关SCI的激活源。

在使用DMAC或DTC进行发送接收操作期间，不应设置DMAC的传输信息
DTC.

26.20.9 Notes on Starting Transfer

At the point where transfer starts when the interrupt status flag (IELSRn.IR flag) in the ICU is 1, follow the procedure in this section to clear interrupt requests before permitting operations (by setting the CCR0.TE or CCR0.RE bit to 1). For details on the interrupt status flag, see section 12, Interrupt Controller Unit (ICU).

1. Confirm that transfer has stopped (the CCR0.TE or CCR0.RE bit is 0)

26.20.9 开始转移注意事项

在ICU中的中断状态标志（IELSRn.IR标志）为1时开始传输的点，按照本节中的步骤在允许操作之前清除中断请求（通过将CCR0.TE或CCR0.RE位设置为1）。有关中断状态标志的详细信息，请参见第12节，中断控制器单元(ICU)。

1.确认传输已停止（CCR0.TE或CCR0.RE位为0）

2. Set the associated interrupt enable bit (CCR0.TIE or CCR0.RIE bit) to 0
3. Read the associated interrupt enable bit (CCR0.TIE or CCR0.RIE bit) to check that it actually becomes 0
4. Set the interrupt status flag, IELSRn.IR, in the ICU to 0

26.20.10 Limitations on Simple SPI Mode

(1) Master mode

- Use a resistor to pull up or pull down the clock line matching the initial settings for the transfer clock set in the CCR3.CPHA and CPOL bits when the CCR0.SSE bit is 1.

  This prevents the clock line from being placed in the high-impedance state when the CCR0.TE bit is set to 0 or unexpected edges from being generated on the clock line when the CCR0.TE bit changes from 0 to 1. When the CCR0.SSE bit is 0 in single master mode, pulling up or pulling down the clock line is not required because the clock line is not placed in the high-impedance state even when the SCR.TE bit is set to 0.
- For the clock delay setting (CCR3.CPHA bit is 1), the receive data full interrupt (SCIn_RXI) is generated before the final clock edge on the SCKn pin as indicated in Figure 26.121. If the TE and RE bits in the CCR0 register become 0 before the final edge of the clock signal on the SCKn pin, the SCKn pin is placed in the high-impedance state, so the width of the last clock pulse of the transfer clock is shortened. Additionally, an SCIn_RXI interrupt might lead to the input signal on the SSn pin of a connected slave going to the high level before the final edge of the clock signal on the SCKn pin, leading to incorrect operation of the slave.
- In a multi-master configuration, the SCKn pin output goes to high-impedance while the input on the SSn pin is at the low level if a mode fault error occurs while a character is being transferred, stopping supply of the clock signal to the connected slave. Reset the connected slave to avoid misaligned bits when transfer is restarted.

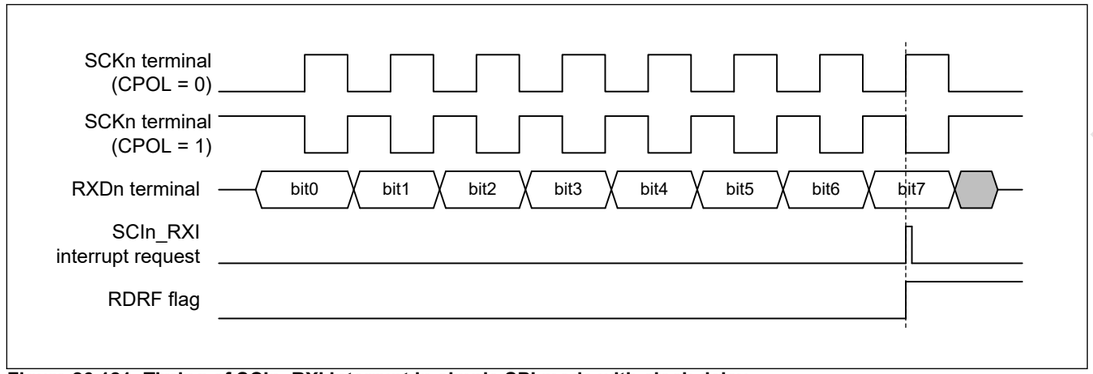


Figure 26.121 Timing of SCIn_RXI interrupt in simple SPI mode with clock delay

(2) Slave mode

- It takes 1PCLK + synchronization delay time + data output delay time (AC spec) from writing the transmit data to the TDR register until the data is output to the RXDn pin. Take these into account when starting external clock input.
- Provide an external clock signal to the master the same as the data length for transfer
- Secure the SSn input setup time (AC spec) from the SSn low-level input to the start of external clock input.
- Control the input on the SSn pin before the start and after the end of data transfer
- When the input level on the SSn pin is to be changed from low to high while a character is being transferred, set the TE and RE bits in the CCR0 register to 0 and, after restoring the settings, restart transfer of the first byte

26.20.11 Notes on Transmit Enable bit (SCR.TE)

In initial register value, when CCR0.TE bit is “0”, the terminal as “TXDn” outputs high impedance.

So please make sure that the TXDn line won’t be high impedance by the following one of ways.

1. The pull-up resistance is connected to the TXDn line.

2.将相关的中断使能位（CCR0.TIE或CCR0.RIE位）设置为0

3.读取相关的中断使能位（CCR0.TIE或CCR0.RIE位），检查它是否真的变为0

4.将ICU中的中断状态标志IELSRn.IR设置为0

26.20.10 简单SPI模式的限制

(1) 主模式

●当CCR0.SSE位为1时，使用电阻上拉或下拉与CCR3.CPHA和CPOL位中设置的传输时钟的初始设置相匹配的时钟线。

这可以防止在CCR0.TE位设置为0时将时钟线置于高阻抗状态或在CCR0.TE位从0变为1时在时钟线上产生意外边沿。SSE位在单主机模式下为0，不需要上拉或下拉时钟线，因为即使SCR.TE位设置为0，时钟线也不会处于高阻状态。

●对于时钟延迟设置（CCR3.CPHA位为1），接收数据满中断（SCIn_RXI）在SCKn引脚的最后一个时钟沿之前产生，如图26.121所示。如果CCR0寄存器中的TE和RE位在SCKn引脚上的时钟信号的最后一个边沿之前变为0，则SCKn引脚处于高阻状态，因此传输时钟的最后一个时钟脉冲的宽度为缩短。此外，SCIn_RXI中断可能会导致所连接从机的SSn引脚上的输入信号在SCKn引脚上的时钟信号的最后一个边沿之前变为高电平，从而导致从机的错误操作。

●在多主机配置中，如果在传输字符时发生模式故障错误，则SCKn引脚输出变为高阻态，而SSn引脚上的输入处于低电平，从而停止向主机提供时钟信号。连接的奴隶。重新启动传输时，重置连接的从机以避免未对齐的位。

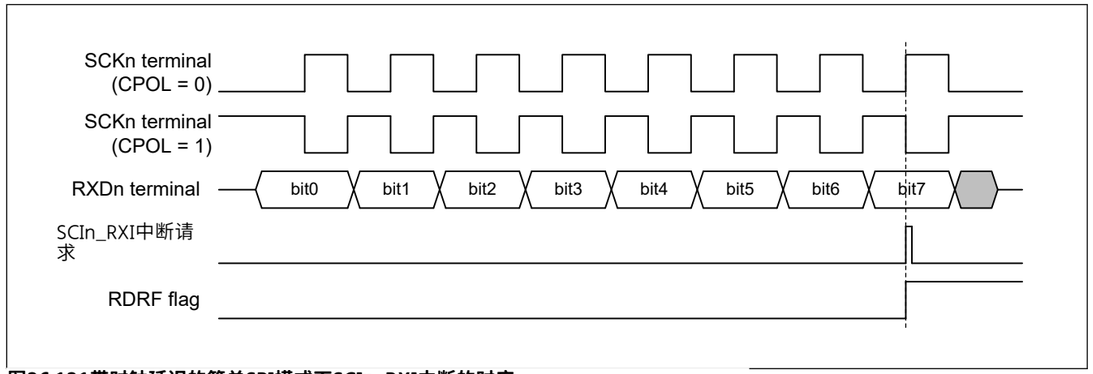


图26.121带时钟延迟的简单SPI模式下SCIn_RXI中断的时序

(2) 从机模式

●从将发送数据写入TDR寄存器到数据输出到RXDn引脚需要1PCLK+同步延迟时间+数据输出延迟时间（AC规格）。在启动外部时钟输入时考虑这些。

●向主机提供与传输数据长度相同的外部时钟信号

●确保从SSn低电平输入到外部时钟输入开始的SSn输入建立时间（AC规格）。

●在数据传输开始前和结束后控制SSn引脚上的输入

●在字符传输过程中，若要将SSn引脚的输入电平从低电平变为高电平，则将CCR0寄存器中的TE和RE位设置为0，并在恢复设置后重新开始传输第一个字节

26.20.11 发送使能位(SCR.TE)的注意事项

在初始寄存器值中，当CCR0.TE位为“0”时，“TXDn”端输出高阻抗。

所以请通过以下方式之一确保TXDn线不会高阻。

1.上拉电阻连接到TXDn线。

2. Before CCR0.TE bit is “0”, the function of the terminal is changed to general-purpose input port or output port. And after CCR0.TE bit is “1”, thr function of the terminal is changed to “TXDn”.
3. In asynchronous mode and Manchester mode, you can set CCR1 and decided level of TXDn terminal during CCR0.TE is “0”.

In the Simple SPI mode slave operation, the RXDn terminal operates in the same way as the above TXDn terminal, so please deal with 1 or 2 in the same way. (3 can not be used.)

26.20.12 Notes on Simple LIN mode

In Simple LIN mode (CCR3.MOD[2:0] = 110), the following functions cannot be used.

- Multi-processor communication function
- Bit Rate Modulation function
- Loopback function
- FIFO buffer

26.20.13 Notes on RS-485 Driver Control function

RS-485 Driver control function is valid only in Asynchronous mode.

When RS-485 Driver control function is active (CCR3.DEN = 1), the CSR.TEND set timing / SCIn_TEI output timing changes as follows. Wait for the SCIn_TEI interrupt and set the CCR0.TE bit in SCI to 0.

When RS-485 Driver control function is inactive: When STOP bit output is completed.

When RS-485 Driver control function is active: At the end of DEn negation time.

26.20.14 Notes on Loopback function

The Loopback function is valid in Asynchronous mode with internal clock, in Manchester mode with internal clock and Clock synchronous mode with internal clock.

26.20.15 Notes regarding register access when operation clock (TCLK) is slower than bus clock (PCLK)

If the operating clock (TCLK) is slower than the bus clock (PCLK), the time until this information is transmitted internally after writing to the CCR0.TE and CCR0.RE registers is slower than the bus access time. In particular, when trying to change the setting register after writing 0 and interrupting communication, do not change the setting register before the signal inside the IP is in the communication stopped state. To prevent this, after setting CCR0.TE and CCR0.RE to 0, check the CESR.TIST and CESR.RIST bits until they are 0 before setting the next register.

26.20.16 Notes on interrupting operation

If 0 is written to CCR0.RE during data reception and the reception operation is interrupted, there is a possibility of an invalid state, so please do not use the received data (RDR register stored value) and the flag value of each status register. To interrupt the reception operation, stop the interrupt or event link reception side and then write 0 to the CCR0.RE bit.

26.20.17 Notes on CCR3.BPEN bit setting

Set the BPEN bit only once when setting the CCR3 register in the SCI initialization flow.

This bit cannot be changed after the initialization.

If you want to change this bit setting, please start from the SCI initialization flow again.

2、在CCR0.TE位为“0”之前，端子功能变为通用输入口或输出口。CCR0.TE位为“1”后，终端的thr功能变为“TXDn”。

3.在异步模式和曼彻斯特模式下，可以设置CCR1和决定CCR0.TE期间TXDn端的电平为“0”。

在SimpleSPI模式从机操作中，RXDn端子与上述TXDn端子的操作方式相同，因此请按相同方式处理1或2。（3个不能用。）

26.20.12 简单LIN模式的注意事项

在简单LIN模式(CCR3.MOD[2:0]=110)下，无法使用以下功能。

●多处理器通讯功能

●比特率调制功能

- Loopback function
- FIFO buffer

26.20.13 RS-485驱动器控制功能注意事项

RS-485驱动器控制功能仅在异步模式下有效。

当RS-485驱动器控制功能激活(CCR3.DEN=1)时，CSR.TEND设置时序SCIn_TEI输出时序变化如下。等待SCIn_TEI中断并将SCI中的CCR0.TE位设置为0。

RS-485驱动器控制功能无效时：STOP位输出完成时。

当RS-485驱动器控制功能激活时：在DEn否定时间结束时。

26.20.14 Loopback功能注意事项

Loopback功能在带内部时钟的异步模式、带内部时钟的曼彻斯特模式和
具有内部时钟的时钟同步模式。

26.20.15 当操作时钟(TCLK)比总线时钟(PCLK)慢时有关寄存器访问的注意事项

如果操作时钟(TCLK)比总线时钟(PCLK)慢，则在写入CCR0.TE和CCR0.RE寄存器之后，直到该信息在内部传输的时间比总线访问时间慢。特别是在写入0并中断通信后尝试更改设置寄存器时，请不要在IP内部的信号处于通信停止状态之前更改设置寄存器。为了防止这种情况发生，在将CCR0.TE和CCR0.RE设置为0后，在设置下一个寄存器之前检查CESR.TIST和CESR.RIST位，直到它们为0。

26.20.16 中断操作注意事项

如果在数据接收过程中向CCR0.RE写入0并中断接收操作，则有可能出现无效状态，因此请不要使用接收到的数据（RDR寄存器存储值）和各状态寄存器的标志值。要中断接收操作，请停止中断或事件链接接收侧，然后将0写入CCR0.RE位。

26.20.17 CCR3.BPEN位设置注意事项

在SCI初始化流程中设置CCR3寄存器时，只需设置一次BPEN位。

该位在初始化后不能更改。

如果要更改此位设置，请重新从SCI初始化流程开始。

27. I²C Bus Interface (IIC)

This is the IIC_B version of the IIC peripheral module.

IIC_B is referred to as IIC in this chapter.

27.1 Overview

27.1.1 Functional Overview

The I²C bus interface (IIC) has 2 channels. The IIC module conform with and provide a subset of the NXP I²C (Inter-Integrated Circuit) bus interface functions.

Table 27.1 lists the I²C specifications.

Table 27.1 I²C specifications

Item	Description
Operation mode	Master mode and slave mode selectable
Data handler	Single buffer transfer
Communication protocol	• I²C bus format – Standard-mode (Sm) : 0 to 100 kbps – Fast-mode (Fm) : 0 to 400 kbps – Fast-mode Plus (Fm+) : 0 to 1 Mbps*1 – High-speed mode (Hs-mode) : 0 to 3.2 Mbps*1 • SMBus format : 10 to 100 kbps
Address format	• 7-bit address • 10-bit address
Address detection	• Slave address (static address) (max 1 address) • General call address • Hs-mode master code*1 • Device ID • Host address • 10-bit slave addressing
Clock stretching	Clock stretching capability
Noise-filter	• Analog noise-filter*2 • Digital noise-filter
Interrupt source	• Rx data buffer full • Tx data buffer empty • START condition detection • STOP condition detection • Transmit end • NACK detection • Arbitration lost • Timeout detection • Wake-up condition detection*2
Error detection	• NACK received • Arbitration lost error • Timeout error
Event link output	• Communication event • Rx data buffer full event • Tx data buffer empty event • Transmit end event
Wake-up source*2	Address detection of slave address

Note 1. Fast-mode Plus and High-speed mode are supported by IIC0 (SCL0_A, SDA0_A)
Note 2. Wake-up function and analog noise filter are available only IIC0.

27. I2C总线接口(IIC)

这是IIC外围模块的IIC_B版本。

IIC_B在本章中称为IIC。

27.1 Overview

27.1.1 功能概述

I2C总线接口(IIC)有2个通道。IIC模块符合并提供NXPI2C(Inter
集成电路）总线接口功能。

表27.1列出了I2C规范。

Table 27.1 I²C specifications

Item	Description
操作模式	主模式和从模式可选
数据处理程序	单缓冲区传输
通讯协议	• I2C总线格式 – Standard-mode (Sm) : 0 to 100 kbps – Fast-mode (Fm) : 0 to 400 kbps – 快速模式Plus(Fm+)：0至1Mbps*1 – 高速模式（Hs-mode）：0至3.2Mbps*1 • SMBus格式：10到100kbps
地址格式	• 7-bit address • 10-bit address
地址检测	• 从站地址（静态地址）（最多1个地址） • 通用呼叫地址 • Hs-mode主码*1 • 设备ID • 主机地址 • 10位从机寻址
时钟拉伸	时钟延长能力
Noise-filter	• Analog noise-filter*2 • Digital noise-filter
中断源	• Rx数据缓冲区已满 • Tx数据缓冲区为空 • START条件检测 • 停止条件检测 • 发射端 • NACK检测 • 仲裁失败 • 超时检测 • 唤醒状态检测*2
错误检测	• 收到NACK • 仲裁失败错误 • 超时错误
事件链接输出	• 交流活动 • Rx数据缓冲区已满事件 • Tx数据缓冲区空事件 • 传输结束事件
Wake-up source*2	从机地址的地址检测

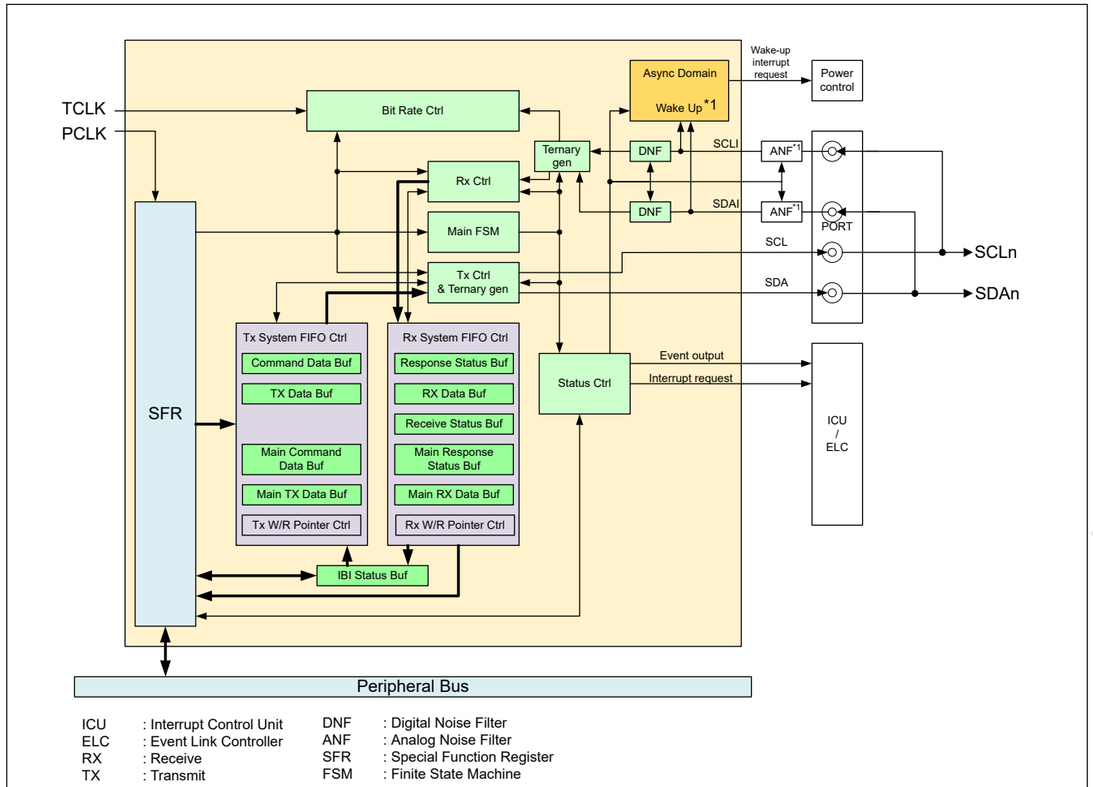
注1.IIC0(SCL0_A SDA0_A)支持Fast-modePlus和High-speed模式
注2.唤醒功能和模拟噪声滤波器仅适用于IIC0。

Table 27.2 IIC I/O pins (n = 0, 1)

Function	Pin name	I/O	Description
IICn	SCLn	I/O	Input/output pins for clock
	SDAn	I/O	Input/output pins for data

27.1.2 Block Diagram

Figure 27.1 shows the main components of this IIC.



Note: TCLK = IICCLK
PCLK = PCLKA
Note 1. Wake up function and analog noise filter are available only IIC0.

Figure 27.1 IIC block diagram

27.2 Registers

27.2.1 List of Registers

IIC registers are listed in the following table.

Table 27.3 List of IIC registers (1 of 2)

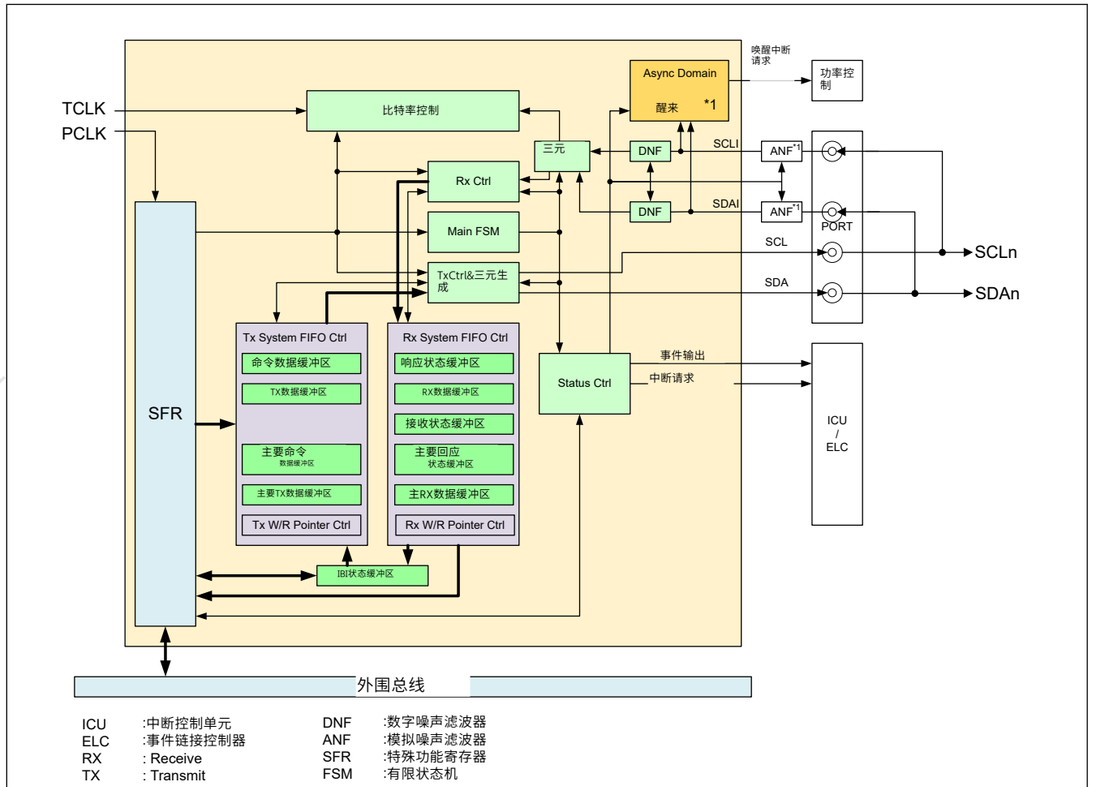
Register	Symbol	Offset address
Bus Control Register	BCTL	0x014
Reset Control Register	RSTCTL	0x020

Table 27.2 IIC I/O pins (n = 0, 1)

Function	引脚名称	I/O	Description
IICn	SCLn	I/O	时钟输入输出引脚
	SDAn	I/O	数据输入输出引脚

27.1.2 框图

图27.1显示了该IIC的主要组件。



Note: TCLK = IICCLK
PCLK = PCLKA
注1.唤醒功能和模拟噪声滤波器仅IIC0可用。

Figure 27.1 IIC框图

27.2 Registers

27.2.1 寄存器列表

IIC寄存器如下表所示。

Table 27.3 IIC寄存器列表(1of2)

Register	Symbol	偏移地址
总线控制寄存器	BCTL	0x014
复位控制寄存器	RSTCTL	0x020

Table 27.3 List of IIC registers (2 of 2)

Register	Symbol	Offset address
Present State Register	PRSST	0x024
Bus Function Control Register	BFCTL	0x060
Slave Control Register	SVCTL	0x064
Reference Clock Control Register	REFCKCTL	0x070
Standard Bit Rate Register	STDBR	0x074
Extended Bit Rate Register	EXTBR	0x078
Bus Free Condition Detection Time Register	BFRECDT	0x07C
Output Control Register	OUTCTL	0x088
Input Control Register	INCTL	0x08C
Timeout Control Register	TMOCTL	0x090
Wake Up Unit Control Register*1	WUCTL	0x098
Acknowledge Control Register	ACKCTL	0x0A0
SCL Stretch Control Register	SCSTRCTL	0x0A4
Condition Control Register	CNDCTL	0x140
Normal Transfer Data Buffer Port Register 0	NTDTBP0/ NTDTBP0_BY	0x158
Bus Status Register	BST	0x1D0
Bus Status Enable Register	BSTE	0x1D4
Bus Interrupt Enable Register	BIE	0x1D8
Bus Status Force Register	BSTFC	0x1DC
Normal Transfer Status Register	NTST	0x1E0
Normal Transfer Status Enable Register	NTSTE	0x1E4
Normal Transfer Interrupt Enable Register	NTIE	0x1E8
Normal Transfer Status Force Register	NTSTFC	0x1EC
Bus Condition Status Register	BCST	0x210
Slave Status Register	SVST	0x214
Wake Up Unit Operating Status Register*1	WUST	0x218
Slave Device Address Table Basic Register 0	SDATBAS0	0x2B0
Slave Device Address Table Basic Register 1	SDATBAS1	0x2B4
Slave Device Address Table Basic Register 2	SDATBAS2	0x2B8
Slave Device Address Register 0	SVDVAD0	0x330
Slave Device Address Register 1	SVDVAD1	0x334
Slave Device Address Register 2	SVDVAD2	0x338
Bit Count Register	BITCNT	0x380
Present State Debug Register	PRSTDBG	0x3CC

Note 1. Reserved register in IIC1

Table 27.3 IIC寄存器列表（2个中的2个）

Register	Symbol	偏移地址
现状登记册	PRSST	0x024
总线功能控制寄存器	BFCTL	0x060
从控制寄存器	SVCTL	0x064
参考时钟控制寄存器	REFCKCTL	0x070
标准比特率寄存器	STDBR	0x074
扩展比特率寄存器	EXTBR	0x078
总线空闲状态检测时间寄存器	BFRECDT	0x07C
输出控制寄存器	OUTCTL	0x088
输入控制寄存器	INCTL	0x08C
超时控制寄存器	TMOCTL	0x090
唤醒单元控制寄存器*1	WUCTL	0x098
确认控制寄存器	ACKCTL	0x0A0
SCL伸展控制寄存器	SCSTRCTL	0x0A4
条件控制寄存器	CNDCTL	0x140
正常传输数据缓冲区端口寄存器0	NTDTBP0/ NTDTBP0_BY	0x158
总线状态寄存器	BST	0x1D0
总线状态使能寄存器	BSTE	0x1D4
总线中断使能寄存器	BIE	0x1D8
总线状态强制寄存器	BSTFC	0x1DC
正常传输状态寄存器	NTST	0x1E0
正常传输状态使能寄存器	NTSTE	0x1E4
正常传输中断使能寄存器	NTIE	0x1E8
正常传输状态强制寄存器	NTSTFC	0x1EC
总线条件状态寄存器	BCST	0x210
从机状态寄存器	SVST	0x214
唤醒单元操作状态寄存器*1	WUST	0x218
从设备地址表基本寄存器0	SDATBAS0	0x2B0
从设备地址表基本寄存器1	SDATBAS1	0x2B4
从设备地址表基本寄存器2	SDATBAS2	0x2B8
从设备地址寄存器0	SVDVAD0	0x330
从设备地址寄存器1	SVDVAD1	0x334
从设备地址寄存器2	SVDVAD2	0x338
位计数寄存器	BITCNT	0x380
当前状态调试寄存器	PRSTDBG	0x3CC

注1.IIC1中的保留寄存器

27.2.2 BCTL : Bus Control Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x014

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BUSE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
30:0	—	These bits are read as 0. The write value should be 0.	R/W
31	BUSE	Bus Enable 0: IIC bus operation is disabled. 1: IIC bus operation is enabled.	R/W

BUSE bit (Bus Enable)

Enables or disables the operation on the I^2C Bus by IIC.

Set the BUSE bit to 1 when using IIC. The SCL and SDA pins are placed in the active state when the BUSE bit is set to 1. Set the BUSE bit to 0 when IIC is not to be used. The SCL and SDA pins are placed in the inactive state when the BUSE bit is set to 0.

If the software sets this bit, then it also confirms that initialization is done, and that IIC can use the programmed register values.

Software may disable IIC bus operation while it is active, However:

- When the software reads the value 0 from this field, this indicates that IIC bus operation disable operation has completed.

27.2.3 RSTCTL : Reset Control Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INTLRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RI2CRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RI2CRST	IIC Software Reset 0: Reset of all registers and internal state. 1: Releases of all registers and internal state.	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

27.2.2 BCTL:总线控制寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x014

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BUSE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
30:0	—	这些位被读取为0。写入值应为0。	R/W
31	BUSE	总线启用 0：IIC总线操作禁用。1：IIC总线操作使能。	R/W

BUSE bit (Bus Enable)

通过IIC启用或禁用I2C总线上的操作。

使用IIC时将BUSE位设置为1。当BUSE位设置为1时，SCL和SDA引脚处于活动状态。
不使用IIC时将BUSE位设置为0。当BUSE位设置为0时，SCL和SDA引脚处于无效状态。

如果软件设置了这个位，那么它也确认初始化已经完成，并且IIC可以使用编程的寄存器值。

软件可能会在IIC总线处于活动状态时禁用它，但是：

●当软件从该字段读取值0时，表示IIC总线操作禁用操作已完成。

27.2.3 RSTCTL:复位控制寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INTLRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RI2CRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RI2CRST	IIC软件复位 0：复位所有寄存器和内部状态。1：释放所有寄存器和内部状态。	R/W
15:1	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
16	INTLRST	Internal Software Reset 0: Releases of some registers and internal state. 1: Resets of some registers and internal state.	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R/W

For details on reset for each register, see section 27.6. Reset Descriptions.

RI2CRST bit (IIC Software Reset)

On Driver setting this bit to 1, IIC shall be reset and disabled.

All registers shall return to their reset values, and the software shall re-initialize IIC.

This field is cleared automatically upon IIC reset completion. This field also resets all Queues in IIC.

Note: Programming this field while it contains a value of 1 may result in undefined behavior.

INTLRST bit (Internal Software Reset)

When set to 1, some of registers is reset, and internal state is reset. For details on the registers to be reset, see section 27.6. Reset Descriptions.

27.2.4 PRSST : Present State Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x024

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	PRSSTWP	—	—	TRMD	—	CRMS	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 0. The write value should be 0.	R/W
2	CRMS	Current Master 0: The Master is not the Current Master, and must request and acquire bus ownership before initiating any transfer. 1: The Master is the Current Master, and as a result can initiate transfers.	R/W*1
3	—	This bit is read as 0. The write value should be 0.	R/W
4	TRMD	Transmit/Receive Mode 0: Receive mode 1: Transmit mode	R
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	PRSSTWP	Present State Write Protect 0: CRMS bit is protected. 1: CRMS bit can be written when writing simultaneously with the value of the target bit.	W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the PRSSTWP bit is set to 1, the CRMS bit can be written to.

CRMS bit (Current Master)

Indicates the set condition and reset condition of each operation mode.

[Clearing conditions]

Bit	Symbol	Function	R/W
16	INTLRST	内部软件复位 0：释放一些寄存器和内部状态。1：一些寄存器和内部状态的复位。	R/W
31:17	—	这些位被读取为0。写入值应为0。	R/W

关于各寄存器的复位详情，请参阅第27.6节。重置说明。

RI2CRST位（IIC软件复位）

在Driver将此位设置为1时，IIC应复位并禁用。

所有寄存器应返回其复位值，软件应重新初始化IIC。

该字段在IIC复位完成后自动清除。此字段还重置IIC中的所有队列。

Note: 在此字段包含值1时对其进行编程可能会导致未定义的行为。

INTLRST位（内部软件复位）

当设置为1时，一些寄存器被复位，并且内部状态被复位。关于要复位的寄存器的详细信息，请参阅第27.6节。重置说明。

27.2.4 PRSST:当前状态寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x024

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	PRSSTWP	—	—	TRMD	—	CRMS	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	这些位被读取为0。写入值应为0。	R/W
2	CRMS	现任大师 0：Master不是当前Master，并且必须在发起任何传输之前请求并获得总线所有权。 1：Master是CurrentMaster，因此可以发起传输。	R/W*1
3	—	该位读取为0。写入值应为0。	R/W
4	TRMD	Transmit/Receive Mode 0：接收模式1：发送模式	R
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	PRSSTWP	当前状态写保护 0：CRMS位被保护。1：与目标位的值同时写入时可以写入CRMS位。	W
31:8	—	这些位被读取为0。写入值应为0。	R/W

注1.当PRSSSTWP位设置为1时，可以写入CRMS位。

CRMS bit (Current Master)

表示各操作模式的设置条件和复位条件。

[Clearing conditions]

- When 0 written to the PRSST.CRMS by the software.
- When STOP is issued.
- When Master Arbitration-Lost.

[Setting conditions]

- When 1 written to the PRSST.CRMS by the software.
- When START is issued.

The PRSST register returns IIC current state.

State has two parts: this register which is mandatory, and an additional optional PRSST_DEBUG register intended for debug purposes (see the Debug Capability registers in the Extended Capabilities list).

TRMD bit (Transmit/Receive Mode)

This bit indicates transmit or receive mode.

IIC is in receive mode when the TRMD bit is set to 0 and is in transmit mode when the bit is set to 1. Combination of this bit and the CRMS bit indicates the operating mode of IIC.

The value of TRMD bit is automatically changed to 1 for transmit mode or 0 for receive mode by issuing or detection of a START condition and setting of the R/W# bit.

[Setting conditions]

- When a START condition is issued normally according to the START condition issuance request (when a START condition is detected with the CNDCTL.STCND bit set to 1).
- When a Repeated START condition is issued normally according to the Repeated START condition issuance request (when a Repeated START condition is detected with the CNDCTL.SRCND bit set to 1).
- When the R/W# bit added to the slave address is set to 0 in master mode.
- When the address received in slave mode matches the address enabled in SVCTL, with the R/W# bit set to 1.

[Clearing conditions]

- When a STOP condition is detected.
- The ALF (arbitration-lost) flag in BST being set to 1.
- In master mode, reception of a slave address to which an R/W# bit with the value 1 is appended.
- In slave mode, a match between the received address and the address enabled in SVCTL when the value of the received R/W# bit is 0 (including cases where the received address is the general call address).
- In slave mode, a Repeated START condition is detected (a Repeated START condition is detected with BCST.BFREF = 0 and CRMS = 0).

PRSSTWP bit (Present State Write Protect)

PRSSTWP is always 0 when reading.

When writing to PRSST, writing 1 to this bit at the same time enables writing to CRMS bit.

●当软件向PRSST.CRMS写入0时。

●发出STOP时。

●当主仲裁失败时。

[Setting conditions]

●当1被软件写入PRSST.CRMS时。

●发出START时。

PRSST寄存器返回IIC当前状态。

状态有两个部分：该寄存器是强制性的，以及一个额外的可选PRSST_DEBUG寄存器，用于调试目的（请参阅扩展功能列表中的调试功能寄存器）。

TRMD bit (Transmit/Receive Mode)

该位指示发送或接收模式。

当TRMD位设置为0时，IIC处于接收模式，而当该位设置为1时，IIC处于发送模式。该位和CRMS位的组合表示IIC的工作模式。

TRMD位的值自动更改为1（发送模式）或0（接收模式）通过发出或检测到START条件和RW#位的设置。

[Setting conditions]

●根据START条件发出请求正常发出START条件时（当CNDCTL.STCND位设置为1时检测到START条件时）。

●当根据重复启动条件发出请求正常发出重复启动条件时（当CNDCTL.SRCND位设置为1时检测到重复启动条件）。

●在主机模式下，添加到从机地址的RW#位设置为0时。

●从机模式接收到的地址与SVCTL中使能的地址匹配时，RW#位设置为1。

[Clearing conditions]

●检测到停止条件时。

●BST中的ALF（仲裁失败）标志设置为1。

●在主机模式下，接收附加了值为1的RW#位的从机地址。

●从机模式下，当接收到的RW#位的值为0时，接收到的地址与SVCTL中使能的地址匹配（包括接收到的地址是广播地址的情况）。

●在从模式下，检测到重复启动条件（在BCST.BFREF=0和CRMS=0时检测到重复启动条件）。

PRSSTWP位（当前状态写保护）

读取时PRSSTWP始终为0。

写入PRSST时，同时向该位写入1可以写入CRMS位。

27.2.5 BFCTL : Bus Function Control Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x060

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	HSME	FMPE	—	SMBS	—	—	—	SCSYNE	—	—	—	—	—	SALE	NALE	MALE
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	MALE	Master Arbitration-Lost Detection Enable 0: Master arbitration-lost detection disables. Disables the arbitration-lost detection function and does not clear the CRMS and TRMD bits in PRSST automatically when arbitration is lost. 1: Master arbitration-lost detection enables. Enables the arbitration-lost detection function and clears the CRMS and TRMD bits in PRSST automatically when arbitration is lost.	R/W
1	NALE	NACK Transmission Arbitration-Lost Detection Enable 0: NACK transmission arbitration-lost detection disables. 1: NACK transmission arbitration-lost detection enables.	R/W
2	SALE	Slave Arbitration-Lost Detection Enable 0: Slave arbitration-lost detection disables. 1: Slave arbitration-lost detection enables.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
8	SCSYNE	SCL Synchronous Circuit Enable 0: No SCL synchronous circuit uses. 1: An SCL synchronous circuit uses.	R/W
11:9	—	These bits are read as 0. The write value should be 0.	R/W
12	SMBS	SMBus/I2C Bus Selection 0: The I2C bus select. 1: The SMBus select.	R/W
13	—	This bit is read as 0. The write value should be 0.	R/W
14	FMPE*1	Fast-mode Plus Enable 0: No Fm+ slope control circuit uses for the SCLn pin and SDAn pin. (n = 0, 1) 1: An Fm+ slope control circuit uses for the SCLn pin and SDAn pin. (n = 0, 1)	R/W
15	HSME*2	High Speed Mode Enable 0: Disable High Speed Mode. 1: Enable High Speed Mode.	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The Fast-mode Plus Enable bit (FMPE) is supported by IIC0 (SCL0_A, SDA0_A). Bit[14] is the reserved bit in the not supported channel.

Note 2. The High Speed Mode Enable bit (HSME) is supported by IIC0 (SCL0_A, SDA0_A). Bit[15] is the reserved bit in the not supported channel.

MALE bit (Master Arbitration-Lost Detection Enable)

This bit is used to specify whether to use the arbitration-lost detection function in master mode. Normally, set this bit to 1.

NALE bit (NACK Transmission Arbitration-Lost Detection Enable)

This bit is used to specify whether to cause arbitration to be lost when ACK is detected during transmission of NACK in receive mode (such as when slaves with the same address exist on the bus or when two or more masters select the same slave device simultaneously with different number of receive bytes).

27.2.5 BFCTL:总线功能控制寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x060

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	HSME	FMPE	—	SMBS	—	—	—	SCSYNE	—	—	—	—	—	SALE	NALE	MALE
重置后的值:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	MALE	主仲裁丢失检测启用 0：主机仲裁丢失检测禁用。禁用仲裁丢失检测功能，不清除CRMS和当仲裁丢失时，PRSST中的TRMD位会自动发生。 1：主仲裁丢失检测使能。启用仲裁丢失检测功能，并在仲裁丢失时自动清除PRST中的CRMS和TRMD位。	R/W
1	NALE	NACK传输仲裁丢失检测使能 0：NACK传输仲裁丢失检测禁用。1：NACK传输仲裁丢失检测使能。	R/W
2	SALE	从设备仲裁丢失检测使能 0：从设备仲裁丢失检测禁用。1：从机仲裁丢失检测使能。	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
8	SCSYNE	SCL同步电路使能 0：不使用SCL同步电路。1：使用SCL同步电路。	R/W
11:9	—	这些位被读取为0。写入值应为0。	R/W
12	SMBS	SMBusI2C总线选择 0：I2C总线选择。1：SMBus选择。	R/W
13	—	该位读取为0。写入值应为0。	R/W
14	FMPE*1	快速模式加启用 0：SCLn引脚和SDAn引脚不使用Fm+斜率控制电路。(n=0 1)1：Fm+斜率控制电路用于SCLn引脚和SDAn引脚。(n=0 1)	R/W
15	HSME*2	高速模式启用 0：禁用高速模式。1：使能高速模式。	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

注1.IIC0(SCL0_A SDA0_A)支持快速模式加使能位(FMPE)。Bit[14]是不支持通道中的保留位。

注2.IIC0(SCL0_A SDA0_A)支持高速模式使能位(HSME)。Bit[15]是不支持通道中的保留位。

MALE位（主仲裁丢失检测使能）

该位用于指定主机模式下是否使用仲裁丢失检测功能。通常，将此位设置为1。

NALE位（NACK传输仲裁丢失检测使能）

该位用于指定在接收模式下发送NACK过程中检测到ACK时是否导致仲裁丢失（例如总线上存在具有相同地址的从设备时，或者当两个或多个主设备同时选择同一个从设备时）不同数量的接收字节）。

SALE bit (Slave Arbitration-Lost Detection Enable)

This bit is used to specify whether to cause arbitration to be lost when a value different from the value being transmitted is detected on the bus in slave transmit mode (such as when slaves with the same address exist on the bus or when a mismatch with the transmit data occurs due to noise).

SCSYNE bit (SCL Synchronous Circuit Enable)

This bit is used to specify whether to synchronize the SCL clock with the SCL input clock. Normally, set this bit to 1.

When the SCSYNE bit set to 0 (no SCL synchronous circuit used), IIC does not synchronize the SCL clock with the SCL input clock. In this setting, IIC outputs the SCL clock with the transfer rate set in STDBR and EXTBR regardless of the SCLn line state. For this reason, if the bus load of the I^2C bus line is much larger than the specification value or if the SCL clock output overlaps in multiple masters, the short-cycle SCL clock that does not meet the specification may be output. When no SCL synchronous circuit uses, it also affects the issuance of a START condition, Repeated START condition, and STOP condition, and the continuous output of extra SCL clock cycles.

This bit must not be set to 0 except for checking the output of the set transfer rate.

FMPE bit (Fast-mode Plus Enable)

This bit is used to specify whether to use a slope control circuit for Fast-mode Plus [Fm+].

When this bit is set to 1, a slope control circuit conforming to the Fast-mode Plus [Fm+] slope control specification (tof) of the IIC-bus is selected. When this bit is set to 0, a slope control circuit conforming to the Standard-mode [Sm] and Fast-mode [fm] slope control specification (tof) of the IIC-bus is selected.

Set this bit to 1 when using the transmission rate within a range up to 1 Mbps (Fast-mode Plus [Fm+]) of the IIC-bus specification. Set this bit to 0 when using the transmission rate at other rates (up to 100 kbps [Sm], up to 400 kbps [Fm]) or for SMBus (10 to 100 kbps).

Note: When communicating in Hs-mode, set as follows.
- Set FMPE to 0 when sending Hs-mode master code (0000 1XXXb) with Fast-mode.
- Set FMPE to 1 when sending Hs-mode master code (0000 1XXXb) with Fast-mode Plus.

HSME bit (High Speed Mode Enable)

This bit is used for communicating in Hs-mode.

When this bit is set to 1, the Hs-mode master code is recognized and Hs-mode communication is possible.

After the START condition is detected, if Hs-mode master code (0000 1XXXb) transmission is recognized, Hs-mode communication starts from Repeated START after receiving the NACK response.

It communicates at the bit rate set in STDBR until the NACK response, and automatically switches from Repeated START condition issuance after receiving the NACK response to the bit rate set in EXTBR.

Hs-mode continues until a STOP condition is detected.

When the STOP condition is detected, the bit rate is automatically switched to the bit rate set in STDBR.

Note: When this bit is set to 1, the BST.NACKDF bit will not be set even if a NACK response is received after sending the Hs-mode master code.

SALE位（从设备仲裁丢失检测使能）

该位用于指定在从机发送模式下，当在总线上检测到与正在发送的值不同的值时（例如，当总线上存在具有相同地址的从机或与发送的值不匹配时，是否导致仲裁丢失由于噪声而发生传输数据）。

SCSYNE位（SCL同步电路使能）

该位用于指定是否将SCL时钟与SCL输入时钟同步。通常，将此位设置为1。

当SCSYNE位设置为0（不使用SCL同步电路）时，IIC不会将SCL时钟与SCL输入时钟同步。在此设置中，IIC以STDBR和EXTBR中设置的传输速率输出SCL时钟，而与SCLn线路状态无关。因此，如果I2C总线的总线负载远大于规格值，或者多个主机的SCL时钟输出重叠，则可能会输出不符合规格的短周期SCL时钟。当没有使用SCL同步电路时，它也会影响START条件、RepeatedSTART条件和

STOP条件，以及额外SCL时钟周期的连续输出。

该位不得设置为0，除非检查设置的传输速率的输出。

FMPE位（Fast-modePlusEnable）

该位用于指定是否对Fast-modePlus[Fm+]使用斜率控制电路。

当该位设置为1时，选择符合IIC总线的Fast-modePlus[Fm+]斜率控制规范(tof)的斜率控制电路。当该位设置为0时，选择符合IIC总线的标准模式[Sm]和快速模式[fm]斜率控制规范(tof)的斜率控制电路。

使用IIC总线规范的高达1Mbps(Fast-modePlus[Fm+])范围内的传输速率时，将此位设置为1。当使用其他速率（最高100kbps[Sm]、最高400kbps[Fm]）或SMBus（10至100kbps）的传输速率时，将此位设置为0。

Note: 在Hs模式下通信时，设置如下。●使用Fast-mode发送Hs-modemastercode(00001XXXb)时将FMPE设置为0。●使用Fast-modePlus发送Hs-mode主码(00001XXXb)时，将FMPE设置为1。

HSME位（高速模式启用）

该位用于在Hs模式下进行通信。

当该位设置为1时，识别Hs模式主代码并且可以进行Hs模式通信。

检测到START条件后，如果识别到Hs-mode主码(00001XXXb)传输，则Hs-mode通信在收到NACK响应后从重复START开始。

在收到NACK响应之前，它以STDBR中设置的比特率进行通信，并在收到NACK响应后自动从重复启动条件发出切换到EXTBR中设置的比特率。

Hs模式一直持续到检测到STOP条件。

当检测到STOP条件时，比特率自动切换到STDBR中设置的比特率。

Note: 当该位设置为1时，即使在发送后收到NACK响应，BST.NACKDF位也不会设置Hs-mode主码。

27.2.6 SVCTL : Slave Control Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x064

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SVAE2	SVAE1	SVAE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	HOAE	—	—	—	—	—	—	—	—	DVIDE	HSMCE	—	—	—	—	GCAE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	GCAE	General Call Address Enable 0: General call address detection disables. 1: General call address detection enables.	R/W
4:1	—	These bits are read as 0. The write value should be 0.	R/W
5	HSMCE*1	Hs-mode Master Code Enable 0: Hs-mode Master Code Detection disables. 1: Hs-mode Master Code Detection enables.	R/W
6	DVIDE	Device-ID Address Enable 0: Device-ID address detection disables. 1: Device-ID address detection enables.	R/W
14:7	—	These bits are read as 0. The write value should be 0.	R/W
15	HOAE	Host Address Enable 0: Host address detection disables. 1: Host address detection enables.	R/W
16	SVAE0	Slave Address Enable 0 0: Slave 0 disables 1: Slave 0 enables	R/W
17	SVAE1	Slave Address Enable 1 0: Slave 1 disables 1: Slave 1 enables	R/W
18	SVAE2	Slave Address Enable 2 0: Slave 2 disables 1: Slave 2 enables	R/W
31:19	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The Hs-mode Master Code Enable bit (HSMCE) is supported by IIC0 (SCL0_A, SDA0_A). Bit[5] is the reserved bit in the not suported channel.

GCAE bit (General Call Address Enable)

This bit is used to specify whether to ignore the general call address (0000 000 + 0 (write): All 0) when it is received. When this bit is set to 1, if the received slave address matches the general call address, IIC recognizes the received slave address as the general call address independently of the slave addresses set in the SVDVADy.SVAD[9:0] bits (y = 0 to 2) and performs data receive operation.

When this bit is set to 0, the received slave address is ignored even if it matches the general call address.

HSMCE bit (Hs-mode Master Code Enable)

This bit is used to specify whether to recognize and execute the Hs-mode master code (0000 1XXXb) is received in the first byte after a START condition is detected.

When this bit is set to 1, if the received first byte matches the Hs-mode master code, IIC recognizes that the Hs-mode master code has been received.

27.2.6 SVCTL:从控制寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x064

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SVAE2	SVAE1	SVAE0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	HOAE	—	—	—	—	—	—	—	—	DVIDE	HSMCE	—	—	—	—	GCAE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	GCAE	广播呼叫地址启用 0：广播呼叫地址检测禁用。1：广播呼叫地址检测使能。	R/W
4:1	—	这些位被读取为0。写入值应为0。	R/W
5	HSMCE*1	Hs模式主码启用 0：禁止Hs模式主码检测。1：Hs模式主码检测使能。	R/W
6	DVIDE	设备ID地址启用 0：禁用设备ID地址检测。1：Device-ID地址检测使能。	R/W
14:7	—	这些位被读取为0。写入值应为0。	R/W
15	HOAE	主机地址启用 0：主机地址检测禁用。1：主机地址检测使能。	R/W
16	SVAE0	从地址使能0 0：从机0禁用1：从机0使能	R/W
17	SVAE1	从地址使能1 0：从机1禁用1：从机1使能	R/W
18	SVAE2	从地址使能2 0：从机2禁用1：从机2使能	R/W
31:19	—	这些位被读取为0。写入值应为0。	R/W

注1.IIC0(SCL0_A SDA0_A)支持Hs模式主代码使能位(HSMCE)。Bit[5]是不支持通道中的保留位。

GCAE位（广播呼叫地址使能）

该位用于指定接收到的广播调用地址（0000000+0（写）：全0）是否忽略。当该位设置为1时，如果接收到的从机地址与广播呼叫地址匹配，IIC将接收到的从机地址识别为广播呼叫地址，独立于SVDVADy.SVAD[9:0]位中设置的从机地址（y=0到2)并执行数据接收操作。

当该位设置为0时，即使接收到的从机地址与广播呼叫地址匹配，也会忽略它。

HSMCE位（Hs模式主码启用）

该位用于指定在检测到START条件后的第一个字节中是否识别和执行Hs模式主代码（00001XXXb）。

当该位设置为1时，如果接收到的第一个字节与Hs模式主代码匹配，则IIC识别已接收到Hs模式主代码。

The first byte after Repeated START after NACK response to Hs-mode master code is recognized as a slave address and compared with the slave address set by SVDVADy.SVAD[9:0].

If the addresses match, the transmission / reception operation continues according to the R/W# bit value.

Hs-mode continues until a STOP condition is detected.

When this bit is set to 0, IIC will ignore the pattern until a STOP condition is detected, even if it matches the Hs-mode master code.

Note: When this bit is set to 1, SCSTRCTL.ACKTWE bit must be set to 0 and SCSTRCTL.RWE bit must be set to 1.

DVIDE bit (Device-ID Address Enable)

This bit is used to specify whether to recognize and execute the Device-ID address when a device ID (1111 100) is received in the first byte after a START condition or Repeated START condition is detected.

When this bit is set to 1, if the received first byte matches the Device-ID, IIC recognizes that the Device-ID address has been received. When the following R/W# bit is 0 (write), IIC recognizes the second and the following bytes as slave addresses and continues the receive operation.

When this bit is set to 0, IIC ignores the received first byte even if it matches the Device ID address and recognizes the first byte as a normal slave address.

For details on the Device-ID address detection, see (3)Device-ID Address Detection .

HOAE bit (Host Address Enable)

This bit is used to specify whether to ignore received host address (0001 000) when the BFCTL.SMBS bit = 1.

When this bit is set to 1 while the SMBS bit = 1, if the received slave address matches the host address, IIC recognizes the received slave address as the host address independently of the slave addresses set in the SVDVADy.SVAD[9:0] bits (y = 0 to 2) and performs the receive operation.

When the SMBS bit or the HOAE bit is set to 0, the received slave address is ignored even if it matches the host address.

SVAEy bits (Slave Address Enable y (y = 0 to 2))

This bit is used to enable or disable the slave address set in the SVDVADy.SVAD[9:0] bits.

When this bit is set to 1, the slave address set in the SVAD[9:0] bits is enabled and is compared with the received slave address.

When this bit is set to 0, the slave address set in the SVAD[9:0] bits is disabled and is ignored even if it matches the received slave address.

27.2.7 REFCKCTL : Reference Clock Control Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x070

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	IREFCKS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NACK响应Hs模式主机代码后重复START后的第一个字节被识别为从机地址，并与SVDVADy.SVAD[9:0]设置的从机地址进行比较。

如果地址匹配，则根据RW#位值继续发送接收操作。

Hs模式一直持续到检测到STOP条件。

当该位设置为0时，IIC将忽略该模式，直到检测到STOP条件，即使它与Hs模式主代码匹配。

Note: 当该位设置为1时，SCSTRCTL.ACKTWE位必须设置为0，SCSTRCTL.RWE位必须设置为1。

DVIDE位（设备ID地址启用）

该位用于指定在检测到START条件或重复START条件后的第一个字节中接收到设备ID(1111100)时是否识别和执行设备ID地址。

当该位设置为1时，如果接收到的第一个字节与Device-ID匹配，则IIC识别出已接收到Device-ID地址。当后面的RW#位为0（写）时，IIC将第二个和后面的字节识别为从地址并继续接收操作。

当该位设置为0时，IIC忽略接收到的第一个字节，即使它与设备ID地址匹配，并将第一个字节识别为正常的从地址。

关于Device-ID地址检测的详细信息，请参见（3）Device-ID地址检测。

HOAE位（主机地址使能）

该位用于指定当BFCTL.SMBS位=1时是否忽略接收到的主机地址(0001000)。

当该位设置为1且SMBS位=1时，如果接收到的从机地址与主机地址匹配，IIC将接收到的从机地址识别为主机地址，而与SVDVADy.SVAD[9:0]中设置的从机地址无关位（y=0到2）并执行接收操作。

当SMBS位或HOAE位设置为0时，即使接收到的从机地址与主机地址匹配，它也会被忽略。

SVAEy位（从地址启用y（y=0到2））

该位用于启用或禁用SVDVADy.SVAD[9:0]位中设置的从机地址。

当该位设置为1时，SVAD[9:0]位中设置的从机地址被启用，并与接收到的从机地址进行比较。

当该位设置为0时，在SVAD[9:0]位中设置的从地址被禁用并被忽略，即使它与接收到的从地址匹配。

27.2.7 RECKCTL:参考时钟控制寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x070

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	IREFCKS[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	IREFCKS[2:0]	Internal Reference Clock Selection Selects the internal reference clock source (IICφ) for IIC. 0 0 0: IICCLK/1 clock 0 0 1: IICCLK/2 clock 0 1 0: IICCLK/4 clock 0 1 1: IICCLK/8 clock 1 0 0: IICCLK/16 clock 1 0 1: IICCLK/32 clock 1 1 0: IICCLK/64 clock 1 1 1: IICCLK/128 clock	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

27.2.8 STDBR : Standard Bit Rate Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x074

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DSBRPO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15							8	7							0
Bit field:	SBRHO[7:0]								SBRLO[7:0]							
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	SBRLO[7:0]	Count value of the Low-level period of SCL clock	R/W
15:8	SBRHO[7:0]	Count value of the High-level period of SCL clock	R/W
30:16	—	These bits are read as 0. The write value should be 0.	R/W
31	DSBRPO	Double the Standard Bit Rate Period for Open-Drain 0: The time period set for SBRHO[7:0] and SBRLO[7:0] is not doubled. 1: The time period set for SBRHO[7:0] and SBRLO[7:0] is doubled.	R/W

The STDBR register sets the bit rate according to the operating speed (Standard-mode / Fast-mode / Fast-mode plus).

The I²C transfer rate and the SCL clock duty are calculated using the following expression.

Transfer rate = 1 / {[(High-Level Period + α*1) + (Low-Level Period + α)] / IICφ*2 + SCLn line rising time [tr]*3 + SCLn line falling time [tf]*3}

Duty cycle = {SCLn line rising time [tr] + (High-Level Period + α) / IICφ} / {SCLn line falling time [tf] + (Low- Level Period + α) / IICφ}

Note 1. α depend on the number of stages in the noise filter.
Note 2. IICφ = TCLK × Division ratio
Note 3. The SCLn line rising time [tr] and SCLn line falling time [tf] depend on the total bus line capacitance [Cb] and the pull-up resistor [Rp]. For details, see the I²C-bus specification from NXP Semiconductors.

SBRLO[7:0] bits (Count value of the Low-level period of SCL clock)

The SBRLO[7:0] bits are used to set the low-level period of SCL clock in Open-Drain mode.

IIC counts the low-level period with the internal reference clock source (IICφ) specified by the REFCKCTL.IREFCKS[2:0] bits. It also works to generate the data setup time for automatic SCL low-hold operation (see section 27.3.1.3.5. Clock Stretching); when IIC is used in I²C slave mode, these bits need to be set to a value longer than the data setup time*1.

If the digital noise filter is enabled (INCTL.DNFE = 1), set the SBRLO[7:0] bits to a value at least one greater than the number of stages in the noise filter. Regarding the number of stages in the noise filter, see the description of the INCTL.DNFS[3:0] bits.

Note 1. Data setup time (tSU: DAT)

Bit	Symbol	Function	R/W
2:0	IREFCKS[2:0]	内部参考时钟选择 为IIC选择内部参考时钟源(IICφ)。 0 0 0: IICCLK/1 clock 0 0 1: IICCLK/2 clock 0 1 0: IICCLK/4 clock 0 1 1: IICCLK/8 clock 1 0 0: IICCLK/16 clock 1 0 1: IICCLK/32 clock 1 1 0: IICCLK/64 clock 1 1 1: IICCLK/128 clock	R/W
31:3	—	这些位被读取为0。写入值应为0。	R/W

27.2.8 STDBR:标准比特率寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x074

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DSBRPO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15							8	7							0
Bit field:	SBRHO[7:0]								SBRLO[7:0]							
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	SBRLO[7:0]	SCL时钟低电平周期的计数值	R/W
15:8	SBRHO[7:0]	SCL时钟高电平周期计数值	R/W
30:16	—	这些位被读取为0。写入值应为0。	R/W
31	DSBRPO	开漏的标准比特率周期加倍 0：为SBRHO[7:0]和SBRLO[7:0]设置的时间周期不加倍。1：为SBRHO[7:0]和SBRLO[7:0]设置的时间周期加倍。	R/W

STDBR寄存器根据运行速度（标准模式快速模式加快速模式）设置比特率。

I2C传输速率和SCL时钟占空比使用以下表达式计算。

传输速率=1{[(High-LevelPeriod+α*1)+(Low-LevelPeriod+α)]IICφ*2+SCLn线上升时间[tr]*3+SCLn线下降时间[tf]*3

占空比={SCLn线路上升时间[tr]+(High-LevelPeriod+α)IICφ {SCLn线路下降时间[tf]+(LowLevelPeriod+α)IICφ

注1.α取决于噪声滤波器的级数。
注2.IICφ=TCLK×分频比
注3.SCLn线上升时间[tr]和SCLn线下降时间[tf]取决于总总线电容[Cb]和上拉电阻[Rp]。有关详细信息，请参阅NXPSemiconductors的I2C总线规范。

SBRLO[7:0]位（SCL时钟低电平周期的计数值）

SBRLO[7:0]位用于设置开漏模式下SCL时钟的低电平周期。

IIC使用REFCKCTL.IREFCKS[2:0]位指定的内部参考时钟源(IICφ)计算低电平周期。它还可以为自动SCL低保持操作生成数据建立时间（参见第27.3.1.3.5节。时钟拉伸）；在I2C从机模式下使用IIC时，需要将这些位设置为比数据建立时间长*1的值。

如果启用了数字噪声滤波器(INCTL.DNFE=1)，请将SBRLO[7:0]位设置为至少比噪声滤波器中的级数大1的值。关于噪声滤波器的级数，请参见INCTL.DNFS[3:0]位的说明。

注1.数据建立时间(tSU:DAT)

250 ns (up to 100 kbps: Standard-mode [Sm])

100 ns (up to 400 kbps: Fast-mode [Fm])

50 ns (up to 1 Mbps: Fast-mode plus [Fm+])

10 ns (up to 3.4 Mbps: Hs-mode [HS])

SBRHO[7:0] bits (Count value of the High-level period of SCL clock)

The SBRHO[7:0] bits use to set the high-level period of SCL clock in Open-Drain mode. SBRHO[7:0] bits are valid in master mode. If IIC is used only in I2C slave mode, these bits need not to set the highlevel period.

IIC counts the high-level period with the internal reference clock source (IICφ) specified by the REFCKCTL.IREFCKS[2:0] bits.

If the digital noise filter is enabled (the INCTL.DNFE bit = 1), set the SBRHO[7:0] bits to a value at least one greater than the number of stages in the noise filter. Regarding the number of stages in the noise filter, see the description of the INCTL.DNFS[3:0] bits.

DSBRPO bit (Double the Standard Bit Rate Period for Open-Drain)

When DSBRPO = 1, double the high-level period that is set in SBRHO[7:0] and double the low-level period that is set in SBRLO[7:0].

Table 27.4 Requirement and usage of setting in each mode

Bit name	Device mode	
	I2C master	I2C slave
SBRHO[7:0]	Setting required*1	Do not use
SBRLO[7:0]	Setting required*1	Setting required*2

Note 1. The setting value is used for the data rate of ST, FM, and FM+ mode.

Note 2. The setting value is used for the data setup time of automatic SCL low-hold operation.

27.2.9 EXTBR : Extended Bit Rate Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x078

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EBRHO[7:0]								EBRLO[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	EBRLO[7:0]	Extended Bit Rate Low-Level Period Open-Drain Count value of the low-level period of SCL clock	R/W
15:8	EBRHO[7:0]	Extended Bit Rate High-Level Period Open-Drain Count value of the high-level period of SCL clock	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The EXTBR register sets the bit rate for communication in high-speed mode.

EBRLO[7:0] bits (Extended Bit Rate Low-Level Period Open-Drain)

See SBRLO[7:0] bits of section 27.2.8. STDBR : Standard Bit Rate Register for details. Watch SBRHO, SBRLO as EBRHO[7:0], EBRLO[7:0].

EBRHO[7:0] bits (Extended Bit Rate High-Level Period Open-Drain)

See SBRHO[7:0] bits of section 27.2.8. STDBR : Standard Bit Rate Register for details. Watch SBRHO, SBRLO as EBRHO[7:0], EBRLO[7:0].

250 ns (up to 100 kbps: Standard-mode [Sm])

100 ns (up to 400 kbps: Fast-mode [Fm])

50ns（高达1Mbps：快速模式加[Fm+]）

10 ns (up to 3.4 Mbps: Hs-mode [HS])

SBRHO[7:0]位（SCL时钟高电平周期的计数值）

SBRHO[7:0]位用于设置开漏模式下SCL时钟的高电平周期。SBRHO[7:0]位在主机模式下有效。如果IIC仅用于I2C从机模式，则这些位无需设置高电平周期。

IIC使用指定的内部参考时钟源(IICφ)计算高电平周期
REFCKCTL.IREFCKS[2:0] bits.

如果启用了数字噪声滤波器（INCTL.DNFE位=1），请将SBRHO[7:0]位设置为至少比噪声滤波器的级数大1的值。关于噪声滤波器的级数，请参见INCTL.DNFS[3:0]位的说明。

DSBRPO位（开漏的标准比特率周期加倍）

当DSBRPO=1时，将SBRHO[7:0]中设置的高电平周期加倍，将SBRHO[7:0]中设置的低电平周期加倍
SBRLO[7:0].

Table 27.4 各模式设置要求及使用

位名称	设备模式	
	I2C master	I2C slave
SBRHO[7:0]	需要设置*1	不使用
SBRLO[7:0]	需要设置*1	需要设置*2

注1.设定值用于ST、FM和FM+模式的数据速率。

注2.该设定值用于自动SCL低保持操作的数据建立时间。

27.2.9 EXTBR:扩展比特率寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x078

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EBRHO[7:0]								EBRLO[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	EBRLO[7:0]	ExtendedBitRateLow-LevelPeriodOpen-DrainCount值SCL时钟的低电平周期	R/W
15:8	EBRHO[7:0]	ExtendedBitRateHigh-LevelPeriodOpen-DrainCount值SCL时钟的高电平周期	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

EXTBR寄存器设置高速模式下通信的比特率。

EBRLO[7:0]位（扩展比特率低电平周期开漏）

请参见第27.2.8节的SBRLO[7:0]位。STDBR：标准比特率寄存器了解详情。将SBRHO、SBRLO视为EBRHO[7:0], EBRLO[7:0].

EBRHO[7:0]位（扩展比特率高电平周期开漏）

请参见第27.2.8节的SBRHO[7:0]位。STDBR：标准比特率寄存器了解详情。将SBRHO、SBRLO视为EBRHO[7:0], EBRLO[7:0].

Table 27.5 Requirement and usage of setting in each mode

Bit name	Device mode	
	I²C master	I²C slave
EBRHO[7:0]	Setting required*1	Do not use
EBRLO[7:0]	Setting required*1	Setting required*2

Note 1. The setting value is used for the data rate of HS-mode.
Note 2. The setting value is used for the data setup time of automatic SCL low-hold operation in HS-mode.

27.2.10 BFRECDT : Bus Free Condition Detection Time Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)
Offset address: 0x07C

Bit position:	31 … 9	8 … 0
Bit field:	—	FRECYC[8:0]
Value after reset:	0	0

Bit	Symbol	Function	R/W
8:0	FRECYC[8:0]	Bus Free Condition Detection Cycle The count value is a period for detecting the Bus free condition.	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

FRECYC[8:0] bits (Bus Free Condition Detection Cycle)

IIC counts the period for detecting the Bus free condition with the IICφ.

These bits set the Bus Free period. This Bus Free period is counted by the internal reference clock (IICφ) selected by the REFCKCTL.IREFCKS[2:0] bits. See the BCST.BFREF flag for Bus Free detection behavior.

27.2.11 OUTCTL : Output Control Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)
Offset address: 0x088

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10 … 8	7	6	5	4	3	2	1	0
Bit field:	SDODCS	—	—	—	—	SDOD[2:0]	—	—	—	EXCYC	—	SOCWP	SCOC	SDOC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	SDOC	SDA Output Control 0: IIC drives the SDAn pin low. 1: IIC releases the SDAn pin.	R/W
1	SCOC	SCL Output Control High level output is achieved through an external pull-up resistor. 0: IIC drives the SCLn pin low. 1: IIC releases the SCLn pin.	R/W

Table 27.5 各模式设置要求及使用

位名称	设备模式	
	I²C master	I²C slave
EBRHO[7:0]	需要设置*1	不使用
EBRLO[7:0]	需要设置*1	需要设置*2

注1.该设置值用于HS模式的数据速率。
注2.该设置值用于HS模式下自动SCL低保持操作的数据建立时间。

27.2.10 BFRECDT:总线空闲状态检测时间寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)
Offset address: 0x07C

Bit position:	31 … 9	8 … 0
Bit field:	—	FRECYC[8:0]
重置后的值:	0	0

Bit	Symbol	Function	R/W
8:0	FRECYC[8:0]	总线空闲状态检测周期 计数值是检测总线空闲状态的周期。	R/W
31:9	—	这些位被读取为0。写入值应为0。	R/W

FRECYC[8:0]位（总线空闲状态检测周期）

IIC使用IICφ计算检测总线空闲状态的周期。

这些位设置总线空闲周期。该总线空闲周期由内部参考时钟(IICφ)由所选的REFCKCTL.IREFCKS[2:0]位。请参阅BCST.BFREF标志了解BusFree检测行为。

27.2.11 OUTCTL:输出控制寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)
Offset address: 0x088

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10 … 8	7	6	5	4	3	2	1	0
Bit field:	SDODCS	—	—	—	—	SDOD[2:0]	—	—	—	EXCYC	—	SOCWP	SCOC	SDOC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	SDOC	SDA输出控制 0：IIC将SDAn引脚驱动为低电平。1：IIC释放SDAn引脚。	R/W
1	SCOC	SCL输出控制 通过外部上拉电阻实现高电平输出。 0：IIC将SCLn引脚驱动为低电平。1：IIC释放SCLn引脚。	R/W

Bit	Symbol	Function	R/W
2	SOCWP	SCL/SDA Output Control Write Protect 0: Bits SCOC and SDOC are protected. 1: Bits SCOC and SDOC can be written (When writing simultaneously with the value of the target bit). This bit is read as 0.	W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	EXCYC	Extra SCL Clock Cycle Output The EXCYC bit is cleared automatically after one clock cycle is output. 0: Does not output an extra SCL clock cycle (default). 1: Outputs an extra SCL clock cycle.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
10:8	SDOD[2:0]	SDA Output Delay 0 0 0: No output delay 0 0 1: 1 IICφ cycle (When OUTCTL.SDODCS = 0 (IICφ)) 1 or 2 IICφ cycles (When OUTCTL.SDODCS = 1 (IICφ/2)) 0 1 0: 2 IICφ cycles (When OUTCTL.SDODCS = 0 (IICφ)) 3 or 4 IICφ cycles (When OUTCTL.SDODCS = 1 (IICφ/2)) 0 1 1: 3 IICφ cycles (When OUTCTL.SDODCS = 0 (IICφ)) 5 or 6 IICφ cycles (When OUTCTL.SDODCS = 1 (IICφ/2)) 1 0 0: 4 IICφ cycles (When OUTCTL.SDODCS = 0 (IICφ)) 7 or 8 IICφ cycles (When OUTCTL.SDODCS = 1 (IICφ/2)) 1 0 1: 5 IICφ cycles (When OUTCTL.SDODCS = 0 (IICφ)) 9 or 10 IICφ cycles (When OUTCTL.SDODCS = 1 (IICφ/2)) 1 1 0: 6 IICφ cycles (When OUTCTL.SDODCS = 0 (IICφ)) 11 or 12 IICφ cycles (When OUTCTL.SDODCS = 1 (IICφ/2)) 1 1 1: 7 IICφ cycles (When OUTCTL.SDODCS = 0 (IICφ)) 13 or 14 IICφ cycles (When OUTCTL.SDODCS = 1 (IICφ/2))	R/W
14:11	—	These bits are read as 0. The write value should be 0.	R/W
15	SDODCS	SDA Output Delay Clock Source Selection 0: The internal reference clock (IICφ) is selected as the clock source of the SDA output delay counter. 1: The internal reference clock divided by 2 (IICφ/2) is selected as the clock source of the SDA output delay counter.*1	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The setting SDODCS = 1 (IICφ/2) only becomes valid when SCL is at the low level. When SCL is at the high level, the setting SDODCS = 1 becomes invalid and the clock source becomes the internal reference clock (IICφ).

SDOC bit (SDA Output Control) and SCOC bit (SCL Output Control)

These bits are used to directly control the SDAn and SCLn signals output from this module.

When writing to these bits, also write 1 to the SOCWP bit at the same time.

The result of setting these bits is input to IIC via the input buffer. When slave mode is selected, a START condition may be detected and the bus may be released depending on the bit settings.

Do not rewrite these bits during a START condition, STOP condition, Repeated START condition, or during transmission or reception. Operation after rewriting under the above conditions is not guaranteed.

EXCYC bit (Extra SCL Clock Cycle Output)

This bit is used to output an extra SCL clock cycle for debugging or error processing.

Normally, set the bit to 0. Setting the bit to 1 in a normal communication state causes a communication error.

For details on this function, see section 27.3.1.3.6. Port Control , (1)Extra SCL Clock Cycle Output Function.

Bit	Symbol	Function	R/W
2	SOCWP	SCLSDA输出控制写保护 0：SCOC和SDOC位被保护。1：可写入位SCOC和SDOC（与目标位的值同时写入时）。该位读为0。	W
3	—	该位读取为0。写入值应为0。	R/W
4	EXCYC	额外的SCL时钟周期输出 EXCYC位在输出一个时钟周期后自动清零。 0：不输出额外的SCL时钟周期（默认）。1：输出一个额外的SCL时钟周期。	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
10:8	SDOD[2:0]	SDA输出延迟 000：无输出延迟001：1个IICφ周期（当OUTCTL.SDODCS=0(IICφ)时） 1或2个IICφ周期（当OUTCTL.SDODCS=1(IICφ2)时） 0 1 0: 2 IICφ cycles (When OUTCTL.SDODCS = 0 (IICφ)) 3或4个IICφ周期（当OUTCTL.SDODCS=1(IICφ2)时） 0 1 1: 3 IICφ cycles (When OUTCTL.SDODCS = 0 (IICφ)) 5或6个IICφ周期（当OUTCTL.SDODCS=1(IICφ2)时） 1 0 0: 4 IICφ cycles (When OUTCTL.SDODCS = 0 (IICφ)) 7或8个IICφ周期（当OUTCTL.SDODCS=1(IICφ2)时） 1 0 1: 5 IICφ cycles (When OUTCTL.SDODCS = 0 (IICφ)) 9或10个IICφ周期（当OUTCTL.SDODCS=1(IICφ2)时） 1 1 0: 6 IICφ cycles (When OUTCTL.SDODCS = 0 (IICφ)) 11或12个IICφ周期（当OUTCTL.SDODCS=1(IICφ2)时） 1 1 1: 7 IICφ cycles (When OUTCTL.SDODCS = 0 (IICφ)) 13或14个IICφ周期（当OUTCTL.SDODCS=1(IICφ2)时）	R/W
14:11	—	这些位被读取为0。写入值应为0。	R/W
15	SDODCS	SDA输出延迟时钟源选择 0：选择内部参考时钟（IICφ）作为SDA输出延迟计数器的时钟源。 1：选择内部参考时钟2分频（IICφ2）作为SDA输出延迟计数器的时钟源。*1	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

注1.设置SDODCS=1(IICφ2)仅在SCL为低电平时有效。当SCL为高电平时，设置SDODCS=1无效，时钟源变为内部参考时钟(IICφ)。

SDOC位（SDA输出控制）和SCOC位（SCL输出控制）

这些位用于直接控制从该模块输出的SDAn和SCLn信号。

写入这些位时，也要同时向SOCWP位写入1。

设置这些位的结果通过输入缓冲器输入到IIC。Whenslavemodeisselected aSTARTconditionmaybedetectedandthebusmaybereleaseddependingonthebitsettings.

请勿在START条件、STOP条件、重复START条件或发送或接收期间重写这些位。不保证在上述条件下重写后的操作。

EXCYC位（额外SCL时钟周期输出）

该位用于输出额外的SCL时钟周期，用于调试或错误处理。

通常将该位设置为0。在正常通信状态下将该位设置为1会导致通信错误。

有关此功能的详细信息，请参见第27.3.1.3.6节。端口控制，（1）额外的SCL时钟周期输出功能。

27.2.12 INCTL : Input Control Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x08C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3			0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DNFE	DNFS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0

Bit	Symbol	Function	R/W
3:0	DNFS[3:0]	Digital Noise Filter Stage Selection 0x0: Noise of up to one IICφ cycle is filtered out (singlestage filter). 0x1: Noise of up to two IICφ cycles is filtered out (2-stage filter). 0x2: Noise of up to three IICφ cycles is filtered out (3-stage filter). 0x3: Noise of up to four IICφ cycles is filtered out (4-stage filter). 0x4: Noise of up to five IICφ cycles is filtered out (5-stage filter). ⋮ 0xF: Noise of up to sixteen IICφ cycles is filtered out (16-stage filter).	R/W
4	DNFE	Digital Noise Filter Circuit Enable 0: No digital noise filter circuit is used. 1: A digital noise filter circuit is used.	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
7:6	—	These bits are read as 1. The write value should be 1.	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

DNFS[3:0] bits (Digital Noise Filter Stage Selection)

These bits are used to select the number of stages in the digital noise filter.

For details on the digital noise filter function, see section 27.3.1.6.3. Digital Noise-Filter Circuits .

In I^2C High Speed mode, the module changes the number of noise filter stage to a quarter of the number of noise filter stage automatically.

Note:
- Set the noise range to be filtered out by the noise filter within a range less than the SCLn line high-level period or low-level period. If the noise range is set to a value of (SCL clock width: high-level period or lowlevel period, whichever is shorter) - [1.5 internal reference clock (IICφ) cycles] or more, the SCL clock is regarded as noise by the noise filter function of IIC, which may prevent IIC from operating normally.
- In I^2C High Speed mode, the lower 2 bits of the DNFS [3:0] bits are ignored, and the number of filter stages for 1 to 4 stages is selected by the upper 2 bits.

27.2.12 INCTL:输入控制寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x08C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3			0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DNFE	DNFS[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0

Bit	Symbol	Function	R/W
3:0	DNFS[3:0]	数字噪声滤波器级选择 0x0：过滤掉最多一个IICφ周期的噪声（单级滤波器）。0x1：过滤掉最多两个IICφ周期的噪声（2级滤波器）。0x2：过滤掉最多三个IICφ周期的噪声（3级滤波器）。0x3：过滤掉最多四个IICφ周期的噪声（4级滤波器）。0x4：过滤掉最多五个IICφ周期的噪声（5级滤波器）。 0xF：过滤掉多达16个IICφ周期的噪声（16级滤波器）。	R/W
4	DNFE	数字噪声滤波器电路使能 0：不使用数字噪声滤波电路。1：使用数字噪声滤波电路。	R/W
5	—	该位读取为0。写入值应为0。	R/W
7:6	—	这些位被读取为1。写入值应为1。	R/W
31:8	—	这些位被读取为0。写入值应为0。	R/W

DNFS[3:0]位（数字噪声滤波器级选择）

这些位用于选择数字噪声滤波器的级数。

有关数字噪声滤波器功能的详细信息，请参阅第27.3.1.6.3节。数字噪声滤波器电路。

在I2C高速模式下，模块自动将噪声滤波器级数更改为噪声滤波器级数的四分之一。

Note:
- ●将噪声滤波器滤除的噪声范围设置在小于SCLn线高电平周期或低电平周期的范围内。如果噪声范围设置为（SCL时钟宽度：高电平周期或低电平周期，以较短者为准）[1.5个内部参考时钟(IICφ)周期]或更大的值，则SCL时钟被噪声视为噪声IIC的过滤功能，可能会导致IIC无法正常工作。
- ●在I2C高速模式下，DNFS[3:0]位的低2位被忽略，1到4级的滤波器级数由高2位选择。

27.2.13 TMOCTL : Timeout Control Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x090

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	TOMDS[1:0]		TOHCTL	TOLCTL	—	—	TODTS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bit	Symbol	Function	R/W
1:0	TODTS[1:0]	Timeout Detection Time Selection 0 0: 16bit-timeout 0 1: 14bit-timeout 1 0: 8bit-timeout 1 1: 6bit-timeout	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	TOLCTL	Timeout L Count Control 0: Count is disabled while the SCLn line is at a low level. 1: Count is enabled while the SCLn line is at a low level.	R/W
5	TOHCTL	Timeout H Count Control 0: Count is disabled while the SCLn line is at a high level. 1: Count is enabled while the SCLn line is at a high level.	R/W
7:6	TOMDS[1:0]	Timeout Operation Mode Selection 0 0: Timeout is detected during the following conditions: ● The bus is busy (BCST.BFREF = 0) in master mode. ● IIC's own slave address is detected and the bus is busy in slave mode. ● The bus is free (BCST.BFREF = 1) while generation of a START condition is requested (CNDCTL.STCND = 1). 0 1: Timeout is detected while the bus is busy. 1 0: Timeout is detected while the bus is free. 1 1: Setting prohibited	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

TODTS[1:0] bits (Timeout Detection Time Selection)

These bits are used to select for the timeout detection time when the timeout function is enabled (BSTE.TODE bit = 1).

When these bits are set to 00b, the timeout detection internal counter functions as a 16-bit counter.

When these bits are set to 01b, the counter functions as a 14-bit counter.

When these bits are set to 10b, the counter functions as a 8-bit counter.

When these bits are set to 11b, the counter functions as a 6-bit counter.

While the SCLn line is in the state that enables this counter as specified by bits TOHCTL and TOLCTL, the counter counts up in synchronization with the internal reference clock (IICφ) as a count source.

For details on the timeout function, see section 27.3.1.4.1. Timeout Error Detection .

TOLCTL bit (Timeout L Count Control)

This bit is used to enable or disable the internal counter of the timeout function to count up while the SCLn line is held low when the timeout function is enabled (BSTE.TODE = 1).

TOHCTL bit (Timeout H Count Control)

This bit is used to enable or disable the internal counter of the timeout function to count up while the SCLn line is held high when the timeout function is enabled (BSTE.TODE = 1).

27.2.13 TMOCTL:超时控制寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x090

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	TOMDS[1:0]		TOHCTL	TOLCTL	—	—	TODTS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bit	Symbol	Function	R/W
1:0	TODTS[1:0]	超时检测时间选择 0 0: 16bit-timeout 0 1: 14bit-timeout 1 0: 8bit-timeout 1 1: 6bit-timeout	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	TOLCTL	超时L计数控制 0：SCLn线为低电平时禁止计数。1：SCLn线为低电平时使能计数。	R/W
5	TOHCTL	超时H计数控制 0：SCLn线为高电平时禁止计数。1：SCLn线为高电平时使能计数。	R/W
7:6	TOMDS[1:0]	超时操作模式选择 00：在以下情况下检测到超时：● 在主机模式下总线繁忙（BCST.BFREF=0）。 ● 检测到IIC自己的从机地址，总线在从机模式下忙。 ● 总线空闲(BCST.BFREF=1)，同时请求生成START条件(CNDCTL.STCND=1)。 01：总线忙时检测到超时。10：总线空闲时检测到超时。11：禁止设定	R/W
31:8	—	这些位被读取为0。写入值应为0。	R/W

TODTS[1:0]位（超时检测时间选择）

这些位用于选择启用超时功能时的超时检测时间（BSTE.TODE位=1）。

当这些位设置为00b时，超时检测内部计数器用作16位计数器。

当这些位设置为01b时，计数器用作14位计数器。

当这些位设置为10b时，计数器用作8位计数器。

当这些位设置为11b时，计数器用作6位计数器。

当SCLn线处于启用由位TOHCTL和TOLCTL指定的该计数器的状态时，计数器与作为计数源的内部参考时钟(IICφ)同步计数。

超时功能详见27.3.1.4.1节。超时错误检测。

TOLCTL位（超时L计数控制）

该位用于启用或禁用超时功能的内部计数器以在启用超时功能时（BSTE.TODE=1）在SCLn线保持低电平时向上计数。

TOHCTL位（超时H计数控制）

该位用于启用或禁用超时功能的内部计数器以在启用超时功能（BSTE.TODE=1）时SCLn线保持高电平时向上计数。

TOMDS[1:0] bits (Timeout Operation Mode Selection)

These bits are used to select the detection condition for timeout when the timeout function is enabled.

27.2.14 WUCTL : Wake Up Unit Control Register

Base address: IIC0WU_B = 0x4009_F098

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	WUFE	WUFSYNE	—	WUANFS	—	—	—	WUACKS
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	WUACKS	Wake-Up Acknowledge Selection Choice of four response mode with a combination of RSTCTL.INTLRST bit and WUACKS bit. Shown in Table 27.6.	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	WUANFS	Wake-Up Analog Noise Filter Selection 0: Do not add the Wake Up analog filter. 1: Add the Wake Up analog filter.	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
6	WUFSYNE	Wake-Up function PCLKA Synchronous Enable 0: IIC asynchronous circuit enable 1: IIC synchronous circuit enable	R/W
7	WUFE	Wake-Up function Enable Do not set WUFE = 0 during Wake-Up operation. 0: Wake-up function disables 1: Wake-up function enables	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

Table 27.6 Wake-Up Mode

INTLRST	WUACKS	Operation mode	Description
0	0	Normal Wake-Up mode 1	ACK response at 9th SCL and SCL low hold after at 9th SCL.
0	1	Normal Wake-Up mode 2	No ACK response immediately and SCL low hold between 8th and 9th SCL. Release SCL low hold and ACK response at 9th SCL.
1	0	Command recovery mode	ACK response at 9th SCL and not SCL low hold.
1	1	EEP response mode	NACK response at 9th SCL and not SCL low hold.

Note: In WakeUp mode 2, HS mode can not be used.

WUFSYNE bit (Wake-Up function PCLKA Synchronous Enable)

This bit is used to switch between the PCLKA/IICCLK synchronous operation and the PCLKA/IICCLK asynchronous operation.

The bit is used in combination with the WUASYNF flag at Wake-Up effective function (WUCTL.WUFE bit = 1).

[When switching from the PCLKA/IICCLK synchronous operation to the PCLKA/IICCLK asynchronous operation]

IIC operation changes into the PCLKA/IICCLK asynchronous operation during BCST.BFREF flag = 1, when the WUASYNF flag set to 1 during WUFSYNE = 0.

TOMDS[1:0]位（超时操作模式选择）

这些位用于选择启用超时功能时的超时检测条件。

27.2.14 WUCTL:唤醒单元控制寄存器

Base address: IIC0WU_B = 0x4009_F098

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	WUFE	WUFSYNE	—	WUANFS	—	—	—	WUACKS
重置后的值：	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	WUACKS	唤醒确认选择 通过RSTCTL.INTLRST位和WUACKS位的组合选择四种响应模式。如表27.6所示。	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
4	WUANFS	唤醒模拟噪声滤波器选择 0：不添加唤醒模拟滤波器。1：添加唤醒模拟滤波器。	R/W
5	—	该位读取为0。写入值应为0。	R/W
6	WUFSYNE	唤醒功能PCLKA同步使能 0：IIC异步电路使能1：IIC同步电路使能	R/W
7	WUFE	唤醒功能启用 在唤醒操作期间不要设置WUFE=0。 0：唤醒功能禁用1：唤醒功能启用	R/W
31:8	—	这些位被读取为0。写入值应为0。	R/W

Table 27.6 Wake-Up Mode

INTLRST	WUACKS	操作模式	Description
0	0	正常唤醒模式1	第9个SCL的ACK响应和第9个SCL后的SCL低电平保持。
0	1	正常唤醒模式2	没有ACK立即响应，并且SCL在第8和第9个SCL之间保持低电平。在第9个SCL释放SCL低保持和ACK响应。
1	0	命令恢复模式	第9个SCL的ACK响应，而不是SCL低保持。
1	1	EEP响应模式	NACK在第9个SCL响应，而不是SCL低保持。

Note: 在唤醒模式2中，不能使用HS模式。

WUFSYNE位（唤醒功能PCLKA同步使能）

该位用于在PCLKAIICCLK同步操作和PCLKAIICCLK异步操作之间切换。

该位与唤醒有效功能中的WUASYNF标志结合使用（WUCTL.WUFE位=1）。

[从PCLKAIICCLK同步操作切换到PCLKAIICCLK异步操作时]

IIC操作在BCST.BFREF标志=1期间变为PCLKAIICCLK异步操作，当WUASYNF标志在WUFSYNE=0期间设置为1。

The reception can operate without depending on the state of operation of PCLKA/IICCLK (With PCLKA/IICCLK stopped) after it switches to the PCLKA/IICCLK asynchronous operation (Wake-Up event detection operation).

[When switching from the PCLKA/IICCLK asynchronous operation to the PCLKA/IICCLK synchronous operation]

IIC operation changes into the PCLKA/IICCLK synchronous operation at the following conditions. (At the same timing when WUFSYNE flag becomes 0)

In the case Wake-Up event detects : right after WUFSYNE bit is set to 1.

In the case Wake-Up event does not detect : when STOP condition is detected after WUFSYNE bit is set to 1.

[Setting condition]

- When 1 is written to the WUFSYNE bit.
- WUCTL.WUFE = 0

[Clearing conditions]

- When 0 is written to the WUFSYNE bit.

27.2.15 ACKCTL : Acknowledge Control Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	ACKTWP	ACKT	ACKR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ACKR	Acknowledge Reception 0: A 0 is received as the acknowledge bit (ACK reception). 1: A 1 is received as the acknowledge bit (NACK reception).	R
1	ACKT	Acknowledge Transmission 0: A 0 is sent as the acknowledge bit (ACK transmission). 1: A 1 is sent as the acknowledge bit (NACK transmission).	R/W
2	ACKTWP	ACKT Write Protect 0: The ACKT bit are protected. 1: The ACKT bit can be written (when writing simultaneously with the value of the target bit). This bit is read as 0.	W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

ACKR bit (Acknowledge Reception)

This bit is used to store the acknowledge bit information received from the receive device in transmit mode.

[Setting condition]

- When 1 is received as the acknowledge bit with the PRSST.TRMD bit set to 1.

[Clearing conditions]

- When 0 is received as the acknowledge bit with the PRSST.TRMD bit set to 1.

ACKT bit (Acknowledge Transmission)

[Setting condition]

在切换到PCLKAIICCLK异步操作（唤醒事件检测操作）后，接收可以不依赖于PCLKAIICCLK的操作状态（PCLKAIICCLK停止）进行操作。

[从PCLKAIICCLK异步操作切换到PCLKAIICCLK同步操作时]

IIC操作在以下条件下变为PCLKAIICCLK同步操作。（在WUFSYNE标志变为0的同时）

如果唤醒事件检测到：在WUFSYNE位设置为1之后。

在未检测到唤醒事件的情况下：当WUFSYNE位设置为1后检测到STOP条件时。

[Setting condition]

●WUFSYNE位写入1时。

- WUCTL.WUFE = 0

[Clearing conditions]

●WUFSYNE位写入0时。

27.2.15 ACKCTL:确认控制寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	ACKTWP	ACKT	ACKR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ACKR	确认接收 0：接收到0作为确认位（ACK接收）。1：接收到1作为确认位（NACK接收）。	R
1	ACKT	确认传输 0：发送0作为确认位（ACK传输）。1：发送1作为确认位（NACK传输）。	R/W
2	ACKTWP	ACKT写保护 0：ACKT位被保护。1：可以写入ACKT位（与目标位的值同时写入时）。该位读为0。	W
31:3	—	这些位被读取为0。写入值应为0。	R/W

ACKR bit (Acknowledge Reception)

该位用于存储在发送模式下从接收设备接收到的确认位信息。

[Setting condition]

●当PRSST.TRMD位设置为1接收到1作为确认位时。

[Clearing conditions]

●当PRSST.TRMD位设置为1接收到0作为确认位时。

ACKT bit (Acknowledge Transmission)

[Setting condition]

- When 1 is written to the ACKT bit and 1 is written to the ACKTWP bit at the same time.

[Clearing conditions]

- When 0 is written to the ACKT bit and 1 is written to the ACKTWP bit at the same time.
- When a STOP condition is detected. (when a STOP condition is detected with the CNDCTL.SPCND bit set to 1.)

Note: Set the ACKT bit to 0 in I²C Slave mode.

ACKTWP bit (ACKT Write Protect)

This bit is used to control the modification of the ACKT bit.

When changing the ACKT bit, setting this bit to 1 at the same time can change the ACKT bit.

When this bit is read, 0 is always read.

27.2.16 SCSTRCTL : SCL Stretch Control Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0A4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RWE	ACKTWE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ACKTWE	Acknowledge Transmission Wait Enable 0: NTST.RDBFF0 is set at the rising edge of the ninth SCL clock cycle. (The SCLn line is not held low at the falling edge of the eighth clock cycle.) 1: NTST.RDBFF0 is set at the rising edge of the eighth SCL clock cycle. (The SCLn line is held low at the falling edge of the eighth clock cycle.) Low-hold is released by writing a value to the ACKCTL.ACKT bit.	R/W
1	RWE	Receive Wait Enable 0: No WAIT (The period between ninth clock cycle and first clock cycle is not held low.) 1: WAIT (The period between ninth clock cycle and first clock cycle is held low.) Low-hold is released by reading NTDTBP0	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

ACKTWE bit (Acknowledge Transmission Wait Enable)

This bit is used to select the NTST.RDBFF0 flag set timing in receive mode and also to select whether to hold the SCLn line low at the falling edge of the eighth SCL clock cycle.

When ACKTWE = 0, the SCLn line is not held low at the falling edge of the eighth SCL clock cycle, and the NTST.RDBFF0 flag is set to 1 at the rising edge of the ninth SCL clock cycle.

When ACKTWE = 1, the NTST.RDBFF0 flag is set to 1 at the rising edge of the eighth SCL clock cycle and the SCLn line is held low at the falling edge of the eighth SCL clock cycle. The low-hold of the SCLn line is released by writing a value to the ACKCTL.ACKT bit.

After data is received with this setting, the SCLn line is automatically held low before the acknowledge bit is sent. This enables processing to send ACK (ACKCTL.ACKT = 0) or NACK (ACKCTL.ACKT = 1) according to receive data.

●向ACKT位写入1和向ACKTWP位同时写入1时。

[Clearing conditions]

●当0被写入ACKT位和1被同时写入ACKTWP位时。

●检测到停止条件时。（当CNDCTL.SPCND位设置为1时检测到STOP条件。）

Note: 在I2C从模式下将ACKT位设置为0。

ACKTWP位（ACKT写保护）

该位用于控制ACKT位的修改。

在改变ACKT位时，同时将该位设置为1可以改变ACKT位。

读取该位时，始终读取0。

27.2.16 SCSTRCTL:SCL拉伸控制寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0A4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RWE	ACKTWE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ACKTWE	确认传输等待启用 0：NTST.RDBFF0在第9个SCL时钟周期的上升沿置位。（SCLn线在第八个时钟周期的下降沿不保持低电平。） 1：NTST.RDBFF0在第8个SCL时钟周期的上升沿置位。（SCLn线在第八个时钟周期的下降沿保持低电平。）通过向ACKCTL.ACKT位写入一个值来释放低电平保持。	R/W
1	RWE	接收等待启用 0：无等待（第9个时钟周期和第一个时钟周期之间的周期不保持低电平。） 1：WAIT（第9个时钟周期和第一个时钟周期之间的周期保持低电平。）通过读取NTDTBP0释放低电平保持	R/W
31:2	—	这些位被读取为0。写入值应为0。	R/W

ACKTWE位（确认发送等待使能）

该位用于选择接收模式下的NTST.RDBFF0标志设置时序，也用于选择是否在第8个SCL时钟周期的下降沿保持SCLn线为低电平。

当ACKTWE=0时，SCLn线在第8个SCL时钟周期的下降沿不保持低电平，并且NTST.RDBFF0标志在第9个SCL时钟周期的上升沿设置为1。

当ACKTWE=1时，NTST.RDBFF0标志在第8个SCL时钟周期的上升沿设置为1，并且SCLn线在第8个SCL时钟周期的下降沿保持低电平。SCLn线的低保持通过向ACKCTL.ACKT位写入一个值来释放。

使用此设置接收数据后，SCLn线在发送确认位之前自动保持低电平。这使得处理能够根据接收数据发送ACK(ACKCTL.ACKT=0)或NACK(ACKCTL.ACKT=1)。

RWE bit (Receive Wait Enable)

This bit is used to control whether to hold the period between the ninth SCL clock cycle and the first SCL clock cycle low until the receive data buffer (NTDTBP0) is completely read each time single-byte data is received in receive mode.

When RWE = 0, the receive operation is continued without holding the period between the ninth and the first SCL clock cycle low. When both the ACKTWE and RWE bits = 0, continuous receive operation is enabled with the double buffer.

When RWE = 1, the SCLn line is held low from the falling edge of the ninth clock cycle until the NTDTBP0 value is read each time single-byte data is received.

This enables receive operation in byte units.

Note: When the value of the RWE bit is to be read, be sure to read the NTDTBP0 beforehand.

27.2.17 CNDCTL : Condition Control Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x140

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SPCND	SRCND	STCND
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCND	START (S) Condition Issuance 0: Does not request to issue a START condition. 1: Requests to issue a START condition.	R/W
1	SRCND	Repeated START (Sr) Condition Issuance 0: Does not request to issue a Repeated START condition. 1: Requests to issue a Repeated START condition.	R/W
2	SPCND	STOP (P) Condition Issuance 0: Does not request to issue a STOP condition. 1: Requests to issue a STOP condition.	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

STCND bit (START (S) Condition Issuance)

This bit is used to request transition to master mode and issuance of a START condition.

For details on the START condition issuance, see section 27.3.1.3.2. START Condition / Repeated START Condition / STOP Condition Issuing Function .

[Setting condition]

- When 1 is written to the STCND bit

[Clearing conditions]

- When 0 is written to the STCND bit
- When a START condition has been issued (A START condition is detected)
- When the BST.ALF (arbitration-lost) flag is set to 1

Note: Set the STCND bit to 1 (START condition issuance request) when the BCST.BFREF flag is set to 1 (bus free state).
Note that arbitration may be lost due to a START condition issuance error if the STCND bit is set to 1 (START condition issuance request) when the BFREF flag is set to 0 (bus busy state).

RWE位（接收等待使能）

该位用于控制在接收模式下每次接收单字节数据时，是否将第9个SCL时钟周期和第一个SCL时钟周期之间的周期保持为低电平，直到接收数据缓冲区(NTDTBP0)被完全读取。

当RWE=0时，继续接收操作，而不会将第9个和第一个SCL时钟周期之间的周期保持为低电平。当ACKTWE和RWE位都=0时，双缓冲器使能连续接收操作。

当RWE=1时，SCLn线从第9个时钟周期的下降沿保持低电平，直到每次接收到单字节数据时读取NTDTBP0值。

这启用了以字节为单位的接收操作。

Note: 当要读取RWE位的值时，请务必事先读取NTDTBP0。

27.2.17 CNDCTL:条件控制寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x140

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SPCND	SRCND	STCND
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCND	START(S)条件签发 0：不请求发出START条件。1：请求发出START条件。	R/W
1	SRCND	重复START(Sr)条件发布 0：不请求发出重复启动条件。1：请求发出重复启动条件。	R/W
2	SPCND	STOP(P)条件发布 0：不请求发出STOP条件。1：请求发出STOP条件。	R/W
31:3	—	这些位被读取为0。写入值应为0。	R/W

STCND位（START(S)条件发布）

该位用于请求转换到主机模式和发出START条件。

有关START条件发布的详细信息，请参阅第27.3.1.3.2节。START条件重复START条件STOP条件发布功能。

[Setting condition]

●向STCND位写入1时

[Clearing conditions]

●向STCND位写入0时

●发出START条件时（检测到START条件）

●当BST.ALF（仲裁失败）标志设置为1时

Note: 当BCST.BFREF标志设置为1（总线空闲状态）时，将STCND位设置为1（开始条件发出请求）。
请注意，如果在BFREF标志设置为0（总线繁忙状态）时将STCND位设置为1（发出START条件请求），则仲裁可能会由于START条件发出错误而丢失。

SRCND bit (Repeated START (Sr) Condition Issuance)

This bit is used to request that a Repeated START condition be issued in master mode.

When this bit is set to 1 to request to issue a Repeated START condition, a Repeated START condition is issued when the BFREF flag is set to 0 (bus busy state) and the PRSST.CRMS bit is set to 1 (master mode).

For details on the Repeated START condition issuance, see section 27.3.1.3.2. START Condition / Repeated START Condition / STOP Condition Issuing Function .

[Setting condition]

- When 1 is written to the SRCND bit with the BCST.BFREF flag set to 0

[Clearing conditions]

- When 0 is written to the SRCND bit
- When a Repeated START condition has been issued (A Repeated START condition is detected)
- When the BST.ALF (arbitration-lost) flag is set to 1

Note: Do not set the SRCND bit to 1 while issuing a STOP condition.

Note: If 1 (requests to issue a Repeated START condition) is written to the SRCND bit in slave mode, the Repeated START condition is not issued but the SRCND bit remains set to 1.

If the operating mode changes to master mode with the bit not being cleared, note that the Repeated START condition may be issued.

SPCND bit (STOP (P) Condition Issuance)

This bit is used to request that a STOP condition be issued in master mode.

When this bit is set to 1 to request to issue a STOP condition, a STOP condition is issued when the BCST.BFREF flag is set to 0 (bus busy state) and the PRSST.CRMS bit is set to 1 (master mode).

For details on the STOP condition issuance, see section 27.3.1.3.2. START Condition / Repeated START Condition / STOP Condition Issuing Function .

[Setting condition]

- When 1 is written to the SPCND bit with the BCST.BFREF flag set to 0 and the PRSST.CRMS bit set to 1

[Clearing conditions]

- When 0 is written to the SPCND bit
- When a STOP condition has been issued (A STOP condition is detected)
- When the BST.ALF (arbitration-lost) flag is set to 1
- When a START condition and a Repeated START condition are detected

Note: Writing to the SPCND bit is not possible while the setting of the BCST.BFREF flag = 1 (bus free state).

Note: Do not set the SPCND bit to 1 while a Repeated START condition is being issued.

27.2.18 NTDTBP0/NTDTBP0_BY : Normal Transfer Data Buffer Port Register 0

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x158

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SRCND位（重复START(Sr)条件发布）

该位用于请求在主机模式下发出重复启动条件。

当该位设置为1以请求发出重复START条件时，发出重复START条件时BFREF标志设置为0（总线繁忙状态）并且PRSST.CRMS位设置为1（主模式）。

有关重复启动条件发布的详细信息，请参阅第27.3.1.3.2节。START条件重复START条件停止条件发布功能。

[Setting condition]

●将1写入SRCND位且BCST.BFREF标志设置为0时

[Clearing conditions]

●向SRCND位写入0时

●发出重复启动条件时（检测到重复启动条件）

●当BST.ALF（仲裁失败）标志设置为1时

Note: 发出STOP条件时不要将SRCND位设置为1。

Note: 如果在从模式下将1（请求发出重复启动条件）写入SRCND位，则重复未发出START条件，但SRCND位保持设置为1。

如果操作模式更改为主机模式且该位未被清除，请注意可能会发出重复启动条件。

SPCND位（STOP(P)条件发布）

该位用于请求在主机模式下发出STOP条件。

当该位设置为1以请求发出STOP条件时，当BCST.BFREF标志设置为0（总线繁忙状态）且PRSST.CRMS位设置为1（主机模式）时，将发出STOP条件。

有关STOP条件发布的详细信息，请参阅第27.3.1.3.2节。START条件重复START条件STOP条件发布函数。

[Setting condition]

●当1写入SPCND位且BCST.BFREF标志设置为0且PRSST.CRMS位设置为1时

[Clearing conditions]

●向SPCND位写入0时

●发出STOP条件时（检测到STOP条件）

●当BST.ALF（仲裁失败）标志设置为1时

●检测到START条件和重复START条件时

Note: 当设置BCST.BFREF标志=1（总线空闲状态）时，无法写入SPCND位。

Note: 发出重复启动条件时不要将SPCND位设置为1。

27.2.18 NTDTBP0NTDTBP0_BY:正常传输数据缓冲区端口寄存器0

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x158

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Normal Transfer Data Buffer Port NTDTBP0 is a 32-bit read/write register. NTDTBP0_BY (NTDTBP0[7:0]) is a 8-bit read/write register.	R/W

32-bit mailbox register NTDTBP0 is a 32-bit bi-directional data transfer register which is used both to read from the Normal Receive Data Buffer, and to write to the Normal Transmit Data Buffer.

In other words, the Normal Receive Data Buffer and the Normal Transmit Data Buffer have the same offset, forming a single bidirectional port for transmitting or receiving IIC data.

Read Operations:

When 1 byte of data has been received, the received data is transferred from the internal shift register to NTDTBP0 to enable the next data to be received. The double-buffer structure of the internal shift register and NTDTBP0 allows continuous receive operation if the received data has been read from NTDTBP0 while the internal shift register is receiving data. Read data from NTDTBP0 once when a receive data full interrupt (IICn_RX) request is generated. If NTDTBP0 receives the next receive data before the current data is read from NTDTBP0 (while the RDBFF0 flag in NTST is 1), this module automatically holds the SCL clock low one cycle before the RDBFF0 flag is set to 1 next. The lower 8 bits of the read 32-bit data are valid as received data.

Write Operations:

When NTDTBP0 detects a space in the internal shift register, it transfers the transmit data that has been written to NTDTBP0 to the internal shift register and starts transmitting data in transmit mode. The double-buffer structure of NTDTBP0 and the internal shift register allows continuous transmit operation if the next transmit data has been written to NTDTBP0 while the the internal shift register data is being transmitted. Write transmit data to NTDTBP0 once when a transmit data empty interrupt (IICn_TX) request is generated. The lower 8 bits of the written 32-bit data are valid as transmission data.

27.2.19 BST : Bus Status Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x1D0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	WUCNDDF	—	—	—	TODF	—	—	—	ALF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TENDF	—	—	—	NACKDF	—	—	SPCNDDF	STCNDDF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCNDDF	START Condition Detection Flag 0: START condition is not detected. 1: START condition is detected.	R/W*1
1	SPCNDDF	STOP Condition Detection Flag 0: STOP condition is not detected. 1: STOP condition is detected.	R/W*1
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	NACKDF	NACK Detection Flag 0: NACK is not detected. 1: NACK is detected.	R/W*1
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
31:0	n/a	正常传输数据缓冲端口 NTDTBP0是一个32位读写寄存器。 NTDTBP0_BY(NTDTBP0[7:0])是一个8位读写寄存器。	R/W

32位邮箱寄存器NTDTBP0是一个32位双向数据传输寄存器，用于读取正常接收数据缓冲区和写入正常发送数据缓冲区。

换言之，NormalReceiveDataBuffer和NormalTransmitDataBuffer具有相同的偏移量，形成一个双向端口，用于发送或接收IIC数据。

Read Operations:

当接收到1个字节的数据时，接收到的数据会从内部移位寄存器传送到NTDTBP0，以便接收下一个数据。内部移位寄存器和NTDTBP0的双缓冲结构允许在内部移位寄存器接收数据时从NTDTBP0读取接收到的数据时连续接收操作。当产生接收数据完全中断(IICn_RX)请求时，从NTDTBP0读取数据一次。如果NTDTBP0在从NTDTBP0读取当前数据之前接收到下一个接收数据（而NTST中的RDBFF0标志为1），则该模块在RDBFF0标志设置为1之前自动将SCL时钟保持低一个周期。读取的32位数据的低8位作为接收数据有效。

Write Operations:

当NTDTBP0检测到内部移位寄存器中有一个空间时，它会传输已写入的发送数据
NTDTBP0到内部移位寄存器并在发送模式下开始发送数据。双缓冲结构
如果下一个发送数据已写入NTDTBP0和内部移位寄存器，则允许连续发送操作
NTDTBP0，而内部移位寄存器数据正在传输。当产生发送数据空中断(IICn_TX)请求时，将发送数据写入NTDTBP0。写入的32位数据的低8位作为传输数据有效。

27.2.19 BST:总线状态寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x1D0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	WUCNDDF	—	—	—	TODF	—	—	—	ALF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TENDF	—	—	—	NACKDF	—	—	SPCNDDF	STCNDDF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCNDDF	开始条件检测标志 0：未检测到启动条件。1：检测到启动条件。	R/W*1
1	SPCNDDF	停止条件检测标志 0：未检测到STOP条件。1：检测到停止条件。	R/W*1
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	NACKDF	NACK检测标志 0：未检测到NACK。1：检测到NACK。	R/W*1
7:5	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
8	TENDF	Transmit End Flag 0: Data is being transmitted. 1: Data has been transmitted.	R/W*1
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	ALF	Arbitration Lost Flag 0: Arbitration is not lost 1: Arbitration is lost.	R/W*1
19:17	—	These bits are read as 0. The write value should be 0.	R/W
20	TODF	Timeout Detection Flag 0: Timeout is not detected. 1: Timeout is detected.	R/W*1
23:21	—	These bits are read as 0. The write value should be 0.	R/W
24	WUCNDDF*2	Wake-Up Condition Detection Flag 0: Wake-Up is not detected. 1: Wake-Up is detected.	R/W*1
31:25	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Clearing (to 0) condition : Writing 0 after 1 is read.
Note 2. This bit is available only IIC0. This bit are read as 0 and the write value should be 0 in IIC1.

STCNDDF bit (START Condition Detection Flag)

[Setting condition]

- All of the followings are satisfied:
  1. The BSTE.STCNDDE bit = 1.
  2. When a START condition (or a Repeated START condition) is detected.

[Clearing condition]

- When 0 is written to the STCNDDF flag after reading STCNDDF flag = 1.
- When a STOP condition is detected.

SPCNDDF bit (STOP Condition Detection Flag)

[Setting condition]

- All of the followings are satisfied:
  1. The BSTE.SPCNDDE bit = 1.
  2. When a STOP condition is detected.

[Clearing condition]

- When 0 is written to the SPCNDDF flag after reading SPCNDDF flag = 1.

NACKDF bit (NACK Detection Flag)

[Setting condition]

- All of the followings are satisfied:
  1. The BSTE.NACKDE bit = 1 (Enables NACK detection interrupt status logging).
  2. When acknowledge is not received (NACK is received) from the receive device in transmit mode.

[Clearing condition]

- When 0 is written to the NACKDF flag after reading NACKDF flag = 1.

TENDF bit (Transmit End Flag)

[Setting condition]

- All of the followings are satisfied:

Bit	Symbol	Function	R/W
8	TENDF	发送结束标志 0：正在传输数据。1：数据已发送。	R/W*1
15:9	—	这些位被读取为0。写入值应为0。	R/W
16	ALF	仲裁丢失标志 0：仲裁不丢失1：仲裁丢失。	R/W*1
19:17	—	这些位被读取为0。写入值应为0。	R/W
20	TODF	超时检测标志 0：未检测到超时。1：检测到超时。	R/W*1
23:21	—	这些位被读取为0。写入值应为0。	R/W
24	WUCNDDF*2	唤醒条件检测标志 0：未检测到唤醒。1：检测到唤醒。	R/W*1
31:25	—	这些位被读取为0。写入值应为0。	R/W

注1.清零（清零）条件：读取1后写入0。
注2.该位仅适用于IIC0。该位读为0，在IIC1中写入值应为0。

STCNDDF位（开始条件检测标志）

[Setting condition]

●满足以下所有条件：

1.BSTE.STCNDDE位=1。

2.检测到启动条件（或重复启动条件）时。

[Clearing condition]

●读取STCNDDF标志=1后向STCNDDF标志写入0时。

●检测到停止条件时。

SPCNDF位（停止条件检测标志）

[Setting condition]

●满足以下所有条件：

1.BSTE.SPCNDE位=1。

2.检测到停止条件时。

[Clearing condition]

●当读取SPCNDDF标志=1后向SPCNDDF标志写入0时。

NACKDF位（NACK检测标志）

[Setting condition]

●满足以下所有条件：

1.BSTE.NACKDE位=1（启用NACK检测中断状态记录）。

2.当在发送模式下没有收到来自接收设备的确认（收到NACK）时。

[Clearing condition]

●读取NACKDF标志=1后向NACKDF标志写入0时。

TENDF位（发送结束标志）

[Setting condition]

●满足以下所有条件：

1. The BSTE.TENDE bit = 1 (Enables Transmit End Interrupt Status logging).
2. At the rising edge of the ninth SCL clock cycle while the NTST.TDBEF0 flag = 1. Excluding when sending an address.

[Clearing condition]

- When 0 is written to the TENDF flag after reading TENDF flag = 1.
- When data is written to the NTDTBP0 register.
- When a STOP condition is detected.

ALF bit (Arbitration Lost Flag)

[Setting condition]

When master arbitration-lost detection is enabled: BSTE.ALE bit = 1, BFCTL.MALE = 1.

- When the internal SDA output state does not match the SDA line level at the rising edge of SCL clock except for the ACK period during data (including slave address) transmission in master transmit mode (when the SDA line is driven low while the internal SDA output is at a high level (the SDA pin is in the highimpedance state)).
- All of the followings are satisfied.
  1. When the START condition is detected while the CNDCTL.STCND bit = 1.
  2. When the internal SDA output state does not match the SDA line level.
- When the CNDCTL.STCND bit is set to 1 (START condition issuance request) while the BCST.BFREF flag = 0.

When NACK arbitration-lost detection is enabled: BSTE.ALE bit = 1, BFCTL.NALE = 1.

- When the internal SDA output state does not match the SDA line level at the rising edge of SCL clock in the ACK period during NACK transmission in receive mode.

When slave arbitration-lost detection is enabled: BSTE.ALE bit = 1, BFCTL.SALE = 1.

- When the internal SDA output state does not match the SDA line level at the rising edge of SCL clock except for the ACK period during data transmission in slave transmit mode.

[Clearing condition]

- When 0 is written to the ALF flag after reading ALF flag = 1.

TODF bit (Timeout Detection Flag)

[Setting condition]

- All of the followings are satisfied.
  1. The BSTE.TODE bit = 1 (Enables Timeout Detection Interrupt Status logging).
  2. When the master mode or the received slave address matches the slave address n in Slave mode.
  3. When the SCL line state remains unchanged for the period specified by TMOCTL register.

[Clearing condition]

- When 0 is written to the TODF flag after reading TODF flag = 1.

WUCNDDF bit (Wake-Up Condition Detection Flag)

[Setting condition]

- When PCLKA and IICCLK are supplied after all of the followings are satisfied.
  1. The WUCTL.WUFE bit = 1 (Wake-up function is enabled).
  2. The BSTE.WUCNDDE bit = 1 (Enables Wake-up Condition Detection Status logging).
  3. The WUST.WUASYNF flag = 1.
  4. When the address received in slave mode matches the address of slave enabled in the SVCTL.SVAEy bit (except for the Device-ID address).

1.BSTE.TENDE位=1（启用发送结束中断状态记录）。

2.在第9个SCL时钟周期的上升沿且NTST.TDBEF0标志=1。发送地址时除外。

[Clearing condition]

●读取TENDF标志=1后向TENDF标志写入0时。

●当数据写入NTDTBP0寄存器时。

●检测到停止条件时。

ALF位（仲裁丢失标志）

[Setting condition]

当启用主机仲裁丢失检测时：BSTE.ALE位=1，BFCTL.MALE=1。

●当内部SDA输出状态在SCL时钟的上升沿与SDA线电平不匹配时，在主机发送模式下的数据（包括从机地址）传输期间（当SDA线被驱动为低电平而内部SDA输出为高电平（SDA引脚处于高阻状态））。

●满足以下所有条件。

1.当CNDCTL.STCND位=1时检测到START条件。

2.当内部SDA输出状态与SDA线电平不匹配时。

●当BCST.BFREF标志=0时CNDCTL.STCND位设置为1（开始条件发出请求）。

当启用NACK仲裁丢失检测时：BSTE.ALE位=1，BFCTL.NALE=1。

●在接收模式下的NACK传输期间，当内部SDA输出状态在ACK周期的SCL时钟上升沿与SDA线电平不匹配时。

当启用从设备仲裁丢失检测时：BSTE.ALE位=1，BFCTL.SALE=1。

●在从机传输模式下，除了ACK周期外，当内部SDA输出状态在SCL时钟的上升沿与SDA线电平不匹配时。

[Clearing condition]

●读取ALF标志=1后向ALF标志写入0时。

TODF位（超时检测标志）

[Setting condition]

●满足以下所有条件。

1.BSTE.TODE位=1（启用超时检测中断状态记录）。

2.当主机模式或接收到的从机地址与从机模式下的从机地址n匹配时。

3.当SCL线状态在TMOCTL寄存器指定的时间段内保持不变时。

[Clearing condition]

●读取TODF标志=1后向TODF标志写入0时。

WUCNDDF位（唤醒条件检测标志）

[Setting condition]

●在满足以下所有条件后提供PCLKA和IICCLK时。

1.WUCTL.WUFE位=1（启用唤醒功能）。

2.BSTE.WUCNDDE位=1（启用唤醒条件检测状态记录）。

3.WUST.WUASYNF标志=1。

4.当从机模式接收到的地址与SVCTL.SVAEy位中使能的从机地址匹配时（Device-ID地址除外）。

[Clearing condition]

- When 0 is written to the WUCNDDF flag after reading WUCNDDF flag = 1 while the WUST.WUASYNF flag = 0.

27.2.20 BSTE : Bus Status Enable Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x1D4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—		WUCNDDE	—	—	—	TODE	—	—	—	ALE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TENDE	—	—	—	NACKDE	—	—	SPCNDDE	STCNDDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCNDDE	START Condition Detection Enable 0: Disables START condition Detection Interrupt Status logging. 1: Enables START condition Detection Interrupt Status logging.	R/W
1	SPCNDDE	STOP Condition Detection Enable 0: Disables STOP condition Detection Interrupt Status logging. 1: Enables STOP condition Detection Interrupt Status logging.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	NACKDE	NACK Detection Enable 0: Disables NACK Detection Interrupt Status logging. 1: Enables NACK Detection Interrupt Status logging.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
8	TENDE	Transmit End Enable 0: Disables Transmit End Interrupt Status logging. 1: Enables Transmit End Interrupt Status logging.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	ALE	Arbitration Lost Enable 0: Disables Arbitration Lost Interrupt Status logging. 1: Enables Arbitration Lost Interrupt Status logging.	R/W
19:17	—	These bits are read as 0. The write value should be 0.	R/W
20	TODE	Timeout Detection Enable 0: Disables Timeout Detection Interrupt Status logging. 1: Enables Timeout Detection Interrupt Status logging.	R/W
23:21	—	These bits are read as 0. The write value should be 0.	R/W
24	WUCNDDE*1	Wake-up Condition Detection Enable 0: Disables Wake-up Condition Detection Status logging. 1: Enables Wake-up Condition Detection Status logging.	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is available only IIC0. This bit are read as 0 and the write value should be 0 in IIC1.

STCNDDE bit (START Condition Detection Enable)

When this bit is 1, operation of BST.STCNDDF is enabled. For the setting conditions and clearing conditions of the BST.STCNDDF flag, see the details of BST.STCNDDF.

SPCNDDE bit (STOP Condition Detection Enable)

When this bit is 1, operation of BST.SPCNDDF is enabled. For the setting conditions and clearing conditions of the BST.SPCNDDF flag, see the details of BST.SPCNDDF.

[Clearing condition]

●当WUST.WUASYNF标志=0时读取WUCNDDF标志=1后将0写入WUCNDDF标志。

27.2.20 BSTE：总线状态使能寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x1D4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—		WUCNDDE	—	—	—	TODE	—	—	—	ALE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TENDE	—	—	—	纳克德	—	—	SPCNDDE	STCNDDE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCNDDE	启动条件检测启用 0：禁用启动条件检测中断状态记录。1：启用启动条件检测中断状态记录。	R/W
1	SPCNDDE	停止条件检测启用 0：禁用STOP条件检测中断状态记录。1：启用STOP条件检测中断状态记录。	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	NACKDE	NACK检测使能 0：禁用NACK检测中断状态记录。1：启用NACK检测中断状态记录。	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
8	TENDE	发送结束使能 0：禁用发送结束中断状态记录。1：启用发送结束中断状态记录。	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
16	ALE	仲裁丢失启用 0：禁用仲裁丢失中断状态记录。1：启用仲裁丢失中断状态记录。	R/W
19:17	—	这些位被读取为0。写入值应为0。	R/W
20	TODE	超时检测启用 0：禁用超时检测中断状态记录。1：启用超时检测中断状态记录。	R/W
23:21	—	这些位被读取为0。写入值应为0。	R/W
24	WUCNDDE*1	唤醒条件检测启用 0：禁用唤醒条件检测状态记录。1：启用唤醒条件检测状态记录。	R/W
31:25	—	这些位被读取为0。写入值应为0。	R/W

注1.该位仅适用于IIC0。该位读为0，在IIC1中写入值应为0。

STCNDDE位（启动条件检测使能）

当该位为1时，启用BST.STCNDDF的操作。对于设置条件和清除条件BST.STCNDDF标志，详见BST.STCNDDF。

SPCNDE位（停止条件检测使能）

当该位为1时，启用BST.SPCNDDF的操作。对于设置条件和清除条件BST.SPNCDDF标志，详见BST.SPNCDDF。

NACKDE bit (NACK Detection Enable)

When this bit is 1, the operation of BST.NACKDF is enabled. This bit is used to specify whether to continue or discontinue the transfer operation when NACK is received from the slave device in transmit mode. Normally, set this bit to 1. For the setting conditions and clearing conditions of the BST.NACKDF flag, see the details of BST.NACKDF.

TENDE bit (Transmit End Enable)

When this bit is 1, the operation of BST.TENDF is enabled. For the setting conditions and clearing conditions of the BST.TENDF flag, see the details of BST.TENDF.

ALE bit (Arbitration Lost Enable)

When this bit is 1, the operation of BST.ALF is enabled. For the setting conditions and clearing conditions of the BST.ALF flag, see the details of BST.ALF.

TODE bit (Timeout Detection Enable)

When this bit is 1, the operation of BST.TODF is enabled. For the setting conditions and clearing conditions of the BST.TODF flag, see the details of BST.TODF.

WUCNDDE bit (Wake-up Condition Detection Enable)

When this bit is 1, the operation of BST.WUCNDDF is enabled. For the setting conditions and clearing conditions of the BST.WUCNDDF flag, see the details of BST.WUCNDDF.

27.2.21 BIE : Bus Interrupt Enable Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x1D8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	WUCNDDIE	—	—	—	TODIE	—	—	—	ALIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TENDIE	—	—	—	NACKDIE	—	—	SPCNDDIE	STCNDDIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCNDDIE	START Condition Detection Interrupt Enable 0: Disables START condition Detection Interrupt Signal. 1: Enables START condition Detection Interrupt Signal.	R/W
1	SPCNDDIE	STOP Condition Detection Interrupt Enable 0: Disables STOP condition Detection Interrupt Signal. 1: Enables STOP condition Detection Interrupt Signal.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	NACKDIE	NACK Detection Interrupt Enable 0: Disables NACK Detection Interrupt Signal. 1: Enables NACK Detection Interrupt Signal.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
8	TENDIE	Transmit End Interrupt Enable 0: Disables Transmit End Interrupt Signal. 1: Enables Transmit End Interrupt Signal.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	ALIE	Arbitration Lost Interrupt Enable 0: Disables Arbitration Lost Interrupt Signal. 1: Enables Arbitration Lost Interrupt Signal.	R/W

NACKDE位（NACK检测使能）

当该位为1时，启用BST.NACKDF的操作。该位用于指定在发送模式下从从设备接收到NACK时是继续还是停止传输操作。通常将此位设置为1。关于BST.NACKDF标志的设置条件和清除条件，请参见BST.NACKDF的详细信息。

TENDE位（发送结束使能）

当该位为1时，启用BST.TENDF的操作。对于设置条件和清除条件BST.TENDF标志，详见BST.TENDF。

ALE位（仲裁丢失启用）

当该位为1时，启用BST.ALF操作。关于BST.ALF标志的设置条件和清除条件，请参见BST.ALF的详细信息。

TODE位（超时检测使能）

当该位为1时，启用BST.TODF的操作。对于设置条件和清除条件BST.TODF标志，详见BST.TODF。

WUCNDDE位（唤醒条件检测启用）

当该位为1时，启用BST.WUCNDDF的操作。对于设置条件和清除条件BST.WUCNDDF标志，详见BST.WUCNDDF。

27.2.21 BIE:总线中断使能寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x1D8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	WUCNDDIE	—	—	—	TODIE	—	—	—	ALIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TENDIE	—	—	—	后模	—	—	SPCNDDIE	STCNDDIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCNDDIE	启动条件检测中断使能 0：禁止启动条件检测中断信号。1：使能启动条件检测中断信号。	R/W
1	SPCNDDIE	停止条件检测中断使能 0：禁止停止条件检测中断信号。1：使能停止条件检测中断信号。	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	NACKDIE	NACK检测中断使能 0：禁止NACK检测中断信号。1：使能NACK检测中断信号。	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
8	TENDIE	发送结束中断使能 0：禁止发送结束中断信号。1：使能发送结束中断信号。	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
16	ALIE	仲裁丢失中断使能 0：禁用仲裁丢失中断信号。1：使能仲裁丢失中断信号。	R/W

Bit	Symbol	Function	R/W
19:17	—	These bits are read as 0. The write value should be 0.	R/W
20	TODIE	Timeout Detection Interrupt Enable 0: Disables Timeout Detection Interrupt Signal. 1: Enables Timeout Detection Interrupt Signal.	R/W
23:21	—	These bits are read as 0. The write value should be 0.	R/W
24	WUCNDDIE*1	Wake-Up Condition Detection Interrupt Enable 0: Disables Wake-Up Condition Detection Interrupt Signal. 1: Enables Wake-Up Condition Detection Interrupt Signal.	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is available only IIC0. This bit are read as 0 and the write value should be 0 in IIC1.

The BIE register enables signaling of outstanding bus interrupts received by IIC.

STCNDDIE bit (START Condition Detection Interrupt Enable)

This bit enables or disables the START Condition Detection interrupt requests when the BST.STCNDDF flag is set to 1.

SPCNDDIE bit (STOP Condition Detection Interrupt Enable)

This bit enables or disables the STOP Condition Detection interrupt requests when the BST.SPCNDDF flag is set to 1.

NACKDIE bit (NACK Detection Interrupt Enable)

This bit enables or disables the NACK Detection interrupt requests when the BST.NACKDF flag is set to 1.

TENDIE bit (Transmit End Interrupt Enable)

This bit enables or disables the Transmit End interrupt (IICn_TEND) requests when the BST.TENDF flag is set to 1.

ALIE bit (Arbitration Lost Interrupt Enable)

This bit enables or disables the Arbitration Llost interrupt requests when the BST.ALF flag is set to 1.

TODIE bit (Timeout Detection Interrupt Enable)

This bit enables or disables the Timeout Detection interrupt requests when the BST.TODF flag is set to 1.

WUCNDDIE bit (Wake-Up Condition Detection Interrupt Enable)

This bit enables or disables the Wake-up Condition Detection interrupt (IIC0_WU) requests when the BST.WUCNDDF flag is set to 1.

27.2.22 BSTFC : Bus Status Force Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x1DC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	WUCNDDFC	—	—	—	TODFC	—	—	—	ALFC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TENDFC	—	—	—	NACKDFC	—	—	SPCNDDFC	STCNDDFC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCNDDFC	START condition Detection Force 0: Not Force START condition Detection Interrupt for software testing. 1: Force START condition Detection Interrupt for software testing.	W

Bit	Symbol	Function	R/W
19:17	—	这些位被读取为0。写入值应为0。	R/W
20	TODIE	超时检测中断使能 0：禁用超时检测中断信号。1：使能超时检测中断信号。	R/W
23:21	—	这些位被读取为0。写入值应为0。	R/W
24	WUCNDDIE*1	唤醒条件检测中断使能 0：禁用唤醒条件检测中断信号。1：使能唤醒条件检测中断信号。	R/W
31:25	—	这些位被读取为0。写入值应为0。	R/W

注1.该位仅适用于IIC0。该位读为0，在IIC1中写入值应为0。

BIE寄存器启用IIC接收到的未完成总线中断的信号。

STCNDDIE位（启动条件检测中断允许）

当BST.STCNDDF标志设置为1时，该位启用或禁用START条件检测中断请求。

SPCNDDIE位（停止条件检测中断使能）

当BST.SPCNDF标志设置为1时，该位启用或禁用STOP条件检测中断请求。

NACKDIE位（NACK检测中断使能）

当BST.NACKDF标志设置为1时，该位启用或禁用NACK检测中断请求。

TENDIE位（发送结束中断允许）

当BST.TENDF标志设置为1时，该位启用或禁用发送结束中断(IICn_TEND)请求。

ALIE位（仲裁丢失中断使能）

当BST.ALF标志设置为1时，该位启用或禁用仲裁丢失中断请求。

TODIE位（超时检测中断使能）

当BST.TODF标志设置为1时，该位启用或禁用超时检测中断请求。

WUCNDDIE位（唤醒条件检测中断使能）

当BST.WUCNDDF标志设置为1时，该位启用或禁用唤醒条件检测中断(IIC0_WU)请求。

27.2.22 BSTFC:总线状态强制寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x1DC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	WUCNDDFC	—	—	—	TODFC	—	—	—	ALFC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TENDFC	—	—	—	NACKDFC	—	—	SPCNDDFC	STCNDDFC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCNDDFC	启动条件检测力 0：不强制启动条件检测中断用于软件测试。1：强制启动条件检测中断，用于软件测试。	W

Bit	Symbol	Function	R/W
1	SPCNDDFC	STOP condition Detection Force 0: Not Force STOP condition Detection Interrupt for software testing. 1: Force STOP condition Detection Interrupt for software testing.	W
3:2	—	These bits are read as 0.	R
4	NACKDFC	NACK Detection Force 0: Not Force NACK Detection Interrupt for software testing. 1: Force NACK Detection Interrupt for software testing.	W
7:5	—	These bits are read as 0.	R
8	TENDFC*1	Transmit End Force 0: Not Force Transmit End Interrupt for software testing. 1: Force Transmit End Interrupt for software testing.	W
15:9	—	These bits are read as 0.	R
16	ALFC	Arbitration Lost Force 0: Not Force Arbitration Lost Interrupt for software testing. 1: Force Arbitration Lost Interrupt for software testing.	W
19:17	—	These bits are read as 0.	R
20	TODFC	Timeout Detection Force 0: Not Force Timeout Detection Interrupt for software testing. 1: Force Timeout Detection Interrupt for software testing.	W
23:21	—	These bits are read as 0.	R
24	WUCNDDFC*2	Wake-Up Condition Detection Force 0: Not Force Wake-Up Condition Detection Interrupt for software testing. 1: Force Wake-Up Condition Detection Interrupt for software testing.	W
31:25	—	These bits are read as 0.	R

Note 1. TENDFC does not work unless TDBEF0 = 1.
Note 2. This bit is available only IIC0. This bit are read as 0 and the write value should be 0 in IIC1.

27.2.23 NTST : Normal Transfer Status Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)
Offset address: 0x1E0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDBFF0	TDBEF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEF0	Normal Transmit Data Buffer Empty Flag 0 0: Normal Transmit Data Buffer 0 contains transmit data. 1: Normal Transmit Data Buffer 0 contains no transmit data.	R/W*1
1	RDBFF0	Normal Receive Data Buffer Full Flag 0 0: Normal Receive Data Buffer0 contains no receive data. 1: Normal Receive Data Buffer0 contains receive data.	R/W*1
31:2	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Clearing (to 0) condition : Writing 0 after the 1 state is read.

TDBEF0 bit (Normal Transmit Data Buffer Empty Flag 0)

[Setting condition]

Bit	Symbol	Function	R/W
1	SPCNDDFC	停止条件检测力 0：不强制停止条件检测中断，用于软件测试。1：强制停止条件检测中断，用于软件测试。	W
3:2	—	这些位读为0。	R
4	NACKDFC	NACK检测力 0：软件测试不强制NACK检测中断。1：强制NACK检测中断用于软件测试。	W
7:5	—	这些位读为0。	R
8	TENDFC*1	传输端力 0：软件测试不强制发送结束中断。1：强制发送结束中断以进行软件测试。	W
15:9	—	这些位读为0。	R
16	ALFC	仲裁失败的力量 0：软件测试不强制仲裁丢失中断。1：强制仲裁丢失中断以进行软件测试。	W
19:17	—	这些位读为0。	R
20	TODFC	超时检测力 0：软件测试不强制超时检测中断。1：强制软件测试超时检测中断。	W
23:21	—	这些位读为0。	R
24	WUCNDDFC*2	唤醒条件检测力 0：不强制软件测试的唤醒条件检测中断。1：强制唤醒条件检测中断用于软件测试。	W
31:25	—	这些位读为0。	R

注1.TENDFC不工作，除非TDBEF0=1。
注2.该位仅适用于IIC0。该位读为0，在IIC1中写入值应为0。

27.2.23 NTST:正常传输状态寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)
Offset address: 0x1E0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDBFF0	TDBEF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEF0	正常发送数据缓冲区空标志0 0：正常发送数据缓冲区0包含发送数据。1：正常发送数据缓冲区0不包含发送数据。	R/W*1
1	RDBFF0	正常接收数据缓冲区满标志0 0：正常接收数据缓冲区0不包含接收数据。1：正常接收数据缓冲区0包含接收数据。	R/W*1
31:2	—	这些位被读取为0。写入值应为0。	R/W

注1.清零（到0）条件：读取1状态后写入0。

TDBEF0位（正常发送数据缓冲区空标志0）

[Setting condition]

The following condition 1 is satisfied and any of the following conditions 2 to 4 are satisfied:

1. The NTSTE.TDBEE0 bit = 1 (enables Tx0 Data Buffer Empty Interrupt Status logging).
2. When data has been transferred from the Normal Transmit Data Buffer 0 to the Shift Register and the Normal Transmit Data Buffer 0 becomes empty*1.
3. When the PRSST.TRMD bit is set to 1.
4. When the received slave address matches while the TRMD bit = 1.

[Clearing condition]

- When data is written to NTDTBP0.
- When the TRMD bit in PRSST is set to 0.

Note 1. When the BST.NACKDF flag is set to 1 while the BSTE.NACKDE bit = 1, IIC aborts data transmission/reception. If the TDBEF0 flag = 0 (next transmit data has been written), data is transferred to the Shift Register and the Normal Transmit Data Buffer 0 register becomes empty at the rising edge of the 9th clock cycle, but the TDBEF0 flag is not set to 1.

RDBFF0 bit (Normal Receive Data Buffer Full Flag 0)

[Setting condition]

The following condition 1 is satisfied and any of the following condition 2 or 3 is satisfied:

1. The NTSTE.RDBFE0 bit = 1 (enables Rx0 Data Buffer Full Interrupt Status logging).
2. When receive data is transferred from Shift Register to Normal Receive Data Buffer 0.
   The RDBFF0 flag is set to 1 on the rising edge of the 8th or 9th SCL clock cycle (selected in the ACKTWE bit in SCSTRCTL).
3. When the received slave address matches after a START (or Repeated START) condition is detected with the TRMD bit in PRSST set to 0.

[Clearing condition]

- When data is read from NTDTBP0.

27.2.24 NTSTE : Normal Transfer Status Enable Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x1E4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDBFE0	TDBEE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEE0	Normal Transmit Data Buffer Empty Enable 0 0: Disables Tx0 Data Buffer Empty Interrupt Status logging. 1: Enables Tx0 Data Buffer Empty Interrupt Status logging.	R/W
1	RDBFE0	Normal Receive Data Buffer Full Enable 0 0: Disables Rx0 Data Buffer Full Interrupt Status logging. 1: Enables Rx0 Data Buffer Full Interrupt Status logging.	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

满足以下条件1并且满足以下条件2至4中的任何一个：

1.NTSTE.TDBEE0位=1（启用Tx0数据缓冲区空中断状态记录）。

2.当数据已从正常发送数据缓冲区0传输到移位寄存器并且正常发送数据缓冲区0变为空*1时。

3.当PRSST.TRMD位设置为1时。

4.当TRMD位=1时接收到的从机地址匹配。

[Clearing condition]

●当数据写入NTDTBP0时。

●PRSST中的TRMD位设置为0时。

注1.当BST.NACKDF标志设置为1且BSTE.NACKDE位=1时，IIC中止数据发送接收。如果TDBEF0标志=0（下一个发送数据已写入），数据被传送到移位寄存器，并且正常发送数据缓冲器0寄存器在第9个时钟周期的上升沿变为空，但TDBEF0标志未设置为1.

RDBFF0位（正常接收数据缓冲区满标志0）

[Setting condition]

满足以下条件1并且满足以下条件2或3中的任何一个：

1.NTSTE.RDBFE0位=1（启用Rx0数据缓冲区满中断状态记录）。

2.当接收数据从移位寄存器传送到正常接收数据缓冲器0时。
RDBFF0标志在第8个或第9个SCL时钟周期的上升沿设置为1（在ACKTWE位中选择）
SCSTRCTL).

3.当在PRSST中的TRMD位设置为0的情况下检测到START（或重复START）条件后接收到的从机地址匹配时。

[Clearing condition]

●从NTDTBP0读取数据时。

27.2.24 NTSTE:正常传输状态使能寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x1E4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDBFE0	TDBEE0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEE0	正常发送数据缓冲区空使能0 0：禁用Tx0数据缓冲区空中断状态记录。1：启用Tx0数据缓冲区空中断状态记录。	R/W
1	RDBFE0	正常接收数据缓冲器满使能0 0：禁用Rx0数据缓冲区满中断状态记录。1：启用Rx0数据缓冲区满中断状态记录。	R/W
31:2	—	这些位被读取为0。写入值应为0。	R/W

TDBEE0 bit (Normal Transmit Data Buffer Empty Enable 0)

When this bit is 1, the operation of NTST.TDBEF0 is enabled.

For the setting conditions and clearing conditions of the NTST.TDBEF0 flag, see the details of NTST.TDBEF0.

RDBFE0 bit (Normal Receive Data Buffer Full Enable 0)

When this bit is 1, the operation of NTST.RDBFF0 is enabled.

For the setting conditions and clearing conditions of the NTST.RDBFF0 flag, see the details of NTST.RDBFF0.

27.2.25 NTIE : Normal Transfer Interrupt Enable Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x1E8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDBFIE0	TDBEIE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEIE0	Normal Transmit Data Buffer Empty Interrupt Enable 0 0: Disables Tx0 Data Buffer Empty Interrupt Signal. 1: Enables Tx0 Data Buffer Empty Interrupt Signal.	R/W
1	RDBFIE0	Normal Receive Data Buffer Full Interrupt Enable 0 0: Disables Rx0 Data Buffer Full Interrupt Signal. 1: Enables Rx0 Data Buffer Full Interrupt Signal.	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

The PIO Interrupt Signal Enable register enables signaling of outstanding interrupts received by IIC.

TDBEIE0 bit (Normal Transmit Data Buffer Empty Interrupt Enable 0)

This bit is used to enable or disable the Normal Tx Data buffer 0 empty interrupt (IICn_TX) requests when the NTST.TDBEF0 flag is set to 1.

RDBFIE0 bit (Normal Receive Data Buffer Full Interrupt Enable 0)

This bit is used to enable or disable the Normal Rx Data buffer 0 full interrupt (IICn_RX) requests when the NTST.RDBFF0 flag is set to 1.

27.2.26 NTSTFC : Normal Transfer Status Force Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x1EC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDBFFC0	TDBEFC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TDBEE0位（正常发送数据缓冲区空使能0）

当该位为1时，启用NTST.TDBEF0的操作。

NTST.TDBEF0标志的设置条件和清除条件见NTST.TDBEF0的详细信息。

RDBFE0位（正常接收数据缓冲器满使能0）

当该位为1时，启用NTST.RDBFF0的操作。

NTST.RDBFF0标志的设置条件和清除条件参见NTST.RDBFF0的详细信息。

27.2.25 NTIE:正常传输中断使能寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x1E8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDBFIE0	TDBEIE0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEIE0	正常发送数据缓冲区空中断使能0 0：禁用Tx0数据缓冲区空中断信号。1：使能Tx0数据缓冲区空中断信号。	R/W
1	RDBFIE0	正常接收数据缓冲区满中断使能0 0：禁用Rx0数据缓冲器满中断信号。1：使能Rx0数据缓冲器满中断信号。	R/W
31:2	—	这些位被读取为0。写入值应为0。	R/W

PIO中断信号使能寄存器启用IIC接收到的未完成中断的信号。

TDBEIE0位（正常发送数据缓冲区空中断允许0）

该位用于启用或禁用正常Tx数据缓冲区0空中断（IICn_TX）请求，当NTST.TDBEF0标志设置为1。

RDBFIE0位（正常接收数据缓冲区满中断允许0）

当NTST.RDBFF0标志设置为1时，该位用于启用或禁用正常Rx数据缓冲区0完全中断(IICn_RX)请求。

27.2.26 NTSTFC:正常传输状态强制寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x1EC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDBFFC0	TDBEFC0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEFC0	Normal Transmit Data Buffer Empty Force 0 0: Not Force Tx0 Data Buffer Empty Interrupt for software testing. 1: Force Tx0 Data Buffer Empty Interrupt for software testing.	W
1	RDBFFC0	Normal Receive Data Buffer Full Force 0 0: Not Force Rx0 Data Buffer Full Interrupt for software testing. 1: Force Rx0 Data Buffer Full Interrupt for software testing.	W
31:2	—	The write value should be 0.	W

The PIO Interrupt Force register is used to force specific interrupt. It can be used for debug purposes.

TDBEFC0 bit (Normal Transmit Data Buffer Empty Force 0)

For software testing, when set to 1, forces the corresponding interrupt, subject to TDBEE0 and TDBEIE0 configuration.

RDBFFC0 bit (Normal Receive Data Buffer Full Force 0)

For software testing, when set to 1, forces the corresponding interrupt, subject to RDBFE0 and RDBFIE0 configuration.

27.2.27 BCST : Bus Condition Status Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x210

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BFREF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BFREF	Bus Free Detection Flag 0: Have not Detected Bus Free 1: Have Detected Bus Free	R
31:1	—	These bits are read as 0.	R

BFREF bit (Bus Free Detection Flag)

The Bus Free Condition is a period occurring after a STOP and before a START, and with the following duration:

- For Pure Bus: A duration of at least tCAS (see section 46.3.11. IIC Timing)
- For Mixed Bus: A duration of at least tBUF (see section 46.3.11. IIC Timing)

[Setting condition]

- After a STOP condition is detected, when the number of cycles (IICφ) that are set by BFRECDT.FRECYC[8:0] has passed in the state of SCL = SDA = 1.
- After setting BCTL.BUSE to 1, when the number of cycles (IICφ) that are set by BFRECDT.FRECYC[8:0] has passed in the state of SCL = SDA = 1.

[Clearing condition]

- When SCL and SDA are other than high.
- When the BCTL.BUSE bit is set to 0.

Bit	Symbol	Function	R/W
0	TDBEFC0	正常发送数据缓冲区清空强制0 0：不强制用于软件测试的Tx0数据缓冲区空中断。1：强制Tx0数据缓冲区清空中断以进行软件测试。	W
1	RDBFFC0	正常接收数据缓冲器满力0 0：不强制Rx0数据缓冲区满中断用于软件测试。1：强制Rx0数据缓冲区满中断以进行软件测试。	W
31:2	—	写入值应为0。	W

PIO中断强制寄存器用于强制特定中断。它可用于调试目的。

TDBEFC0位（正常发送数据缓冲区清空强制0）

对于软件测试，当设置为1时，强制相应的中断，取决于TDBEE0和TDBEIE0配置。

RDBFFC0位（正常接收数据缓冲器满力0）

对于软件测试，当设置为1时，强制相应的中断，取决于RDBFE0和RDBIE0配置。

27.2.27 BCST:总线条件状态寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x210

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BFREF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BFREF	总线空闲检测标志 0：未检测到总线空闲1：已检测到总线空闲	R
31:1	—	这些位读为0。	R

BFREF位（总线空闲检测标志）

总线空闲状态是在STOP之后和START之前发生的一段时间，持续时间如下：

●对于纯总线：至少tCAS的持续时间（参见第46.3.11节。IIC时序）

●对于混合总线：至少tBUF的持续时间（参见第46.3.11节。IIC时序）

[Setting condition]

●检测到STOP条件后，当在SCL=SDA=1的状态下经过BFRECDT.FRECYC[8:0]设置的周期数(IICφ)时。

●设置BCTL.BUSE为1后，在SCL=SDA=1的状态下，当BFRECDT.FRECYC[8:0]设置的周期数(IICφ)已经过去时。

[Clearing condition]

●当SCL和SDA不是高电平时。

●当BCTL.BUSE位设置为0时。

27.2.28 SVST : Slave Status Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x214

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SVAF2	SVAF1	SVAF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	HOAF	—	—	—	—	—	—	—	—	DVIDF	HSMCF	—	—	—	—	GCAF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	GCAF	General Call Address Detection Flag 0: General call address does not detect. 1: General call address detects.	R/W*1
4:1	—	These bits are read as 0. The write value should be 0.	R/W
5	HSMCF*2	Hs-mode Master Code Detection Flag 0: Hs-mode Master Code does not detect. 1: Hs-mode Master Code detects.	R/W*1
6	DVIDF	Device-ID Address Detection Flag 0: Device-ID command does not detect. 1: Device-ID command detects. • This bit set to 1 when the first frame received immediately after a START condition is detected matches a value of (device ID (1111 100) + 0[W]).	R/W*1
14:7	—	These bits are read as 0. The write value should be 0.	R/W
15	HOAF	Host Address Detection Flag 0: Host address does not detect. 1: Host address detects. • This bit set to 1 when the received slave address matches the host address (0001 000).	R/W*1
16	SVAF0	Slave Address Detection Flag 0 0: Slave 0 does not detect 1: Slave 0 detect	R/W*1
17	SVAF1	Slave Address Detection Flag 1 0: Slave 1 does not detect 1: Slave 1 detect	R/W*1
18	SVAF2	Slave Address Detection Flag 2 0: Slave 2 does not detect 1: Slave 2 detect	R/W*1
31:19	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Clearing (to 0) condition : Writing 0 after the 1 state is read.
Note 2. The HSMCF bit is supported by IIC0(SCL0_A, SDA0_A). The HSMCF is a reserved bit in the not supported channel.

GCAF flag (General Call Address Detection Flag)

I2C Normal Wake-Up Mode1 / 2 sets GCAF to 1 when switching from asynchronous operation to synchronous unit.

[Setting condition]

- This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the first byte when all of the followings are satisfied.
  1. The SVCTL.GCAE bit = 1 (General call address detection is enabled).
  2. When the received slave address matches the general call address (0000 000 + 0 (write)).

[Clearing condition]

27.2.28 SVST：从机状态寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x214

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SVAF2	SVAF1	SVAF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	HOAF	—	—	—	—	—	—	—	—	DVIDF	HSMCF	—	—	—	—	GCAF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	GCAF	广播呼叫地址检测标志 0：不检测广播地址。1：广播地址检测 。	R/W*1
4:1	—	这些位被读取为0。写入值应为0。	R/W
5	HSMCF*2	Hs-mode主码检测标志 0：不检测Hs模式主码。1：Hs模式主码检 测。	R/W*1
6	DVIDF	设备ID地址检测标志 0：未检测到Device-ID命令。1：Device -ID命令检测。● 当检测到START条件后立即接收到的第一个帧与(设备ID(1111100)+0[W]) 的值匹配时，该位设置为1。	R/W*1
14:7	—	这些位被读取为0。写入值应为0。	R/W
15	HOAF	主机地址检测标志 0：不检测主机地址。1：主机地 址检测。● 当接收到的从机地址与主机地址(0001000)匹配时，该位设置为1。	R/W*1
16	SVAF0	从地址检测标志0 0：从机0未检测1：从机0 检测	R/W*1
17	SVAF1	从地址检测标志1 0：从机1未检测1：从机1 检测	R/W*1
18	SVAF2	从地址检测标志2 0：从机2未检测1：从机2 检测	R/W*1
31:19	—	这些位被读取为0。写入值应为0。	R/W

注1.清零（到0）条件：读取1状态后写入0。
注2.IIC0(SCL0_A SDA0_A)支持HSMCF位。HSMCF是不受支持通道中的保留位。

GCAF标志（广播呼叫地址检测标志）

I2C正常唤醒模式12当从异步操作切换到同步单元时，将GCAF设置为1。

[Setting condition]

●当满足以下所有条件时，该标志在第一个字节的第9个SCL时钟周期的上升沿设置为1。

1.SVCTL.GCAE位=1（启用广播呼叫地址检测）。
2.当接收到的从机地址与广播地址匹配时（0000000+0（写））。

[Clearing condition]

- When 0 is written to the GCAF flag after reading GCAF flag to be 1.
- When a STOP condition is detected.
- When a Repeated START condition is detected.

HSMCF flag (Hs-mode Master Code Detection Flag)

The I2C Normal Wake-Up Mode 1/2 sets 1 to HSMCF when switching from asynchronous operation to synchronous unit.

[Setting condition]

- This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the first byte when all of the followings are satisfied.
  1. The SVCTL.HSMCE bit = 1 (Hs-mode master code detection is enabled).
  2. When the first byte received immediately after a START condition is detected matches a value of Hs-mode master code (0000 1XXX) + 1 (NACK).

[Clearing condition]

- When 0 is written to the HSMCF flag after reading HSMCF flag to be 1.
- When a STOP condition is detected.

DVIDF flag (Device-ID Address Detection Flag)

[Setting condition]

- This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the first byte when all of the followings are satisfied.
  1. The SVCTL.DVIDE bit = 1 (Device-ID address detection is enabled).
  2. When the first byte received immediately after a START condition or Repeated START condition is detected matches a value of Device ID (1111 100) + 0 (write).

[Clearing condition]

- When 0 is written to the DVIDF flag after reading DVIDF flag to be 1.
- When a STOP condition is detected.
- This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the first byte when the following 1 and 2 or 1 and 3 are satisfied.
  1. The SVCTL.DVIDE bit = 1 (Device-ID address detection is enabled).
  2. When the first byte received immediately after a START condition or Repeated START condition is detected does not match a value of Device ID (1111 100).
  3. When the first byte received immediately after a START condition or Repeated START condition is detected matches a value of (device ID (1111 100) + 0 [W]) and the second byte does not match any of slave addresses 0 to 2.

HOAF flag (Host Address Detection Flag)

I2C Normal Wake-Up Mode1 / 2 sets HOAF to 1 at the time of switching from asynchronous operation to synchronous unit.

[Setting condition]

- This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the first byte when all of the followings are satisfied.
  1. The SVCTL.HOAE bit = 1 (Host address detection is enabled).
  2. When the received slave address matches the host address (0001 000).

[Clearing condition]

- When 0 is written to the HOAF flag after reading HOAF flag to be 1.
- When a STOP condition is detected.
- When a Repeated START condition is detected.

●读取GCAF标志为1后，向GCAF标志写入0时。
●检测到停止条件时。
●当检测到重复启动条件时。

HSMCF标志（Hs模式主码检测标志）

当从异步操作切换到同步单元时，I2C正常唤醒模式12将1设置为HSMCF。

[Setting condition]

●当满足以下所有条件时，该标志在第一个字节的第9个SCL时钟周期的上升沿设置为1。

1.SVCTL.HSMCE位=1（启用Hs模式主机代码检测）。
2.当检测到START条件后立即接收到的第一个字节与Hs模式主码(00001XXX)+1(NACK)的值匹配时。

[Clearing condition]

●读取HSMCF标志为1后向HSMCF标志写入0时。
●检测到停止条件时。

DVIDF标志（设备ID地址检测标志）

[Setting condition]

●当满足以下所有条件时，该标志在第一个字节的第9个SCL时钟周期的上升沿设置为1。

1.SVCTL.DVIDE位=1（启用设备ID地址检测）。
2.当检测到START条件或重复START条件后立即接收到的第一个字节与设备ID(1111100)+0（写入）的值匹配时。

[Clearing condition]

●将DVIDF标志读取为1后，向DVIDF标志写入0时。
●检测到停止条件时。
●当满足后面的1和2或1和3时，该标志在第一个字节的第9个SCL时钟周期的上升沿设置为0。

1.SVCTL.DVIDE位=1（启用设备ID地址检测）。
2.当检测到START条件或重复START条件后立即接收到的第一个字节与设备ID(1111100)的值不匹配时。

3.检测到START条件或重复START条件后立即接收到的第一个字节时
匹配值(设备ID(1111100)+0[W])并且第二个字节不匹配从地址0到2中的任何一个。

HOAF标志（主机地址检测标志）

I2C正常唤醒模式12在从异步操作切换到同步单元时将HOAF设置为1。

[Setting condition]

●当满足以下所有条件时，该标志在第一个字节的第9个SCL时钟周期的上升沿设置为1。

1.SVCTL.HOAE位=1（启用主机地址检测）。
2.当接收到的从机地址与主机地址（0001000）匹配时。

[Clearing condition]

●读取HOAF标志为1后向HOAF标志写入0时。
●检测到停止条件时。
●当检测到重复启动条件时。

SVAFy flags (Slave Address Detection Flag y (y = 0 to 2))

I²C Normal Wake-Up Mode1 / 2 sets 1 to SVAF2 / 1 / 0 when switching from asynchronous operation to synchronous unit.

[Setting condition]

For 7-bit address format: SVDVADy.SADLG bit = 0.

- This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the first byte when all of the followings are satisfied.
  1. The SVCTL.SVAEy bit = 1 (Slave n enabled).
  2. When the received slave address matches the SVDVADy.SVAD[6:0] bits value.

For 10-bit address format: SVDVADy.SADLG bit = 1.

- This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the second byte when all of the followings are satisfied.
  1. The SVCTL.SVAEy bit = 1 (Slave n enabled).
  2. When the received slave address matches a value of 11110 + SVDVADy.SVAD[9:8] bits and the following address matches the SVDVADy.SVAD[7:0] value.

[Clearing condition]

- When 0 is written to the SVAFy flag after reading SVAFy flag to be 1.
- When a STOP condition is detected.

For 7-bit address format: SVDVADy.SADLG bit = 0.

- This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the first byte when all of the followings are satisfied.
  1. The SVCTL.SVAEy bit = 1 (Slave y enabled).
  2. When the received slave address does not match SVDVADy.SVAD[6:0] bits value.

For 10-bit address format: SVDVADy.SADLG bit = 1.

- This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the first byte when all of the followings are satisfied.
  1. The SVCTL.SVAEy bit = 1 (Slave y enabled).
  2. When the received slave address does not match a value of 11110 + SVDVADy.SVAD[9:8] bits.
- This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the second byte when all of the followings are satisfied.
  1. The SVCTL.SVAEy bit = 1 (Slave y enabled).
  2. When the received slave address matches a value of 11110 + SVDVADy.SVAD[9:8] bits and the following address does not match the SVDVADy.SVAD[7:0] value.

SVAFy标志（从机地址检测标志y（y=0到2））

I2CNormalWake-UpMode12当从异步操作切换到同步单元时，将1设置为SVAF210。

[Setting condition]

对于7位地址格式：SVDVADy.SADLG位=0。

●当满足以下所有条件时，该标志在第一个字节的第9个SCL时钟周期的上升沿设置为1。

1.SVCTL.SVAEy位=1（从机n启用）。

2.当接收到的从机地址与SVDVADy.SVAD[6:0]位值匹配时。

对于10位地址格式：SVDVADy.SADLG位=1。

●当满足以下所有条件时，该标志在第二个字节的第9个SCL时钟周期的上升沿设置为1。

1.SVCTL.SVAEy位=1（从机n启用）。

2.当接收到的从机地址与11110+SVDVADy.SVAD[9:8]位的值匹配且以下地址与SVDVADy.SVAD[7:0]值匹配时。

[Clearing condition]

●将SVAFy标志读取为1后，将0写入SVAFy标志时。

●检测到停止条件时。

对于7位地址格式：SVDVADy.SADLG位=0。

●当满足以下所有条件时，该标志在第一个字节的第9个SCL时钟周期的上升沿设置为0。

1.SVCTL.SVAEy位=1（从机y启用）。

2.当接收到的从机地址与SVDVADy.SVAD[6:0]位值不匹配时。

对于10位地址格式：SVDVADy.SADLG位=1。

●当满足以下所有条件时，该标志在第一个字节的第9个SCL时钟周期的上升沿设置为0。

1.SVCTL.SVAEy位=1（从机y启用）。

2.当接收到的从机地址与11110+SVDVADy.SVAD[9:8]位的值不匹配时。

●当满足以下所有条件时，该标志在第二个字节的第9个SCL时钟周期的上升沿设置为0。

1.SVCTL.SVAEy位=1（从机y启用）。

2.当接收到的从机地址与11110+SVDVADy.SVAD[9:8]位的值匹配，并且后面的地址与SVDVADy.SVAD[7:0]的值不匹配时。

27.2.29 WUST : Wake Up Unit Operating Status Register

Base address: IIC0WU_B = 0x4009_F098

Offset address: 0x180

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WUASYNF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WUASYNF	Wake-up function asynchronous operation status flag 0: IIC synchronous circuit enable condition. 1: IIC asynchronous circuit enable condition.	R
31:1	—	These bits are read as 0.	R

WUASYNF flag (Wake-up function asynchronous operation status flag)

This bit shows whether IIC is in the PCLKA/IICCLK asynchronous operation (WUCTL.WUFE bit = 1).

[Setting condition]

- All of the followings are satisfied.
  1. The WUCTL.WUFE bit = 1 (Wake-up function is enabled)
  2. When the BCST.BFREF flag = 1 after 0 is written to the WUCTL.WUFSYNE bit

[Clearing condition]

- The WUCTL.WUFE bit = 0 (Wake-up function is disabled)
- All of the followings are satisfied.
  1. The WUCTL.WUFE bit = 1 (Wake-up function is enabled)
  2. Wake-up event is detected
  3. When 1 is written to the WUCTL.WUFSYNE bit during WUASYNF flag = 1

27.2.30 SDATBASy : Slave Device Address Table Basic Register y (y = 0 to 2)

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x2B0 + 0x04 × y

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SDADLS	SDSTAD[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	SDSTAD[9:0]	Slave Device Static Address IIC Static Address	R/W

27.2.29 WUST：唤醒单元操作状态寄存器

Base address: IIC0WU_B = 0x4009_F098

Offset address: 0x180

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WUASYNF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WUASYNF	唤醒功能异步操作状态标志 0：IIC同步电路使能条件。1：IIC异步电路使能条件。	R
31:1	—	这些位读为0。	R

WUASYNF标志（唤醒功能异步操作状态标志）

该位显示IIC是否处于PCLKAIICCLK异步操作（WUCTL.WUFE位=1）。

[Setting condition]

●满足以下所有条件。

1.WUCTL.WUFE位=1（启用唤醒功能）

2.当BCST.BFREF标志=1后将0写入WUCTL.WUFSYNE位

[Clearing condition]

●WUCTL.WUFE位=0（禁用唤醒功能）

●满足以下所有条件。

1.WUCTL.WUFE位=1（启用唤醒功能）

2.检测到唤醒事件

3.在WUASYNF标志=1期间向WUCTL.WUFSYNE位写入1时

27.2.30 SDATBASy：从设备地址表基本寄存器y（y=0到2）

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x2B0 + 0x04 × y

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SDADLS	SDSTAD[9:0]									
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	SDSTAD[9:0]	从设备静态地址 IIC静态地址	R/W

Bit	Symbol	Function	R/W
10	SDADLS	Slave Device Address Length Selection 0: Slave Device address length 7 bits selected. 1: Slave Device address length 10 bits selected. (I^2C device only)	R/W
31:11	—	These bits are read as 0. The write value should be 0.	R/W

Note: SW write to the SDATBAS register of the main master is prohibited.

SDSTAD[9:0] bit (Slave Device Static Address)

When the 7-bit address format is selected (SDADLS bit is 0), the lower 7 bits of SDSTAD[9:0] function as the 7-bit address. When the 10-bit address format is selected (SDADLS bit is 1), the SDSTAD[9:0] function as the 10-bit address. While the SVCTL.SVAEy bit is 0, the setting of this bit is ignored.

27.2.31 SVDVADy : Slave Device Address Register y (y = 0 to 2)

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x330 + 0x04 × y

Bit position:	31	30	29	28	27	26	25									16
Bit field:	—	SSTADV	—	—	SADLG	—	SVAD[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 0.	R
25:16	SVAD[9:0]	Slave Address A slave address is set. When rewriting SVAD, change to SVAE = 0 and rewrite.	R
26	—	This bit is read as 0.	R
27	SADLG	Slave Address Length 0: The 7-bit address format is selected. 1: The 10-bit address format is selected.	R
29:28	—	These bits are read as 0.	R
30	SSTADV	Slave Static Address Valid 0: Slave address is disabled. 1: Slave address is enabled.	R
31	—	These bits are read as 0.	R

SVAD[9:0] bits (Slave Address)

The SVAD[9:0] bits indicate a valid slave address.

[The SVDVAD0.SDYADV bit = 1]

Note: This condition is only for SVDVAD0.SVAD[9:0].

- The SVAD[9:7] bits = 0
- The SVAD[6:0] bits = the SDATBAS0.SDDYAD[6:0] bits

[The SVDVADy.SSTADV bit = 1 and the SVDVADy.SADLG bit = 0]

- The SVAD[9:7] bits = 0
- The SVAD[6:0] bits = the SDATBASy.SDSTAD[6:0] bits

Bit	Symbol	Function	R/W
10	SDADLS	从设备地址长度选择 0：选择从设备地址长度7位。1：选择从设备地址长度10位。（仅限I2C设备）	R/W
31:11	—	这些位被读取为0。写入值应为0。	R/W

Note: 禁止SW写入主主机的SDATBAS寄存器。

SDSTAD[9:0]位（从设备静态地址）

Whenthe7-bitaddressformatisselected(SDADLSbitis0) thelower7bitsofSDSTAD[9:0]functionasthe7-bitaddress. Whenthe10-bitaddressformatisselected(SDADLSbitis1) theSDSTAD[9:0]functionasthe10-bitaddress.虽然SVCTL.SVAEy位为0，该位的设置被忽略。

27.2.31 SVDVADy：从设备地址寄存器y（y=0到2）

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x330 + 0x04 × y

Bit position:	31	30	29	28	27	26	25									16
Bit field:	—	SSTADV	—	—	SADLG	—	SVAD[9:0]									
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	这些位读为0。	R
25:16	SVAD[9:0]	从地址 从机地址被设置。 重写SVAD时，更改为SVAE=0并重写。	R
26	—	该位读为0。	R
27	SADLG	从地址长度 0：选择7位地址格式。1：选择10位地址格式。	R
29:28	—	这些位读为0。	R
30	SSTADV	从站静态地址有效 0：从地址禁用。1：从地址使能。	R
31	—	这些位读为0。R	

SVAD[9:0] bits (Slave Address)

SVAD[9:0]位指示有效的从地址。

[The SVDVAD0.SDYADV bit = 1]

Note: 此条件仅适用于SVDVAD0.SVAD[9:0]。

- SVAD[9:7]位=0
- SVAD[6:0]位=SDATBAS0.SDDYAD[6:0]位

[SVDVADy.SSTADV位=1且SVDVADy.SADLG位=0]

- SVAD[9:7]位=0
- SVAD[6:0]位=SDATBASy.SDSTAD[6:0]位

[The SVDVADy.SSTADV bit = 1 and the SVDVADy.SADLG bit = 1]

- The SVAD[9:0] bits = the SDATBASy.SDSTAD[9:0] bits

SADLG bit (Slave Address Length)

[Setting condition]

- All of the followings are satisfied:

1. The SVCTL.SVAEy bit = 1 (Slave y is enabled)
2. The SDATBASy.SDADLS bit = 1 (The address length is 10 bits)

[Clearing condition]

- [Setting condition] is not satisfied.

SSTADV bit (Slave Static Address Valid)

[Setting condition]

- All of the followings are satisfied:

1. The SVCTL.SVAEy bit = 1 (Slave y is enabled)
2. The SVDVAD0.SDYADV bit = 0 (Dynamic Address is disabled)

   Note: This condition is only for SVDVAD0.SSTADV.

3. If the SVDVADy.SADLG bit = 0, the SDATBASy.SDSTAD[6:0] bits are not all 0
   If the SVDVADy.SADLG bit = 1, the SDATBASy.SDSTAD[9:0] bits are not all 0

[Clearing condition]

- [Setting condition] is not satisfied.

27.2.32 BITCNT : Bit Count Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x380

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BCNT[4:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	BCNT[4:0]	Bit Counter Indicates the number of bits remaining to be transferred. For details on the values, see Table 27.7.	R
31:5	—	These bits are read as 0.	R

BCNT[4:0] bits (Bit Counter)

These bits function as a counter that indicates the number of bits remaining to be transferred at the detection of a sampling edge on the SCLn line.

Table 27.7 I^2C transfer (1 of 2)

BCNT[4:0]	Master		Slave	
	Address phase	Data phase	Address phase	Data phase
0x00	2 to 1 bits	2 to 1 bits	3 to 1 bits	2 to 1 bits
0x01	3 bits	3 bits	4 bits	3 bits

[SVDVADy.SSTADV位=1且SVDVADy.SADLG位=1]

●SVAD[9:0]位=SDATBASy.SDSTAD[9:0]位

SADLG位（从地址长度）

[Setting condition]

●满足以下所有条件：

1.SVCTL.SVAEy位=1（从机y使能）

2.SDATBASy.SDADLS位=1（地址长度为10位）

[Clearing condition]

●[设定条件]不成立。

SSTADV位（从机静态地址有效）

[Setting condition]

●满足以下所有条件：

1.SVCTL.SVAEy位=1（从机y使能）

2.SVDVAD0.SDYADV位=0（禁用动态地址）

Note: 此条件仅适用于SVDVAD0.SSTADV。

3.如果SVDVADy.SADLG位=0，则SDATBASy.SDSTAD[6:0]位不全为0
如果SVDVADy.SADLG位=1，则SDATBASy.SDSTAD[9:0]位不全为0

[Clearing condition]

●[设定条件]不成立。

27.2.32 BITCNT:位计数寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x380

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BCNT[4:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	BCNT[4:0]	位计数器 指示剩余要传输的位数。 有关值的详细信息，请参见表27.7。	R
31:5	—	这些位读为0。	R

BCNT[4:0] bits (Bit Counter)

这些位用作计数器，指示在检测到SCLn线上的采样边沿时要传输的剩余位数。

Table 27.7 I2C转移(1of2)

BCNT[4:0]	Master		Slave	
	地址阶段	数据阶段	地址阶段	数据阶段
0x00	2比1位	2比1位	3比1位	2比1位
0x01	3 bits	3 bits	4 bits	3 bits

Table 27.7 I^2C transfer (2 of 2)

BCNT[4:0]	Master		Slave	
	Address phase	Data phase	Address phase	Data phase
0x02	4 bits	4 bits	5 bits	4 bits
0x03	5 bits	5 bits	6 bits	5 bits
0x04	6 bits	6 bits	7 bits	6 bits
0x05	7 bits	7 bits	8 bits	7 bits
0x06	8 bits	8 bits	9 bits	8 bits
0x07	9 bits	9 bits	—	9 bits

27.2.33 PRSTDBG : Present State Debug Register

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x3CC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	SDOLV	SCOLV	SDILV	SCILV
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SCILV	SCL Line Signal Level This bit is used to check the SCL Line level, in order to recover from errors and for debugging.	R
1	SDILV	SDA Line Signal Level This bit is used to check the SDA Line level, in order to recover from errors and for debugging.	R
2	SCOLV	SCL Output Level 0: IIC has driven the SCL pin low. 1: IIC has released the SCL pin.	R
3	SDOLV	SDA Output Level 0: IIC has driven the SDA pin low. 1: IIC has released the SDA pin.	R
31:4	—	These bits are read as 0.	R

SDOLV bit (SDA Output Level) and SCOLV bit (SCL Output Level)

When reading these bits, the state of signals output from IIC can be read.

27.3 Operation

27.3.1 Details of Function

27.3.1.1 Operation Mode

IIC has 2 operation modes which are master mode operation and slave mode operation.

Table 27.7 I2C转移(2of2)

BCNT[4:0]	Master		Slave	
	地址阶段	数据阶段	地址阶段	数据阶段
0x02	4 bits	4 bits	5 bits	4 bits
0x03	5 bits	5 bits	6 bits	5 bits
0x04	6 bits	6 bits	7 bits	6 bits
0x05	7 bits	7 bits	8 bits	7 bits
0x06	8 bits	8 bits	9 bits	8 bits
0x07	9 bits	9 bits	—	9 bits

27.2.33 PRSTDBG:当前状态调试寄存器

Base address: IIC_Bn = 0x4009_F000 + 0x0100 × n (n = 0, 1)

Offset address: 0x3CC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	SDOLV	SCOLV	SDILV	SCILV
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SCILV	SCL线路信号电平 该位用于检查SCL线路电平，以便从错误中恢复和调试。	R
1	SDILV	SDA线路信号电平 该位用于检查SDA线路电平，以便从错误中恢复和调试。	R
2	SCOLV	SCL输出电平 0：IIC已将SCL引脚驱动为低电平 。1：IIC已释放SCL引脚。	R
3	SDOLV	SDA输出电平 0：IIC已将SDA引脚驱动为低电平 。1：IIC已释放SDA引脚。	R
31:4	—	这些位读为0。	R

SDOLV位（SDA输出电平）和SCOLV位（SCL输出电平）

读取这些位时，可以读取IIC输出的信号状态。

27.3 Operation

27.3.1 功能详情

27.3.1.1 操作模式

IIC有2种操作模式，即主模式操作和从模式操作。

27.3.1.1.1 Master Mode Operation

(1) I2C Master Operation

(a) Data Write Transfer (Single Buffer transfer)

In master transmit operation, IIC outputs the SCL clock and transmitted data signals as the master device, and the slave device returns acknowledgments. Figure 27.47 shows an example of usage of master transmission and Figure 27.2 to Figure 27.4 show the timing of operations in master transmission.

The following describes the procedure and operations for master transmission.

1. Initial settings. For details, see section 27.3.2.1. Initial Setting Flow.
2. Read the BCST.BFREF flag to check that the bus is open, and then set the CNDCTL.STCND bit to 1 (START condition issuance request). Upon receiving the request, IIC issues a START condition. At the same time, the BFREF flag bit is automatically set to 0, the BST.STCNDDF flag is automatically set to 1 and the STCND bit is automatically set to 0. At this time, if the START condition is detected and the internal levels for the SDA output state and the levels on the SDAn line have matched while the STCND bit = 1, IIC recognizes that issuing of the START condition as requested by the STCND bit has been successfully completed, and bits CRMS and TRMD in the PRSST register are automatically set to 1, placing IIC in master transmit mode. The NTST.TDBEF0 flag is also automatically set to 1 in response to setting of the TRMD bit to 1.
3. Check that the NTST.TDBEF0 flag = 1, and then write the value for transmission (the slave address and the R/W# bit) to the NTDTBP0 register. Once the data for transmission are written to the NTDTBP0 register, the TDBEF0 flag is automatically set to 0, the data are transferred from the Normal Transmit Data Buffer 0 to the Shift Register, and the TDBEF0 flag is again set to 1. After the byte containing the slave address and R/W# bit has been transmitted, the value of the TRMD bit is automatically updated to select master transmit or master receive mode in accord with the value of the transmitted R/W# bit. If the value of the R/W# bit was 0, IIC continues in master transmit mode. Because the BST.NACKDF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to the CNDCTL.SPCND bit to issue a STOP condition. For data transmission with an address in the 10-bit format, start by writing 1111 0, the 2 higher-order bits of the slave address, and W to the NTDTBP0 register as the first address transmission. Then, as the second address transmission, write the 8 lower-order bits of the slave address to the NTDTBP0 register.
4. After confirming that the NTST.TDBEF0 flag = 1, write the data for transmission to the NTDTBP0 register. IIC automatically holds the SCLn line low until the data for transmission are ready or a STOP condition is issued.
5. After all bytes of data for transmission have been written to the NTDTBP0 register, wait until the value of the BST.TENDF flag returns to 1, and then set the CNDCTL.SPCND bit to 1 (STOP condition issuance request). Upon receiving a STOP condition issuance request, IIC issues the STOP condition.
6. Upon detecting the STOP condition, IIC automatically sets bits CRMS and TRMD in the PRSST register to 00 and enters slave receive mode. Furthermore, it automatically sets the TDBEF0 and TENDF flags to 0, and sets the BST.SPCNDDF flag to 1.
7. After checking that the BST.SPCNDDF flag = 1, set the BST.NACKDF and SPCNDDF flags to 0 for the next transfer operation.

27.3.1.1.1 主模式操作

(1) I2C主操作

(a)数据写入传输（单缓冲区传输）

在主设备发送操作中，IIC作为主设备输出SCL时钟和发送的数据信号，从设备返回确认。图27.47显示了主传输的使用示例，图27.2至图27.4显示了主传输中的操作时序。

下面介绍主传输的步骤和操作。

1.初始设置。详见27.3.2.1节。初始设定流程。

2.读取BCST.BFREF标志以检查总线是否打开，然后将CNDCTL.STCND位设置为1（开始条件发出请求）。收到请求后，IIC发出START条件。同时，BFREF标志位自动置0，BST.STCNDDF标志位自动置1，STCND位自动置0。此时，如果检测到START条件且内部电平为当SDA输出状态和SDAn线上的电平匹配时，STCND位=1，IIC识别出由STCND位请求的START条件的发布已成功完成，并且PRSST寄存器中的CRMS和TRMD位自动设置为1，将IIC置于主机发送模式。响应TRMD位设置为1，NTST.TDBEF0标志也自动设置为1。

3.检查NTST.TDBEF0标志=1，然后将传输值（从机地址和RW#位）写入NTDTBP0寄存器。一旦要发送的数据写入NTDTBP0寄存器，TDBEF0标志自动设置为0，数据从正常发送数据缓冲区0传输到移位寄存器，并且TDBEF0标志再次设置为1。如果包含从机地址和RW#位已发送，则TRMD位的值会自动更新，以根据发送的RW#位的值选择主机发送或主机接收模式。如果RW#位的值为0，IIC继续在主机发送模式。由于此时BST.NACKDF标志为1表示没有从设备识别该地址或通信中存在错误，因此向CNDCTL.SPCND位写入1以发出STOP条件。对于地址为10位格式的数据传输，首先将11110、从机地址的高2位和W写入NTDTBP0寄存器作为第一个地址传输。然后，作为第二次地址传输，将从机地址的低8位写入NTDTBP0寄存器。

4.确认NTST.TDBEF0标志=1后，将要发送的数据写入NTDTBP0寄存器。IIC自动将SCLn线保持为低电平，直到传输数据准备好或发出STOP条件。

5.待传输数据的所有字节写入NTDTBP0寄存器后，等待
BST.TENDF标志返回1，然后将CNDCTL.SPCND位设置为1（发出停止条件请求）。IIC收到STOP条件发布请求后，发布STOP条件。

6.检测到STOP条件后，IIC自动将PRSST寄存器中的CRMS和TRMD位设置为00，并进入从机接收模式。此外，它自动将TDBEF0和TENDF标志设置为0，并将BST.SPCNDF标志设置为1。

7.检查BST.SPNCDDF标志=1后，将BST.NACKDF和SPCNDDF标志设置为0以进行下一次传输操作。

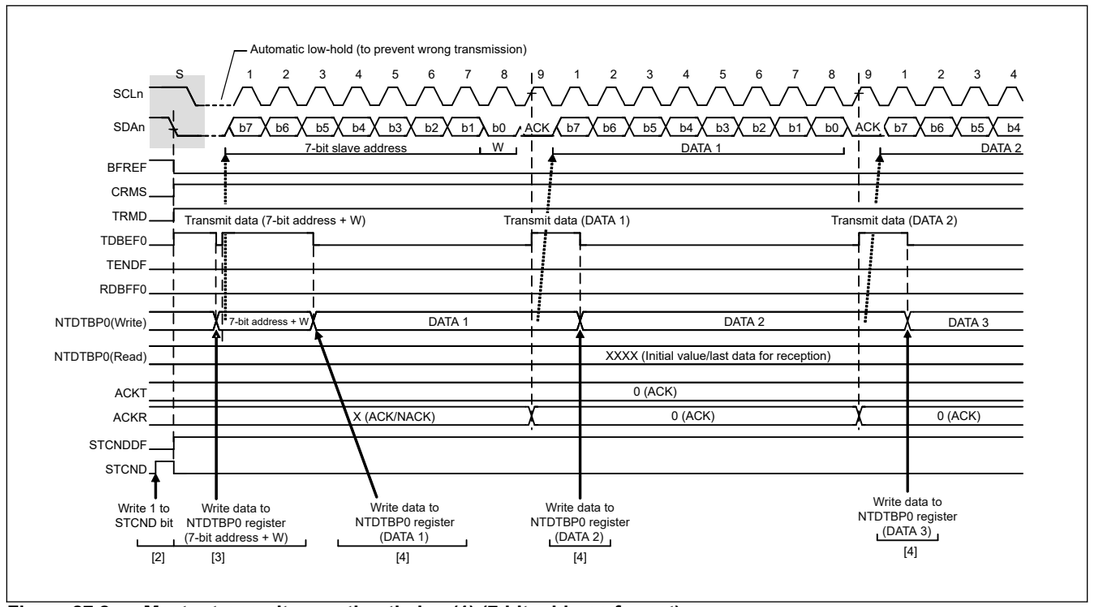


Figure 27.2 Master transmit operation timing (1) (7-bit address format)

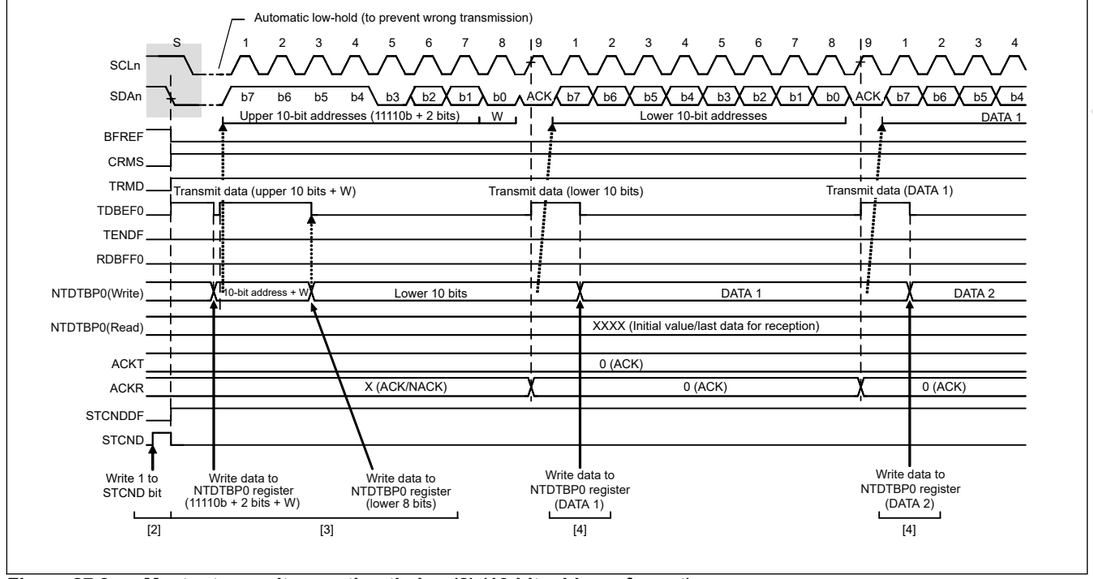


Figure 27.3 Master transmit operation timing (2) (10-bit address format)

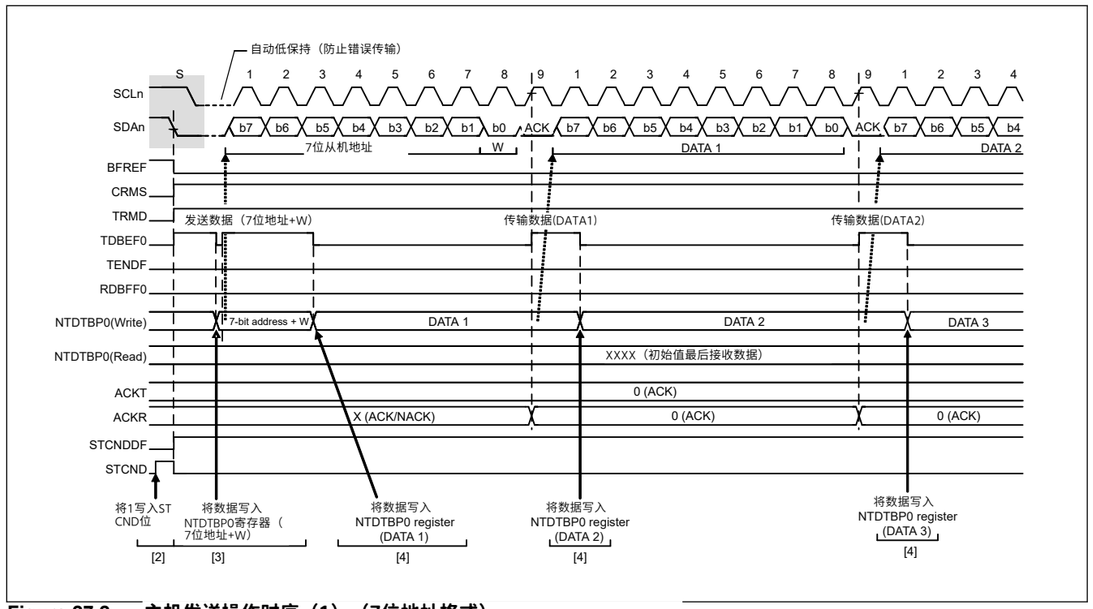


Figure 27.2 主机发送操作时序（1）（7位地址格式）

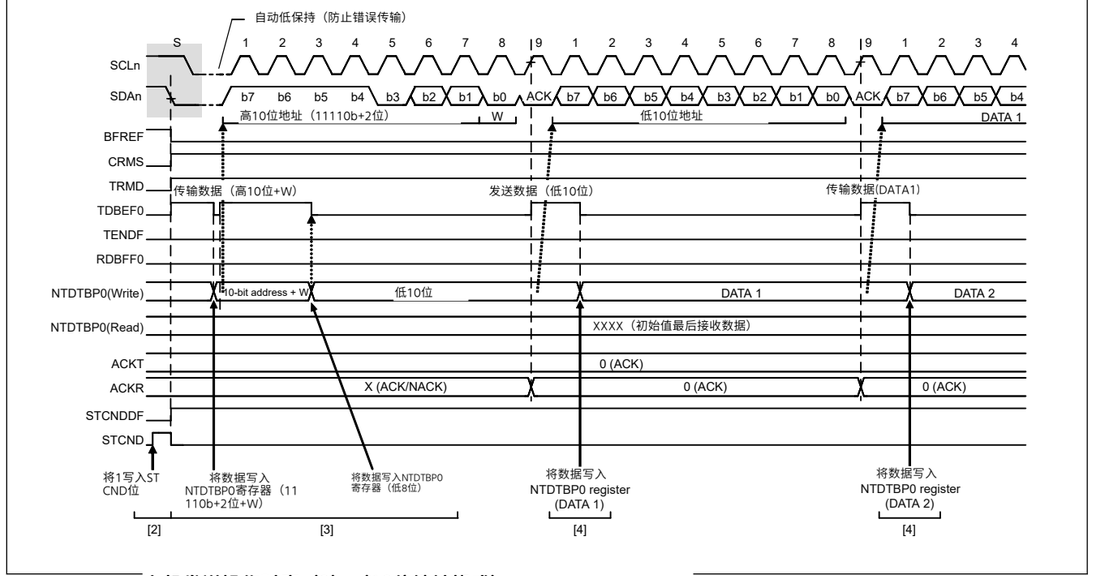


Figure 27.3 主机发送操作时序（2）（10位地址格式）

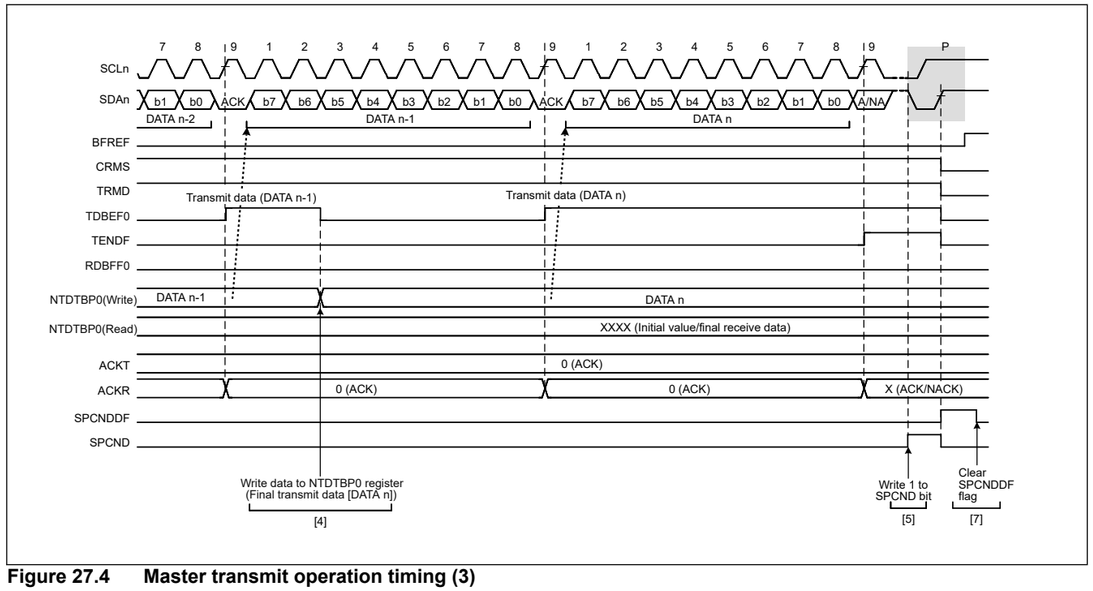


Figure 27.4 Master transmit operation timing (3)

(b) Data Read Transfer (Single Buffer transfer)

In master receive operation, IIC as a master device outputs the SCL clock, receives data from the slave device, and returns acknowledgments. Because IIC must start by sending a slave address to the corresponding slave device, this part of the procedure is performed in master transmit mode, but the subsequent steps are in master receive mode.

Figure 27.48 and Figure 27.49 show examples of usage of master reception (7-bit address format) and Figure 27.5 to Figure 27.7 show the timing of operations in master reception.

The following describes the procedure and operations for master reception.

1. Initial settings. For details, see section 27.3.2.1. Initial Setting Flow.
2. Read the BCST.BFREF flag to check that the bus is open, and then set the CNDCTL.STCND bit to 1 (START condition issuance request). Upon receiving the request, IIC issues a START condition. When IIC detects the START condition, the BFREF flag is automatically set to 0 and the BST.STCNDDF flag is automatically set to 1 and the STCND bit is automatically set to 0. At this time, if the START condition is detected and the levels for the SDA output and the levels on the SDAn line have matched while the STCND bit = 1, IIC recognizes that issuing of the START condition as requested by the STCND bit has been successfully completed, and bits CRMS and TRMD in the PRSST register are automatically set to 1, placing IIC in master transmit mode. The NTST.TDBEF0 flag is also automatically set to 1 in response to setting of the TRMD bit to 1.
3. Check that the NTST.TDBEF0 flag = 1, and then write the value for transmission (the first byte indicates the slave address and value of the R/W# bit) to the NTDTBP0 register. Once the data for transmission are written to the NTDTBP0 register, the TDBEF0 flag is automatically set to 0, the data are transferred from the Normal Transmit Data Buffer 0 to the Shift Register, and the TDBEF0 flag is again set to 1. Once the byte containing the slave address and R/W# bit has been transmitted, the value of the PRSST.TRMD bit is automatically updated to select transmit or receive mode in accord with the value of the transmitted R/W# bit. If the value of the R/W# bit was 1, the TRMD bit is set to 0 on the rising edge of the ninth cycle of SCL clock, placing IIC in master receive mode. At this time, the TDBEF0 flag is set to 0. The NTST.RDBFF0 flag is automatically set to 1 when ACK response is received from the slave device. If the slave device is not recognized or a communication failure occurs, the BST.NACKDF flag will be set to 1. At this time, set 1 to the CNDCTL.SPCND bit to issue a STOP condition. For master reception from a device with a 10-bit address, start by using master transmission to issue the 10-bit address, and then issue a Repeated START condition. After that, transmitting 1111 0, the two higher-order bits of the slave address, and the R bit places IIC in master receive mode.
4. Dummy read the NTDTBP0 register after confirming that the NTST.RDBFF0 flag = 1; this makes IIC start output of the SCL clock and start data reception.
5. After 1 byte of data has been received, the NTST.RDBFF0 flag is set to 1 on the rising edge of the eighth or ninth cycle of SCL clock (the clock signal) as selected by the SCSTRCTL.ACKTWE bit. Reading the NTDTBP0 register at this

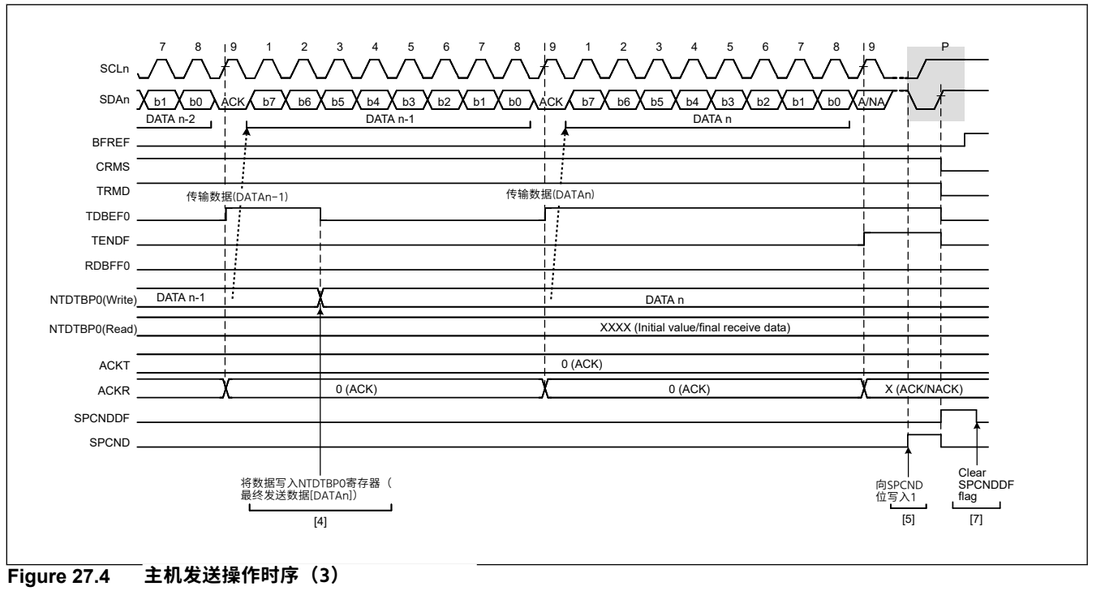


Figure 27.4 主机发送操作时序（3）

(b)数据读取传输（单缓冲区传输）

在主设备接收操作中，IIC作为主设备输出SCL时钟，从从设备接收数据，并返回确认。因为IIC必须先向对应的从设备发送一个从地址开始，所以这部分程序在主发送模式下执行，但后续步骤在主接收模式下进行。

图27.48和图27.49显示了主接收（7位地址格式）的使用示例，图27.5至图27.7显示了主接收中的操作时序。

下面介绍主接收的步骤和操作。

1.初始设置。详见27.3.2.1节。初始设定流程。

2.读取BCST.BFREF标志以检查总线是否打开，然后将CNDCTL.STCND位设置为1（开始条件发出请求）。收到请求后，IIC发出START条件。当IIC检测到START条件时，BFREF标志自动置0，BST.STCNDDF标志自动置1，STCND位自动置0。此时，如果检测到START条件且电平为SDA输出和SDAn线上的电平匹配，而STCND位=1，IIC识别出由STCND位请求的START条件的发出已成功完成，并且PRSST寄存器中的CRMS和TRMD位自动置位为1，将IIC置于主机发送模式。响应TRMD位设置为1，NTST.TDBEF0标志也自动设置为1。

3.检查NTST.TDBEF0标志=1，然后将要发送的值（第一个字节表示从机地址和RW#位的值）写入NTDTBP0寄存器。一旦要发送的数据写入NTDTBP0寄存器，TDBEF0标志自动设置为0，数据从正常发送数据缓冲区0传输到移位寄存器，并且TDBEF0标志再次设置为1。一旦字节包含从地址和

RW#位已发送，PRSST.TRMD位的值会自动更新，以根据发送的RW#位的值选择发送或接收模式。如果RW#位的值为1，则TRMD位在SCL时钟的第9个周期的上升沿设置为0，将IIC置于主机接收模式。此时，TDBEF0标志设置为0。当从从设备接收到ACK响应时，NTST.RDBFF0标志自动设置为1。如果从设备未被识别或发生通信故障，则BST.NACKDF标志将设置为1。此时，将CNDCTL.SPCND位设置为1以发出STOP条件。对于来自具有10位地址的设备的主机接收，首先使用主机发送来发出10位地址，然后发出重复启动条件。之后，发送11110、从机地址的两个高位位和R位将IIC置于主机接收模式。

4、确认NTST.RDBFF0标志=1后，假读NTDTBP0寄存器；这使得IIC开始输出SCL时钟并开始数据接收。

5.接收到1个字节的数据后，NTST.RDBFF0标志在由SCSTRCTL.ACKTWE位选择的SCL时钟（时钟信号）的第8个或第9个周期的上升沿设置为1。此时读取NTDTBP0寄存器

time will produce the received data, and the RDBFF0 flag is automatically set to 0 at the same time. Furthermore, the value of the acknowledgment field received during the ninth cycle of SCL clock is returned as the value set in the ACKCTL.ACKT bit. Furthermore, if the next byte to be received is the next to last byte, set the SCSTRCTL.RWE bit to 1 (for wait insertion) before reading the NTDTBP0 register (containing the second byte from last). As well as enabling NACK output even in the case of delays in processing to set the ACKCTL.ACKT bit to 1 (NACK) in step 6, due to other interrupts, etc., this fixes the SCLn line to the low level on the falling edge of the ninth clock cycle in reception of the last byte, so the state is such that issuing a STOP condition is possible.

6. When the SCSTRCTL.ACKTWE bit = 0 and the slave device must be notified that it is to end transfer for data reception after transfer of the next (final) byte, set the ACKCTL.ACKT bit to 1 (NACK).
7. After reading the byte before last from the NTDTBP0 register, if the value of the NTST.RDBFF0 flag is confirmed to be 1, write 1 to the CNDCTL.SPCND bit (STOP condition issuance request) and then read the last byte from the NTDTBP0 register. When 1 is written to the CNDCTL.SPCND bit, IIC is released from the wait state and issues the STOP condition after low-level output in the ninth clock cycle is completed or the SCLn line is released from the low-hold state.
8. Upon detecting the STOP condition, IIC automatically sets bits CRMS and TRMD in the PRSST register to 00 and enters slave receive mode. Furthermore, detection of the STOP condition leads to setting of the BST.SPCNDDF flag to 1.
9. After checking that the BST.SPCNDDF flag = 1, set the BST.NACKDF and SPCNDDF flags to 0 for the next transfer operation.

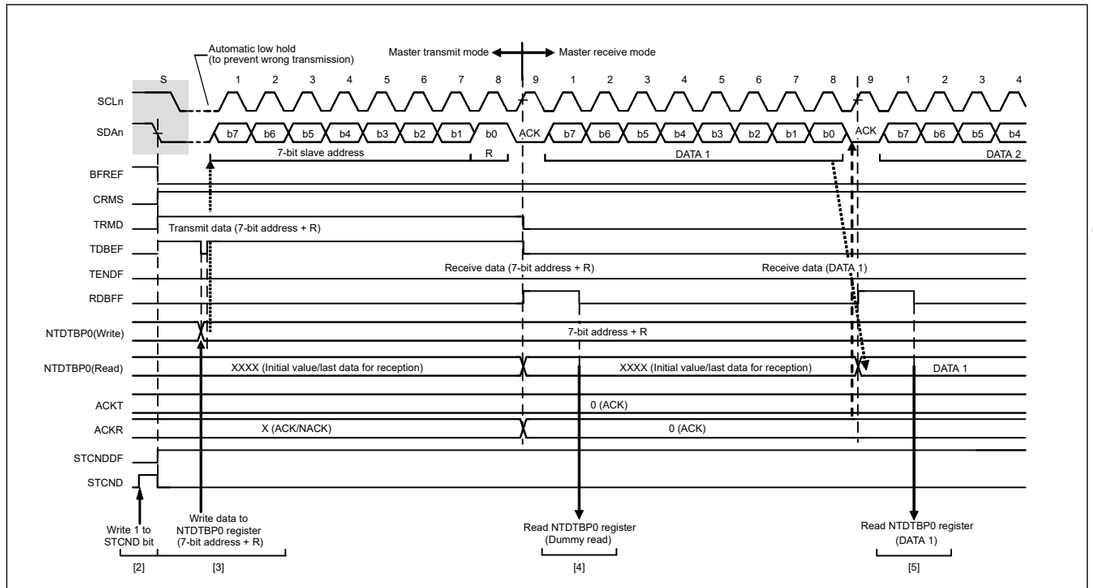


Figure 27.5 Master receive operation timing (1) (7-bit address format, when ACKTWE = 0)

time将产生接收到的数据，同时RDBFF0标志位自动设置为0。此外，在SCL时钟的第9个周期内接收到的确认字段的值作为ACKCTL.ACKT位中设置的值返回。此外，如果要接收的下一个字节是倒数第二个字节，则在读取NTDTBP0寄存器（包含倒数第二个字节）之前将SCSTRCTL.RWE位设置为1（等待插入）。即使在步骤6中将ACKCTL.ACKT位设置为1(NACK)的处理延迟的情况下，由于其他中断等，也可以启用NACK输出，这在下降时将SCLn线固定为低电平在接收最后一个字节时的第9个时钟周期的边沿，因此该状态使得发出STOP条件是可能的。

6.当SCSTRCTL.ACKTWE位=0且必须通知从设备在传输下一个（最终）字节后结束数据接收传输时，将ACKCTL.ACKT位设置为1（NACK）。

7.从NTDTBP0寄存器读取前一个字节后，如果确认NTST.RDBFF0标志的值为1，则将1写入CNDCTL.SPCND位（STOP条件发出请求），然后从NTDTBP0寄存器。当向CNDCTL.SPCND位写入1时，IIC从等待状态中释放并发出

第9个时钟周期的低电平输出完成或SCLn线从低保持状态释放后的STOP条件。

8.检测到STOP条件后，IIC自动将PRSST寄存器中的CRMS和TRMD位设置为00，并且
进入从机接收模式。此外，检测到STOP条件会导致将BST.SPCNDDF标志设置为1。

9.在检查BST.SPNCDDF标志=1后，将BST.NACKDF和SPCNDDF标志设置为0以进行下一次传输操作。

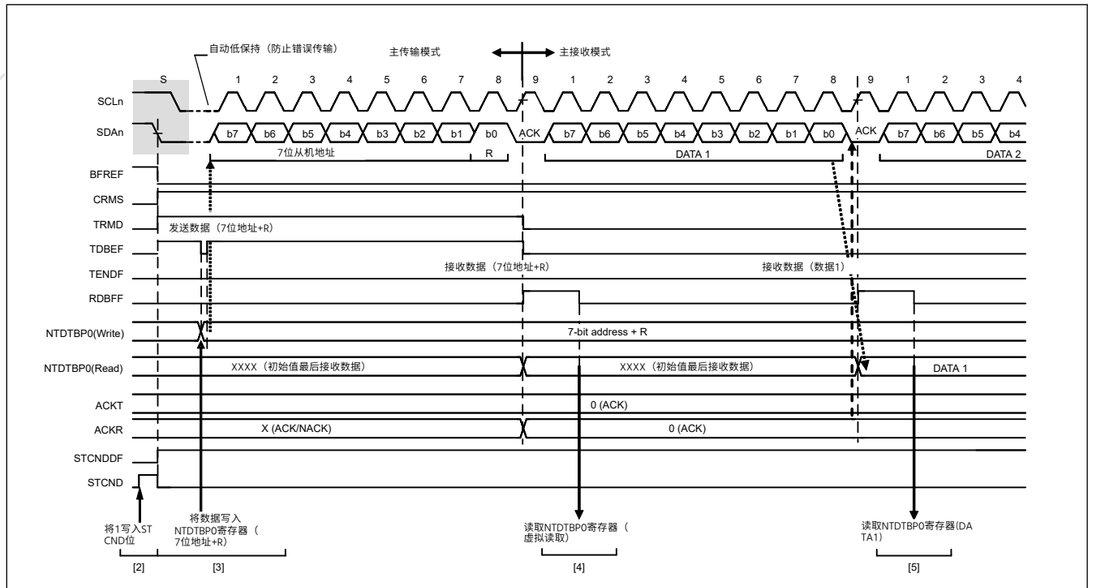


Figure 27.5 主机接收操作时序(1)（7位地址格式，当ACKTWE=0时）

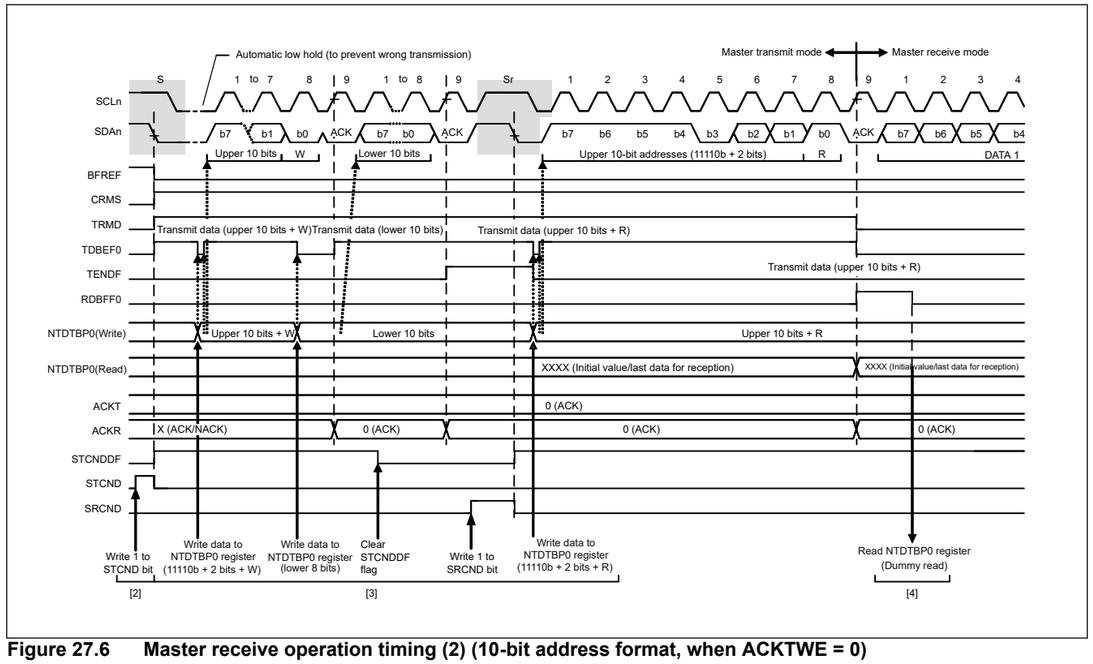


Figure 27.6 Master receive operation timing (2) (10-bit address format, when ACKTWE = 0)

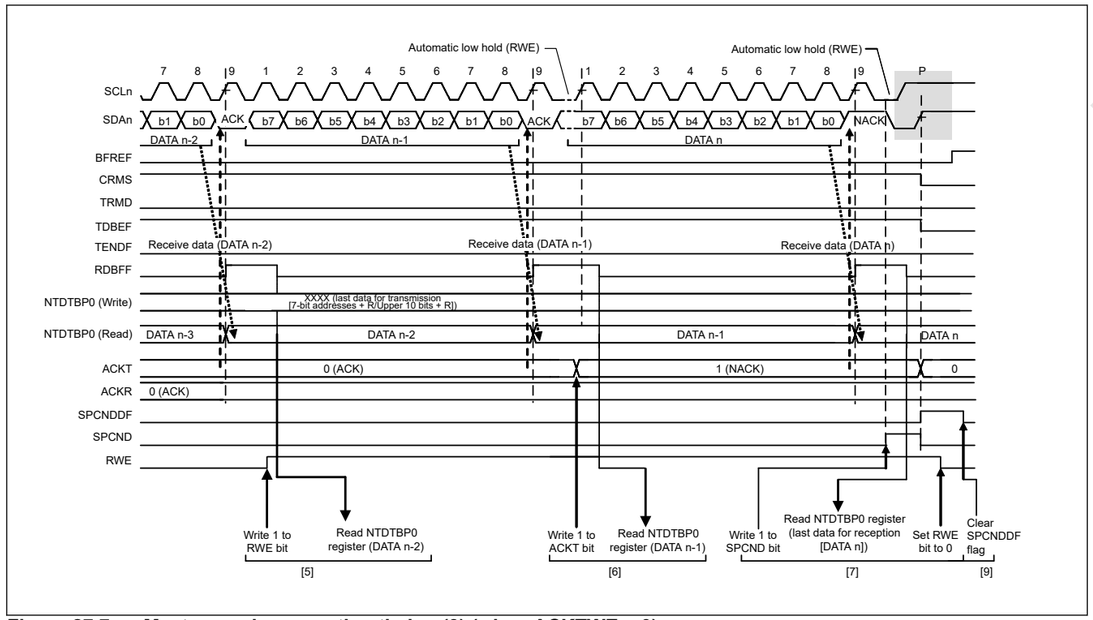


Figure 27.7 Master receive operation timing (3) (when ACKTWE = 0)

27.3.1.1.2 Slave Mode Operation

(1) I²C Slave Operation

(a) Data Write Transfer (Single Buffer transfer)

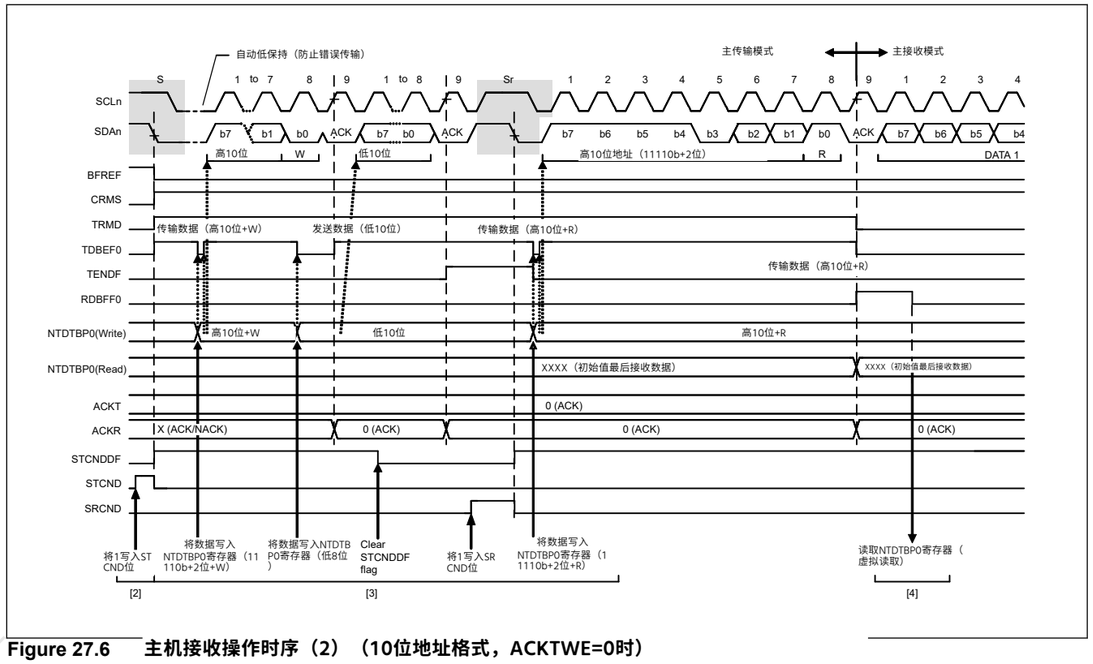


Figure 27.6 主机接收操作时序（2）（10位地址格式，ACKTWE=0时）

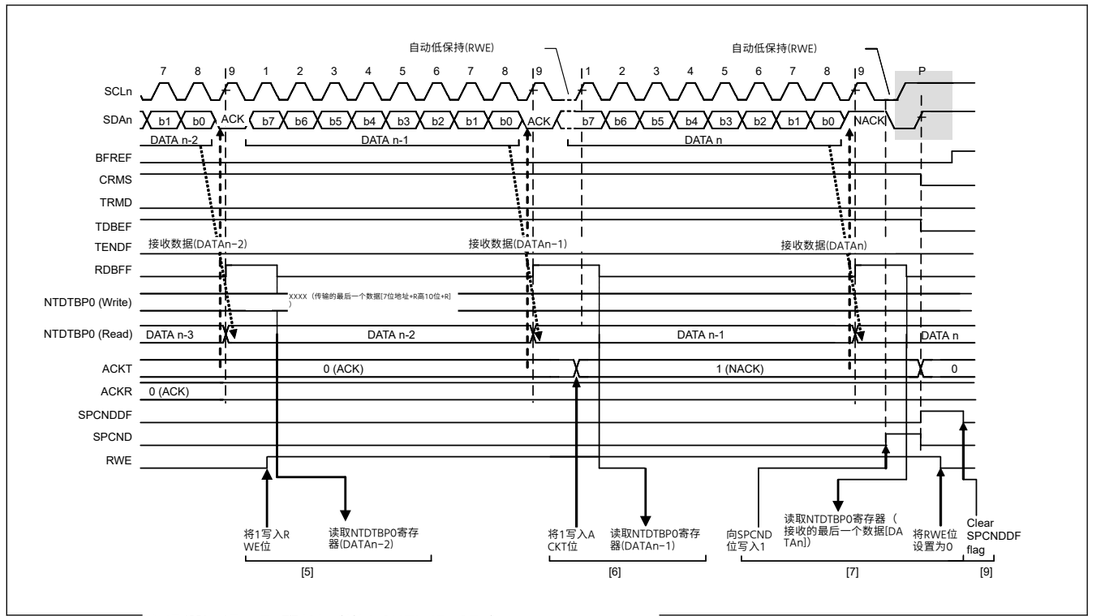


Figure 27.7 主机接收操作时序(3)（当ACKTWE=0时）

27.3.1.1.2 从模式操作

(1) 我2C从操作

(a)数据写入传输（单缓冲区传输）

In slave receive operation, the master device outputs the SCL clock and transmit data, and IIC returns acknowledgments as a slave device.

Figure 27.51 shows an example of usage of slave reception and Figure 1.41 and Figure 1.42 show the timing of operations in slave reception.

The following describes the procedure and operations for slave reception.

1. Initial settings. For details, see section 27.3.2.1. Initial Setting Flow. After initial settings, IIC will stay in the standby state until it receives a slave address that it matches.
2. After receiving a matching slave address, IIC sets one of the corresponding bits SVST.HOAF, GCAF, and SVAFy (y = 0 to 2) to 1 on the rising edge of the ninth cycle of SCL clock (the clock signal) and outputs the acknowledge bit (ACK) on the ninth cycle of SCL clock. If the value of the R/W# bit that was also received at this time is 0, IIC continues to place itself in slave receive mode and sets the NTST.RDBFF0 flag to 1.
3. After the BST.SPCNDDF flag is confirmed to be 0 and the NTST.RDBFF0 flag to be 1, dummy read the NTDTBP0 register (the dummy value consists of the slave address and R/W# bit when the 7-bit address format is selected, or the lower 8 bits when the 10-bit address format is selected).
4. When the NTDTBP0 register is read, IIC automatically sets the NTST.RDBFF0 flag to 0. If reading of the NTDTBP0 register is delayed and a next byte is received while the RDBFF0 flag is still set to 1, IIC holds the SCLn line low from one SCL cycle before the timing with which RDBFF0 should be set. In this case, reading the NTDTBP0 register releases the SCLn line from being held at the low level. When the BST.SPCNDDF flag = 1 and the NTST.RDBFF0 flag is also 1, read the NTDTBP0 register until all the data is completely received.
5. Upon detecting the STOP condition, IIC automatically clears bits SVST.HOAF, GCAF, and SVAFy (y = 0 to 2) to 0.
6. After checking that the BST.SPCNDDF flag = 1, set the BST.SPCNDDF flag to 0 for the next transfer operation.

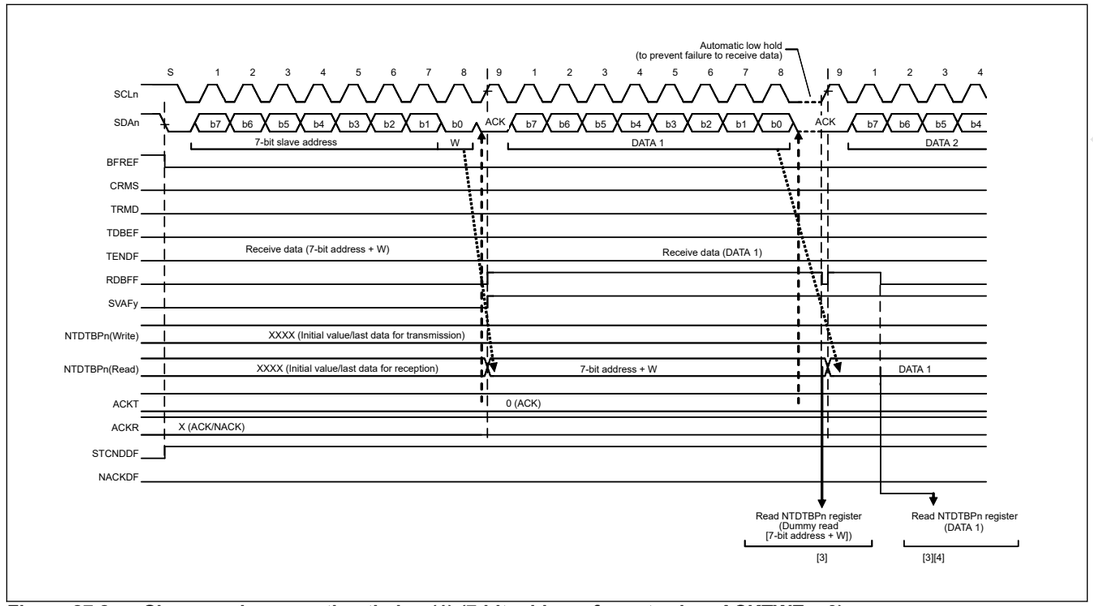


Figure 27.8 Slave receive operation timing (1) (7-bit address format, when ACKTWE = 0)

在从机接收操作中，主设备输出SCL时钟并发送数据，IIC作为从设备返回确认。

图27.51显示了从机接收的使用示例，图1.41和图1.42显示了从机接收中的操作时序。

下面描述从属接收的步骤和操作。

1.初始设置。详见27.3.2.1节。初始设定流程。初始设置后，IIC将保持待机状态，直到收到匹配的从地址。

2.接收到匹配的从机地址后，IIC在SCL时钟（时钟信号）的第9个周期的上升沿将相应的位SVST.HOAF、GCAF和SVAFy（y=0到2）之一设置为1，并且在SCL时钟的第9个周期输出确认位(ACK)。如果此时也接收到的RW#位的值为0，则IIC继续将自身置于从接收模式并将NTST.RDBFF0标志设置为1。

3、确认BST.SPCNDDF标志为0，NTST.RDBFF0标志为1后，虚拟读取NTDTBP0寄存器（选择7位地址格式时，虚拟值由从机地址和RW#位组成，或选择10位地址格式时的低8位）。

4.读取NTDTBP0寄存器时，IIC自动将NTST.RDBFF0标志设置为0。如果读取NTDTBP0寄存器延迟并且在RDBFF0标志仍设置为1时接收到下一个字节，IIC将SCLn线保持为低电平从应该设置RDBFF0的时序之前的一个SCL周期开始。在这种情况下，读取NTDTBP0寄存器会解除SCLn线保持在低电平的状态。当BST.SPCNDDF标志=1且NTST.RDBFF0标志也为1时，读取NTDTBP0寄存器，直到所有数据都接收完毕。

5.检测到STOP条件后，IIC自动将位SVST.HOAF、GCAF和SVAFy（y=0至2）清零。

6.检查BST.SPNCDDF标志=1后，将BST.SPCNDDF标志设置为0以进行下一次传输操作。

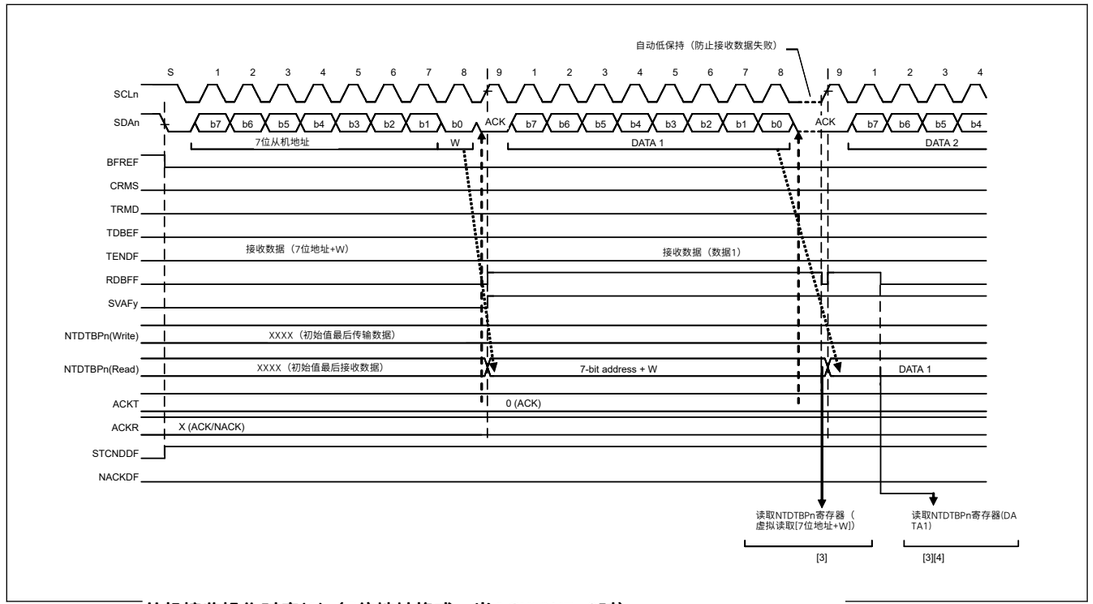


Figure 27.8 从机接收操作时序(1)（7位地址格式，当ACKTWE=0时）

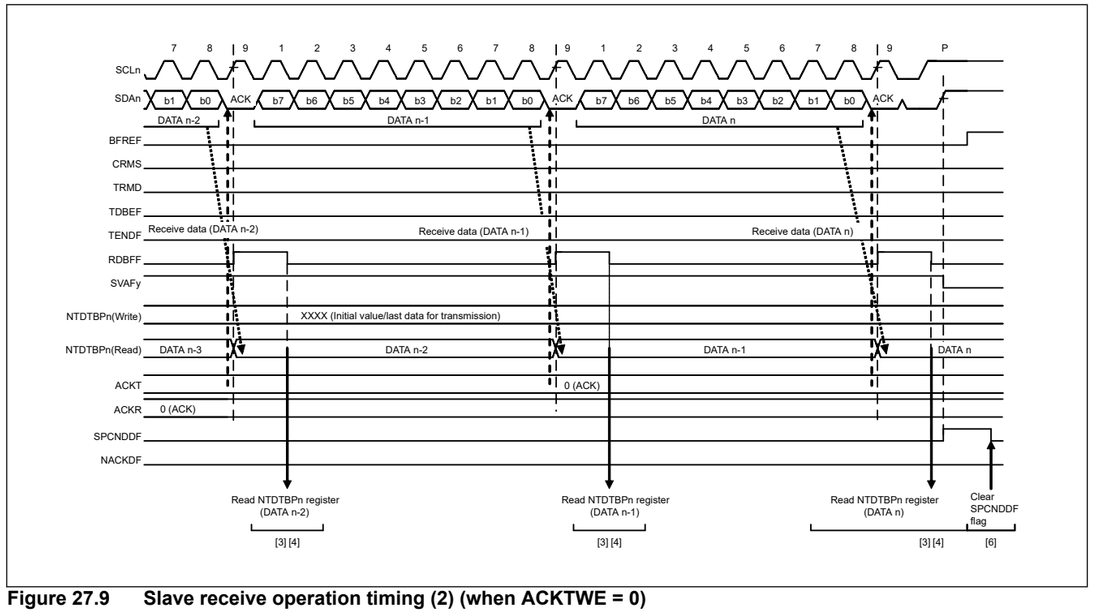


Figure 27.9 Slave receive operation timing (2) (when ACKTWE = 0)

(b) Data Read Transfer (Single Buffer transfer)

In slave transmit operation, the master device outputs the SCL clock, IIC transmits data as a slave device, and the master device returns acknowledgments.

Figure 27.50 shows an example of usage of slave transmission and Figure 27.10 and Figure 27.11 show the timing of operations in slave transmission.

The following describes the procedure and operations for slave transmission.

1. Initial settings. For details, see section 27.3.2.1. Initial Setting Flow.
   After initial settings, IIC will stay in the standby state until it receives a slave address that it matches.
2. After receiving a matching slave address, IIC sets one of the corresponding bits SVST.HOAF, GCAF, and SVAFy (y = 0 to 2) to 1 on the rising edge of the ninth cycle of SCL clock (the clock signal) and outputs the acknowledge bit (ACK) on the ninth cycle of SCL clock. If the value of the R/W# bit that was also received at this time is 1, IIC automatically places itself in slave transmit mode by setting both the PRSST.TRMD bit and the NTST.TDBEF0 flag to 1.
3. After the NTST.TDBEF0 flag is confirmed to be 1, write the data for transmission to the NTDTBP0 register. At this time, if IIC does not receive acknowledge from the master device (receives an NACK signal) while the BSTE.NACKDE bit = 1, IIC aborts transfer of the next data.
4. Wait until the following (a) or (b) condition.
   (a) The BST.NACKDF flag is set to 1.
   (b) The BST.TENDF flag is set to 1 while the NTST.TDBEF0 flag = 1, after the last byte for transmission is written to the NTDTBP0 register.

   When the BST.NACKDF flag or the TENDF flag = 1, IIC drives the SCLn line low on the ninth falling edge of SCL clock.
5. When the BST.NACKDF flag or the BST.TENDF flag = 1, dummy read the NTDTBP0 register to complete the processing. This releases the SCLn line.
6. Upon detecting the STOP condition, IIC automatically sets bits SVST.HOAF, GCAF, and SVAFy (y = 0 to 2), flags NTST.TDBEF0 and BST.TENDF, and the PRSST.TRMD bit to 0, and enters slave receive mode.
7. After checking that the BST.SPCNDDF flag = 1, set the BST.NACKDF and SPCNDDF flags to 0 for the next transfer operation.

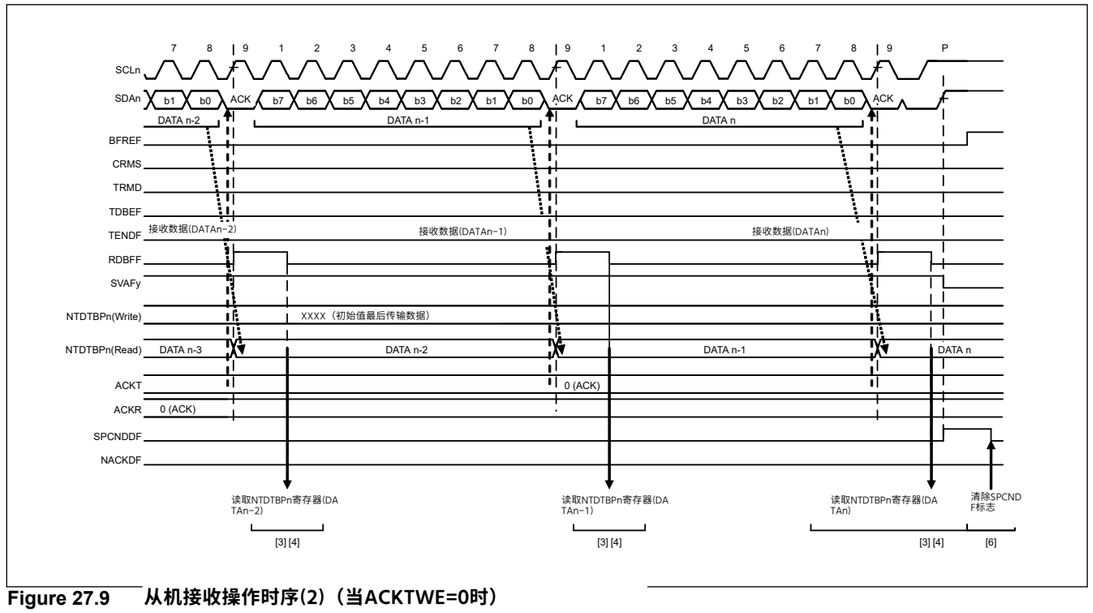


Figure 27.9 从机接收操作时序(2)（当ACKTWE=0时）

(b)数据读取传输（单缓冲区传输）

在从发送操作中，主设备输出SCL时钟，IIC作为从设备发送数据，主设备返回确认。

图27.50显示了从属传输的使用示例，图27.10和图27.11显示了从属传输中的操作时序。

下面介绍从属传输的步骤和操作。

1.初始设置。详见27.3.2.1节。初始设定流程。
初始设置后，IIC将保持待机状态，直到收到匹配的从地址。

2.接收到匹配的从机地址后，IIC在SCL时钟（时钟信号）的第9个周期的上升沿将相应的位SVST.HOAF、GCAF和SVAFy（y=0到2）之一设置为1，并且在SCL时钟的第9个周期输出确认位(ACK)。如果此时也接收到的RW#位的值为1，IIC通过将PRSST.TRMD位和NTST.TDBEF0标志都设置为1自动将自身置于从发送模式。

3.确认NTST.TDBEF0标志为1后，将要发送的数据写入NTDTBP0寄存器。在这
时间，如果IIC在BSTE.NACKDE位=1时没有收到来自主设备的确认（接收到NACK信号），则IIC中止下一个数据的传输。

4.等到以下(a)或(b)条件。

(a) BST.NACKDF标志设置为1。

(b) 在将要发送的最后一个字节写入NTDTBP0寄存器后，BST.TENDF标志设置为1，而NTST.TDBEF0标志=1。

当BST.NACKDF标志或TENDF标志=1时，IIC在SCL时钟的第九个下降沿将SCLn线驱动为低电平。

5.当BST.NACKDF标志或BST.TENDF标志=1时，虚拟读取NTDTBP0寄存器以完成处理。这将释放SCLn线。

6.检测到STOP条件后，IIC自动设置SVST.HOAF、GCAF和SVAFy位（y=0到2），标志NTST.TDBEF0和BST.TENDF，以及PRSST.TRMD位为0，并进入从机接收模式。

7.检查BST.SPNCDDF标志=1后，将BST.NACKDF和SPCNDDF标志设置为0以进行下一次传输操作。

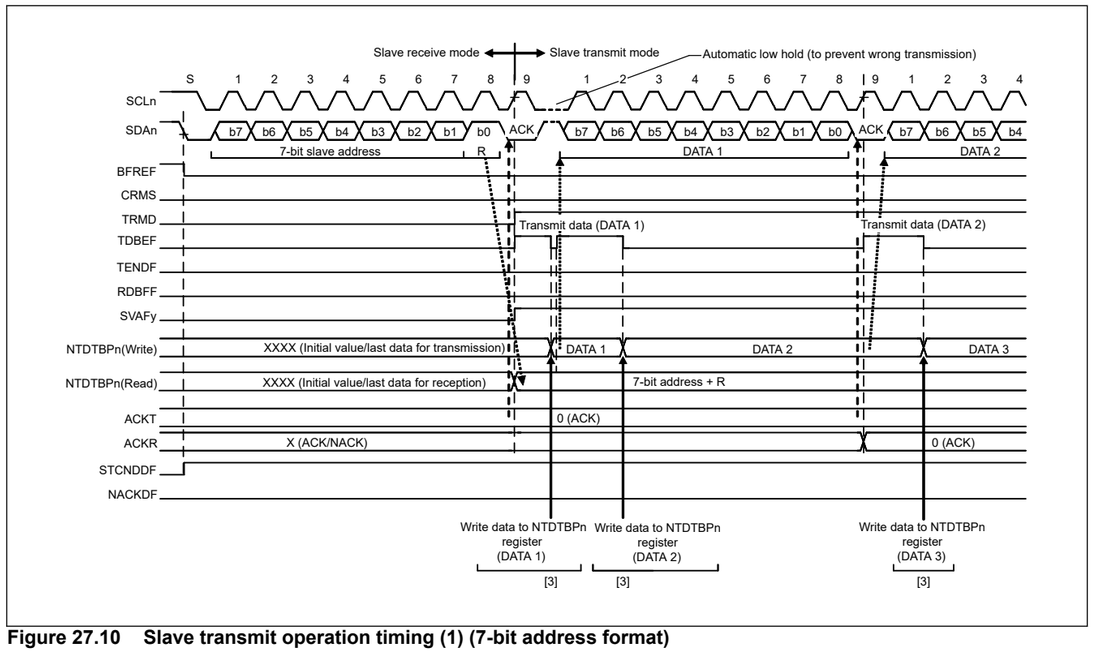


Figure 27.10 Slave transmit operation timing (1) (7-bit address format)

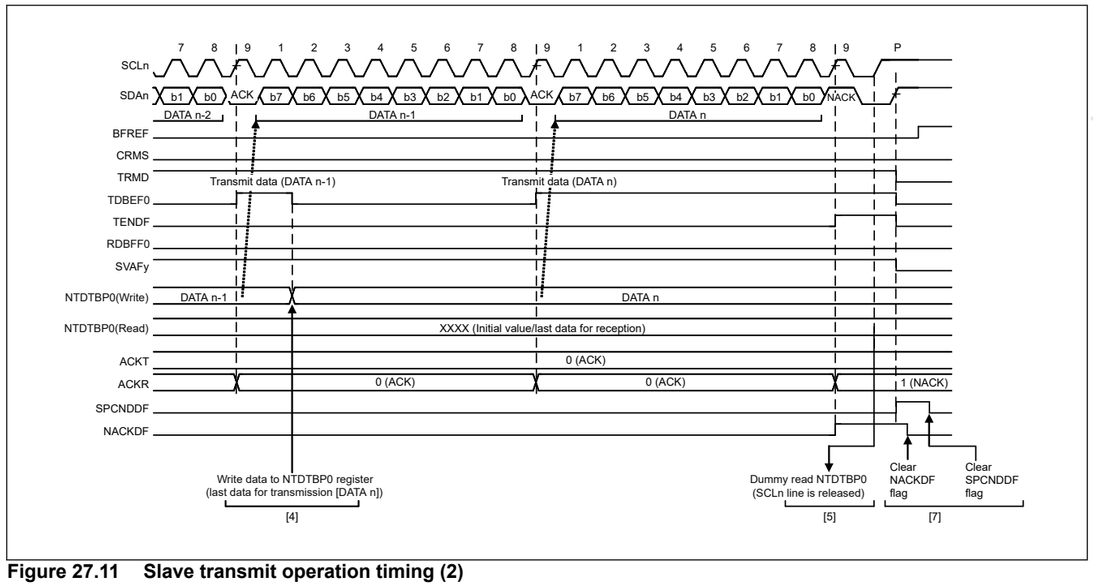


Figure 27.11 Slave transmit operation timing (2)

27.3.1.2 Data Handler

The relationship between the transfer method and the queue is shown in Table 27.8.

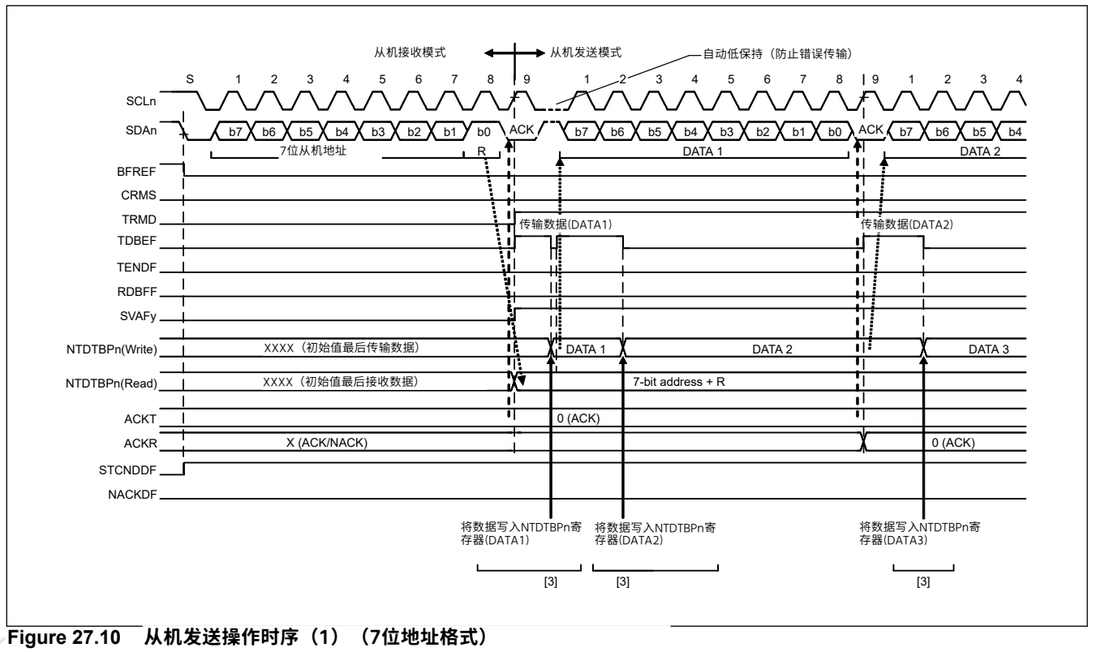


Figure 27.10 从机发送操作时序（1）（7位地址格式）

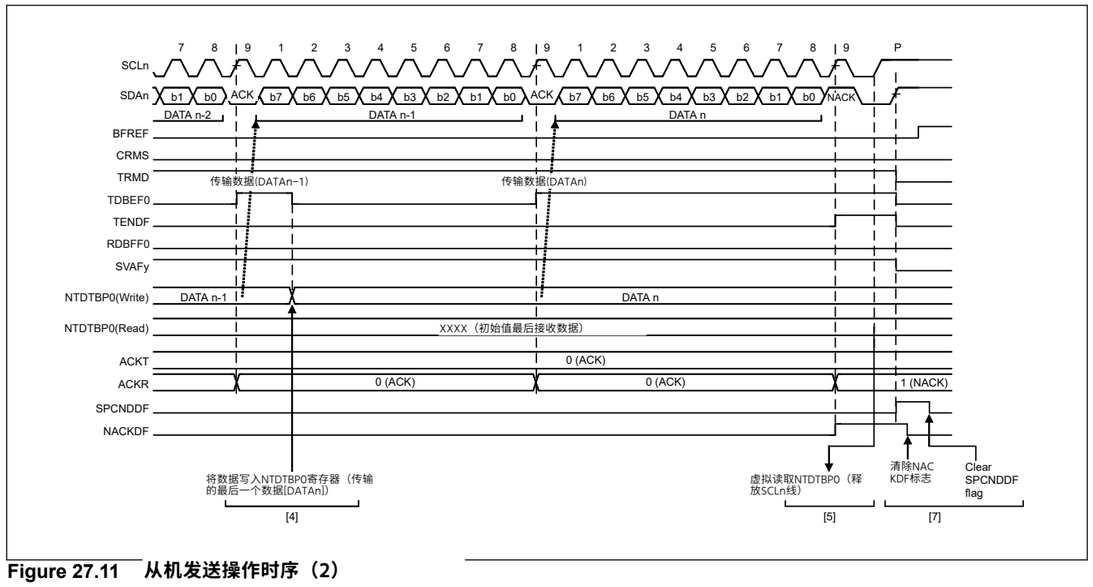


Figure 27.11 从机发送操作时序（2）

27.3.1.2 数据处理程序

传输方式与队列的关系如表27.8所示。

Table 27.8 Transfer method

Transfer method	Buffer	size	Master	Slave
Single buffer transfer	Normal Transmit Data	1 byte	✓	✓
	Normal Receive Data	1 byte	✓	✓

27.3.1.2.1 Transfer Method

(1) Single Buffer transfer

Each process (condition issue, data transfer, ACK / NACK response) is controlled by software.

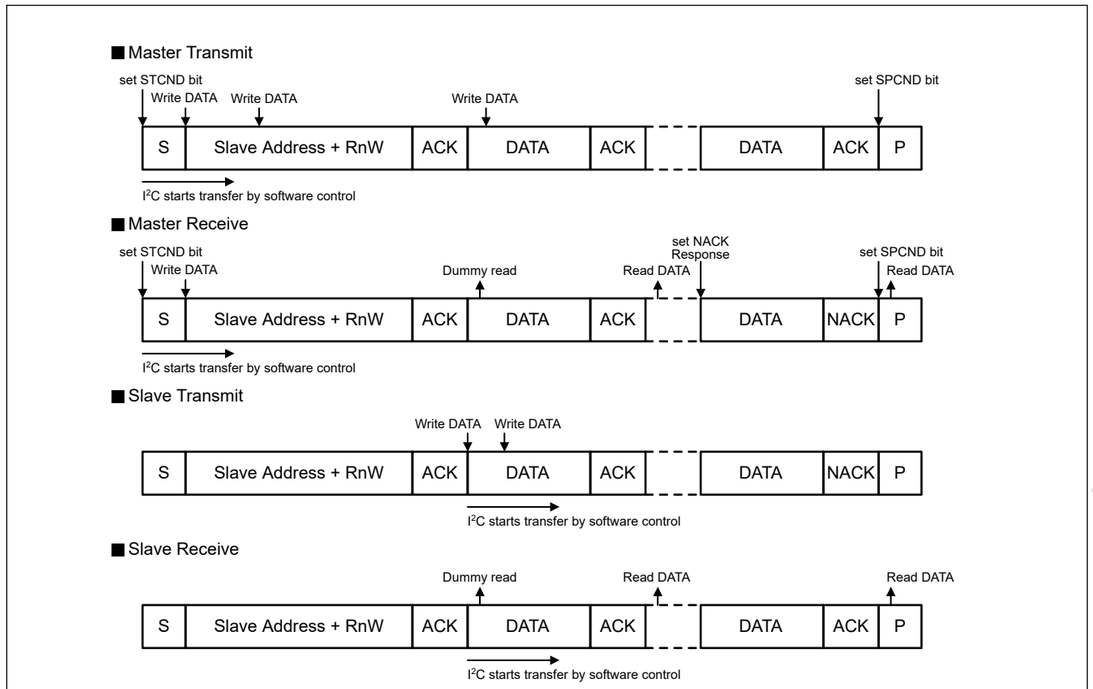


Figure 27.12 Data handler with single buffer transfer

27.3.1.3 I²C Protocol

27.3.1.3.1 Communication Protocol

(1) I²C Communication Data Format

The I²C bus format consists of 8-bit data and 1-bit acknowledge. The frame following a START condition or Repeated START condition is an address frame used to specify a slave device with which the master device communicates. The specified slave is valid until a new slave is specified or a STOP condition is issued.

Figure 27.13 shows the I²C bus format, and Figure 27.14 shows the I²C bus timing.

Table 27.8 转移方式

转移方式	Buffer	size	Master	Slave
单缓冲区传输	正常传输数据	1 byte	✓	✓
	正常接收数据	1 byte	✓	✓

27.3.1.2.1 转移方式

(1) 单缓冲区传输

每个过程（条件发出、数据传输、ACKNACK响应）都由软件控制。

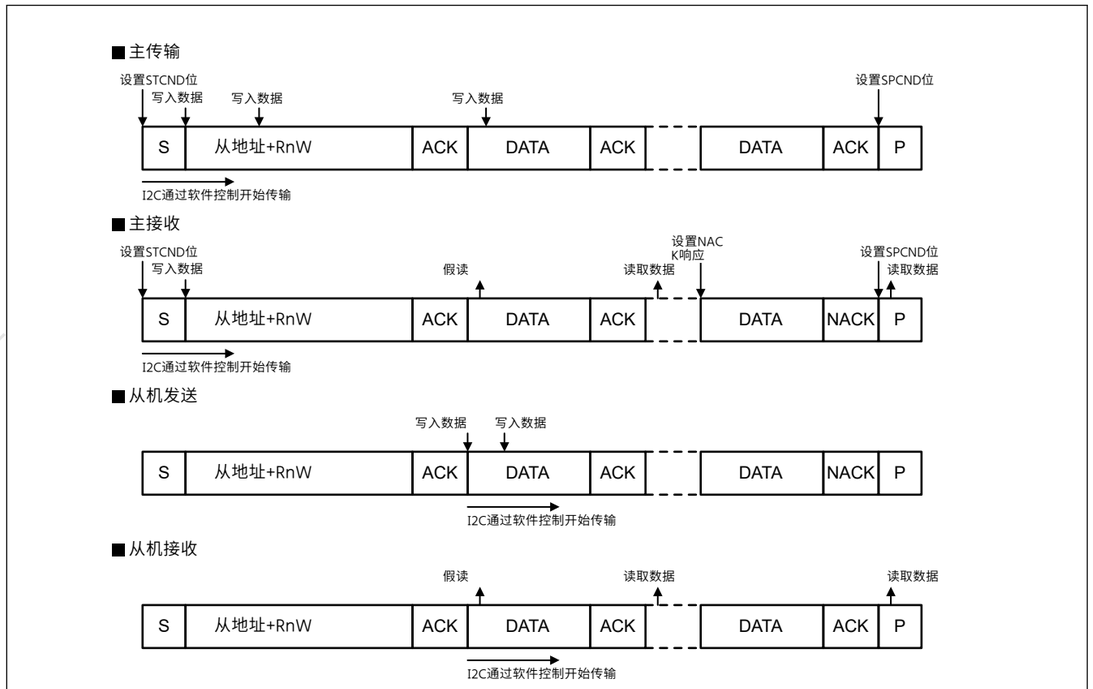


Figure 27.12 具有单缓冲区传输的数据处理程序

27.3.1.3 I²C Protocol

27.3.1.3.1 通讯协议

(1) I2C通信数据格式

I2C总线格式由8位数据和1位确认组成。START条件或重复START条件之后的帧是地址帧，用于指定与主设备通信的从设备。指定的从站一直有效，直到指定新的从站或发出STOP条件。

图27.13显示了I2C总线格式，图27.14显示了I2C总线时序。

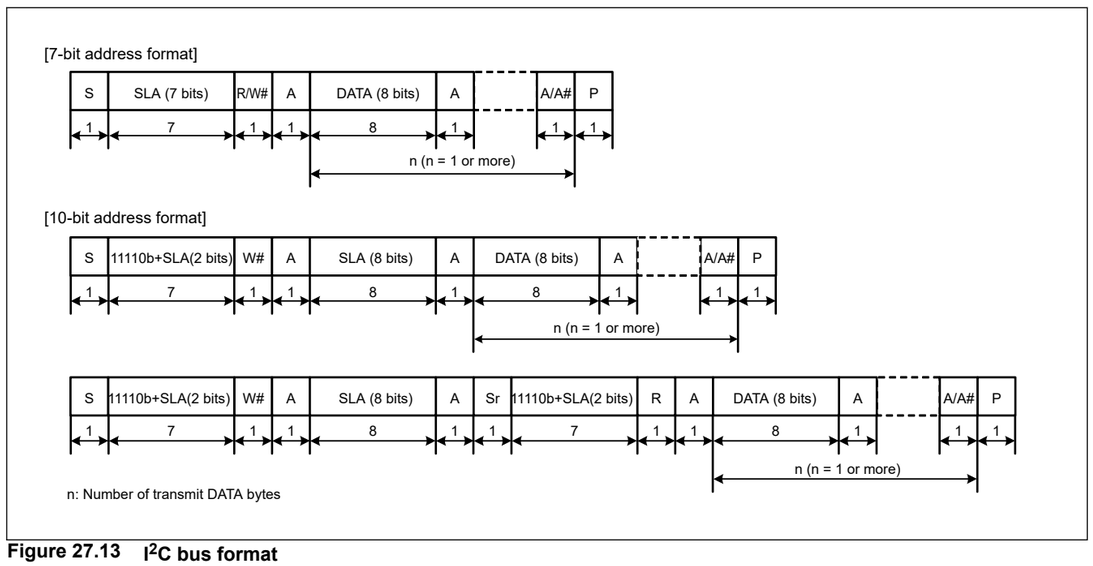


Figure 27.13 I^2C bus format

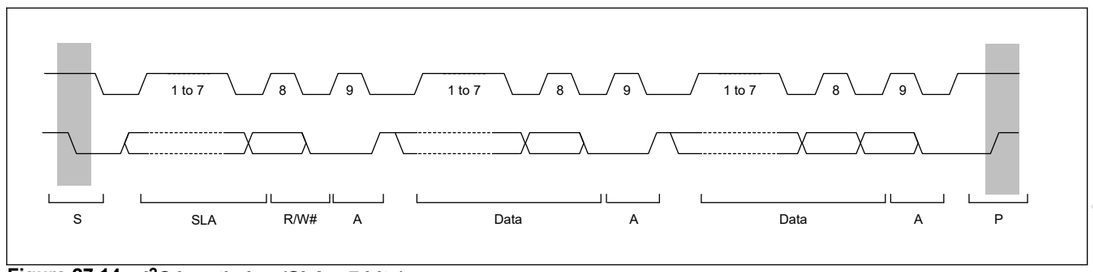


Figure 27.14 I^2C bus timing (SLA = 7 bits)

S: START condition. The master device drives the SDAn line low from high level while the SCLn line is at a high level.

SLA: Slave address, by which the master device selects a slave device.

R/W#: Indicates the direction of data transfer: from the slave device to the master device when R/W = 1, or from the master device to the slave device when R/W = 0.

A: Acknowledge. The receive device drives the SDAn line low. (In master transmit mode, the slave device returns acknowledge. In master receive mode, the master device returns acknowledge.)

A#: Not Acknowledge. The receive device drives the SDAn line high.

Sr: Repeated START condition. The master device drives the SDAn line low from the high level after the setup time has elapsed with the SCLn line at the high level.

DATA: Transmitted or received data

P: STOP condition. The master device drives the SDAn line high from low level while the SCLn line is at a high level.

27.3.1.3.2 START Condition / Repeated START Condition / STOP Condition Issuing Function

(1) Issuing a START Condition

IIC issues a START condition when the CNDCTL.STCND bit is set to 1.

Set the STCND bit to 1 (START condition issuance request) when the BCST.BFREF flag is set to 1 (bus free state).

IIC issues a START condition.

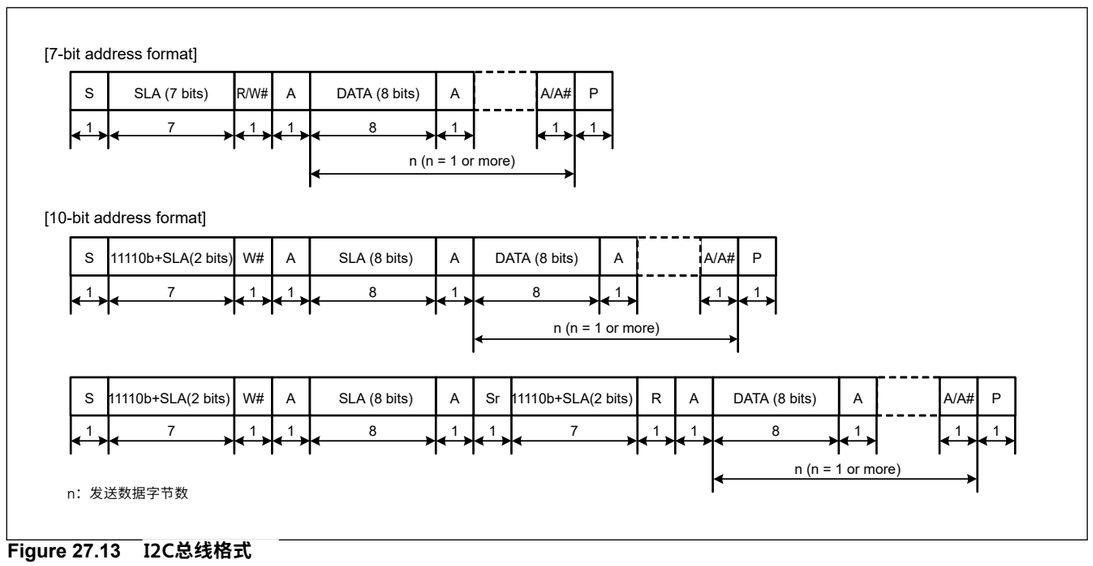


Figure 27.13 I2C总线格式

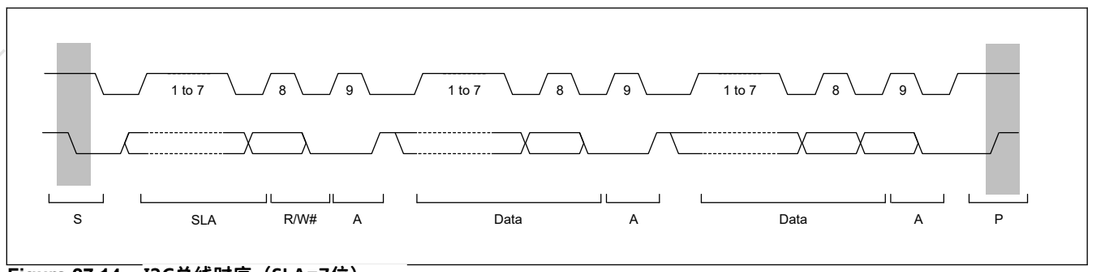


Figure 27.14 I2C总线时序（SLA=7位）

S: 开始条件。主设备将SDAn线从高电平驱动为低电平，而SCLn线处于高电平。

SLA: 从地址，主设备通过该地址选择从设备。

R/W#: 指示数据传输的方向：当RW=1时从从设备到主设备，或者当RW=0时从主设备到从设备。

A: 承认。接收设备将SDAn线驱动为低电平。（在主发送模式下，从设备返回确认。
在主接收模式下，主设备返回确认。）

A#: 不承认。接收设备将SDAn线驱动为高电平。

Sr: 重复启动条件。建立时间过后，主器件将SDAn线从高电平驱动为低电平，SCLn线处于高电平。

DATA: 传输或接收的数据

P: 停止条件。主设备将SDAn线从低电平驱动为高电平，而SCLn线处于高电平。

27.3.1.3.2 START条件重复START条件STOP条件发出 Function

(1) 发出START条件

当CNDCTL.STCND位设置为1时，IIC发出START条件。

当BCST.BFREF标志设置为1（总线空闲状态）时，将STCND位设置为1（开始条件发出请求）。

IIC发出一个START条件。

When a START condition is issued normally, IIC automatically shifts to the master transmit mode. A START condition is issued in the following sequence.

[START condition issuance]

- Drive the SDAn line low (high level to low level).
- Ensure the time set in STDBR.SBRHO[7:0] and the START condition hold time.
- Drive the SCLn line low (high level to low level).
- Detect low level of the SCLn line and ensure the low-level period of SCLn line set in STDBR.SBRLO[7:0].

(2) Issuing a Repeated START Condition

IIC issues a Repeated START condition when the CNDCTL.SRCND bit is set to 1.

When the SRCND bit is set to 1, a Repeated START condition issuance request is made and IIC issues a Repeated START condition when the BCST.BFREF flag = 0 (bus busy state) and the PRSST.CRMS bit = 1 (master mode).

A Repeated START condition is issued in the following sequence.

[Repeated START condition issuance]

- Release the SDAn line.
- Ensure the low-level period of SCLn line set in STDBR.SBRLO[7:0].
- Release the SCLn line (low level to high level).
- Detect a high level of the SCLn line and ensure the time set in STDBR.SBRLO[7:0] and the Repeated START condition setup time.
- Drive the SDAn line low (high level to low level).
- Ensure the time set in STDBR.SBRHO[7:0] and the Repeated START condition hold time.
- Drive the SCLn line low (high level to low level).
- Detect a low level of the SCLn line and ensure the low-level period of SCLn line set in STDBR.SBRLO[7:0].

Note: When issuing Repeated START conditions request, please write the slave address to NTDTBP0 after confirming CNDCTL.SRCND = 0. Data written in the period of CNDCTL.SRCND = 1 is not forwarded because retransmission condition before the occurrence.

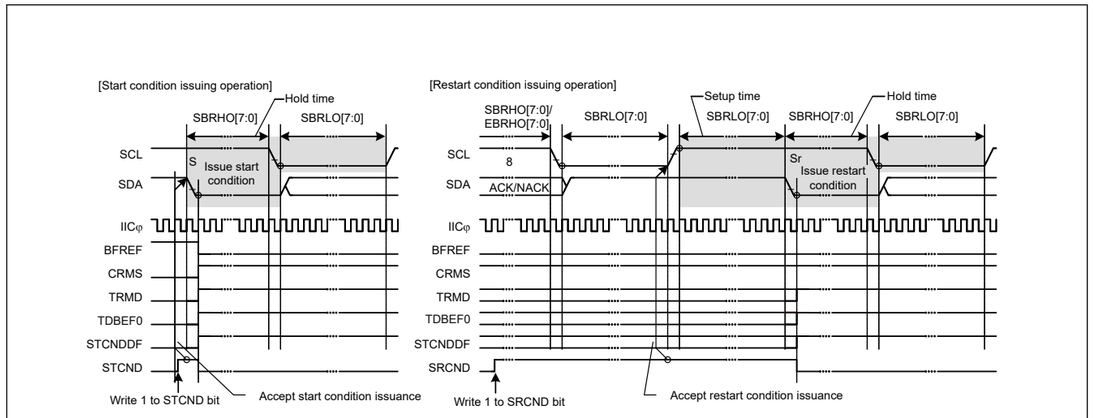


Figure 27.15 START condition / repeated START condition issue timing (STCND and SRCND bits)

Figure 27.16 shows the operation to issue a Repeated START condition after the master transmission.

[Repeated START condition issuance after the master transmission]

- Initial setting. For details, see section 27.3.2.1. Initial Setting Flow.

当START条件正常发出时，IIC自动切换到主机发送模式。START条件按以下顺序发出。

[START condition issuance]

- ●将SDAn线拉低（从高电平到低电平）。
- ●确保STDBR.SBRHO[7:0]中设置的时间和START条件保持时间。
- ●将SCLn线拉低（高电平转低电平）。
- ●检测SCLn线的低电平，保证STDBR.SBRLO[7:0]中设置的SCLn线的低电平周期。

(2) 发出重复的START条件

当CNDCTL.SRCND位设置为1时，IIC发出重复启动条件。

当SRCND位设置为1时，发出重复START条件发出请求，并且IIC在BCST.BFREF标志=0（总线忙状态）和PRSST.CRMS位=1（主机模式）时发出重复START条件。

重复启动条件按以下顺序发出。

[重复START条件发布]

- ●释放SDAn线。
- ●确保STDBR.SBRLO[7:0]中设置的SCLn线的低电平周期。
- ●释放SCLn线（低电平到高电平）。
- ●检测SCLn线的高电平，确保STDBR.SBRLO[7:0]中设置的时间和RepeatedSTART条件建立时间。
- ●将SDAn线拉低（从高电平到低电平）。
- ●确保STDBR.SBRHO[7:0]中设置的时间和RepeatedSTART条件保持时间。
- ●将SCLn线拉低（高电平转低电平）。
- ●检测SCLn线的低电平，保证STDBR.SBRLO[7:0]中设置的SCLn线的低电平周期。

Note: 发出重复启动条件请求时，请在确认后将从机地址写入NTDTBP0 CNDCTL.SRCND=0。在CNDCTL.SRCND=1期间写入的数据不转发，因为发生之前的重传条件。

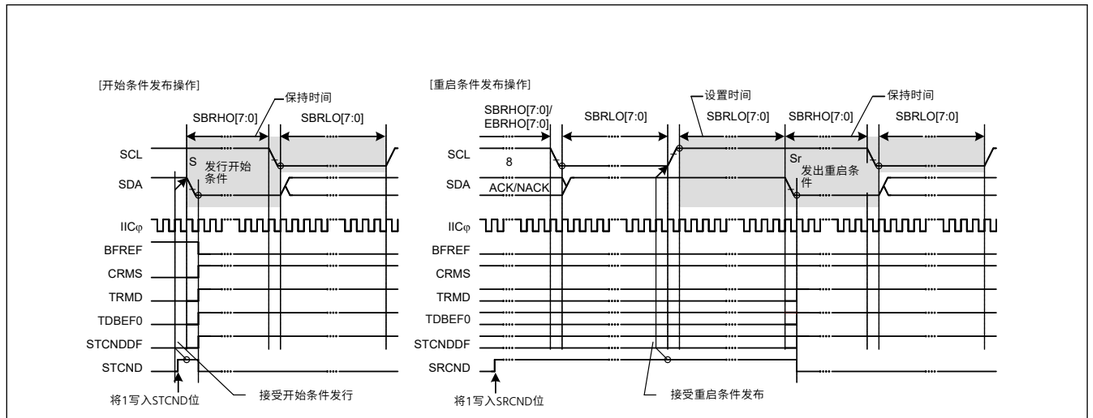


Figure 27.15 START条件重复START条件发出时序（STCND和SRCND位）

图27.16显示了在主机发送后发出重复启动条件的操作。

[主传输后重复START条件发布]

- ●初始设置。详见27.3.2.1节。初始设定流程。

- Read the BFREF flag in BCST to check that the bus is open, and then set the STCND bit in CNDCTL to 1 (START condition issuance request). Upon receiving the request, IIC issues a START condition. At the same time, the BFREF flag is automatically set to 0 and the STCNDDF flag in BST is automatically set to 1 and the STCND bit is automatically set to 0. At this time, if the START condition is detected and the internal levels for the SDA output state and the levels on the SDAn line have matched while the STCND bit = 1, IIC recognizes that issuing of the START condition as requested by the STCND bit has been successfully completed, and CRMS and TRMD bits in PRSST is automatically set to 1, placing IIC in master transmit mode. The NTST.TDBEF0 flag is also automatically set to 1 in response to setting of the TRMD bit to 1.
- Check that the NTST.TDBEF0 flag = 1, and then write the value for transmission (the slave address and the R/W# bit) to NTDTBP0. Once the data for transmission are written to NTDTBP0, the TDBEF0 flag is automatically set to 0, the data are transferred from NTDTBP0, and the TDBEF0 flag is again set to 1. After the byte containing the slave address and R/W# bit has been transmitted, the value of the TRMD bit is automatically updated to select master transmit or master receive mode in accord with the value of the transmitted R/W# bit. If the value of the R/W# bit was 0, IIC continues in master transmit mode. Since the BST.NACKDF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to CNDCTL.SPCND bit to issue a STOP condition. For data transmission with an address in the 10-bit format, start by writing 1111 0, the 2 higher-order bits of the slave address, and W to NTDTBP0 as the first address transmission. Then, as the second address transmission, write the 8 lower-order bits of the slave address to NTDTBP0.
- After confirming that the NTST.TDBEF0 flag = 1, write the data for transmission to the NTDTBP0 register. IIC automatically holds the SCLn line low until the data for transmission are ready, a Repeated START condition is issued or a STOP condition is issued.
- After all bytes of data for transmission have been written to the NTDTBP0 register, wait until the value of the BST.TENDF flag returns to 1, and then, after check that the BST.STCNDDF flag = 1, set the BST.STCNDDF flag to 0.
- Set the SRCND bit in CNDCTL to 1 (Repeated START condition issuance request). Upon receiving the request, IIC issues a Repeated START condition.
- After check that the BST.STCNDDF flag = 1, write the value for transmission (the slave address and the R/W# bit) to NTDTBP0.

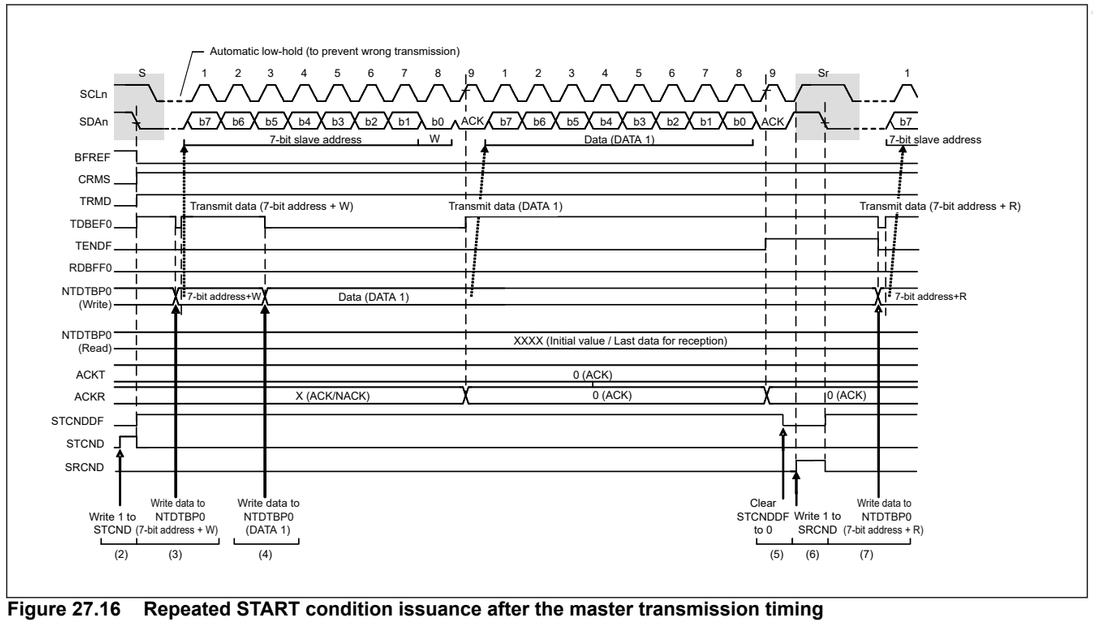


Figure 27.16 Repeated START condition issuance after the master transmission timing

(3) Issuing a STOP Condition

IIC issues a STOP condition when the SPCND bit in CNDCTL is set to 1.

●读取BCST中的BFREF标志以检查总线是否打开，然后将CNDCTL中的STCND位设置为1（START条件发出请求）。收到请求后，IIC发出START条件。同时，BFREF标志位自动置0，BST中的STCNDDF标志位自动置1，STCND位自动置0。此时，如果检测到START条件且内部电平为SDA输出状态和SDAn线上的电平匹配，当STCND位=1时，IIC识别出由STCND位请求的START条件的发布已成功完成，并且PRSST中的CRMS和TRMD位自动设置为1，将IIC置于主发送模式。响应TRMD位设置为1，NTST.TDBEF0标志也自动设置为1。

●检查NTST.TDBEF0标志=1，然后将传输值（从机地址和RW#位）写入NTDTBP0。一旦将要发送的数据写入NTDTBP0，TDBEF0标志自动设置为0，数据从NTDTBP0传输，并且TDBEF0标志再次设置为1。在包含从机地址和RW#位的字节被发送后时，TRMD位的值会自动更新，以根据发送的RW#位的值选择主机发送或主机接收模式。如果RW#位的值为0，IIC继续在主机发送模式。由于此时BST.NACKDF标志为1表示没有从设备识别该地址或通信出现错误，因此向CNDCTL.SPCND位写入1以发出STOP条件。对于地址为10位格式的数据传输，首先将11110、从机地址的高2位和W写入NTDTBP0作为第一个地址传输。然后，作为第二次地址传输，将从机地址的低8位写入NTDTBP0。

●确认NTST.TDBEF0标志=1后，将发送数据写入NTDTBP0寄存器。国际集成电路
自动将SCLn线保持为低电平，直到传输数据准备好、发出重复START条件或发出STOP条件。

●待发送数据的所有字节写入NTDTBP0寄存器后，等待
BST.TENDF标志返回1，然后在检查BST.STCNDDF标志=1后，将BST.STCNDDF标志设置为0。

●将CNDCTL中的SRCND位设置为1（重复START条件发出请求）。收到请求后，IIC发出重复启动条件。

●检查BST.STCNDDF标志=1后，将发送值（从机地址和RW#位）写入NTDTBP0。

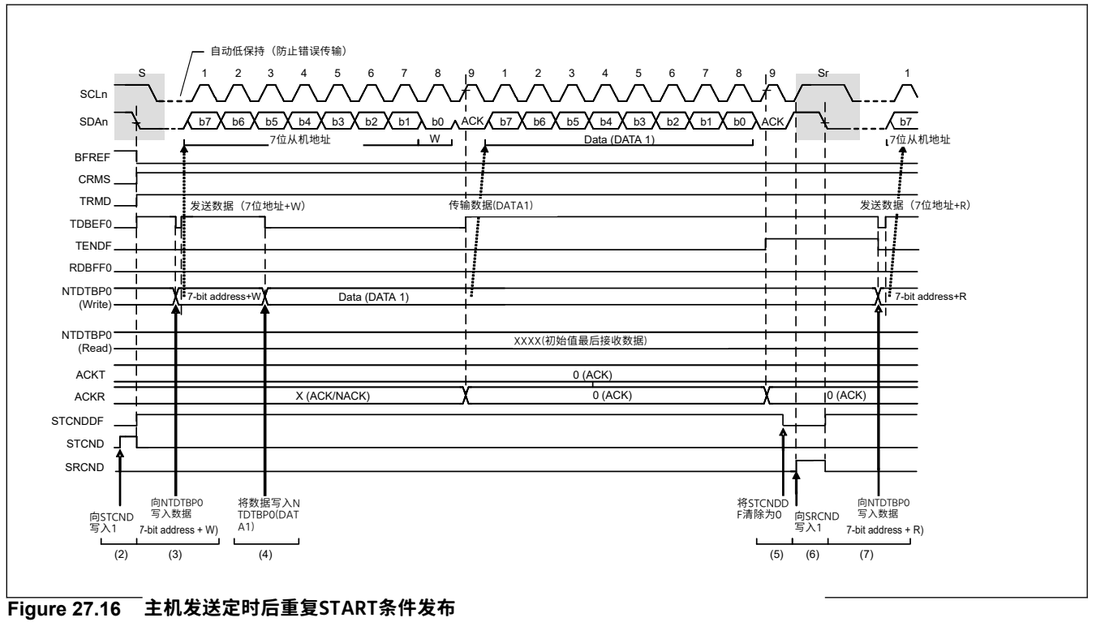


Figure 27.16 主机发送定时后重复START条件发布

(3) 发出停止条件

当CNDCTL中的SPCND位设置为1时，IIC发出STOP条件。

When the SPCND bit is set to 1, a STOP condition issuance request is made and IIC issues a STOP condition when the BCST.BFREF flag = 0 (bus busy state) and the PRSST.MST bit = 1 (master mode).

A STOP condition is issued in the following sequence.

[STOP condition issuance]

- Drive the SDAn line low (high level to low level).
- Ensure the low-level period of SCLn line set in STDBR.SBRLO[7:0].
- Release the SCLn line (low level to high level).
- Detect a high level of the SCLn line and ensure the time set in STDBR.SBRHO[7:0] and the STOP condition setup time.
- Release the SDAn line (low level to high level).
- Ensure the time set in STDBR.SBRLO[7:0] and the bus free time.
- Set the BFREF flag to 1 (to release the bus mastership).

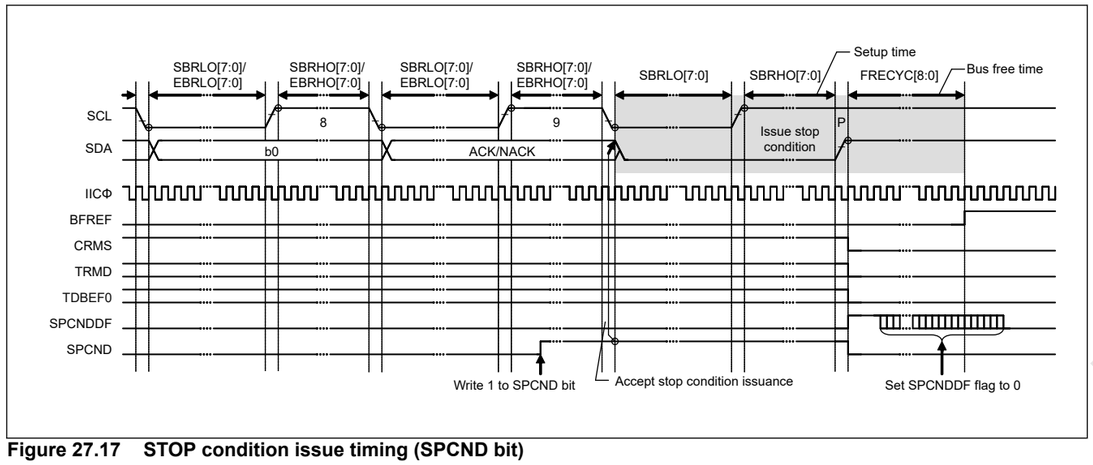


Figure 27.17 STOP condition issue timing (SPCND bit)

27.3.1.3.3 Address Match Detection

IIC can set three unique slave addresses in addition to the general call address and host address, and also can set 7- bit or 10-bit slave addresses.

(1) Slave-Address Match Detection

IIC can set three unique slave addresses, and has a slave address detection function for each unique slave address.

When the SVCTL.SVAEy bit (y = 0 to 2) is set to 1, the slave addresses set in the SVDVADy register (y = 0 to 2) can be detected.

When IIC detects a match of the set slave address, the corresponding SVST.SVAFy flag (y = 0 to 2) is set to 1 at the rising edge of the ninth SCL clock cycle, and the NTST.RDBFF0 flag or the NTST.TDBEF0 flag is set to 1 by the following R/W# bit. This causes a receive data full interrupt (IICn_RX) or transmit data empty interrupt (IICn_TX) to be generated. The SVAFy flag is used to identify which slave address has been specified.

Figure 27.18 to Figure 27.20 show the SVAFy flag set timing in three cases.

当SPCND位设置为1时，发出STOP条件发出请求，当IIC发出STOP条件时BCST.BFREF标志=0（总线繁忙状态）和PRSST.MST位=1（主模式）。

STOP条件按以下顺序发出。

[STOP condition issuance]

●将SDAn线拉低（从高电平到低电平）。

●确保STDBR.SBRLO[7:0]中设置的SCLn线的低电平周期。

●释放SCLn线（低电平到高电平）。

●检测SCLn线的高电平，确保STDBR.SBRHO[7:0]中设置的时间和STOP条件建立时间。

●释放SDAn线（低电平到高电平）。

●确保STDBR.SBRLO[7:0]中设置的时间和总线空闲时间。

●将BFREF标志设置为1（以释放总线控制权）。

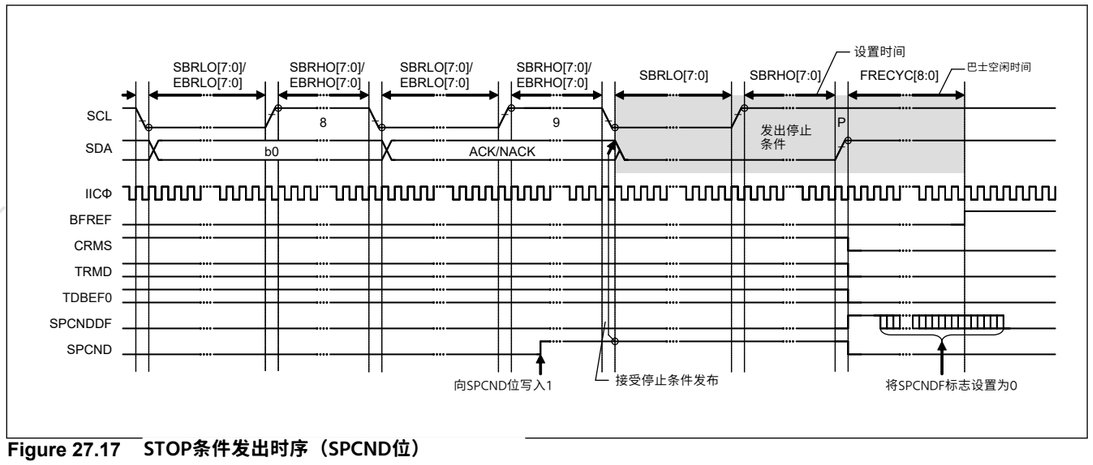


Figure 27.17 STOP条件发出时序（SPCND位）

27.3.1.3.3 地址匹配检测

IIC除了可以设置广播地址和主机地址外，还可以设置三个唯一的从机地址，也可以设置7bit或10bit的从机地址。

(1) 从地址匹配检测

IIC可以设置三个唯一的从地址，并且对每个唯一的从地址都有从地址检测功能。

当SVCTL.SVAEy位（y=0到2）设置为1时，可以检测SVDVADy寄存器（y=0到2）中设置的从机地址。

当IIC检测到设置的从地址匹配时，对应的SVST.SVAFy标志（y=0到2）在第9个SCL时钟周期的上升沿设置为1，并且NTST.RDBFF0标志或NTST.TDBEF0flag由后面的RW#位设置为1。这会导致产生接收数据满中断(IICn_RX)或发送数据空中断(IICn_TX)。

SVAFy标志用于标识已指定哪个从地址。

图27.18至图27.20显示了三种情况下的SVAFy标志设置时序。

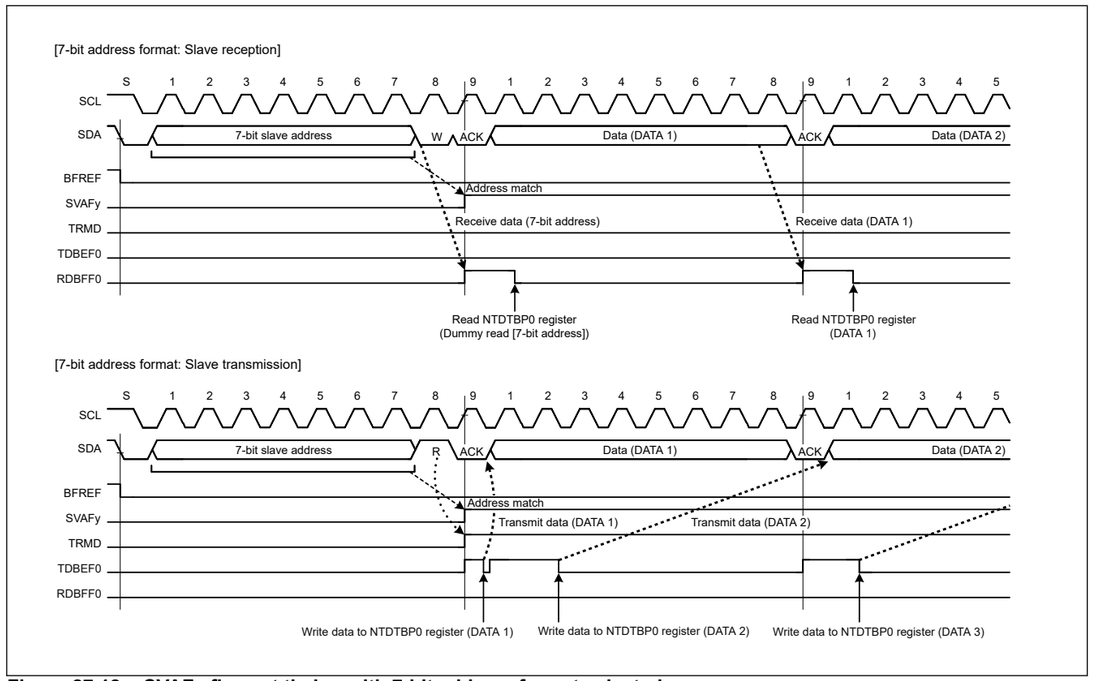


Figure 27.18 SVAFy flag set timing with 7-bit address format selected

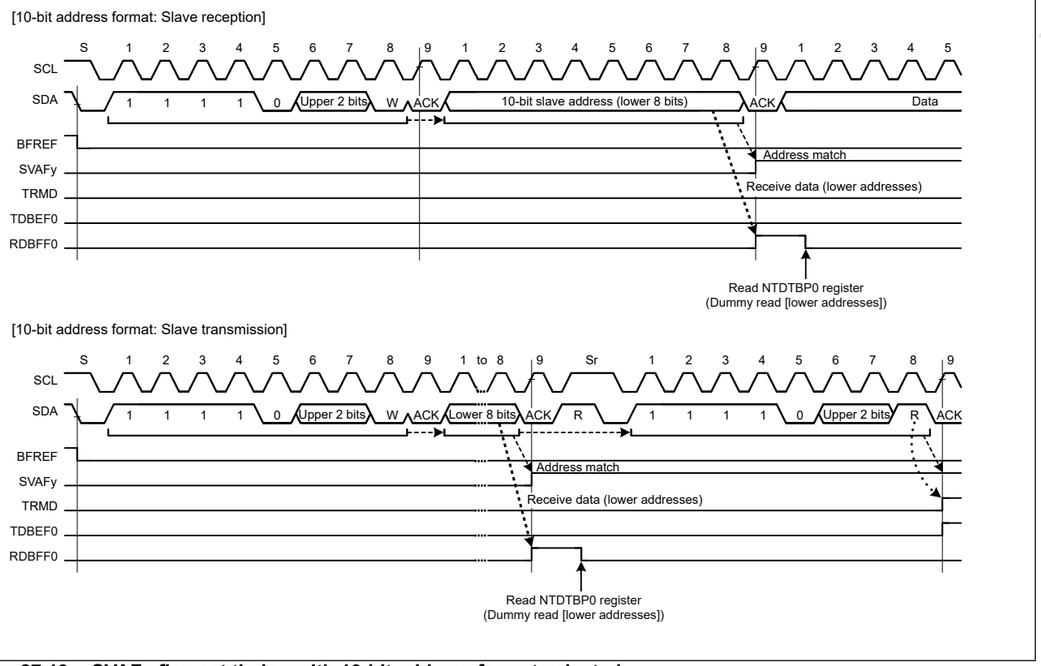


Figure 27.19 SVAFy flag set timing with 10-bit address format selected

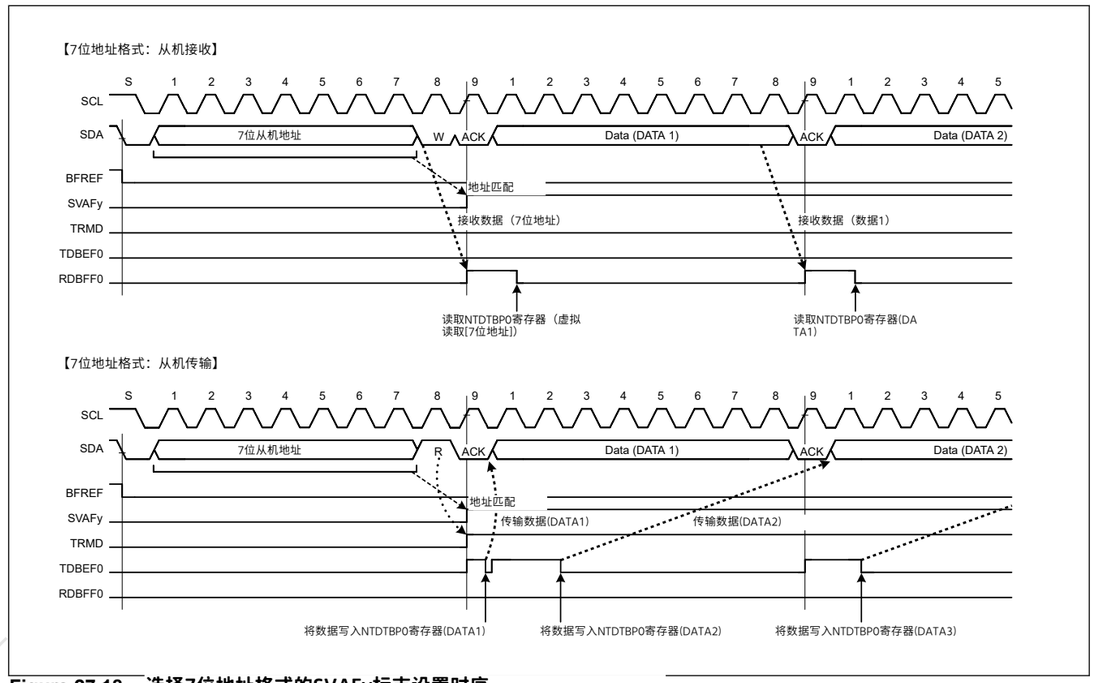


Figure 27.18 选择7位地址格式的SVAFy标志设置时序

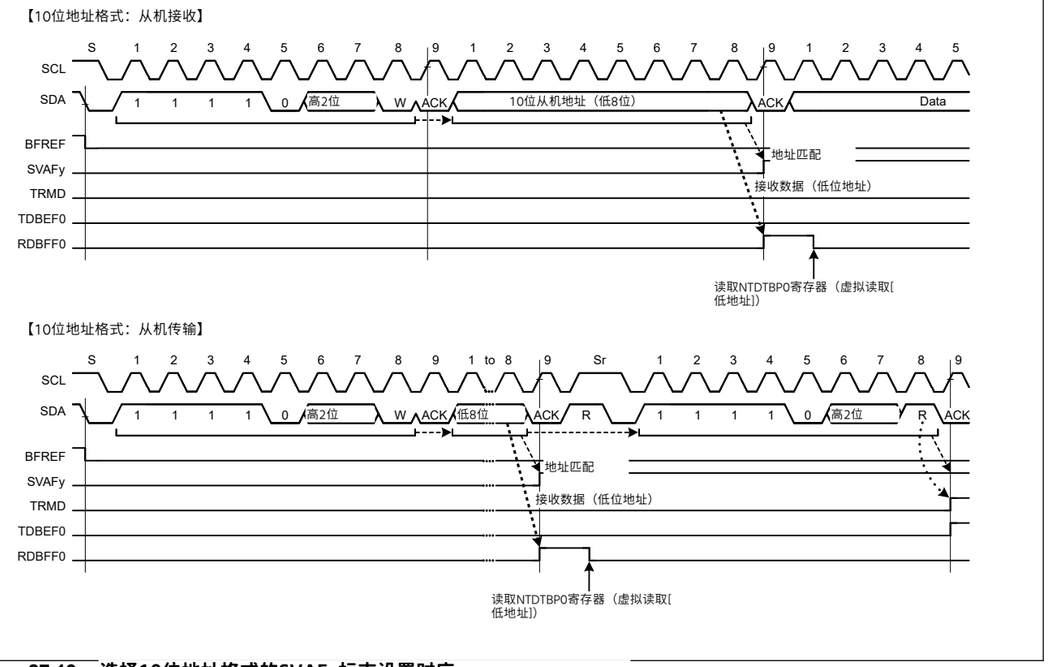


Figure 27.19 选择10位地址格式的SVAFy标志设置时序

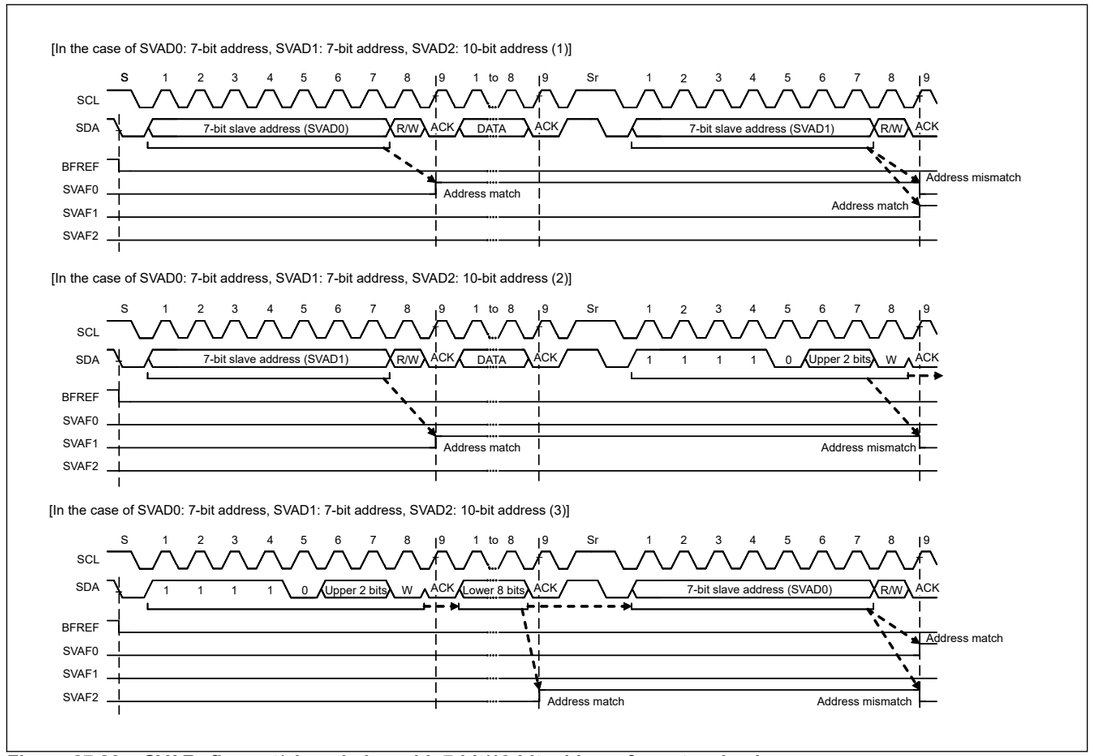


Figure 27.20 SVAFy flag set/clear timing with 7-bit/10-bit address formats mixed

(2) Detection of the General Call Address

IIC has a facility for detecting the general call address (0000 000 + 0 (write)). This is enabled by setting the SVCTL.GCAE bit to 1.

If the address received after a START or Repeated START condition is issued is 0000 000 + 1 (read) (start byte), IIC recognizes this as the address of a slave device with an all-zero address but not as the general call address.

When IIC detects the general call address, both the SVST.GCAF flag and the NTST.RDBFF0 flag are set to 1 on the rising edge of the ninth cycle of SCL clock. This leads to the generation of a receive data full interrupt (IICn_RX). The value of the GCAF flag can be confirmed to recognize that the general call address has been transmitted.

Operation after detection of the general call address is the same as normal slave receive operation.

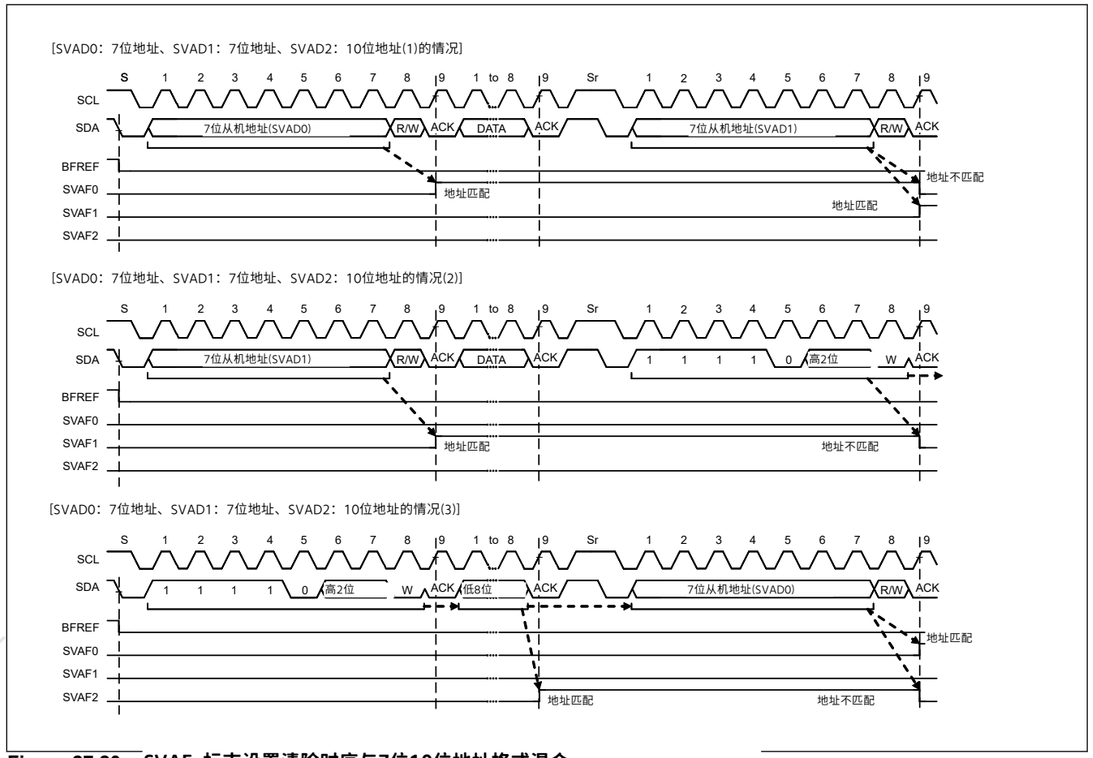


Figure 27.20 SVAFy标志设置清除时序与7位10位地址格式混合

(2) 检测广播呼叫地址

IIC具有检测广播呼叫地址（0000000+0（写入））的功能。这通过将SVCTL.GCAE位设置为1来启用。

如果在发出START或重复START条件后接收到的地址为0000000+1（读取）（起始字节），IIC将其识别为具有全零地址的从设备的地址，但不识别为广播呼叫地址。

当IIC检测到广播呼叫地址时，SVST.GCAF标志和NTST.RDBFF0标志都在SCL时钟的第9个周期的上升沿设置为1。这会导致接收数据完全中断(IICn_RX)的产生。可以确认GCAF标志的值来识别广播呼叫地址已被发送。

检测到广播呼叫地址后的操作与正常的从机接收操作相同。

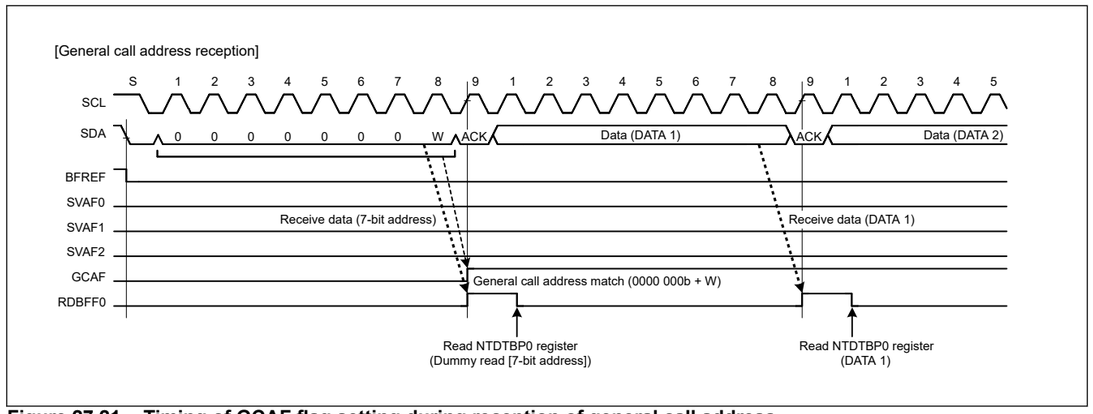


Figure 27.21 Timing of GCAF flag setting during reception of general call address

(3) Device-ID Address Detection

IIC module has a facility for detecting device-ID addresses conformant with the I²C-bus specification (Rev.03). When IIC receives 1111 100 as the first byte after a START condition or Repeated START condition was issued with the SVCTL.DVIDE bit set to 1, IIC recognizes the address as a device ID, sets the SVST.DVIDF flag to 1 on the rising edge of the ninth SCL clock cycle when the following R/W# bit = 0, and then compares the second and subsequent bytes with its own slave address. If the address matches the value in the slave address register, IIC sets the corresponding SVST.SVAFy flag (y = 0 to 2) to 1.

After that, when the first byte received after a START or Repeated START condition is issued matches the device ID address (1111 100) again and the following R/W# bit = 1, IIC does not compare the second and subsequent bytes and sets the NTST.TDBEF0 flag to 1.

In the device-ID address detection function, IIC sets the DVIDF flag to 0 if a match with IIC's own slave address is not obtained or a match with the device ID address is not obtained after a match with IIC's own slave address and the detection of a Repeated START condition. If the first byte after detection of a START or Repeated START condition matches the device ID address (1111 100) and the R/W# bit = 0, IIC sets the DVIDF flag to 1 and compares the second and subsequent bytes with IIC's slave address. If the R/W# bit = 1, the DVIDF flag holds the previous value and IIC does not compare the second and subsequent bytes. Therefore, the reception of a device-ID address can be checked by reading the DVIDF flag after confirming that TDBEF0 flag = 1.

Furthermore, prepare the device-ID fields (3 bytes: 12 bits indicating the manufacturer + 9 bits identifying the part + 3 bits indicating the revision) that must be sent to the host after reception of a continuous device-ID field as normal data for transmission. For details of the information that must be included in device-ID fields, contact NXP Semiconductors.

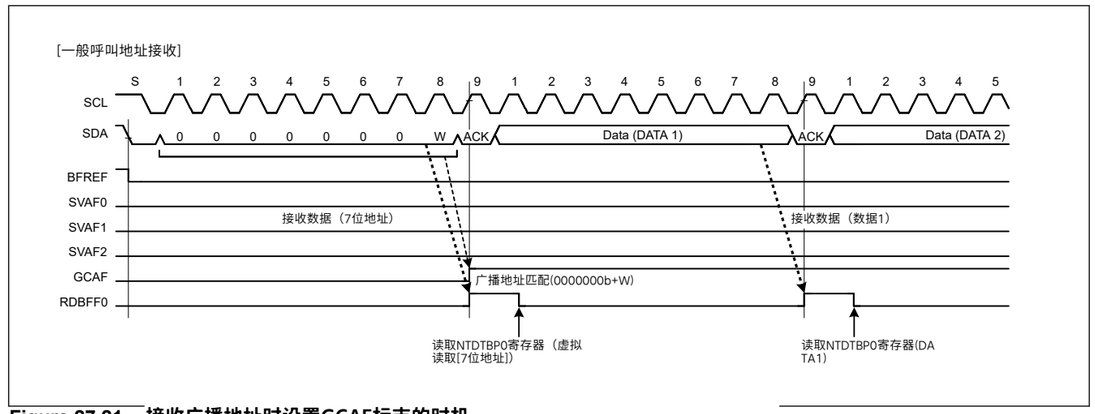


Figure 27.21 接收广播地址时设置GCAF标志的时机

(3) 设备ID地址检测

IIC模块具有用于检测符合I2C总线规范(Rev.03)的设备ID地址的工具。当IIC在发出START条件或重复START条件且SVCTL.DVIDE位设置为1后接收到1111100作为第一个字节时，IIC将地址识别为设备ID，在上升沿将SVST.DVIDF标志设置为1当后面的RW#位=0时，第9个SCL时钟周期，然后将第二个和后续字节与其自己的从地址进行比较。如果地址与从地址寄存器中的值匹配，IIC将相应的SVST.SVAFy标志（y=0到2）设置为1。

之后，当发出START或重复START条件后接收到的第一个字节再次与设备ID地址(1111100)匹配且随后的RW#位=1时，IIC不比较第二个和后续字节并设置NTST。TDBEF0标志为1。

在device-ID地址检测功能中，如果与IIC自己的从机地址匹配没有得到匹配，或者在与IIC自己的从机地址匹配并且检测到没有得到与设备ID地址匹配后，IIC设置DVIDF标志为0。重复启动条件。如果检测到START或重复START条件后的第一个字节与设备ID地址(1111100)匹配并且RW#位=0，则IIC将DVIDF标志设置为1，并将第二个和后续字节与IIC的从地址进行比较。如果RW#位=1，则DVIDF标志保持前一个值，并且IIC不比较第二个和后续字节。因此，在确认TDBEF0标志=1后，可以通过读取DVIDF标志来检查设备ID地址的接收。

此外，准备设备ID字段（3个字节：12位表示制造商+9位表示部件+3位表示版本），在接收到连续的设备ID字段作为正常数据后必须发送到主机传播。有关必须包含在设备ID字段中的信息的详细信息，请联系NXPSemiconductors。

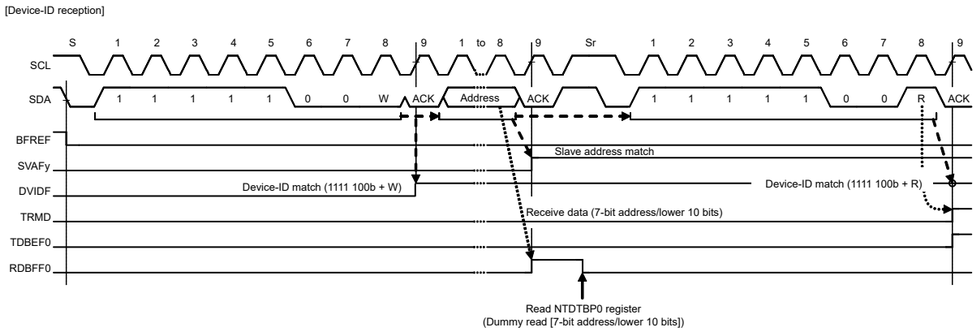


Figure 27.22 SVAFy/DVIDF flag set/clear timing during reception of device-ID

(4) Host Address Detection

IIC has a function to detect the host address while the SMBus is operating. When the SVCTL.HOAE bit is set to 1 while the BFCTL.SMBS bit = 1, IIC can detect the host address (0001 000) in slave receive mode (bits CRMS and TRMD in the PRSST register = 00).

If the bit following the host address (0001 000) is an Rd bit (R/W# bit = 1), IIC can also detect the host address. After the host address is detected, IIC operates in the same manner as normal slave operation.

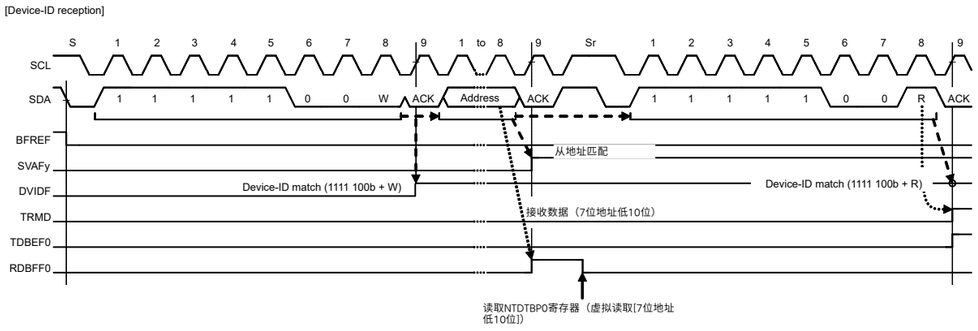


Figure 27.22 SVAFyDVIDF标志在接收设备ID期间设置清除时序

(4) 主机地址检测

IIC具有在SMBus运行时检测主机地址的功能。当SVCTL.HOAE位设置为1而BFCTL.SMBS位=1，IIC可以在从机接收模式下检测主机地址（0001000）（位CRMS和TRMD在PRSST register = 00).

如果主机地址（0001000）后面的位是Rd位（RW#位=1），IIC也可以检测主机地址。检测到主机地址后，IIC以与正常从机操作相同的方式运行。

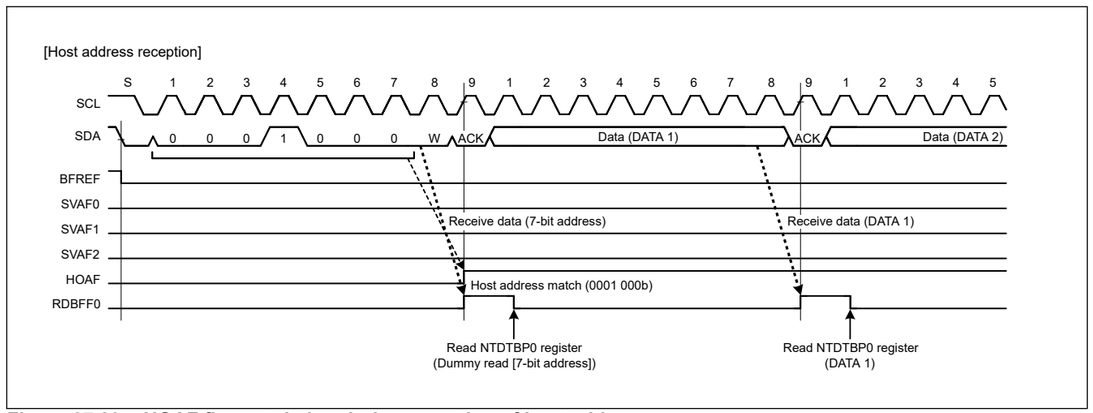


Figure 27.23 HOAF flag set timing during reception of host address

(5) Hs-mode master code Detection

IIC has a facility for detecting the Hs-mode master code (0000 1XXXb). When IIC receives the Hs-mode master code (0000 1XXXb) as the first byte after a START condition was issued with the SVCTL.HSMCE bit set to 1, this module recognizes the address as the Hs-mode master code, sets the SVST.HSMCF flag to 1 on the rising edge of the ninth SCL clock cycle. The first byte after Repeated START after NACK response to Hs-mode master code is recognized as a slave address and compared with the slave address set by SVDVADy.SVAD[9:0] (y = 0 to 2). When IIC detects a match of the set slave address, the corresponding SVST.SVAFy flag (y = 0 to 2) is set to 1 at the rising edge of the ninth SCL clock cycle, and the NTST.RDBFF0 flag or the NTST.TDBEF0 flag is set to 1 by the following R/W# bit. This causes a receive data full interrupt (IICn_RX) or transmit data empty interrupt (IICn_TX) to be generated. The SVAFy flag is used to identify which slave address has been specified. The SVST.HSMCF flag is cleared to 0 when the STOP condition is detected.

Note: If the Hs-mode master code (0000 1XXXb) is received with the SVCTL.HSMCE bit set to 0, other patterns are ignored until the STOP condition is detected.

Note: Hs-mode is supported by IIC0(SCL0_A, SDA0_A).

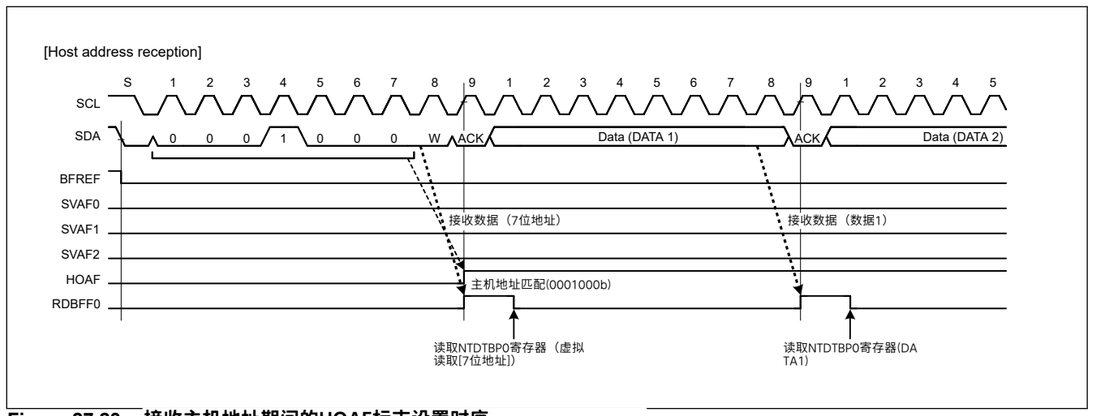


Figure 27.23 接收主机地址期间的HOAF标志设置时序

(5) Hs-mode主码检测

IIC具有检测Hs模式主代码(00001XXXb)的功能。当IIC在SVCTL.HSMCE位设置为1的情况下发出START条件后接收到Hs模式主代码(00001XXXb)作为第一个字节时，该模块将该地址识别为Hs模式主代码，设置SVST。在第9个SCL时钟周期的上升沿，HSMCF标志为1。NACK响应Hs模式主机代码后重复START后的第一个字节被识别为从机地址，并与SVDVADy.SVAD[9:0]设置的从机地址进行比较（y=0到2）。当IIC检测到设置的从地址匹配时，对应的SVST.SVAFy标志（y=0到2）在第9个SCL时钟周期的上升沿设置为1，并且NTST.RDBFF0标志或NTST.TDBEF0flag由后面的RW#位设置为1。这会导致产生接收数据满中断(IICn_RX)或发送数据空中断(IICn_TX)。SVAFy标志用于标识已指定哪个从地址。当检测到STOP条件时，SVST.HSMCF标志清零。

Note: 如果在SVCTL.HSMCE位设置为0的情况下接收到Hs模式主代码(00001XXXb)，则忽略其他模式，直到检测到STOP条件。

Note: IIC0(SCL0_A SDA0_A)支持Hs模式。

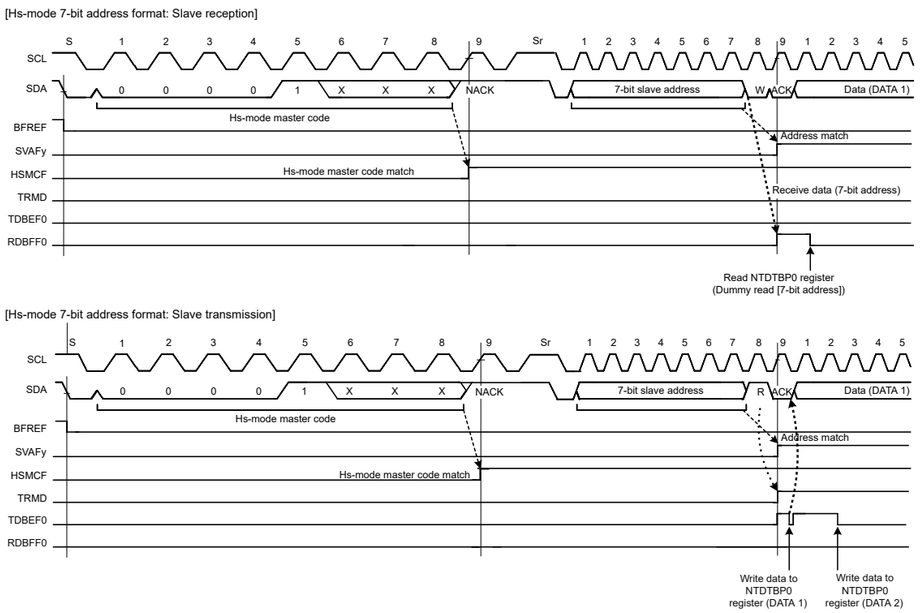


Figure 27.24 SVAFy/HSMCF Flag Set Timing during Reception of Hs-mode master code

27.3.1.3.4 Arbitration-Lost Detection

In addition to the normal arbitration-lost detection function defined by the I^2C-bus specification, the IIC has functions to prevent double-issue of a start condition, to detect arbitration-lost during transmission of NACK, and to detect arbitration-lost in slave transmit mode.

(1) Master Arbitration-Lost Detection (MALE Bit)

The IIC drives the SDAn line low to issue a start condition. However, if the SDAn line has already been driven low by another master device issuing a start condition, this module causes arbitration to be lost, so priority is given to transfer by the other master device. Similarly, if the CNDCTL.STCND bit is set to 1 while the BCST.BFREF flag is 0 (bus busy state), arbitration is lost, so priority is given to transfer by the other master device. No start condition is issued in this case.

When a start condition is issued successfully, if the data for transmission including the address bits (the internal SDA output level) and the level on the SDAn line do not match (the high output as the internal SDA output, that is, the SDA0 pin is in the high-impedance state) and the low level is detected on the SDAn line, the IIC loses in arbitration.

IIC detects master arbitration-lost when the following conditions are met while the BSTE.ALE bit = 1 and the BFCTL.MALE bit = 1 (master arbitration-lost detection enabled).

If arbitration of mastership is lost, IIC immediately enters slave receive mode.

If a slave address (including the general call address) matches its own address at this time, IIC continues in slave operation.

[Conditions for master arbitration-lost]

- Non-matching of the internal level for output on SDA and the level on the SDAn line after a START condition was issued by setting the CNDCTL.STCND bit to 1 while the BCST.BFREF flag was set to 1 (erroneous issuing of a START condition)
- Setting of the CNDCTL.STCND bit to 1 (START condition double-issue error) while the BFREF flag is set to 0

Note: IIC does not issue a START condition.

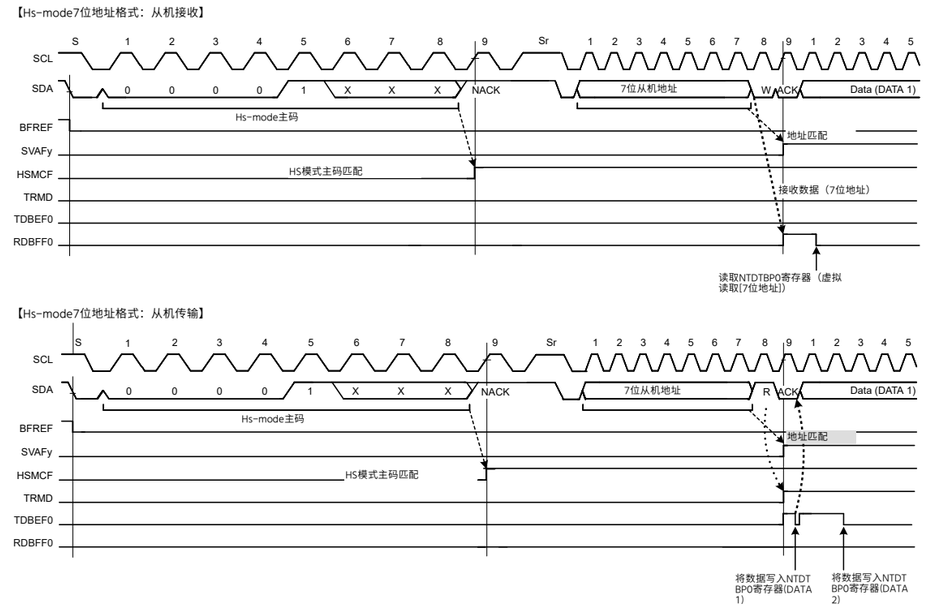


Figure 27.24 接收Hs模式主码期间的SVAFyHSMCF标志设置时序

27.3.1.3.4 Arbitration-Lost Detection

除了I2C总线规范定义的正常仲裁丢失检测功能外，IIC还具有防止重复发出启动条件、在NACK传输期间检测仲裁丢失以及检测从机中的仲裁丢失等功能。传输模式。

(1) 主仲裁丢失检测（MALE位）

IIC将SDAn线驱动为低电平以发出启动条件。但是，如果SDAn线已经被另一个发出启动条件的主设备驱动为低电平，则该模块会导致仲裁丢失，因此优先由另一个主设备进行传输。类似地，如果CNDCTL.STCND位设置为1，而BCST.BFREF标志为0（总线繁忙状态），则仲裁丢失，因此优先由其他主设备传输。在这种情况下不发出启动条件。

启动条件发出成功时，如果发送的数据包括地址位（内部SDA输出电平）与SDAn线上的电平不匹配（高电平输出作为内部SDA输出，即SDA0引脚）处于高阻状态）并且在SDAn线上检测到低电平，则IIC仲裁失败。

当BSTE.ALE位=1且满足以下条件时，IIC检测到主机仲裁丢失
BFCTL.MALE位=1（使能主机仲裁丢失检测）。

如果主控仲裁失败，IIC立即进入从机接收模式。

如果此时从机地址（包括广播地址）与自己的地址匹配，则IIC继续从机操作。

【主仲裁失败的条件】

●通过将CNDCTL.STCND位设置为1而BCST.BFREF标志设置为1（错误发出START健康）状况）

●将CNDCTL.STCND位设置为1（START条件双发出错误），同时BFREF标志设置为0

Note: IIC不发出START条件。

- When the transmit data excluding acknowledge (internal SDA output level) does not match the level on the SDAn line in master transmit mode (bits CRMS and TRMD in the PRSST register = 11)

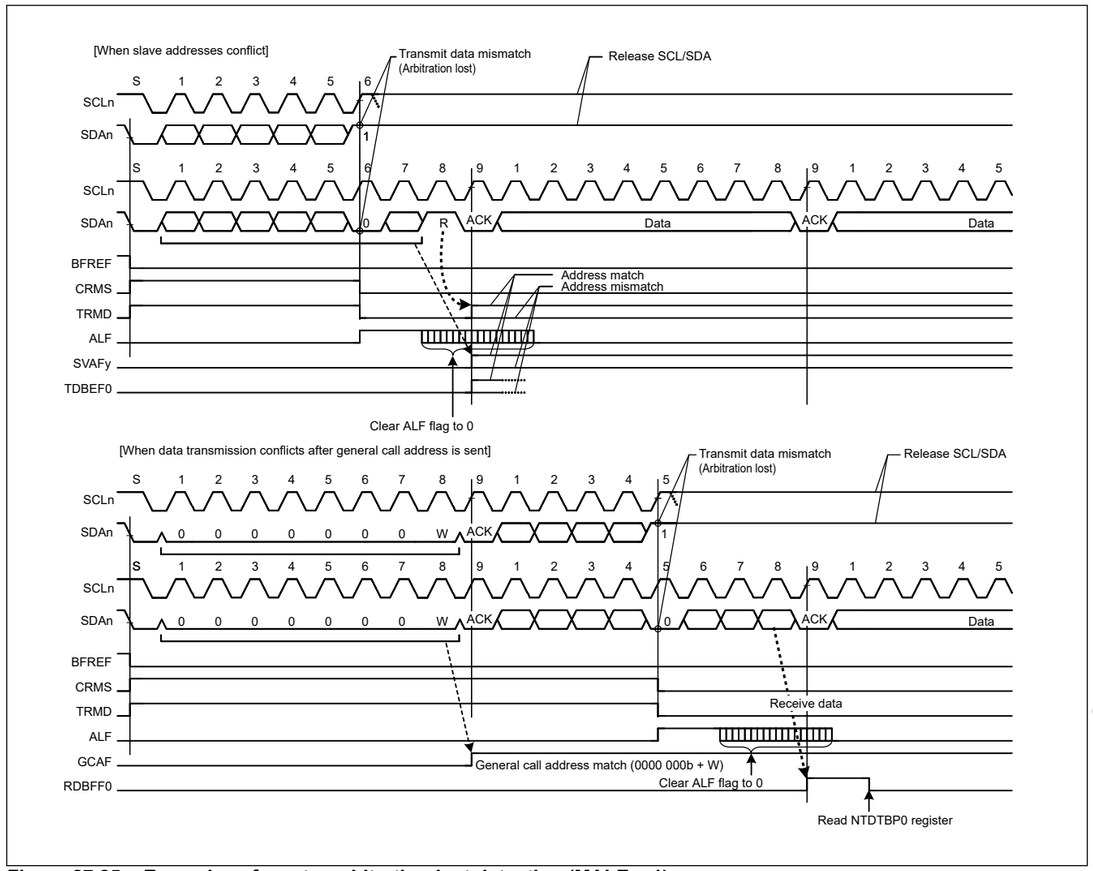


Figure 27.25 Examples of master arbitration-lost detection (MALE = 1)

●当发送数据不包括确认（内部SDA输出电平）与主发送模式下SDAn线上的电平不匹配时（PRSST寄存器中的CRMS和TRMD位=11）

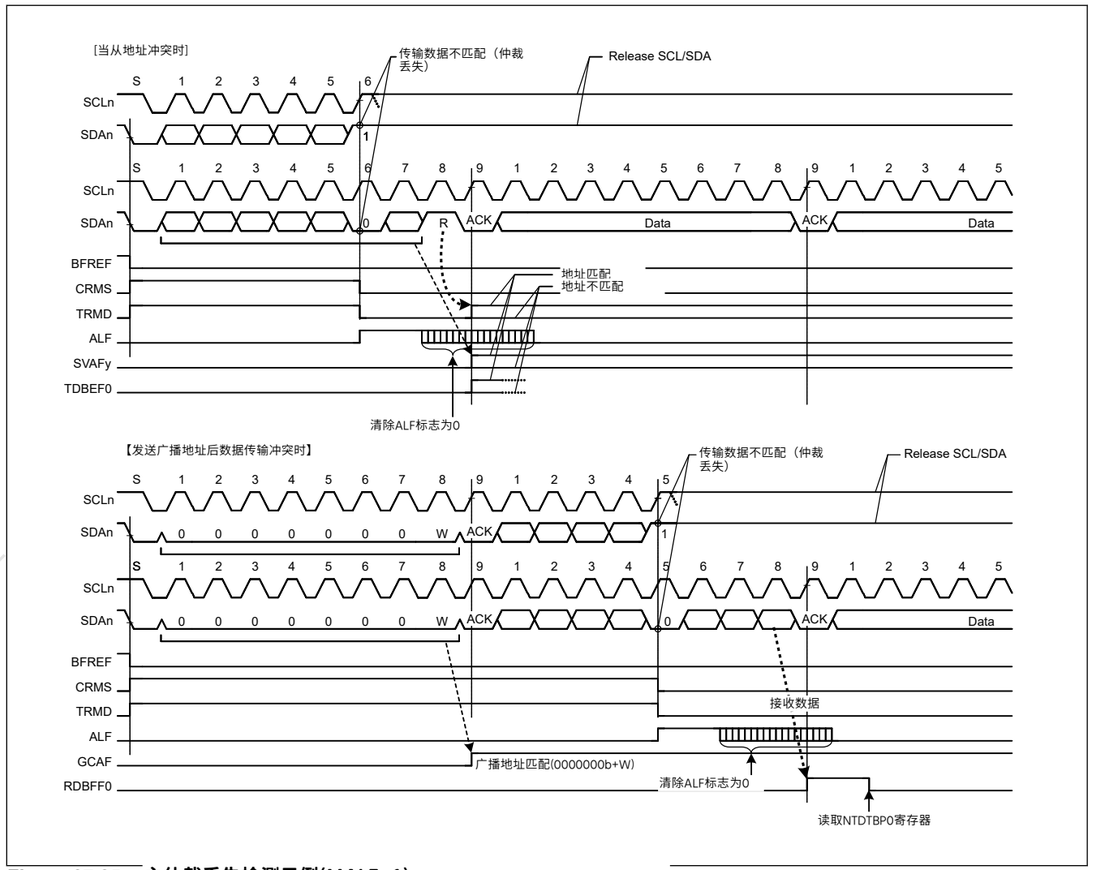
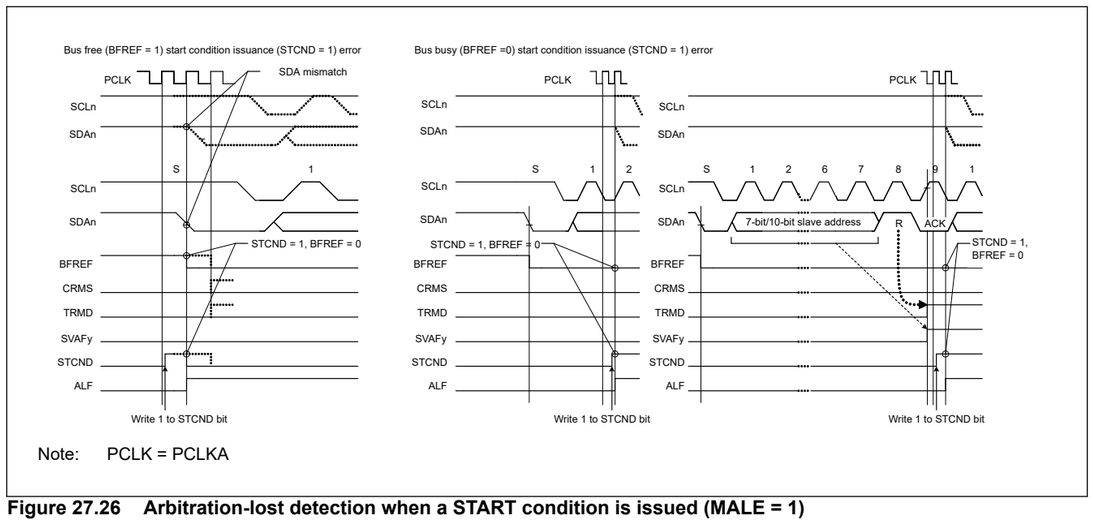


Figure 27.25 主仲裁丢失检测示例(MALE=1)



Note: PCLK = PCLKA

Figure 27.26 Arbitration-lost detection when a START condition is issued (MALE = 1)

(2) Arbitration-Lost Detection during NACK Transmission (NALE Bit)

The IIC has a function to cause arbitration to be lost if the internal SDA output level does not match the level on the SDAn line (the high output as the internal SDA output; i.e. the SDAn pin is in the high-impedance state) and the low level is detected on the SDAn line during transmission of NACK in receive mode. Arbitration is lost due to a conflict of NACK transmission and ACK transmission when two or more master devices receive data from the same slave device simultaneously in a multi-master system. Such conflict occurs when multiple master devices send/receive the same information through a single slave device.

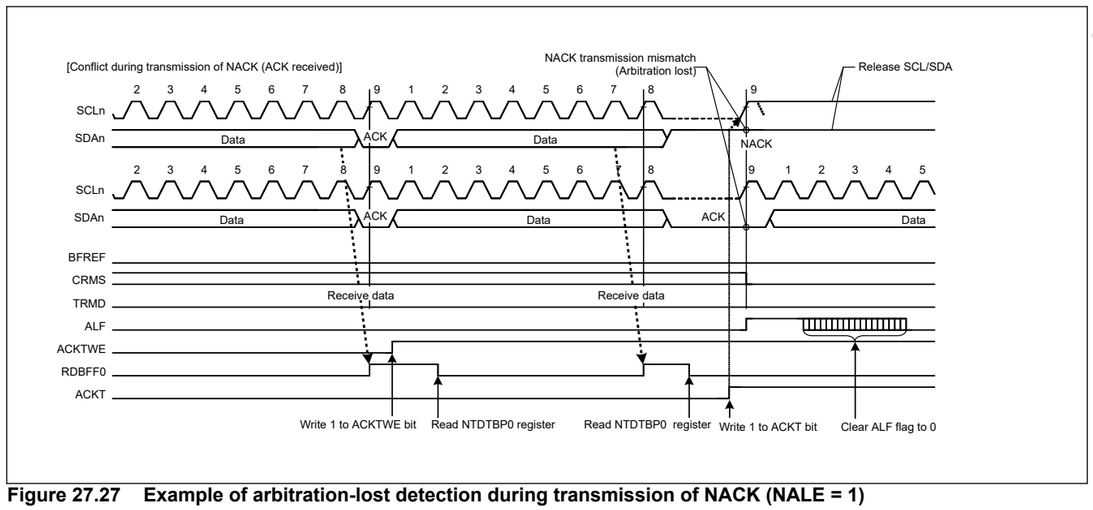
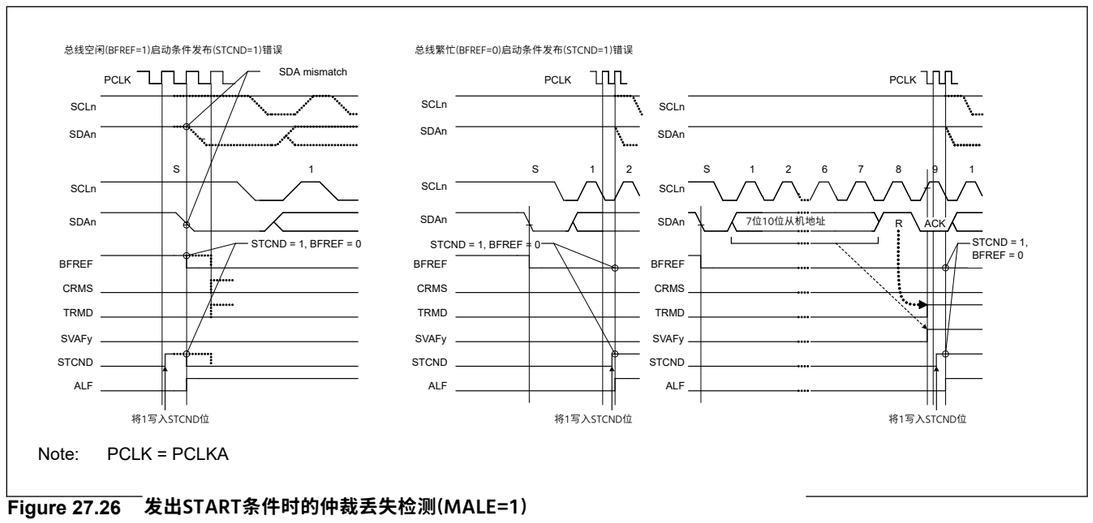


Figure 27.27 Example of arbitration-lost detection during transmission of NACK (NALE = 1)

The following section explains arbitration-lost detection using an example where two master devices (master A and master B) and a single slave device are connected through the bus. In this example, master A receives 2 bytes of data from the slave device, and master B receives 4 bytes of data from the slave device.

If master A and master B access the slave device simultaneously, because the slave address is identical, arbitration is not lost in both master A and master B during access to the slave device. Therefore, both master A and master B recognize that they have obtained the bus mastership and operate as such. In this example,, master A sends NACK when it has received 2 final bytes of data from the slave device. Meanwhile, master B sends ACK because it has not received the necessary 4 bytes of data. At this time, the NACK transmission from master A and the ACK transmission from master B conflict. In general, if a



Note: PCLK = PCLKA

Figure 27.26 发出START条件时的仲裁丢失检测(MALE=1)

(2) NACK传输期间的仲裁丢失检测（NALE位）

如果内部SDA输出电平与SDAn线上的电平不匹配（高输出作为内部SDA输出；即SDAn引脚处于高阻抗状态），IIC具有导致仲裁丢失的功能，并且在接收模式下发送NACK期间，在SDAn线上检测到低电平。在多主系统中，当两个或多个主设备同时从同一从设备接收数据时，由于NACK传输和ACK传输冲突，导致仲裁丢失。当多个主设备通过单个从设备发送接收相同的信息时，就会发生这种冲突。

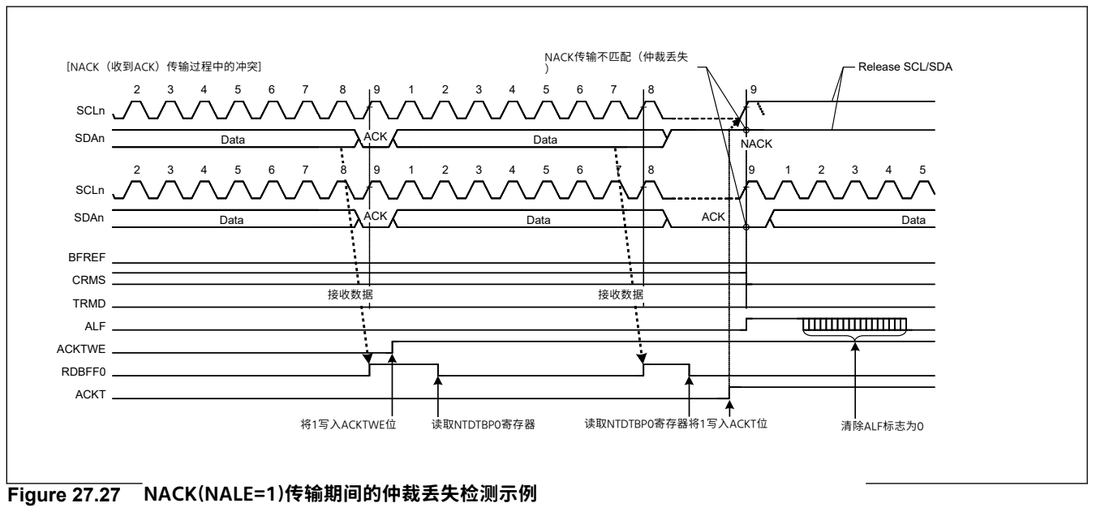


Figure 27.27 NACK(NALE=1)传输期间的仲裁丢失检测示例

以下部分使用两个主设备（主设备A和主设备）的示例解释仲裁丢失检测
B)和单个从设备通过总线连接。在本例中，主设备A从从设备接收2个字节的数据，主设备B从从设备接收4个字节的数据。

如果主设备A和主设备B同时访问从设备，由于从设备地址相同，在访问从设备期间，主设备A和主设备B都不会丢失仲裁。因此，主机A和主机B都承认他们已经获得了总线控制权并照此运行。在此示例中，主设备A在从从设备接收到最后2个字节的数据时发送NACK。同时，masterB发送ACK，因为它没有收到必要的4字节数据。此时，来自masterA的NACK传输和来自masterB的ACK传输冲突。一般来说，如果一个

conflict like this occurs, master A cannot detect ACK transmitted by master B and issues a stop condition. Therefore, the issuance of the stop condition conflicts with the SCL clock output of master B, which disturbs communication.

When this module receives ACK during transmission of NACK, it detects a defeat in conflict with other master devices and causes arbitration to be lost.

If arbitration is lost during transmission of NACK, this module is immediately released from the slave-matched state and enters slave receive mode. This prevents a stop condition from being issued, preventing a communication failure on the bus.

Similarly, in the ARP command processing of SMBus, the function to detect loss of arbitration during transmission of NACK is also available for eliminating the extra clock cycle processing (such as FFh transmission processing) necessary if the UDID (Unique Device Identifier) of assign address does not match in the Get UDID (general) processing after the Assign Address command.

The IIC detects arbitration-lost during transmission of NACK when the following condition is met while the BSTE.ALE bit = 1 and the BFCTL.NALE bit = 1 (arbitration-lost detection during NACK transmission enabled).

[Condition for arbitration-lost during NACK transmission]

- When the internal SDA output level does not match the SDAn line (ACK is received) during transmission of NACK (ACKCTL.ACKT bit = 1)

(3) Slave Arbitration-Lost Detection (SALE Bit)

The IIC has a function to cause arbitration to be lost if the data for transmission (the internal SDA output level) and the level on the SDAn line do not match (the high output as the internal SDA output, that is, the SDAn pin is in the high impedance state) and the low level is detected on the SDAn line in slave transmit mode. This arbitration-lost detection function is mainly used when transmitting a UDID (Unique Device Identifier) over an SMBus.

If arbitration is lost during transmission of DATA, this module is immediately released from the slave-matched state and enters slave receive mode. This function can detect conflicts of data during transmission of UDIDs over an SMBus and eliminate subsequent redundant processing (processing for the transmission of 0xFF).

The IIC detects slave arbitration-lost when the following condition is met while the BSTE.ALE bit = 1 and the BFCTL.SALE bit = 1 (slave arbitration-lost detection enabled).

[Condition for slave arbitration-lost]

- When the transmit data excluding acknowledge (internal SDA output level) does not match the level on the SDAn line in slave transmit mode (bits CRMS and TRMD in the PRSST register = 01).

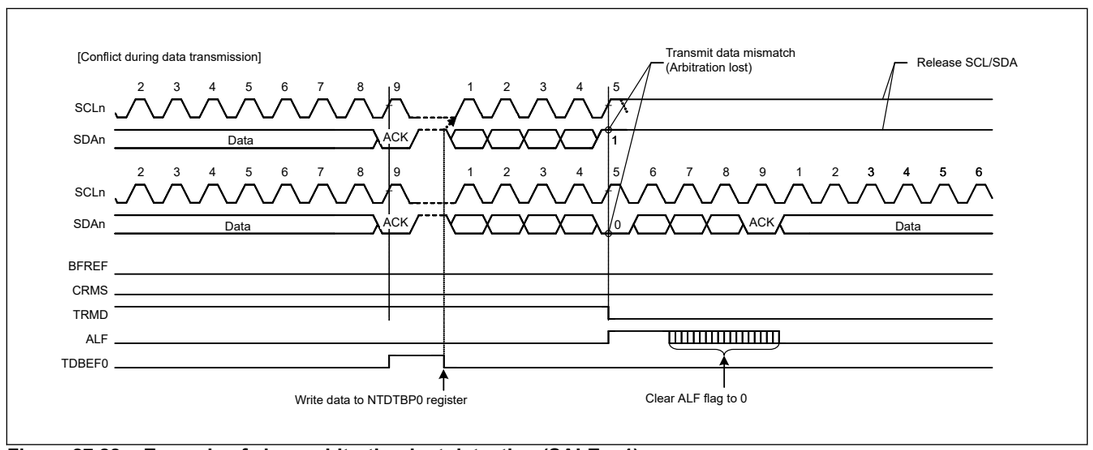


Figure 27.28 Example of slave arbitration-lost detection (SALE = 1)

发生这样的冲突时，masterA无法检测到masterB发送的ACK并发出停止条件。因此，停止条件的发出与主机B的SCL时钟输出相冲突，从而干扰了通信。

当本模块在NACK传输过程中接收到ACK时，它会检测到与其他主设备冲突的失败并导致仲裁丢失。

如果在NACK传输过程中仲裁丢失，该模块立即从从机匹配状态释放并进入从机接收模式。这可以防止发出停止条件，从而防止总线上的通信故障。

同样，在SMBus的ARP命令处理中，如果分配地址的UDID（UniqueDeviceIdentifier），也可以通过检测NACK传输过程中仲裁丢失的功能来消除额外的时钟周期处理（例如FFh传输处理）。在分配地址命令之后的获取UDID（一般）处理中不匹配。

当BSTE.ALE位=1且BFCTL.NALE位=1（启用NACK传输期间仲裁丢失检测）时满足以下条件时，IIC在NACK传输期间检测仲裁丢失。

[在NACK传输期间仲裁丢失的条件]

●在NACK传输期间，当内部SDA输出电平与SDAn线不匹配时（接收到ACK）（ACKCTL.ACKT位=1）

(3) 从设备仲裁丢失检测（SALE位）

IIC有一个功能，如果要发送的数据（内部SDA输出电平）和SDAn线上的电平不匹配（高输出作为内部SDA输出，即SDAn引脚为处于高阻抗状态）并且在从发送模式下在SDAn线上检测到低电平。这种仲裁丢失检测功能主要用于通过SMBus传输UDID（唯一设备标识符）时。

如果在DATA传输过程中仲裁丢失，该模块立即从从机匹配状态释放并进入从机接收模式。该功能可以检测通过SMBus传输UDID期间的数据冲突，并消除后续的冗余处理（传输0xFF的处理）。

当满足以下条件且BSTE.ALE位=1且
BFCTL.SALE位=1（启用从设备仲裁丢失检测）。

[从机仲裁失败的条件]

●当发送数据不包括确认（内部SDA输出电平）与从发送模式下SDAn线上的电平不匹配时（PRSST寄存器中的位CRMS和TRMD=01）。

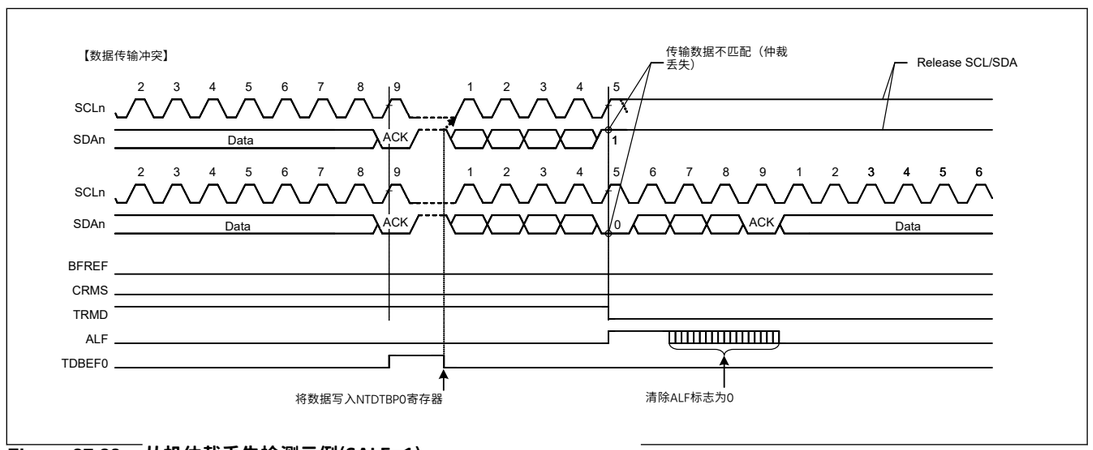


Figure 27.28 从机仲裁丢失检测示例(SALE=1)

27.3.1.3.5 Clock Stretching

(1) Function to Prevent Wrong Transmission of Transmit Data

When data have not been written to the I^2C bus transmit data register (NTDTBP0) with IIC in transmission mode (PRSST.TRMD = 1), the SCLn line is automatically held at the low level over the intervals shown below. This low-hold period is extended until data for transmission have been written, which prevents the unintended transmission of erroneous data.

Master transmit mode

- Low-level interval after a START condition or Repeated START condition is issued
- Low-level interval between the ninth clock cycle of one transfer and the first clock cycle of the next

Slave transmit mode

- Low-level interval between the ninth clock cycle of one transfer and the first clock cycle of the next

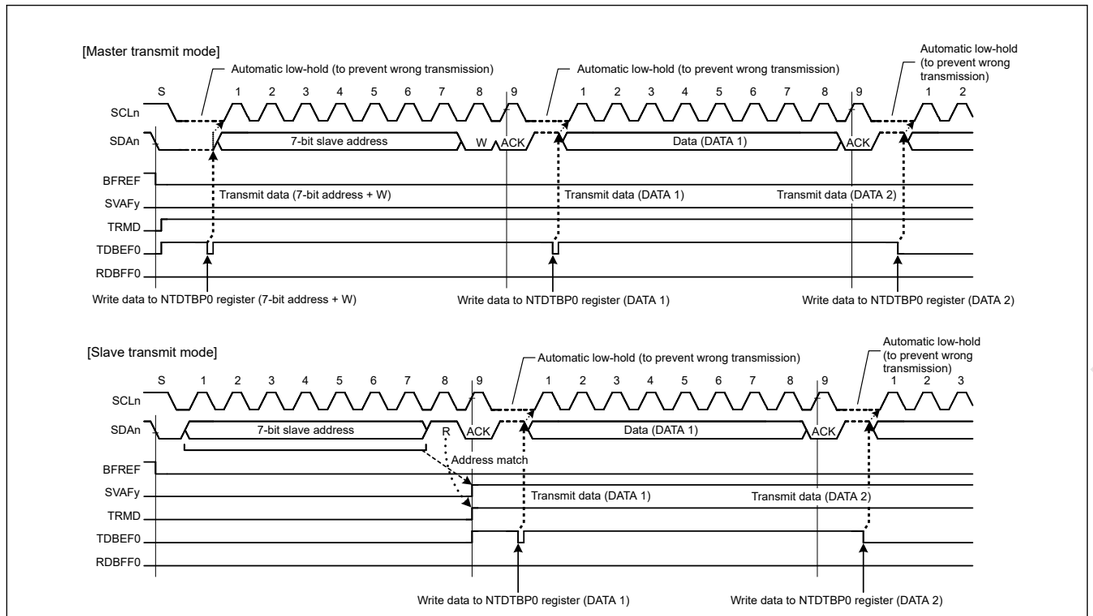


Figure 27.29 Automatic low-hold operation in transmit mode

(2) NACK Reception Transfer Abort Function

IIC has a function to abort transfer operation when NACK is received in transmit mode (PRSST.TRMD = 1). This function is enabled when the BSTE.NACKDE bit is set to 1 (transfer abort enabled). If the next transmit data has already been written (NTST.TDBEF0 = 0) when NACK is received, next data transmission at the falling edge of the ninth SCL clock cycle is automatically aborted. This prevents the SDAn line output level from being held low when the MSB of the next transmit data is 0.

If the transfer operation is aborted by this function (BST.NACKDF = 1), transmit operation and receive operation are discontinued. To restore transmit/receive operation, be sure to set the NACKDF flag to 0. In master transmit mode, restore operation using either of the methods below:

- After issuing a Repeated START condition, set the NACKDF flag to 0
- After issuing a STOP condition, set the NACKDF flag to 0 and then issue a START condition

27.3.1.3.5 时钟拉伸

(1) 防止传输数据错误传输的功能

当IIC处于传输模式(PRSST.TRMD=1)时尚未将数据写入I2C总线传输数据寄存器(NTDTBP0)时，SCLn线在如下所示的时间间隔内自动保持在低电平。这个低保持期一直延长到要传输的数据已经被写入，这样可以防止错误数据的意外传输。

主传输模式

●发出START条件或RepeatedSTART条件后的低电平间隔

●一次传输的第9个时钟周期与下一次传输的第一个时钟周期之间的低电平间隔

从机发送模式

●一次传输的第9个时钟周期与下一次传输的第一个时钟周期之间的低电平间隔

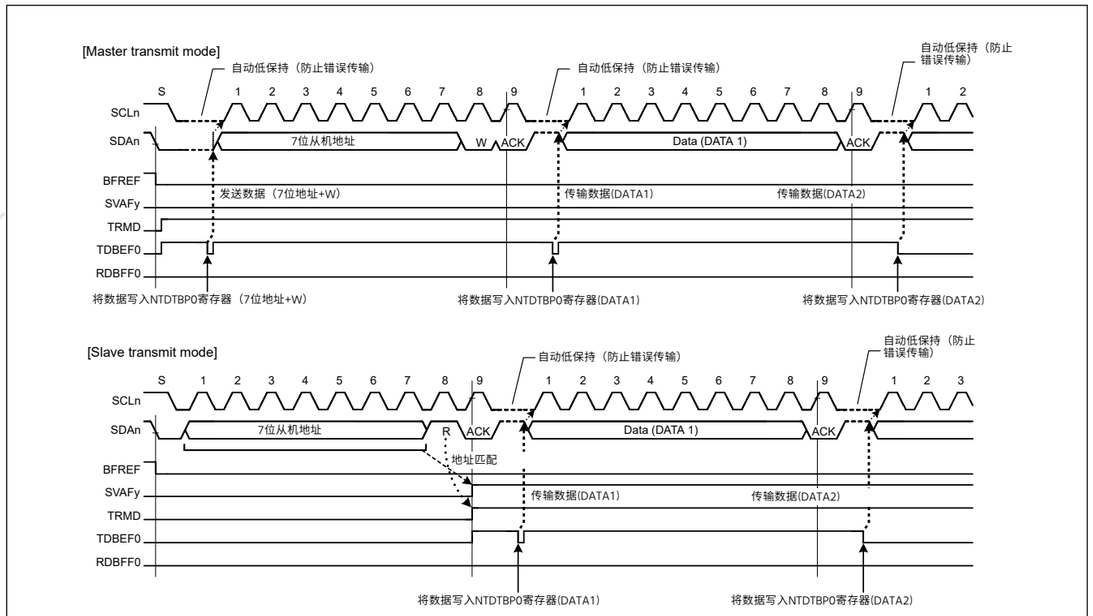


Figure 27.29 发送模式下的自动低保持操作

(2) NACK接收传输中止功能

IIC具有在发送模式下（PRSST.TRMD=1）接收到NACK时中止传输操作的功能。当BSTE.NACKDE位设置为1（使能传输中止）时，该功能被启用。如果在收到NACK时已经写入下一个发送数据（NTST.TDBEF0=0），则在第9个SCL时钟周期的下降沿自动中止下一个数据发送。这可以防止SDAn线路输出电平在下一个发送数据的MSB为0时保持低电平。

如果传输操作被此函数中止（BST.NACKDF=1），发送操作和接收操作将中断。要恢复发送接收操作，请务必将NACKDF标志设置为0。在主发送模式下，使用以下任一方法恢复操作：

●发出重复启动条件后，将NACKDF标志设置为0

●发出STOP条件后，将NACKDF标志设置为0，然后发出START条件

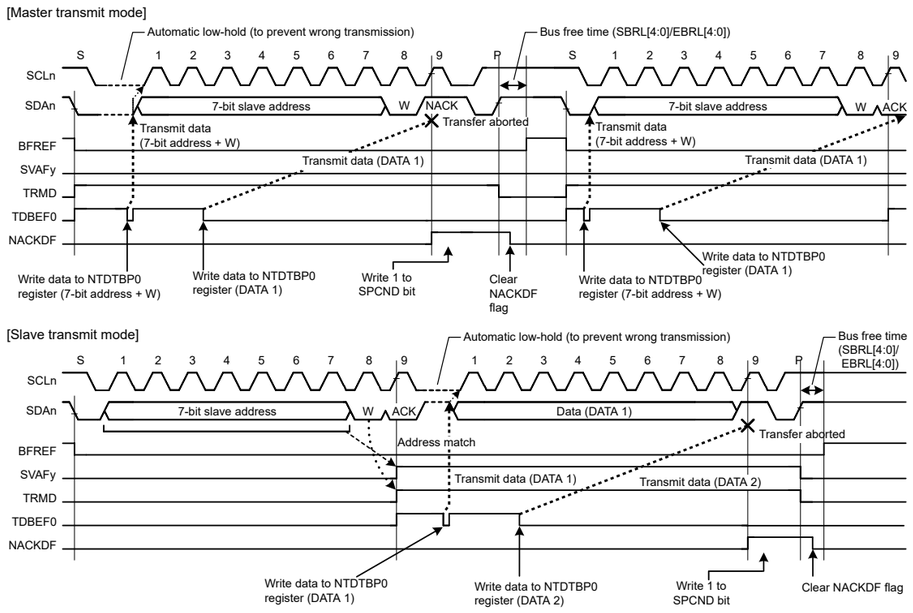


Figure 27.30 Abort of data transfer when NACK is received (NACKE = 1)

(3) Function to Prevent Failure to Receive Data

If response processing is delayed when receive data (NTDTBP0) read is delayed for a period of one transfer frame or more with receive data full (NTST.RDBFF0 = 1) in receive mode (PRSST.TRMD = 0), IIC holds the SCLn line low automatically immediately before the next data is received to prevent failure to receive data.

This function to prevent failure to receive data using the automatic low-hold function is also enabled even if the read processing of the final receive data is delayed and, in the meantime, IIC's own slave address or another slave address is received after a STOP condition is issued.

Sections in which the SCLn line is held low can be selected with a combination of the RWE and ACKTWE bits in SCSTRCTL.

(a) 1-Byte Receive Operation and Automatic Low-Hold Function Using the RWE Bit

When the SCSTRCTL.RWE bit is set to 1, IIC performs 1-byte receive operation using the RWE bit function.

Furthermore, when the SCSTRCTL.ACKTWE bit = 0, IIC automatically sends the ACKCTL.ACKT bit value for the acknowledge bit in the period from the falling edge of the eighth SCL clock cycle to the falling edge of the ninth SCL clock cycle, and automatically holds the SCLn line low at the falling edge of the ninth SCL clock cycle using the RWE bit function. This low-hold is released by reading data from NTDTBP0, which enables bytewise receive operation.

The RWE bit function is enabled for receive frames after a match with IIC's own slave address (including the general call address and host address) is obtained in master receive mode or slave receive mode.

(b) 1-Byte Receive Operation (ACK/NACK Transmission Control) and Automatic Low-Hold Function Using the ACKTWE Bit

When the SCSTRCTL.ACKTWE bit is set to 1, IIC performs 1-byte receive operation using the ACKTWE bit function.

When the ACKTWE bit is set to 1, the NTST.RDBFF0 flag (receive data full) is set to 1 at the rising edge of the eighth SCL clock cycle, and the SCLn line is automatically held low at the falling edge of the eighth SCL clock cycle. This lowhold is

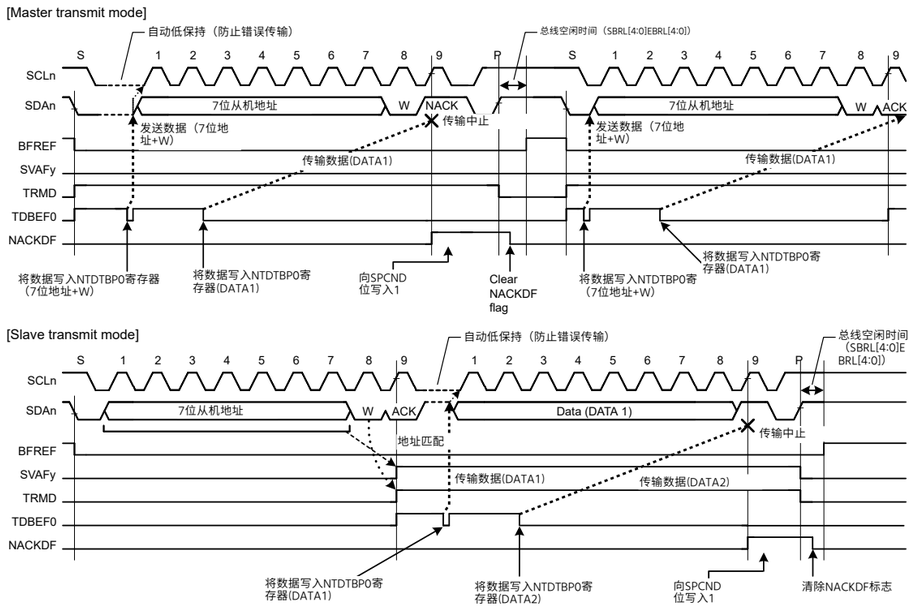


Figure 27.30 收到NACK时中止数据传输(NACKE=1)

(3) 防止数据接收失败的功能

如果在接收模式(PRSST.TRMD=0)下接收数据(NTDTBP0)读取延迟一个传输帧或更长时间且接收数据已满(NTST.RDBFF0=1)时响应处理延迟，则IIC保持SCLn线在接收到下一个数据之前自动拉低，以防止接收数据失败。

即使最终接收数据的读取处理延迟，同时，在STOP条件后接收到IIC自己的从地址或另一个从地址，该功能也启用了使用自动低保持功能防止接收数据失败的功能发出。

SCLn线保持低电平的部分可以通过RWE和ACKTWE位的组合来选择
SCSTRCTL.

(a)1字节接收操作和使用RWE位的自动低保持功能

当SCSTRCTL.RWE位设置为1时，IIC使用RWE位功能执行1字节接收操作。

此外，当SCSTRCTL.ACKTWE位=0时，IIC在第8个SCL时钟周期的下降沿到第9个SCL时钟周期的下降沿期间自动发送ACKCTL.ACKT位值作为确认位，并自动使用RWE位功能在第9个SCL时钟周期的下降沿将SCLn线保持为低电平。该低保持通过从NTDTBP0读取数据来释放，从而启用按字节接收操作。

在主接收模式或从接收模式下，获得与IIC自己的从地址（包括广播地址和主机地址）匹配后的接收帧使能RWE位功能。

(b)1字节接收操作（ACKNACK传输控制）和使用ACKTWE位的自动低保持功能

当SCSTRCTL.ACKTWE位设置为1时，IIC使用ACKTWE位功能执行1字节接收操作。

当ACKTWE位设置为1时，NTST.RDBFF0标志（接收数据已满）在第8个SCL时钟周期的上升沿设置为1，并且SCLn线在第8个SCL的下降沿自动保持为低时钟周期。这个低点是

released by writing a value to the ACKCTL.ACKT bit, but cannot be released by reading data from NTDTBP0, which enables receive operation by the ACK/NACK transmission control according to the data received in byte units.

The ACKTWE bit function is enabled for receive frames after a match with IIC's own slave address (including the general call address and host address) is obtained in master receive mode or slave receive mode.

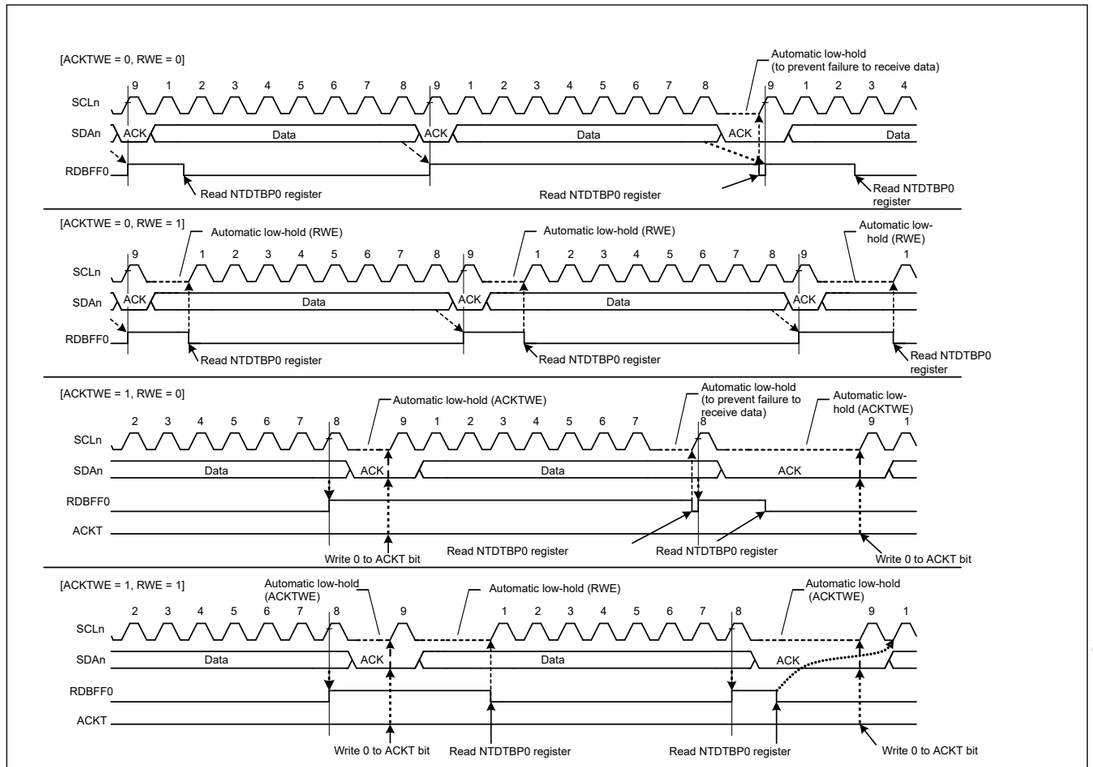


Figure 27.31 Automatic low-hold operation in receive mode (using ACKTWE and RWE bits)

27.3.1.3.6 Port Control

(1) Extra SCL Clock Cycle Output Function

In master mode, IIC module has a facility for the output of extra SCL clock cycles to release the SDAn line of the slave device from being held at the low level due to the master being out of synchronization with the slave device.

This function is mainly used in master mode to release the SDAn line of the slave device from the state of being fixed to the low level by including extra cycles of SCL output from IIC with single cycles of the SCL clock as the unit in the case of a bus error where IIC cannot issue a Repeated START condition or a STOP condition because the slave device is holding the SDAn line at the low level. Do not use this facility in normal situations. Using it when communications are proceeding correctly will lead to malfunctions.

When the OUTCTL.EXCYC bit is set to 1, an additional clock pulse at the frequency set by the REFCKCTL.IREFCKS[2:0] bits and the STDBR.SBRHO[7:0] and STDBR.SBRLO[7:0] registers is output from the SCLn pin. After output of this clock pulse, the EXCYC bit automatically becomes 0. After confirming that the EXCYC bit is 0, wait for the setup time of the Repeated START condition or STOP condition, and then confirm the detection of the Repeated START condition or STOP condition. If the Repeated START condition or STOP condition is not detected, consecutive additional clock pulses can be output by writing 1 to the EXCYC bit again.

When IIC module is in master mode and the slave device is holding the SDAn line at the low level because synchronization with the slave device has been lost due to the effects of noise, etc., the output of a Repeated START condition or a STOP

通过向ACKCTL.ACKT位写入值来释放，但不能通过从NTDTBP0读取数据来释放，这将根据以字节为单位接收到的数据，通过ACKNACK传输控制进行接收操作。

在主接收模式或从接收模式下获得与IIC自己的从地址（包括广播地址和主机地址）匹配后的接收帧使能ACKTWE位功能。

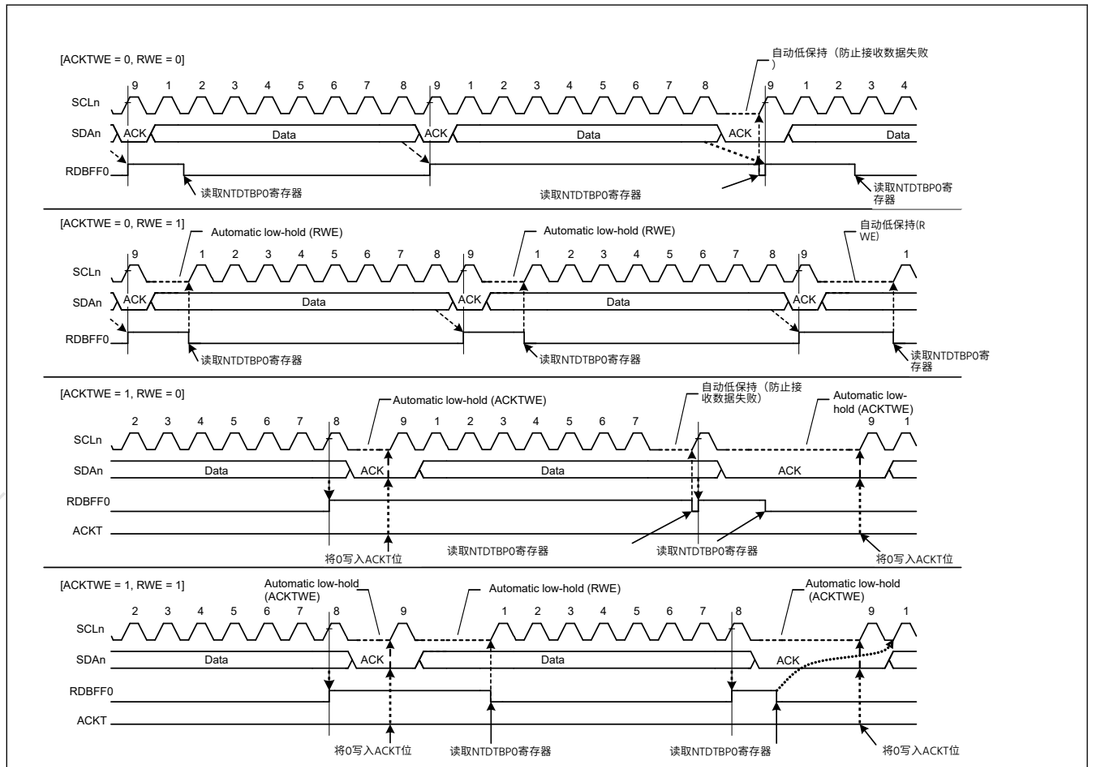


Figure 27.31 接收模式下的自动低保持操作（使用ACKTWE和RWE位）

27.3.1.3.6 端口控制

(1) 额外的SCL时钟周期输出功能

在主模式下，IIC模块具有输出额外SCL时钟周期的功能，以释放从设备的SDAn线由于主设备与从设备不同步而保持在低电平。

该功能主要用于主机模式下，以单周期SCL时钟为单位，包含IIC输出的额外SCL周期，使从机的SDAn线从固定状态释放到低电平。IIC无法发出重复启动条件或停止条件的总线错误，因为从设备将SDAn线保持在低电平。请勿在正常情况下使用此设施。在通信正常进行时使用它会导致故障。

当OUTCTL.EXCYC位设置为1时，一个额外的时钟脉冲在由设置的频率REFCKCTL.IREFCKS[2:0]位和STDBR.SBRHO[7:0]和STDBR.SBRLO[7:0]寄存器从SCLn引脚输出。此时钟脉冲输出后，EXCYC位自动变为0。确认EXCYC位为0后，等待重复START条件或STOP条件的建立时间，然后确认检测到重复START条件或STOP条件.如果未检测到重复启动条件或停止条件，则可以通过再次向EXCYC位写入1来输出连续的附加时钟脉冲。

当IIC模块处于主模式并且从设备保持SDAn线为低电平时，因为与从设备的同步由于噪声等的影响而丢失，重复START条件或STOP的输出

condition is not possible. The facility for output of an extra cycle of the SCL clock can be used to output extra cycles of SCL one by one to make the slave device release the SDAn line from being held at the low level, thus recovering the bus from an unusable state. Release of the SDAn line by the slave device can be monitored by reading the SDILV bit in PRSTDBG. After the SDAn line has been released by the slave device, the preset of a Repeated START condition or a STOP condition is issued.

Use this function with the BFCTL.MALE bit set to 0 (master arbitration-lost detection is disabled).

[Output conditions for using the EXCYC bit in OUTCTL]

- When the bus is free (BFREF flag in BCST = 1) or in master mode (CRMS bit = 1 in PRSST and BFREF flag = 0 in BCST)
- When the communication device does not hold the SCLn line low

Figure 27.32 shows the operation timing of the extra SCL clock cycle output function (EXCYC bit).

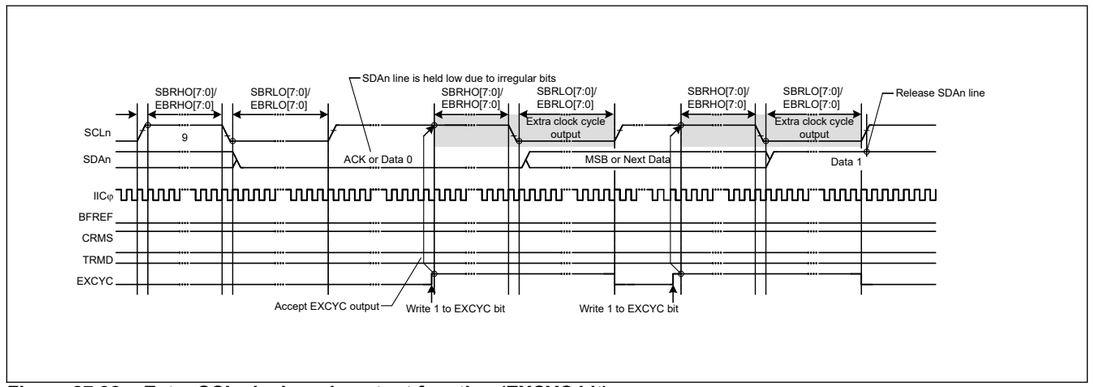


Figure 27.32 Extra SCL clock cycle output function (EXCYC bit)

27.3.1.3.7 SMBus Operation

IIC is available for data communication conforming to the SMBus (Version 2.0). To perform SMBus communication, set the BFCTL.SMBS bit to 1. To use the transfer rate within a range of 10 kbps to 100 kbps of the SMBus specification, set the REFCKCTL.IREFCKS[2:0] bits, the STDBR.SBRHO[7:0] bits, and the STDBR.SBRLO[7:0] bits. In addition, determine the values of the OUTCTL.SDODCS bit and the OUTCTL.SDOD[2:0] bits to meet the data hold time specification of 300 ns or more. If IIC is used only as an I^2C slave device, the transfer rate setting is not necessary, whereas the STDBR.SBRLO[7:0] bits needs to be set to a value longer than the data setup time (250 ns).

For the SMBus device default address (1100 001), use one of the slave device address table basic registers 0 to 2 (SDATBASy.SDSTAD[6:0] bits (y = 0 to 2), and set the corresponding SDATBASy.SDADLS bit (7-bit/10-bit address format select) (y = 0 to 2) to 0 (7-bit address format).

When transmitting the UDID (Unique Device Identifier), set the BFCTL.SALE bit to 1 to enable the slave arbitrationlost detection function.

(1) SMBus Timeout Measurement

(a) Measuring timeout of slave device

The following period (timeout interval: $T_{LOW:SEXT}$) must be measured for slave devices in SMBus communication.

- From START condition to STOP condition

To measure timeout for slave devices, measure the period from START condition detection to STOP condition detection with the GPT timer using a START condition detection interrupt (IICn_EEI) and STOP condition detection interrupt (IICn_EEI) of IIC. The measured timeout period must be within the total clock low-level period [slave device] $T_{LOW:SEXT}$: 25 ms (max.) of the SMBus specification.

If the time measured with the GPT exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (min.) of the SMBus specification, the slave device must release the bus by writing 1 to the RSTCTL.INTLRST bit to issue an internal reset of

条件是不可能的。SCL时钟的额外周期输出功能可用于逐个输出额外的SCL周期，使从设备释放SDAn线保持在低电平，从而使总线从不可用状态恢复。从设备释放SDAn线可以通过读取PRSTDBG中的SDILV位来监控。从设备释放SDAn线后，预设的重复启动条件或

发出停止条件。

在BFCTL.MALE位设置为0（禁用主机仲裁丢失检测）的情况下使用此功能。

[使用OUTCTL中的EXCYC位的输出条件]

●当总线空闲（BCST中的BFREF标志=1）或主机模式（PRSST中的CRMS位=1和BCST中的BFREF标志=0）时

●当通信设备不保持SCLn线为低电平时

图27.32显示了额外SCL时钟周期输出功能（EXCYC位）的操作时序。

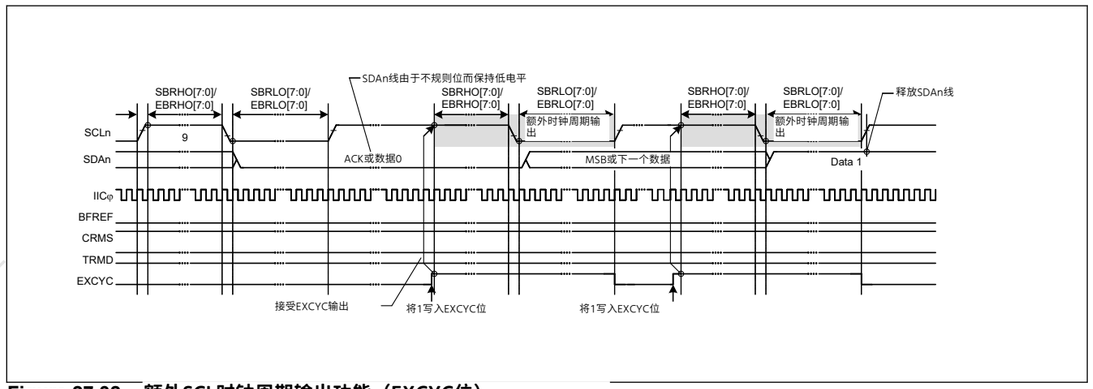


Figure 27.32 额外SCL时钟周期输出功能（EXCYC位）

27.3.1.3.7 SMBus Operation

IIC可用于符合SMBus（2.0版）的数据通信。要执行SMBus通信，请将BFCTL.SMBS位为1。要使用SMBus规范的10kbps到100kbps范围内的传输速率，请将REFCKCTL.IREFCKS[2:0]位、STDBR.SBRHO[7:0]位和STDBR.SBRLO[7:0]位。此外，确定OUTCTL.SDODCS位和OUTCTL.SDOD[2:0]位的值以满足300ns或更长的数据保持时间规范。如果IIC仅用作I2C从设备，则无需设置传输速率，而STDBR.SBRLO[7:0]位需要设置为比数据建立时间(250ns)更长的值。

对于SMBus设备默认地址（1100001），使用从设备地址表基本寄存器0到2之一（SDATBASy.SDSTAD[6:0]位（y=0到2），并设置相应的SDATBASy.SDADLS位（7位10位地址格式选择）（y=0到2）到0（7位地址格式）。

发送UDID（唯一设备标识符）时，将BFCTL.SALE位设置为1，以启用从设备仲裁丢失检测功能。

(1) SMBus超时测量

(a)测量从设备的超时

对于SMBus通信中的从设备，必须测量以下周期（超时间隔：TLOW:SEXT）。

●从START条件到STOP条件

要测量从设备的超时，请使用GPT定时器使用IIC的START条件检测中断(IICn_EEI)和STOP条件检测中断(IICn_EEI)测量从START条件检测到STOP条件检测的周期。测得的超时周期必须在总时钟低电平周期[从设备]TLOW:SEXT:SMBus规范的25毫秒（最大值）内。

如果使用GPT测量的时间超过时钟低电平检测超时TTIMEOUT:SMBus规范的25ms（分钟），从设备必须通过向RSTCTL.INTLRST位写入1来释放总线以发出内部复位的

IIC. When an internal reset is issued, IIC stops driving the bus for the SCLn pin and SDAn pin and make the SCLn/SDAn pin outputs high-impedance, which releases the bus.

(b) Measuring timeout of master device

The following periods (timeout interval: $T_{LOW:MEXT}$) must be measured for master devices in SMBus communication.

- From START condition to acknowledge bit
- Between acknowledge bits
- From acknowledge bit to STOP condition

To measure timeout for master devices, measure these periods with the GPT timer using a START condition detection interrupt (IICn_EEI), STOP condition detection interrupt (IICn_EEI), and transmit end interrupt (IICn_TEND) or receive data buffer full interrupt (IICn_RX) of IIC. The measured timeout period must be within the total clock lowlevel extended period (master device) $T_{LOW:MEXT}$: 10 ms (max.) of the SMBus specification, and the total of all $T_{LOW:MEXT}$ from START condition to STOP condition must be within $T_{LOW:SEXT}$: 25 ms (max.).

For the ACK receive timing (rising edge of the ninth SCL clock cycle), monitor the BST.TENDF flag in master transmit mode (master transmitter) and the NTST.RDBFF0 flag in master receive mode (master receiver). For this reason, perform bytewise transmit operation in master transmit mode, and hold the SCSTRCTL.ACKTWE bit 0 until the byte just before reception of the final byte in master receive mode. While the ACKTWE bit = 0, the RDBFF0 flag is set to 1 at the rising edge of the ninth SCL clock cycle.

If the period measured with the GPT exceeds the total clock low-level extended period (master device) $T_{LOW:MEXT}$: 10 ms (max.) of the SMBus specification or the total of measured periods exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (min.) of the SMBus specification, the master device must stop the transaction by issuing a STOP condition. In master transmit mode, immediately stop the transmit operation (writing data to NTDTBP0).

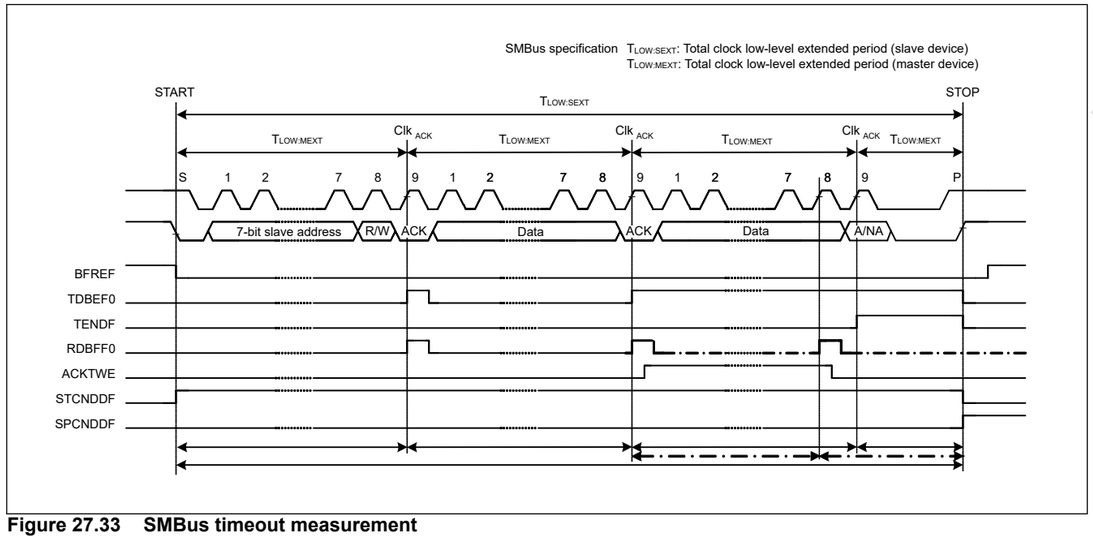


Figure 27.33 SMBus timeout measurement

(2) Packet Error Code (PEC)

This MCU incorporates a CRC calculator. The CRC calculator enables transmission of a packet error code (PEC) or checking the received data of the SMBus in data communication of IIC. For the CRC generating polynomials of the CRC calculator, see section 31, Cyclic Redundancy Check (CRC).

The PEC data in master transmit mode can be generated by writing all transmit data to the CRC data input register (CRCDIR) in the CRC calculator.

The PEC data in master receive mode can be checked by writing all receive data to CRCDIR in the CRC calculator and comparing the obtained value in the CRC data output register (CRCDOR) with the received PEC data.

国际集成电路。当内部复位发出时，IIC停止驱动SCLn引脚和SDAn引脚的总线，并使SCLnSDAn引脚输出高阻态，从而释放总线。

(b)测量主设备超时

对于SMBus通信中的主设备，必须测量以下周期（超时间隔：TLOW:MEXT）。

●从START条件到确认位

●确认位之间

●从确认位到停止条件

要测量主设备的超时，请使用GPT定时器使用IIC的START条件检测中断(IICn_EEI)、STOP条件检测中断(IICn_EEI)和发送结束中断(IICn_TEND)或接收数据缓冲区满中断(IICn_RX)来测量这些周期.测量的超时周期必须在总时钟低电平扩展周期（主设备）TLOW:MEXT：SMBus规范的10毫秒（最大值）内，并且从START条件到STOP条件的所有TLOW:MEXT的总和必须为在TLOW:SEXT内：25毫秒（最大）。

对于ACK接收时序（第9个SCL时钟周期的上升沿），在主机发送模式（主机发送器）和NTST.RDBFF0标志在主机接收模式（主机接收器）监视BST.TENDF标志。因此，在主机发送模式下执行逐字节发送操作，并保持SCSTRCTL.ACKTWE位0直到在主机接收模式下接收到最后一个字节之前的字节。当ACKTWE位=0时，RDBFF0标志在第9个SCL时钟周期的上升沿设置为1。

如果使用GPT测量的周期超过总时钟低电平扩展周期（主设备）TLOW:MEXT:SMBus规范的10ms（最大值）或总测量周期超过时钟低电平检测超时TTIMEOUT：SMBus规范的25ms（分钟），主设备必须通过发出STOP条件来停止事务。在主机发送模式下，立即停止发送操作（向NTDTBP0写入数据）。

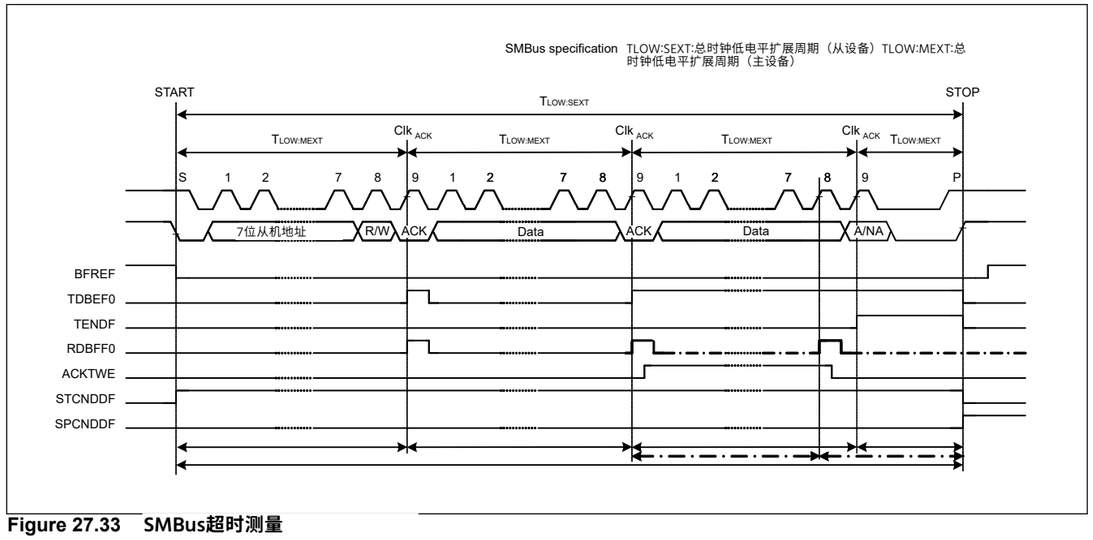


Figure 27.33 SMBus超时测量

(2) 数据包错误代码(PEC)

该MCU包含一个CRC计算器。CRC计算器可以传输数据包错误代码(PEC)或在IIC的数据通信中检查SMBus的接收数据。对于CRC生成多项式CRC计算器，参见第31节，循环冗余校验(CRC)。

主机发送模式下的PEC数据可以通过将所有发送数据写入CRC计算器中的CRC数据输入寄存器(CRCDIR)来生成。

通过将所有接收数据写入CRC计算器中的CRCDIR并将CRC数据输出寄存器(CRCDOR)中获得的值与接收到的PEC数据进行比较，可以检查主机接收模式下的PEC数据。

To send ACK or NACK according to the match or mismatch result when the final byte is received as a result of the PEC code check, set the SCSTRCTL.ACKTWE bit to 1 before the rising edge of the eighth SCL clock cycle during reception of the final byte, and hold the SCLn line low at the falling edge of the eighth clock cycle.

(3) SMBus Host Notification Protocol (Notify ARP Master Command)

In communications over an SMBus, a slave device can temporarily act as a master device to notify the SMBus host (or ARP master) of its own slave address or to request its own slave address from the SMBus host.

For a product of this MCU to operate as an SMBus host (or ARP master), the host address (0001 000) sent from the slave device must be detected as a slave address, so IIC has a function for detecting the host address. To detect the host address as a slave address, set the BFCTL.SMBS bit and the SVCTL.HOAE bit to 1. Operation after the host address has been detected is the same as normal slave operation.

27.3.1.4 Error Detection

27.3.1.4.1 Timeout Error Detection

IIC includes a timeout function for detecting when the SCLn line has been stuck longer than the predetermined time. IIC can detect an abnormal bus state by monitoring that the SCLn line is stuck low or high for a predetermined time.

The timeout function monitors the SCLn line state and counts the low-level period or high-level period using the internal counter. The timeout function resets the internal counter each time the SCLn line changes (rising or falling), but continues to count unless the SCLn line changes. If the internal counter overflows due to no SCLn line change, IIC can detect the timeout and report the bus hung state.

This timeout function is enabled when BSTE.TODE = 1. It detects a hung state that the SCLn line is stuck low or high during the following conditions: (When TMOCTL.TOMDS[1:0] = 00b)

- The bus is busy (BCST.BFREF = 0) in master mode (PRSST.CRMS = 1).
- IIC's own slave address is detected (SVST register is not 0x0000) and the bus is busy (BCST.BFREF = 0) in slave mode (PRSST.CRMS = 0).
- The bus is free (BCST.BFREF = 1) while generation of a START condition is requested (CNDCTL.STCND = 1).

要在接收到作为PEC代码检查的结果的最后一个字节时根据匹配或不匹配结果发送ACK或NACK，请在接收最后一个字节期间在第8个SCL时钟周期的上升沿之前将SCSTRCTL.ACKTWE位设置为1字节，并在第八个时钟周期的下降沿保持SCLn线为低电平。

(3) SMBus主机通知协议（通知ARP主机命令）

在通过SMBus进行通信时，从设备可以临时充当主设备来通知SMBus主机（或ARP主机）它自己的从地址或从SMBus主机请求它自己的从地址。

本MCU的产品要作为SMBus主机（或ARP主机）工作，从机发送的主机地址（0001000）必须被检测为从机地址，所以IIC具有主机地址检测功能。要将主机地址检测为从机地址，请将BFCTL.SMBS位和SVCTL.HOAE位设置为1。检测到主机地址后的操作与正常从机操作相同。

27.3.1.4 错误检测

27.3.1.4.1 超时错误检测

IIC包括一个超时功能，用于检测SCLn线路何时卡住超过预定时间。IIC可以通过监视SCLn线在预定时间内保持低电平或高电平来检测异常总线状态。

超时功能监控SCLn线路状态并使用内部计数器计算低电平周期或高电平周期。每次SCLn线改变（上升或下降）时，超时功能都会复位内部计数器，但除非SCLn线改变，否则会继续计数。如果内部计数器由于SCLn线没有变化而溢出，IIC可以检测到超时并报告总线挂起状态。

此超时功能在BSTE.TODE=1时启用。它在以下情况下检测到SCLn线卡在低电平或高电平的挂起状态：（当TMOCTL.TOMDS[1:0]=00b时）

●在主模式(PRSST.CRMS=1)中，总线繁忙(BCST.BFREF=0)。

●IIC自身的从机地址被检测到（SVST寄存器不是0x0000）并且在从机模式（PRSST.CRMS=0）下总线繁忙（BCST.BFREF=0）。

●总线空闲(BCST.BFREF=1)，同时请求生成START条件(CNDCTL.STCND=1)。

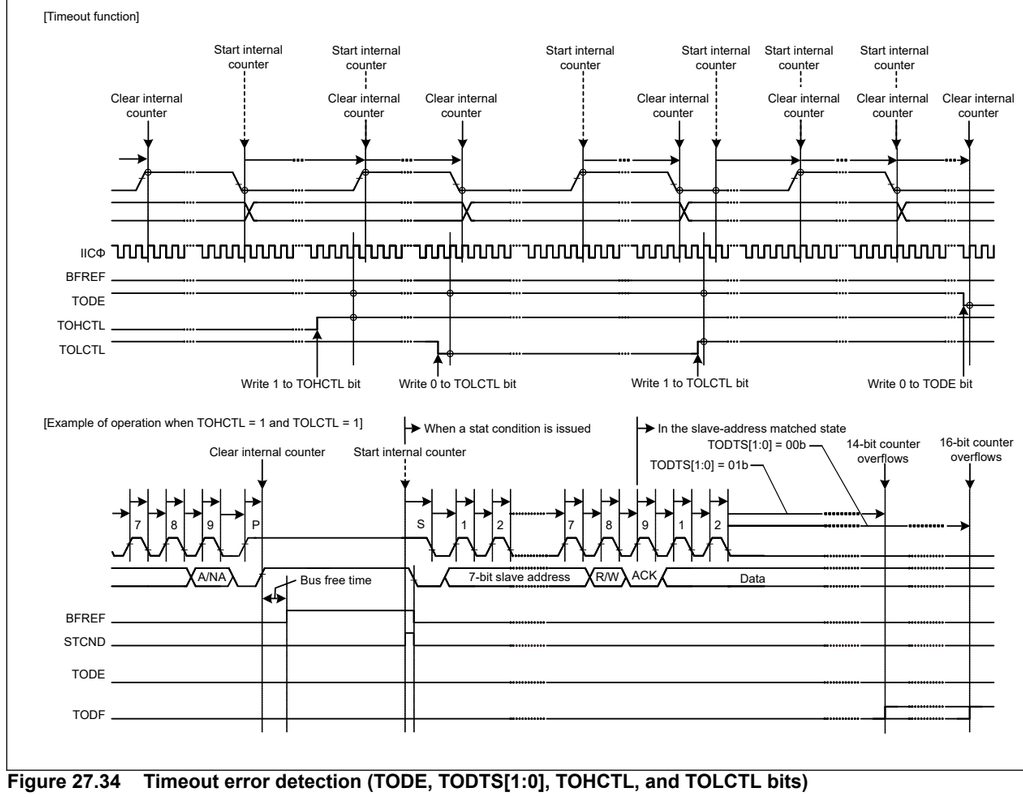


Figure 27.34 Timeout error detection (TODE, TODTS[1:0], TOHCTL, and TOLCTL bits)

27.3.1.5 Low Power Function

27.3.1.5.1 Wake Up function

IIC is equipped with the Wake-up function that causes the microcomputer to transition from low power consumption mode with system clock is stopped (software standby mode, snooze, etc.) to the normal operation. The Wake-up function is used to generate a Wake-up interrupt signal when the received data matches the address set to Wake-up interrupt factor also receives data in a state where the operating clock (PCLKA/IICCLK) is stopped (PCLKA/IICCLK asynchronous operation). This wake-up interrupt signal causes the microcomputer to transition to the normal operation. After Wake-up interrupt occurs, switch IIC to PCLKA/IICCLK synchronous operation, it will be able to continue the communication operation.

The Wake-up function has four wake-up operation modes (normal WU mode 1, normal WU mode 2, command recovery mode, and EEP response mode). The table below describes the behavior in these four wake-up operation modes.

Table 27.9 Wake-up operation mode (1 of 2)

	ACK response timing	ACK Type responded before recovery to PCLKA/IICCLK synchronous operation	SCL state before recovery to PCLKA/IICCLK synchronous operation
Normal WU mode 1	Before recovery to PCLKA/IICCLK synchronous operation*1	ACK	Fixed to L
Normal WU mode 2	After recovery to PCLKA/IICCLK synchronous operation*2	Before recovery: no response (NACK level retained) After recovery: ACK response	Fixed to L
Command recovery mode	Before recovery to PCLKA/IICCLK synchronous operation*1	ACK	Open

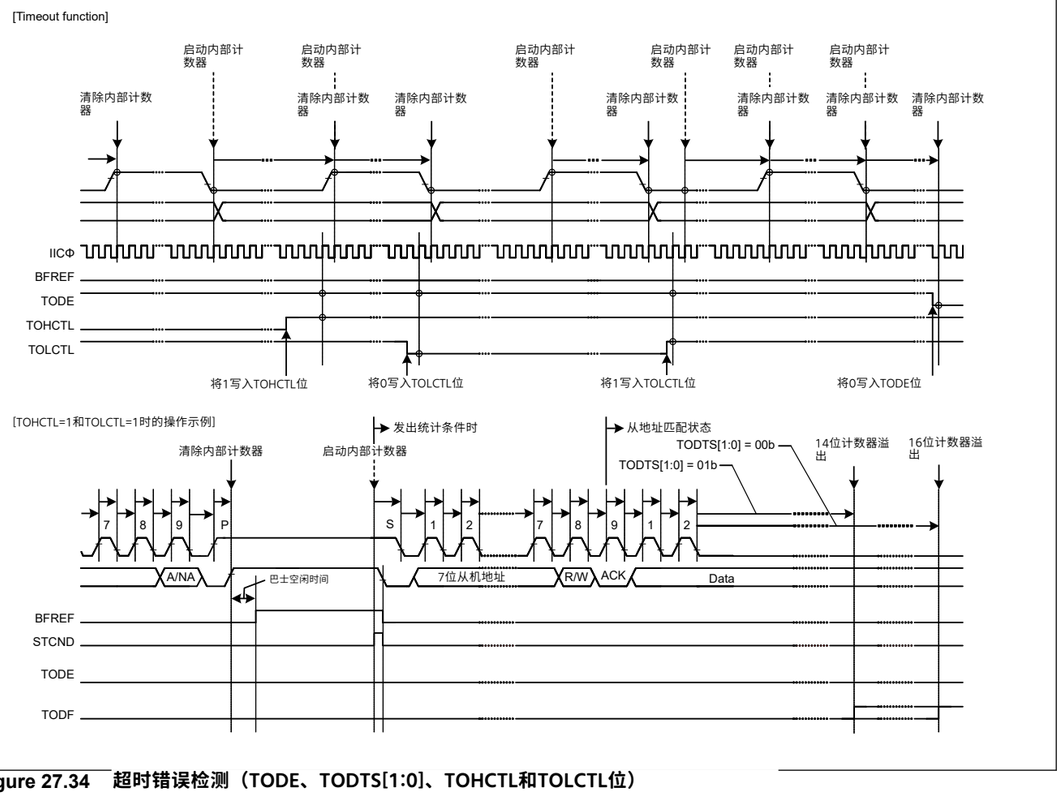


Figure 27.34 超时错误检测（TODE、TODTS[1:0]、TOHCTL和TOLCTL位）

27.3.1.5 低功耗功能

27.3.1.5.1 唤醒功能

IIC配备唤醒功能，使微机在系统时钟停止（软件待机模式、贪睡等）时从低功耗模式转换到正常操作。唤醒功能用于在接收到的数据与设置为唤醒中断因子的地址匹配时生成唤醒中断信号，同时在工作时钟（PCLKAIICCLK）停止（PCLKAIICCLK异步操作）的状态下接收数据）。该唤醒中断信号使微型计算机转变为正常操作。唤醒中断发生后，将IIC切换到PCLKAIICCLK同步操作，即可继续通讯操作。

唤醒功能有四种唤醒操作模式（正常WU模式1、正常WU模式2、命令恢复模式和EEP响应模式）。下表描述了这四种唤醒操作模式下的行为。

Table 27.9 唤醒操作模式(1of2)

	ACK响应时间	ACK类型在恢复到PCLKAIICCLK同步操作之前响应	恢复到PCLKAIICCLK同步操作之前的SCL状态
普通WU模式1	恢复到PCLKA之前IICCLK同步操作*1	ACK	固定为L
普通WU模式2	恢复到PCLKAIICCLK同步操作后*2	恢复前：无响应（保留NACK电平）恢复后：ACK响应	固定为L
命令恢复模式	恢复到PCLKA之前IICCLK同步操作*1	ACK	Open

Table 27.9 Wake-up operation mode (2 of 2)

	ACK response timing	ACK Type responded before recovery to PCLKA/IICCLK synchronous operation	SCL state before recovery to PCLKA/IICCLK synchronous operation
EEP response mode	Before recovery to PCLKA/IICCLK synchronous operation*1	NACK	Open

Note 1. Switching timing from PCLKA/IICCLK asynchronous operation to PCLKA/IICCLK synchronous operation is the fall of the 9th clock of SCL.
Note 2. Switching timing from PCLKA/IICCLK asynchronous operation to PCLKA/IICCLK synchronous operation is the fall of the 8th clock of SCL.

The following is able to select as Wake-Up interrupt factor.

- Host address detection (valid when SVCTL.HOAE = 1)
- General call address detection (valid when SVCTL.GCAE = 1)
- Slave address 0*1 detection (valid when SVCTL.SVAE0 = 1)
- Slave address 1*1 detection (valid when SVCTL.SVAE1 = 1)
- Slave address 2*1 detection (valid when SVCTL.SVAE2 = 1)

Note 1. 7-bit address only can be set. Set SDADLS bit to 0 in SDATBASy.

(1) Normal Wake-Up mode 1

This section describes the behavior, the timing, and a use case of normal WU mode 1.

A wake-up interrupt triggered by the match of the slave address makes the transition to the normal operation in the manner described below. Also, the detailed timing is provided in Figure 27.37.

Before wake-up recovery:	ACK is sent in response to the data received with its own slave address.
During wake-up recovery:	ACK response is made at the 9th clock cycle of SCL, and the SCL is held low afterwards.*1
After wake-up recovery:	Normal operation continues.

Note 1. Between ninth clock cycle and first clock cycle during Wake-Up recovery, SCSTRCTL.RWE = 1 does not work.

If the slave address does not match, the SCL line is not held low after the fall of the 9th clock cycle of SCL, and the slave operation continues.

See Figure 27.35 below for a use case.

A wake-up interrupt is not generated at the transition to the normal operation if the transition is triggered by a cause (other recovery causes (IRQ)) other than a wake-up interrupt signal generated by a slave address match. BST.WUCNDDF is not set in this case. Carry out the following processing according to Figure 27.36.

Table 27.9 唤醒操作模式(2of2)

	ACK响应时间	ACK类型在恢复到PCLKAIICCLK同步操作之前响应	恢复到PCLKAIICCLK同步操作之前的SCL状态
EEP响应模式	恢复到PCLKA之前IICCLK同步操作*1	NACK	Open

注1.从PCLKAIICCLK异步操作切换到PCLKAIICCLK同步操作的时序是SCL的第9个时钟的下降沿。

注2.从PCLKAIICCLK异步操作切换到PCLKAIICCLK同步操作的时序是SCL的第8个时钟的下降沿。

以下可以选择作为唤醒中断因素。

- ●主机地址检测（SVCTL.HOAE=1时有效）
- ●广播地址检测（SVCTL.GCAE=1时有效）
- ●从机地址0*1检测（SVCTL.SVAE0=1时有效）
- ●从机地址1*1检测（SVCTL.SVAE1=1时有效）
- ●从机地址2*1检测（SVCTL.SVAE2=1时有效）

注1.只能设置7位地址。在SDATBASy中将SDADLS位设置为0。

(1) 正常唤醒模式1

本节介绍正常WU模式1的行为、时序和用例。

从机地址匹配触发的唤醒中断以下述方式转换到正常操作。此外，图27.37中提供了详细的时序。

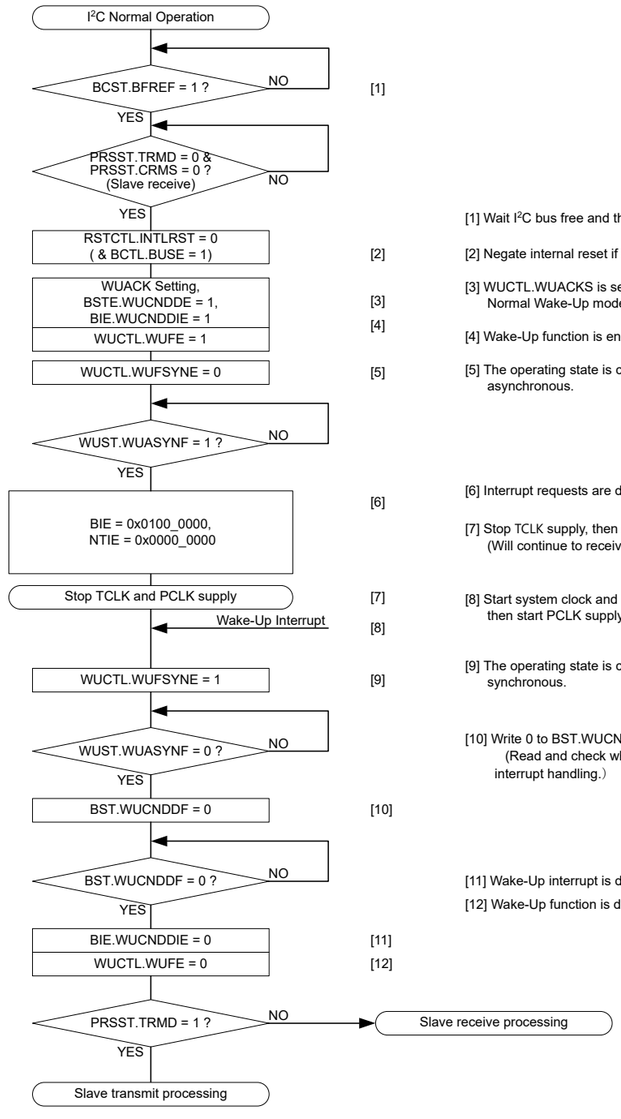
Before wake-up recovery:	ACK是响应接收到的数据而发送的，带有它自己的从地址。
During wake-up recovery:	在SCL的第9个时钟周期做出ACK响应，之后SCL保持低电平。*1
After wake-up recovery:	正常操作继续。

注1.在唤醒恢复期间的第9个时钟周期和第一个时钟周期之间，SCSTRCTL.RWE=1不起作用。

如果从机地址不匹配，则在SCL的第9个时钟周期下降后，SCL线不保持低电平，从机操作继续。

有关用例，请参见下面的图27.35。

如果转换是由除从地址匹配产生的唤醒中断信号之外的原因（其他恢复原因(IRQ)）触发的，则在转换到正常操作时不会产生唤醒中断。在这种情况下未设置BST.WUCNDDF。按照图27.36进行如下处理。



[1] Wait I²C bus free and this module*1 stay in the standby state.

[2] Negate internal reset if assert the internal reset.

[3] WUCTL.WUACKS is set up according to each mode. (Normal Wake-Up mode 1/ Normal Wake-Up mode 2) Wake-Up Interrupt is enabled.

[4] Wake-Up function is enabled.

[5] The operating state is changed from PCLK/TCLK synchronous to PCLK/TCLK asynchronous.

[6] Interrupt requests are disabled except WUI.

[7] Stop TCLK supply, then stop PCLK supply. (Will continue to receive)

[8] Start system clock and TCLK supply by Wake-Up interrupt (address match), then start PCLK supply.

[9] The operating state is changed from PCLK/TCLK asynchronous to PCLK/TCLK synchronous.

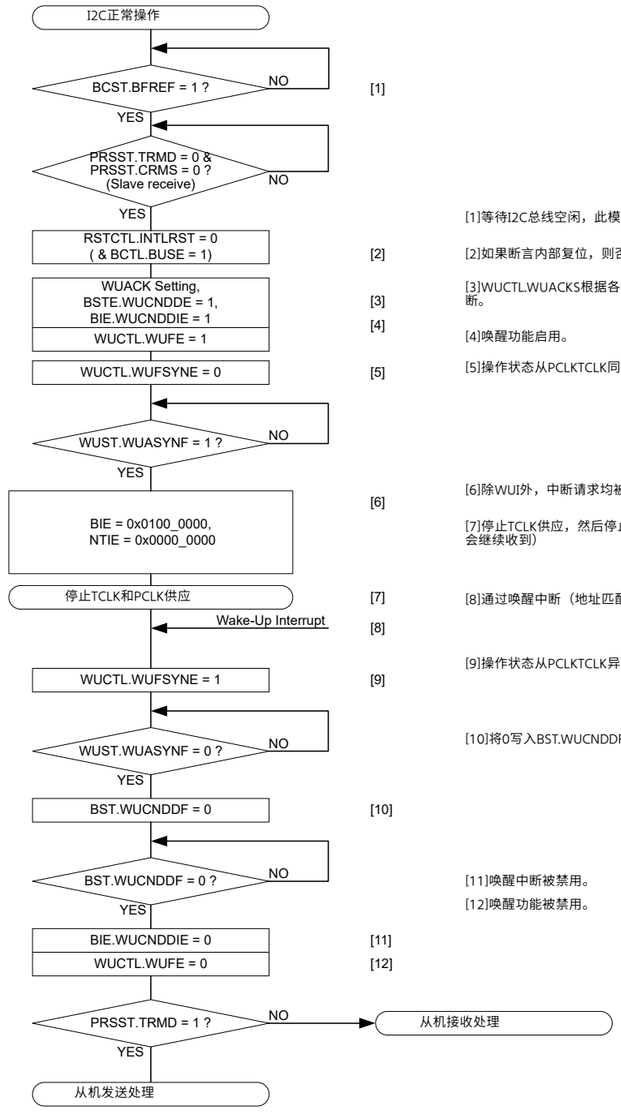
[10] Write 0 to BST.WUCNDDF. (Read and check whether clearing has been completed befor return from interrupt handling.)

[11] Wake-Up interrupt is disabled.

[12] Wake-Up function is disabled.

Note: TCLK = IICCLK
PCLK = PCLKA

Figure 27.35 Use case of normal WU mode 1 (wake-up recovery by a wake-up interrupt triggered by the match of the slave address)



[1]等待I2C总线空闲，此模块*1保持待机状态。

[2]如果断言内部复位，则否定内部复位。

[3]WUCTL.WUACKS根据各模式设定。（正常唤醒模式1正常唤醒模式2）启用唤醒中断。

[4]唤醒功能启用。

[5]操作状态从PCLKTCLK同步变为PCLKTCLK异步。

[6]除WUI外，中断请求均被禁用。

[7]停止TCLK供应，然后停止PCLK供应。（会继续收到）

[8]通过唤醒中断（地址匹配）启动系统时钟和TCLK供应，然后启动PCLK供应。

[9]操作状态从PCLKTCLK异步变为PCLKTCLK同步。

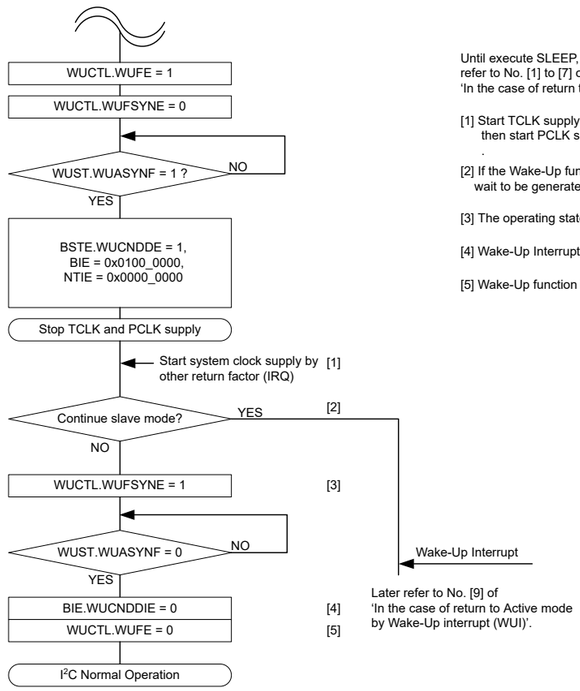
[10]将0写入BST.WUCNDDF。（从中断处理返回前读取并检查是否已完成清除。）

[11]唤醒中断被禁用。

[12]唤醒功能被禁用。

Note: TCLK = IICCLK
PCLK = PCLKA

Figure 27.35 普通WU模式1的用例（从机地址匹配触发唤醒中断唤醒恢复）



Until execute SLEEP, it is the same method,
refer to No. [1] to [7] of
'In the case of return to Active mode by Wake-Up interrupt (WUI)'.

[1] Start TCLK supply by other return factor (IRQ),
then start PCLK supply.
.

[2] If the Wake-Up function is used continuously by the slave mode,
wait to be generated of the Wake-Up interrupt request.

[3] The operating state is changed from PCLK/TCLK asynchronous to PCLK/TCLK synchronous.

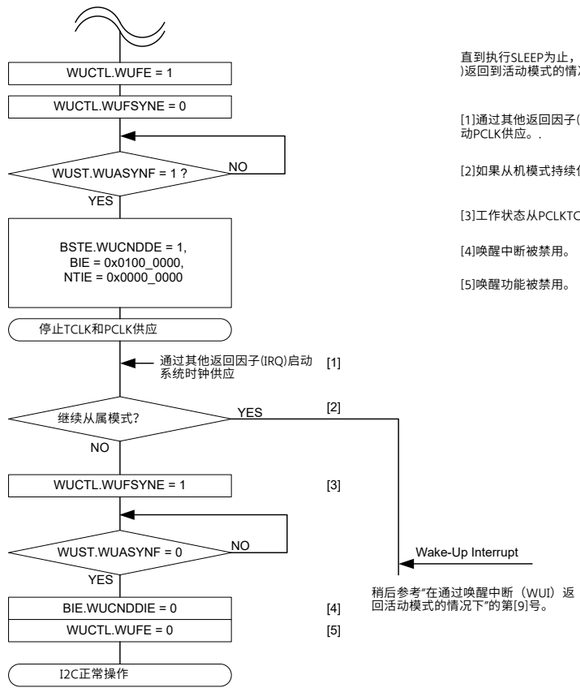
[4] Wake-Up Interrupt is disabled.

[5] Wake-Up function is disabled.

Later refer to No. [9] of
'In the case of return to Active mode
by Wake-Up interrupt (WUI)'.

Note: TCLK = IICCLK
PCLK = PCLKA

Figure 27.36 Use case of normal WU modes 1 and 2 (wake-up recovery by other recovery causes (IRQ))



直到执行SLEEP为止，都是同样的方法，请参考'通过唤醒中断(WUI)返回到活动模式的情况下'的第[1]至[7]项。

[1]通过其他返回因子(IRQ)启动TCLK供应，然后启动PCLK供应。.

[2]如果从机模式持续使用唤醒功能，则等待唤醒中断请求的产生。

[3]工作状态从PCLKTCLK异步变为PCLKTCLK同步。

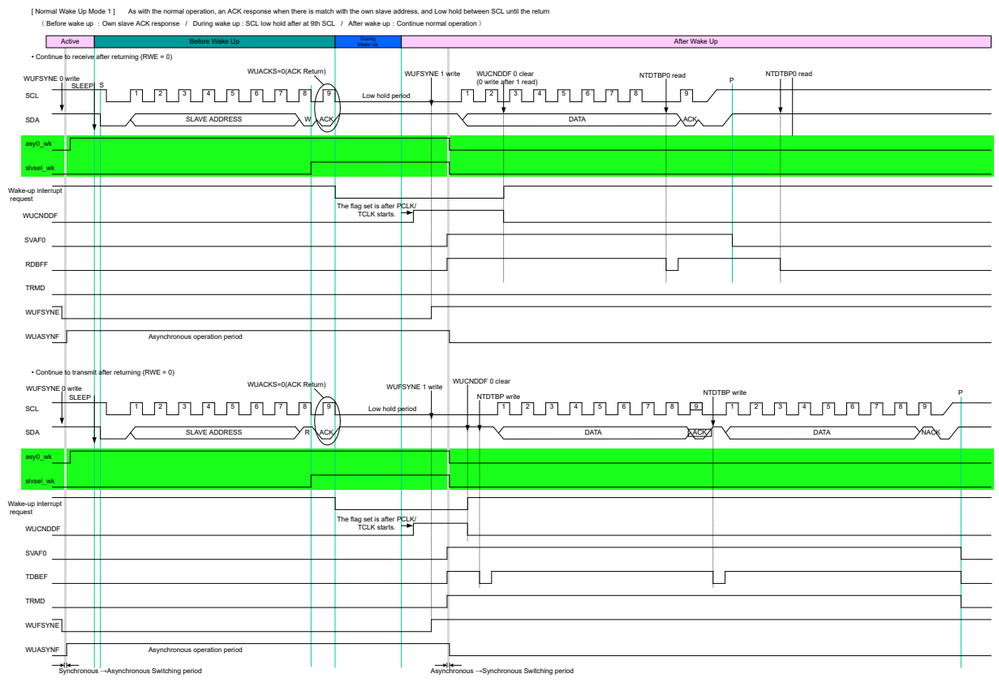
[4]唤醒中断被禁用。

[5]唤醒功能被禁用。

稍后参考"在通过唤醒中断（WUI）返回活动模式的情况下"的第[9]号。

Note: TCLK = IICCLK
PCLK = PCLKA

Figure 27.36 正常WU模式1和2的用例（由其他恢复原因（IRQ）唤醒恢复）



Note: TCLK = IICCLK
PCLK = PCLKA

Figure 27.37 Timing of normal wake up mode 1

(2) Normal Wake Up Mode 2

This section describes the behavior, the timing, and a use case of normal WU mode 2.

A wake-up interrupt triggered by the match of the slave address makes the transition to the normal operation in the manner described below.

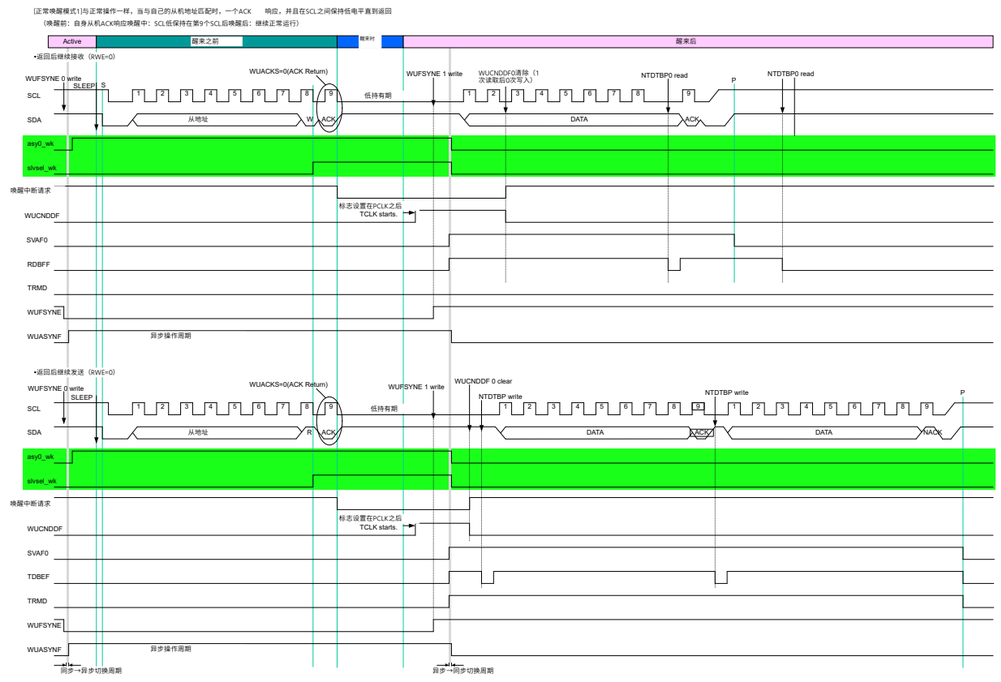
Also, the detailed timing is provided in Figure 27.39.

Before wake-up recovery:	No response to the data received with its own slave address (until 8th SCL cycle end)
During wake-up recovery:	Holding the SCL line low during the 8th and 9th clock cycles
After wake-up recovery:	Returning ACK at the 9th clock cycle of SCL, and continuing the normal operation

If the slave address does not match, the SCL line is not held low after the fall of the 8th SCL v clock cycle. The slave operation continues.

See Figure 27.38 below for a use case.

A wake-up interrupt is not generated at the transition to the normal operation if the transition is triggered by a cause (other recovery causes (IRQ)) other than a wake-up interrupt signal generated by a slave address match. BST.WUCNDDF is not set in this case. Carry out the following processing according to Figure 27.36.



Note: TCLK = IICCLK
PCLK = PCLKA

Figure 27.37 正常唤醒模式1的时序

(2) 正常唤醒模式2

本节介绍正常WU模式2的行为、时序和用例。

从机地址匹配触发的唤醒中断以下述方式转换到正常操作。

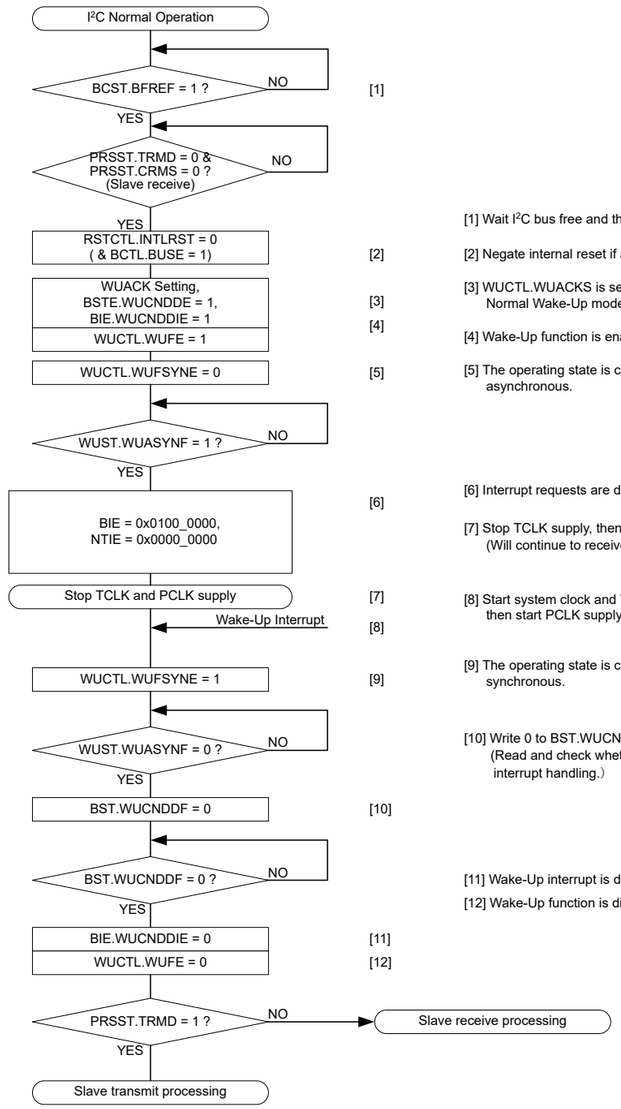
此外，图27.39中提供了详细的时序。

Before wake-up recovery:	对接收到的带有自己的从机地址的数据没有响应（直到第8个SCL周期结束）
During wake-up recovery:	在第8和第9个时钟周期内保持SCL线为低电平
After wake-up recovery:	在SCL的第9个时钟周期返回ACK，并继续正常运行

如果从地址不匹配，则在第8个SCLv时钟周期下降后，SCL线不会保持低电平。从操作继续。

有关用例，请参见下面的图27.38。

如果转换是由除从地址匹配产生的唤醒中断信号之外的原因（其他恢复原因(IRQ)）触发的，则在转换到正常操作时不会产生唤醒中断。在这种情况下未设置BST.WUCNDDF。按照图27.36进行如下处理。



[1] Wait I²C bus free and this module stay in the standby state.

[2] Negate internal reset if assert the internal reset.

[3] WUCTL.WUACKS is set up according to each mode. (Normal Wake-Up mode 1/ Normal Wake-Up mode 2) Wake-Up Interrupt is enabled.

[4] Wake-Up function is enabled.

[5] The operating state is changed from PCLK/TCLK synchronous to PCLK/TCLK asynchronous.

[6] Interrupt requests are disabled except WUI.

[7] Stop TCLK supply, then stop PCLK supply. (Will continue to receive）

[8] Start system clock and TCLK supply by Wake-Up interrupt (address match), then start PCLK supply.

[9] The operating state is changed from PCLK/TCLK asynchronous to PCLK/TCLK synchronous.

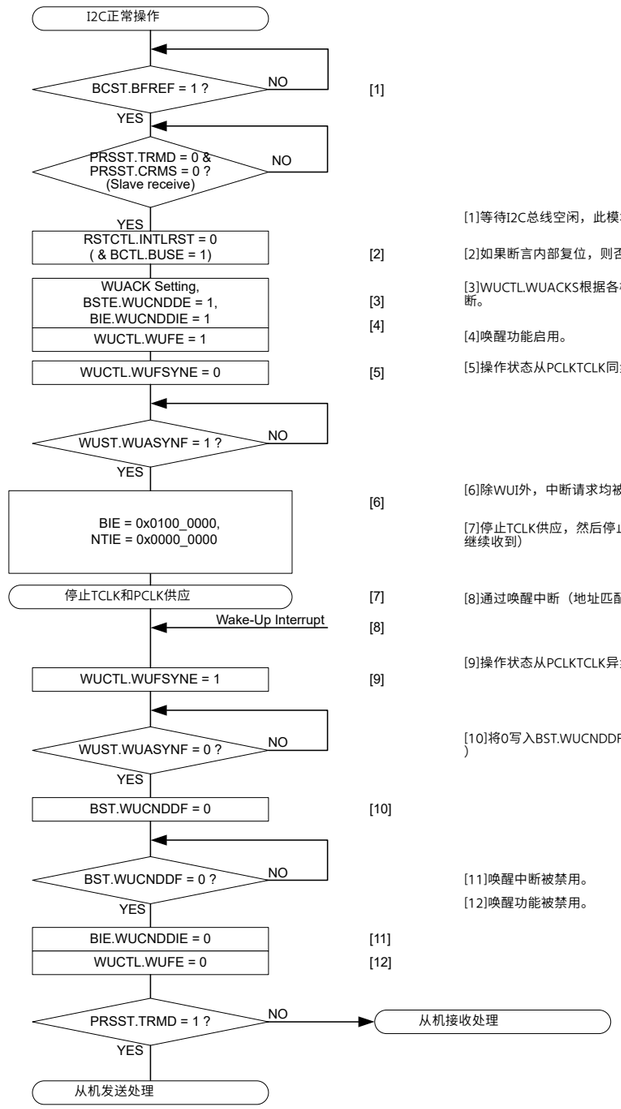
[10] Write 0 to BST.WUCNDDF. (Read and check whether clearing has been completed befor return from interrupt handling.）

[11] Wake-Up interrupt is disabled.

[12] Wake-Up function is disabled.

Note: TCLK = IICCLK
PCLK = PCLKA

Figure 27.38 Use case of normal WU mode 2 (wake-up recovery by a wake-up interrupt triggered by the match of the slave address)



[1]等待I2C总线空闲，此模块处于待机状态。

[2]如果断言内部复位，则否定内部复位。

[3]WUCTL.WUACKS根据各模式设定。（正常唤醒模式1正常唤醒模式2）启用唤醒中断。

[4]唤醒功能启用。

[5]操作状态从PCLKTCLK同步变为PCLKTCLK异步。

[6]除WUI外，中断请求均被禁用。

[7]停止TCLK供应，然后停止PCLK供应。（会继续收到）

[8]通过唤醒中断（地址匹配）启动系统时钟和TCLK供应，然后启动PCLK供应。

[9]操作状态从PCLKTCLK异步变为PCLKTCLK同步。

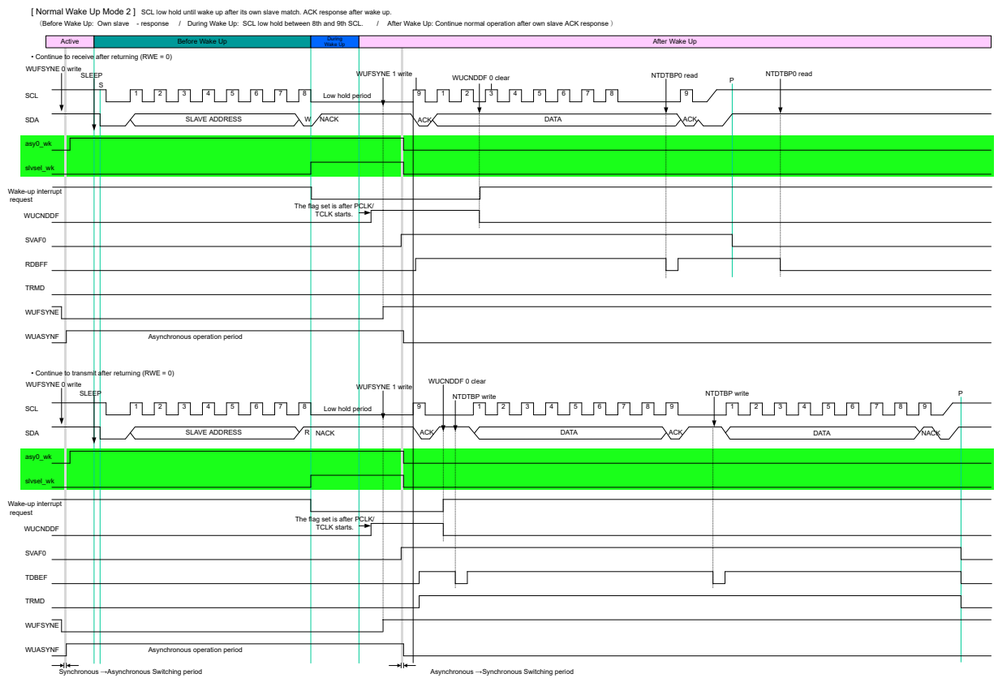
[10]将0写入BST.WUCNDDF。（从中断处理返回前读取并检查是否已完成清除。）

[11]唤醒中断被禁用。

[12]唤醒功能被禁用。

Note: TCLK = IICCLK
PCLK = PCLKA

Figure 27.38 普通WU模式2的用例（通过从地址匹配触发的唤醒中断唤醒恢复）



Note: TCLK = IICCLK
PCLK = PCLKA

Figure 27.39 Timing of normal wake up mode 2

(3) Command recovery mode/ EEP response mode (Special Wake Up mode)

In the command recovery mode and EEP response mode, the SCL line is not held low during the wake-up recovery period (after the rise of the 9th clock cycle of SCL), so other I^2C devices can use the I^2C bus during this period. This section describes the behavior, the timing, and use cases of the command recovery mode and the EEP response mode.

A wake-up interrupt triggered by the match of the slave address makes the transition to the normal operation in the manner described below. Also, the detailed timing is provided in Figure 27.42.

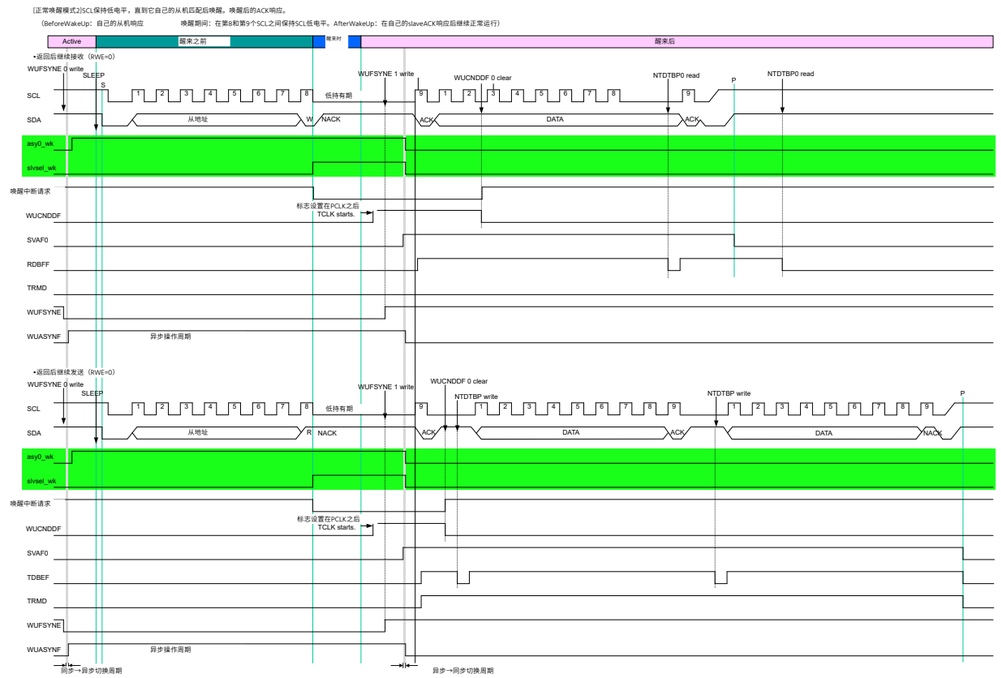
Before wake-up recovery:	In response to the data received with its own slave address, ACK (command recovery mode) or NACK (EEP response mode) is returned.
During wake-up recovery:	The SCL line is not held low.
After wake-up recovery:	Normal operation continues after IIC initial setting.

Note: Because the SCL line is not held low during wake-up recovery, the transmission/reception of the data that follows the slave address is not possible.
Note: The command recovery mode and the EEP response mode are internal reset (RSTCTL.INTLRST = 1) states. Therefore, the match of the slave address does not set the SVST flags (HOAF, GCAF, and SVAF2, SVAF1, SVAF0).

If the slave address does not match, the slave operation continues.

See Figure 27.41 below for a use case.

A wake-up interrupt is not generated at the transition to the normal operation if the transition is triggered by a cause (other recovery causes (IRQ)) other than a wake-up interrupt signal generated by a slave address match. BST.WUCNDDF is not set in this case. Carry out the following processing according to Figure 27.41.



Note: TCLK = IICCLK
PCLK = PCLKA

Figure 27.39 正常唤醒模式2的时序

(3) 命令恢复模式EEP响应模式（特殊唤醒模式）

在命令恢复模式和EEP响应模式下，SCL线在唤醒恢复期间（SCL第9个时钟周期上升后）不保持低电平，因此其他I2C设备可以使用I2C总线在这段时期。本节介绍命令恢复模式和EEP响应模式的行为、时序和用例。

从机地址匹配触发的唤醒中断以下述方式转换到正常操作。此外，图27.42中提供了详细的时序。

Before wake-up recovery:	以自己的从机地址接收到的数据，返回ACK（命令恢复模式）或NACK（EEP响应模式）。
During wake-up recovery:	SCL线没有保持低电平。
After wake-up recovery:	IIC初始设置后继续正常操作。

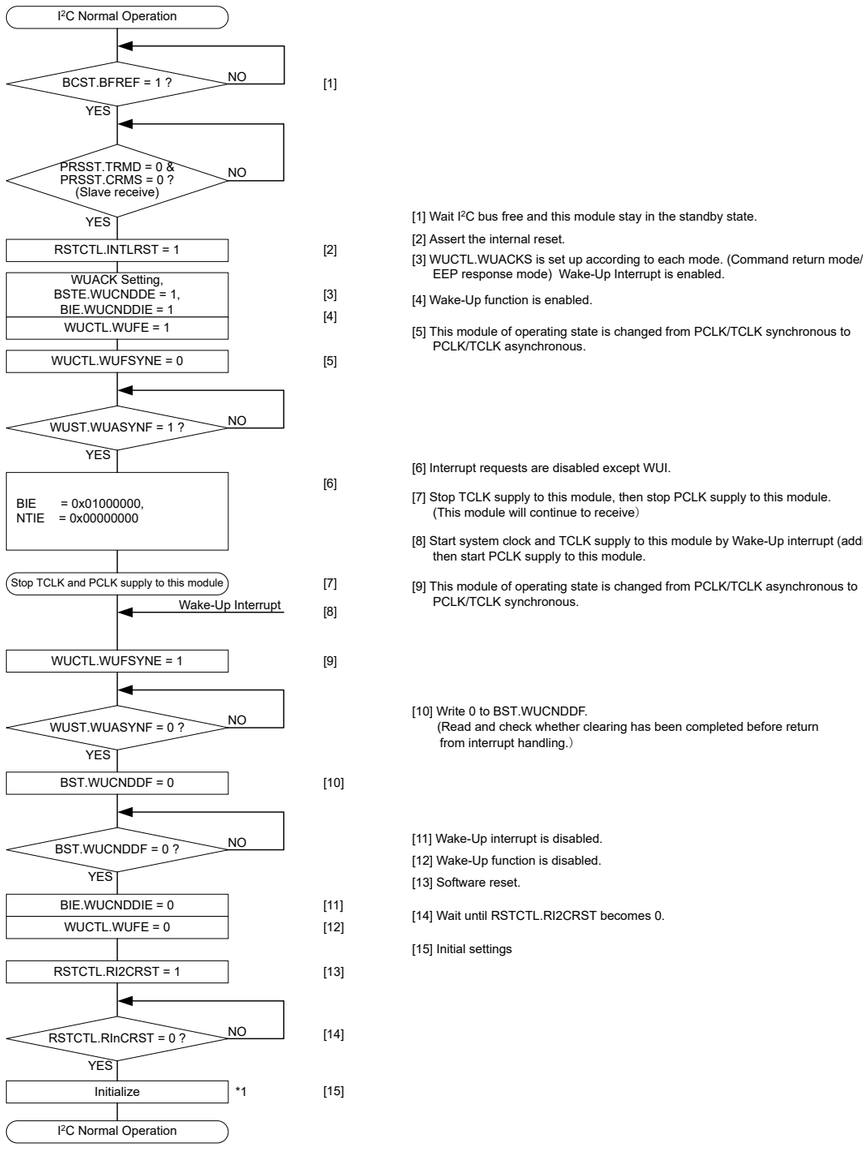
Note: 由于在唤醒恢复期间SCL线不保持低电平，因此无法发送接收从地址之后的数据。

Note: 命令恢复模式和EEP响应模式是内部复位(RSTCTL.INTLRST=1)状态。因此，从地址的匹配不会设置SVST标志（HOAF、GCAF和SVAF2、SVAF1、SVAF0）。

如果从机地址不匹配，从机操作继续。

有关用例，请参见下面的图27.41。

如果转换是由除从地址匹配产生的唤醒中断信号之外的原因（其他恢复原因(IRQ)）触发的，则在转换到正常操作时不会产生唤醒中断。在这种情况下未设置BST.WUCNDDF。按照图27.41进行如下处理。



[1] Wait I²C bus free and this module stay in the standby state.

[2] Assert the internal reset.

[3] WUCTL.WUACKS is set up according to each mode. (Command return mode/ EEP response mode) Wake-Up Interrupt is enabled.

[4] Wake-Up function is enabled.

[5] This module of operating state is changed from PCLK/TCLK synchronous to PCLK/TCLK asynchronous.

[6] Interrupt requests are disabled except WUI.

[7] Stop TCLK supply to this module, then stop PCLK supply to this module. (This module will continue to receive)

[8] Start system clock and TCLK supply to this module by Wake-Up interrupt (address match), then start PCLK supply to this module.

[9] This module of operating state is changed from PCLK/TCLK asynchronous to PCLK/TCLK synchronous.

[10] Write 0 to BST.WUCNDDF.
(Read and check whether clearing has been completed before return from interrupt handling.)

[11] Wake-Up interrupt is disabled.

[12] Wake-Up function is disabled.

[13] Software reset.

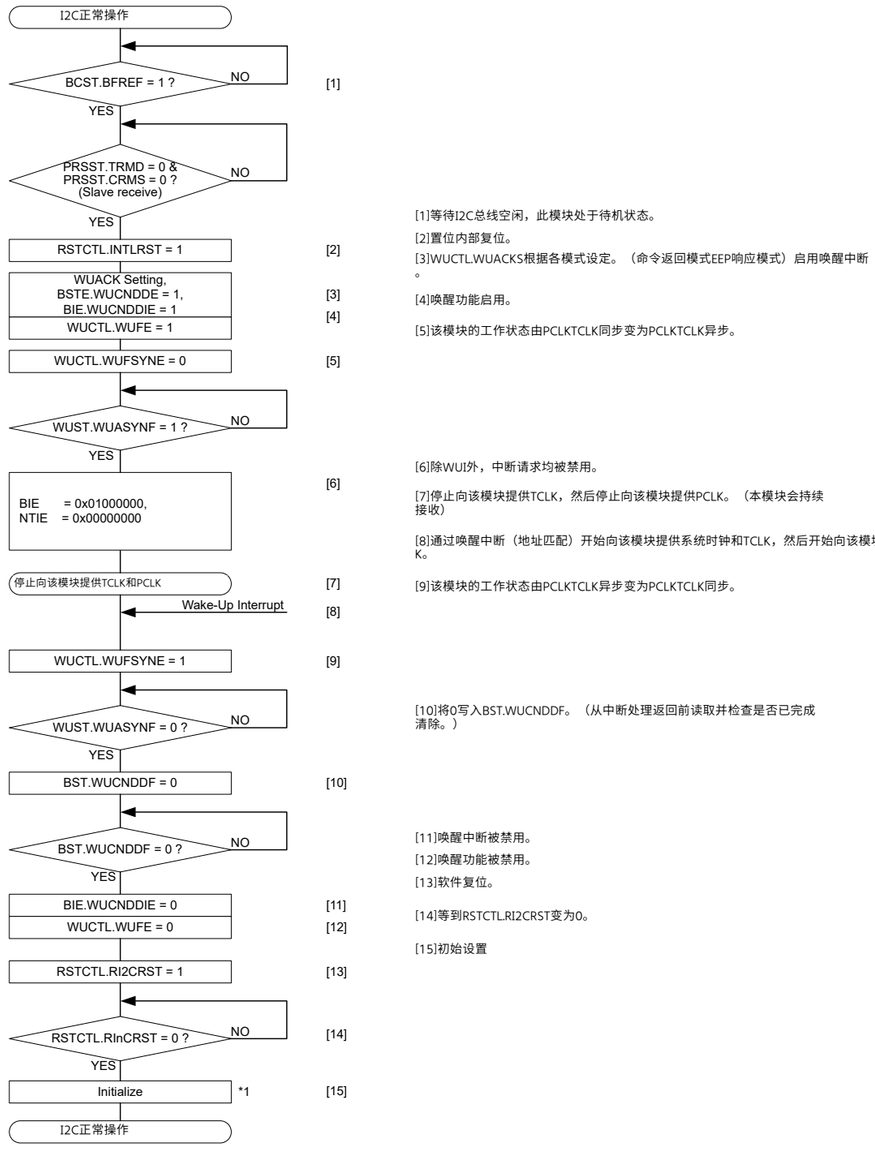
[14] Wait until RSTCTL.RI2CRST becomes 0.

[15] Initial settings

Note: TCLK = IICCLK
PCLK = PCLKA

Note 1. See section 27.3.2.1. Initial Setting Flow for details of initialization.

Figure 27.40 Use case of command recover mode and EEP response mode (wake-up recovery by a wake-up interrupt triggered by the match of the slave address)



[1]等待I2C总线空闲，此模块处于待机状态。

[2]置位内部复位。

[3]WUCTL.WUACKS根据各模式设定。（命令返回模式EEP响应模式）启用唤醒中断。

[4]唤醒功能启用。

[5]该模块的工作状态由PCLKTCLK同步变为PCLKTCLK异步。

[6]除WUI外，中断请求均被禁用。

[7]停止向该模块提供TCLK，然后停止向该模块提供PCLK。（本模块会持续接收）

[8]通过唤醒中断（地址匹配）开始向该模块提供系统时钟和TCLK，然后开始向该模块提供PCLK。

[9]该模块的工作状态由PCLKTCLK异步变为PCLKTCLK同步。

[10]将0写入BST.WUCNDDF。（从中断处理返回前读取并检查是否已完成清除。）

[11]唤醒中断被禁用。

[12]唤醒功能被禁用。

[13]软件复位。

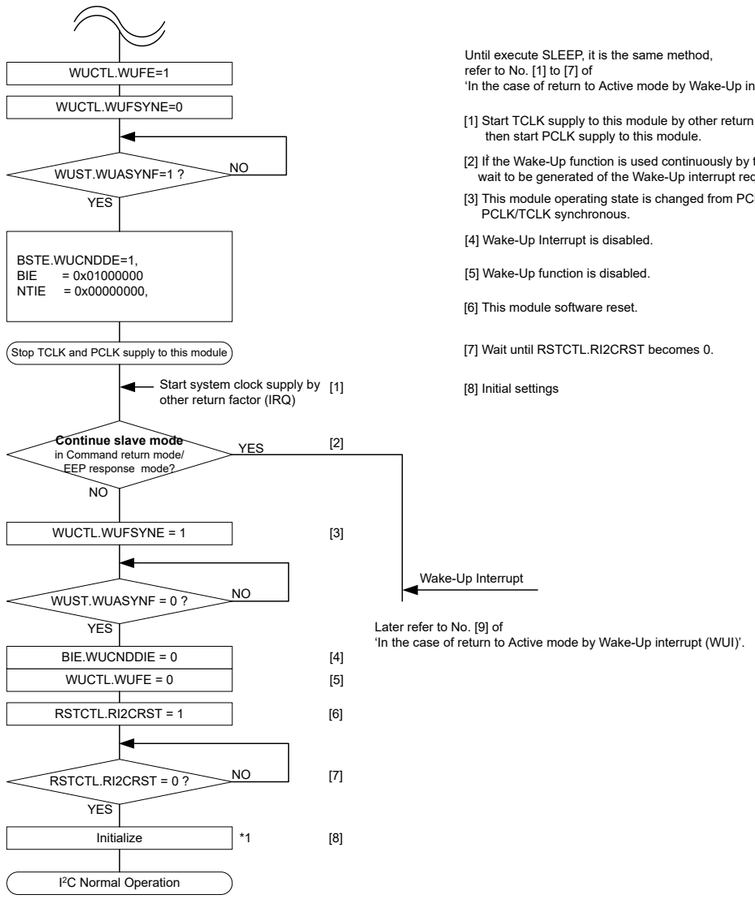
[14]等到RSTCTL.RI2CRST变为0。

[15]初始设置

Note: TCLK = IICCLK
PCLK = PCLKA

注1.见第27.3.2.1节。初始化详细信息的初始化设置流程。

Figure 27.40 命令恢复模式和EEP响应模式的使用案例（通过从地址匹配触发的唤醒中断唤醒恢复）



Until execute SLEEP, it is the same method,
refer to No. [1] to [7] of
'In the case of return to Active mode by Wake-Up interrupt (WUI)'.

[1] Start TCLK supply to this module by other return factor (IRQ),
then start PCLK supply to this module.

[2] If the Wake-Up function is used continuously by the slave mode,
wait to be generated of the Wake-Up interrupt request.

[3] This module operating state is changed from PCLK/TCLK asynchronous to PCLK/TCLK synchronous.

[4] Wake-Up Interrupt is disabled.

[5] Wake-Up function is disabled.

[6] This module software reset.

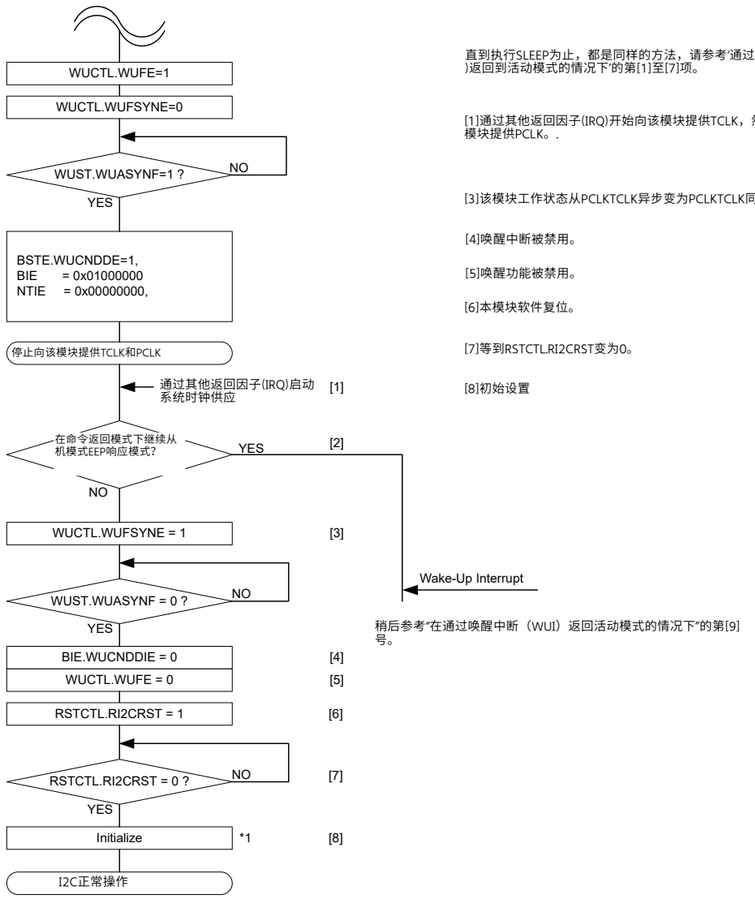
[7] Wait until RSTCTL.RI2CRST becomes 0.

[8] Initial settings

Later refer to No. [9] of
'In the case of return to Active mode by Wake-Up interrupt (WUI)'.

Note: TCLK = IICCLK
PCLK = PCLKA
Note 1. See section 27.3.2.1. Initial Setting Flow for details of initialization.

Figure 27.41 Use case of command recover mode and EEP response mode (wake-up recovery by other recovery causes (IRQ))



直到执行SLEEP为止，都是同样的方法，请参考"通过唤醒中断(WUI)返回到活动模式的情况下"的第[1]至[7]项。

[1]通过其他返回因子(IRQ)开始向该模块提供TCLK，然后开始向该模块提供PCLK。.

[3]该模块工作状态从PCLKTCLK异步变为PCLKTCLK同步。

[4]唤醒中断被禁用。

[5]唤醒功能被禁用。

[6]本模块软件复位。

[7]等到RSTCTL.RI2CRST变为0。

[8]初始设置

稍后参考"在通过唤醒中断（WUI）返回活动模式的情况下"的第[9]号。

Note: TCLK = IICCLK
PCLK = PCLKA
注1.见第27.3.2.1节。初始化详细信息的初始化设置流程。

Figure 27.41 命令恢复模式和EEP响应模式的用例（由其他恢复原因（IRQ）唤醒恢复）

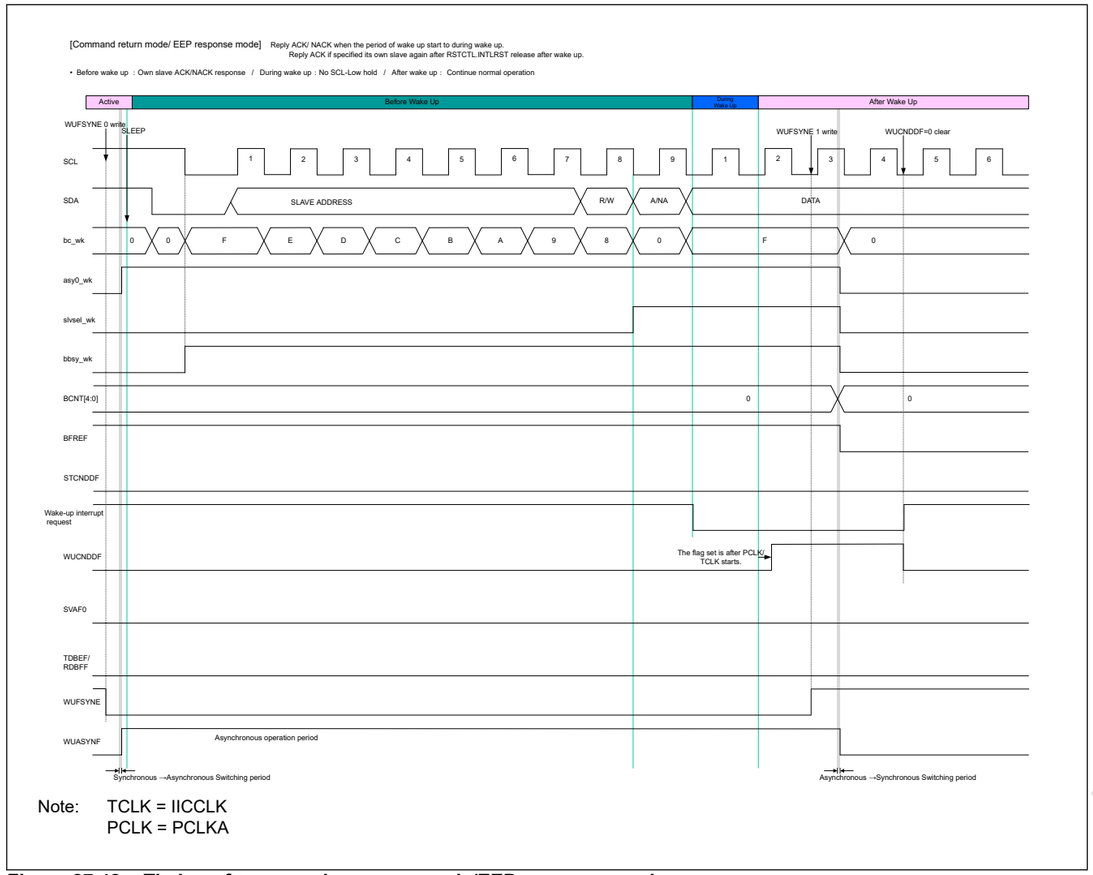


Figure 27.42 Timing of command recovery mode/EEP response mode

(4) Precautions on the use of the Wake-Up function

Precautions on the use of the Wake-up function is shown below.

- Do not change the registers in IIC except the WUCTL.WUFSYNE bit while the WUST.WUASYNF flag = 1 (while PCLKA/IICCLK asynchronous operation).
- Set WUCTL.WUFE = BSTE.WUCNDDE = BIE.WUCNDDIE = 1 and PRSST.CRMS = PRSST.TRMD = 0 (slave reception mode) before switching PCLKA/IICCLK asynchronous mode.
- Can not select the device ID and the 10-bit slave address for wake-up interrupt factor. Set the DVIDE bit in SVCTL and SDADLS bit in SDATBASy to 0.
- Sets all bits in BIE (TENDIE, NACKDIE, SPCNDDIE, STCNDDIE, ALIE, TODIE) and TDBEIE0 and RDBFIE0 bits in NTIE to 0 (Interrupt disabled) before switching the asynchronous operation.
- Do not use the timeout function while the Wake-up function is enabled (WUCTL.WUFE = 1).
- Wake-up interrupt is generated while PCLKA/IICCLK asynchronous operation (when WUST.WUASYNF = 1). In case of detecting slave address matching, The case of detect slave address match in PCLKA/IICCLK synchronous mode (WUST.WUASYNF = 0), does not occur Wake-up interrupt, and BST.WUCNDDF flag will be not set also.
- If WUCTL.WUFSYNE bit to 0 write timing and START condition of detecting a conflict, IIC might start the next reception in PCLKA/IICCLK synchronous operation mode. In this case, WUST.WUASYNF flag becomes 1 (switch to PCLKA/IICCLK asynchronous mode) when data communication is finished and detected STOP condition and starts the Wake-up event detection.

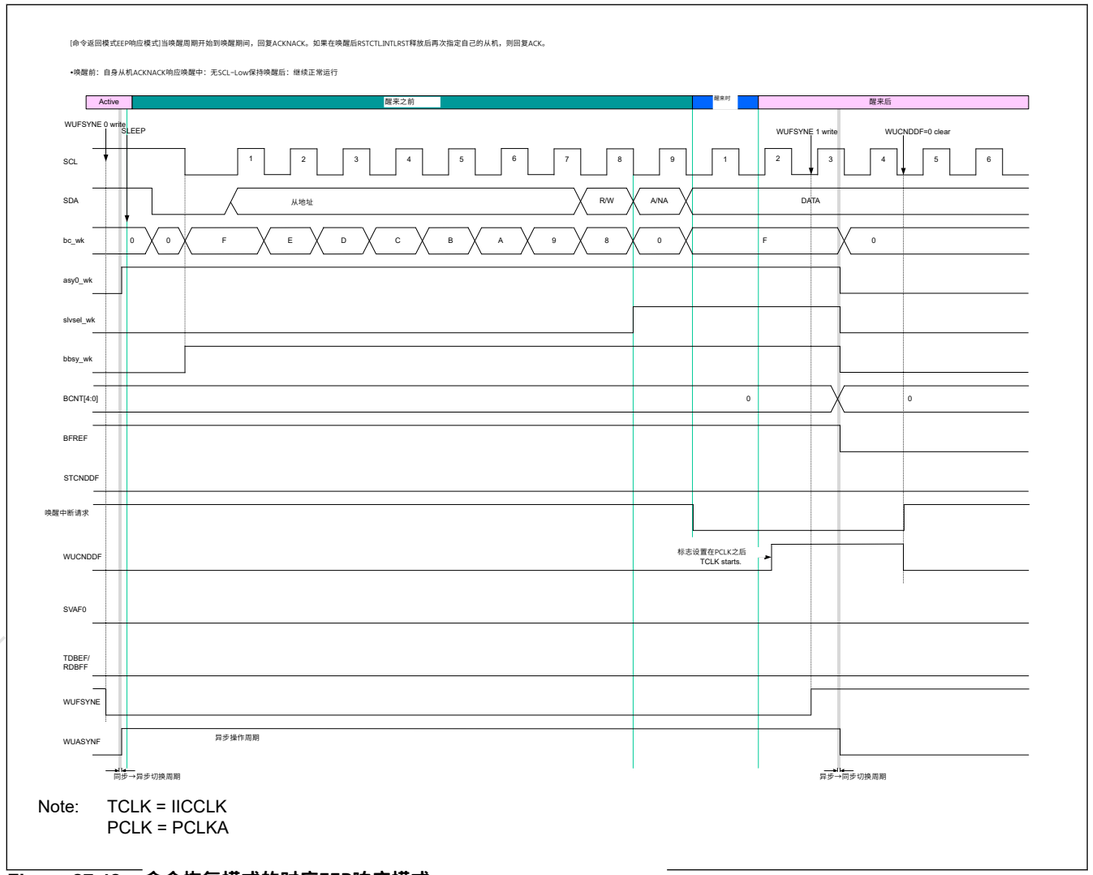


Figure 27.42 命令恢复模式的时序EEP响应模式

(4) 唤醒功能使用注意事项

使用唤醒功能的注意事项如下所示。

●当WUST.WUASYNF标志=1时（当PCLKAIICCLK异步操作时），不要更改IIC中的寄存器，除了WUCTL.WUFSYNE位。

●在切换PCLKAIICCLK异步模式之前设置WUCTL.WUFE=BSTE.WUCNDDE=BIE.WUCNDDIE=1和PRSST.CRMS=PRSST.TRMD=0（从接收模式）。

●唤醒中断因子不能选择设备ID和10位从机地址。将SVCTL中的DVIDE位和SDATBASy中的SDADLS位设置为0。

●在切换异步操作之前，将BIE中的所有位（TENDIE、NACKDIE、SPCNDDIE、STCNDDIE、ALIE、TODIE）和NTIE中的TDBEIE0和RDBFIE0位设置为0（中断禁用）。

●唤醒功能启用时不要使用超时功能（WUCTL.WUFE=1）。

●PCLKAIICCLK异步操作时产生唤醒中断（当WUST.WUASYNF=1时）。在检测从机地址匹配的情况下，在PCLKAIICCLK同步模式（WUST.WUASYNF=0）检测从机地址匹配的情况下，不会发生唤醒中断，也不会设置BST.WUCNDDF标志。

●如果WUCTL.WUFSYNE位为0写入时序和检测到的START条件冲突，IIC可能会启动下一个
在PCLKAIICCLK同步操作模式下接收。在这种情况下，当数据通信完成并检测到STOP条件并启动

唤醒事件检测。

- If you want to switch from PCLKA/IICCLK asynchronous operation to PCLKA/IICCLK synchronous operation without address match detection, it will switch in the STOP condition detection. When the WUCTL.WUFSYNE bit was set to 1 in a bus free state, it is continued PCLKA/IICCLK asynchronous operation (Reception operation: waiting communication frame). WUST.WUASYNF flag becomes to 0 when IIC detect the STOP condition of the next communication frame, and IIC switches to PCLKA/IICCLK synchronous operation.
- After writing 0 to WUFSYNE bit in WUCTL, do not change IIC operation mode setting register (BFCTL, SCSTRCTL, ACKCTL, INCTL, SVCTL, SDATBASy) until switched to the PCLKA/IICCLK asynchronous operation from PCLKA/IICCLK synchronous operation (while WUST.WUASYNF flag = 1). If register value changes by the interrupt processing etc. in this period, IIC might malfunction without succeeding to the setting to the asynchronous operation.
- During PCLKA/IICCLK asynchronous operation (WUST.WUASYNF = 1), do not refer to each flag of SVST, BST, NTST register and BCST.BFREF flag.
- Do not set ACKCTL.ACKT = 1 in order to make an ACK response in the synchronization unit when Wake-up is performed by slave address match in Normal wake-up mode 2.

27.3.1.6 Other

27.3.1.6.1 SCL Synchronization Circuit

In generation of the SCL clock, IIC starts counting out the value for width at high level specified in STDBR.SBRHO[7:0] when it detects a rising edge on the SCLn line and drives the SCLn line low once counting of the width at high level is complete.

When IIC detects the falling edge of the SCLn line, it starts counting out the width at low level period specified in STDBR.SBRLO[7:0], and then stops driving the SCLn line (releases the line) once counting of the width at low level is complete. The SCL clock is thus generated.

If multiple master devices are connected to the I^2C bus, a collision of SCL signals may arise due to contention with another master device. In such cases, the master devices have to synchronize their SCL signals. Since this synchronization of SCL signals must be bit by bit, IIC is equipped with a facility (the SCL synchronization circuit) to obtain bit-by-bit synchronization of the SCL clock signals by monitoring the SCLn line while in master mode.

When IIC has detected a rising edge on the SCLn line and thus started counting out the width at high level specified in STDBR.SBRHO[7:0], and the level on the SCLn line falls because an SCL signal is being generated by another master device, IIC stops counting when it detects the falling edge, drives the level on the SCLn line low, and starts counting out the width at low level specified in STDBR.SBRLO[7:0]. When IIC finishes counting out the width at low level, it stops driving the SCLn line to the low level (releases the line). At this time, if the width at low level of the SCL clock signal from the other master device is longer than the width at low level set in this module, the width at low level of the SCL signal will be extended. Once the width at low level for the other master device has ended, the SCL signal rises because the SCLn line has been released. When IIC finishes outputting the low-level period of the SCL clock, the SCLn line is released and the SCL clock rises. That is, in cases of contention of SCL signals from more than one master, the width at high level of the SCL signal is synchronized with that of the clock having the narrower width, and the width at low level of the SCL signal is synchronized with that of the clock having the broader width. However, such synchronization of the SCL signal is only enabled when the SCSYNE bit in BFCTL is set to 1.

●如果要从PCLKAIICCLK异步操作切换到PCLKAIICCLK同步操作
如果没有地址匹配检测，它将切换到STOP条件检测。当WUCTL.WUFSYNE位在总线空闲状态设置为1时，继续PCLKAIICCLK异步操作（接收操作：等待通信帧）。当IIC检测到下一个通信帧的STOP条件时，WUST.WUASYNF标志变为0，并且IIC切换到PCLKAIICCLK同步操作。

●将WUCTL中的WUFSYNE位写入0后，不要更改IIC操作模式设置寄存器（BFCTL、SCSTRCTL、ACKCTL、INCTL、SVCTL、SDATBASy），直到从IICCLK异步操作切换到PCLKA
PCLKAIICCLK同步操作（当WUST.WUASYNF标志=1时）。如果在此期间寄存器值因中断处理等而发生变化，则IIC可能会发生故障，而无法成功设置异步操作。

●在PCLKAIICCLK异步操作期间（WUST.WUASYNF=1），不要参考SVST、BST、NTST寄存器的每个标志和BCST.BFREF标志。

●在Normal唤醒模式2中通过从机地址匹配执行唤醒时，不要设置ACKCTL.ACKT=1以便在同步单元中做出ACK响应。

27.3.1.6 Other

27.3.1.6.1 SCL同步电路

在生成SCL时钟时，IIC在检测到SCLn线上的上升沿时开始计算STDBR.SBRHO[7:0]中指定的高电平宽度值，并在计数到高水平完成。

当IIC检测到SCLn线的下降沿时，它开始计数指定的低电平周期的宽度
STDBR.SBRLO[7:0]，然后在低电平宽度计数完成后停止驱动SCLn线（释放线）。这样就生成了SCL时钟。

如果多个主设备连接到I2C总线，由于与另一个主设备的争用，可能会出现SCL信号的冲突。在这种情况下，主设备必须同步它们的SCL信号。由于SCL信号的这种同步必须逐位进行，因此IIC配备了一个设备（SCL同步电路），通过在主机模式下监视SCLn线来获得SCL时钟信号的逐位同步。

当IIC检测到SCLn线上的上升沿并因此开始计算STDBR.SBRHO[7:0]中指定的高电平宽度时，由于另一个主控器正在生成SCL信号，因此SCLn线上的电平下降IIC在检测到下降沿时停止计数，将SCLn线上的电平驱动为低电平，并在STDBR.SBRLO[7:0]中指定的低电平开始计数宽度。当IIC在低电平完成宽度计数时，停止将SCLn线驱动到低电平（释放线）。此时，如果来自其他主设备的SCL时钟信号的低电平宽度大于本模块设置的低电平宽度，则SCL信号的低电平宽度将被扩展。一旦另一个主设备的低电平宽度结束，SCL信号就会上升，因为SCLn线已被释放。当IIC输出完SCL时钟的低电平周期后，SCLn线被释放，SCL时钟上升。即，在来自多个主机的SCL信号竞争的情况下，SCL信号的高电平宽度与宽度较窄的时钟的宽度同步，而SCL信号的低电平宽度与时钟具有更宽的宽度。然而，只有当BFCTL中的SCSYNE位设置为1时，才启用SCL信号的这种同步。

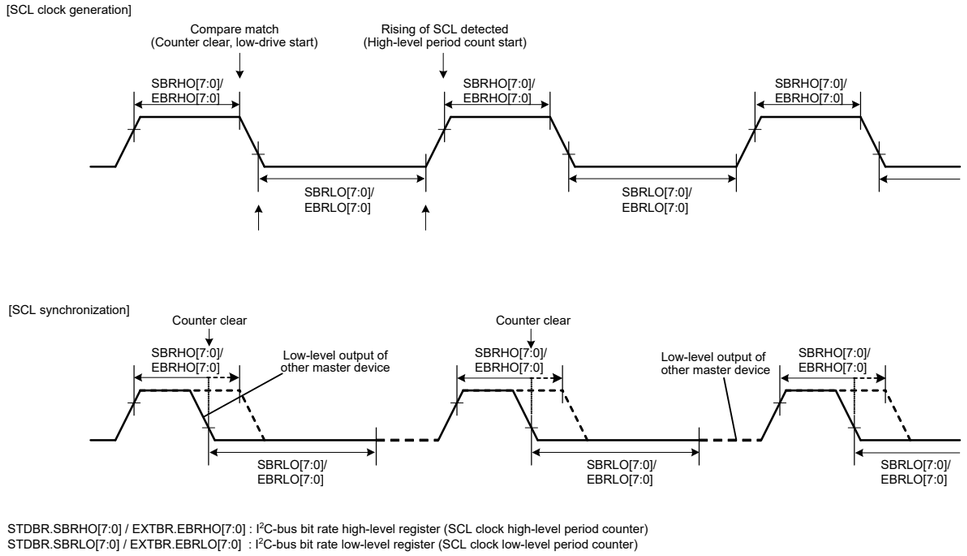


Figure 27.43 Generation and synchronization of the SCL signal

27.3.1.6.2 Facility for Delaying SDA Output

IIC module incorporates a facility for delaying output on the SDA line. The delay can be applied to all output (issuing of the START, Repeated START, and STOP conditions, data, and the ACK and NACK signals) on the SDA line.

With the SDA output delay facility, SDA output is delayed from detection of a falling edge of the SCL signal to ensure that the SDA signal is output within the interval over which the SCL clock is at the low level. Doing this leads to usage with the aim of preventing erroneous operation of communications devices, with the aim of satisfying the 300 ns (minimum) data-hold time requirement of the SMBus specification.

The output delay facility is enabled by setting the SDOD[2:0] bits in OUTCTL to any value other than 000b, and disabled by setting the same bits to 000b.

While the SDA output delay facility is enabled (while the SDOD[2:0] bits in OUTCTL are set to any value other than 000b), the SDODCS bit in OUTCTL selects the clock source for counting by the SDA output delay counter as the internal base clock (IICφ) for IIC module or as a clock signal derived by dividing the frequency of the internal base clock by two (IICφ/2). The counter counts the number of cycles set in the SDOD[2:0] bits in OUTCTL. After counting of the set number of cycles of delay is completed, IIC module places the required output (START, Repeated START, or STOP condition, data, or an ACK or NACK signal) on the SDA line.

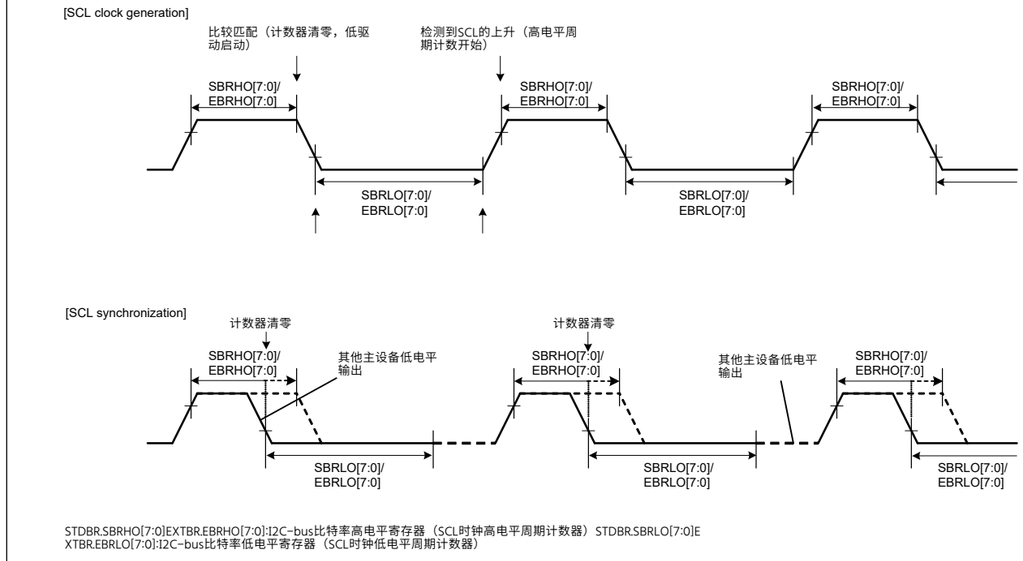


Figure 27.43 SCL信号的生成和同步

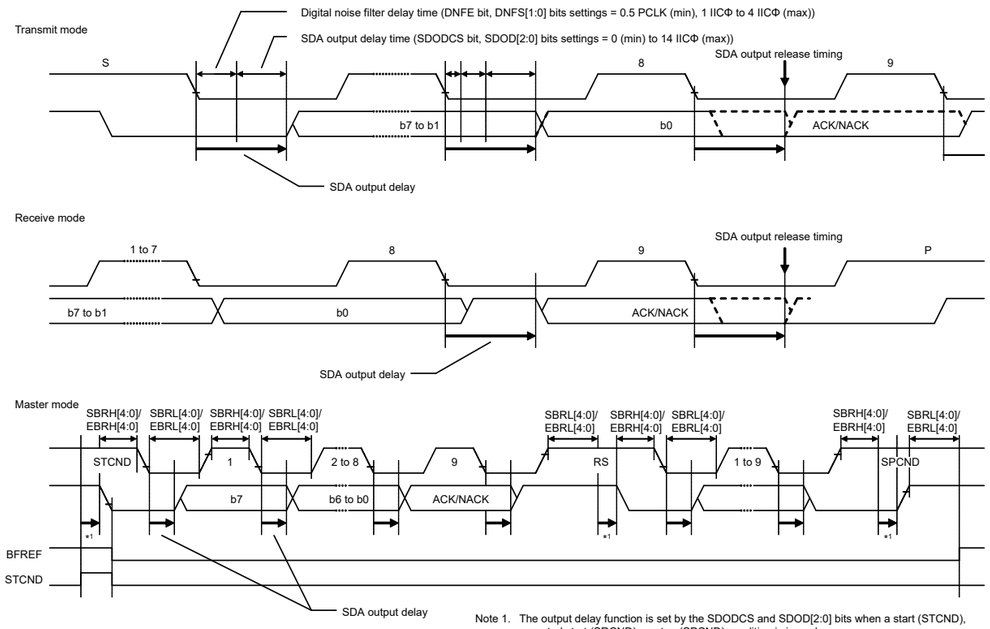
27.3.1.6.2 延迟SDA输出的设备

IIC模块包含一个用于延迟SDA线路上的输出的功能。延迟可以应用于所有输出（发出SDA线上的START、重复START和STOP条件、数据以及ACK和NACK信号。

使用SDA输出延迟功能，SDA输出从检测到SCL信号的下降沿开始延迟，以确保SDA信号在SCL时钟处于低电平的时间间隔内输出。这样做会导致使用目的是防止通信设备的错误操作，目的是满足SMBus规范的300ns（最小）数据保持时间要求。

输出延迟功能通过将OUTCTL中的SDOD[2:0]位设置为000b以外的任何值来启用，并通过将相同位设置为000b来禁用。

当SDA输出延迟功能被使能时（同时OUTCTL中的SDOD[2:0]位设置为000b以外的任何值），OUTCTL中的SDODCS位选择SDA输出延迟计数器计数的时钟源作为内部IIC模块的基本时钟(IICφ)或作为通过将内部基本时钟的频率除以2(IICφ2)得到的时钟信号。计数器计算在OUTCTL的SDOD[2:0]位中设置的周期数。在完成对设定的延迟周期数的计数后，IIC模块将所需的输出（START、RepeatedSTART或STOP条件、数据或ACK或NACK信号）放在SDA线上。



Note 1. The output delay function is set by the SDODCS and SDOD[2:0] bits when a start (STCND), repeated start (SRCND), or stop (SPCND) condition is issued.

Note: PCLK = PCLKA

Figure 27.44 SDA output delay facility

27.3.1.6.3 Digital Noise-Filter Circuits

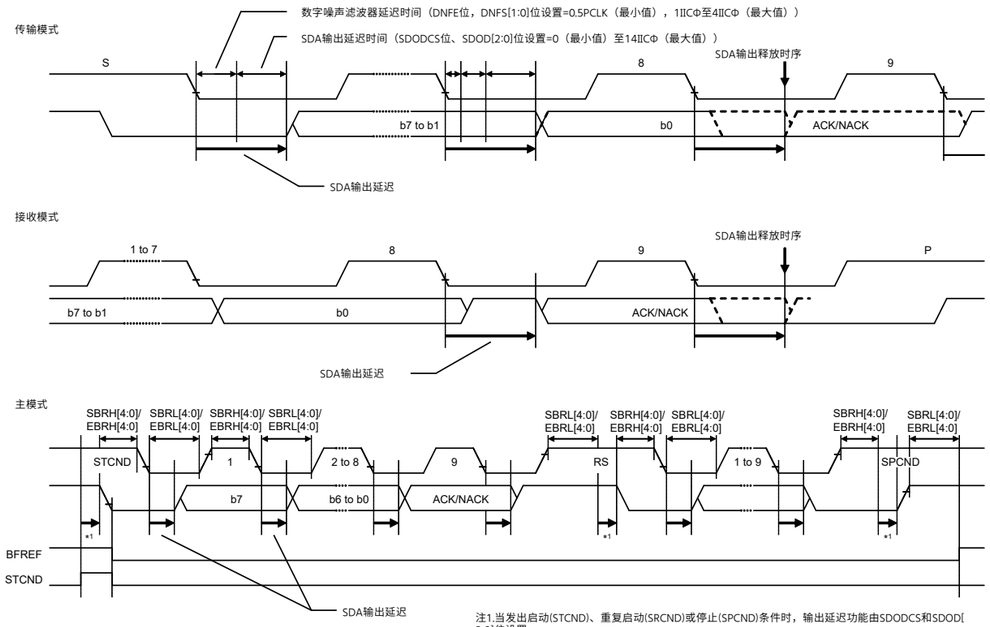
The states of the SCLn and SDAn pins are conveyed to the internal circuitry through digital noise-filter circuits. Figure 27.45 is a block diagram of the digital noise-filter circuit.

The on-chip digital noise-filter circuit of IIC consists of 16 flip-flop circuit stages connected in series and a match detection circuit. When HS mode is selected, only the first four flip-flop circuits stages are enabled.

The number of effective stages in the digital noise filter is selected by the INCTL.DNFS[3:0] bits. The selected number of effective stages determines the noise-filtering capability as a period from one to sixteen IICφ cycles.

The input signal to the SCLn pin (or SDAn pin) is sampled on rising edges of the IICφ signal. When the input signal level matches the output level of the number of effective flip-flop circuit stages as selected by the INCTL.DNFS[3:0] bits, the signal level is conveyed to the subsequent stage. If the signal levels do not match, the previous value is retained.

If the ratio between the frequency of the internal operating clock (IICCLK) and the transfer rate is small (For example, data transfer at 400 kbps with IICCLK = 4 MHz), the characteristics of the digital noise filter may lead to the elimination of needed signals as noise.



注1.当发出启动(STCND)、重复启动(SRCND)或停止(SPCND)条件时，输出延迟功能由SDODCS和SDOD[2:0]位设置。

Note: PCLK = PCLKA

Figure 27.44 SDA输出延迟功能

27.3.1.6.3 数字噪声滤波器电路

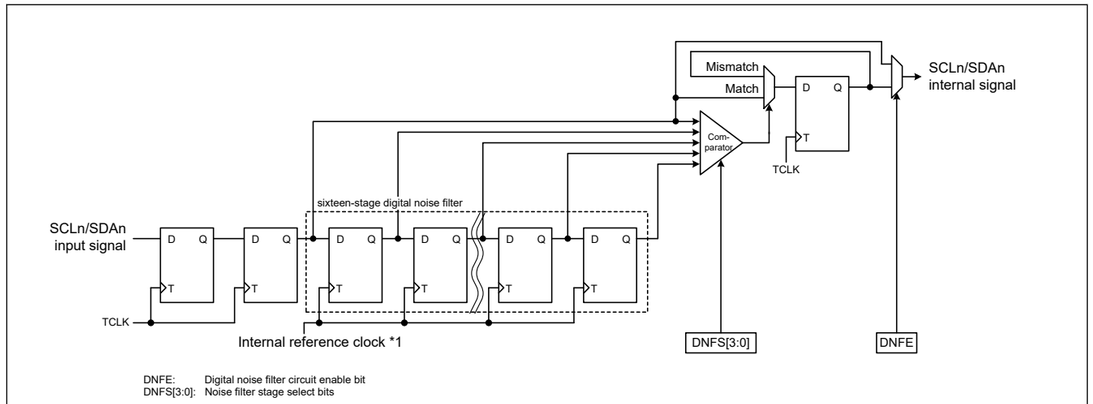
SCLn和SDAn引脚的状态通过数字噪声滤波器电路传送到内部电路。图27.45是数字噪声滤波器电路的框图。

IIC的片上数字噪声滤波电路由16个串联的触发器电路级和一个匹配检测电路组成。选择HS模式时，仅启用前四个触发器电路级。

数字噪声滤波器的有效级数由INCTL.DNFS[3:0]位选择。选定的有效级数将噪声过滤能力确定为从1到16个IICφ周期的周期。

SCLn引脚（或SDAn引脚）的输入信号在IICφ信号的上升沿采样。当输入信号电平与由INCTL.DNFS[3:0]位选择的有效触发器电路级数的输出电平匹配时，信号电平被传送到下一级。如果信号电平不匹配，则保留先前的值。

如果内部工作时钟(IICCLK)的频率与传输速率之间的比率很小（例如，数据传输速率为400kbps，IICCLK=4MHz），则数字噪声滤波器的特性可能会导致消除所需的信号作为噪声。



Note: TCLK = IICCLK
Note 1. Internal reference clock = IICφ

Figure 27.45 Block diagram of digital noise filter circuit

27.3.2 Operation

27.3.2.1 Initial Setting Flow

27.3.2.1.1 I2C Initial Setting Flow (Single Buffer Transfer)

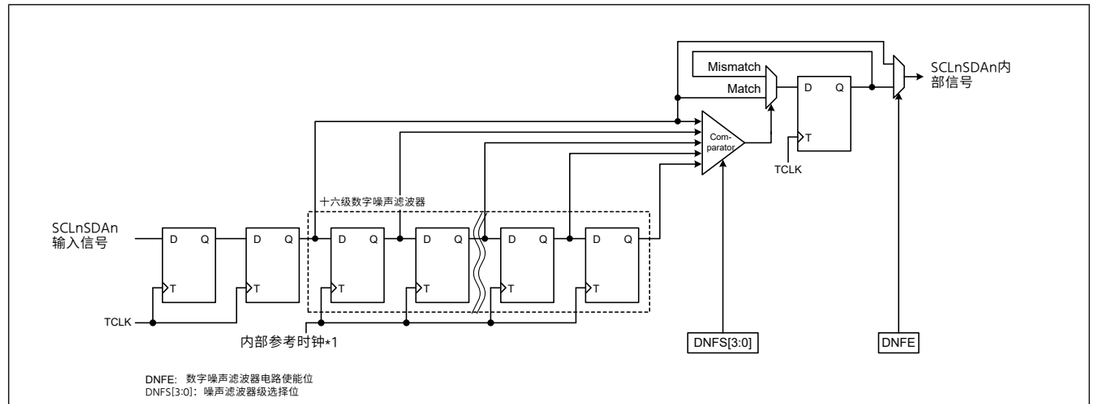
Before starting data transmission and reception, initialize IIC according to the procedure in Figure 27.46.

First, set the BCTL.BUSE bit to 0 (SCLn, SDAn pins not driven).

Next, set the RSTCTL.RI2CRST bit to 1 (IIC reset). This initializes the all registers and internal state. Then, waits for RI2CRST to become 0.

This initializes the various flags and some registers. See Reset Descriptions.

After that, set registers SDATBAS.SDADLS, SDATBAS.SDATAD[9:0], STDBR, INCTL, OUTCTL, TMOCTL, TMOCNT, SCSTRCTL, ACKCTL, and BFCTL, then set the other registers as necessary (for initial settings of IIC, see Figure 27.46).



Note: TCLK = IICCLK
注1.内部参考时钟=IICφ

Figure 27.45 数字噪声滤波电路框图

27.3.2 Operation

27.3.2.1 初始设定流程

27.3.2.1.1 I2C初始设置流程（单缓冲区传输）

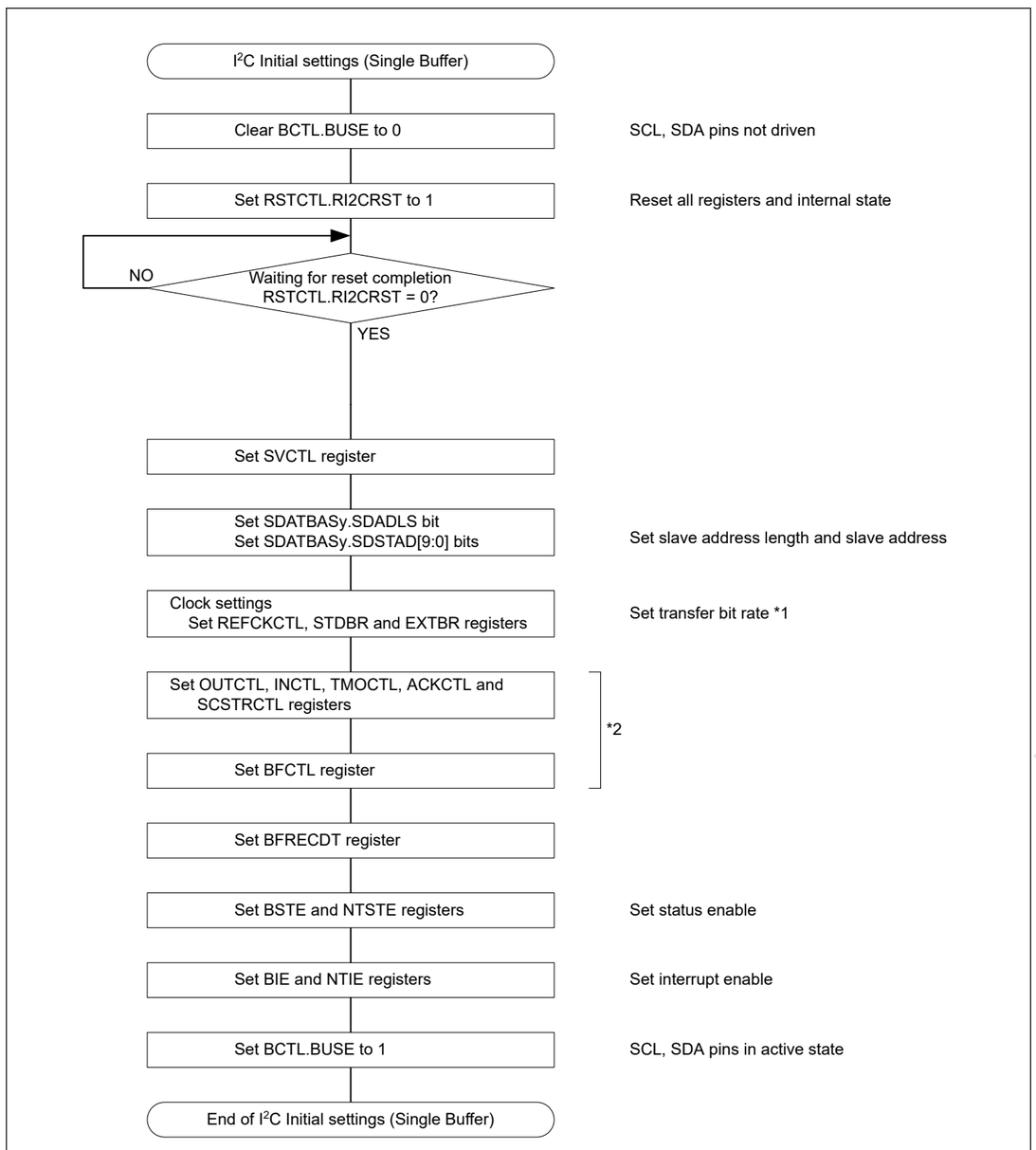
在开始数据发送和接收之前，按照图27.46中的过程初始化IIC。

首先，将BCTL.BUSE位设置为0（SCLn、SDAn引脚未驱动）。

接下来，将RSTCTL.RI2CRST位设置为1（IIC复位）。这将初始化所有寄存器和内部状态。然后，等待RI2CRST变为0。

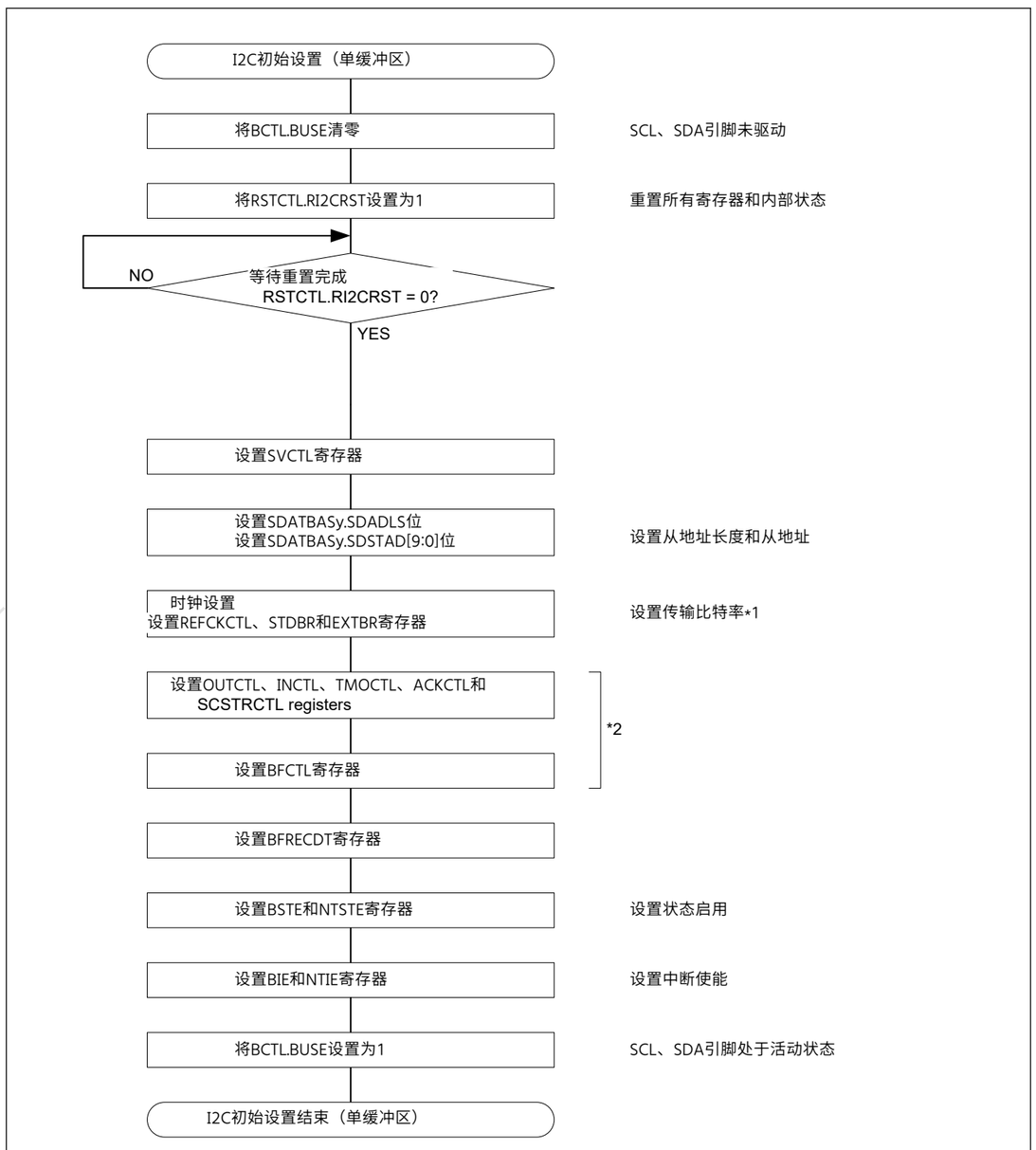
这会初始化各种标志和一些寄存器。请参阅重置说明。

之后，设置寄存器SDATBAS.SDADLS、SDATBAS.SDATAD[9:0]、STDBR、INCTL、OUTCTL、TMOCTL、TMOCNT、SCSTRCTL、ACKCTL和BFCTL，然后根据需要设置其他寄存器（有关IIC的初始设置，请参见Figure 27.46）.



Note: n = 0 to 2
Note 1. When the IIC is used only in slave mode, set the STDBR register to a value longer than the data setup time.
Note 2. Set these registers as necessary.

Figure 27.46 Block diagram of digital noise filter circuit



Note: n = 0 to 2
注1.当IIC仅用于从模式时，将STDBR寄存器设置为比数据建立时间长的值。
注2.根据需要设置这些寄存器。

Figure 27.46 数字噪声滤波电路框图

27.3.2.2 Master Mode Communication Flow

27.3.2.2.1 I²C Master Transmission Flow (Single Buffer Transfer)

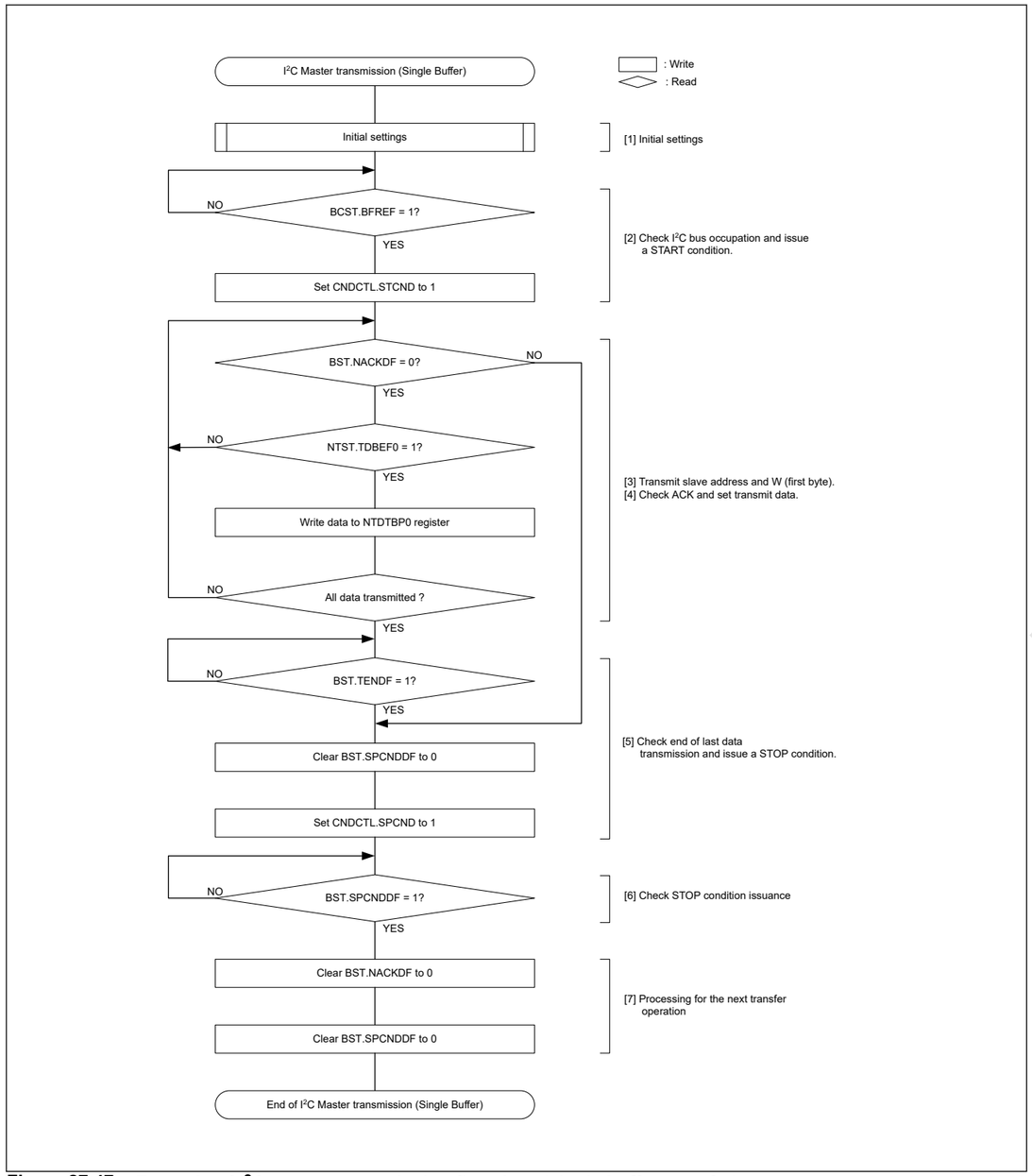


Figure 27.47 Example of I²C master transmission flowchart (single buffer transfer)

27.3.2.2 主模式通信流程

27.3.2.2.1 I2C主机传输流程（单缓冲区传输）

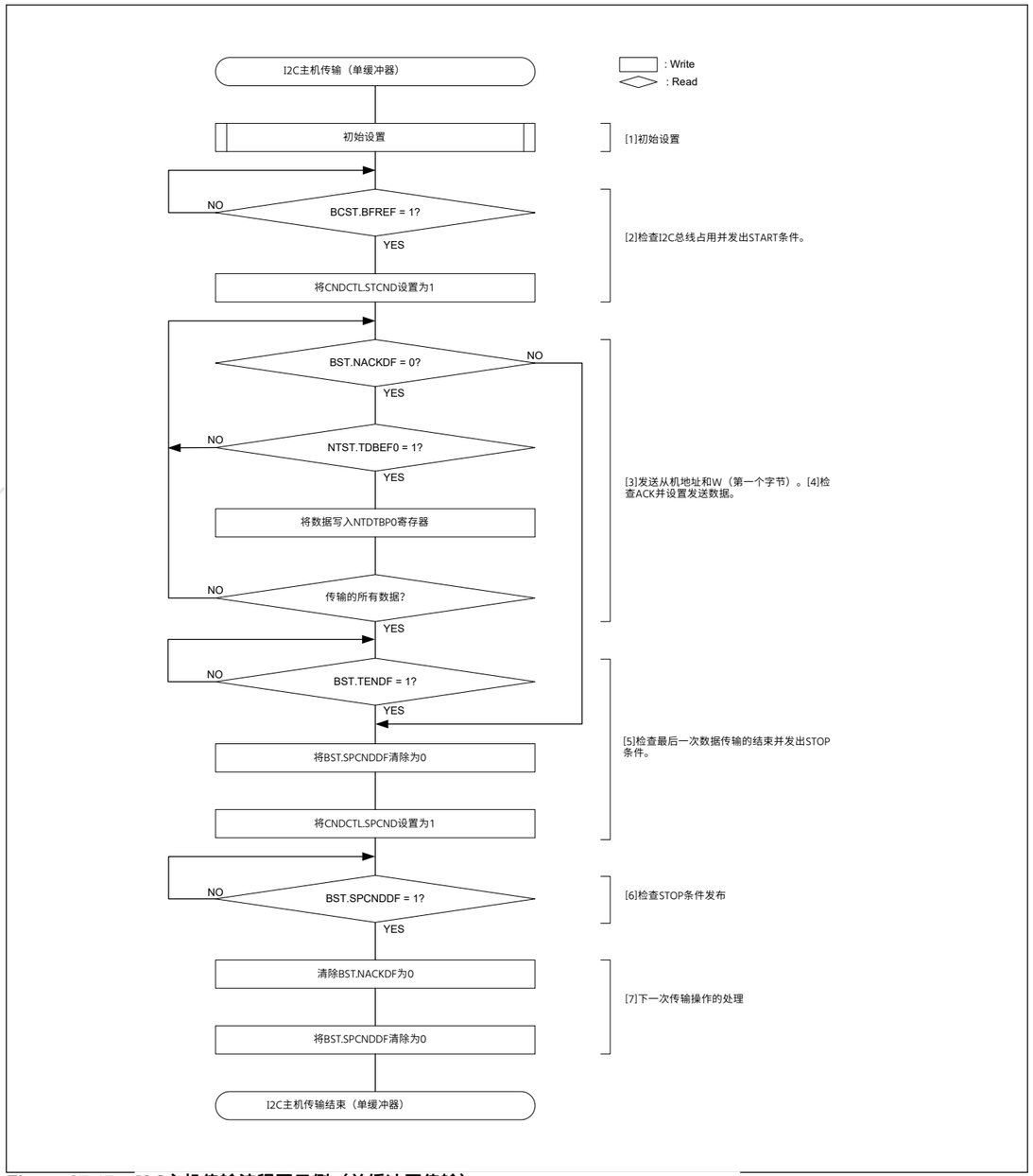


Figure 27.47 I2C主机传输流程图示例（单缓冲区传输）

27.3.2.2.2 I²C Master Reception Flow (Single Buffer Transfer)

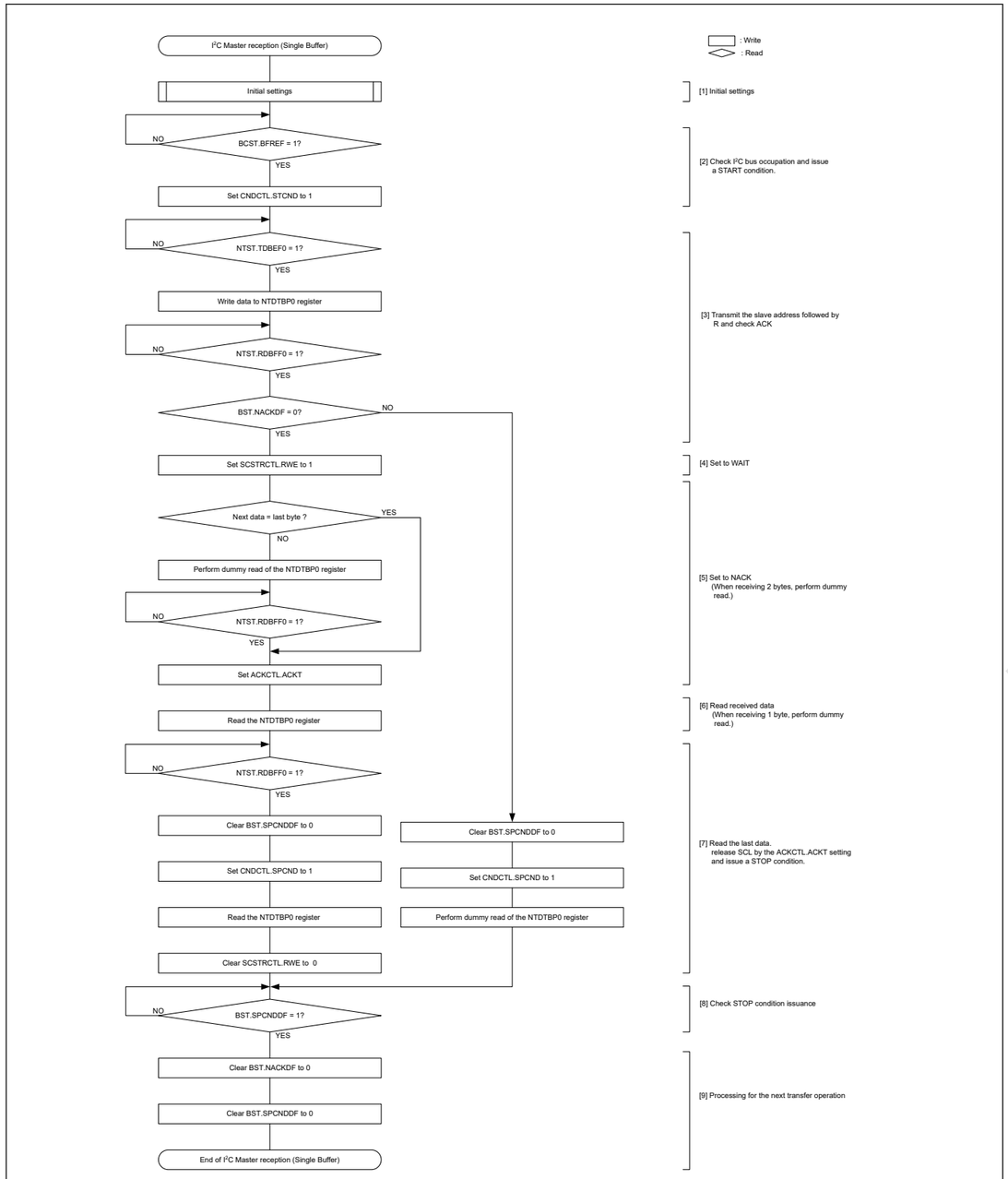


Figure 27.48 Example of I²C master reception flowchart (7-bit address format, 1 or 2 bytes)

27.3.2.2.2 I2C主机接收流程（单缓冲区传输）

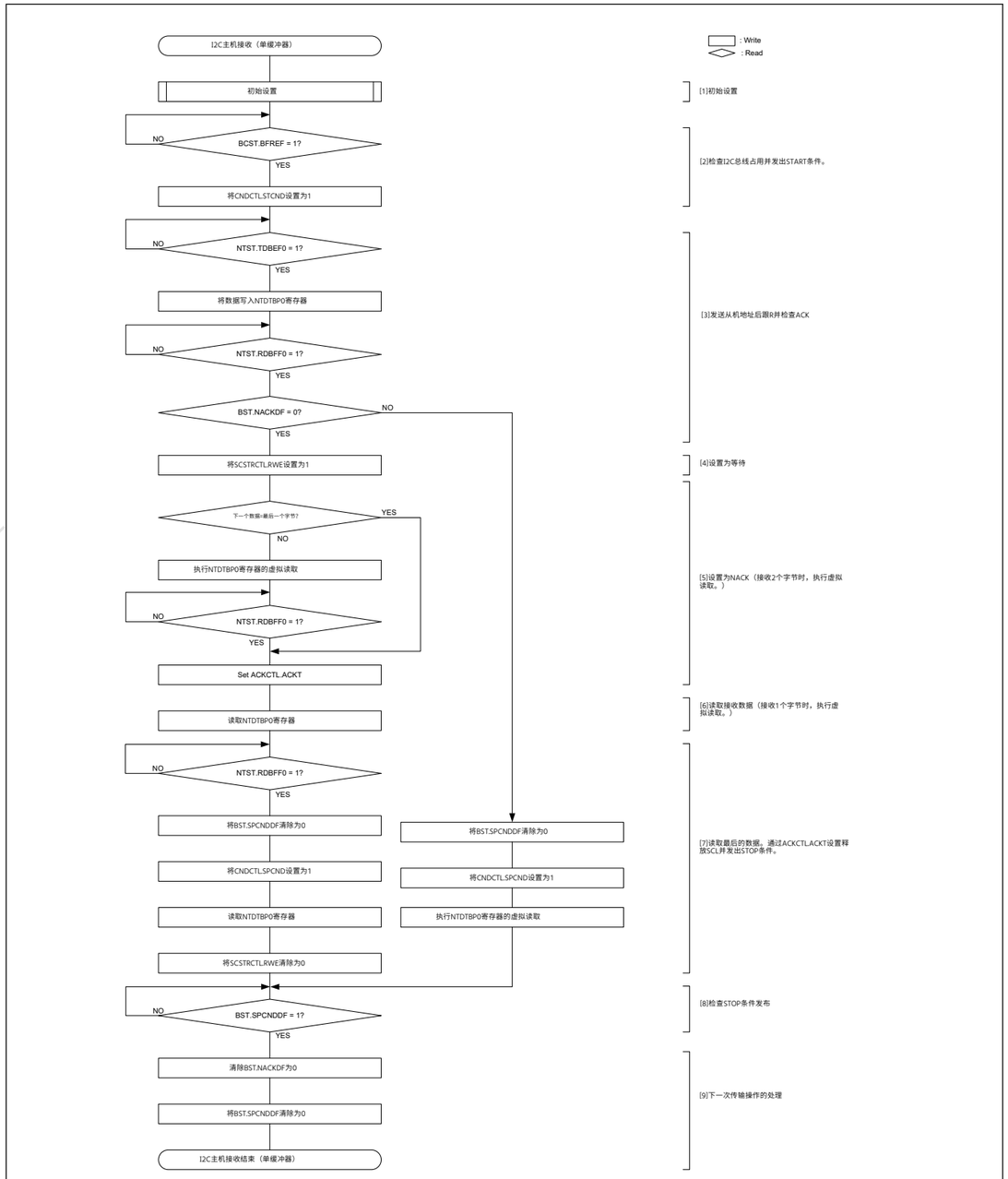


Figure 27.48 I2C主机接收流程图示例（7位地址格式，1或2个字节）

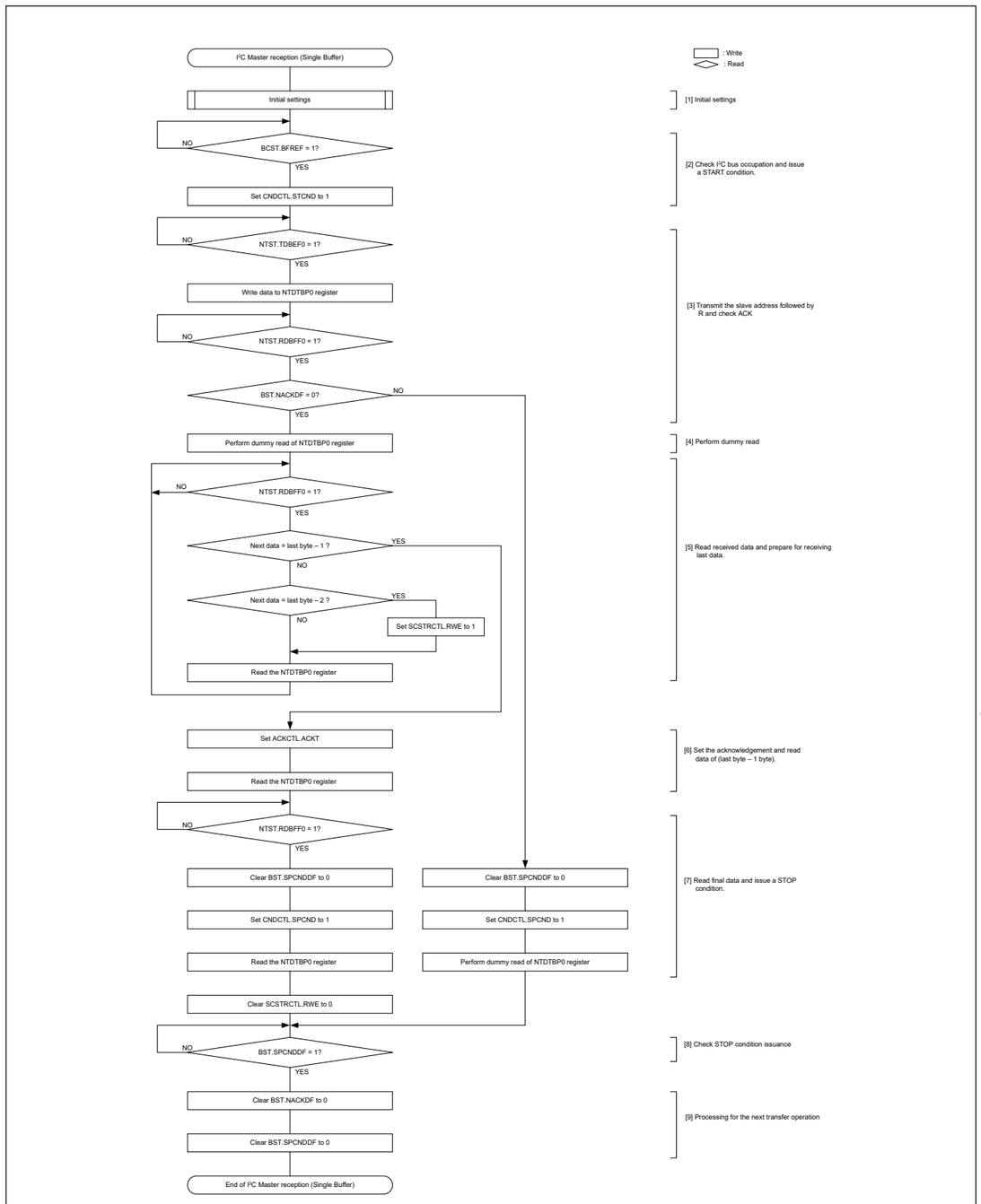


Figure 27.49 Example of I²C master reception flowchart (7-bit address format, 3 bytes or more)

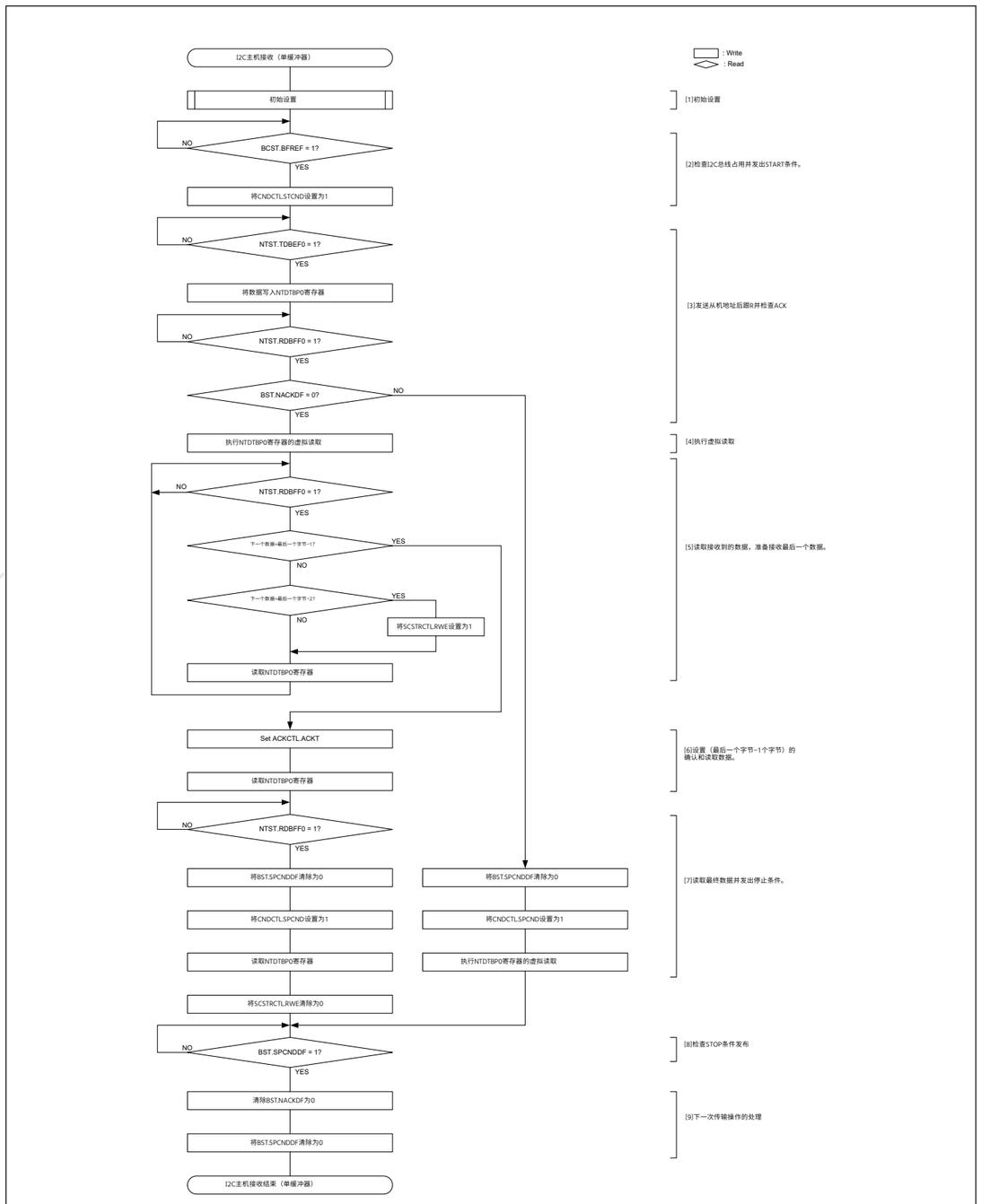


Figure 27.49 I2C主机接收流程图示例（7位地址格式，3字节或更多）

27.3.2.3 Slave Mode Communication Flow

27.3.2.3.1 I²C Slave Transmission Flow (Single Buffer Transfer)

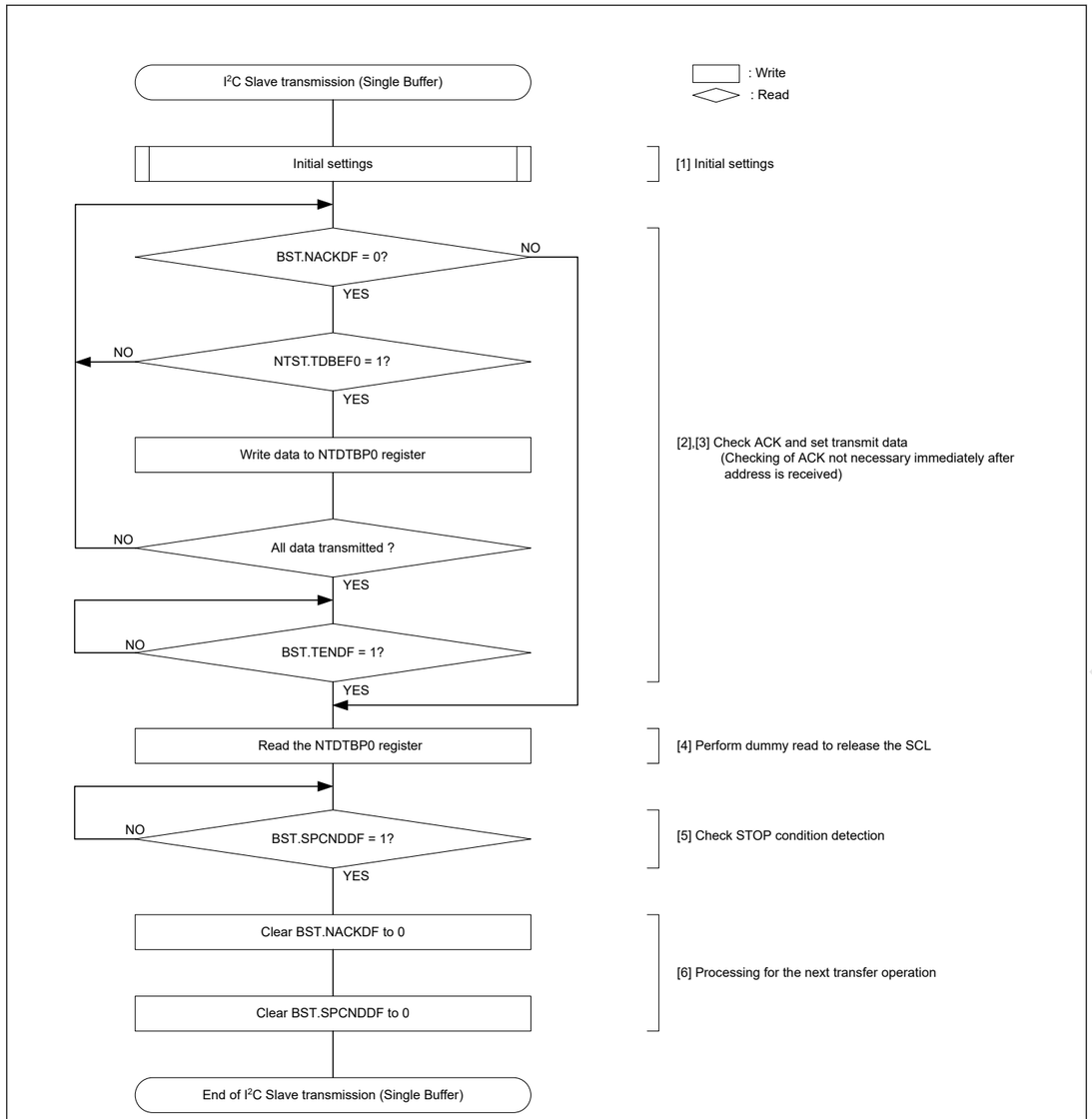


Figure 27.50 Example of I²C slave transmission flowchart (single buffer transfer)

27.3.2.3 从模式通信流程

27.3.2.3.1 I2C从机传输流程（单缓冲区传输）

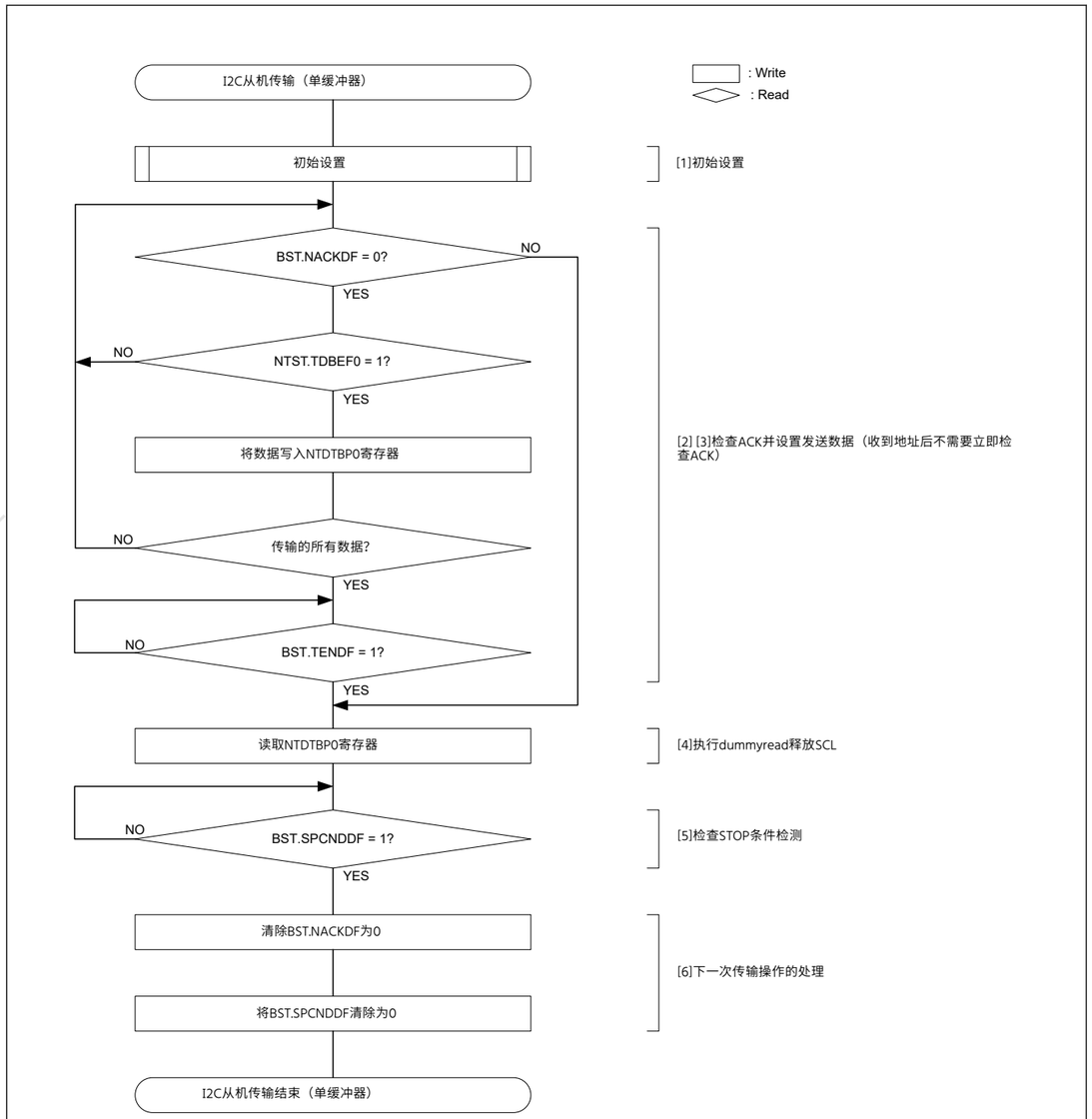


Figure 27.50 I2C从机传输流程图示例（单缓冲区传输）

27.3.2.3.2 I²C Slave Reception Flow (Single Buffer Transfer)

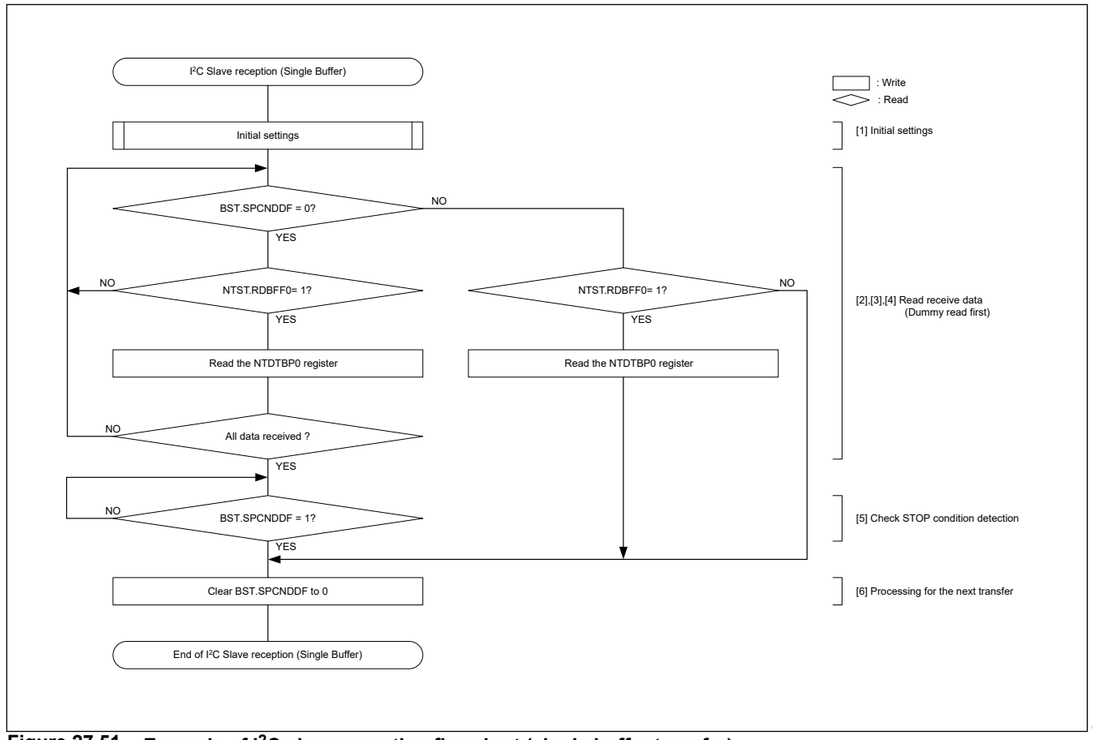


Figure 27.51 Example of I²C slave reception flowchart (single buffer transfer)

27.4 Interrupt Sources

IIC can generate the following interrupt requests:

27.4.1 Overview

The IIC has the interrupt factors shown in Table 27.10.

The interrupt indicated by Possible in the DMAC/DTC Activation column are capable of activating data transfer by the DTC or DMAC.

Table 27.10 Interrupt Generation

Symbol	Interrupt source		Interrupt flag
IICn_RX	Normal receive data buffer full		NTST.RDBEF0
IICn_TX	Normal transmit data buffer empty		NTST.TDBEF0
IICn_TEND	Transmit end		BST.TENDF
IICn_EEI	Transfer error or event occurrence	Start condition detection interrupt	BST.STCNDDF
		STOP condition detection interrupt	BST.SPCNDDF
		NACK detection interrupt	BST.NACKDF
		Arbitration lost interrupt	BST.ALF
		Timeout detection interrupt	BST.TODF
IIC0_WU	Wake-up condition detection		BST.WUCNDDF

Note: n = 0, 1

27.3.2.3.2 I2C从机接收流程（单缓冲区传输）

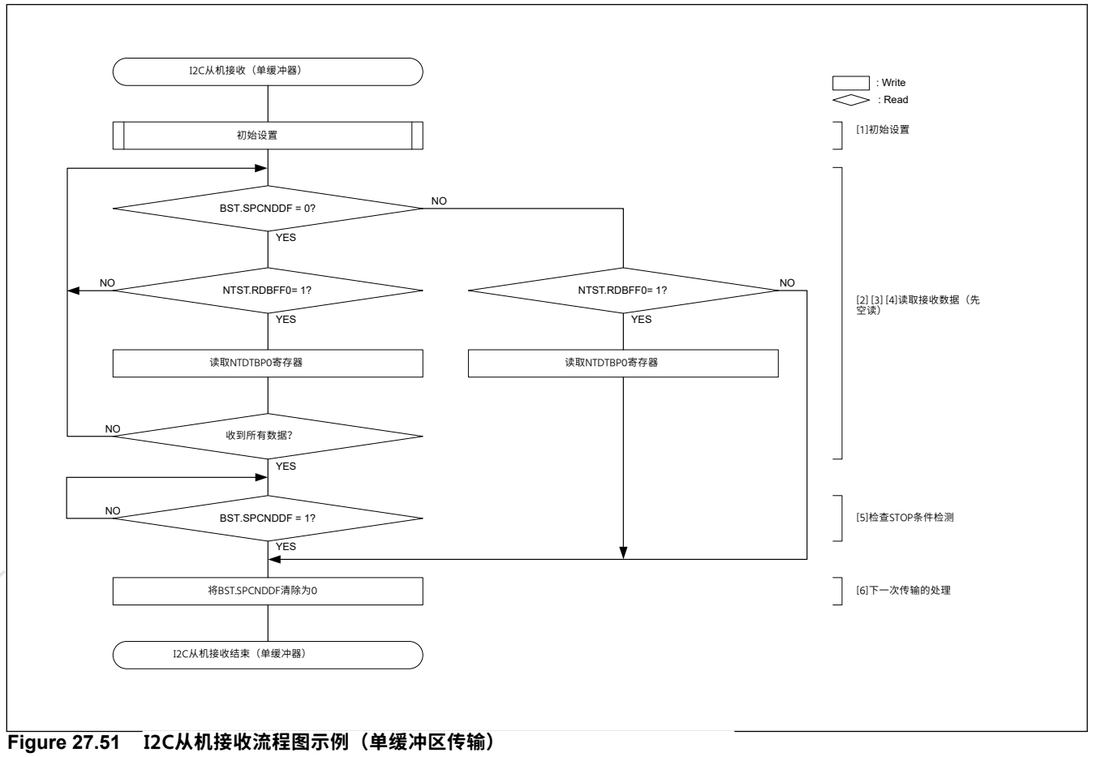


Figure 27.51 I2C从机接收流程图示例（单缓冲区传输）

27.4 中断源

IIC可以产生以下中断请求：

27.4.1 Overview

IIC具有表27.10所示的中断因素。

DMACDTCActivation列中的可能指示的中断能够通过
DTC or DMAC.

Table 27.10 中断产生

Symbol	中断源		中断标志
IICn_RX	正常接收数据缓冲区已满		NTST.RDBEF0
IICn_TX	正常发送数据缓冲区为空		NTST.TDBEF0
IICn_TEND	发射端		BST.TENDF
IICn_EEI	传输错误或事件发生	开始条件检测中断	BST.STCNDDF
		STOP条件检测中断	BST.SPCNDDF
		NACK检测中断	BST.NACKDF
		仲裁丢失中断	BST.ALF
		超时检测中断	BST.TODF
IIC0_WU	唤醒状态检测		BST.WUCNDDF

Note: n = 0, 1

27.4.2 Buffer Operation for Buffer Full/Empty Interrupts

If the conditions for generating the each buffer full/empty interrupts are satisfied while the corresponding IR flag is 1, the interrupt request is not output for the ICU but retained internally (the capacity for internal retention is one request per source).

An interrupt request that was being retained within the ICU is output when the value of the ICU.IRn.IR flag becomes 0. Internally retained interrupt requests are automatically cleared under normal conditions of usage. Internally retained interrupt requests can also be cleared by writing 0 to the interrupt enable bit within the given peripheral module.

27.5 Event Link Output

IIC handles event output for the event link controller (ELC) corresponding to the following sources.

(1) Communication event

When a Communication event (arbitration-lost detection, detection of NACK, detection of timeout, detection of a START condition, or detection of a STOP condition) occurs, the corresponding event signal can be output for another module via the ELC.

(2) Receive data full

When a receive data register becomes full, the corresponding event signal can be output for another module via the ELC.

(3) Transmit data empty

When a transmit data register becomes empty, the corresponding event signal can be output for another module via the ELC.

(4) Transmit end

On completion of transfer, the corresponding event signal can be output for another module via the ELC.

27.5.1 Interrupt Handling and Event Linking

IIC module produces four kinds of interrupt: communication event (arbitration-lost detection, detection of NACK, detection of timeout, detection of a START condition, or detection of a STOP condition), receive data full, transmit data empty, and transmit end interrupts. Each of these has an enable bit to control enabling and disabling of the interrupt signal. An interrupt request signal is output for the CPU when an interrupt source condition is satisfied while the setting of the corresponding enable bit is enabled.

The corresponding event link output signals are sent to other modules as event signals via the ELC when the interrupt source conditions are satisfied, regardless of the settings of the interrupt enable bits. For details on interrupt sources, see section 27.4.1. Overview.

27.6 Reset Descriptions

Table 27.11 Register states when issuing each condition (1) (1 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register	
			RI2CRST	INTLRST
BCTL	BUSE	In reset	In reset	Saved
RSTCTL	INTLRST	In reset	In reset	Saved
	RI2CRST	In reset	Saved	Saved
PRSST	PRSSTWP	In reset	In reset	In reset
	TRMD	In reset	In reset	In reset
	CRMS	In reset	In reset	In reset

27.4.2 缓冲区满空中断的缓冲区操作

如果在相应的IR标志为1时满足产生每个缓冲区满空中断的条件，则该中断请求不输出给ICU，而是在内部保留（内部保留的容量为每个源一个请求）。

当ICU.IRn.IR标志的值变为0时，输出一直保留在ICU内的中断请求。
在正常使用条件下，内部保留的中断请求会自动清除。内部保留的中断请求也可以通过将0写入给定外设模块中的中断使能位来清除。

27.5 事件链接输出

IIC处理与以下源相对应的事件链接控制器(ELC)的事件输出。

(1) 交流活动

当发生通信事件（仲裁丢失检测、NACK检测、超时检测、START条件检测或STOP条件检测）时，可以通过ELC为另一个模块输出相应的事件信号。

(2) 接收数据已满

当接收数据寄存器变满时，可以通过ELC为另一个模块输出相应的事件信号。

(3) 传输数据为空

当发送数据寄存器为空时，可以通过ELC为另一个模块输出相应的事件信号。

(4) 发射端

传输完成后，可以通过ELC为另一个模块输出相应的事件信号。

27.5.1 中断处理和事件链接

IIC模块产生四种中断：通信事件（仲裁丢失检测、NACK检测、超时检测、START条件检测或STOP条件检测）、接收数据满、发送数据空和发送结束中断.其中每一个都有一个启用位来控制中断信号的启用和禁用。当相应的使能位设置为使能时，如果满足中断源条件，则向CPU输出中断请求信号。

当满足中断源条件时，无论中断允许位的设置如何，相应的事件链接输出信号都会通过ELC作为事件信号发送到其他模块。有关中断源的详细信息，请参阅第27.4.1节。概述。

27.6 重置说明

Table 27.11 发出每个条件时的寄存器状态(1)(1of2)

注册符号	寄存器位名称	系统重置	RSTCTL Register	
			RI2CRST	INTLRST
BCTL	BUSE	复位中	复位中	Saved
RSTCTL	INTLRST	复位中	复位中	Saved
	RI2CRST	复位中	Saved	Saved
PRSST	PRSSTWP	复位中	复位中	复位中
	TRMD	复位中	复位中	复位中
	CRMS	复位中	复位中	复位中

Table 27.11 Register states when issuing each condition (1) (2 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register	
			RI2CRST	INTLRST
BFCTL	HSME	In reset	In reset	Saved
	FMPE	In reset	In reset	Saved
	SMBS	In reset	In reset	Saved
	SCSYNE	In reset	In reset	Saved
	SALE	In reset	In reset	Saved
	NALE	In reset	In reset	Saved
	MALE	In reset	In reset	Saved

Table 27.12 Register states when issuing each condition (2) (1 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register	
			RI2CRST	INTLRST
SVCTL	SVAE2	In reset	In reset	Saved
	SVAE1	In reset	In reset	Saved
	SVAE0	In reset	In reset	Saved
	HOAE	In reset	In reset	Saved
	DVIDE	In reset	In reset	Saved
	HSMCE	In reset	In reset	Saved
	GCAE	In reset	In reset	Saved
REFCKCTL	IREFCKS[2:0]	In reset	In reset	Saved
STDBR	DSBRPO	In reset	In reset	Saved
	SBRHP[5:0]	In reset	In reset	Saved
	SBRLO[7:0]	In reset	In reset	Saved
EXTBR	EBRHO[7:0]	In reset	In reset	Saved
	EBRLO[7:0]	In reset	In reset	Saved
BFRECDT	FRECYC[8:0]	In reset	In reset	Saved
OUTCTL	SDODCS	In reset	In reset	Saved
	SDOD[2:0]	In reset	In reset	Saved
	EXCYC	In reset	In reset	Saved
	SOCWP	In reset	In reset	In reset
	SCOC	In reset	In reset	Saved
	SDOC	In reset	In reset	Saved
INCTL	SDID[1:0]	In reset	In reset	Saved
	DNFE	In reset	In reset	Saved
	DNFS[3:0]	In reset	In reset	Saved
TMOCTL	TOMDS[1:0]	In reset	In reset	Saved
	TOHCTL	In reset	In reset	Saved
	TOLCTL	In reset	In reset	Saved
	TODTS[1:0]	In reset	In reset	Saved

Table 27.11 发出每个条件时的寄存器状态(1)(2of2)

注册符号	寄存器位名称	系统重置	RSTCTL Register	
			RI2CRST	INTLRST
BFCTL	HSME	复位中	复位中	Saved
	FMPE	复位中	复位中	Saved
	SMBS	复位中	复位中	Saved
	SCSYNE	复位中	复位中	Saved
	SALE	复位中	复位中	Saved
	NALE	复位中	复位中	Saved
	MALE	复位中	复位中	Saved

Table 27.12 发出每个条件时的寄存器状态(2)(1of2)

注册符号	寄存器位名称	系统重置	RSTCTL Register	
			RI2CRST	INTLRST
SVCTL	SVAE2	复位中	复位中	Saved
	SVAE1	复位中	复位中	Saved
	SVAE0	复位中	复位中	Saved
	HOAE	复位中	复位中	Saved
	DVIDE	复位中	复位中	Saved
	HSMCE	复位中	复位中	Saved
	GCAE	复位中	复位中	Saved
REFCKCTL	IREFCKS[2:0]	复位中	复位中	Saved
STDBR	DSBRPO	复位中	复位中	Saved
	SBRHP[5:0]	复位中	复位中	Saved
	SBRLO[7:0]	复位中	复位中	Saved
EXTBR	EBRHO[7:0]	复位中	复位中	Saved
	EBRLO[7:0]	复位中	复位中	Saved
BFRECDT	FRECYC[8:0]	复位中	复位中	Saved
OUTCTL	SDODCS	复位中	复位中	Saved
	SDOD[2:0]	复位中	复位中	Saved
	EXCYC	复位中	复位中	Saved
	SOCWP	复位中	复位中	复位中
	SCOC	复位中	复位中	Saved
	SDOC	复位中	复位中	Saved
INCTL	SDID[1:0]	复位中	复位中	Saved
	DNFE	复位中	复位中	Saved
	DNFS[3:0]	复位中	复位中	Saved
TMOCTL	TOMDS[1:0]	复位中	复位中	Saved
	TOHCTL	复位中	复位中	Saved
	TOLCTL	复位中	复位中	Saved
	TODTS[1:0]	复位中	复位中	Saved

Table 27.12 Register states when issuing each condition (2) (2 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register	
			RI2CRST	INTLRST
WUCTL	WUFE	In reset	In reset	Saved
	WUFSYNE	In reset	In reset	Saved
	WUANFS	In reset	In reset	Saved
	WUACKS	In reset	In reset	Saved
ACKCTL	ACKTWP	In reset	In reset	In reset
	ACKT	In reset	In reset	In reset
	ACKR	In reset	In reset	In reset
SCSTRCTL	RWE	In reset	In reset	Saved
	ACKTWE	In reset	In reset	Saved

Table 27.13 Register states when issuing each condition (3)

Register symbol	Register bit name	System reset	RSTCTL Register	
			RI2CRST	INTLRST
CNDCTL	SPCND	In reset	In reset	In reset
	SRCND	In reset	In reset	In reset
	STCND	In reset	In reset	In reset
NTDTBP0	NTDTBP0[31:0]	In reset	In reset	In reset
BST	WUCNDDF	In reset	In reset	Saved
	TODF	In reset	In reset	In reset
	ALF	In reset	In reset	In reset
	TENDF	In reset	In reset	In reset
	NACKDF	In reset	In reset	In reset
	SPCNDDF	In reset	In reset	In reset
	STCNDDF	In reset	In reset	In reset
BSTE	WUCNDDE	In reset	In reset	Saved
	TODE	In reset	In reset	Saved
	ALE	In reset	In reset	Saved
	TENDE	In reset	In reset	Saved
	NACKDE	In reset	In reset	Saved
	SPCNDDE	In reset	In reset	Saved
	STCNDDE	In reset	In reset	Saved

Table 27.12 发出每个条件时的寄存器状态(2)(2of2)

注册符号	寄存器位名称	系统重置	RSTCTL Register	
			RI2CRST	INTLRST
WUCTL	WUFE	复位中	复位中	Saved
	WUFSYNE	复位中	复位中	Saved
	WUANFS	复位中	复位中	Saved
	WUACKS	复位中	复位中	Saved
ACKCTL	ACKTWP	复位中	复位中	复位中
	ACKT	复位中	复位中	复位中
	ACKR	复位中	复位中	复位中
SCSTRCTL	RWE	复位中	复位中	Saved
	ACKTWE	复位中	复位中	Saved

Table 27.13 发出每个条件时注册状态(3)

注册符号	寄存器位名称	系统重置	RSTCTL Register	
			RI2CRST	INTLRST
CNDCTL	SPCND	复位中	复位中	复位中
	SRCND	复位中	复位中	复位中
	STCND	复位中	复位中	复位中
NTDTBP0	NTDTBP0[31:0]	复位中	复位中	复位中
BST	WUCNDDF	复位中	复位中	Saved
	TODF	复位中	复位中	复位中
	ALF	复位中	复位中	复位中
	TENDF	复位中	复位中	复位中
	NACKDF	复位中	复位中	复位中
	SPCNDDF	复位中	复位中	复位中
	STCNDDF	复位中	复位中	复位中
BSTE	WUCNDDE	复位中	复位中	Saved
	TODE	复位中	复位中	Saved
	ALE	复位中	复位中	Saved
	TENDE	复位中	复位中	Saved
	NACKDE	复位中	复位中	Saved
	SPCNDDE	复位中	复位中	Saved
	STCNDDE	复位中	复位中	Saved

Table 27.14 Register states when issuing each condition (4)

Register symbol	Register bit name	System reset	RSTCTL Register	
			RI2CRST	INTLRST
BIE	WUCNDDIE	In reset	In reset	Saved
	TODIE	In reset	In reset	Saved
	ALIE	In reset	In reset	Saved
	TENDIE	In reset	In reset	Saved
	NACKDIE	In reset	In reset	Saved
	SPCNDDIE	In reset	In reset	Saved
	STCNDDIE	In reset	In reset	Saved
BSTFC	WUCNDDFC	In reset	In reset	Saved
	TODFC	In reset	In reset	Saved
	ALFC	In reset	In reset	Saved
	TENDFC	In reset	In reset	Saved
	NACKDFC	In reset	In reset	Saved
	SPCNDDFC	In reset	In reset	Saved
	STCNDDFC	In reset	In reset	Saved
NTST	RDBFF0	In reset	In reset	In reset
	TDBEF0	In reset	In reset	In reset
NTSTE	RDBFE0	In reset	In reset	Saved
	TDBEE0	In reset	In reset	Saved
NTIE	RDBFIE0	In reset	In reset	Saved
	TDBEIE0	In reset	In reset	Saved

Table 27.15 Register states when issuing each condition (5)

Register symbol	Register bit name	System reset	RSTCTL Register	
			RI2CRST	INTLRST
NTSTFC	RDBFFC0	In reset	In reset	Saved
	TDBEFC0	In reset	In reset	Saved

Table 27.16 Register states when issuing each condition (6)

Register symbol	Register bit name	System reset	RSTCTL Register	
			RI2CRST	INTLRST
BCST	BFREF	In reset	In reset	Saved
SVST	SVAF2	In reset	In reset	In reset
	SVAF1	In reset	In reset	In reset
	SVAF0	In reset	In reset	In reset
	HOAF	In reset	In reset	In reset
	DVIDF	In reset	In reset	In reset
	HSMCF	In reset	In reset	In reset
	GCAF	In reset	In reset	In reset
WUST	WUASYNF	In reset	In reset	Saved

Table 27.14 发出每个条件时注册状态(4)

注册符号	寄存器位名称	系统重置	RSTCTL Register	
			RI2CRST	INTLRST
BIE	WUCNDDIE	复位中	复位中	Saved
	TODIE	复位中	复位中	Saved
	ALIE	复位中	复位中	Saved
	TENDIE	复位中	复位中	Saved
	NACKDIE	复位中	复位中	Saved
	SPCNDDIE	复位中	复位中	Saved
	STCNDDIE	复位中	复位中	Saved
BSTFC	WUCNDDFC	复位中	复位中	Saved
	TODFC	复位中	复位中	Saved
	ALFC	复位中	复位中	Saved
	TENDFC	复位中	复位中	Saved
	NACKDFC	复位中	复位中	Saved
	SPCNDDFC	复位中	复位中	Saved
	STCNDDFC	复位中	复位中	Saved
NTST	RDBFF0	复位中	复位中	复位中
	TDBEF0	复位中	复位中	复位中
NTSTE	RDBFE0	复位中	复位中	Saved
	TDBEE0	复位中	复位中	Saved
NTIE	RDBFIE0	复位中	复位中	Saved
	TDBEIE0	复位中	复位中	Saved

Table 27.15 发布每个条件时注册状态(5)

注册符号	寄存器位名称	系统重置	RSTCTL Register	
			RI2CRST	INTLRST
NTSTFC	RDBFFC0	复位中	复位中	Saved
	TDBEFC0	复位中	复位中	Saved

Table 27.16 发出每个条件时注册状态(6)

注册符号	寄存器位名称	系统重置	RSTCTL Register	
			RI2CRST	INTLRST
BCST	BFREF	复位中	复位中	Saved
SVST	SVAF2	复位中	复位中	复位中
	SVAF1	复位中	复位中	复位中
	SVAF0	复位中	复位中	复位中
	HOAF	复位中	复位中	复位中
	DVIDF	复位中	复位中	复位中
	HSMCF	复位中	复位中	复位中
	GCAF	复位中	复位中	复位中
WUST	WUASYNF	复位中	复位中	Saved

Table 27.17 Register states when issuing each condition (7)

Register symbol	Register bit name	System reset	RSTCTL Register	
			RI2CRST	INTLRST
SDATBASy (y = 0 to 2)	SDADLS	In reset	In reset	Saved
	SDSTAD[9:0]	In reset	In reset	Saved

Table 27.18 Register states when issuing each condition (8)

Register symbol	Register bit name	System reset	RSTCTL Register	
			RI2CRST	INTLRST
SVDVADy (y = 0 to 2)	SSTADV	In reset	In reset	Saved
	SADLG	In reset	In reset	Saved
	SVAD[9:0]	In reset	In reset	Saved

Table 27.19 Register states when issuing each condition (9)

Register symbol	Register bit name	System reset	RSTCTL Register	
			RI2CRST	INTLRST
BITCNT	BCNT[4:0]	In reset	In reset	In reset
PRSTDBG	SDOLV	In reset	In reset	In reset
	SCOLV	In reset	In reset	In reset
	SDILV	In reset	In reset	Saved
	SCILV	In reset	In reset	Saved

27.7 Usage Notes

27.7.1 Settings for the Operating Clock

The following relation is required between the frequencies of the bus clock (PCLKA) and transfer clock (IICCLK):

IICCLK/2 ≤ PCLKA ≤ IICCLK

Table 27.17 发出每个条件时注册状态(7)

注册符号	寄存器位名称	系统重置	RSTCTL Register	
			RI2CRST	INTLRST
SDATBASy (y = 0 to 2)	SDADLS	复位中	复位中	Saved
	SDSTAD[9:0]	复位中	复位中	Saved

Table 27.18 发布每个条件时注册状态(8)

注册符号	寄存器位名称	系统重置	RSTCTL Register	
			RI2CRST	INTLRST
SVDVADy (y = 0 to 2)	SSTADV	复位中	复位中	Saved
	SADLG	复位中	复位中	Saved
	SVAD[9:0]	复位中	复位中	Saved

Table 27.19 发布每个条件时注册状态(9)

注册符号	寄存器位名称	系统重置	RSTCTL Register	
			RI2CRST	INTLRST
BITCNT	BCNT[4:0]	复位中	复位中	复位中
PRSTDBG	SDOLV	复位中	复位中	复位中
	SCOLV	复位中	复位中	复位中
	SDILV	复位中	复位中	Saved
	SCILV	复位中	复位中	Saved

27.7 使用说明

27.7.1 工作时钟设置

总线时钟(PCLKA)和传输时钟(IICCLK)的频率之间需要以下关系：

IICCLK/2 ≤ PCLKA ≤ IICCLK

28. CAN with Flexible Data-rate (CANFD)

This is the CANFD_B version of the CANFD peripheral module.

CANFD_B is referred to as CANFD in this chapter.

28.1 Overview

The CAN with Flexible Data-rate (CANFD) supports the following functions:

- CAN with Flexible Data rate.*1

Note 1. This feature is not available in the classical CAN function.

The CANFD module has a flexible message buffer and FIFO structure that meet the requirements of various applications. It also provides test modes to achieve high testability of the module that can be useful for power-on testing.

This specification describes of the CANFD module.

The CANFD mode is only available in certain products that support it.

28.1.1 CANFD Module

Table 28.1 CANFD module specifications (1 of 2)

Parameter		Specifications
Communication		CAN functionality conforms to CANFD ISO 11898-1 (2015)
Protocol engine version		RS-CANFD_PE V3.0
Data transfer rate	CANFD*1	Up to 1 Mbps for arbitration phase and up to 5 Mbps for data phase
	Classical CAN	Up to 1 Mbps
Operation frequency Peripheral clock		50 MHz (PCLKB) RAM clock: 100 MHz (PCLKA)
Data Link Layer (DLL) clock		Max ≤ 40 MHz
Input/Output pins		CTX0/CRX0
CAN channels		1 channel
Selectable ID type		11-bit Standard ID
		11-bit Standard ID + 18-bit Extended ID
Selectable frame type		Data frame (RTR = 0) (CAN and CANFD frames)
		Remote frame (RTR = 1) (only CAN frames)
Variable data byte count for data frames		DLC range: 0 to F
Message buffer		Up to 32 reception message buffers
		4 transmit message buffers
		1 transmission queue Automatic message transfer into transmission queues supported
FIFO number		2 reception FIFO buffers 1 COMMON FIFOs individually configurable as: ● Reception FIFO ● Transmission FIFO
Automatic delay interval timer for transmission		The delay timer can be applied to: ● Transmission FIFO

28. 具有灵活数据速率的CAN(CANFD)

这是CANFD外围模块的CANFD_B版本。

CANFD_B在本章中称为CANFD。

28.1 Overview

具有灵活数据速率的CAN(CANFD)支持以下功能：

●具有灵活数据速率的CAN。*1

注1.此功能在经典CAN功能中不可用。

CANFD模块具有灵活的报文缓冲区和FIFO结构，可以满足各种应用的要求。它还提供了测试模式来实现模块的高可测试性，这对于上电测试很有用。

本规范描述了CANFD模块。

CANFD模式仅在某些支持它的产品中可用。

28.1.1 CANFD Module

Table 28.1 CANFD模块规格(1of2)

Parameter		Specifications
Communication		CAN功能符合CANFDISO11898-1(2015)
协议引擎版本		RS-CANFD_PE V3.0
数据传输率	CANFD*1	仲裁阶段高达1Mbps，数据阶段高达5Mbps
	经典CAN	高达1Mbps
工作频率外设时钟		50 MHz (PCLKB) RAM clock: 100 MHz (PCLKA)
数据链路层(DLL)时钟		Max ≤ 40 MHz
Input/Output pins		CTX0/CRX0
CAN通道		1 channel
可选择的ID类型		11位标准ID
		11位标准ID+18位扩展ID
可选择的框架类型		数据帧(RTR=0)（CAN和CANFD帧）
		远程帧(RTR=1)（仅限CAN帧）
数据帧的可变数据字节数		DLC range: 0 to F
消息缓冲区		多达32个接收消息缓冲区
		4个发送消息缓冲区
		1个传输队列支持自动将消息传输到传输队列
FIFO number		2个接收FIFO缓冲器1个COMMONFIFO可单独配置为：● ● Transmission FIFO
传输的自动延迟间隔定时器		延时定时器可应用于：●

Table 28.1 CANFD module specifications (2 of 2)

Parameter	Specifications
Enhanced reception filtering	Support of 11 bits and 29 bits CAN identifier
	Programmable 29 bits CAN identifier acceptance filter mask for each entry
	Programmable routing capability for each FIFO and reception message buffers (up to 2 routing destinations)
	RTR and IDE masking
	Data Length Code (DLC) filter
	Message buffer payload overload protection
	Updating Acceptance Filter List (AFL) entry during communication
General software support	Automatic label information added to receive message (for upper software layer support)
Timer	TX and RX Time Stamp function
Power down function	Module start stop function for CAN node (Channel and Global Sleep mode)
RAM	RAM ECC protected (2 bits error detection, 1-bit error correction)
TrustZone Filter	One security attribution can be set

Note 1. The CANFD mode is available only for CANFD supported product.

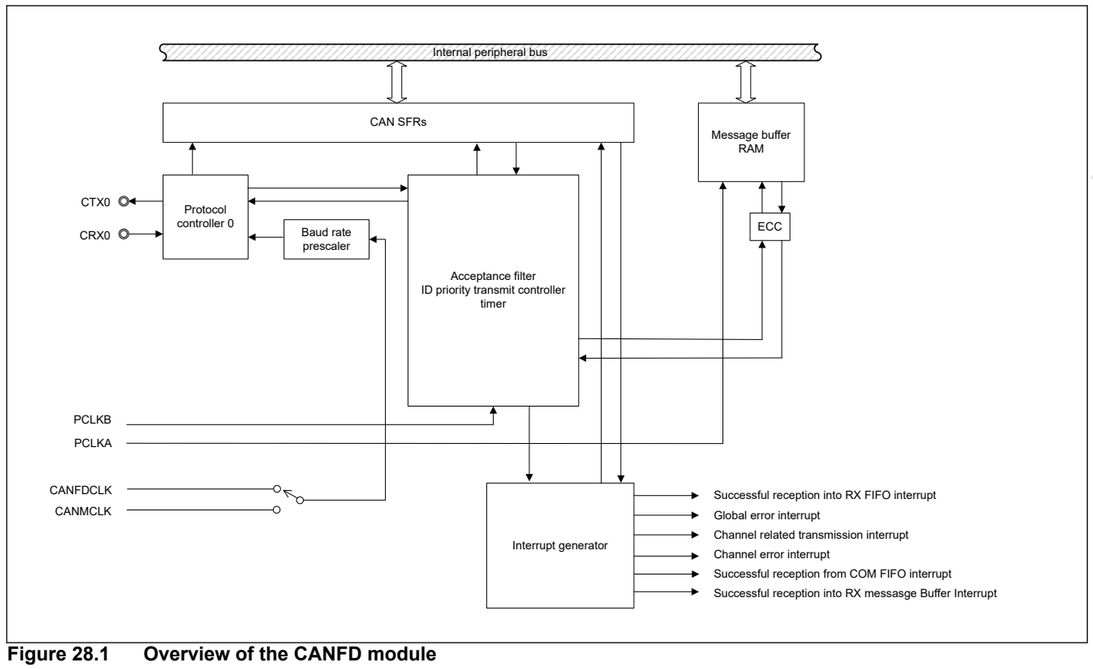


Figure 28.1 Overview of the CANFD module

- CTX0/CRX0:
  Input/Output pins of the CANFD module
- Protocol controller:
  Handles CAN protocol processing such as bus arbitration, bit timing at transmission and reception, stuffing, error handling
- Message buffer RAM:

Table 28.1 CANFD模块规格(2of2)

Parameter	Specifications
增强的接收过滤	支持11位和29位CAN标识符
	每个条目的可编程29位CAN标识符接受过滤器掩码
	每个FIFO和接收消息缓冲区的可编程路由功能（最多2个路由目标）
	RTR和IDE掩码
	数据长度代码(DLC)过滤器
	消息缓冲区负载过载保护
	在通信期间更新接受过滤器列表(AFL)条目
通用软件支持	接收消息自动添加标签信息（用于上层软件层支持）
Timer	TX和RX时间戳功能
断电功能	CAN节点的模块启动停止功能（通道和全局睡眠模式）
RAM	RAMECC保护（2位错误检测，1位错误纠正）
TrustZone Filter	可以设置一种安全属性

注1.CANFD模式仅适用于支持CANFD的产品。

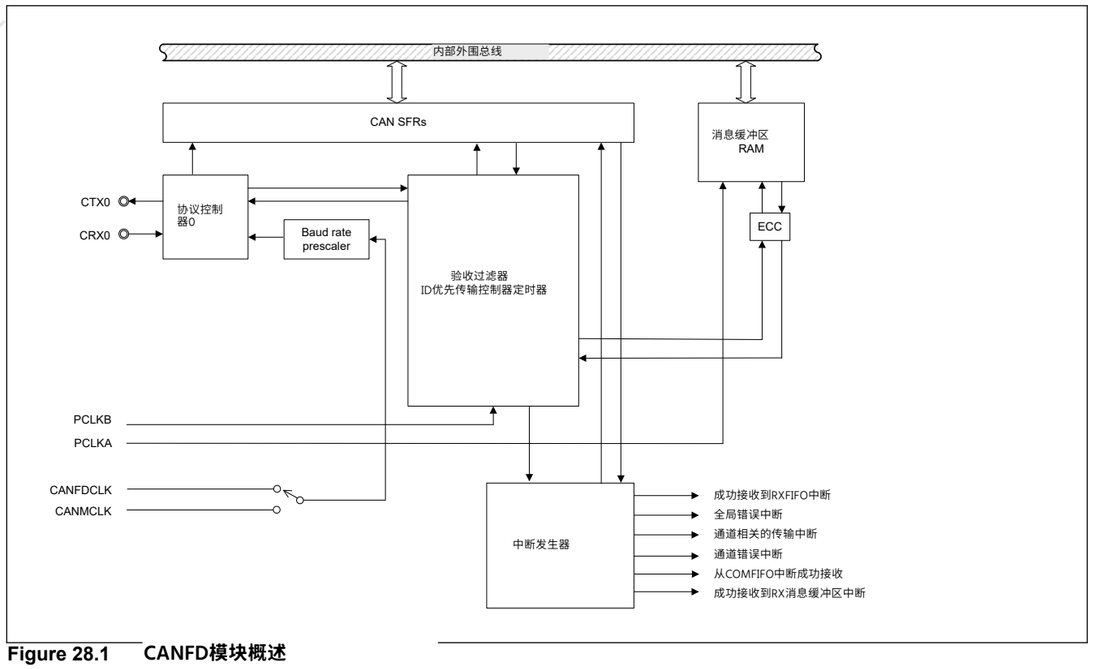


Figure 28.1 CANFD模块概述

- CTX0/CRX0:
  输入CANFD模块的输出引脚
- Protocol controller:
  处理CAN协议处理，例如总线仲裁、发送和接收时的位时序、填充、错误处理

●消息缓冲区RAM：

This RAM is used to store messages after reception or for transmission using a normal message buffer or a FIFO. Each message entry has an individual ID, data length code, data field, message pointer for upper layer application usage and a time stamp.
This RAM is used to store the message acceptance filtering entries. Each acceptance filter entry has an individual ID, data length code, data field, message pointer for upper layer application usage and message direction pointer.

- Acceptance filter:
  Performs filtering of received messages. The entries in the Acceptance filter list RAM are used for the filtering process.
- Two timers:
  - Reception Timestamp function
  - Transmission separation time for FIFO buffers
- Interrupt generator:
  Generates several types of global and channel interrupts
- CAN Special Function Registers (SFRs):
  Registers associated with CAN. See section 28.2. Register Descriptions.

28.1.2 Clock restriction

For the CAN communication the following restriction for the clocks should be satisfied:

- PCLKA / 2 = PCLKB ≥ CANFDCLK
- PCLKA / 2 = PCLKB ≥ CANMCLK

To avoid missing events the CAN engine clock (CANFDCLK or CANMCLK) frequency must be less than the PCLKB clock frequency.

To avoid loss of CAN message, the PCLKB should be set to a clock with a frequacy depend on the CAN communication Baud Rate. The constraint of a baud rate and a PCLKB clock is shown in Table 28.2.

Table 28.2 Clock restriction

	Baud rate	PCLKB
CANFD	1Mbps Nominal 5Mbps Data	PCLKB ≥ 40MHz
	500Kbps Nominall 5Mbps Data	PCLKB ≥ 32MHz
Classical CAN	1Mbps Data	PCLKB ≥ 32MHz

The frequency of CANFD and CANMCLK depend on the required baud rate. For information how to configure the baud rate, refer to section 28.4.1.3. Baud Rate.

28.2 Register Descriptions

28.2.1 Register Table

The reset value shown for the RAM area, consisting of CFDGAFLIDr, CFDGAFLMr, CFDGAFLP0r, CFDGAFLP1r, CFDRMBCPb, CFDRFMBCPb, CFDCFMBCP0, CFDTMBCPb, CFDTHLACC0, CFDTHLACC1 and CFDRPGACCk is valid after initialization of a hardware reset. See section 28.4.2. CAN Module Configuration after Hardware Reset for details of the initialization process.

If a write access with a size of 8 or 16 bits is performed for the RAM area, then the CANFD module does a read-modify write-access to the RAM location, because the RAM requires a 32-bit access through the ECC module.

For single bit error, the correct data is written back. For multiple bit errors, unknown data is written back.

Do not access the space where the register is not assigned.

The read data from the space where the register is not assigned is unknown.

此RAM用于在接收后存储消息或使用普通消息缓冲区或FIFO进行传输。每个消息条目都有一个单独的ID、数据长度代码、数据字段、供上层应用程序使用的消息指针和时间戳。此RAM用于存储消息接受过滤条目。每个接受过滤器条目都有一个单独的ID、数据长度代码、数据字段、供上层应用程序使用的消息指针和消息方向指针。

- Acceptance filter:
  对收到的消息执行过滤。接受过滤器列表RAM中的条目用于过滤过程。
- Two timers:
  –接收时间戳功能
  FIFO缓冲区的传输分离时间
- Interrupt generator:
  生成多种类型的全局和通道中断
- CAN特殊功能寄存器(SFR):
  与CAN相关的寄存器。请参阅第28.2节。注册说明。

28.1.2 时钟限制

对于CAN通信，应满足以下时钟限制：

- PCLKA / 2 = PCLKB ≥ CANFDCLK
- PCLKA / 2 = PCLKB ≥ CANMCLK

为避免丢失事件，CAN引擎时钟（CANFDCLK或CANMCLK）频率必须低于PCLKB时钟频率。

为避免CAN报文丢失，PCLKB应设置为频率取决于CAN通信的时钟波特率。波特率和PCLKB时钟的约束如表28.2所示。

Table 28.2 时钟限制

	Baud rate	PCLKB
CANFD	1Mbps标称5M bps数据	PCLKB ≥ 40MHz
	500Kbps Nominall 5Mbps Data	PCLKB ≥ 32MHz
经典CAN	1Mbps Data	PCLKB ≥ 32MHz

CANFD和CANMCLK的频率取决于所需的波特率。有关如何配置波特率的信息，请参阅第28.4.1.3节。波特率。

28.2 注册说明

28.2.1 寄存器表

RAM区域的复位值，包括CFDGAFLIDr、CFDGAFLMr、CFDGAFLP0r、CFDGAFLP1r、CFDRMBCPb、CFDRFMBCPb、CFDCFMBCP0、CFDTMBCPb、CFDTHLACC0、CFDTHLACC1和CFDRPGACCk在硬件复位初始化后有效。请参阅第28.4.2节。有关初始化过程的详细信息，请参阅硬件复位后的CAN模块配置。

如果对RAM区域执行大小为8或16位的写访问，则CANFD模块对RAM位置执行读–修改写访问，因为RAM需要通过ECC模块进行32位访问。

对于单位错误，正确的数据被写回。对于多位错误，将写回未知数据。

不要访问未分配寄存器的空间。

从未分配寄存器的空间读取的数据是未知的。

28.2.2 Legend

For all repetitive registers and bits, a lowercase index is used to indicate which slice is being referenced. If an index is being used, it is defined and described in the Register table it is being used in.

There is one global index used across all the registers and bits that need it.

Table 28.3 CANFD Registers (1 of 3)

Register name	Symbol	Value after Reset	Offset Address	Access size
Channel 0 Nominal Bitrate Configuration Register	CFDC0NCFG	0x00000000	0x0000	8, 16, 32
Channel 0 Control Register	CFDC0CTR	0x00000005	0x0004	8, 16, 32
Channel 0 Status Register	CFDC0STS	0x00000005	0x0008	8, 16, 32
Channel 0 Error Flag Register	CFDC0ERFL	0x00000000	0x000C	8, 16, 32
Global Configuration Register	CFDGCFG	0x00000000	0x0014	8, 16, 32
Global Control Register	CFDGCTR	0x00000005	0x0018	8, 16, 32
Global Status Register	CFDGSTS	0x0000000D	0x001C	8, 16, 32
Global Error Flag Register	CFDGERFL	0x00000000	0x0020	8, 16, 32
Global Timestamp Counter Register	CFDGTSC	0x00000000	0x0024	16, 32
Global Acceptance Filter List Entry Control Register	CFDGAFLECTR	0x00000000	0x0028	8, 16, 32
Global Acceptance Filter List Configuration Register	CFDGAFLCFG	0x00000000	0x002C	8, 16, 32
RX Message Buffer Number Register	CFDRMNB	0x00000000	0x0030	8, 16, 32
RX Message Buffer New Data Register	CFDRMND	0x00000000	0x0034	8, 16, 32
RX Message Buffer Interrupt Enable Configuration Register	CFDRMIEC	0x00000000	0x0038	8, 16, 32
RX FIFO Configuration / Control Registers a = [0:1]	CFDRFCCa	0x00000000	0x003C + a × 0x0004	8, 16, 32
RX FIFO Status Registers a = [0:1]	CFDRFSTSa	0x00000001	0x0044 + a × 0x0004	8, 16, 32
RX FIFO Pointer Control Registers a = [0:1]	CFDRFPCTRa	0x00000000	0x004C + a × 0x0004	8, 16, 32
Common FIFO Configuration / Control Register	CFDCFCC	0x00000000	0x0054	8, 16, 32
Common FIFO Status Register	CFDCFSTS	0x00000001	0x0058	8, 16, 32
Common FIFO Pointer Control Register	CFDCFPCTR	0x00000000	0x005C	8, 16, 32
FIFO Empty Status Register	CFDFESTS	0x00000103	0x0060	8, 16, 32
FIFO Full Status Register	CFDFFSTS	0x00000000	0x0064	8, 16, 32
FIFO Message Lost Status Register	CFDFMSTS	0x00000000	0x0068	8, 16, 32
RX FIFO Interrupt Flag Status Register	CFDRFISTS	0x00000000	0x006C	8, 16, 32
TX Message Buffer Control Registers i = [0:3]	CFDTMCi	0x00	0x0070 + i × 0x0001	8
TX Message Buffer Status Registers j = [0:3]	CFDTMSTSj	0x00	0x0074 + j × 0x0001	8
TX Message Buffer Transmission Request Status Register	CFDTMTRSTS	0x00000000	0x0078	8, 16, 32
TX Message Buffer Transmission Abort Request Status Register	CFDTMTARSTS	0x00000000	0x007C	8, 16, 32
TX Message Buffer Transmission Completion Status Register	CFDTMTCSTS	0x00000000	0x0080	8, 16, 32

28.2.2 Legend

对于所有重复的寄存器和位，小写索引用于指示正在引用哪个切片。如果正在使用索引，则在使用它的寄存器表中对其进行定义和描述。

所有需要它的寄存器和位都使用一个全局索引。

Table 28.3 CANFD寄存器(1of3)

注册名称	Symbol	复位后的值	偏移地址	访问大小
通道0标称比特率配置 Register	CFDC0NCFG	0x00000000	0x0000	8, 16, 32
通道0控制寄存器	CFDC0CTR	0x00000005	0x0004	8, 16, 32
通道0状态寄存器	CFDC0STS	0x00000005	0x0008	8, 16, 32
通道0错误标志寄存器	CFDC0ERFL	0x00000000	0x000C	8, 16, 32
全局配置寄存器	CFDGCFG	0x00000000	0x0014	8, 16, 32
全局控制寄存器	CFDGCTR	0x00000005	0x0018	8, 16, 32
全局状态寄存器	CFDGSTS	0x0000000D	0x001C	8, 16, 32
全局错误标志寄存器	CFDGERFL	0x00000000	0x0020	8, 16, 32
全局时间戳计数器寄存器	CFDGTSC	0x00000000	0x0024	16, 32
全局接受过滤器列表条目 控制寄存器	CFDGAFLECTR	0x00000000	0x0028	8, 16, 32
全局接受过滤器列表 配置寄存器	CFDGAFLCFG	0x00000000	0x002C	8, 16, 32
RX消息缓冲区编号寄存器	CFDRMNB	0x00000000	0x0030	8, 16, 32
RX报文缓冲区新数据寄存器	CFDRMND	0x00000000	0x0034	8, 16, 32
RX消息缓冲区中断使能 配置寄存器	CFDRMIEC	0x00000000	0x0038	8, 16, 32
RXFIFO配置控制 Registers a = [0:1]	CFDRFCCa	0x00000000	0x003C + a × 0x0004	8, 16, 32
RXFIFO状态寄存器a=[0:1]	CFDRFSTSa	0x00000001	0x0044 + a × 0x0004	8, 16, 32
RXFIFO指针控制寄存器a=[0:1]	CFDRFPCTRa	0x00000000	0x004C + a × 0x0004	8, 16, 32
通用FIFO配置控制 Register	CFDCFCC	0x00000000	0x0054	8, 16, 32
通用FIFO状态寄存器	CFDCFSTS	0x00000001	0x0058	8, 16, 32
通用FIFO指针控制寄存器	CFDCFPCTR	0x00000000	0x005C	8, 16, 32
FIFO空状态寄存器	CFDFESTS	0x00000103	0x0060	8, 16, 32
FIFO满状态寄存器	CFDFFSTS	0x00000000	0x0064	8, 16, 32
FIFO消息丢失状态寄存器	CFDFMSTS	0x00000000	0x0068	8, 16, 32
RXFIFO中断标志 状态寄存器	CFDRFISTS	0x00000000	0x006C	8, 16, 32
TX报文缓冲区控制寄存器i=[0:3]	CFDTMCi	0x00	0x0070 + i × 0x0001	8
TX报文缓冲区状态寄存器j=[0:3]	CFDTMSTSj	0x00	0x0074 + j × 0x0001	8
TX消息缓冲区传输 请求状态寄存器	CFDTMTRSTS	0x00000000	0x0078	8, 16, 32
TX消息缓冲区传输中止 请求状态寄存器	CFDTMTARSTS	0x00000000	0x007C	8, 16, 32
TX消息缓冲区传输 完成状态寄存器	CFDTMTCSTS	0x00000000	0x0080	8, 16, 32

Table 28.3 CANFD Registers (2 of 3)

Register name	Symbol	Value after Reset	Offset Address	Access size
TX Message Buffer Transmission Abort Status Register	CFDTMTASTS	0x00000000	0x0084	8, 16, 32
TX Message Buffer Interrupt Enable Configuration Register	CFDTMIEC	0x00000000	0x0088	8, 16, 32
TX Queue Configuration / Control Register	CFDTXQCC	0x00000000	0x008C	8, 16, 32
TX Queue Status Register	CFDTXQSTS	0x00000001	0x0090	8, 16, 32
TX Queue Pointer Control Register	CFDTXQPCTR	0x00000000	0x0094	8, 16, 32
TX History List Configuration / Control Register	CFDTHLCC	0x00000000	0x0098	8, 16, 32
TX History List Status Register	CFDTHLSTS	0x00000001	0x009C	8, 16, 32
TX History List Pointer Control Register	CFDTHLPCTR	0x00000000	0x00A0	8, 16, 32
Global TX Interrupt Status Register	CFDGTINTSTS	0x00000000	0x00A4	8, 16, 32
Global Test Configuration Register	CFDGTSTCFG	0x00000000	0x00A8	8, 16, 32
Global Test Control Register	CFDGTSTCTR	0x00000000	0x00AC	8, 16, 32
Global FD Configuration register	CFDGFDCFG	0x00000000	0x00B0	8, 16, 32
Global Lock Key Register	CFDGLOCKK	0x00000000	0x00B8	16, 32
Global AFL Ignore Entry Register	CFDGAFLIGNENT	0x00000000	0x00C0	8, 16, 32
Global AFL Ignore Control Register	CFDGAFLIGNCTR	0x00000000	0x00C4	16, 32
DMA Transfer Control Register	CFDCDTCT	0x00000000	0x00C8	8, 16, 32
DMA Transfer Status Register	CFDCDTSTS	0x00000000	0x00CC	8, 16, 32
Global SW reset Register	CFDGRSTC	0x00000000	0x00D8	16, 32
Channel 0 Data Bitrate Configuration Register	CFDC0DCFG	0x00000000	0x0100	8, 16, 32
Channel 0 CANFD Configuration Register	CFDC0FDCFG	0x00000000	0x0104	8, 16, 32
Channel 0 CANFD Control Register	CFDC0FDCTR	0x00000000	0x0108	8, 16, 32
Channel 0 CANFD Status Register	CFDC0FDSTS	0x00000000	0x010C	8, 16, 32
Channel 0 CANFD CRC Register	CFDC0FDCRC	0x00000000	0x0110	8, 16, 32
Global Acceptance Filter List ID Registers r = [1…16]	CFDGAFLIDr	0x00000000*1	0x0120 + (r-1) × 0x0010	8, 16, 32
Global Acceptance Filter List Mask Registers r = [1…16]	CFDGAFLMr	0x00000000*1	0x0124 + (r-1) × 0x0010	8, 16, 32
Global Acceptance Filter List Pointer 0 Registers r = [1…16]	CFDGAFLP0r	0x00000000*1	0x0128 + (r-1) × 0x0010	8, 16, 32
Global Acceptance Filter List Pointer 1 Registers r = [1…16]	CFDGAFLP1r	0x00000000*1	0x012C + (r-1) × 0x0010	8, 16, 32
RAM Test Page Access Registers k = [0…63]	CFDRPGACCk	0x00000000*1	0x0280 + k × 0x0004	8, 16, 32
RX FIFO Access ID Registers b = [0…1]	CFDRFIDb	0x00000000*1	0x0520 + b × 0x004C	8, 16, 32
RX FIFO Access Pointer Registers b = [0…1]	CFDRFPTRb	0x00000000*1	0x0524 + b × 0x004C	8, 16, 32
RX FIFO Access CANFD Status Registers b = [0…1]	CFDRFFDSTSb	0x00000000*1	0x0528 + b × 0x004C	8, 16, 32
RX FIFO Access Data Field p Registers b = [0…1] p = [0…15]	CFDRFDFbp	0x00000000*1	0x052C + p × 0x0004 + b × 0x004C	8, 16, 32
Common FIFO Access ID Register	CFDCFID	0x00000000*1	0x05B8	8, 16, 32

Table 28.3 CANFD寄存器(2of3)

注册名称	Symbol	复位后的值	偏移地址	访问大小
TX消息缓冲区传输中止状态寄存器	CFDTMTASTS	0x00000000	0x0084	8, 16, 32
TX报文缓冲区中断使能配置寄存器	CFDTMIEC	0x00000000	0x0088	8, 16, 32
TX队列配置控制Register	CFDTXQCC	0x00000000	0x008C	8, 16, 32
TX队列状态寄存器	CFDTXQSTS	0x00000001	0x0090	8, 16, 32
TX队列指针控制寄存器	CFDTXQPCTR	0x00000000	0x0094	8, 16, 32
TX历史列表配置控制Register	CFDTHLCC	0x00000000	0x0098	8, 16, 32
TX历史列表状态寄存器	CFDTHLSTS	0x00000001	0x009C	8, 16, 32
TX历史列表指针控制寄存器	CFDTHLPCTR	0x00000000	0x00A0	8, 16, 32
全局TX中断状态寄存器	CFDGTINTSTS	0x00000000	0x00A4	8, 16, 32
全局测试配置寄存器	CFDGTSTCFG	0x00000000	0x00A8	8, 16, 32
全局测试控制寄存器	CFDGTSTCTR	0x00000000	0x00AC	8, 16, 32
全局FD配置寄存器	CFDGFDCFG	0x00000000	0x00B0	8, 16, 32
全局锁定密钥寄存器	CFDGLOCKK	0x00000000	0x00B8	16, 32
全局AFL忽略条目寄存器	CFDGAFLIGNENT	0x00000000	0x00C0	8, 16, 32
全局AFL忽略控制寄存器	CFDGAFLIGNCTR	0x00000000	0x00C4	16, 32
DMA传输控制寄存器	CFDCDTCT	0x00000000	0x00C8	8, 16, 32
DMA传输状态寄存器	CFDCDTSTS	0x00000000	0x00CC	8, 16, 32
全局软件复位寄存器	CFDGRSTC	0x00000000	0x00D8	16, 32
通道0数据比特率配置Register	CFDC0DCFG	0x00000000	0x0100	8, 16, 32
通道0CANFD配置寄存器	CFDC0FDCFG	0x00000000	0x0104	8, 16, 32
通道0CANFD控制寄存器	CFDC0FDCTR	0x00000000	0x0108	8, 16, 32
通道0CANFD状态寄存器	CFDC0FDSTS	0x00000000	0x010C	8, 16, 32
通道0CANFDCRC寄存器	CFDC0FDCRC	0x00000000	0x0110	8, 16, 32
全局接受过滤器列表ID寄存器r=[1…16]	CFDGAFLIDr	0x00000000*1	0x0120 + (r-1) × 0x0010	8, 16, 32
全局接受过滤器列表掩码Registers r = [1…16]	CFDGAFLMr	0x00000000*1	0x0124 + (r-1) × 0x0010	8, 16, 32
全局接受过滤器列表指针0Registers r = [1…16]	CFDGAFLP0r	0x00000000*1	0x0128 + (r-1) × 0x0010	8, 16, 32
全局接受过滤器列表指针1Registers r = [1…16]	CFDGAFLP1r	0x00000000*1	0x012C + (r-1) × 0x0010	8, 16, 32
RAM测试页访问寄存器k=[0…63]	CFDRPGACCk	0x00000000*1	0x0280 + k × 0x0004	8, 16, 32
RXFIFO访问ID寄存器b=[0…1]	CFDRFIDb	0x00000000*1	0x0520 + b × 0x004C	8, 16, 32
RXFIFO访问指针寄存器b=[0…1]	CFDRFPTRb	0x00000000*1	0x0524 + b × 0x004C	8, 16, 32
RXFIFO访问CANFD状态Registers b = [0…1]	CFDRFFDSTSb	0x00000000*1	0x0528 + b × 0x004C	8, 16, 32
RXFIFO访问数据字段p寄存器b=[0…1]p=[0…15]	CFDRFDFbp	0x00000000*1	0x052C + p × 0x0004 + b × 0x004C	8, 16, 32
通用FIFO访问ID寄存器	CFDCFID	0x00000000*1	0x05B8	8, 16, 32

Table 28.3 CANFD Registers (3 of 3)

Register name	Symbol	Value after Reset	Offset Address	Access size
Common FIFO Access Pointer Register	CFDCFPTR	0x00000000*1	0x05BC	8, 16, 32
Common FIFO Access CANFD Control/ Status Register	CFDCFFDCSTS	0x00000000*1	0x05C0	8, 16, 32
Common FIFO Access Data Field p Registers p = [0…15]	CFDCFDFp	0x00000000*1	0x05C4 + p × 0x0004	8, 16, 32
TX Message Buffer ID Registers b = [0…3]	CFDTMIDb	0x00000000*1	0x0604 + b × 0x004C	8, 16, 32
TX Message Buffer Pointer Registers b = [0…3]	CFDTMPTRb	0x00000000*1	0x0608 + b × 0x004C	8, 16, 32
TX Message Buffer CANFD Control Registers b = [0…3]	CFDTMFDCTRb	0x00000000*1	0x060C + b × 0x004C	8, 16, 32
TX Message Buffer Data Field p Registers b = [0…3] p = [0…15]	CFDTMDFbp	0x00000000*1	0x0610 + p × 0x0004 + b × 0x004C	8, 16, 32
Channel 0 TX History List Access Registers 0	CFDTHLACC0	0x00000000*1	0x0740	8, 16, 32
Channel 0 TX History List Access Registers 1	CFDTHLACC1	0x00000000*1	0x0744	8, 16, 32
RX Message Buffer ID Registers b = [0…7]	CFDRMIDb	0x00000000*1	0x0920 + b × 0x004C	8, 16, 32
RX Message Buffer Pointer Registers b = [0…7]	CFDRMPTRb	0x00000000*1	0x0924 + b × 0x004C	8, 16, 32
RX Message Buffer CANFD Status Registers b = [0…7]	CFDRMFDSTSb	0x00000000*1	0x0928 + b × 0x004C	8, 16, 32
RX Message Buffer Data Field p Registers b = [0…7] p = [0…15]	CFDRMDFbp	0x00000000*1	0x092C + p × 0x0004 + b × 0x004C	8, 16, 32
RX Message Buffer ID Registers b = [8…15]	CFDRMIDb	0x00000000*1	0x0D20 + (b - 8) × 0x004C	8, 16, 32
RX Message Buffer Pointer Registers b = [8…15]	CFDRMPTRb	0x00000000*1	0x0D24 + (b - 8) × 0x004C	8, 16, 32
RX Message Buffer CANFD Status Registers b = [8…15]	CFDRMFDSTSb	0x00000000*1	0x0D28 + (b - 8) × 0x004C	8, 16, 32
RX Message Buffer Data Field p Registers b = [8…15] p = [0…15]	CFDRMDFbp	0x00000000*1	0x0D2C + p × 0x0004 + (b - 8) × 0x004C	8, 16, 32
RX Message Buffer ID Registers b = [16…23]	CFDRMIDb	0x00000000*1	0x1120 + (b - 16) × 0x004C	8, 16, 32
RX Message Buffer Pointer Registers b = [16…23]	CFDRMPTRb	0x00000000*1	0x1124 + (b - 16) × 0x004C	8, 16, 32
RX Message Buffer CANFD Status Registers b = [16…23]	CFDRMFDSTSb	0x00000000*1	0x1128 + (b - 16) × 0x004C	8, 16, 32
RX Message Buffer Data Field p Registers b = [16…23] p = [0…15]	CFDRMDFbp	0x00000000*1	0x112C + p × 0004 + (b - 16) × 0x004C	8, 16, 32
RX Message Buffer ID Registers b = [24…31]	CFDRMIDb	0x00000000*1	0x1520 + (b - 24) × 0x004C	8, 16, 32
RX Message Buffer Pointer Registers b = [24…31]	CFDRMPTRb	0x00000000*1	0x1524 + (b - 24) × 0x004C	8, 16, 32
RX Message Buffer CANFD Status Registers b = [24…31]	CFDRMFDSTSb	0x00000000*1	0x1528 + (b - 24) × 0x004C	8, 16, 32
RX Message Buffer Data Field p Registers b = [24…31] p = [0…15]	CFDRMDFbp	0x00000000*1	0x152C + p × 0x0004 + (b - 24) × 0x004C	8, 16, 32

Note 1. The RAM area is initialized after a hardware reset, see section 28.4.2. CAN Module Configuration after Hardware Reset.

Table 28.3 CANFD寄存器（3个中的3个）

注册名称	Symbol	复位后的值	偏移地址	访问大小
通用FIFO访问指针寄存器	CFDCFPTR	0x00000000*1	0x05BC	8, 16, 32
通用FIFO访问CANFD控制 状态寄存器	CFDCFFDCSTS	0x00000000*1	0x05C0	8, 16, 32
通用FIFO访问数据字段p Registers p = [0…15]	CFDCFDFp	0x00000000*1	0x05C4 + p × 0x0004	8, 16, 32
TX报文缓冲区ID寄存器b=[0…3]	CFDTMIDb	0x00000000*1	0x0604 + b × 0x004C	8, 16, 32
TX报文缓冲区指针寄存器b=[0…3]	CFDTMPTRb	0x00000000*1	0x0608 + b × 0x004C	8, 16, 32
TX消息缓冲区CANFD控制 Registers b = [0…3]	CFDTMFDCTRb	0x00000000*1	0x060C + b × 0x004C	8, 16, 32
TX报文缓冲区数据字段p寄存器 b=[0…3]p=[0…15]	CFDTMDFbp	0x00000000*1	0x0610 + p × 0x0004 + b × 0x004C	8, 16, 32
通道0TX历史列表访问 Registers 0	CFDTHLACC0	0x00000000*1	0x0740	8, 16, 32
通道0TX历史列表访问 Registers 1	CFDTHLACC1	0x00000000*1	0x0744	8, 16, 32
RX报文缓冲区ID寄存器b=[0…7]	CFDRMIDb	0x00000000*1	0x0920 + b × 0x004C	8, 16, 32
RX报文缓冲区指针寄存器b=[0…7]	CFDRMPTRb	0x00000000*1	0x0924 + b × 0x004C	8, 16, 32
RX消息缓冲区CANFD状态 Registers b = [0…7]	CFDRMFDSTSb	0x00000000*1	0x0928 + b × 0x004C	8, 16, 32
RX报文缓冲区数据字段p寄存器 b=[0…7]p=[0…15]	CFDRMDFbp	0x00000000*1	0x092C + p × 0x0004 + b × 0x004C	8, 16, 32
RX消息缓冲区ID寄存器b=[8…15]	CFDRMIDb	0x00000000*1	0x0D20 + (b - 8) × 0x004C	8, 16, 32
RX报文缓冲区指针寄存器b=[8…15]	CFDRMPTRb	0x00000000*1	0x0D24 + (b - 8) × 0x004C	8, 16, 32
RX消息缓冲区CANFD状态 Registers b = [8…15]	CFDRMFDSTSb	0x00000000*1	0x0D28 + (b - 8) × 0x004C	8, 16, 32
RX报文缓冲区数据字段p寄存器b =[8…15]p=[0…15]	CFDRMDFbp	0x00000000*1	0x0D2C + p × 0x0004 + (b - 8) × 0x004C	8, 16, 32
RX报文缓冲区ID寄存器b=[16…23]	CFDRMIDb	0x00000000*1	0x1120 + (b - 16) × 0x004C	8, 16, 32
RX报文缓冲区指针寄存器b=[16…23]	CFDRMPTRb	0x00000000*1	0x1124 + (b - 16) × 0x004C	8, 16, 32
RX消息缓冲区CANFD状态 Registers b = [16…23]	CFDRMFDSTSb	0x00000000*1	0x1128 + (b - 16) × 0x004C	8, 16, 32
RX消息缓冲区数据字段p Registers b = [16…23] p = [0…15]	CFDRMDFbp	0x00000000*1	0x112C + p × 0004 + (b - 16) × 0x004C	8, 16, 32
RX报文缓冲区ID寄存器b=[24…31]	CFDRMIDb	0x00000000*1	0x1520 + (b - 24) × 0x004C	8, 16, 32
RX报文缓冲区指针寄存器b=[24…31]	CFDRMPTRb	0x00000000*1	0x1524 + (b - 24) × 0x004C	8, 16, 32
RX消息缓冲区CANFD状态 Registers b = [24…31]	CFDRMFDSTSb	0x00000000*1	0x1528 + (b - 24) × 0x004C	8, 16, 32
RX消息缓冲区数据字段p Registers b = [24…31] p = [0…15]	CFDRMDFbp	0x00000000*1	0x152C + p × 0x0004 + (b - 24) × 0x004C	8, 16, 32

注1.RAM区在硬件复位后初始化，见28.4.2节。硬件复位后的CAN模块配置。

28.2.3 CFDC0NCFG : Channel 0 Nominal Bitrate Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0000

Bit position:	31							25	24							17	16							10	9							0
Bit field:	NTSEG2[6:0]								NTSEG1[7:0]								NSJW[6:0]								NBRP[9:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	NBRP[9:0]	Channel Nominal Baud Rate Prescaler Nominal baud rate prescaler division ratio	R/W
16:10	NSJW[6:0]	Resynchronization Jump Width 0x00: 1 Tq 0x01: 2 Tq ⋮ 0x7E: 127 Tq 0x7F: 128 Tq	R/W
24:17	NTSEG1[7:0]	Timing Segment 1 0x00: Reserved 0x01: 2 Tq 0x02: 3 Tq 0x03: 4 Tq ⋮ 0xFE: 255 Tq 0xFF: 256 Tq	R/W
31:25	NTSEG2[6:0]	Timing Segment 2 0x00: Reserved 0x01: 2 Tq ⋮ 0x7E: 127 Tq 0x7F: 128 Tq	R/W

Note: Tq means time quantum.

This register configures the transmission/reception nominal baud rate parameters of the channels.

NBRP[9:0] bits (Channel Nominal Baud Rate Prescaler)

The NBRP[9:0] bits are used to define the peripheral bus clock periods contained in a time quantum.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the CANFD channel is in CH_RESET or CH_HALT mode.

NSJW[6:0] bits (Resynchronization Jump Width)

The NSJW[6:0] bits set the synchronization jump width. A value from 1 to 128 time quanta can be set.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the CANFD channel is in CH_RESET or CH_HALT mode.

NTSEG1[7:0] bits (Timing Segment 1)

The NTSEG1[7:0] bits set the segment TSEG1 to compensate for edges on the CAN bus with a positive phase error. These bits contain the propagation segment.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the CANFD channel is in CH_RESET or CH_HALT mode.

Additionally, configure a Tq value only between 2 and 256, inclusive. See section 28.4.1.2. CAN Bit Timing for more details.

28.2.3 CFDC0NCFG：通道0标称比特率配置寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0000

Bit position:	31							25	24							17	16							10	9							0
Bit field:	NTSEG2[6:0]								NTSEG1[7:0]								NSJW[6:0]								NBRP[9:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	NBRP[9:0]	通道标称波特率预分频器 标称波特率预分频比	R/W
16:10	NSJW[6:0]	再同步跳转宽度 0x00: 1 Tq 0x01: 2 Tq ⋮ 0x7E: 127 Tq 0x7F: 128 Tq	R/W
24:17	NTSEG1[7:0]	时序段1 0x00: Reserved 0x01: 2 Tq 0x02: 3 Tq 0x03: 4 Tq ⋮ 0xFE: 255 Tq 0xFF: 256 Tq	R/W
31:25	NTSEG2[6:0]	计时段2 0x00: Reserved 0x01: 2 Tq ⋮ 0x7E: 127 Tq 0x7F: 128 Tq	R/W

Note: Tq表示时间量。

该寄存器配置通道的发送接收标称波特率参数。

NBRP[9:0]位（通道标称波特率预分频器）

NBRP[9:0]位用于定义包含在时间片中的外围总线时钟周期。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。

NSJW[6:0]位（重新同步跳转宽度）

NSJW[6:0]位设置同步跳转宽度。可以设置1到128个时间量子的值。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。

NTSEG1[7:0]位（时序段1）

NTSEG1[7:0]位设置段TSEG1以补偿CAN总线上具有正相位误差的边沿。这些位包含传播段。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。

此外，仅在2和256之间配置Tq值（包括2和256）。请参阅第28.4.1.2节。CAN位时序了解更多详情。

NTSEG2[6:0] bits (Timing Segment 2)

The NTSEG2[6:0] bits set the segment TSEG2 to compensate for edges on the CAN bus with a negative phase error.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the CANFD channel is in CH_RESET or CH_HALT mode.

Additionally, configure a Tq value only between 2 and 128, inclusive.

28.2.4 CFDC0CTR : Channel 0 Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ROM	BFT	—	—	—	CTMS[1:0]		CTME	ERRD	BOM[1:0]		—	TDCV FIE	SOCO IE	EOCO IE	TAIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ALIE	BLIE	OLIE	BORIE	BOEIE	EPIE	EWIE	BEIE	—	—	—	—	RTBO	CSLP R	CHMDC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
1:0	CHMDC[1:0]	Channel Mode Control 0 0: Channel operation mode request 0 1: Channel reset request 1 0: Channel halt request 1 1: Keep current value	R/W
2	CSLPR	Channel Sleep Request 0: Channel sleep request disabled 1: Channel sleep request enabled	R/W
3	RTBO	Return from Bus-Off 0: Channel is not forced to return from bus-off 1: Channel is forced to return from bus-off	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	BEIE	Bus Error Interrupt Enable 0: Bus error interrupt disabled 1: Bus error interrupt enabled	R/W
9	EWIE	Error Warning Interrupt Enable 0: Error warning interrupt disabled 1: Error warning interrupt enabled	R/W
10	EPIE	Error Passive Interrupt Enable 0: Error passive interrupt disabled 1: Error passive interrupt enabled	R/W
11	BOEIE	Bus-Off Entry Interrupt Enable 0: Bus-off entry interrupt disabled 1: Bus-off entry interrupt enabled	R/W
12	BORIE	Bus-Off Recovery Interrupt Enable 0: Bus-off recovery interrupt disabled 1: Bus-off recovery interrupt enabled	R/W
13	OLIE	Overload Interrupt Enable 0: Overload interrupt disabled 1: Overload interrupt enabled	R/W
14	BLIE	Bus Lock Interrupt Enable 0: Bus lock interrupt disabled 1: Bus lock interrupt enabled	R/W

NTSEG2[6:0]位（时序段2）

NTSEG2[6:0]位设置段TSEG2以补偿CAN总线上的边沿与负相位误差。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。

此外，仅将Tq值配置在2到128之间（包括2到128）。

28.2.4 CFDC0CTR:通道0控制寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ROM	BFT	—	—	—	CTMS[1:0]		CTME	ERRD	BOM[1:0]		—	TDCV FIE	SOCO IE	EOCO IE	TAIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ALIE	BLIE	OLIE	BORIE	BOEIE	EPIE	EWIE	BEIE	—	—	—	—	RTBO	CSLP R	CHMDC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
1:0	CHMDC[1:0]	通道模式控制 00：通道操作模式请求01：通道复位请求10：通道停止请求11：保持当前值	R/W
2	CSLPR	通道休眠请求 0：禁用通道睡眠请求1：启用通道睡眠请求	R/W
3	RTBO	从巴士下车返回 0：通道不强制从总线关闭返回1：通道强制从总线关闭返回	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	BEIE	总线错误中断使能 0：禁止总线错误中断1：允许总线错误中断	R/W
9	EWIE	错误警告中断使能 0：禁止错误警告中断1：允许错误警告中断	R/W
10	EPIE	错误被动中断使能 0：禁用错误被动中断1：启用错误被动中断	R/W
11	BOEIE	总线关闭进入中断使能 0：禁止总线关闭进入中断1：允许总线关闭进入中断	R/W
12	BORIE	总线关闭恢复中断使能 0：禁止总线关闭恢复中断1：允许总线关闭恢复中断	R/W
13	OLIE	过载中断使能 0：禁止过载中断1：允许过载中断	R/W
14	BLIE	总线锁定中断使能 0：禁止总线锁定中断1：使能总线锁定中断	R/W

Bit	Symbol	Function	R/W
15	ALIE	Arbitration Lost Interrupt Enable 0: Arbitration lost interrupt disabled 1: Arbitration lost interrupt enabled	R/W
16	TAIE	Transmission Abort Interrupt Enable 0: TX abort interrupt disabled 1: TX abort interrupt enabled	R/W
17	EOCOIE	Error Occurrence Counter Overflow Interrupt Enable 0: Error occurrence counter overflow interrupt disabled 1: Error occurrence counter overflow interrupt enabled	R/W
18	SOCOIE	Successful Occurrence Counter Overflow Interrupt Enable 0: Successful occurrence counter overflow interrupt disabled 1: Successful occurrence counter overflow interrupt enabled	R/W
19	TDCVFIE*1	Transceiver Delay Compensation Violation Interrupt Enable 0: Transceiver delay compensation violation interrupt disabled 1: Transceiver delay compensation violation interrupt enabled	R/W
20	—	This bit is read as 0. The write value should be 0.	R/W
22:21	BOM[1:0]	Channel Bus-Off Mode 0 0: Normal mode (comply with ISO 11898-1) 0 1: Entry to Halt mode automatically at bus-off start 1 0: Entry to Halt mode automatically at bus-off end 1 1: Entry to Halt mode (during bus-off recovery period) by software	R/W
23	ERRD	Channel Error Display 0: Only the first set of error codes displayed 1: Accumulated error codes displayed	R/W
24	CTME	Channel Test Mode Enable 0: Channel test mode disabled 1: Channel test mode enabled	R/W
26:25	CTMS[1:0]	Channel Test Mode Select 0 0: Basic test mode 0 1: Listen-only mode 1 0: Self-test mode 0 (External loopback mode) 1 1: Self-test mode 1 (Internal loopback mode)	R/W
29:27	—	These bits are read as 0. The write value should be 0.	R/W
30	BFT	Bit Flip Test 0: First data bit of reception stream not inverted 1: First data bit of reception stream inverted	R/W
31	ROM*1	Restricted Operation Mode 0: Restricted operation mode disabled 1: Restricted operation mode enabled	R/W

Note 1. These bits are not available in the classical CAN function.

Channel Control register controls the modes of the related channel. It is used to enable generation of interrupts if errors are detected on the CAN bus connected to this channel. It is also used to configure the channel in test mode.

CHMDC[1:0] bits (Channel Mode Control)

The CHMDC[1:0] bits can be used to configure modes of the CAN channel.

CAN mode transitions are described in more details in section 28.3.3. Channel Modes.

Setting CHMDC[1:0] bits to 11b has no effect. When the CANFD module is in GL_HALT mode, these bits can only be set to 10b or 01b. These bits cannot be set in CH_SLEEP mode.

These bits can change automatically when transitioning to Halt mode by the CFDC0CTR.BOM settings.

If CPU write access to CFDC0CTR.CHMDC occurs at the same time when the CAN channel enters Halt mode (at the start of bus-off when CFDC0CTR.BOM = 01b, or at the end of bus-off when CFDC0CTR.BOM = 10b), then the CPU write access has the highest priority.

The CAN channel changes the value of CFDC0CTR.CHMDC within the Channel Control Registers for the specified cases only if the CFDC0CTR.CHMDC value is 00b (Operation mode).

Bit	Symbol	Function	R/W
15	ALIE	仲裁丢失中断使能 0：禁止仲裁丢失中断1：使能仲裁丢失中断	R/W
16	TAIE	传输中止中断使能 0：禁用TX中止中断1：启用TX中止中断	R/W
17	EOCOIE	错误发生计数器溢出中断使能 0：错误发生计数器溢出中断禁止1：错误发生计数器溢出中断允许	R/W
18	SOCOIE	成功发生计数器溢出中断使能 0：禁止成功发生计数器溢出中断1：使能成功发生计数器溢出中断	R/W
19	TDCVFIE*1	收发器延迟补偿违规中断使能 0：禁止收发器延迟补偿违规中断1：使能收发器延迟补偿违规中断	R/W
20	—	该位读取为0。写入值应为0。	R/W
22:21	BOM[1:0]	通道总线关闭模式 00：正常模式（符合ISO11898-1）01：在总线关闭开始时自动进入停止模式10：在总线关闭结束时自动进入停止模式11：进入停止模式（在总线关闭期间）关闭恢复期）通过软件	R/W
23	ERRD	通道错误显示 0：只显示第一组错误码1：显示累计错误码	R/W
24	CTME	通道测试模式启用 0：禁用通道测试模式1：启用通道测试模式	R/W
26:25	CTMS[1:0]	通道测试模式选择 00：基本测试模式01：只听模式10：自测模式0（外部环回模式）11：自测模式1（内部环回模式）	R/W
29:27	—	这些位被读取为0。写入值应为0。	R/W
30	BFT	位翻转测试 0：接收流的第一个数据位不反转1：接收流的第一个数据位反转	R/W
31	ROM*1	受限操作模式 0：禁用限制操作模式1：启用限制操作模式	R/W

注1.这些位在经典CAN功能中不可用。

通道控制寄存器控制相关通道的模式。如果在连接到此通道的CAN总线上检测到错误，它用于启用中断生成。它还用于在测试模式下配置通道。

CHMDC[1:0]位（通道模式控制）

CHMDC[1:0]位可用于配置CAN通道的模式。

CAN模式转换在第28.3.3节中有更详细的描述。频道模式。

将CHMDC[1:0]位设置为11b无效。当CANFD模块处于GL_HALT模式时，这些位只能设置为10b或01b。这些位不能在CH_SLEEP模式下设置。

当通过CFDC0CTR.BOM设置转换到暂停模式时，这些位可以自动更改。

如果CPU对CFDC0CTR.CHMDC的写访问发生在CAN通道进入Halt模式的同时（当CFDC0CTR.BOM=01b时在总线关闭开始时，或者当CFDC0CTR.BOM=10b时在总线关闭结束时），则CPU写访问的优先级最高。

仅当CFDC0CTR.CHMDC值为00b（操作模式）时，CAN通道才会在指定情况下更改通道控制寄存器中CFDC0CTR.CHMDC的值。

CSLPR bit (Channel Sleep Request)

When the CSLPR bit is 1, a Sleep mode request is generated for the corresponding CAN channel

When this bit is 0, a request to exit Sleep mode is generated for the related CANFD channel.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_SLEEP mode.

RTBO bit (Return from Bus-Off)

When the protocol controller of the CAN channel enters bus-off state, you can force a recovery from bus-off state by setting the RTBO bit in the Channel Control Register to 1.

The error state changes from bus-off state to integrating with a maximum delay of 1 CAN bit time.

When the RTBO bit is set to 1, the REC and TEC registers are initialized and the Bus-Off Status bit (Channel Bus-off Status, CFDC0STS.BOSTS) is set to 0.

Registers other than the REC and TEC registers are not initialized by this command. Even if CFDC0CTR.BORIE is set, a bus-off recovery interrupt is not generated by this recovery from the bus-off state.

The RTBO bit cannot be set in CH_SLEEP mode. Setting this bit in any state other than bus-off state has no effect and the bit is cleared immediately. The read value is always 0.

Return from the Bus-Off command should be used only when CFDC0CTR.BOM is set to 00b.

Only write to this bit when the related CANFD channel is in CH_OPERATION mode. This bit is automatically cleared when set by software.

BEIE bit (Bus Error Interrupt Enable)

When the BEIE and the CFDC0ERFL.BEF bits are both 1, an error interrupt request is generated.

This bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

EWIE bit (Error Warning Interrupt Enable)

When the EWIE and the CFDC0ERFL.EWF bits are both 1, an error interrupt request is generated.

The EWIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

EPIE bit (Error Passive Interrupt Enable)

An error interrupt request is generated when the EPIE bit and the CFDC0ERFL.EPF are both 1.

The EPIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

BOEIE bit (Bus-Off Entry Interrupt Enable)

When the BOEIE and the CFDC0ERFL.BOEF bits are both 1, an error interrupt request is generated.

The BOEIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

BORIE bit (Bus-Off Recovery Interrupt Enable)

When the BORIE and the CFDC0ERFL.BORF bits are both 1, an error interrupt request is generated.

The BORIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

OLIE bit (Overload Interrupt Enable)

When the OLIE and the CFDC0ERFL.OVLF bits are both 1, an error interrupt request is generated.

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

BLIE bit (Bus Lock Interrupt Enable)

When the BLIE and the CFDC0ERFL.BLF bits are both 1, an error interrupt request is generated.

CSLPR位（通道休眠请求）

当CSLPR位为1时，为相应的CAN通道生成休眠模式请求

当该位为0时，会为相关CANFD通道生成退出休眠模式的请求。

仅当相关CANFD通道处于CH_RESET或CH_SLEEP模式时才写入该位。

RTBO位（从总线关闭返回）

当CAN通道的协议控制器进入总线关闭状态时，您可以通过将通道控制寄存器中的RTBO位设置为1来强制从总线关闭状态恢复。

错误状态从总线关闭状态变为积分，最大延迟为1个CAN位时间。

当RTBO位设置为1时，REC和TEC寄存器被初始化并且总线关闭状态位（通道总线关闭状态，CFDC0STS.BOSTS)设置为0。

该命令不初始化REC和TEC寄存器以外的寄存器。即使设置了CFDC0CTR.BORIE，从总线关闭状态恢复也不会产生总线关闭恢复中断。

在CH_SLEEP模式下不能设置RTBO位。将该位设置为总线关闭状态以外的任何状态均无效，并且该位立即被清除。读取值始终为0。

只有当CFDC0CTR.BOM设置为00b时，才应使用从总线关闭命令返回。

仅当相关CANFD通道处于CH_OPERATION模式时才写入该位。该位由软件置位时自动清零。

BEIE位（总线错误中断使能）

当BEIE和CFDC0ERFL.BEF位都为1时，产生错误中断请求。

在CH_SLEEP模式下不能设置该位。仅当相关CANFD通道处于CH_RESET模式时才写入该位。

EWIE位（错误警告中断使能）

当EWIE和CFDC0ERFL.EWF位都为1时，会产生错误中断请求。

在CH_SLEEP模式下不能设置EWIE位。仅当相关CANFD通道处于CH_RESET模式时才写入该位。

EPIE位（错误被动中断使能）

当EPIE位和CFDC0ERFL.EPF都为1时产生错误中断请求。

在CH_SLEEP模式下不能设置EPIE位。仅当相关CANFD通道处于CH_RESET模式时才写入该位。

BOEIE位（总线关闭进入中断允许）

当BOEIE和CFDC0ERFL.BOEF位均为1时，会产生错误中断请求。

在CH_SLEEP模式下不能设置BOEIE位。仅当相关CANFD通道处于CH_RESET mode.

BORIE位（总线关闭恢复中断使能）

当BORIE和CFDC0ERFL.BORF位均为1时，会产生错误中断请求。

在CH_SLEEP模式下不能设置BORIE位。仅当相关CANFD通道处于CH_RESET mode.

OLIE位（过载中断使能）

当OLIE和CFDC0ERFL.OVLF位均为1时，将产生错误中断请求。

在CH_SLEEP模式下不要写入该位。仅当相关CANFD通道处于CH_RESET模式时才写入该位。

BLIE位（总线锁定中断使能）

当BLIE和CFDC0ERFL.BLF位都为1时，会产生错误中断请求。

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

ALIE bit (Arbitration Lost Interrupt Enable)

When the ALIE and the CFDC0ERFL.ALF bits are both 1, an error interrupt request is generated.

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

TAIE bit (Transmission Abort Interrupt Enable)

When the TAIE bit is 1 and a transmission is successfully aborted from a TX MB belonging to the corresponding CAN channel, an interrupt request is generated.

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

EOCOIE bit (Error Occurrence Counter Overflow Interrupt Enable)

When the EOCOIE bit is 1 and the CFDC0FDSTS.EOCO bit belonging to the corresponding CAN channel is 1, an error interrupt request is generated.

The EOCOIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

SOCOIE bit (Successful Occurrence Counter Overflow Interrupt Enable)

When the SOCOIE bit is 1 and the CFDC0FDSTS.SOCO bit belonging to the corresponding CAN channel is 1, an error interrupt request is generated.

The SOCOIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

TDCVFIE bit (Transceiver Delay Compensation Violation Interrupt Enable)

When the TDCVFIE bit is 1 and the CFDC0FDSTS.TDCVF bit belonging to the corresponding CAN channel is 1, an error interrupt request is generated.

The TDCVFIE bit cannot be set in CH_SLEEP mode.

Only write to this bit when the related CANFD channel is in CH_RESET mode. Do not set this bit when in Classical-only mode.

Note: This bit is not available in the classical CAN function.

BOM[1:0] bits (Channel Bus-Off Mode)

The BOM[1:0]bits control the timing of the recovery from Bus-Off mode of the CANFD Channel.

Do not write to these bits in CH_SLEEP mode. Only write to these bits when the related CANFD channel is in CH_RESET mode.

Only write to these bits when the related CANFD channel is in CH_RESET mode.

ERRD bit (Channel Error Display)

The ERRD bit controls the display mode of the error flag bits [14:8] in the Channel Error Flag Register (CFDC0ERFL).

If the ERRD bit is 0 and more than one error occur at the same time, the error flag bits are set for all the errors that occurred at the same time. No further errors are flagged until CFDC0ERFL[14:8] is cleared.

Do not write to the ERRD bit in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

CTME bit (Channel Test Mode Enable)

The CTME bit enables the channel test modes.

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_HALT mode.

在CH_SLEEP模式下不要写入该位。仅当相关CANFD通道处于CH_RESET模式时才写入该位。

ALIE位（仲裁丢失中断使能）

当ALIE和CFDC0ERFL.ALF位都为1时，会产生错误中断请求。

在CH_SLEEP模式下不要写入该位。仅当相关CANFD通道处于CH_RESET模式时才写入该位。

TAIE位（发送中止中断使能）

当TAIE位为1并且从属于相应CAN通道的TXMB成功中止传输时，将产生中断请求。

在CH_SLEEP模式下不要写入该位。仅当相关CANFD通道处于CH_RESET模式时才写入该位。

EOCOIE位（错误发生计数器溢出中断使能）

当EOCOIE位为1且属于相应CAN通道的CFDC0FDSTS.EOCO位为1时，产生错误中断请求。

在CH_SLEEP模式下不能设置EOCOIE位。仅当相关CANFD通道处于CH_RESET mode.

SOCOIE位（成功发生计数器溢出中断使能）

当SOCOIE位为1且属于相应CAN通道的CFDC0FDSTS.SOCO位为1时，产生错误中断请求。

在CH_SLEEP模式下不能设置SOCOIE位。仅当相关CANFD通道处于CH_RESET mode.

TDCVFIE位（收发器延迟补偿违反中断允许）

当TDCVFIE位为1且属于相应CAN通道的CFDC0FDSTS.TDDCF位为1时，产生错误中断请求。

在CH_SLEEP模式下不能设置TDCVFIE位。

仅当相关CANFD通道处于CH_RESET模式时才写入该位。在仅经典模式下不要设置该位。

Note: 该位在经典CAN功能中不可用。

BOM[1:0] bits (Channel Bus-Off Mode)

BOM[1:0]位控制CANFD通道从总线关闭模式恢复的时序。

请勿在CH_SLEEP模式下写入这些位。仅当相关CANFD通道处于CH_RESET模式时才写入这些位。

仅当相关CANFD通道处于CH_RESET模式时才写入这些位。

ERRD位（通道错误显示）

ERRD位控制通道错误标志寄存器(CFDC0ERFL)中错误标志位[14:8]的显示模式。

如果ERRD位为0并且同时发生多个错误，则为同时发生的所有错误设置错误标志位。在清除CFDC0ERFL[14:8]之前不会标记更多错误。

请勿在CH_SLEEP模式下写入ERRD位。仅当相关CANFD通道处于CH_RESET或CH_HALT模式。

CTME位（通道测试模式启用）

CTME位启用通道测试模式。

在CH_SLEEP模式下不要写入该位。仅当相关CANFD通道处于CH_HALT模式时才写入该位。

CTMS[1:0] bits (Channel Test Mode Select)

The CTMS[1:0] bits are used to select the required test mode.

Do not write to these bits in CH_SLEEP or CH_RESET mode. Only write to these bits when the related CANFD channel is in CH_HALT mode.

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

BFT bit (Bit Flip Test)

The BFT bit checks the internal CRC generator logic of the protocol controller.

It inverts the first bit (ID bit) of the CAN message data stream being received, so that the internal generated CRC result will not match the received CRC value of the frame. Refer to the bit stuffing rule, when using this feature, as there is the possibility of receiving a stuff error (due to the inversion) rather than a CRC error.

The internal generated CRC value is always observed in the following registers:

- CFDC0ERFL.CRCREG (Classical CAN frames)
- CFDC0FDCRC.CRCREG (CANFD frames).*1

Note 1. This feature is not available in the classical CAN function.

Some restriction exist when using this bit:

Other CAN node will send a reference message and the receiver node(s) can invert one bit of incoming bit stream.

Note: The transmitter and receiver modes share the same CRC generator, therefore it is not necessary to consider the modes separately when testing.

The Bit Flip test mode is enabled if the BFT (new control signal that inverts the first bit of the bit stream) and CTME bits are both 1 and CFDC0CTR.CTMS is 0x00.

If this function is used by a transmitting node, a bit error or an arbitration lost will occur.

Do not write to the BFT bit in CH_SLEEP mode. Users should not use this function when the Self test mode 1 (Internal Loop back mode). Only write to this bit when the related CANFD channel is in CH_HALT mode.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

ROM bit (Restricted Operation Mode)

When the ROM and CTME bits are both 1, the restricted operation mode is enabled. This mode should only be used in basic test mode (CFDC0CTR.CTMS[1:0] = 00b).

The ROM bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_HALT mode.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. Do not set this bit when in Classical-only mode.

Note: This bit is not available in the classical CAN function.

28.2.5 CFDC0STS : Channel 0 Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TEC[7:0]								REC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ESIF	COMSTS	RECSTS	TRMSTS	BOSTS	EPSTS	CSLPSTS	CHLTSTS	CRSTSTS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

CTMS[1:0]位（通道测试模式选择）

CTMS[1:0]位用于选择所需的测试模式。

不要在CH_SLEEP或CH_RESET模式下写入这些位。仅当相关CANFD通道处于CH_HALT模式时才写入这些位。

当相关CANFD通道处于CH_RESET模式时，这些位会自动清零。

BFT位（位翻转测试）

BFT位检查协议控制器的内部CRC生成器逻辑。

它将正在接收的CAN报文数据流的第一位（ID位）反转，使得内部生成的CRC结果与接收到的帧的CRC值不匹配。使用此功能时，请参阅位填充规则，因为可能会收到填充错误（由于反转）而不是CRC错误。

内部生成的CRC值始终在以下寄存器中观察：

- CFDC0ERFL.CRCREG (Classical CAN frames)
- CFDC0FDCRC.CRCREG (CANFD frames).*1

注1.此功能在经典CAN功能中不可用。

使用该位时存在一些限制：

其他CAN节点将发送参考消息，并且接收节点可以反转输入比特流的一位。

Note: 发送器和接收器模式共享相同的CRC生成器，因此在测试时无需单独考虑这些模式。

如果BFT（反转位流第一位的新控制信号）和CTME位均为1且CFDC0CTR.CTMS为0x00，则启用位翻转测试模式。

如果发送节点使用此功能，则会发生误码或仲裁丢失。

请勿在CH_SLEEP模式下写入BFT位。自检模式1（内部环回模式）。仅当相关CANFD通道处于CH_HALT模式时才写入该位。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。

ROM位（受限操作模式）

当ROM和CTME位都为1时，限制操作模式被使能。该模式只能用于基本测试模式（CFDC0CTR.CTMS[1:0]=00b）。

在CH_SLEEP模式下不能设置ROM位。仅当相关CANFD通道处于CH_HALT模式时才写入该位。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。不要设置该位时Classical-only mode.

Note: 该位在经典CAN功能中不可用。

28.2.5 CFDC0STS:通道0状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TEC[7:0]								REC[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ESIF	COMSTS	RECSTS	TRMSTS	BOSTS	EPSTS	CSLPSTS	CHLTSTS	CRSTSTS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
0	CRSTSTS	Channel Reset Status 0: Channel not in Reset mode 1: Channel in Reset mode	R
1	CHLTSTS	Channel Halt Status 0: Channel not in Halt mode 1: Channel in Halt mode	R
2	CSLPSTS	Channel Sleep Status 0: Channel not in Sleep mode 1: Channel in Sleep mode	R
3	EPSTS	Channel Error Passive Status 0: Channel not in error passive state 1: Channel in error passive state	R
4	BOSTS	Channel Bus-Off Status 0: Channel not in bus-off state 1: Channel in bus-off state	R
5	TRMSTS	Channel Transmit Status 0: Channel is not transmitting 1: Channel is transmitting	R
6	RECSTS	Channel Receive Status 0: Channel is not receiving 1: Channel is receiving	R
7	COMSTS	Channel Communication Status 0: Channel is not ready for communication 1: Channel is ready for communication	R
8	ESIF*1	Error State Indication Flag 0: No CANFD message has been received when the ESI flag was set 1: At least one CANFD message was received when the ESI flag was set	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
23:16	REC[7:0]	Reception Error Count These bits increment or decrement the counter value according to error status of the CAN channel during reception.	R
31:24	TEC[7:0]	Transmission Error Count These bits increment or decrement the counter value according to error status of the CAN channel during transmission.	R

Note 1. This bit is not available in the classical CAN function.

Channel Status Register shows the mode, error and transmission or reception status of the related channel together with its reception and transmission error count values.

CRSTSTS bit (Channel Reset Status)

The CRSTSTS bit indicates whether the related CAN channel is in Reset mode.

This bit is set automatically when the related CAN channel enters Channel Reset mode. When the mode is changed from Reset mode to Sleep mode, the CRSTSTS bit remains 1.

This bit is cleared automatically when the related CAN channel exits the Channel Reset mode, except when changing to Sleep mode.

CHLTSTS bit (Channel Halt Status)

The CHLTSTS bit indicates whether the related CAN channel is in Halt mode.

This bit is set automatically when the related CAN module enters Halt mode, and is cleared automatically when the related CAN module exits Halt mode.

CSLPSTS bit (Channel Sleep Status)

The CSLPSTS bit indicates whether the related CAN channel is in Sleep mode.

This bit is set automatically when the related CANFD channel enters Sleep mode, and is cleared automatically when the related CANFD channel exits Sleep mode.

Bit	Symbol	Function	R/W
0	CRSTSTS	通道复位状态 0：通道不处于复位模式1：通道处于复位模式	R
1	CHLTSTS	通道暂停状态 0：通道未处于暂停模式1：通道处于暂停模式	R
2	CSLPSTS	通道休眠状态 0：通道不处于休眠模式1：通道处于休眠模式	R
3	EPSTS	通道错误被动状态 0：通道未处于错误被动状态1：通道处于错误被动状态	R
4	BOSTS	通道总线关闭状态 0：通道未处于总线关闭状态1：通道处于总线关闭状态	R
5	TRMSTS	通道传输状态 0：通道未发送1：通道正在发送	R
6	RECSTS	频道接收状态 0：通道未接收1：通道正在接收	R
7	COMSTS	通道通讯状态 0：通道未准备好通讯1：通道准备好通讯	R
8	ESIF*1	错误状态指示标志 0：设置ESI标志时未接收到CANFD消息1：设置ESI标志时至少接收到一条CANFD消息	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
23:16	REC[7:0]	接收错误计数 这些位根据接收期间CAN通道的错误状态递增或递减计数器值。	R
31:24	TEC[7:0]	传输错误计数 这些位在传输过程中根据CAN通道的错误状态递增或递减计数器值。	R

注1.该位在经典CAN功能中不可用。

通道状态寄存器显示相关通道的模式、错误和发送或接收状态及其接收和发送错误计数值。

CRSTSTS位（通道复位状态）

CRSTSTS位指示相关CAN通道是否处于复位模式。

当相关CAN通道进入通道复位模式时，该位自动置位。当模式从将模式复位为休眠模式，CRSTSTS位保持为1。

当相关CAN通道退出通道复位模式时，该位自动清零，除非更改为睡眠模式。

CHLTSTS位（通道暂停状态）

CHLTSTS位指示相关CAN通道是否处于暂停模式。

该位在相关CAN模块进入Halt模式时自动置位，当相关CAN模块进入Halt模式时自动清零CAN模块退出暂停模式。

CSLPSTS位（通道休眠状态）

CSLPSTS位指示相关CAN通道是否处于休眠模式。

该位在相关CANFD通道进入休眠模式时自动置位，并在相关CANFD通道退出休眠模式时自动清零。

EPSTS bit (Channel Error Passive Status)

The EPSTS bit indicates whether the related CANFD channel has entered the error passive state.

This bit is set automatically when the value of the CAN Transmission or Reception Counter Register exceeds the value of 0x7F.

This bit is cleared automatically when the related CANFD channel exits the error passive state or enters Reset mode.

BOSTS bit (Channel Bus-Off Status)

The BOSTS bit indicates whether the related CANFD channel has entered the error bus-off state.

This bit is set automatically when the value of the related CAN Transmission Error Count Register exceeds 0xFF and the related CANFD channel is in the bus-off state (CAN Transmission Error Count Register > 0xFF).

This bit is cleared automatically when the related CANFD channel exits bus-off state.

TRMSTS bit (Channel Transmit Status)

The TRMSTS bit indicates whether the related CANFD channel is transmitting a message.

This bit is set automatically when the related CANFD channel is operating as a transmitter node or is in the bus-off state.

This bit is cleared automatically when the related CANFD channel is in the bus-idle state or starts operating as a receiver node.

RECSTS bit (Channel Receive Status)

The RECSTS bit indicates whether the related CANFD channel is receiving a message.

This bit is set automatically when the related CANFD channel is operating as a receiver node.

This bit is cleared automatically when the related CANFD channel is in the bus-idle state or starts operating as a transmitter node.

COMSTS bit (Channel Communication Status)

The COMSTS bit indicates whether the related CANFD channel is ready for communication.

This bit is set automatically when the related CANFD channel is ready to perform communication following the detection of 11 consecutive recessive bits after exiting the Reset or Halt mode.

This bit is cleared automatically when the related CANFD channel is in CH_RESET or CD_HALT mode.

Note: This bit is 1 during bus-off state.

ESIF bit (Error State Indication Flag)

The ESIF bit is set when the ESI bit is sampled recessively for a reception CAN message without any error. When in Loopback or Mirror mode, the self-transmitted messages are considered reception messages.

If a set from the CANFD channel occurs simultaneously with a clear by a write access, then the bit is set.

This bit is cleared by writing 0 to it. This bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

Note: This bit is not available in the classical CAN function.

REC[7:0] bits (Reception Error Count)

The REC[7:0] bits increment or decrement the counter value according to error status of the CANFD channel during reception, and display the value of the REC error counter.

The value in bus-off state is indeterminate.

These bits are cleared automatically when the CANFD module enters GL_RESET or the CANFD channel is in CH_RESET mode.

EPSTS位（通道错误被动状态）

EPSTS位指示相关CANFD通道是否已进入错误被动状态。

当CAN发送或接收计数器寄存器的值超过0x7F的值时，该位自动置位。

当相关CANFD通道退出错误被动状态或进入复位模式时，该位自动清零。

BOSTS bit (Channel Bus-Off Status)

BOSTS位指示相关CANFD通道是否已进入错误总线关闭状态。

当相关CAN传输错误计数寄存器的值超过0xFF且相关CANFD通道处于总线关闭状态（CAN传输错误计数寄存器>0xFF）时，该位自动置位。

当相关CANFD通道退出总线关闭状态时，该位自动清零。

TRMSTS位（通道发送状态）

TRMSTS位指示相关CANFD通道是否正在发送消息。

当相关CANFD通道作为发送器节点运行或处于总线关闭状态时，该位自动设置。

当相关CANFD通道处于总线空闲状态或开始作为接收节点运行时，该位自动清零。

RECSTS位（通道接收状态）

RECSTS位指示相关CANFD通道是否正在接收消息。

当相关CANFD通道作为接收器节点运行时，该位自动设置。

当相关CANFD通道处于总线空闲状态或开始作为发送器节点运行时，该位自动清零。

COMSTS位（通道通信状态）

COMSTS位指示相关CANFD通道是否已准备好进行通信。

当相关CANFD通道在退出复位或暂停模式后检测到11个连续隐性位后准备好执行通信时，该位自动置位。

当相关CANFD通道处于CH_RESET或CD_HALT模式时，该位自动清零。

Note: 该位在总线关闭状态下为1。

ESIF位（错误状态指示标志）

当ESI位被隐性采样以接收CAN报文且没有任何错误时，设置ESIF位。当在Loopback或Mirror模式下，自发的消息被认为是接收消息。

如果来自CANFD通道的设置与写访问清除同时发生，则该位被设置。

该位通过写入0清零。当相关CANFD通道处于CH_RESET模式时，该位自动清零。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

Note: 该位在经典CAN功能中不可用。

REC[7:0]位（接收错误计数）

REC[7:0]位根据接收时CANFD通道的错误状态递增或递减计数器值，并显示REC错误计数器的值。

总线关闭状态的值是不确定的。

当CANFD模块进入GL_RESET或CANFD通道处于CH_RESET模式时，这些位会自动清除。

TEC[7:0] bits (Transmission Error Count)

The TEC[7:0] bits increment or decrement the counter value according to error status of the CANFD channel during transmission, and display the value of the TEC error counter.

Only write to these bits when in test mode and CANFD channel is in CH_HALT mode.

These bits are cleared automatically when CANFD module is in GL_RESET or CANFD channel is in CH_RESET mode.

28.2.6 CFDC0ERFL : Channel 0 Error Flag Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x000C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	CRCREG[14:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	ADERR	B0ERR	B1ERR	CERR	AERR	FERR	SERR	ALF	BLF	OVLF	BORF	BOEF	EPF	EWF	BEF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BEF	Bus Error Flag 0: Channel bus error not detected 1: Channel bus error detected	R/W
1	EWF	Error Warning Flag 0: Channel error warning not detected 1: Channel error warning detected	R/W
2	EPF	Error Passive Flag 0: Channel error passive not detected 1: Channel error passive detected	R/W
3	BOEF	Bus-Off Entry Flag 0: Channel bus-off entry not detected 1: Channel bus-off entry detected	R/W
4	BORF	Bus-Off Recovery Flag 0: Channel bus-off recovery not detected 1: Channel bus-off recovery detected	R/W
5	OVLF	Overload Flag 0: Channel overload not detected 1: Channel overload detected	R/W
6	BLF	Bus Lock Flag 0: Channel bus lock not detected 1: Channel bus lock detected	R/W
7	ALF	Arbitration Lost Flag 0: Channel arbitration lost not detected 1: Channel arbitration lost detected	R/W
8	SERR	Stuff Error 0: Channel stuff error not detected 1: Channel stuff error detected	R/W
9	FERR	Form Error 0: Channel form error not detected 1: Channel form error detected	R/W
10	AERR	Acknowledge Error 0: Channel acknowledge error not detected 1: Channel acknowledge error detected	R/W

TEC[7:0]位（传输错误计数）

TEC[7:0]位根据CANFD通道在传输过程中的错误状态递增或递减计数器值，并显示TEC错误计数器的值。

仅当处于测试模式且CANFD通道处于CH_HALT模式时写入这些位。

当CANFD模块处于GL_RESET或CANFD通道处于CH_RESET模式时，这些位会自动清除。

28.2.6 CFDC0ERFL:通道0错误标志寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x000C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	CRCREG[14:0]														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	ADERR	B0ERR	B1ERR	CERR	AERR	FERR	SERR	ALF	BLF	OVLF	BORF	BOEF	EPF	EWF	BEF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BEF	总线错误标志 0：未检测到通道总线错误1：检测到通道总线错误	R/W
1	EWF	错误警告标志 0：未检测到通道错误警告1：检测到通道错误警告	R/W
2	EPF	错误被动标志 0：未检测到被动通道错误1：检测到被动通道错误	R/W
3	BOEF	总线关闭进入标志 0：未检测到通道总线关闭条目1：检测到通道总线关闭条目	R/W
4	BORF	总线关闭恢复标志 0：未检测到通道总线关闭恢复1：检测到通道总线关闭恢复	R/W
5	OVLF	过载标志 0：未检测到通道过载1：检测到通道过载	R/W
6	BLF	总线锁标志 0：未检测到通道总线锁定1：检测到通道总线锁定	R/W
7	ALF	仲裁丢失标志 0：未检测到通道仲裁丢失1：检测到通道仲裁丢失	R/W
8	SERR	东西错误 0：未检测到通道填充错误1：检测到通道填充错误	R/W
9	FERR	表格错误 0：未检测到通道形式错误1：检测到通道形式错误	R/W
10	AERR	确认错误 0：未检测到通道确认错误1：检测到通道确认错误	R/W

Bit	Symbol	Function	R/W
11	CERR	CRC Error 0: Channel CRC error not detected 1: Channel CRC error detected	R/W
12	B1ERR	Bit 1 Error 0: Channel bit 1 error not detected 1: Channel bit 1 error detected	R/W
13	B0ERR	Bit 0 Error 0: Channel bit 0 error not detected 1: Channel bit 0 error detected	R/W
14	ADERR	Acknowledge Delimiter Error 0: Channel acknowledge delimiter error not detected 1: Channel acknowledge delimiter error detected	R/W
15	—	This bit is read as 0. The write value should be 0.	R/W
30:16	CRCREG[14:0]	CRC Register value These bits show the CRC value calculated for the CAN2.0 CAN frame.	R
31	—	This bit is read as 0. The write value should be 0.	R/W

Channel Error Flag register shows the status of various error conditions detectable regardless of the setting of the related CAN Channel Error Interrupt Enable Register. It also shows the status of the various bus errors detectable by the CAN channel. Refer to the CAN specification (ISO 11898-1) to check when each error condition occurs.

For this register, only a single bit can be cleared by software. Do not use the bit clear instruction to clear the bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

Example in assembler language to clear the CFDC0ERFL.BEF bit:

mov.b #0x0FE, CFDC0ERFL ;

BEF bit (Bus Error Flag)

The BEF bit indicates a detection of a CAN channel bus error state, flagged by bits [14:8] in this register.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

This bit is set automatically when a bus error is detected, and is cleared automatically when the related CANFD channel is in CH_RESET mode.

If a set from the CAN channel occurs simultaneously with a clear by a write access, then the bit is set.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

EWF bit (Error Warning Flag)

The EWF bit indicates whether an error warning condition has been detected for the CAN channel.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

This bit is set automatically when either TEC or REC exceeds 0x5F.

The setting of this bit only occurs when the TEC or REC initially exceeds 0x5F. Therefore, if the TEC or REC remains > 0x5F and the EWF bit is cleared by software, it is not set again until both the TEC and REC go below 0x60 and either TEC or REC crosses over again from a value 0x5F to a value > 0x5F.

If a set condition occurs simultaneously with a clear condition, then the bit is set. It is cleared automatically when the related CANFD channel is in CH_RESET mode.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

EPF bit (Error Passive Flag)

The EPF bit indicates a detection of a CAN channel error passive state.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

This bit is set automatically when the CAN error state becomes error passive state.

Bit	Symbol	Function	R/W
11	CERR	CRC Error 0：未检测到通道CRC错误1：检测到通道CRC错误	R/W
12	B1ERR	位1错误 0：未检测到通道位1错误1：检测到通道位1错误	R/W
13	B0ERR	位0错误 0：未检测到通道位0错误1：检测到通道位0错误	R/W
14	ADERR	确认分隔符错误 0：未检测到通道确认分隔符错误1：检测到通道确认分隔符错误	R/W
15	—	该位读取为0。写入值应为0。	R/W
30:16	CRCREG[14:0]	CRC寄存器值 这些位显示为CAN2.0CAN帧计算的CRC值。	R
31	—	该位读取为0。写入值应为0。	R/W

通道错误标志寄存器显示可检测到的各种错误条件的状态，无论相关设置如何CAN通道错误中断使能寄存器。它还显示CAN通道可检测到的各种总线错误的状态。请参阅CAN规范(ISO11898-1)以检查每个错误情况何时发生。

对于该寄存器，软件只能清零一个位。不要使用位清除指令来清除位。使用MOV指令确保只清除指定位。其他位保持1。

用汇编语言清除CFDC0ERFL.BEF位的示例：

mov.b #0x0FE, CFDC0ERFL ;

BEF位（总线错误标志）

BEF位指示检测到CAN通道总线错误状态，由该寄存器中的位[14:8]标记。

该位通过写入0清零，并且只能由CANFD模块逻辑设置。写1无效。

该位在检测到总线错误时自动置位，并在相关CANFD通道处于CH_RESET模式时自动清零。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

EWF位（错误警告标志）

EWF位指示是否检测到CAN通道的错误警告条件。

该位通过写入0清零，并且只能由CANFD模块逻辑设置。写1无效。

当TEC或REC超过0x5F时，该位自动置位。

该位的设置仅在TEC或REC最初超过0x5F时发生。因此，如果TEC或REC保持>0x5F并且EWF位由软件清零，则不会再次设置，直到TEC和REC都低于0x60并且TEC或REC再次从值0x5F跨越到值>0x5F.

如果设置条件与清除条件同时出现，则设置该位。相关时自动清除CANFD通道处于CH_RESET模式。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

EPF位（错误被动标志）

EPF位指示检测到CAN通道错误被动状态。

该位通过写入0清零，并且只能由CANFD模块逻辑设置。写1无效。

当CAN错误状态变为错误被动状态时，该位自动设置。

The setting of this bit only occurs when the TEC or REC initially exceeds 0x7F. Therefore, if the TEC or REC remains > 0x7F and the bit is cleared by software, it is not set again until both the TEC and REC go below 0x80 and either TEC or REC crosses over again from a value ≤ 0x7F to a value > 0x7F.

If a set condition occurs simultaneously with a clear condition, then the bit is set. It is cleared automatically when the related CANFD channel is in CH_RESET mode.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

BOEF bit (Bus-Off Entry Flag)

The BOEF bit indicates a detection of a CAN channel bus-off entry state.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

This bit is set automatically when the CAN error state enters the bus-off state.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If a set condition occurs simultaneously with a clear condition, then the bit is set.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

BORF bit (Bus-Off Recovery Flag)

The BORF bit indicates a detection of a CAN channel bus-off recovery state.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

This bit is set automatically if CAN channel recovers from bus-off state in the following conditions:

- When CFDC0CTR.BOM is 00b and normal recovery (11 consecutive recessive bits x 128 times detected) occurs
- When CFDC0CTR.BOM is 10b and normal recovery (11 consecutive recessive bits x 128 times detected) occurs
- When CFDC0CTR.BOM is 11b and normal recovery (11 consecutive recessive bits x 128 times detected) occurs.

The bit is not set if CAN channel recovers from bus-off state in the following conditions:

- When CAN Reset mode is requested
- When CFDC0CTR.RTBO is set to 1 (the CAN channel returns to error active)
- When CFDC0CTR.BOM is 01b
- When CFDC0CTR.BOM is 11b and a halt request is asserted before the CAN channel reaches the end of the bus-off state.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If a set condition occurs simultaneously with a clear condition, the flag is set.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

OVLF bit (Overload Flag)

The OVLF flag indicates a detection of a CAN channel overload state.

The OVLF bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

This bit is set automatically when an overload condition is detected. If a set condition occurs simultaneously with a clear condition, then the bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

Only write to this bit when when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

BLF bit (Bus Lock Flag)

The BLF bit indicates a detection of a CAN channel bus lock condition.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

This bit is set automatically when 32 consecutive dominant bits are detected on the CAN bus while the CAN channel is in Operation mode.

If a set condition occurs simultaneously with a clear condition, then the bit is set. It is cleared automatically when the related CANFD channel is in CH_RESET mode.

该位的设置仅在TEC或REC最初超过0x7F时发生。因此，如果TEC或REC保持>0x7F并且该位由软件清除，则不会再次设置，直到TEC和REC都低于0x80并且TEC或REC再次从值≤0x7F跨越到值>0x7F.

如果设置条件与清除条件同时出现，则设置该位。相关时自动清除
CANFD通道处于CH_RESET模式。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

BOEF位（总线关闭进入标志）

BOEF位指示检测到CAN通道总线关闭进入状态。

该位通过写入0清零，并且只能由CANFD模块逻辑设置。写1无效。

当CAN错误状态进入总线关闭状态时，该位自动置位。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。如果设置条件与清除条件同时出现，则设置该位。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

BORF位（总线关闭恢复标志）

BORF位指示检测到CAN通道总线关闭恢复状态。

该位通过写入0清零，并且只能由CANFD模块逻辑设置。写1无效。

如果CAN通道在以下情况下从总线关闭状态恢复，则该位自动设置：

●CFDC0CTR.BOM为00b且发生正常恢复（11个连续隐性位x128次检测）时

●CFDC0CTR.BOM为10b且发生正常恢复（11个连续隐性位x检测128次）时

●当CFDC0CTR.BOM为11b并且发生正常恢复（11个连续隐性位x检测到128次）时。

如果CAN通道在以下情况下从总线关闭状态恢复，则不会设置该位：

●请求CAN复位模式时

●当CFDC0CTR.RTBO设置为1时（CAN通道返回错误激活）

●当CFDC0CTR.BOM为01b时

●当CFDC0CTR.BOM为11b并且在CAN通道到达总线关闭状态结束之前发出停止请求时。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。如果设置条件与清除条件同时出现，则设置标志。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

OVLF bit (Overload Flag)

OVLF标志指示检测到CAN通道过载状态。

OVLF位通过向其写入0来清除，并且只能由CANFD模块逻辑设置。写1无效。

当检测到过载情况时，该位自动置位。如果设置条件与清除条件同时出现，则设置该位。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

BLF位（总线锁定标志）

BLF位指示检测到CAN通道总线锁定条件。

该位通过写入0清零，并且只能由CANFD模块逻辑设置。写1无效。

当CAN通道在CAN总线上检测到32个连续显性位时，该位自动设置操作模式。

如果设置条件与清除条件同时出现，则设置该位。相关时自动清除
CANFD通道处于CH_RESET模式。

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

It is cleared automatically when the related CANFD channel is in CH_RESET mode.

ALF bit (Arbitration Lost Flag)

The ALF bit indicates a detection of a CAN channel bus arbitration lost condition.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

The bit is set automatically when an arbitration lost condition is detected on the CAN bus while the CAN channel is in Operation mode.

If a set condition occurs simultaneously with a clear condition, then the bit is set. It is cleared automatically when the related CANFD channel is in CH_RESET mode.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

SERR bit (Stuff Error)

The SERR bit indicates a detection of a CAN stuff error.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a stuff error is detected. If CFDC0CTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If CFDC0CTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDC0ERFL[14:8] is already set. Otherwise, this bit is set if CFDC0ERFL[14:8] is 0000000b.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

FERR bit (Form Error)

The FERR bit indicates a detection of a CAN form error.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a form error is detected. If CFDC0CTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If CFDC0CTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDC0ERFL[14:8] is already set. Otherwise, this bit is set if CFDC0ERFL[14:8] is 0000000b.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

AERR bit (Acknowledge Error)

The AERR bit indicates a detection of a CAN acknowledge error.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

当相关CANFD通道处于CH_RESET模式时自动清零。

ALF位（仲裁丢失标志）

ALF位指示检测到CAN通道总线仲裁丢失情况。

该位通过写入0清零，并且只能由CANFD模块逻辑设置。写1无效。

当CAN通道在CAN总线上检测到仲裁丢失条件时，该位自动设置
操作模式。

如果设置条件与清除条件同时出现，则设置该位。相关时自动清除
CANFD通道处于CH_RESET模式。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

SERR bit (Stuff Error)

SERR位指示检测到CAN填充错误。

该位通过写入0清零，并且只能由CANFD模块逻辑设置。写1无效。

要清除该位，请使用以下序列：

1.清除对应的标志位。

2.读取标志位是否被清除。

3.如果是，继续，否则返回步骤1。

当检测到填充错误时，该位自动设置。如果CFDC0CTR.ERRD位为1，并且该位的置位和清零条件同时发生，则该位被置位。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。如果CFDC0CTR.ERRD位为0并且该位的置位和清零条件同时发生，则如果CFDC0ERFL[14:8]的位已置位，则清零。否则，如果CFDC0ERFL[14:8]为0000000b，则设置该位。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

FERR bit (Form Error)

FERR位指示检测到CAN格式错误。

该位通过写入0清零，并且只能由CANFD模块逻辑设置。写1无效。

要清除该位，请使用以下序列：

1.清除对应的标志位。

2.读取标志位是否被清除。

3.如果是，继续，否则返回步骤1。

当检测到表格错误时，该位自动置位。如果CFDC0CTR.ERRD位为1，并且该位的置位和清零条件同时发生，则该位被置位。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。如果CFDC0CTR.ERRD位为0并且该位的置位和清零条件同时发生，则如果CFDC0ERFL[14:8]的位已置位，则清零。否则，如果CFDC0ERFL[14:8]为0000000b，则设置该位。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

AERR bit (Acknowledge Error)

AERR位指示检测到CAN确认错误。

该位通过写入0清零，并且只能由CANFD模块逻辑设置。写1无效。

要清除该位，请使用以下序列：

1.清除对应的标志位。

2.读取标志位是否被清除。

3.如果是，继续，否则返回步骤1。

This bit is set automatically when an acknowledge error is detected. If CFDC0CTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If CFDC0CTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDC0ERFL[14:8] is already set. Otherwise, this bit is set if CFDC0ERFL[14:8] is 0000000b.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION.

CERR bit (CRC Error)

The CERR bit indicates a detection of a CAN CRC error.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a CRC error is detected. If CFDC0CTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If CFDC0CTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDC0ERFL[14:8] is already set. Otherwise, this bit is set if CFDC0ERFL[14:8] is 0000000b.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

B1ERR bit (Bit 1 Error)

The B1ERR bit indicates a detection of a recessive bit error.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a recessive bit error (expected recessive bit, sampled as dominant bit) is detected. If CFDC0CTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If CFDC0CTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDC0ERFL[14:8] is already set. Otherwise, this bit is set if CFDC0ERFL[14:8] is 0000000b.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

B0ERR bit (Bit 0 Error)

The B0ERR bit indicates a detection of a dominant bit error.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a dominant bit error (expected dominant bit, sampled as recessive bit) is detected. If CFDC0CTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If CFDC0CTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDC0ERFL[14:8] is already set. Otherwise, this bit is set if CFDC0ERFL[14:8] is 0000000b.

当检测到确认错误时，该位自动置位。如果CFDC0CTR.ERRD位为1，并且该位的置位和清零条件同时发生，则该位被置位。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。如果CFDC0CTR.ERRD位为0并且该位的置位和清零条件同时发生，则如果CFDC0ERFL[14:8]的位已置位，则清零。否则，如果CFDC0ERFL[14:8]为0000000b，则设置该位。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION时才写入该位。

CERR bit (CRC Error)

CERR位指示检测到CANCRC错误。

该位通过写入0清零，并且只能由CANFD模块逻辑设置。写1无效。

要清除该位，请使用以下序列：

1.清除对应的标志位。

2.读取标志位是否被清除。

3.如果是，继续，否则返回步骤1。

当检测到CRC错误时，该位自动置位。如果CFDC0CTR.ERRD位为1，并且该位的置位和清零条件同时发生，则该位被置位。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。如果CFDC0CTR.ERRD位为0并且该位的置位和清零条件同时发生，则如果CFDC0ERFL[14:8]的位已置位，则清零。否则，如果CFDC0ERFL[14:8]为0000000b，则设置该位。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

B1ERR bit (Bit 1 Error)

B1ERR位指示检测到隐性位错误。

该位通过写入0清零，并且只能由CANFD模块逻辑设置。写1无效。

要清除该位，请使用以下序列：

1.清除对应的标志位。

2.读取标志位是否被清除。

3.如果是，继续，否则返回步骤1。

当检测到隐性位错误（预期的隐性位，采样为显性位）时，该位自动置位。如果CFDC0CTR.ERRD位为1，如果该位的设置和清除条件同时发生，则该位被设置。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。如果CFDC0CTR.ERRD位为0并且该位的置位和清零条件同时发生，则如果CFDC0ERFL[14:8]的位已置位，则清零。否则，如果CFDC0ERFL[14:8]为0000000b，则设置该位。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

B0ERR bit (Bit 0 Error)

B0ERR位指示检测到显性位错误。

该位通过写入0清零，并且只能由CANFD模块逻辑设置。写1无效。

要清除该位，请使用以下序列：

1.清除对应的标志位。

2.读取标志位是否被清除。

3.如果是，继续，否则返回步骤1。

当检测到显性位错误（预期显性位，采样为隐性位）时，该位自动置位。如果CFDC0CTR.ERRD位为1，如果该位的设置和清除条件同时发生，则该位被设置。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。如果CFDC0CTR.ERRD位为0并且该位的置位和清零条件同时发生，则如果CFDC0ERFL[14:8]的位已置位，则清零。否则，如果CFDC0ERFL[14:8]为0000000b，则设置该位。

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

ADERR bit (Acknowledge Delimiter Error)

The ADERR bit indicates a detection of an acknowledge delimiter bit error.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a form error is detected during the acknowledge delimiter state of frame transmission. If CFDC0CTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If CFDC0CTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDC0ERFL[14:8] is already set. Otherwise, this bit is set if CFDC0ERFL[14:8] is 0000000b.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

CRCREG[14:0] bits (CRC Register value)

The CRCREG[14:0] bits read the calculated CRC value when CFDC0CTR.CTME bit is 1 for the channel.

If CFDC0CTR.CTME bit is 0, then these bits are always read as 0.

These bits show the CAN2.0 CRC value calculated by the CANFD channel logic when the CTME bit is enabled.

The CFDC0ERFL.CRCREG value is updated in the first bit of the CRC field of the CAN frame (reception and transmission).

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

28.2.7 CFDC0DCFG : Channel 0 Data Bitrate Configuration Register

This register is not available in the classical CAN function.

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	DSJW[3:0]				—	—	—	—	DTSEG2[3:0]				—	—	—	DTSEG1[4:0]					DBRP[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DBRP[7:0]	Channel Data Baud Rate Prescaler Data Baud Rate Prescaler division ratio	R/W
12:8	DTSEG1[4:0]	Timing Segment 1 0x00: Reserved 0x01: 2 Tq 0x02: 3 Tq 0x03: 4 Tq ⋮ 0x1E: 31 Tq 0x1F: 32 Tq	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

ADERR bit (Acknowledge Delimiter Error)

ADERR位指示检测到确认分隔符位错误。

该位通过写入0清零，并且只能由CANFD模块逻辑设置。写1无效。

要清除该位，请使用以下序列：

1.清除对应的标志位。

2.读取标志位是否被清除。

3.如果是，继续，否则返回步骤1。

当在帧传输的确认分隔符状态期间检测到格式错误时，该位自动设置。如果CFDC0CTR.ERRD位为1，如果该位的设置和清除条件同时发生，则该位被设置。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。如果CFDC0CTR.ERRD位为0并且该位的置位和清零条件同时发生，则如果CFDC0ERFL[14:8]的位已置位，则清零。否则，如果CFDC0ERFL[14:8]为0000000b，则设置该位。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

CRCREG[14:0]位（CRC寄存器值）

当通道的CFDC0CTR.CTME位为1时，CRCREG[14:0]位读取计算的CRC值。

如果CFDC0CTR.CTME位为0，则这些位始终读为0。

这些位显示CTME位使能时CANFD通道逻辑计算的CAN2.0CRC值。

CFDC0ERFL.CRCREG值在CAN帧（接收和发送）的CRC字段的第一位更新。

当相关CANFD通道处于CH_RESET模式时，这些位会自动清零。

28.2.7 CFDC0DCFG：通道0数据比特率配置寄存器

该寄存器在经典CAN功能中不可用。

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	DSJW[3:0]				—	—	—	—	DTSEG2[3:0]				—	—	—	DTSEG1[4:0]					DBRP[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DBRP[7:0]	通道数据波特率预分频器 数据波特率预分频比	R/W
12:8	DTSEG1[4:0]	时序段1 0x00: Reserved 0x01: 2 Tq 0x02: 3 Tq 0x03: 4 Tq ⋮ 0x1E: 31 Tq 0x1F: 32 Tq	R/W
15:13	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
19:16	DTSEG2[3:0]	Timing Segment 2 0x0: Reserved 0x1: 2 Tq ⋮ 0xE: 15 Tq 0xF: 16 Tq	R/W
23:20	—	These bits are read as 0. The write value should be 0.	R/W
27:24	DSJW[3:0]	Resynchronization Jump Width 0x0: 1 Tq 0x1: 2 Tq ⋮ 0xF: 16 Tq	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

Note: Tq means time quantum.

The Channel 0 Data Bitrate Configuration Register configures the transmission/reception data baud rate parameters of the channels.

The channel of Classical-only mode does not perform configuration of this register.

DBRP[7:0] bits (Channel Data Baud Rate Prescaler)

The DBRP[7:0] bits define the peripheral bus clock periods contained in a time quantum.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

DTSEG1[4:0] bits (Timing Segment 1)

The DTSEG1[4:0] bits set the segment TSEG1 to compensate for edges on the CAN bus with a positive phase error. A value from 2 to 32 time quanta can be set.

The DTSEG1[4:0] bits are also used to set the propagation segment.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode. Do not write any other value to these bits. See section 28.4.1.2. CAN Bit Timing for more details.

DTSEG2[3:0] bits (Timing Segment 2)

The DTSEG2[3:0] bits set the segment TSEG2 to compensate for edges on the CAN bus with a negative phase error. A value from 2 to 16 time quanta can be set.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode. Do not write any other value to these bits.

DSJW[3:0] bits (Resynchronization Jump Width)

The DSJW[3:0] bits set the synchronization jump width. A value from 1 to 16 time quanta can be set.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

28.2.8 CFDC0FDCFG : Channel 0 CANFD Configuration Register

This register is not available in the classical CAN function.

Bit	Symbol	Function	R/W
19:16	DTSEG2[3:0]	计时段2 0x0: Reserved 0x1: 2 Tq ⋮ 0xE: 15 Tq 0xF: 16 Tq	R/W
23:20	—	这些位被读取为0。写入值应为0。	R/W
27:24	DSJW[3:0]	再同步跳转宽度 0x0: 1 Tq 0x1: 2 Tq ⋮ 0xF: 16 Tq	R/W
31:28	—	这些位被读取为0。写入值应为0。	R/W

Note: Tq表示时间量。

通道0数据比特率配置寄存器配置通道的发送接收数据波特率参数。

Classical-only模式的通道不执行该寄存器的配置。

DBRP[7:0]位（通道数据波特率预分频器）

DBRP[7:0]位定义包含在时间片中的外围总线时钟周期。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。

DTSEG1[4:0]位（时序段1）

DTSEG1[4:0]位设置段TSEG1以补偿CAN总线上的正相位误差边沿。可以设置2到32个时间量的值。

DTSEG1[4:0]位也用于设置传播段。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。不要将任何其他值写入这些位。请参阅第28.4.1.2节。CAN位时序了解更多详情。

DTSEG2[3:0]位（时序段2）

DTSEG2[3:0]位设置段TSEG2以补偿CAN总线上具有负相位误差的边沿。可以设置2到16个时间量子的值。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。不要将任何其他值写入这些位。

DSJW[3:0]位（再同步跳转宽度）

DSJW[3:0]位设置同步跳转宽度。可以设置1到16个时间量的值。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。

28.2.8 CFDC0FDCFG：通道0CANFD配置寄存器

该寄存器在经典CAN功能中不可用。

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0104

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	CLOE	REFE	FDOE	—	—	—	—	TDCO[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	ESIC	TDCE	TDCOC	—	—	—	—	—	EOCCFG[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	EOCCFG[2:0]	Error Occurrence Counter Configuration 0 0 0: All transmitter or receiver CAN frames 0 0 1: All transmitter CAN frames 0 1 0: All receiver CAN frames 0 1 1: Reserved 1 0 0: Only transmitter or receiver CANFD data-phase (fast bits) 1 0 1: Only transmitter CANFD data-phase (fast bits) 1 1 0: Only receiver CANFD data-phase (fast bits) 1 1 1: Reserved	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
8	TDCOC*1	Transceiver Delay Compensation Offset Configuration 0: Measured + offset 1: Offset-only	R/W
9	TDCE*1	Transceiver Delay Compensation Enable 0: Transceiver delay compensation disabled 1: Transceiver delay compensation enabled	R/W
10	ESIC*1	Error State Indication Configuration 0: The ESI bit in the frame represents the error state of the node itself 1: The ESI bit in the frame represents the error state of the message buffer if the node itself is not in error passive. If the node is in error passive, then the ESI bit is driven by the node itself.	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
23:16	TDCO[7:0]*1	Transceiver Delay Compensation Offset	R/W
27:24	—	These bits are read as 0. The write value should be 0.	R/W
28	FDOE*1	FD-Only Enable 0: FD-only mode disabled 1: FD-only mode enabled	R/W
29	REFE	RX Edge Filter Enable 0: RX edge filter disabled 1: RX edge filter enabled	R/W
30	CLOE*1	Classical CAN-Only Enable 0: Classical-only mode disabled 1: Classical-only mode enabled	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. These bits are not available in the classical CAN function.

The Channel 0 CANFD Configuration Register configures which communication direction (transmitter/receiver) errors are counted.

EOCCFG[2:0] bits (Error Occurrence Counter Configuration)

The EOCCFG[2:0] bits select which type of CAN frame configuration and direction, including protocol errors are counted.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0104

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	CLOE	REFE	FDOE	—	—	—	—	TDCO[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	ESIC	TDCE	TDCOC	—	—	—	—	—	EOCCFG[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	EOCCFG[2:0]	错误发生计数器配置 000：所有发送器或接收器CAN帧001：所有发送器CAN帧010：所有接收器CAN帧011：保留100：仅发送器或接收器CANFD数据阶段（快速位）101：仅发送器CANFD数据阶段（快速位）110：仅接收器CANFD数据阶段（快速位）111：保留	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
8	TDCOC*1	收发器延迟补偿偏移配置 0：测量+偏移1：仅偏移	R/W
9	TDCE*1	收发器延迟补偿使能 0：收发器延迟补偿禁用1：收发器延迟补偿启用	R/W
10	ESIC*1	错误状态指示配置 0：帧中的ESI位表示节点本身的错误状态1：帧中的ESI位表示消息缓冲区的错误状态，如果 节点本身没有错误被动。如果节点处于被动错误，则ESI位由节点本身驱动。	R/W
11	—	该位读取为0。写入值应为0。	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W
23:16	TDCO[7:0]*1	收发器延迟补偿偏移	R/W
27:24	—	这些位被读取为0。写入值应为0。	R/W
28	FDOE*1	FD-Only Enable 0：FD-only模式禁用1：FD-only模式启用	R/W
29	REFE	RX边缘滤波器启用 0：RX边缘过滤器禁用1：RX边缘过滤器启用	R/W
30	CLOE*1	经典CAN-Only启用 0：仅经典模式禁用1：仅经典模式启用	R/W
31	—	该位读取为0。写入值应为0。	R/W

注1.这些位在经典CAN功能中不可用。

通道0CANFD配置寄存器配置计算哪个通信方向（发送器接收器）错误。

EOCCFG[2:0]位（错误发生计数器配置）

EOCCFG[2:0]位选择计算哪种类型的CAN帧配置和方向，包括协议错误。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

TDCOC bit (Transceiver Delay Compensation Offset Configuration)*1

The TDCOC bit selects which offset is used when defining the position of the secondary sample point (SSP) for the CANFD channel. If the bit is set to 0, the position of the SSP is the measured transceiver delay plus the fixed offset. If the bit is 1, the position of the SSP is defined only by the offset.

Do not write to this bit in CH_OPERATION or CH_SLEEP mode.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode. Do not set this bit when in Classical-only mode.

TDCE bit (Transceiver Delay Compensation Enable)*1

The TDCE bit enables the transceiver delay compensation for the CANFD channel.

Do not write to this bit in CH_OPERATION or CH_SLEEP mode.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode. Do not set this bit when in Classical-only mode.

ESIC bit (Error State Indication Configuration)*1

The ESIC bit controls the transmission of either the ESI flag information or the message of ESI flag information (CFDCFFDCSTS.CFESI or CFDTMFDCTRb.TMESI).

Do not write to this bit in CH_OPERATION or CH_SLEEP mode.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode. Do not set this bit when in Classical-only mode.

TDCO[7:0] bits (Transceiver Delay Compensation Offset)*1

The TDCO[7:0] bits set the secondary sample point offset. How this value is used, depends on the CFDC0FDCFG.TDCOC setting.

If CFDC0FDCFG.TDCOC = 0, the transceiver delay compensation result is equal to the Trv_Delay (measured delay) + the value in CFDC0FDCFG.TDCO, rounded down to the nearest integer number of time quanta. Otherwise, the result is equal to the value in CFDC0FDCFG.TDCO. See section 28.4.1.5. Transmitter Delay Compensation for details on how CFDC0FDCFG.TDCO is used.

The actual offset value is interpreted as TDCO + 1. For example, if 4 is set in TDCO, the offset is 5 clock cycles. Clock cycle is 1 cycle of CAN channel DLL clock.

Do not write to the TDCO[7:0] bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode. Do not set to this bit when in Classical-only mode.

FDOE bit (FD-Only Enable)*1

The FDOE bit enables the reception and transmission of CANFD-only frames. If enabled, communication in Classical CAN frame format is disabled. Transmission of Classical CAN frames is not possible because the FDF bit of the message buffer is a don't care (CFDCFFDCSTS.CFFDF/CFDTMFDCTRb.TMFDF).

If messages with Classical CAN frame format are received, the protocol controller treats them as invalid frames and response with error frames. When a Classical CAN frame is configured for transmitting, the FDF bit is sent as recessive, therefore an FD frame is sent. If the data length code (DLC) is configured of greater than 8 bytes, the remaining data bytes are padded with 0xCC.

The FDOE bit cannot be written in CH_OPERATION, CH_HALT or CH_SLEEP mode.

Do not set CFDC0FDCFG.FDOE and CFDC0FDCFG.CLOE simultaneously.

REFE bit (RX Edge Filter Enable)

The REFE bit enables the RX edge filter during the IDLE detection (bus integration). When the bit is enabled, two consecutive dominant time quanta are required to detect a synchronization edge.

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。

TDCOC位（收发器延迟补偿偏移配置）*1

TDCOC位选择在定义辅助采样点(SSP)的位置时使用哪个偏移量
CANFD通道。如果该位设置为0，则SSP的位置是测量的收发器延迟加上固定偏移。如果该位为1，则SSP的位置仅由偏移量定义。

请勿在CH_OPERATION或CH_SLEEP模式下写入该位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入该位。不要设置该位时
Classical-only mode.

TDCE位（收发器延迟补偿启用）*1

TDCE位使能CANFD通道的收发器延迟补偿。

请勿在CH_OPERATION或CH_SLEEP模式下写入该位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入该位。不要设置该位时
Classical-only mode.

ESIC位（错误状态指示配置）*1

ESIC位控制ESI标志信息或ESI标志信息消息（CFDCFFDCSTS.CFESI或CFDTMFDCTRb.TMESI）的传输。

请勿在CH_OPERATION或CH_SLEEP模式下写入该位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入该位。不要设置该位时
Classical-only mode.

TDCO[7:0]位（收发器延迟补偿偏移）*1

TDCO[7:0]位设置辅助采样点偏移。该值的使用方式取决于CFDC0FDCFG.TDCOC设置。

如果CFDC0FDCFG.TDCOC=0，则收发器延迟补偿结果等于Trv_Delay（测量延迟）+CFDC0FDCFG.TDCO中的值，向下舍入到最接近的时间量子整数。否则，结果等于CFDC0FDCFG.TDCO中的值。请参阅第28.4.1.5节。发送器延迟补偿，了解如何使用CFDC0FDCFG.TDCO的详细信息。

实际偏移值被解释为TDCO+1。例如，如果TDCO设置为4，则偏移为5个时钟周期。时钟周期为CAN通道DLL时钟的1个周期。

请勿在CH_OPERATION或CH_SLEEP模式下写入TDCO[7:0]位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。在仅经典模式下不要设置此位。

FDOE bit (FD-Only Enable)*1

FDOE位使能CANFD-only帧的接收和发送。如果启用，则会禁用经典CAN帧格式的通信。传统CAN帧的传输是不可能的，因为消息缓冲区的FDF位是无关紧要的(CFDCFFDCSTS.CFFDFCFDTMFDCTRb.TMFDF)。

如果接收到具有经典CAN帧格式的消息，协议控制器会将其视为无效帧并以错误帧响应。当经典CAN帧配置为发送时，FDF位作为隐性发送，因此发送FD帧。如果数据长度代码(DLC)配置为大于8个字节，则剩余的数据字节用0xCC填充。

FDOE位不能在CH_OPERATION、CH_HALT或CH_SLEEP模式下写入。

不要同时设置CFDC0FDCFG.FDOE和CFDC0FDCFG.CLOE。

REFE位（RX边沿过滤器使能）

在空闲检测（总线集成）期间，REFE位使能RX边沿滤波器。当该位使能时，需要两个连续的显性时间量来检测同步边沿。

The REFE bit cannot be written in CH_OPERATION, CH_HALT and CH_SLEEP mode. Do not set this bit when in Classical-only mode.

CLOE bit (Classical CAN-Only Enable)*1

The CLOE bit enables the Classical CAN-only mode. If this bit is 1, the protocol controller can only send classical frames and response with a form or CRC error on FD frames.

Do not set CFDC0FDCFG.CLOE and CFDC0FDCFG.FDOE simultaneously.

CFDC0FDCFG.CLOE	CFDC0FDCFG.FDOE	Channel mode
0	0	CANFD mode
0	1	FD-only mode
1	0	Classical CAN-only mode
1	1	Reserved

The CANFD mode is available only for CANFD supported product.

Do not write to this bit in CH_OPERATION, CH_HALT or CH_SLEEP mode.

Only write to these bits when the CANFD channel is in CH_RESET mode.

Note 1. These bits are not available in the classical CAN function.

28.2.9 CFDC0FDCTR : Channel 0 CANFD Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0108

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOCCLR	EOCCLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EOCCLR	Error Occurrence Counter Clear 0: No error occurrence counter clear 1: Clear error occurrence counter	R/W
1	SOCCLR	Successful Occurrence Counter Clear 0: No successful occurrence counter clear 1: Clear successful occurrence counter	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

The Channel n CANFD Control Register (n = 0) controls the error and successful occurrence counters.

EOCCLR bit (Error Occurrence Counter Clear)

The EOCCLR bit is used to clear the error occurrence counter.

Do not write to this bit in CH_SLEEP or CH_RESET mode. The read value is always 0.

This bit is cleared automatically by the CANFD module logic and when the related CANFD channel is in CH_RESET mode.

SOCCLR bit (Successful Occurrence Counter Clear)

The SOCCLR bit is used to clear the successful occurrence counter.

在CH_OPERATION、CH_HALT和CH_SLEEP模式下不能写入REFE位。不要设置该位时
Classical-only mode.

CLOE bit (Classical CAN-Only Enable)*1

CLOE位启用经典CAN-only模式。如果该位为1，则协议控制器只能发送经典帧并在FD帧上带有格式或CRC错误的响应。

不要同时设置CFDC0FDCFG.CLOE和CFDC0FDCFG.FDOE。

CFDC0FDCFG.CLOE	CFDC0FDCFG.FDOE	频道模式
0	0	CANFD mode
0	1	FD-only mode
1	0	经典CAN-only模式
1	1	Reserved

CANFD模式仅适用于支持CANFD的产品。

请勿在CH_OPERATION、CH_HALT或CH_SLEEP模式下写入该位。

仅当CANFD通道处于CH_RESET模式时才写入这些位。

注1.这些位在经典CAN功能中不可用。

28.2.9 CFDC0FDCTR:通道0CANFD控制寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0108

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOCCLR	EOCCLR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EOCCLR	错误发生计数器清除 0：不清除错误发生计数器1：清除错误发生计数器	R/W
1	SOCCLR	成功发生计数器清除 0：无成功发生计数器清零1：清零成功发生计数器	R/W
31:2	—	这些位被读取为0。写入值应为0。	R/W

通道nCANFD控制寄存器(n=0)控制错误和成功发生计数器。

EOCCLR位（错误发生计数器清除）

EOCCLR位用于清除错误发生计数器。

请勿在CH_SLEEP或CH_RESET模式下写入该位。读取值始终为0。

当相关CANFD通道处于CH_RESET模式时，该位由CANFD模块逻辑自动清零。

SOCCLR位（成功发生计数器清零）

SOCCLR位用于清除成功发生计数器。

Do not write to this bit in CH_SLEEP or CH_RESET mode. The read value is always 0.

This bit is cleared automatically by the CANFD module logic and when the related CANFD channel is in CH_RESET mode.

28.2.10 CFDC0FDSTS : Channel 0 CANFD Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x010C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SOC[7:0]								EOC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TDCVF	—	—	—	—	—	SOCO	EOCO	TDCR[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TDCR[7:0]*1	Transceiver Delay Compensation Result	R
8	EOCO	Error Occurrence Counter Overflow 0: Error occurrence counter has not overflowed 1: Error occurrence counter has overflowed	R/W
9	SOCO	Successful Occurrence Counter Overflow 0: Successful occurrence counter has not overflowed 1: Successful occurrence counter has overflowed	R/W
14:10	—	These bits are read as 0. The write value should be 0.	R/W
15	TDCVF*1	Transceiver Delay Compensation Violation Flag 0: Transceiver delay compensation violation has not occurred 1: Transceiver delay compensation violation has occurred	R/W
23:16	EOC[7:0]	Error Occurrence Counter These bits show the error occurrence counter value.	R
31:24	SOC[7:0]	Successful occurrence counter These bits show the successful occurrence counter value.	R

Note 1. These bits are not available in the classical CAN function.

The Channel 0 CANFD Status Register indicates the transceiver compensation delay result and its related FIFO message lost status.

TDCR[7:0] bits (Transceiver Delay Compensation Result)

The TDCR[7:0] bits are set when the transceiver delay has been measured.

The measured delay is a multiple of the CAN channel DLL clock. The result depends on the CFDC0FDCFG.TDCOC configuration and the offset value in CFDC0FDCFG.TDCO. See section 28.4.1.5. Transmitter Delay Compensation for details on how this value is derived.

The TDCR[7:0] bits are updated at the falling edge between FDF and the RES bit when CFDC0FDCFG.TDCOC = 0 and the transceiver delay compensation is enabled (CFDC0FDCFG.TDCE = 1).

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

Note: These bits are not available in the classical CAN function.

EOCO bit (Error Occurrence Counter Overflow)

The EOCO bit indicates whether the related CAN channel error occurrence counter has overflowed. This bit is cleared by writing 0 to it. Writing 1 has no effect.

请勿在CH_SLEEP或CH_RESET模式下写入该位。读取值始终为0。

当相关CANFD通道处于CH_RESET模式时，该位由CANFD模块逻辑自动清零。

28.2.10 CFDC0FDSTS:通道0CANFD状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x010C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SOC[7:0]								EOC[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TDCVF	—	—	—	—	—	SOCO	EOCO	TDCR[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TDCR[7:0]*1	收发器延迟补偿结果	R
8	EOCO	错误发生计数器溢出 0：错误发生计数器未溢出1：错误发生计数器已溢出	R/W
9	SOCO	成功发生计数器溢出 0：成功发生计数器未溢出1：成功发生计数器已溢出	R/W
14:10	—	这些位被读取为0。写入值应为0。	R/W
15	TDCVF*1	收发器延迟补偿违规标志 0：未发生收发器延迟补偿违规1：已发生收发器延迟补偿违规	R/W
23:16	EOC[7:0]	错误发生计数器 这些位显示错误发生计数器的值。	R
31:24	SOC[7:0]	成功发生计数器 这些位显示成功发生计数器的值。	R

注1.这些位在经典CAN功能中不可用。

通道0CANFD状态寄存器指示收发器补偿延迟结果及其相关的FIFO消息丢失状态。

TDCR[7:0]位（收发器延迟补偿结果）

TDCR[7:0]位在测量到收发器延迟后置位。

测得的延迟是CAN通道DLL时钟的倍数。结果取决于CFDC0FDCFG.TDCOC配置和CFDC0FDCFG.TDCO中的偏移值。请参阅第28.4.1.5节。TransmitterDelayCompensation了解有关如何得出此值的详细信息。

当CFDC0FDCFG.TDCOC=0并且使能收发器延迟补偿(CFDC0FDCFG.TDCE=1)时，TDCR[7:0]位在FDF和RES位之间的下降沿更新。

当相关CANFD通道处于CH_RESET模式时，这些位会自动清零。

Note: 这些位在经典CAN功能中不可用。

EOCO位（错误发生计数器溢出）

EOCO位指示相关的CAN通道错误发生计数器是否溢出。该位通过写入0清零。写1无效。

This bit is set automatically when CFDC0FDSTS.EOC is 0xFF and a CAN bus error is detected based on the configuration defined in CFDC0FDCFG.EOCCFG.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

SOCO bit (Successful Occurrence Counter Overflow)

The SOCO bit indicates whether the related CAN channel successful occurrence counter has overflowed. This bit is cleared by writing 0 to it. Writing 1 has no effect.

This bit is set automatically when CFDC0FDSTS.SOC is 0xFF and a successful message reception or successful message transmission occurs.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

Write to this bit only when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

TDCVF bit (Transceiver Delay Compensation Violation Flag)

The CANFD module captures internally the transmitted data bit-by-bit. This data is then compared against the received CAN bus level which is delayed by the transceiver loop delay.

The transceiver delay has some variations depending on the physical parameters such as temperature. The result bit CFDC0FDSTS.TDCR is updated by each message. However, temporary maximum delay violation could be missed. Therefore, the TDCVF bit captures this violation.

This bit is cleared by writing 0 to it. Writing 1 has no effect.

This bit is set automatically when the transceiver delay compensation is greater than the maximum delay compensation (6 data bit times - 2 clk_dlc) and the internal bit is overrun.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

Note: This bit is not available in the classical CAN function.

EOC[7:0] bits (Error Occurrence Counter)

The EOC[7:0] bits are used together with the SOC[7:0] bits to support an option for host-controlled fall-back to payload bit rate identical to arbitration bit rate when messages utilizing the reduced payload bit length have significant higher error rates compared to other messages.

This higher error rate can be detected depending on the configuration of the CFDC0FDCFG.EOCCFG bits.

The EOC[7:0] bits are set only by CANFD module logic. These bits are cleared by writing 1 to CFDC0FDCTR.EOCCLR. Writing any other value has no effect.

These bits are updated when an error occurs, according to the configuration of the CFDC0FDCFG.EOCCFG bits. When the counter reaches the value of 0xFF, the update stops.

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

当CFDC0FDSTS.EOC为0xFF并且根据CFDC0FDCFG.EOCCFG中定义的配置检测到CAN总线错误时，该位自动设置。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

SOCO位（成功发生计数器溢出）

SOCO位指示相关CAN通道成功发生计数器是否溢出。该位通过写入0清零。写1无效。

当CFDC0FDSTS.SOC为0xFF并且成功接收消息或成功发送消息时，该位自动置位。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

TDCVF位（收发器延迟补偿违规标志）

CANFD模块在内部逐位捕获传输的数据。然后将该数据与接收到的数据进行比较
由收发器环路延迟延迟的CAN总线电平。

收发器延迟有一些变化，具体取决于温度等物理参数。结果位CFDC0FDSTS.TDCR由每个消息更新。但是，可能会错过临时最大延迟违规。
因此，TDCVF位捕获此违规。

该位通过写入0清零。写1无效。

当收发器延迟补偿大于最大延迟补偿（6个数据位乘以2个clk_dlc）并且内部位溢出时，该位自动置位。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

Note: 该位在经典CAN功能中不可用。

EOC[7:0]位（错误发生计数器）

EOC[7:0]位与SOC[7:0]位一起使用，以支持主机控制的回退到与仲裁比特率相同的有效负载比特率选项，当使用减少的有效负载位长度的消息具有显着性时与其他消息相比，错误率更高。

根据CFDC0FDCFG.EOCCFG位的配置，可以检测到这种较高的错误率。

EOC[7:0]位仅由CANFD模块逻辑设置。这些位通过向CFDC0FDCTR.EOCCLR写入1来清除。
写入任何其他值均无效。

根据CFDC0FDCFG.EOCCFG位的配置，这些位在发生错误时更新。当计数器达到0xFF的值时，更新停止。

当相关CANFD通道处于CH_RESET模式时，这些位会自动清零。

SOC[7:0] bits (Successful occurrence counter)

The SOC[7:0] bits are used together with the EOC[7:0] bits to support an option for host-controlled fall-back to payload bit rate identical to arbitration bit rate when messages utilizing the reduced payload bit length have significant higher error rates compared to other messages.

The SOC[7:0] bits are set only by CANFD module logic. Writing any other value has no effect.

These bits are updated when the occurrence of any error-free messages on the bus is detected through reception or transmission. When the counter reaches the value of 0xFF, the update stops.

Note: In Loopback mode, the counter is incremented twice.

These bits are cleared by writing 1 to CFDC0FDCTR.SOCCLR.

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

28.2.11 CFDC0FDCRC : Channel 0 CANFD CRC Register

This register is not available in the classical CAN function.

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0110

Bit position:	31				27			24			20																			0
Bit field:	—	—	—	—	SCNT[3:0]				—	—	—	CRCREG[20:0]																			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
20:0	CRCREG[20:0]	CRC Register value These bits show the CRC value calculated for the CANFD frame.	R
23:21	—	These bits are read as 0. The write value should be 0.	R/W
27:24	SCNT[3:0]	Stuff bit count These bits shows the stuff bit count (mod 8) for the CANFD frame.	R
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The Channel 0 CANFD CRC Register holds the CRC value calculated for the CANFD frame.

CRCREG[20:0] bits (CRC Register value)

The CRCREG[20:0] bits contain the CRC value calculated by the CANFD channel logic when the CFDC0CTR.CTME bit is enabled.

The CFDC0FDCRC.CRCREG value is updated in the first bit of the CRC field of the CANFD frame (reception and transmission).

When the CFDC0CTR.CTME bit is 0, the CRCREG[20:0] bits are always read as 0.

When bit 17th of the CRC field is used, CRCREG[20:17] are always read as 0.

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

SCNT[3:0] bits (Stuff bit count)

The SCNT[3:0] bits contain the stuff count value of the CANFD frame. These bits indicate the number of inserted stuff bits (modulo 8, Graycoded) for a CANFD frame when the CFDC0CTR.CTME bit is enabled in CFDC0FDCRC.SCNT[3:1]. SCNT[0] is the parity bit.

When the CFDC0CTR.CTME bit is 0, the SCNT[3:0] bits are always read as 0.

The SCNT value is updated in the first bit of CRC field of the CANFD frame (reception and transmission).

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

SOC[7:0]位（成功发生计数器）

SOC[7:0]位与EOC[7:0]位一起使用，以支持主机控制的回退到与仲裁比特率相同的有效负载比特率选项，当使用减少的有效负载位长度的消息具有显着与其他消息相比，错误率更高。

SOC[7:0]位仅由CANFD模块逻辑设置。写入任何其他值均无效。

当通过接收或传输检测到总线上出现任何无错误消息时，这些位将被更新。当计数器达到0xFF的值时，更新停止。

Note: 在环回模式下，计数器增加两次。

这些位通过向CFDC0FDCTR.SOCCLR写入1来清除。

当相关CANFD通道处于CH_RESET模式时，这些位会自动清零。

28.2.11 CFDC0FDCRC:通道0CANFDCRC寄存器

该寄存器在经典CAN功能中不可用。

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0110

Bit position:	31				27			24			20																			0
Bit field:	—	—	—	—	SCNT[3:0]				—	—	—	CRCREG[20:0]																			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
20:0	CRCREG[20:0]	CRC寄存器值 这些位显示为CANFD帧计算的CRC值。	R
23:21	—	这些位被读取为0。写入值应为0。	R/W
27:24	SCNT[3:0]	东西位数 这些位显示CANFD帧的填充位计数(mod8)。	R
31:28	—	这些位被读取为0。写入值应为0。	R/W

通道0CANFDCRC寄存器保存为CANFD帧计算的CRC值。

CRCREG[20:0]位（CRC寄存器值）

CRCREG[20:0]位包含在使能CFDC0CTR.CTME位时由CANFD通道逻辑计算的CRC值。

CFDC0FDCRC.CRCREG值在CANFD帧（接收和发送）的CRC字段的第一位更新。

当CFDC0CTR.CTME位为0时，CRCREG[20:0]位总是读为0。

当使用CRC字段的第17位时，CRCREG[20:17]总是读为0。

当相关CANFD通道处于CH_RESET模式时，这些位会自动清零。

SCNT[3:0]位（填充位计数）

SCNT[3:0]位包含CANFD帧的填充计数值。当CFDC0FDCRC.SCNT[3:1]中的CFDC0CTR.CTME位使能时，这些位指示CANFD帧的插入填充位（模8，格雷编码）的数量。SCNT[0]是奇偶校验位。

当CFDC0CTR.CTME位为0时，SCNT[3:0]位总是读为0。

SCNT值在CANFD帧（接收和发送）的CRC字段的第一位更新。

当相关CANFD通道处于CH_RESET模式时，这些位会自动清零。

28.2.12 CFDGCFG : Global Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0014

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ITRCP[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TSSS	TSP[3:0]				—	—	CMPOC	DCS	MME	DRE	DCE	TPRI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TPRI	Transmission Priority 0: ID priority 1: Message buffer number priority	R/W
1	DCE	DLC Check Enable 0: DLC check disabled 1: DLC check enabled	R/W
2	DRE	DLC Replacement Enable 0: DLC replacement disabled 1: DLC replacement enabled	R/W
3	MME	Mirror Mode Enable 0: Mirror mode disabled 1: Mirror mode enabled	R/W
4	DCS	Data Link Controller Clock Select 0: Internal clean clock 1: External clock source connected to CANMCLK pin	R/W
5	CMPOC*1	CANFD Message Payload Overflow Configuration 0: Message is rejected 1: Message payload is cut to fit to configured message size	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
11:8	TSP[3:0]	Timestamp Prescaler 0x0: Timestamp prescaler = 1 0x1: Timestamp prescaler = 2 0x2: Timestamp prescaler = 4 0x3: Timestamp prescaler = 8 ⋮ 0xD: Timestamp prescaler = 8192 0xE: Timestamp prescaler = 16384 0xF: Timestamp prescaler = 32768	R/W
12	TSSS	Timestamp Source Select 0: Source clock for timestamp counter is peripheral clock 1: Source clock for timestamp counter is bit time clock	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W
31:16	ITRCP[15:0]	Interval Timer Reference Clock Prescaler FIFO interval timer prescaler value	R/W

Note 1. This bit are not available in the classical CAN function.

The Global Configuration Register is used to select the transmission priority to be used for all the TX message buffers and the clock source for the CAN protocol engine of CAN channel. The CFDGCFG register is also used to select the source for the timestamp clock and to configure the frequency for the timestamp clock and interval timer reference clock.

TPRI bit (Transmission Priority)

The TPRI bit selects the transmission priority for CAN channel.

28.2.12 CFDGCFG:全局配置寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0014

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ITRCP[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TSSS	TSP[3:0]				—	—	CMPOC	DCS	MME	DRE	DCE	TPRI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TPRI	传输优先级 0：ID优先1：消息缓冲区编号优先	R/W
1	DCE	DLC检查启用 0：禁用DLC检查1：启用DLC检查	R/W
2	DRE	DLC替换启用 0：禁用DLC替换1：启用DLC替换	R/W
3	MME	镜像模式启用 0：镜像模式关闭1：镜像模式开启	R/W
4	DCS	数据链路控制器时钟选择 0：内部清洁时钟1：连接到CANMCLK引脚的外部时钟源	R/W
5	CMPOC*1	CANFD消息负载溢出配置 0：消息被拒绝1：消息负载被剪切以适合配置的消息大小	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
11:8	TSP[3:0]	Timestamp Prescaler 0x0: Timestamp prescaler = 1 0x1: Timestamp prescaler = 2 0x2: Timestamp prescaler = 4 0x3: Timestamp prescaler = 8 ⋮ 0xD: Timestamp prescaler = 8192 0xE: Timestamp prescaler = 16384 0xF: Timestamp prescaler = 32768	R/W
12	TSSS	时间戳源选择 0：时间戳计数器的源时钟为外设时钟1：时间戳计数器的源时钟为位时钟	R/W
15:13	—	这些位被读取为0。写入值应为0。	R/W
31:16	ITRCP[15:0]	间隔定时器参考时钟预分频器 FIFO间隔定时器预分频器值	R/W

注1.该位在经典CAN功能中不可用。

全局配置寄存器用于选择用于所有TX报文缓冲区的传输优先级和CAN通道的CAN协议引擎的时钟源。CFDGCFG寄存器还用于选择时间戳时钟源以及配置时间戳时钟和间隔定时器参考时钟的频率。

TPRI bit (Transmission Priority)

TPRI位选择CAN通道的传输优先级。

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CANFD module is in GL_RESET mode.

Message buffer number priority should not be used together with TX queue transmission.

DCE bit (DLC Check Enable)

The DCE bit enables data length code (DLC) check for CAN channel.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CANFD module is in GL_RESET mode.

DRE bit (DLC Replacement Enable)

When the DRE bit is 1 and the DCE is 1, the CANFD stores the configured value (CFDGAFLP0r.GAFLDLC) of the DLC in the destination RX message buffer or FIFO buffer if the DLC check passes. Otherwise, the DLC value in the destination RX message buffer or FIFO buffer is unchanged.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CANFD module is in GL_RESET mode.

MME bit (Mirror Mode Enable)

The MME bit enables the Mirror mode for CAN channel.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CANFD module is in GL_RESET mode.

DCS bit (Data Link Controller Clock Select)

The DCS bit selects the clock source for CAN communication. Internal clean clock has a smaller clock jitter than the peripheral clock B (PCLKB).

Do not write to this bit in GL_SLEEP or GL_OPERATION mode. Only write to this bit when CANFD module is in GL_RESET mode.

CMPOC bit (CANFD Message Payload Overflow Configuration)

The CMPOC bit controls the message payload acceptance mechanism when the received payload is higher than the message buffer payload size CFDRMNB.RMPLS, CFDRFCCa.RFPLS, and CFDCFCC.CFPLS. The received message payload is always compared with the available message payload size in the message buffer.

Do not write to this bit in GL_SLEEP or GL_OPERATION mode. Only write to this bit when CANFD module is in GL_RESET mode.

When this bit is set and payload overflow occurs, the DLC value is stored in the RX message buffer or FIFO buffer unchanged.

Note: This bit is not available in the classical CAN function.

TSP[3:0] bits (Timestamp Prescaler)

The value configured in the TSP[3:0] bits defines the period of the clock source used for the timestamp counter.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CANFD module is in GL_RESET mode.

TSSS bit (Timestamp Source Select)

The TSSS bit allows the selection of the clock source for the timestamp counter.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CANFD module is in GL_RESET mode. Additionally, do not set this bit to 1 when CANFD communication is used.*1

Note: The bit time clock varies depending on the nominal and data rate bit configuration.

Note 1. This feature is not available in the classical CAN function.

ITRCP[15:0] bits (Interval Timer Reference Clock Prescaler)

The ITRCP[15:0] bits allow the definition of a reference clock for the FIFO interval timer source clock.

When these bits are 0x0000, the timer is disabled.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CANFD module is in GL_RESET mode.

不要在GL_SLEEP模式下写入该位。仅当CANFD模块处于GL_RESET模式时写入该位。

消息缓冲区编号优先级不应与TX队列传输一起使用。

DCE位（DLC检查启用）

DCE位启用CAN通道的数据长度代码(DLC)检查。

不要在GL_SLEEP模式下写入该位。仅当CANFD模块处于GL_RESET模式时写入该位。

DRE位（DLC替换启用）

当DRE位为1且DCE为1时，如果DLC检查通过，CANFD将DLC的配置值（CFDGAFLP0r.GAFLDLC）存储在目标RX消息缓冲区或FIFO缓冲区中。否则，目标RX消息缓冲区或FIFO缓冲区中的DLC值不变。

不要在GL_SLEEP模式下写入该位。仅当CANFD模块处于GL_RESET模式时写入该位。

MME位（镜像模式启用）

MME位使能CAN通道的镜像模式。

不要在GL_SLEEP模式下写入该位。仅当CANFD模块处于GL_RESET模式时写入该位。

DCS位（数据链路控制器时钟选择）

DCS位选择CAN通信的时钟源。内部干净时钟的时钟抖动小于外设时钟B(PCLKB)。

不要在GL_SLEEP或GL_OPERATION模式下写入该位。仅当CANFD模块在时写入该位
GL_RESET mode.

CMPOC位（CANFD消息有效负载溢出配置）

当接收到的有效载荷高于消息缓冲区有效载荷大小CFDRMNB.RMPLS、CFDRFCCa.RFPLS和CFDCFCC.CFPLS时，CMPOC位控制消息有效载荷接受机制。接收到的消息负载总是与消息缓冲区中可用的消息负载大小进行比较。

不要在GL_SLEEP或GL_OPERATION模式下写入该位。仅当CANFD模块在时写入该位
GL_RESET mode.

当该位被置位并发生有效载荷溢出时，DLC值不变地存储在RX报文缓冲区或FIFO缓冲区中。

Note: 该位在经典CAN功能中不可用。

TSP[3:0] bits (Timestamp Prescaler)

TSP[3:0]位中配置的值定义了用于时间戳计数器的时钟源的周期。

不要在GL_SLEEP模式下写入该位。仅当CANFD模块处于GL_RESET模式时写入该位。

TSSS位（时间戳源选择）

TSSS位允许选择时间戳计数器的时钟源。

不要在GL_SLEEP模式下写入该位。仅当CANFD模块处于GL_RESET模式时写入该位。
此外，使用CANFD通信时，请勿将此位设置为1。*1

Note: 位时钟取决于标称和数据速率位配置。

注1.此功能在经典CAN功能中不可用。

ITRCP[15:0]位（间隔定时器参考时钟预分频器）

ITRCP[15:0]位允许为FIFO间隔定时器源时钟定义参考时钟。

当这些位为0x0000时，定时器被禁用。

不要在GL_SLEEP模式下写入该位。仅当CANFD模块处于GL_RESET模式时写入该位。

28.2.13 CFDGCTR : Global Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0018

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TSRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CMPOFIE	THLEIE	MEIE	DEIE	—	—	—	—	—	GSLPR	GMDC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
1:0	GMDC[1:0]	Global Mode Control 0 0: Global operation mode request 0 1: Global reset mode request 1 0: Global halt mode request 1 1: Keep current value	R/W
2	GSLPR	Global Sleep Request 0: Global sleep request disabled 1: Global sleep request enabled	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
8	DEIE	DLC Check Interrupt Enable 0: DLC check interrupt disabled 1: DLC check interrupt enabled	R/W
9	MEIE	Message Lost Error Interrupt Enable 0: Message lost error interrupt disabled 1: Message lost error interrupt enabled	R/W
10	THLEIE	TX History List Entry Lost Interrupt Enable 0: TX history list entry lost interrupt disabled 1: TX history list entry lost interrupt enabled	R/W
11	CMPOFIE*1	CANFD Message Payload Overflow Flag Interrupt Enable 0: CANFD message payload overflow flag interrupt disabled 1: CANFD message payload overflow flag interrupt enabled	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
16	TSRST	Timestamp Reset 0: Timestamp not reset 1: Timestamp reset	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is not available in the classical CAN function.

The Global Control Register controls the global mode of the CANFD module and the timestamp function. The register also enables and disables the global error interrupts.

GMDC bits (Global Mode Control)

The GMDC bits can be used to configure the modes for the CANFD module. Additionally, if CFDGCTR.GSLPR bit is 1 when the CANFD module is in Reset mode, the CANFD module enters Global Sleep mode.

Setting the GMDC bits to 11b has no effect. Mode transition is described in detail in section 28.3.2. Global Modes.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

GSLPR bit (Global Sleep Request)

The GSLPR bit globally selects the sleep request for CANFD module including CAN channels. Channel sleep request is set automatically for channels.

28.2.13 CFDGCTR:全局控制寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0018

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TSRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CMPOFIE	THLEIE	MEIE	DEIE	—	—	—	—	—	GSLPR	GMDC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
1:0	GMDC[1:0]	全局模式控制 00：全局操作模式请求01：全局复位模式请求10：全局停止模式请求11：保持当前值	R/W
2	GSLPR	全局睡眠请求 0：禁用全局睡眠请求1：启用全局睡眠请求	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
8	DEIE	DLC检查中断启用 0：禁用DLC检查中断1：启用DLC检查中断	R/W
9	MEIE	消息丢失错误中断使能 0：禁用消息丢失错误中断1：启用消息丢失错误中断	R/W
10	THLEIE	TX历史列表条目丢失中断启用 0：禁用TX历史列表条目丢失中断1：启用TX历史列表条目丢失中断	R/W
11	CMPOFIE*1	CANFD消息有效负载溢出标志中断使能 0：禁止CANFD报文有效载荷溢出标志中断1：使能CANFD报文有效载荷溢出标志中断	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W
16	TSRST	时间戳重置 0：时间戳不复位1：时间戳复位	R/W
31:17	—	这些位被读取为0。写入值应为0。	R/W

注1.该位在经典CAN功能中不可用。

全局控制寄存器控制CANFD模块的全局模式和时间戳功能。该寄存器还启用和禁用全局错误中断。

GMDC位（全局模式控制）

GMDC位可用于配置CANFD模块的模式。此外，如果当CANFD模块处于复位模式时CFDGCTR.GSLPR位为1，则CANFD模块进入全局休眠模式。

将GMDC位设置为11b无效。模式转换在28.3.2节中有详细描述。全局模式。

CANFD模块处于GL_SLEEP模式时不要写入该位。

GSLPR位（全局休眠请求）

GSLPR位全局选择CANFD模块的睡眠请求，包括CAN通道。频道睡眠请求是自动为频道设置的。

Only write to this bit when the CANFD module is in GL_RESET or GL_SLEEP mode.

DEIE bit (DLC Check Interrupt Enable)

When the DEIE bit is 1, an interrupt is generated if a DLC error is detected in the received frames.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

MEIE bit (Message Lost Error Interrupt Enable)

When the MEIE bit is 1, an interrupt is generated if a message lost condition occurs.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

THLEIE bit (TX History List Entry Lost Interrupt Enable)

When the THLEIE bit is 1, an interrupt is generated if a TX history list entry lost condition occurs.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

CMPOFIE bit (CANFD Message Payload Overflow Flag Interrupt Enable)

When the CMPOFIE bit is 1, an interrupt is generated when a CANFD message payload overflow condition occurs.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

Note: This bit is not available in the classical CAN function

TSRST bit (Timestamp Reset)

When the TSRST bit is 1, the Global Timestamp Register is reset to 0x0000.

Do not write to this bit when the CANFD module is in GL_SLEEP or GL_RESET mode.

Read value is always 0.

This bit is cleared automatically by the CANFD module logic.

28.2.14 CFDGSTS : Global Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x001C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	GRAMINIT	GSLPSTS	GHLTSTS	GRSTSTS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bit	Symbol	Function	R/W
0	GRSTSTS	Global Reset Status 0: Not in Reset mode 1: In Reset mode	R
1	GHLTSTS	Global Halt Status 0: Not in Halt mode 1: In Halt mode	R
2	GSLPSTS	Global Sleep Status 0: Not in Sleep mode 1: In Sleep mode	R
3	GRAMINIT	Global RAM Initialization 0: RAM initialization is complete 1: RAM initialization is ongoing	R

仅当CANFD模块处于GL_RESET或GL_SLEEP模式时写入该位。

DEIE位（DLC检查中断使能）

当DEIE位为1时，如果在接收的帧中检测到DLC错误，则产生中断。

CANFD模块处于GL_SLEEP模式时不要写入该位。

MEIE位（消息丢失错误中断使能）

当MEIE位为1时，如果发生信息丢失情况，将产生中断。

CANFD模块处于GL_SLEEP模式时不要写入该位。

THLEIE位（TX历史列表条目丢失中断使能）

当THLEIE位为1时，如果发生TX历史列表条目丢失情况，将产生中断。

CANFD模块处于GL_SLEEP模式时不要写入该位。

CMPOFIE位（CANFD消息有效负载溢出标志中断使能）

当CMPOFIE位为1时，当CANFD报文有效负载溢出条件发生时产生中断。

CANFD模块处于GL_SLEEP模式时不要写入该位。

Note: 该位在经典CAN功能中不可用

TSRST bit (Timestamp Reset)

当TSRST位为1时，全局时间戳寄存器复位为0x0000。

当CANFD模块处于GL_SLEEP或GL_RESET模式时，请勿写入该位。

读取值始终为0。

该位由CANFD模块逻辑自动清零。

28.2.14 CFDGSTS:全局状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x001C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	克初始化	GSLPSTS	GHLTSTS	GRSTSTS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bit	Symbol	Function	R/W
0	GRSTSTS	全局重置状态 0：不处于复位模式1 ：处于复位模式	R
1	GHLTSTS	全局停止状态 0：不处于暂停模式 1：处于暂停模式	R
2	GSLPSTS	全局睡眠状态 0：不处于休眠模式1 ：处于休眠模式	R
3	GRAMINIT	全局RAM初始化 0：RAM初始化完成1：RAM初始化正在进行	R

Bit	Symbol	Function	R/W
31:4	—	These bits are read as 0. The write value should be 0.	R/W

The Global Status Register indicates the global status of the CANFD module.

GRSTSTS bit (Global Reset Status)

The GRSTSTS bit indicates the status of Global CANFD module Reset mode.

This bit is set automatically when the CANFD module enters GL_RESET mode. When the mode changes from GL_RESET mode to GL_SLEEP mode, this bit remains set.

This bit is cleared automatically when the CANFD module exits the GL_RESET mode.

GHLTSTS bit (Global Halt Status)

The GHLTSTS bit indicates the status of Global CANFD module Halt mode.

This bit is set automatically when the CANFD module enters GL_HALT mode.

This bit is cleared automatically when the CANFD module exits the GL_HALT mode.

GSLPSTS bit (Global Sleep Status)

The GSLPSTS bit indicates the status of Global CANFD module Sleep mode.

This bit is set automatically when the CANFD module enters GL_SLEEP mode.

This bit is cleared automatically when the CANFD module exits the GL_SLEEP mode.

GRAMINIT bit (Global RAM Initialization)

The GRAMINIT bit indicates the status of Global CANFD module RAM initialization.

This bit is set automatically when the CANFD module enters GL_SLEEP mode after a hardware reset.

This bit is cleared automatically when the CANFD module completed RAM initialization.

This bit is cleared when the test_mode input port is set to 1.

28.2.15 CFDGERFL : Global Error Flag Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EEF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	CMPOF	THLES	MES	DEF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DEF	DLC Error Flag 0: DLC error not detected 1: DLC error detected	R/W
1	MES	Message Lost Error Status 0: Message lost error not detected 1: Message lost error detected	R
2	THLES	TX History List Entry Lost Error Status 0: TX history list entry lost error not detected 1: TX history list entry lost error detected	R

Bit	Symbol	Function	R/W
31:4	—	这些位被读取为0。写入值应为0。	R/W

全局状态寄存器指示CANFD模块的全局状态。

GRSTSTS位（全局复位状态）

GRSTSTS位指示全局CANFD模块复位模式的状态。

当CANFD模块进入GL_RESET模式时，该位自动设置。当模式从GL_RESET模式更改为GL_SLEEP模式时，该位保持设置。

当CANFD模块退出GL_RESET模式时，该位自动清零。

GHLTSTS位（全局停止状态）

GHLTSTS位指示全局CANFD模块停止模式的状态。

当CANFD模块进入GL_HALT模式时，该位自动置位。

当CANFD模块退出GL_HALT模式时，该位自动清零。

GSLPSTS位（全局休眠状态）

GSLPSTS位指示全局CANFD模块休眠模式的状态。

当CANFD模块进入GL_SLEEP模式时，该位自动置位。

当CANFD模块退出GL_SLEEP模式时，该位自动清零。

GRAMMINIT位（全局RAM初始化）

GRAMMINIT位指示全局CANFD模块RAM初始化的状态。

当CANFD模块在硬件复位后进入GL_SLEEP模式时，该位自动置位。

当CANFD模块完成RAM初始化时，该位自动清零。

当test_mode输入端口设置为1时，该位清零。

28.2.15 CFDGERFL:全局错误标志寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EEF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	CMPOF	THLES	MES	DEF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DEF	DLC错误标志 0：未检测到DLC错误1： 检测到DLC错误	R/W
1	MES	消息丢失错误状态 0：未检测到消息丢失错误1：检测 到消息丢失错误	R
2	THLES	TX历史列表条目丢失错误状态 0：未检测到TX历史列表条目丢失错误1：检 测到TX历史列表条目丢失错误	R

Bit	Symbol	Function	R/W
3	CMPOF*1	CANFD Message Payload Overflow Flag 0: CANFD message payload overflow not detected 1: CANFD message payload overflow detected	R/W
4	—	This bit is read as 0. The write value should be 0.	R
5	—	This bit is read as 0. The write value should be 0.	R
6	—	This bit is read as 0. The write value should be 0.	R
15:7	—	These bits are read as 0. The write value should be 0.	R/W
16	EEF0	ECC Error Flag for 0: ECC error not detected during TX-SCAN 1: ECC error detected during TX-SCAN	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is not available in the classical CAN function.

The Global Error Flag register indicates the detection of global errors.

DEF bit (DLC Error Flag)

The DEF bit indicates the error status of the DLC.

Do not write to this bit when the CANFD module is in GL_SLEEP or GL_RESET mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically when a DLC error is detected in a received frame.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set

The bit is cleared by writing 0 to it.

This bit is cleared automatically in GL_RESET mode.

MES bit (Message Lost Error Status)

The MES bit indicates status of the message lost error.

This bit is set automatically when a FIFO message lost error is detected.

This bit is cleared automatically when:

- All FIFO message lost flags are cleared
- The CANFD module is in GL_RESET mode.

THLES bit (TX History List Entry Lost Error Status)

The THLES bit indicates status of the TX history list entry lost error.

This bit is set automatically when a TX history list entry lost error is detected.

This bit is cleared automatically when:

- All TX history list entry lost flags are cleared
- The CANFD module is in GL_RESET mode.

CMPOF bit (CANFD Message Payload Overflow Flag)

The CMPOF bit is set automatically when a CANFD message payload overflow is detected on at least one channel.

Do not write to this bit when the CANFD module is in GL_SLEEP or GL_RESET mode.

This bit is cleared by writing 0 to it. Writing 1 to this bit has no effect.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is cleared automatically in GL_RESET mode.

Bit	Symbol	Function	R/W
3	CMPOF*1	CANFD消息有效负载溢出标志 0：未检测到CANFD消息负载溢出1：检测到CANFD消息负载溢出	R/W
4	—	该位读取为0。写入值应为0。	R
5	—	该位读取为0。写入值应为0。	R
6	—	该位读取为0。写入值应为0。	R
15:7	—	这些位被读取为0。写入值应为0。	R/W
16	EEF0	ECC错误标志 0：在TX-SCAN期间未检测到ECC错误1：在TX-SCAN期间检测到ECC错误	R/W
31:17	—	这些位被读取为0。写入值应为0。	R/W

注1.该位在经典CAN功能中不可用。

全局错误标志寄存器指示全局错误的检测。

DEF位（DLC错误标志）

DEF位指示DLC的错误状态。

当CANFD模块处于GL_SLEEP或GL_RESET模式时，请勿写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

当在接收帧中检测到DLC错误时，该位自动设置。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置

该位通过向其写入0来清除。

该位在GL_RESET模式下自动清除。

MES位（消息丢失错误状态）

MES位指示消息丢失错误的状态。

当检测到FIFO消息丢失错误时，该位自动置位。

该位在以下情况下自动清零：

●清除所有FIFO消息丢失标志

●CANFD模块处于GL_RESET模式。

THLES位（TX历史列表条目丢失错误状态）

THLES位指示TX历史列表条目丢失错误的状态。

当检测到TX历史列表条目丢失错误时，该位自动设置。

该位在以下情况下自动清零：

●清除所有TX历史列表条目丢失标志

●CANFD模块处于GL_RESET模式。

CMPOF位（CANFD消息有效负载溢出标志）

当在至少一个通道上检测到CANFD消息有效负载溢出时，CMPOF位自动置位。

当CANFD模块处于GL_SLEEP或GL_RESET模式时，请勿写入该位。

该位通过写入0清零。向该位写入1无效。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

该位在GL_RESET模式下自动清除。

Note: This bit is not available in the classical CAN function

EEF0 bit (ECC Error Flag for)

The EEF0 bit specifies whether an ECC error has occurred on Channel 0.

Do not write to this bit when the CANFD module is in GL_SLEEP or GL_RESET mode. Writing 1 to this bit has no effect.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

The bit is cleared by writing 0 to it. This bit is cleared automatically in GL_RESET mode.

28.2.16 CFDGTINTSTS : Global TX Interrupt Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00A4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	THIF0	CFTIF0	TQIF0	TAI0	TSIF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSIF0	TX Successful Interrupt Flag 0: Channel n TX Successful Interrupt flag not set 1: Channel n TX Successful Interrupt flag set	R
1	TAI0	TX Abort Interrupt Flag 0: Channel n TX Abort Interrupt flag not set 1: Channel n TX Abort Interrupt flag set	R
2	TQIF0	TX Queue Interrupt Flag 0: Channel n TX Queue Interrupt flag not set 1: Channel n TX Queue Interrupt flag set	R
3	CFTIF0	COM FIFO TX Mode Interrupt Flag 0: Channel n COM FIFO TX Mode Interrupt flag not set 1: Channel n COM FIFO TX Mode Interrupt flag set	R
4	THIF0	TX History List Interrupt 0: Channel n TX History List Interrupt flag not set 1: Channel n TX History List Interrupt flag set	R
31:5	—	These bits are read as 0. The write value should be 0.	R/W

The Global TX Interrupt Status register indicates the detection of transmit specific interrupts.

TSIF0 bit (TX Successful Interrupt Flag)

The TSIF0 bit is set to 1 when the TX Successful Interrupt flag of the related channel is set (when the interrupt is enabled). This bit is cleared automatically:

- When the related TX MB Result Status bits are cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

TAI0 bit (TX Abort Interrupt Flag)

The TAIF0 bit is set to 1 when the TX Abort Interrupt flag of the related channel is set (when the interrupt is enabled).

This bit is cleared automatically:

Note: 该位在经典CAN功能中不可用

EEF0位（ECC错误标志）

EEF0位指定通道0上是否发生ECC错误。

当CANFD模块处于GL_SLEEP或GL_RESET模式时，请勿写入该位。向该位写入1无效。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

该位通过向其写入0来清除。该位在GL_RESET模式下自动清除。

28.2.16 CFDGTINTSTS:全局TX中断状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00A4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	THIF0	CFTIF0	TQIF0	TAI0	TSIF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSIF0	TX成功中断标志 0：未设置通道nTX成功中断标志1：设置了通道nTX成功中断标志	R
1	TAI0	TX中止中断标志 0：未设置通道nTX中止中断标志1：设置了通道nTX中止中断标志	R
2	TQIF0	TX队列中断标志 0：未设置通道nTX队列中断标志1：设置了通道nTX队列中断标志	R
3	CFTIF0	COMFIFOTX模式中断标志 0：未设置通道nCOMFIFOTX模式中断标志1：设置了通道nCOMFIFOTX模式中断标志	R
4	THIF0	TX历史列表中断 0：通道nTX历史列表中断标志未设置1：通道nTX历史列表中断标志设置	R
31:5	—	这些位被读取为0。写入值应为0。	R/W

全局TX中断状态寄存器指示发送特定中断的检测。

TSIF0位（TX成功中断标志）

当相关通道的TX成功中断标志置位时（中断使能时），TSIF0位设置为1。
该位自动清零：

- 当相关的TXMBResultStatus位被清除时（当中断使能被禁用时）
- 在GL_RESET或CH_RESET模式下。

TAI0位（TX中止中断标志）

当相关通道的TXAbortInterrupt标志置位时（中断使能时），TAIF0位被置1。

该位自动清零：

- When the related TX MB Result Status bits are cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

TQIF0 bit (TX Queue Interrupt Flag)

The TQIF0 bit is set to 1 when the TX Queue Interrupt flag of the related channel is set (when the interrupt is enabled). This bit is cleared automatically:

- When the related TX Queue Interrupt flag is cleared (when the interrupt is enable disabled)
- When in GL_RESET or CH_RESET mode.

CFTIF0 bit (COM FIFO TX Mode Interrupt Flag)

The CFTIF0 bit is set to 1 when the related COM TX FIFO Mode Interrupt flag (CFDCFSTS.CFTXIF) is set (when the interrupt is enabled).

This bit is cleared automatically:

- When the related COM TXW FIFO Mode Interrupt flag (CFDCFSTS.CFTXIF) is cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

THIF0 bit (TX History List Interrupt)

The THIF0 bit is set to 1 when the related TX History List Interrupt flag (CFDTHLSTS.THLIF) is set (when the interrupt is enabled).

This bit is cleared automatically:

- When the related TX History List Interrupt flag (CFDTHLSTS.THLIF) is cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

28.2.17 CFDGTSC : Global Timestamp Counter Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0024

Bit position:	31															15															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TS[15:0]	Timestamp value	R
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The Global Timestamp Counter register stores the timestamp based on the selected configuration.

TS[15:0] bits (Timestamp value)

The Timestamp value is stored in the Global Timestamp Counter register based on the configuration of TSSS, TSBTCS and TSP. The accuracy of the timestamp counter cannot be guaranteed when transitioning to halt state.

The Timestamp value is stored in this register based on the configuration of TSSS, TSBTCS and TSP.

Do not write to bits TS[15:0] when the CANFD module is in GL_RESET or GL_SLEEP mode.

The TS[15:0] bits are cleared automatically in GL_RESET mode.

●当相关的TXMBResultStatus位被清除时（当中断使能被禁用时）

●在GL_RESET或CH_RESET模式下。

TQIF0位（TX队列中断标志）

当相关通道的TX队列中断标志置位（中断使能时）时，TQIF0位被置1。
该位自动清零：

●相关TXQueueInterrupt标志清零时（中断使能禁止时）

●在GL_RESET或CH_RESET模式下。

CFTIF0位（COMFIFOTX模式中断标志）

当相关的COMTXFIFO模式中断标志(CFDCFSTS.CFTXIF)置位时（中断使能时），CFTIF0位被置1。

该位自动清零：

●当相关的COMTXWFIFO模式中断标志（CFDCFSTS.CFTXIF）被清除时（当中断使能被禁用时）

●在GL_RESET或CH_RESET模式下。

THIF0位（TX历史列表中断）

当相关的TX历史列表中断标志(CFDTHLSTS.THLIF)置位时（中断使能时），THIF0位被置1。

该位自动清零：

●当相关的TX历史列表中断标志(CFDTHLSTS.THLIF)被清除时（当中断使能被禁用时）

●在GL_RESET或CH_RESET模式下。

28.2.17 CFDGTSC:全球时间戳计数器寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0024

Bit position:	31															15															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TS[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TS[15:0]	时间戳值	R
31:16	—	这些位被读取为0。写入值应为0。	R/W

全局时间戳计数器寄存器存储基于所选配置的时间戳。

TS[15:0] bits (Timestamp value)

Timestamp值根据TSSS、TSBTCS和
茶多酚。转换到停止状态时，无法保证时间戳计数器的准确性。

Timestamp值根据TSSS、TSBTCS和TSP的配置存储在该寄存器中。

当CANFD模块处于GL_RESET或GL_SLEEP模式时，请勿写入位TS[15:0]。

TS[15:0]位在GL_RESET模式下自动清零。

28.2.18 CFDGAFLECTR : Global Acceptance Filter List Entry Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0028

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	AFLDAE	—	—	—	—	—	—	—	AFLPN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AFLPN	Acceptance Filter List Page Number Select an Acceptance Filter List page	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
8	AFLDAE	Acceptance Filter List Data Access Enable 0: Acceptance Filter List data access disabled 1: Acceptance Filter List data access enabled	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

The Global Acceptance Filter List Entry Control Register is used to select the Global Acceptance Filter List page for reading or writing entries into the Global Acceptance Filter List.

AFLPN bit (Acceptance Filter List Page Number)

The AFLPN bit select the page number to access the desired RAM area of the Acceptance Filter List. Acceptance Filter List page consists of 16 Acceptance Filter List entries.

Read/write accesses to the Acceptance Filter List can only be performed through a fixed window.

Do not write to these bits when the CANFD module is in GL_SLEEP mode. Enter only the values between 0 and 1, inclusive.

AFLDAE bit (Acceptance Filter List Data Access Enable)

The AFLDAE bit prevents write access to the Acceptance Filter List when cleared after configuration of the Acceptance Filter List.

Data can be read from the Acceptance Filter List independent of the status of this bit.

Do not write to this bit when the CANFD module is in GL_SLEEP mode. Set this bit to enable write access for the Acceptance Filter List.

28.2.19 CFDGAFLCFG : Global Acceptance Filter List Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x002C

Bit position:	31	21	16	0
Bit field:	—	RNC0[5:0]	—	—
Value after reset:	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 0. The write value should be 0.	R/W

28.2.18 CFDGAFLECTR:全局接受过滤器列表条目控制寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0028

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	AFLDAE	—	—	—	—	—	—	—	AFLPN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AFLPN	接受过滤器列表页码选择接受过滤器 列表页面	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
8	AFLDAE	接受过滤器列表数据访问启用 0：禁用接受过滤器列表数据访问1：启用接受 过滤器列表数据访问	R/W
31:9	—	这些位被读取为0。写入值应为0。	R/W

全局接受过滤器列表条目控制寄存器用于选择全局接受过滤器列表页面，以将条目读取或写入全局接受过滤器列表。

AFLPN位（接受过滤器列表页码）

AFLPN位选择页码以访问验收过滤器列表的所需RAM区域。接受过滤器列表页面由16个接受过滤器列表条目组成。

只能通过固定窗口执行对接受过滤器列表的读写访问。

当CANFD模块处于GL_SLEEP模式时，不要写入这些位。仅输入0和1之间的值，包括0和1。

AFLDAE位（接受过滤器列表数据访问使能）

AFLDAE位在配置接受后清除时可防止对接受过滤器列表的写访问
过滤器列表。

可以从接受过滤器列表中读取数据，而与该位的状态无关。

CANFD模块处于GL_SLEEP模式时不要写入该位。设置该位以启用写访问
接受过滤器列表。

28.2.19 CFDGAFLCFG:全局接受过滤器列表配置寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x002C

Bit position:	31	21	16	0
Bit field:	—	RNC0[5:0]	—	—
重置后的值:	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
21:16	RNC0[5:0]	Rule Number Number of rules dedicated to channel 0	R/W
31:22	—	These bits are read as 0. The write value should be 0.	R/W

The Global Acceptance Filter List Configuration Register is used to define the number of rules for entries in the Acceptance Filter List.

The total number of available entries in the Acceptance Filter List is 32.

RNC0[5:0] bits (Rule Number)

The RNC0[5:0] bits define the number of rules in the Acceptance Filter List for channel n.

Only write to these bits when the CANFD module is in GL_RESET mode. These bits can set to 6 bits for 32 rules.

28.2.20 CFDGAFLIDr : Global Acceptance Filter List ID Registers (r = 1 to 16)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0120 + 0x0010 × (r - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLIDE	GAFLRTR	GAFLLB	GAFLID[28:16]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFLID[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	GAFLID[28:0]	Global Acceptance Filter List Entry ID Field ID part of the Global Acceptance Filter List entry	R/W
29	GAFLLB	Global Acceptance Filter List Entry Loopback Configuration 0: Global Acceptance Filter List entry ID for acceptance filtering with attribute RX 1: Global Acceptance Filter List entry ID for acceptance filtering with attribute TX	R/W
30	GAFLRTR	Global Acceptance Filter List Entry RTR Field 0: Data frame 1: Remote frame	R/W
31	GAFLIDE	Global Acceptance Filter List Entry IDE Field 0: Standard identifier of rule entry ID is valid for acceptance filtering 1: Extended identifier of rule entry ID is valid for acceptance filtering	R/W

The Global Acceptance Filter List ID Registers are used to configure the ID field for the rules of entries in the Global Acceptance Filter List.

GAFLID[28:0] bits (Global Acceptance Filter List Entry ID Field)

The GAFLID[28:0] bits represent the CAN identifier (ID) field of each entry in the Global Acceptance Filter List.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

GAFLLB bit (Global Acceptance Filter List Entry Loopback Configuration)

The GAFLLB bit selects whether entry in the Global Acceptance Filter List gets the attribute RX or TX.

This attribute determines the validity of the entry in Mirror mode, Loopback test mode, and during standard (non-loopback) reception. See section 28.5.5. Loopback Modes for detailed description of the validity of the Global Acceptance Filter List entry depending on transmitter/receiver case, the type of loopback mode, and RX/TX attribute.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Bit	Symbol	Function	R/W
21:16	RNC0[5:0]	规则编号 专用于通道0的规则数	R/W
31:22	—	这些位被读取为0。写入值应为0。	R/W

GlobalAcceptanceFilterListConfigurationRegister用于定义Acceptance中条目的规则数量
过滤器列表。

接受过滤器列表中的可用条目总数为32。

RNC0[5:0] bits (Rule Number)

RNC0[5:0]位定义通道n的接受过滤器列表中的规则数量。

仅当CANFD模块处于GL_RESET模式时才写入这些位。对于32条规则，这些位可以设置为6位。

28.2.20 CFDGAFLIDr：全局接受过滤器列表ID寄存器（r=1到16）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0120 + 0x0010 × (r - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLIDE	GAFLRTR	GAFLLB	GAFLID[28:16]												
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFLID[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	GAFLID[28:0]	全局接受过滤器列表条目ID字段 全局接受过滤器列表条目的ID部分	R/W
29	GAFLLB	全局接受过滤器列表条目环回配置 0：全局接受过滤器列表条目ID，用于带有属性RX的接受过滤1：全局接受过滤器列表条目ID，用于带有属性TX的接受过滤	R/W
30	GAFLRTR	全局接受过滤器列表条目RTR字段 0：数据帧1：远程帧	R/W
31	GAFLIDE	全局验收过滤器列表条目IDE字段 0：规则条目ID的标准标识符对接受过滤有效1：规则条目ID的扩展标识符对接受过滤有效	R/W

GlobalAcceptanceFilterListIDRegisters用于配置全局条目规则的ID字段
接受过滤器列表。

GAFLID[28:0]位（全局接受过滤器列表条目ID字段）

GAFLID[28:0]位代表全局接受过滤器列表中每个条目的CAN标识符(ID)字段。

当CFDGAFLECTR.AFLDAE位为0时，不要写入这些位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。

GAFLLB位（全局接受过滤器列表条目环回配置）

GAFLLB位选择全局接受过滤器列表中的条目是否获得属性RX或TX。

此属性确定条目在镜像模式、环回测试模式和标准（非环回）接收期间的有效性。请参阅第28.5.5节。Loopback Modes用于详细描述GlobalAcceptanceFilterList条目的有效性，具体取决于发送器接收器情况、环回模式的类型和RXTX属性。

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

GAFLRTR bit (Global Acceptance Filter List Entry RTR Field)

The GAFLRTR bit allows the configuration of the specified frame format (data frame or remote frame) for each entry of the Global Acceptance Filter List. For each rule entry in a CAN channel, the acceptance filter process compares this bit against the RTR bit of the received CAN message.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

GAFLIDE bit (Global Acceptance Filter List Entry IDE Field)

The GAFLIDE bit allows the configuration of the ID format (standard ID or extended ID) for each entry in the Global Acceptance Filter List. For each rule entry in a CAN channel, the acceptance filter process compares this bit against the IDE bit of the received CAN message.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

28.2.21 CFDGAFLMr : Global Acceptance Filter List Mask Registers (r = 1 to 16)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0124 + 0x0010 × (r - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLIDEM	GAFLRTRM	GAFLIFL1	GAFLIDM[28:16]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFLIDM[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	GAFLIDM[28:0]	Global Acceptance Filter List ID Mask Field Global Acceptance Filter List Mask field bits for ID field	R/W
29	GAFLIFL1	Global Acceptance Filter List Information Label 1 Global Acceptance Filter List information label bit 1	R/W
30	GAFLRTRM	Global Acceptance Filter List Entry RTR Mask 0: RTR bit is not used for ID matching 1: RTR bit is used for ID matching	R/W
31	GAFLIDEM	Global Acceptance Filter List IDE Mask 0: IDE bit is not used for ID matching 1: IDE bit is used for ID matching	R/W

The Global Acceptance Filter List Mask Registers are used to configure the Mask field of each rule for entries in the Global Acceptance Filter List.

GAFLIDM[28:0] bits (Global Acceptance Filter List ID Mask Field)

GAFLIDM[28:0] bits are the filter mask bits for the related bits in the CAN Identifier field of each Global Acceptance Filter List entry.

0	Corresponding STD-ID/EXT-ID bit is not used for ID matching
1	Corresponding STD-ID/EXT-ID bit is used for ID matching

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入该位。

GAFLRTR位（全局接受过滤器列表条目RTR字段）

GAFLRTR位允许为全局接受过滤器列表的每个条目配置指定的帧格式（数据帧或远程帧）。对于CAN通道中的每个规则条目，接受过滤器进程将该位与接收到的CAN消息的RTR位进行比较。

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入该位。

GAFLIDE位（全局接受过滤器列表条目IDE字段）

GAFLIDE位允许为全局中的每个条目配置ID格式（标准ID或扩展ID）
接受过滤器列表。对于CAN通道中的每个规则条目，接受过滤器进程将该位与接收到的CAN消息的IDE位进行比较。

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入该位。

28.2.21 CFDGAFLMr：全局验收过滤器列表屏蔽寄存器（r=1到16）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0124 + 0x0010 × (r - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLIDEM	GAFLRTRM	GAFLIFL1	GAFLIDM[28:16]												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFLIDM[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	GAFLIDM[28:0]	全局接受过滤器列表ID掩码字段 ID字段的全局接受过滤器列表掩码字段位	R/W
29	GAFLIFL1	全局接受过滤器列表信息标签1 全局接受过滤器列表信息标签位1	R/W
30	GAFLRTRM	全局接受过滤器列表条目RTR掩码 0：RTR位不用于ID匹配1：RTR位用于ID匹配	R/W
31	GAFLIDEM	全局接受过滤器列表IDE掩码 0：IDE位不用于ID匹配1：IDE位用于ID匹配	R/W

全局接受过滤器列表掩码寄存器用于为全局中的条目配置每个规则的掩码字段
接受过滤器列表。

GAFLIDM[28:0]位（全局接受过滤器列表ID掩码字段）

GAFLIDM[28:0]位是每个全局接受过滤器的CAN标识符字段中相关位的过滤器掩码位
列表条目。

0	对应的STD-IDEXT-ID位不用于ID匹配
1	对应的STD-IDEXT-ID位用于ID匹配

当CFDGAFLECTR.AFLDAE位为0时，不要写入这些位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。

GAFLIFL1 bit (Global Acceptance Filter List Information Label 1)

The GAFLIFL1 bit allows the configuration of a 2-bit information label to be attached to a received message accepted by the associated entry in the Global Acceptance Filter List. This bit is a MSB bit of an information label.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

This bit is stored in the Information Label Field [1] (CFDRMFDSTSb.RMIFL [1], CFDRFFDSTSb.RFIFL [1], CFDCFFDCSTS.CFIFL [1]) of the storage location of an incoming message.

GAFLRTRM bit (Global Acceptance Filter List Entry RTR Mask)

The GAFLRTRM bit allows the configuration of the RTR mask bit for each entry in the Global Acceptance Filter List.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

GAFLIDEM bit (Global Acceptance Filter List IDE Mask)

The GAFLIDEM bit allows the configuration of the IDE mask bit for each entry in the Global Acceptance Filter List.

When the IDE mask bit is 0, the ID comparison depends on the received IDE bit.

If the received IDE bit is 0, the STD-ID comparison takes place.

If the received IDE bit is 1, the EXT-ID comparison takes place.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

28.2.22 CFDGAFLP0r : Global Acceptance Filter List Pointer 0 Registers (r = 1 to 16)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0128 + 0x0010 × (r - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFLRMV	—	—	GAFLRMDP[4:0]					GAFLIFL0	—	—	—	GAFLDLC[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	GAFLDLC[3:0]	Global Acceptance Filter List DLC Field Minimum number of data bytes in a data frame required for acceptance	R/W
6:4	—	These bits are read as 0. The write value should be 0.	R/W
7	GAFLIFL0	Global Acceptance Filter List Information Label 0	R/W
12:8	GAFLRMDP[4:0]	Global Acceptance Filter List RX Message Buffer Direction Pointer RX message buffer number for storage of received messages	R/W
14:13	—	These bits are read as 0. The write value should be 0.	R/W
15	GAFLRMV	Global Acceptance Filter List RX Message Buffer Valid 0: Single message buffer direction pointer is invalid 1: Single message buffer direction pointer is valid	R/W
31:16	GAFLPTR[15:0]	Global Acceptance Filter List Pointer	R/W

The Global Acceptance Filter List Pointer 0 Registers are used to configure the data length code (DLC), software pointer, single message buffer select, and message buffer direction pointer for each rule entry in the Global Acceptance Filter List.

GAFLIFL1位（全局接受过滤器列表信息标签1）

GAFLIFL1位允许将2位信息标签的配置附加到由全局接受过滤器列表中的相关条目接受的接收消息。该位是信息标签的MSB位。

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入该位。

该位存储在信息标签字段[1]（CFDRMFDSTSb.RMIFL[1]、CFDRFFDSTSb.RFIFL[1]、CFDCFFDCSTS.CFIFL[1])传入消息的存储位置。

GAFLRTRM位（全局接受过滤器列表条目RTR掩码）

GAFLRTRM位允许为全局接受过滤器列表中的每个条目配置RTR掩码位。

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入该位。

GAFLIDEM位（全局接受过滤器列表IDE掩码）

GAFLIDEM位允许为全局接受过滤器列表中的每个条目配置IDE掩码位。

当IDE掩码位为0时，ID比较取决于接收到的IDE位。

如果接收到的IDE位为0，则进行STD-ID比较。

如果接收到的IDE位为1，则进行EXT-ID比较。

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入该位。

28.2.22 CFDGAFLP0r：全局验收过滤器列表指针0寄存器（r=1到16）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0128 + 0x0010 × (r - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLPTR[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFLRMV	—	—	GAFLRMDP[4:0]					GAFLIFL0	—	—	—	GAFLDLC[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	GAFLDLC[3:0]	全局接受过滤器列表DLC字段 接受所需的数据帧中的最小数据字节数	R/W
6:4	—	这些位被读取为0。写入值应为0。	R/W
7	GAFLIFL0	全局接受过滤器列表信息标签0	R/W
12:8	GAFLRMDP[4:0]	全局接受过滤器列表RX消息缓冲区方向指针 RX消息缓冲区号，用于存储接收到的消息	R/W
14:13	—	这些位被读取为0。写入值应为0。	R/W
15	GAFLRMV	全局接受过滤器列表RX消息缓冲区有效 0：单报文缓冲区方向指针无效1：单报文缓冲区方向指针有效	R/W
31:16	GAFLPTR[15:0]	全局接受过滤器列表指针	R/W

全局接受过滤器列表指针0寄存器用于为全局接受过滤器列表中的每个规则条目配置数据长度代码(DLC)、软件指针、单个消息缓冲区选择和消息缓冲区方向指针。

GAFLDLC[3:0] bits (Global Acceptance Filter List DLC Field)

The GAFLDLC[3:0] bits allow the configuration of a minimum data length code (DLC) value for a message to be accepted by the associated entry in the Global Acceptance Filter List (automatic DLC filter function).

DLC filter process is only passed if the DLC value of the message accepted by an entry in the Global Acceptance Filter List is equal to or higher than the DLC value configured for this associated Global Acceptance Filter List entry. Automatic DLC filter function is disabled for the corresponding rule entry when this field is set to 0.

Table 28.4 shows DLC value that can be configured.

Table 28.4 Configuration of DLC value

Format	DLC[3]	DLC[2]	DLC[1]	DLC[0]	Description
CAN and CANFD	0	0	0	0	DLC of received message = 0 or more (DLC filter check is disabled)
CAN and CANFD	0	0	0	1	DLC of received message = 1 or more
CAN and CANFD	0	0	1	0	DLC of received message = 2 or more
CAN and CANFD	0	0	1	1	DLC of received message = 3 or more
CAN and CANFD	0	1	0	0	DLC of received message = 4 or more
CAN and CANFD	0	1	0	1	DLC of received message = 5 or more
CAN and CANFD	0	1	1	0	DLC of received message = 6 or more
CAN and CANFD	0	1	1	1	DLC of received message = 7 or more
CAN	1	x	x	x	DLC of received message = 8 or more
CANFD	1	0	0	0	DLC of received message = 8 or more*1
CANFD	1	0	0	1	DLC of received message = 12 or more*1
CANFD	1	0	1	0	DLC of received message = 16 or more*1
CANFD	1	0	1	1	DLC of received message = 20 or more*1
CANFD	1	1	0	0	DLC of received message = 24 or more*1
CANFD	1	1	0	1	DLC of received message = 32 or more*1
CANFD	1	1	1	0	DLC of received message = 48 or more*1
CANFD	1	1	1	1	DLC of received message = 64*1

Note 1. This setting is not available in the classical CAN function.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

GAFLIFL0 bit (Global Acceptance Filter List Information Label 0)

The GAFLIFL0 bit allows the configuration of a 2-bit information label that can be attached to a received message accepted by the related Global Acceptance Filter List entry. This bit is a LSB bit of an information label.

You cannot write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to the bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

This bit is stored in Information Label Field[0] (CFDRMFDSTSb.RMIFL[0], CFDRFFDSTSb.RFIFL[0], CFDCFFDCSTS.CFIFL[0]) of the storage location of an incoming message.

GAFLDLC[3:0]位（全局接受过滤器列表DLC字段）

GAFLDLC[3:0]位允许配置消息的最小数据长度代码(DLC)值，以便被全局接受过滤器列表中的相关条目接受（自动DLC过滤器功能）。

仅当全局接受过滤器列表中的条目接受的消息的DLC值等于或高于为此关联的全局接受过滤器列表条目配置的DLC值时，才通过DLC过滤器过程。该字段设置为0时，对应规则条目禁用DLC自动过滤功能。

表28.4显示了可配置的DLC值。

Table 28.4 DLC值的配置

Format	DLC[3]	DLC[2]	DLC[1]	DLC[0]	Description
CAN和CANFD	0	0	0	0	收到消息的DLC=0或更多（DLC过滤器检查已禁用）
CAN和CANFD	0	0	0	1	收到消息的DLC=1或更多
CAN和CANFD	0	0	1	0	收到消息的DLC=2或更多
CAN和CANFD	0	0	1	1	收到消息的DLC=3或更多
CAN和CANFD	0	1	0	0	收到消息的DLC=4或更多
CAN和CANFD	0	1	0	1	收到消息的DLC=5或更多
CAN和CANFD	0	1	1	0	收到消息的DLC=6或更多
CAN和CANFD	0	1	1	1	收到消息的DLC=7或更多
CAN	1	x	x	x	收到消息的DLC=8或更多
CANFD	1	0	0	0	收到消息的DLC=8个或更多*1
CANFD	1	0	0	1	收到消息的DLC=12或更多*1
CANFD	1	0	1	0	收到消息的DLC=16或更多*1
CANFD	1	0	1	1	收到消息的DLC=20或更多*1
CANFD	1	1	0	0	收到消息的DLC=24或更多*1
CANFD	1	1	0	1	收到消息的DLC=32或更多*1
CANFD	1	1	1	0	收到消息的DLC=48或更多*1
CANFD	1	1	1	1	收到消息的DLC=64*1

注1.此设置在经典CAN功能中不可用。

当CFDGAFLECTR.AFLDAE位为0时，不要写入这些位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。

GAFLIFL0位（全局接受过滤器列表信息标签0）

GAFLIFL0位允许配置2位信息标签，该标签可以附加到相关全局接受过滤器列表条目接受的接收消息。该位是信息标签的LSB位。

当CFDGAFLECTR.AFLDAE位为0时，您不能写入该位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入该位。

该位存储在信息标签字段[0]（CFDRMFDSTSb.RMIFL[0]、CFDRFFDSTSb.RFIFL[0]、CFDCFFDCSTS.CFIFL[0])传入消息的存储位置。

GAFLRMDP[4:0] bits (Global Acceptance Filter List RX Message Buffer Direction Pointer)

The GAFLRMDP[4:0] bits allow the configuration of a single reception message buffer as the destination target for a received message that passes the acceptance check of the related Global Acceptance Filter List entry. The value entered is the single destination message buffer number.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

CFDRMNB.NRXMB[5:0] is the value entered in the RX Message Buffer Number Register to configure the number of RX message buffers. The value to be entered in CFDGAFLP0r.GAFLRMDP[4:0] bits should only be between 0x00 and CFDMNB.NMB[5:0] to 1 less.

If CFDRMNB.NRXMB[5:0] = 0x00, the GAFLRMV bit should be configured as 0.

GAFLRMV bit (Global Acceptance Filter List RX Message Buffer Valid)

The GAFLRMV bit allows the enabling or disabling of a single reception message buffer as the target for a received message that passes the acceptance check of the related Global Acceptance Filter List entry.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

GAFLPTR[15:0] bits (Global Acceptance Filter List Pointer)

The GAFLPTR[15:0] bits allow the configuration of a 16-bit pointer to be attached to a received message accepted by the related Global Acceptance Filter List entry. The pointer is added during message storage in the Message Buffer area and can be used by the application as a support function. The pointer information can be used for example, to support PDU Identifier allocation for the received message in AUTOSAR systems.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

28.2.23 CFDGAFLP1r : Global Acceptance Filter List Pointer 1 Registers (r = 1 to 16)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x012C + 0x0010 × (r - 1)

Bit position:	31																								8							1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GAFLFDP8	—	—	—	—	—	—	GAFLFDP1	GAFLFDP0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	GAFLFDP0	Global Acceptance Filter List FIFO Direction Pointer FIFO direction pointer bits for received message storage 0: Disable RX FIFO 0 as target for reception 1: Enable RX FIFO 0 as target for reception	R/W
1	GAFLFDP1	Global Acceptance Filter List FIFO Direction Pointer FIFO direction pointer bits for received message storage 0: Disable RX FIFO 1 as target for reception 1: Enable RX FIFO 1 as target for reception	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	GAFLFDP8	Global Acceptance Filter List FIFO Direction Pointer FIFO direction pointer bits for received message storage 0: Disable Common FIFO as target for reception 1: Enable Common FIFO as target for reception	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

GAFLRMDP[4:0]位（全局接受过滤器列表RX消息缓冲区方向指针）

GAFLRMDP[4:0]位允许将单个接收消息缓冲区配置为接收消息的目标目标，该消息通过相关全局接受过滤器列表条目的接受检查。输入的值是单个目标消息缓冲区号。

当CFDGAFLECTR.AFLDAE位为0时，不要写入这些位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。

CFDRMNB.NRXMB[5:0]是在RX消息缓冲区编号寄存器中输入的值，用于配置RX消息缓冲区的数量。要在CFDGAFLP0r.GAFLRMDP[4:0]位中输入的值只能在0x00和CFDMNB.NMB[5:0]之间减去1。

如果CFDRMNB.NRXMB[5:0]=0x00，则GAFLRMV位应配置为0。

GAFLRMV位（全局接受过滤器列表RX消息缓冲区有效）

GAFLRMV位允许启用或禁用单个接收消息缓冲区作为通过相关全局接受过滤器列表条目的接受检查的接收消息的目标。

当CFDGAFLECTR.AFLDAE位为0时，不要写入这些位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。

GAFLPTR[15:0]位（全局接受过滤器列表指针）

GAFLPTR[15:0]位允许配置一个16位指针，以附加到相关全局接受过滤器列表条目所接受的接收消息。该指针是在消息缓冲区中的消息存储期间添加的，并且可以由应用程序用作支持功能。例如，指针信息可用于支持AUTOSAR系统中接收到的消息的PDU标识符分配。

当CFDGAFLECTR.AFLDAE位为0时，不要写入这些位。

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。

28.2.23 CFDGAFLP1r：全局验收过滤器列表指针1寄存器（r=1到16）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x012C + 0x0010 × (r - 1)

Bit position:	31																								8							1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GAFLFDP8	—	—	—	—	—	—	GAFLFDP1	GAFLFDP0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	GAFLFDP0	全局验收过滤器列表FIFO方向指针 用于接收消息存储的FIFO方向指针位 0：禁用RXFIFO0作为接收目标1：启用RXFIFO0作为接收目标	R/W
1	GAFLFDP1	全局验收过滤器列表FIFO方向指针 用于接收消息存储的FIFO方向指针位 0：禁用RXFIFO1作为接收目标1：启用RXFIFO1作为接收目标	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
8	GAFLFDP8	全局验收过滤器列表FIFO方向指针 用于接收消息存储的FIFO方向指针位 0：禁用CommonFIFO作为接收目标1：启用CommonFIFO作为接收目标	R/W
31:9	—	这些位被读取为0。写入值应为0。	R/W

The Global Acceptance Filter List Pointer 1 registers are used to configure the FIFO direction pointer fields in each Rule Entry of the Global Acceptance Filter List.

GAFLFDP8, GAFLFDP1, GAFLFDP0 bits (Global Acceptance Filter List FIFO Direction Pointer)

These bits allow the configuration of FIFO Buffers as the target for a received message passing the acceptance check of the related Global Acceptance Filter List entry. Each bit of the GAFLFDP8, GAFLFDP1, GAFLFDP0 is configuring a dedicated FIFO.

Users cannot write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

For storage in Common FIFO, target for reception can only be those Common FIFO Buffers that are configured as RX FIFO.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

Users should only configure up to 2 destination FIFO Buffers or 1 destination FIFO Buffers plus one RX Message Buffer.

28.2.24 CFDRMNB : RX Message Buffer Number Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0030

Bit position:	31																				10	8		5		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RMPLS[2:0]		—	—	NRXMB[5:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	NRXMB[5:0]	Number of RX Message Buffers	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
10:8	RMPLS[2:0]	Reception Message Buffer Payload Data Size 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
31:11	—	These bits are read as 0. The write value should be 0.	R/W

The RX Message Buffer Number register is used to configure the total number of RX message buffers allocated to channels.

NRXMB[5:0] bits (Number of RX Message Buffers)

The NRXMB[5:0] bits are used to configure the number of RX message buffers.

Only write to these bits when the CANFD module is in GL_RESET mode.

Enter only values between 0 and 32 inclusive, with 0x00 indicating that no RX message buffer is allocated.

RMPLS[2:0] bits (Reception Message Buffer Payload Data Size)

The RMPLS[2:0] bits are used to configure the message buffer payload data size.

Only write to these bits when the CANFD module is in GL_RESET mode.

全局接受过滤器列表指针1寄存器用于配置每个规则中的FIFO方向指针字段
全局接受过滤器列表的条目。

GAFLFDP8、GAFLFDP1、GAFLFDP0位（全局接受过滤器列表FIFO方向指针）

这些位允许将FIFO缓冲区配置为接收到的消息通过相关全局接受过滤器列表条目的接受检查的目标。GAFLFDP8、GAFLFDP1、GAFLFDP0的每一位都在配置一个专用的FIFO。

当CFDGAFLECTR.AFLDAE位为0时，用户不能写入这些位。

对于存储在CommonFIFO中，接收目标只能是那些配置为RX的CommonFIFO缓冲区FIFO.

仅当相关CANFD通道处于CH_RESET或CH_HALT模式时才写入这些位。

用户最多只能配置2个目标FIFO缓冲区或1个目标FIFO缓冲区加上1个RX消息缓冲区。

28.2.24 CFDRMNB:RX消息缓冲区编号寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0030

Bit position:	31																				10	8		5		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RMPLS[2:0]		—	—	NRXMB[5:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	NRXMB[5:0]	RX消息缓冲区的数量	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
10:8	RMPLS[2:0]	接收消息缓冲区有效负载数据大小 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
31:11	—	这些位被读取为0。写入值应为0。	R/W

RX消息缓冲区编号寄存器用于配置分配给通道的RX消息缓冲区的总数。

NRXMB[5:0]位（RX消息缓冲区的数量）

NRXMB[5:0]位用于配置RX消息缓冲区的数量。

仅当CANFD模块处于GL_RESET模式时才写入这些位。

仅输入介于0和32之间的值，其中0x00表示未分配RX消息缓冲区。

RMPLS[2:0]位（接收消息缓冲区有效负载数据大小）

RMPLS[2:0]位用于配置消息缓冲区有效负载数据大小。

仅当CANFD模块处于GL_RESET模式时才写入这些位。

28.2.25 CFDRMND : RX Message Buffer New Data Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0034

Bit position:	31																													0
Bit field:	RMNS[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	RMNS[31:0]	RX Message Buffer New Data Status 0: New data not stored in corresponding RX message buffer 1: New data stored in corresponding RX message buffer	R/W

The RX Message Buffer New Data Status Register specifies the new data storage status of the RX message buffers.

RMNS[31:0] bits (RX Message Buffer New Data Status)

The RMNS[31:0] bits indicate the status of new data for the corresponding RX message buffer. RMNS bit [0] corresponds to RX message buffer [0] and so on.

The bit position of CFDRMND corresponds to the buffer number of RXMB.

Do not write to these bits when the CANFD module is in GL_RESET or GL_SLEEP mode. Writing 1 has no effect.

These bits cannot be cleared when message storage in the corresponding RX message buffer is in progress.
Do not use the bit clear instruction to clear these bits. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

These bits are set automatically when storage of new messages are in the corresponding RX message buffer. These bits are cleared by writing 0. These bits are cleared automatically when the CANFD module is in GL_RESET mode.

When CFDRMNB.RMPLS = 000b (maximum 8 bytes payload), the duration of message storage is 6 PCLKB cycles.

When CFDRMNB.RMPLS > 000b, the duration of message storage is 6 PCLKB cycles + 1 for each 4 bytes (maximum of 20 PCLKB cycles for 64 bytes).

Note: This feature is not available in the classical CAN function.

28.2.26 CFDRFCCa : RX FIFO Configuration/Control Registers a (a = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x003C + 0x04 × a

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RFIGCV[2:0]			RFIM	—	RFDC[2:0]			—	RFPLS[2:0]			—	—	RFIE	RFE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFE	RX FIFO Enable 0: FIFO disabled 1: FIFO enabled	R/W

28.2.25 CFDRMND:RX消息缓冲区新数据寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0034

Bit position:	31																													0
Bit field:	RMNS[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	RMNS[31:0]	RX消息缓冲区新数据状态 0：新数据未存储在相应的RX报文缓冲区中1：新数据存储在相应的RX报文缓冲区中	R/W

RX报文缓冲区新数据状态寄存器指定RX报文缓冲区的新数据存储状态。

RMNS[31:0]位（RX报文缓冲区新数据状态）

RMNS[31:0]位指示相应RX消息缓冲区的新数据状态。RMNS位[0]对应于RX消息缓冲区[0]等等。

CFDRMND的位位置对应于RXMB的缓冲区号。

当CANFD模块处于GL_RESET或GL_SLEEP模式时，不要写入这些位。写1无效。

当相应RX消息缓冲区中的消息存储正在进行时，这些位不能被清除。
不要使用位清除指令来清除这些位。使用MOV指令确保只清除指定位。其他位保持1。

当新消息存储在相应的RX消息缓冲区中时，这些位会自动设置。这些位通过写0清除。当CANFD模块处于GL_RESET模式时，这些位会自动清除。

当CFDRMNB.RMPLS=000b（最大8字节有效载荷）时，消息存储的持续时间为6个PCLKB周期。

当CFDRMNB.RMPLS>000b时，消息存储的持续时间为6个PCLKB周期+每4个字节1个（64个字节最多20个PCLKB周期）。

Note: 此功能在经典CAN功能中不可用。

28.2.26 CFDRFCCa:RXFIFO配置控制寄存器a(a=0to1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x003C + 0x04 × a

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RFIGCV[2:0]			RFIM	—	RFDC[2:0]			—	RFPLS[2:0]			—	—	RFIE	RFE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFE	RX FIFO Enable 0：禁用FIFO1： 启用FIFO	R/W

Bit	Symbol	Function	R/W
1	RFIE	RX FIFO Interrupt Enable 0: FIFO interrupt generation disabled 1: FIFO interrupt generation enabled	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
6:4	RFPLS[2:0]*1	Rx FIFO Payload Data Size Configuration 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
10:8	RFDC[2:0]	RX FIFO Depth Configuration 0 0 0: FIFO Depth = 0 message 0 0 1: FIFO Depth = 4 messages 0 1 0: FIFO Depth = 8 messages 0 1 1: FIFO Depth = 16 messages 1 0 0: FIFO Depth = 32 essages 1 0 1: FIFO Depth = 48 messages 1 1 0: Reserved 1 1 1: Reserved	R/W
11	—	This bit is read as 0. The write value should be 0.	R
12	RFIM	RX FIFO Interrupt Mode 0: Interrupt generated when RX FIFO counter reaches RFIGCV value from values smaller than RFIGCV 1: Interrupt generated at the end of every received message storage	R/W
15:13	RFIGCV[2:0]	RX FIFO Interrupt Generation Counter Value 0 0 0: Interrupt generated when FIFO is 1/8th full 0 0 1: Interrupt generated when FIFO is 1/4th full 0 1 0: Interrupt generated when FIFO is 3/8th full 0 1 1: Interrupt generated when FIFO is 1/2 full 1 0 0: Interrupt generated when FIFO is 5/8th full 1 0 1: Interrupt generated when FIFO is 3/4th full 1 1 0: Interrupt generated when FIFO is 7/8th full 1 1 1: Interrupt generated when FIFO is full	R/W
16	—	These bits are read as 0. The write value should be 0.	R
31:17	—	These bits are read as 0. The write value should be 0.	R

Note 1. These bits are not available in the classical CAN function.

The RX FIFO Configuration/Control Registers are used to configure and control the two RX FIFOs.

RFE bit (RX FIFO Enable)

The RFE bit enables the FIFO. When this bit is set to 0, the RX FIFO is cleared to empty.

Only write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode.

This bit can only be set if the configured FIFO depth is greater than 0x000 (CFDRFCCa.RFDC > 0x000) and less than 0x110.

Set the RFE bit with a separate write access to the CFDRFCCa register, after all the other bits in the CFDRFCCa register are set.

This bit is cleared automatically when the CANFD module is in GL_RESET mode.

RFIE bit (RX FIFO Interrupt Enable)

The RFIE bit enables generation of the FIFO interrupt.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

Bit	Symbol	Function	R/W
1	RFIE	RXFIFO中断使能 0：禁用FIFO中断生成1：启用FIFO中断生成	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
6:4	RFPLS[2:0]*1	RxFIFO有效负载数据大小配置 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
7	—	该位读取为0。写入值应为0。	R/W
10:8	RFDC[2:0]	RXFIFO深度配置 000：FIFO深度=0条消息001：FIFO深度=4条消息010：FIFO深度=8条消息011：FIFO深度=16条消息100：FIFO深度=32条消息101：FIFO深度=48条消息110：保留111：保留	R/W
11	—	该位读取为0。写入值应为0。	R
12	RFIM	RXFIFO中断模式 0：当RXFIFO计数器从小于RFIGCV的值到达RFIGCV值时产生中断 1：在每个接收到的消息存储结束时产生中断	R/W
15:13	RFIGCV[2:0]	RXFIFO中断产生计数器值 000：FIFO1第8满时产生中断001：FIFO1第4满时产生中断010：FIFO3第8满时产生中断011：FIFO12满时产生中断100：当FIFO为5第8个满时产生中断101：当FIFO第3个满时产生中断110：当FIFO第8个满时产生中断111：当FIFO满时产生中断	R/W
16	—	这些位被读取为0。写入值应为0。	R
31:17	—	这些位被读取为0。写入值应为0。	R

注1.这些位在经典CAN功能中不可用。

RXFIFO配置控制寄存器用于配置和控制两个RXFIFO。

RFE bit (RX FIFO Enable)

RFE位使能FIFO。当该位设置为0时，RXFIFO被清空。

仅当CANFD模块处于GL_HALT或GL_OPERATION模式时写入该位。

仅当配置的FIFO深度大于0x000(CFDRFCCa.RFDC>0x000)且小于0x110时，才能设置该位。

在设置CFDRFCCa寄存器中的所有其他位之后，通过对CFDRFCCa寄存器的单独写访问来设置RFE位。

当CANFD模块处于GL_RESET模式时，该位会自动清零。

RFIE位（RXFIFO中断允许）

RFIE位使能FIFO中断的产生。

CANFD模块处于GL_SLEEP模式时不要写入该位。

RFPLS[2:0] bits (Rx FIFO Payload Data Size Configuration)

The RFPLS[2:0] bits define the message data payload allocation in the RAM.

This is the maximum number of bytes which can be received by this FIFO.

Only write to these bits when the CANFD module is in GL_RESET mode.

Note: These bits are not available in the classical CAN function.

RFDC[2:0] bits (RX FIFO Depth Configuration)

The RFDC[2:0] bits select the depth of the FIFO in terms of the number of messages. If the FIFO depth is configured to 0 messages, the FIFO cannot be used.

Only write to these bits when the CANFD module is in GL_RESET mode.

RFIM bit (RX FIFO Interrupt Mode)

The RFIM bit selects the interrupt generation condition for the FIFO.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

Only write to this bit when the CANFD module is in GL_RESET mode.

RFIGCV[2:0] bits (RX FIFO Interrupt Generation Counter Value)

The RFIGCV[2:0] bits select the counter value of the FIFO for generation of FIFO interrupts. These values represent fractions of the FIFO depth for which an interrupt is generated.

Do not write to these bits when the CANFD module is in GL_SLEEP mode.

The setting of the RFIGCV[2:0] bits should be synchronized with the RFDC[2:0] bits.

Only write to these bits when the CANFD module is in GL_RESET mode.

28.2.27 CFDRFSTSa : RX FIFO Status Registers a (a = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0044 + 0x04 × a

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	RFMC[5:0]						—	—	—	—	RFIF	RFMLT	RFFLL	RFEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	RFEMP	RX FIFO Empty 0: FIFO not empty 1: FIFO empty	R
1	RFFLL	RX FIFO Full 0: FIFO not full 1: FIFO full	R
2	RFMLT	RX FIFO Message Lost 0: No message lost in FIFO 1: FIFO message lost	R/W
3	RFIF	RX FIFO Interrupt Flag 0: FIFO interrupt condition not satisfied 1: FIFO interrupt condition satisfied	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

RFPLS[2:0]位（RxFIFO有效负载数据大小配置）

RFPLS[2:0]位定义RAM中的消息数据有效负载分配。

这是该FIFO可以接收的最大字节数。

仅当CANFD模块处于GL_RESET模式时才写入这些位。

Note: 这些位在经典CAN功能中不可用。

RFDC[2:0]位（RXFIFO深度配置）

RFDC[2:0]位根据消息数量选择FIFO的深度。如果FIFO深度配置为0消息，则无法使用FIFO。

仅当CANFD模块处于GL_RESET模式时才写入这些位。

RFIM位（RXFIFO中断模式）

RFIM位选择FIFO的中断产生条件。

CANFD模块处于GL_SLEEP模式时不要写入该位。

仅当CANFD模块处于GL_RESET模式时写入该位。

RFIGCV[2:0]位（RXFIFO中断生成计数器值）

RFIGCV[2:0]位选择FIFO的计数器值以生成FIFO中断。这些值代表产生中断的FIFO深度的分数。

当CANFD模块处于GL_SLEEP模式时，不要写入这些位。

RFIGCV[2:0]位的设置应与RFDC[2:0]位同步。

仅当CANFD模块处于GL_RESET模式时才写入这些位。

28.2.27 CFDRFSTSa：RXFIFO状态寄存器a（a=0到1）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0044 + 0x04 × a

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	RFMC[5:0]						—	—	—	—	RFIF	RFMLT	RFFLL	RFEMP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	RFEMP	RX FIFO Empty 0：FIFO非空1：FIFO空	R
1	RFFLL	RX FIFO Full 0：FIFO未满1：FIFO已满	R
2	RFMLT	RXFIFO消息丢失 0：FIFO中没有消息丢失1：FIFO消息丢失	R/W
3	RFIF	RXFIFO中断标志 0：不满足FIFO中断条件1：满足FIFO中断条件	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
13:8	RFMC[5:0]	RX FIFO Message Count Number of messages stored in FIFO	R
31:14	—	These bits are read as 0. The write value should be 0.	R/W

The RX FIFO Status Registers show the status of messages stored in the corresponding FIFO buffers.

RFEMP bit (RX FIFO Empty)

The RFEMP bit is set automatically when:

- The RFMC bit is 0
- RX FIFO is disabled by setting the CFDRFCCa.RFE bit to 0
- The CANFD module is in GL_RESET mode.

The RFEMP bit is cleared automatically when the first message is stored in the RX FIFO buffer.

RFFLL bit (RX FIFO Full)

The RFFLL bit is set automatically when the number of CAN messages stored in the FIFO buffer matches the configured FIFO depth.

The RFFLL is cleared automatically when:

- The number of CAN messages stored in the FIFO buffer is less than the configured FIFO depth
- RX FIFO is disabled by setting the CFDRFCCa.RFE bit to 0
- The CANFD module is in GL_RESET mode.

RFMLT bit (RX FIFO Message Lost)

Only write to the RFMLT bit when CANFD module is in GL_HALT or GL_OPERATION mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically whenever a message is lost due to attempted storage when the FIFO buffer is already full. If a set from the CAN channel occurs simultaneously with a clear by a write access, then the bit is set.

The bit is cleared:

- By writing 0 to it
- When the CANFD module is in GL_RESET mode.

RFIF bit (RX FIFO Interrupt Flag)

The RFIF bit is set automatically when the configured interrupt condition is satisfied. This bit is not automatically cleared when the RX FIFO buffer is disabled.

Only write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

If a set from the CAN channel occurs simultaneously with a clear by a write access, then this bit is set.

The bit is cleared by writing 0 to it. The bit is also cleared when CANFD module is in GL_RESET mode.

RFMC[5:0] bits (RX FIFO Message Count)

The RFMC[5:0] bits indicate the number of CAN messages stored in the RX FIFO buffer that can be read by the CPU.

These bits are cleared automatically when the FIFO is disabled and when the CANFD module is in GL_RESET mode.

Bit	Symbol	Function	R/W
13:8	RFMC[5:0]	RXFIFO消息计数 存储在FIFO中的消息数	R
31:14	—	这些位被读取为0。写入值应为0。	R/W

RXFIFO状态寄存器显示存储在相应FIFO缓冲区中的消息的状态。

RFEMP bit (RX FIFO Empty)

RFEMP位在以下情况下自动设置：

●RFMC位为0

●通过将CFDRFCCa.RFE位设置为0来禁用RXFIFO

●CANFD模块处于GL_RESET模式。

当第一条消息存储在RXFIFO缓冲区中时，RFEMP位会自动清零。

RFFLL bit (RX FIFO Full)

当存储在FIFO缓冲区中的CAN报文数量与配置的匹配时，RFFLL位会自动设置
FIFO depth.

RFFLL在以下情况下自动清除：

●FIFO缓冲区中存储的CAN报文数小于配置的FIFO深度

●通过将CFDRFCCa.RFE位设置为0来禁用RXFIFO

●CANFD模块处于GL_RESET模式。

RFMLT位（RXFIFO消息丢失）

仅当CANFD模块处于GL_HALT或GL_OPERATION模式时才写入RFMLT位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

当FIFO缓冲区已满时，每当由于尝试存储而导致消息丢失时，该位会自动设置。如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

该位被清除：

●写入0

●CANFD模块处于GL_RESET模式时。

RFIF位（RXFIFO中断标志 ）

当配置的中断条件满足时，RFIF位自动置位。当RXFIFO缓冲器被禁用时，该位不会自动清除。

仅当CANFD模块处于GL_HALT或GL_OPERATION模式时写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

如果来自CAN通道的设置与写访问清除同时发生，则设置该位。

该位通过向其写入0来清除。当CANFD模块处于GL_RESET模式时，该位也会被清除。

RFMC[5:0]位（RXFIFO消息计数）

RFMC[5:0]位指示存储在RXFIFO缓冲区中可供CPU读取的CAN报文数量。

当FIFO被禁用并且CANFD模块处于GL_RESET模式时，这些位会自动清除。

28.2.28 CFDRFPCTRa : RX FIFO Pointer Control Registers a (a = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x004C + 0x04 × a

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	RFPC[7:0]	RX FIFO Pointer Control Increments read pointer of the corresponding RX FIFO buffers	W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The RX FIFO Pointer Control Registers can be used to increment the read pointer of the corresponding RX FIFO buffers.

RFPC bits (RX FIFO Pointer Control)

When the value 0xFF is written to the RFPC bits, the pointer of the corresponding RX FIFO buffer is moved to the next FIFO entry. Only write 0xFF to these registers when the corresponding RX FIFO buffer is enabled and not empty.

The read value from these bits is always 0x00.

Only write to these bits when the CANFD module is in GL_HALT or GL_OPERATION mode.

Do not write to the RX FIFO Pointer Control registers when DMA is enabled.

28.2.29 CFDCFCC : Common FIFO Configuration/Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0054

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFITT[7:0]								CFDC[2:0]			—	—	—	CFTML[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CFIGCV[2:0]			CFIM	CFITR	CFITSS	—	CFM	—	CFPLS[2:0]			—	CFTXIE	CFRXIE	CFE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFE	Common FIFO Enable 0: FIFO disabled 1: FIFO enabled	R/W
1	CFRXIE	Common FIFO RX Interrupt Enable 0: FIFO interrupt generation disabled for Frame RX 1: FIFO interrupt generation enabled for Frame RX	R/W
2	CFTXIE	Common FIFO TX Interrupt Enable 0: FIFO interrupt generation disabled for Frame TX 1: FIFO interrupt generation enabled for Frame TX	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W

28.2.28 CFDRFPCTRa:RXFIFO指针控制寄存器a(a=0to1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x004C + 0x04 × a

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFPC[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	RFPC[7:0]	RXFIFO指针控制 增加相应RXFIFO缓冲区的读指针	W
31:8	—	这些位被读取为0。写入值应为0。	R/W

RXFIFO指针控制寄存器可用于递增相应RXFIFO缓冲区的读指针。

RFPC位（RXFIFO指针控制）

当值0xFF写入RFPC位时，相应的RXFIFO缓冲区的指针移动到下一个
先进先出入口。仅当相应的RXFIFO缓冲区启用且不为空时，才将0xFF写入这些寄存器。

从这些位读取的值始终为0x00。

仅当CANFD模块处于GL_HALT或GL_OPERATION模式时才写入这些位。

启用DMA时不要写入RXFIFO指针控制寄存器。

28.2.29 CFDCFCC:通用FIFO配置控制寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0054

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFITT[7:0]								CFDC[2:0]			—	—	—	CFTML[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CFIGCV[2:0]			CFIM	CFITR	CFITSS	—	CFM	—	CFPLS[2:0]			—	CFTXIE	CFRXIE	CFE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFE	通用FIFO使能 0：禁用FIFO1： 启用FIFO	R/W
1	CFRXIE	通用FIFORX中断使能 0：禁用帧RX的FIFO中断生成1：启用帧RX的FIFO中 断生成	R/W
2	CFTXIE	通用FIFOTX中断使能 0：禁用帧TX的FIFO中断生成1：启用帧TX的FIFO中 断生成	R/W
3	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
6:4	CFPLS[2:0]*1	Common FIFO Payload Data Size Configuration 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
8	CFM	Common FIFO Mode 0: RX FIFO mode 1: TX FIFO mode	R/W
9	—	This bit is read as 0. The write value should be 0.	R/W
10	CFITSS	Common FIFO Interval Timer Source Select 0: Reference clock (× 1 / × 10 period) 1: Bit time clock of related channel (FIFO is linked to fixed channel)	R/W
11	CFITR	Common FIFO Interval Timer Resolution 0: Reference clock period × 1 1: Reference clock period × 10	R/W
12	CFIM	Common FIFO Interrupt Mode 0: RX FIFO mode: RX interrupt generated when Common FIFO counter reaches CFIGCV value from a lower value TX FIFO mode: TX interrupt generated when Common FIFO transmits the last message successfully 1: RX FIFO mode: RX interrupt generated at the end of every received message storage TX FIFO mode: interrupt generated for every successfully transmitted message	R/W
15:13	CFIGCV[2:0]	Common FIFO Interrupt Generation Counter Value 0 0 0: Interrupt generated when FIFO is 1/8th full 0 0 1: Interrupt generated when FIFO is 1/4th full 0 1 0: Interrupt generated when FIFO is 3/8th full 0 1 1: Interrupt generated when FIFO is 1/2 full 1 0 0: Interrupt generated when FIFO is 5/8th full 1 0 1: Interrupt generated when FIFO is 3/4th full 1 1 0: Interrupt generated when FIFO is 7/8th full 1 1 1: Interrupt generated when FIFO is full	R/W
17:16	CFTML[1:0]	Common FIFO TX Message Buffer Link Transmission scan link position of the corresponding channel	R/W
20:18	—	These bits are read as 0. The write value should be 0.	R/W
23:21	CFDC[2:0]	Common FIFO Depth Configuration 0 0 0: FIFO Depth = 0 message 0 0 1: FIFO Depth = 4 messages 0 1 0: FIFO Depth = 8 messages 0 1 1: FIFO Depth = 16 messages 1 0 0: FIFO Depth = 32 messages 1 0 1: FIFO Depth = 48 messages 1 1 0: FIFO Depth = Reserved 1 1 1: FIFO Depth = Reserved	R/W
31:24	CFITT[7:0]	Common FIFO Interval Transmission Time Delay the start of transmission from the FIFO if configured in TX mode, delay is a multiple of basic Interval Timer Clock Source unit	R/W

Note 1. These bits are not available in the classical CAN function.

CFE bit (Common FIFO Enable)

The CFE bit enables the FIFO when set. FIFO is disabled when this bit is cleared.

This bit can also be used, by clearing it, to abort transmission from Common FIFO when configured in TX mode, or to stop reception into the Common FIFO in RX mode.

Bit	Symbol	Function	R/W
6:4	CFPLS[2:0]*1	通用FIFO有效负载数据大小配置 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
7	—	该位读取为0。写入值应为0。	R/W
8	CFM	普通先进先出模式 0: RX FIFO mode 1: TX FIFO mode	R/W
9	—	该位读取为0。写入值应为0。	R/W
10	CFITSS	通用FIFO间隔定时器源选择 0：参考时钟（×1×10周期）1：相关通道的位时钟（FIFO链接到固定通道）	R/W
11	CFITR	通用FIFO间隔定时器分辨率 0：参考时钟周期×11：参考时钟周期×10	R/W
12	CFIM	通用FIFO中断模式 0：RXFIFO模式：CommonFIFO计数器从较低值到达CFIGCV值时产生RX中断 TXFIFO模式：CommonFIFO成功发送最后一条报文时产生TX中断 1：RXFIFO模式：在每个接收到的消息存储结束时产生RX中断TXFIFO模式：在每个成功发送的消息产生中断	R/W
15:13	CFIGCV[2:0]	通用FIFO中断生成计数器值 000：FIFO1第8满时产生中断001：FIFO1第4满时产生中断010：FIFO3第8满时产生中断011：FIFO12满时产生中断100：当FIFO为5第8个满时产生中断101：当FIFO第3个满时产生中断110：当FIFO第8个满时产生中断111：当FIFO满时产生中断	R/W
17:16	CFTML[1:0]	通用FIFOTX消息缓冲区链接 对应通道的传输扫描链接位置	R/W
20:18	—	这些位被读取为0。写入值应为0。	R/W
23:21	CFDC[2:0]	通用FIFO深度配置 000：FIFO深度=0条消息001：FIFO深度=4条消息010：FIFO深度=8条消息011：FIFO深度=16条消息100：FIFO深度=32条消息101：FIFO深度=48条消息110：FIFO深度=保留111：FIFO深度=保留	R/W
31:24	CFITT[7:0]	公共FIFO间隔传输时间 如果配置为TX模式，则延迟从FIFO开始传输，延迟是基本间隔定时器时钟源单元的倍数	R/W

注1.这些位在经典CAN功能中不可用。

CFE bit (Common FIFO Enable)

CFE位在设置时启用FIFO。当该位清零时，FIFO被禁用。

当配置为TX模式时，通过清零该位也可用于中止从CommonFIFO发送，或在RX模式下停止接收到CommonFIFO。

Only write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode and the related CANFD channel is not in CH_RESET mode for FIFOs configured as TX FIFO.

This bit can only be set if the configured FIFO depth is greater than 0x000 (CFDCFCC.CFDC > 0x000 and less than 0x110 (0x110 > CFDCFCC.CFDC > 0x000).

Set the CFE bit with a separate write access to the CFDCFCC register, after all the other bits in this register are set.

This bit is cleared automatically when the CANFD module is in GL_RESET mode.

This bit is also cleared automatically when the related channel is in CH_RESET mode if the FIFO is configured in TX mode.

CFRXIE bit (Common FIFO RX Interrupt Enable)

The CFRXIE bit enables generation of FIFO interrupts when the interrupt flag is set after reception of a frame in the corresponding FIFO buffer.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

CFTXIE bit (Common FIFO TX Interrupt Enable)

The CFTXIE bit enables generation of common FIFO interrupts when the interrupt flag is set after transmission of a frame from the corresponding FIFO buffer.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

CFPLS[2:0] bits (Common FIFO Payload Data Size Configuration)

The CFPLS[2:0] bits define the message data payload allocation in the RAM. This is the maximum number of bytes which can be received or transmitted by the FIFO buffer.

For details, see section 28.6. FIFO Buffers and Normal Message Buffer Configuration.

Only write to this bit when the CANFD module is in GL_RESET mode.

Note: These bits are not available in the classical CAN function.

CFM bit (Common FIFO Mode)

The CFM bit selects the mode of the FIFO. When a hardware reset is applied, all the Common FIFO buffers are configured in RX FIFO mode.

Do not write to these bits in GL_OPERATION or GL_SLEEP mode.

Only write to these bits when the CANFD module is in GL_RESET mode.

CFITSS bit (Common FIFO Interval Timer Source Select)

The CFITSS bit selects the basic clock source for the Interval Transmission Timer.

Do not write to this bit when the CANFD module is in GL_SLEEP mode. In addition, do not write to this bit when the CFE bit is set to 1.

Do not write 1 to this bit when CANFD communication is used.*1

Note: The bit time clock can vary depending on the nominal and data rate bit configuration.

Note 1. This feature is not available in the classical CAN function.

CFITR bit (Common FIFO Interval Timer Resolution)

The CFITR bit selects the resolution of the reference clock for the Interval Transmission Timer (peripheral clock is the source for the reference clock).

Do not write to this bit when the CANFD module is in GL_SLEEP mode. Also, do not write to this bit when the CFE bit is set to 1.

CFIM bit (Common FIFO Interrupt Mode)

The CFIM bit selects the interrupt generation condition for the FIFO buffer.

Do not write to this bit in GL_SLEEP mode.

仅当CANFD模块处于GL_HALT或GL_OPERATION模式且相关CANFD通道未处于CH_RESET模式（对于配置为TXFIFO的FIFO）时才写入该位。

仅当配置的FIFO深度大于0x000（CFDCFCC.CFDC>0x000且小于0x110（0x110>CFDCFCC.CFDC>0x000）时，才能设置该位。

在设置该寄存器中的所有其他位之后，通过对CFDCFCC寄存器的单独写访问来设置CFE位。

当CANFD模块处于GL_RESET模式时，该位会自动清零。

如果FIFO配置为TX模式，则当相关通道处于CH_RESET模式时，该位也会自动清零。

CFRXIE位（通用FIFORX中断使能）

当在相应的FIFO缓冲区中接收到帧后设置中断标志时，CFRXIE位允许生成FIFO中断。

CANFD模块处于GL_SLEEP模式时不要写入该位。

CFTXIE位（通用FIFOTX中断使能）

当从相应的FIFO缓冲区传输帧后设置中断标志时，CFTXIE位使能通用FIFO中断的生成。

CANFD模块处于GL_SLEEP模式时不要写入该位。

CFPLS[2:0]位（通用FIFO有效负载数据大小配置）

CFPLS[2:0]位定义RAM中的消息数据有效负载分配。这是FIFO缓冲区可以接收或发送的最大字节数。

有关详细信息，请参阅第28.6节。FIFO缓冲区和正常消息缓冲区配置。

仅当CANFD模块处于GL_RESET模式时写入该位。

Note: 这些位在经典CAN功能中不可用。

CFM bit (Common FIFO Mode)

CFM位选择FIFO的模式。应用硬件复位时，所有通用FIFO缓冲区都配置为RXFIFO模式。

不要在GL_OPERATION或GL_SLEEP模式下写入这些位。

仅当CANFD模块处于GL_RESET模式时才写入这些位。

CFITSS位（通用FIFO间隔定时器源选择）

CFITSS位选择间隔传输定时器的基本时钟源。

CANFD模块处于GL_SLEEP模式时不要写入该位。此外，当CFE位设置为1时，请勿写入该位。

使用CANFD通信时，请勿向该位写入1。*1

Note: 位时钟可以根据标称和数据速率位配置而变化。

注1.此功能在经典CAN功能中不可用。

CFITR位（通用FIFO间隔定时器分辨率）

CFITR位为间隔传输定时器选择参考时钟的分辨率（外围时钟是参考时钟的来源）。

CANFD模块处于GL_SLEEP模式时不要写入该位。此外，当CFE位设置为1时，请勿写入该位。

CFIM位（通用FIFO中断模式）

CFIM位选择FIFO缓冲器的中断产生条件。

不要在GL_SLEEP模式下写入该位。

Only write to this bit when the CANFD module is in GL_RESET mode.

CFIGCV[2:0] bits (Common FIFO Interrupt Generation Counter Value)

The CFIGCV[2:0] bits select the message counter value for the generation of FIFO interrupts. These values represent fractions of the FIFO depth at which the interrupt is to be generated.

Do not write to these bits when the CANFD module is in GL_SLEEP mode.

The setting of these bits should be synchronized with the CFDC[2:0] bits.

Only write to these bits when the CANFD module is in GL_RESET mode.

CFTML[1:0] bits (Common FIFO TX Message Buffer Link)

The CFTML[1:0] bits select the normal transmit message buffer position where the TX FIFO is linked to, for transmission scanning.

Do not write to these bits in GL_OPERATION or GL_SLEEP mode.

Only write to this bit when the CANFD module is in GL_RESET mode.

CFDC[2:0] bits (Common FIFO Depth Configuration)

The CFDC[2:0] bits select the depth of the common FIFO in terms of the number of messages. If the FIFO depth is configured to 0 message, the FIFO cannot be used.

Only write to these bits when the CANFD module is in GL_RESET mode.

CFITT[7:0] bits (Common FIFO Interval Transmission Time)

The CFITT[7:0] bits select the delay in the start of transmission for all messages transmitted from this FIFO buffer when configured in TX mode. The delay is a multiple of the basic interval timer clock source period (reference clock × 1, reference clock × 10, or bit time clock of the related CAN channel).

Do not write to these bits when the CANFD module is in GL_SLEEP mode.

Do not write to these bits when the CFE bit is set to 1.

When CFDGCFG.ITRCP[15:0] = 0x0000, set the CFITT[7:0] bits to 0x0000.

28.2.30 CFDCFSTS : Common FIFO Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0058

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	CFMC[5:0]						—	—	—	CFTXIF	CFRXIF	CFMLT	CFFLL	CFEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	CFEMP	Common FIFO Empty 0: FIFO not empty 1: FIFO empty	R
1	CFFLL	Common FIFO Full 0: FIFO not full 1: FIFO full	R
2	CFMLT	Common FIFO Message Lost 0: Number of message lost in FIFO 1: FIFO message lost	R/W

仅当CANFD模块处于GL_RESET模式时写入该位。

CFIGCV[2:0]位（通用FIFO中断生成计数器值）

CFIGCV[2:0]位选择用于生成FIFO中断的消息计数器值。这些值表示要生成中断的FIFO深度的分数。

当CANFD模块处于GL_SLEEP模式时，不要写入这些位。

这些位的设置应与CFDC[2:0]位同步。

仅当CANFD模块处于GL_RESET模式时才写入这些位。

CFTML[1:0]位（通用FIFOTX报文缓冲区链接）

CFTML[1:0]位选择TXFIFO链接到的正常发送报文缓冲区位置，用于发送扫描。

不要在GL_OPERATION或GL_SLEEP模式下写入这些位。

仅当CANFD模块处于GL_RESET模式时写入该位。

CFDC[2:0]位（通用FIFO深度配置）

CFDC[2:0]位根据消息数量选择公共FIFO的深度。如果FIFO深度配置为0报文，则无法使用FIFO。

仅当CANFD模块处于GL_RESET模式时才写入这些位。

CFITT[7:0]位（通用FIFO间隔传输时间）

当配置为TX模式时，CFTT[7:0]位选择从此FIFO缓冲区发送的所有消息的开始发送延迟。延迟是基本间隔定时器时钟源周期（参考时钟×1，参考时钟×10，或相关CAN通道的位时钟）的倍数。

当CANFD模块处于GL_SLEEP模式时，不要写入这些位。

当CFE位设置为1时，请勿写入这些位。

当CFDGCFG.ITRCP[15:0]=0x0000时，将CFITT[7:0]位设置为0x0000。

28.2.30 CFDCFSTS:通用FIFO状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0058

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	CFMC[5:0]						—	—	—	CFTXIF	CFRXIF	CFMLT	CFFLL	CFEMP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	CFEMP	普通FIFO空 0：FIFO非空1：FIFO空	R
1	CFFLL	通用FIFO已满 0：FIFO未满1：FIFO已满	R
2	CFMLT	普通FIFO消息丢失 0：FIFO中丢失的报文数1：FIFO报文丢失	R/W

Bit	Symbol	Function	R/W
3	CFRXIF	Common RX FIFO Interrupt Flag 0: FIFO interrupt condition not satisfied after frame reception 1: FIFO interrupt condition satisfied after frame reception	R/W
4	CFTXIF	Common TX FIFO Interrupt Flag 0: FIFO interrupt condition not satisfied after frame transmission 1: FIFO Interrupt condition satisfied after frame transmission	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
13:8	CFMC[5:0]	Common FIFO Message Count Number of messages stored in FIFO	R
31:14	—	These bits are read as 0. The write value should be 0.	R/W

CFEMP bit (Common FIFO Empty)

The CFEMP bit is set automatically when:

- The CPU has read all messages from the FIFO configured in RX mode
- All messages have been transmitted from the FIFO configured in TX mode
- The FIFO is disabled by setting the CFE bit to 0
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET when FIFO configured in TX mode.

The CFEMP bit is cleared automatically when:

- The first reception message is stored in the FIFO buffer when configured in RX mode
- The first message to be transmitted is stored in the FIFO buffer when configured in TX mode.

CFFLL bit (Common FIFO Full)

The CFFLL bit is set automatically when the number of CAN messages stored in the FIFO matches the configured FIFO depth.

The CFFLL bit is cleared automatically when:

- The number of CAN messages stored in the FIFO is less than the configured FIFO depth
- The FIFO is disabled by setting the CFE bit to 0
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET mode when FIFO buffer is configured in TX mode.

CFMLT bit (Common FIFO Message Lost)

The CFMLT bit is set automatically whenever a message is lost due to attempted storage of a new message when FIFO is already full in RX mode.

If a set from the CAN channel occurs simultaneously with a clear by a write access, then this bit is set.

Only write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode and the related CANFD channel is not in CH_RESET mode for FIFO configured as TX FIFO. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

The CFMLT bit is cleared:

- By writing 0 to it
- When the CANFD module is in GL_RESET mode
- When the related CANFD channel is in CH_RESET mode if the FIFO buffer is configured in TX mode.

CFRXIF bit (Common RX FIFO Interrupt Flag)

The CFRXIF bit is not cleared automatically if the Common FIFO buffer is disabled.

Bit	Symbol	Function	R/W
3	CFRXIF	通用RXFIFO中断标志 0：接收帧后不满足FIFO中断条件1：接收帧后满足FIFO中断条件	R/W
4	CFTXIF	通用TXFIFO中断标志 0：帧发送后不满足FIFO中断条件1：帧发送后满足FIFO中断条件	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
13:8	CFMC[5:0]	通用FIFO消息计数 存储在FIFO中的消息数	R
31:14	—	这些位被读取为0。写入值应为0。	R/W

CFEMP bit (Common FIFO Empty)

CFEMP位在以下情况下自动设置：

●CPU已从配置为RX模式的FIFO中读取所有消息

●所有报文均已从配置为TX模式的FIFO发送

●通过将CFE位设置为0来禁用FIFO

●CANFD模块处于GL_RESET模式

●当FIFO配置为TX模式时，相关的CANFD通道处于CH_RESET。

CFEMP位在以下情况下自动清零：

●当配置为RX模式时，第一个接收报文存储在FIFO缓冲区中

●当配置为TX模式时，要发送的第一个报文存储在FIFO缓冲区中。

CFFLL bit (Common FIFO Full)

当存储在FIFO中的CAN报文数量与配置的FIFO深度匹配时，CFFLL位会自动设置。

CFFLL位在以下情况下自动清零：

●FIFO中存储的CAN报文数量小于配置的FIFO深度

●通过将CFE位设置为0来禁用FIFO

●CANFD模块处于GL_RESET模式

●当FIFO缓冲区配置为TX模式时，相关的CANFD通道处于CH_RESET模式。

CFMLT位（通用FIFO消息丢失）

当RX模式下FIFO已满时，由于尝试存储新消息而导致消息丢失，CFMLT位会自动设置。

如果来自CAN通道的设置与写访问清除同时发生，则设置该位。

仅当CANFD模块处于GL_HALT或GL_OPERATION模式并且相关的CANFD通道不处于CH_RESET模式（对于配置为TXFIFO的FIFO）时才写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

CFMLT位清零：

●写入0

●CANFD模块处于GL_RESET模式时

●如果FIFO缓冲区配置为TX模式，则相关CANFD通道处于CH_RESET模式时。

CFRXIF位（通用RXFIFO中断标志 ）

如果禁用通用FIFO缓冲区，则CFRXIF位不会自动清除。

Only write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode and the related CANFD channel is not in CH_RESET mode for FIFO configured as TX FIFO. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically when the configured interrupt condition is satisfied for Common FIFO buffers when configured in RX mode.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

The CFRXIF bit is cleared:

- By writing 0 to it
- When the CANFD module is in GL_RESET mode

CFTXIF bit (Common TX FIFO Interrupt Flag)

The CFTXIF bit is not cleared automatically if the Common FIFO buffer is disabled.

Only write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode and the related CANFD channel is not in CH_RESET mode for FIFO buffer configured as TX FIFO. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically when the configured interrupt condition is satisfied for Common FIFO buffers configured in TX mode.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

The CFTXIF bit is cleared:

- By writing 0 to it
- When the CANFD module is in GL_RESET mode
- When the related CANFD channel is in CH_RESET mode if the FIFO buffer is configured in TX mode.

CFMC[5:0] bits (Common FIFO Message Count)

The CFMC[5:0] bits indicate the following:

- Number of CAN messages stored by the CPU in the FIFO buffer configured in TX mode pending for transmission
- Number of CAN messages stored in the FIFO buffer configured in RX mode by CANFD module to be read by the CPU

The CFMC[5:0] bits are cleared automatically when:

- The FIFO is disabled
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET mode if the FIFO buffer is configured in TX mode.

28.2.31 CFDCFPCTR : Common FIFO Pointer Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x005C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CFPC[7:0]	Common FIFO Pointer Control Increments read or write pointer of the corresponding Common FIFO buffers depending on the mode configuration.	W

仅当CANFD模块处于GL_HALT或GL_OPERATION模式并且相关的CANFD通道不处于CH_RESET模式（对于配置为TXFIFO的FIFO）时才写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

当配置为RX模式时，当通用FIFO缓冲区满足配置的中断条件时，该位自动设置。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

CFRXIF位清零：

●写入0

●CANFD模块处于GL_RESET模式时

CFTXIF位（通用TXFIFO中断标志 ）

如果禁用通用FIFO缓冲区，CFTXIF位不会自动清除。

仅当CANFD模块处于GL_HALT或GL_OPERATION模式且相关CANFD通道未处于CH_RESET模式时才写入该位，FIFO缓冲区配置为TXFIFO。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

当配置为TX模式的通用FIFO缓冲区满足配置的中断条件时，该位自动设置。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

CFTXIF位清零：

●写入0

●CANFD模块处于GL_RESET模式时

●如果FIFO缓冲区配置为TX模式，则相关CANFD通道处于CH_RESET模式时。

CFMC[5:0]位（通用FIFO消息计数）

CFMC[5:0]位指示以下内容：

●CPU存储在TX模式下配置的FIFO缓冲区中等待传输的CAN报文数

●CANFD模块在RX模式下配置的FIFO缓冲区中存储的可供CPU读取的CAN报文数

CFMC[5:0]位在以下情况下自动清零：

●FIFO被禁用

●CANFD模块处于GL_RESET模式

●如果FIFO缓冲区配置为TX模式，则相关CANFD通道处于CH_RESET模式。

28.2.31 CFDCFPCTR:通用FIFO指针控制寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x005C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFPC[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CFPC[7:0]	通用FIFO指针控制 根据模式配置增加相应通用FIFO缓冲区的读取或写入指针。	W

Bit	Symbol	Function	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The Common FIFO Pointer Control Registers can be used to increment the read or write pointer of the corresponding Common FIFO buffer.

CFPC[7:0] bits (Common FIFO Pointer Control)

When the value 0xFF is written into the CFPC[7:0] bits, the read pointer of the corresponding Common FIFO buffer (when configured in RX mode), or the write pointer of the corresponding Common FIFO buffer (when configured in TX mode) moves to the next FIFO entry.

The read value from these bits is always 0x00.

Only write to these bits when the CANFD module is in GL_HALT or GL_OPERATION mode.

Only write 0xFF to this register when:

- The Common FIFO buffer is enabled and is not empty if configured in RX mode
- The Common FIFO buffer is enabled and is not full if configured in TX mode

Do not write to the Common FIFO Pointer Control registers when DMA is enabled.

28.2.32 CFDFESTS : FIFO Empty Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0060

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFEMP	—	—	—	—	—	—	RFXEMP[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
1:0	RFXEMP[1:0]	RX FIFO Empty Status 0: Corresponding FIFO not empty 1: Corresponding FIFO empty	R
7:2	—	These bits are read as 0. The write value should be 0.	R
8	CFEMP	Common FIFO Empty Status 0: Corresponding FIFO not empty 1: Corresponding FIFO empty	R
31:9	—	These bits are read as 0. The write value should be 0.	R

The FIFO Empty Status register shows status of the empty bits of the FIFO buffers.

RFXEMP[1:0] bits (RX FIFO Empty Status)

The RFXEMP[1:0] bits are set when the CANFD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the RX FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the RX FIFO Status Registers.

CFEMP bits (Common FIFO Empty Status)

The CFEMP bits are set when the CANFD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the Common FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the Common FIFO Status Registers.

Bit	Symbol	Function	R/W
31:8	—	这些位被读取为0。写入值应为0。	R/W

通用FIFO指针控制寄存器可用于递增相应的读或写指针
通用FIFO缓冲区。

CFPC[7:0]位（通用FIFO指针控制）

当值0xFF写入CFPC[7:0]位时，对应CommonFIFO缓冲区的读指针（配置为RX模式时），或对应的CommonFIFO缓冲区的写指针（配置为TX模式时）移动到下一个FIFO条目。

从这些位读取的值始终为0x00。

仅当CANFD模块处于GL_HALT或GL_OPERATION模式时才写入这些位。

仅在以下情况下向该寄存器写入0xFF：

●如果配置为RX模式，则CommonFIFO缓冲区已启用且不为空

●如果配置为TX模式，则CommonFIFO缓冲区已启用且未满

启用DMA时不要写入通用FIFO指针控制寄存器。

28.2.32 CFDFESTS:FIFO空状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0060

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFEMP	—	—	—	—	—	—	RFXEMP[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
1:0	RFXEMP[1:0]	RXFIFO空状态 0：对应的FIFO不为空1：对应的FIFO为空	R
7:2	—	这些位被读取为0。写入值应为0。	R
8	CFEMP	常见FIFO空状态 0：对应的FIFO不为空1：对应的FIFO为空	R
31:9	—	这些位被读取为0。写入值应为0。	R

FIFOEmptyStatus寄存器显示FIFO缓冲区的空位状态。

RFXEMP[1:0]位（RXFIFO空状态）

当CANFD模块处于GL_RESET模式时，RFXEMP[1:0]位被设置。

当在RXFIFO状态寄存器中设置相应位时，每个位都会自动设置。

当RXFIFO状态寄存器中的相应位清零时，每个位都会自动清零。

CFEMP位（通用FIFO空状态）

CFEMP位在CANFD模块处于GL_RESET模式时置位。

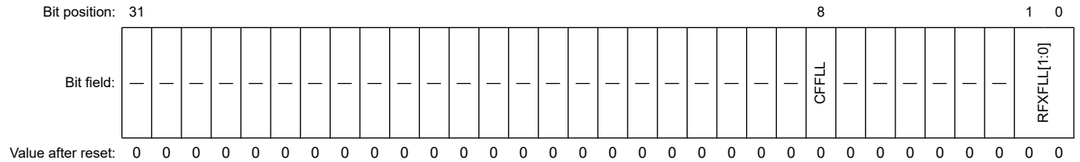
当在通用FIFO状态寄存器中设置相应位时，每个位都会自动设置。

当公共FIFO状态寄存器中的相应位清零时，每个位都会自动清零。

28.2.33 CFDFFSTS : FIFO Full Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0064



Bit	Symbol	Function	R/W
1:0	RFXFLL[1:0]	RX FIF0 Full Status 0: Corresponding FIFO not full 1: Corresponding FIFO full	R
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	CFFLL	Common FIF0 Full Status 0: Corresponding FIFO not full 1: Corresponding FIFO full	R
31:9	—	These bits are read as 0. The write value should be 0.	R/W

The FIFO Full Status Register shows status of the full bits of the FIFO buffers.

RFXFLL[1:0] bits (RX FIF0 Full Status)

The RFXFLL[1:0] bits are cleared when CANFD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the RX FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the RX FIFO Status Registers.

CFFLL bits (Common FIF0 Full Status)

The CFFLL bits are cleared when the CANFD module is in GL_RESET mode.

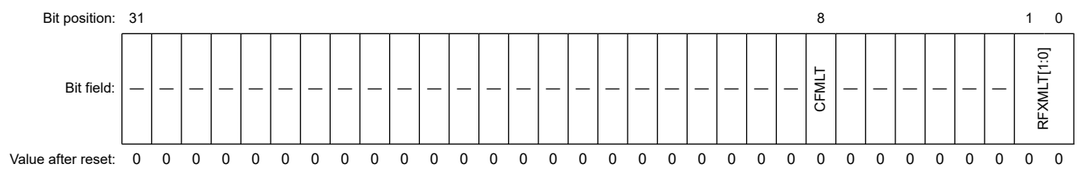
Each bit is set automatically when the corresponding bit is set in the Common FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the Common FIFO Status Registers.

28.2.34 CFDFMSTS : FIFO Message Lost Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0068

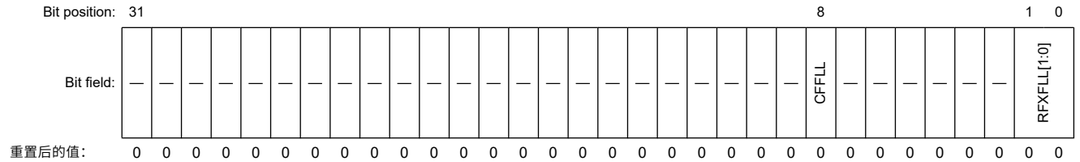


Bit	Symbol	Function	R/W
1:0	RFXMLT[1:0]	RX FIFO Message Lost Status 0: Corresponding FIFO Message Lost flag not set 1: Corresponding FIFO Message Lost flag set	R
7:2	—	These bits are read as 0. The write value should be 0.	R/W

28.2.33 CFDFFSTS:FIFO满状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0064



Bit	Symbol	Function	R/W
1:0	RFXFLL[1:0]	RXFIF0完整状态 0：对应FIFO未满1：对应FIFO已满	R
7:2	—	这些位被读取为0。写入值应为0。	R/W
8	CFFLL	常见的FIF0完整状态 0：对应FIFO未满1：对应FIFO已满	R
31:9	—	这些位被读取为0。写入值应为0。	R/W

FIFO满状态寄存器显示FIFO缓冲器的满位状态。

RFXFLL[1:0]位（RXFIF0完整状态）

当CANFD模块处于GL_RESET模式时，RFXFLL[1:0]位被清除。

当在RXFIFO状态寄存器中设置相应位时，每个位都会自动设置。

当RXFIFO状态寄存器中的相应位清零时，每个位都会自动清零。

CFFLL位（通用FIF0完整状态）

当CANFD模块处于GL_RESET模式时，CFFLL位被清除。

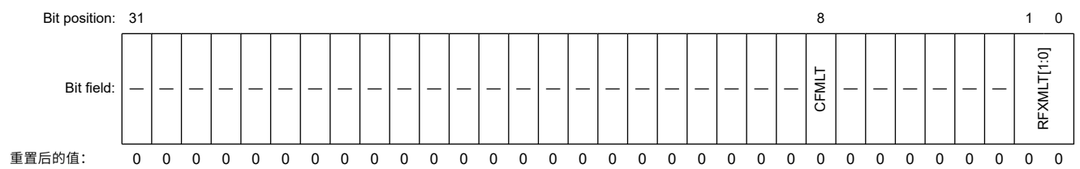
当在通用FIFO状态寄存器中设置相应位时，每个位都会自动设置。

当公共FIFO状态寄存器中的相应位清零时，每个位都会自动清零。

28.2.34 CFDFMSTS:FIFO消息丢失状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0068



Bit	Symbol	Function	R/W
1:0	RFXMLT[1:0]	RXFIFO消息丢失状态 0：未设置对应的FIFO报文丢失标志1：设置了对应的FIFO报文丢失标志	R
7:2	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
8	CFMLT	Common FIFO Message Lost Status 0: Corresponding FIFO Message Lost flag not set 1: Corresponding FIFO Message Lost flag set	R
31:9	—	These bits are read as 0. The write value should be 0.	R/W

The FIFO Message Lost Status Register shows status of the Msg Lost bits of the FIFO buffers.

RFXMLT[1:0] bits (RX FIFO Message Lost Status)

The RFXMLT[1:0] bits are cleared when the CANFD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the RX FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the RX FIFO Status Registers.

CFMLT bits (Common FIFO Message Lost Status)

The CFMLT bits are cleared when the CANFD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the Common FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the Common FIFO Status Registers.

28.2.35 CFDRFISTS : RX FIFO Interrupt Flag Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x006C

Bit position:	31																												1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFXIF[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	RFXIF[1:0]	RX FIFO[x] Interrupt Flag Status 0: Corresponding RX FIFO Interrupt flag not set 1: Corresponding RX FIFO Interrupt flag set	R
31:2	—	These bits are read as 0. The write value should be 0.	R/W

The FIFO Interrupt Flag Status Register shows status of the interrupt flag bits of the RX FIFO buffers.

RFXIF[1:0] bits (RX FIFO[x] Interrupt Flag Status)

Each bit is set automatically when the corresponding interrupt flag bit is set in the RX FIFO Status Registers.

The RFXIF[1:0] bits are cleared when the CANFD module is in GL_RESET mode.

Each bit is cleared automatically when the corresponding interrupt flag bit is cleared in the RX FIFO Status Registers.

Bit	Symbol	Function	R/W
8	CFMLT	常见FIFO消息丢失状态 0：未设置对应的FIFO报文丢失标志1：设置了对应的FIFO报文丢失标志	R
31:9	—	这些位被读取为0。写入值应为0。	R/W

FIFO消息丢失状态寄存器显示FIFO缓冲区的MsgLost位的状态。

RFXMLT[1:0]位（RXFIFO消息丢失状态）

当CANFD模块处于GL_RESET模式时，RFXMLT[1:0]位被清除。

当在RXFIFO状态寄存器中设置相应位时，每个位都会自动设置。

当RXFIFO状态寄存器中的相应位清零时，每个位都会自动清零。

CFMLT位（通用FIFO消息丢失状态）

当CANFD模块处于GL_RESET模式时，CFMLT位被清除。

当在通用FIFO状态寄存器中设置相应位时，每个位都会自动设置。

当公共FIFO状态寄存器中的相应位清零时，每个位都会自动清零。

28.2.35 CFDRFISTS:RXFIFO中断标志 状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x006C

Bit position:	31																												1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFXIF[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	RFXIF[1:0]	RXFIFO[x]中断标志 状态 0：未设置相应的RXFIFO中断标志 1：设置了相应的RXFIFO中断标志	R
31:2	—	这些位被读取为0。写入值应为0。	R/W

FIFO中断标志 状态寄存器显示RXFIFO缓冲区的中断标志位的状态。

RFXIF[1:0]位（RXFIFO[x]中断标志 状态）

当在RXFIFO状态寄存器中设置相应的中断标志位时，每个位都会自动设置。

当CANFD模块处于GL_RESET模式时，RFXIF[1:0]位被清除。

当RXFIFO状态寄存器中相应的中断标志位清零时，每个位都会自动清零。

28.2.36 CFDCDTCT : DMA Transfer Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00C8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFDMAE	—	—	—	—	—	—	RFDMAE1	RFDMAE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFDMAE0	DMA Transfer Enable for RXFIFO 0 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
1	RFDMAE1	DMA Transfer Enable for RXFIFO 1 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	CFDMAE	DMA Transfer Enable for Common FIFO 0 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

The DMA Transfer Control Register controls the start and stop of DMA transfer operation.

RFDMAEe (e = 0 to 1) bit (DMA Transfer Enable for RXFIFO e)

The RFDMAEe bit cannot be set in GL_SLEEP or GL_RESET mode.

This bit is cleared when the CANFD module is in GL_RESET mode.

CFDMAE bit (DMA Transfer Enable for Common FIFO)

The CFDMAE bit enables or disables DMA transfer request for common FIFO

The CFDMAE bit cannot be set in GL_SLEEP or GL_RESET mode.

Do not enable a DMA transfer for a Common FIFO that is configured as TX FIFO.

This bit is cleared when the CANFD module is in GL_RESET mode.

28.2.37 CFDCDTSTS : DMA Transfer Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00CC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFDMASTS	—	—	—	—	—	—	RFDMASTS1	RFDMASTS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

28.2.36 CFDDTCT:DMA传输控制寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00C8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFDMAE	—	—	—	—	—	—	RFDMAE1	RFDMAE0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFDMAE0	RXFIFO0的DMA传输使能 0：禁用DMA传输请求1：启用DMA传输请求	R/W
1	RFDMAE1	RXFIFO1的DMA传输使能 0：禁用DMA传输请求1：启用DMA传输请求	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
8	CFDMAE	CommonFIFO0的DMA传输使能 0：禁用DMA传输请求1：启用DMA传输请求	R/W
31:9	—	这些位被读取为0。写入值应为0。	R/W

DMA传输控制寄存器控制DMA传输操作的开始和停止。

RFDMAEe（e=0到1）位（RXFIFOe的DMA传输使能）

RFDMAEe位不能在GL_SLEEP或GL_RESET模式下设置。

当CANFD模块处于GL_RESET模式时，该位清零。

CDMAE位（通用FIFO的DMA传输使能）

CDMAE位启用或禁用通用FIFO的DMA传输请求

CFDMAE位不能在GL_SLEEP或GL_RESET模式下设置。

不要为配置为TXFIFO的CommonFIFO启用DMA传输。

当CANFD模块处于GL_RESET模式时，该位清零。

28.2.37 CFDCDTSTS:DMA传输状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00CC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFDMASTS	—	—	—	—	—	—	RFDMASTS1	RFDMASTS0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFDMASTS0	DMA Transfer Status for RX FIFO 0 0: DMA transfer stopped 1: DMA transfer on going	R
1	RFDMASTS1	DMA Transfer Status for RX FIFO 1 0: DMA transfer stopped 1: DMA transfer on going	R
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	CFDMASTS	DMA Transfer Status only for Common FIFO 0: DMA transfer stopped 1: DMA transfer on going	R
31:9	—	These bits are read as 0.	R

The DMA Transfer Status Register shows the status of the DMA transfer.

RFDMASTSe (e = 0 to 1) bit (DMA Transfer Status for RX FIFO e)

Each bit is set automatically when the corresponding DMA enable bit is set and the corresponding DMA FIFO is not empty.

Each bit is cleared automatically when the DMA transfer stops either because the DMA is disabled or the DMA FIFO is empty.

When CFDCDTCT.RFDMAEe (see CFDCDTCT.RFDMAEe bit in section 28.2.36. CFDCDTCT : DMA Transfer Control Register) is set to 0 while DMA transfer for the corresponding FIFO is on going, the RFDMASTSe bit becomes 0 when the DMA transfer is complete.

This bit is cleared when the CANFD module is in GL_RESET mode.

CFDMASTS bit (DMA Transfer Status only for Common FIFO)

Each bit is set automatically when the corresponding DMA enable bit is set and the corresponding DMA FIFO is not empty.

Each bit is cleared automatically when the DMA transfer stops either because the DMA is disabled or the DMA FIFO is empty.

When CFDCDTCT.CFDMAE (see CFDCDTCT.CFDMAE bit in section 28.2.36. CFDCDTCT : DMA Transfer Control Register) is set to 0 while DMA transfer for the corresponding FIFO is on going, the CFDMASTS bit becomes 0 when the DMA transfer is complete.

This bit is cleared when the CANFD module is in GL_RESET mode.

28.2.38 CFDTMCi : TX Message Buffer Control Registers i (i = 0 to 3)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0070 + 0x01 × i

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	TMOM	TMTAR	TMTR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMTR	TX Message Buffer Transmission Request 0: TX Message buffer transmission not requested 1: TX message buffer transmission requested	R/W
1	TMTAR	TX Message Buffer Transmission Abort Request 0: TX message buffer transmission request abort not requested 1: TX message buffer transmission request abort requested	R/W
2	TMOM	TX Message Buffer One-shot Mode 0: TX message buffer not configured in one-shot mode 1: TX message buffer configured in one-shot mode	R/W

Bit	Symbol	Function	R/W
0	RFDMASTS0	RXFIFO0的DMA传输状态 0：DMA传输停止1：DMA传输正在进行	R
1	RFDMASTS1	RXFIFO1的DMA传输状态 0：DMA传输停止1：DMA传输正在进行	R
7:2	—	这些位被读取为0。写入值应为0。	R/W
8	CFDMASTS	DMA传输状态仅适用于CommonFIFO 0：DMA传输停止1：DMA传输正在进行	R
31:9	—	这些位读为0。	R

DMA传输状态寄存器显示DMA传输的状态。

RFDMASTSe（e=0到1）位（RXFIFOe的DMA传输状态）

当设置相应的DMA使能位且相应的DMAFIFO不为空时，每个位都会自动设置。

当DMA传输停止时，每个位都会自动清除，因为DMA被禁用或DMAFIFO为空。

当CFDCDTCT.RFDMAEe（参见第28.2.36节中的CFDCDTCT.RFDMAEe位。CFDCDTCT：DMA传输控制寄存器）设置为0，同时相应FIFO的DMA传输正在进行时，RFDMASTSe位变为0，当
DMA传输完成。

当CANFD模块处于GL_RESET模式时，该位清零。

CFDMATS位（仅用于通用FIFO的DMA传输状态）

当设置相应的DMA使能位且相应的DMAFIFO不为空时，每个位都会自动设置。

当DMA传输停止时，每个位都会自动清除，因为DMA被禁用或DMAFIFO为空。

当CFDCDTCT.CFDMAE（参见第28.2.36节中的CFDCDTCT.CFDMAE位。CFDCDTCT：DMA传输控制寄存器)设置为0，而相应FIFO的DMA传输正在进行，CFDMATS位变为0
DMA传输完成。

当CANFD模块处于GL_RESET模式时，该位清零。

28.2.38 CFDTMCi：TX消息缓冲区控制寄存器i（i=0到3）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0070 + 0x01 × i

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	TMOM	TMTAR	TMTR
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMTR	TX消息缓冲区传输请求 0：未请求TX报文缓冲区传输1：已请求TX报文缓冲区传输	R/W
1	TMTAR	TX消息缓冲区传输中止请求 0：未请求TX报文缓冲区传输请求中止1：已请求TX报文缓冲区传输请求中止	R/W
2	TMOM	TX消息缓冲区一次性模式 0：TX报文缓冲区未配置为one-shot模式1：TX报文缓冲区配置为one-shot模式	R/W

Bit	Symbol	Function	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

The TX Message Buffer Control Registers configure the TX message buffer functions.

TMTR bit (TX Message Buffer Transmission Request)

When the TMTR bit is set, the CANFD module logic tries to transmit the message stored in the corresponding message buffer.

Only write to this bit when the related CANFD module is in CH_HALT or CH_OPERATION mode.

Do not set this bit if the corresponding TX message buffer is linked to a COM FIFO in TX mode or is a part of TX Queue.

This bit cannot be directly cleared by a CPU write access.

This bit can only be set when the Transmission Result flag bits (CFDTMSTSj.TMTRF) in the CFDTMSTSj register corresponding to the message buffer are cleared to 00b.

The TMTR bit is automatically cleared by the:

- CANFD module logic at the end of a successful transmission
- CANFD module logic at the end of a transmission abort, requested by the corresponding CFDTMCi.TMTAR bit
- CANFD module logic when there is a detection of a CAN bus error or arbitration loss if CFDTMCi.TMOM bit is set for the message buffer
- CANFD module logic when the CANFD module is in GL_RESET mode or the related channel is in CH_RESET mode.

TMTAR bit (TX Message Buffer Transmission Abort Request)

When the TMTAR bit is set, the CANFD module logic tries to abort the transmission of the frame stored in the corresponding message buffer.

In most cases, transmission cannot be aborted if the internal scan for transmission is complete and the message buffer has already been selected for transmission. In this case, frame may be transmitted successfully from the message buffer. The message buffer selection is released by entering CH_HALT mode.

However, message buffer selected for transmission can be aborted by an abort request when the CAN node detects a new message on the bus (RX pin) before it starts transmission from the selected message buffer.

Only write to the TMTAR bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode. This bit can only be set when the related transmit request TMTR bit is set.

The TMTAR bit cannot be cleared by a CPU write access. Clearing of this bit by CANFD has priority over setting by a CPU write access.

The TMTAR bit is automatically cleared by:

- The CANFD module logic at the end of a successful transmission
- The CANFD module logic at the end of a transmission abort
- The CANFD module logic when there is detection of a CAN bus error or arbitration loss
- The CANFD module logic when the CANFD module is in GL_RESET mode or the related channel enters CH_RESET mode.

TMOM bit (TX Message Buffer One-shot Mode)

When the TMOM bit is set, the CANFD module logic tries to transmit the message only once.

If the transmission is successful, the CFDTMSTSj.TMTRF bits are set to 10b or 11b. Otherwise, the transmission is automatically aborted and CFDTMSTSj.TMTRF bits are set to 01b due to a bus error or a bus arbitration lost.

The TMOM bit remains set if the transmission has completed successfully or aborted due to an error or a loss of arbitration.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

Set this bit at the same time as the TMTR bit. Clear this bit with a write access.

If a message has already been requested for transmission, do not write to this bit until the message has been successfully transmitted or transmission has been aborted.

Bit	Symbol	Function	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

TX报文缓冲区控制寄存器配置TX报文缓冲区功能。

TMTR位（TX报文缓冲区传输请求）

当设置TMTR位时，CANFD模块逻辑尝试发送存储在相应消息缓冲区中的消息。

仅当相关CANFD模块处于CH_HALT或CH_OPERATION模式时才写入该位。

如果相应的TX消息缓冲区链接到TX模式下的COMFIFO或者是TX队列的一部分，则不要设置该位。

该位不能通过CPU写访问直接清除。

仅当与消息缓冲区对应的CFDTMSTSj寄存器中的传输结果标志位(CFDTMSTSj.TMTRF)被清除为00b时，才能设置该位。

TMTR位通过以下方式自动清零：

●成功传输结束时的CANFD模块逻辑

●发送中止结束时的CANFD模块逻辑，由相应的CFDTMCi.TMTAR位请求

●如果为消息缓冲区设置了CFDTMCi.TMOM位，则检测到CAN总线错误或仲裁丢失时的CANFD模块逻辑

●CANFD模块处于GL_RESET模式或相关通道处于CH_RESET模式时的CANFD模块逻辑。

TMTAR位（TX报文缓冲区传输中止请求）

当设置TMTAR位时，CANFD模块逻辑尝试中止存储在相应消息缓冲区中的帧的传输。

在大多数情况下，如果内部扫描传输完成并且消息缓冲区已被选择用于传输，则无法中止传输。在这种情况下，可以从消息缓冲区成功传输帧。通过进入CH_HALT模式释放消息缓冲区选择。

但是，当CAN节点在从选定的消息缓冲区开始传输之前检测到总线（RX引脚）上的新消息时，可以通过中止请求中止选择用于传输的消息缓冲区。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入TMTAR位。只有当相关的发送请求TMTR位被置位时，该位才能被置位。

CPU写访问不能清除TMTAR位。CANFD清除该位优先于CPU写访问设置。

TMTAR位通过以下方式自动清零：

●成功传输结束时的CANFD模块逻辑

●传输中止结束时的CANFD模块逻辑

●检测到CAN总线错误或仲裁丢失时的CANFD模块逻辑

●CANFD模块处于GL_RESET模式或相关通道进入CH_RESET模式时的CANFD模块逻辑。

TMOM位（TX消息缓冲区一次性模式）

当TMOM位置位时，CANFD模块逻辑尝试仅发送一次报文。

如果传输成功，CFDTMSTSj.TMTRF位设置为10b或11b。否则，由于总线错误或总线仲裁丢失，传输将自动中止，CFDTMSTSj.TMTRF位设置为01b。

如果传输成功完成或由于错误或仲裁丢失而中止，则TMOM位保持设置。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

该位与TMTR位同时置位。通过写访问清除该位。

如果已请求发送消息，则在消息成功发送或发送中止之前不要写入该位。

The TMOM bit is automatically cleared by the CANFD module logic when the CANFD module is in GL_RESET mode or the related channel is in CH_RESET mode.

28.2.39 CFDTMSTSj : TX Message Buffer Status Registers j (j = 0 to 3)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0074 + 0x01 × j

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TMTARM	TMTRM	TMTRF[1:0]		TMTSTS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMTSTS	TX Message Buffer Transmission Status 0: No on-going transmission 1: On-going transmission	R
2:1	TMTRF[1:0]	TX Message Buffer Transmission Result Flag 0 0: No result 0 1: Transmission aborted from the TX message buffer 1 0: Transmission successful from the TX message buffer and transmission abort was not requested 1 1: Transmission successful from the TX message buffer and transmission abort was requested	R/W
3	TMTRM	TX Message Buffer Transmission Request Mirrored 0: TX message buffer transmission not requested 1: TX message buffer transmission requested	R
4	TMTARM	TX Message Buffer Transmission Abort Request Mirrored 0: TX message buffer transmission request abort not requested 1: TX message buffer transmission request abort requested	R
7:5	—	These bits are read as 0. The write value should be 0.	R/W

The TX Message Buffer Status Registers show status of the transmission and transmission abort for the corresponding message buffers.

TMTSTS bit (TX Message Buffer Transmission Status)

The TMTSTS bit is set automatically at the start of the transmission from the corresponding TX message buffer.

This bit is cleared automatically when:

- Transmission stops
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET mode.

TMTRF[1:0] bits (TX Message Buffer Transmission Result Flag)

The TMTRF[1:0] bits show the result for the corresponding TX message buffer. The status is as follows:

- 00: Transmission in progress or has not been requested
- 01: Transmission has been aborted from the corresponding TX message buffer
- 10: Transmission was successful from the corresponding TX message buffer and the CFDTMCi.TMTAR bit was not set for this TX message buffer
- 11: Transmission was successful from the corresponding TX message buffer, but the CFDTMCi.TMTAR bit was set for this TX message buffer.

Only write to these bits when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

The TMTRF[1:0] bits are cleared automatically when the CANFD module is in GL_RESET mode or the related channel is in CH_RESET mode.

当CANFD模块处于GL_RESET模式或相关通道处于CH_RESET模式时，TMOM位由CANFD模块逻辑自动清零。

28.2.39 CFDTMSTSj：TX消息缓冲区状态寄存器j（j=0到3）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0074 + 0x01 × j

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TMTARM	TMTRM	TMTRF[1:0]		TMTSTS
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMTSTS	TX消息缓冲区传输状态 0：没有进行中的传输1：进行中的传输	R
2:1	TMTRF[1:0]	TX消息缓冲区传输结果标志 00：无结果01：从TX报文缓冲区中止传输10：从TX报文缓冲区传输成功并且未请求传输中止 11：从TX报文缓冲区传输成功并请求传输中止	R/W
3	TMTRM	TX消息缓冲区传输请求已镜像 0：未请求TX消息缓冲区传输1：请求TX消息缓冲区传输	R
4	TMTARM	TX消息缓冲区传输中止请求已镜像 0：未请求TX报文缓冲区传输请求中止1：已请求TX报文缓冲区传输请求中止	R
7:5	—	这些位被读取为0。写入值应为0。	R/W

TX报文缓冲区状态寄存器显示相应报文缓冲区的传输和传输中止状态。

TMTSTS位（TX报文缓冲区传输状态）

TMTSTS位在相应TX报文缓冲区的传输开始时自动设置。

该位在以下情况下自动清零：

●传输停止

●CANFD模块处于GL_RESET模式

●相关CANFD通道处于CH_RESET模式。

TMTRF[1:0]位（TX报文缓冲区传输结果标志）

TMTRF[1:0]位显示相应TX报文缓冲区的结果。状态如下：

●00：传输中或未请求

●01：已从相应的TX消息缓冲区中止传输

●10：从相应的TX报文缓冲区发送成功，并且没有为该TX报文缓冲区设置CFDTMCi.TMTAR位

●11：从相应的TX报文缓冲区发送成功，但为此TX报文缓冲区设置了CFDTMCi.TMTAR位。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入这些位。

当CANFD模块处于GL_RESET模式或相关通道处于CH_RESET模式时，TMTRF[1:0]位会自动清零。

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

TMTRM bit (TX Message Buffer Transmission Request Mirrored)

The TMTRM bit is set when the CFDTMCi.TMTR bit in the corresponding CFDTMCi register is set.

This bit is cleared when the CFDTMCi.TMTR bit in the corresponding CFDTMCi register is cleared.

TMTARM bit (TX Message Buffer Transmission Abort Request Mirrored)

The TMTARM bit is set when the CFDTMCi.TMTAR bit in the corresponding CFDTMCi register is set.

This bit is cleared when the CFDTMCi.TMTAR bit in the corresponding CFDTMCi register is cleared.

28.2.40 CFDTMTRSTS : TX Message Buffer Transmission Request Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0078

Bit position:	31 … 4	3	2	1	0
Bit field:	—	CFDTMTRSTS[3:0]			
Value after reset:	0 … 0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CFDTMTRSTS[3:0]	TX Message Buffer Transmission Request Status 0: Transmission not requested for corresponding TX message buffer 1: Transmission requested for corresponding TX message buffer	R
31:4	—	These bits are read as 0. The write value should be 0.	R

These bits show the TX Message Buffer Transmission Request Status for the corresponding TX Message Buffer. The bit 0 of a CFDTMTRSTS register corresponds to the TX message buffer 0.

The bit position of CFDTMTRSTS corresponds to the buffer number of TX message buffer.

CFDTMTRSTS[3:0] bits (TX Message Buffer Transmission Request Status)

The CFDTMTRSTS[3:0] bits show status of the CFDTMCi.TMTR bits of the TX Message Buffer Control Registers.

Each bit is set automatically when the corresponding bit is set in the TX Message Buffer Control Registers (CFDTMCi), and only when the message buffer does not belong to a TX Queue.

Each bit is cleared automatically when:

- The corresponding bit is cleared in the TX Message Buffer Control Registers
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET mode.

28.2.41 CFDTMTARSTS : TX Message Buffer Transmission Abort Request Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x007C

Bit position:	31 … 4	3	2	1	0
Bit field:	—	CFDTMTARSTS[3:0]			
Value after reset:	0 … 0	0	0	0	0

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

TMTRM位（镜像的TX消息缓冲区传输请求）

当相应CFDTMCi寄存器中的CFDTMCi.TMTR位置1时，TMTRM位置1。

当相应CFDTMCi寄存器中的CFDTMCi.TMTR位清零时，该位清零。

TMTARM位（已镜像TX消息缓冲区传输中止请求）

当相应的CFDTMCi寄存器中的CFDTMCi.TMTAR位被置位时，TMTARM位被置位。

当相应CFDTMCi寄存器中的CFDTMCi.TMTAR位清零时，该位清零。

28.2.40 CFDTMTRSTS:TX报文缓冲区传输请求状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0078

Bit position:	31 … 4	3	2	1	0
Bit field:	—	CFDTMTRSTS[3:0]			
重置后的值:	0 … 0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CFDTMTRSTS[3:0]	TX消息缓冲区传输请求状态 0：对应的TX报文缓冲区未请求传输1：对应的TX报文缓冲区请求传输	R
31:4	—	这些位被读取为0。写入值应为0。	R

这些位显示相应TX报文缓冲区的TX报文缓冲区传输请求状态。CFDTMTRSTS寄存器的位0对应于TX消息缓冲区0。

CFDTMTRSTS的位位置对应于TX报文缓冲区的缓冲区号。

CFDTMTRSTS[3:0]位（TX消息缓冲区传输请求状态）

CFDTMTRSTS[3:0]位显示TX报文缓冲区控制寄存器的CFDTMCi.TMTR位的状态。

当在TX消息缓冲区控制寄存器(CFDTMCi)中设置相应位时，每个位都会自动设置，并且仅当消息缓冲区不属于TX队列时。

在以下情况下，每个位都会自动清除：

- TX报文缓冲区控制寄存器中的相应位清零
- CANFD模块处于GL_RESET模式
- 相关CANFD通道处于CH_RESET模式。

28.2.41 CFDTMTARSTS：TX消息缓冲区传输中止请求状态 Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x007C

Bit position:	31 … 4	3	2	1	0
Bit field:	—	CFDTMTARSTS[3:0]			
重置后的值:	0 … 0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CFDTMTARSTS[3:0]	TX Message Buffer Transmission Abort Request Status 0: Transmission abort not requested for corresponding TX message buffer 1: Transmission abort requested for corresponding TX message buffer	R
31:4	—	These bits are read as 0. The write value should be 0.	R

These bits show the TX Message Buffer Transmission Abort Request Status for the corresponding TX Message Buffer. The bit 0 of a CFDTMTARSTS register corresponds to the TX message buffer 0.

The bit position of CFDTMTARSTS corresponds to the buffer number of TX message buffer.

CFDTMTARSTS[3:0] bits (TX Message Buffer Transmission Abort Request Status)

The CFDTMTARSTS[3:0] bits show status of the CFDTMCi.TMTAR bits of the TX Message Buffer Control Registers.

Each bit is set automatically when the corresponding bit is set in the TX Message Buffer Control Registers, and when the message buffer belongs to a TX Queue.

Each bit is cleared automatically when:

- The corresponding bit is cleared in the TX Message Buffer Control Registers
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET mode.

28.2.42 CFDTMTCSTS : TX Message Buffer Transmission Completion Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0080

Bit position:	31																								3	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFDTMTCSTS[3:0]
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CFDTMTCSTS[3:0]	TX Message Buffer Transmission Completion Status 0: Transmission not complete for corresponding TX message buffer 1: Transmission completed for corresponding TX message buffer	R
31:4	—	These bits are read as 0. The write value should be 0.	R

These bits show the TX Message Buffer Transmission Completion Status for the corresponding TX Message Buffer. The bit 0 of a CFDTMTCSTS register corresponds to the TX message buffer 0.

The bit position of CFDTMTCSTS corresponds to the buffer number of TX message buffer.

CFDTMTCSTS[3:0] bits (TX Message Buffer Transmission Completion Status)

The CFDTMTCSTS[3:0] bits show status of successful completion of the TX Message Buffer Status Registers.

Each bit is set automatically when the corresponding bit is set in the TX Message Buffer Status Registers.

Each bit is cleared automatically when:

- The corresponding bit is cleared in the TX Message Buffer Status Registers
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET mode.

If a CAN channel enters CH_RESET mode, then the bits related to that channel are cleared.

Bit	Symbol	Function	R/W
3:0	CFDTMTARSTS[3:0]	TX消息缓冲区传输中止请求状态 0：对应的TX报文缓冲区未请求发送中止1：对应的TX报文缓冲区请求发送中止	R
31:4	—	这些位被读取为0。写入值应为0。	R

这些位显示相应TX报文缓冲区的TX报文缓冲区传输中止请求状态。CFDTMTARSTS寄存器的位0对应于TX报文缓冲区0。

CFDTMTARSTS的位位置对应于TX报文缓冲区的缓冲区号。

CFDTMTARSTS[3:0]位（TX报文缓冲区传输中止请求状态）

CFDTMTARSTS[3:0]位显示TX报文缓冲区控制寄存器的CFDMCi.TMTAR位的状态。

当TX报文缓冲区控制寄存器中的相应位被设置时，并且报文缓冲区属于TX队列时，每个位都会自动设置。

在以下情况下，每个位都会自动清除：

●TX报文缓冲区控制寄存器中的相应位清零

●CANFD模块处于GL_RESET模式

●相关CANFD通道处于CH_RESET模式。

28.2.42 CFDTMTCSTS:TX消息缓冲区传输完成状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0080

Bit position:	31																								3	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFDTMTCSTS[3:0]
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CFDTMTCSTS[3:0]	TX消息缓冲区传输完成状态 0：对应的TX报文缓冲区的传输未完成1：对应的TX报文缓冲区的传输完成	R
31:4	—	这些位被读取为0。写入值应为0。	R

这些位显示相应TX报文缓冲区的TX报文缓冲区传输完成状态。CFDTMTCSTS寄存器的位0对应于TX消息缓冲区0。

CFDTMTCSTS的位位置对应于TX报文缓冲区的缓冲区号。

CFDTMTCSTS[3:0]位（TX消息缓冲区传输完成状态）

CFDTMTCSTS[3:0]位显示成功完成TX报文缓冲区状态寄存器的状态。

当在TX报文缓冲区状态寄存器中设置相应位时，每个位都会自动设置。

在以下情况下，每个位都会自动清除：

●TX报文缓冲区状态寄存器中的相应位清零

●CANFD模块处于GL_RESET模式

●相关CANFD通道处于CH_RESET模式。

如果CAN通道进入CH_RESET模式，则与该通道相关的位被清除。

28.2.43 CFDTMTASTS : TX Message Buffer Transmission Abort Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0084

Bit position:	31																												3	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFDTMTASTS[3:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CFDTMTASTS[3:0]	TX Message Buffer Transmission Abort Status 0: Transmission not aborted for corresponding TX message buffer 1: Transmission aborted for corresponding TX message buffer	R
31:4	—	These bits are read as 0.	R

These bits show the TX Message Buffer Transmission abort Status for the corresponding TX Message Buffer. The bit 0 of a CFDTMTASTS register corresponds to the TX message buffer 0.

The bit position of CFDTMTASTS corresponds to the buffer number of TX message buffer.

CFDTMTASTS[3:0] bits (TX Message Buffer Transmission Abort Status)

The CFDTMTASTS[3:0] bits show status of the successful transmission abort of the corresponding TX message buffer.

Each bit is set automatically when the CFDTMSTSj.TMTRF bits are set to 01b in the corresponding TX Message Buffer Status Register.

Each bit is cleared automatically when:

- The CFDTMSTSj.TMTRF bits are cleared in the corresponding TX Message Buffer Status Register
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET mode.

28.2.44 CFDTMIEC : TX Message Buffer Interrupt Enable Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0088

Bit position:	31																												3	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TMIEg[3:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	TMIEg[3:0]	TX Message Buffer Interrupt Enable 0: TX message buffer interrupt disabled for corresponding TX message buffer 1: TX message buffer interrupt enabled for corresponding TX message buffer	R/W
31:4	—	These bits are read as 0. The write value should be 0.	R

These bits show the TX Message Buffer Interrupt Enable for the corresponding TX Message Buffer.

The bit 0 of a CFDTMIEC register corresponds to the TX message buffer 0.

The bit position of CFDTMIEC corresponds to the buffer number of TX message buffer.

g = [0…3]

TMIEg[3:0] bits (TX Message Buffer Interrupt Enable)

If the TMIEg[3:0] bits are set, an interrupt is generated at the end of a successful transmission from the corresponding message buffer.

28.2.43 CFDTMTASTS:TX报文缓冲区传输中止状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0084

Bit position:	31																												3	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFDTMTASTS[3:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CFDTMTASTS[3:0]	TX报文缓冲区传输中止状态 0：相应的TX报文缓冲区的传输未中止1：相应的TX报文缓冲区的传输中止	R
31:4	—	这些位读为0。	R

这些位显示相应TX报文缓冲区的TX报文缓冲区传输中止状态。a的位0 CFDTMTASTS寄存器对应于TX报文缓冲区0。

CFDTMTASTS的位位置对应于TX报文缓冲区的缓冲区号。

CFDTMTASTS[3:0]位（TX报文缓冲区传输中止状态）

CFDTMTASTS[3:0]位显示相应TX消息缓冲区的成功传输中止状态。

当相应的TX消息缓冲区中的CFDTMSTSj.TMTRF位设置为01b时，每个位都会自动设置状态寄存器。

在以下情况下，每个位都会自动清除：

- CFDTMSTSj.TMTRF位在相应的TX报文缓冲区状态寄存器中清零
- CANFD模块处于GL_RESET模式
- 相关CANFD通道处于CH_RESET模式。

28.2.44 CFDTMIEC:TX报文缓冲区中断使能配置寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0088

Bit position:	31																												3	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TMIEg[3:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	TMIEg[3:0]	TX报文缓冲区中断使能 0：禁用相应TX报文缓冲区的TX报文缓冲区中断1：启用相应TX报文缓冲区的TX报文缓冲区中断	R/W
31:4	—	这些位被读取为0。写入值应为0。	R

这些位显示相应TX报文缓冲区的TX报文缓冲区中断使能。

CFDTMIEC寄存器的位0对应于TX报文缓冲区0。

CFDTMIEC的位位置对应于TX报文缓冲区的缓冲区号。

g = [0…3]

TMIEg[3:0]位（TX报文缓冲区中断使能）

如果设置了TMIEg[3:0]位，则在从相应的消息缓冲区成功传输结束时会产生中断。

See section 28.7. Interrupts and DMA for TX Message Buffer Interrupt specification.

Do not write to the TMIEg[7:0] bits when:

- The CANFD module is in GL_SLEEP mode
- The related CANFD channel is in CH_SLEEP mode
- The corresponding TX message buffer is part of a TX Queue
- The corresponding TX message buffer is linked to a Common FIFO with the CFDCFCC.CFTML bits.

28.2.45 CFDTXQCC : TX Queue Configuration/Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x008C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TXQDC[1:0]		TXQIM	—	TXQTXIE	—	—	—	—	TXQE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TXQE	TX Queue Enable 0: TX Queue disabled 1: TX Queue enabled	R/W
4:1	—	These bits are read as 0. The write value should be 0.	R/W
5	TXQTXIE	TX Queue TX Interrupt Enable 0: TX Queue TX interrupt disabled 1: TX Queue TX interrupt enabled	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	TXQIM	TX Queue Interrupt Mode 0: When the last message is successfully transmitted 1: At every successful transmission	R/W
9:8	TXQDC[1:0]	TX Queue Depth Configuration 0x00: 0 messages 0x01: Reserved 0x10: 3 messages 0x11: 4 messages	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Configuration/Control Registers are used to configure the TX Queue transmission.

TXQ is composed of TXMB0 to TXMB3 (at the maximum) when TXQE is enabled.

TXQE bit (TX Queue Enable)

The TXQE bit cannot be set if the configured TX Queue depth is 0x00 (CFDTXQCC.TXQDC == 0x00).

You cannot write to this bit when the CANFD module is in GL_SLEEP mode.

Do not write to this bit when the related CANFD channel is in CH_RESET or CH_SLEEP mode.

The TXQE bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

TXQTXIE bit (TX Queue TX Interrupt Enable)

When the TXQTXIE bit is set, an interrupt is generated based on the setting of the TXQIM bit.

You cannot write to this bit when the CANFD module is in GL_SLEEP mode.

见第28.7节。TX消息缓冲区中断规范的中断和DMA。

在以下情况下不要写入TMIEg[7:0]位：

●CANFD模块处于GL_SLEEP模式

●相关CANFD通道处于CH_SLEEP模式

●对应的TX消息缓冲区是TXQueue的一部分

●相应的TX消息缓冲区通过CFDCFCC.CFTML位链接到CommonFIFO。

28.2.45 CFDTXQCC:TX队列配置控制寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x008C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TXQDC[1:0]		TXQIM	—	TXQTXIE	—	—	—	—	TXQE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TXQE	TX队列启用 0：禁用TX队列1：启用TX队列	R/W
4:1	—	这些位被读取为0。写入值应为0。	R/W
5	TXQTXIE	TX队列TX中断使能 0：禁止发送队列发送中断1：允许发送队列发送中断	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	TXQIM	TX队列中断模式 0：最后一条信息发送成功时1：每次发送成功时	R/W
9:8	TXQDC[1:0]	TX队列深度配置 0x00：0条消息0x01：保留0x10：3条消息0x11：4条消息	R/W
31:10	—	这些位被读取为0。写入值应为0。	R/W

TX队列配置控制寄存器用于配置TX队列传输。

当TXQE使能时，TXQ由TXMB0到TXMB3（最大）组成。

TXQE位（TX队列使能）

如果配置的TX队列深度为0x00(CFDTXQCC.TXQDC==0x00)，则无法设置TXQE位。

当CANFD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CANFD通道处于CH_RESET或CH_SLEEP模式时，请勿写入该位。

当相关CANFD通道处于CH_RESET模式时，TXQE位会自动清零。

TXQTXIE位（TX队列TX中断允许）

当TXQTXIE位置位时，会根据TXQIM位的设置产生中断。

当CANFD模块处于GL_SLEEP模式时，您无法写入该位。

Do not write to this bit when the related CANFD channel is in CH_SLEEP mode.

TXQIM bit (TX Queue Interrupt Mode)

The TXQIM bit selects the interrupt generation condition for the TX Queue.

You cannot write to this bit when the CANFD module is in GL_SLEEP mode.

Do not write to this bit when the related CANFD channel is in any of the following modes:

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQDC[1:0] bits (TX Queue Depth Configuration)

The TXQDC[1:0] bits select the depth of the transmission queue. The message buffer selection starts from MB[0] up to MB[3] depending on the configured depth.

You cannot write to this bit when the CANFD module is in GL_SLEEP mode.

Do not write to this bit when the related CANFD channel is in any of the following modes:

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

28.2.46 CFDTXQSTS : TX Queue Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0090

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	TXQMC[2:0]			—	—	—	—	—	TXQTXIF	TXQFLL	TXQEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	TXQEMP	TX Queue Empty 0: TX Queue not empty 1: TX Queue empty	R
1	TXQFLL	TX Queue Full 0: TX Queue not full 1: TX Queue full	R
2	TXQTXIF	TX Queue TX Interrupt Flag 0: TX Queue interrupt condition not satisfied after a frame TX 1: TX Queue interrupt condition satisfied after a frame TX	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
10:8	TXQMC[2:0]	TX Queue Message Count Number of messages in the TX Queue.	R
31:11	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Status Registers show the status of the TX Queue of corresponding CAN channel.

TXQEMP bit (TX Queue Empty)

The TXQEMP bit is set automatically when the TX Queue is disabled or no messages are stored in the TX Queue.

当相关CANFD通道处于CH_SLEEP模式时，请勿写入该位。

TXQIM位（TX队列中断模式）

TXQIM位选择TX队列的中断产生条件。

当CANFD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CANFD通道处于以下任一模式时，请勿写入该位：

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQDC[1:0]位（TX队列深度配置）

TXQDC[1:0]位选择传输队列的深度。消息缓冲区选择从MB[0]开始直到MB[3]取决于配置的深度。

当CANFD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CANFD通道处于以下任一模式时，请勿写入该位：

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

28.2.46 CFDTXQSTS:TX队列状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0090

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	TXQMC[2:0]			—	—	—	—	—	TXQTXIF	TXQFLL	TXQEMP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	TXQEMP	TX队列空 0：TX队列不为空1：TX队列为空	R
1	TXQFLL	TX队列已满 0：TX队列未满1：TX队列已满	R
2	TXQTXIF	TX队列TX中断标志 0：一帧TX后不满足TX队列中断条件1：一帧TX后满足TX队列中断条件	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
10:8	TXQMC[2:0]	TX队列消息计数 TX队列中的消息数。	R
31:11	—	这些位被读取为0。写入值应为0。	R/W

TXQueueStatusRegisters显示相应CAN通道的TXQueue状态。

TXQEMP位（TX队列空）

当TX队列被禁用或没有消息存储在TX队列中时，TXQEMP位自动置位。

This bit is set automatically when:

- The last message is transmitted from the TX Queue
- The related CANFD channel is in CH_RESET mode.

The bit is cleared automatically when the first message to be transmitted is stored in the TX Queue.

TXQFLL bit (TX Queue Full)

The TXQFLL bit is set automatically when the number of CAN messages stored in the TX Queue matches the configured TX Queue depth.

This bit is cleared automatically when:

- The number of CAN messages stored in the TX Queue is less than the configured TX Queue depth
- The related CANFD channel is in CH_RESET mode.

TXQTXIF bit (TX Queue TX Interrupt Flag)

The TXQTXIF bit is not cleared automatically if the TX Queue is disabled.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

This bit is set automatically when the configured interrupt condition is satisfied for the TX Queue.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

You cannot write to this bit when the related CANFD channel is in CH_SLEEP or CH_RESET mode.

The bit is cleared:

- By writing 0 to it
- When the related CANFD channel is in CH_RESET mode.

TXQMC[2:0][13:8] bits (TX Queue Message Count)

The TXQMC[2:0] bits show the number of CAN messages in the TX Queue.

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

28.2.47 CFDTXQPCTR : TX Queue Pointer Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0094

Bit position:	31																						7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TXQPC[7:0]	TX Queue Pointer Control Increments the write pointer to the TX Queue buffer in the corresponding channel	W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Pointer Control Registers are used to confirm storage of a full message in the corresponding TX Queue buffers.

TXQPC[7:0] bits (TX Queue Pointer Control)

When the value 0xFF is written to the TXQPC[7:0] bits, the write pointer of the corresponding TX Queue buffer is updated and a transmit request is initiated for this message.

The read value from these bits is always 0x00. Do not write to the FIFO control registers when DMA is enabled.

该位在以下情况下自动设置：

●最后一条消息是从TXQueue发送的

●相关CANFD通道处于CH_RESET模式。

当要发送的第一个消息存储在TX队列中时，该位会自动清除。

TXQFLL位（TX队列已满）

当存储在TX队列中的CAN报文数量与配置的匹配时，自动设置TXQFLL位
TX队列深度。

该位在以下情况下自动清零：

●TXQueue中存储的CAN报文数量小于配置的TXQueue深度

●相关CANFD通道处于CH_RESET模式。

TXQTXIF位（TX队列TX中断标志 ）

如果TX队列被禁止，TXQTXIF位不会自动清零。

停止TX队列时，应在禁用TXQE并检查TX队列的空状态后清除该位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

当为TX队列配置的中断条件满足时，该位自动置位。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

当相关CANFD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

该位被清除：

●写入0

●当相关CANFD通道处于CH_RESET模式时。

TXQMC[2:0][13:8]位（TX队列消息计数）

TXQMC[2:0]位显示TX队列中的CAN报文数。

当相关CANFD通道处于CH_RESET模式时，这些位会自动清零。

28.2.47 CFDTXQPCTR:TX队列指针控制寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0094

Bit position:	31																						7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQPC[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TXQPC[7:0]	TX队列指针控制 将写入指针递增到相应通道中的TX队列缓冲区	W
31:8	—	这些位被读取为0。写入值应为0。	R/W

TX队列指针控制寄存器用于确认在相应的TX队列缓冲区中存储完整消息。

TXQPC[7:0]位（TX队列指针控制）

当值0xFF写入TXQPC[7:0]位时，相应的TX队列缓冲区的写指针被更新，并为此消息启动发送请求。

从这些位读取的值始终为0x00。启用DMA时不要写入FIFO控制寄存器。

You cannot write to these bits when the related CANFD channel is in CH_SLEEP or CH_RESET mode.

Only write 0xFF to this register when:

- The corresponding TX Queue is enabled and not full
- The Common FIFO is enabled.

28.2.48 CFDTHLCC : TX History List Configuration/Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0098

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	THLDTE	THLIM	THLIE	—	—	—	—	—	—	—	THLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	THLE	TX History List Enable 0: TX History List disabled 1: TX History List enabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
8	THLIE	TX History List Interrupt Enable 0: TX History List Interrupt disabled 1: TX History List Interrupt enabled	R/W
9	THLIM	TX History List Interrupt Mode 0: Interrupt generated if TX History List level reaches ¾ of the TX History List depth 1: Interrupt generated for every successfully stored entry	R/W
10	THLDTE	TX History List Dedicated TX Enable 0: TX FIFO + TX Queue 1: Flat TX MB + TX FIFO + TX Queue	R/W
31:11	—	These bits are read as 0. The write value should be 0.	R/W

The TX History List Configuration/Control Register configures the TX History List functions.

THLE bit (TX History List Enable)

The THLE bit enables the TX History List buffer when it is set.

You cannot write to this bit when the related CANFD channel is in CH_RESET or CH_SLEEP mode.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

THLIE bit (TX History List Interrupt Enable)

The THLIE bit enables the generation of the TX History List interrupt when it is set.

You cannot write to this bit when the CANFD module is in GL_SLEEP mode.

THLIM bit (TX History List Interrupt Mode)

The THLIM bit selects the interrupt generation condition for the FIFO.

You cannot write to this bit when the CANFD module is in GL_SLEEP mode.

Do not write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode.

THLDTE bit (TX History List Dedicated TX Enable)

The THLDTE bit selects the condition for storing an entry in the TX History List after successful transmission.

当相关CANFD通道处于CH_SLEEP或CH_RESET模式时，您无法写入这些位。

仅在以下情况下向该寄存器写入0xFF：

●对应的TXQueue已启用且未满

●CommonFIFO已启用。

28.2.48 CFDTHLCC:TX历史列表配置控制寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0098

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	THLDTE	THLIM	THLIE	—	—	—	—	—	—	—	THLE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	THLE	TX历史列表启用 0：禁用TX历史列表1：启用TX历史列表	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
8	THLIE	TX历史列表中断使能 0：禁止发送历史列表中断1：允许发送历史列表中断	R/W
9	THLIM	TX历史列表中断模式 0：如果TX历史列表级别达到TX历史列表深度的3/4，则生成中断1：为每个成功存储的条目生成中断	R/W
10	THLDTE	TX历史列表专用TX启用 0：TXFIFO+TX队列1：平坦TXMB+TXFIFO+TX队列	R/W
31:11	—	这些位被读取为0。写入值应为0。	R/W

TX历史列表配置控制寄存器配置TX历史列表功能。

THLE位（TX历史列表启用）

THLE位在设置时启用TX历史列表缓冲区。

当相关CANFD通道处于CH_RESET或CH_SLEEP模式时，您无法写入该位。

当相关CANFD通道处于CH_RESET模式时，该位自动清零。

THLIE位（TX历史列表中断允许）

THLIE位在设置时允许生成TX历史列表中断。

当CANFD模块处于GL_SLEEP模式时，您无法写入该位。

THLIM位（TX历史列表中断模式）

THLIM位选择FIFO的中断产生条件。

当CANFD模块处于GL_SLEEP模式时，您无法写入该位。

当CANFD模块处于GL_HALT或GL_OPERATION模式时，请勿写入该位。

THLDTE位（TX历史列表专用TX使能）

THLDTE位选择在成功发送后将条目存储在TX历史列表中的条件。

You cannot write to this bit when the CANFD module is in GL_SLEEP mode.

Do not write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode.

28.2.49 CFDTHLSTS : TX History List Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x009C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	THLMC[3:0]				—	—	—	—	THLIF	THLELT	THLFLL	THLEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	THLEMP	TX History List Empty 0: TX History List not empty 1: TX History List empty	R
1	THLFLL	TX History List Full 0: TX History List not full 1: TX History List full	R
2	THLELT	TX History List Entry Lost 0: No entry lost in TX History List 1: TX History List entry Lost	R/W
3	THLIF	TX History List Interrupt Flag 0: TX History List interrupt condition not satisfied 1: TX History List interrupt condition satisfied	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
11:8	THLMC[3:0]	TX History List Message Count Number of messages stored in TX History List	R
31:12	—	These bits are read as 0. The write value should be 0.	R/W

The TX History List Status register shows the status of data stored in the TX History List buffer.

THLEMP bit (TX History List Empty)

The THLEMP bit is set automatically when the CPU has read all the entries from the TX History List buffer.

This bit is cleared automatically when the first entry is stored to the TX History List.

This bit is set automatically when:

- TX History List is disabled
- The related CANFD channel is in CH_RESET mode.

THLFLL bit (TX History List Full)

The THLFLL bit is set automatically when the number of entries in the TX History List buffer matches the TX History List depth.

Each TX History List can store up to 8 entries.

This bit is cleared automatically when:

- The number of entries in the TX History List buffer is less than the TX History List depth
- The TX History List is disabled
- The related CANFD channel is in CH_RESET mode.

当CANFD模块处于GL_SLEEP模式时，您无法写入该位。

当CANFD模块处于GL_HALT或GL_OPERATION模式时，请勿写入该位。

28.2.49 CFDTHLSTS:TX历史列表状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x009C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	THLMC[3:0]				—	—	—	—	THLIF	THLELT	THLFLL	THLEMP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	THLEMP	TX历史列表空 0：TX历史列表不为空1：TX历史列表为空	R
1	THLFLL	TX历史列表完整 0：TX历史列表未满1：TX历史列表已满	R
2	THLELT	TX历史列表条目丢失 0：TX历史列表中没有条目丢失1：TX历史列表条目丢失	R/W
3	THLIF	TX历史列表中断标志 0：不满足TX历史列表中断条件1：满足TX历史列表中断条件	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
11:8	THLMC[3:0]	TX历史列表消息计数 TX历史列表中存储的信息数量	R
31:12	—	这些位被读取为0。写入值应为0。	R/W

TX历史列表状态寄存器显示TX历史列表缓冲区中存储的数据的状态。

THLEMP位（TX历史列表空）

当CPU从TXHistoryList缓冲区读取所有条目时，THLEMP位自动置位。

当第一个条目存储到TX历史列表时，该位自动清零。

该位在以下情况下自动设置：

●TX历史列表被禁用

●相关CANFD通道处于CH_RESET模式。

THLFLL位（TX历史列表已满）

当TX历史列表缓冲区中的条目数与TX历史列表深度匹配时，自动设置THLFLL位。

每个TXHistoryList最多可以存储8个条目。

该位在以下情况下自动清零：

●TX历史列表缓冲区中的条目数小于TX历史列表深度

●TX历史列表被禁用

●相关CANFD通道处于CH_RESET模式。

THLELT bit (TX History List Entry Lost)

The THLELT bit is set when a new entry cannot be stored because the related TX History List buffer is already full.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

This bit is cleared:

- By writing 0 to it
- When the related CANFD channel is in CH_RESET mode.

THLIF bit (TX History List Interrupt Flag)

The THLIF bit is set when the configured interrupt condition is satisfied.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

This bit is cleared:

- By writing 0 to it
- When the related CANFD channel is in CH_RESET mode.

The bit is cleared by writing 0 to it.

This bit is automatically cleared in CH_RESET mode.

THLMC[3:0] bits (TX History List Message Count)

The THLMC[3:0] bits show the number of transmitted messages stored in the TX History List.

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

28.2.50 CFDTHLACC0 : TX History List Access Register 0

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0740

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TMTS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	BN[1:0]		BT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	BT[2:0]	Buffer Type 0 0 1: Flat TX message buffer 0 1 0: TX FIFO message buffer number 1 0 0: TX Queue message buffer number	R
4:3	BN[1:0]	Buffer Number Number of the message buffer	R

THLELT位（TX历史列表条目丢失）

当由于相关的TX历史列表缓冲区已满而无法存储新条目时，将设置THLELT位。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

该位被清除：

●写入0

●当相关CANFD通道处于CH_RESET模式时。

THLIF位（TX历史列表中断标志）

当配置的中断条件满足时，THLIF位置位。

仅当相关CANFD通道处于CH_HALT或CH_OPERATION模式时才写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

该位被清除：

●写入0

●当相关CANFD通道处于CH_RESET模式时。

该位通过向其写入0来清除。

该位在CH_RESET模式下自动清零。

THLMC[3:0]位（TX历史列表消息计数）

THLMC[3:0]位显示存储在TX历史列表中的已发送消息的数量。

当相关CANFD通道处于CH_RESET模式时，这些位会自动清零。

28.2.50 CFDTHLACC0：TX历史列表访问寄存器0

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0740

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TMTS[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	BN[1:0]		BT[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	BT[2:0]	缓冲器类型 001：平坦的TX消息缓冲区010：TXFIFO 消息缓冲区号100：TX队列消息缓冲区号	R
4:3	BN[1:0]	缓冲区号 消息缓冲区的编号	R

Bit	Symbol	Function	R/W
15:5	—	These bits are read as 0. The write value should be 0.	R
31:16	TMTS[15:0]	Transmit Timestamp Transmit timestamp value for software drivers	R

The TX History List Access Registers 0 provide access to the entry in the TX History List based on the read timestamp value.

BT[2:0] bits (Buffer Type)

The BT[2:0] bits indicate whether data has been stored following a transmission from a FIFO buffer, a TX Queue or a TX message buffer.

BN[1:0] bits (Buffer Number)

The BN[1:0] bits show the message buffer from which transmission was successfully completed. If a message from a Common FIFO is transmitted, then these bits show the message buffer that is linked to the Common FIFO for transmission.

TMTS[15:0] bits (Transmit Timestamp)

The TMTS[15:0] bits indicate the timestamp for use by software drivers.

28.2.51 CFDTHLACC1 : TX History List Access Register 1

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0744

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TIFL[1:0]		TID[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TID[15:0]	Transmit ID These bits indicate that message buffer reference ID, TX FIFO reference ID, or AFL pointer field is stored for software drivers.	R
17:16	TIFL[1:0]	Transmit Information Label These bits indicate that message buffer information label, TX FIFO information label, or AFL information label is stored for software drivers.	R
31:18	—	These bits are read as 0. The write value should be 0.	R/W

The TX History List Access Registers 1 provide access to entry in the TX History List based on the read pointer value.

TID[15:0] bits (Transmit ID)

The TID[15:0] bits indicate whether the message buffer reference ID (CFDTMFDCTRb.TMPTR) or the TX FIFO reference ID (CFDCFFDCSTS.CFPTR) is for use by software drivers.

TIFL[1:0] bits (Transmit Information Label)

The TIFL[1:0] bits indicate whether the message buffer information label (CFDTMFDCTRb.TMIFL) or the TX FIFO information label (CFDCFFDCSTS.CFIFL) is for use by software drivers.

Bit	Symbol	Function	R/W
15:5	—	这些位被读取为0。写入值应为0。	R
31:16	TMTS[15:0]	传输时间戳 传输软件驱动程序的时间戳值	R

TX历史列表访问寄存器0根据读取的时间戳值提供对TX历史列表中条目的访问。

BT[2:0] bits (Buffer Type)

BT[2:0]位指示数据是否已在从FIFO缓冲区、TX队列或TX消息缓冲区传输后存储。

BN[1:0] bits (Buffer Number)

BN[1:0]位显示成功完成传输的消息缓冲区。如果一个消息来自
传输通用FIFO，然后这些位显示链接到通用FIFO以进行传输的消息缓冲区。

TMTS[15:0] bits (Transmit Timestamp)

TMTS[15:0]位指示软件驱动程序使用的时间戳。

28.2.51 CFDTHLACC1：TX历史列表访问寄存器1

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0744

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TIFL[1:0]		TID[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TID[15:0]	传输ID 这些位指示为软件驱动程序存储消息缓冲区参考ID、TXFIFO参考ID或AFL指针字段。	R
17:16	TIFL[1:0]	传输信息标签 这些位指示为软件驱动程序存储消息缓冲区信息标签、TXFIFO信息标签或AFL信息标签。	R
31:18	—	这些位被读取为0。写入值应为0。	R/W

TX历史列表访问寄存器1根据读取的指针值提供对TX历史列表中条目的访问。

TID[15:0] bits (Transmit ID)

TID[15:0]位指示消息缓冲区参考ID(CFDTMFDCTRb.TMPTR)还是TXFIFO参考
ID(CFDCFFDCSTS.CFPTR)供软件驱动程序使用。

TIFL[1:0]位（发送信息标签）

TIFL[1:0]位指示消息缓冲区信息标签(CFDTMFDCTRb.TMIFL)或TXFIFO信息标签(CFDCFFDCSTS.CFIFL)是否供
软件驱动程序使用。

28.2.52 CFDTHLPCTR : TX History List Pointer Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	THLPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	THLPC[7:0]	TX History List Pointer Control Increments the write pointer to the TX History List in the corresponding channel	W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The TX History List Pointer Control Registers are used to increment the read pointer of the TX History List.

THLPC[7:0] bits (TX History List Pointer Control)

When 0xFF is written to the THLPC[7:0] bits, the read pointer of the TX History List is moved to the next TX History List entry address.

The read value from these bits is always 0x00. Only write to these bits when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

Only write 0xFF to these registers when the corresponding TX History List is enabled and not empty.

28.2.53 CFDGRSTC : Global SW reset Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00D8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	SRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRST	SW Reset 0: Normal state 1: SW reset state	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits control the validity of rewriting of a SRST bit.	W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

SRST bit (SW Reset)

When the SRST bit is set, the CANFD module is in the same state as hardware reset. When a reset is required, write 1 then write 0 to this bit.

This bit is cleared when the CANFD module is in GL_SLEEP mode.

When this bit is cleared, the RAM initialization sequence does not operate. The configuration of RAM is performed by software.

28.2.52 CFDTHLPCTR:TX历史列表指针控制寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	THLPC[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	THLPC[7:0]	TX历史列表指针控制 将写入指针递增到相应通道中的TX历史列表	W
31:8	—	这些位被读取为0。写入值应为0。	R/W

TX历史列表指针控制寄存器用于递增TX历史列表的读指针。

THLPC[7:0]位（TX历史列表指针控制）

当0xFF写入THLPC[7:0]位时，TX历史列表的读指针将移动到下一个TX历史列表条目地址。

从这些位读取的值始终为0x00。仅当相关CANFD通道处于CH_HALT或
CH_OPERATION mode.
仅当相应的TX历史列表启用且不为空时，才向这些寄存器写入0xFF。

28.2.53 CFDGRSTC:全局软件复位寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00D8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	SRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRST	SW Reset 0：正常状态1： 软件复位状态	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位控制SRST位重写的有效性。	W
31:16	—	这些位被读取为0。写入值应为0。	R/W

SRST bit (SW Reset)

当SRST位置位时，CANFD模块处于与硬件复位相同的状态。当需要复位时，先写1然后写0到该位。

当CANFD模块处于GL_SLEEP模式时，该位清零。

当该位清零时，RAM初始化序列不工作。RAM的配置由软件执行。

The RAM is not initialized when software reset is performed during the initialization of RAM. Software must perform the initialization of RAM.

KEY[7:0] bits (Key Code)

When 0xC4 is written in the KEY[15:8] bits, a write to the SRST bit is valid.

The read value from these bits is always 0x00.

CFDGRSTC.SRST bit and the CFDGRSTC.KEY bit should be written simultaneously.

28.2.54 CFDGTSTCFG : Global Test Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00A8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	RTMPS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 0. The write value should be 0.	R/W
19:16	RTMPS[3:0]	RAM Test Mode Page Select Select a RAM test mode page	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The Global Test Configuration Register is used to configure the RAM test mode page.

RTMPS[3:0] bits (RAM Test Mode Page Select)

The RTMPS[3:0] bits select the RAM page mode for CPU read/write access when the CANFD module is configured in RAM test mode.

See section 28.9.2.1. RAM Test Mode for the RAM test mode specification.

Do not write to these bits when the CANFD module is in GL_RESET or GL_SLEEP mode.

Only enter values from 0 to 9 (0x009) for the message buffer RAM.

Only write to these bits when the CANFD module is in GL_HALT mode.

These bits are cleared automatically when the related CANFD channel is in GL_RESET mode.

28.2.55 CFDGTSTCTR : Global Test Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00AC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	RTME	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

在RAM初始化过程中执行软件复位时，RAM不会被初始化。软件必须执行RAM的初始化。

KEY[7:0] bits (Key Code)

当KEY[15:8]位写入0xC4时，写入SRST位有效。

从这些位读取的值始终为0x00。

CFDGRSTC.SRST位和CFDGRSTC.KEY位应同时写入。

28.2.54 CFDGTSTCFG:全局测试配置寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00A8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	RTMPS[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	这些位被读取为0。写入值应为0。	R/W
19:16	RTMPS[3:0]	RAM测试模式页面Select选择 RAM测试模式页面	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

全局测试配置寄存器用于配置RAM测试模式页面。

RTMPS[3:0]位（RAM测试模式页面选择）

当CANFD模块配置为
RAM测试模式。

请参阅第28.9.2.1节。RAM测试模式用于RAM测试模式规范。

当CANFD模块处于GL_RESET或GL_SLEEP模式时，不要写入这些位。

只为消息缓冲区RAM输入0到9(0x009)之间的值。

仅当CANFD模块处于GL_HALT模式时才写入这些位。

当相关CANFD通道处于GL_RESET模式时，这些位会自动清除。

28.2.55 CFDGTTSTCTR:全局测试控制寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00AC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	RTME	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W
2	RTME	RAM Test Mode Enable 0: RAM test mode disabled 1: RAM test mode enabled	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

The Global Test Control register is used to control the global test modes of the CANFD module.

RTME bit (RAM Test Mode Enable)

When the RTME bit is set, the CANFD module is configured in RAM test mode. See section 28.9.2.1. RAM Test Mode for RAM test mode specification.

Only write to this bit when the CANFD module is in GL_HALT mode.

Clear this bit when the CANFD module is in GL_HALT mode.

This bit is cleared automatically when the CANFD module is in GL_RESET mode.

28.2.56 CFDGFDCFG : Global FD Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00B0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TSCCFG[1:0]		—	—	—	—	—	—	—	RPED
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPED	RES Bit Protocol Exception Disable 0: Protocol exception event detection enabled 1: Protocol exception event detection disabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
9:8	TSCCFG[1:0]	Timestamp Capture Configuration 0 0: Timestamp capture at the sample point of SOF (start of frame) 0 1: Timestamp capture at frame valid indication 1 0: Timestamp capture at the sample point of RES bit 1 1: Reserved	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

RPED bit (RES Bit Protocol Exception Disable)

The RPED bit configures the protocol exception event handling according to ISO 11898-1.

When this bit is enabled, the protocol exception event detection is disabled, and the protocol controller transmits an error frame when the protocol exception event is detected (RES bit is sampled recessive).

Only write to this bit when the CANFD module is in GL_RESET mode.

TSCCFG[1:0] bits (Timestamp Capture Configuration)

The TSCCFG[1:0] bits configure the different capture points of the timestamp for transmission and reception.

Bit	Symbol	Function	R/W
0	—	该位读取为0。写入值应为0。	R/W
1	—	该位读取为0。写入值应为0。	R/W
2	RTME	RAM测试模式启用 0：禁用RAM测试模式1：启用RAM测试模式	R/W
31:3	—	这些位被读取为0。写入值应为0。	R/W

全局测试控制寄存器用于控制CANFD模块的全局测试模式。

RTME位（RAM测试模式启用）

当RTME位置位时，CANFD模块配置为RAM测试模式。请参阅第28.9.2.1节。RAM测试模式RAM测试模式规范。

仅当CANFD模块处于GL_HALT模式时写入该位。

CANFD模块处于GL_HALT模式时清零该位。

当CANFD模块处于GL_RESET模式时，该位会自动清零。

28.2.56 CFDGFDCFG:全局FD配置寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00B0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TSCCFG[1:0]		—	—	—	—	—	—	—	RPED
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPED	RES位协议异常禁用 0：启用协议异常事件检测1：禁用协议异常事件检测	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
9:8	TSCCFG[1:0]	时间戳捕获配置 00：在SOF（帧开始）采样点捕获时间戳01：在帧有效指示处捕获时间戳0：在RES位1采样点捕获时间戳1：保留	R/W
31:10	—	这些位被读取为0。写入值应为0。	R/W

RPED位（RES位协议异常禁用）

RPED位根据ISO11898-1配置协议异常事件处理。

当该位被使能时，协议异常事件检测被禁用，并且协议控制器在检测到协议异常事件时发送一个错误帧（RES位被采样为隐性）。

仅当CANFD模块处于GL_RESET模式时写入该位。

TSCCFG[1:0]位（时间戳捕获配置）

TSCCFG[1:0]位配置发送和接收时间戳的不同捕获点。

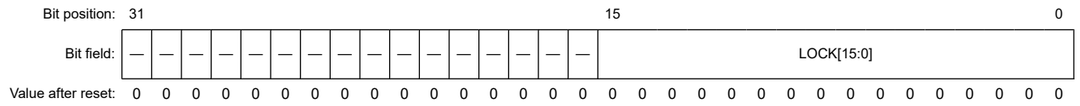
When CFDGFDCFG.TSCCFG[1:0] = 10b, the timestamp capture is performed for CANFD frames at RES bit and for Classical frames at the start of frame.

Only write to these bits when the CANFD module is in GL_RESET mode.

28.2.57 CFDGLOCKK : Global Lock Key Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00B8



Bit	Symbol	Function	R/W
15:0	LOCK[15:0]	Lock Key Key bits for unlocking the protection of test modes	W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The Global Lock Key register is a write-only register that is used to unlock the protection for special test bits.

See section 28.9.2. Global Test Modes for Lock key specification.

LOCK[15:0] bits (Lock Key)

The unlock key sequence must be written in the LOCK[15:0] bits to configure the CANFD module in FIFO OTB disable and RAM test modes.

The read value from these bits is always 0x0000.

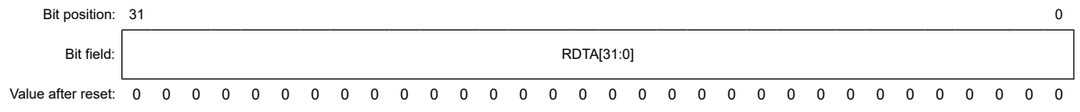
You cannot write to these bits when the CANFD module is in GL_SLEEP or GL_RESET mode.

Do not write to these bits when the CANFD module is in GL_OPERATION mode.

28.2.58 CFDRPGACCk : RAM Test Page Access Registers k (k = 0 to 63)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0280 + 0x0004 × k



Bit	Symbol	Function	R/W
31:0	RDTA[31:0]	RAM Data Test Access RAM data bytes	R/W

RDTA[31:0] bits (RAM Data Test Access)

Data can be read from or written into the RDTA[31:0] bits when the CANFD module is configured in RAM test mode.

Only write to this bit when the CANFD module is in GL_HALT mode and RAM test mode is enabled.

Software data should be read/written in the RAM Test Page Access registers during RAM test mode.

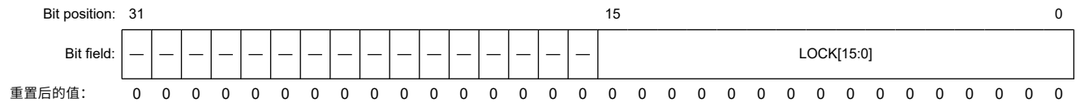
当CFDGFDCFG.TSCCFG[1:0]=10b时，对CANFD帧的RES位执行时间戳捕获，并为帧开始处的经典帧。

仅当CANFD模块处于GL_RESET模式时才写入这些位。

28.2.57 CFDGLOCKK:全局锁定密钥寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00B8



Bit	Symbol	Function	R/W
15:0	LOCK[15:0]	钥匙 用于解锁测试模式保护的密钥位	W
31:16	—	这些位被读取为0。写入值应为0。	R/W

全局锁定密钥寄存器是一个只写寄存器，用于解锁对特殊测试位的保护。

请参阅第28.9.2节。锁键规范的全局测试模式。

LOCK[15:0] bits (Lock Key)

解锁密钥序列必须写入LOCK[15:0]位，以将CANFD模块配置为FIFOOTB禁用和RAM测试模式。

从这些位读取的值始终为0x0000。

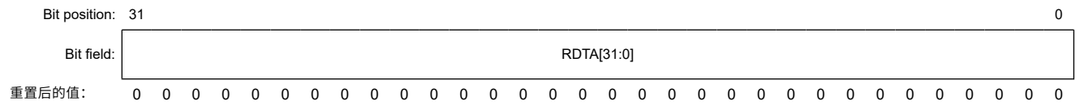
当CANFD模块处于GL_SLEEP或GL_RESET模式时，您无法写入这些位。

当CANFD模块处于GL_OPERATION模式时，不要写入这些位。

28.2.58 CFDRPGACCk：RAM测试页访问寄存器k（k=0到63）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0280 + 0x0004 × k



Bit	Symbol	Function	R/W
31:0	RDTA[31:0]	RAM数据测试访问 RAM数据字节	R/W

RDTA[31:0]位（RAM数据测试访问）

当CANFD模块配置为RAM测试模式时，可以从RDTA[31:0]位读取或写入数据。

仅当CANFD模块处于GL_HALT模式且RAM测试模式启用时写入该位。

在RAM测试模式期间，软件数据应被读取写入RAM测试页访问寄存器。

28.2.59 CFDGAFLIGNENT : Global AFL Ignore Entry Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00C0

Bit position:	31																										4	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IRN[4:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	IRN[4:0]	Ignore Rule Number Define rule number which ignores an AFL entry.	R/W
31:5	—	These bits are read as 0. The write value should be 0.	R/W

IRN[4:0] bits (Ignore Rule Number)

The IRN[4:0] bits define the rule number which updates an AFL entry.

Enter only values between 0 and 31 (0x1F) inclusive.

Only write to these bits when the CFDGAFLIGNCTR.IREN bit is 0.

You cannot write to these bits when the CANFD module is in GL_SLEEP mode.

28.2.60 CFDGAFLIGNCTR : Global AFL Ignore Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00C4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	IREN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IREN	Ignore Rule Enable 0: AFL entry number is not ignored 1: AFL entry number is ignored	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits control the validity of rewriting the IREN bit.	W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

IREN bit (Ignore Rule Enable)

When the IREN bit is set, the entry number (selected by CFDGAFLIGNENT register) is ignored.

This bit is cleared automatically when the CANFD module is in GL_RESET mode.

KEY[7:0] bits (Key Code)

When 0xC4 is written in the KEY[7:0] bits, a write to the IREN bit is valid.

The read value from these bits is always 0x00.

CFDGAFLIGNCTR.IREN bit and the CFDGAFLIGNCTR.KEY bit should be written simultaneously

28.2.59 CFDGAFLIGNENT:全局AFL忽略条目寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00C0

Bit position:	31																										4	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IRN[4:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	IRN[4:0]	忽略规则编号 定义忽略AFL条目的规则编号。	R/W
31:5	—	这些位被读取为0。写入值应为0。	R/W

IRN[4:0]位（忽略规则编号）

IRN[4:0]位定义更新AFL条目的规则编号。

仅输入0到31(0x1F)之间的值（含）。

仅当CFDGAFLIGNCTR.IREN位为0时才写入这些位。

当CANFD模块处于GL_SLEEP模式时，您无法写入这些位。

28.2.60 CFDGAFLIGNCTR:全局AFL忽略控制寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00C4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	IREN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IREN	忽略规则启用 0：不忽略AFL条目号1：忽略AFL条目号	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位控制重写IREN位的有效性。	W
31:16	—	这些位被读取为0。写入值应为0。	R/W

IREN位（忽略规则启用）

当IREN位置位时，条目号（由CFDGAFLIGNENT寄存器选择）被忽略。

当CANFD模块处于GL_RESET模式时，该位会自动清零。

KEY[7:0] bits (Key Code)

当KEY[7:0]位写入0xC4时，写入IREN位有效。

从这些位读取的值始终为0x00。

CFDGAFLIGNCTR.IREN位和CFDGAFLIGNCTR.KEY位应同时写入

28.2.61 CFDRMIEC : RX Message Buffer Interrupt Enable Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0038

Bit position:	31																												0
Bit field:	RMIEg[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	RMIEg[31:0]	RX Message Buffer Interrupt Enable 0: RX Message Buffer Interrupt disabled for corresponding RX message buffer 1: RX Message Buffer Interrupt enabled for corresponding RX message buffer	R/W

These bits show the RX Message Buffer Interrupt Enable for the corresponding RX Message Buffer. CFDRMIEC bit 0 corresponds to RX Message Buffer 0 and so on.

The bit position of CFDRMIEC corresponds to the buffer number of RXMB.

RMIEg[31:0] bit (RX Message Buffer Interrupt Enable)

If this bit is set, then an interrupt will be generated at the end of a successful reception from the corresponding Message Buffer.

Please refer to section 28.7.1. Interrupts.

Users cannot write to this bit when the CANFD module is in GL_SLEEP mode.

28.2.62 Message Buffer Component Structure

28.2.62.1 Start Addresses

The start address for each of the Message Buffer component is calculated using the number of related Message Buffer components.

The start addresses for each register in the Message Buffer component are depicted in Table 28.5.

Table 28.5 Message Buffer Component Register Start Addresses (1 of 2)

b = Message buffer component index	MBCP	p	Register	Start Address
[0…31] b = [0…7]	RMBCPb[0]	x	RMID	0x0920 + b × 0x004C
		x	RMPTR	0x0924 + b × 0x004C
		x	RMFDSTSb	0x0928 + b × 0x004C
		[1…15]	RMDFbp	0x092C + b × 0x004C + p × 0x0004
[0…31] b = [8…15]	RMBCPb[0]	x	RMIDb	0x0D20 + (b-8) × 0x004C
		x	RMPTRb	0x0D24 + (b-8) × 0x004C
		x	RMFDSTSb	0x0D28 + (b-8) × 0x004C
		[1…15]	RMDFbp	0x0D2C + (b-8) × 0x004C + p × 0x0004
[0…31] b = [16…23]	RMBCPb[0]	x	RMIDb	0x1120 + (b-16) × 0x004C
		x	RMPTRb	0x1124 + (b-16) × 0x004C
		x	RMFDSTSb	0x1128 + (b-16) × 0x004C
		[1…15]	RMDFbp	0x112C + (b-16) × 0x004C + p × 0x0004

28.2.61 CFDRMIEC:RX消息缓冲区中断使能配置寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0038

Bit position:	31																												0
Bit field:	RMIEg[31:0]																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	RMIEg[31:0]	RX消息缓冲区中断使能 0：禁止相应RX消息缓冲区的RX消息缓冲区中断1：允许相应RX消息缓冲区的RX消息缓冲区中断	R/W

这些位显示相应RX报文缓冲区的RX报文缓冲区中断使能。CFDRMIEC位0对应于RX消息缓冲区0，依此类推。

CFDRMIEC的位位置对应于RXMB的缓冲区号。

RMIEg[31:0]位（RX报文缓冲区中断使能）

如果该位置位，则在成功接收到相应消息后将产生中断
Buffer.

请参阅第28.7.1节。中断。

CANFD模块处于GL_SLEEP模式时，用户不能写入该位。

28.2.62 消息缓冲区组件结构

28.2.62.1 起始地址

每个消息缓冲区组件的起始地址是使用相关消息缓冲区组件的数量计算的。

消息缓冲区组件中每个寄存器的起始地址如表28.5所示。

Table 28.5 消息缓冲区组件寄存器起始地址(1of2)

b=消息缓冲区组件索引	MBCP	p	Register	起始地址
[0…31] b = [0…7]	RMBCPb[0]	x	RMID	0x0920 + b × 0x004C
		x	RMPTR	0x0924 + b × 0x004C
		x	RMFDSTSb	0x0928 + b × 0x004C
		[1…15]	RMDFbp	0x092C + b × 0x004C + p × 0x0004
[0…31] b = [8…15]	RMBCPb[0]	x	RMIDb	0x0D20 + (b-8) × 0x004C
		x	RMPTRb	0x0D24 + (b-8) × 0x004C
		x	RMFDSTSb	0x0D28 + (b-8) × 0x004C
		[1…15]	RMDFbp	0x0D2C + (b-8) × 0x004C + p × 0x0004
[0…31] b = [16…23]	RMBCPb[0]	x	RMIDb	0x1120 + (b-16) × 0x004C
		x	RMPTRb	0x1124 + (b-16) × 0x004C
		x	RMFDSTSb	0x1128 + (b-16) × 0x004C
		[1…15]	RMDFbp	0x112C + (b-16) × 0x004C + p × 0x0004

Table 28.5 Message Buffer Component Register Start Addresses (2 of 2)

b = Message buffer component index	MBCP	p	Register	Start Address
[0…31] b = [24…31]	RMBCPb[0]	x	RMIDb	0x1520 + (b-24) × 0x004C
		x	RMPTRb	0x1524 + (b-24) × 0x004C
		x	RMFDSTSb	0x1528 + (b-24) × 0x004C
		[1…15]	RMDFbp	0x152C + (b-24) × 0x004C + p × 0x0004
[0…1]	RFMBCPb[0]	x	RFIDb	0x0520 + b × 0x004C
		x	RFPTRb	0x0524 + b × 0x004C
		x	RFFDSTSb	0x0528 + b × 0x004C
		[1…15]	RFDFbp	0x052C + b × 0x004C + p × 0x0004
[0]	CFMBCPb[0]	x	CFID	0x05B8
		x	CFPTR0	0x05BC
		x	CFFDCSTS0	0x05C0
		[1…15]	CFDFp0	0x05C4 + p × 0x0004
[0…3]	TMBCPb[0]	x	TMIDb	0x0604 + b × 0x004C
		x	TMPTRb	0x0608 + b × 0x004C
		x	TMFDCTRb	0x060C + b × 0x004C
		[1…15]	TMDFbp	0x0610 + b × 0x004C + p × 0x0004

The message buffer configuration consists of four types of Message Buffer components:

- RX Message Buffer Component (CFDRMBCPb[0])
- RX FIFO Access Message Buffer Component (CFDRFMBCPb[0])
- Common FIFO Access Message Buffer Component (CFDCFMBCP0[0])
- TX Message Buffer Component (CFDTMBCPb[0]).

Where b = the Message Buffer component index that has a range that varies based on the type of Message Buffer component.

For a summary of this configuration, see Figure 28.29. For a detailed description of the number of and the different types of message buffers, see section 28.6. FIFO Buffers and Normal Message Buffer Configuration.

As described in section 28.2. Register Descriptions, each Message Buffer component consists of the following registers:

- Identifier (ID)
- Pointer (PTR)
- Data Field (DFp).

Where p = the Data Field register index that has a range that varies based on the type of message buffer component.

Rc is the Message Buffer Component register where c = Message Buffer Component register index that has a range that varies based on the type of Message Buffer component.

A description of the registers, their associated bits and their accessibility are shown below the summary and detailed figures of each component.

In each of the figures, a cell that contains '-' means reserved and has the same behavio as reserved bits for registers in section 28.2.62. Message Buffer Component Structure.

Table 28.5 消息缓冲区组件寄存器起始地址(2of2)

b=消息缓冲区组件索引	MBCP	p	Register	起始地址
[0…31] b = [24…31]	RMBCPb[0]	x	RMIDb	0x1520 + (b-24) × 0x004C
		x	RMPTRb	0x1524 + (b-24) × 0x004C
		x	RMFDSTSb	0x1528 + (b-24) × 0x004C
		[1…15]	RMDFbp	0x152C + (b-24) × 0x004C + p × 0x0004
[0…1]	RFMBCPb[0]	x	RFIDb	0x0520 + b × 0x004C
		x	RFPTRb	0x0524 + b × 0x004C
		x	RFFDSTSb	0x0528 + b × 0x004C
		[1…15]	RFDFbp	0x052C + b × 0x004C + p × 0x0004
[0]	CFMBCPb[0]	x	CFID	0x05B8
		x	CFPTR0	0x05BC
		x	CFFDCSTS0	0x05C0
		[1…15]	CFDFp0	0x05C4 + p × 0x0004
[0…3]	TMBCPb[0]	x	TMIDb	0x0604 + b × 0x004C
		x	TMPTRb	0x0608 + b × 0x004C
		x	TMFDCTRb	0x060C + b × 0x004C
		[1…15]	TMDFbp	0x0610 + b × 0x004C + p × 0x0004

消息缓冲区配置由四种类型的消息缓冲区组件组成：

●RX消息缓冲区组件(CFDRMBCPb[0])

●RXFIFO访问消息缓冲区组件(CFDRFMBCPb[0])

●通用FIFO访问消息缓冲区组件(CFDCFMBCP0[0])

●TX消息缓冲区组件(CFDTMBCPb[0])。

其中b=消息缓冲区组件索引，其范围因消息缓冲区组件的类型而异。

有关此配置的摘要，请参见图28.29。有关消息缓冲区的数量和不同类型的详细说明，请参见第28.6节。FIFO缓冲区和正常消息缓冲区配置。

如第28.2节所述。寄存器说明，每个MessageBuffer组件由以下寄存器组成：

- Identifier (ID)
- Pointer (PTR)

●数据字段(DFp)。

其中p=数据字段寄存器索引，其范围根据消息缓冲区组件的类型而变化。

Rc是消息缓冲区组件寄存器，其中c=消息缓冲区组件寄存器索引，其范围根据消息缓冲区组件的类型而变化。

每个组件的摘要和详细图下方显示了寄存器、相关位及其可访问性的描述。

在每个图中，包含"–"的单元格表示保留，并且与第28.2.62节中的寄存器保留位具有相同的行为。消息缓冲区组件结构。

28.2.62.2 CFDRMBCPb[0] : RX Message Buffer Component b (b = 0 to 31)

Base address: CANFD_B = 0x400B_0000

Offset address: See Table 28.5

Bit position:	31																													0
Bit field:	Rc[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	Rc[31:0]	RX Message Buffer Component c Refer to Table 28.6, Table 28.7 and the descriptions that follow for a detailed description of each register and its related bits, contained within this message buffer component.	R/W

Where the total number of CFDRMBCPb = 32 as shown in Figure 28.29 (c = RX Message Buffer Component Register index = [0…18])

Rc[31:0] bit (RX Message Buffer Component c)

The RX Message Buffer Component is made up of the following registers: CFDRMIDb, CFDRMPTRb, CFDRMFDSTSb, and CFDRMDFbp. Refer to Table 28.7 for details of how to interpret the structure of this buffer component and how to access the respective registers.

Table 28.6 RX Message Buffer Component Summary

RX Message Buffer Component (RMBCP)	
Rc	**CANFD mode (CAN_FD_MODE = 1'b1)**
R0	RX Message Buffer (b) ID Registers
R1	RX Message Buffer (b) Pointer Registers
R2	RX Message Buffer (b) CANFD Status Registers
R3	RX Message Buffer (b) Data Field 0 Registers
R4	RX Message Buffer (b) Data Field 1 Registers
R5	RX Message Buffer (b) Data Field 2 Registers
R6	RX Message Buffer (b) Data Field 3 Registers
R7	RX Message Buffer (b) Data Field 4 Registers
R8	RX Message Buffer (b) Data Field 5 Registers
R9	RX Message Buffer (b) Data Field 6 Registers
R10	RX Message Buffer (b) Data Field 7 Registers
R11	RX Message Buffer (b) Data Field 8 Registers
R12	RX Message Buffer (b) Data Field 9 Registers
R13	RX Message Buffer (b) Data Field 10 Registers
R14	RX Message Buffer (b) Data Field 11 Registers
R15	RX Message Buffer (b) Data Field 12 Registers
R16	RX Message Buffer (b) Data Field 13 Registers
R17	RX Message Buffer (b) Data Field 14 Registers
R18	RX Message Buffer (b) Data Field 15 Registers
R[19…31]	—

28.2.62.2 CDFDRMBCPb[0]：RX消息缓冲区组件b（b=0到31）

Base address: CANFD_B = 0x400B_0000

Offset address: 见表28.5

Bit position:	31																													0
Bit field:	Rc[31:0]																													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	Rc[31:0]	RX消息缓冲区组件c 请参阅表28.6、表28.7和随后的说明，以了解有关此消息缓冲区组件中包含的每个寄存器及其相关位的详细说明。	R/W

其中，CFDRMBCPb的总数=32，如图28.29所示（c=RX消息缓冲区组件寄存器索引=[0…18]）

Rc[31:0]位（RX消息缓冲区组件c）

RX报文缓冲区组件由以下寄存器组成：CFDRMIDb、CFDRMPTRb、CFDRMFDSTSb和CFDRMDFbp。有关如何解释此缓冲区组件的结构以及如何访问相应寄存器的详细信息，请参见表28.7。

Table 28.6 RX消息缓冲区组件摘要

RX消息缓冲区组件(RMBCP)	
Rc	**CANFD mode (CAN_FD_MODE = 1'b1)**
R0	RX报文缓冲器(b)ID寄存器
R1	RX报文缓冲区(b)指针寄存器
R2	RX报文缓冲区(b)CANFD状态寄存器
R3	RX报文缓冲区(b)数据字段0寄存器
R4	RX报文缓冲区(b)数据字段1寄存器
R5	RX报文缓冲区(b)数据字段2寄存器
R6	RX报文缓冲区(b)数据字段3寄存器
R7	RX报文缓冲区(b)数据字段4寄存器
R8	RX报文缓冲区(b)数据字段5寄存器
R9	RX报文缓冲区(b)数据字段6寄存器
R10	RX报文缓冲区(b)数据字段7寄存器
R11	RX报文缓冲区(b)数据字段8寄存器
R12	RX报文缓冲区(b)数据字段9寄存器
R13	RX报文缓冲区(b)数据字段10寄存器
R14	RX报文缓冲区(b)数据字段11寄存器
R15	RX报文缓冲区(b)数据字段12寄存器
R16	RX报文缓冲区(b)数据字段13寄存器
R17	RX报文缓冲区(b)数据字段14寄存器
R18	RX报文缓冲区(b)数据字段15寄存器
R[19…31]	—

Table 28.7 RX Message Buffer Component (RMBCP) Detailed

Rc	p	Symbol	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDRMIDb	RMIDE	RMRTR	—	RMID																												
R1	x	CFDRMPTRb	RMDLC				—	—	—	—	—	—	—	—	—	—	—	—	RMTS															
R2	x	CFDRMFDSTSb	RMPTR																—	—	—	—	—	—	RMIFL	—	—	—	—	—	RMFDF	RMBRS	RMESI
R3	0	CFDRMDFbp	RMDB_HH																RMDB_HL															
R[4…18]	[1…15]	CFDRMDFbp	RMDB_HH																RMDB_HL															

28.2.62.3 CFDRMIDb : RX Message Buffer ID Registers (b = 0 to 31)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0920 + 0x004C × b (b = 0 to 7)
0x0D20 + 0x004C × (b - 8) (b = 8 to 15)
0x01120 + 0x004C × (b - 16) (b = 16 to 23)
0x01520 + 0x004C × (b - 24) (b = 24 to 31)

Bit position:	31	30	28	0
Bit field:	RMIDE	RMRTR	—	RMID[28:0]
Value after reset:	0	0	0	0

Bit	Symbol	Function	R/W
28:0	RMID[28:0]	RX Message Buffer ID Field STD-ID/EXT-ID fields	R
29	—	This bit is read as 0. The write value should be 0.	R
30	RMRTR	RX Message Buffer RTR Bit 0: Data frame 1: Remote frame	R
31	RMIDE	RX Message Buffer IDE Bit 0: STD-ID is stored 1: EXT-ID is stored	R

The RX Message Buffer ID Register b (b = 0 to 31) store the ID field, IDE bit, and RTR bit of the received message.

RMID[28:0] bits (RX Message Buffer ID Field)

The RMID[28:0] are the bits of the STD-ID/EXT-ID fields of the message stored in the RX message buffer.

See section 28.2.62.1. Start Addresses for details on how to interpret the structure of this buffer component.

RMRTR bit (RX Message Buffer RTR Bit)

The RMRTR bit shows whether a data frame or a remote frame was stored in the RX message buffer.

Note: There are no remote frames in CANFD format. When a CANFD frame is received, the register reflects the state of the received value (the RRS bit in FD frame format).

RMIDE bit (RX Message Buffer IDE Bit)

The RMIDE bit shows whether message with Standard Identifier or Extended Identifier was stored in the RX message buffer.

Table 28.7 RX消息缓冲区组件(RMBCP)详细信息

Rc	p	Symbol	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDRMIDb	RMIDE	RMRTR	—	RMID																												
R1	x	CFDRMPTRb	RMDLC				—	—	—	—	—	—	—	—	—	—	—	—	RMTS															
R2	x	CFDRMFDSTSb	RMPTR																—	—	—	—	—	—	RMIFL	—	—	—	—	—	RMFDF	RMBRS	RMESI
R3	0	CFDRMDFbp	RMDB_HH																RMDB_HL															
R[4…18]	[1…15]	CFDRMDFbp	RMDB_HH																RMDB_HL															

28.2.62.3 CFDRMIDb：RX消息缓冲区ID寄存器（b=0到31）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0920 + 0x004C × b (b = 0 to 7)
0x0D20 + 0x004C × (b - 8) (b = 8 to 15)
0x01120 + 0x004C × (b - 16) (b = 16 to 23)
0x01520 + 0x004C × (b - 24) (b = 24 to 31)

Bit position:	31	30	28	0
Bit field:	RMIDE	RMRTR	—	RMID[28:0]
重置后的值：	0	0	0	0

Bit	Symbol	Function	R/W
28:0	RMID[28:0]	RX消息缓冲区ID字段 STD-ID/EXT-ID fields	R
29	—	该位读取为0。写入值应为0。	R
30	RMRTR	RX报文缓冲区RTR位 0：数据帧1：远程帧	R
31	RMIDE	RX消息缓冲区IDE位 0：存储STD-ID1：存储EXT-ID	R

RX报文缓冲区ID寄存器b（b=0到31）存储接收报文的ID字段、IDE位和RTR位。

RMID[28:0]位（RX消息缓冲区ID字段）

RMID[28:0]是存储在RX消息缓冲区中的消息的STD-IDEXT-ID字段的位。

请参阅第28.2.62.1节。起始地址以获取有关如何解释此缓冲区组件结构的详细信息。

RMRTR位（RX报文缓冲区RTR位）

RMRTR位显示数据帧或远程帧是否存储在RX报文缓冲区中。

Note: CANFD格式中没有远程帧。当接收到CANFD帧时，寄存器反映接收值的状态（FD帧格式中的RRS位）。

RMIDE位（RX报文缓冲区IDE位）

RMIDE位显示带有标准标识符或扩展标识符的消息是否存储在RX消息缓冲区中。

28.2.62.4 CFDRMPTRb : RX Message Buffer Pointer Registers (b = 0 to 31)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0924 + 0x004C × b (b = 0 to 7)
0x0D24 + 0x004C × (b - 8) (b = 8 to 15)
0x01124 + 0x004C × (b - 16) (b = 16 to 23)
0x01524 + 0x004C × (b - 24) (b = 24 to 31)

Bit position:	31			28												15															0
Bit field:	RMDLC[3:0]				—	—	—	—	—	—	—	—	—	—	—	RMTS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	RMTS[15:0]	RX Message Buffer Timestamp Field Timestamp value stored for the message in the RX message buffer	R
27:16	—	These bits are read as 0. The write value should be 0.	R
31:28	RMDLC[3:0]	RX Message Buffer DLC Field Number of data bytes received in a CAN frame.	R

The RX Message Buffer Pointer Register b (b = 0 to 31) store the DLC and Timestamp fields for the received message.

RMTS[15:0] bits (RX Message Buffer Timestamp Field)

The RMTS[15:0] bits store the timestamp value taken at the capture point as configured by CFDGFDCFG.TSCCFG of the received message.

RMDLC[3:0] bits (RX Message Buffer DLC Field)

The RMDLC[3:0] bits store the number of data bytes that were received in the RX message buffer.

See Table 5 in ISO 11898-1 (2015) Specification for details in defining the number of data bytes that were received.

Note: The maximum capacity of the buffer belongs to CFDRMNB.RMPLS and this is not available in the classical CAN function.

28.2.62.5 CFDRMFDSTSb : RX Message Buffer CANFD Status Registers (b = 0 to 31)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0928 + 0x004C × b (b = 0 to 7)
0x0D28 + 0x004C × (b - 8) (b = 8 to 15)
0x01128 + 0x004C × (b - 16) (b = 16 to 23)
0x01528 + 0x004C × (b - 24) (b = 24 to 31)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	RMPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	RMIFL[1:0]		—	—	—	—	—	RMFDF	RMBRS	RMESI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RMESI*1	Error State Indicator bit 0: CANFD frame received from error active node 1: CANFD frame received from error passive node	R
1	RMBRS*1	Bit Rate Switch bit 0: CANFD frame received with no bit rate switch 1: CANFD frame received with bit rate switch	R

28.2.62.4 CFDRMPTRb：RX消息缓冲区指针寄存器（b=0到31）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0924 + 0x004C × b (b = 0 to 7)
0x0D24 + 0x004C × (b - 8) (b = 8 to 15)
0x01124 + 0x004C × (b - 16) (b = 16 to 23)
0x01524 + 0x004C × (b - 24) (b = 24 to 31)

Bit position:	31			28												15															0
Bit field:	RMDLC[3:0]				—	—	—	—	—	—	—	—	—	—	—	RMTS[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	RMTS[15:0]	RX消息缓冲区时间戳字段 为RX消息缓冲区中的消息存储的时间戳值	R
27:16	—	这些位被读取为0。写入值应为0。	R
31:28	RMDLC[3:0]	RX消息缓冲区DLC字段 CAN帧中接收的数据字节数。	R

RX消息缓冲区指针寄存器b（b=0到31）存储接收消息的DLC和时间戳字段。

RMTS[15:0]位（RX消息缓冲区时间戳字段）

RMTS[15:0]位存储在捕获点获取的时间戳值，由接收到的消息的CFDGFDCFG.TSCCFG配置。

RMDLC[3:0]位（RX消息缓冲区DLC字段）

RMDLC[3:0]位存储在RX报文缓冲区中接收到的数据字节数。

有关定义接收的数据字节数的详细信息，请参见ISO11898-1(2015)规范中的表5。

Note: 缓冲区的最大容量属于CFDRMNB.RMPLS，这在经典CAN功能中不可用。

28.2.62.5 CFDRMFDSTSb：RX报文缓冲区CANFD状态寄存器（b=0到31）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0928 + 0x004C × b (b = 0 to 7)
0x0D28 + 0x004C × (b - 8) (b = 8 to 15)
0x01128 + 0x004C × (b - 16) (b = 16 to 23)
0x01528 + 0x004C × (b - 24) (b = 24 to 31)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	RMPTR[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	RMIFL[1:0]		—	—	—	—	—	RMFDF	RMBRS	RMESI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RMESI*1	错误状态指示位 0：从错误主动节点接收到CANFD帧1：从错误被动节点接收到CANFD帧	R
1	RMBRS*1	比特率切换位 0：接收到CANFD帧，没有比特率切换1：接收到CANFD帧，有比特率切换	R

Bit	Symbol	Function	R/W
2	RMFDF*1	CAN FD Format bit 0: Non CANFD frame received 1: CANFD frame received	R
7:3	—	These bits are read as 0. The write value should be 0.	R
9:8	RMIFL[1:0]	RX Message Buffer Information Label Field	R
15:10	—	These bits are read as 0. The write value should be 0.	R
31:16	RMPTR[15:0]	RX Message Buffer Pointer Field	R

Note 1. This bit is not available in the classical CAN function.

The RX Message Buffer CANFD Status Register b (b = 0 to 31) show the status of the FDF, BRS and ESI bits, and pointer of the received CANFD frame.

RMESI bit (Error State Indicator bit)

The RMESI bit has the same value as the ESI bit of the received CANFD frame.

When the received FDF bit is 0, this means a CAN2.0 frame is received and 0 is stored to this bit.

Note: This bit is not available in the classical CAN function.

RMBRS bit (Bit Rate Switch bit)

The RMBRS bit has the same value as the BRS bit of the received CANFD frame.

When the received FDF bit is 0, this means a CAN2.0 frame is received and 0 is stored to this bit.

Note: This bit is not available in the classical CAN function.

RMFDF bit (CAN FD Format bit)

The RMFDF bit has the same value as the FDF bit of the received CANFD frame.

Note: This bit is not available in the classical CAN function.

RMIFL[1:0] bits (RX Message Buffer Information Label Field)

The RMIFL[1:0] bits store the information label value from the related Global Acceptance Filter List entry.

RMPTR[15:0] bits (RX Message Buffer Pointer Field)

The RMPTR[15:0] bits store the pointer value from the related Global Acceptance Filter List entry.

28.2.62.6 CFDRMDFb_p : RX Message Buffer Data Field p Registers (p = 0 to 15, b = 0 to 31)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x092C + 0x004C × b + 0x0004 × p (b = 0 to 7 , p = 0 to 15)
0x0D2C + 0x004C × (b - 8) + 0x0004 × p (b = 8 to 15 , p = 0 to 15)
0x0112C + 0x004C × (b - 16) + 0x0004 × p (b = 16 to 23 , p = 0 to 15)
0x0152C + 0x004C × (b - 24) + 0x0004 × p (b = 24 to 31 , p = 0 to 15)

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	RMDB_HH[7:0]	RMDB_HL[7:0]	RMDB_LH[7:0]	RMDB_LL[7:0]
Value after reset:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	RMDB_LL[7:0]	RX Message Buffer Data Byte (p × 4)	R
15:8	RMDB_LH[7:0]	RX Message Buffer Data Byte ((p × 4) + 1)	R
23:16	RMDB_HL[7:0]	RX Message Buffer Data Byte ((p × 4) + 2)	R
31:24	RMDB_HH[7:0]*1	RX Message Buffer Data Byte ((p × 4) + 3)	R

Bit	Symbol	Function	R/W
2	RMFDF*1	CANFD格式位 0：接收到非CANFD帧1：接收到CANFD帧	R
7:3	—	这些位被读取为0。写入值应为0。	R
9:8	RMIFL[1:0]	RX消息缓冲区信息标签字段	R
15:10	—	这些位被读取为0。写入值应为0。	R
31:16	RMPTR[15:0]	RX消息缓冲区指针字段	R

注1.该位在经典CAN功能中不可用。

RX报文缓冲区CANFD状态寄存器b（b=0到31）显示FDF、BRS和ESI位的状态，以及接收到的CANFD帧的指针。

RMESI位（错误状态指示位）

RMESI位与接收到的CANFD帧的ESI位具有相同的值。

当接收到的FDF位为0时，表示接收到CAN2.0帧，并将0存储到该位。

Note: 该位在经典CAN功能中不可用。

RMBRS位（比特率切换位）

RMBRS位与接收到的CANFD帧的BRS位具有相同的值。

当接收到的FDF位为0时，表示接收到CAN2.0帧，并将0存储到该位。

Note: 该位在经典CAN功能中不可用。

RMFDF位（CANFD格式位）

RMFDF位与接收到的CANFD帧的FDF位具有相同的值。

Note: 该位在经典CAN功能中不可用。

RMIFL[1:0]位（RX消息缓冲区信息标签字段）

RMIFL[1:0]位存储来自相关全局接受过滤器列表条目的信息标签值。

RMPTR[15:0]位（RX消息缓冲区指针字段）

RMPTR[15:0]位存储来自相关全局接受过滤器列表条目的指针值。

28.2.62.6 CFDRMDFb_p：RX消息缓冲区数据字段p寄存器（p=0到15，b=0到31）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x092C + 0x004C × b + 0x0004 × p (b = 0 to 7 , p = 0 to 15)
0x0D2C + 0x004C × (b - 8) + 0x0004 × p (b = 8 to 15 , p = 0 to 15)
0x0112C + 0x004C × (b - 16) + 0x0004 × p (b = 16 to 23 , p = 0 to 15)
0x0152C + 0x004C × (b - 24) + 0x0004 × p (b = 24 to 31 , p = 0 to 15)

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	RMDB_HH[7:0]	RMDB_HL[7:0]	RMDB_LH[7:0]	RMDB_LL[7:0]
重置后的值:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	RMDB_LL[7:0]	RX消息缓冲区数据字节(p×4)	R
15:8	RMDB_LH[7:0]	RX消息缓冲区数据字节((p×4)+1)	R
23:16	RMDB_HL[7:0]	RX报文缓冲区数据字节((p×4)+2)	R
31:24	RMDB_HH[7:0]*1	RX消息缓冲区数据字节((p×4)+3)	R

Note 1. These bits are not available in the classical CAN function.

The RX Message Buffer Data Field p Register b (p = 0 to 15, b = 0 to 31) store the data bytes (p × 4) to data bytes ((p × 4) + 3) of the received message.

RMDB_LL[7:0] bits (RX Message Buffer Data Byte (p × 4))

The RMDB_LL[7:0] bits store data bytes (p × 4) of the message in the RX message buffer.

Unused data bytes are filled with 0x00.

RMDB_LH[7:0] bits (RX Message Buffer Data Byte ((p × 4) + 1))

The RMDB_LH[7:0] bits store data bytes ((p × 4) + 1) of the message in the RX message buffer.

Unused Data Bytes will be filled with 0x00.

RMDB_HL[7:0] bits (RX Message Buffer Data Byte ((p × 4) + 2))

The RMDB_HL[7:0] bits store data bytes ((p × 4) + 2) of the message in the RX message buffer.

Unused data bytes are filled with 0x00.

RMDB_HH[7:0] bits (RX Message Buffer Data Byte ((p × 4) + 3))

The RMDB_HH[7:0] bits store data bytes ((p × 4) + 3) of the message in the RX message buffer.

Unused data bytes are filled with 0x00.

28.2.62.7 CFDRFMBCPb[0] : RX FIFO Access Message Buffer Component b (b = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: see Table 28.5

Bit position:	31																													0
Bit field:	Rc[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	Rc[31:0]	RX FIFO Access Message Buffer Component c See Table 28.8, Table 28.9 and the descriptions that follow for a detailed description of each register and its related bits, contained within this message buffer component.	R

Where the total number of CFDRFMBCPb = 2 as shown in Figure 28.29 (c = RX FIFO Access Message Buffer Component Register index = [0…18])

Rc[31:0] bits (RX FIFO Access Message Buffer Component c)

The RX FIFO Access Message Buffer component comprises of the following registers:

- CFDRFIDb
- CFDRFPTRb
- CFDRFFDSTSb
- CFDRFDFbp

See Table 28.9 for details on how to interpret the structure of this buffer component and how to access the respective registers.

Table 28.8 RX FIFO Access Message Buffer component summary (1 of 2)

Rc	
R0	RX FIFO Access ID Registers
R1	RX FIFO Access Pointer Register

注1.这些位在经典CAN功能中不可用。

RX报文缓冲区数据字段p寄存器b（p=0到15，b=0到31）存储接收到的报文的数据字节（p×4）到数据字节（（p×4）+3）。

RMDB_LL[7:0]位（RX消息缓冲区数据字节(p×4)）

RMDB_LL[7:0]位将消息的数据字节(p×4)存储在RX消息缓冲区中。

未使用的数据字节用0x00填充。

RMDB_LH[7:0]位（RX报文缓冲区数据字节((p×4)+1)）

RMDB_LH[7:0]位将消息的数据字节((p×4)+1)存储在RX消息缓冲区中。

未使用的数据字节将用0x00填充。

RMDB_HL[7:0]位（RX消息缓冲区数据字节((p×4)+2)）

RMDB_HL[7:0]位将消息的数据字节((p×4)+2)存储在RX消息缓冲区中。

未使用的数据字节用0x00填充。

RMDB_HH[7:0]位（RX消息缓冲区数据字节((p×4)+3)）

RMDB_HH[7:0]位将消息的数据字节((p×4)+3)存储在RX消息缓冲区中。

未使用的数据字节用0x00填充。

28.2.62.7 CFDRFMBCPb[0]：RXFIFO访问消息缓冲区组件b（b=0到1）

Base address: CANFD_B = 0x400B_0000

Offset address: 见表28.5

Bit position:	31																													0
Bit field:	Rc[31:0]																													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	Rc[31:0]	RXFIFO访问报文缓冲区组件c 请参阅表28.8、表28.9和随后的描述，了解此消息缓冲区组件中包含的每个寄存器及其相关位的详细描述。	R

其中CFDRFMBCPb的总数=2，如图28.29所示（c=RXFIFO访问消息缓冲区组件寄存器索引=[0…18]）

Rc[31:0]位（RXFIFO访问消息缓冲区组件c）

RXFIFO访问报文缓冲区组件包含以下寄存器：

- CFDRFIDb
- CFDRFPTRb
- CFDRFFDSTSb
- CFDRFDFbp

有关如何解释此缓冲区组件的结构以及如何访问相应寄存器的详细信息，请参见表28.9。

Table 28.8 RXFIFO访问消息缓冲区组件摘要（1of2）

Rc	
R0	RXFIFO访问ID寄存器
R1	RXFIFO访问指针寄存器

Table 28.8 RX FIFO Access Message Buffer component summary (2 of 2)

Rc	
R2	RX FIFO Access CANFD Status Registers
R3	RX FIFO Access Data Field 0 Registers
R4	RX FIFO Access Data Field 1 Registers
R5	RX FIFO Access Data Field 2 Registers
R6	RX FIFO Access Data Field 3 Registers
R7	RX FIFO Access Data Field 4 Registers
R8	RX FIFO Access Data Field 5 Registers
R9	RX FIFO Access Data Field 6 Registers
R10	RX FIFO Access Data Field 7 Registers
R11	RX FIFO Access Data Field 8 Registers
R12	RX FIFO Access Data Field 9 Registers
R13	RX FIFO Access Data Field 10 Registers
R14	RX FIFO Access Data Field 11 Registers
R15	RX FIFO Access Data Field 12 Registers
R16	RX FIFO Access Data Field 13 Registers
R17	RX FIFO Access Data Field 14 Registers
R18	RX FIFO Access Data Field 15 Registers
R[19...31]	—

Table 28.9 RX Message Buffer Component (RMBCP) Detailed

Rc	p	Symbol	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDRMIDb	RMIDE	RMRTR	—	RMID																												
R1	x	CFDRMPTRb	RMDLC																—	—	—	—	—	—	—	—	—	—	RMTS					
R2	x	CFDRMFDSTSb	RMPTR																—	—	—	—	—	—	RMIFL		—	—	—	—	—	RMFDF	RMBRS	RMESI
R3	0	CFDRMDFbp	RMDB_HH																RMDB_HL															
R[4…18]	[1…15]	CFDRMDFbp	RMDB_HH																RMDB_HL															

28.2.62.8 CFDRFIDb : RX FIFO Access ID Register b (b = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0520 + 0x004C × b

Bit position:	31	30	28	0
Bit field:	RFIDE	RFRTR	—	RFID[28:0]
Value after reset:	0	0	0	0

Table 28.8 RXFIFO访问消息缓冲区组件摘要（2之2）

Rc	
R2	RXFIFO访问CANFD状态寄存器
R3	RXFIFO访问数据字段0寄存器
R4	RXFIFO访问数据字段1寄存器
R5	RXFIFO访问数据字段2寄存器
R6	RXFIFO访问数据字段3寄存器
R7	RXFIFO访问数据字段4寄存器
R8	RXFIFO访问数据字段5寄存器
R9	RXFIFO访问数据字段6寄存器
R10	RXFIFO访问数据字段7寄存器
R11	RXFIFO访问数据字段8寄存器
R12	RXFIFO访问数据字段9寄存器
R13	RXFIFO访问数据字段10寄存器
R14	RXFIFO访问数据字段11寄存器
R15	RXFIFO访问数据字段12寄存器
R16	RXFIFO访问数据字段13寄存器
R17	RXFIFO访问数据字段14寄存器
R18	RXFIFO访问数据字段15寄存器
R[19...31]	—

Table 28.9 RX消息缓冲区组件(RMBCP)详细信息

Rc	p	Symbol	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDRMIDb	RMIDE	RMRTR	—	RMID																												
R1	x	CFDRMPTRb	RMDLC																—	—	—	—	—	—	—	—	—	—	RMTS					
R2	x	CFDRMFDSTSb	RMPTR																—	—	—	—	—	—	RMIFL		—	—	—	—	—	RMFDF	RMBRS	RMESI
R3	0	CFDRMDFbp	RMDB_HH																RMDB_HL															
R[4…18]	[1…15]	CFDRMDFbp	RMDB_HH																RMDB_HL															

28.2.62.8 CFDRFIDb：RXFIFO访问ID寄存器b（b=0到1）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0520 + 0x004C × b

Bit position:	31	30	28	0
Bit field:	RFIDE	RFRTR	—	RFID[28:0]
重置后的值：	0	0	0	0

Bit	Symbol	Function	R/W
28:0	RFID[28:0]	RX FIFO Buffer ID Field STD-ID/EXT-ID fields	R
29	—	This bit is read as 0.	R
30	RFRTR	RX FIFO Buffer RTR bit 0: Data frame 1: Remote frame	R
31	RFIDE	RX FIFO Buffer IDE bit 0: STD-ID has been received 1: EXT-ID has been received	R

The RX FIFO Access ID Registers b (b = 0 to 1) store the ID field, IDE bit and RTR bit of the message.

RFID[28:0] bits (RX FIFO Buffer ID Field)

The RFID[28:0] bits are the bits of the STD-ID/EXT-ID fields of the message in the FIFO buffer.

For alignment of these bits in standard and extended frame format, see Identifier Bits Alignment.

RFRTR bit (RX FIFO Buffer RTR bit)

The RFRTR bit shows whether a data frame or a remote frame was stored in the FIFO buffer.

Note: There are no remote frames in CANFD format. When a CANFD frame was received, the register reflects the state of the received value (RRS bit in FD frame format).

RFIDE bit (RX FIFO Buffer IDE bit)

The RFIDE bit shows whether message with the Standard Identifier or Extended Identifier was received in the FIFO buffer.

28.2.62.9 CFDRFPTRb : RX FIFO Access Pointer Register b (b = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0524 + 0x004C × b

Bit position:	31	28														15														0
Bit field:	RFDLC[3:0]				—	—	—	—	—	—	—	—	—	—	—	RFTS[15:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	RFTS[15:0]	RX FIFO Timestamp Value Timestamp value of the received CAN frame	R
27:16	—	These bits are read as 0. The write value should be 0.	R
31:28	RFDLC[3:0]	RX FIFO Buffer DLC Field Number of data bytes received in a CAN frame	R

The FIFO Access Pointer Registers b (b = 0 to 1) store the DLC and Timestamp fields for the received message.

RFTS[15:0] bits (RX FIFO Timestamp Value)

The RFTS[15:0] bits store the timestamp value taken at the capture point as configured by the CFDGFDCFG.TSCCFG bit of the received message.

RFDLC[3:0] bits (RX FIFO Buffer DLC Field)

The RFDLC[3:0] bits store the number of data bytes that were received in the RX FIFO buffer.

See Table 5 in ISO 11898-1 (2015) Specification for details in defining the number of data bytes that were received.

Bit	Symbol	Function	R/W
28:0	RFID[28:0]	RXFIFO缓冲区ID字段 STD-ID/EXT-ID fields	R
29	—	该位读为0。	R
30	RFRTR	RXFIFO缓冲区RTR位 0：数据帧1：远程帧	R
31	RFIDE	RXFIFO缓冲器IDE位 0：接收到STD-ID1：接收到EXT-ID	R

RXFIFO访问ID寄存器b（b=0到1）存储消息的ID字段、IDE位和RTR位。

RFID[28:0]位（RXFIFO缓冲区ID字段）

RFID[28:0]位是FIFO缓冲区中消息的STD-IDEXT-ID字段的位。

有关标准和扩展帧格式中这些位的对齐方式，请参阅标识符位对齐。

RFRTR位（RXFIFO缓冲器RTR位）

RFRTR位显示数据帧或远程帧是否存储在FIFO缓冲区中。

Note: CANFD格式中没有远程帧。当接收到CANFD帧时，寄存器反映接收值的状态（FD帧格式中的RRS位）。

RFIDE位（RXFIFO缓冲器IDE位）

RFIDE位显示在FIFO缓冲区中是否接收到带有标准标识符或扩展标识符的消息。

28.2.62.9 CFDRFPTRb：RXFIFO访问指针寄存器b（b=0到1）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0524 + 0x004C × b

Bit position:	31	28														15														0
Bit field:	RFDLC[3:0]				—	—	—	—	—	—	—	—	—	—	—	RFTS[15:0]														
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	RFTS[15:0]	RXFIFO时间戳值 接收到的CAN帧的时间戳值	R
27:16	—	这些位被读取为0。写入值应为0。	R
31:28	RFDLC[3:0]	RXFIFO缓冲区DLC字段 CAN帧中接收的数据字节数	R

FIFO访问指针寄存器b（b=0到1）存储接收消息的DLC和时间戳字段。

RFTS[15:0]位（RXFIFO时间戳值）

RFTS[15:0]位存储在捕获点获取的时间戳值，由接收到的消息的CFDGFDCFG.TSCCFG位配置。

RFDLC[3:0]位（RXFIFO缓冲区DLC字段）

RFDLC[3:0]位存储在RXFIFO缓冲区中接收到的数据字节数。

有关定义接收的数据字节数的详细信息，请参见ISO11898-1(2015)规范中的表5。

28.2.62.10 CFDRFFDSTSb : RX FIFO Access CANFD Status Register b (b = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0528 + 0x004C × b

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFDRFPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	RFIFL[1:0]		—	—	—	—	—	RFFDF	RFBRS	RFESI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFESI*1	Error State Indicator bit 0: CANFD frame received from error active node 1: CANFD frame received from error passive node	R
1	RFBRS*1	Bit Rate Switch bit 0: CANFD frame received with no bit rate switch 1: CANFD frame received with bit rate switch	R
2	RFFDF*1	CAN FD Format bit 0: Non CANFD frame received 1: CANFD frame received	R
7:3	—	These bits are read as 0. The write value should be 0.	R
9:8	RFIFL[1:0]	RX FIFO Buffer Information Label Field	R
15:10	—	These bits are read as 0. The write value should be 0.	R
31:16	CFDRFPTR[15:0]	RX FIFO Buffer Pointer Field	R

Note 1. This bit is not available in the classical CAN function.

The RX FIFO Access CANFD Status Registers b (b = 0 to 1) show the status of the FDF, BRS, and ESI bits, including the pointer of the received CANFD frame.

RFESI bit (Error State Indicator bit)

The RFESI bit has the same value as the ESI bit of the received CANFD frame.

When the received FDF bit is 0, this means a CAN2.0 frame is received and 0 is stored to this bit.

Note: This bit is not available in the classical CAN function.

RFBRS bit (Bit Rate Switch bit)

The RFBRS bit has the same value as the BRS bit of the received CANFD frame.

When the received FDF bit is 0, this means a CAN2.0 frame is received and 0 is stored to this bit.

Note: This bit is not available in the classical CAN function.

RFFDF bit (CAN FD Format bit)

The RFFDF bit has the same value as the FDF bit of the received CANFD frame.

Note: This bit is not available in the classical CAN function.

RFIFL[1:0] bits (RX FIFO Buffer Information Label Field)

The RFIFL[1:0] bits store the information label value from the related Global Acceptance Filter List entry.

CFDRFPTR[15:0] bits (RX FIFO Buffer Pointer Field)

The CFDRFPTR[15:0] bits store the pointer value from the related Global Acceptance Filter List entry.

28.2.62.10 CFDRFFDSTSb：RXFIFO访问CANFD状态寄存器b（b=0到1）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0528 + 0x004C × b

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFDRFPTR[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	RFIFL[1:0]		—	—	—	—	—	RFFDF	RFBRS	RFESI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFESI*1	错误状态指示位 0：从错误主动节点接收到CANFD帧1：从错误被动节点接收到CANFD帧	R
1	RFBRS*1	比特率切换位 0：接收到CANFD帧，没有比特率切换1：接收到CANFD帧，有比特率切换	R
2	RFFDF*1	CANFD格式位 0：接收到非CANFD帧1：接收到CANFD帧	R
7:3	—	这些位被读取为0。写入值应为0。	R
9:8	RFIFL[1:0]	RXFIFO缓冲区信息标签字段	R
15:10	—	这些位被读取为0。写入值应为0。	R
31:16	CFDRFPTR[15:0]	RXFIFO缓冲区指针字段	R

注1.该位在经典CAN功能中不可用。

RXFIFO访问CANFD状态寄存器b（b=0到1）显示FDF、BRS和ESI位的状态，包括接收到的CANFD帧的指针。

RFESI位（错误状态指示位）

RFESI位与接收到的CANFD帧的ESI位具有相同的值。

当接收到的FDF位为0时，表示接收到CAN2.0帧，并将0存储到该位。

Note: 该位在经典CAN功能中不可用。

RFBRS位（比特率切换位）

RFBRS位与接收到的CANFD帧的BRS位具有相同的值。

当接收到的FDF位为0时，表示接收到CAN2.0帧，并将0存储到该位。

Note: 该位在经典CAN功能中不可用。

RFFDF位（CANFD格式位）

RFFDF位与接收到的CANFD帧的FDF位具有相同的值。

Note: 该位在经典CAN功能中不可用。

RFIFL[1:0]位（RXFIFO缓冲区信息标签字段）

RFIFL[1:0]位存储来自相关全局接受过滤器列表条目的信息标签值。

CFDRFPTR[15:0]位（RXFIFO缓冲区指针字段）

CFDRFPTR[15:0]位存储来自相关全局接受过滤器列表条目的指针值。

28.2.62.11 CFDRFDFb_p : RX FIFO Access Data Field p Register b (p = 0 to 15, b = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x052C + 0x004 × p + 0x04C × b

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	RFDB_HH[7:0]	RFDB_HL[7:0]	RFDB_LH[7:0]	RFDB_LL[7:0]
Value after reset:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	RFDB_LL[7:0]	RX FIFO Buffer Data Byte (p × 4)	R
15:8	RFDB_LH[7:0]	RX FIFO Buffer Data Byte ((p × 4) + 1)	R
23:16	RFDB_HL[7:0]	RX FIFO Buffer Data Byte ((p × 4) + 2)	R
31:24	RFDB_HH[7:0]	RX FIFO Buffer Data Byte ((p × 4) + 3)	R

The RX FIFO Access Data Field p Registers b (p = 0 to 15, b = 0 to 1) store data bytes ((p × 4) to data byte ((p × 4) + 3) of the received message.

RFDB_LL[7:0] bits (RX FIFO Buffer Data Byte (p × 4))

The RFDB_LL[7:0] bits store data bytes (p × 4) of the message present in the FIFO buffer.

Unused data bytes are filled with 0x00 according to the configured data payload size CFDRFCCa.RFPLS.

RFDB_LH[7:0] bits (RX FIFO Buffer Data Byte ((p × 4) + 1))

The RFDB_LH[7:0] bits store data bytes ((p × 4) + 1)) of the message present in the FIFO buffer.

Unused data bytes are filled with 0x00.

RFDB_HL[7:0] bits (RX FIFO Buffer Data Byte ((p × 4) + 2))

The RFDB_HL[7:0] bits store data bytes ((p × 4) + 2) of the message present in the FIFO buffer.

Unused data bytes are filled with 0x00.

RFDB_HH[7:0] bits (RX FIFO Buffer Data Byte ((p × 4) + 3))

The RFDB_HH[7:0] bits store data bytes ((p × 4) + 3) of the message present in the FIFO buffer.

Unused data bytes are filled with 0x00.

28.2.62.12 CFDCFMBCP0[0] : Common FIFO Access Message Buffer Component

Base address: CANFD_B = 0x400B_0000

Offset address: See Table 28.5

Bit position:	31 … 0
Bit field:	Rc[31:0]
Value after reset:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
31:0	Rc[31:0]	Common FIFO Access Message Buffer Component c Refer to Table 28.10, Table 28.11 and the descriptions that follow for a detailed description of each register and its related bits, contained within this message buffer component.	R

Where the total number of CFDCFMBCP0 = 1 as shown in Figure 28.29 (c = Common FIFO Message Buffer Component Register index = [0…18])

28.2.62.11 CFDRFDFb_p：RXFIFO访问数据字段p寄存器b（p=0到15，b=0到1）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x052C + 0x004 × p + 0x04C × b

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	RFDB_HH[7:0]	RFDB_HL[7:0]	RFDB_LH[7:0]	RFDB_LL[7:0]
重置后的值：	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	RFDB_LL[7:0]	RXFIFO缓冲区数据字节(p×4)	R
15:8	RFDB_LH[7:0]	RXFIFO缓冲区数据字节((p×4)+1)	R
23:16	RFDB_HL[7:0]	RXFIFO缓冲区数据字节((p×4)+2)	R
31:24	RFDB_HH[7:0]	RXFIFO缓冲区数据字节((p×4)+3)	R

RXFIFO访问数据字段p寄存器b(p=0到15，b=0到1)存储接收到的报文的数据字节((p×4)到数据字节((p×4)+3)。

RFDB_LL[7:0]位（RXFIFO缓冲区数据字节(p×4)）

RFDB_LL[7:0]位存储FIFO缓冲区中存在的消息的数据字节(p×4)。

根据配置的数据有效负载大小CFDRFCCa.RFPLS用0x00填充未使用的数据字节。

RFDB_LH[7:0]位（RXFIFO缓冲区数据字节((p×4)+1)）

RFDB_LH[7:0]位存储FIFO缓冲区中存在的消息的数据字节((p×4)+1))。

未使用的数据字节用0x00填充。

RFDB_HL[7:0]位（RXFIFO缓冲区数据字节((p×4)+2)）

RFDB_HL[7:0]位存储FIFO缓冲区中存在的消息的数据字节((p×4)+2)。

未使用的数据字节用0x00填充。

RFDB_HH[7:0]位（RXFIFO缓冲区数据字节((p×4)+3)）

RFDB_HH[7:0]位存储FIFO缓冲区中存在的消息的数据字节((p×4)+3)。

未使用的数据字节用0x00填充。

28.2.62.12 CFDCFMBCP0[0]：通用FIFO访问消息缓冲区组件

Base address: CANFD_B = 0x400B_0000

Offset address: 见表28.5

Bit position:	31 … 0
Bit field:	Rc[31:0]
重置后的值：	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
31:0	Rc[31:0]	通用FIFO访问消息缓冲区组件c 请参阅表28.10、表28.11和随后的描述，了解该消息缓冲区组件中包含的每个寄存器及其相关位的详细描述。	R

其中CFDCFMBCP0的总数=1，如图28.29所示（c=通用FIFO消息缓冲区组件寄存器索引=[0…18]）

Rc[31:0] bit (Common FIFO Access Message Buffer Component c)

The Common FIFO Access Message Buffer Component is made up of the following registers: CFDCFID, CFDCFPTR, CFFDSTS0, and CFDCFDFp. Refer to Table 28.11 for details of how to interpret the structure of this buffer component and how to access the respective registers.

Table 28.10 Common FIFO Access Message Buffer Component Summary

Common FIFO Access Message Buffer Component (CFMBCP)	
Rc	**CANFD mode (CAN_FD_MODE = 1'b1)**
R0	Common FIFO Access ID Registers
R1	Common FIFO Access Pointer Register
R2	Common FIFO Access CANFD Status Registers
R3	Common FIFO Access Data Field 0 Registers
R4	Common FIFO Access Data Field 1 Registers
R5	Common FIFO Access Data Field 2 Registers
R6	Common FIFO Access Data Field 3 Registers
R7	Common FIFO Access Data Field 4 Registers
R8	Common FIFO Access Data Field 5 Registers
R9	Common FIFO Access Data Field 6 Registers
R10	Common FIFO Access Data Field 7 Registers
R11	Common FIFO Access Data Field 8 Registers
R12	Common FIFO Access Data Field 9 Registers
R13	Common FIFO Access Data Field 10 Registers
R14	Common FIFO Access Data Field 11 Registers
R15	Common FIFO Access Data Field 12 Registers
R16	Common FIFO Access Data Field 13 Registers
R17	Common FIFO Access Data Field 14 Registers
R18	Common FIFO Access Data Field 15 Registers
R[19…31]	—

Table 28.11 Common FIFO Access Message Buffer Component (CFMBCP) Detailed

Rc	p	Symbol	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDCFID	CFIDE	CFRTR	THLEN	CFID																												
R1	x	CFDCFPTR	CFDLC				—	—	—	—	—	—	—	—	—	—	—	—	CFTS															
R2	x	CFDCFFDCSTS	CFPTR																—	—	—	—	—	—	CFIFL	—	—	—	—	—	CFFDF	CFBRS	CFESI
R3	0	CFDCFDFp	CFDB_HH								CFDB_HL								CFDB_LH							CFDB_LL							
R[4…18]	[1…15]	CFDCFDFp	CFDB_HH								CFDB_HL								CFDB_LH							CFDB_LL							
R[19…31]	x	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Rc[31:0]位（通用FIFO访问消息缓冲区组件c）

通用FIFO访问消息缓冲区组件由以下寄存器组成：CFDCFID、CFDCFPTR、CFFDSTS0和CFDCFDFp。有关如何解释此缓冲区组件的结构以及如何访问相应寄存器的详细信息，请参阅表28.11。

Table 28.10 通用FIFO访问消息缓冲区组件摘要

通用FIFO访问消息缓冲区组件(CFMBCP)	
Rc	**CANFD mode (CAN_FD_MODE = 1'b1)**
R0	通用FIFO访问ID寄存器
R1	通用FIFO访问指针寄存器
R2	通用FIFO访问CANFD状态寄存器
R3	通用FIFO访问数据字段0寄存器
R4	通用FIFO访问数据字段1寄存器
R5	通用FIFO访问数据字段2寄存器
R6	通用FIFO访问数据字段3寄存器
R7	通用FIFO访问数据字段4寄存器
R8	通用FIFO访问数据字段5寄存器
R9	通用FIFO访问数据字段6寄存器
R10	通用FIFO访问数据字段7寄存器
R11	通用FIFO访问数据字段8寄存器
R12	通用FIFO访问数据字段9寄存器
R13	通用FIFO访问数据字段10寄存器
R14	通用FIFO访问数据字段11寄存器
R15	通用FIFO访问数据字段12寄存器
R16	通用FIFO访问数据字段13寄存器
R17	通用FIFO访问数据字段14寄存器
R18	通用FIFO访问数据字段15寄存器
R[19…31]	—

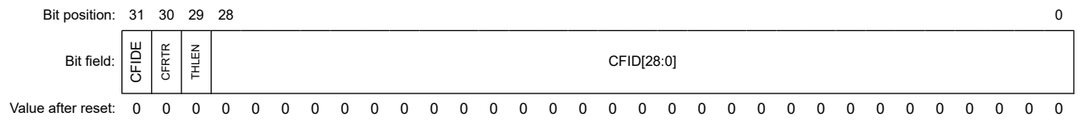
Table 28.11 通用FIFO访问消息缓冲区组件(CFMBCP)详解

Rc	p	Symbol	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDCFID	CFIDE	CFRTR	THLEN	CFID																												
R1	x	CFDCFPTR	CFDLC				—	—	—	—	—	—	—	—	—	—	—	—	CFTS															
R2	x	CFDCFFDCSTS	CFPTR																—	—	—	—	—	—	CFIFL	—	—	—	—	—	CFFDF	CFBRS	CFESI
R3	0	CFDCFDFp	CFDB_HH								CFDB_HL								CFDB_LH							CFDB_LL							
R[4…18]	[1…15]	CFDCFDFp	CFDB_HH								CFDB_HL								CFDB_LH							CFDB_LL							
R[19…31]	x	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

28.2.62.13 CFDCFID : Common FIFO Access ID Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x05B8



Bit	Symbol	Function	R/W
28:0	CFID[28:0]	Common FIFO Buffer ID Field STD-ID / EXT-ID fields	R/W
29	THLEN	THL Entry enable TX FIFO Mode: 0: Entry will not be stored in THL after successful TX. 1: Entry will be stored in THL after successful TX. RX FIFO Mode: Reserved, this bit is read as 0	R/W
30	CFRTR	Common FIFO Buffer RTR Bit 0: Data Frame 1: Remote Frame	R/W
31	CFIDE	Common FIFO Buffer IDE Bit 0: STD-ID will be transmitted or has been received 1: EXT-ID will be transmitted or has been received	R/W

The Common FIFO Access ID registers store the ID field, IDE bit and RTR bit of the message.

In TX mode, users can read data from the FIFO, only for the current entry based on the write pointer value, not for the other entries.

CFID[28:0] bit (Common FIFO Buffer ID Field)

These are the bits of the STD-ID / EXT-ID fields of the message in the FIFO Buffer.

In TX mode, users can write and read from FIFO buffers.

In RX mode, users can only read data from FIFO buffers.

THLEN bit (THL Entry enable)

This bit controls the storage of an entry corresponding to the transmitted message in the TX History list at the end of a successful transmission.

In TX mode, users can write and read from FIFO buffers.

In RX mode, users can only read data from FIFO buffers.

CFRTR bit (Common FIFO Buffer RTR Bit)

This bit selects whether a Data Frame or a Remote Frame will be transmitted from or was received in the FIFO Buffer.

Note: There are no remote frames in CANFD format. In case a CANFD frame was received (RX mode) the register reflects the state of the received value (RRS bit in FD frame format). In case of CANFD transmission (TX mode CFDCFID.CFFDF =1) the bit is always transmitted dominant (Data Frame).

In TX mode, users can write and read from FIFO buffers.

In RX mode, users can only read data from FIFO buffers.

CFIDE bit (Common FIFO Buffer IDE Bit)

This bit selects whether a message with EXT-ID or STD-ID will be transmitted from or was received in the FIFO Buffer.

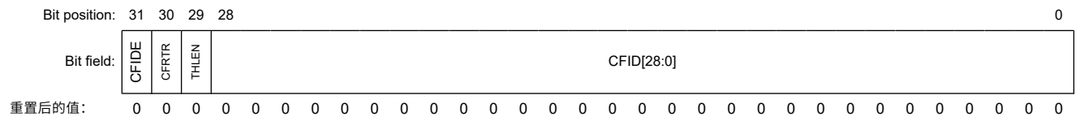
In TX mode, users can write and read from FIFO buffers.

In RX mode, users can only read data from FIFO buffers.

28.2.62.13 CFDCFID:通用FIFO访问ID寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x05B8



Bit	Symbol	Function	R/W
28:0	CFID[28:0]	通用FIFO缓冲区ID字段 STD-ID / EXT-ID fields	R/W
29	THLEN	THL条目启用 TX FIFO Mode: 0：TX成功后，条目不会存储在THL中。1：TX成功后，条目将存储在THL中。 RX FIFO Mode: 保留，该位读为0	R/W
30	CFRTR	通用FIFO缓冲器RTR位 0：数据帧1：远程帧	R/W
31	CFIDE	通用FIFO缓冲器IDE位 0：将发送或已接收STD-ID1：将发送或已接收EXT-ID	R/W

通用FIFO访问ID寄存器存储消息的ID字段、IDE位和RTR位。

在TX模式下，用户可以从FIFO中读取数据，只能根据写指针值读取当前条目，不能读取其他条目。

CFID[28:0]位（通用FIFO缓冲区ID字段）

这些是FIFO缓冲区中消息的STD-IDEXT-ID字段的位。

在TX模式下，用户可以写入和读取FIFO缓冲区。

在RX模式下，用户只能从FIFO缓冲区读取数据。

THLEN位（THL入口使能）

该位控制在成功传输结束时在TXHistory列表中存储与已传输消息相对应的条目。

在TX模式下，用户可以写入和读取FIFO缓冲区。

在RX模式下，用户只能从FIFO缓冲区读取数据。

CFRTR位（通用FIFO缓冲区RTR位）

该位选择数据帧或远程帧是从FIFO缓冲区发送还是在FIFO缓冲区中接收。

注意：CANFD格式中没有远程帧。如果接收到CANFD帧（RX模式），寄存器会反映接收值的状态（FD帧格式中的RRS位）。在CANFD传输（TX模式CFDCFID.CFFDF=1）的情况下，该位始终以显性方式传输（数据帧）。

在TX模式下，用户可以写入和读取FIFO缓冲区。

在RX模式下，用户只能从FIFO缓冲区读取数据。

CFIDE位（通用FIFO缓冲器IDE位）

该位选择是从FIFO缓冲区发送还是接收具有EXT-ID或STD-ID的消息。

在TX模式下，用户可以写入和读取FIFO缓冲区。

在RX模式下，用户只能从FIFO缓冲区读取数据。

28.2.62.14 CFDCFPTR : Common FIFO Access Pointer Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x05BC

Bit position:	31	28														15															0
Bit field:	CFDLC[3:0]				—	—	—	—	—	—	—	—	—	—	—	CFTS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CFTS[15:0]	Common FIFO Timestamp Value Timestamp value of the received CAN frame (FIFO in RX mode).	R/W
27:16	—	These bits are read as 0. The write value should be 0.	R/W
31:28	CFDLC[3:0]	Common FIFO Buffer DLC Field Number of data bytes received in a CAN frame, or to be transmitted in a CAN frame.	R/W

The Common FIFO Access Pointer Registers store the DLC and Timestamp fields.

In TX mode, you can read data from the FIFO buffer, only for the current entry based on the write pointer value, and not for the other entries.

CFTS[15:0] bits (Common FIFO Timestamp Value)

The CFTS[15:0] bits store the timestamp value taken at the capture point as configured by the CFDGFDCFG.TSCCFG bit of the received message (if FIFO is configured in RX mode).

In TX mode, you can read and write from FIFO buffers.

In RX mode, you can only read data from FIFO buffers.

CFDLC[3:0] bits (Common FIFO Buffer DLC Field)

The CFDLC[3:0] bits store the number of data bytes that were received in the FIFO buffer or are to be transmitted.

See Table 5 in ISO 11898-1 (2015) Specification for details in defining the number of data bytes.

In TX mode, you can read and write from the FIFO buffers. Do not read data for the other entries in the FIFO when configured in TX mode.

In RX mode, you can only read data from the FIFO buffers.

28.2.62.15 CFDCFFDCSTS : Common FIFO Access CANFD Control/Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x05C0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CFIFL[1:0]		—	—	—	—	—	CFFDF	CFBRS	CFESI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFESI*1	Error State Indicator bit 0: CANFD frame received or to transmit by error active node 1: CANFD frame received or to transmit by error passive node	R/W

28.2.62.14 CFDCFPTR:通用FIFO访问指针寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x05BC

Bit position:	31	28														15															0
Bit field:	CFDLC[3:0]				—	—	—	—	—	—	—	—	—	—	—	CFTS[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CFTS[15:0]	通用FIFO时间戳值 接收到的CAN帧的时间戳值（RX模式下的FIFO）。	R/W
27:16	—	这些位被读取为0。写入值应为0。	R/W
31:28	CFDLC[3:0]	通用FIFO缓冲区DLC字段 在一个CAN帧中接收的数据字节数，或在一个CAN帧中传输的数据字节数。	R/W

公共FIFO访问指针寄存器存储DLC和时间戳字段。

在TX模式下，您可以从FIFO缓冲区读取数据，仅基于写指针值读取当前条目，而不能读取其他条目。

CFTS[15:0]位（通用FIFO时间戳值）

CFTS[15:0]位存储由接收消息的CFDGFDCFG.TSCCFG位配置的捕获点的时间戳值（如果FIFO配置为RX模式）。

在TX模式下，您可以从FIFO缓冲区读取和写入。

在RX模式下，您只能从FIFO缓冲区读取数据。

CFDLC[3:0]位（通用FIFO缓冲区DLC字段）

CFDLC[3:0]位存储已在FIFO缓冲区中接收或将要发送的数据字节数。

有关定义数据字节数的详细信息，请参见ISO11898-1(2015)规范中的表5。

在TX模式下，您可以从FIFO缓冲区读取和写入。在TX模式下配置时，不要读取FIFO中其他条目的数据。

在RX模式下，您只能从FIFO缓冲区读取数据。

28.2.62.15 CFDCFFDCSTS:通用FIFO访问CANFD控制状态寄存器

Base address: CANFD_B = 0x400B_0000

Offset address: 0x05C0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFPTR[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CFIFL[1:0]		—	—	—	—	—	CFFDF	CFBRS	CFESI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFESI*1	错误状态指示位 0：CANFD帧接收或发送错误主动节点1：CANFD帧接收或发送错误被动节点	R/W

Bit	Symbol	Function	R/W
1	CFBRS*1	Bit Rate Switch bit 0: CANFD frame received or to transmit with no bit rate switch 1: CANFD frame received or to transmit with bit rate switch	R/W
2	CFFDF*1	CAN FD Format bit 0: Non CANFD frame received or to transmit 1: CANFD frame received or to transmit	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
9:8	CFIFL[1:0]	COMMON FIFO Buffer Information Label Field	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
31:16	CFPTR[15:0]	Common FIFO Buffer Pointer Field	R/W

Note 1. This bit is not available in the classical CAN function.

The Common FIFO Access CANFD Control/Status Registers show the status of the FDF, BRS and ESI bits, including the pointer of the received CANFD frame or the CANFD frame to transmit.

In TX mode, you can read data from the FIFO, only for the current entry based on the write pointer value, and not for the other entries.

CFESI bit (Error State Indicator bit)

In TX mode, you can read and write from FIFO buffers. In this mode, when the CANFD module is not in error passive, the CFESI bit equals the write value. Otherwise, it is a don't care and the bit is transmitted as 1 on the CAN bus, indicating this is an error passive node.

In RX mode, you can only read data from FIFO buffers.

In RX mode, the CFESI bit is updated with the ESI bit value of the CANFD frame when it has been received, indicating the error state of the transmitting node. In RX mode, 0 is stored to this bit when the received FDF bit is 0, this means a CAN 2.0 frame is received.

Note: This bit is not available in the classical CAN function.

CFBRS bit (Bit Rate Switch bit)

In TX mode, you can read and write from FIFO buffers. In this mode, the CANFD module either transmits a 0 to indicate no bit rate switch in the frame to be transmitted or a 1 to indicate a bit rate switch in the frame to be transmitted.

In RX mode, you can only read data from FIFO buffers.

In RX mode, the CFBRS bit is updated with the BRS bit value of the CANFD frame when it has been received, indicating whether there is a bit rate switch (1) or (0) on the CANFD frame.

In RX mode, 0 is stored to the CFBRS bit when the received FDF bit is 0, this means a CAN 2.0 frame is received.

Note: This bit is not available in the classical CAN function.

CFFDF bit (CAN FD Format bit)

In TX mode, you can read and write from FIFO buffers. In this mode, the CANFD module either transmits a 0 to indicate a CAN 2.0 frame is to be transmitted or a 1 to indicate a CANFD frame is to be transmitted.

In RX mode, you can only read data from FIFO buffers.

In RX mode, the CFFDF bit is updated with the FDF bit value of the CAN frame when it has been received, indicating whether it is a CAN 2.0 frame (0) or a CANFD frame (1).

Note: This bit is not available in the classical CAN function.

CFIFL[1:0] bits (COMMON FIFO Buffer Information Label Field)

If the Common FIFO is configured in TX mode, the value programmed in CFDCFFDCSTS.CFIFL[1:0] is stored together with additional message information, to the TX History List after successful transmission of the message.

The information label value from the related Global Acceptance Filter List entry is stored in these bits (if FIFO is configured in either RX mode).

Bit	Symbol	Function	R/W
1	CFBRS*1	比特率切换位 0：接收或发送CANFD帧，无比特率切换1：接收或发送CANFD帧，使用比特率切换	R/W
2	CFFDF*1	CANFD格式位 0：接收或发送非CANFD帧1：接收或发送CANFD帧	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
9:8	CFIFL[1:0]	COMMONFIFO缓冲区信息标签字段	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W
31:16	CFPTR[15:0]	通用FIFO缓冲区指针字段	R/W

注1.该位在经典CAN功能中不可用。

通用FIFO访问CANFD控制状态寄存器显示FDF、BRS和ESI位的状态，包括接收到的CANFD帧或要发送的CANFD帧的指针。

在TX模式下，您可以从FIFO中读取数据，仅针对基于写指针值的当前条目，而不能针对其他条目。

CFESI位（错误状态指示位）

在TX模式下，您可以从FIFO缓冲区读取和写入。在此模式下，当CANFD模块未处于错误被动状态时，CFESI位等于写入值。否则，它是无关紧要的，该位在CAN总线上传输为1，表示这是一个错误被动节点。

在RX模式下，您只能从FIFO缓冲区读取数据。

在RX模式下，CFESI位在接收到CANFD帧时更新为ESI位值，指示发送节点的错误状态。在RX模式下，当接收到的FDF位为0时，将0存储到该位，这意味着接收到CAN2.0帧。

Note: 该位在经典CAN功能中不可用。

CFBRS位（比特率切换位）

在TX模式下，您可以从FIFO缓冲区读取和写入。在这种模式下，CANFD模块要么发送0表示要发送的帧中没有比特率切换，要么发送1表示要发送的帧中的比特率切换。

在RX模式下，您只能从FIFO缓冲区读取数据。

在RX模式下，CFBRS位在接收到CANFD帧时更新为BRS位值，指示CANFD帧上是否存在比特率切换（1）或（0）。

在RX模式下，当接收到的FDF位为0时，将0存储到CFBRS位，这意味着接收到CAN2.0帧。

Note: 该位在经典CAN功能中不可用。

CFFDF位（CANFD格式位）

在TX模式下，您可以从FIFO缓冲区读取和写入。在这种模式下，CANFD模块要么发送一个0来表示一个将发送CAN2.0帧或1表示要发送CANFD帧。

在RX模式下，您只能从FIFO缓冲区读取数据。

在RX模式下，CFFDF位在接收到CAN帧时更新为CAN帧的FDF位值，指示它是CAN2.0帧（0）还是CANFD帧（1）。

Note: 该位在经典CAN功能中不可用。

CFIFL[1:0]位（通用FIFO缓冲区信息标签字段）

如果CommonFIFO配置为TX模式，则在成功传输消息后，CFDCFDCSTS.CFIFL[1:0]中编程的值与附加消息信息一起存储到TX历史列表中。

来自相关全局接受过滤器列表条目的信息标签值存储在这些位中（如果FIFO配置为任一RX模式）。

In TX mode, you can read and write from FIFO buffers.

In RX mode, you can only read data from FIFO buffers.

CFPTR[15:0] bits (Common FIFO Buffer Pointer Field)

If the Common FIFO is configured in TX mode, the value programmed in CFDCFFDCSTS.CFPTR[15:0] is stored together with additional message information, to the TX History List after successful transmission of the message.

The pointer value from the related Global Acceptance Filter List entry is stored in these bits (if FIFO is configured in either RX mode).

In TX mode, you can read and write from FIFO buffers.

In RX mode, you can only read data from FIFO buffers.

28.2.62.16 CFDCFDFp : Common FIFO Access Data Field p Registers (p = 0 to 15)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x05C4 + 0x004 × p

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	CFDB_HH[7:0]	CFDB_HL[7:0]	CFDB_LH[7:0]	CFDB_LL[7:0]
Value after reset:	0 … 0	0 … 0	0 … 0	0 … 0

Bit	Symbol	Function	R/W
7:0	CFDB_LL[7:0]	Common FIFO Buffer Data Bytes (p × 4)	R/W
15:8	CFDB_LH[7:0]	Common FIFO Buffer Data Bytes ((p × 4) + 1)	R/W
23:16	CFDB_HL[7:0]	Common FIFO Buffer Data Bytes ((p × 4) + 2)	R/W
31:24	CFDB_HH[7:0]	Common FIFO Buffer Data Bytes ((p × 4) + 3)	R/W

The FIFO Access Data Field p Registers (p = 0 to 15) store data bytes (p × 4) to data bytes ((p × 4) + 3) of the message.

In TX mode, you can read data from the FIFO, only for the current entry based on the write pointer value, and not for the other entries.

CFDB_LL[7:0] bits (Common FIFO Buffer Data Bytes (p × 4))

The CFDB_LL[7:0] bits store data bytes (p × 4) of the message present in the FIFO buffer.

In TX mode, you can read and write from the FIFO buffers.

In RX mode, you can only read data from the FIFO buffers.

In RX mode, unused data bytes are filled with 0x00, according to their configured data payload size CFDCFCC.CFPLS.*1

CFDB_LH[7:0] bits (Common FIFO Buffer Data Bytes ((p × 4) + 1))

The CFDB_LH[7:0] bits store data bytes ((p × 4) + 1) of the message present in the FIFO buffer.

In TX mode, you can read and write from the FIFO buffers.

In RX mode, you can only read data from the FIFO buffers.

In RX mode, unused data bytes are filled with 0x00, according to their configured data payload size CFDCFCC.CFPLS.*1

CFDB_HL[7:0] bits (Common FIFO Buffer Data Bytes ((p × 4) + 2))

The CFDB_HL[7:0] bits store data bytes ((p × 4) + 2) of the message present in the FIFO buffer.

In TX mode, you can read and write from the FIFO buffers.

In RX mode, you can only read data from the FIFO buffers.

In RX mode, unused data bytes are filled with 0x00, according to their configured data payload size CFDCFCC.CFPLS.*1

在TX模式下，您可以从FIFO缓冲区读取和写入。

在RX模式下，您只能从FIFO缓冲区读取数据。

CFPTR[15:0]位（通用FIFO缓冲区指针字段）

如果CommonFIFO配置为TX模式，则在成功发送消息后，CFDCFDCSTS.CFPTR[15:0]中编程的值与附加消息信息一起存储到TX历史列表中。

来自相关全局接受过滤器列表条目的指针值存储在这些位中（如果FIFO被配置为
RX mode).

在TX模式下，您可以从FIFO缓冲区读取和写入。

在RX模式下，您只能从FIFO缓冲区读取数据。

28.2.62.16 CFDCFDFp：通用FIFO访问数据字段p寄存器（p=0到15）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x05C4 + 0x004 × p

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	CFDB_HH[7:0]	CFDB_HL[7:0]	CFDB_LH[7:0]	CFDB_LL[7:0]
重置后的值：	0 … 0	0 … 0	0 … 0	0 … 0

Bit	Symbol	Function	R/W
7:0	CFDB_LL[7:0]	通用FIFO缓冲区数据字节(p×4)	R/W
15:8	CFDB_LH[7:0]	公共FIFO缓冲区数据字节((p×4)+1)	R/W
23:16	CFDB_HL[7:0]	公共FIFO缓冲区数据字节((p×4)+2)	R/W
31:24	CFDB_HH[7:0]	公共FIFO缓冲区数据字节((p×4)+3)	R/W

FIFO访问数据字段p寄存器(p=0到15)将数据字节(p×4)存储到消息的数据字节((p×4)+3)。

在TX模式下，您可以从FIFO中读取数据，仅针对基于写指针值的当前条目，而不能针对其他条目。

CFDB_LL[7:0]位（通用FIFO缓冲区数据字节(p×4)）

CFDB_LL[7:0]位存储FIFO缓冲区中存在的消息的数据字节(p×4)。

在TX模式下，您可以从FIFO缓冲区读取和写入。

在RX模式下，您只能从FIFO缓冲区读取数据。

在RX模式下，未使用的数据字节根据其配置的数据有效负载大小CFDCFCC.CFPLS填充为0x00。*1

CFDB_LH[7:0]位（通用FIFO缓冲区数据字节((p×4)+1)）

CFDB_LH[7:0]位存储FIFO缓冲区中存在的消息的数据字节((p×4)+1)。

在TX模式下，您可以从FIFO缓冲区读取和写入。

在RX模式下，您只能从FIFO缓冲区读取数据。

在RX模式下，未使用的数据字节根据其配置的数据有效负载大小CFDCFCC.CFPLS填充为0x00。*1

CFDB_HL[7:0]位（通用FIFO缓冲区数据字节((p×4)+2)）

CFDB_HL[7:0]位存储FIFO缓冲区中存在的消息的数据字节((p×4)+2)。

在TX模式下，您可以从FIFO缓冲区读取和写入。

在RX模式下，您只能从FIFO缓冲区读取数据。

在RX模式下，未使用的数据字节根据其配置的数据有效负载大小CFDCFCC.CFPLS填充为0x00。*1

CFDB_HH[7:0] bits (Common FIFO Buffer Data Bytes ((p × 4) + 3))

The CFDB_HH[7:0] bits store data bytes ((p × 4) + 3) of the message present in the FIFO buffer.

In TX mode, you can read and write from the FIFO buffers.

In RX mode, you can only read data from the FIFO buffers.

In RX mode, unused data bytes are filled with 0x00, according to their configured data payload size CFDCFCC.CFPLS.*1

Note 1. In RX mode, unused data bytes are filled with 0x00 according to the configured data payload size CFDCFCC.CFPLS, which is a CANFD feature not found in classical CAN.

28.2.62.17 CFDTMBCPb[0] : TX Message Buffer Component b (b = 0 to 3)

Base address: CANFD_B = 0x400B_0000

Offset address: See Table 28.5

Bit position:	31																													0
Bit field:	Rc[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	Rc[31:0]	TX Message Buffer Component c Refer to Table 28.12, Table 28.13 and the descriptions that follow for a detailed description of each register and its related bits, contained within this message buffer component.	R

Where the total number of CFDTMBCPn = 4 as shown in Figure 28.29 (c = TX Message Buffer Component Register index = [0…18])

Rc[31:0] bit (TX Message Buffer Component c)

TX Message Buffer Component c

The TX Message Buffer Component is made up of the following registers: CFDTMIDb, CFDTMPTRb, CFDTMFDCTRb, and CFDTMDFbp. Refer to Table 28.13 for details of how to interpret the structure of this buffer component and how to access the respective registers.

Table 28.12 TX Message Buffer Component Summary (1 of 2)

TX Message Buffer Component (TMBCP)	
Rc	**CANFD mode (CAN_FD_MODE = 1'b1)**
R0	TX Message Buffer (b) ID Registers CHn
R1	TX Message Buffer (b) Pointer Registers CHn
R2	TX Message Buffer (b) CANFD Status Registers CHn
R3	TX Message Buffer (b) Data Field 0 Registers CHn
R4	TX Message Buffer (b) Data Field 1 Registers CHn
R5	TX Message Buffer (b) Data Field 2 Registers CHn
R6	TX Message Buffer (b) Data Field 3 Registers CHn
R7	TX Message Buffer (b) Data Field 4 Registers CHn
R8	TX Message Buffer (b) Data Field 5 Registers CHn
R9	TX Message Buffer (b) Data Field 6 Registers CHn
R10	TX Message Buffer (b) Data Field 7 Registers CHn
R11	TX Message Buffer (b) Data Field 8 Registers CHn
R12	TX Message Buffer (b) Data Field 9 Registers CHn
R13	TX Message Buffer (b) Data Field 10 Registers CHn

CFDB_HH[7:0]位（通用FIFO缓冲区数据字节((p×4)+3)）

CFDB_HH[7:0]位存储FIFO缓冲区中存在的消息的数据字节((p×4)+3)。

在TX模式下，您可以从FIFO缓冲区读取和写入。

在RX模式下，您只能从FIFO缓冲区读取数据。

在RX模式下，未使用的数据字节根据其配置的数据有效负载大小CFDCFCC.CFPLS填充为0x00。*1

注1.在RX模式下，未使用的数据字节根据配置的数据有效负载大小用0x00填充
CFDCFCC.CFPLS，这是经典CAN中没有的CANFD功能。

28.2.62.17 CFDTMBCPb[0]：TX消息缓冲区组件b（b=0到3）

Base address: CANFD_B = 0x400B_0000

Offset address: 见表28.5

Bit position:	31																													0
Bit field:	Rc[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	Rc[31:0]	TX消息缓冲区组件c 请参阅表28.12、表28.13和随后的描述，了解该消息缓冲区组件中包含的每个寄存器及其相关位的详细描述。	R

其中，CFDTMBCPn的总数=4，如图28.29所示（c=TX消息缓冲区组件寄存器索引=[0…18]）

Rc[31:0]位（TX消息缓冲区组件c）

TX消息缓冲区组件c

TX报文缓冲区组件由以下寄存器组成：CFDTMIDb、CFDTMPTRb、CFDTMFDCTRb和CFDTMDFbp。有关如何解释此缓冲区组件的结构以及如何访问相应寄存器的详细信息，请参见表28.13。

Table 28.12 TX消息缓冲区组件摘要(1of2)

TX消息缓冲区组件(TMBCP)	
Rc	**CANFD mode (CAN_FD_MODE = 1'b1)**
R0	TX报文缓冲器(b)ID寄存器CHn
R1	TX报文缓冲区(b)指针寄存器CHn
R2	TX报文缓冲器(b)CANFD状态寄存器CHn
R3	TX报文缓冲区(b)数据字段0寄存器CHn
R4	TX报文缓冲区(b)数据字段1寄存器CHn
R5	TX报文缓冲区(b)数据字段2寄存器CHn
R6	TX报文缓冲区(b)数据字段3寄存器CHn
R7	TX报文缓冲区(b)数据字段4寄存器CHn
R8	TX报文缓冲区(b)数据字段5寄存器CHn
R9	TX报文缓冲区(b)数据字段6寄存器CHn
R10	TX报文缓冲区(b)数据字段7寄存器CHn
R11	TX报文缓冲区(b)数据字段8寄存器CHn
R12	TX报文缓冲区(b)数据字段9寄存器CHn
R13	TX报文缓冲区(b)数据字段10寄存器CHn

Table 28.12 TX Message Buffer Component Summary (2 of 2)

TX Message Buffer Component (TMBCP)	
Rc	**CANFD mode (CAN_FD_MODE = 1'b1)**
R14	TX Message Buffer (b) Data Field 11 Registers CHn
R15	TX Message Buffer (b) Data Field 12 Registers CHn
R16	TX Message Buffer (b) Data Field 13 Registers CHn
R17	TX Message Buffer (b) Data Field 14 Registers CHn
R18	TX Message Buffer (b) Data Field 15 Registers CHn
R[19…31]	—

Table 28.13 TX Message Buffer Component (TMBCP) Detailed

Rc	p	Symbol	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDTMIDb	TMIDE	TMRTR	THLEN	TMID																												
R1	x	CFDTMPTRb	TMDLC				—	—	—	—	—	—	—	—	—	—	—	—	CFTS															
R2	x	CFDTMFDCTRb	TMPTR																—	—	—	—	—	—	TMIFL		—	—	—	—	—	TMFDF	TMBRS	TMESI
R3	0	CFDTMDFbp	TMDB_HH								TMDB_HL								TMDB_LH								TMDB_LL						
R[4…18]	[1…15]	CFDTMDFbp	TMDB_HH								TMDB_HL								TMDB_LH								TMDB_LL						

28.2.62.18 CFDTMIDb : TX Message Buffer ID Registers (b = 0 to 3)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0604 + 0x004C × b

Bit position:	31	30	29	28	…	0
Bit field:	TMIDE	TMRTR	THLEN	TMID[28:0]		
Value after reset:	0	0	0	0	…	0

Bit	Symbol	Function	R/W
28:0	TMID[28:0]	TX Message Buffer ID Field STD-ID/EXT-ID fields	R/W
29	THLEN	Tx History List Entry 0: Entry not stored in THL after successful TX 1: Entry stored in THL after successful TX	R/W
30	TMRTR	TX Message Buffer RTR bit 0: Data frame 1: Remote frame	R/W
31	TMIDE	TX Message Buffer IDE bit 0: STD-ID is transmitted 1: EXT-ID is transmitted	R/W

Each TX Message Buffer ID Register b (b = 0 to 3) are used to store the ID, IDE, RTR fields and history configuration of the message to be transmitted from the associated buffer.

Table 28.12 TX消息缓冲区组件摘要(2of2)

TX消息缓冲区组件(TMBCP)	
Rc	**CANFD mode (CAN_FD_MODE = 1'b1)**
R14	TX报文缓冲区(b)数据字段11寄存器CHn
R15	TX报文缓冲区(b)数据字段12寄存器CHn
R16	TX报文缓冲区(b)数据字段13寄存器CHn
R17	TX报文缓冲区(b)数据字段14寄存器CHn
R18	TX报文缓冲区(b)数据字段15寄存器CHn
R[19…31]	—

Table 28.13 TX消息缓冲区组件(TMBCP)详细信息

Rc	p	Symbol	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDTMIDb	TMIDE	TMRTR	THLEN	TMID																												
R1	x	CFDTMPTRb	TMDLC				—	—	—	—	—	—	—	—	—	—	—	—	CFTS															
R2	x	CFDTMFDCTRb	TMPTR																—	—	—	—	—	—	TMIFL		—	—	—	—	—	TMFDF	TMBRS	TMESI
R3	0	CFDTMDFbp	TMDB_HH								TMDB_HL								TMDB_LH								TMDB_LL						
R[4…18]	[1…15]	CFDTMDFbp	TMDB_HH								TMDB_HL								TMDB_LH								TMDB_LL						

28.2.62.18 CFDTMIDb：TX报文缓冲区ID寄存器（b=0到3）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0604 + 0x004C × b

Bit position:	31	30	29	28	…	0
Bit field:	TMIDE	TMRTR	THLEN	TMID[28:0]		
重置后的值：	0	0	0	0	…	0

Bit	Symbol	Function	R/W
28:0	TMID[28:0]	TX消息缓冲区ID字段 STD-ID/EXT-ID fields	R/W
29	THLEN	Tx历史列表条目 0：成功TX后条目不存储在THL中1：成功TX后条目存储在THL	R/W
30	TMRTR	TX报文缓冲区RTR位 0：数据帧1：远程帧	R/W
31	TMIDE	TX消息缓冲区IDE位 0：发送STD-ID1：发送EXT-ID	R/W

每个TX报文缓冲区ID寄存器b（b=0到3）用于存储要从相关缓冲区发送的报文的ID、IDE、RTR字段和历史配置。

TMID[28:0] bits (TX Message Buffer ID Field)

The TMID[28:0] bits are bits of the STD-ID/EXT-ID fields of the message stored in this TX message buffer.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

THLEN bit (Tx History List Entry)

The THLEN bit controls the storage of an entry corresponding to the transmitted message in the TX History list at the end of a successful transmission.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

TMRTR bit (TX Message Buffer RTR bit)

The TMRTR bit selects whether a data frame or remote frame is to be transmitted from this TX message buffer.

Note: There are no remote frames in CANFD format. For a CANFD transmission (CFDTMFDCTRb.CFFDF = 1), this bit is always transmitted dominant (data frame).

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

TMIDE bit (TX Message Buffer IDE bit)

The TMIDE bit selects whether a message with EXT-ID or STD-ID is to be transmitted from this TX message buffer.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

28.2.62.19 CFDTMPTRb : TX Message Buffer Pointer Register (b = 0 to 3)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0608 + 0x004C × b

Bit position:	31	28	0
Bit field:	TMDLC[3:0]	—	
Value after reset:	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bit	Symbol	Function	R/W
27:0	—	The read values are undefined. The write value should be 0.	R/W
31:28	TMDLC[3:0]	TX Message Buffer DLC Field Number of data bytes to be transmitted in a CAN frame.	R/W

Each TX Message Buffer Pointer Register b (b = 0 to 3) is used to store the DLC fields of the message to transmit from the associated buffer.

TMDLC[3:0] bits (TX Message Buffer DLC Field)

The TMDLC[3:0] bits select the number of data bytes to be transmitted from this TX message buffer when the corresponding TMRTR bit is configured as 0.

See Table 5 in ISO 11898-1 (2015) Specification for details in defining the number of data bytes to be transmitted.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

TMID[28:0]位（TX消息缓冲区ID字段）

TMID[28:0]位是存储在此TX消息缓冲区中的消息的STD-IDEXT-ID字段的位。

当相关CANFD通道处于CH_SLEEP模式时，请勿写入这些位。

THLEN位（Tx历史列表条目）

THLEN位控制在成功发送结束时将对应于发送消息的条目存储在TX历史列表中。

当相关CANFD通道处于CH_SLEEP模式时，请勿写入这些位。

TMRTR位（TX报文缓冲区RTR位）

TMRTR位选择是从该TX报文缓冲区发送数据帧还是远程帧。

Note: CANFD格式中没有远程帧。对于CANFD传输(CFDTMFDCTRb.CFFDF=1)，该位始终为显性传输（数据帧）。

当相关CANFD通道处于CH_SLEEP模式时，请勿写入这些位。

TMIDE位（TX消息缓冲区IDE位）

TMIDE位选择是从该TX报文缓冲区发送带有EXT-ID还是STD-ID的报文。

当相关CANFD通道处于CH_SLEEP模式时，请勿写入这些位。

28.2.62.19 CFDTMPTRb：TX报文缓冲区指针寄存器（b=0到3）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0608 + 0x004C × b

Bit position:	31	28	0
Bit field:	TMDLC[3:0]	—	
重置后的值：	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bit	Symbol	Function	R/W
27:0	—	读取的值未定义。写入值应为0。	R/W
31:28	TMDLC[3:0]	TX消息缓冲区DLC字段 CAN帧中要传输的数据字节数。	R/W

每个TX消息缓冲区指针寄存器b（b=0到3）用于存储要从相关缓冲区发送的消息的DLC字段。

TMDLC[3:0]位（TX消息缓冲区DLC字段）

当相应的TMRTR位配置为0时，TMDLC[3:0]位选择要从该TX报文缓冲区发送的数据字节数。

有关定义要传输的数据字节数的详细信息，请参见ISO11898-1(2015)规范中的表5。

当相关CANFD通道处于CH_SLEEP模式时，请勿写入这些位。

28.2.62.20 CFDTMFDCTRb : TX Message Buffer CANFD Control Register (b = 0 to 3)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x060C + 0x004C × b

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TMPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TMIFL[1:0]		—	—	—	—	—	TMFDF	TMBRS	TMESI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMESI*1	Error State Indicator bit 0: CANFD frame to transmit by error active node 1: CANFD frame to transmit by error passive node	R/W
1	TMBRS*1	Bit Rate Switch bit 0: CANFD frame to transmit with no bit rate switch 1: CANFD frame to transmit with bit rate switch	R/W
2	TMFDF*1	CAN FD Format bit 0: Non CANFD frame to transmit 1: CANFD frame to transmit	R/W
7:3	—	The read values are undefined. The write value should be 0.	R/W
9:8	TMIFL[1:0]	TX Message Buffer Information Label Field	R/W
15:10	—	The read values are undefined. The write value should be 0.	R/W
31:16	TMPTR[15:0]	TX Message Buffer Pointer Field	R/W

Note 1. This bit is not available in the classical CAN function.

The TX Message Buffer CANFD Control Registers b (b = 0 to 3) show the status of the FDF, BRS and ESI bits, including the pointer fields of the CANFD frame to be transmitted.

TMESI bit (Error State Indicator bit)

If the channel is not in error passive, then the TMESI bit equals the write value, otherwise it is a don't care and the bit is transmitted as 1 on the CAN bus, indicating this is an error passive node.

Do not write to the TMESI bit when the related CANFD channel is in CH_SLEEP mode.

Note: This bit is not available in the classical CAN function.

TMBRS bit (Bit Rate Switch bit)

Do not write to the TMBRS bit when the related CANFD channel is in CH_SLEEP mode.

Note: This bit is not available in the classical CAN function.

TMFDF bit (CAN FD Format bit)

Do not write to the TMFDF bit when the related CANFD channel is in CH_SLEEP mode.

Note: This bit is not available in the classical CAN function.

TMIFL[1:0] bits (TX Message Buffer Information Label Field)

The TMIFL[1:0] bits store the information label value to be copied, together with additional message information, in the TX History List after successful transmission of the message.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

28.2.62.20 CFDTMFDCTRb：TX报文缓冲区CANFD控制寄存器（b=0到3）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x060C + 0x004C × b

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TMPTR[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TMIFL[1:0]		—	—	—	—	—	TMFDF	TMBRS	TMESI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMESI*1	错误状态指示位 0：CANFD帧由错误主动节点发送1：CANFD帧由错误被动节点发送	R/W
1	TMBRS*1	比特率切换位 0：CANFD帧传输，无码率切换1：CANFD帧传输，码率切换	R/W
2	TMFDF*1	CANFD格式位 0：发送非CANFD帧1：发送CANFD帧	R/W
7:3	—	读取的值未定义。写入值应为0。	R/W
9:8	TMIFL[1:0]	TX消息缓冲区信息标签字段	R/W
15:10	—	读取的值未定义。写入值应为0。	R/W
31:16	TMPTR[15:0]	TX消息缓冲区指针字段	R/W

注1.该位在经典CAN功能中不可用。

TX报文缓冲区CANFD控制寄存器b（b=0到3）显示FDF、BRS和ESI位的状态，包括要发送的CANFD帧的指针字段。

TMESI位（错误状态指示位）

如果通道不是被动错误，则TMESI位等于写入值，否则为无关位，该位在CAN总线上传输为1，表示这是一个错误被动节点。

当相关CANFD通道处于CH_SLEEP模式时，请勿写入TMESI位。

Note: 该位在经典CAN功能中不可用。

TMBRS位（比特率切换位）

当相关CANFD通道处于CH_SLEEP模式时，不要写入TMBRS位。

Note: 该位在经典CAN功能中不可用。

TMFDF位（CANFD格式位）

当相关CANFD通道处于CH_SLEEP模式时，请勿写入TMFDF位。

Note: 该位在经典CAN功能中不可用。

TMIFL[1:0]位（TX消息缓冲区信息标签字段）

TMIFL[1:0]位将要复制的信息标签值与附加消息信息一起存储在TX中成功传输消息后的历史列表。

当相关CANFD通道处于CH_SLEEP模式时，请勿写入这些位。

TMPTR[15:0] bits (TX Message Buffer Pointer Field)

The TMPTR[15:0] bits store the pointer value to be copied, together with additional message information in the TX History List after successful transmission of the message.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

28.2.62.21 CFDTMDFb_p : TX Message Buffer Data Field Register (p= 0 to 15 , b= 0 to 3)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0610 + 0x004 × p + 0x004C × b

Bit position:	31								24	23							16	15							8	7							0
Bit field:	TMDB_HH[7:0]									TMDB_HL[7:0]								TMDB_LH[7:0]								TMDB_LL[7:0]							
Value after reset:	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TMDB_LL[7:0]	TX Message Buffer Data Byte (p × 4)	R/W
15:8	TMDB_LH[7:0]	TX Message Buffer Data Byte ((p × 4) + 1)	R/W
23:16	TMDB_HL[7:0]	TX Message Buffer Data Byte ((p × 4) + 2)	R/W
31:24	TMDB_HH[7:0]	TX Message Buffer Data Byte ((p × 4) + 3)	R/W

i = Channel number

Each TX Message Buffer Data Field p Register b (p = 0 to 15, b = 0 to 3) is used to store data bytes (p × 4) to data bytes ((p × 4) + 3) of the message to transmit from the associated buffer.

TMDB_LL[7:0] bits (TX Message Buffer Data Byte (p × 4))

TMDB_LL[7:0] bits store data bytes (p × 4) of the message in the TX message buffer.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

TMDB_LH[7:0] bits (TX Message Buffer Data Byte ((p × 4) + 1))

TMDB_LH[7:0] bits store data bytes ((p × 4) + 1) of the message in the TX message buffer.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

TMDB_HL[7:0] bits (TX Message Buffer Data Byte ((p × 4) + 2))

TMDB_HL[7:0] bits store data bytes ((p × 4) + 2) of the message in the TX message buffer.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

TMDB_HH[7:0] bits (TX Message Buffer Data Byte ((p × 4) + 3))

TMDB_HH[7:0] bits store data bytes ((p × 4) + 3) of the message in the TX message buffer.

Do not write to these bits when the related CANFD hannel is in CH_SLEEP mode.

28.3 Modes of Operation

28.3.1 Overview

The modes of the CANFD module can be classified into 2 groups:

- Global modes
- Channel modes

TMPTR[15:0]位（TX消息缓冲区指针字段）

TMPTR[15:0]位存储要复制的指针值，以及TX历史记录中的附加消息信息
成功传输消息后的列表。

当相关CANFD通道处于CH_SLEEP模式时，请勿写入这些位。

28.2.62.21 CFDTMDFb_p：TX消息缓冲区数据字段寄存器（p=0到15，b=0到3）

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0610 + 0x004 × p + 0x004C × b

Bit position:	31								24	23							16	15							8	7							0
Bit field:	TMDB_HH[7:0]									TMDB_HL[7:0]								TMDB_LH[7:0]								TMDB_LL[7:0]							
重置后的值：	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TMDB_LL[7:0]	TX消息缓冲区数据字节(p×4)	R/W
15:8	TMDB_LH[7:0]	TX消息缓冲区数据字节((p×4)+1)	R/W
23:16	TMDB_HL[7:0]	TX消息缓冲区数据字节((p×4)+2)	R/W
31:24	TMDB_HH[7:0]	TX消息缓冲区数据字节((p×4)+3)	R/W

i=通道号

每个TX报文缓冲区数据字段p寄存器b(p=0到15，b=0到3)用于存储要发送的报文的数据字节(p×4)到数据字节((p×4)+3)从关联的缓冲区。

TMDB_LL[7:0]位（TX消息缓冲区数据字节(p×4)）

TMDB_LL[7:0]位将消息的数据字节(p×4)存储在TX消息缓冲区中。

当相关CANFD通道处于CH_SLEEP模式时，请勿写入这些位。

TMDB_LH[7:0]位（TX报文缓冲区数据字节((p×4)+1)）

TMDB_LH[7:0]位将消息的数据字节((p×4)+1)存储在TX消息缓冲区中。

当相关CANFD通道处于CH_SLEEP模式时，请勿写入这些位。

TMDB_HL[7:0]位（TX消息缓冲区数据字节((p×4)+2)）

TMDB_HL[7:0]位将消息的数据字节((p×4)+2)存储在TX消息缓冲区中。

当相关CANFD通道处于CH_SLEEP模式时，请勿写入这些位。

TMDB_HH[7:0]位（TX报文缓冲区数据字节((p×4)+3)）

TMDB_HH[7:0]位将消息的数据字节((p×4)+3)存储在TX消息缓冲区中。

当相关CANFD通道处于CH_SLEEP模式时，请勿写入这些位。

28.3 运作模式

28.3.1 Overview

CANFD模块的模式可分为2组：

●全局模式

●频道模式

28.3.2 Global Modes

These modes are applicable for the complete CANFD module and therefore are called Global modes. The global modes of the CANFD module are:

- Global Sleep
- Global Reset
- Global Halt
- Global Operation.

Figure 28.2 shows the possible transitions between the Global modes.

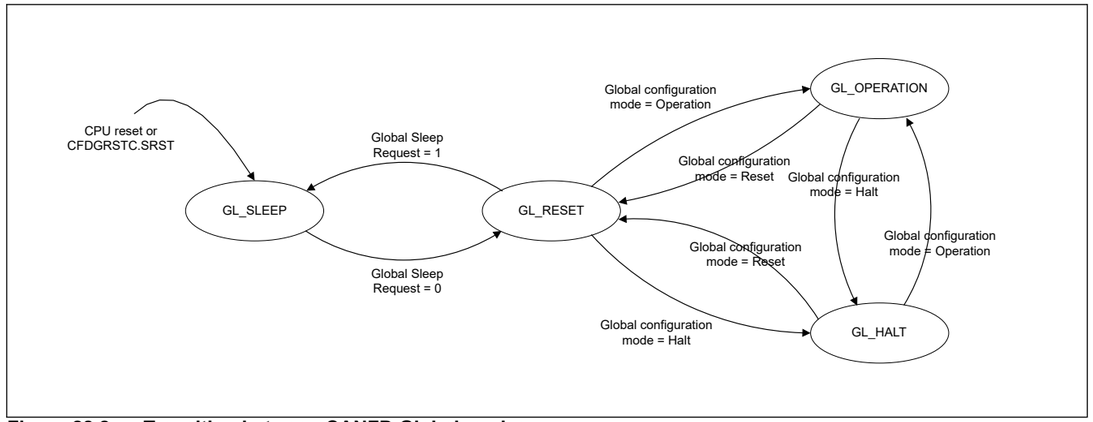


Figure 28.2 Transition between CANFD Global modes

Change in the Global mode can affect the Channel mode. Table 28.14 shows the effect of a Global mode transition on a Channel mode.

Table 28.14 Possible CANFD Channel modes and Global modes

Current Global mode	Target Global mode			
	Sleep	Reset	Halt	Operation
Sleep		Ch-Sleep: Keep Ch-Reset: N/A Ch-Halt: N/A Ch-Oper: N/A		
Reset	Ch-Sleep: Keep Ch-Reset: → Ch-Sleep Ch-Halt: N/A Ch-Oper: N/A		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: N/A Ch-Oper: N/A	Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: N/A Ch-Oper: N/A
Halt		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: → Ch-Reset Ch-Oper: N/A		Ch-Sleep:Keep Ch-Reset: Keep Ch-Halt: Keep Ch-Oper: N/A
Operation		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: → Ch-Reset Ch-Oper: → Ch-Reset	Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: Keep Ch-Oper: → Ch-Halt	

28.3.2.1 Global Sleep Mode

After the release of a hardware reset or after setting and clearing a CFDGRSTC.SRST bit, the CANFD module automatically enters Global Sleep mode.

The CANFD module also enters the Global Sleep mode when the Global Sleep Request bit is set while it is in Global Reset mode. This control bit cannot be set in Global Halt mode or Global Operation mode.

28.3.2 全局模式

这些模式适用于完整的CANFD模块，因此称为全局模式。CANFD模块的全局模式有：

●全局睡眠
●全局重置
●全球暂停
●全球运营。

图28.2显示了全局模式之间可能的转换。

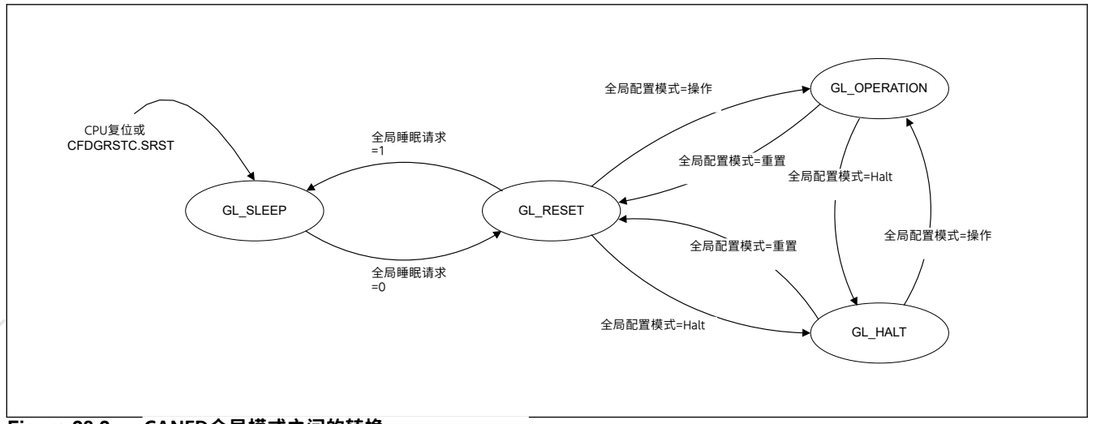


Figure 28.2 CANFD全局模式之间的转换

全局模式的变化会影响通道模式。表28.14显示了全局模式转换对频道模式。

Table 28.14 可能的CANFD通道模式和全局模式

当前全局模式	目标全局模式			
	Sleep	Reset	Halt	Operation
Sleep		Ch-Sleep: Keep Ch-Reset: N/A Ch-Halt: N/A Ch-Oper: N/A		
Reset	Ch-Sleep: Keep Ch-Reset: → Ch-Sleep Ch-Halt: N/A Ch-Oper: N/A		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: N/A Ch-Oper: N/A	Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: N/A Ch-Oper: N/A
Halt		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: → Ch-Reset Ch-Oper: N/A		Ch-Sleep:Keep Ch-Reset: Keep Ch-Halt: Keep Ch-Oper: N/A
Operation		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: → Ch-Reset Ch-Oper: → Ch-Reset	Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: Keep Ch-Oper: → Ch-Halt	

28.3.2.1 全局睡眠模式

释放硬件复位或设置和清除CFDGRSTC.SRST位后，CANFD模块自动进入全局休眠模式。

当CANFD模块在全局复位模式下设置全局休眠请求位时，它也会进入全局休眠模式。该控制位不能在GlobalHalt模式或GlobalOperation模式下设置。

Setting the Global Sleep Request bit sets Channel Sleep Request bit and forces the channel into the Channel Sleep mode.

Sleep mode is used for power saving purpose. When CANFD module is in Global Sleep mode, only the clock for CPU write access to the Global Sleep Mode Request bit is active. All other clocks are stopped and all other functions of the CANFD module are suspended.

Read access from all registers is still possible and all register values are preserved.

After setting the Global Sleep Request bit, it is necessary to confirm that the Global Sleep status has been updated, indicating successful transition to Global Sleep mode before the Global Sleep Request bit can be cleared again.

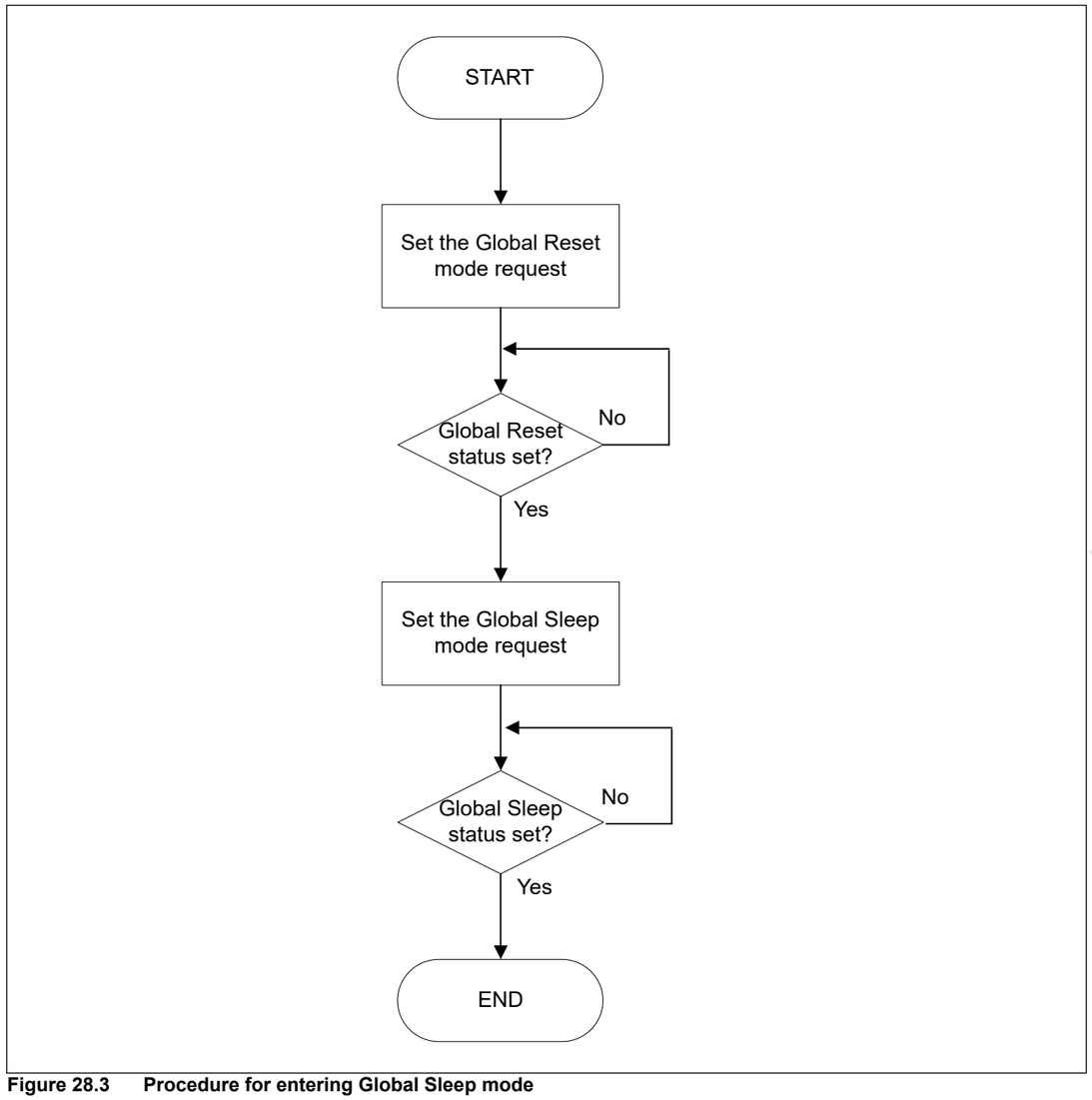


Figure 28.3 Procedure for entering Global Sleep mode

设置全局休眠请求位会设置通道休眠请求位并强制通道进入通道休眠模式。

睡眠模式用于省电目的。当CANFD模块处于全局休眠模式时，只有CPU对全局休眠模式请求位进行写访问的时钟有效。所有其他时钟停止，CANFD模块的所有其他功能暂停。

仍然可以从所有寄存器进行读取访问，并且所有寄存器值都被保留。

设置全局休眠请求位后，需要确认全局休眠状态已更新，表示成功转换到全局休眠模式，然后才能再次清除全局休眠请求位。

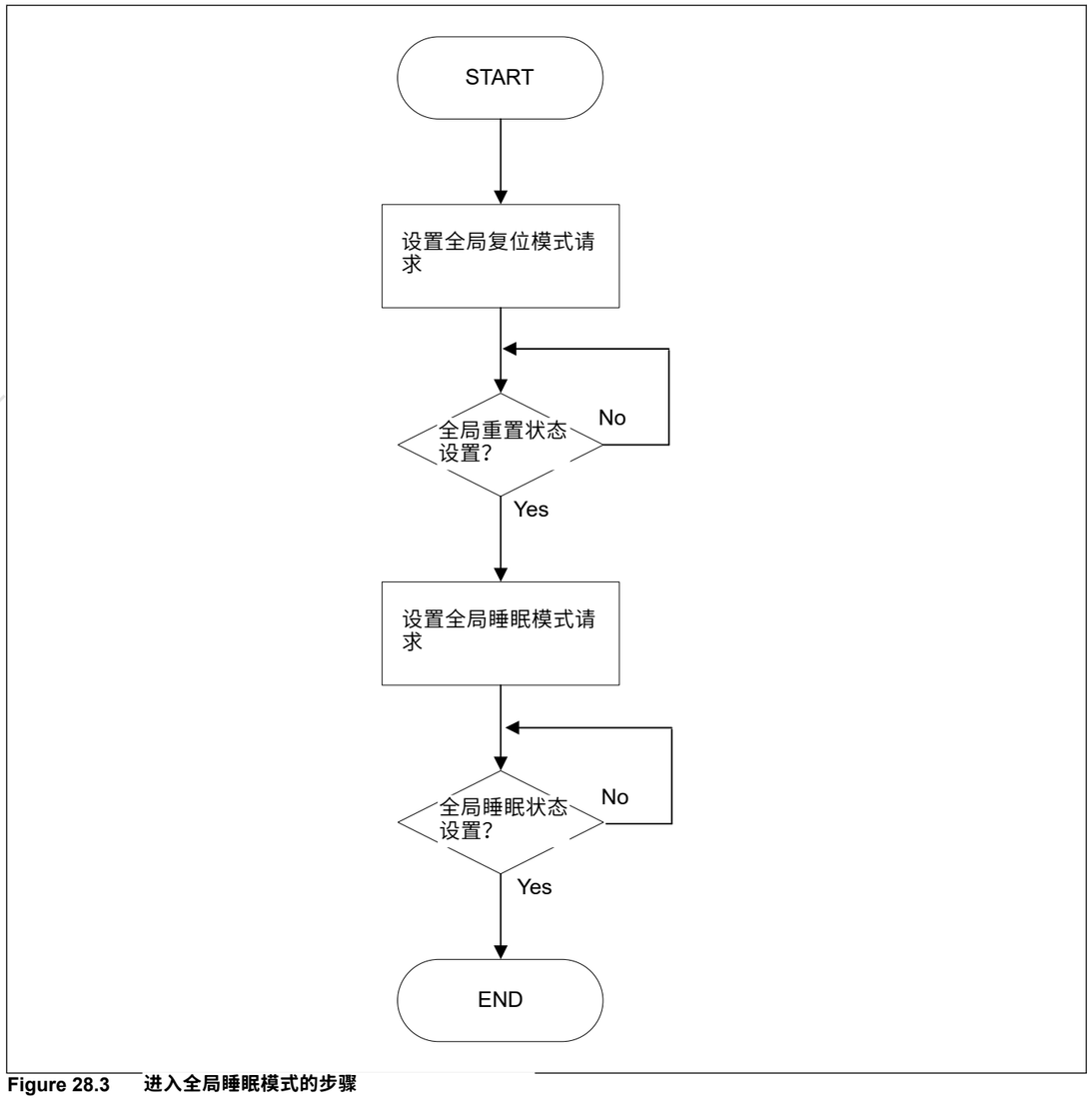


Figure 28.3 进入全局睡眠模式的步骤

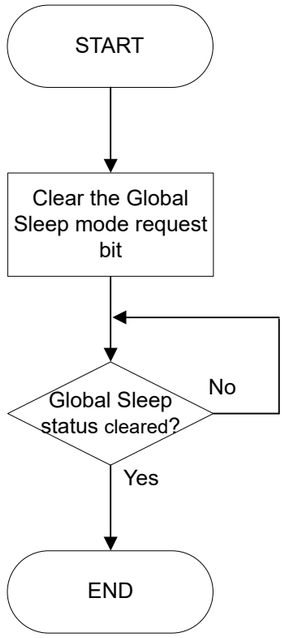


Figure 28.4 Procedure for exiting Global Sleep mode

28.3.2.2 Global Reset Mode

The CANFD module enters this mode in the following ways:

- Global Mode Control bit CFDGCTR.GMDC in the Global Control Register is configured for Global Reset mode while the CANFD module is in Global Halt or Global Operation mode
- Global Sleep Mode Request bit is cleared while CANFD module is in Global Sleep mode.

In Global Reset mode, all CANFD module functions are suspended and all status and flag registers are initialized.

Additionally all FIFOs and TX Queues are disabled and transmission control bits are cleared.

Configuration registers (except the test mode registers) are not initialized in this mode to their MCU reset values and the CANFD module can be configured.

See section 28.3.4. Global Mode and Channel Mode Transition Interactions for a detailed description of the behavior of all registers when transition to Global Reset mode is performed.

Setting the Global mode to Reset by setting the Global Mode Control bits CFDGCTR.GMDC in the Global Control Register to 01b sets Channel Mode Control bits CFDC0CTR.CHMDC in the Channel Control Registers to 01b and forces the channel into the Channel Reset mode.

For channels that are already in Channel Reset mode or Channel Sleep mode, this automatic transition is not performed (CFDC0CTR.CHMDC of related channel already set to 01b).

After setting Global Mode Control bit CFDGCTR.GMDC to Reset mode, it is necessary to confirm that the Reset Mode Status bit CFDGSTS.GRSTSTS in the Global Status Register has been updated, indicating successful transition to Global Reset mode before CFDGCTR.GMDC can be changed again.

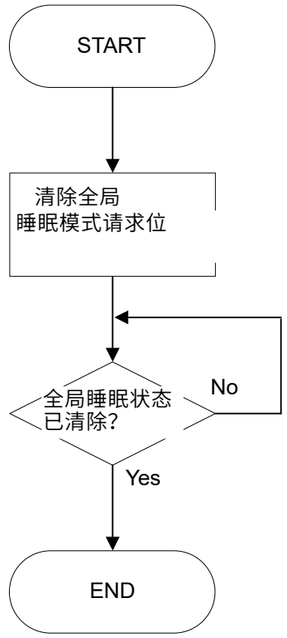


Figure 28.4 退出全局休眠模式的步骤

28.3.2.2 全局重置模式

CANFD模块通过以下方式进入该模式：

●全局控制寄存器中的全局模式控制位CFDGCTR.GMDC配置为全局复位模式，而CANFD模块处于全局暂停或全局操作模式

●CANFD模块处于全局休眠模式时，全局休眠模式请求位被清零。

在全局复位模式下，所有CANFD模块功能都被挂起，所有状态和标志寄存器都被初始化。

此外，所有FIFO和TX队列都被禁用，传输控制位被清除。

配置寄存器（测试模式寄存器除外）在此模式下未初始化为其MCU复位值，并且CANFD模块可以配置。

请参阅第28.3.4节。GlobalModeandChannelModeTransitionInteractions详细描述了当转换到全局复位模式时所有寄存器的行为。

通过设置全局控制中的全局模式控制位CFDGCTR.GMDC将全局模式设置为复位寄存器01b将通道控制寄存器中的通道模式控制位CFDC0CTR.CHMDC设置为01b，并强制通道进入通道复位模式。

对于已经处于通道复位模式或通道休眠模式的通道，不执行此自动转换（相关通道的CFDC0CTR.CHMDC已设置为01b）。

将全局模式控制位CFDGCTR.GMDC设置为复位模式后，需要确认复位模式GlobalStatusRegister中的状态位CFDGSTS.GRSTSTS已更新，表示成功转换到Global可以再次更改CFDGCTR.GMDC之前的复位模式。

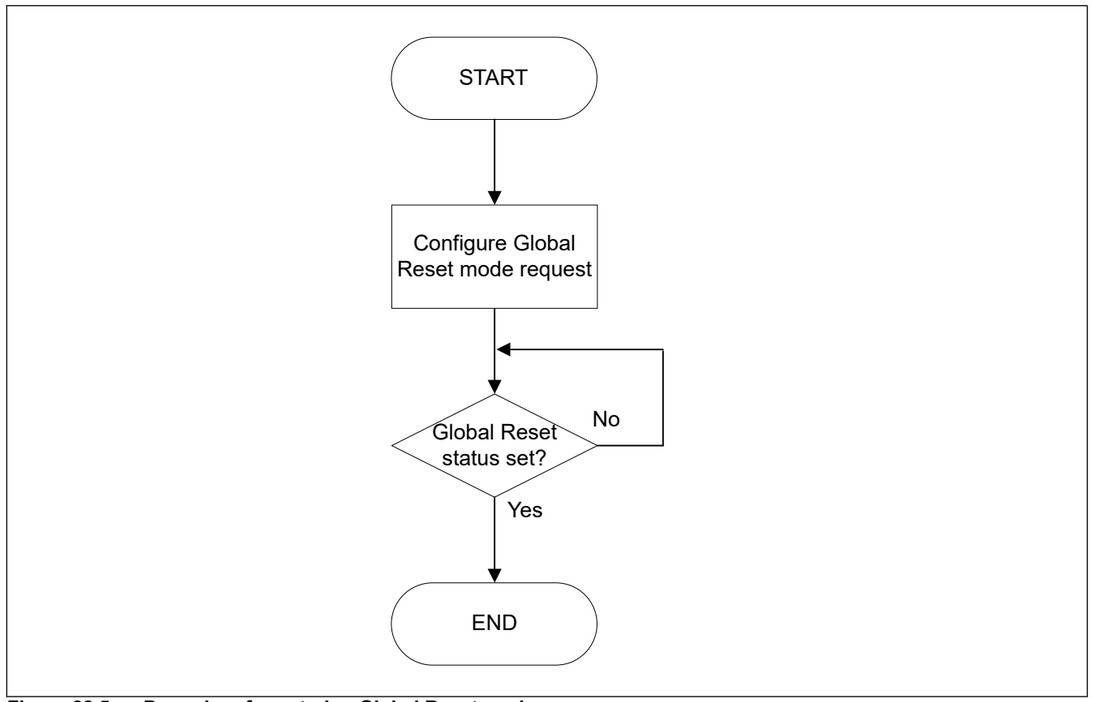


Figure 28.5 Procedure for entering Global Reset mode

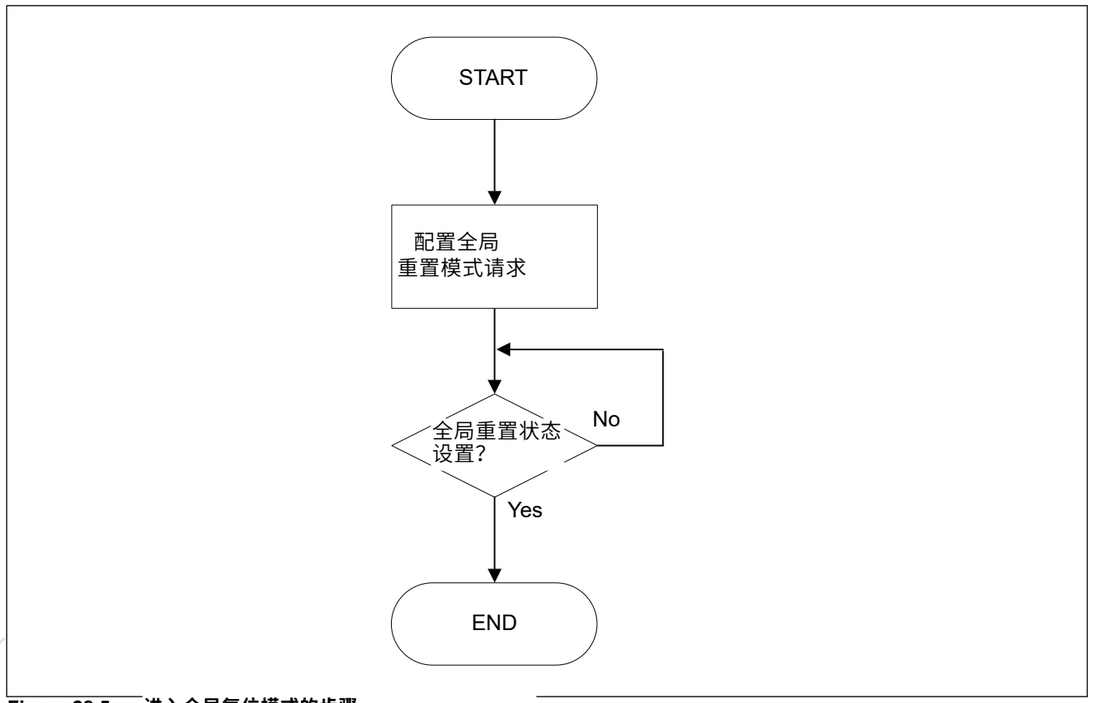


Figure 28.5 进入全局复位模式的步骤

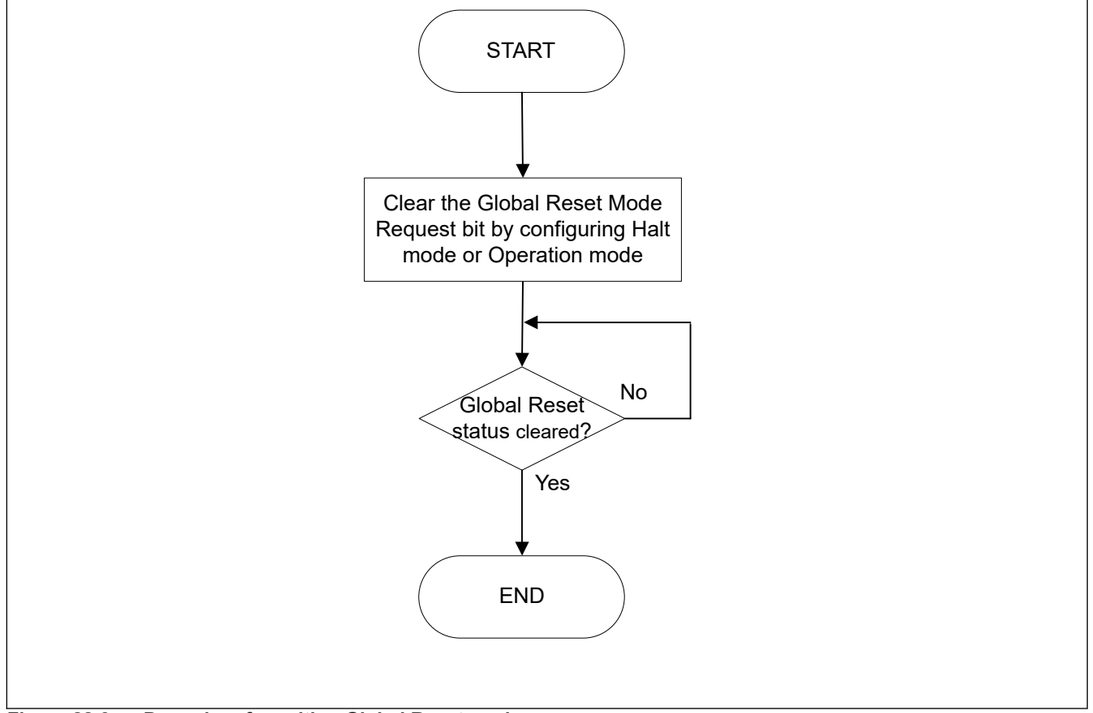


Figure 28.6 Procedure for exiting Global Reset mode

28.3.2.3 Global Halt Mode

The CANFD module enters this mode in the following ways:

- Global Mode Control bit CFDGCTR.GMDC in the Global Control Register is configured for Global Halt mode while the CANFD module is in Global Reset mode:
  - the channel is in either Channel Reset or Channel Sleep mode and remains in this mode
- Global Mode Control bit CFDGCTR.GMDC in the Global Control Register is configured for Global Halt mode while the CANFD module is in Global Operation mode:
  - the channel in Channel Reset, Channel Halt, or Channel Sleep mode remain in this mode
  - the channel in Channel Operation mode transit to Channel Halt mode
  - Global Halt Mode Status bit is set when the channel have left Channel Operation mode.

If a transmission or reception is ongoing for a channel, the transition to Channel Halt mode is delayed until completion of the communication.

Similarly, if a channel is in bus-off, the full bus-off recovery sequence may be delayed depending on the channel configuration.

In Global Halt mode, all communications are suspended and CANFD logic does not cause any change to the Status and Flag registers (only when a channel is in the bus-off that its REC and TEC values are cleared). Additionally, the test mode configuration and control registers are not initialized in this mode.

The Global Halt mode should be used to configure global module test modes.

See section 28.3.4. Global Mode and Channel Mode Transition Interactions for a detailed description of the behavior of all registers when transition to Global Halt mode is performed.

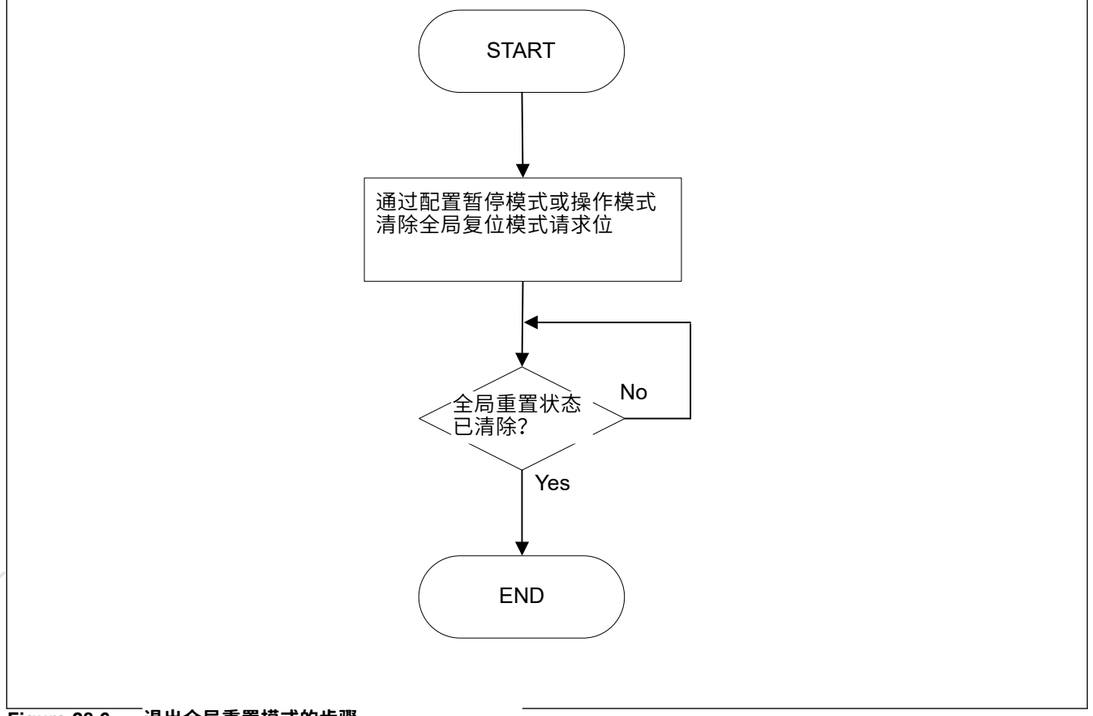


Figure 28.6 退出全局重置模式的步骤

28.3.2.3 全局停止模式

CANFD模块通过以下方式进入该模式：

●当CANFD模块处于全局复位模式时，全局控制寄存器中的全局模式控制位CFDGCTR.GMDC配置为全局暂停模式：

通道处于通道复位或通道休眠模式并保持在该模式

●当CANFD模块处于全局操作模式时，全局控制寄存器中的全局模式控制位CFDGCTR.GMDC配置为全局暂停模式：

处于通道复位、通道暂停或通道休眠模式的通道保持在此模式

通道操作模式中的通道转换到通道暂停模式

当通道离开通道操作模式时，设置全局暂停模式状态位。

如果通道正在进行传输或接收，则延迟到通道暂停模式的转换，直到通信完成。

类似地，如果通道处于总线关闭状态，则完全总线关闭恢复序列可能会延迟，具体取决于通道配置。

在全局暂停模式下，所有通信都暂停，CANFD逻辑不会导致状态和标志寄存器发生任何变化（仅当通道处于总线关闭状态时，其REC和TEC值才会被清除）。此外，测试模式配置和控制寄存器在此模式下未初始化。

GlobalHalt模式应该用于配置全局模块测试模式。

请参阅第28.3.4节。GlobalModeandChannelModeTransitionInteractions详细描述了在转换到全局暂停模式时所有寄存器的行为。

Setting the Global mode to Halt by setting the Global Mode Control bit CFDGCTR.GMDC in the Global Control Register to 10b sets Channel Mode Control bits CFDC0CTR.CHMDC in the Channel Control Registers to 10b for the channel that are in Channel Operation mode and forces these channels into the Channel Halt mode.

For the channel that are already in Channel Reset, Channel Halt, or Channel Sleep mode, this automatic transition is not performed.

Therefore, the Global Halt mode request can be used to shut down all CANFD channel communications without loss of messages and disruption on the related CAN bus (no interruption of reception/transmission processes on the channels).

After setting the Global Mode Control bit CFDGCTR.GMDC to Halt mode, it is necessary to confirm that the Halt Mode Status bit CFDGSTS.GHLTSTS in the Global Status Register has been updated to indicate a successful transition to Global Halt mode. Do not specify any other SFR setting until confirming CFDGSTS.GHLTSTS is set.

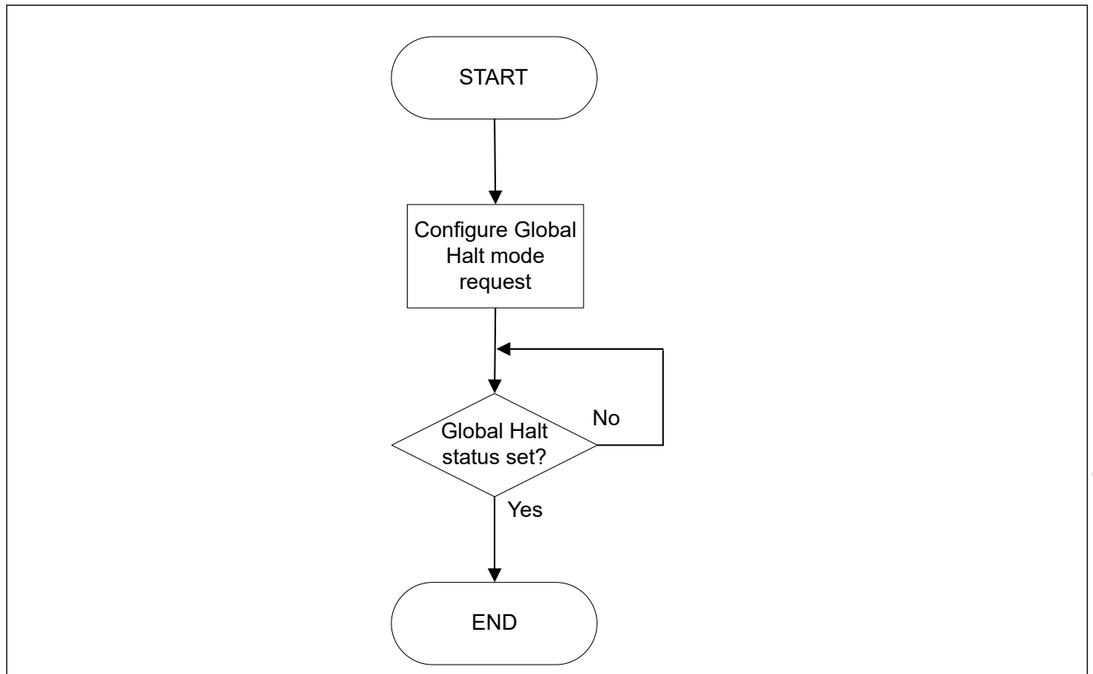


Figure 28.7 Procedure for entering Global Halt mode

通过将全局控制寄存器中的全局模式控制位CFDGCTR.GMDC设置为10b将全局模式设置为暂停，对于处于通道操作模式的通道，将通道控制寄存器中的通道模式控制位CFDC0CTR.CHMDC设置为10b，并强制这些通道进入通道暂停模式。

对于已经处于通道复位、通道暂停或通道休眠模式的通道，不会执行此自动转换。

因此，全局停止模式请求可用于关闭所有CANFD通道通信，而不会丢失消息和中断相关CAN总线（不会中断通道上的接收传输过程）。

将GlobalModeControl位CFDGCTR.GMDC设置为Halt模式后，需要确认HaltMode全局状态寄存器中的状态位CFDGSTS.GHLTTSTS已更新以指示成功转换到全局暂停模式。在确认设置CFDGSTS.GHLTTSTS之前，不要指定任何其他SFR设置。

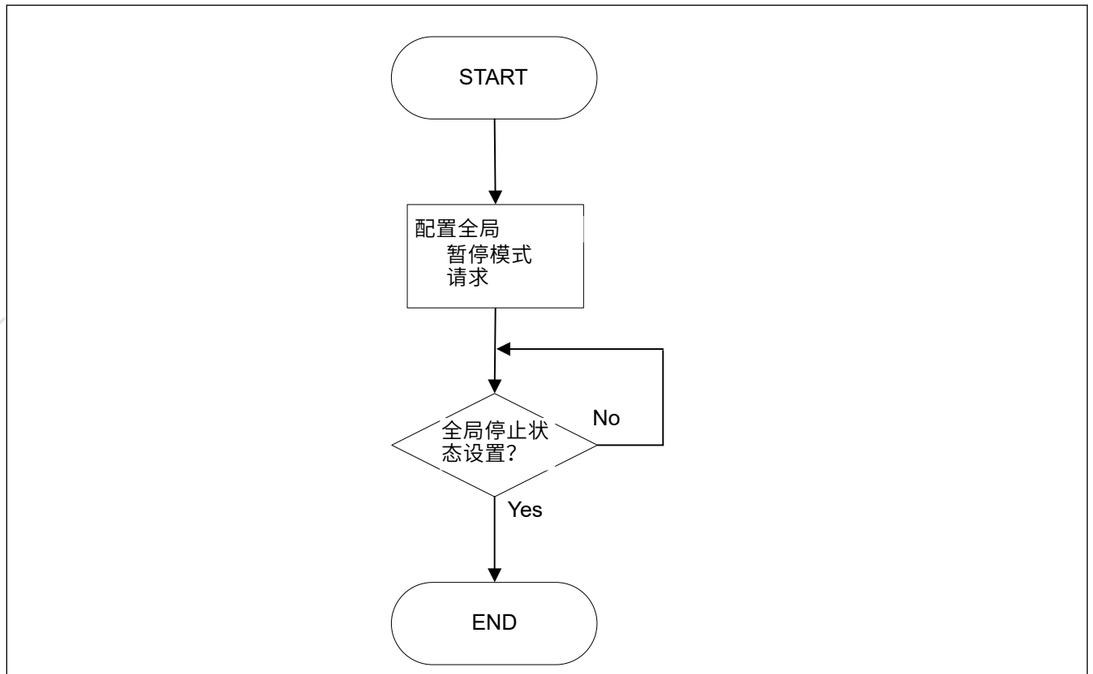


Figure 28.7 进入GlobalHalt模式的步骤

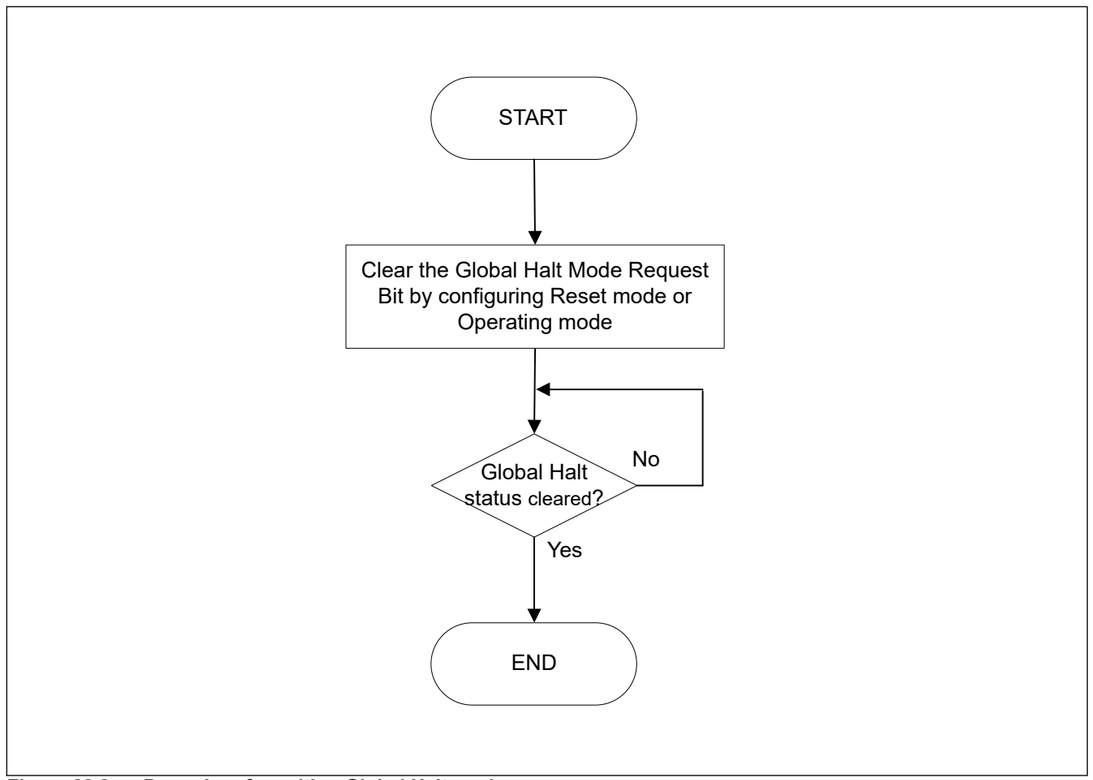


Figure 28.8 Procedure for exiting Global Halt mode

28.3.2.4 Global Operation Mode

The CANFD module enters this mode when the Global Mode Configuration bits are set to Global Operation mode.

The CANFD channel can only be set to Channel Operation mode and start CAN communication when CANFD is in Global Operation mode.

After setting the Global Mode Control bit CFDGCTR.GMDC to Global Operation mode, it is necessary to confirm that the Global Reset Mode Status bit CFDGSTS.GRSTSTS and the Global Halt Mode Status bit CFDGSTS.GHLTSTS in the Global Status Register have been cleared to indicate a successful transition to Global Operation mode before CFDGCTR.GMDC can be modified again.

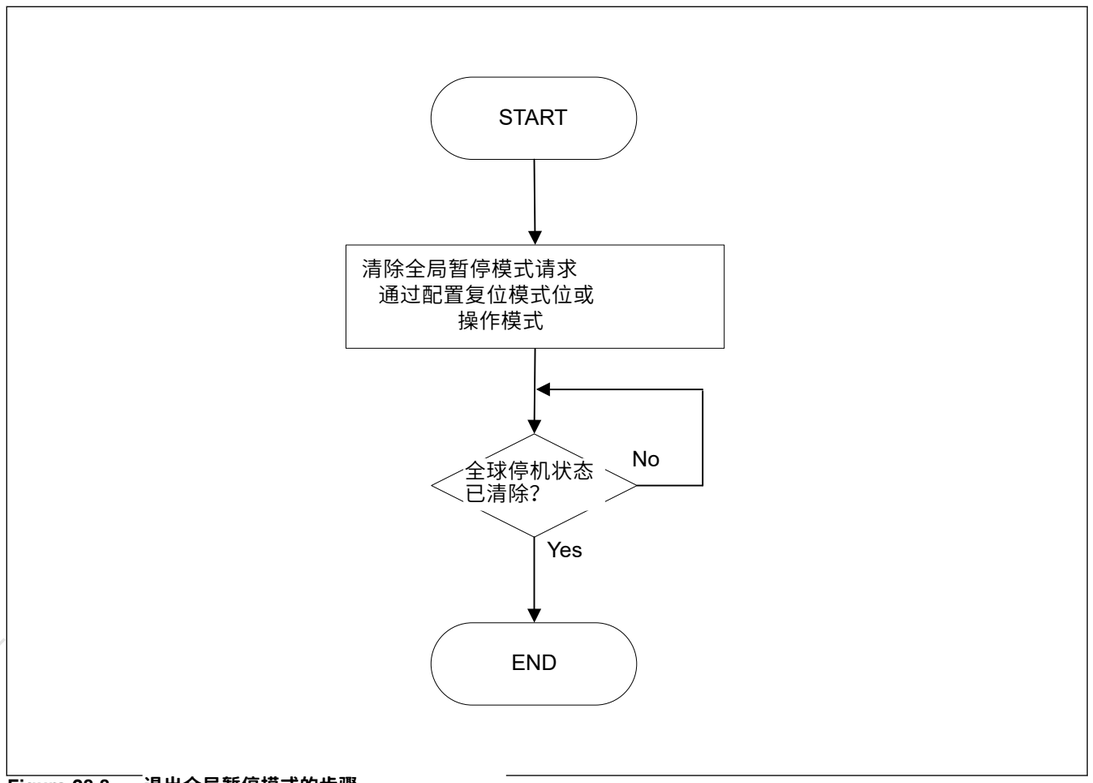


Figure 28.8 退出全局暂停模式的步骤

28.3.2.4 全球运营模式

当全局模式配置位设置为全局操作模式时，CANFD模块进入此模式。

CANFD通道只能设置为ChannelOperation模式并在CANFD处于Global时启动CAN通讯操作模式。

将全局模式控制位CFDGCTR.GMDC设置为全局操作模式后，需要确认
全局复位模式状态位CFDGSTS.GRSTSTS和全局暂停模式状态位CFDGSTS.GHLTSTS在
全局状态寄存器已被清除以指示成功转换到全局操作模式之前
CFDGCTR.GMDC可以再次修改。

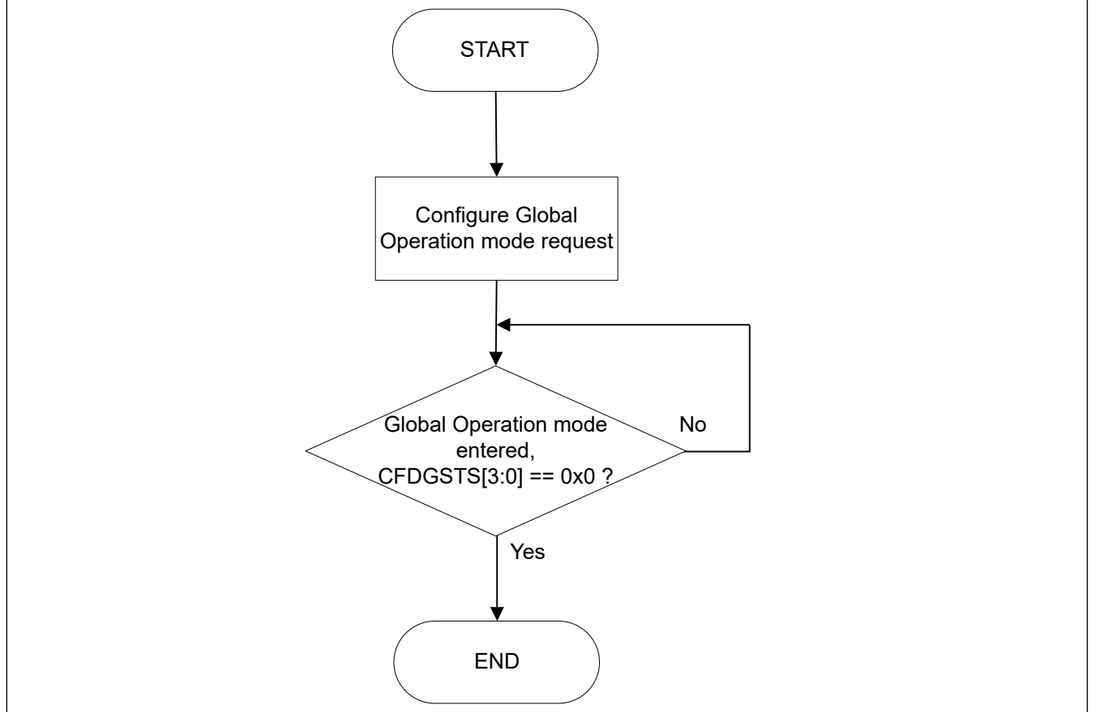


Figure 28.9 Procedure for entering Global Operation mode

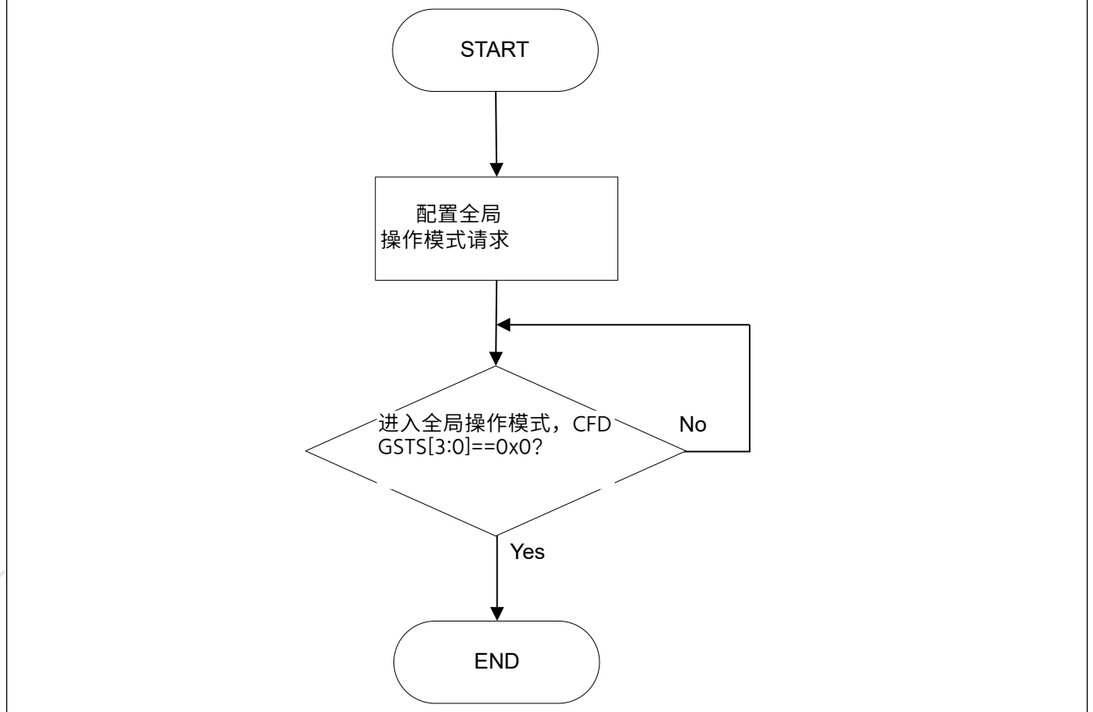


Figure 28.9 进入全局操作模式的步骤

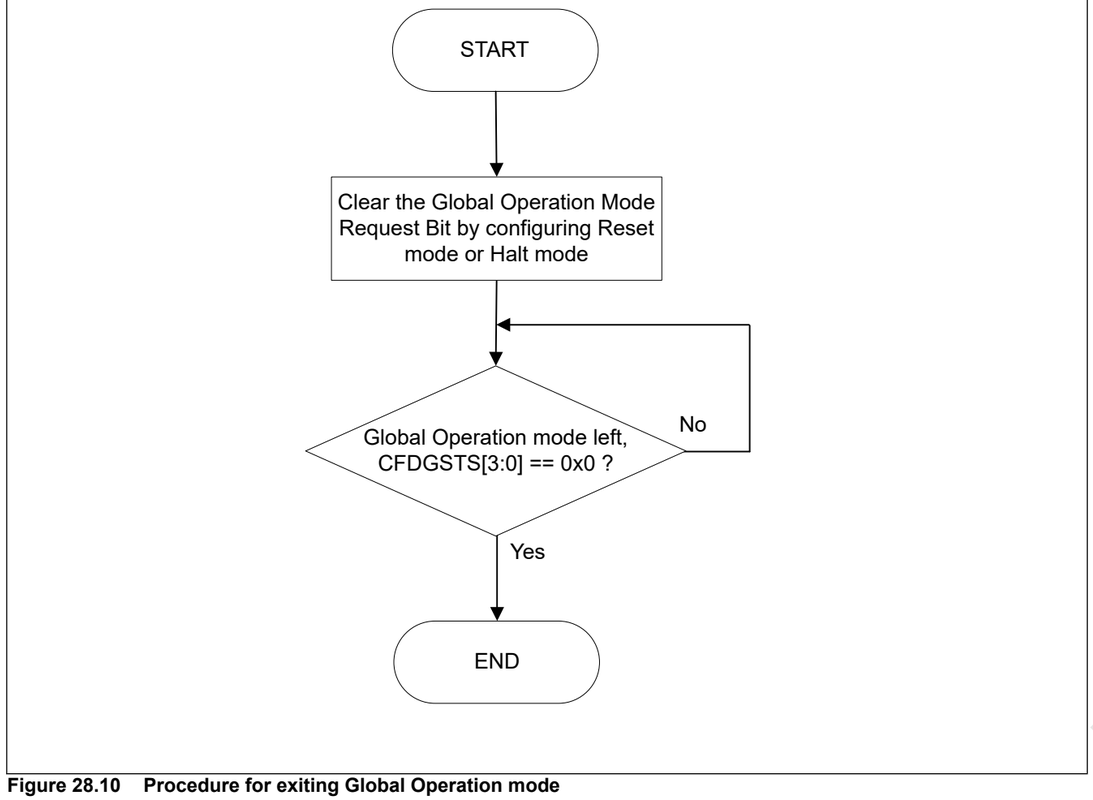


Figure 28.10 Procedure for exiting Global Operation mode

28.3.3 Channel Modes

A CAN channel can be in one of the following four channel modes:

- Reset
- Halt
- Operation
- Sleep.

Figure 28.11 shows the possible transitions between the channel modes.

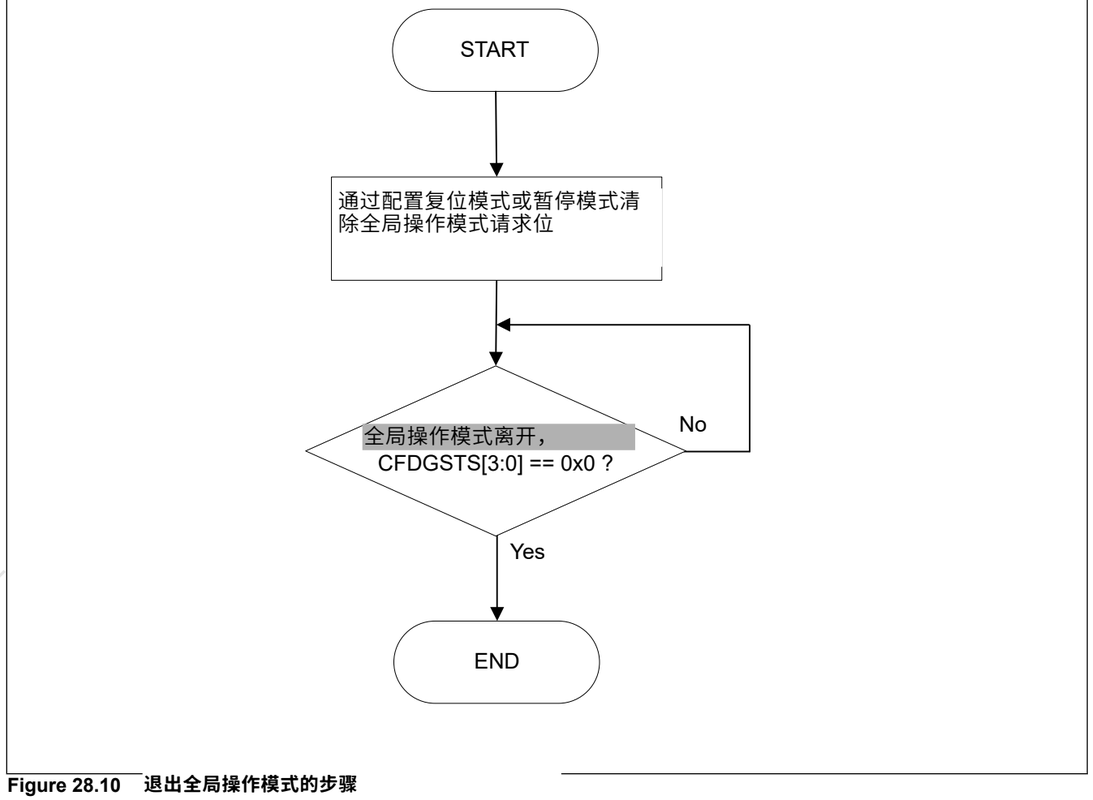


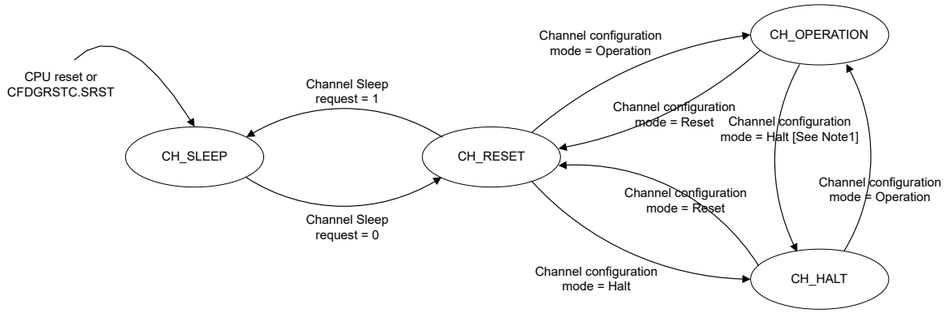
Figure 28.10 退出全局操作模式的步骤

28.3.3 频道模式

CAN通道可以处于以下四种通道模式之一：

- Reset
- Halt
- Operation
- Sleep.

图28.11显示了通道模式之间可能的转换。



Note 1. The transition timing depends on BOM setting in the Channel Configuration Register:
- when BOM = 01b, the state transition timing is immediate after entering bus-off state
- when BOM = 10b, the state transition timing is at the end of bus-off state
- when BOM = 11b, the state transition timing is matching with the setting of CHMDC to Halt mode.

Figure 28.11 Transition between CAN channel modes

28.3.3.1 CAN Channel Sleep Mode

After the release of a hardware reset or after setting and clearing the CFDGRSTC.SRST bit, a CAN channel of the CANFD module automatically enters Channel Sleep mode.

A CAN channel also enters Channel Sleep mode when the related Channel Sleep Mode Request bit is set while the CAN channel is in Channel Reset mode. Do not set this control bit in Channel Halt mode or Channel Operation mode.

Entering the CAN Channel Sleep mode instantly stops the clock supplied to the CAN channel unit and therefore reduces power consumption.

After setting the Channel Sleep Mode Request bit, it is necessary to confirm that the Channel Sleep mode status has been updated to indicate a successful transition to Channel Sleep mode before the Channel Sleep Mode Request bit can be cleared again.

During Channel Sleep mode, do not write to channel related registers. Read operation is still possible.

28.3.3.2 CAN Channel Reset Mode

A CANFD CAN channel enters this mode in the following ways:

- Channel Mode Control bit CFDC0CTR.CHMDC in the Channel Control Registers is configured for Channel Reset mode while the related CAN channel is in Channel Halt mode or Channel Operation mode
- Channel Sleep Mode Request bit is cleared while the related CAN channel is in Channel Sleep mode
- Global Mode Control bit CFDGCTR.GMDC is set to Global Reset mode and CAN channel is not in Channel Sleep mode or Channel Reset mode.

In Channel Reset mode, all CAN channel status and flag registers are initialized.

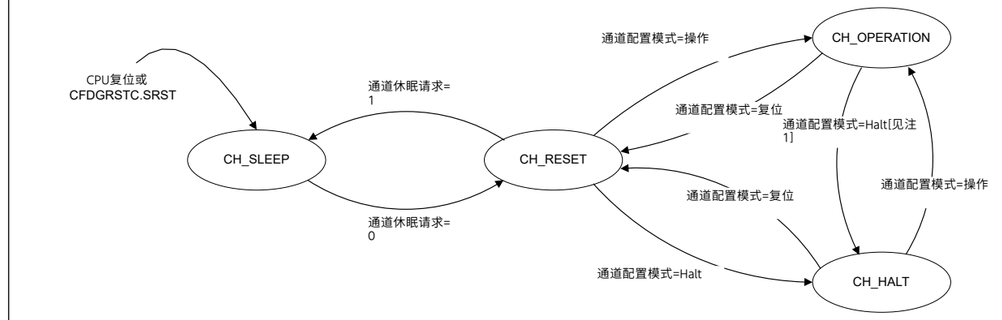
Additionally all channel related transmission control bits are cleared and the channel related TX Queue is disabled.

Configuration registers (except the Channel Test Mode registers) are not initialized in this mode and the CAN channel can be configured for communication.

See section 28.3.4. Global Mode and Channel Mode Transition Interactions for a detailed description of the behavior of all registers when transition to Channel Reset mode is performed.

After setting the Channel Mode Control bit CFDC0CTR.CHMDC to Channel Reset mode, it is necessary to confirm that the Reset Mode Status bit CFDC0STS.CRSTSTS in the related Channel Status Registers has been updated to indicate a successful transition to Channel Reset mode before the related CFDC0CTR.CHMDC bit can be modified again.

See Table 28.15 for the behavior of transitioning to Channel Reset mode while CAN communication is ongoing.



注1.转换时序取决于通道配置寄存器中的BOM设置：●
当BOM=01b时，状态转换时序在进入总线关闭状态后立即进行
- 当BOM=10b时，状态转换时序在总线关闭状态结束时
- 当BOM=11b时，状态转换时序与CHMDC设置为Halt模式相匹配。

Figure 28.11 CAN通道模式之间的转换

28.3.3.1 CAN通道休眠模式

硬件复位释放后或CFDGRSTC.SRST位设置和清零后，CANFD模块的一个CAN通道自动进入通道休眠模式。

当CAN通道处于通道复位模式时相关的通道休眠模式请求位置位，CAN通道也会进入通道休眠模式。不要在ChannelHalt模式或ChannelOperation模式下设置该控制位。

进入CAN通道休眠模式会立即停止提供给CAN通道单元的时钟，从而降低功耗。

设置通道休眠模式请求位后，必须确认通道休眠模式状态已更新以指示成功转换到通道休眠模式，然后才能再次清除通道休眠模式请求位。

在通道休眠模式期间，不要写入通道相关寄存器。仍然可以进行读取操作。

28.3.3.2 CAN通道复位模式

CANFDCAN通道通过以下方式进入此模式：

●通道控制寄存器中的通道模式控制位CFDC0CTR.CHMDC配置为通道复位模式，而相关的CAN通道处于通道暂停模式或通道操作模式

●通道休眠模式请求位在相关CAN通道处于通道休眠模式时清零

●全局模式控制位CFDGCTR.GMDC设置为全局复位模式，CAN通道不处于通道休眠模式或通道复位模式。

在通道复位模式下，所有CAN通道状态和标志寄存器都被初始化。

此外，所有通道相关的传输控制位都被清除，通道相关的TX队列被禁用。

配置寄存器（通道测试模式寄存器除外）在此模式下未初始化，CAN通道可配置为进行通信。

请参阅第28.3.4节。GlobalModeandChannelModeTransitionInteractions详细描述了当转换到通道复位模式时所有寄存器的行为。

将通道模式控制位CFDC0CTR.CHMDC设置为通道复位模式后，需要确认
相关通道状态寄存器中的复位模式状态位CFDC0STS.CRSTSTS已更新，以指示在可以再次修改相关CFDC0CTR.CHMDC位之前成功转换到通道复位模式。

有关在CAN通信进行时转换到通道复位模式的行为，请参见表28.15。

28.3.3.3 CAN Channel Halt Mode

A CANFD CAN channel enters this mode in the following ways:

- Channel Mode Control bit CFDC0CTR.CHMDC in the Channel Control Registers is configured for Channel Halt mode while the related CAN channel is in Channel Reset mode or Channel Operation mode
- Global Mode Control bit CFDGCTR.GMDC is set to Global Halt mode and CAN channel is in Channel Operation mode.

In Channel Halt mode, all channel CAN communication is suspended but all status and flag registers remain unchanged during Channel Halt mode entry (except for the bus-off case where REC and TEC values are cleared for this channel).

In addition, the Channel Test Mode Configuration and Control registers are not initialized in this mode.

The Channel Halt mode should be used to configure channel test modes.

See section 28.3.4. Global Mode and Channel Mode Transition Interactions for a detailed description of the behavior of all registers when transition to Channel Halt mode is performed.

After setting the Channel Mode Control bit CFDC0CTR.CHMDC to Channel Halt mode, it is necessary to confirm that the Halt Mode Status bit CFDC0STS.CHLTSTS in the related Channel Status Register has been updated to indicate a successful transition to Channel Halt mode before the related CFDC0CTR.CHMDC can be modified again.

See Table 28.15 for the transition behavior to Channel Halt mode while CAN communication is ongoing.

Table 28.15 Transition behavior in CAN Reset mode and Halt mode

Mode	State		
	Receiver	Transmitter	Bus-Off
CAN Channel Reset mode (CFDC0CTR.CHMDC = 01b)	The CAN channel enters Channel Reset mode without waiting for the completion of the ongoing reception.*1	The CAN channel enters Channel Reset mode without waiting for the completion of the ongoing transmission.*1	The CAN channel enters Channel Reset mode without waiting for the completion of the bus-off recovery.
CAN Channel Halt mode (CFDC0CTR.CHMDC = 10b)	CAN channel enters Channel Halt mode at the end of the ongoing reception or error.*2	CAN channel enters Channel Halt mode after completion of the ongoing transmission.	When CFDC0CTR.BOM is set to 00b, a Channel Halt mode request is accepted only after the completion of the full bus-off recovery sequence. When CFDC0CTR.BOM is set to 10b, the CAN channel transits automatically to Channel Halt mode after waiting for the completion of the bus-off recovery. When CFDC0CTR.BOM is set to 01b, the CAN channel transits automatically to Channel Halt mode without waiting for the completion of the bus-off recovery. When CFDC0CTR.BOM is set to 11b, the CAN channel enters Channel Halt mode as soon as Channel Halt mode is requested (without waiting for the completion of the bus-off recovery).

Note 1. If the entry to Channel Reset mode is required only at the end of an ongoing communication, then Channel Halt mode can be requested first to prevent interruption of CAN communication by direct transition to Channel Reset mode. After the CAN channel enters Channel Halt mode, the Channel Reset mode can be requested.

Note 2. If CAN communication is locked at dominant level after an error flag, software can detect this situation by monitoring the channel related BusLock flag and resolve lock condition by setting the CAN channel to Channel Reset mode.

28.3.3.4 CAN Channel Operation Mode

The Channel Operation mode is activated by setting the CFDC0CTR.CHMDC bits to 00b. If 11 consecutive recessive bits are detected after entering the CAN Operation mode, the CFDC0STS.COMSTS bit is set and the CAN channel:

28.3.3.3 CAN通道暂停模式

CANFDCAN通道通过以下方式进入此模式：

●通道控制寄存器中的通道模式控制位CFDC0CTR.CHMDC配置为通道暂停模式，而相关的CAN通道处于通道复位模式或通道操作模式

●全局模式控制位CFDGCTR.GMDC设置为全局暂停模式，CAN通道处于通道操作模式。

在ChannelHalt模式下，所有通道CAN通信都暂停，但在ChannelHalt模式进入期间所有状态和标志寄存器保持不变（总线关闭情况除外，该通道的REC和TEC值被清除）。

此外，通道测试模式配置和控制寄存器在此模式下未初始化。

通道暂停模式应该用于配置通道测试模式。

请参阅第28.3.4节。GlobalModeandChannelModeTransitionInteractions详细描述了当转换到ChannelHalt模式时所有寄存器的行为。

将通道模式控制位CFDC0CTR.CHMDC设置为通道暂停模式后，需要确认
相关通道状态寄存器中的暂停模式状态位CFDC0STS.CHLTSTS已更新，以指示在可以再次修改相关CFDC0CTR.CHMDC之前成功转换到通道暂停模式。

有关CAN通信正在进行时到通道暂停模式的转换行为，请参见表28.15。

Table 28.15 CAN复位模式和暂停模式下的转换行为

Mode	State		
	Receiver	Transmitter	Bus-Off
CAN通道复位模式(CFDC0CTR.CHMDC=01b)	CAN通道进入 通道复位模式无需等待正在进行的接收完成。*1	CAN通道进入 通道复位模式无需等待正在进行的传输完成。*1	CAN通道进入 通道复位模式无需等待总线关闭恢复完成。
CAN通道暂停模式(CFDC0CTR.CHMDC=10b)	CAN通道在正在进行的接收或错误结束时进入通道暂停模式。*2	CAN通道进入Channel 正在进行的传输完成后暂停模式。	当CFDC0CTR.BOM设置为00b时，仅在完成完整的总线关闭恢复序列后才接受通道暂停模式请求。当CFDC0CTR.BOM设置为10b时，CAN通道在等待总线关闭恢复完成后自动转换到通道暂停模式。当CFDC0CTR.BOM设置为01b时，CAN通道自动转换到通道暂停模式，无需等待总线关闭恢复完成。当CFDC0CTR.BOM设置为11b时，只要请求ChannelHalt模式，CAN通道就会进入ChannelHalt模式（无需等待总线关闭恢复完成）。

注1.如果仅在正在进行的通信结束时需要进入通道复位模式，则通道暂停模式可以是
首先请求通过直接转换到通道复位模式来防止CAN通信中断。CAN通道进入ChannelHalt模式后，可以请求ChannelReset模式。

注2.如果CAN通信在出现错误标志后被锁定在显性电平，软件可以通过监控与通道相关的BusLock标志来检测这种情况，并通过将CAN通道设置为通道复位模式来解决锁定条件。

28.3.3.4 CAN通道操作模式

通道操作模式通过将CFDC0CTR.CHMDC位设置为00b来激活。如果在进入CAN操作模式后检测到11个连续的隐性位，则CFDC0STS.COMSTS位置位并且CAN通道：

- Enables the functions of the channel communication by allowing the channel to become an active node on the CAN network
- Releases the internal fault confinement logic including receive and transmit error counters

At this point, the CAN channel can start transmission and reception of CAN messages.

Within the CAN Channel Operation mode, the channel may be in four different sub-modes, depending on which type of communication functions are performed (see Figure 28.12):

- Channel idle: The CAN channel is neither receiving nor transmitting
- Channel receives: The channel is receiving a CAN message sent by another CAN node
- Channel transmits: The channel is transmitting a CAN message

  Note: The channel may receive its own message simultaneously when Self-test mode is enabled.
- Channel is in bus-off state: The CAN channel is cut-off from CAN bus communication.

After setting the Channel Mode Control bit CFDC0CTR.CHMDC to Channel Operation mode, it is necessary to confirm that the Channel Reset Mode Status bit CFDC0STS.CRSTSTS and the Channel Halt Mode Status bit CFDC0STS.CHLTSTS in the Channel Status Register have been updated to indicate a successful transition to Channel Operation mode before the related CFDC0CTR.CHMDC bit can be changed again.

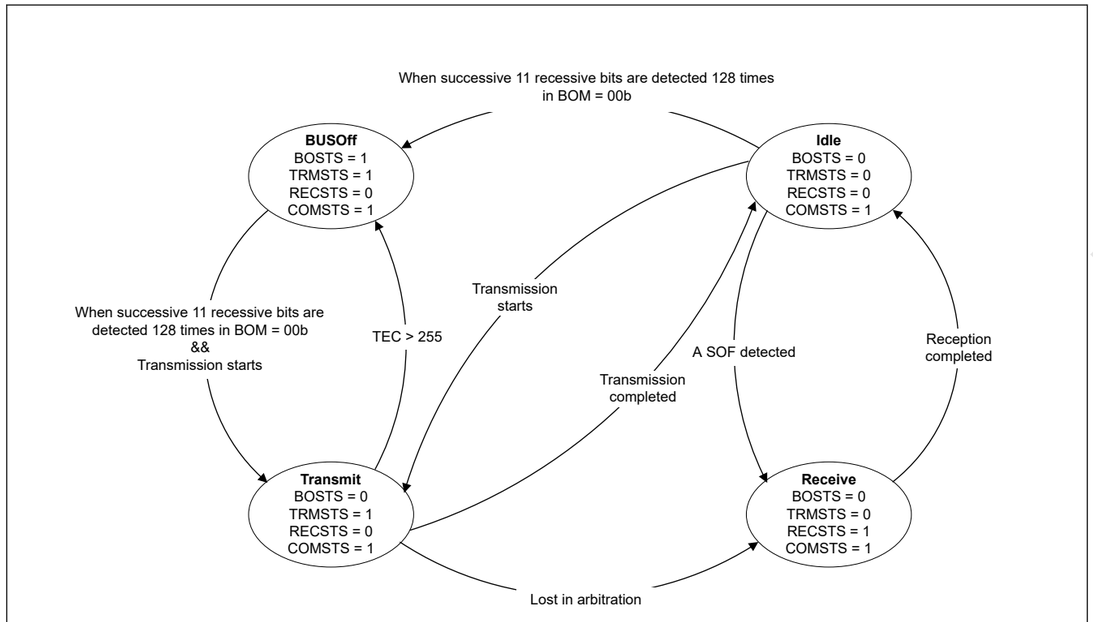


Figure 28.12 Sub-modes of CAN Channel Operation mode (only when BOM = 00b)

28.3.3.5 CAN Channel Bus-Off State

The CAN channel bus-off state is entered according to the fault confinement rules of the CAN specification. The following modes can be configured for returning to the CAN Channel Operation mode from the bus-off state:

- CFDC0CTR.BOM = 00b:
  Bus-Off recovery is compliant to ISO 11898-1, namely the CAN channel re-enters CAN communication (error active state) after 11 consecutive recessive bits are detected 128 times. TEC and REC counters are initialized to 0. The Bus-Off Recovery Flag CFDC0ERFL.BORF is set in this case.
- CFDC0CTR.BOM = 01b:

●通过让通道成为CAN网络上的活动节点来启用通道通信的功能

●释放内部故障限制逻辑，包括接收和发送错误计数器

此时，CAN通道就可以开始发送和接收CAN报文了。

在CAN通道操作模式下，通道可能处于四种不同的子模式，具体取决于执行的通信功能类型（参见图28.12）：

●Channelidle：CAN通道既不接收也不发送

●通道接收：通道正在接收另一个CAN节点发送的CAN报文

●通道传输：通道正在传输CAN报文

Note: 启用自检模式后，通道可能会同时收到自己的消息。

●通道处于总线关闭状态：CAN通道与CAN总线通讯中断。

将通道模式控制位CFDC0CTR.CHMDC设置为通道操作模式后，需要确认通道状态寄存器中的通道复位模式状态位CFDC0STS.CRSTSTS和通道暂停模式状态位CFDC0STS.CHLTSTS已更新以指示成功过渡到频道

可以再次更改相关CFDC0CTR.CHMDC位之前的操作模式。

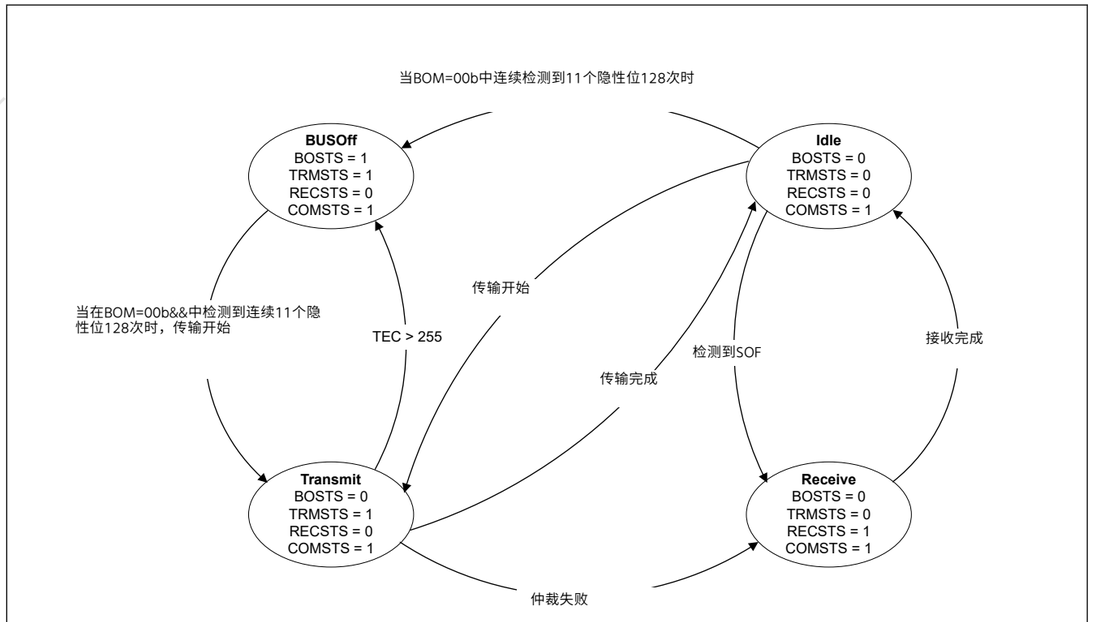


Figure 28.12 CAN通道操作模式的子模式（仅当BOM=00b时）

28.3.3.5 CAN通道总线关闭状态

根据CAN规范的故障限制规则进入CAN通道总线关闭状态。可以配置以下模式以从总线关闭状态返回到CAN通道操作模式：

- CFDC0CTR.BOM = 00b:
  Bus-Off恢复符合ISO11898-1标准，即CAN通道在连续检测到11个隐性位128次后重新进入CAN通信（错误激活状态）。TEC和REC计数器初始化为0。在这种情况下，总线关闭恢复标志CFDC0ERFL.BORF被设置。
- CFDC0CTR.BOM = 01b:

The CAN channel changes the value of the CFDC0CTR.CHMDC bits within the CAN Channel Control Register to 10b and switches immediately to Channel Halt mode automatically after entering bus-off state. TEC and REC counters are initialized to 0 and the Bus-Off Recovery Flag CFDC0ERFL.BORF is not set in this case.

- CFDC0CTR.BOM = 10b:
  The CAN channel changes the value of the CFDC0CTR.CHMDC bits within the CAN Channel Control Register to 10b as soon as it reaches bus-off state and enters Channel Halt mode automatically after the CAN channel has completed the bus-off recovery sequence (after 11 consecutive recessive bits are detected 128 times). TEC and REC counters are initialized to 0 and the Bus-Off Recovery Flag CFDC0ERFL.BORF is set in this case.
- CFDC0CTR.BOM = 11b:
  Bus-off recovery is initiated but CAN channel can immediately enter Channel Halt mode when still in bus-off state if a request is made to enter Channel Halt mode.
  TEC and REC counters are initialized to 0 and the Bus-Off Recovery Flag CFDC0ERFL.BORF is not set.
  Without setting CFDC0CTR.CHMDC [1:0] = 10b and when 11 recessive bits is detected 128 times continuously, transition conditions become the same as CFDC0CTR.BOM = 00b.

Note: If the recovery from bus-off occurs normally in this mode (after waiting for 128 sequences of 11 consecutive recessive bits), and no halt request has been generated during this period, then the Bus-Off Recovery flag CFDC0ERFL.BORF is set.

When software writes to the CFDC0CTR.CHMDC bit at the same time as the CAN channel enters Halt mode (at the start of bus-off when CFDC0CTR.BOM = 01b, or at the end of bus-off when CFDC0CTR.BOM = 10b), the software request has the highest priority.

Note: In the above case, the automatic setting of the CFDC0CTR.CHMDC bit to Channel Halt mode request is performed when the CFDC0CTR.CHMDC bit value is previously 00b (Channel Operation mode).

Additionally, it is possible to force the CAN channel to recover from the bus-off state by setting CFDC0CTR.RTBO to 1. The error state changes from bus-off state to integrating state with a maximum delay of 1 CAN bit time, and the CAN communication becomes possible again after 11 consecutive recessive bits are detected. The Bus-Off Recovery Flag is not set in this case, and the TEC and REC counters are initialized to 0.

Before setting CFDC0CTR.RTBO to 1, all pending transmissions from the TX message buffers, TX Queues and/or Common FIFO in TX mode should be disabled.

The disable of the pending transmission message buffer, TX Queue or FIFO must be confirmed by the corresponding acknowledge flags.

For the TX message buffer, the acknowledge flags are the Transmission Result Flags (CFDTMSTSj.TMTRF). For the TX Queue, it is the TX Queue Empty flag (CFDTXQSTS.TXQEMP). For the FIFO, it is the FIFO Empty flag (CFDCFSTS.CFEMP).

The CFDC0CTR.RTBO bit should be used for bus-off recovery only when CFDC0CTR.BOM is set to 00b.

Setting this bit in any state other than bus-off has no effect and the bit is cleared immediately.

Table 28.16 shows the settings for the Bus-Off Entry flag CFDC0ERFL.BOEF and the Bus-Off Recovery flag CFDC0ERFL.BORF for the different configurations of CFDC0CTR.BOM.

Table 28.16 Behavior of Bus-off Entry and Recovery flags

BOM	BOEF bit set	BORF bit set
00b	Always (on entry to bus-off)	Always (on exit from bus-off)
00b CFDC0CTR.RTBO set to 1	Always (on entry to bus-off)	Only if normal bus-off recovery occurs before software sets CFDC0CTR.RTBO to 1'
01b	Always (on entry to bus-off)	Never
10b	Always (on entry to bus-off)	Always (on exit from bus-off)
11b	Always (on entry to bus-off)	Only if normal bus-off recovery occurs before software issues a Halt request

For an efficient software procedure, it is not necessary to wait for the bus-off recovery sequence to end.

CAN通道将CAN通道控制寄存器中的CFDC0CTR.CHMDC位的值更改为10b，并在进入总线关闭状态后立即自动切换到通道暂停模式。在这种情况下，TEC和REC计数器初始化为0，并且总线关闭恢复标志CFDC0ERFL.BORF未设置。

- CFDC0CTR.BOM = 10b:
  CAN通道一旦到达总线关闭状态，就会将CAN通道控制寄存器中的CFDC0CTR.CHMDC位的值更改为10b，并在CAN通道完成总线关闭恢复序列后自动进入ChannelHalt模式（经过11连续的隐性位被检测到128次）。在这种情况下，TEC和REC计数器被初始化为0，并且总线关闭恢复标志CFDC0ERFL.BORF被设置。

- CFDC0CTR.BOM = 11b:
  总线关闭恢复已启动，但如果请求进入通道暂停模式，CAN通道仍处于总线关闭状态时可立即进入通道暂停模式。TEC和REC计数器初始化为0，并且总线关闭恢复标志CFDC0ERFL.BORF未设置。

  不设置CFDC0CTR.CHMDC[1:0]=10b且连续128次检测到11个隐性位时，转换条件与CFDC0CTR.BOM=00b相同。

Note: 如果在此模式下从总线关闭中恢复正常（在等待128个序列的11个连续隐性位之后），并且在此期间没有产生暂停请求，则总线关闭恢复标志CFDC0ERFL.BORF被设置。

当软件在CAN通道进入暂停模式的同时写入CFDC0CTR.CHMDC位（当CFDC0CTR.BOM=01b时在总线关闭开始时，或者当CFDC0CTR.BOM=10b时在总线关闭结束时），软件请求具有最高优先级。

Note: 在上述情况下，当CFDC0CTR.CHMDC位的值先前为00b（通道操作模式）时，会执行将CFDC0CTR.CHMDC位自动设置为通道暂停模式请求。

此外，可以通过将CFDC0CTR.RTBO设置为1来强制CAN通道从总线关闭状态恢复。错误状态从总线关闭状态变为积分状态，最大延迟为1个CAN位时间，并且在检测到11个连续的隐性位后，CAN通信再次成为可能。在这种情况下，不设置总线关闭恢复标志，并且TEC和REC计数器初始化为0。

在将CFDC0CTR.RTBO设置为1之前，来自TX消息缓冲区、TX队列和或TX模式下的通用FIFO应禁用。

未决传输消息缓冲区、TX队列或FIFO的禁用必须由相应的确认标志确认。

对于TX消息缓冲区，确认标志是传输结果标志(CFDTMSTSj.TMTRF)。对于TX Queue，它是TXQueueEmpty标志（CFDTXQSTS.TXQEMP）。对于FIFO，它是FIFO空标志(CFDCFSTS.CFEMP)。

只有当CFDC0CTR.BOM设置为00b时，才应使用CFDC0CTR.RTBO位进行总线关闭恢复。

将该位设置为除总线关闭以外的任何状态均无效，并且该位立即被清除。

表28.16显示了Bus-OffEntry标志CFDC0ERFL.BOEF和Bus-OffRecovery标志的设置CFDC0ERFL.BORF用于CFDC0CTR.BOM的不同配置。

Table 28.16 总线关闭进入和恢复标志的行为

BOM	BOEF位组	BORF位组
00b	总是（在进入巴士下车时）	总是（在巴士下车的出口处）
00bCFDC0CTR.RTBO设置为1	总是（在进入巴士下车时）	只有在软件设置之前发生正常的总线关闭恢复CFDC0CTR.RTBO to 1'
01b	总是（在进入巴士下车时）	Never
10b	总是（在进入巴士下车时）	总是（在巴士下车的出口处）
11b	总是（在进入巴士下车时）	只有在软件发出暂停请求之前发生正常的总线关闭恢复

对于有效的软件程序，不必等待总线关闭恢复序列结束。

It is possible to perform a transmission re-initialization during bus-off recovery. To do this, follow the recommended software flow in Figure 28.13.

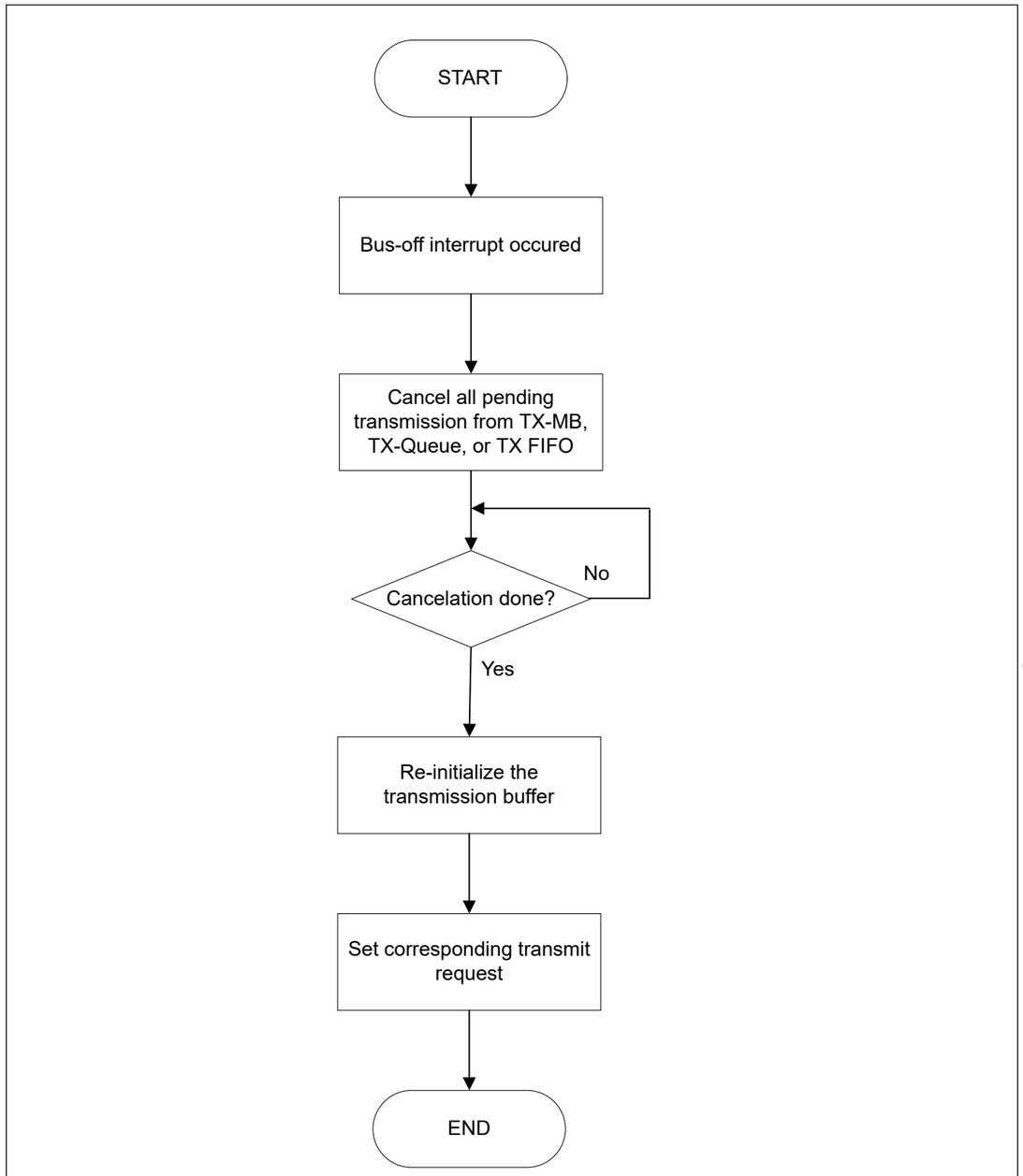


Figure 28.13 Transmission re-initialization during bus-off

28.3.4 Global Mode and Channel Mode Transition Interactions

The interaction between Global mode setting and Channel mode setting is as follows:

可以在总线关闭恢复期间执行传输重新初始化。为此，请遵循图28.13中推荐的软件流程。

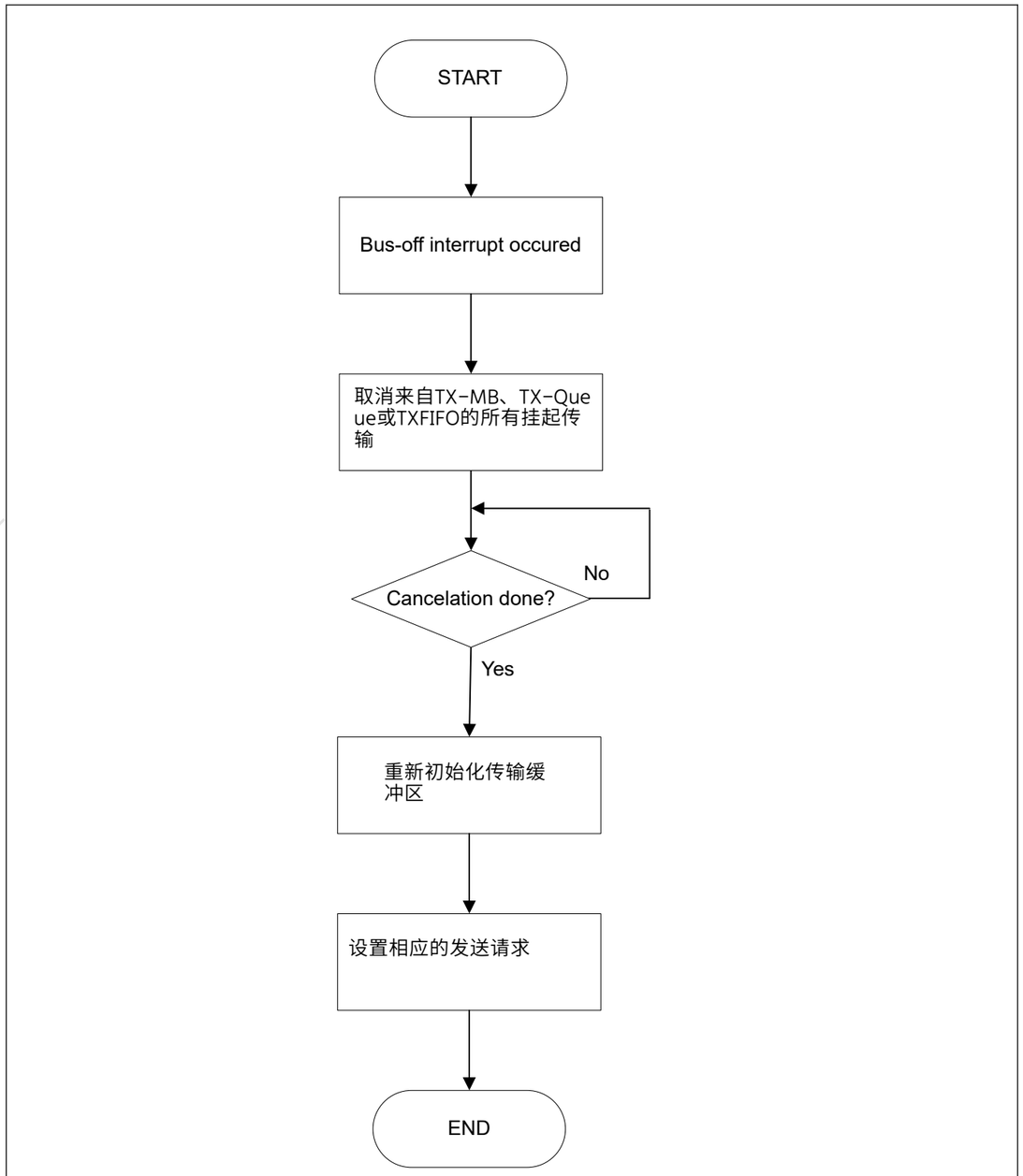


Figure 28.13 总线关闭期间的传输重新初始化

28.3.4 全局模式和通道模式转换交互

Global模式设置和Channel模式设置的交互如下：

- Changing the Channel Mode Control bit CFDC0CTR.CHMDC in the Channel Control Registers does not affect the Global Mode Control bit CFDGCTR.GMDC.
- Changing the Global Mode Control bit CFDGCTR.GMDC affects the channel mode control as described in Table 28.17.

Table 28.17 Interaction between Global and Channel mode transition

Global mode change	Channel mode	Channel mode transition action
Sleep → Reset	Sleep	Channel remains in Sleep mode
Sleep → Halt	— (Global mode change not possible)	
Sleep → Operation	— (Global mode change not possible)	
Reset → Sleep	Sleep	Channel remains in Sleep mode
	Reset	Channel Sleep request bit is set automatically, channel enters Sleep Mode
Reset → Halt	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
Reset → Operation	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
Halt → Sleep	— (Global mode change not possible)	
Halt → Reset	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
	Halt	Channel mode control is set to Reset mode, channel enters Reset mode
Halt → Operation	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
	Halt	Channel remains in Halt mode
Operation → Sleep	— (Global mode change not possible)	
Operation → Reset	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
	Halt	Channel mode control is set to Reset mode, channel enters Reset mode
	Operation	Channel mode control is set to Reset mode, channel enters Reset mode
Operation → Halt	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
	Halt	Channel remains in Halt mode
	Operation	Channel mode control is set to Halt mode, channel enters Halt mode after communication finished

28.3.4.1 Timing of Global Mode Change

The transition time for the Global mode changes are shown in the following table.

Table 28.18 Maximum transition time for the global mode (1 of 2)

From	To	Maximum transition time
GL_SLEEP	GL_RESET	3 peripheral clock cycles*2
GL_RESET	GL_SLEEP	3 peripheral clock cycles
GL_RESET	GL_HALT	10 peripheral clock cycles
GL_RESET	GL_OPERATION	10 peripheral clock cycles

●更改通道控制寄存器中的通道模式控制位CFDC0CTR.CHMDC不会影响全局模式控制位CFDGCTR.GMDC。

●更改全局模式控制位CFDGCTR.GMDC会影响通道模式控制，如表28.17所述。

Table 28.17 全局和通道模式转换之间的交互

全局模式改变	频道模式	通道模式转换动作
睡眠→重置	Sleep	通道保持休眠模式
睡眠→暂停	—（无法更改全局模式）	
睡眠→操作	—（无法更改全局模式）	
重置→睡眠	Sleep	通道保持休眠模式
	Reset	通道休眠请求位自动置位，通道进入休眠状态 Mode
重置→暂停	Sleep	通道保持休眠模式
	Reset	通道保持在复位模式
重置→操作	Sleep	通道保持休眠模式
	Reset	通道保持在复位模式
暂停→睡眠	—（无法更改全局模式）	
暂停→重置	Sleep	通道保持休眠模式
	Reset	通道保持在复位模式
	Halt	通道模式控制设置为复位模式，通道进入复位模式
暂停→运行	Sleep	通道保持休眠模式
	Reset	通道保持在复位模式
	Halt	通道保持暂停模式
运行→睡眠	—（无法更改全局模式）	
操作→复位	Sleep	通道保持休眠模式
	Reset	通道保持在复位模式
	Halt	通道模式控制设置为复位模式，通道进入复位模式
	Operation	通道模式控制设置为复位模式，通道进入复位模式
运行→停止	Sleep	通道保持休眠模式
	Reset	通道保持在复位模式
	Halt	通道保持暂停模式
	Operation	通道模式控制设置为Halt模式，通讯结束后通道进入Halt模式

28.3.4.1 全局模式变化的时机

全局模式更改的转换时间如下表所示。

Table 28.18 全局模式的最大转换时间（1of2）

From	To	最长过渡时间
GL_SLEEP	GL_RESET	3个外设时钟周期*2
GL_RESET	GL_SLEEP	3个外设时钟周期
GL_RESET	GL_HALT	10个外设时钟周期
GL_RESET	GL_OPERATION	10个外设时钟周期

Table 28.18 Maximum transition time for the global mode (2 of 2)

From	To	Maximum transition time
GL_HALT	GL_RESET	2 CAN bit times
GL_HALT	GL_OPERATION	3 peripheral clock cycles
GL_OPERATION	GL_RESET	2 CAN bit times
GL_OPERATION	GL_HALT	3 CAN frames*1 *3

Note 1. The given transition time is the time without any errors on the bus. In case of an error condition, the transition time can lengthen to an uncalculated result. The transition time can also come to a stuck condition for locked RX lines or continued error conditions.
Note 2. Exit GL_SLEEP mode only when CFDGSTS.GRAMINIT is cleared.
Note 3. TQ, CAN frame and CAN bits are related to the individual channels. For the maximum transition time, the channel with the lowest baud rate must be used.

28.3.4.2 Timing of Channel Mode Change

The transition time for the Channel mode changes are shown in the following table.

Table 28.19 Maximum transition time for the channel mode

From	To	max. transition time
CH_SLEEP	CH_RESET	3 peripheral clock cycles
CH_RESET	CH_SLEEP	3 peripheral clock cycles
CH_RESET	CH_HALT	3 CAN bit times
CH_RESET	CH_OPERATION	4 CAN bit times
CH_HALT	CH_RESET	2 CAN bit times
CH_HALT	CH_OPERATION	4 CAN bit times*3
CH_OPERATION	CH_RESET	2 CAN bit times
CH_OPERATION	CH_HALT	2 CAN frames*1 *2

Note 1. The time specified for this transition does not include the case where channel enters bus-off state. For bus-off, the timing depends on the configuration of the CFDC0CTR.BOM[1:0] bits.
Note 2. The given transition time is the time without any errors on the bus. In case of an error condition, the transition time can lengthen to an uncalculated result. The transition time can also come to a stuck condition for locked RX lines or continued error conditions.
Note 3. In general, if the baudrate prescaler value CFDC0NCFG.NBRP is changed in CH_HALT mode, the transition time can deviate. The internal prescaler is a free running down counter that creates the TQ clock, and new BRP value is captured when the counter reaches the value 0.

28.4 Initialization

Before joining CAN communications, configure the following settings:

- Clock setting
- Bit timing setting (nominal and data rate)
- Baud Rate setting (nominal and data rate)
- CANFD setting
- Acceptance Filter setting (configuration of Global Acceptance Filter List)
- Reception, Transmission and GW-FIFO setting
- CAN Operation mode setting

28.4.1 Initialization of CAN Clock, Bit Timing and Baud Rate

28.4.1.1 Bit Timing Conditions

The following lines describe the composition of each segment and the restriction that apply to the segment setting.

1. Each segment setting
   SS = Fixed to 1 TQ

Table 28.18 全局模式的最大转换时间（2之2）

From	To	最长过渡时间
GL_HALT	GL_RESET	2个CAN位时间
GL_HALT	GL_OPERATION	3个外设时钟周期
GL_OPERATION	GL_RESET	2个CAN位时间
GL_OPERATION	GL_HALT	3个CAN帧*1*3

注1.给定的转换时间是总线上没有任何错误的时间。如果出现错误情况，转换时间可能会延长到无法计算的结果。对于锁定的RX线或持续的错误情况，转换时间也可能达到卡住状态。
注2.仅当CFDGSTS.GRAMINIT被清除时才退出GL_SLEEP模式。
注3.TQ、CAN帧和CAN位与各个通道相关。对于最大转换时间，必须使用具有最低波特率的通道。

28.3.4.2 频道模式改变的时机

通道模式更改的转换时间如下表所示。

Table 28.19 通道模式的最大转换时间

From	To	最大限度。过渡时间
CH_SLEEP	CH_RESET	3个外设时钟周期
CH_RESET	CH_SLEEP	3个外设时钟周期
CH_RESET	CH_HALT	3CAN位时间
CH_RESET	CH_OPERATION	4个CAN位时间
CH_HALT	CH_RESET	2个CAN位时间
CH_HALT	CH_OPERATION	4CAN位时间*3
CH_OPERATION	CH_RESET	2个CAN位时间
CH_OPERATION	CH_HALT	2个CAN帧*1*2

注1.为该转换指定的时间不包括通道进入总线关闭状态的情况。对于总线关闭，时序取决于CFDC0CTR.BOM[1:0]位的配置。

注2.给定的转换时间是总线上没有任何错误的时间。如果出现错误情况，转换时间可能会延长到无法计算的结果。对于锁定的RX线或持续的错误情况，转换时间也可能达到卡住状态。
注3.一般情况下，如果在CH_HALT模式下改变波特率预分频器值CFDC0NCFG.NBRP，则转换时间可能会发生偏差。内部预分频器是一个自由运行的递减计数器，它创建TQ时钟，当计数器达到值0时，捕获新的BRP值。

28.4 Initialization

在加入CAN通信之前，请配置以下设置：

●时钟设置
●位定时设置（标称和数据速率）
●波特率设置（标称和数据速率）
- CANFD setting
●验收过滤器设置（全局验收过滤器列表的配置）
●接收、发送和GW-FIFO设置
●CAN操作模式设置

28.4.1 CAN时钟、位时序和波特率的初始化

28.4.1.1 位时序条件

以下几行描述了每个段的组成以及适用于段设置的限制。

1.每段设置SS=Fixedto
1TQ

TSEG1 = See to (CFDC0NCFG) and (CFDC0DCFG)*1
TSEG2 = See to (CFDC0NCFG) and (CFDC0DCFG)*1
SJW = See to (CFDC0NCFG) and (CFDC0DCFG)*1
SS + TSEG1 + TSEG2 = 5 to 49 TQs for Data Bit Rate and 8 to 385 for Nominal Bit Rate

2. Restriction on TSEG1, TSEG2 and SJW
TSEG1(N) > TSEG2(N) ≥ SJW(N)
TSEG1(D) ≥ TSEG2(D) ≥ SJW(D)*1
When only classical frames are used, configure the bit fields TSEG1 and TSEG2 of CFDC0DCFG to valid values.

Note 1. This feature is not available in the classical CAN function.

Table 28.20 shows an example of how to set the bit timing to achieve the required Sample Point settings.

Table 28.20 Bit timing examples

1 bit	Set value (TQ)				Sample point*1(%)
	SS	TSEG1	TSEG2	SJW	
5TQ	1	2	2	1	60.00
8TQ	1	4	3	1	62.50
	1	5	2	1	75.00
10TQ	1	6	3	1	70.00
	1	7	2	1	80.00
12TQ	1	8	3	1	75.00
	1	9	2	1	83.33
15TQ	1	10	4	1	73.33
	1	11	3	1	80.00
16TQ	1	10	5	1	68.75
	1	11	4	1	75.00
20TQ	1	12	7	1	65.00
	1	13	6	1	70.00
24TQ	1	15	8	1	66.66
	1	16	7	1	70.83
50TQ	1	39	10	4	80.00

Note 1. Sample point (in case of 75%)

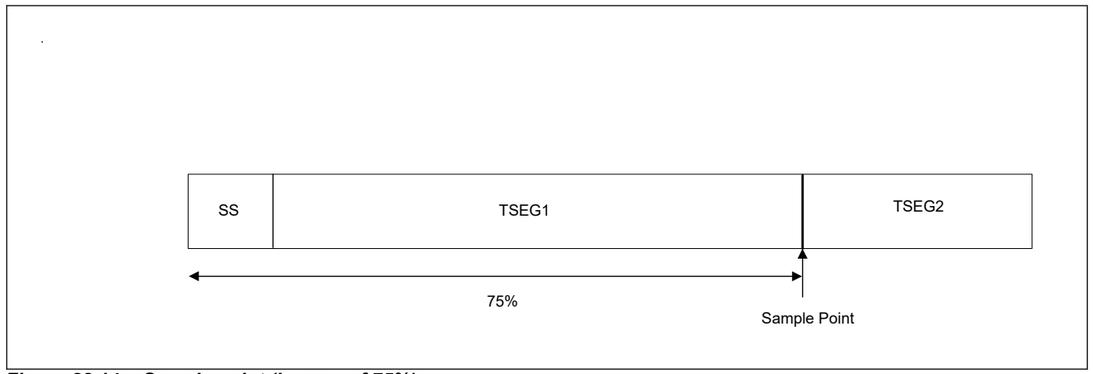


Figure 28.14 Sample point (in case of 75%)

TSEG1=参见(CFDC0NCFG)和(CFDC0DCFG)*1
TSEG2=参见(CFDC0NCFG)和(CFDC0DCFG)*1
SJW=参见(CFDC0NCFG)和(CFDC0DCFG)*1
SS+TSEG1+TSEG2=5到49个TQ用于数据比特率，8到385个用于标称比特率

2.对TSEG1、TSEG2和SJW的限制TSEG1(
N)>TSEG2(N)≥SJW(N)
TSEG1(D) ≥ TSEG2(D) ≥ SJW(D)*1
当仅使用经典帧时，将CFDC0DCFG的位域TSEG1和TSEG2配置为有效值。

注1.此功能在经典CAN功能中不可用。

表28.20显示了如何设置位时序以实现所需采样点设置的示例。

Table 28.20 位时序示例

1 bit	设定值(TQ)				采样点*1(%)
	SS	TSEG1	TSEG2	SJW	
5TQ	1	2	2	1	60.00
8TQ	1	4	3	1	62.50
	1	5	2	1	75.00
10TQ	1	6	3	1	70.00
	1	7	2	1	80.00
12TQ	1	8	3	1	75.00
	1	9	2	1	83.33
15TQ	1	10	4	1	73.33
	1	11	3	1	80.00
16TQ	1	10	5	1	68.75
	1	11	4	1	75.00
20TQ	1	12	7	1	65.00
	1	13	6	1	70.00
24TQ	1	15	8	1	66.66
	1	16	7	1	70.83
50TQ	1	39	10	4	80.00

注1.采样点（在75%的情况下）

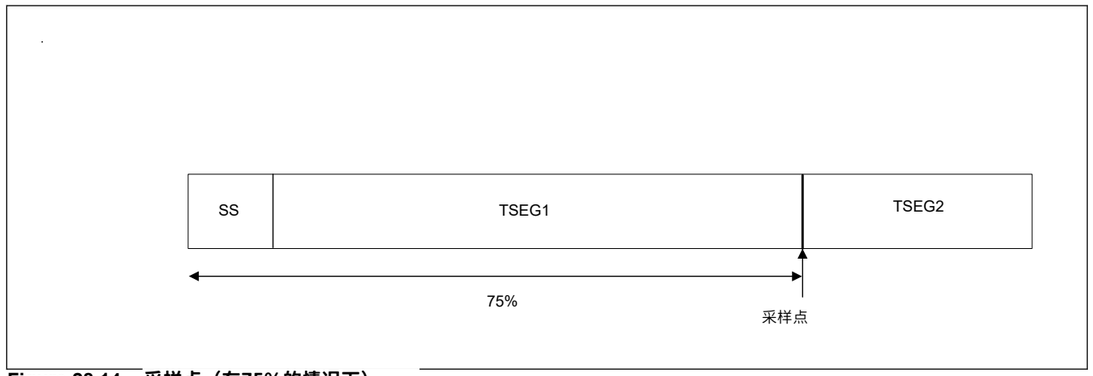


Figure 28.14 采样点（在75%的情况下）

28.4.1.2 CAN Bit Timing

In the CAN protocol, each bit in a communication frame is composed of three segments that can be configured individually for channel using the related CFDC0NCFG and CFDC0DCFG*1 registers.

Note 1. This register is not available in the classical CAN function.

Figure 28.15 shows the segment composition of a bit and the sample point in it.

Of these segments, the Time Segment 1 (TSEG1) and Time Segment 2 (TSEG2) are used to specify the position of the sample point, so that the timing at which each bit on the CAN bus is sampled can be altered by changing the values of these segments.

The minimum resolution for this timing is referred to as Time Quantum (TQ), which is determined by the clock frequency supplied to the CAN channel and the divide-by-N value of the baud rate prescaler (nominal and data rate).

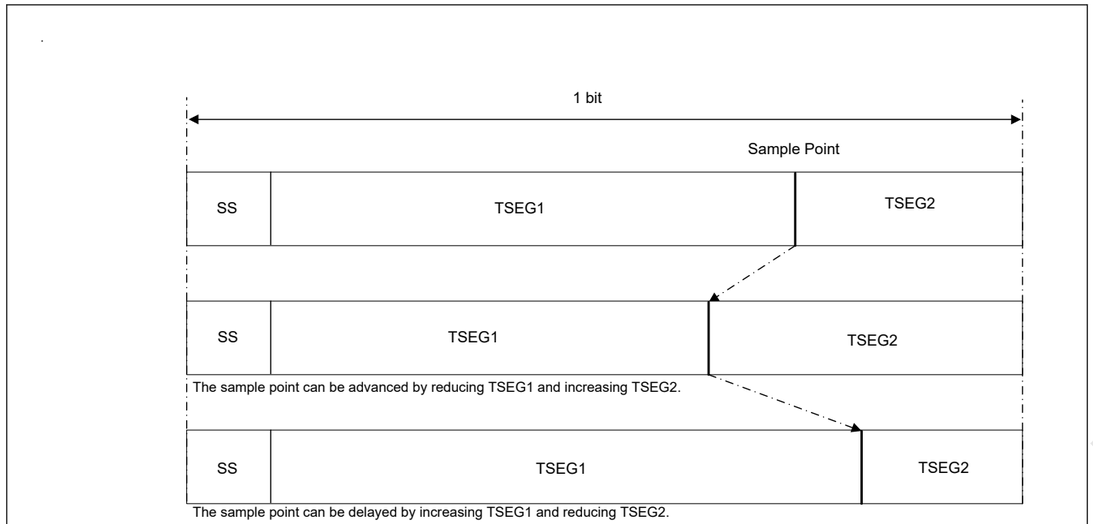


Figure 28.15 Segment composition of a bit and the sample point

1. SS: Synchronization Segment
   This segment is used to synchronize bits by monitoring a recessive-to-dominant edge during the interframe space. This comprises of intermission, suspend transmission, bus idle, during bus idle, and all nodes that can start transmission.
2. TSEG1: Time Segment 1
   This segment absorbs physical delays on the CAN network. A physical delay on the network is two times the total sum of a bus delay, input comparator delay, and output driver delay. It can be lengthened by SJW.
3. TSEG2: Time Segment 2
   This segment is used to correct a phase error by performing resynchronization. It can be shortened by SJW. While sending or receiving a message, communication frames between some nodes may get out of sync due to a drift in the oscillator frequency or a delay in the transmission path. This is referred to as a phase error.
4. SJW: Resynchronization Jump Width
   This is the maximum width by which bits that have become out of sync due to a phase error may be corrected.

Figure 28.15 shows only one symbolic sample point.

28.4.1.3 Baud Rate

Either the CAN channel system clock (clean clock) or the external oscillator clock can be selected globally as CAN communication clock.

The transfer speed is determined by the DLL clock, the divide-by-N value of the baud rate prescaler, and the number of TQs in one bit.

28.4.1.2 CAN位时序

在CAN协议中，通信帧中的每个位由三个段组成，可以使用相关的CFDC0NCFG和CFDC0DCFG*1寄存器单独配置通道。

注1.该寄存器在经典CAN功能中不可用。

图28.15显示了一个位的分段组成和其中的采样点。

在这些段中，时间段1(TSEG1)和时间段2(TSEG2)用于指定采样点的位置，因此可以通过更改值来更改CAN总线上每个位的采样时序这些细分市场。

此时序的最小分辨率称为时间量子(TQ)，它由提供给CAN通道的时钟频率和波特率预分频器的N分频值（标称和数据速率）决定。

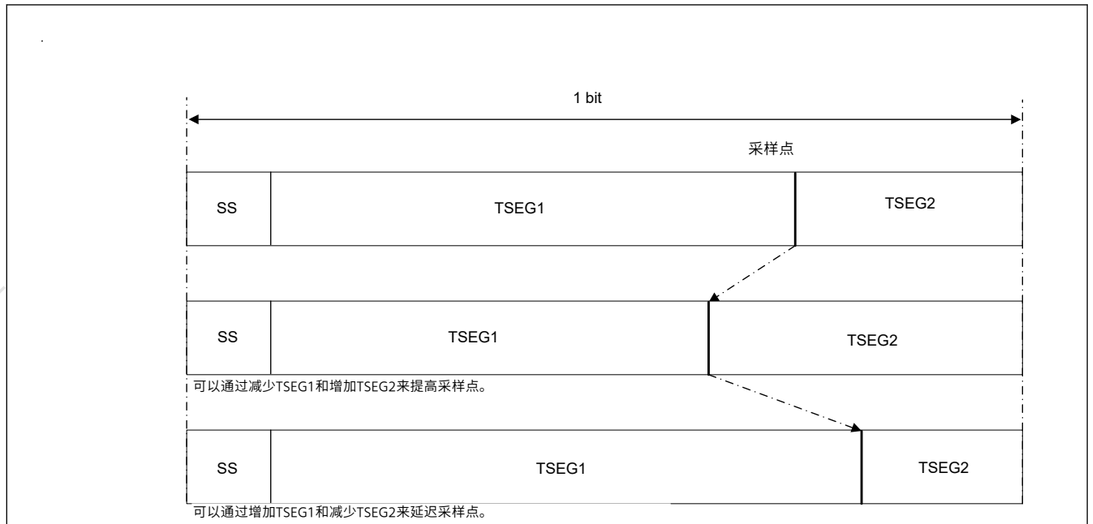


Figure 28.15 位和采样点的段组成

1.SS：同步段
该段用于通过监视帧间空间期间的隐性到显性边缘来同步位。这包括中断、暂停传输、总线空闲、总线空闲期间以及所有可以开始传输的节点。

2.TSEG1：时间段1
该段吸收CAN网络上的物理延迟。网络上的物理延迟是总线延迟、输入比较器延迟和输出驱动器延迟总和的两倍。它可以通过SJW加长。

3.TSEG2：时间段2
该段用于通过执行重新同步来纠正相位误差。它可以被SJW缩短。在发送或接收消息时，某些节点之间的通信帧可能会由于振荡器频率的漂移或传输路径的延迟而失去同步。这被称为相位误差。

4.SJW：再同步跳转宽度
这是由于相位误差而变得不同步的位可以被纠正的最大宽度。

图28.15只显示了一个符号采样点。

28.4.1.3 Baud Rate

CAN通道系统时钟（干净时钟）或外部振荡器时钟均可全局选择作为CAN通信时钟。

传输速度由DLL时钟、波特率预分频器的N分频值和一位TQ的数量决定。

$$\text{baudrate} = \frac{\text{DLL\_Clock}}{(\text{number\_of\_time\_quanta\_per\_bit}) \times (\text{BRP} + 1)}$$

Figure 28.16 shows a block diagram of the circuit that generates the CAN channel system clock and Table 28.21 shows a baud rate examples.

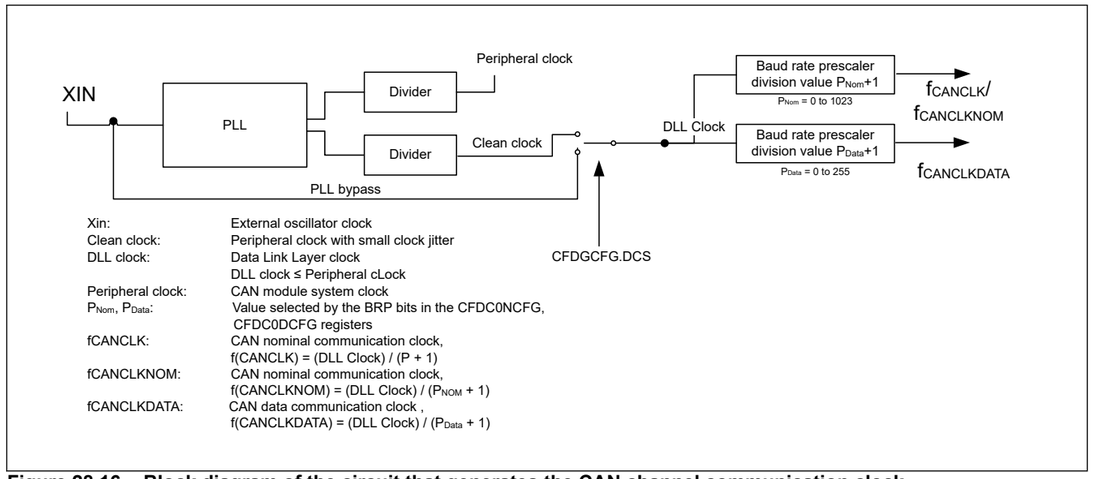


Figure 28.16 Block diagram of the circuit that generates the CAN channel communication clock

Table 28.21 Nominal baud rate calculation formula and example CAN communication configurations

Baud rate calculation formula	(DLL clock) (baud rate prescaler divide-by-N value*1) × (number of TQs in one bit)							
	40 MHz	32 MHz	30 MHz	24 MHz	20 MHz	16 MHz	10 MHz	8 MHz*2
1 Mbps	8TQ (5) 20TQ (2)	8TQ (4) 16TQ (2)	10TQ (3) 15TQ (2)	8TQ (3) 12TQ (2) 24TQ (1)	10TQ (2) 20TQ (1)	8TQ (2) 16TQ (1)	10TQ (1)	8TQ (1)
500 Kbps	8TQ (10) 20TQ (4)	8TQ (8) 16TQ (4)	10TQ (6) 15TQ (4) 20TQ (3)	8TQ (6) 12TQ (4) 24TQ (2)	10TQ (4) 20TQ (2)	8TQ (4) 16TQ (2)	10TQ (2) 20TQ (1)	8TQ (2) 16TQ (1)
250 Kbps	8TQ (20) 20TQ (8)	8TQ (16) 16TQ (8)	10TQ (12) 15TQ (8) 20TQ (6)	8TQ (12) 12TQ (8) 24TQ (4)	10TQ (8) 20TQ (4)	8TQ (8) 16TQ (4)	10TQ (4) 20TQ (2)	8TQ (4) 16TQ (2)
125 Kbps	8TQ (40) 20TQ (16)	8TQ (32) 16TQ (16)	10TQ (24) 15TQ (16) 20TQ (12)	8TQ (24) 12TQ (16) 24TQ (8)	10TQ (16) 20TQ (8)	8TQ (16) 16TQ (8)	10TQ (8) 20TQ (4)	8TQ (8) 16TQ (4)
83.3 Kbps	8TQ (60) 12TQ (40) 16TQ (30) 24TQ (20)	8TQ (48) 12TQ (32) 16TQ (24) 24TQ (16)	8TQ (45) 10TQ (36) 12TQ (30) 15TQ (24) 20TQ (18) 24TQ (15)	8TQ (36) 12TQ (24) 16TQ (18) 24TQ (12)	8TQ (30) 10TQ (24) 12TQ (20) 15TQ (16) 16TQ (15) 20TQ (12) 24TQ (10)	8TQ (24) 12TQ (16) 16TQ (12) 24TQ (8)	8TQ (15) 10TQ (12) 12TQ (10) 15TQ (8) 20TQ (6) 24TQ (5)	8TQ (12)
33.3 Kbps	8TQ (150) 12TQ (100) 16TQ (75) 20TQ (60) 24TQ (50)	8TQ (120) 10TQ (96) 12TQ (80) 15TQ (64) 16TQ (60) 20TQ (48) 24TQ (40)	10TQ (90) 12TQ (75) 15TQ (60) 20TQ (45)	8TQ (90) 10TQ (72) 12TQ (60) 15TQ (48) 16TQ (45) 20TQ (36) 24TQ (30)	8TQ (75) 10TQ (60) 12TQ (50) 15TQ (40) 20TQ (30) 24TQ (25)	8TQ (60) 10TQ (48) 12TQ (40) 15TQ (32) 16TQ (30) 20TQ (24) 24TQ (20)	10TQ (30) 12TQ (25) 15TQ (20) 20TQ (15)	8TQ (30)

Note: Shown in ( ) are the baud rate prescaler divide-by-N value.
Note 1. Baud rate prescaler divide-by-N value = P + 1 (P = 0 - 1023) P: value selected by the BRP bits in the Channel Configuration Registers.
Note 2. Minimum frequency to achieve maximum nominal baud rate of 1 Mbps.

$$\text{baudrate} = \frac{\text{DLL\_Clock}}{(\text{number\_of\_time\_quanta\_per\_bit}) \times (\text{BRP} + 1)}$$

图28.16显示了生成CAN通道系统时钟的电路框图，表28.21显示了波特率示例。

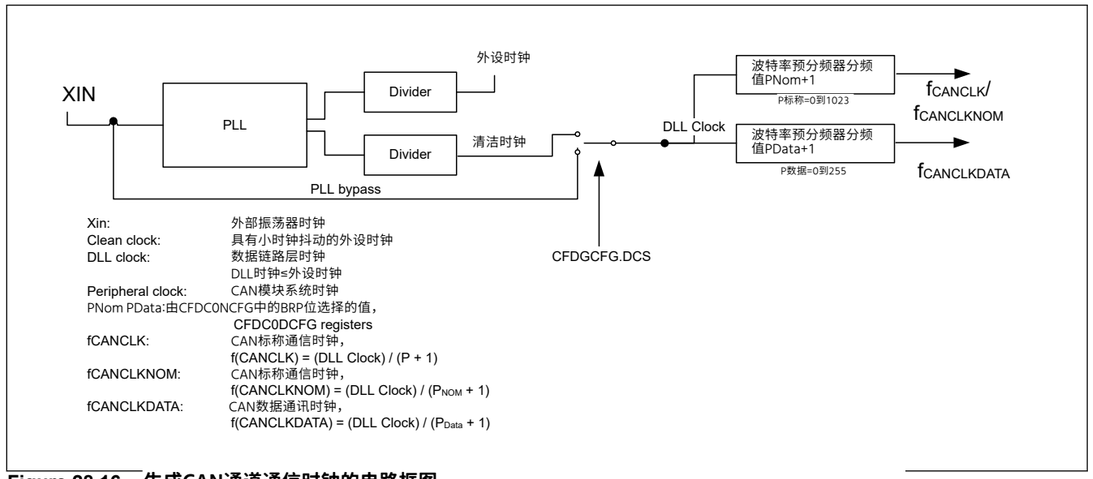


Figure 28.16 生成CAN通道通信时钟的电路框图

Table 28.21 标称波特率计算公式和示例CAN通信配置

波特率计算公式	（DLL时钟）（波特率预分频器除以N值*1）×（一位TQ的数量）							
	40 MHz	32 MHz	30 MHz	24 MHz	20 MHz	16 MHz	10 MHz	8 MHz*2
1 Mbps	8TQ (5) 20TQ (2)	8TQ (4) 16TQ (2)	10TQ (3) 15TQ (2)	8TQ (3) 12TQ (2) 24TQ (1)	10TQ (2) 20TQ (1)	8TQ (2) 16TQ (1)	10TQ (1)	8TQ (1)
500 Kbps	8TQ (10) 20TQ (4)	8TQ (8) 16TQ (4)	10TQ (6) 15TQ (4) 20TQ (3)	8TQ (6) 12TQ (4) 24TQ (2)	10TQ (4) 20TQ (2)	8TQ (4) 16TQ (2)	10TQ (2) 20TQ (1)	8TQ (2) 16TQ (1)
250 Kbps	8TQ (20) 20TQ (8)	8TQ (16) 16TQ (8)	10TQ (12) 15TQ (8) 20TQ (6)	8TQ (12) 12TQ (8) 24TQ (4)	10TQ (8) 20TQ (4)	8TQ (8) 16TQ (4)	10TQ (4) 20TQ (2)	8TQ (4) 16TQ (2)
125 Kbps	8TQ (40) 20TQ (16)	8TQ (32) 16TQ (16)	10TQ (24) 15TQ (16) 20TQ (12)	8TQ (24) 12TQ (16) 24TQ (8)	10TQ (16) 20TQ (8)	8TQ (16) 16TQ (8)	10TQ (8) 20TQ (4)	8TQ (8) 16TQ (4)
83.3 Kbps	8TQ (60) 12TQ (40) 16TQ (30) 24TQ (20)	8TQ (48) 12TQ (32) 16TQ (24) 24TQ (16)	8TQ (45) 10TQ (36) 12TQ (30) 15TQ (24) 20TQ (18) 24TQ (15)	8TQ (36) 12TQ (24) 16TQ (18) 24TQ (12)	8TQ (30) 10TQ (24) 12TQ (20) 15TQ (16) 16TQ (15) 20TQ (12) 24TQ (10)	8TQ (24) 12TQ (16) 16TQ (12) 24TQ (8)	8TQ (15) 10TQ (12) 12TQ (10) 15TQ (8) 20TQ (6) 24TQ (5)	8TQ (12)
33.3 Kbps	8TQ (150) 12TQ (100) 16TQ (75) 20TQ (60) 24TQ (50)	8TQ (120) 10TQ (96) 12TQ (80) 15TQ (64) 16TQ (60) 20TQ (48) 24TQ (40)	10TQ (90) 12TQ (75) 15TQ (60) 20TQ (45)	8TQ (90) 10TQ (72) 12TQ (60) 15TQ (48) 16TQ (45) 20TQ (36) 24TQ (30)	8TQ (75) 10TQ (60) 12TQ (50) 15TQ (40) 20TQ (30) 24TQ (25)	8TQ (60) 10TQ (48) 12TQ (40) 15TQ (32) 16TQ (30) 20TQ (24) 24TQ (20)	10TQ (30) 12TQ (25) 15TQ (20) 20TQ (15)	8TQ (30)

Note: ()中显示的是波特率预分频器除以N的值。
注1.波特率预分频器除以N值=P+1(P=01023)P：由通道配置中的BRP位选择的值
Registers.
注2.实现1Mbps的最大标称波特率的最小频率。

Table 28.22 Baud rate calculation example for nominal and data bit rate CAN communication configurations

Baud rate calculation formula	(DLL clock) (baud rate prescaler divide-by-N value*1) × (number of TQs in one bit)	
	40 MHz	20 MHz
Nominal 1 Mbps Data 5 Mbps	40TQ (1)	20TQ (1)
	8TQ (1)	Not possible
Nominal 500 Kbps Data 2 Mbps	80TQ (1)	40TQ (1)
	20TQ (1)	10TQ (1)

Note: Shown in ( ) are the baud rate prescaler divide-by-N values and this table is not available in the classical CAN function.
Note 1. Baud rate prescaler divide-by-N value = P + 1 (P = 0 - 1023) P: value selected by the BRP bits in the Channel Configuration Registers.

For optimum clock tolerance in networks using the FD frame format, the length of the time quantum should be the same in nominal bit time and in data bit time. This means CFDC0NCFG.NBRP = CFDC0DCFG.DBRP.

Additionally, if transceiver delay compensation is used, do not program the CFDC0DCFG.DBRP bit to be greater than 1, as 1 means divide by 2.

28.4.1.4 Setting of CAN Clock, Bit Timing and Baud Rate

Figure 28.17 shows the procedure for setting the CAN clock and the baud rate for a channel.

These settings should be performed during Channel Reset mode (Configuration mode) for the CAN channels.

Before going to channel communication state, the baud rate must be configured, otherwise the mode does not switch correctly.

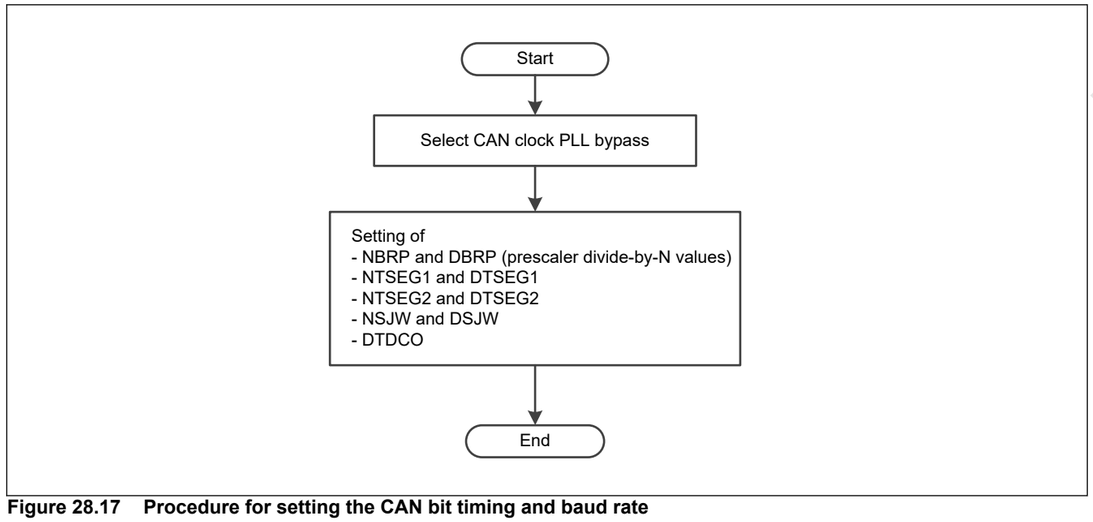


Figure 28.17 Procedure for setting the CAN bit timing and baud rate

28.4.1.5 Transmitter Delay Compensation

This chapter is not valid for classical CAN.

When a high baud rate is used such as 5 Mbps for the data phase, the transmitter delay can become greater than TSEG1. In this case, the transmitter always detects a bit-error in the data phase of the CANFD frame. The TDC compensates for the inability of the transmitter to receive its own transmitted bit at the sample point of that bit.

There is another symbolic sample point known as the Secondary Sample Point (SSP) that is used only during the data phase of CANFD frames. This is derived from the Transceiver Delay Compensation Result bit (CFDC0FDSTS.TDCR) as shown in Figure 28.18.

Table 28.22 标称和数据比特率CAN通信配置的波特率计算示例

波特率计算公式	（DLL时钟）（波特率预分频器除以N值*1）×（一位TQ的数量）	
	40 MHz	20 MHz
Nominal 1 Mbps Data 5 Mbps	40TQ (1)	20TQ (1)
	8TQ (1)	不可能
Nominal 500 Kbps Data 2 Mbps	80TQ (1)	40TQ (1)
	20TQ (1)	10TQ (1)

Note: ()中显示的是波特率预分频器除以N的值，该表在经典CAN函数中不可用。
注1.波特率预分频器除以N值=P+1(P=01023)P：由通道配置中的BRP位选择的值
Registers.

为了在使用FD帧格式的网络中获得最佳时钟容限，时间片的长度在标称位时间和数据位时间中应该相同。这意味着CFDC0NCFG.NBRP=CFDC0DCFG.DBRP。

此外，如果使用收发器延迟补偿，请勿将CFDC0DCFG.DBRP位编程为大于1，因为1表示除以2。

28.4.1.4 CAN时钟、位时序和波特率的设置

图28.17显示了为通道设置CAN时钟和波特率的过程。

这些设置应在CAN通道的通道复位模式（配置模式）期间执行。

在进入通道通信状态之前，必须配置波特率，否则无法正确切换模式。

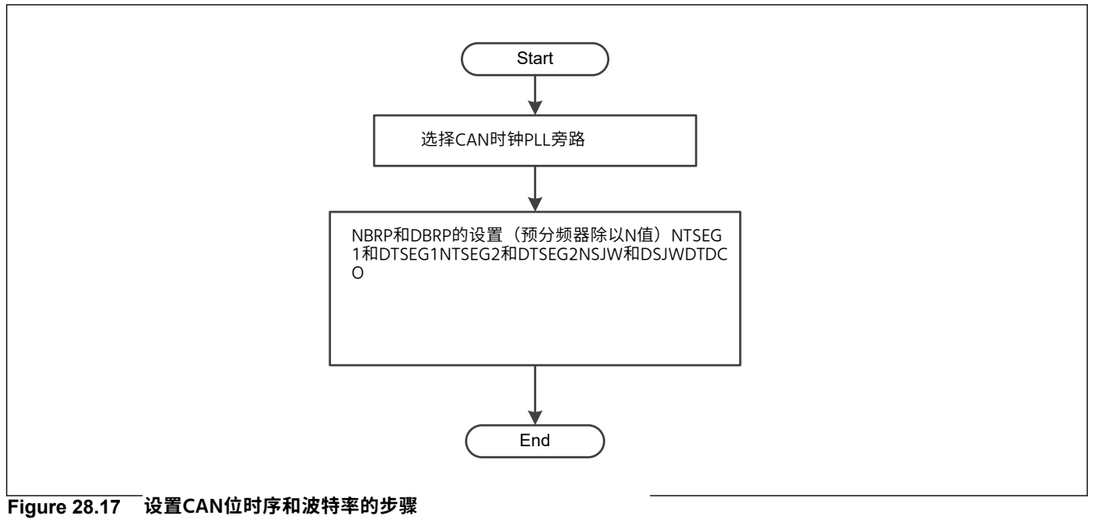


Figure 28.17 设置CAN位时序和波特率的步骤

28.4.1.5 发射机延迟补偿

本章不适用于经典CAN。

当数据阶段使用高波特率（例如5Mbps）时，发送器延迟可能会大于TSEG1。在这种情况下，发送器始终会在CANFD帧的数据阶段检测到位错误。TDC补偿发送器无法在该位的采样点接收其自己的发送位。

还有另一个符号采样点，称为辅助采样点(SSP)，仅在CANFD帧的数据阶段使用。这来自收发器延迟补偿结果位(CFDC0FDSTS.TDCR)，如图28.18所示。

The resolution of the configuration, measured and offset values is based on the CAN channel DLL clock.

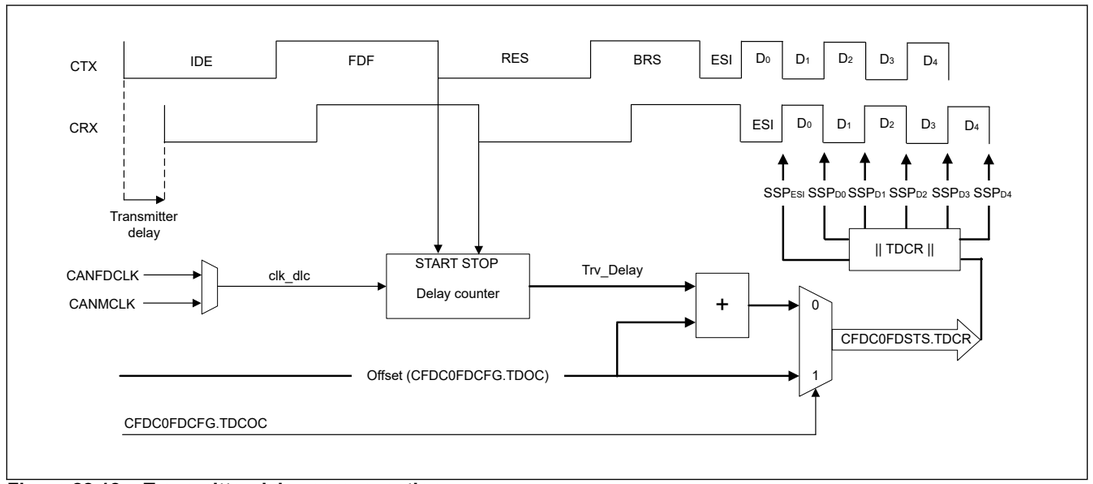


Figure 28.18 Transmitter delay compensation

The measured Trv_Delay is based on the number of clk_dlc clock cycles.The delay is counted up by one for each started clock until the dominant value is seen on CAN_RX. Figure 28.19 shows the measured result. Trv_Delay counted to maximum 127 with a clk_dlc clock.

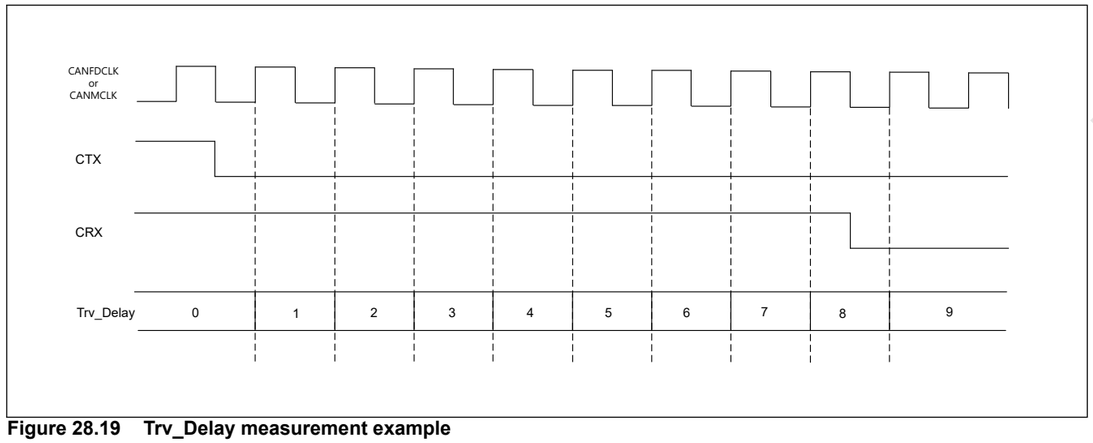


Figure 28.19 Trv_Delay measurement example

The SSP is calculated by taking the result from CFDC0FDSTS.TDCR and rounding the value down to the nearest integer number of data time quanta.

Figure 28.20 shows the positioning of the secondary sample point. When CFDC0FDCFG.TDCOC is equal to 0, the SSP is equal to the Trv_Delay (measured delay) + CFDC0FDCFG.TDCO, rounded down to the nearest integer number of time quanta. Usually, the TDCO value should have the size of (SyncSegmentdata + TSEG1data) to position the SSP to a theoretical location of the sample point.

If the CFDC0FDCFG.TDCOC is equal to 1, the SSP is defined by CFDC0FDCFG.TDCO. If CFDC0DCFG.DBRP is greater than 0, the value is also rounded down to the nearest integer number of time quanta.

配置、测量值和偏移值的分辨率基于CAN通道DLL时钟。

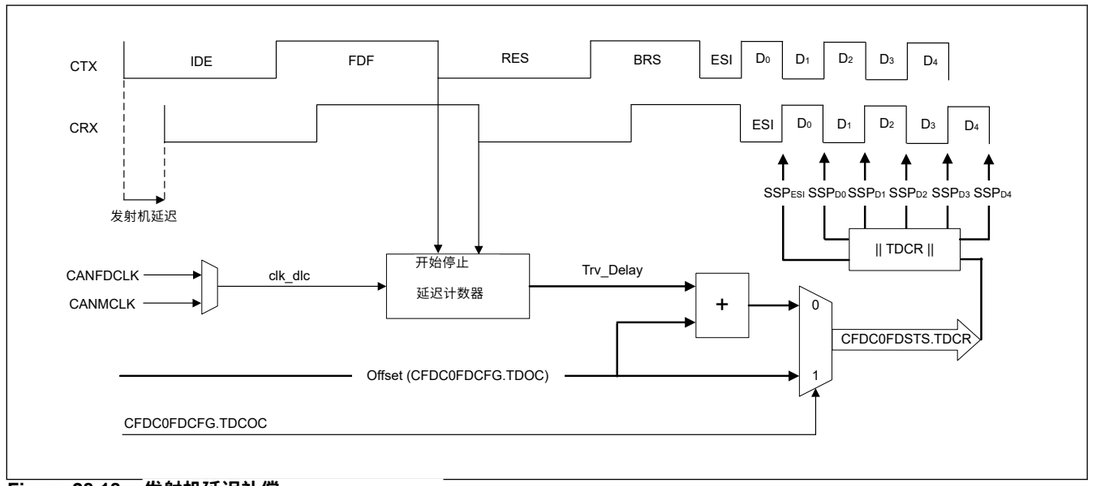


Figure 28.18 发射机延迟补偿

测得的Trv_Delay基于clk_dlc时钟周期数。对于每个启动的时钟，延迟将加一，直到在CAN_RX上看到显性值。图28.19显示了测量结果。使用clk_dlc时钟时，Trv_Delay最大计数为127。

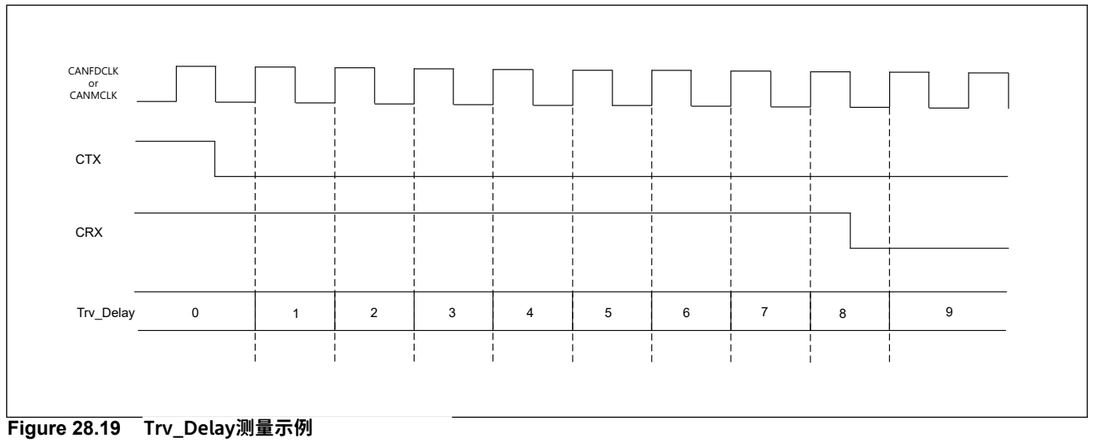


Figure 28.19 Trv_Delay测量示例

SSP是通过从CFDC0FDSTS.TDCR获取结果并将该值向下舍入到最接近的数据时间量整数来计算的。

图28.20显示了辅助采样点的定位。当CFDC0FDCFG.TDCOC等于0时，SSP等于Trv_Delay（测量延迟）+CFDC0FDCFG.TDCO，向下舍入到最接近的整数时间量。通常，TDCO值的大小应为(SyncSegmentdata+TSEG1data)以将SSP定位到采样点的理论位置。

如果CFDC0FDCFG.TDCOC等于1，则SSP由CFDC0FDCFG.TDCO定义。如果CFDC0DCFG.DBRP大于0，则该值也向下舍入到最接近的整数时间量。

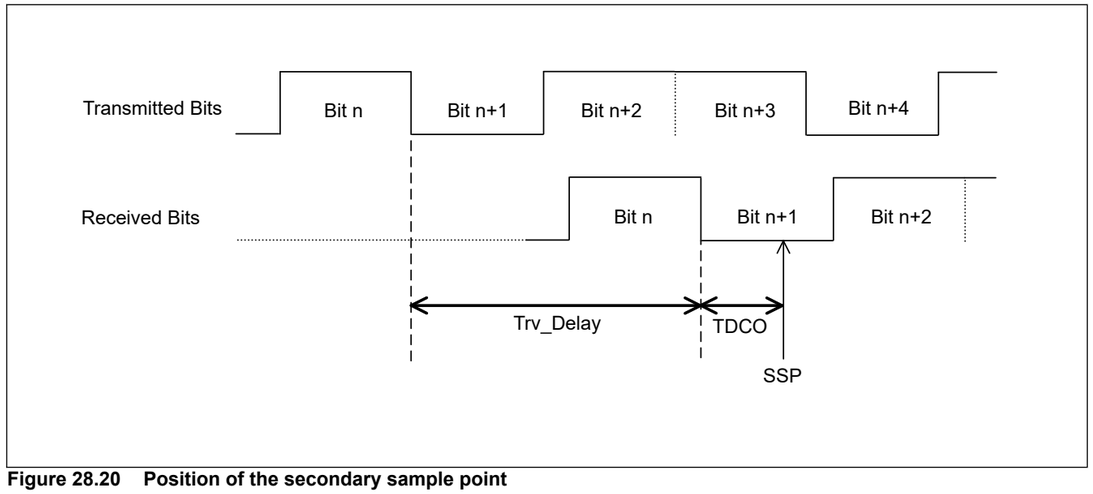


Figure 28.20 Position of the secondary sample point

The maximum delay (Trv_Delay + TDCO) which can be compensated by the CANFD module is (6 data bits - 2clk_dlc).

The ISO 11898-1 allows you to set different values for BRP_data and BRP_nom.

If different values are used for CFDC0NCFG.NBRP and CFDC0DCFG.DBRP, then two CAN nodes may be out of synchronization at the point when the bit rate changes from nominal bit rate to data bit rate after sample point of the BRS bit. This condition is shown in Figure 28.21.

The length of the time quantum should be the same in the nominal bit time and in the data bit time. This means CFDC0NCFG.NBRP = CFDC0DCFG.DBRP.

Different bit rates can be achieved by selecting different configuration values for the Time Segments. The nominal bit rate can be configured from 8 to 385 TQs and the data bit rate from 5 to 49 TQs.

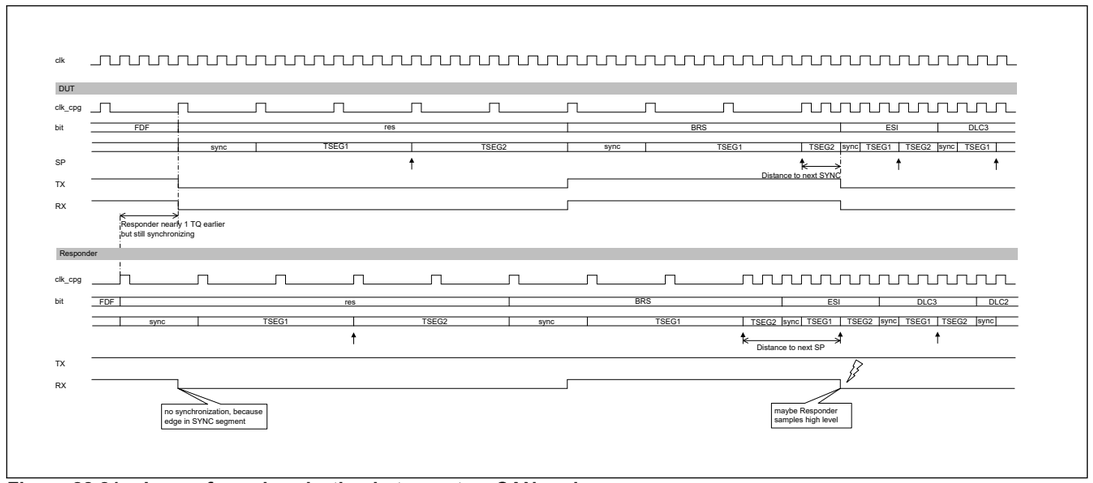


Figure 28.21 Loss of synchronization between two CAN nodes

The transmitter delay compensation measurement result is updated at the falling edge from FDF bit to RES bit when configured accordingly (CFDC0FDCFG.TDCE = 1, CFDC0FDCFG.TDCOC = 0).

Figure 28.22 shows the read flow to get the measured transmitter delay compensation result.

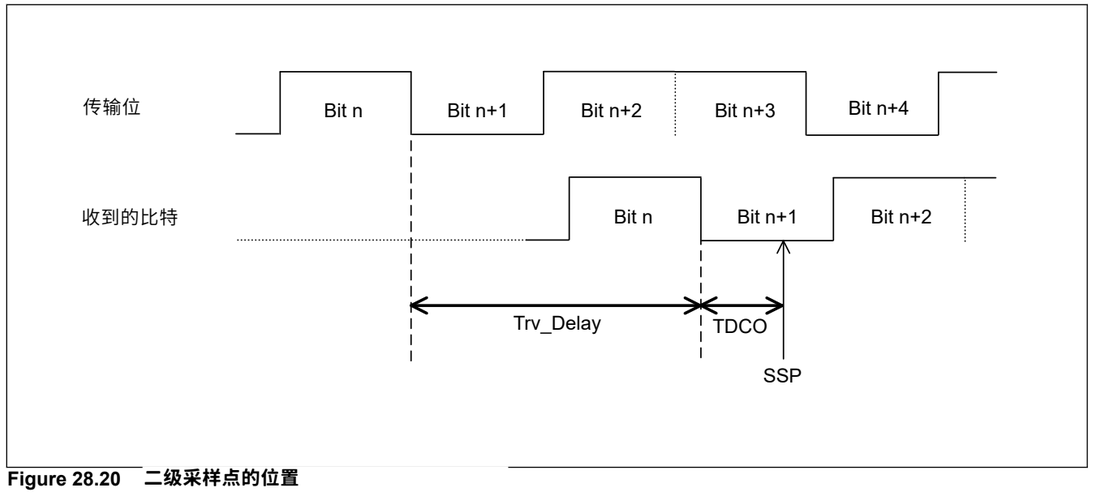


Figure 28.20 二级采样点的位置

CANFD模块可以补偿的最大延迟（Trv_Delay+TDCO）为（6个数据位2clk_dlc）。

ISO11898-1允许您为BRP_data和BRP_nom设置不同的值。

如果CFDC0NCFG.NBRP和CFDC0DCFG.DBRP使用不同的值，则在BRS位采样点之后，当比特率从标称比特率变为数据比特率时，两个CAN节点可能不同步。这种情况如图28.21所示。

时间段的长度在标称位时间和数据位时间中应该相同。这表示
CFDC0NCFG.NBRP = CFDC0DCFG.DBRP.

通过为时间段选择不同的配置值可以实现不同的比特率。标称比特率可配置为8至385TQ，数据比特率可配置为5至49TQ。

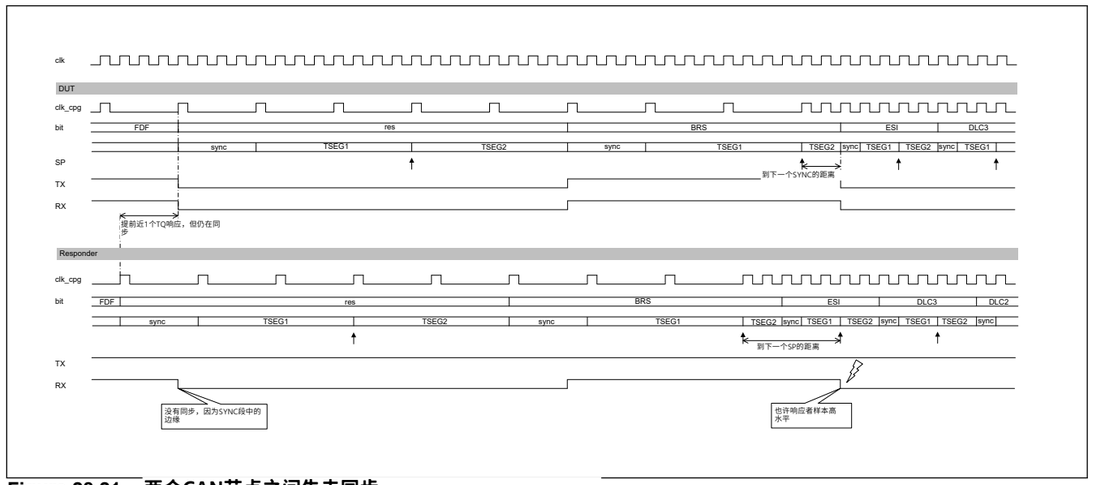


Figure 28.21 两个CAN节点之间失去同步

当相应配置时（CFDC0FDCFG.TDCE=1，CFDC0FDCFG.TDCOC=0），发送器延迟补偿测量结果在FDF位到RES位的下降沿更新。

图28.22显示了读取流程以获得测量的发送器延迟补偿结果。

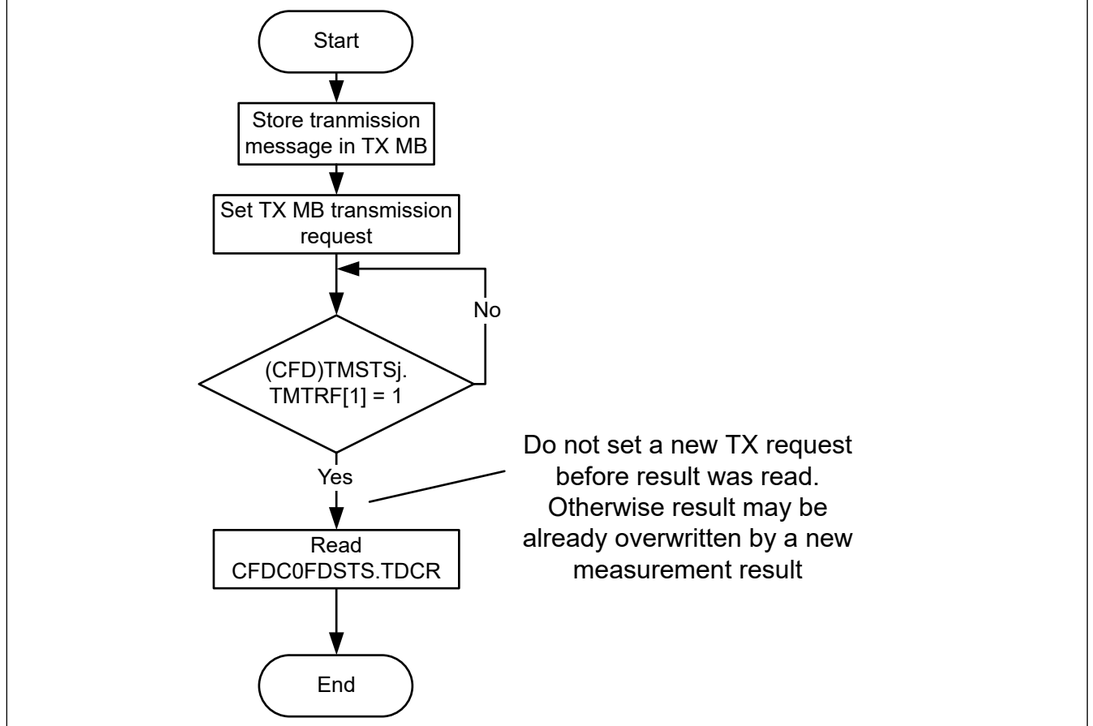


Figure 28.22 TDC result read flow

28.4.2 CAN Module Configuration after Hardware Reset

After a hardware reset (power on reset) or after setting and clearing a CFDGRSTC.SRST bit, the CANFD module enters Global Sleep mode automatically.

To enable configuration of the CANFD module, you must exit Sleep mode by clearing the Global Sleep Request bit CFDGCTR.GSLPR to 0.

After a hardware reset, the module starts RAM initialization, the CFDGSTS.GRAMINIT bit in the Global Status Register is set automatically to indicate that the CANFD logic is initializing the RAM.

After RAM initialization is complete, this bit is cleared automatically.

RAM initialization is necessary to avoid setting of false ECC error flag after HW reset the random data presented in the RAM.

Do not access registers of CANFD in either read or write until RAM initialization is complete and the CFDGSTS.GRAMINIT bit is cleared.

Before going to communication mode, the Global Acceptance Filter List and message FIFO buffers must be configured. In addition, CAN channel must be configured such as CAN bit timing. For this configuration, CAN channel must be released from Channel Sleep mode and must be configured for communication in Channel Reset mode (Configuration mode).

Figure 28.23 shows the configuration procedure. For details about each step, seesection 28.5. Acceptance Filtering Function using Global Acceptance Filter List (AFL), section 28.6. FIFO Buffers and Normal Message Buffer Configuration, section 28.7. Interrupts and DMA and section 28.4.1.3. Baud Rate.

The CANFD module does not perform the RAM initialization sequence after executing a software reset by setting CFDGRSTC.SRST.

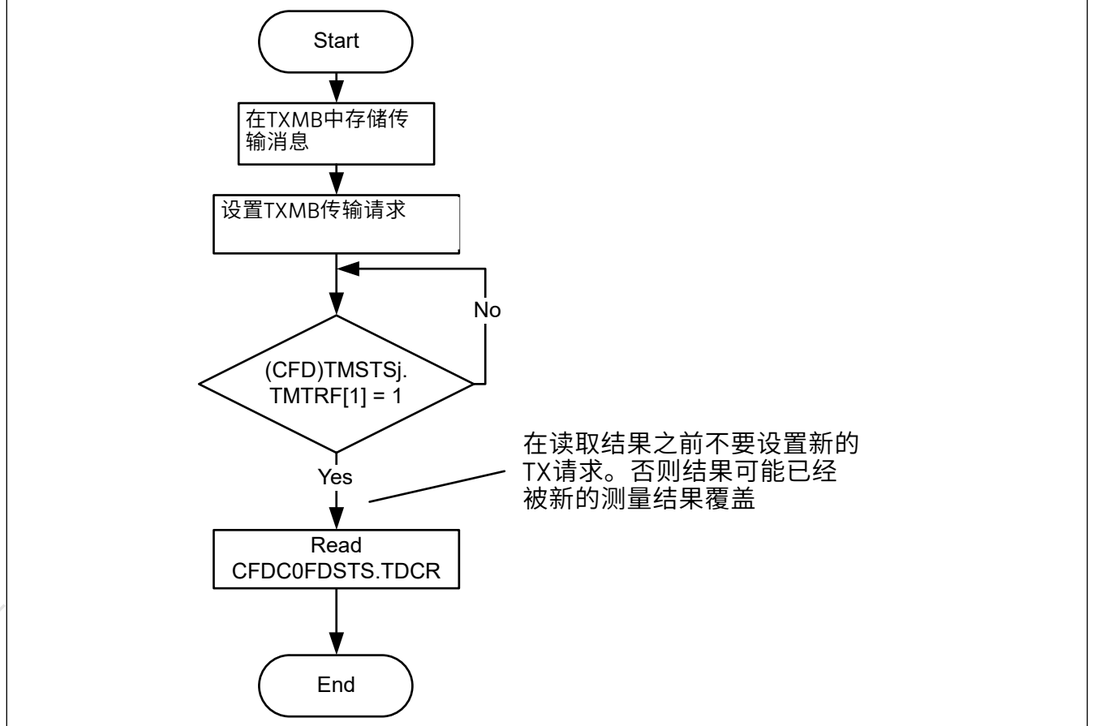


Figure 28.22 TDC结果读取流程

28.4.2 硬件复位后的CAN模块配置

在硬件复位（上电复位）或设置和清除CFDGRSTC.SRST位后，CANFD模块进入全局睡眠模式自动。

要启用CANFD模块的配置，您必须通过清除全局休眠请求位来退出休眠模式CFDGCTR.GSLPR to 0.

硬件复位后，模块开始RAM初始化，全局状态寄存器中的CFDGSTS.GRAMINIT位自动置位，表示CANFD逻辑正在初始化RAM。

RAM初始化完成后，该位自动清零。

RAM初始化是必要的，以避免在硬件重置随机数据后设置错误的ECC错误标志RAM.

在RAM初始化完成之前，不要以读或写方式访问CANFD的寄存器并且CFDGSTS.GRAMINIT位清零。

在进入通信模式之前，必须配置全局接受过滤器列表和消息FIFO缓冲区。此外，CAN通道必须配置如CAN位时序。对于此配置，CAN通道必须从通道休眠模式中释放，并且必须配置为在通道复位模式（配置模式）下进行通信。

图28.23显示了配置过程。有关每个步骤的详细信息，请参阅第28.5节。使用全局接受过滤器列表(AFL)的接受过滤功能，第28.6节。FIFO缓冲区和正常消息缓冲区配置，第28.7节。中断和DMA以及第28.4.1.3节。波特率。

CANFD模块在通过设置执行软件复位后不执行RAM初始化序列CFDGRSTC.SRST.

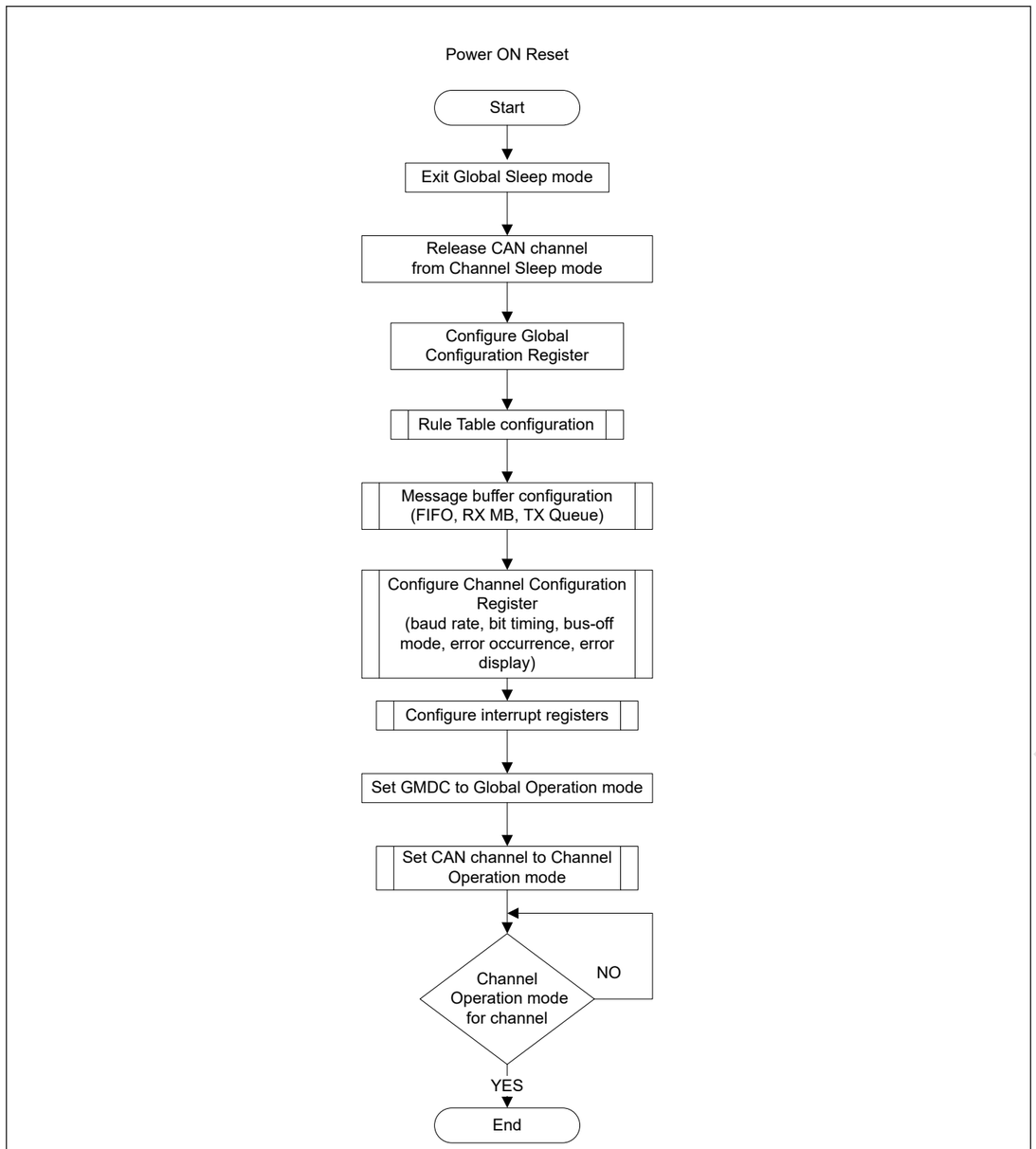


Figure 28.23 Configuration procedure after a hardware reset

28.5 Acceptance Filtering Function using Global Acceptance Filter List (AFL)

28.5.1 Overview

The CANFD module can handle message acceptance filtering with a global Acceptance Filter List (called AFL). Each element of the AFL defines a filter rule for messages received on a specific channel.

The following actions are performed based on the AFL entries:

- Acceptance filtering based on received CAN Identifier and masking

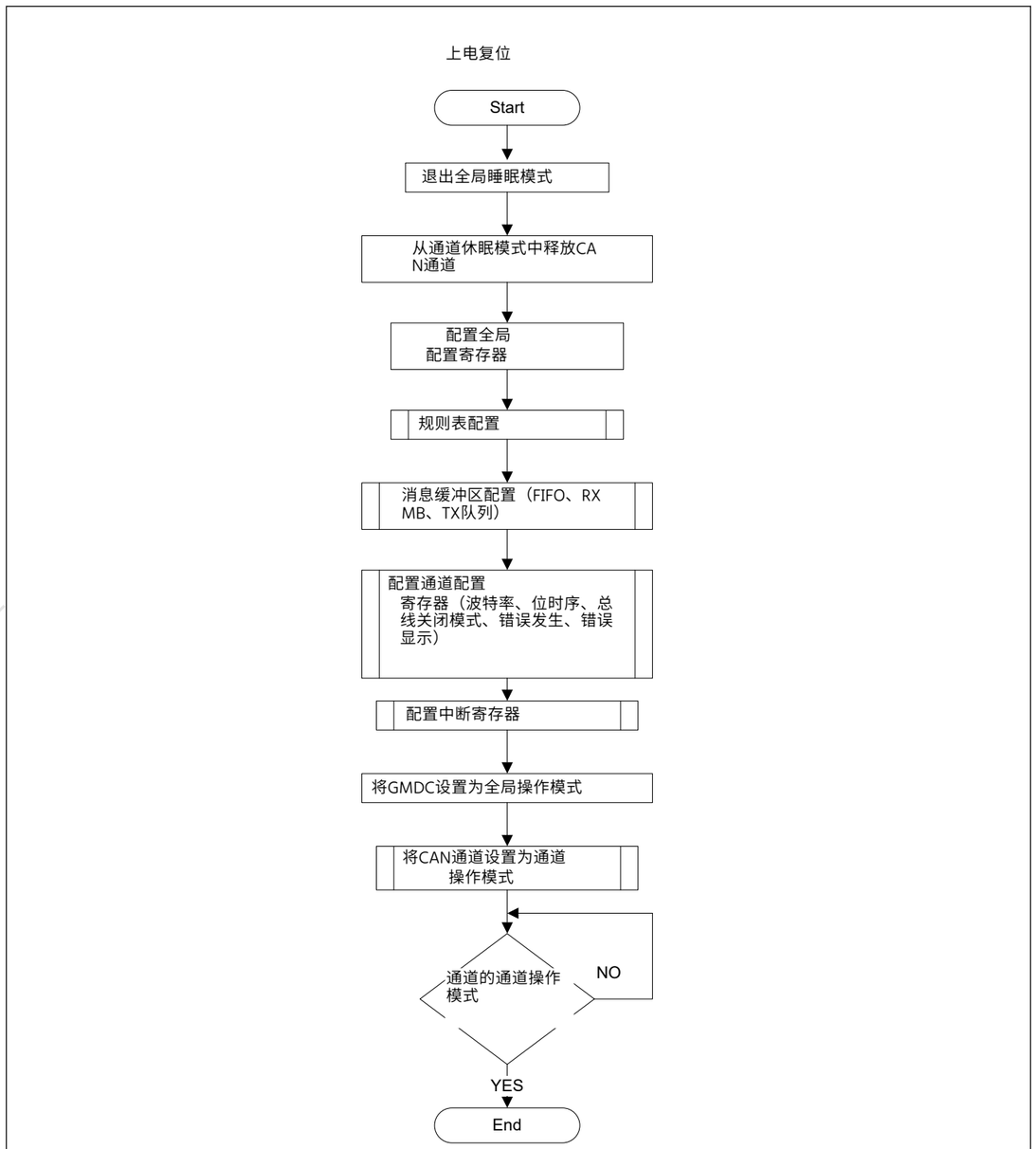


Figure 28.23 硬件复位后的配置过程

28.5 使用全局接受过滤器列表(AFL)的接受过滤功能

28.5.1 Overview

CANFD模块可以使用全局接受过滤器列表（称为AFL）处理消息接受过滤。AFL的每个元素都为在特定通道上接收到的消息定义了一个过滤规则。

根据AFL条目执行以下操作：

- 基于接收到的CAN标识符和掩码的接受过滤

- DLC filtering based on received DLC value
- Message data payload according to the CFDGCFG.CMPOC bit*1
- Storage of accepted messages in the message buffer objects defined in the related AFL entry
- Attaching a 16-bit pointer to the stored messages defined in the related AFL entry, for example to support AUTOSAR applications
- Attaching a 2-bit information label to the stored messages defined in the related AFL entry

Note 1. This feature is not available in the classical CAN function.

The CANFD module allows a maximum of 32 AFL entries.

During acceptance filtering process, each AFL entry in a channel is checked against the received message by the acceptance filter unit. The check starts from the lowest AFL entry number for this channel.

AFL search stops when a match of the received identifier with a configured identifier/mask combination occurs or when the received identifier has been compared against all AFL entries defined for the related channel. If no match occurs, then the received message is rejected. No notification is given to the application in this case.

Additionally, an automatic DLC filtering is performed for each accepted message if DLC check is globally enabled. If the DLC value of the received message is equal to or higher than the configured DLC value in the matching AFL entry, the DLC check is passed.

If DLC replacement (CFDGCFG.DRE bit) is enabled, DLC value configured in the matching AFL entry is greater than 0x0 and DLC check passes, then the configured value of DLC in the matching AFL entry is stored in the destination RXMB or FIFO Buffer.

If the received value of DLC is greater than the configured DLC value in the matching AFL entry, then the additional data bytes received on the CAN Bus are not stored in the destination RXMB or FIFO Buffer. These additional data bytes are stored as 0x00 in the destination RXMB or FIFO Buffer.

If DLC replacement is enabled and DLC value of matching AFL entry is 0x0, then the received value of DLC is stored in the destination RX MB or FIFO Buffer.

If DLC replacement (the CFDGCFG.DRE bit) is disabled and DLC check passes, then the received value of DLC on the CAN bus is stored in the destination RXMB or FIFO buffer.

If the received value of DLC is greater than the configured DLC value in the matching AFL entry, then the additional data bytes received from the CAN bus are also stored in the destination RXMB or FIFO buffer.

If DLC value of the received message is less than the configured DLC value in the matching AFL entry, then DLC check fails. In this case, the received message is rejected and is not stored in any RXMB or FIFO buffer.

Additionally, DLC check failure is flagged by the DLC Error Flag in the Global Error Flag Register. If configured, an error interrupt is also generated. The DLC replacement configuration has no impact if the DLC check fails.

If a message has passed both acceptance filtering and DLC filtering, it is stored in a single reception message buffer and/or in FIFO buffers configured for reception function.

This message storage target information is also defined in the same AFL entry. Do not set a target at the AFL entry which is not configured.

Each accepted received message can be stored into a maximum of 2 different target destinations (single reception message buffer and/or FIFO buffers).

The programming of more than 2 target destinations is not allowed. If more destinations are programmed, then the internal timing might lead to a race condition that prevents the storage of received messages in the message RAM.. Correct configuration of the numbers of target destination is the responsibility of the application.

Additional protection mechanism is made for the case when a received message contains more data payload Bytes than possible to store in the target destination (CFDRMNB.RMPLS, CFDRFCCa.RFPLS or CFDCFCC.CFPLS).

If CFDGCFG.CMPOC = 0, the message is completely rejected and is stored in the target destination. When CFDGCFG.CMPOC = 0 and RX or Common FIFO full including the received message contains more data payload bytes than possible to store in the target destination (CFDRMNB.RMPLS, CFDRFCCa.RFPLS or CFDCFCC.CFPLS), the corresponding CFDFMSTS.RFxMLT or CFDFMSTS.CFxMLT bit is not set to 1, respectively.

●根据接收到的DLC值进行DLC过滤

●根据CFDGCFG.CMPOC位的消息数据有效负载*1

●将接受的消息存储在相关AFL条目中定义的消息缓冲区对象中

●将16位指针附加到相关AFL条目中定义的存储消息，例如以支持AUTOSAR应用程序

●将2位信息标签附加到相关AFL条目中定义的存储消息

注1.此功能在经典CAN功能中不可用。

CANFD模块最多允许32个AFL条目。

在接受过滤过程中，接受过滤单元根据接收到的消息检查通道中的每个AFL条目。检查从该通道的最低AFL条目号开始。

当接收到的标识符与配置的标识符掩码组合发生匹配时，或者当接收到的标识符已与为相关通道定义的所有AFL条目进行比较时，AFL搜索停止。如果不匹配，则拒绝接收到的消息。在这种情况下，不会向应用程序发出通知。

此外，如果全局启用DLC检查，则会对每个接受的消息执行自动DLC过滤。如果
接收到的消息的DLC值等于或高于匹配的AFL条目中配置的DLC值，则
DLC检查通过。

如果启用DLC替换（CFDGCFG.DRE位），匹配AFL条目中配置的DLC值大于0x0并且DLC检查通过，则匹配AFL条目中的DLC配置值存储在目标RXMB或FIFO缓冲区中。

如果接收到的DLC值大于匹配AFL条目中配置的DLC值，则CAN总线上接收到的附加数据字节不会存储在目标RXMB或FIFO缓冲区中。这些额外的数据字节作为0x00存储在目标RXMB或FIFO缓冲区中。

如果启用DLC替换并且匹配AFL条目的DLC值为0x0，则接收到的DLC值存储在目标RXMB或FIFO缓冲区中。

如果DLC替换（CFDGCFG.DRE位）被禁用并且DLC检查通过，则接收到的DLC值在
CAN总线存储在目标RXMB或FIFO缓冲区中。

如果接收到的DLC值大于匹配AFL条目中配置的DLC值，则从CAN总线接收的附加数据字节也将存储在目标RXMB或FIFO缓冲区中。

如果接收到的消息的DLC值小于匹配的AFL条目中配置的DLC值，则DLC检查失败。在这种情况下，接收到的报文被拒绝并且不存储在任何RXMB或FIFO缓冲区中。

此外，DLC检查失败由全局错误标志寄存器中的DLC错误标志标记。如果已配置，还会生成错误中断。如果DLC检查失败，则DLC替换配置没有影响。

如果消息已通过接受过滤和DLC过滤，则将其存储在单个接收消息缓冲区和/或为接收功能配置的FIFO缓冲区中。

该消息存储目标信息也在同一个AFL条目中定义。不要在未配置的AFL条目上设置目标。

每个接受的接收消息最多可以存储到2个不同的目标目的地（单个接收消息缓冲区和/或FIFO缓冲区）。

不允许对超过2个目标目的地进行编程。如果对更多目的地进行了编程，则内部计时可能会导致竞争条件，从而阻止将接收到的消息存储在消息RAM中。正确配置目标目的地的数量是应用程序的责任。

当接收到的消息包含的数据有效负载字节多于目标目的地（CFDRMBB.RMPLS、CFDRFCCa.RFPLS或CFDCFCC.CFPLS）中可能存储的数据时，会采用额外的保护机制。

如果CFDGCFG.CMPOC=0，则消息被完全拒绝并存储在目标目的地中。什么时候
CFDGCFG.CMPOC=0并且RX或CommonFIFOfull（包括接收到的消息）包含的数据有效负载字节数比可能存储在目标目的地（CFDRMNB.RMPLS、CFDRFCCa.RFPLS或CFDCFCC.CFPLS）、相应的CFDFMSTS.RFxMLT或CFDFMSTS中的要多。CFxMLT位不分别设置为1。

When CFDGCFG.CMPOC = 1, the received data bytes greater than CFDRMNB.RMPLS is rejected. When CFDGCFG.CMPOC = 1 and RX or Common FIFO full including the received message contains more data payload bytes than possible to store in the target destination (CFDRMNB.RMPLS, CFDRFCCa.RFPLS or CFDCFCC.CFPLS), the corresponding CFDFMSTS.RFxMLT or CFDFMSTS.CFxMLT bit is set to 1, respectively.

Depending on the CFDGCFG.DRE bit, the original received DLC or the DLC value configured at the AFL entry is stored.

Regardless of the CFDGCFG.CMPOC bit setting, CFDGERFL.CMPOF is set to 1 if a payload overflow condition is detected.

The DLC filtering is performed before the payload overflow function. So for one reception frame, only one flag can be set at the same time with CFDGERFL.DEF or CFDGERFL.CMPOF*1.

Note 1. This bit is not available in the classical CAN function.

28.5.2 Allocation of AFL Entries

The number of AFL entries per channel can be configured using the dedicated field in the related Global Acceptance Filter Configuration Registers (see Figure 28.24).

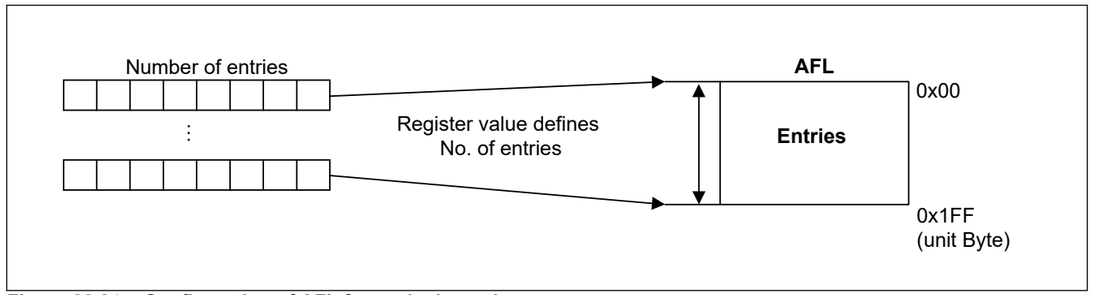


Figure 28.24 Configuration of AFL for each channel

The minimum number of entries for one channel is 0 (no entries defined for the channel) and the maximum number of entries is 32.

All entries are unique for a channel and overlapping or sharing of entries is not supported. Correct configuration of the AFL is the responsibility of the application.

The CANFD module does not flag errors related to the configuration of the AFL.

28.5.3 AFL Entry Description

Each AFL entry consists of 16 bytes. The fields in all entries are identical.

Each entry contains the following information for acceptance filtering and DLC filtering:

- Identifier (11 bits for Standard Frame format, 29 bits for Extended Frame format):
  Acceptance filter unit checks the identifier field of the received message against the identifier field of each AFL entry (full 29 bits masking of identifier bits is possible, see information that follows).
- IDE bit:
  Acceptance filter unit checks the IDE bit of the received message against this bit and selects the relevant part of the identifier field for acceptance filtering (masking of IDE bit is possible, see the information that follows).
- RTR bit:
  Acceptance filter unit only accepts data frames (RTR = 0) or remote frames (RTR = 1) according to the setting of this bit (masking of RTR bit is possible, see the information that follows).
- Loopback Configuration bit:
  This bit can enable or disable the AFL entry depending on the Loopback Configuration or Mirror mode condition.
- Mask for Identifier bits (29 bits):

当CFDGCFG.CMPOC=1时，大于CFDRMNB.RMPLS的接收数据字节被拒绝。什么时候CFDGCFG.CMPOC=1并且RX或CommonFIFOfull（包括接收到的消息）包含的数据有效负载字节数比可能存储在目标目的地（CFDRMNB.RMPLS、CFDRFCCa.RFPLS或CFDCFCC.CFPLS）、相应的CFDFMSTS.RFxMLT或CFDFMSTS中的要多。CFxMLT位分别设置为1。

根据CFDGCFG.DRE位，存储原始接收的DLC或在AFL条目中配置的DLC值。

无论CFDGCFG.CMPOC位设置如何，如果检测到有效负载溢出条件，CFDGERFL.CMPOF将设置为1。

DLC过滤在有效载荷溢出功能之前执行。因此对于一个接收帧，只能使用CFDGERFL.DEF或CFDGERFL.CMPOF*1同时设置一个标志。

注1.该位在经典CAN功能中不可用。

28.5.2 AFL参赛作品的分配

可以使用相关全局接受过滤器中的专用字段配置每个通道的AFL条目数
配置寄存器（见图28.24）。

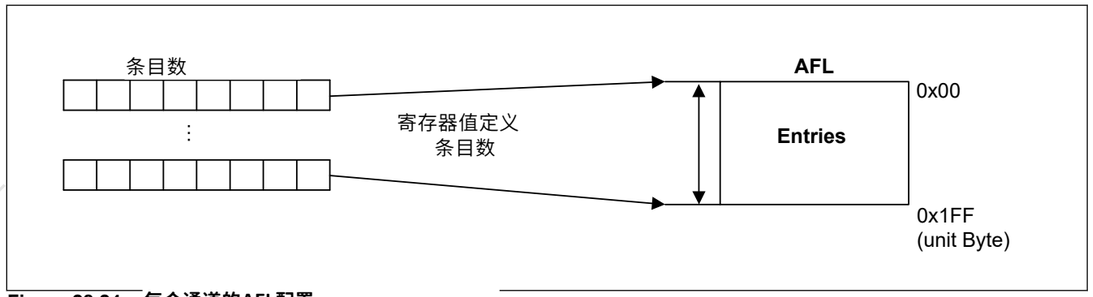


Figure 28.24 每个通道的AFL配置

一个通道的最小条目数为0（没有为通道定义条目），最大条目数为32。

频道的所有条目都是唯一的，不支持条目的重叠或共享。正确配置AFL是应用程序的责任。

CANFD模块不会标记与AFL配置相关的错误。

28.5.3 AFL条目说明

每个AFL条目由16个字节组成。所有条目中的字段都是相同的。

每个条目都包含以下接受过滤和DLC过滤的信息：

●标识符（标准帧格式为11位，扩展帧格式为29位）：
接受过滤器单元根据每个AFL条目的标识符字段检查接收到的消息的标识符字段（标识符位的全29位掩码是可能的，请参阅以下信息）。

- IDE bit:
  接受过滤器单元根据该位检查接收到的消息的IDE位，并选择标识符字段的相关部分进行接受过滤（可以屏蔽IDE位，参见以下信息）。
- RTR bit:
  接受过滤器单元仅根据该位的设置接受数据帧（RTR=0）或远程帧（RTR=1）（RTR位的屏蔽是可能的，参见下面的信息）。
- Loopback Configuration bit:
  该位可以根据环回配置或镜像模式条件启用或禁用AFL条目。

●标识符位掩码（29位）：

Each bit in the identifier mask can mask the corresponding identifier bit in the AFL entry during acceptance filtering, see Figure 28.25.

- Mask for IDE bit:
  If this Mask bit masks the IDE bit of the AFL entry in both Standard Identifier and Extended Identifier format, messages can be accepted by this AFL entry. The identifier of the received message is compared against the Standard Identifier part of the AFL entry for Standard Identifier format messages and against the Extended Identifier part of the AFL entry for Extended Identifier format messages.

- Mask for RTR bit:
  If this Mask bit masks the RTR bit of the AFL entry in both frame formats, data frame and remote frame formats are accepted by this AFL entry.

- Pointer information (16 bits):
  This 16-bit pointer is attached to a received message accepted by the related AFL entry. The pointer is added during message storage in the message buffer area and can be used by application as support function. The pointer information can be used for example to support PDU identifier allocation for the received message in AUTOSAR systems.

- Information label (2 bits):
  This 2-bit label is attached to a received message accepted by the related AFL entry. The label is added during message storage in the message buffer area and can be used by application as support function.

- DLC value for automatic DLC filtering:
  If the DLC value of the received message is equal or higher than the configured DLC value, the DLC check is passed.

If the DLC value in this AFL entry is configured to 0, DLC filtering is effectively disabled for this entry (all accepted messages pass DLC filtering).

Each AFL entry contains the following information for the handling of received messages:

- Message buffer number of one single reception message buffer as target for received message storage
- Single reception message buffer enable bit to configure the single reception message buffer number to be valid or invalid, as target for received message storage
- FIFO direction pointer - each bit of the FIFO direction pointer configures a dedicated FIFO as possible target for a received message

There is no hardware protection against such storage of message. Therefore, the FIFO direction pointer must be configured carefully.

标识符掩码中的每个位都可以在接受过滤期间屏蔽AFL条目中的相应标识符位，见图28.25。

●IDE位掩码：
如果此掩码位以标准标识符和扩展标识符格式屏蔽AFL条目的IDE位，则此AFL条目可以接受消息。接收消息的标识符与标准标识符格式消息的AFL条目的标准标识符部分和扩展标识符部分进行比较

扩展标识符格式消息的AFL条目。

●RTR位掩码：
如果此掩码位在两种帧格式中屏蔽AFL条目的RTR位，则此AFL条目接受数据帧和远程帧格式。

●指针信息（16位）：
这个16位指针附加到相关AFL条目接受的接收消息。该指针是在消息存储过程中在消息缓冲区中添加的，可供应用程序用作支持函数。例如，指针信息可用于支持AUTOSAR系统中接收到的消息的PDU标识符分配。

●信息标签（2位）：
这个2位标签附加到相关AFL条目接受的接收消息。该标签是在消息存储过程中在消息缓冲区中添加的，可供应用程序用作支持功能。

●自动DLC过滤的DLC值：
如果接收到的消息的DLC值等于或大于配置的DLC值，则DLC检查通过。

如果此AFL条目中的DLC值配置为0，则有效禁用此条目的DLC过滤（所有接受的消息都通过DLC过滤）。

每个AFL条目都包含以下用于处理接收到的消息的信息：

●作为接收消息存储目标的单个接收消息缓冲区的消息缓冲区号
●单次接收报文缓冲区使能位，用于配置单次接收报文缓冲区号有效或无效，作为接收报文存储的目标

●FIFO方向指针FIFO方向指针的每一位配置一个专用的FIFO作为接收消息的可能目标

没有针对此类消息存储的硬件保护。因此，必须仔细配置FIFO方向指针。

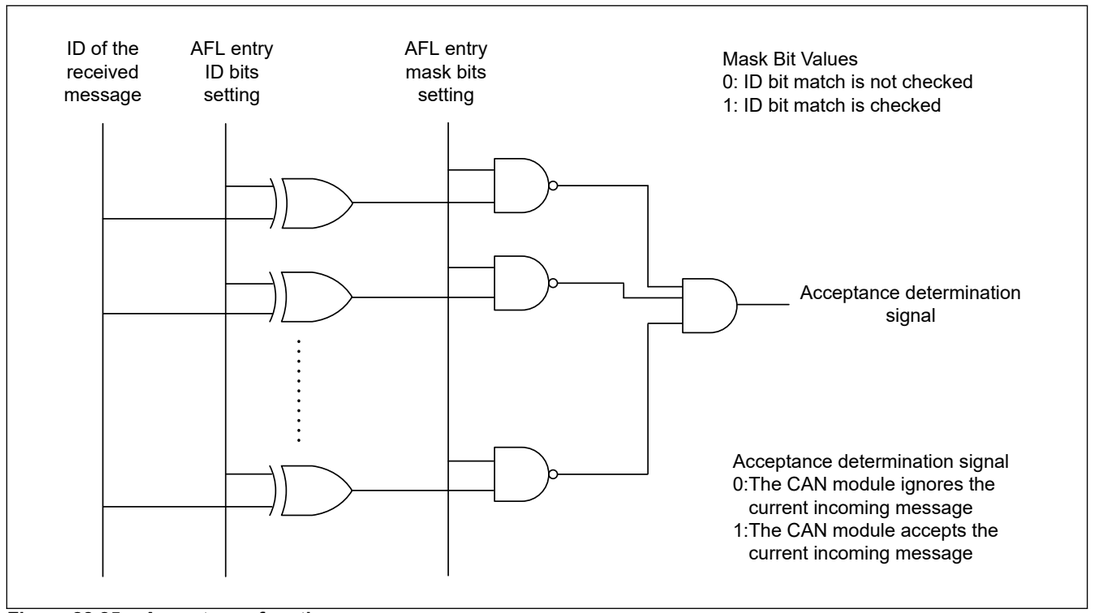


Figure 28.25 Acceptance function

28.5.4 Entering Entries in the AFL

Application software can enter one full entry into the AFL using the following registers:

- Global AFL ID Entry Register: Part 1 of the AFL entry
- Global AFL Mask Entry Register: Part 2 of the AFL entry
- Global AFL Pointer 0 Entry Register: Part 3 of the AFL entry
- Global AFL Pointer 1 Entry Register: Part 4 of the AFL entry.

16 sets of these registers form a group of AFL entries. Each group can be accessed through a page mechanism. For the CANFD module, 32 of these pages exist to allow access to the whole AFL range. The AFL should only be configured in CH_RESET or CH_HALT mode. Pages are linked to the AFL entries in the following way:

Page 0	Entry 0 — 15
Page 1	Entry 16 — 31

The selection of the AFL access page is done using the Global Acceptance Filter List Entry Control Register (CFDGAFLECTR) (Figure 28.26). This register has the following fields:

- 1 bit to select the AFL page number
- 1 bit to enable or disable the AFL data access to prevent unwanted write access to the AFL.

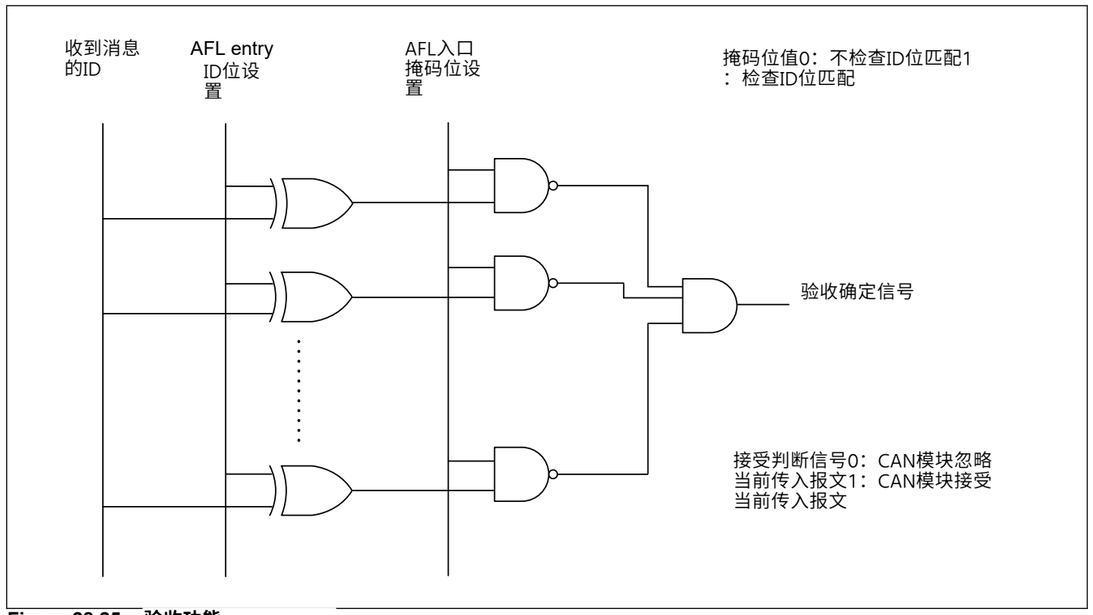


Figure 28.25 验收功能

28.5.4 在AFL中输入条目

应用软件可以使用以下寄存器将一个完整条目输入AFL：

- 全球AFLID条目寄存器：AFL条目的第1部分
- 全局AFL掩码条目寄存器：AFL条目的第2部分
- 全局AFL指针0条目寄存器：AFL条目的第3部分
- 全局AFL指针1条目寄存器：AFL条目的第4部分。

16组这些寄存器形成一组AFL条目。每个组都可以通过页面机制访问。对于CANFD模块，存在32个这样的页面以允许访问整个AFL范围。AFL只能在
CH_RESET或CH_HALT模式。页面通过以下方式链接到AFL条目：

Page 0	Entry 0 — 15
Page 1	Entry 16 — 31

AFL访问页面的选择是使用全局接受过滤器列表条目控制寄存器(CFDGAFLECTR)完成的（图28.26）。该寄存器具有以下字段：

- 1位选择AFL页码
- 1位启用或禁用AFL数据访问，以防止对AFL的不必要的写访问。

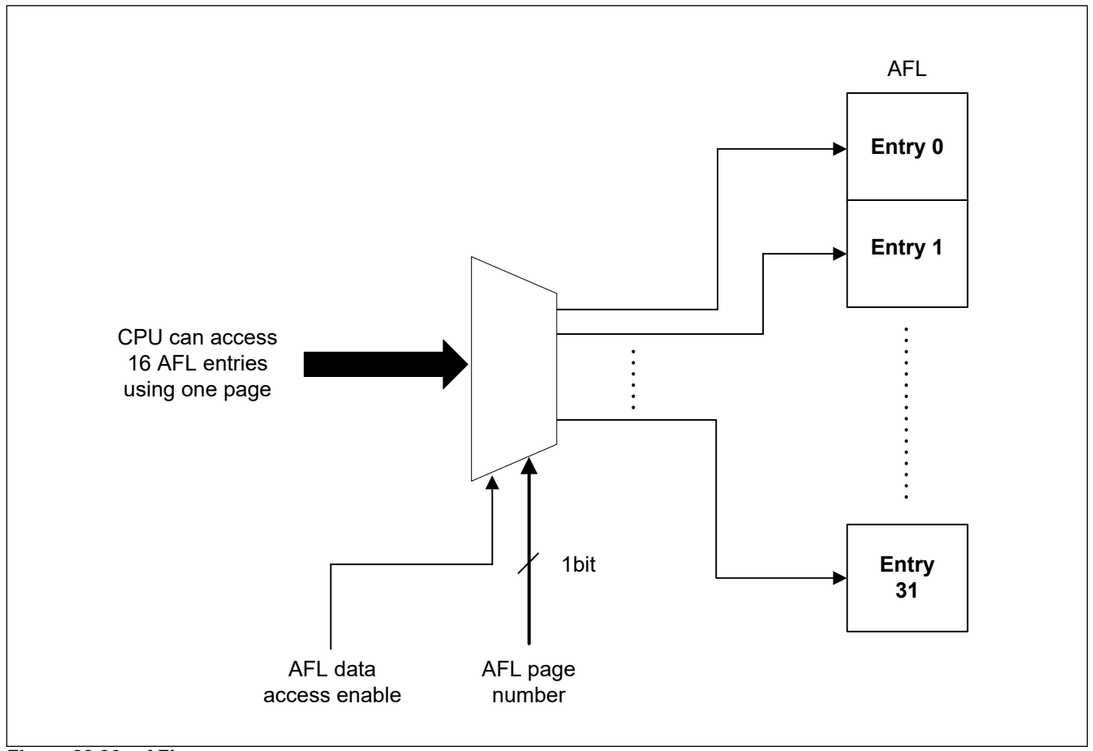


Figure 28.26 AFL page access

Application software should not write numbers higher than 0x1 for the AFL page number.

Follow the configuration shown in Figure 28.27 to program the AFL.

After entering all entries in Configuration mode, locking of the AFL access should be performed to protect unwanted write access to the AFL.

Write protection is active during all Global modes (GL_RESET, GL_HALT, and GL_OPERATION) if the lock bit is set.

Read access to AFL is still possible during all Global modes even when AFL data access is disabled (consistency check of AFL contents is possible during run time).

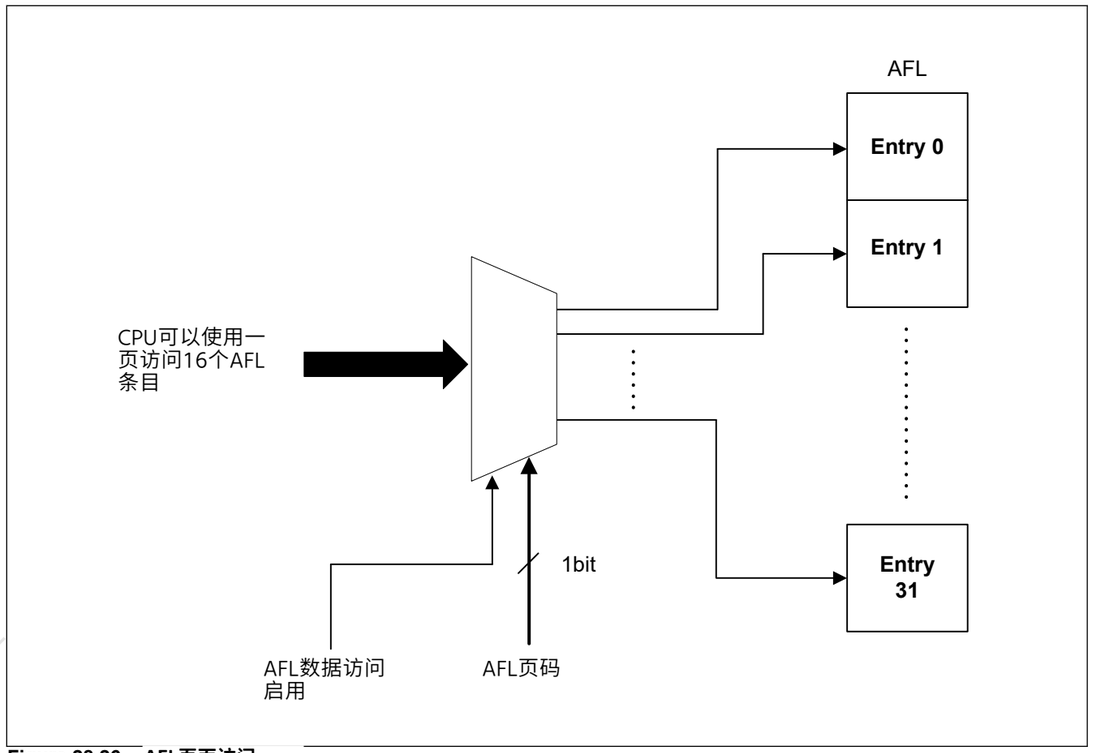


Figure 28.26 AFL页面访问

应用软件不应为AFL页号写入高于0x1的数字。

按照图28.27所示的配置对AFL进行编程。

在配置模式下输入所有条目后，应执行AFL访问锁定以保护对AFL的不需要的写访问。

如果设置了锁定位，则写保护在所有全局模式（GL_RESET、GL_HALT和GL_OPERATION）期间都处于活动状态。

即使禁用AFL数据访问（一致性检查
AFL内容在运行时是可能的）。

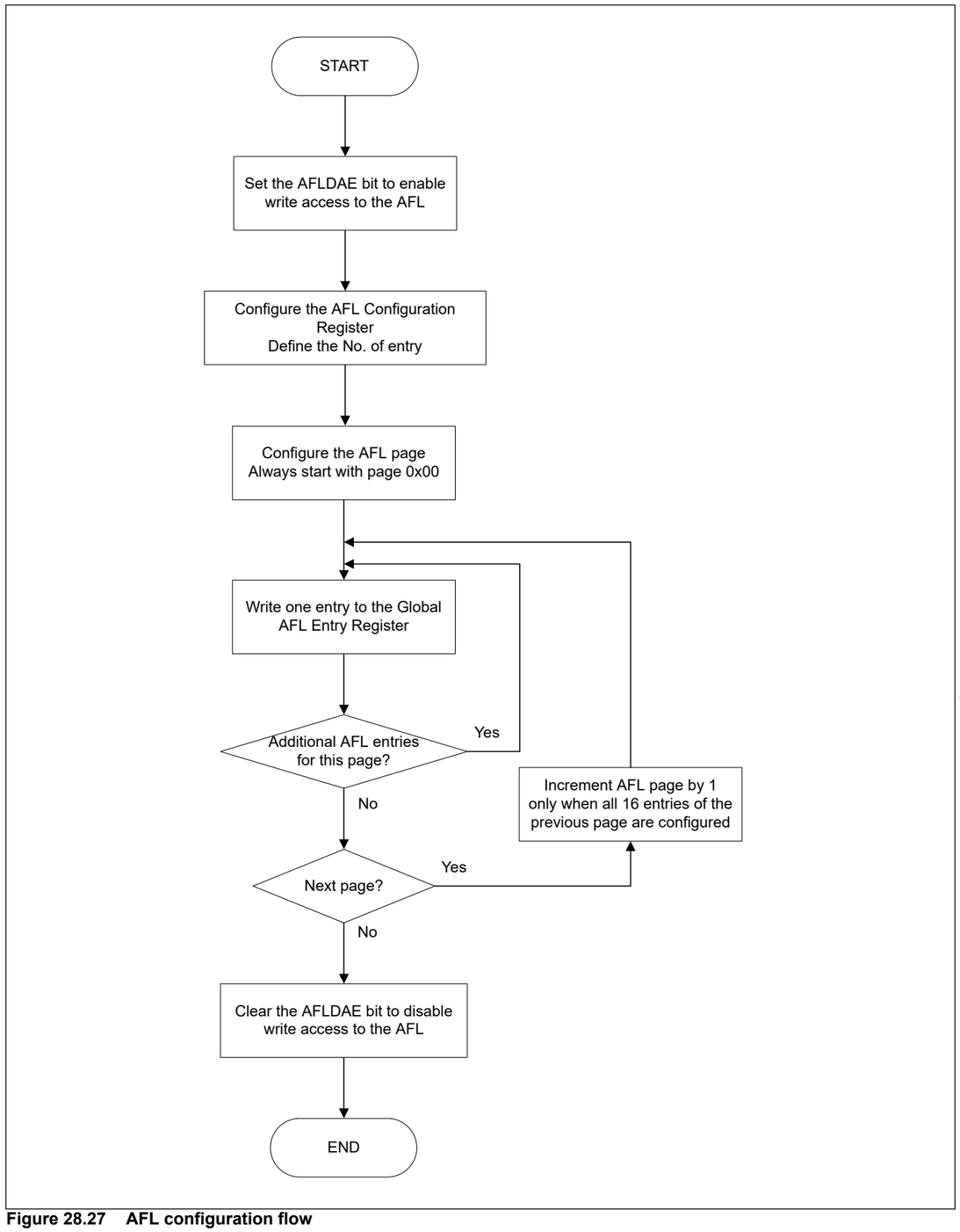


Figure 28.27 AFL configuration flow

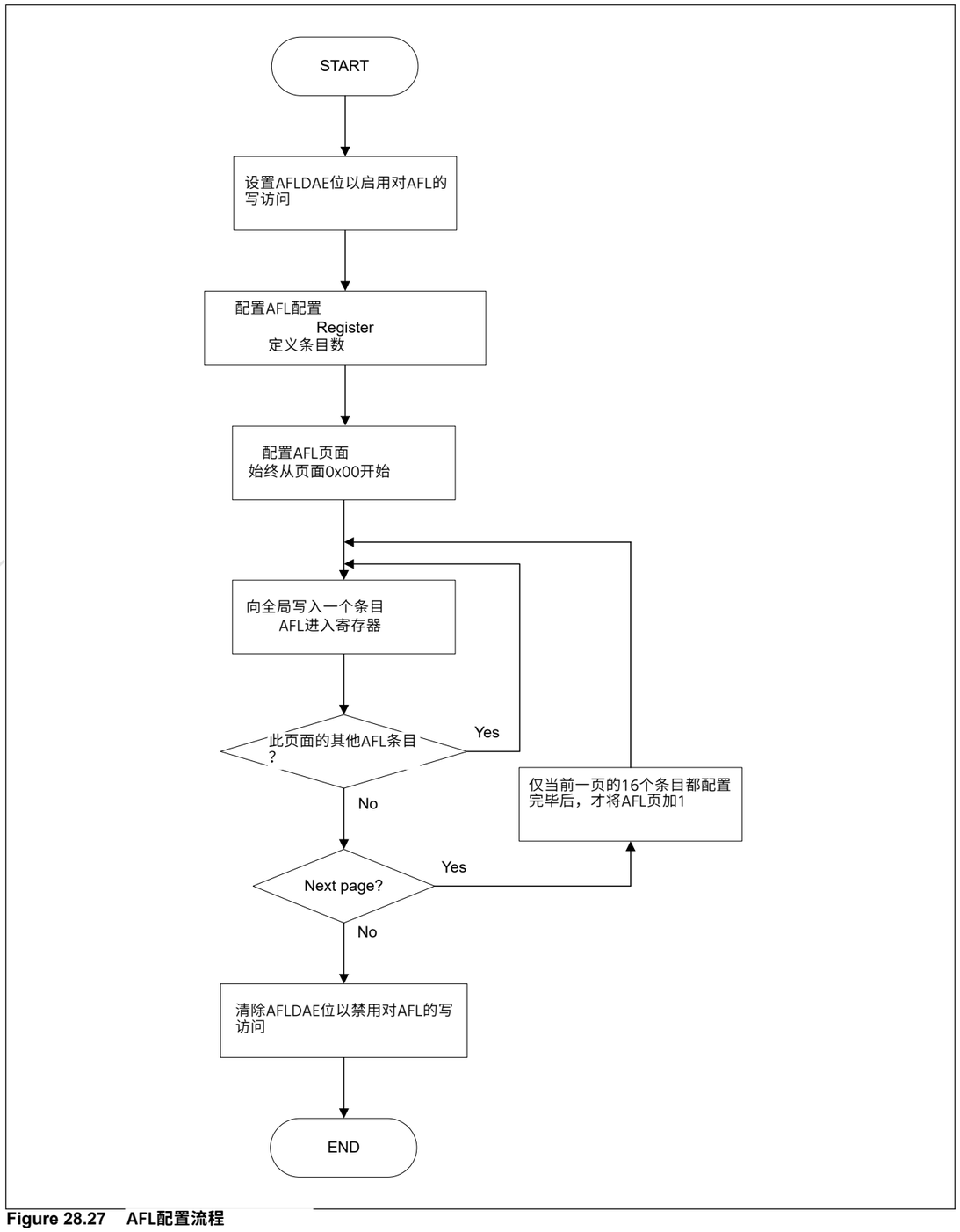


Figure 28.27 AFL配置流程

28.5.5 Loopback Modes

If the Loopback Configuration bit is set, the AFL entry is only valid in Loopback test mode (Self-test mode 0 or Self-test mode 1) or in mirror mode when receiving messages that were transmitted by the respective CAN channel itself.

The AFL entry is not valid for received messages in loopback mode transmitted by other CAN nodes on the bus. The expression valid or invalid for the related entry means that this AFL entry is or is not compared against the received message ID respectively.

If the Loopback Configuration bit is 0, the AFL entry is only valid for:

- Received messages transmitted by other CAN nodes on the bus in normal (non-loopback mode) and mirror modes
- Received messages transmitted by other CAN nodes or the CAN channel itself in Loopback test mode.

The mirror mode can be enabled with the CFDGCFG.MME bit in the Global Configuration Register. If CFDGCFG.MME bit is set, then a successfully transmitted message can be stored back in an RX message buffer or FIFO buffer if a matching entry is configured in the AFL for that channel.

The Loopback Configuration bit in the matching AFL entry must be set to store this frame.

If Mirror mode and Loopback test mode are configured at the same time, the Loopback test mode behavior applies.

Table 28.23 shows the behavior of the acceptance filter unit depending on the setting of the related input signals.

Table 28.23 Behavior of acceptance filter based on the loopback configuration setting in AFL entry

Mirror Mode Enable (MME Configuration bit)	Loopback in test mode (Self-test mode 0 or Self-test mode 1)	Channel mode	Loopback Configuration bit in AFL entry	AFL entry
0	0	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Invalid
			1	Invalid
	1	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Valid
			1	Valid
1	0	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Invalid
			1	Valid
	1	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Valid
			1	Valid

Note: The expression valid or invalid for the related entry means that this AFL entry is or is not compared against the received message ID, respectively.

28.5.6 IDE Masking

When the GAFLIDEM bit is 0 in an AFL entry, the IDE bit configured in the AFL entry is not used for ID matching. In this case, the use of ID[10:0] or ID[28:0] matching is based on the received IDE bit.

Consider the following example:

- The ID and Mask fields of an AFL entry x is configured as follows:
  - CFDGAFLID [x] = 0xC0553A20 → IDE = 1, RTR = 1, LLB = 0, ID[10:0] = 0x220 / ID[28:0] = 0x00553A20
  - CFDGAFLMr = 0x0000FFFF → IDEM = 0. RTRM = 0, IDM[10:0] = 0x7FF / IDM[28:0] = 0x0000FFFF

28.5.5 Loopback Modes

如果设置了环回配置位，则AFL条目仅在环回测试模式（自测模式0或自测模式1）或在接收由相应CAN通道本身发送的消息时的镜像模式下有效。

AFL条目对于总线上其他CAN节点发送的环回模式下接收到的消息无效。相关条目的表达式有效或无效表示该AFL条目分别与接收到的消息ID进行比较或不进行比较。

如果环回配置位为0，则AFL条目仅对以下情况有效：

- 接收到总线上其他CAN节点在正常（非环回模式）和镜像模式下发送的报文
- Loopback测试模式下接收到其他CAN节点或CAN通道本身发送的报文。

可以使用全局配置寄存器中的CFDGCFG.MME位启用镜像模式。如果设置了CFDGCFG.MME位，则如果在AFL中为该通道配置了匹配条目，则成功传输的消息可以存储回RX消息缓冲区或FIFO缓冲区。

必须设置匹配AFL条目中的环回配置位以存储该帧。

如果同时配置了镜像模式和环回测试模式，则应用环回测试模式行为。

表28.23显示了接收滤波器单元的行为，具体取决于相关输入信号的设置。

Table 28.23 基于AFL条目中环回配置设置的验收过滤器的行为

镜像模式启用（MME配置位）	测试模式环回（自检模式0或自检模式1）	频道模式	AFL条目中的环回配置位	AFL entry
0	0	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Invalid
			1	Invalid
	1	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Valid
			1	Valid
1	0	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Invalid
			1	Valid
	1	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Valid
			1	Valid

Note: 相关条目的表达式有效或无效表示此AFL条目是否与接收到的消息进行比较身份证，分别。

28.5.6 IDE屏蔽

当AFL条目中的GAFLIDEM位为0时，AFL条目中配置的IDE位不用于ID匹配。在这种情况下，ID[10:0]或ID[28:0]匹配的使用基于接收到的IDE位。

考虑以下示例：

- AFL表项x的ID和Mask字段配置如下：
  - CFDGAFLID [x] = 0xC0553A20 → IDE = 1, RTR = 1, LLB = 0, ID[10:0] = 0x220 / ID[28:0] = 0x00553A20
  - CFDGAFLMr = 0x0000FFFF → IDEM = 0. RTRM = 0, IDM[10:0] = 0x7FF / IDM[28:0] = 0x0000FFFF

- The comparison result for the four different received IDs with AFL entry x is described as follows:
  - If a frame with IDE = 0 and ID = 0x220 is received, this is considered as a match
  - If a frame with IDE = 0 and ID = 0x320 is received, this is not a match
  - If a frame with IDE = 1 and ID = 0x1FFF3A20 is received, this is considered as a match
  - If a frame with IDE = 1 and ID = 0x08803220 is received, this is not a match.

28.5.7 Updating AFL Entry during Communication

You can update the AFL entry without disabling all CAN communications. Choose the entry number to be updated by setting the AFL entry number, and ignore the enable bit.

This entry number is ignored from the AFL matching while the entry is being updated.

Figure 28.28 shows the update flow for an AFL entry.

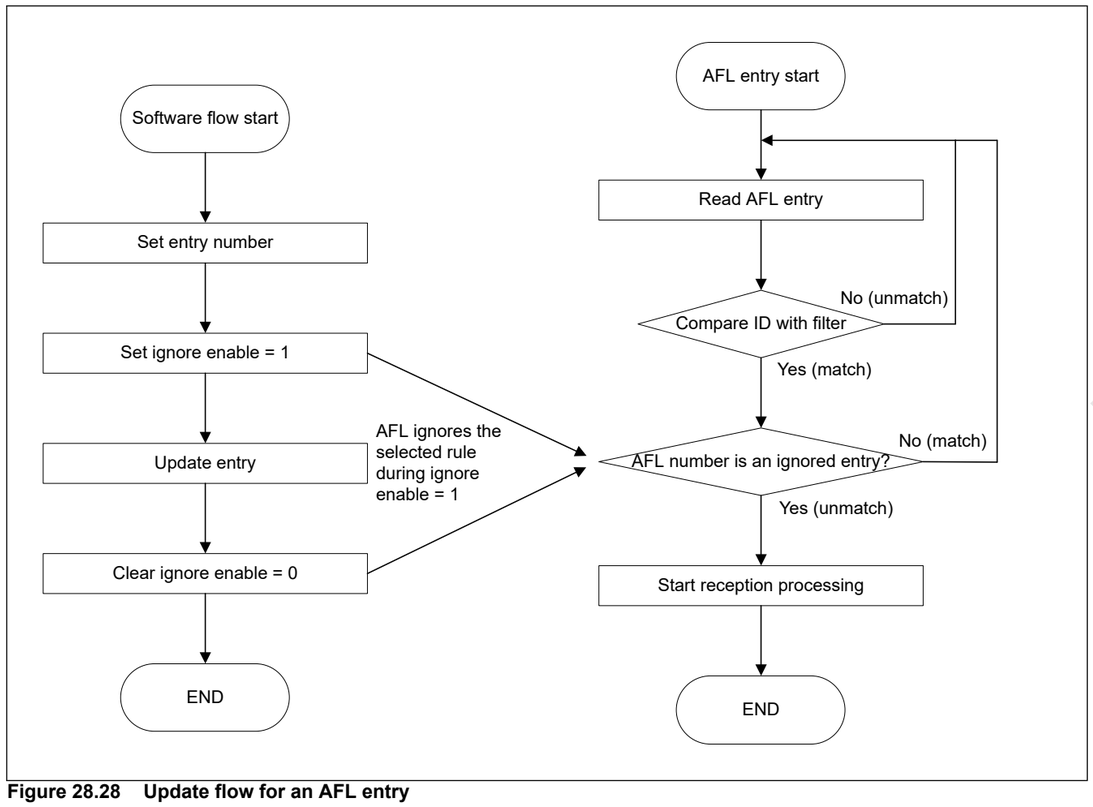


Figure 28.28 Update flow for an AFL entry

The method to update an AFL entry is as follows:

1. Set the entry number to CFDGAFLIGNENT register.
2. Set the value 0xC401 (key code and enable bit) to CFDGAFLIGNCTR register.
3. Set the entry page to CFDGAFLECTR register. This page includes the selected entry. CFDGAFLECTR.AFLDAE is set to 1.
4. Set the new rule to CFDGAFLIDr, CFDGAFLMr, CFDGAFLP0r, CFDGAFLP1r registers.
5. CFDGAFLECTR.AFLDAE is cleared to 0.
6. Set the value 0xC400 (key code and clear enable bit) to CFDGAFLIGNCTR register.

●四种不同的接收ID与AFL条目x的比较结果描述如下：

如果接收到IDE=0且ID=0x220的帧，则视为匹配

如果接收到IDE=0且ID=0x320的帧，则不匹配

如果接收到IDE=1且ID=0x1FFF3A20的帧，则视为匹配

如果接收到IDE=1且ID=0x08803220的帧，则不匹配。

28.5.7 在通信期间更新AFL条目

您可以在不禁用所有CAN通信的情况下更新AFL条目。通过设置AFL条目号来选择要更新的条目号，忽略使能位。

在更新条目时，此条目号会从AFL匹配中忽略。

图28.28显示了AFL条目的更新流程。

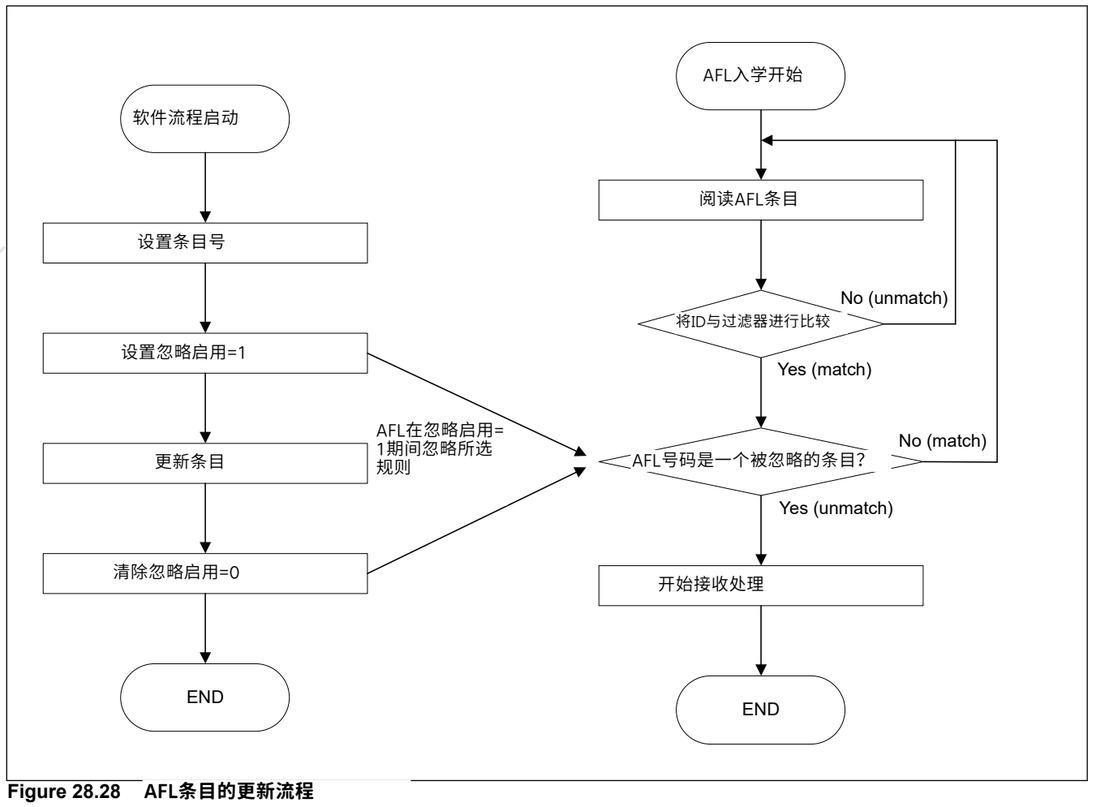


Figure 28.28 AFL条目的更新流程

更新AFL条目的方法如下：

1.将条目号设置为CFDGAFLIGNENT寄存器。

2.将值0xC401（键码和使能位）设置到CFDGAFLIGNCTR寄存器。

3.将入口页面设置为CFDGAFLECTR寄存器。此页面包括所选条目。CFDGAFLECTR.AFLDAE设置为1。

4.为CFDGAFLIDr、CFDGAFLMr、CFDGAFLP0r、CFDGAFLP1r寄存器设置新规则。

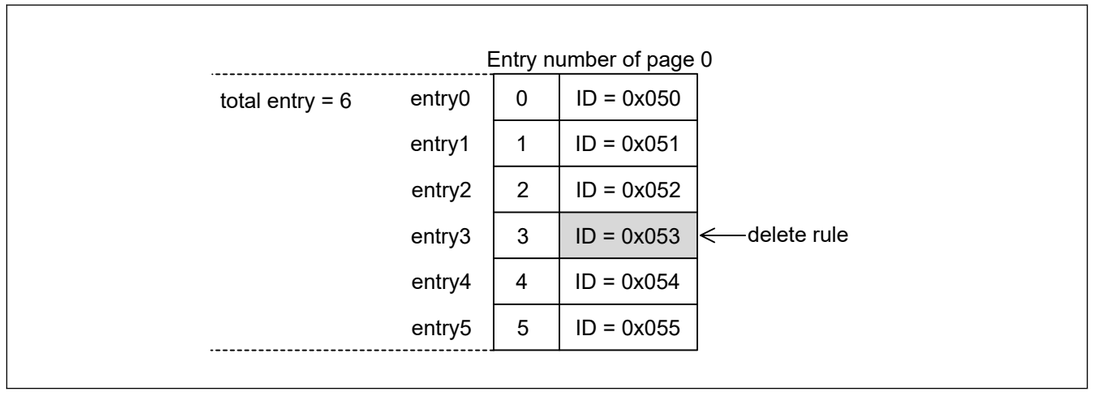
5.CFDGAFLECTR.AFLDAE清零。

6.将值0xC400（键码和清除使能位）设置到CFDGAFLIGNCTR寄存器。

Note: This entry number is ignored during the periods from (2) to (5).

(1) Example 1: Deleting an entry

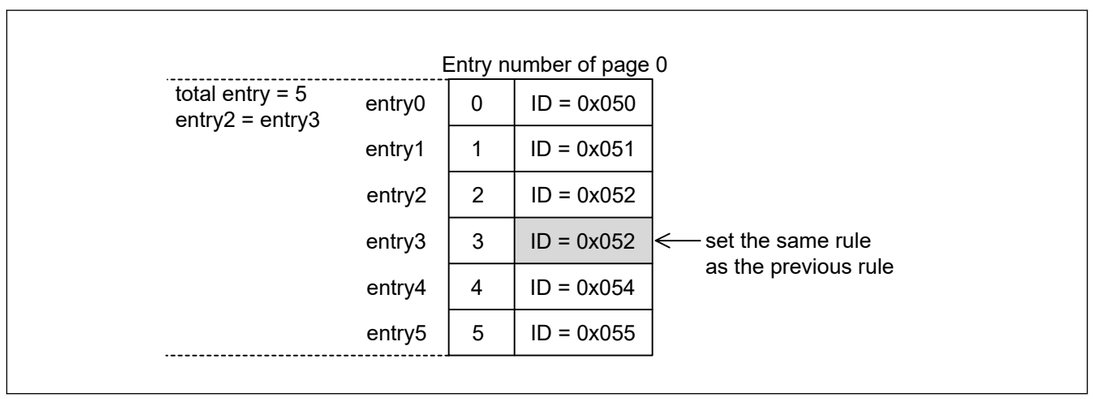
Deleting entry3 when the total number of entries is 6 channel.



How to delete an entry

1. Set 0x00000003 to CFDGAFLIGNENT register.
2. Set 0x0000C401 to CFDGAFLIGNCTR register.
3. Set 0x00000100 to CFDGAFLECTR register.
4. Set the same rule as the previous rule by accessing CFDGAFLIDr, CFDGAFLMr, CFDGAFLP0r, CFDGAFLP1r (r = 3, this is entry3).
5. Set 0x00000000 to CFDGAFLECTR register.
6. Set 0x0000C400 to CFDGAFLIGNCTR register.

Entry3 is now deleted.



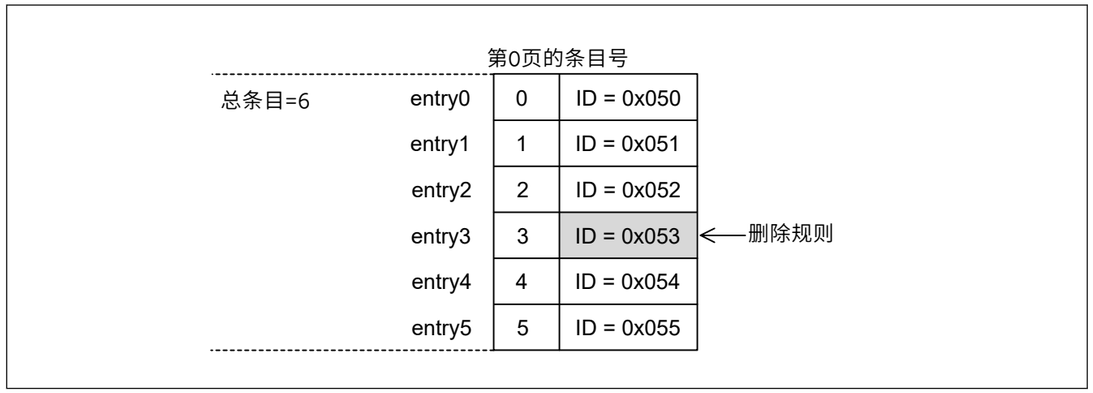
(2) Example 2: Adding an entry

Adding a new entry to entry3 when the total number of entries is 6.

Note: 在从(2)到(5)的期间，该条目号被忽略。

(1) 示例1：删除条目

当条目总数为6个通道时，删除条目3。



如何删除条目

1.将0x00000003设置为CFDGAFLIGNENT寄存器。

2.将0x0000C401设置为CFDGAFLIGNCTR寄存器。

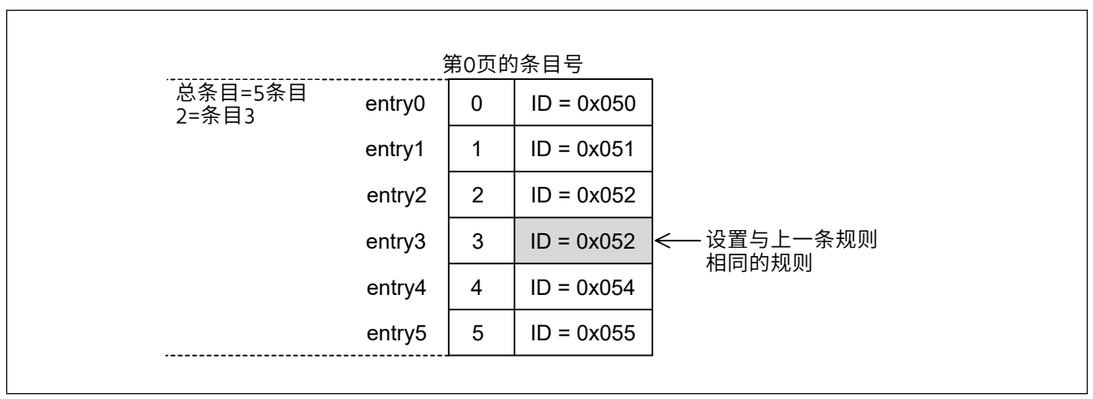
3.将0x00000100设置为CFDGAFLECTR寄存器。

4.通过访问CFDGAFLIDr、CFDGAFLMr、CFDGAFLP0r、CFDGAFLP1r（r=3，这是entry3）设置与上一个规则相同的规则。

5.将0x00000000设置为CFDGAFLECTR寄存器。

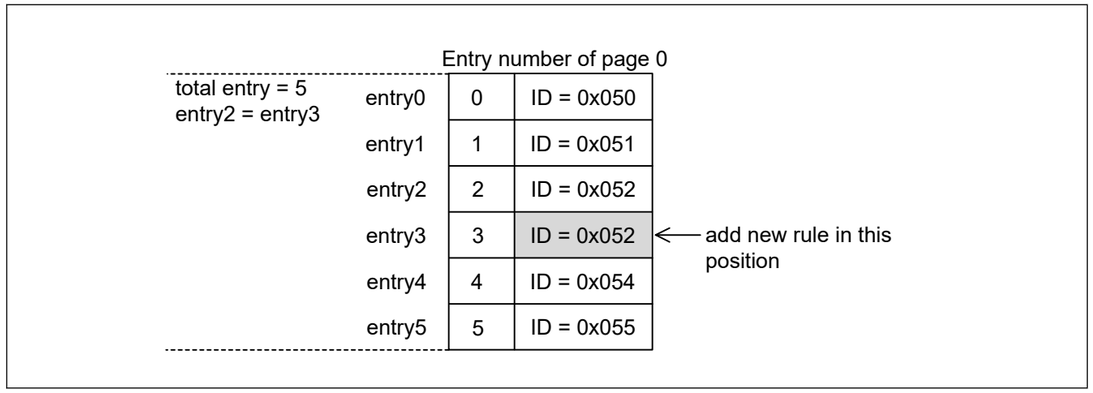
6.将0x0000C400设置为CFDGAFLIGNCTR寄存器。

现在已删除条目3。



(2) 示例2：添加条目

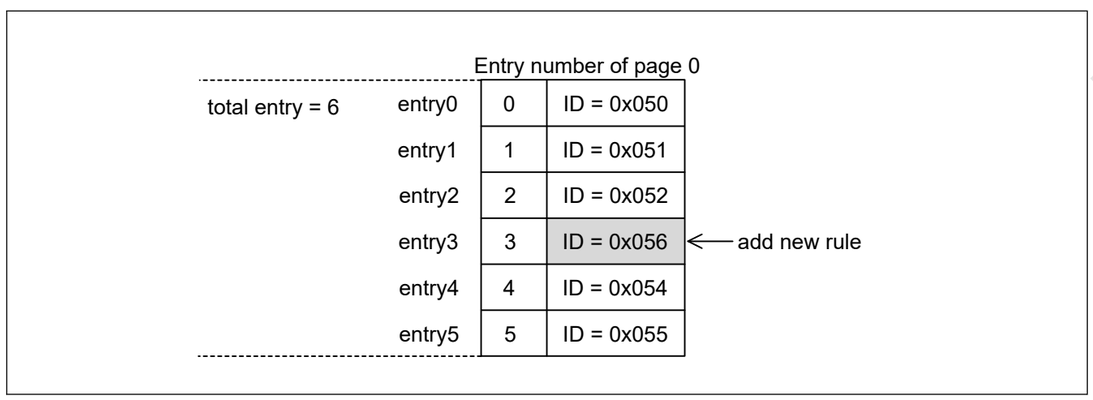
当条目总数为6时，向entry3添加一个新条目。



How to add an entry

1. Set 0x00000003 to CFDGAFLIGNENT register.
2. Set 0x0000C401 to CFDGAFLIGNCTR register.
3. Set 0x00000100 to CFDGAFLECTR register.
4. Set the new rule by accessing CFDGAFLIDr, CFDGAFLMr, CFDGAFLP0r, CFDGAFLP1r (r = 3, this is entry3).
5. Set 0x00000000 to CFDGAFLECTR register.
6. Set 0x0000C400 to CFDGAFLIGNCTR register.

The new entry is now added.



The AFL filter can be used to set CFDGAFLCFG, and addition/deletion of an entry is possible. Therefore, it is necessary to set the maximum number to be used to CFDGAFLCFG.

28.6 FIFO Buffers and Normal Message Buffer Configuration

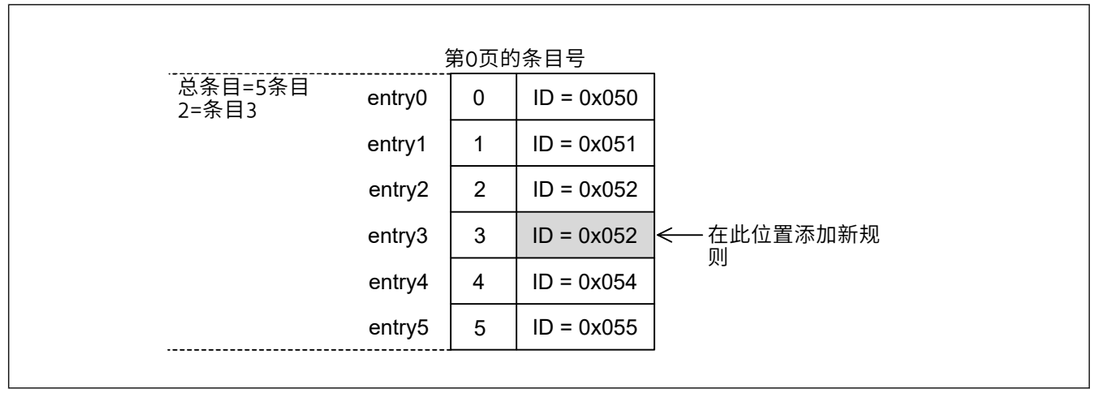
This section describes the process for configuring the number of RX message buffers, the FIFO buffers, and the flat TX message buffers in the CANFD module. The message buffers are mapped as shown in Figure 28.29.

The RX message buffers can be accessed with the RX Message Buffer Registers.

The RX FIFO buffers and the common FIFO buffers configured in RX mode or TX mode can only be accessed with the FIFO Access Registers.

If the common FIFO is configured in TX mode, you can only write data into the FIFO buffer using the FIFO Access registers.

If the common FIFO is configured in RX mode, you can only read data from the FIFO Access Registers.



如何添加条目

1.将0x00000003设置为CFDGAFLIGNENT寄存器。

2.将0x0000C401设置为CFDGAFLIGNCTR寄存器。

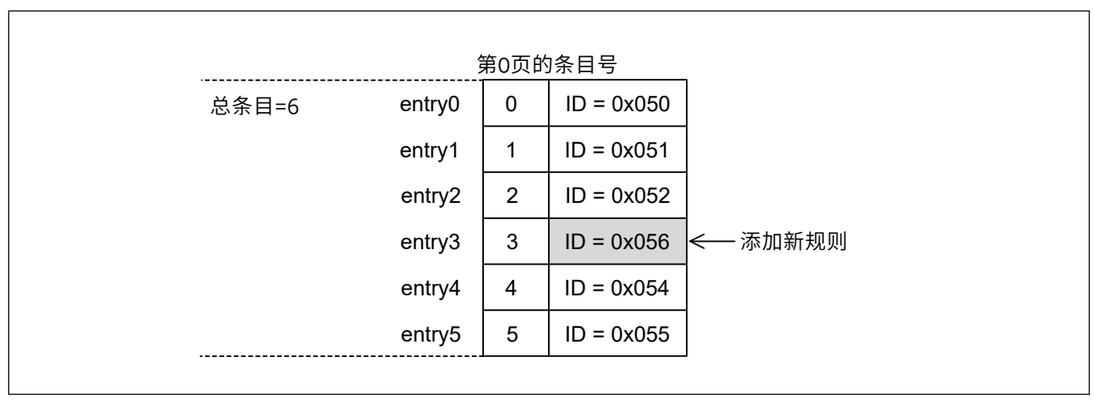
3.将0x00000100设置为CFDGAFLECTR寄存器。

4.通过访问CFDGAFLIDr、CFDGAFLMr、CFDGAFLP0r、CFDGAFLP1r设置新规则（r=3，这是entry3）。

5.将0x00000000设置为CFDGAFLECTR寄存器。

6.将0x0000C400设置为CFDGAFLIGNCTR寄存器。

现在添加了新条目。



AFL过滤器可用于设置CFDGAFLCFG，并且可以添加删除条目。因此，有必要将要使用的最大数量设置为CFDGAF cessary to LCFG。

28.6 FIFO缓冲区和正常消息缓冲区配置

本节介绍在CANFD模块中配置RX报文缓冲区、FIFO缓冲区和平面TX报文缓冲区数量的过程。消息缓冲区的映射如图28.29所示。

RX报文缓冲区可以通过RX报文缓冲区寄存器访问。

RXFIFO缓冲区和配置为RX模式或TX模式的通用FIFO缓冲区只能通过FIFO访问寄存器。

如果普通FIFO配置为TX模式，则只能使用FIFO访问寄存器将数据写入FIFO缓冲区。

如果普通FIFO配置为RX模式，则只能从FIFO访问寄存器中读取数据。

The TX message buffers can be accessed with the TX Message Buffer Registers.

If unused message buffer locations are read, the message buffer locations are read as unknown values.

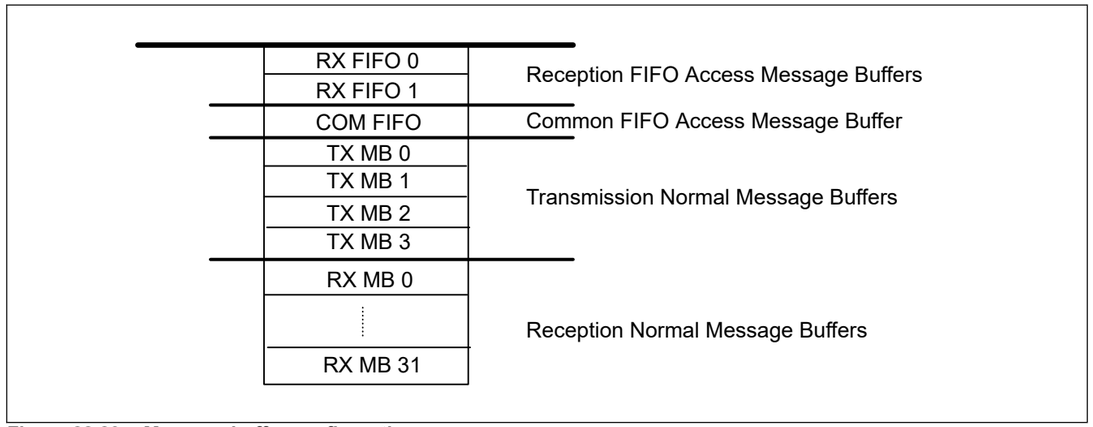


Figure 28.29 Message buffer configuration

28.6.1 Normal RX Message Buffers

In CANFD module, the frames received can be stored in normal RX message buffers based on the configuration of the AFL entries.

Additionally, the number of normal RX message buffers required in the system can be chosen up to a fixed maximum limit.

28.6.1.1 Normal RX Message Buffer Configuration

In CANFD module, the number of normal RX message buffers can be configured by writing to the RX Message Buffer Number Register.

The limiting values for the configuration of number of message buffers are:

- Minimum value = 0x00 (no normal RX MB)
- Maximum value = 0x20

Do not use values outside these limits.

The AFL entries for routing the received messages to normal RX message buffers must be configured to match the requirements of the system.

The AFL entries must also be configured properly, and an AFL entry for normal RX message buffers should not exceed the number of message buffers configured in the RX Message Buffer Number Register.

Note: There is no internal check procedure provided in CANFD module against wrong configuration of the AFL.

The data field size of the RX message buffer can be configured with the CFDRMNB.RMPLS bit. The default size is 8 bytes and the maximum data payload size is 64 bytes.

When the receiving frame exceeds the data field size, then the acceptance depends on the configuration of CFDGCFG.CMPOC (message rejecting or data payload cut).

Note: RMPLS and CMPOC bit is not available in the classical CAN function, so, these feature is not valid for classical CAN.

28.6.2 FIFO Buffers

The CANFD module provides a fixed number of FIFO buffers to support storage of frames for reception and transmission functions .

TX报文缓冲区可以通过TX报文缓冲区寄存器访问。

如果读取未使用的消息缓冲区位置，则将消息缓冲区位置作为未知值读取。

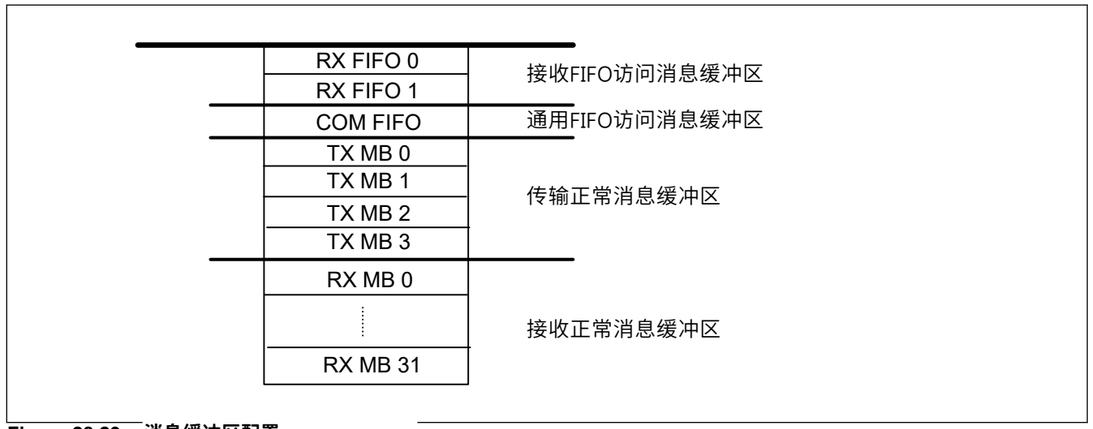


Figure 28.29 消息缓冲区配置

28.6.1 正常RX消息缓冲区

在CANFD模块中，接收到的帧可以根据AFL条目的配置存储在正常的RX消息缓冲区中。

此外，系统所需的正常RX消息缓冲区的数量可以选择为固定的最大限制。

28.6.1.1 正常RX报文缓冲区配置

在CANFD模块中，可以通过写入RX消息缓冲区来配置正常RX消息缓冲区的数量
号码寄存器。

消息缓冲区数量配置的限制值为：

- 最小值=0x00（非正常RXMB）
- 最大值=0x20

不要使用超出这些限制的值。

用于将接收到的消息路由到正常RX消息缓冲区的AFL条目必须配置为匹配系统的要求。

AFL条目也必须正确配置，正常RX消息缓冲区的AFL条目不应超过RX消息缓冲区编号寄存器中配置的消息缓冲区数。

Note: CANFD模块中没有针对AFL的错误配置提供内部检查程序。

RX消息缓冲区的数据字段大小可以通过CFDRMNB.RMPLS位进行配置。默认大小为8字节，最大数据负载大小为64字节。

当接收帧超过数据字段大小时，则接受取决于配置
CFDGCFG.CMPOC（消息拒绝或数据有效负载切断）。

Note: RMPLS和CMPOC位在经典CAN功能中不可用，因此，这些功能对经典CAN功能无效
CAN.

28.6.2 FIFO Buffers

CANFD模块提供固定数量的FIFO缓冲区，以支持存储接收和发送功能的帧。

The number of reception-only FIFO buffers is fixed to 2. However, common FIFO buffer channel can be configured to store messages for transmission or reception function.

These FIFO buffers can be enabled or disabled, and the following parameters can be configured to match the system requirements:

- Size
- Interrupt structure
- Message lost mechanism
- Message overwrite mechanism of the FIFO buffers
- Location of the TX FIFO.

When the receiving frame exceeds the data field size, the acceptance depends on the configuration of the CFDGCFG.CMPOC bit (message rejecting or data payload cut).

28.6.2.1 FIFO Buffers Configuration

In CANFD module, the FIFO buffers can be configured to match the system requirements.

The total number of FIFO buffers = 2 RX FIFO buffers + 1 common FIFO buffer = 3 FIFO buffers.

仅接收FIFO缓冲区的数量固定为2。但是，可以配置通用FIFO缓冲区通道来存储用于发送或接收功能的消息。

可以启用或禁用这些FIFO缓冲区，并且可以配置以下参数以匹配系统要求：

- Size
- ●中断结构
- ●消息丢失机制
- ●FIFO缓冲区的消息覆盖机制
- ●TXFIFO的位置 。

当接收帧超过数据字段大小时，接受取决于配置的
CFDGCFG.CMPOC位（消息拒绝或数据有效负载切断）。

28.6.2.1 FIFO缓冲器配置

在CANFD模块中，可以配置FIFO缓冲区以匹配系统要求。

FIFO缓冲区的总数=2个RXFIFO缓冲区+1个通用FIFO缓冲区=3个FIFO缓冲区。

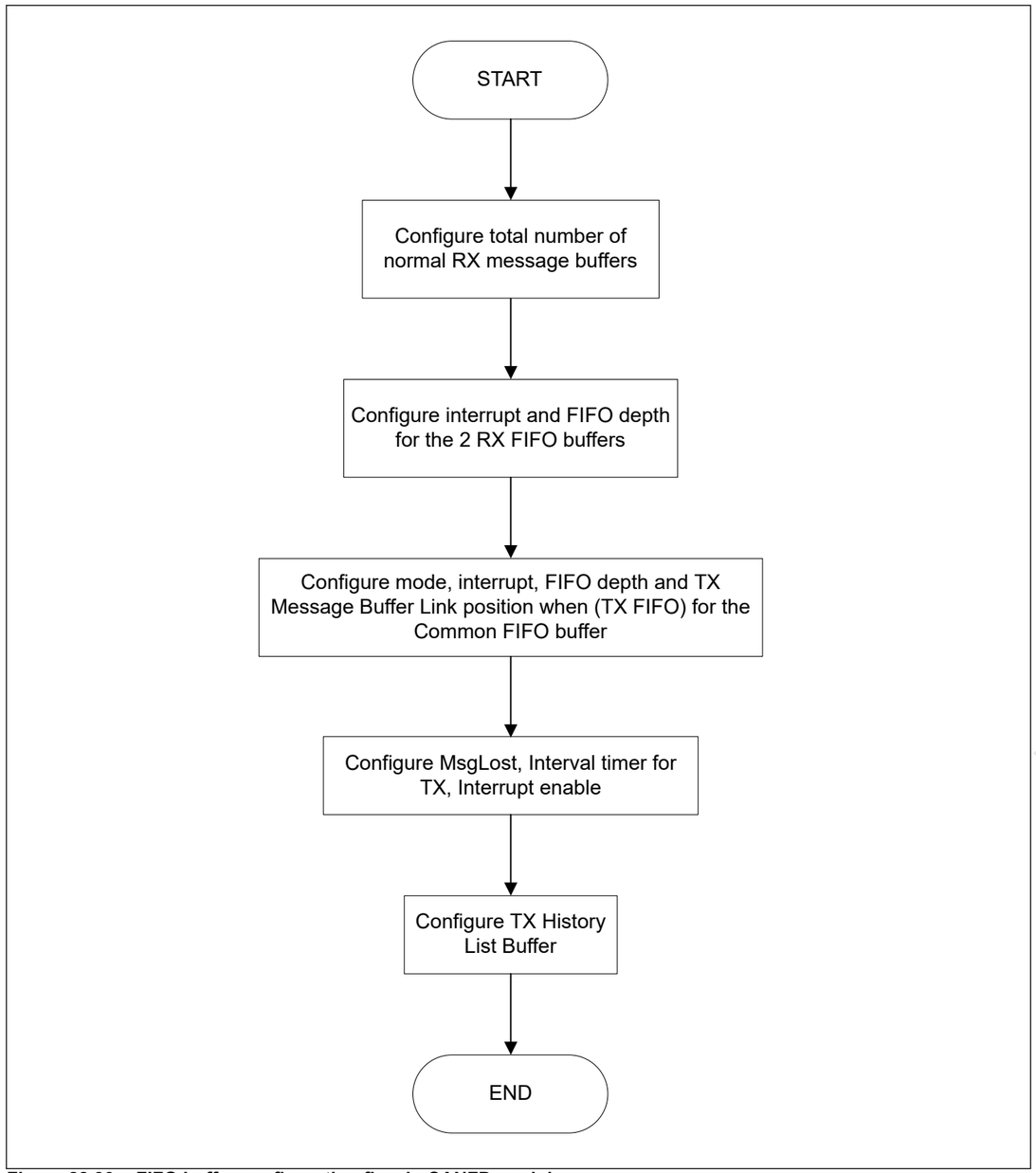


Figure 28.30 FIFO buffer configuration flow in CANFD module

As shown in Figure 28.30, the various FIFO buffers can be configured by writing to the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers.

For the 2 RX FIFO buffers, the following parameters can be configured:

- Interrupts
- FIFO depth
- FIFO payload data size.

For the common FIFO buffer, the following parameters can be configured:

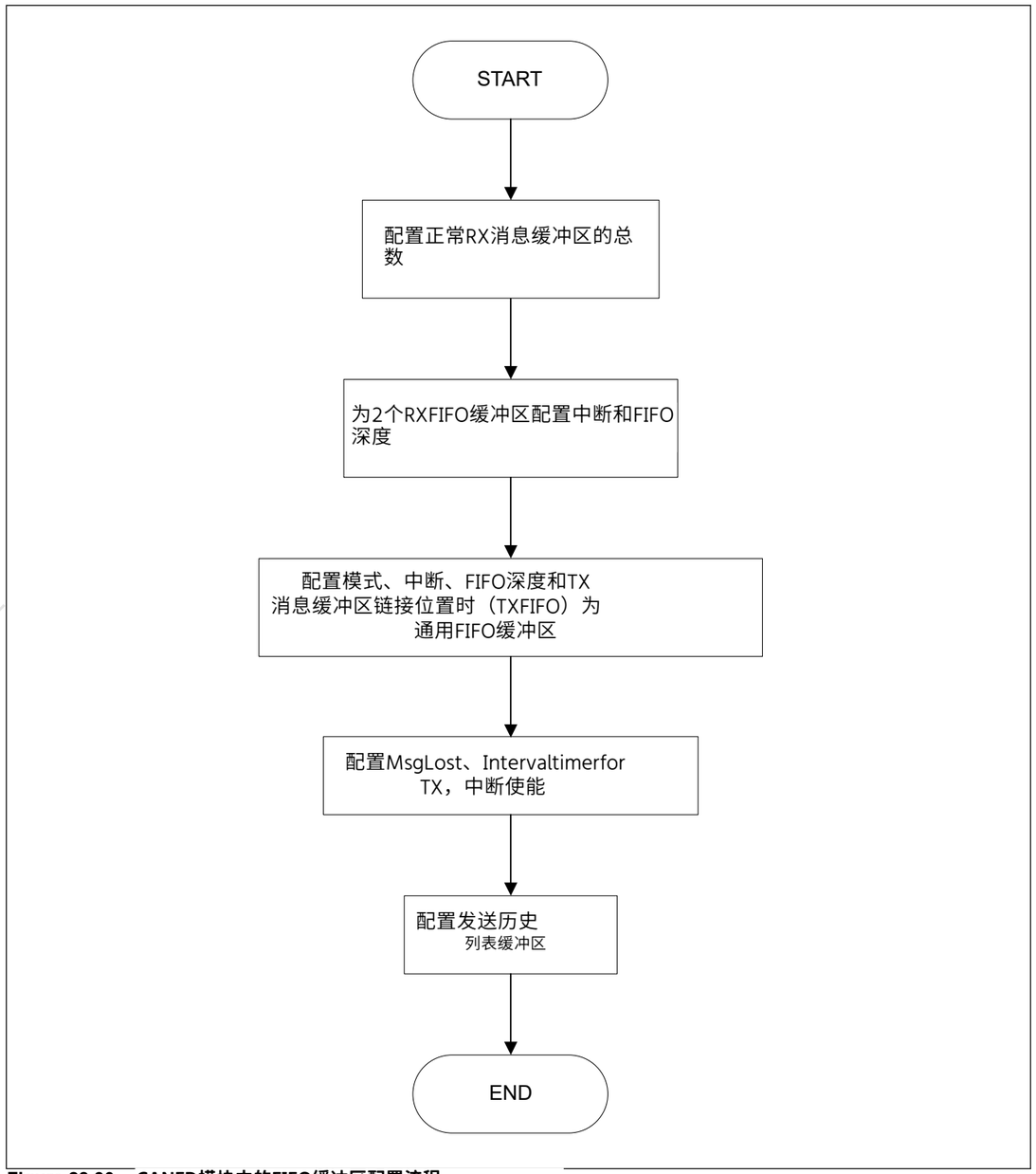


Figure 28.30 CANFD模块中的FIFO缓冲区配置流程

如图28.30所示，可以通过写入RXFIFOConfigurationControl来配置各种FIFO缓冲区寄存器和通用FIFO配置控制寄存器。

对于2个RXFIFO缓冲区，可以配置以下参数：

- Interrupts
- FIFO depth
- FIFO有效负载数据大小。

对于普通的FIFO缓冲区，可以配置以下参数：

- Mode
- Interrupts FIFO depth
- FIFO payload data size
- FIFO TX link position.

(1) FIFO mode configuration of Common FIFO buffer

The mode of the common FIFO buffer can be configured by writing to the CFDCFCC.CFM[1:0] bits in the Common FIFO Configuration/Control Register. The possible modes of configuration for Common FIFO buffer are:

- 0b RX mode (default mode after hardware reset)
- 1b TX mode

Messages can only be read from the RX FIFO buffers and the Common FIFO buffer configured in RX mode. Messages are stored by the CAN module in these FIFO buffers based on the AFL entries.

Messages can be read and written into the Common FIFO buffer configured in TX mode. These messages are transmitted on the appropriate CAN channel.

The pointers can only be incremented when a new message is stored in the FIFO buffer and decremented when a message is transmitted on the corresponding CAN channel by the CANFD module.

After a hardware reset, the Common FIFO buffer is configured in RX mode by default. Only enable the FIFO buffers after configuring the Common FIFO buffer in the required modes.

(2) FIFO TX message buffer link configuration

When the common FIFO is configured as TX FIFO, the FIFO buffer must be linked to a normal TX message buffer to participate in the transmission scan.

Do not write data into a TX message buffer that is linked to a Common FIFO buffer. Also, the TX message buffer linked to a Common FIFO buffer should not be a part of the TX Queue.

The TX message buffer link of each Common FIFO buffer can be configured by writing to the CFDCFCC.CFTML[1:0] bits in the Common FIFO Configuration/Control Registers. Available options for TX message buffer link configuration are:

- 0x00: TX Message Buffer 0
- 0x01: TX Message Buffer 1
- 0x10: TX Message Buffer 2
- 0x11: TX Message Buffer 3

(3) FIFO depth configuration

The depth of each FIFO buffer can be configured by writing to the CFDRFCCa.RFDC[2:0] bits and CFDCFCC.CFDC[2:0] bits in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers. The 6 available options for depth configuration are:

- 0x000: 0 Messages (FIFO buffer cannot be enabled)
- 0x001: 4 Messages
- 0x010: 8 Messages
- 0x011: 16 Messages
- 0x100: 32 Messages
- 0x101: 48 Messages

The RAM allocation for RX message buffers along with FIFO buffers is limited to 16 messages with 64 data bytes. Configuration of the RX message buffers, along with FIFO buffers, that exceeds this maximum limit should not be done.

CANFD module logic does not check the validity of the configuration.

Note: If the FIFO depth of a common FIFO is 4 messages or more (CFDCFCC.CFDC[2:0] > 000b), then the Common FIFO TX message buffer link is valid when the FIFO is disabled or enabled.

- Mode

●中断FIFO深度

●FIFO有效负载数据大小

●FIFOTX链路位置。

(1) CommonFIFO缓冲区的FIFO模式配置

可通过写入CommonFIFO中的CFDCFCC.CFM[1:0]位来配 置commonFIFO缓冲区的模式
配置控制寄存器。CommonFIFO缓冲区的可能配置模式有：

●0bRX模式（硬件复位后的默认模式）

- 1b TX mode

只能从RXFIFO缓冲区和配置为RX模式的CommonFIFO缓冲区读取消息。CAN模块根据AFL条目将消息存储在这些FIFO缓冲区中。

可以将消息读取和写入在TX模式下配置的CommonFIFO缓冲区。这些消息在适当的CAN通道上传输。

只有当新消息存储在FIFO缓冲区中时，指针才能递增，而当CANFD模块在相应CAN通道上传输消息时，指针才能递减。

硬件复位后，CommonFIFO缓冲区默认配置为RX模式。仅在所需模式下配置CommonFIFO缓冲区后才启用FIFO缓冲区。

(2) FIFOTX消息缓冲区链接配置

当通用FIFO配置为TXFIFO时，FIFO缓冲区必须链接到正常的TX报文缓冲区才能参与传输扫描。

不要将数据写入链接到通用FIFO缓冲区的TX消息缓冲区。此外，链接到通用FIFO缓冲区的TX消息缓冲区不应成为TX队列的一部分。

每个通用FIFO缓冲区的TX报文缓冲区链接可以通过写入通用FIFO配置控制寄存器中的CFDCFCC.CFTML[1:0]位来配置。TX消息缓冲区链路配置的可用选项包括：

●0x00：TX消息缓冲区0

●0x01：TX报文缓冲区1

●0x10：TX消息缓冲区2

●0x11：TX报文缓冲区3

(3) FIFO深度配置

每个FIFO缓冲区的深度可以通过写入RXFIFO配置控制寄存器和通用FIFO配置控制寄存器中的CFDRFCCa.RFDC[2:0]位和CFDCFCC.CFDC[2:0]位来配 置。深度配置的6个可用选项是：

●0x000：0条消息（无法启用FIFO缓冲区）

- 0x001: 4 Messages
- 0x010: 8 Messages
- 0x011: 16 Messages
- 0x100: 32 Messages
- 0x101: 48 Messages

RX消息缓冲区和FIFO缓冲区的RAM分配限制为16条消息和64个数据字节。
不应配置超过此最大限制的RX消息缓冲区以及FIFO缓冲区。

CANFD模块逻辑不检查配置的有效性。

Note: 如果公共FIFO的FIFO深度为4条或更多消息（CFDCFCC.CFDC[2:0]>000b），则公共FIFOTX报文缓冲区链接在FIFO禁用或启用时有效。

If FIFO depth is 0 messages, then the Common FIFO TX message buffer link is not valid when the FIFO is disabled or enabled.

(4) FIFO payload size configuration

The data size of each FIFO buffer can be configured by writing to the CFDRFCCa.RFPLS[2:0] bits and CFDCFCC.CFPLS[2:0] bits in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers. The eight available options for depth configuration are:

- 000b: 8 bytes
- 001b: 12 bytes
- 010b: 16 bytes
- 011b: 20 bytes
- 100b: 24 bytes
- 101b: 32 bytes
- 110b: 48 bytes
- 111b: 64 bytes

The RAM allocation for RX message buffers along with FIFO buffers is limited to 16 messages with 64 data bytes. Configuration of the RX message buffers, along with FIFO buffers, that exceeds this maximum limit should not be done.

CANFD module logic does not check the validity of the configuration.

Note: This feature is not available in the classical CAN function.

(5) FIFO interrupt configuration

The Interrupt generation conditions for the FIFO buffers can be configured by writing to the CFDRFCCa.RFIM and CFDCFCC.CFIM bit in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers. The two available options are:

- 0:
  - RX FIFO mode: Interrupt generated when the Common FIFO counter reaches CFDRFCCa.RFIGCV/ CFDCFCC.CFIGCV value
  - TX FIFO mode: Interrupt generated when the Common FIFO transmits the last message successfully
- 1:
  - RX FIFO mode: Interrupt generated at the end of storage of every received message
  - TX FIFO mode: Interrupt generated for every successfully transmitted message

If the Interrupt Mode bit is 0 for a RX FIFO, then interrupt is generated based on the configuration of the CFDRFCCa.RFIGCV[2:0] bits.

Similarly, if the Interrupt Mode bit is 0 for a Common FIFO configured in RX mode, then interrupt is generated based on the configuration of CFDCFCC.CFIGCV[2:0] bits.

The eight available options for configuring the FIFO counter value for generation of an interrupt are:

- 000b: Interrupt generated when FIFO is 1/8th Full
- 001b: Interrupt generated when FIFO is 1/4th Full
- 010b: Interrupt generated when FIFO is 3/8th Full
- 011b: Interrupt generated when FIFO is 1/2 Full
- 100b: Interrupt generated when FIFO is 5/8th Full
- 101b: Interrupt generated when FIFO is 3/4th Full
- 110b: Interrupt generated when FIFO is 7/8th Full
- 111b: Interrupt generated when FIFO is Full.

如果FIFO深度为0消息，则在禁用或启用FIFO时通用FIFOTX消息缓冲区链接无效。

(4) FIFO有效载荷大小配置

每个FIFO缓冲区的数据大小可以通过写入CFDRFCCa.RFPLS[2:0]位和RXFIFO配置控制寄存器和通用FIFO配置控制中的CFDCFCC.CFPLS[2:0]位寄存器。深度配置的八个可用选项是：

- 000b: 8 bytes
- 001b: 12 bytes
- 010b: 16 bytes
- 011b: 20 bytes
- 100b: 24 bytes
- 101b: 32 bytes
- 110b: 48 bytes
- 111b: 64 bytes

RX消息缓冲区和FIFO缓冲区的RAM分配限制为16条消息和64个数据字节。不应配置超过此最大限制的RX消息缓冲区以及FIFO缓冲区。

CANFD模块逻辑不检查配置的有效性。

Note: 此功能在经典CAN功能中不可用。

(5) FIFO中断配置

FIFO缓冲区的中断生成条件可以通过写入CFDRFCCa.RFIM和RXFIFO配置控制寄存器和通用FIFO配置控制中的CFDCFCC.CFIM位寄存器。两个可用选项是：

- 0:
  RXFIFO模式：CommonFIFO计数器达到CFDRFCCa.RFIGCVCFDCFCC.CFIGCV值时产生中断

  TXFIFO模式：CommonFIFO成功发送最后一条报文时产生中断
- 1:
  RXFIFO模式：在每个接收到的消息存储结束时产生中断
  TXFIFO模式：为每个成功传输的消息生成中断

如果RXFIFO的中断模式位为0，则根据配置生成中断
CFDRFCCa.RFIGCV[2:0] bits.

同样，如果配置为RX模式的CommonFIFO的中断模式位为0，则根据CFDCFCC.CFIGCV[2:0]位的配置生成中断。

配置FIFO计数器值以生成中断的八个可用选项是：

- 000b：FIFO为18thFull时产生的中断
- 001b：FIFO为14thFull时产生中断
- 010b：FIFO为38thFull时产生中断
- 011b：FIFO为12Full时产生中断
- 100b：FIFO为58thFull时产生的中断
- 101b：FIFO为34thFull时产生中断
- 110b：FIFO为78thFull时产生中断
- 111b：FIFO满时产生中断。

In this case, an interrupt is generated when the message count matches the configured value.

However, there are some limitations on the configuration of the CFDRFCCa.RFIGCV[2:0] and CFDCFCC.CFIGCV[2:0] bits depending on the FDC[2:0] bits (FIFO Depth Configuration), see Table 28.24.

Table 28.24 FIFO interrupt generation counter and FIFO depth configuration

RFDC[2:0] (CFDC[2:0])	RFIGCV[2:0] (CFIGCV[2:0])							
	111b	110b	101b	100b	011b	010b	001b	000b
000b	Don't care (FIFO cannot be enabled)							
001b	Allowed	Not allowed	Allowed	Not allowed	Allowed	Not allowed	Allowed	Not allowed
010b	Allowed							
011b	Allowed							
100b	Allowed							
101b	Allowed							
110b	Allowed							
111b	Allowed							

28.6.2.2 FIFO Buffers Control

The FIFO interrupt must be enabled by setting any one of the following bits in the RX FIFO Configuration/Control Registers:

- CFDRFCCa.RFIE

In addition, the FIFO interrupt must be enabled by setting any one of the following bits in the Common FIFO Configuration/Control Register:

- CFDCFCC.CFRXIE
- CFDCFCC.CFTXIE

After configuration is complete, each FIFO can be enabled by setting the CFDRFCCa.RFE and CFDCFCC.CFE bits in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Register to allow transmission and reception of messages.

28.7 Interrupts and DMA

28.7.1 Interrupts

The CANFD module generates several interrupts. The interrupt output, which is connected to the Interrupt Controller Unit (ICU), can be controlled by the corresponding interrupt enable bit.

The status flag is set independent from this enable bit.

The channel transmission interrupt has an additional status flag register. The status bits are set when the corresponding interrupt enables are set.

The status flag register supports the identification of the interrupt source for the channel transmission, as this interrupt is driven by several trigger sources.

The interrupts in the CANFD module can be classified into two groups, global interrupts and channel interrupts:

- Global interrupts:
  The CANFD module can generate 3 global interrupts:
  - Global interrupt for successful reception into the 2 RX FIFO buffers
  - Global error interrupt.
  - Global Interrupt for successful reception into the 32 RX message buffers
- Channel interrupts:
  Channel of the CANFD module can generate 3 channel interrupts:

在这种情况下，当消息计数与配置值匹配时会产生中断。

但是，CFDRFCCa.RFIGCV[2:0]和CFDCFCC.CFIGCV[2:0]位的配置有一些限制，具体取决于FDC[2:0]位（FIFO深度配置），请参见表28.24。

Table 28.24 FIFO中断生成计数器和FIFO深度配置

RFDC[2:0] (CFDC[2:0])	RFIGCV[2:0] (CFIGCV[2:0])							
	111b	110b	101b	100b	011b	010b	001b	000b
000b	无关（无法启用FIFO）							
001b	Allowed	不允许	Allowed	不允许	Allowed	不允许	Allowed	不允许
010b	Allowed							
011b	Allowed							
100b	Allowed							
101b	Allowed							
110b	Allowed							
111b	Allowed							

28.6.2.2 FIFO缓冲器控制

必须通过设置RXFIFO配置控制中的以下任一位来启用FIFO中断
Registers:

- CFDRFCCa.RFIE

此外，必须通过设置CommonFIFO中的以下任一位来启用FIFO中断
Configuration/Control Register:

- CFDCFCC.CFRXIE
- CFDCFCC.CFTXIE

配置完成后，可以通过设置CFDRFCCa.RFE和CFDCFCC.CFE位来使能每个FIFO
RXFIFO配置控制寄存器和通用FIFO配置控制寄存器，以允许发送和接收消息。

28.7 中断和DMA

28.7.1 Interrupts

CANFD模块产生几个中断。连接到中断控制器单元（ICU）的中断输出可由相应的中断使能位控制。

状态标志的设置独立于该使能位。
通道传输中断有一个额外的状态标志寄存器。当相应的中断使能被设置时，状态位被设置。

状态标志寄存器支持识别通道传输的中断源，因为该中断由多个触发源驱动。

CANFD模块中的中断可以分为两类，全局中断和通道中断：

- Global interrupts:
  CANFD模块可以产生3个全局中断：
  成功接收到2个RXFIFO缓冲区的全局中断
  全局错误中断。
  成功接收到32个RX消息缓冲区的全局中断
- Channel interrupts:
  CANFD模块的通道可以产生3个通道中断：

1. Channel transmission
   - Transmission completion from channel
   - Transmission abort from channel
   - Transmission from TX Queue for a channel
   - Channel THL interrupt
   - Successful transmission from a Common FIFO in TX mode for a channel.
2. Channel error interrupt
3. Successful reception in a Common FIFO in RX mode for a channel.

The interrupts are cleared when the corresponding flag bits are cleared or the Interrupt enable bits are cleared.

Table 28.25 gives an overview of interrupt sources for the different interrupt outputs. The interrupt outputs are active-high.

Table 28.25 Interrupt source overview

Parameter	Interrupt	Name	Interrupt source	Interrupt clearing
Global Interrupts	Successful reception into at least one RX FIFO	CAN_RXF	interrupt flag of corresponding RX FIFO for which interrupt is enabled	clear the interrupt flag of corresponding RX FIFO buffer for which interrupt is enabled
	Global Error	CAN_GLR	any of the following: ● DLC Error Flag ● Message Lost Status bit ● TX History Entry Lost Status bit ● CANFD Message Payload overflow flag	clear all of : ● DLC Error Flag ● Message Lost Flags in all of the FIFO Status Registers ● TX History List Entry Lost Flag ● CANFD Message Payload overflow flag
	Successful reception into at least one RXMB	CAN0_RXMB	interrupt flag of corresponding RXMB for which interrupt is enabled	clear the interrupt flag of corresponding RXMB buffer for which interrupt is enabled
Channel Transmission Interrupts	Channel successful transmission	CAN0_TX	any channel related TXMB Successful flag when Interrupt is enabled*1	clear all channel related TX MB Result status bits for which the Interrupt is enabled
	Channel Abort		any channel related TXMB Abort f lag when Interrupt is enabled*1	clear all channel related TX MB Result Status bits for which the Interrupt is enabled globally
	Channel transmission from TX Queue		related channel TX Queue Interrupt Flag	clear related channel TX Queue Interrupt Flag
	Channel THL Interrupt		Channel THL Interrupt status flag	clear the relevant THL Interrupt status flag
	Channel COM FIFO TX Interrupt		Interrupt Flag for Common FIFOs in TX mode belonging to the related channel	clear the interrupt f lags of Common FIFOs in TX mode belonging to the related channel
Channel Error Interrupt	Channel Error	CAN0_CHERR	any channel related error flag in the Channel Error Flag Register for which Interrupt is enabled in the Channel Error Interrupt Enable Register	clear all channel related error f lags in the Channel Error Flag Register for which Interrupt is enabled in the Channel Error Interrupt Enable Register
Channel COM RX FIFO Interrupt	Channel COM FIFO RX Interrupt	CAN0_COMFRX	Interrupt flag for Common FIFOs in RX mode belonging to the related channel	clear the interrupt flags of Common FIFOs in RX mode belonging to the related channel

Note 1. These interrupts are only set for TX Message Buffers that do not belong to anenabled TX Queue andare not pointing to a common FIFO.
Separate interrupts are provided for common FIFO buffers and TX Queue.

1.渠道传输
从通道传输完成
从通道中止传输
从通道的TX队列传输
通道THL中断
通道在TX模式下从CommonFIFO成功传输。
2.通道错误中断
3.通道在RX模式下的CommonFIFO中成功接收。

当相应的标志位被清除或中断使能位被清除时，中断被清除。

表28.25概述了不同中断输出的中断源。中断输出为高电平有效。

Table 28.25 中断源概述

Parameter	Interrupt	Name	中断源	中断清除
Global Interrupts	成功接收到至少一个RXFIFO	CAN_RXF	对应的RXFIFO的中断标志，其中断使能	清除相应的允许中断的RXFIFO缓冲区的中断标志
	全局错误	CAN_GLR	以下任何一项：● DLC错误标志 ● 消息丢失状态位 ● TX历史条目丢失状态位 ● CANFD消息负载溢出标志	清除所有： ● DLC错误标志 ● 所有FIFO状态寄存器中的消息丢失标志 ● TX历史列表条目丢失Flag ● CANFD消息负载溢出标志
	成功接收到至少一个RXMB	CAN0_RXMB	中断使能的相应RXMB的中断标志	清除相应的允许中断的RXMB缓冲区的中断标志
通道传输 Interrupts	通道传输成功	CAN0_TX	允许中断时任何与通道相关的TXMB成功标志*1	清除所有通道相关的TXMB结果状态位 中断已启用
	频道中止		允许中断时任何与通道相关的TXMB中止标志*1	清除所有通道相关的TXMB结果状态位 全局启用中断
	来自TXQueue的通道传输		相关通道TX队列中断标志	清除相关通道TX队列中断标志
	Channel THL Interrupt		通道THL中断状态标志	清除相关的THL中断状态标志
	通道COMFIFO TX Interrupt		属于相关通道的TX模式下CommonFIFO的中断标志	清除属于相关通道的TX模式下CommonFIFO的中断标志
通道错误Interrupt	通道错误	CAN0_CHERR	通道错误标志寄存器中的任何通道相关错误标志 在通道错误中启用中断 中断使能寄存器	清除通道错误标志寄存器中所有通道相关的错误标志，在通道错误中断允许寄存器中允许中断
通道COM RX FIFO Interrupt	通道COMFIFO RX Interrupt	CAN0_COMFRX	属于相关通道的RX模式下CommonFIFO的中断标志	清除属于相关通道的RX模式下CommonFIFO的中断标志

注1.这些中断仅针对不属于启用的TX队列且不指向公共的TX消息缓冲区设置FIFO.
为常见的FIFO缓冲区和TX队列提供了单独的中断。

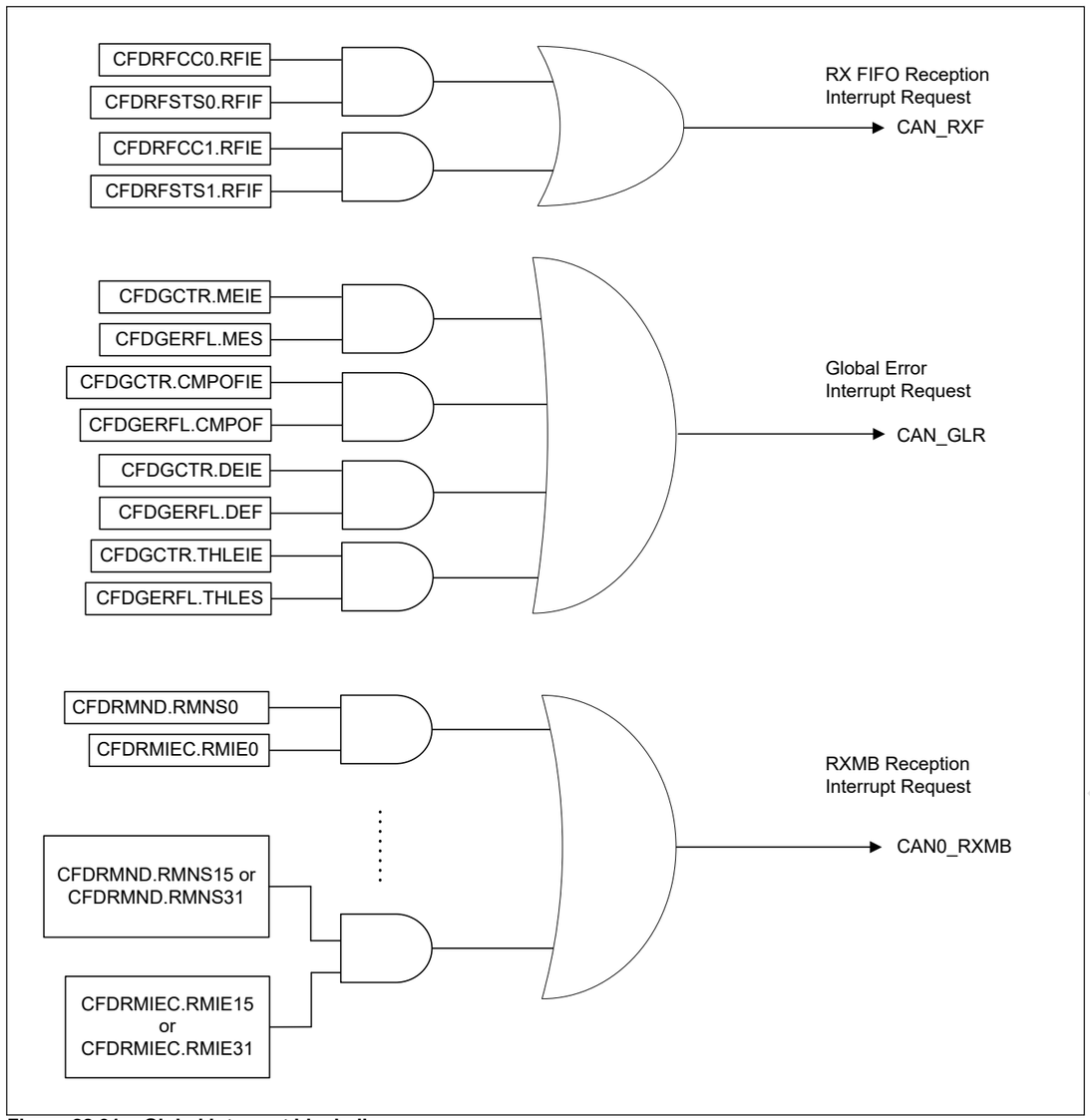


Figure 28.31 Global interrupt block diagram

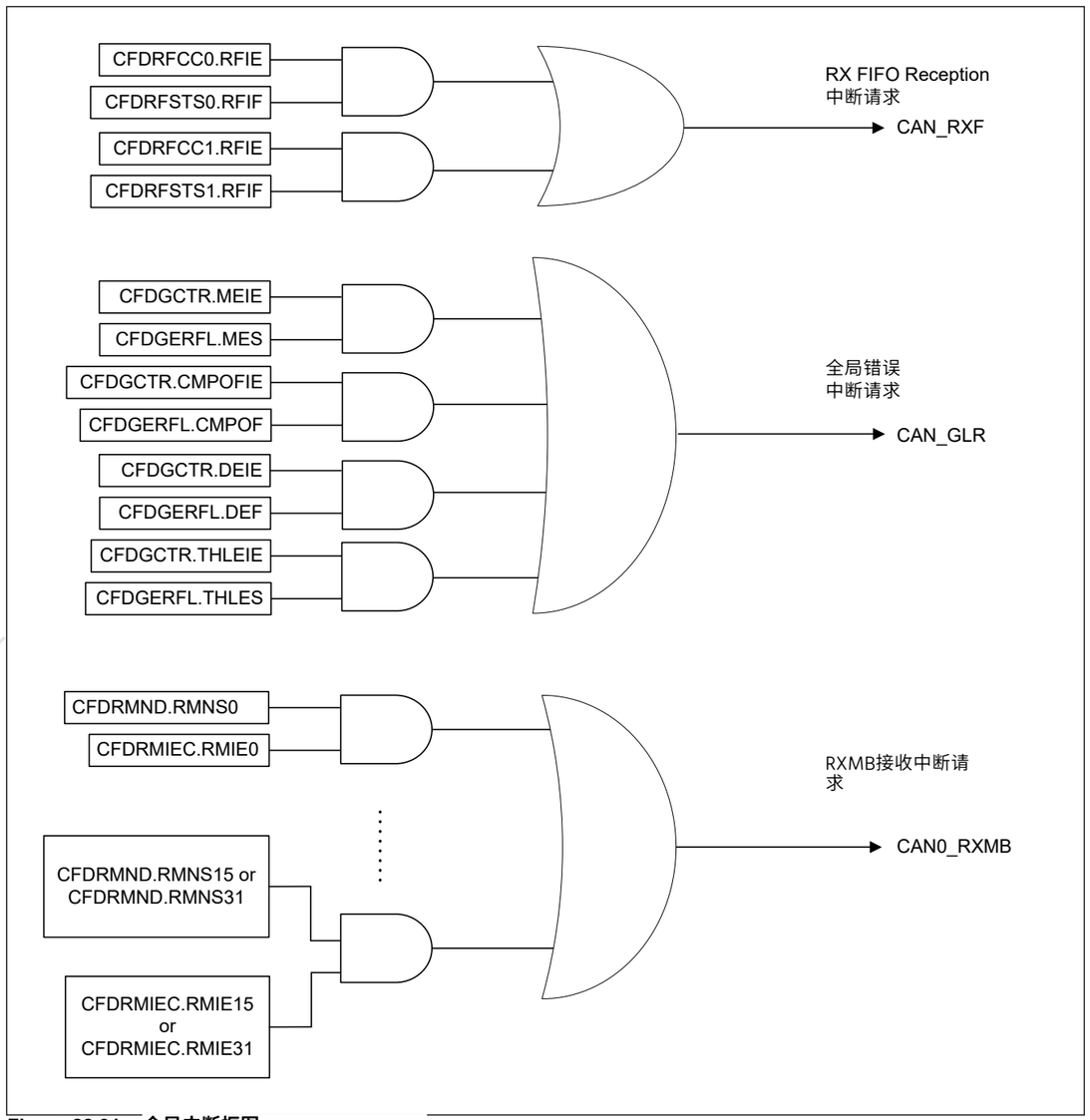


Figure 28.31 全局中断框图

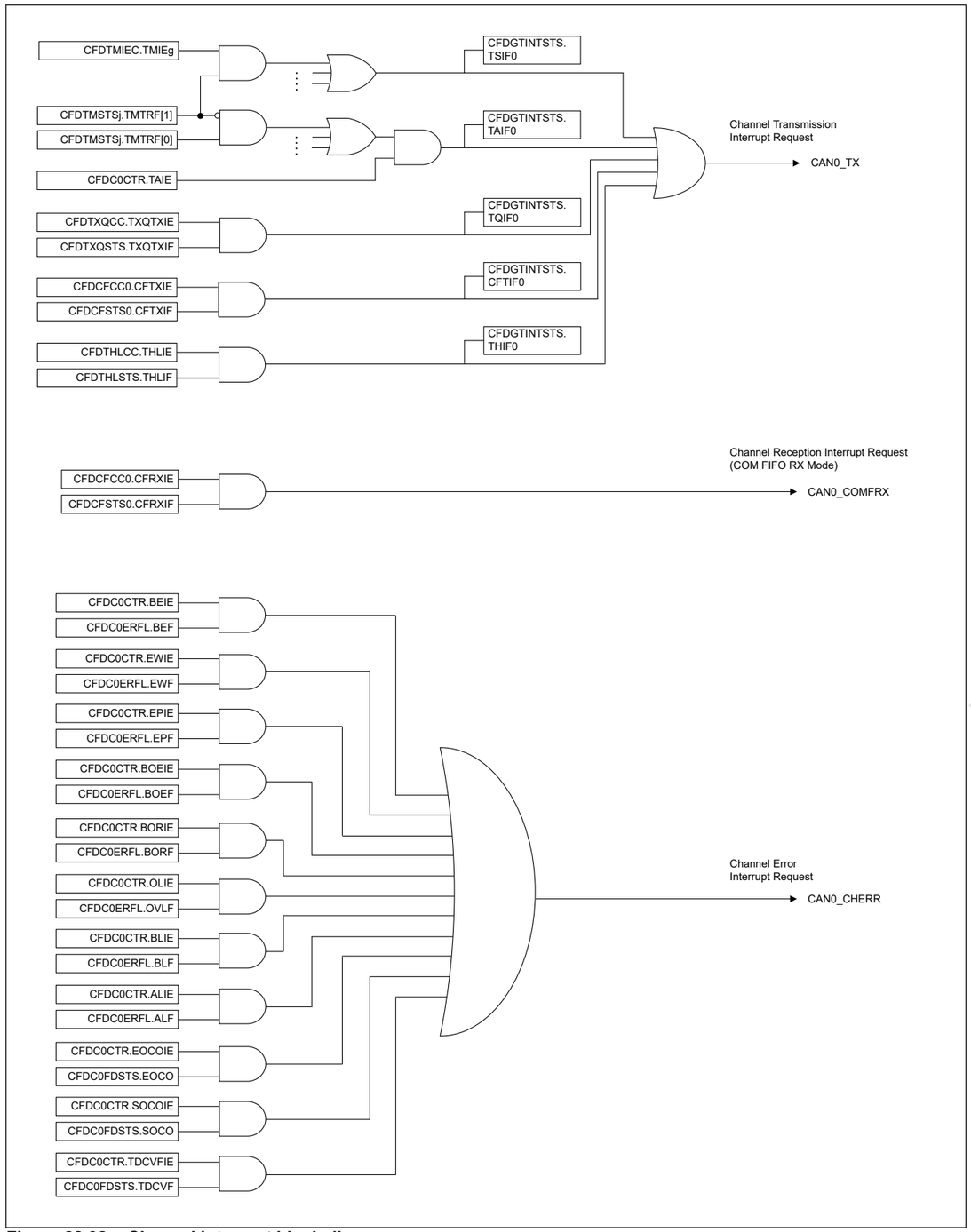


Figure 28.32 Channel interrupt block diagram

28.7.2 DMA Transfer

The CANFD module has message buffers that can be associated with a DMA channel:

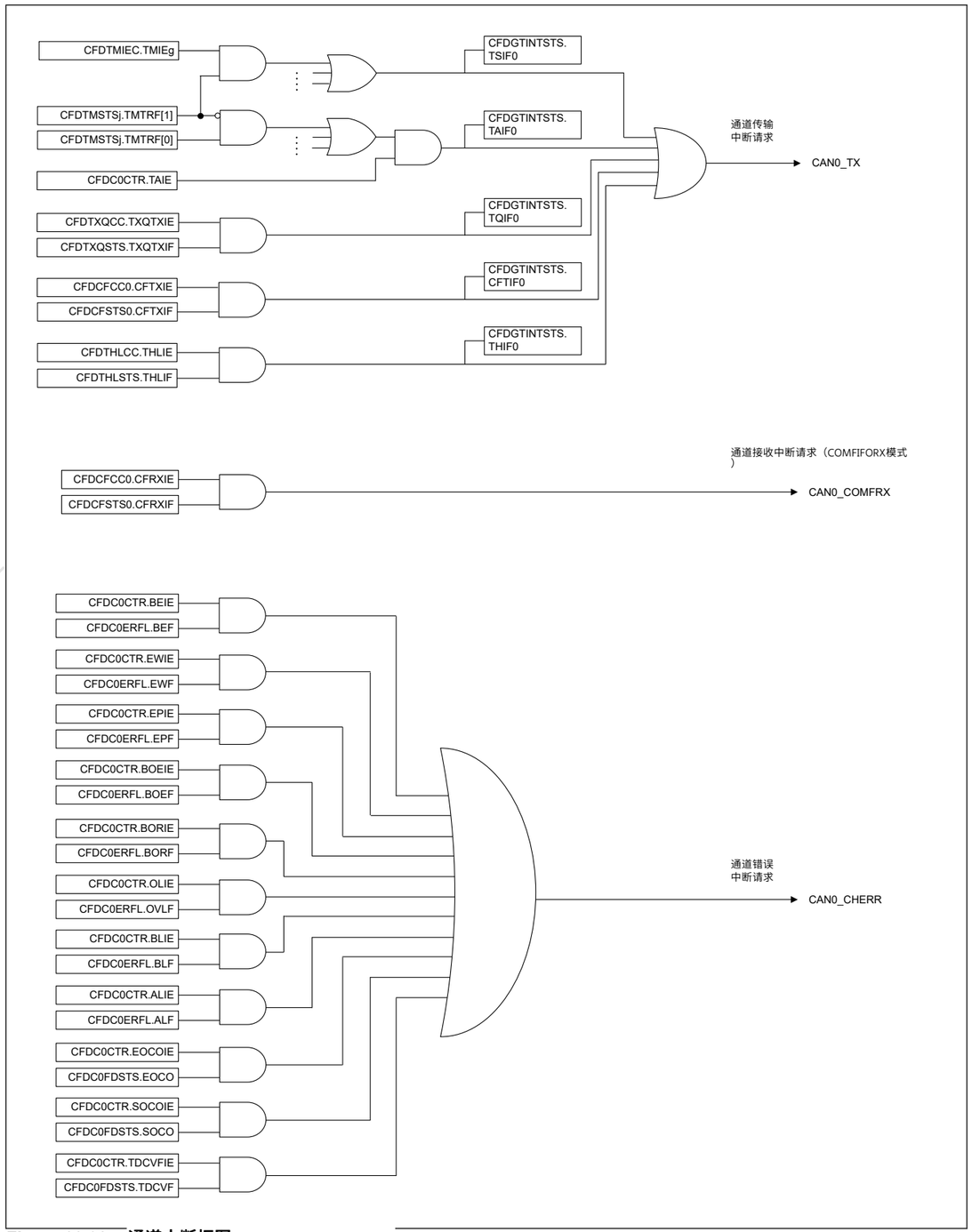


Figure 28.32 通道中断框图

28.7.2 DMA Transfer

CANFD模块具有可与DMA通道关联的消息缓冲区：

- Reception DMA
  - 2 RX FIFO message buffers
  - Common FIFO Message Buffer

Figure 28.33 shows the potential DMA channels.

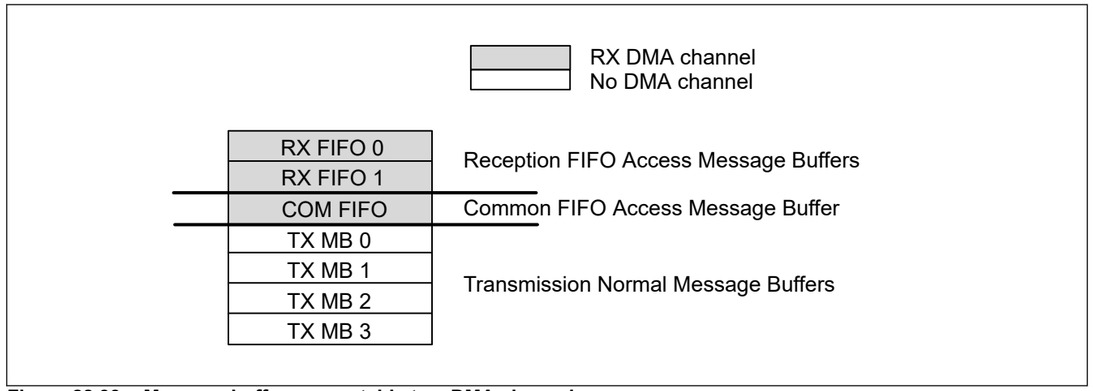


Figure 28.33 Message buffer connectable to a DMA channel

A DMA channel transfer request is generated for each FIFO entry to the DMAC when the related CFDCDTCT.RFDMAE or CFDCDTCT.CFDMAE is set to 1 and the belonging FIFO is not empty.

Reception FIFO Interrupt should be disabled for this particular FIFO (CFDRFCCa.RFIE or CFDCFCC.CFRXIE)

Use the regular start address for the DMA access window address. See Figure 28.34.

Table 28.26 DMA channel access window address

b = Message buffer component index	Message Buffer Component	Register	P	Regular Start Address
b = [0…1]	RFMBCPb[0]	CFDRFIDb	x	0x0520 + b × 0x004C
		CFDRFPTRb	x	0x0524 + b × 0x004C
		CFDRFFDSTSb	x	0x0528 + b × 0x004C
		CFDRFDFbp	[0…15]	0x052C + p × 0x0004 + b × 0x004C
—	CFMBCP0[0]	CFDCFID	x	0x05B8
		CFDCFPTR	x	0x05BC
		CFDCFFDCSTS	x	0x05C0
		CFDCFDFp	[0…15]	0x05C4 + p × 0x0004

DMA FIFO pointer decrement is done automatically by reading the last configured data payload byte (CFDRFCCa.RFPLS or CFDCFCC.CFPLS).

Note: The DMA must read the exact length of the configured data payload size (CFDRFCCa.RFPLS or CFDCFCC.CFPLS).

Note: This feature is not available for classical CAN function because CFDRFCCa.RFPLS and CFDCFCC.CFPLS are not in classical CAN.

Do not write to the FIFO control registers when DMA is enabled. The DMA enable of the particular DMA FIFO (CFDCDTCT.RFDMAE or CFDCDTCT.CFDMAE) can be set at any time. Figure 28.34 shows a configuration flow for an initial setup.

- Reception DMA
  2个RXFIFO消息缓冲区
  通用FIFO消息缓冲区

图28.33显示了潜在的DMA通道。

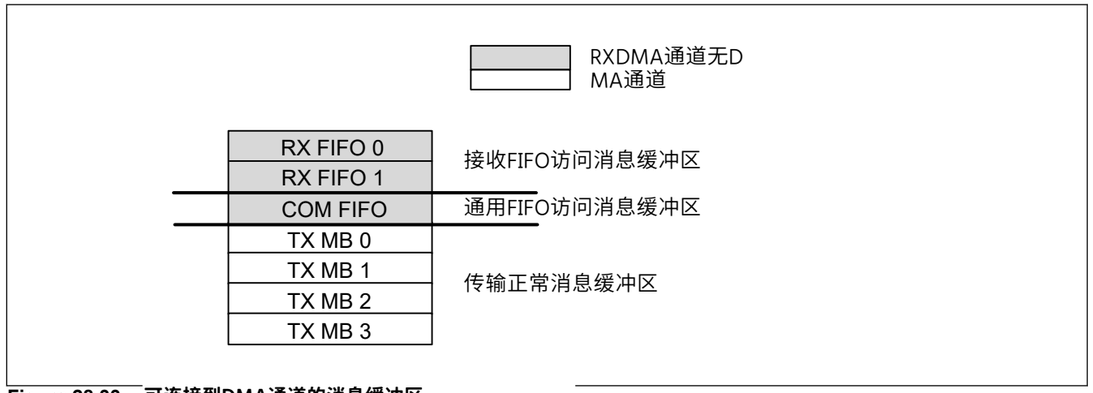


Figure 28.33 可连接到DMA通道的消息缓冲区

当相关的CFDCDTCT.RFDMAE或
CFDCDTCT.CFDMAE设置为1并且所属的FIFO不为空。

应禁用此特定FIFO（CFDRFCCa.RFIE或CFDCFCC.CFRXIE）的接收FIFO中断

使用常规起始地址作为DMA访问窗口地址。请参见图28.34。

Table 28.26 DMA通道访问窗口地址

b=消息缓冲区组件索引	Message Buffer Component	Register	P	常规起始地址
b = [0…1]	RFMBCPb[0]	CFDRFIDb	x	0x0520 + b × 0x004C
		CFDRFPTRb	x	0x0524 + b × 0x004C
		CFDRFFDSTSb	x	0x0528 + b × 0x004C
		CFDRFDFbp	[0…15]	0x052C + p × 0x0004 + b × 0x004C
—	CFMBCP0[0]	CFDCFID	x	0x05B8
		CFDCFPTR	x	0x05BC
		CFDCFFDCSTS	x	0x05C0
		CFDCFDFp	[0…15]	0x05C4 + p × 0x0004

DMAFIFO指针递减是通过读取最后配置的数据有效负载字节（CFDRFCCa.RFPLS或CFDCFCC.CFPLS）自动完成的。

Note: DMA必须读取配置的数据有效负载大小（CFDRFCCa.RFPLS或CFDCFCC.CFPLS).

Note: 此功能不适用于经典CAN功能，因为CFDRFCCa.RFPLS和CFDCFCC.CFPLS不在经典CAN中。

启用DMA时不要写入FIFO控制寄存器。可以随时设置特定DMAFIFO（CFDCDTCT.RFDMAE或CFDCDTCT.CFDMAE）的DMA使能。图28.34显示了初始设置的配置流程。

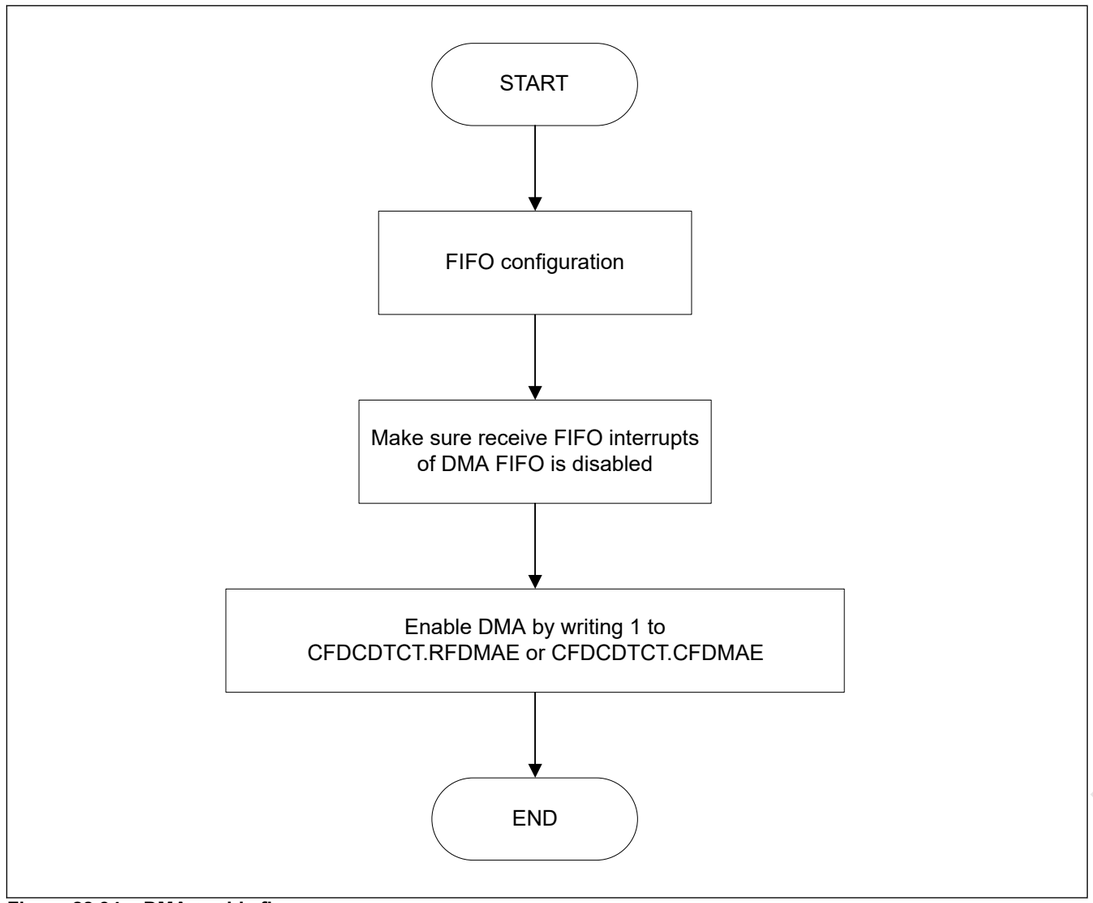


Figure 28.34 DMA enable flow

To disable a DMA transfer request, you must disable the particular DMA enable bit (CFDCDTCT.RFDMAE or CFDCDTCT.CFDMAE). If the disable is made during an ongoing transfer, then the transfer must be completed first before further action can be taken. The transfer status can be identified by the CFDCDTSTS.RFDMASTS or CFDCDTSTS.CFDMASTS bit. See Figure 28.35 for the DMA disable flow. When the DMA is disabled, consideration should be made for the remaining or new incoming messages to this particular reception FIFO.

When the FIFO is not disabled, reception to the FIFO continues.

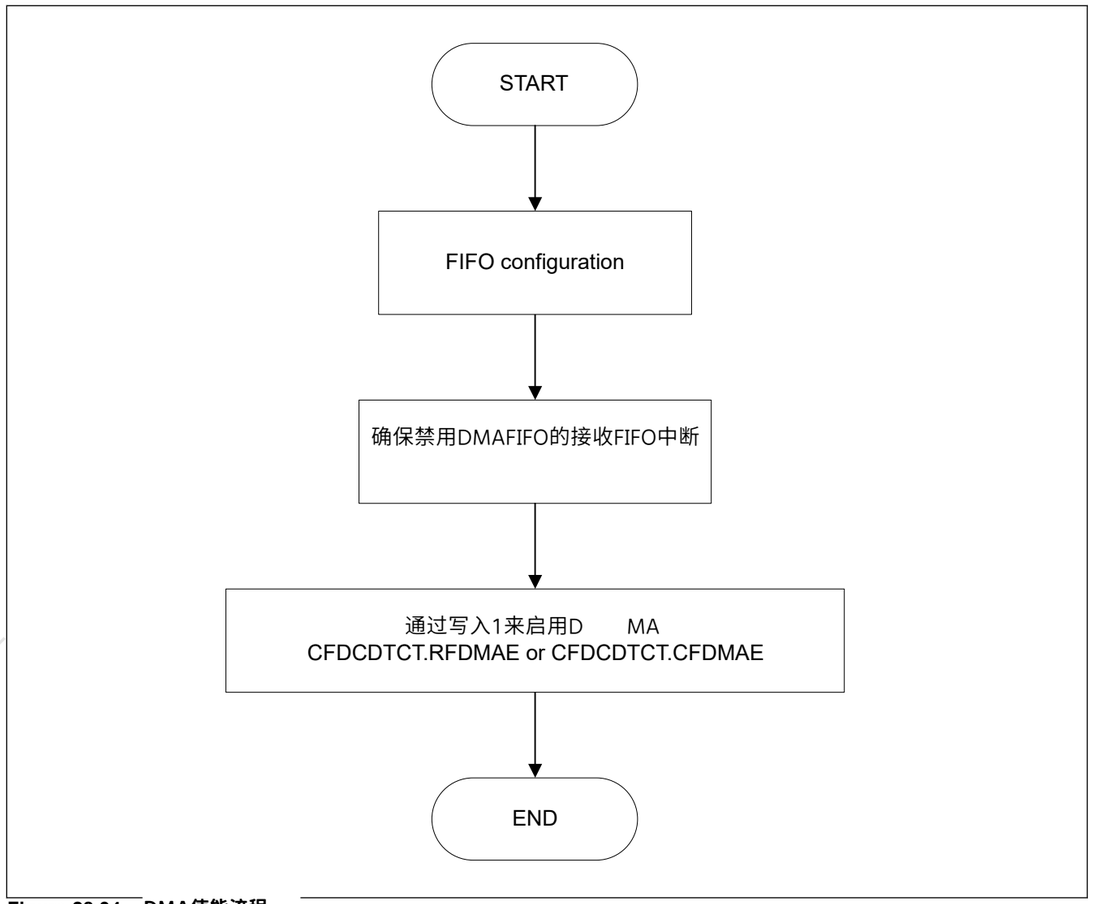


Figure 28.34 DMA使能流程

要禁用DMA传输请求，您必须禁用特定的DMA启用位（CFDCDTCT.RFDMAE或CFDCDTCT.CFDMAE)。如果在正在进行的传输过程中进行了禁用，则必须先完成传输，然后才能采取进一步的操作。传输状态可以通过CFDCDTSTS.RFDMASTS或CFDCDTSTS.CFDMASTS位来识别。有关DMA禁用流程，请参见图28.35。禁用DMA时，应考虑到此特定接收FIFO的剩余或新传入消息。

当FIFO未被禁用时，继续接收FIFO。

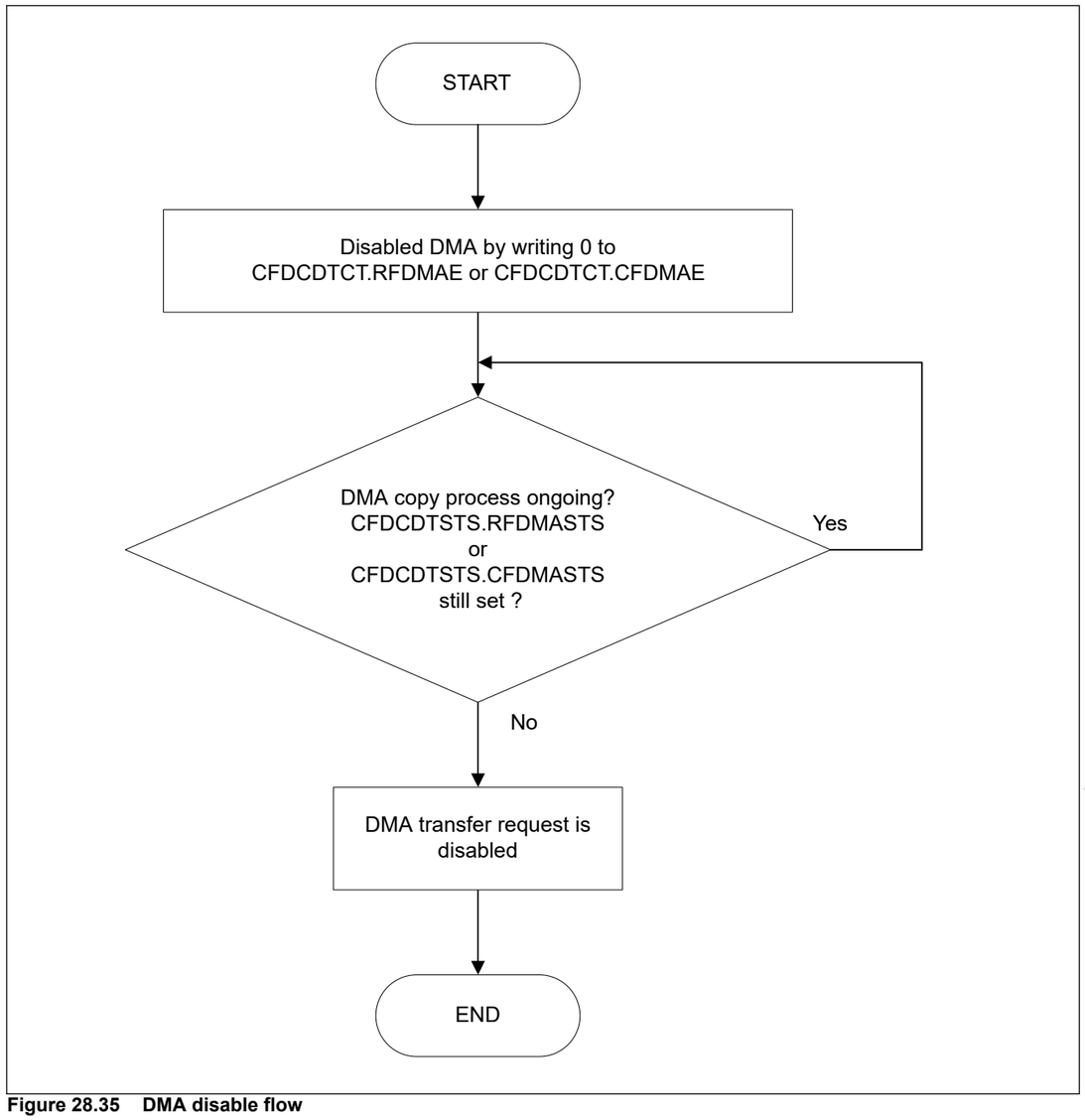


Figure 28.35 DMA disable flow

28.8 Reception and Transmission

28.8.1 Reception

In the CANFD module, CAN messages received on any of the channels are stored in RX message buffers, RX FIFO buffers, or Common FIFO buffers configured in RX mode depending on the Acceptance Filter List entries.

- Up to 32 RX message buffers can be configured
- 2 RX FIFO buffers available
- 1 Common FIFO Buffer can be configured in RX mode

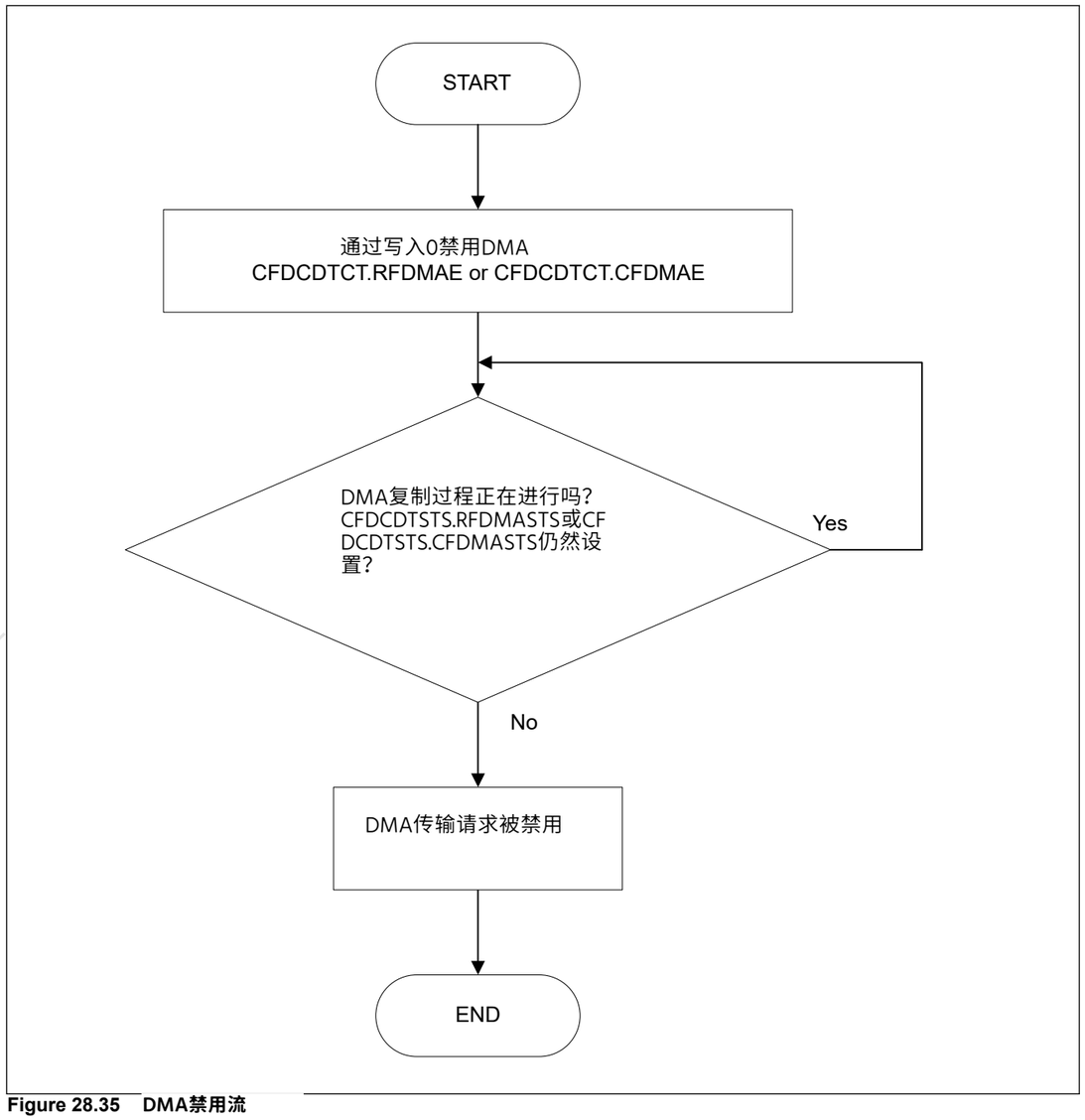


Figure 28.35 DMA禁用流

28.8 接收和传输

28.8.1 Reception

在CANFD模块中，任何通道上接收的CAN报文都存储在RX报文缓冲区、RXFIFO缓冲区或配置为RX模式的Common FIFO缓冲区中，具体取决于AcceptanceFilterList条目。

- ●最多可配置32个RX报文缓冲区
- ●2个RXFIFO缓冲器可用
- ●RX模式下可配置1个CommonFIFOBuffer

28.8.1.1 Message Storage in RX Message Buffers

When a message is successfully received and stored in a RX message buffer, the corresponding New Data flag is set in the RX Message Buffer New Data Register.

The CAN message can be read from the corresponding RX message buffer.

If a new message is stored into a RX message buffer before the previous message in this message buffer can be read, then the original message is overwritten. There is no mechanism for preventing a new message from overwriting the current message in the RX message buffer. If such a loss of messages is not acceptable, then RX FIFO should be used for storing related messages.

Note: Users should do the same processing as the existing software flow also when using interrupt. (see Figure 28.37)

Note: Unused data bytes are filled with 0x00 depending on the DLC value.

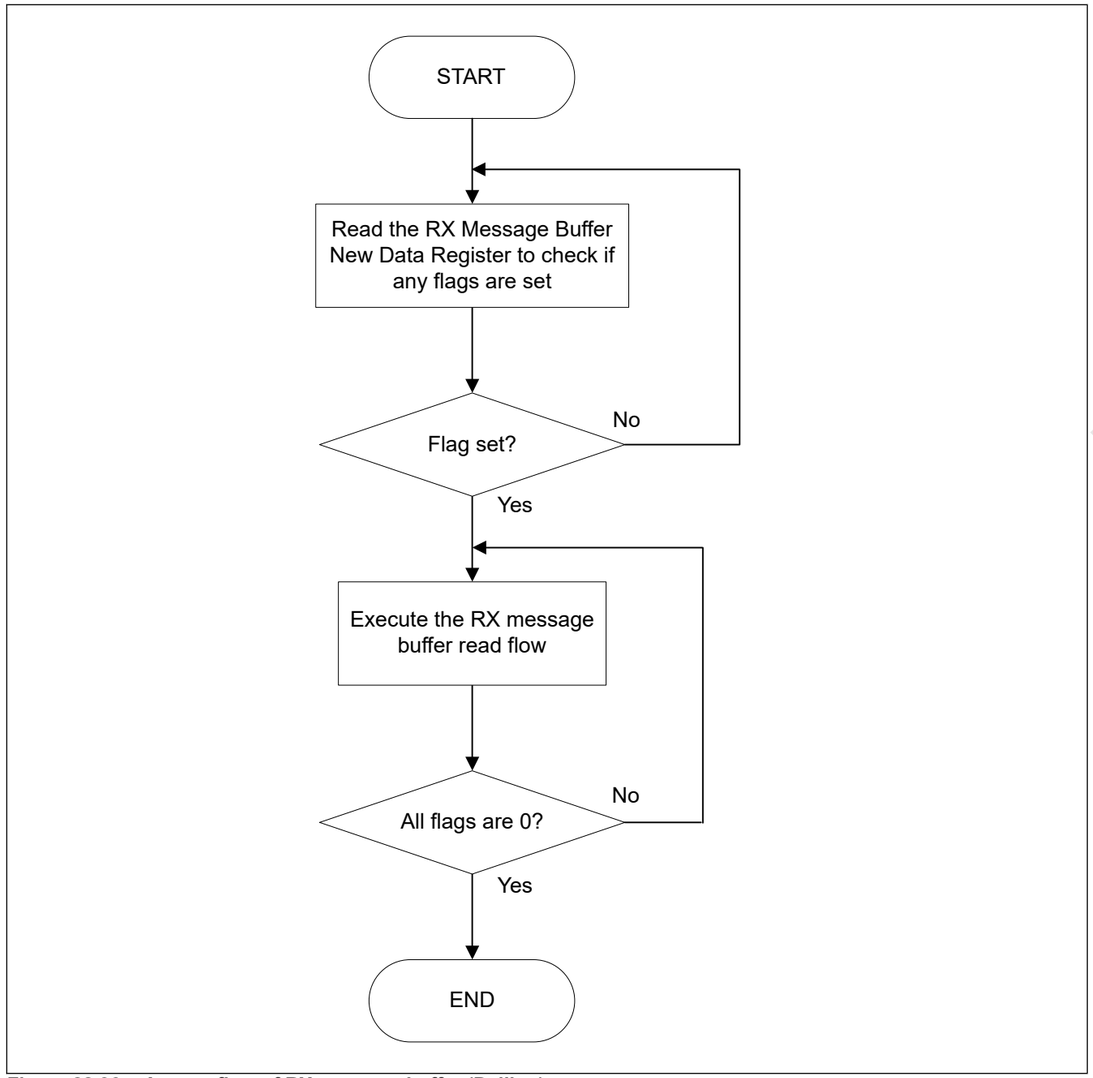


Figure 28.36 Access flow of RX message buffer (Polling)

28.8.1.1 RX消息缓冲区中的消息存储

当消息被成功接收并存储在RX消息缓冲区中时，相应的NewData标志在RX消息缓冲区新数据寄存器。

CAN报文可以从相应的RX报文缓冲区中读取。

如果在可以读取此消息缓冲区中的前一个消息之前将新消息存储到RX消息缓冲区中，则原始消息将被覆盖。没有机制可以防止新消息覆盖RX消息缓冲区中的当前消息。如果这样的消息丢失是不可接受的，则应使用RXFIFO来存储相关消息。

Note: 用户在使用中断时也应与现有软件流程进行相同的处理。（见图28.37）

Note: 未使用的数据字节根据DLC值填充为0x00。

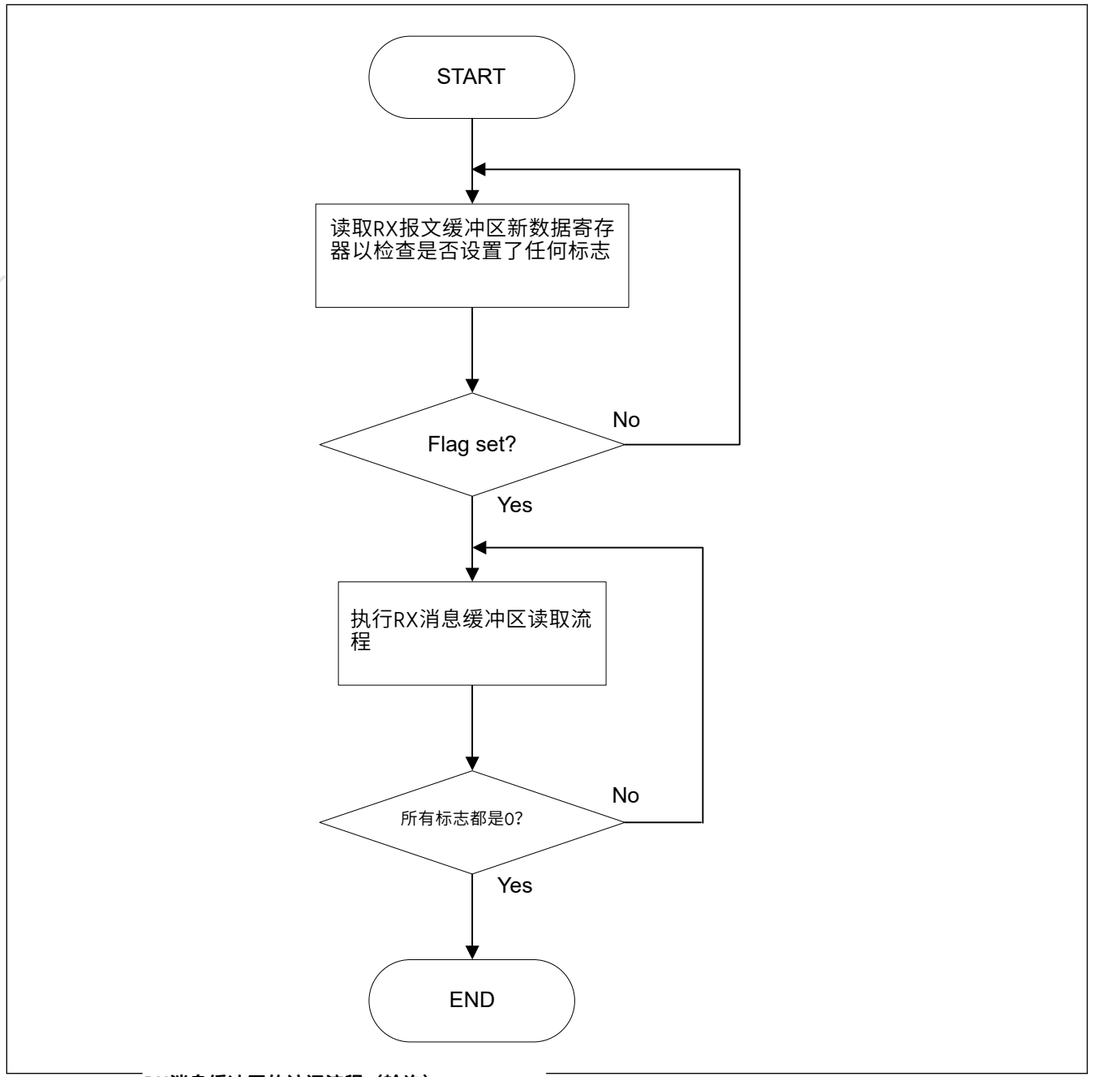


Figure 28.36 RX消息缓冲区的访问流程（轮询）

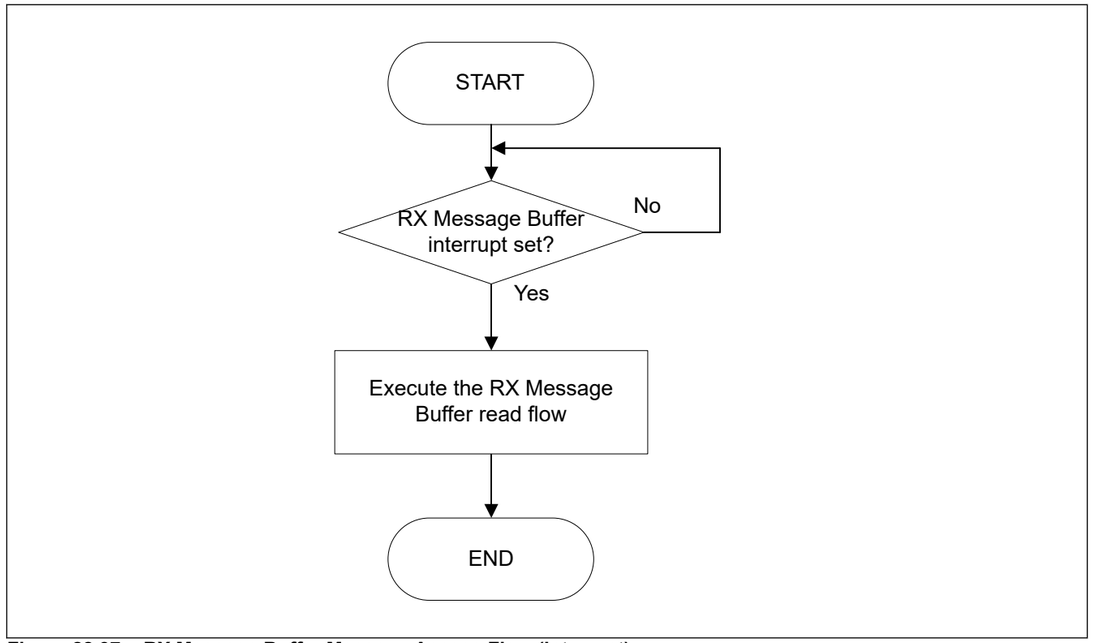


Figure 28.37 RX Message Buffer Message Access Flow (interrupt)

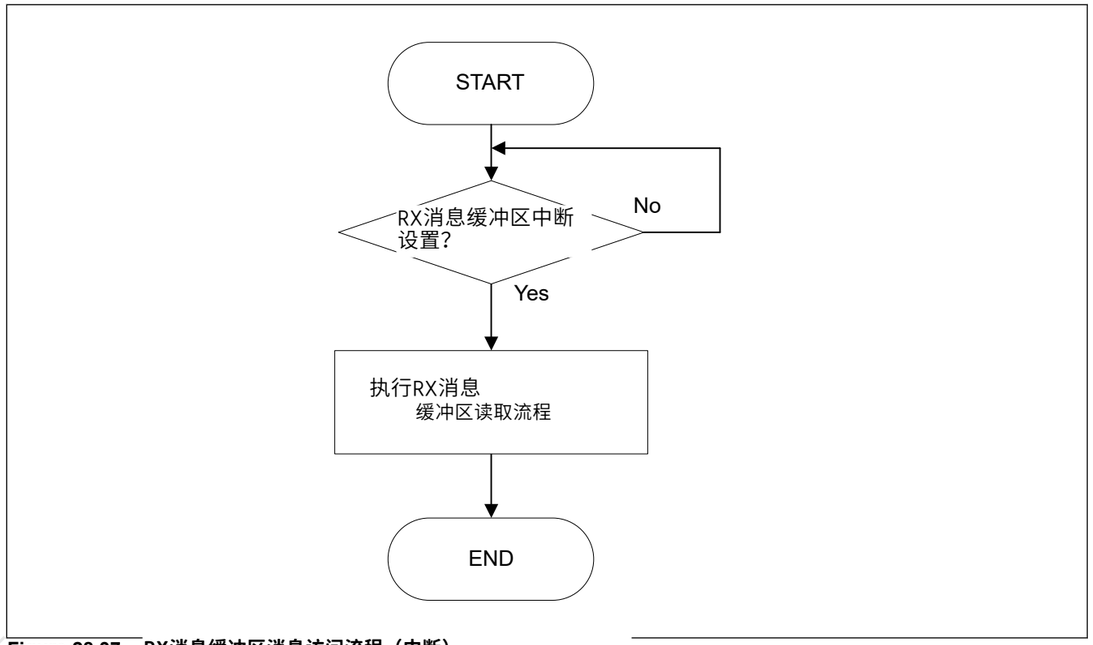


Figure 28.37 RX消息缓冲区消息访问流程（中断）

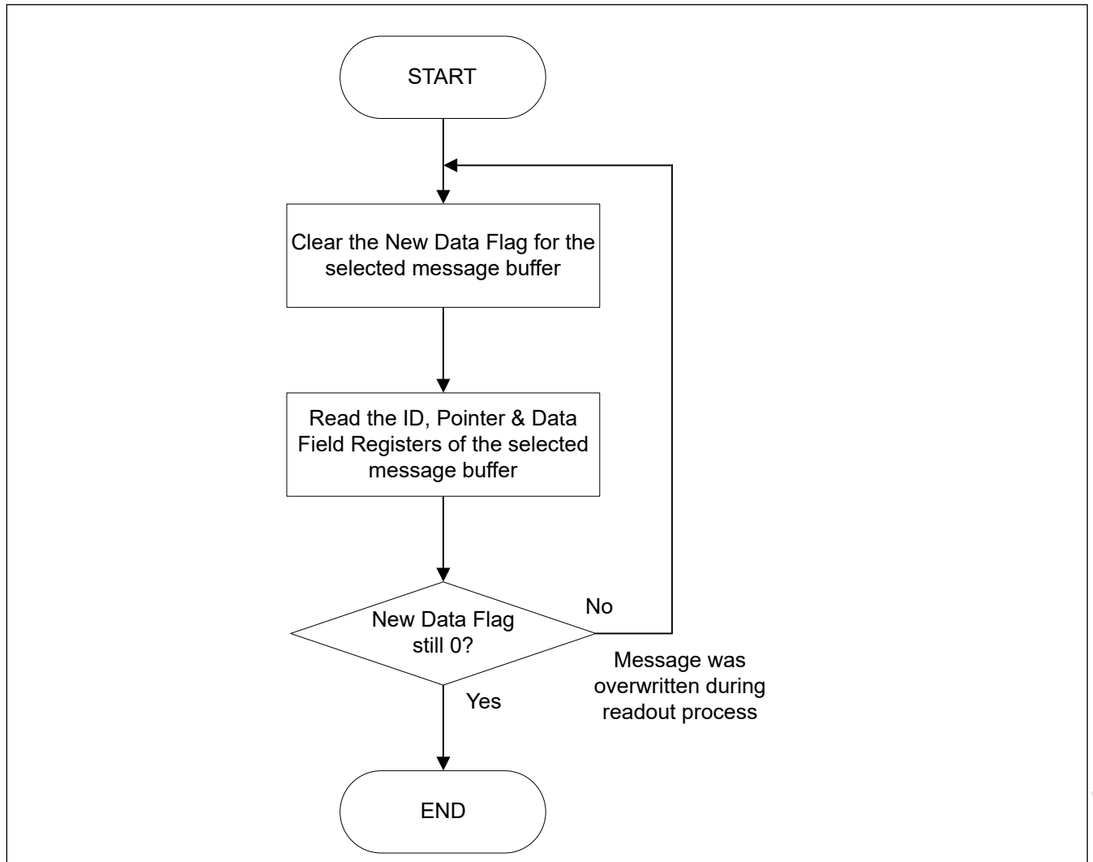


Figure 28.38 Read flow of RX message buffer

28.8.1.2 Message Storage in FIFO Buffers

The AFL entries for routing the received messages to RX FIFO buffers or Common FIFO buffer configured in RX mode should be configured based on system requirements.

The CFDGAFLP1r.GAFLFDP[8,1:0] field in the matching AFL entry selects the FIFO buffers to which the related reception message is stored.

When the received message is stored in one or more RX FIFO buffers or Common FIFO buffer configured in RX mode, the message counter value is incremented in the corresponding RX FIFO Status Registers or Common FIFO Status Register.

Depending on the configuration of the FIFO buffers, an interrupt might also be generated.

The message can be read from the corresponding FIFO Access registers.

Note: Because many messages can be stored in the FIFO buffers, reading more than one message may be required to read the latest message stored in a FIFO buffer.

If the message count value matches the FIFO depth, the FIFO Full flag is set.

When the value 0xFF is written to the corresponding FIFO Pointer Control Register, the message count is decremented by 1.

Only write 0xFF to the FIFO Pointer Control register after reading the complete message from the FIFO Access registers of the corresponding FIFO.

When all the messages stored in the FIFO are read, the FIFO Empty flag is set.

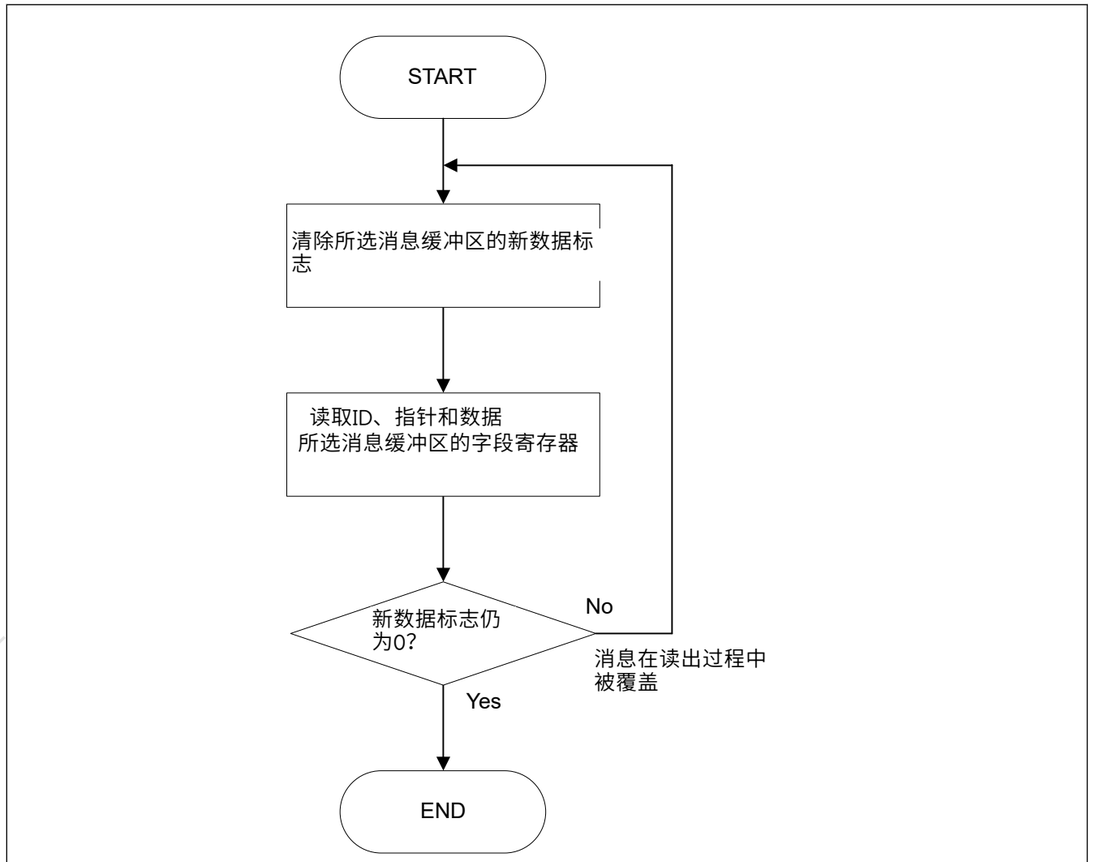


Figure 28.38 读取RX消息缓冲区的流程

28.8.1.2 FIFO缓冲区中的消息存储

将接收到的报文路由到RXFIFO缓冲区或配置为RX模式的CommonFIFO缓冲区的AFL条目应根据系统要求进行配置。

匹配AFL条目中的CFDGAFLP1r.GAFLFDP[8 1:0]字段选择存储相关接收消息的FIFO缓冲区。

当接收到的报文存储在一个或多个配置为RX模式的RXFIFO缓冲区或CommonFIFO缓冲区时，报文计数器值在相应的RXFIFO状态寄存器或CommonFIFO状态寄存器中递增。

根据FIFO缓冲区的配置，也可能会产生中断。

该消息可以从相应的FIFO访问寄存器中读取。

Note: 因为许多消息可以存储在FIFO缓冲区中，所以可能需要读取多个消息才能读取存储在FIFO缓冲区中的最新消息。

如果消息计数值与FIFO深度匹配，则设置FIFO满标志。

当值0xFF写入相应的FIFO指针控制寄存器时，消息计数减1。

仅在从相应FIFO的FIFO访问寄存器中读取完整报文后，将0xFF写入FIFO指针控制寄存器。

当读取存储在FIFO中的所有消息时，设置FIFOEmpty标志。

If a new message is stored into the FIFO when the FIFO message count matches the FIFO depth (FIFO full condition), the FIFO Message Lost flag is set and the new message is lost (no overwrite of already stored messages takes place).

An appropriate value can be configured as warning level to generate an interrupt before the FIFO full condition occurs to avoid loss of a message due to an overrun condition.

Note: The message lost can be set only in RX mode by CAN, and the flag is not set when the CPU is overloading the FIFO buffers.

The RX FIFO buffers and the Common FIFO buffers configured in RX mode can be disabled at any time by clearing the CFDRFCCa.RFE or CFDCFCC.CFE bit in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers.

When the CFDRFCCa.RFE or CFDCFCC.CFE bit is cleared, the message read and write pointers of the FIFO are cleared and are no longer active. Therefore, all messages in the FIFO buffers are lost and no further messages can be stored into the FIFO.

When the RX FIFO buffers or Common FIFO buffer configured in RX mode is assigned as a DMA channel, software should not access the FIFO Access Register of this FIFO buffer or write 0xFF to the FIFO Pointer Control Register (CFDCFPCTR.CFPC or CFDRFPCTRa.RFPC). This can lead to unintended FIFO message decrement. The DMA channel controls the FIFO decrement automatically.

Note: If the interrupt flag is set for a FIFO buffer and then the FIFO is disabled, the interrupt flag is not cleared automatically. The interrupt flag should be cleared before disabling the FIFO.

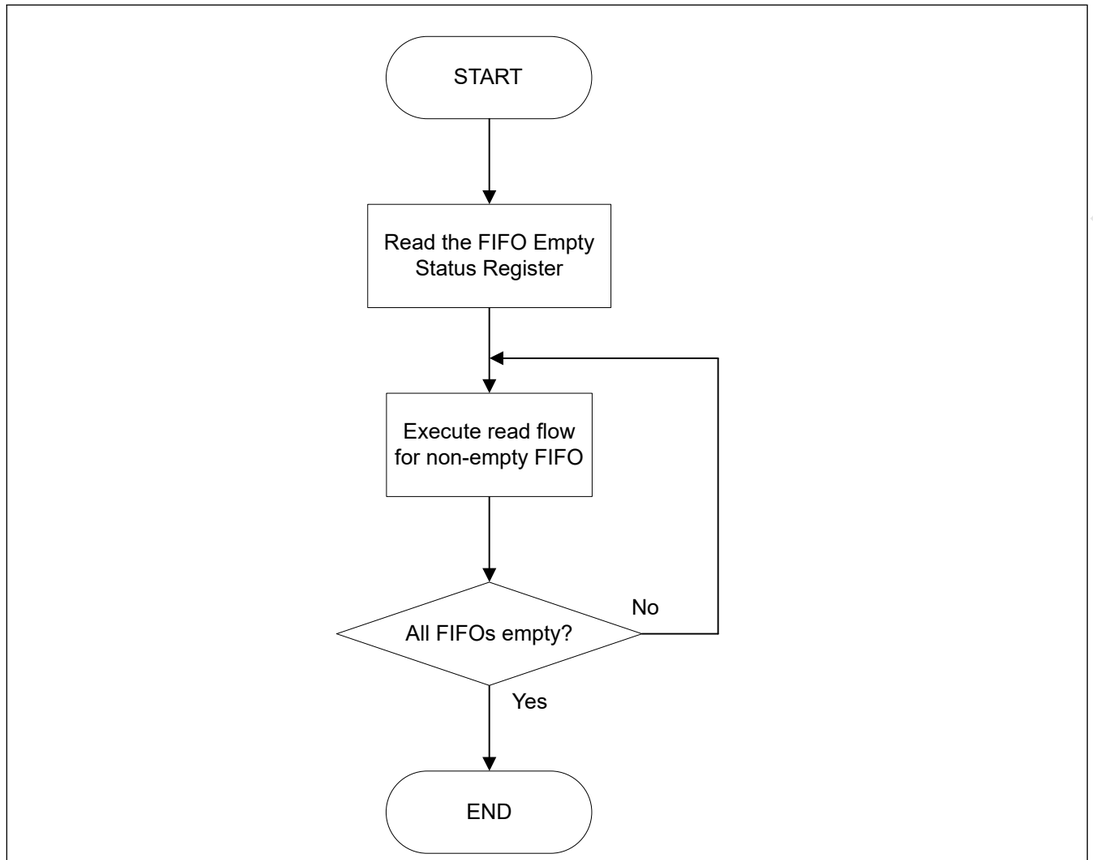


Figure 28.39 Access flow of FIFO buffer message (example for polling case)

如果在FIFO消息计数与FIFO深度匹配（FIFO满状态）时将新消息存储到FIFO，则
FIFO消息丢失标志被设置，新消息丢失（不会覆盖已存储的消息）。

可以将适当的值配置为警告级别，以在FIFO满情况发生之前生成中断，以避免由于溢出情况而丢失消息。

Note: 消息丢失只能在RX模式下由CAN设置，并且在CPU过载时不设置标志
FIFO buffers.

RXFIFO缓冲区和配置为RX模式的通用FIFO缓冲区可以通过清除
RXFIFO配置控制寄存器和通用FIFO中的CFDRFCCa.RFE或CFDCFCC.CFE位
Configuration/Control Registers.

当CFDRFCCa.RFE或CFDCFCC.CFE位清零时，FIFO的报文读写指针被清零，不再处于活动状态。因此，FIFO缓冲区中的所有消息都将丢失，并且无法将更多消息存储到FIFO中。

当RXFIFO缓冲区或配置为RX模式的通用FIFO缓冲区分配为DMA通道时，软件不应访问该FIFO缓冲区的FIFO访问寄存器或将0xFF写入FIFO指针控制寄存器（CFDCFPCTR.CFPC或CFDRFPCTRa.RFPC）.这可能导致意外的FIFO消息递减。DMA通道自动控制FIFO递减。

Note: 如果为FIFO缓冲区设置了中断标志，然后禁用了FIFO，则不会自动清除中断标志。在禁用FIFO之前应清除中断标志。

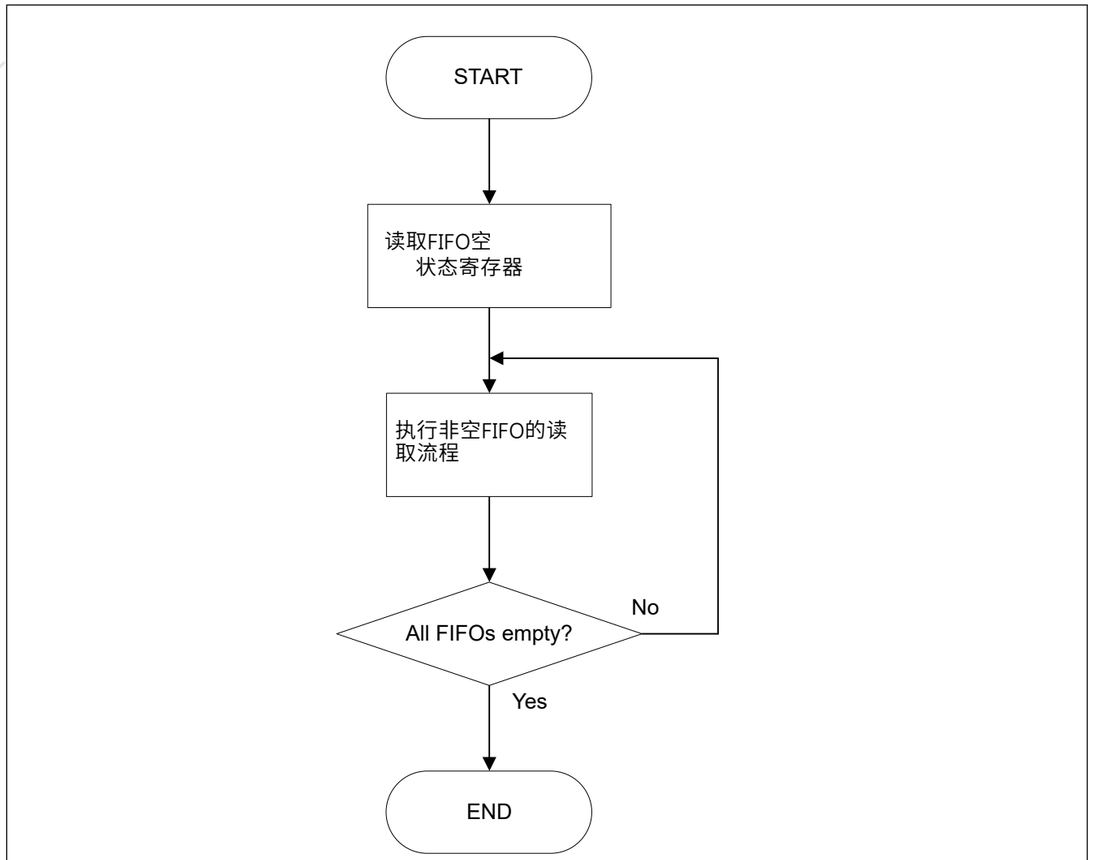


Figure 28.39 FIFO缓冲报文的访问流程（以轮询为例）

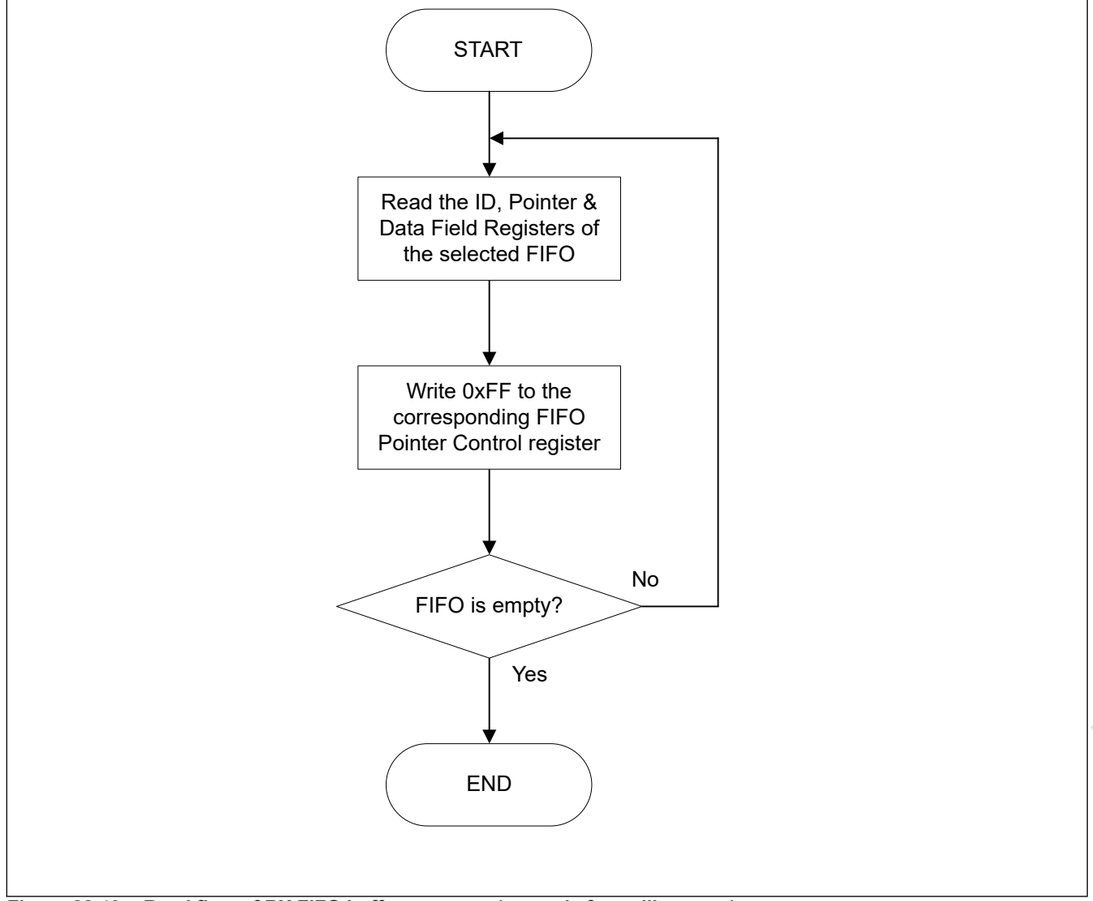


Figure 28.40 Read flow of RX FIFO buffer message (example for polling case)

Note: When the next frame is received before clearing the completion interrupt flag of reception, the completion interrupt of reception is not set again.

Even when an interruption flag is cleared after the completion processing of reception, the already received interrupt flag is not set.

It is necessary to perform the completion processing of reception even before the next completion of frame reception, and to clear an interruption flag.

When processing does not meet the condition, after checking that receiving data is empty, interrupt flag is cleared and it checks that receiving data is empty again.

28.8.1.3 Timestamp

The timestamp counter is a free-running counter that can be used to check reception time of an incoming message or transmission time of successful transmitted messages. The Timestamp counter value is captured based on the CFDGFDCFG.TSCCFG[1:0] configuration (at the sample point of start of frame, point in time when the frame is valid, or for CANFD frames also at the sample point of the RES bit). For reception, it is stored together with the message ID and data into the target RX message buffer or RX FIFO.

For transmit message, the timestamp counter value is stored as part of the TX History List entry.

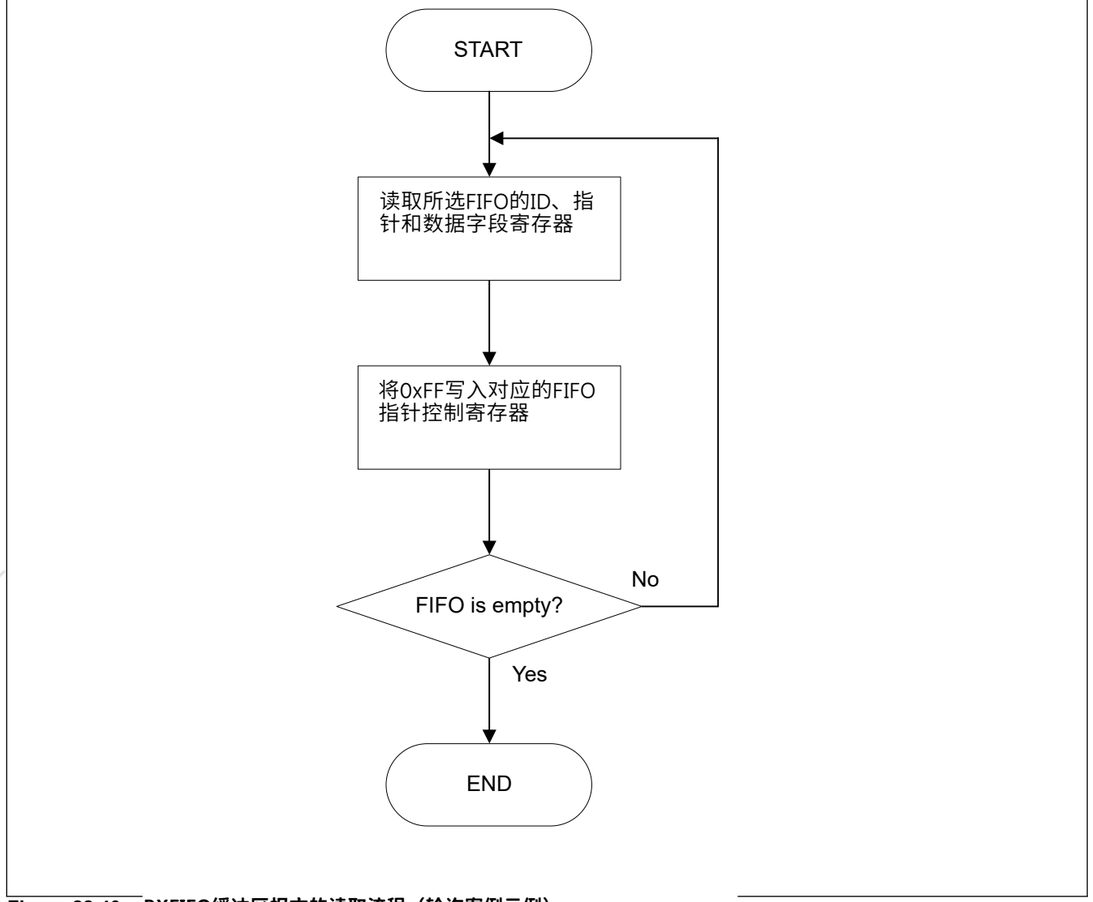


Figure 28.40 RXFIFO缓冲区报文的读取流程（轮询案例示例）

Note: 在清除接收完成中断标志之前接收到下一帧时，不再设置接收完成中断。

即使在接收完成处理后清除中断标志，已接收中断标志也不会置位。

甚至在下一次帧接收完成之前也需要执行接收完成处理，并清除中断标志。

当处理不满足条件时，检查接收数据为空后，清除中断标志，再次检查接收数据是否为空。

28.8.1.3 Timestamp

时间戳计数器是一个自由运行的计数器，可用于检查传入消息的接收时间或成功传输消息的传输时间。Timestamp计数器值是根据CFDGFDCFG.TSCCFG[1:0]配置捕获的（在帧开始的采样点、帧有效的时间点，或者对于CANFD帧也在RES位的采样点）。对于接收，它与消息ID和数据一起存储到目标RX消息缓冲区或RXFIFO中。

对于发送消息，时间戳计数器值存储为TX历史列表条目的一部分。

The counter can be clocked with the peripheral clock or with the CAN channel bit timing clock. The counter source clock can be configured with the CFDGCFG.TSSS bit of the Global Configuration Register. If this bit is 0, the peripheral clock is used. If the bit is 1, the selected CAN channel bit time clock is used.

The channel selection is performed with the CFDGCFG.TSBTCS bit of the Global Configuration Register.

Care must be taken when using selected CAN channel bit time clock as the clock source. When entering Channel Halt mode or Channel Reset node, for this channel, the timestamp counter is stopped. For other CAN channels, the timestamp counter value is not updated.

If peripheral clock is selected as the timestamp counter clock source, Channel modes do not affect the timestamp counter function.

The source clock for the timestamp counter can be divided by a factor defined by the CFDGCFG.TSP bits (timestamp prescaler) in the Global Configuration Register.

The timestamp counter can be reset to 0x0000 with the CFDGCTR.TSRST bit (timestamp reset).

28.8.2 Transmission

There are several possible transmission configurations:

- Normal transmission
- FIFO transmission
- TX Queue transmission
  A fixed number of transmission message buffers (4 TX message buffers) are dedicated. These message buffers are only used for transmission and cannot be configured for reception.
  Additionally transmission from TX Queue or Common FIFO in TX mode can be configured in the following way (see Figure 28.41):
  – TX Queue: Up to four transmission message buffers can be grouped to form a TX Queue with a common access window.
    Upper transmission message buffers are used to form the TXQ.
    TXQ has an access window.
    • TXQ is transmission Message Buffer 0.
- Common FIFO (TX mode): Common FIFO in TX mode is linked to a dedicated channel.
  Channel has a fixed number of one Common FIFO assigned to it. Within the channel, a Common FIFO configured in TX mode, can be freely linked (assigned) between 0 and 3 transmission message buffers (only one FIFO to one transmission message buffer).
  The Common FIFO buffer then replaces the transmission message buffer linked to it.
  Transmission Control and Status registers of these transmission message buffers should not be used.

See Figure 28.29 for information about Common FIFO buffer assignment to related channel.

Note: Common FIFO buffer should not be linked to TX message buffers that are already part of a TX Queue.

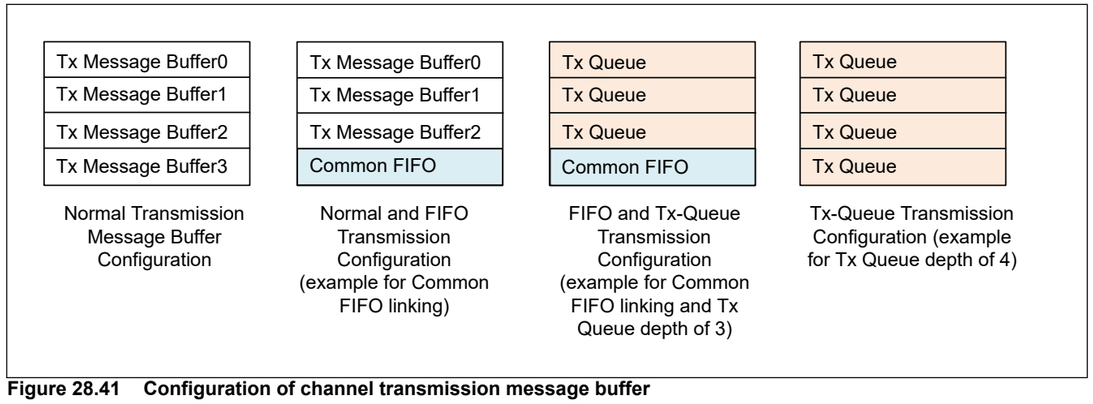


Figure 28.41 Configuration of channel transmission message buffer

计数器可以使用外设时钟或CAN通道位定时时钟进行计时。计数器源时钟可以通过全局配置寄存器的CFDGCFG.TSSS位进行配置。如果该位为0，则使用外设时钟。如果该位为1，则使用选定的CAN通道位时钟。

通道选择通过全局配置寄存器的CFDGCFG.TSBTCS位执行。

使用选定的CAN通道位时钟作为时钟源时必须小心。当进入ChannelHalt模式或ChannelReset节点时，对于该通道，时间戳计数器停止。对于其他CAN通道，时间戳计数器值不会更新。

如果选择外设时钟作为时间戳计数器时钟源，通道模式不影响时间戳计数器功能。

时间戳计数器的源时钟可以除以全局配置寄存器中的CFDGCFG.TSP位（时间戳预分频器）定义的因子。

时间戳计数器可通过CFDGCTR.TSRST位（时间戳复位）复位为0x0000。

28.8.2 Transmission

有几种可能的传输配置：

●正常传输

- FIFO transmission

●TX队列传输
固定数量的传输消息缓冲区（4个TX消息缓冲区）是专用的。这些消息缓冲区仅用于传输，不能配置为接收。
此外，在TX模式下从TXQueue或CommonFIFO进行的传输可以通过以下方式进行配置（请参阅

Figure 28.41):

TXQueue：最多可以将四个传输消息缓冲区分组以形成具有公共访问窗口的TXQueue。上层传输消息缓冲区用于形成TXQ。

TXQ有一个访问窗口。

- TXQ是传输消息缓冲区0。

●CommonFIFO（TX模式）：TX模式下的CommonFIFO链接到一个专用通道。
通道有一个固定数量的分配给它的通用FIFO。在通道内，配置了一个通用FIFO TX模式，可以在0到3个传输报文缓冲区（只有1个FIFO到1个传输报文缓冲区）之间自由链接（分配）。通用FIFO缓冲区然后替换链接到它的传输消息缓冲区。

不应使用这些传输消息缓冲区的传输控制和状态寄存器。

有关分配给相关通道的通用FIFO缓冲区的信息，请参见图28.29。

Note: 公共FIFO缓冲区不应链接到已经是TX队列一部分的TX消息缓冲区。

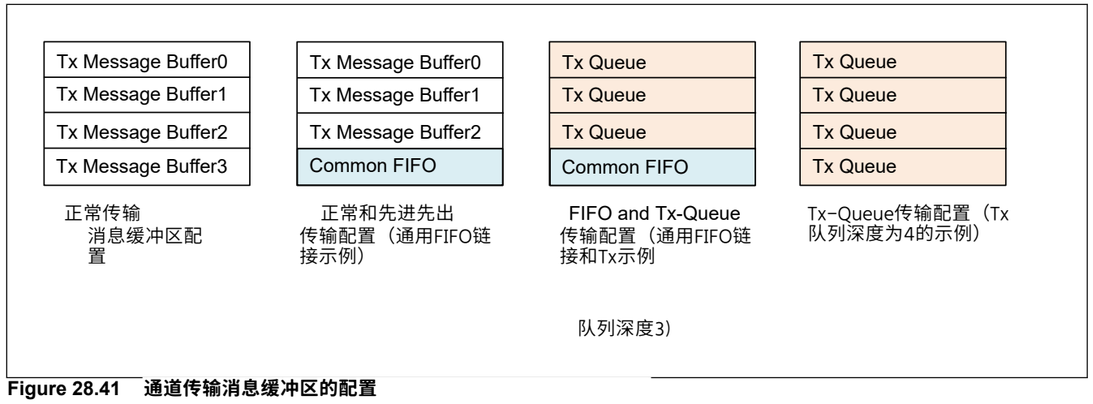


Figure 28.41 通道传输消息缓冲区的配置

28.8.2.1 Transmission Priority

If two or more transmission message buffers of a channel are configured for transmission, then the transmission priority in the CANFD module can be selected from the following two modes:

- CAN ID priority
- Message buffer number priority.

The transmission priority mode is common for all message buffers. It can be configured with the CFDGCFG.TPRI bit in the Global Configuration Register.

For message buffer number priority transmission, the smallest message buffer number with transmission request has the highest priority for transmission. This also includes the TX message buffers linked to the Common FIFO buffer configured in TX mode.

However, message buffer number priority should not be used if TX Queue is enabled.

For CAN ID priority transmission, ID priority complies with the CAN bus arbitration rule (as specified in ISO 11898-1 specification). All TX message buffers can enter the ID priority comparison for message buffers configured for transmission. This also includes the TX message buffers linked to the Common FIFO buffer configured in TX mode and includes the TX Queue message buffers.

If the ID of two or more message buffers is the same, then the smaller message buffer number has higher priority for transmission.

Note: For Common FIFO buffer configured in TX mode, only the message currently being pointed to by the FIFO read pointer can be included in the transmission arbitration.

If the message is being transmitted from the FIFO, then the next pending message within the same FIFO is considered in the transmission arbitration.

In contrast to this, all transmission message buffers of a TX Queue participate in internal transmission arbitration.

Figure 28.42 shows the transmission configuration flow.

28.8.2.1 传输优先级

如果配置了一个通道的两个或多个传输报文缓冲区进行传输，则CANFD模块中的传输优先级可以从以下两种模式中选择：

●CANID优先级

●消息缓冲区编号优先级。

传输优先模式对所有消息缓冲区都是通用的。它可以用CFDGCFG.TPRI位在全局配置寄存器。

对于消息缓冲区号优先传输，具有传输请求的最小消息缓冲区号具有最高传输优先级。这还包括链接到在TX模式下配置的CommonFIFO缓冲区的TX消息缓冲区。

但是，如果启用了TXQueue，则不应使用消息缓冲区编号优先级。

对于CANID优先级传输，ID优先级符合CAN总线仲裁规则（在ISO11898-1规范中指定）。所有TX报文缓冲区都可以进入配置为传输的报文缓冲区的ID优先级比较。这还包括链接到在TX模式下配置的CommonFIFO缓冲区的TX消息缓冲区，并包括TXQueue消息缓冲区。

如果两个或多个消息缓冲区的ID相同，则较小的消息缓冲区号具有较高的传输优先级。

Note: 对于配置为TX模式的CommonFIFO缓冲区，只有FIFO读指针当前指向的报文可以包含在传输仲裁中。

如果消息是从FIFO传输的，则在传输仲裁中考虑同一FIFO中的下一个待处理消息。

与此相反，TXQueue的所有传输消息缓冲区都参与内部传输仲裁。

图28.42显示了传输配置流程。

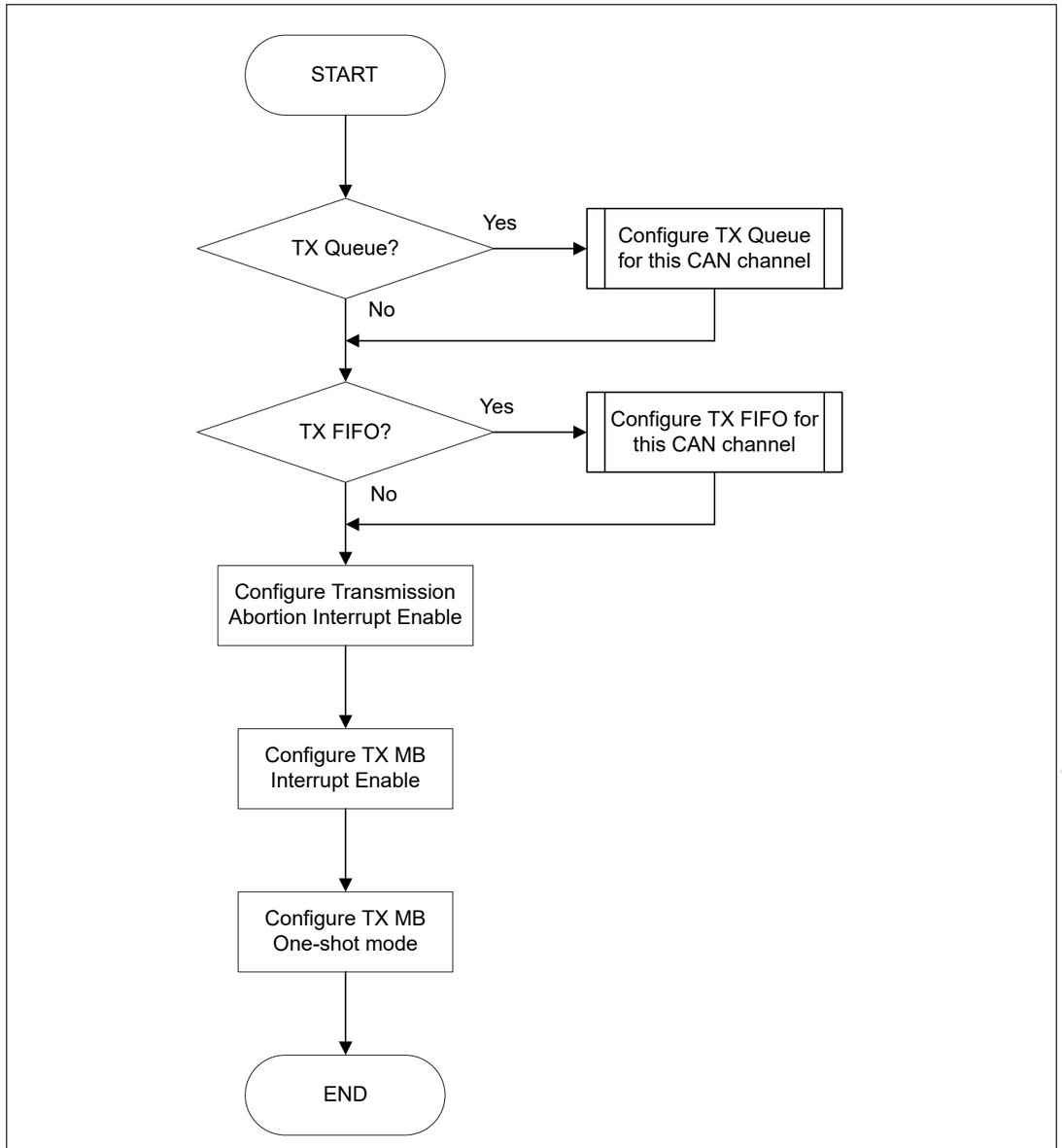


Figure 28.42 Flow for transmission configuration

28.8.2.2 Normal Transmission

Each transmission message buffer has two modes of message transmission:

1. Regular transmission mode
   If the message buffer is placed in regular transmission mode, the data frame or remote frame set in that message buffer can be transmitted.
   Completion of regular transmission can be checked through the related TX Message Buffer Transmission Result flag bits (CFDTMSTSj.TMTRF) in the TX Message Buffer Status Registers. These bits are set to 10b or 11b when the regular transmission is successful.

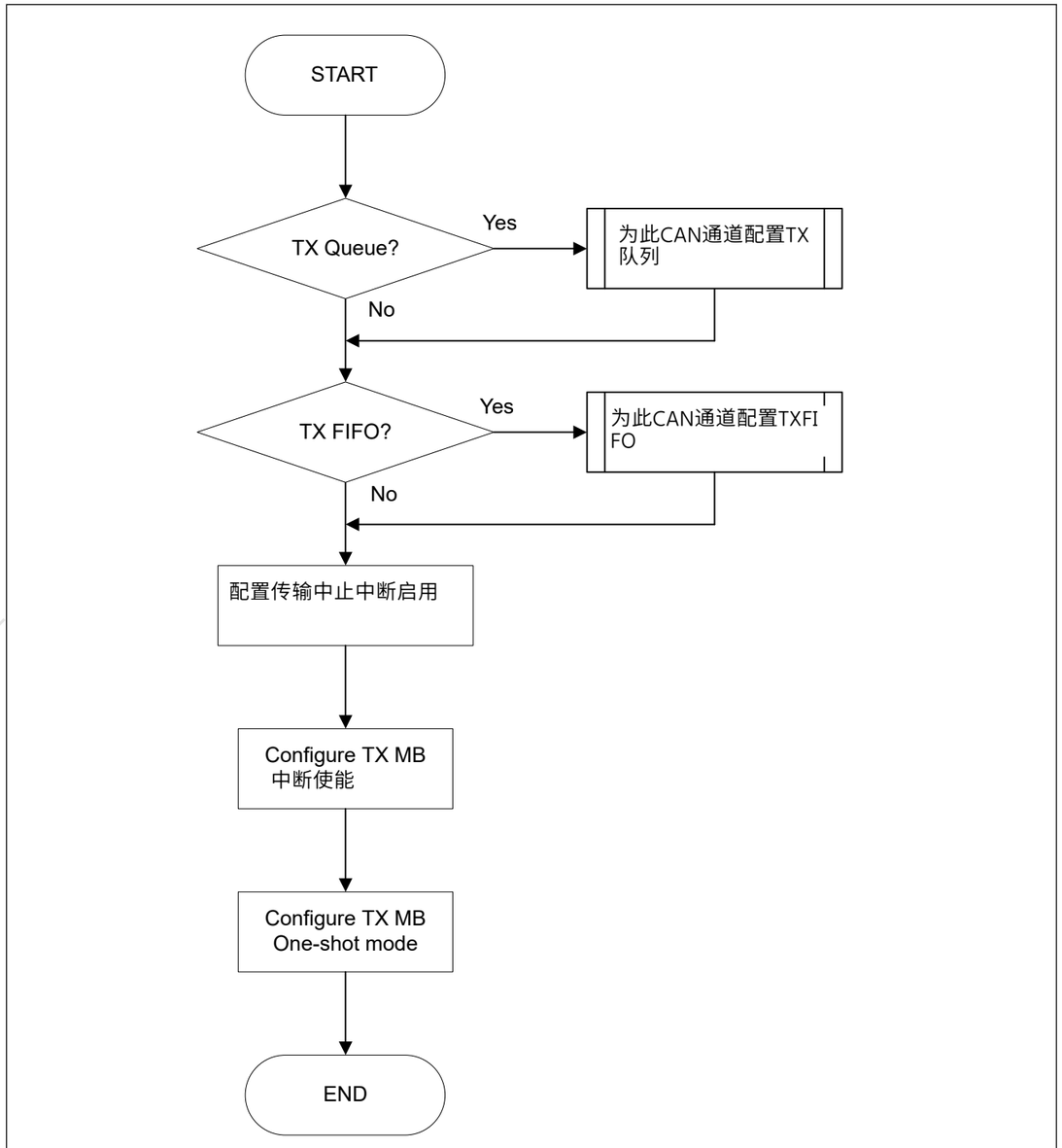


Figure 28.42 传输配置流程

28.8.2.2 正常传输

每个传输消息缓冲区有两种消息传输模式：

1.常规传输方式
如果将消息缓冲区置于常规传输模式，则可以传输该消息缓冲区中设置的数据帧或远程帧。可以通过TX报文缓冲区状态寄存器中相关的TX报文缓冲区传输结果标志位(CFDTMSTSj.TMTRF)来检查是否完成了定期传输。当常规传输成功时，这些位设置为10b或11b。

When arbitration is lost or an error occurs, message transmission is further attempted if no transmission abort request is set for this transmission message buffer.
New internal transmission arbitration for this channel is performed for all message buffers with transmission request.

2. One-shot transmission mode

When the CFDTMCi.TMOM bit of the TX Message Buffer Control Registers is set for a transmission message buffer, the message buffer is placed in One-shot transmission mode and attempts to transmit a message only once.

Completion of One shot transmission can be checked through the related TX Message Buffer Transmission Result Flag bits (CFDTMSTSj.TMTRF) in the TX Message Buffer Status Registers. The CFDTMSTSj.TMTRF bits are set to 10b or 11b when One-shot transmission is successful.

The CFDTMSTSj.TMTRF bits are set to 01b when arbitration is lost or an error occurs during transmission of the related message buffer.

Additional message transmission is not attempted in this case.

The regular transmission request procedure after a configuration is shown in Figure 28.43.

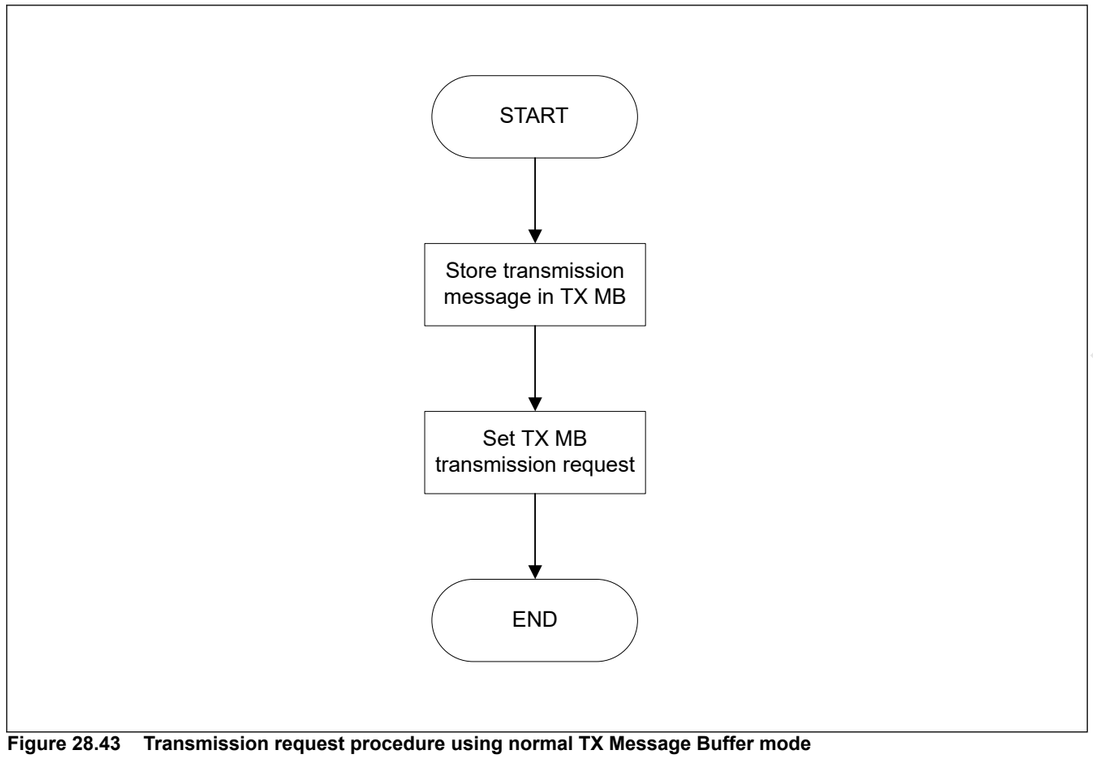


Figure 28.43 Transmission request procedure using normal TX Message Buffer mode

(1) Setting for TX Message Buffer Control Register

Table 28.27 shows configuration of a normal CAN transmission mode.

Table 28.27 Configuration of CAN transmission mode (1 of 2)

Transmission request CFDTMCi.TMTR	Transmission abort request CFDTMCi.TMTAR	One-shot enable CFDTMCi.TMOM	Communication activity
0	0	0	Message buffer disabled
0	0	1	Message buffer disabled

当仲裁丢失或发生错误时，如果没有为此发送消息缓冲区设置发送中止请求，则进一步尝试发送消息。该通道的新内部传输仲裁针对所有具有传输请求的消息缓冲区执行。

2.一键传输模式

当TX报文缓冲区控制寄存器的CFDTMCi.TMOM位设置为发送报文缓冲区时，报文缓冲区被置于一次性发送模式，并且仅尝试发送一次报文。

可以通过TX报文缓冲区状态寄存器中的相关TX报文缓冲区传输结果标志位(CFDTMSTSj.TMTRF)检查Oneshot传输是否完成。当One-shot传输成功时，CFDTMSTSj.TMTRF位设置为10b或11b。

当仲裁丢失或在相关消息缓冲区的传输过程中发生错误时，CFDTMSTSj.TMTRF位设置为01b。

在这种情况下，不会尝试额外的消息传输。

配置后的常规传输请求流程如图28.43所示。

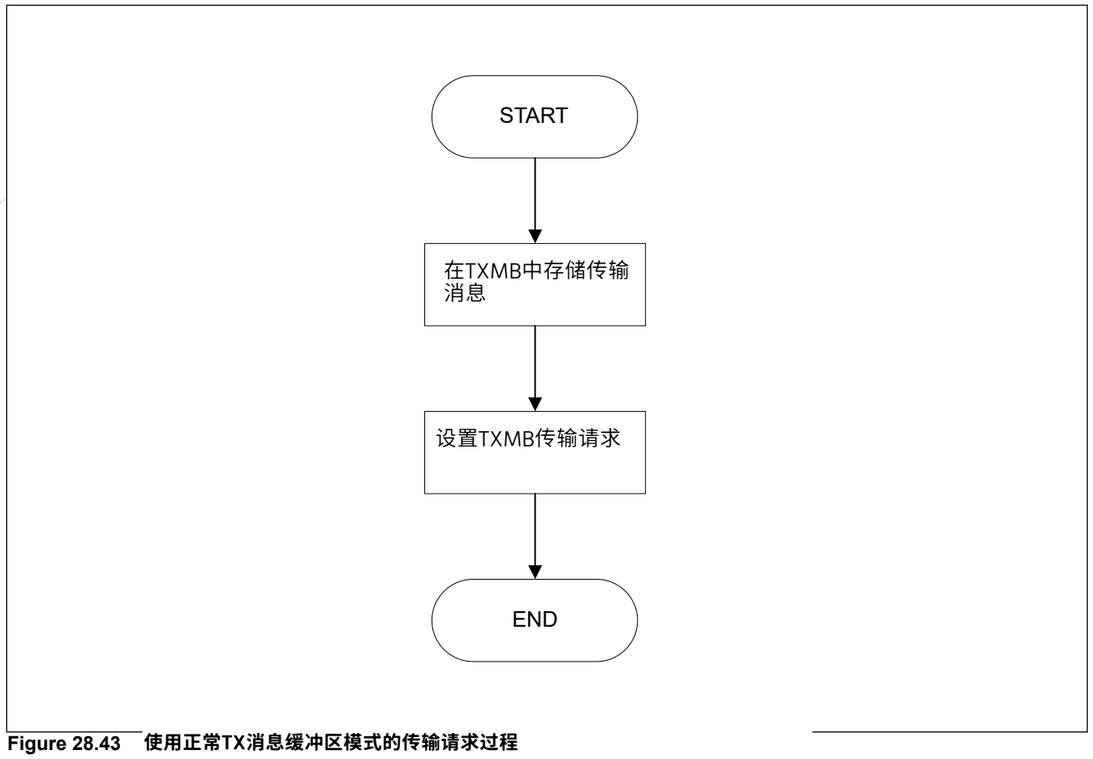


Figure 28.43 使用正常TX消息缓冲区模式的传输请求过程

(1) TX报文缓冲区控制寄存器的设置

表28.27显示了普通CAN传输模式的配置。

Table 28.27 CAN传输模式的配置（1of2）

传输请求 CFDTMCi.TMTR	传输中止请求 CFDTMCi.TMTAR	One-shot enable CFDTMCi.TMOM	通信活动
0	0	0	消息缓冲区已禁用
0	0	1	消息缓冲区已禁用

Table 28.27 Configuration of CAN transmission mode (2 of 2)

Transmission request CFDTMCi.TMTR	Transmission abort request CFDTMCi.TMTAR	One-shot enable CFDTMCi.TMOM	Communication activity
1	0	0	Configured as a transmission message buffer for a data frame or a remote frame
1	0	1	Configured as a one-shot transmission message buffer for a data frame or a remote frame
1	1	0	Transmission abort requested
1	1	1	One-shot transmission abort requested

The configuration bits can be configured in the TX Message Buffer Control Registers.

Figure 28.44 shows timings for successful transmission for two message buffers.

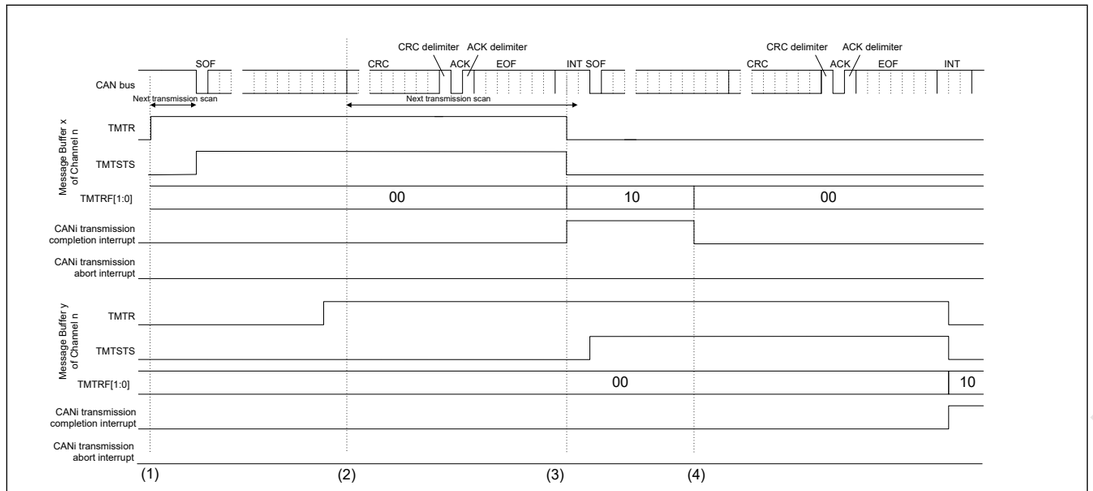


Figure 28.44 Timing of request and flag bits for successful transmission

1. If the CFDTMCi.TMTR bit in the TX Message Buffer Control Registers is set in the bus idle state, the message buffer scanning procedure determines the highest priority message buffer for transmission.
   When the transmission message buffer is determined, the CFDTMSTSj.TMTSTS bit in the related TX Message Buffer Status Registers is set (transmitting/transmitter), and CAN channel starts the transmission *1.
2. At the first bit of CRC, the transmission scanning procedure starts for the next possible transmission when pending transmission requests exist.
3. If the message has been successfully transmitted, the CFDTMSTSj.TMTRF[1:0] bits in the corresponding TX Message Buffer Status Registers are set to 10b and CFDTMSTSj.TMTSTS and the CFDTMCi.TMTR bits are cleared.
   When the TMIE bit in the TX Message Buffer Interrupt Enable Configuration Registers is set (interrupt enabled), the CAN successful transmission interrupt request is generated.
   To clear the related interrupt line, clear the CFDTMSTSj.TMTRF flag bits.
4. Before starting the next transmission, clear the CFDTMSTSj.TMTRF bits. Load the next message in the transmission message buffer and set the CFDTMCi.TMTR bit again.
   CFDTMCi.TMTR bit cannot be set again before CFDTMSTSj.TMTRF[1:0] bits are cleared.

Note 1. If arbitration is lost after the CAN channel starts the transmission, the CFDTMSTSj.TMTSTS bit is cleared.
The transmission scanning procedure is performed again to search for the highest priority transmission message buffer from the beginning of the first CRC bit.
If an error occurs either during transmission or following the loss of arbitration, then during the error frame, the transmission scanning procedure is performed again to search for the highest priority transmission message buffer.

Table 28.27 CAN传输模式的配置（2of2）

传输请求 CFDTMCi.TMTR	传输中止请求 CFDTMCi.TMTAR	One-shot enable CFDTMCi.TMOM	通信活动
1	0	0	配置为数据帧或远程帧的传输消息缓冲区
1	0	1	配置为数据帧或远程帧的一次性传输消息缓冲区
1	1	0	请求传输中止
1	1	1	请求单发传输中止

配置位可以在TX报文缓冲区控制寄存器中进行配置。

图28.44显示了成功传输两个消息缓冲区的时序。

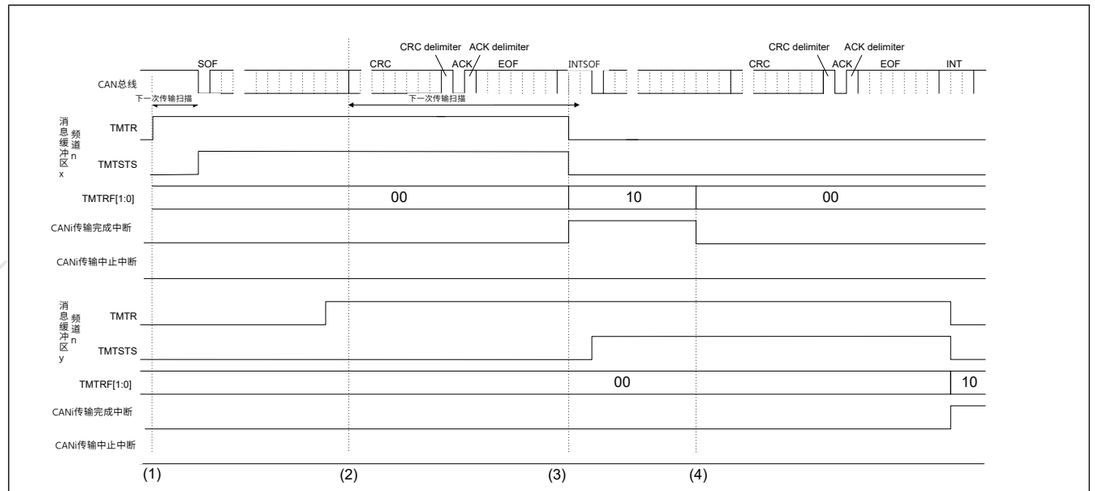


Figure 28.44 成功传输的请求和标志位的时序

1.如果TX报文缓冲区控制寄存器中的CFDTMCi.TMTR位在总线空闲状态下设置，报文缓冲区扫描程序会确定发送的最高优先级报文缓冲区。当确定发送消息缓冲区时，相关的TX消息缓冲区中的CFDTMSTSj.TMTSTS位

设置状态寄存器（发送发送器），CAN通道开始发送*1。

2.在CRC的第一位，当存在未决的传输请求时，传输扫描程序开始为下一个可能的传输。

3.如果报文已成功发送，则相应的TX报文缓冲区状态寄存器中的CFDTMSTSj.TMTRF[1:0]位设置为10b，CFDTMSTSj.TMTSTS和CFDTMCi.TMTR位清零。

当TX报文缓冲区中断允许配置寄存器中的TMIE位置位（允许中断）时，
CAN成功传输中断请求产生。
要清除相关中断线，请清除CFDTMSTSj.TMTRF标志位。

4.在开始下一次传输之前，清除CFDTMSTSj.TMTRF位。将下一条消息加载到传输消息缓冲区中并再次设置CFDTMCi.TMTR位。在清除CFDTMSTSj.TMTRF[1:0]位之前，CFDTMCi.TMTR位不能再次置位。

注1.如果CAN通道开始传输后仲裁丢失，CFDTMSTSj.TMTSTS位被清零。

再次执行传输扫描程序，以从第一个CRC位的开头搜索最高优先级的传输消息缓冲区。

如果在传输过程中或仲裁失败后发生错误，则在错误帧期间，再次执行传输扫描程序以搜索最高优先级的传输消息缓冲区。

Note: The setting point of CFDTMSTSj.TMTSTS is not always fixed at the start of the SOF. It may be delayed up to the start of the standard ID due to the synchronization logic implemented for the PLL bypass.

Figure 28.45 shows timings for transmission abort for two message buffers.

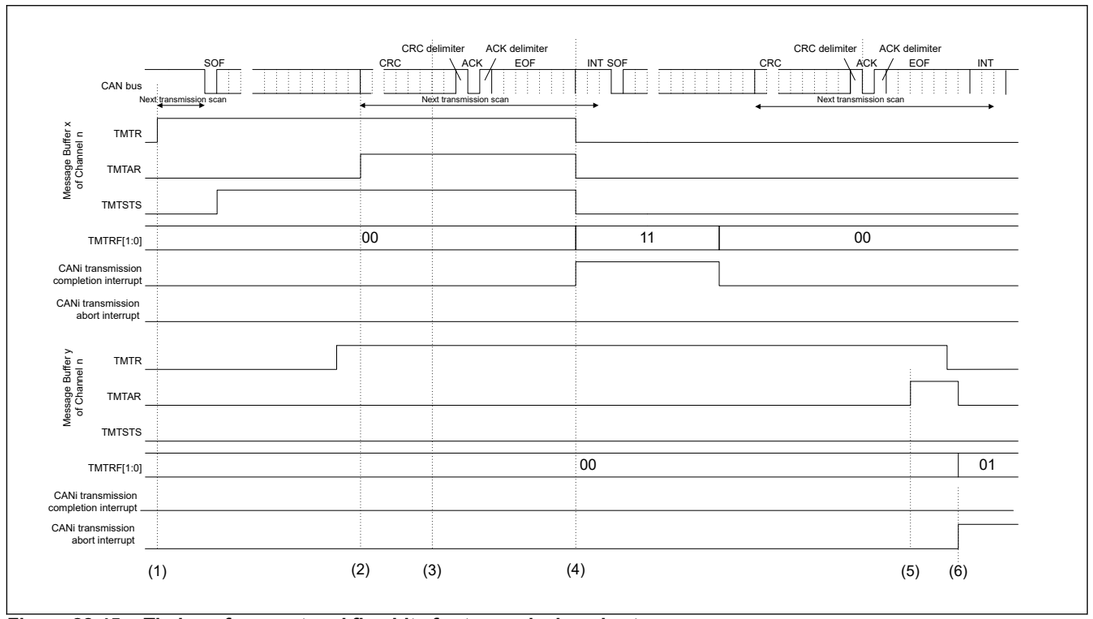


Figure 28.45 Timing of request and flag bits for transmission abort

1. If the CFDTMCi.TMTR bit in the TX Message Buffer Control Registers is set in the bus idle state, the message buffer scanning procedure determines the highest priority message buffer for transmission.
   When the transmission message buffer is determined, the CFDTMSTSj.TMTSTS bit in the TX Message Buffer Status Registers is set (transmitting/transmitter), and CAN channel starts the transmission*1.
2. If the CFDTMCi.TMTAR bit is set when the related message buffer is already selected for transmission or currently transmitting, the message is not aborted, if no error occurs or arbitration is lost.
3. At the first CRC bit, the transmission scanning procedure starts for the next transmission. In this example, timing chart message buffer y is not selected as the next transmission message buffer.
4. If the message has been successfully transmitted, the CFDTMSTSj.TMTRF[1:0] bits in the corresponding TX Message Buffer Status Registers are set to 11b and the CFDTMSTSj.TMTSTS and CFDTMCi.TMTR bits are cleared.
   When the TMIE bit in the TX Message Buffer Interrupt Enable Configuration Registers is set (interrupt enabled), the CAN successful transmission interrupt request is generated.
   To clear the related interrupt line, clear the CFDTMSTSj.TMTRF[1:0] bits.
5. Another CAN node is transmitting on the CAN bus (CFDTMSTSj.TMTSTS is not set). If the CFDTMCi.TMTAR bit is set when the related channel is under transmission scan, the transmission request cannot be cleared.
6. After internal processing time, the transmission is aborted and the CFDTMSTSj.TMTRF[1:0] bits are set to 01b.
   If the message buffer is not transmitting or selected as the next transmission message buffer or under transmit scan, then the abort is immediately accepted and the corresponding CFDTMSTSj.TMTRF[1:0] bits in the TX Message Buffer Status Registers are set to 01b.
   In addition, CFDTMCi.TMTR, and CFDTMCi.TMTAR bits are cleared automatically.
   When the transmission abort interrupt enable TAIE bit of the related Channel Control Register is set then an interrupt is generated for successful transmission abort.
   To clear the related interrupt line the CFDTMSTSj.TMTRF[1:0] bits have to be cleared.

Note 1. If arbitration is lost after the CAN channel starts the transmission, the CFDTMSTSj.TMTSTS bit is cleared.

Note: CFDTMSTSj.TMTSTS的设定点并不总是固定在SOF的开始处。由于为PLL旁路实现的同步逻辑，它可能会延迟到标准ID的开始。

图28.45显示了两个消息缓冲区的传输中止时序。

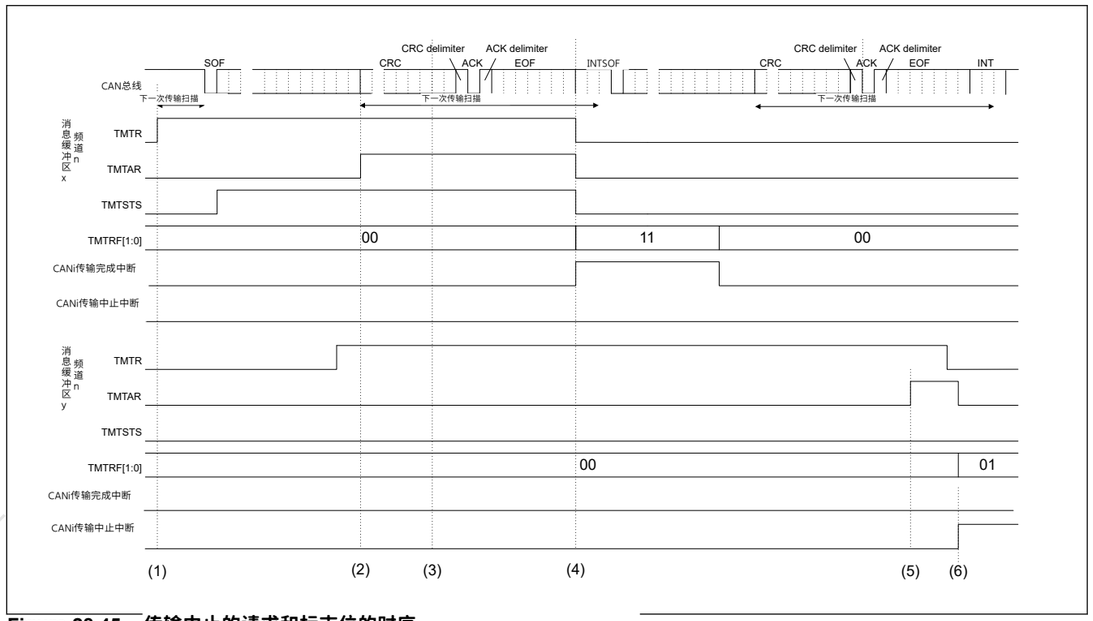


Figure 28.45 传输中止的请求和标志位的时序

1.如果TX报文缓冲区控制寄存器中的CFDTMCi.TMTR位在总线空闲状态下设置，报文缓冲区扫描程序会确定发送的最高优先级报文缓冲区。当确定发送消息缓冲区时，TX消息缓冲区状态中的CFDTMSTSj.TMTSTS位

设置寄存器（发送发送器），CAN通道开始发送*1。

2.如果CFDTMCi.TMTAR位在相关报文缓冲区已被选择发送或正在发送时被设置，如果没有错误发生或仲裁丢失，则不会中止报文。

3.在第一个CRC位，传输扫描程序开始下一次传输。在这个例子中，时序图消息缓冲区y没有被选为下一个传输消息缓冲区。

4.如果报文已成功发送，则相应的TX报文缓冲区状态寄存器中的CFDTMSTSj.TMTRF[1:0]位设置为11b，CFDTMSTSj.TMTSTS和CFDTMCi.TMTR位清零。
当TX报文缓冲区中断允许配置寄存器中的TMIE位置位（允许中断）时，
CAN成功传输中断请求产生。
要清除相关中断线，请清除CFDTMSTSj.TMTRF[1:0]位。

5.另一个CAN节点正在CAN总线上传输（CFDTMSTSj.TMTSTS未设置）。如果CFDTMCi.TMTAR位在相关通道处于发送扫描状态时被置位，则发送请求不能被清除。

6.内部处理时间过后，发送中止，CFDTMSTSj.TMTRF[1:0]位设置为01b。
如果报文缓冲区未发送或未选择作为下一个发送报文缓冲区或正在发送扫描，则立即接受中止并将TX报文缓冲区状态寄存器中的相应CFDTMSTSj.TMTRF[1:0]位设置为01b。

此外，CFDTMCi.TMTR和CFDTMCi.TMTAR位会自动清零。
当相关通道控制寄存器的发送中止中断使能位TAIE置位时，将产生中断以成功发送中止。要清除相关的中断线，必须清除CFDTMSTSj.TMTRF[1:0]位。

注1.如果CAN通道开始传输后仲裁丢失，CFDTMSTSj.TMTSTS位被清零。

The transmission scanning procedure is performed again to search for the highest priority transmission message buffer from the beginning of the first CRC bit.

If an error occurs, either during transmission, or following the loss of arbitration, then during the error frame, the transmission scanning procedure is performed again to search for the highest priority transmission message buffer.

28.8.2.3 TX FIFO Transmission

One common FIFO buffer is assigned to CANFD module. The FIFO buffer can be linked to any normal TX message buffer position for this channel with the CFDCFCC.CFTML bits in the Common FIFO Configuration/Control Register if configured in TX mode.

When the transmission scan starts and the FIFO buffer corresponding to this TX message buffer is enabled, the relevant message in the FIFO buffer participates in the transmission scan.

Configuration of a TX message buffer linked to a FIFO buffer configured in TX mode should not be done.

(1) TX FIFO Operation

CAN messages can be written into the TX FIFO by writing to the corresponding FIFO Access registers.

When the value 0xFF is written into the corresponding FIFO Pointer Control Register, the message count of the related FIFO is incremented by 1.

Only write to the FIFO Pointer Control register after writing the complete message to the corresponding FIFO Access registers. If the message count matches the FIFO depth, the FIFO Full flag is set.

The oldest message in the TX FIFO is included in the scan for transmission by the corresponding CANFD module channel logic.

When a message is successfully transmitted from the TX FIFO, the message count value is decremented by 1. When all the messages from the FIFO are transmitted, the FIFO Empty flag is set.

The interrupt generation conditions for the TX FIFO buffer can be configured by configuring the CFDCFCC.CFIM bit in the corresponding Common FIFO Configuration/Control Register.

If CFDCFCC.CFIM bit is 0, then interrupt is generated when the last message is successfully transmitted from the TX FIFO buffer.

If CFDCFCC.CFIM bit is 1, then interrupt is generated for every successfully transmitted message from the TX FIFO buffer.

The Common FIFO can set interrupt when CAN frame transmission is complete.

The Common FIFO buffer configured in TX Mode can be disabled by clearing the CFDCFCC.CFE bit in the Common FIFO Configuration/Control Register. If this bit is cleared to 0, the FIFO Empty flag is set as follows:

- Immediately if the message from the TX FIFO is neither scheduled for the next transmission nor in transmission
- Following the transmission completion, the detection of an error on the CAN bus, loss of arbitration or transition to Channel or Global Halt mode if the transmission from the TX FIFO is already scheduled for transmission or already in transmission.

Note: The Common FIFO buffer is considered as disabled after clearing the CFDCFCC.CFE bit only when the Empty flag is set for the corresponding Common FIFO buffer.

Other possible messages pending from the TX FIFO are lost and their transmission must be requested again. Before CFDCFCC.CFE is set again, ensure that CFDCFSTS.CFEMP bit is set and that there are no pending abort from the TX FIFO.

When the CFDCFCC.CFE bit is cleared, the message read and write pointers of the FIFO are cleared and are no longer active. Therefore, all messages in the FIFO buffers are lost and no further message can be stored into the FIFO.

The FIFO transmission request procedure after configuration is shown in Figure 28.46.

再次执行传输扫描程序，以从第一个CRC位的开头搜索最高优先级的传输消息缓冲区。

如果在传输过程中或在仲裁失败之后发生错误，则在错误帧期间，再次执行传输扫描程序以搜索最高优先级的传输消息缓冲区。

28.8.2.3 TX FIFO Transmission

为CANFD模块分配了一个通用FIFO缓冲区。如果配置为TX模式，则FIFO缓冲区可以通过通用FIFO配置控制寄存器中的CFDCFCC.CFTML位链接到该通道的任何正常TX消息缓冲区位置。

当发送扫描开始并且与该TX报文缓冲区对应的FIFO缓冲区使能时，FIFO缓冲区中的相关报文参与发送扫描。

不应配置链接到在TX模式下配置的FIFO缓冲区的TX消息缓冲区。

(1) TX FIFO Operation

通过写入相应的FIFO访问寄存器，可以将CAN消息写入TXFIFO。

当值0xFF被写入对应的FIFO指针控制寄存器时，相关的报文计数
FIFO加1。

仅在将完整消息写入相应的FIFO访问寄存器后才写入FIFO指针控制寄存器。如果消息计数与FIFO深度匹配，则设置FIFO满标志。

TXFIFO中最旧的消息包含在相应CANFD模块通道逻辑的传输扫描中。

当一条消息从TXFIFO成功发送时，消息计数值减1。当FIFO中的所有消息都发送完毕时，FIFO空标志置位。

TXFIFO缓冲区的中断生成条件可以通过配置相应通用FIFO配置控制寄存器中的CFDCFCC.CFIM位来配置。

如果CFDCFCC.CFIM位为0，则当最后一条消息从TXFIFO缓冲区成功发送时，将产生中断。

如果CFDCFCC.CFIM位为1，则从TXFIFO缓冲区中成功发送的每个消息都会产生中断。

当CAN帧传输完成时，CommonFIFO可以设置中断。

在TX模式下配置的CommonFIFO缓冲区可以通过清除Common中的CFDCFCC.CFE位来禁用
FIFO配置控制寄存器。如果该位清0，FIFO空标志设置如下：

●如果来自TXFIFO的消息既没有安排下一次传输也没有在传输中，则立即执行

●传输完成后，检测到CAN总线错误、仲裁丢失或转换到
如果来自TXFIFO的传输已被安排传输或已在传输中，则为通道或全局暂停模式。

Note: 仅当为相应的CommonFIFO缓冲区设置Empty标志时，在清除CFDCFCC.CFE位后，CommonFIFO缓冲区才被视为禁用。

来自TXFIFO的其他可能未决消息丢失，必须再次请求它们的传输。前
再次设置CFDCFCC.CFE，确保设置了CFDCFSTS.CFEMP位并且没有来自TX的挂起中止
FIFO.

当CFDCFCC.CFE位清零时，FIFO的报文读写指针被清零，不再处于活动状态。因此，FIFO缓冲区中的所有消息都将丢失，并且无法将更多消息存储到FIFO中。

配置后的FIFO发送请求流程如图28.46所示。

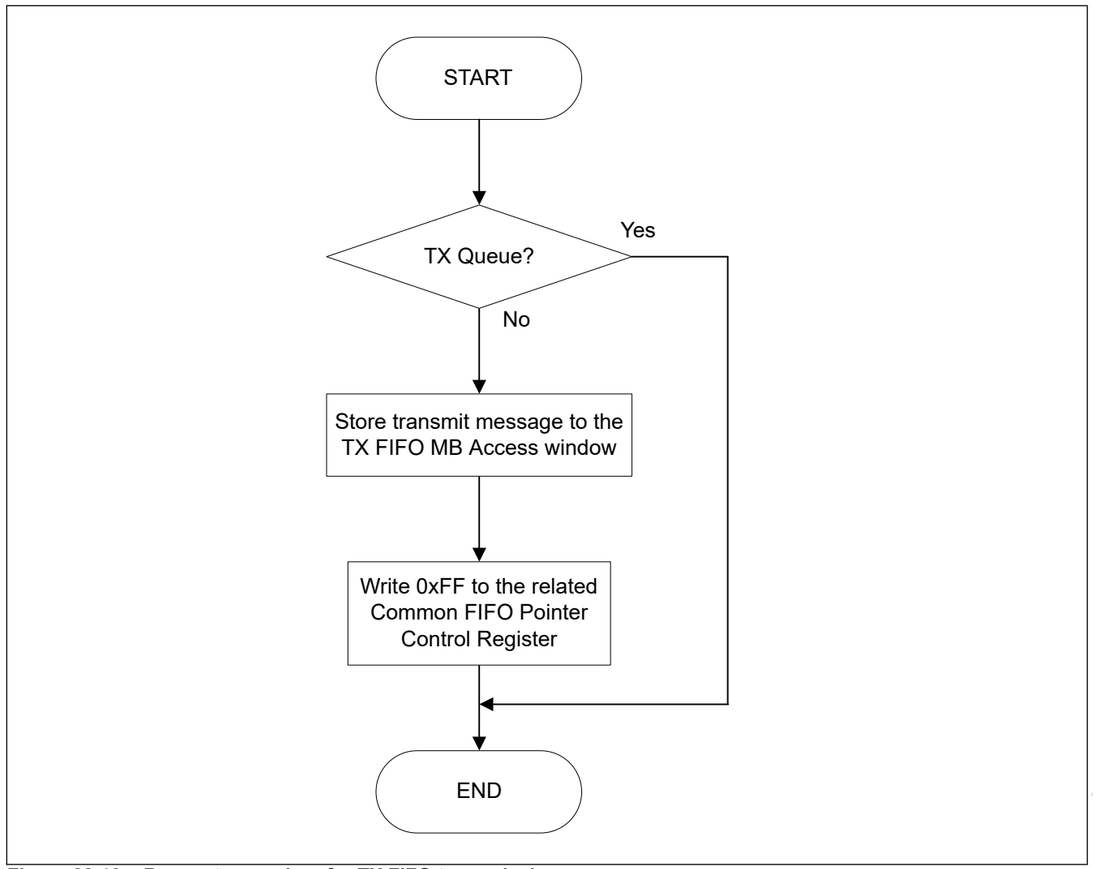


Figure 28.46 Request procedure for TX FIFO transmission

(2) Interval Timer for FIFO Transmission

For each Common FIFO in TX mode, it is possible to specify a delay between two consecutive messages that are configured for transmission from the same FIFO buffer. This delay is called interval time. This interval time starts after the first message has been successfully transmitted from the FIFO buffer after the CFDCFCC.CFE bit is set.

When the Common FIFO in TX mode is enabled, the first message is transmitted without considering this interval time.

The interval timer stops counting when:

- FIFO is disabled by clearing the CFDCFCC.CFE bit.
- CAN channel is in CH_RESET mode.

The interval time is specified by the CFDCFCC.CFITT value from 0 to 255 timer units in the Common FIFO Configuration/ Control Register.

The timer unit can be defined based on two different source clocks for the interval timer. To disable the interval timer for FIFO transmission, select a value of 0.

The timer source can be selected with the configuration bit CFITSS in the Common FIFO Configuration/Control Register.

If CAN channel bit time clock is configured as the clock source, and the CAN channel enters CH_HALT, CH_RESET, or CH_SLEEP mode, the interval timer is stopped for that channel.

If peripheral clock is selected as the interval timer clock source, the interval timer is stopped only when the CAN channel is in CH_RESET or CH_SLEEP mode.

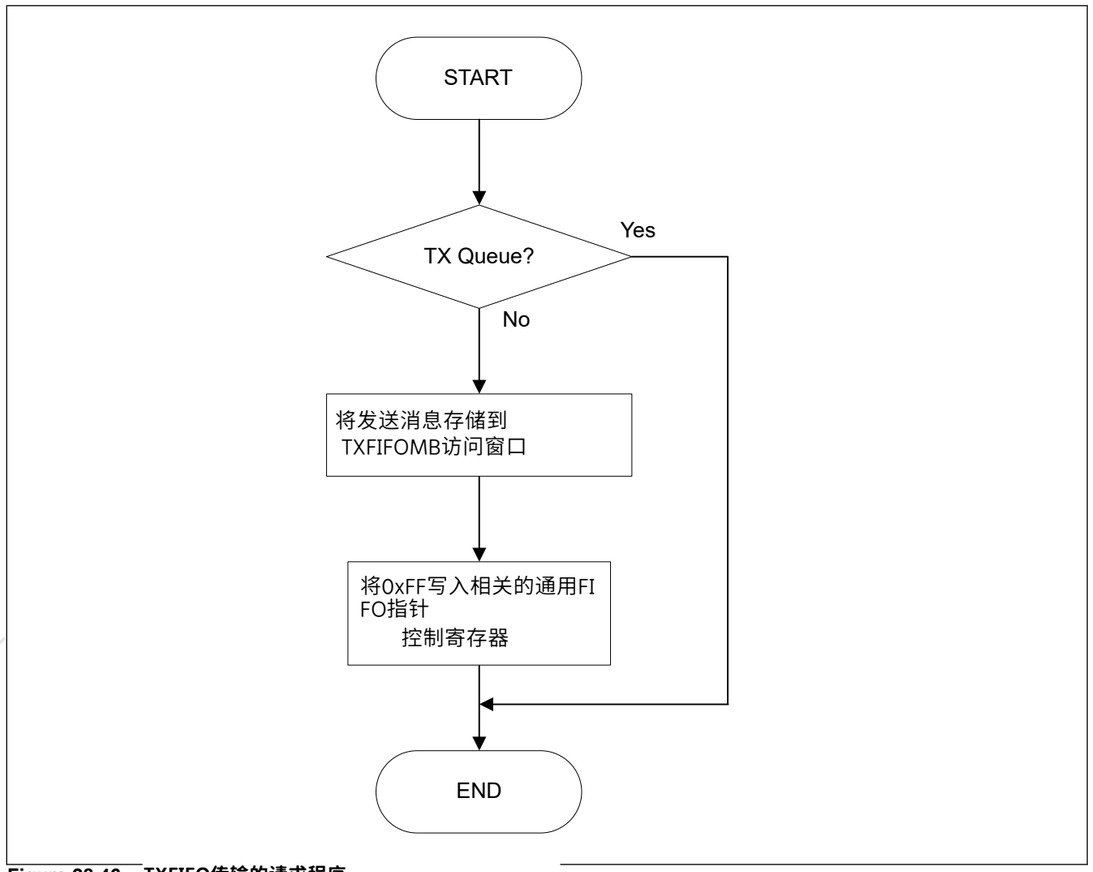


Figure 28.46 TXFIFO传输的请求程序

(2) FIFO传输间隔定时器

对于TX模式下的每个CommonFIFO，可以指定配置为从同一FIFO缓冲区传输的两个连续消息之间的延迟。这种延迟称为间隔时间。在CFDCFCC.CFE位置位后，从FIFO缓冲区成功发送第一条消息后，此间隔时间开始。

当TX模式下的CommonFIFO被使能时，第一个报文被发送而不考虑这个间隔时间。

间隔计时器在以下情况下停止计数：

- 通过清除CFDCFCC.CFE位禁用FIFO。
- CAN通道处于CH_RESET模式。

间隔时间由CommonFIFOConfiguration中的CFDCFCC.CFITT值从0到255个定时器单位指定控制寄存器。

可以根据间隔定时器的两个不同源时钟来定义定时器单元。禁用间隔计时器FIFO传输，选择值0。

定时器源可以通过通用FIFO配置控制寄存器中的配置位CFITSS来选择。

如果CAN通道位时间时钟配置为时钟源，并且CAN通道进入CH_HALT、CH_RESET或CH_SLEEP模式，该通道的间隔定时器停止。

如果选择外设时钟作为间隔定时器时钟源，则间隔定时器只有在CAN通道处于CH_RESET或CH_SLEEP模式时才会停止。

The reference clock can be used to configure the interval time in fixed time units. It is based on the peripheral clock. The reference clock prescaler value CFDGCFG.ITRCP in the Global Configuration Register defines the relation between the peripheral clock frequency/period and the reference clock period.

See Table 28.28 for CFDGCFG.ITRCP configuration values to achieve different reference clock periods based on the peripheral clock frequency and period.

Table 28.28 Configuration example for the reference clock of the FIFO interval timer

Reference clock/Peripheral clock	1 µs	100 µs	500 µs
16 MHz/62.5 ns	16	1600	8000
20 MHz/50 ns	20	2000	10000
32 MHz/31.25 ns	32	3200	16000
50 MHz/20 ns	50	5000	25000

The reference clock resolution can be specified by the interval timer reference clock resolution value CFDCFCC.CFITR in the Common FIFO Configuration/Control Register.

The interval time is based on the reference clock period multiplied by the configured value (x1 or x10). The reference clock based interval timer can be used to satisfy the requirements of the ISO 15765-2 Separation Time. The whole range for the separation time from 100 µs to 127 ms can be covered.

The specified interval time starts after successful transmission event (after EOF7 state of the CAN protocol).

When the interval time has elapsed, the next transmission request is raised by the related TX FIFO. Therefore, the interval time defines the minimum time between two messages transmitted from one FIFO.

The next message is sent at earliest after this interval time. Figure 28.47 shows an example timing of the internal processing.

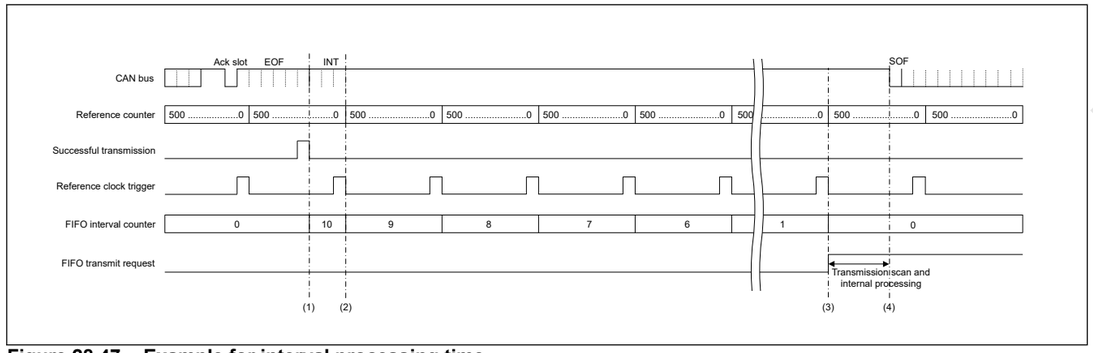


Figure 28.47 Example for interval processing time

The configuration for the timing in Figure 28.47 is as follows:

- Peripheral clock frequency = 50 MHz
- Interval timer reference clock (CFDGCFG.ITRCP) = 500 times
- Reference clock from the settings in Figure 28.47 = 10 µs
- Common FIFO interval timer source selection (CFDCFCC.CFITSS) = 0
- Common FIFO interval timer resolution (CFDCFCC.CFITR) = 0
- Common FIFO interval transmission time (CFDCFCC.CFITT) = 10 times
- Theoretical message separation interval = 100 µs

1. Internal FIFO interval timer is restarted with the occurrence of successful transmission result. This restart is not synchronized to the reference clock trigger. Therefore, the first interval is counting less or equal to 1 reference clock interval.
2. With the next reference clock trigger the FIFO interval timer is decremented.
3. When the FIFO interval timer reached the value 0, the FIFO transmit request is set.

参考时钟可用于以固定时间单位配置间隔时间。它基于外设时钟。全局配置寄存器中的参考时钟预分频器值CFDGCFG.ITRCP定义了外设时钟频率周期和参考时钟周期之间的关系。

有关CFDGCFG.ITRCP配置值，请参见表28.28，以根据外设时钟频率和周期实现不同的参考时钟周期。

Table 28.28 FIFO间隔定时器的参考时钟配置示例

参考时钟外设时钟	1 µs	100 µs	500 µs
16 MHz/62.5 ns	16	1600	8000
20 MHz/50 ns	20	2000	10000
32 MHz/31.25 ns	32	3200	16000
50 MHz/20 ns	50	5000	25000

参考时钟分辨率可以通过通用FIFO配置控制寄存器中的间隔定时器参考时钟分辨率值CFDCFCC.CFITR来指定。

间隔时间基于参考时钟周期乘以配置值（x1或x10）。基于参考时钟的间隔定时器可用于满足ISO15765-2分离时间的要求。可以覆盖从100µs到127ms的整个分离时间范围。

指定的间隔时间在成功传输事件后（在CAN协议的EOF7状态后）开始。

当间隔时间过去时，下一个传输请求由相关的TXFIFO提出。因此，间隔时间定义了从一个FIFO传输的两条消息之间的最短时间。

下一条消息最早在此间隔时间之后发送。图28.47显示了内部处理的示例时序。

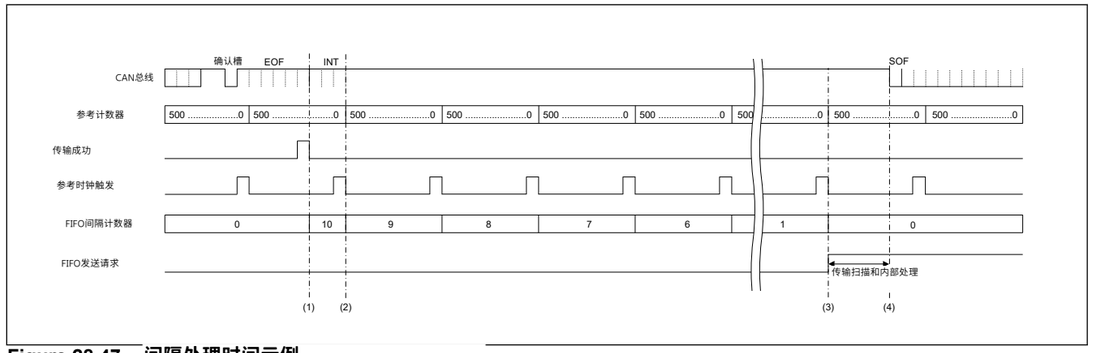


Figure 28.47 间隔处理时间示例

图28.47中的时序配置如下：

- ●外设时钟频率=50MHz
- ●间隔定时器参考时钟(CFDGCFG.ITRCP)=500次
- ●图28.47中设置的参考时钟=10µs
- ●通用FIFO间隔定时器源选择(CFDCFCC.CFITSS)=0
- ●通用FIFO间隔定时器分辨率(CFDCFCC.CFITR)=0
- ●普通FIFO间隔传输时间（CFDCFCC.CFITT）=10次
- ●理论消息分离间隔=100µs

1.内部FIFO间隔定时器随着成功传输结果的出现而重新启动。这次重启不同步到参考时钟触发。因此，第一个间隔计数小于或等于1个参考时钟间隔。

2.随着下一个参考时钟触发，FIFO间隔定时器递减。

3.当FIFO间隔定时器达到值0时，设置FIFO发送请求。

4. When the FIFO is selected for transmission, the transmission starts. Due to internal processing, this usually takes less than 3 CAN bit time, between the internal FIFO transmit request set in step 3. and the actual transmission.

In the worst case when multiple events such as a reception scan, an internal message routing, a transmit scan on all channels occur, it can take up to 126 peripheral clock cycles.

As shown in Figure 28.47, it is not guaranteed that the minimum interval is always equal to the configured value. If a minimum time must never be breached, configure CFDCFCC.CFITT to the required minimum value plus 1.

If additional TX message buffers or TX FIFO are configured for transmission of the same channel, the real delay between two messages transmitted from a TX FIFO can be much longer than specified by the interval time. This is due to higher priority message transmission from these TX message buffers or TX FIFO.

Figure 28.48 shows a block diagram of the FIFO interval time generation circuit.

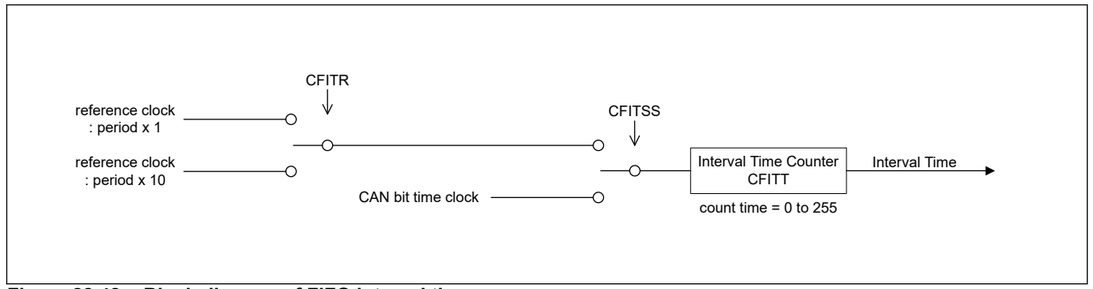


Figure 28.48 Block diagram of FIFO interval timer

28.8.2.4 TX Queue

Each enabled TX Queue for a specific channel consists of three to 4 TX message buffers, which are accessed through one access window.

- The first TX Queue can be configured with a depth of three up to four buffers and uses TX Message Buffer No. 0 as access window (referred to as TXQ)

All the TXQ messages enter the priority comparison for the transmission, which should be only ID Priority (CFDGCFG.TPRI = 0).

The registers for TXQ are:

- CFDTXQCC
- CFDTXQSTS
- CFDTXQPCTR

See related access registers TX Message Buffer ID Registers (TMID[m]), TX Message Buffer Pointer Registers (TMPTR[m]), TX Message Buffer Data Field 0 Registers, and TX Message Buffer Data Field 1 Registers (TMDF[0:1][m]) when access window TXQ0 is used.

The depth of each TXQ buffer can be configured by writing to the CFDTXQCC.TXQDC[1:0] bits of the TX Queue Configuration/Control Register. TXQ can be set from TXMB0 to TXMB3 as a queue buffer at the maximum.

The 4 available options for the depth configuration of TXQ buffer are:

- 0x00: TX Queue disabled
- 0x01: reserved
- 0x10: 3 Messages
- 0x11: 4 Messages

Do not access all the TX message buffers forming the TX Queue directly (except TX Message Buffer No. 0, which act as TX Queue access window).

When a system writes in TXQ, it writes in send data, after checking the state of TXQ.

4.WhentheFIFOisselectedfortransmission thetransmissionstarts.由于内部处理，在步骤3中设置的内部FIFO发送请求和实际发送之间，这通常需要不到3个CAN位时间。

在最坏的情况下，当接收扫描、内部消息路由、所有通道上的发送扫描等多个事件发生时，可能需要多达126个外设时钟周期。

如图28.47所示，不能保证最小间隔总是等于配置的值。如果决不能超过最短时间，请将CFDCFCC.CFITT配置为所需的最小值加1。

如果额外的TX报文缓冲区或TXFIFO配置为传输同一通道，则从TXFIFO传输的两个报文之间的实际延迟可能比间隔时间指定的长得多。这是由于来自这些TX消息缓冲区或TXFIFO的更高优先级的消息传输。

图28.48显示了FIFO间隔时间生成电路的框图。

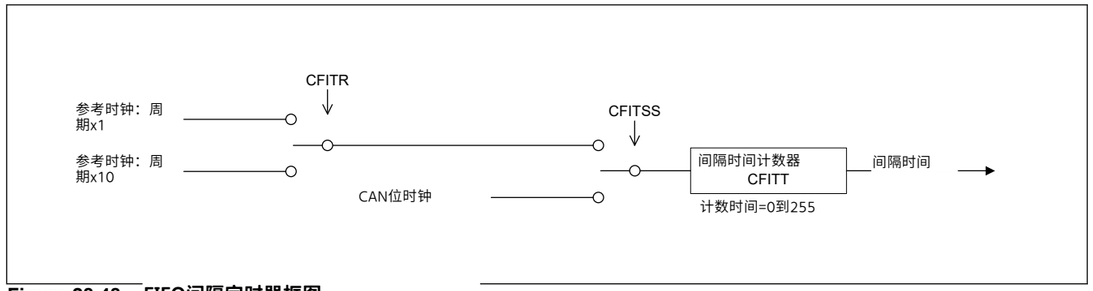


Figure 28.48 FIFO间隔定时器框图

28.8.2.4 TX Queue

为特定通道启用的每个TX队列由3到4个TX消息缓冲区组成，通过一个访问窗口访问这些缓冲区。

●第一个TXQueue可以配置深度为3到4个缓冲区，并使用0号TX消息缓冲区作为访问窗口（简称TXQ）

所有的TXQ消息都进入传输的优先级比较，应该只有ID优先级（CFDGCFG.TPRI=0）。

TXQ的寄存器是：

- CFDTXQCC
- CFDTXQSTS
- CFDTXQPCTR

请参阅相关访问寄存器TX报文缓冲区ID寄存器(TMID[m])、TX报文缓冲区指针寄存器(TMPTR[m])、TX报文缓冲区数据字段0寄存器和TX报文缓冲区数据字段1寄存器(TMDF[0:1][m])当使用访问窗口TXQ0时。

每个TXQ缓冲区的深度可以通过写入TX队列的CFDTXQCC.TXQDC[1:0]位来配置配置控制寄存器。TXQ最大可以设置为TXMB0到TXMB3作为队列缓冲区。

TXQ缓冲区深度配置的4个可用选项是：

●0x00：TX队列禁用

- 0x01: reserved
- 0x10: 3 Messages
- 0x11: 4 Messages

不要直接访问构成TXQueue的所有TX消息缓冲区（除了0号TX消息缓冲区，它充当TX队列访问窗口）。

当系统写入TXQ时，它会在检查TXQ的状态后写入发送数据。

Do not access or configure the related TX Message Buffer Control Registers.

The messages stored to the TX Queue access window are internally stored to a free buffer of the TX Queue.

When the buffer is full, no further access should be done to the queue, until it is no longer full. If access is a software write when the buffer of TXQ is full, send data is overwritten.

The TX Queue can be disabled by clearing the TXQE bit in the TX Queue Configuration/Control Register. If this bit is cleared, the TX Queue Empty flag is set as follows:

- Immediately if the message from the TX Queue is neither scheduled for the next transmission nor in transmission
- Following the transmission completion, the detection of an error on the CAN bus, loss of arbitration or transition to Channel or Global Halt mode if the transmission from the TX Queue is already scheduled for transmission or already in transmission.

Note: The TX Queue is disabled only when the Empty flag is set after clearing the TXQE bit for the corresponding TX Queue.

Other possible messages pending from the TX Queue are lost and their transmission must be requested again.

Before TXQE is set again, ensure that the CFDTXQSTS.TXQEMP bit is set and that there is no pending abort from the TX Queue.

When the TXQE bit is cleared, all messages in the TX Queue buffers are lost and no further message should be stored in the TX Queue.

When a message has been stored to the TX Queue, write 0xFF in the TX Queue Pointer Control Register. This sets the transmit request automatically and changes the internal message buffer pointer to the next free message buffer location of the TX Queue.

Note: If two messages with the same ID are stored in the TX Queue, the order of transmission of these messages can be different from the order in which they were stored in the TX Queue.

To avoid this condition, it is important to confirm that the previous message with the same ID was successfully transmitted before a new message with the same ID is stored in the TX Queue.

For the TX Queue, a dedicated interrupt can be enabled by setting the TXQIE bit of the TX Queue Configuration/Control Register.

The interrupt mode can be configured with the CFDTXQCC.TXQIM bit of the same register either to generate an interrupt for every transmitted message or for the last transmitted message.

The TX Queue transmission request procedure after configuration is shown in Figure 28.49.

不要访问或配置相关的TX报文缓冲区控制寄存器。

存储到TXQueue访问窗口的消息在内部存储到TXQueue的空闲缓冲区中。

当缓冲区已满时，不应进一步访问队列，直到它不再满为止。如果在TXQ的缓冲区已满时访问是软件写入，则发送数据将被覆盖。

可以通过清除TX队列配置控制寄存器中的TXQE位来禁用TX队列。如果该位清零，则TXQueueEmpty标志设置如下：

- 如果来自TXQueue的消息既没有安排下一次传输也没有在传输中，则立即执行
- 传输完成后，检测到CAN总线错误、仲裁丢失或转换到
  如果来自TX队列的传输已被安排传输或已在传输中，则通道或全局暂停模式。

Note: 只有在清除相应TX的TXQE位后设置Empty标志时，才会禁用TX队列
Queue.

其他可能从TXQueue挂起的消息丢失，必须再次请求它们的传输。

在再次设置TXQE之前，确保CFDTXQSTS.TXQEMP位已设置并且没有来自TX的挂起中止
Queue.

当TXQE位被清零时，TX队列缓冲区中的所有消息都将丢失，并且不应将更多消息存储在
TX Queue.

当消息已存储到TX队列时，在TX队列指针控制寄存器中写入0xFF。这会自动设置发送请求并将内部消息缓冲区指针更改为TX队列的下一个空闲消息缓冲区位置。

Note: 如果两个具有相同ID的消息存储在TXQueue中，则这些消息的传输顺序可能与它们存储在TXQueue中的顺序不同。

为避免这种情况，重要的是在将具有相同ID的新消息存储到TXQueue之前确认先前具有相同ID的消息已成功传输。

对于TX队列，可以通过设置TX队列配置控制的TXQIE位来启用专用中断
Register.

可以使用同一寄存器的CFDTXQCC.TXQIM位配置中断模式，以便为每个发送的消息或最后发送的消息产生中断。

配置后的TXQueue发送请求流程如图28.49所示。

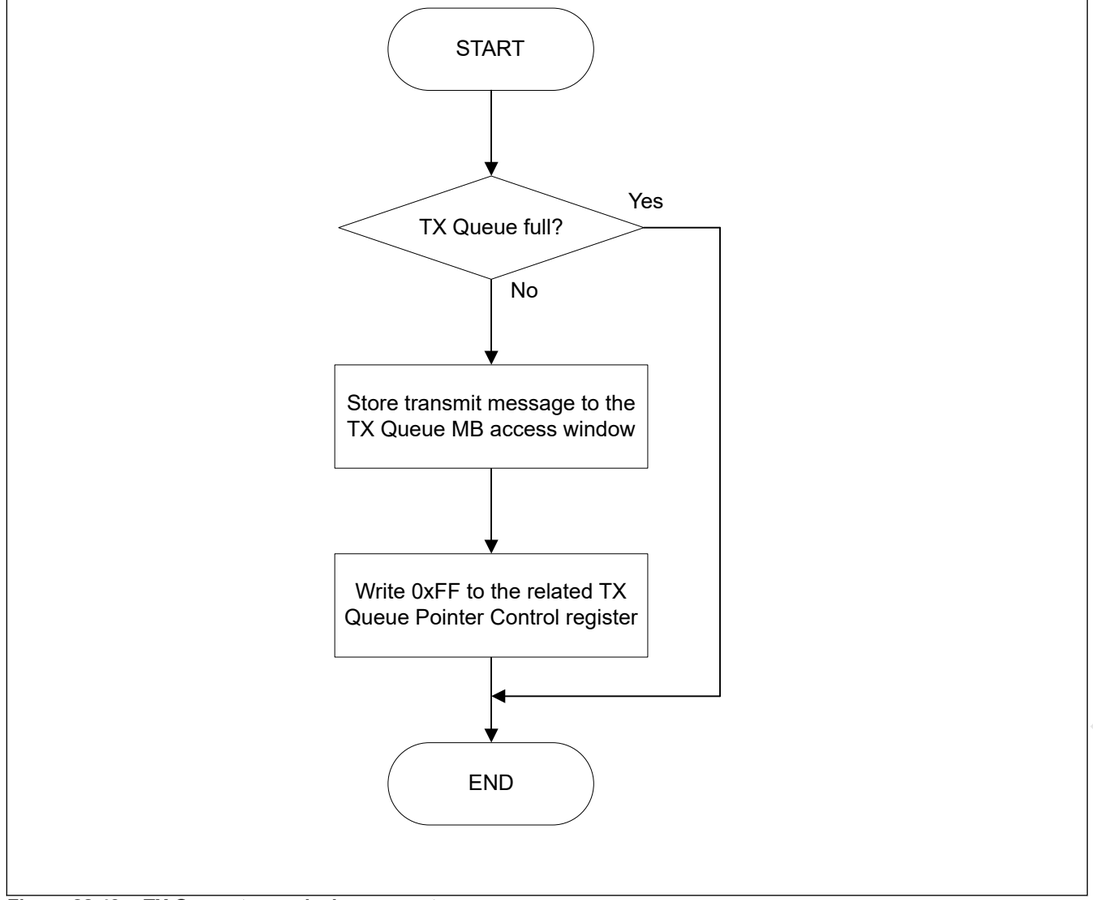


Figure 28.49 TX Queue transmission request

28.8.2.5 TX History List

The TX History List function records the information of the successfully transmitted message in the TX History List Buffers. Two TX History List buffers are provided and THL buffer can store up to 8 TX History List entries.

The CFDTHLCC.THLDTE bit of the TX History List Configuration/Control Register can be used to configure if only message information from TX FIFO or TX Queue is stored, or if all transmit message information from TX Queue, TX FIFO, or normal TX message buffers is stored in the TX History List.

Each transmit message can be individually configured for acceptance to the TX History List with the CFDCFID.THLEN bit in the Message Buffer Pointer Register.

The message information is stored to the TX History List Buffer of a CAN channel after the message is successfully transmitted.

Storing to the list is not synchronized with the status of CFDTMSTSj.TMTRF[1:0] bits in the TX Message Buffer Status Register.

Due to internal processing, the storage to the list can happen with a delay after the successful transmission indication.

Storing the TX History List data can be recognized by the condition that the THLIF is set to 1 when the THLIE bit is configured to 1 or when the TX History List counter CFDTHLSTS.THLMC[5:0] is increased.

In worst case when multi events like reception scan, internal message routing on happen.

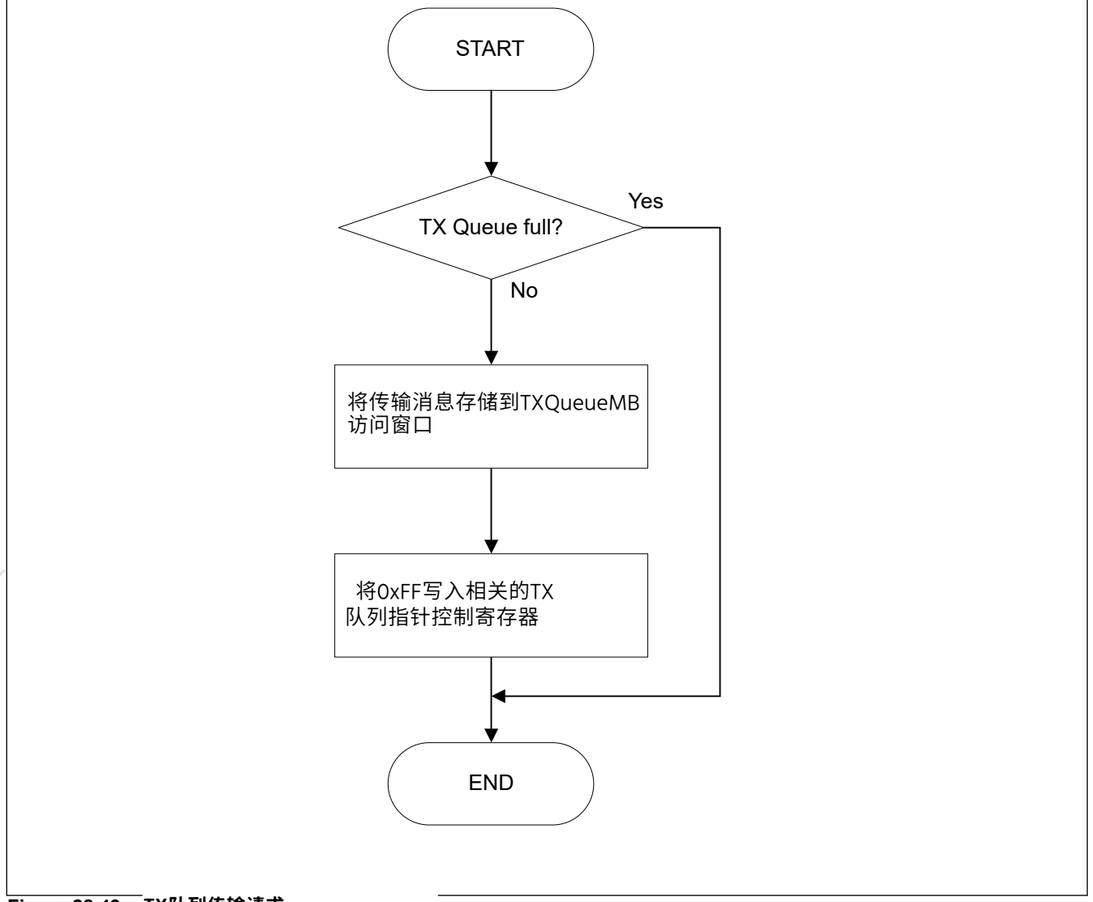


Figure 28.49 TX队列传输请求

28.8.2.5 交易历史列表

TXHistoryList功能将成功发送的报文信息记录在TXHistoryList中缓冲器。提供了两个TX历史列表缓冲区，THL缓冲区可以存储多达8个TX历史列表条目。

TX历史列表配置控制寄存器的CFDTHLCC.THLDTE位可用于配置是否仅存储来自TXFIFO或TX队列的报文信息，或者是否存储了来自TXQueue、TXFIFO或正常TX报文缓冲区的所有发送报文信息存储在TX历史列表中。

可以使用消息缓冲区指针寄存器中的CFDCFID.THLEN位单独配置每个发送消息以接受TX历史列表。

报文发送成功后，报文信息存储到CAN通道的TXHistoryListBuffer中。

存储到列表与TX消息缓冲区状态中CFDTMSTSj.TMTRF[1:0]位的状态不同步
Register.

由于内部处理，在成功传输指示后存储到列表可能会有延迟。

当THLIE位配置为1或TX历史列表计数器CFDTHLSTS.THLMC[5:0]增加时，THLIF设置为1可以识别存储TX历史列表数据。

在最坏的情况下，当接收扫描等多事件发生时，内部消息路由会发生。

- Maximum delay time from setting the CFDTMSTSj.TMTRF to store the TX History List data is 76 peripheral bus clock cycles.

The History list records the following information of a transmitted message:

- Buffer type:
  - 001: TX Message Buffer
  - 010: TX FIFO
  - 100: TX Queue
- Buffer number:
  TX message buffer, TX Queue message buffer or TX message buffer link for the Common FIFO buffer from which transmission occurred. The number depends on the buffer type. See Table 28.29.
- Transmission ID:
  Transmission pointer stored in the transmission message
- Transmit timestamp:
  Message timestamp captured at capture point as configured by CFDGFDCFG.TSCCFG.
- Transmission information label:
  Transmission information label stored in the transmission message.

Table 28.29 TX History List Buffer number entry

Buffer Number	BT[2:0] Buffer Type		
	001b TX Message Buffer	101b TX FIFO	100b TX Queue
00b	Message Buffer 0	Number shown corresponds to the common FIFO. TX Message Buffer Link CFTML of the related Common FIFO configuration	Number shown corresponds to the Message Buffer belonging to the TX Queue which the frame was transmitted
01b	Message Buffer 1		
10b	Message Buffer 2		
11b	Message Buffer 3		

The Transmission ID entry is used to identify which message of a TX FIFO or TX Queue has been successfully transmitted because the TX FIFO or TX Queue number alone is not sufficient.

Therefore, a unique number can be attached to each transmission message stored in a TX FIFO or TX Queue. This unique identification number should be written to the CFDCFFDCSTS.CFPTR[15:0] part of the Common FIFO Access Pointer Register for a TX FIFO or to the CFDTMFDCTRb.TMPTR[15:0] part of the TX Message Buffer Pointer Register of the TX Queue access window message buffer.

When the message is successfully transmitted, this identification number is stored together with the other message related information to the TX History List and can be read using the Transmission ID (TID) of the TX History List Access Register.

Also, for normal TX message buffers, the CFDTMFDCTRb.TMPTR[15:0] part of the TX Message Buffer Pointer Register is stored in the Transmission History List and the information label is the same.

Figure 28.50 shows a transmission preparation flow when TX History List is used.

Read access to the TX History List Access Register is done for every single entry.

After reading one entry, 0xFF must be written to the corresponding TX History List Pointer Control Register to be able to access the next entry until TX History List is empty.

Figure 28.51 shows an example flow for processing the TX History List information.

The TX History Lists have dedicated interrupts, which can be configured with the CFDTHLCC.THLIM bit of the corresponding TX History List Configuration/Control Register and enabled with the CFDTHLCC.THLIE bit of the same

●从设置CFDTMSTSj.TMTRF到存储TXHistoryList数据的最大延迟时间为76个外设总线时钟周期。

历史列表记录传输消息的以下信息：

- Buffer type:
  001：TX消息缓冲区
  - 010: TX FIFO
  - 100: TX Queue
- Buffer number:
  用于发生传输的通用FIFO缓冲区的TX消息缓冲区、TX队列消息缓冲区或TX消息缓冲区链接。数量取决于缓冲区类型。见表28.29。
- Transmission ID:
  传输消息中存储的传输指针
- Transmit timestamp:
  在CFDGFDCFG.TSCCFG配置的捕获点捕获的消息时间戳。

●传输信息标签：
传输信息标签存储在传输消息中。

Table 28.29 TX历史列表缓冲区编号条目

缓冲区号	BT[2:0]缓冲器类型		
	001b TX Message Buffer	101b TX FIFO	100b TX Queue
00b	消息缓冲区0	显示的数字对应于常见的FIFO。德克萨斯州 相关CommonFIFO配置的MessageBufferLinkCFTML	显示的数字对应于属于发送帧的TX队列的消息缓冲区
01b	消息缓冲区1		
10b	消息缓冲区2		
11b	消息缓冲区3		

传输ID条目用于识别TXFIFO或TXQueue的哪个消息已成功传输，因为仅TXFIFO或TXQueue编号是不够的。

因此，可以将唯一编号附加到存储在TXFIFO或TX队列中的每个传输消息。此唯一标识号应写入TXFIFO的通用FIFO访问指针寄存器的CFDCFFDCSTS.CFPTR[15:0]部分或TXFIFO的TX消息缓冲区指针寄存器的CFDTMFDCTRb.TMPTR[15:0]部分德克萨斯州

队列访问窗口消息缓冲区。

当报文成功发送时，该标识号与其他报文相关信息一起存储到TX历史列表中，并可使用TX历史列表访问寄存器的发送ID(TID)读取。

此外，对于普通的TX报文缓冲区，TX报文缓冲区指针寄存器的CFDTMFDCTRb.TMPTR[15:0]部分存储在传输历史列表中，并且信息标签相同。

图28.50显示了使用TXHistoryList时的传输准备流程。

对TX历史列表访问寄存器的读取访问针对每个条目进行。

读取一个条目后，必须将0xFF写入相应的TX历史列表指针控制寄存器，才能访问下一个条目，直到TX历史列表为空。

图28.51显示了处理TX历史列表信息的示例流程。

TX历史列表具有专用中断，可以通过相应的TX历史列表配置控制寄存器的CFDTHLCC.THLIM位进行配置，并通过相同的CFDTHLCC.THLIE位启用

registers, either to generate an interrupt when the History List reached a filling level of 75% or for every new TX History List entry.

An entry lost indication is flagged by the CFDTHLSTS.THLELT bit in the TX History List Status Register. The status of this bit is also shown by the THLES bit in the Global Error Flag Register.

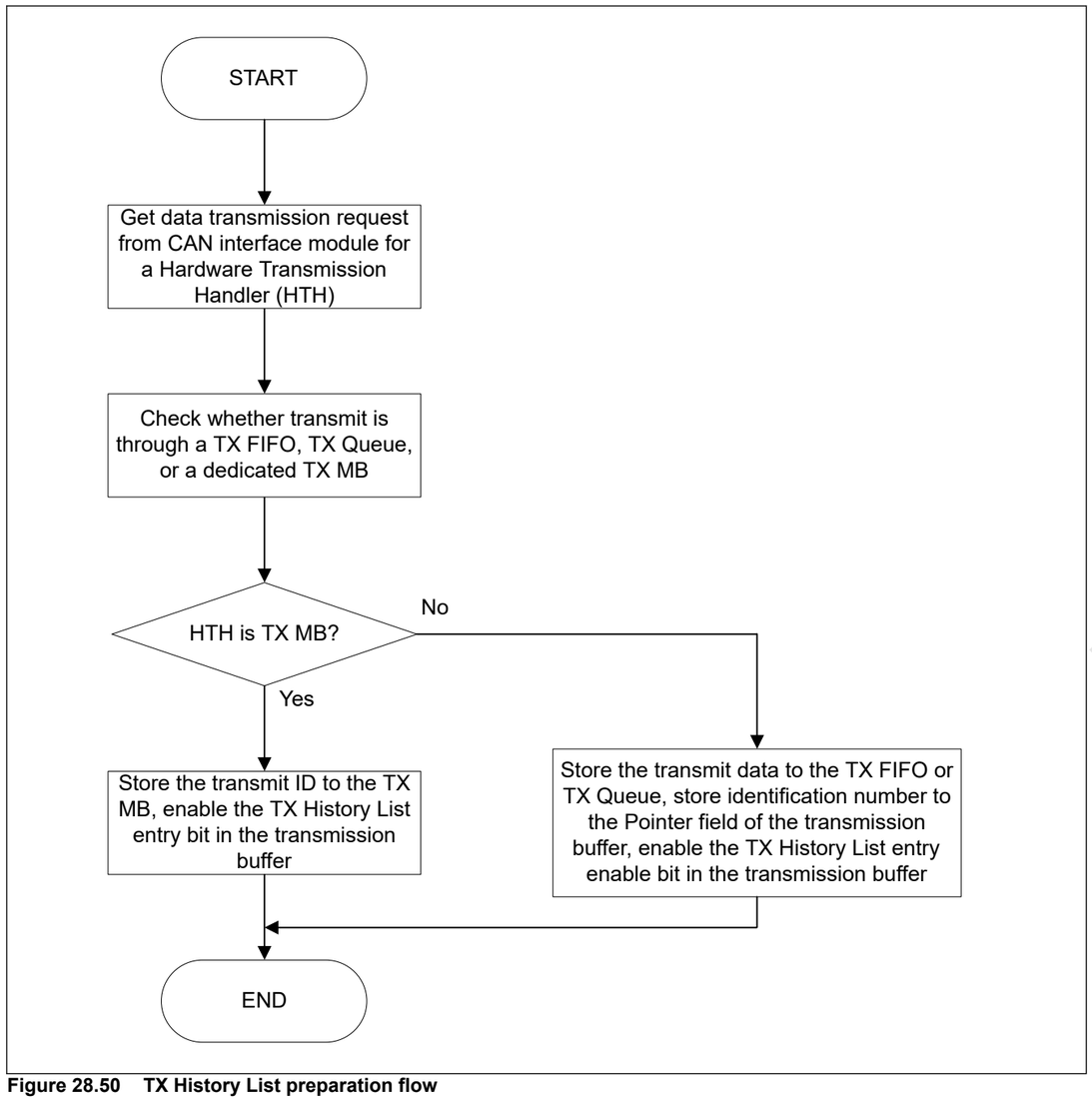


Figure 28.50 TX History List preparation flow

寄存器，当历史列表达到75%的填充水平或每个新的TX历史列表条目时产生中断。

条目丢失指示由TX历史列表状态寄存器中的CFDTHLSTS.THLELT位标记。该位的状态也由全局错误标志寄存器中的THLES位显示。

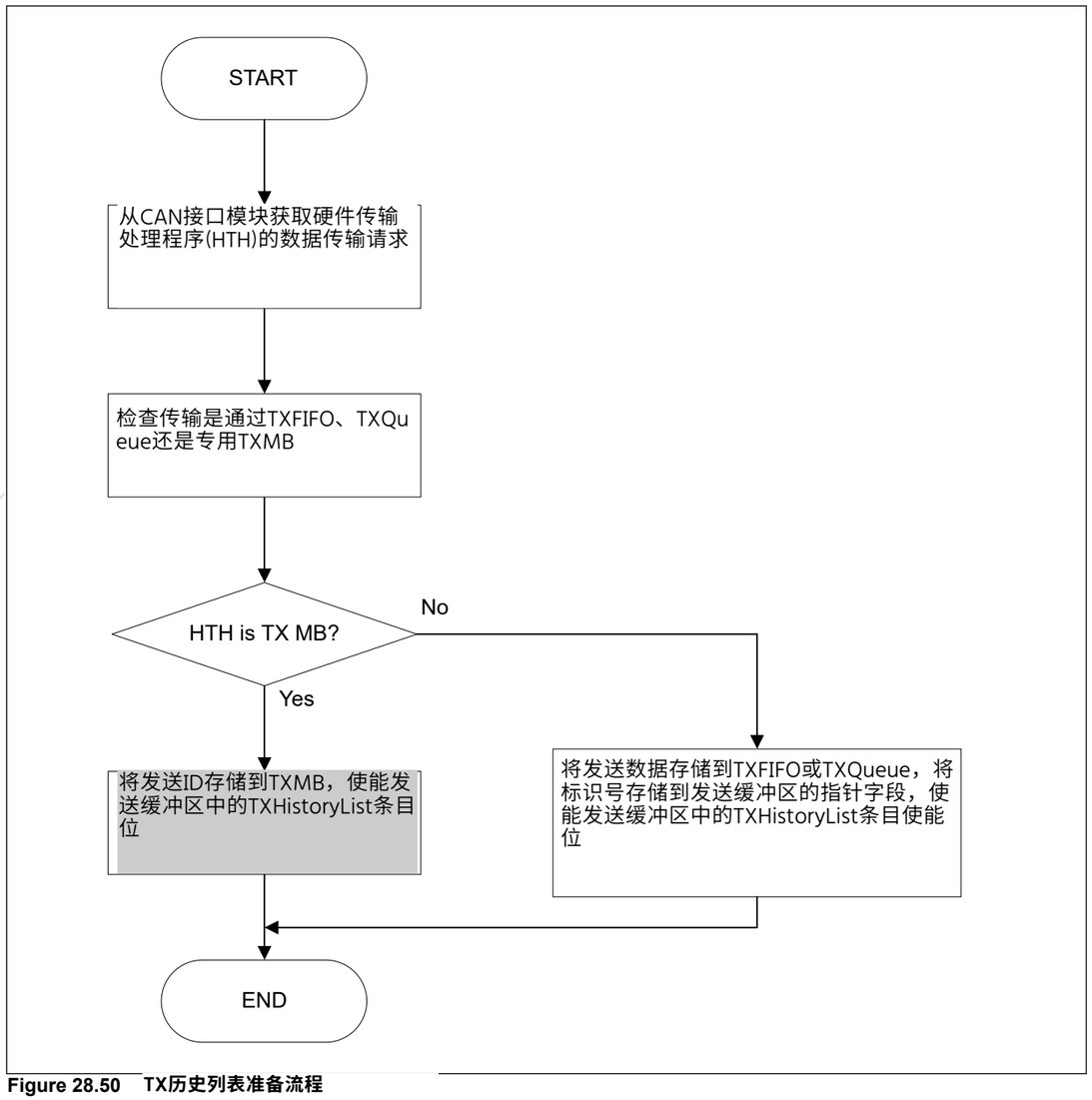


Figure 28.50 TX历史列表准备流程

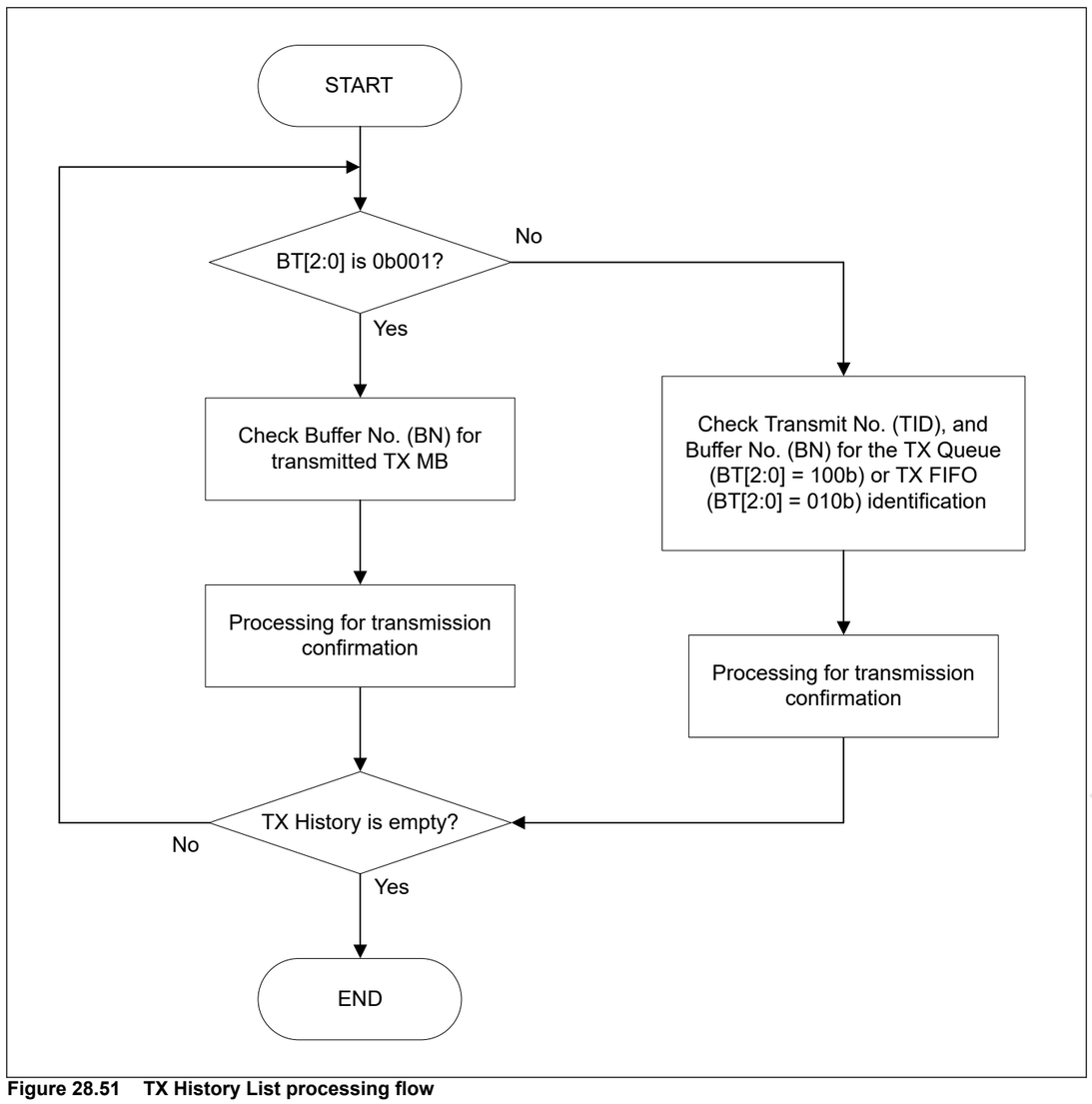


Figure 28.51 TX History List processing flow

28.8.2.6 TX Data Padding

This chapter is not valid for classical CAN.

If the data length code (DLC) of the transmitting message has a higher number of data bytes than the buffer size, the data bytes beyond the restricted range are replaced by bytes with the value of 0xCC.

This can happen for Common FIFO configured as (TX mode) when the transmit message DLC is higher than the CFDCFCC.CFPLS.

This can also happen in FD only mode, if a Classical frame is configured with a DLC bigger than 8.

28.9 Test Mode

The CANFD module can be configured into test modes to allow testing of certain features. These features are provided only for special purposes and care must be taken when configuring the CANFD module in test modes.

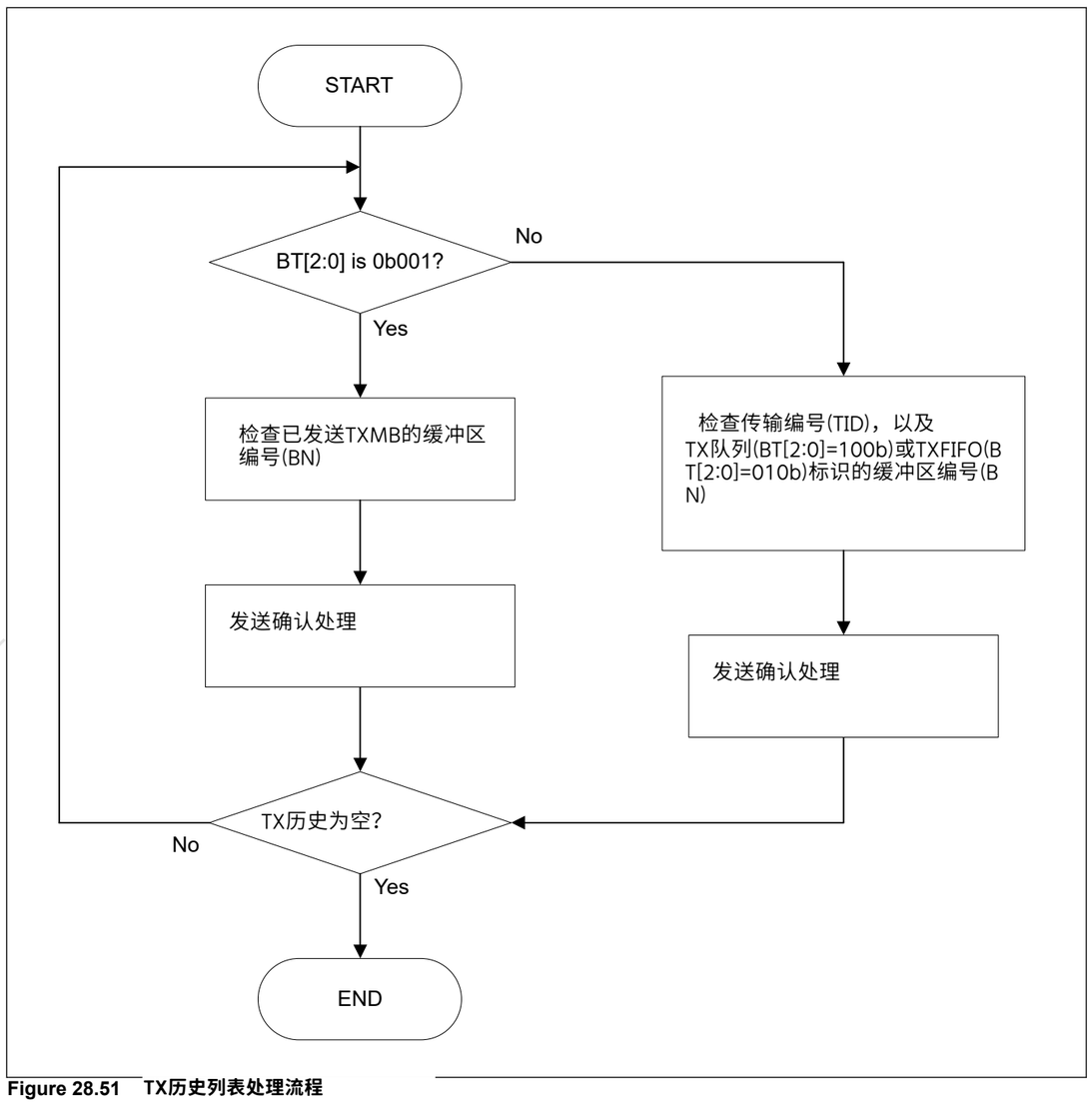


Figure 28.51 TX历史列表处理流程

28.8.2.6 TX数据填充

本章不适用于经典CAN。

如果发送报文的数据长度码(DLC)的数据字节数大于缓冲区大小，则超出限制范围的数据字节将替换为值为0xCC的字节。

当发送消息DLC高于
CFDCFCC.CFPLS.

如果经典帧配置了大于8的DLC，这也可能发生在仅FD模式下。

28.9 测试模式

CANFD模块可以配置为测试模式以允许测试某些功能。这些功能仅用于特殊目的，在测试模式下配置CANFD模块时必须小心。

Note: All test modes are mutually exclusive unless it is explicitly stated that some functions can be enabled across other test modes.

Do not enable any combination of the various test modes specified in this section.

The test modes can be broadly split into 2 groups:

- Channel specific test modes
- Global test modes.

28.9.1 Channel Specific Test Modes

CAN channel can be configured into the following test modes:

- Basic test mode
- Listen-only mode
- Self-test mode 0 (External loop back mode)
- Self-test mode 1 (Internal loop back mode)
- Restricted operation mode.

28.9.1.1 Basic Test Mode

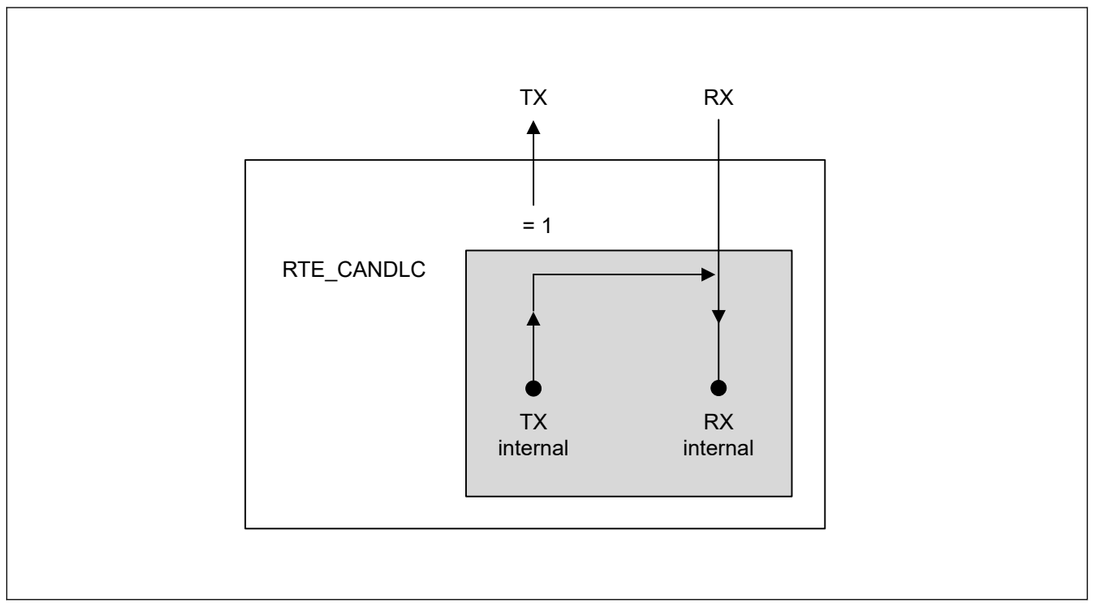
The basic test mode should be used when there is requirement for a particular test setting to be enabled other than when in Listen-only and Self-test modes.

28.9.1.2 Listen-only Mode

The ISO 11898-1 recommends an optional bus-monitoring mode. In this mode, the CAN channel is able to receive valid data frames and valid remote frames. However, it sends only recessive bits on the CAN bus and is not allowed to transmit. If the CAN engine is required to send a dominant bit (ACK bit, overload flag, active error flag), the bit is routed internally so that the CAN engine monitors this as dominant. The external TX pin remains in recessive state.

This mode can be used for baud rate detection. In this mode, an error interrupt is generated if a bus error occurs and the interrupt is enabled.

In this mode, it is not permitted to request transmission from any normal TX message buffer or TX FIFO.



Note: 所有测试模式都是互斥的，除非明确声明某些功能可以跨其他测试模式启用。

不要启用本节中指定的各种测试模式的任何组合。

测试模式可以大致分为两组：

●通道特定的测试模式

●全局测试模式。

28.9.1 通道特定测试模式

CAN通道可配置为以下测试模式：

●基本测试模式

- Listen-only mode

●自检模式0（外部环回模式）

●自检模式1（内部环回模式）

●受限操作模式。

28.9.1.1 基本测试模式

当需要启用特定测试设置时，应使用基本测试模式，而不是在
只听和自测模式。

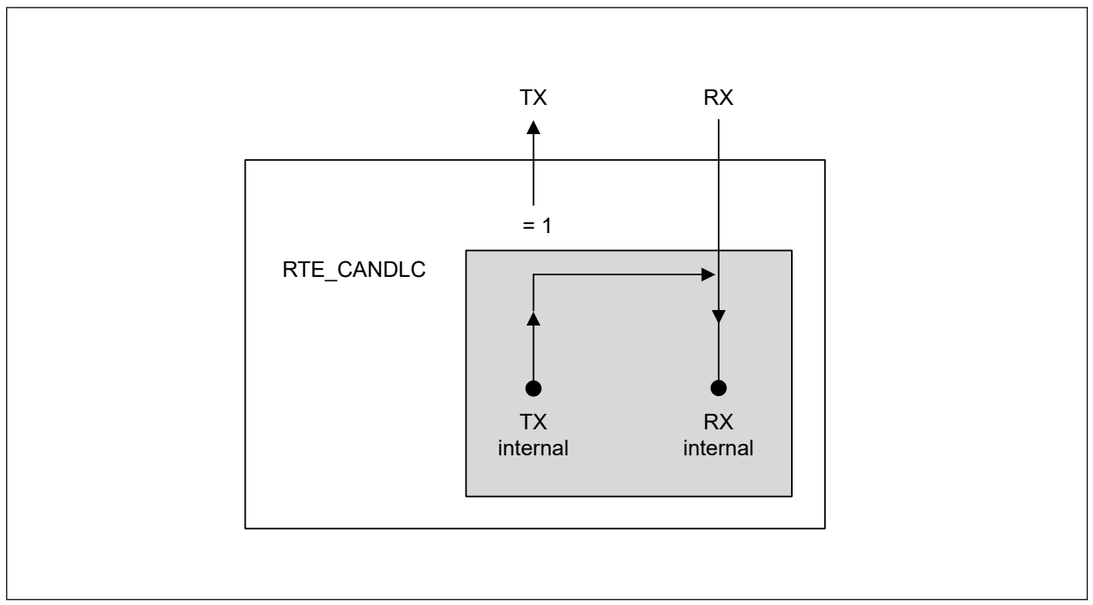
28.9.1.2 Listen-only Mode

ISO11898-1推荐一种可选的总线监控模式。在此模式下，CAN通道能够接收有效的数据帧和有效的远程帧。但是，它只在CAN总线上发送隐性位，不允许发送。

如果CAN引擎需要发送显性位（ACK位、过载标志、活动错误标志），则该位在内部路由，以便CAN引擎将其监控为显性。外部TX引脚保持隐性状态。

该模式可用于波特率检测。在此模式下，如果发生总线错误并启用中断，则会产生错误中断。

在此模式下，不允许从任何正常的TX消息缓冲区或TXFIFO请求传输。

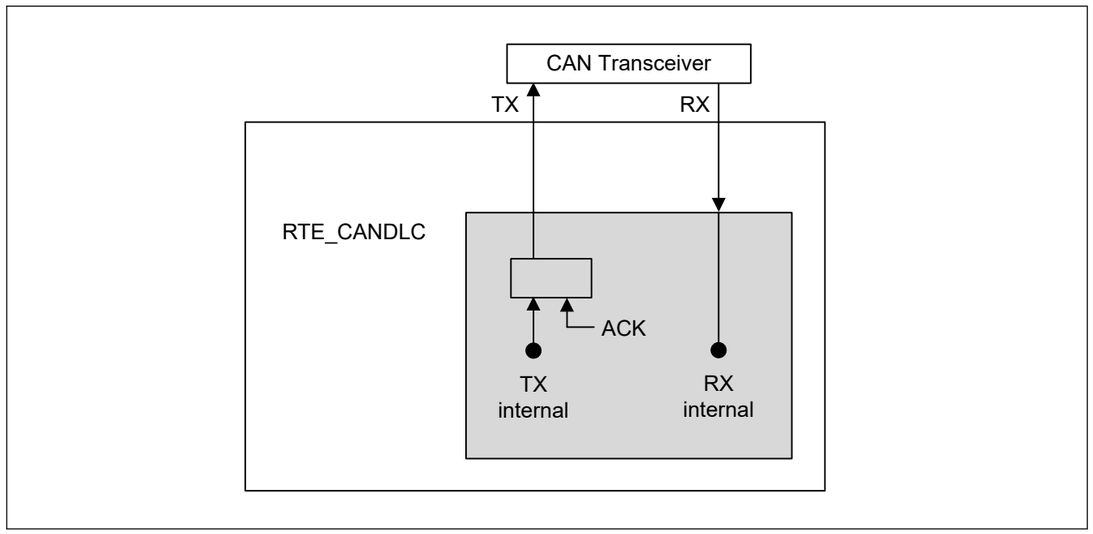


28.9.1.3 Self-test Mode 0 (External loopback mode)

In Self-test mode 0, the CAN engine treats its own transmitted messages as received messages through the CAN transceiver and stores them into its receive message buffers.

To be independent from external stimulation, the engine generates its own Acknowledge bit.

This test can be used for CAN transceiver tests and the RX/TX pins should be connected to the transceiver.



28.9.1.4 Self-test Mode 1 (Internal loopback mode)

In Self-test mode 1, the CAN engine treats its own transmitted messages as received messages and stores them into the receive buffer. This mode is provided for self-test functions. To be independent from external stimulation, the CAN engine generates its own Acknowledge bit. In this mode the CAN engine performs an internal feedback from TX internal to RX internal. The actual value of the external RX input is disregarded by the CAN engine.

The external TX pin outputs only recessive bits. The RX/TX pins do not need to be connected to the CAN bus or any external device.

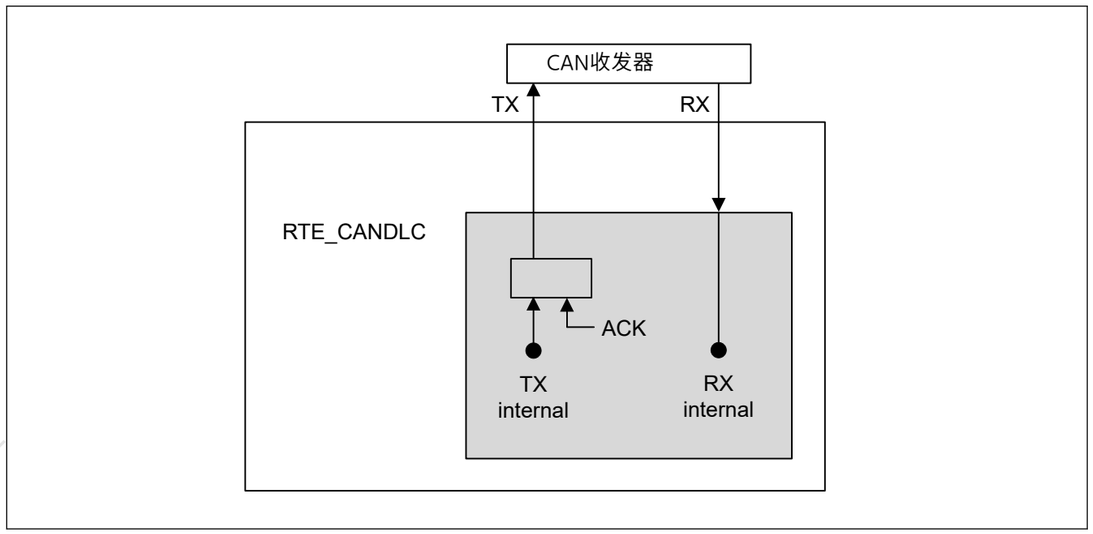
Note: The channel pins are also disconnected from the internal CAN bus communication line.

28.9.1.3 Self-test Mode 0 (External loopback mode)

在自检模式0中，CAN引擎将自己发送的消息视为通过CAN收发器接收到的消息，并将它们存储到其接收消息缓冲区中。

为了独立于外部刺激，引擎会生成自己的确认位。

此测试可用于CAN收发器测试，并且RXTX引脚应连接到收发器。

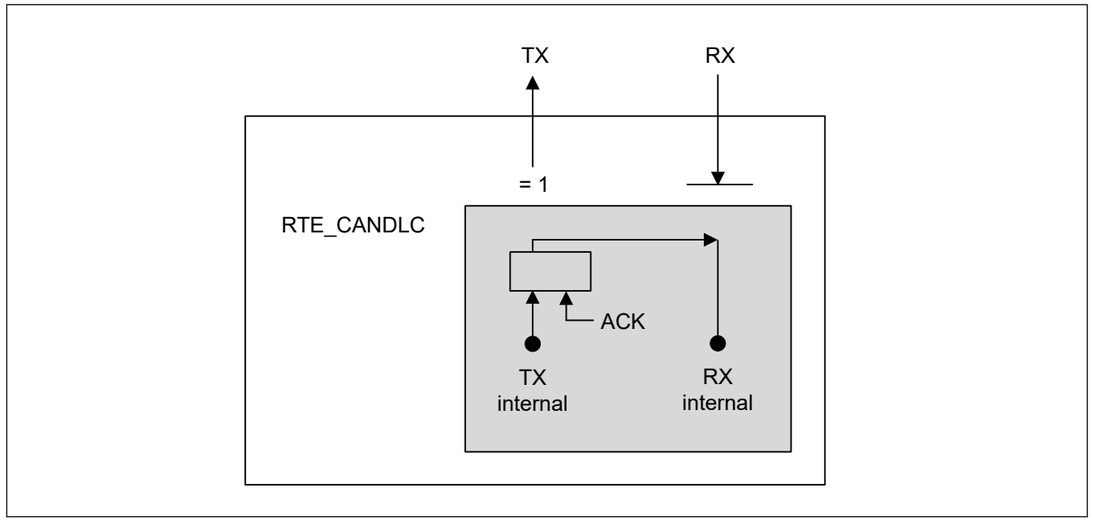


28.9.1.4 Self-test Mode 1 (Internal loopback mode)

在自检模式1中，CAN引擎将自己发送的消息视为接收的消息，并将它们存储到接收缓冲区中。此模式用于自检功能。为了独立于外部刺激，CAN引擎生成自己的确认位。在这种模式下，CAN引擎执行从TX内部到RX内部的内部反馈。CAN引擎忽略外部RX输入的实际值。

外部TX引脚仅输出隐性位。RXTX引脚不需要连接到CAN总线或任何外部设备。

Note: 通道引脚也与内部CAN总线通信线路断开。



28.9.1.5 Restricted Operation Mode

This chapter is not valid for classical CAN.

In Restricted operation mode, the CAN node is able to receive valid data and remote frames generating the Acknowledge bit.

Active error or overload frames cannot be transmitted, instead it waits for the occurrence of bus idle condition to resynchronize itself to the CAN communication after an error or overload condition occurs.

Additionally, the Receive and Transmit Error Counter (REC and TEC) are frozen independently from the occurrence of errors. The mode is specified in ISO 11898-1 and the setting of transmit request is permitted.

28.9.2 Global Test Modes

The CANFD module can be configured into the following test modes:

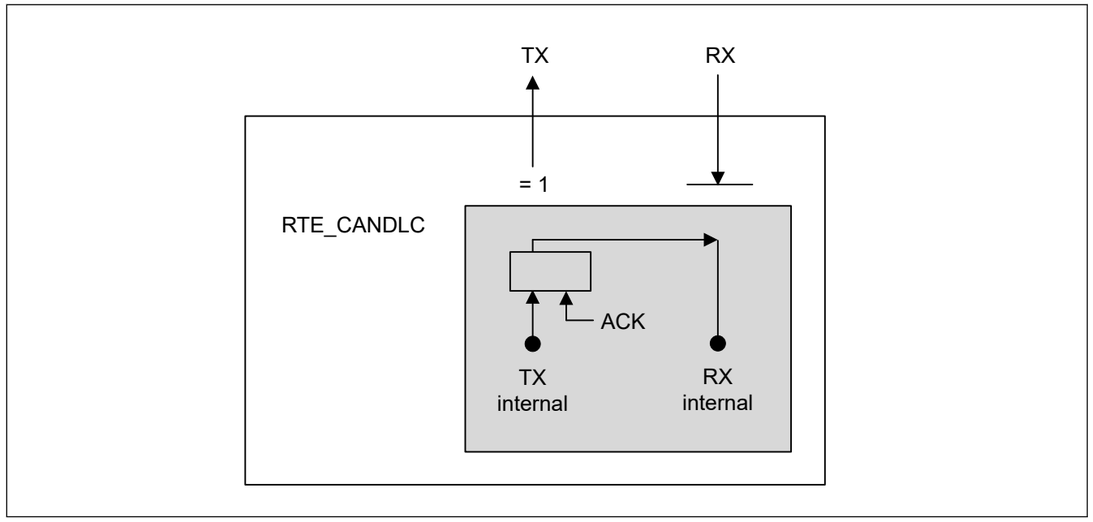
- RAM test mode
- Bit Flip Test

The test modes in the following table are protected by a special software procedure to enable the mode. This software procedure enables write access to the test mode by a specific unlock key as shown in the table.

Test mode	Unlock key 1	Unlock key 2
RAM test mode	0x7575	0x8A8A

If the software sequence of the two consecutive unlock key write accesses (half-word or word access) is interrupted by any other write access to the register or if incorrect data is written to the Global Unlock Key Register, the corresponding test mode cannot be set and the sequence must be restarted.

After the two unlock key write accesses, the next write access should be to set the corresponding test mode enable bit. If this is not followed, the unlock mechanism reset and the test mode enable bit cannot be set and the unlock sequence must be restarted.



28.9.1.5 受限操作模式

本章不适用于经典CAN。

在受限操作模式下，CAN节点能够接收有效数据和生成确认位的远程帧。

无法传输主动错误或过载帧，而是在发生错误或过载情况后等待总线空闲条件的出现以重新同步到CAN通信。

此外，接收和发送错误计数器（REC和TEC）独立于错误发生而被冻结。模式在ISO11898-1中指定，允许设置发送请求。

28.9.2 全局测试模式

CANFD模块可配置为以下测试模式：

- RAM测试模式
- 位翻转测试

下表中的测试模式受特殊软件程序保护以启用该模式。该软件程序允许通过特定的解锁密钥对测试模式进行写访问，如表中所示。

测试模式	解锁钥匙1	解锁钥匙2
RAM测试模式	0x7575	0x8A8A

如果两次连续的解锁密钥写访问（半字或字访问）的软件序列被对寄存器的任何其他写访问中断，或者如果向全局解锁密钥寄存器写入不正确的数据，则无法设置相应的测试模式并且必须重新启动序列。

在两次解锁密钥写访问之后，下一次写访问应该是设置相应的测试模式使能位。如果不遵循，解锁机制复位和测试模式使能位不能设置，解锁序列必须重新启动。

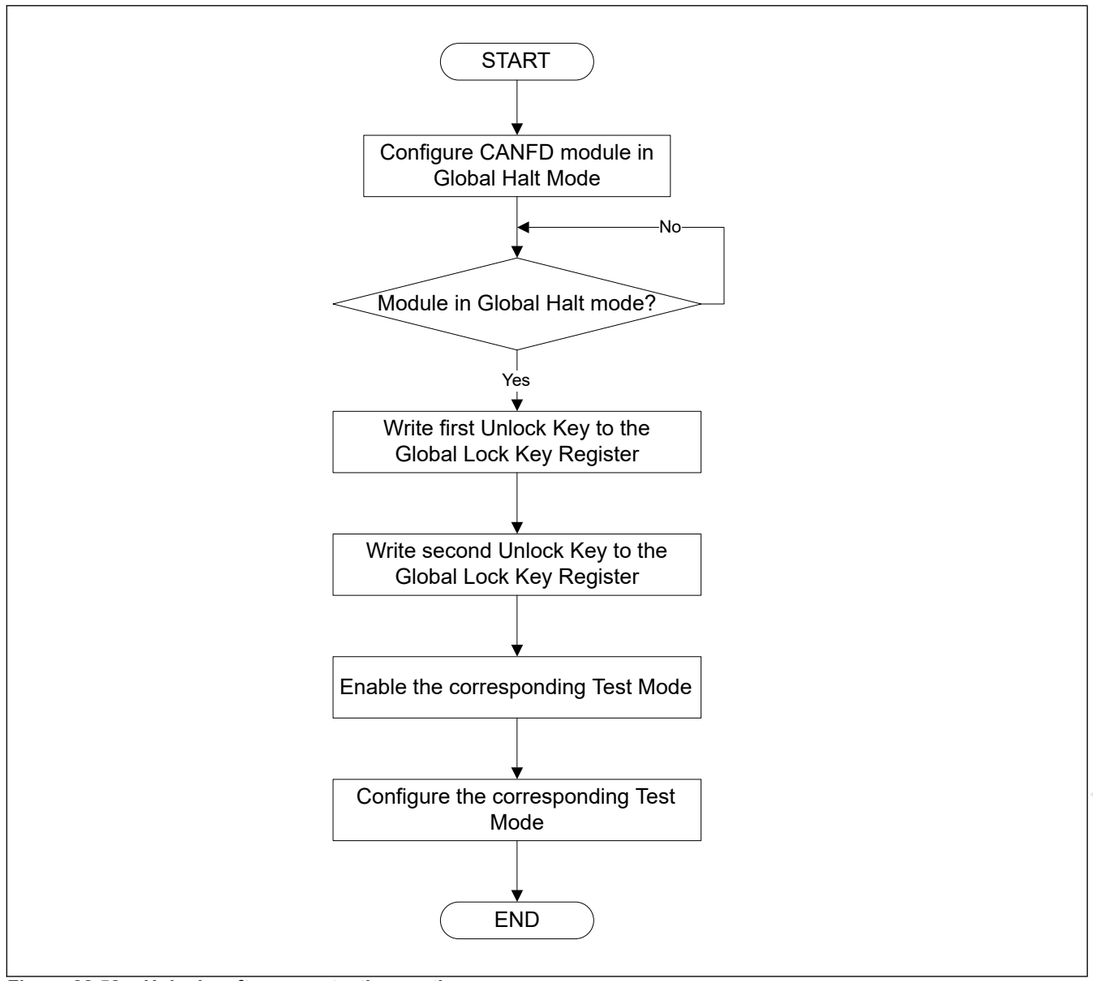


Figure 28.52 Unlock software protection routine

28.9.2.1 RAM Test Mode

The CANFD module can be configured in RAM test mode by setting the CFDGTSTCTR.RTME bit in the Global Test Control Register when the corresponding lock key is previously written. This is a special test mode, in which, the complete RAM area can be accessed.

Note: The actual RAM size is bigger than the RAM area initialized after a hardware reset. Therefore, ECC error flag (of the ECC macro) may be set if CPU reads data from this uninitialized RAM area while CANFD module is in RAM test mode.

In this mode, the RAM area is split into number of pages (pn) of 256 bytes, each which can be accessed with the CFDRPGACCk register.

The page should be selected for read/write access by writing to the CFDGTSTCFG.RTMPS[3:0] bits in the Global Test Control Register. Data can then be read from or written in to the RAM Test Page Access Registers.

Figure 28.53 shows the structure of the pages in the RAM when performing a RAM test mode.

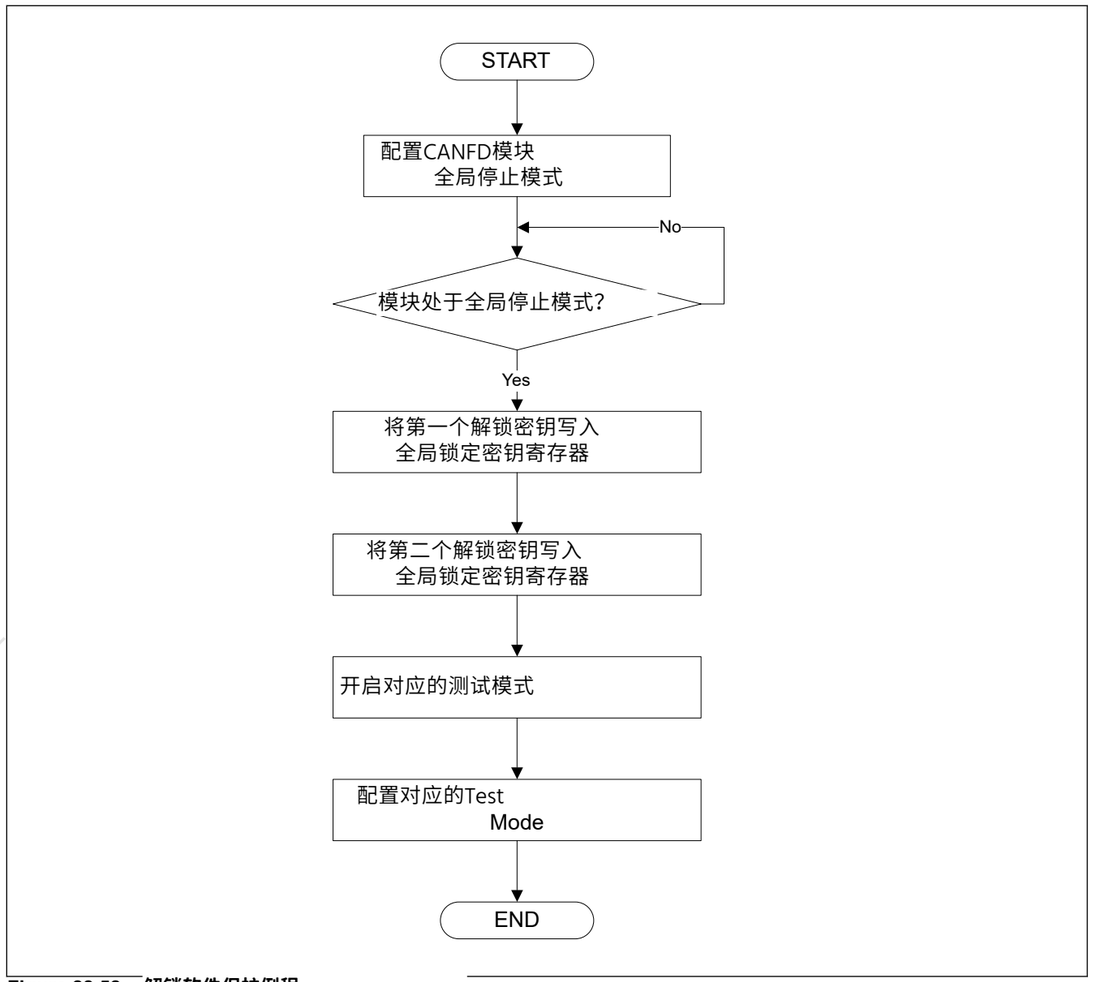


Figure 28.52 解锁软件保护例程

28.9.2.1 RAM测试模式

CANFD模块可通过设置GlobalTest中的CFDGTTSTCTR.RTME位配置为RAM测试模式控制寄存器，当相应的锁定键先前被写入时。这是一种特殊的测试模式，其中，完整的可以访问RAM区域。

Note: 实际RAM大小大于硬件复位后初始化的RAM区域。因此，ECC错误标志（的如果在CANFD模块处于RAM测试模式时CPU从该未初始化的RAM区域读取数据，则可以设置ECC宏。

在这种模式下，RAM区域被分成256字节的页数(pn)，每个页都可以通过CFDRPGACCk register.

应通过写入全局测试中的CFDGTSTCFG.RTMPS[3:0]位来选择该页面进行读写访问控制寄存器。然后可以从RAM测试页访问寄存器读取或写入数据。

图28.53显示了执行RAM测试模式时RAM中的页面结构。

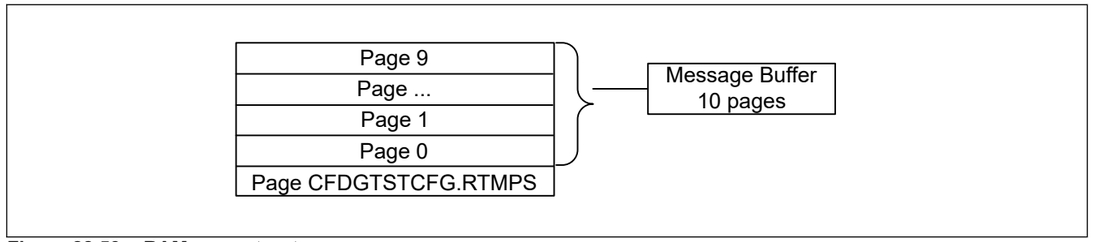


Figure 28.53 RAM page structure

The total available RAM size is 2328 bytes for the Message Buffer RAM.

The pn and CFDGTSTCFG.RTMPS[3:0] values for the MB RAMs are calculated in the following way:

pn = ceil (total RAM size in bytes / number of bytes per page)

- MB RAM:
  pn = ceil (2328 / 256) = 10 pages
  CFDGTSTCFG.RTMPS[3:0] = 0 to 9 inclusive

Figure 28.54 shows the software flow for RAM test mode.

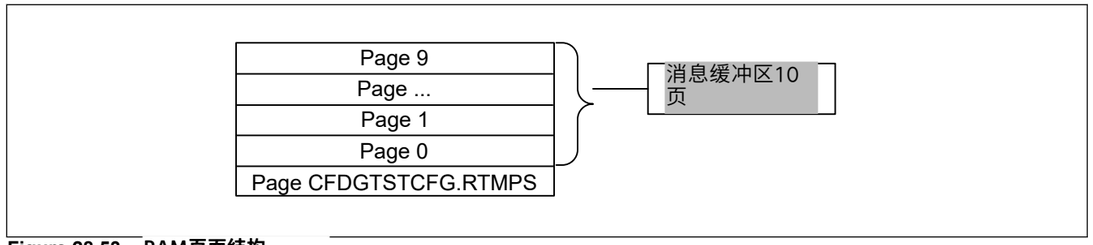


Figure 28.53 RAM页面结构

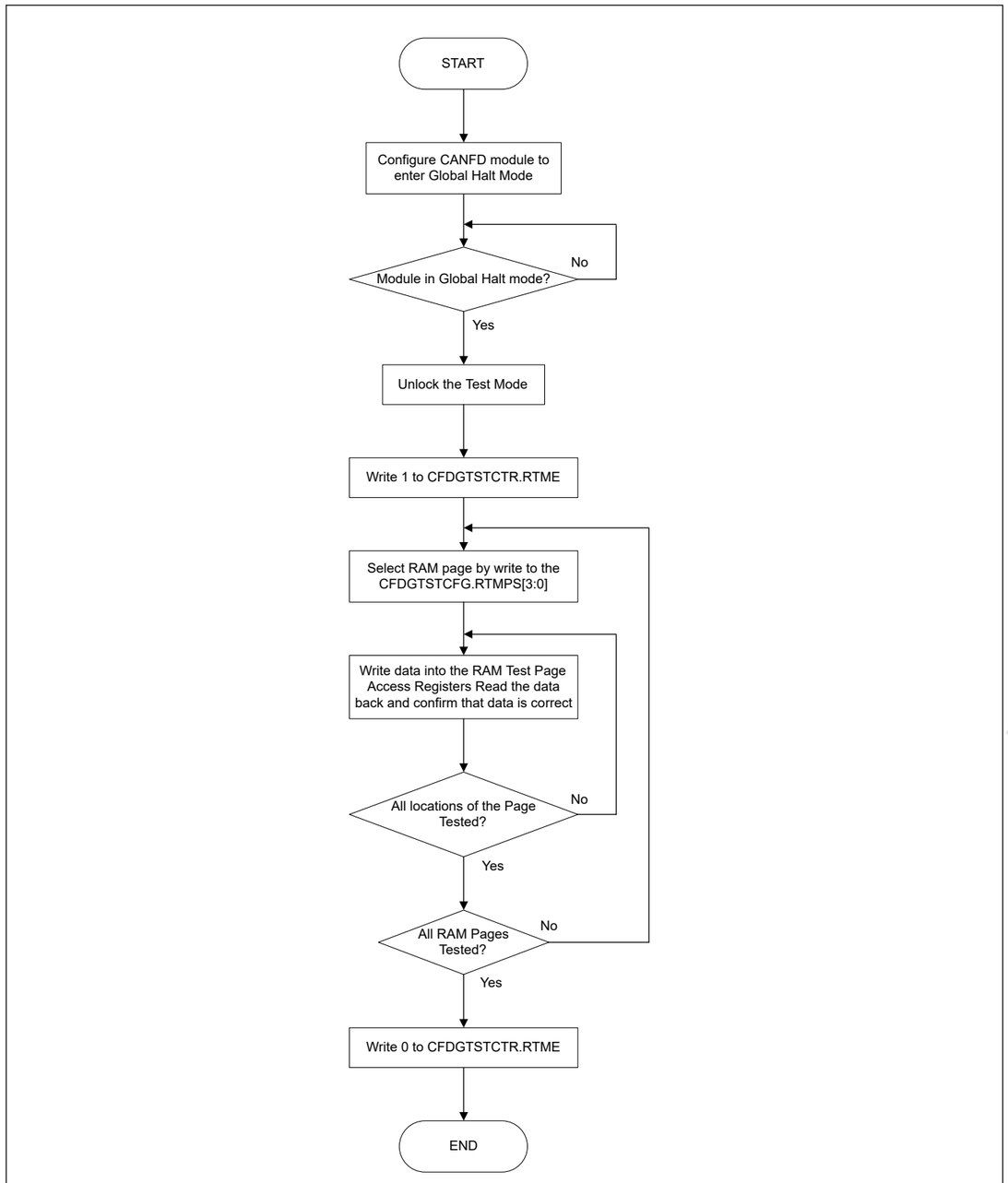
消息缓冲区RAM的总可用RAM大小为2328字节。

MBRAM的pn和CFDGTSTCFG.RTMPS[3:0]值按以下方式计算：

pn=ceil（以字节为单位的总RAM大小每页的字节数）

- MB RAM:
  pn=ceil(2328256)=10页CFDGTSTCFG.RTM
  PS[3:0]=0到9（含）

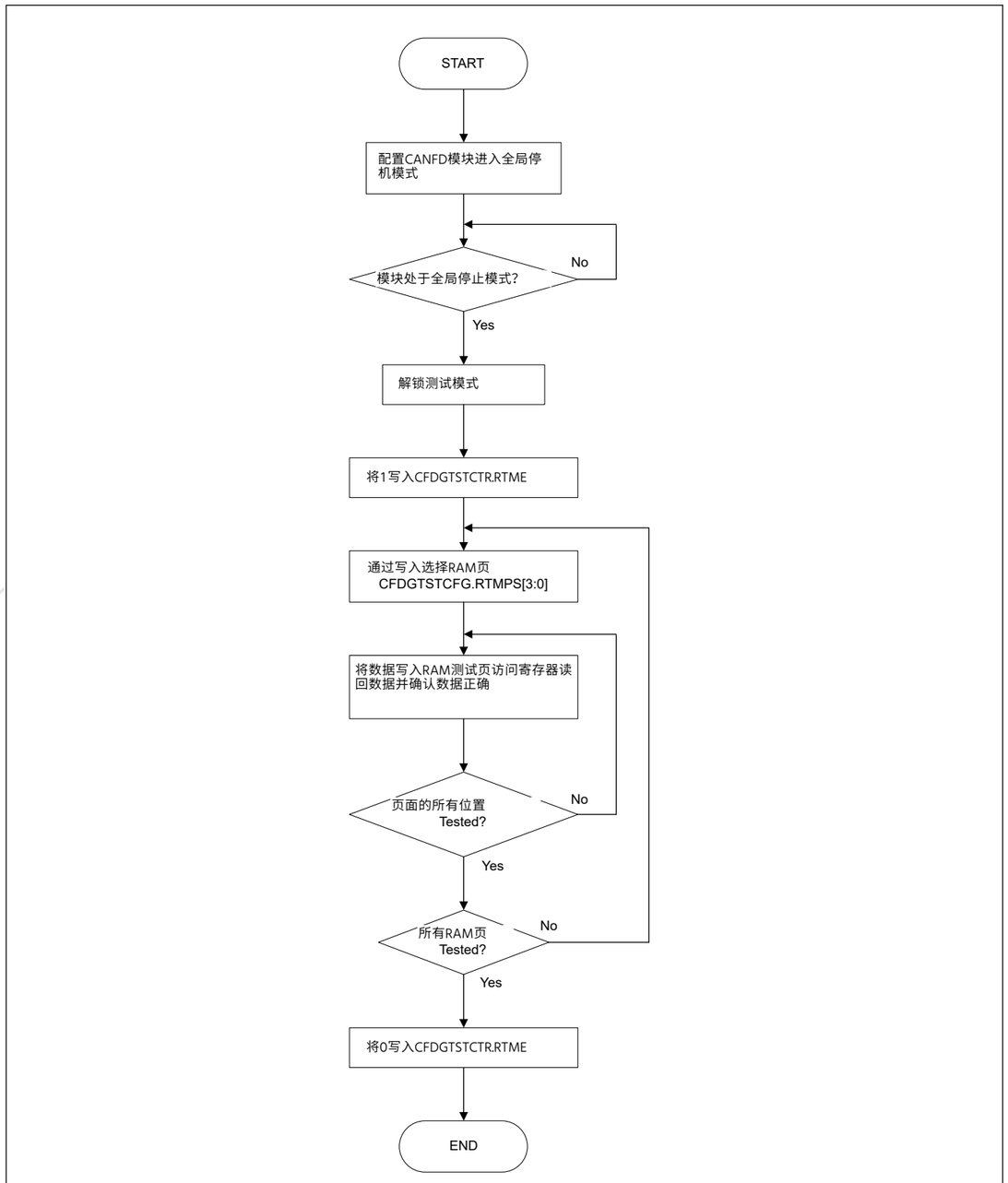
图28.54显示了RAM测试模式的软件流程。



Note 1. Change into the following status before changing to RAMTEST.
- Cancel of a request for transmission.
- Disable of all the FIFO and TXQ.
- Clear of the receiving flag for a receiving buffer.

Figure 28.54 Software flow for RAM test mode

To exit this test mode, the CFDGTSTCTR.RTME bit must be cleared. The CFDGTSTCTR.RTME bit is cleared by writing 0 to it.



注1.更改为RAMTEST之前，请更改为以下状态。
- 取消传输请求。
- 禁用所有FIFO和TXQ。
- 清除接收缓冲区的接收标志。

Figure 28.54 RAM测试模式的软件流程

要退出此测试模式，CFDGTSTCTR.RTME位必须清零。CFDGTSTCTR.RTME位通过向其写入0来清除。

The CFDGTSTCTR.RTME bit is cleared automatically when the CANFD module enters Global Reset mode from the test mode.

28.9.2.2 Bit Flip Test

Bit Flip Test can invert the bit (the 1st bit of ID) of the beginning of the bit stream to receive.

If this function is used by a transmitting node, a bit error or an arbitration lost will occur.

If this function is used by a receiving node, a CRC error or a stuff error will occur.

Users should refer to the bit stuffing rule when using this feature, as there is the possibility of receiving a stuff error (due to the inversion) rather than a CRC error.

The following sequence should be used to perform CRC Error testing. In the sequence below CANFD module is the receiver.

1. Set the CFDC0CTR.BFT bit to 1'b1, in order to invert the first bit of the incoming bit stream from sending node
2. Wait for the can_cherr_int output signal to set to 1'b1
3. Read either the CFDC0ERFL.CRCREG or the CFDC0FDCRC.CRCREG (depending on the received frame type: Classical or FD). The value should be different from the received CRC value of the reference message from sending node.
4. Check that CFDC0ERFL.CERR is 1'b1

As the CRC generator logic is shared for RX and TX there is no need to create a separate TX CRC Error test.

当CANFD模块从测试模式进入全局复位模式时，CFDGTSTCTR.RTME位会自动清零。

28.9.2.2 位翻转测试

位翻转测试可以反转要接收的位流开始的位（ID的第1位）。

如果发送节点使用此功能，则会发生误码或仲裁丢失。

如果接收节点使用此功能，则会发生CRC错误或填充错误。

用户在使用此功能时应参考比特填充规则，因为可能会收到填充错误（由于反转）而不是CRC错误。

应使用以下序列执行CRC错误测试。在下面的序列中，CANFD模块是接收器。

1.将CFDC0CTR.BFT位设置为1'b1，以反转来自发送节点的传入比特流的第一位

2.等待can_cherr_int输出信号设置为1'b1

3.读取CFDC0ERFL.CRCREG或CFDC0FDCRC.CRCREG（取决于接收到的帧类型：古典或FD）。该值应不同于从发送节点接收到的参考消息的CRC值。

4.检查CFDC0ERFL.CERR是否为1'b1

由于RX和TX共享CRC生成器逻辑，因此无需创建单独的TXCRC错误测试。

29. CANFD ECC (CNECC)

29.1 Overview

MBRAM have ECC function of 2-bit ECC error detection and 1-bit ECC error detection and correction*1. The ECC module adds 7 bits ECC data to 32 bits RAM data.

Note 1. The ECC module cannot detect 3 or more bits error. In this case, the ECC module detects 1-bit or 2-bit error, does not detect errors, or corrects the erroneous bit to erroneous data by setting. When all RAM data are fixed to 0 or 1, it is detected as 2-bit ECC error.

29.2 Register Descriptions

29.2.1 EC710CTL : ECC Control Register

Base address: ECCMB = 0x4012_F200

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ECDEDF0	ECSEDF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EMCA[1:0]		—	—	ECOVFF	ECER2C	ECER1C	—	—	ECERVF	EC1ECP	EC2EDIC	EC1EDIC	ECER2F	ECER1F	ECEMF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
0	ECEMF	ECC Error Message Flag 0: There is no bit error in present RAM output data 1: There is bit error in present RAM output data	R
1	ECER1F	ECC Error Detection and Correction Flag 0: After clearing this bit, 1-bit error correction has not occurred 1: 1-bit error has occurred	R
2	ECER2F	2-bit ECC Error Detection Flag 0: After clearing this bit, 2-bit error has not occurred 1: 2-bit error has occurred	R
3	EC1EDIC	ECC 1-bit Error Detection Interrupt Control 0: Disable 1-bit error detection interrupt request 1: Enable 1-bit error detection interrupt request	R/W
4	EC2EDIC	ECC 2-bit Error Detection Interrupt Control 0: Disable 2-bit error detection interrupt request 1: Enable 2-bit error detection interrupt request	R/W
5	EC1ECP	ECC 1-bit Error Correction Permission 0: At 1-bit error detection, the error correction is executed 1: At 1-bit error detection, the error correction is not executed	R/W
6	ECERVF	ECC Error Judgment Enable Flag 0: Error judgment disable 1: Error judgment enable	R/W
8:7	—	These bits are read as 0. The write value should be 0.	R/W
9	ECER1C	Accumulating ECC Error Detection and Correction Flag Clear 0: No effect 1: Clear accumulating ECC error detection and correction flag	R/W
10	ECER2C	2-bit ECC Error Detection Flag Clear 0: No effect 1: Clear 2-bit ECC error detection flag	R/W

29. CANFD ECC (CNECC)

29.1 Overview

MBRAM具有2位ECC错误检测和1位ECC错误检测和纠正的ECC功能*1。ECC模块将7位ECC数据添加到32位RAM数据中。

注1.ECC模块无法检测3位或更多位错误。在这种情况下，ECC模块检测1位或2位错误，不检测错误，或通过设置将错误位纠正为错误数据。当所有RAM数据固定为0或1时，将被检测为2位ECC错误。

29.2 注册说明

29.2.1 EC710CTL:ECC控制寄存器

Base address: ECCMB = 0x4012_F200

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ECDEDF0	ECSEDF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EMCA[1:0]		—	—	ECOVFF	ECER2C	ECER1C	—	—	ECERVF	EC1ECP	EC2EDIC	EC1EDIC	ECER2F	ECER1F	ECEMF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
0	ECEMF	ECC错误消息标志 0：当前RAM输出数据无误码1：当前RAM输出数据有误码	R
1	ECER1F	ECC错误检测和纠正标志 0：清除该位后，未发生1位错误纠正1：发生1位错误	R
2	ECER2F	2位ECC错误检测标志 0：清除该位后，未发生2位错误1：发生2位错误	R
3	EC1EDIC	ECC1位错误检测中断控制 0：禁止1位错误检测中断请求1：允许1位错误检测中断请求	R/W
4	EC2EDIC	ECC2位错误检测中断控制 0：禁止2位错误检测中断请求1：允许2位错误检测中断请求	R/W
5	EC1ECP	ECC1位纠错权限 0：1位错误检测时执行纠错1：1位错误检测时不执行错误纠正	R/W
6	ECERVF	ECC错误判断使能标志 0：错误判断无效1：错误判断有效	R/W
8:7	—	这些位被读取为0。写入值应为0。	R/W
9	ECER1C	累积ECC错误检测和纠正标志清除 0：无效1：清除累积ECC错误检测和纠正标志	R/W
10	ECER2C	2位ECC错误检测标志清除 0：无效1：清除2位ECC错误检测标志	R/W

Bit	Symbol	Function	R/W
11	ECOVFF	ECC Overflow Detection Flag 0: No effect 1: ECC overflow detection flag	R
13:12	—	These bits are read as 0. The write value should be 0.	R/W
15:14	EMCA[1:0]	Access Control to ECC Mode Select bit These bits enable or disable write access to ECERVF bit.	R/W
16	ECSEDF0	ECC Single bit Error Address Detection Flag 0: There is no bit error in EC710EAD0 after reset or clearing ECER1F bit 1: Address captured in EC710EAD0 shows that 1-bit error occurred and captured	R
17	ECDEDF0	ECC Dual Bit Error Address Detection Flag 0: There is no bit error in EC710EAD0 after reset or clearing ECER2F bit 1: Address captured in EC710EAD0 shows that 2-bit error occurred and captured	R
31:18	—	These bits are read as 0. The write value should be 0.	R/W

ECEMF bit (ECC Error Message Flag)

The ECEMF bit shows that there is error in present read data bus. This bit is updated by every RAM output data.

When RAM output data is undefined and the ECERVF bit is set to 1, the value of this bit is undefined.

[Setting condition]

There is bit error in present RAM output data under the condition that error judgement is enabled.

[Clearing condition]

- Under the condition that there is no 1-bit error in input data to decode circuit
- When ECC error judgement is disabled (ECERVF = 0).

ECER1F bit (ECC Error Detection and Correction Flag)

The ECER1F bit shows that the bit errors are detected in the one part of RAM read data [38:0] at RAM read access when the error judgment is enabled.

When the 1-bit error interrupt output is enabled, error interrupt is generated by setting this flag.

This bit is read-only, so writing 1 or 0 has no effect.

At clearing, write 1 to the ECER1C bit.

When 1-bit error is detected again under the condition that this bit is set, the interrupt is not generated.

[Setting condition]

When the error judgment is enabled and there is 1-bit error to RAM output data (when not setting ECER1C = 1).

[Clearing condition]

- Writing ECER1C = 1
- When ECC error judgement is disabled (ECERVF = 0).

ECER2F bit (2-bit ECC Error Detection Flag)

The ECER2F bit shows that the bit errors are detected in the two parts of RAM read data [38:0] at RAM read access when the error judgment is enabled.

When the 2-bit error interrupt output is enabled, error interrupt is generated by setting this flag.

This bit is read-only, so writing 1 or 0 has no effect.

At clearing, write 1 to the ECER2C bit.

When 2-bit error is detected again under the condition that this bit is set, the interrupt is not generated.

[Setting condition]

When the error judgment is enabled and there is 2-bit error to RAM output data (when not setting ECER2C = 1).

[Clearing condition]

Bit	Symbol	Function	R/W
11	ECOVFF	ECC溢出检测标志 0：无效1：ECC溢出检测标志	R
13:12	—	这些位被读取为0。写入值应为0。	R/W
15:14	EMCA[1:0]	ECC模式选择位的访问控制 这些位启用或禁用对ECERVF位的写访问。	R/W
16	ECSEDF0	ECC单位错误地址检测标志 0：复位或清除ECER1F后EC710EAD0中没有位错误位1：EC710EAD0中捕获的地址显示发生并捕获了1位错误	R
17	ECDEDF0	ECC双位错误地址检测标志 0：复位或清除ECER2F位后EC710EAD0中没有位错误1：EC710EAD0中捕获的地址显示发生并捕获了2位错误	R
31:18	—	这些位被读取为0。写入值应为0。	R/W

ECEMF位（ECC错误消息标志）

ECEMF位显示当前读数据总线有错误。该位由每个RAM输出数据更新。

当RAM输出数据未定义且ECERVF位设置为1时，该位的值未定义。

[Setting condition]

在启用错误判断的情况下，当前RAM输出数据存在位错误。

[Clearing condition]

●解码电路的输入数据无1位错误的情况下

●ECC错误判断无效时（ECERVF=0）。

ECER1F位（ECC错误检测和纠正标志）

ECER1F位表示当启用错误判断时，在RAM读取访问时，在RAM读取数据[38:0]的一部分中检测到位错误。

当1位错误中断输出使能时，通过设置该标志产生错误中断。

该位是只读的，因此写入1或0无效。

清零时，将1写入ECER1C位。

在该位置位的情况下再次检测到1位错误时，不会产生中断。

[Setting condition]

启用错误判断且RAM输出数据有1位错误时（未设置ECER1C=1时）。

[Clearing condition]

- Writing ECER1C = 1

●ECC错误判断无效时（ECERVF=0）。

ECER2F位（2位ECC错误检测标志）

ECER2F位表示当错误判断使能时，在RAM读取访问的两部分RAM读取数据[38:0]中检测到位错误。

当2位错误中断输出使能时，通过设置该标志产生错误中断。

该位是只读的，因此写入1或0无效。

清除时，将1写入ECER2C位。

在该位置位的情况下再次检测到2位错误时，不会产生中断。

[Setting condition]

启用错误判断且RAM输出数据有2位错误时（未设置ECER2C=1时）。

[Clearing condition]

- Writing ECER2C = 1
- When ECC error judgement is disabled (ECERVF = 0).

EC1EDIC bit (ECC 1-bit Error Detection Interrupt Control)

The EC1EDIC controls the interrupt output at detecting 1-bit error. By setting 1 to this bit, the 1-bit error interrupt is outputted when 1-bit error detected.

EC2EDIC bit (ECC 2-bit Error Detection Interrupt Control)

The EC2EDIC controls the interrupt output at detecting 2-bit error. By setting 1 to this bit, the 2-bit error interrupt is outputted when 2-bit error detected.

EC1ECP bit (ECC 1-bit Error Correction Permission)

The EC1ECP sets enable or disable to correct the 1-bit error when ECC error detection and correction is valid. By setting 1 to this bit, the non-corrected data is outputted if 1-bit error is detected.

ECERVF bit (ECC Error Judgment Enable Flag)

Setting the ECERVF bit to 1 enables the judgment of error. The correction of output data and the interrupt output depend on setting of the EC1ECP bit, EC2EDIC bit, and EC1EDIC bit.

The write access to this bit is valid when the write value of the EMCA[1:0] is 01b. So only the 16 bits or 32 bits operation command is valid in the case of the write access to this bit.

ECER1C bit (Accumulating ECC Error Detection and Correction Flag Clear)

The ECER1C bit clears the status flag of the ECER1F bit.

The read value is always 0. By writing 0, the internal condition is not changed. When the competition between writing 1 to this bit and setting the ECER1F bit, the former has priority.

The ECER1F bit is cleared by writing 1 to this bit while the ECER1F bit is set. Additionally, the Overflow Detection flag (ECOVFF), ECC Dual Bit Error flag (ECDEDF0) and ECC Single Bit Error flag (ECSEDF0) are also cleared.

ECER2C bit (2-bit ECC Error Detection Flag Clear)

The ECER2C bit clears the status flag of the ECER2F bit.

The read value is always 0. By writing 0, the internal condition is not changed. When the competition between writing 1 to this bit and setting the ECER2F bit, the former has priority.

The ECER2F bit is cleared by writing 1 to this bit while the ECER2F bit is set. Additionally, the Overflow Detection flag (ECOVFF), ECC Dual Bit Error flag (ECDEDF0), and ECC Single Bit Error flag (ECSEDF0) are also cleared.

ECOVFF bit (ECC Overflow Detection Flag)

The ECOVFF bit is set and the overflow interruption is outputted by detecting the new error address under the condition that error address is already captured in the EC710EAD0 register. The overflow interrupt is outputted again when this bit is set and new error is detected.

This bit is read-only, so writing 1 or 0 has no effect.

To clear this bit, write 1 to the ECER2C bit and the ECER1C bit.

[Setting condition]

When new error address is captured under the condition that error address is already captured in the EC710EAD0 register (when not setting ECER2C = 1 or ECER1C = 1).

[Clearing condition]

- Writing ECER2C = 1 or ECER1C = 1
- When ECC error judgement is disabled (ECERVF = 0).

EMCA[1:0] bit (Access Control to ECC Mode Select bit)

The EMCA[1:0] bits are the write trigger reserved bits to the ECERVF bit. The read value is always 0. When the value of these bits is 01b, it is possible to have write access to the ECERVF bit. If these bits are not 01b, write access to the ECERVF bit is ignored and the value is not written.

- Writing ECER2C = 1
- ●ECC错误判断无效时（ECERVF=0）。

EC1EDIC位（ECC1位错误检测中断控制）

EC1EDIC在检测到1位错误时控制中断输出。通过将该位设置为1，当检测到1位错误时输出1位错误中断。

EC2EDIC位（ECC2位错误检测中断控制）

EC2EDIC在检测到2位错误时控制中断输出。通过将此位设置为1，当检测到2位错误时输出2位错误中断。

EC1ECP位（ECC1位纠错权限）

当ECC错误检测和纠正有效时，EC1ECP设置启用或禁用以纠正1位错误。通过将此位设置为1，如果检测到1位错误，则输出未校正的数据。

ECERVF位（ECC错误判断使能标志）

将ECERVF位设置为1可以进行错误判断。输出数据的校正和中断输出取决于EC1ECP位、EC2EDIC位和EC1EDIC位的设置。

当EMCA[1:0]的写值为01b时，对该位的写访问有效。因此在对该位进行写访问的情况下，只有16位或32位操作命令有效。

ECER1C位（累积ECC错误检测和纠正标志清除）

ECER1C位清除ECER1F位的状态标志。

读取值始终为0。通过写入0，内部条件不会改变。当向该位写1与设置ECER1F位竞争时，前者具有优先权。

当ECER1F位置位时，通过向该位写入1来清除ECER1F位。此外，溢出检测标志(ECOVFF)、ECC双比特错误标志(ECDEDF0)和ECC单比特错误标志(ECSEDF0)也被清除。

ECER2C位（2位ECC错误检测标志清除）

ECER2C位清除ECER2F位的状态标志。

读取值始终为0。通过写入0，内部条件不会改变。当向该位写1与设置ECER2F位竞争时，前者具有优先权。

当ECER2F位置位时，通过向该位写入1来清除ECER2F位。此外，溢出检测标志(ECOVFF)、ECC双比特错误标志(ECDEDF0)和ECC单比特错误标志(ECSEDF0)也被清除。

ECOVFF位（ECC溢出检测标志）

在EC710EAD0寄存器中已经捕捉到错误地址的情况下，通过检测新的错误地址，设置ECOVFF位并输出溢出中断。当该位置位并检测到新错误时，溢出中断再次输出。

该位是只读的，因此写入1或0无效。

要清除该位，向ECER2C位和ECER1C位写入1。

[Setting condition]

在EC710EAD0寄存器中已捕获错误地址的情况下捕获新的错误地址时（未设置ECER2C=1或ECER1C=1时）。

[Clearing condition]

- ●写入ECER2C=1或ECER1C=1
- ●ECC错误判断无效时（ECERVF=0）。

EMCA[1:0]位（ECC模式选择位的访问控制）

EMCA[1:0]位是ECERVF位的写触发保留位。读取值始终为0。当这些位的值为01b时，可以对ECERVF位进行写访问。如果这些位不是01b，则忽略对ECERVF位的写访问并且不写入该值。

ECSEDF0 bit (ECC Single bit Error Address Detection Flag)

The ECSEDF0 bit shows that the error is captured in the error address register when error detection is valid. This bit is set by 1-bit error detection.

When 1-bit error is detected after the 2-bit error address is already captured in the EC710EAD0 register, this bit is not updated but the EC710EAD0 register is updated.

This bit is read-only, so writing 1 or 0 has no effect. To clear these bits, write 1 to the ECER1C bit.

[Setting condition]

When there is 1-bit error to RAM output data and error address is captured in EC710EAD0 under the condition that the error judgment is permitted (when not setting ECER1C = 1).

[Clearing condition]

- Writing ECER1C = 1
- When ECC error judgement is disabled (ECERVF = 0).

ECDEDF0 bit (ECC Dual Bit Error Address Detection Flag)

The ECDEDF0 bit shows that the error is captured in the error address register when error detection is valid. This bit is set by 2-bit error detection.

When 2-bit error is detected after the 1-bit error address is already captured in the EC710EAD0 register, this bit is not updated and the EC710EAD0 register is updated.

This bit is read-only, so writing 1 or 0 has no effect. To clear these bits, write 1 to the ECER2C bit.

[Setting condition]

When there is 2-bit error to RAM output data and error address is captured in EC710EAD0 under the condition that the error judgment is permitted (when not setting ECER2C = 1).

[Clearing condition]

- Writing ECER2C = 1
- When ECC error judgement is disabled (ECERVF = 0).

29.2.2 EC710TMC : ECC Test Mode Control Register

Base address: ECCMB = 0x4012_F200

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ETMA[1:0]		—	—	—	—	—	—	ECTMCE	—	—	—	—	—	ECDCS	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	ECDCS	ECC Decode Input Select 0: Input lower 32 bits of RAM output data to data area of decode circuit 1: Input ECEDB31-0 in EC710TED register to data area of decode circuit	R/W
6:2	—	These bits are read as 0. The write value should be 0.	R/W
7	ECTMCE	ECC Test Mode Control Enable 0: The access to test mode register and bit is disabled 1: The access to test mode register and bit is enabled	R/W
13:8	—	These bits are read as 0. The write value should be 0.	R/W
15:14	ETMA[1:0]	ECC Test Mode Bit Access Control These bits enable or disable write access to ECTMCE bit.	R/W

ECSEDF0位（ECC单个位错误地址检测标志）

ECSEDF0位表示当错误检测有效时，错误被捕获到错误地址寄存器中。该位由1位错误检测设置。

当在EC710EAD0寄存器中已捕获2位错误地址后检测到1位错误时，该位不会更新，但EC710EAD0寄存器会更新。

该位是只读的，因此写入1或0无效。要清除这些位，请将1写入ECER1C位。

[Setting condition]

在允许错误判断的条件下（未设置ECER1C=1时），当RAM输出数据出现1位错误并在EC710EAD0中捕获错误地址时。

[Clearing condition]

- Writing ECER1C = 1
- ●ECC错误判断无效时（ECERVF=0）。

ECDEDF0位（ECC双位错误地址检测标志）

ECDEDF0位表示当错误检测有效时，错误被捕获在错误地址寄存器中。该位由2位错误检测设置。

当在EC710EAD0寄存器中已捕获1位错误地址后检测到2位错误时，该位不更新，EC710EAD0寄存器更新。

该位是只读的，因此写入1或0无效。要清除这些位，请将1写入ECER2C位。

[Setting condition]

在允许错误判断的条件下（未设置ECER2C=1时），当RAM输出数据有2位错误并且错误地址被捕获到EC710EAD0中时。

[Clearing condition]

- Writing ECER2C = 1
- ●ECC错误判断无效时（ECERVF=0）。

29.2.2 EC710TMC：ECC测试模式控制寄存器

Base address: ECCMB = 0x4012_F200

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ETMA[1:0]		—	—	—	—	—	—	ECTMCE	—	—	—	—	—	ECDCS	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	该位读取为0。写入值应为0。	R/W
1	ECDCS	ECC解码输入选择 0：将RAM输出数据的低32位输入到解码电路的数据区1：将EC710TED寄存器中的ECEDB31-0输入到解码电路的数据区	R/W
6:2	—	这些位被读取为0。写入值应为0。	R/W
7	ECTMCE	ECC测试模式控制启用 0：禁止访问测试模式寄存器和位1：允许访问测试模式寄存器和位	R/W
13:8	—	这些位被读取为0。写入值应为0。	R/W
15:14	ETMA[1:0]	ECC测试模式位访问控制 这些位启用或禁用对ECTMCE位的写访问。	R/W

ECDCS bit (ECC Decode Input Select)

The ECDCS bit selects either the lower 32 bits data value from RAM or value from the internal test register (EDEDB[31:0] in EC710TED) as input signal to decoder.

The write access to this bit is valid under the condition of ECTMCE = 1 (it is possible to set them at the same time.)

This bit is cleared by setting ECTMCE = 0.

ECTMCE bit (ECC Test Mode Control Enable)

The ECTMCE bit selects the access enable or disable to test register and test control bit.

The write access to this bit is valid under the condition that the value of the ETMA[1:0] bits is 10b.

ETMA[1:0] bits (ECC Test Mode Bit Access Control)

The ETMA[1:0] bits are the write trigger reserved bits to the ECTMCE bit. The read value is always 0. When the value of these bits is 10b, it is possible to have write access to the ECTMCE bit. If these bits are not 10b, the write access to the ECTMCE bit is ignored and the value is not written.

29.2.3 EC710TED : ECC Test Substitute Data Register

Base address: ECCMB = 0x4012_F200

Offset address: 0x0C

Bit position:	31																													0
Bit field:	ECEDB[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	ECEDB[31:0]	ECC Test Substitute Data Substitute data in ECC test mode.	R/W

This register is for the 32 bits data for ECC decode. It is possible to read and write using 32 bits operation command when ECTMCE = 1. When ECTMCE = 0, all bits are always 0.

ECEDB[31:0] bits (ECC Test Substitute Data)

When ECDCS in EC710TMC register is 1, the value of this register is bits [31:0] of the input data to the decode circuit.

29.2.4 EC710EAD0 : ECC Error Address Register

Base address: ECCMB = 0x4012_F200

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	ECEAD[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	ECEAD[10:0]	ECC Error Address	R
31:11	—	These bits are read as 0. The write value should be 0.	R

This is a read-only register to hold the ECC error address.

ECDCS位（ECC解码输入选择）

ECDCS位选择来自RAM的低32位数据值或来自内部测试寄存器（EC710TED中的EEDB[31:0]）的值作为解码器的输入信号。

对该位的写访问在ECTMCE=1的条件下有效（可以同时置位）。

该位通过设置ECTMCE=0清零。

ECTMCE位（ECC测试模式控制使能）

ECTMCE位选择对测试寄存器和测试控制位的访问启用或禁用。

在ETMA[1:0]位的值为10b的情况下，对该位的写访问是有效的。

ETMA[1:0]位（ECC测试模式位访问控制）

ETMA[1:0]位是ECTMCE位的写触发保留位。读取值始终为0。当这些位的值为10b时，可以对ECTMCE位进行写访问。如果这些位不是10b，则忽略对ECTMCE位的写访问并且不写入该值。

29.2.3 EC710TED:ECC测试替代数据寄存器

Base address: ECCMB = 0x4012_F200

Offset address: 0x0C

Bit position:	31																													0
Bit field:	ECEDB[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	ECEDB[31:0]	ECC测试替代数据 在ECC测试模式下替换数据。	R/W

该寄存器用于ECC解码的32位数据。可以使用32位操作命令读取和写入时ECTMCE=1。当ECTMCE=0时，所有位始终为0。

ECEDB[31:0]位（ECC测试替代数据）

当EC710TMC寄存器中的ECDCS为1时，该寄存器的值为解码电路输入数据的位[31:0]。

29.2.4 EC710EAD0：ECC错误地址寄存器

Base address: ECCMB = 0x4012_F200

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	ECEAD[10:0]										
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	ECEAD[10:0]	ECC错误地址	R
31:11	—	这些位被读取为0。写入值应为0。	R

这是一个只读寄存器，用于保存ECC错误地址。

ECEAD[10:0] bits (ECC Error Address)

When ECC error is detected for permitting ECC error judgment, RAM address is captured by the detected signal as a trigger and is hold as the error occurring address. The error address is not captured when the error occurred again to the one held by the same factor.

If 2-bit error occurred under the condition that 1-bit error address is already captured, the 2-bit error address is over-written and the ECDEDF0 bit is set to 1.

If 1-bit error occurred under the condition that 2-bit error address is already captured, the 1-bit error address is not overwritten and the ECSEDF0 bit is not set to 1.

29.3 Operation

29.3.1 ECC Function Setting

Figure 29.1 shows a procedure for ECC function setting.

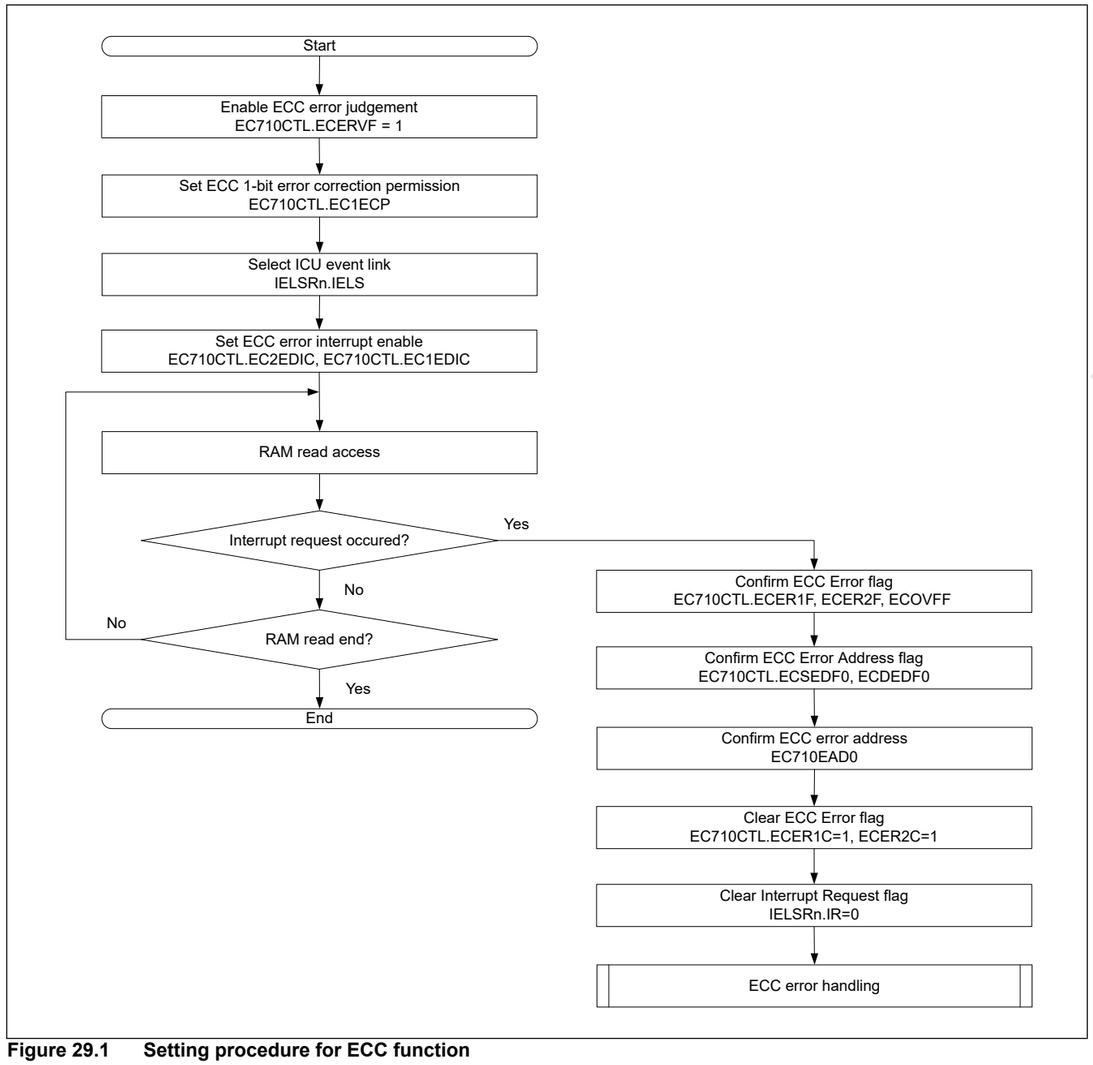


Figure 29.1 Setting procedure for ECC function

ECEAD[10:0]位（ECC错误地址）

当检测到ECC错误以允许ECC错误判断时，RAM地址被检测信号捕获作为触发，并作为错误发生地址保持。当错误再次发生到相同因素持有的地址时，错误地址不会被捕获。

如果在已捕获1位错误地址的情况下发生2位错误，则覆盖2位错误地址并将ECDEDF0位设置为1。

如果在已捕获2位错误地址的情况下发生1位错误，则不会覆盖1位错误地址且ECSEDF0位不会设置为1。

29.3 Operation

29.3.1 ECC功能设置

图29.1显示了ECC功能设置的过程。

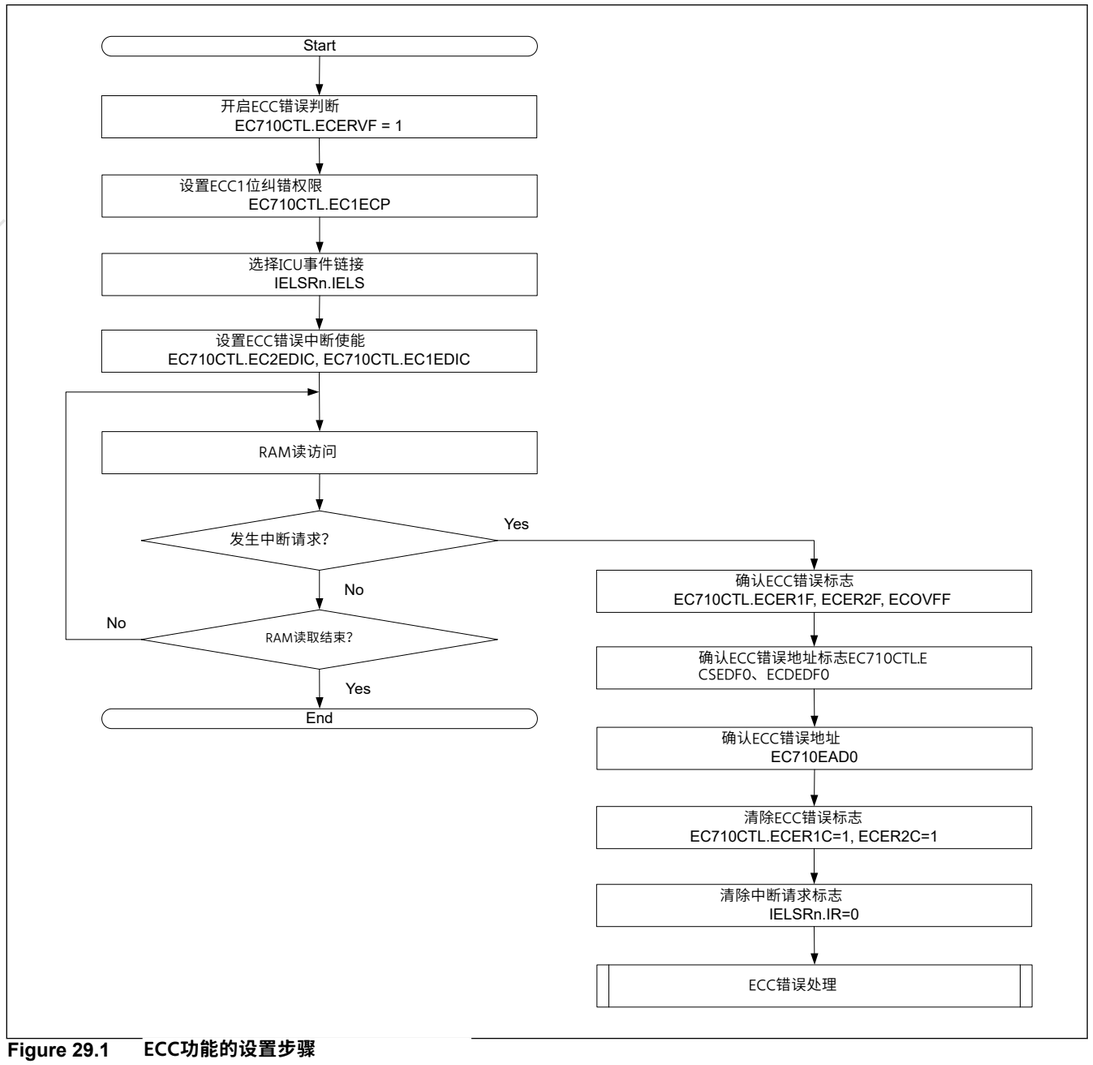


Figure 29.1 ECC功能的设置步骤

29.3.2 ECC Decoder Testing

ECC interrupts can be intentionally generated by ECC test mode. Figure 29.2 shows a procedure for ECC decoder testing.

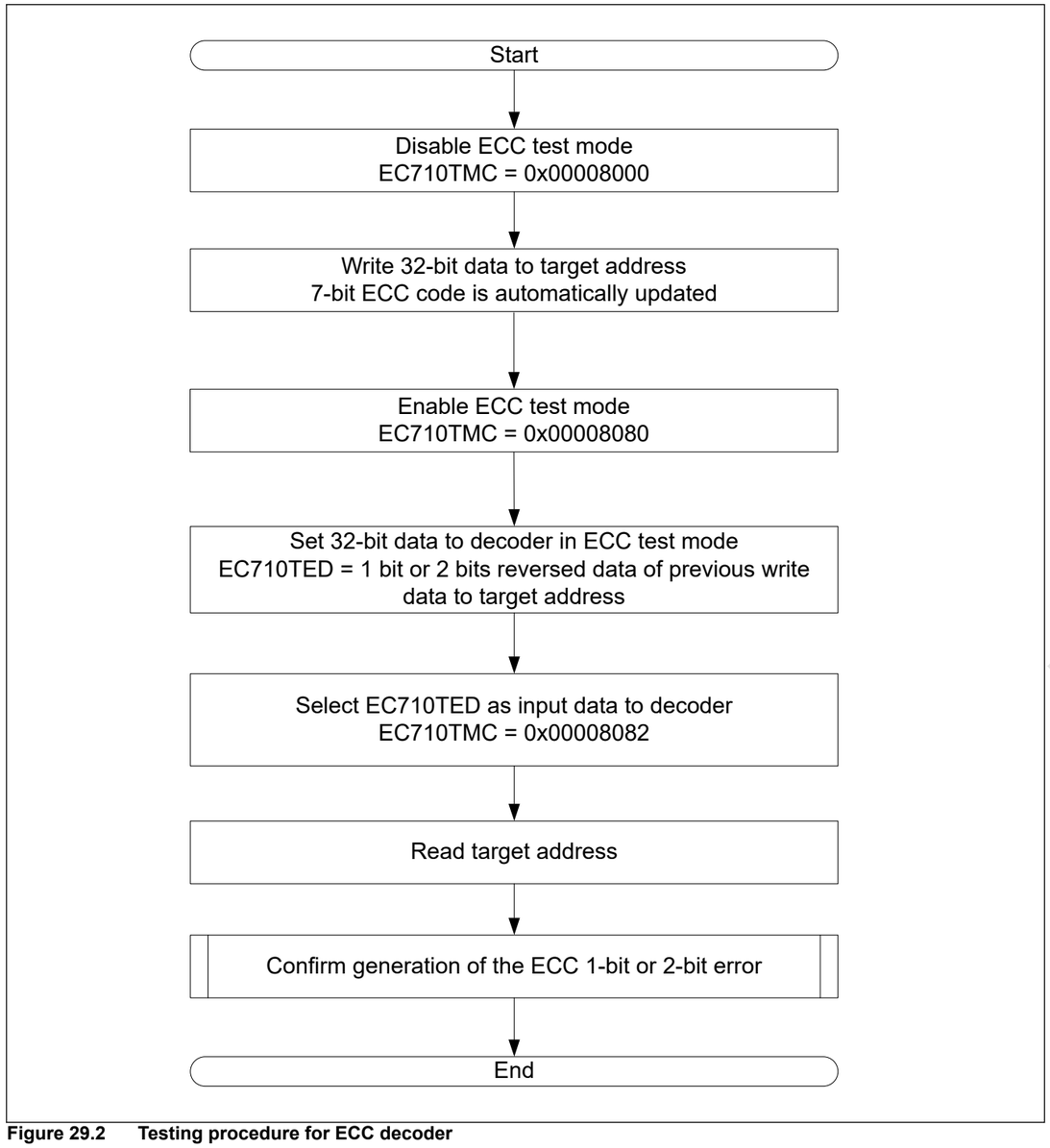


Figure 29.2 Testing procedure for ECC decoder

29.4 Interrupts

The ECC module issues three interrupt requests:

- CAN_MRAM_ERI.

Interrupt sources of each interrupt request include:

- 1-bit ECC error

29.3.2 ECC解码器测试

ECC测试模式可以有意生成ECC中断。图29.2显示了ECC解码器测试的过程。

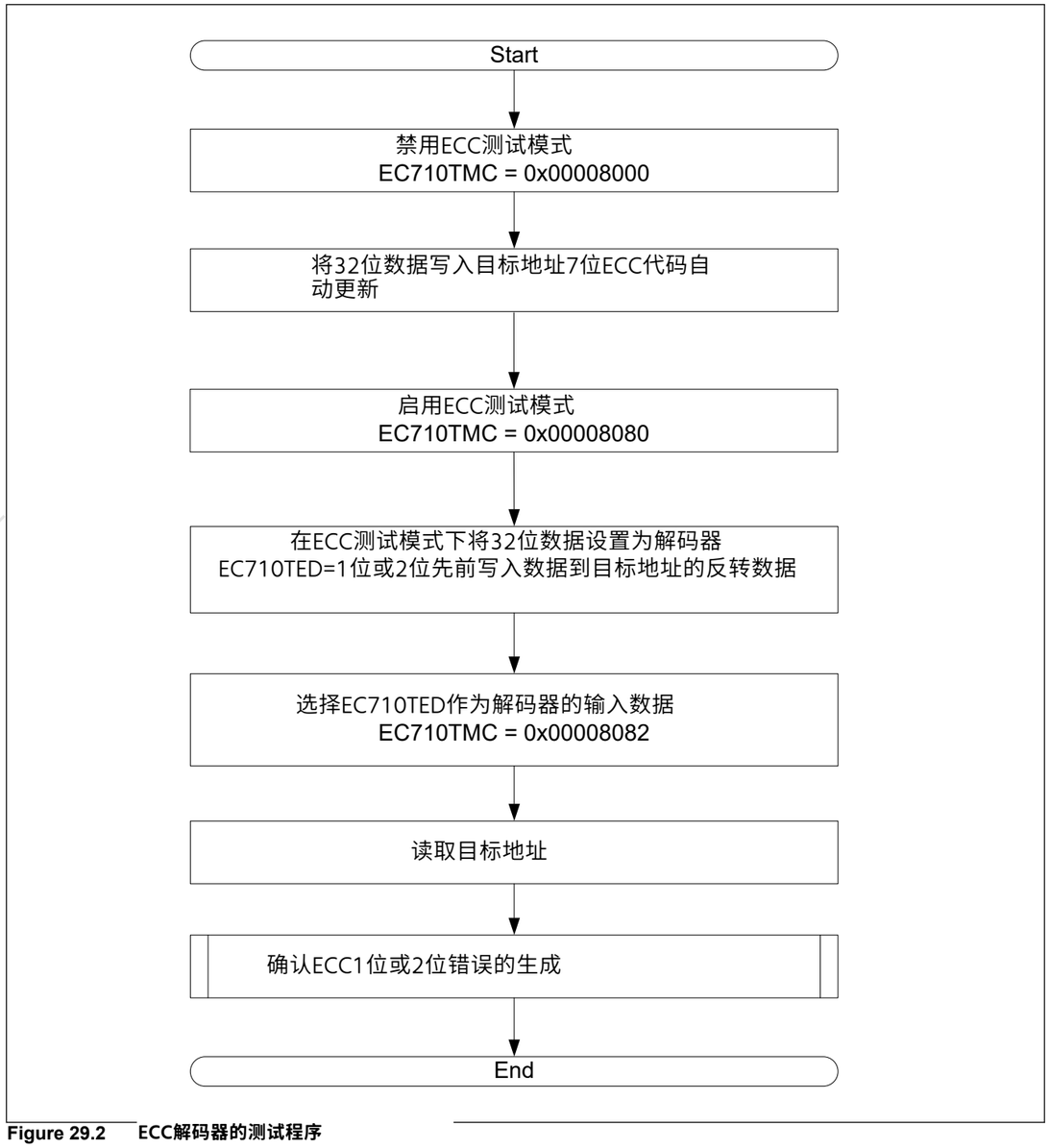


Figure 29.2 ECC解码器的测试程序

29.4 Interrupts

ECC模块发出三个中断请求：

- CAN_MRAM_ERI.

每个中断请求的中断源包括：

- 1-bit ECC error

- 2-bit ECC error
- ECC error overflow.

- 2-bit ECC error
- ECC错误溢出。

30. Serial Peripheral Interface (SPI)

This is the SPI_B version of the SPI peripheral module.

SPI_B is referred to as SPI in this chapter.

30.1 Overview

The Serial Peripheral Interface (SPI) has 2 channels. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. Table 30.1 lists the SPI specifications, Figure 30.1 shows a block diagram, and Table 30.2 lists the I/O pins.

In this section, PCLK refers to PCLKA. TCLK refers to SPITCLK.

Table 30.1 SPI specifications (1 of 2)

Parameter	Specifications
Number of channels	Two channels
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Receive-only operation is available • Communication mode selectable to full-duplex, transmit-only or receive-only • RSPCK polarity switching • RSPCK phase switching
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable from 4 to 32 bits • 32 bit × 4 stages FIFO is available as transmit buffer or receive buffer • Byte swap operating function • Transmit/receive data can be inverted.
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing TCLK (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum TCLK clock divided by 2 can be input as RSPCK (TCLK divided by 2 is the maximum RSPCK frequency) Width at high level: 1 TCLK cycles; width at low level: 1 TCLK cycles
Buffer configuration	• Double buffer configuration for the transmit and receive buffers
Error detection	• Mode fault error detection • Underrun error detection • Overrun error detection*1 • Parity error detection • Receive data ready detection
SSL control function	[motorola SPI mode/TI SSP mode common] • Four SSL pins (SSLni: SSLn0 to SSLn3) (n = A, B) for each channel • In single-master mode, SSLn0 to SSLn3 pins are output • In multi-master mode, SSLn0 pin for input, and SSLn1 to SSLn3 pins either for output or unused • In slave mode, SSLn0 pin for input and SSLn1 to SSLn3 pins unused • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity • Delay between frames in burst transfer is settable [only Motorola mode] • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) [only TI SSP mode] • Controllable delay from OE output assertion to RSPCK operation (RSPCK delay) Range: 0 to 8 RSPCK cycles (set in RSPCK-cycle units)
Communication protocol	• Motorola SPI • TI SSP(Synchronous Serial Protocol)

30. 串行外设接口(SPI)

这是SPI外设模块的SPI_B版本。

SPI_B在本章中称为SPI。

30.1 Overview

串行外设接口(SPI)有2个通道。SPI提供与多个处理器和外围设备的高速全双工同步串行通信。表30.1列出了SPI规格，图30.1显示了框图，表30.2列出了IO引脚。

在本节中，PCLK指的是PCLKA。TCLK指的是SPITCLK。

Table 30.1 SPI规格（2个中的1个）

Parameter	Specifications
通道数	两个通道
SPI传输函数	• 使用MOSI（主输出从输入）、MISO（主输入从输出）、SSL（从选择）和RSPCK（SPI时钟）信号允许通过SPI操作（4线方法）或时钟同步操作（3-线法） • 仅传输操作可用 • 仅接收操作可用 • 可选择全双工、仅发送或仅接收的通信模式 • RSPCK极性切换 • RSPCK相位切换
数据格式	• 可选择MSB优先或LSB优先 • 传输位长度可选择4至32位 • 32位×4级FIFO可用作发送缓冲器或接收缓冲器 • 字节交换操作功能 • 发送接收数据可以反转。
比特率	• 在主机模式下，片内波特率发生器通过分频产生RSPCK TCLK（分频比范围从2分频到4096分频） • 从机模式下，可以输入最小TCLK时钟2分频作为RSPCK（TCLK2分频为最大RSPCK频率）高电平宽度：1个TCLK周期；低电平宽度：1TCLK周期
缓冲区配置	• 发送和接收缓冲区的双缓冲区配置
错误检测	• 模式故障错误检测 • 欠载错误检测 • 溢出错误检测*1 • 奇偶校验错误检测 • 接收数据就绪检测
SSL控制功能	【摩托罗拉SPI模式TISSP模式常用】● 每个通道有四个SSL引脚（SSLni：SSLn0到SSLn3）（n=A、B） • 在单主模式下，输出SSLn0到SSLn3引脚 • 在多主模式下，SSLn0引脚用于输入，SSLn1至SSLn3引脚用于输出或未使用 • 在从机模式下，SSLn0引脚用于输入，SSLn1到SSLn3引脚未使用 • 从SSL输出断言到RSPCK操作的可控延迟（RSPCK延迟） 范围：1到8个RSPCK循环（以RSPCK循环为单位设置） • 从RSPCK停止到SSL输出否定的可控延迟（SSL否定延迟） 范围：1到8个RSPCK循环（以RSPCK循环为单位设置） • 下一次访问SSL输出断言的可控等待（下一次访问延迟） 范围：1到8个RSPCK循环（以RSPCK循环为单位设置） • 更改SSL极性的功能 ●可设置突发传输中帧之间的延迟[仅限摩托罗拉模式] ● 从SSL输出断言到RSPCK操作的可控延迟（RSPCK延迟） 范围：1到8个RSPCK周期（以RSPCK周期为单位设置）[仅限TI SSP模式]● 从OE输出断言到RSPCK操作的可控延迟（RSPCK延迟） 范围：0到8个RSPCK周期（以RSPCK周期为单位设置）
通讯协议	• Motorola SPI • TISSP（同步串行协议）

Table 30.1 SPI specifications (2 of 2)

Parameter	Specifications
Control in master transfer	● Transfers of up to eight commands each can be executed sequentially in looped execution ● For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity and phase, transfer data length, MSB- or LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay ● Transfers can be initiated by writing to the transmit buffer ● MOSI signal value specifiable in SSL negation ● RSPCK auto-stop function
Interrupt sources	Interrupt sources: ● Receive buffer full / Receive data ready interrupt ● Transmit buffer empty interrupt ● SPI error interrupt (mode fault error, under run error, over run error, parity error, receive data ready) ● SPI idle interrupt (SPI idle) ● Communication end interrupt
Event link function	The following events can be output to the Event Link Controller (ELC): ● Receive buffer full / receive data ready signal ● Transmit buffer empty signal ● Mode fault, underrun, overrun, parity error, or receive data ready signal ● SPI idle signal ● Communication end signal
Other functions	● Switching between CMOS output and open-drain output ● SPI initialization function ● Loopback mode
Module-stop function	Module-stop state can be set to reduce power consumption.
TrustZone Filter	Security attribution can be set

Note 1. In master reception and when the RSPCK auto-stop function is enabled, an overrun error does not occur because the transfer clock is stopped on overrun error detection.

Table 30.1 SPI规范（2个中的2个）

Parameter	Specifications
主传输中的控制	● 最多可传输8个命令，每个命令可以在循环执行中顺序执行 ● 对于每个命令，可以设置以下内容： SSL信号值、比特率、RSPCK极性和相位、传输数据长度、MSBorLSB在前、突发、RSPCK延迟、SSL否定延迟和下一次访问延迟 ● 可以通过写入发送缓冲区来启动传输 ● 在SSL否定中可指定的MOSI信号值 ● RSPCK auto-stop function
中断源	Interrupt sources: ● 接收缓冲区满接收数据就绪中断 ● 发送缓冲区空中断 ● SPI错误中断（模式故障错误、欠载错误、超载错误、奇偶校验错误、接收数据就绪） ● SPI空闲中断（SPI空闲） ● 通讯结束中断
事件链接功能	以下事件可以输出到事件链接控制器(ELC)：● 接收缓冲器满接收数据就绪信号 ● 发送缓冲器空信号 ● 模式故障、欠载、溢出、奇偶校验错误或接收数据就绪信号 ● SPI空闲信号 ● 通讯结束信号
其他功能	● 在CMOS输出和开漏输出之间切换 ● SPI初始化函数 ● Loopback mode
Module-stop function	可设置模块停止状态以降低功耗。
TrustZone Filter	可设置安全属性

注1.在主机接收和启用RSPCK自动停止功能时，不会发生溢出错误，因为在检测到溢出错误时会停止传输时钟。

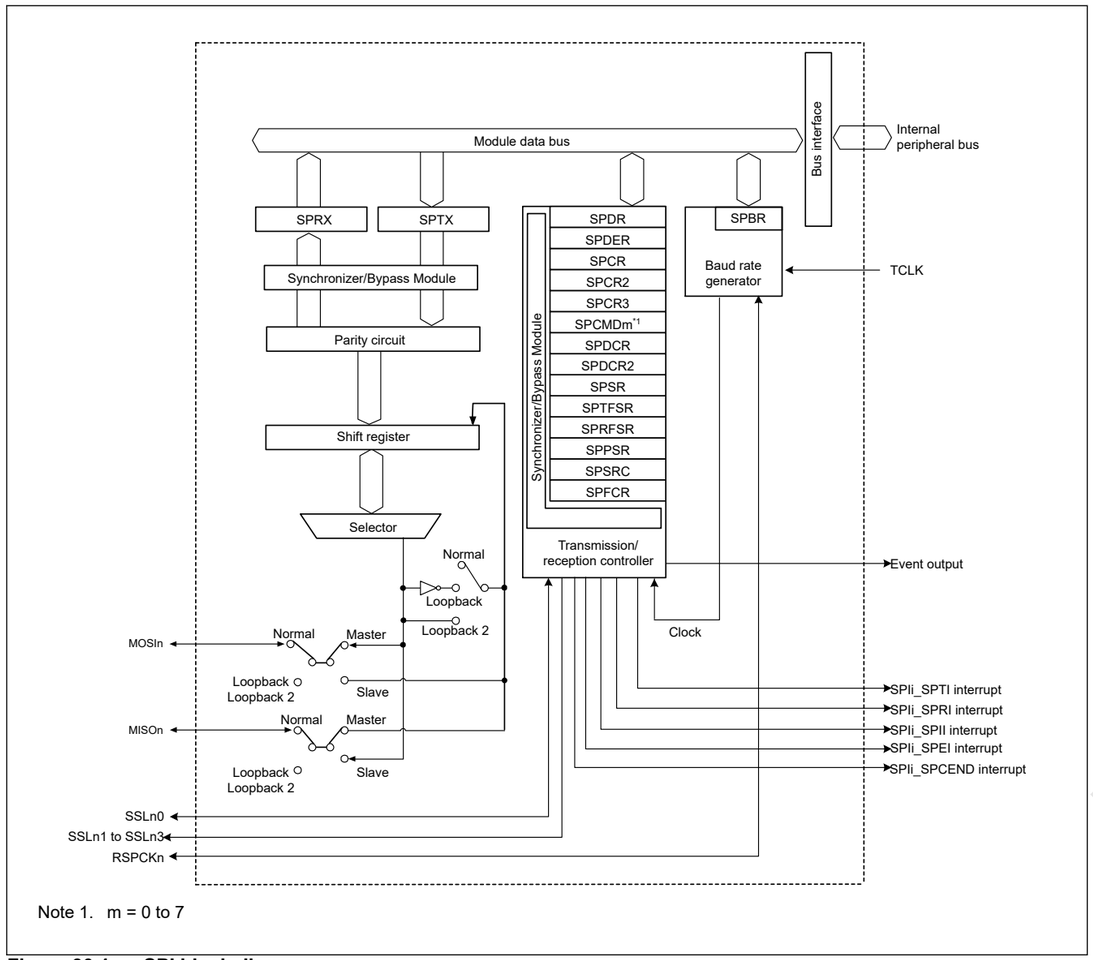


Figure 30.1 SPI block diagram

The SPI automatically switches the I/O direction of the SSLn0 pin. SSLn0 is set as an output when the SPI is a single master, and as an input when the SPI is a multi-master or a slave. The RSPCKn, MOSIn, and MISOn pins are automatically set as inputs or outputs based on the master or slave setting and the level input on the SSLn0 pin. For details, see section 30.3.2. Controlling the SPI Pins.

Table 30.2 SPI I/O pins (1 of 2)

Channel	Pin name	I/O	Description
SPI0	RSPCKA	I/O	Clock input/output pin
	SSLA0	I/O	Slave selection input/output
	SSLA1 to SSLA3	Output	Slave selection output
	MOSIA	I/O	Master transmit data input/output
	MISOA	I/O	Slave transmit data input/output
SPI1	RSPCKB	I/O	Clock input/output pin
	MOSIB	I/O	Master transmit data input/output
	MISOB	I/O	Slave transmit data input/output
	SSLB0	I/O	Slave selection input/output

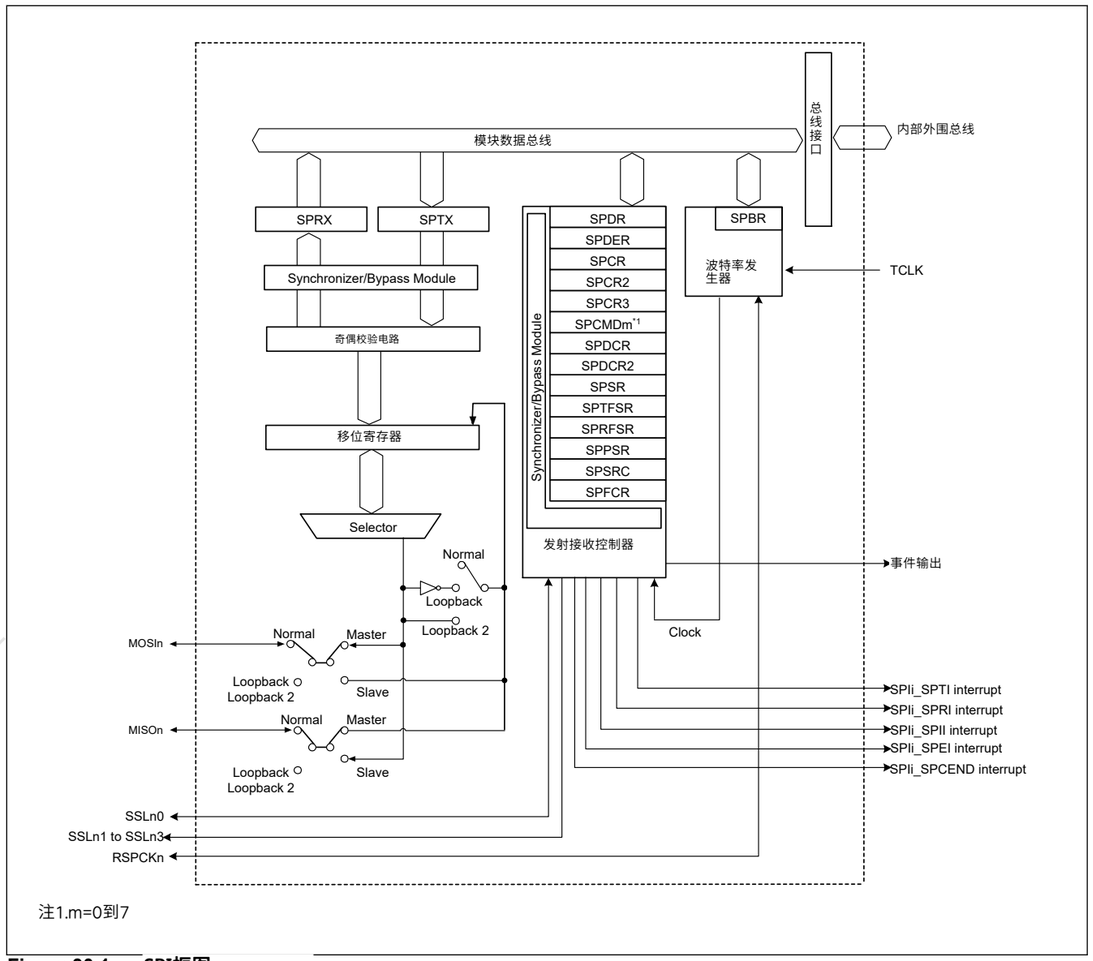


Figure 30.1 SPI框图

SPI自动切换SSLn0引脚的IO方向。当SPI为单主机时SSLn0设置为输出，当SPI为多主机或从机时设置为输入。RSPCKn、MOSIn和MISOn引脚会根据主机或从机设置以及SSLn0引脚上的电平输入自动设置为输入或输出。有关详细信息，请参阅第30.3.2节。控制SPI引脚。

Table 30.2 SPIIO引脚（2个中的1个）

Channel	引脚名称	I/O	Description
SPI0	RSPCKA	I/O	时钟输入输出引脚
	SSLA0	I/O	从机选择输入输出
	SSLA1 to SSLA3	Output	从机选择输出
	MOSIA	I/O	主机发送数据输入输出
	MISOA	I/O	从机发送数据输入输出
SPI1	RSPCKB	I/O	时钟输入输出引脚
	MOSIB	I/O	主机发送数据输入输出
	MISOB	I/O	从机发送数据输入输出
	SSLB0	I/O	从机选择输入输出

Table 30.2 SPI I/O pins (2 of 2)

Channel	Pin name	I/O	Description
	SSLB1 to SSLB3	Output	Slave selection output

Note: Pin names are indicated as "...A" or "...An" for SPI0, and "...B" or "...Bn" for SPI1 (n = 0, 1, 2, or 3).

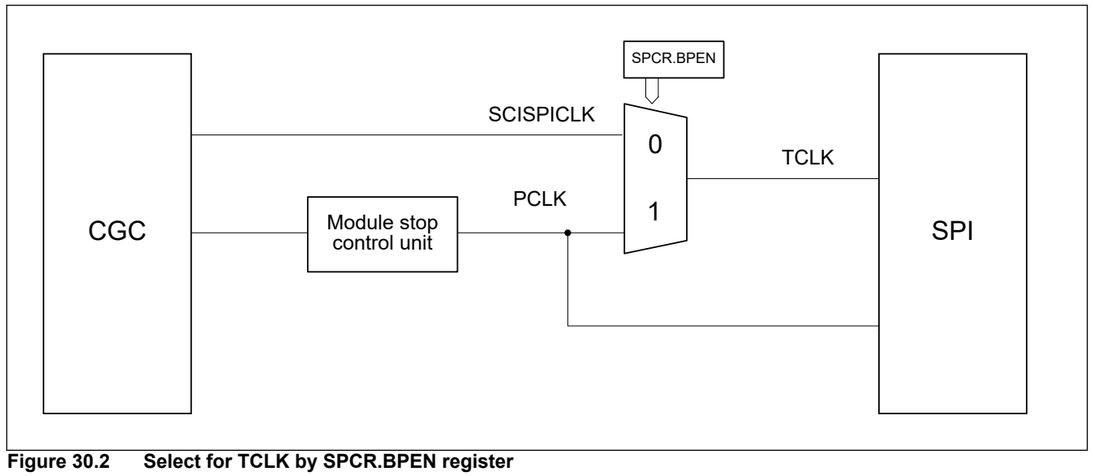


Figure 30.2 Select for TCLK by SPCR.BPEN register

30.2 Register Descriptions

30.2.1 SPDR : RSPI Data Register

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SPD[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SPD[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPDR is the interface with the buffers that hold data for transmission and reception by the SPI. When accessing this register in words, access SPDR. The transmit buffer (SPTX) and receive buffer (SPRX) are independent but both are mapped to SPDR. Figure 30.3 shows the configuration of the SPDR register.

Table 30.2 SPIIO引脚（2个中的2个）

Channel	引脚名称	I/O	Description
	SSLB1 to SSLB3	Output	从机选择输出

Note: SPI0的引脚名称表示为"...A"或"...An"，SPI1的引脚名称表示为"...B"或"...Bn"（n=0、1、2或3）。

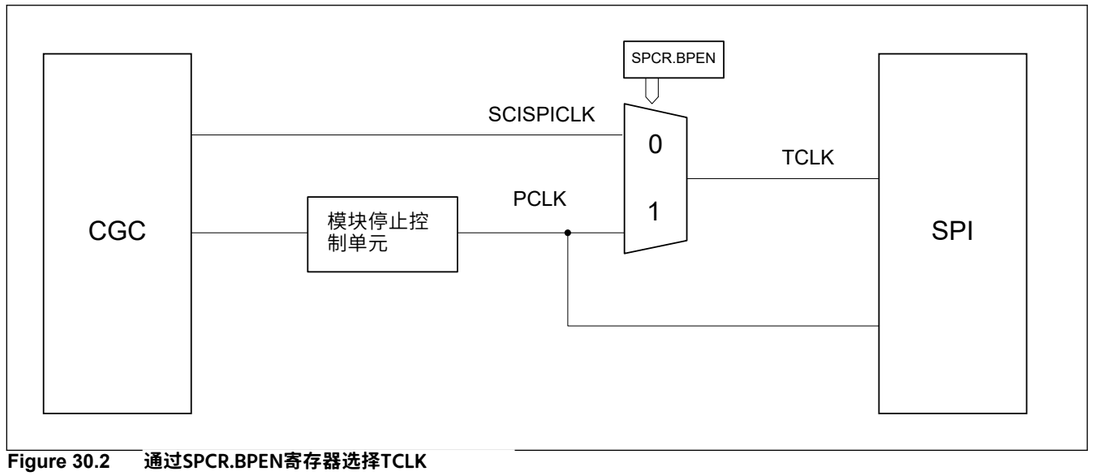


Figure 30.2 通过SPCR.BPEN寄存器选择TCLK

30.2 注册说明

30.2.1 SPDR:RSPI数据寄存器

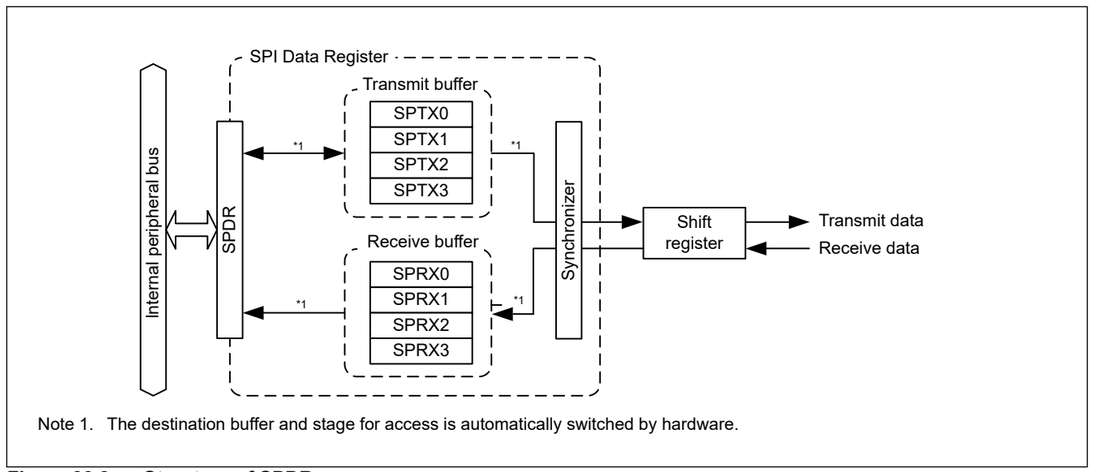
Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SPD[31:16]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SPD[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPDR是与保存数据以供SPI发送和接收的缓冲区的接口。以字访问该寄存器时，访问SPDR。发送缓冲区(SPTX)和接收缓冲区(SPRX)是独立的，但都映射到SPDR。图30.3显示了SPDR寄存器的配置。



Note 1. The destination buffer and stage for access is automatically switched by hardware.

Figure 30.3 Structure of SPDR

32bit × 4 stage transmit FIFO and 32bit × 4 receive FIFO are provided. These 8 stage FIFO are mapped to one address in the SPDR. Transmit buffers (SPTXn, n = 0 to 3) can be written by writing data to SPDR to transmit written data.

Upon completion of receiving data, receive buffers store received data. When an overrun error occurs, data in the receive buffer is not updated.

(1) Bus Interface

The RSPI data register has 32bit x 4 stage transmit FIFO and 32bit x 4 receive FIFO (32 bytes in total). These 32 bytes are mapped to the 4-byte space of SPDR. Write transmit data from the LSB. Received data is stored from the LSB.

SPDR register write operation and read operation are described below.

1. Write
   A transmit buffer write pointer is provided for transmit buffers. When data is written to SPDR, the pointer automatically switches to the next buffer. The following illustrates the structure of the transmit buffer bus interface (write).

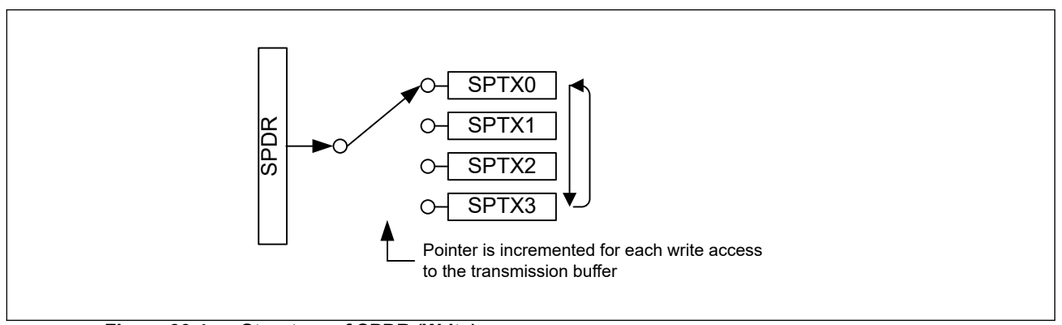
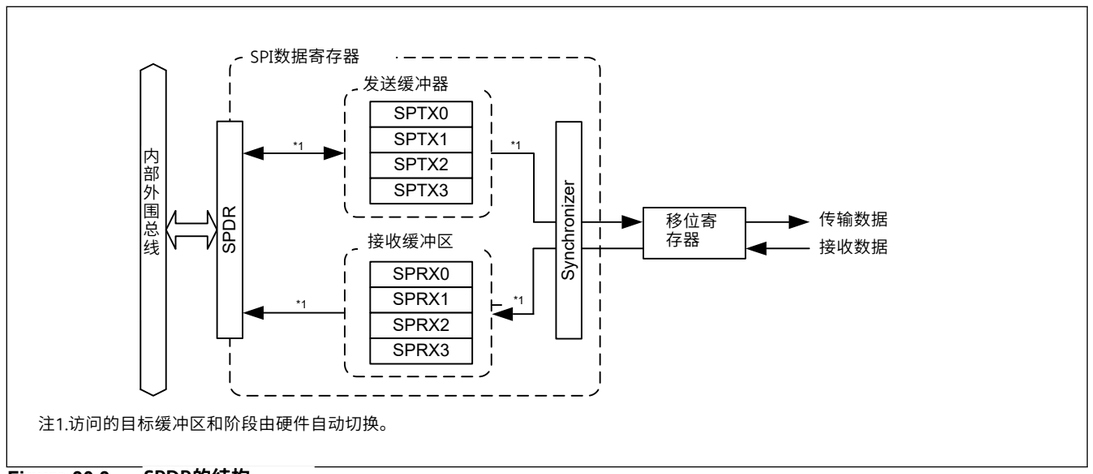


Figure 30.4 Structure of SPDR (Write)

The transmit buffer (SPTX0 to SPTX3) switching order:
SPTX0→SPTX1→SPTX2→SPTX3→SPTX0→SPTX1→…
When writing transmit data to transmit buffers (SPTXn), write transmit data of frames +1 specified by the Transmission FIFO threshold setting bits of RSPI data control register 2 (SPDCR2.TTRG [1: 0]) while an RSPI transmit buffer empty interrupt is present (SPSR.SPTEF flag = 1). Writing to the transmit buffer (SPTXn, n = 0 to 3) in the state where there is no empty stage in the transmit FIFO does not update the buffer value.

2. Read
   Values can be read from receive buffers (SPRXn, n = 0 to 3) or transmit buffers (SPTXn, n = 0 to 3) by reading the SPDR register. Reading a receive buffer or reading a transmit buffer can be selected by the RSPI receive data or transmit data select bit (SPDCR.SPRDTD) in the RSPI data control register.
   The SPDR register is read according to the independent receive buffer read pointer and the transmit buffer read pointer.



注1.访问的目标缓冲区和阶段由硬件自动切换。

Figure 30.3 SPDR的结构

提供32位×4级发送FIFO和32位×4级接收FIFO。这些8级FIFO映射到SPDR中的一个地址。发送缓冲器（SPTXn，n=0到3）可以通过向SPDR写入数据来写入，以发送写入的数据。

接收数据完成后，接收缓冲区存储接收到的数据。发生溢出错误时，接收缓冲区中的数据不会更新。

(1) 总线接口

RSPI数据寄存器有32bitx4级发送FIFO和32bitx4接收FIFO（共32字节）。这32个字节映射到SPDR的4个字节空间。从LSB写入发送数据。接收到的数据从LSB存储。

SPDR寄存器的写操作和读操作如下所述。

1. Write
   为发送缓冲器提供了发送缓冲器写指针。当数据写入SPDR时，指针自动切换到下一个缓冲区。下面说明了发送缓冲区总线接口（写）的结构。

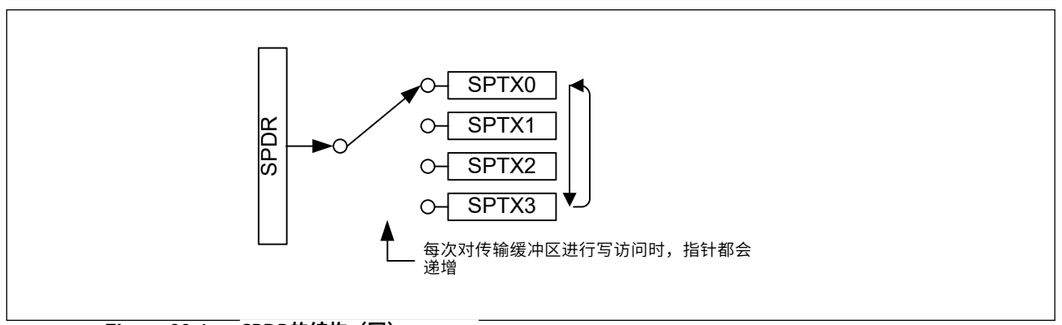


Figure 30.4 SPDR的结构（写）

发送缓冲器（SPTX0到SPTX3）切换顺序：
SPTX0→SPTX1→SPTX2→SPTX3→SPTX0→SPTX1→…
将发送数据写入发送缓冲区(SPTXn)时，写入由RSPI数据控制寄存器2(SPDCR2.TTRG[1:0])的发送FIFO阈值设置位指定的帧+1的发送数据，同时RSPI发送缓冲区空中断存在（SPSR.SPTEF标志=1）。在发送FIFO中没有空级的状态下写入发送缓冲区（SPTXn，n=0到3）不会更新缓冲区值。

2. Read
   通过读取
   SPDR寄存器。可以通过RSPI数据控制寄存器中的RSPI接收数据或发送数据选择位(SPDCR.SPRDTD)来选择读取接收缓冲区或读取发送缓冲区。根据独立的接收缓冲区读指针和发送缓冲区读指针读取SPDR寄存器。

The following illustrates the structure of the receive buffer and transmit buffer bus interface (read).

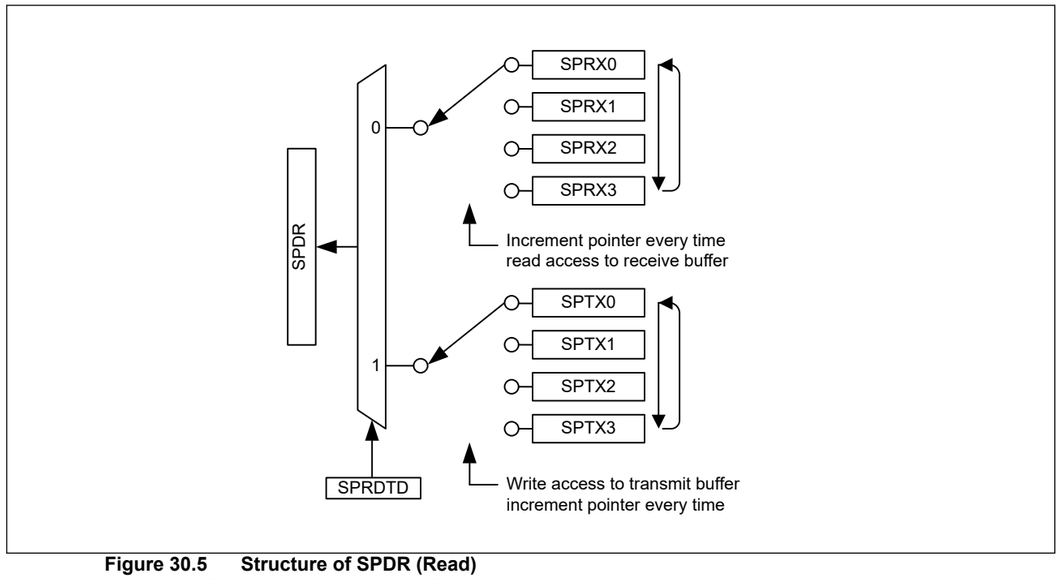


Figure 30.5 Structure of SPDR (Read)

When a receive buffer is read, the receive buffer read pointer automatically switches to the next buffer. The receive buffer read pointer switches in the same order as the transmit buffer write pointer.

The transmit buffer read pointer is updated during the SPDR write access, but it is not updated during the transmit buffer read access. When a transmit buffer is read, the value written to SPDR last can be read.

30.2.2 SPDECR : RSPI Delay Control Register

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SPNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SLNDL[2:0]			—	—	—	—	—	SCKDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SCKDL[2:0]	RSPCK Delay 0 0 0: 1RSPCK 0 0 1: 2RSPCK 0 1 0: 3RSPCK 0 1 1: 4RSPCK 1 0 0: 5RSPCK 1 0 1: 6RSPCK 1 1 0: 7RSPCK 1 1 1: 8RSPCK	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

下面说明接收缓冲区和发送缓冲区总线接口（读取）的结构。

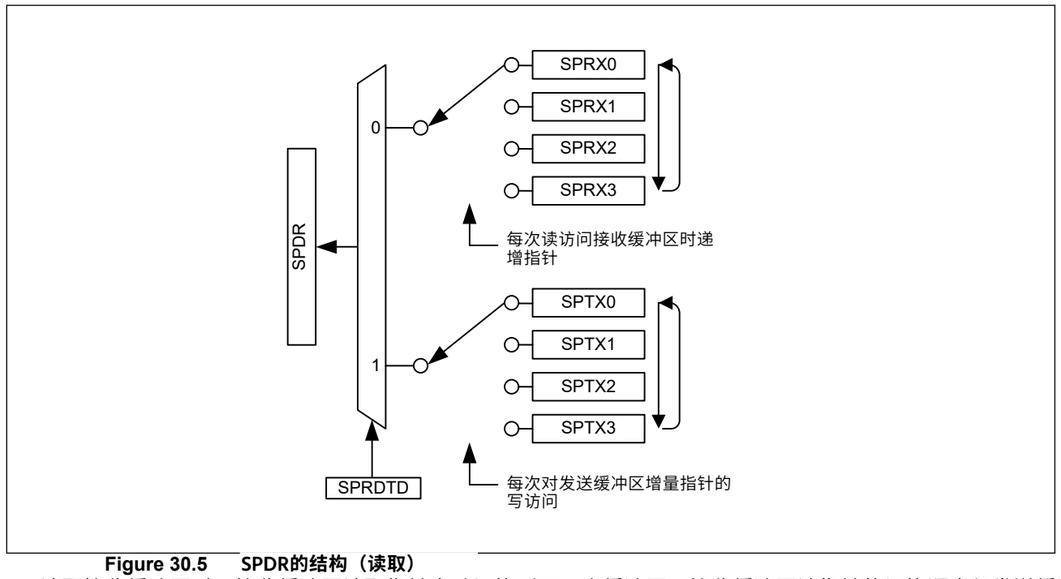


Figure 30.5 SPDR的结构（读取）

读取接收缓冲区时，接收缓冲区读取指针自动切换到下一个缓冲区。接收缓冲区读指针的切换顺序与发送缓冲区写指针的顺序相同。发送缓冲区读指针在SPDR写访问期间更新，但在发送缓冲区读访问期间不更新。读取发送缓冲区时，可以读取最后写入SPDR的值。

30.2.2 SPDECR:RSPI延迟控制寄存器

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SPNDL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SLNDL[2:0]			—	—	—	—	—	SCKDL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SCKDL[2:0]	RSPCK Delay 0 0 0: 1RSPCK 0 0 1: 2RSPCK 0 1 0: 3RSPCK 0 1 1: 4RSPCK 1 0 0: 5RSPCK 1 0 1: 6RSPCK 1 1 0: 7RSPCK 1 1 1: 8RSPCK	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
10:8	SLNDL[2:0]	SSL Negation Delay [Master Mode] 0 0 0: 1RSPCK 0 0 1: 2RSPCK 0 1 0: 3RSPCK 0 1 1: 4RSPCK 1 0 0: 5RSPCK 1 0 1: 6RSPCK 1 1 0: 7RSPCK 1 1 1: 8RSPCK [TI-SSP case in Slave Mode] 0 0 0: 1 TCLK 0 0 1: 2 TCLK 0 1 0: 3 TCLK 0 1 1: 4 TCLK 1 0 0: 5 TCLK 1 0 1: 6 TCLK 1 1 0: 7 TCLK 1 1 1: 8 TCLK	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W
18:16	SPNDL[2:0]	RSPI Next-Access Delay 0 0 0: 1RSPCK + 5TCLK 0 0 1: 2RSPCK + 5TCLK 0 1 0: 3RSPCK + 5TCLK 0 1 1: 4RSPCK + 5TCLK 1 0 0: 5RSPCK + 5TCLK 1 0 1: 6RSPCK + 5TCLK 1 1 0: 7RSPCK + 5TCLK 1 1 1: 8RSPCK + 5TCLK	R/W
31:19	—	These bits are read as 0. The write value should be 0.	R/W

SCKDL[2:0] bit (RSPCK Delay)

[In the Motorola-SPI case]

The RSPCK delay bits (SCKDL) are used to set the period (RSPCK delay) from SSL signal assertion start until RSPCK oscillates while the SCKDEN bit in the RSPI command register (SPCMD) is 1. If SCKDL is modified while the MSTR bit and the SPE bit in the RSPI control register (SPCR) are 1, subsequent operation is not guaranteed.

To use the RSPI in slave mode, set SCKDL[2:0] bits to 000.

[In the TI-SSP case]

The RSPCK delay bits (SCKDL) are used to set the period (RSPCK delay) from SSL signal assertion start until RSPCK oscillates while the SCKDEN bit in the RSPI command register (SPCMD) is 1. Also that is used to set the period until the SSL signal is negated. If SCKDL is modified while the MSTR bit and the SPE bit in the RSPI control register (SPCR) are 1, subsequent operation is not guaranteed.

To use the RSPI in slave mode, set SCKDL[2:0] bits to 000.

SLNDL[2:0] bit (SSL Negation Delay)

[In the Motorola-SPI case]

The SSL negation delay bits (SLNDL) are used to set the period (SSL negation delay) after the RSPI in master mode sends the final RSPCK edge during serial transfer until it negates the SSL signal while the SLNDEN bit in the RSPI command register (SPCMD) is 1. If SLNDL is modified while the MSTR bit and the SPE bit in the RSPI control register (SPCR) are 1, subsequent operation is not guaranteed.

To use the RSPI in slave mode except TI-SSP, set SLNDL[2:0] bits to 000.

[In the TI-SSP case]

The SSL negation delay bits (SLNDL) are used to set the period (OE negation delay) after the RSPI in master mode sends the final RSPCK edge during serial transfer until it negates the OE signal while the SLNDEN bit in the RSPI command register (SPCMD) is 1. Also, that is used to set the period from when the RSPI in slave mode detects the last RSPCK edge

Bit	Symbol	Function	R/W
10:8	SLNDL[2:0]	SSL否定延迟[主模式] 0 0 0: 1RSPCK 0 0 1: 2RSPCK 0 1 0: 3RSPCK 0 1 1: 4RSPCK 1 0 0: 5RSPCK 1 0 1: 6RSPCK 1 1 0: 7RSPCK 1 1 1: 8RSPCK [从模式下的TI-SSP案例] 0 0 0: 1 TCLK 0 0 1: 2 TCLK 0 1 0: 3 TCLK 0 1 1: 4 TCLK 1 0 0: 5 TCLK 1 0 1: 6 TCLK 1 1 0: 7 TCLK 1 1 1: 8 TCLK	R/W
15:11	—	这些位被读取为0。写入值应为0。	R/W
18:16	SPNDL[2:0]	RSPI Next-Access Delay 0 0 0: 1RSPCK + 5TCLK 0 0 1: 2RSPCK + 5TCLK 0 1 0: 3RSPCK + 5TCLK 0 1 1: 4RSPCK + 5TCLK 1 0 0: 5RSPCK + 5TCLK 1 0 1: 6RSPCK + 5TCLK 1 1 0: 7RSPCK + 5TCLK 1 1 1: 8RSPCK + 5TCLK	R/W
31:19	—	这些位被读取为0。写入值应为0。	R/W

SCKDL[2:0] bit (RSPCK Delay)

[In the Motorola-SPI case]

RSPCK延迟位(SCKDL)用于设置从SSL信号断言开始到RSPCK振荡的周期（RSPCK延迟），同时RSPI命令寄存器(SPCMD)中的SCKDEN位为1。如果在MSTR位和RSPI控制寄存器（SPCR）中的SPE位为1，不保证后续操作。

要在从机模式下使用RSPI，请将SCKDL[2:0]位设置为000。

[In the TI-SSP case]

RSPCK延迟位(SCKDL)用于设置从SSL信号断言开始到RSPCK振荡的周期（RSPCK延迟），而RSPI命令寄存器(SPCMD)中的SCKDEN位为1。也用于设置周期，直到SSL信号被否定。如果在RSPI控制寄存器(SPCR)中的MSTR位和SPE位为1时修改SCKDL，则无法保证后续操作。

要在从机模式下使用RSPI，请将SCKDL[2:0]位设置为000。

SLNDL[2:0]位（SSL否定延迟）

[In the Motorola-SPI case]

SSL否定延迟位(SLNDL)用于设置在主模式下的RSPI在串行传输期间发送最后一个RSPCK边沿之后的周期（SSL否定延迟），直到它否定SSL信号，而RSPI命令寄存器(SPCMD)中的SLNDEN位)为1。如果在RSPI控制寄存器(SPCR)中的MSTR位和SPE位为1时修改SLNDL，则无法保证后续操作。

要在除TI-SSP之外的从模式下使用RSPI，请将SLNDL[2:0]位设置为000。

[In the TI-SSP case]

SSL否定延迟位(SLNDL)用于设置在主模式下的RSPI在串行传输期间发送最后一个RSPCK边沿之后的周期（OE否定延迟），直到它否定OE信号，而RSPI命令寄存器(SPCMD)中的SLNDEN位)为1。此外，它用于设置从机模式下的RSPI检测到最后一个RSPCK边沿的时间段

of serial transfer to when the OE signal is negated. If SLNDL is modified while the SPE bit in the RSPI control register (SPCR) are 1, subsequent operation is not guaranteed.

SPNDL[2:0] bit (RSPI Next-Access Delay)

The RSPI next-access delay register (SPDECR.SPNDL) is used to set the SSL signal inactive period (next-access delay) after completion of serial transfer while the SPNDEN bit in the RSPI command register (SPCMD) is 1. If SPNDL is modified while the MSTR bit and the SPE bit in the RSPI control register (SPCR) are 1, subsequent operation is not guaranteed.

These bits are used to set the next-access delay value when the SPNDEN bit in SPCMD is 1. To use the RSPI in slave mode, set SPNDL[2:0] bits to 000.

30.2.3 SPCR : RSPI Control Register

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BPEN	MSTR	TXMD[1:0]		—	—	SPFRF	SPMS	—	—	CENDIE	SPTIE	SPDRES	SPIIE	SPRIE	SPEIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MODFEN	BFDS	SCKASE	PTE	—	SPOE	SPPE	—	—	—	—	—	—	—	SPE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPE	RSPI Function Enable 0: RSPI function is disabled. 1: RSPI function is enabled.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R
8	SPPE	Parity Enable 0: A parity bit is not added to transmit data. Received-data parity check is not performed. 1: A parity bit is added to transmit data. Received-data parity check is performed.	R/W
9	SPOE	Parity Mode 0: Even parity is used for transmission and reception. 1: Odd parity is used for transmission and reception.	R/W
10	—	This bit is read as 0. The write value should be 0.	R
11	PTE	Parity Self-Diagnosis Enable 0: Parity circuit self-diagnosis function is disabled. 1: Parity circuit self-diagnosis function is enabled.	R/W
12	SCKASE	RSPCK Auto-Stop Function Enable 0: RSPCK auto-stop function is disabled. 1: RSPCK auto-stop function is enabled.	R/W
13	BFDS	Between Burst Transfer Frames Delay Select 0: Delay (RSPCK delay, SSL negation delay and next-access delay) between frames is inserted in burst transfer 1: Delay between frames is not inserted in burst transfer.	R/W
14	MODFEN	Mode Fault Error Detection Enable 0: Mode fault error detection is disabled. 1: Mode fault error detection is enabled.	R/W
15	—	This bit is read as 0. The write value should be 0.	R

串行传输到当OE信号被否定时。如果在RSPI控制寄存器(SPCR)中的SPE位为1时修改SLNDL，则无法保证后续操作。

SPNDL[2:0] bit (RSPI Next-Access Delay)

RSPI下一次访问延迟寄存器(SPDECR.SPNDL)用于在RSPI命令寄存器(SPCMD)中的SPNDEN位为1时设置串行传输完成后SSL信号无效周期（下一次访问延迟）。如果SPNDL为当RSPI控制寄存器(SPCR)中的MSTR位和SPE位为1时修改，不保证后续操作。

当SPCMD中的SPNDEN位为1时，这些位用于设置下一次访问延迟值。要在从机模式下使用RSPI，请将SPNDL[2:0]位设置为000。

30.2.3 SPCR:RSPI控制寄存器

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BPEN	MSTR	TXMD[1:0]		—	—	SPFRF	SPMS	—	—	CENDIE	SPTIE	SPDRES	SPIIE	SPRIE	SPEIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MODFEN	BFDS	SCKASE	PTE	—	SPOE	SPPE	—	—	—	—	—	—	—	SPE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPE	RSPI功能使能 0：禁用RSPI功能。1：RSPI功能使能。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R
8	SPPE	奇偶校验使能 0：发送数据时不添加奇偶校验位。不执行接收数据奇偶校验。 1：添加奇偶校验位来发送数据。执行接收数据奇偶校验。	R/W
9	SPOE	奇偶校验模式 0：发送和接收使用偶校验。1：奇校验用于发送和接收。	R/W
10	—	该位读取为0。写入值应为0。	R
11	PTE	奇偶校验自诊断启用 0：奇偶电路自诊断功能无效。1：奇偶电路自诊断功能使能。	R/W
12	SCKASE	RSPCK自动停止功能启用 0：RSPCK自动停止功能禁用。1：RSPCK自动停止功能使能。	R/W
13	BFDS	突发传输帧之间延迟选择 0：在突发传输中插入帧之间的延迟（RSPCK延迟、SSL否定延迟和下一次访问延迟） 1：突发传输中不插入帧间延迟。	R/W
14	MODFEN	模式故障错误检测启用 0：禁用模式故障错误检测。1：启用模式故障错误检测。	R/W
15	—	该位读取为0。写入值应为0。	R

Bit	Symbol	Function	R/W
16	SPEIE	RSPI Error Interrupt Enable 0: RSPI error interrupt request is disabled. 1: RSPI error interrupt request is enabled.	R/W
17	SPRIE	RSPI Receive Buffer Full Interrupt Enable 0: RSPI receive buffer full interrupt request is disabled. 1: RSPI receive buffer full interrupt request is enabled.	R/W
18	SPIIE	RSPI Idle Interrupt Enable 0: Idle interrupt request is disabled. 1: Idle interrupt request is enabled.	R/W
19	SPDRES	RSPI receive data ready error select Select the interrupt request to be generated when the reception data ready is detected 0: Receive data full interrupt 1: Error interrupt	R/W
20	SPTIE	RSPI Transmit Buffer Empty Interrupt Enable 0: RSPI transmit buffer empty interrupt request is disabled. 1: RSPI transmit buffer empty interrupt request is enabled.	R/W
21	CENDIE	RSPI Communication End Interrupt Enable 0: Communication end interrupt request is disabled. 1: Communication end interrupt request is enabled.	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R
24	SPMS	RSPI Mode Select 0: SPI operation (4-wire) 1: Clock synchronous operation (3-wire)	R/W
25	SPFRF	RSPI Frame Format Select 0: Motorola-SPI 1: TI-SSP Note: When SPMS = 1 (clock synchronous operation (3-wire)), this bit setting is invalid.	R/W
27:26	—	These bits are read as 0. The write value should be 0.	R
29:28	TXMD[1:0]	Communication Mode Select 0 0: Transmit-Receive 0 1: Transmit only Others: Receive only	R/W
30	MSTR	RSPI Master/Slave Mode Select 0: Slave mode 1: Master mode	R/W
31	BPEN	Synchronization Circuit Bypass Enable 0: Non-Bypass 1: Bypass	R/W

The RSPI control register (SPCR) is used to set operating mode of the RSPI. If the set BPEN, MSTR, TXMD[1:0], SPFRF, SPMS, MODFEN, BFDS, SCKASE, PTE, SPOE, SPPE bit value is modified while the SPE bit = 1, subsequent operation is not guaranteed.

SPE bit (RSPI Function Enable)

This bit is used to enable or disable RSPI functions. Setting this bit to 1 enables RSPI functions. When the MODF flag in the RSPI status register (SPSR) is 1, the SPE bit is cleared to 0 and the SPE bit cannot be set to 1 until the MODF flag is cleared to 0. (See section 30.3.10. Error Detection) Setting the SPE bit to 0 disables RSPI functions and initializes a part of module functions. (See section 30.3.11. Initializing the SPI)

SPPE bit (Parity Enable)

This bit is used to enable or disable the parity function.

SPOE bit (Parity Mode)

This bit is used to specify even parity or odd parity.

Bit	Symbol	Function	R/W
16	SPEIE	RSPI错误中断使能 0：禁止RSPI错误中断请求。1：RSPI错误中断请求使能。	R/W
17	SPRIE	RSPI接收缓冲器满中断使能 0：禁止RSPI接收缓冲区满中断请求。1：RSPI接收缓冲器满中断请求使能。	R/W
18	SPIIE	RSPI空闲中断使能 0：禁止空闲中断请求。1：允许空闲中断请求。	R/W
19	SPDRES	RSPI接收数据就绪错误选择 选择检测到接收数据就绪时产生的中断请求 0：接收数据满中断1：错误中断	R/W
20	SPTIE	RSPI发送缓冲区空中断使能 0：禁止RSPI发送缓冲区空中断请求。1：RSPI发送缓冲区空中断请求使能。	R/W
21	CENDIE	RSPI通信结束中断使能 0：禁止通讯结束中断请求。1：使能通信结束中断请求。	R/W
23:22	—	这些位被读取为0。写入值应为0。	R
24	SPMS	RSPI模式选择 0：SPI操作（4线）1：时钟同步操作（3线）	R/W
25	SPFRF	RSPI帧格式选择 0: Motorola-SPI 1: TI-SSP Note: 当SPMS=1（时钟同步操作（3线））时，该位设置无效。	R/W
27:26	—	这些位被读取为0。写入值应为0。	R
29:28	TXMD[1:0]	通讯模式选择 00：发送-接收01：仅发送 其他：只收	R/W
30	MSTR	RSPI主从模式选择 0：从模式1：主模式	R/W
31	BPEN	同步电路旁路使能 0: Non-Bypass 1: Bypass	R/W

RSPI控制寄存器(SPCR)用于设置RSPI的工作模式。如果设置的BPEN、MSTR、TXMD[1:0]、SPFRF、SPMS、MODFEN、BFDS、SCKASE、PTE、SPOE、SPPE位值在SPE位=1时被修改，则无法保证后续操作。

SPE位（RSPI功能使能）

该位用于启用或禁用RSPI功能。将该位设置为1启用RSPI功能。当RSPI状态寄存器(SPSR)中的MODF标志为1时，SPE位被清除为0，并且在MODF标志被清除为0之前，SPE位不能被设置为1。（参见第30.3.10节错误检测）将SPE位设置为0将禁用RSPI功能并初始化部分模块功能。（参见第30.3.11节。初始化SPI）

SPPE bit (Parity Enable)

该位用于启用或禁用奇偶校验功能。

SPOE bit (Parity Mode)

该位用于指定偶校验或奇校验。

In even parity mode, the parity bit is determined so that the sum of 1 (parity bit + transmit characters or receive characters) becomes an even number. In the same way, in odd parity mode, a parity bit is determined so that the sum of 1 (parity bit + transmit characters or receive characters) becomes an odd number. The SPOE bit is valid only when the SPPE bit in SPCR is set to 1.

PTE bit (Parity Self-Diagnosis Enable)

This bit is used to enable or disable self-diagnosis of the parity circuit to confirm that the parity function is normal.

SCKASE bit (RSPCK Auto-Stop Function Enable)

This bit is used to enable or disable the RSPCK auto-stop function. When this function is enabled, the RSPCK clock stops immediately before an overrun error occurs during data reception in master mode. For details, see section 30.3.10.1. Overrun errors.

BFDS bit (Between Burst Transfer Frames Delay Select)

This bit controls whether insert the delay time between the burst transfer frames.

Valid in the master mode (SPCR.MSTR = 1) for frames with the SPCMDn.SSLKP bit set to 1.

This bit should be set to 0 in slave mode. The usage of SSL delay control between transfer frames is shown as below. Refer to section 30.3.12.1. Master mode operation in detail.

1. Non-burst transmits
2. Burst transmit with delay between frames
   2-1. From the 1st frame to the last previous frame
   2-2. The last frame
3. Burst transmit with no delay between frames
   3-1. From the 1st frame to the last previous frame
   3-2. The last frame

Table 30.3 Usage of SSL delay control between transfer frames (Master mode)

	SPCMDn. SSLKP bit	SPCR.BF DS bit	SSL delay control register*1 (RSPCK clock delay, SSL negation delay, next access delay)
1	0	0	Any given value. You can control each delay value according to setting for RSPCK clock delay, SSL negation delay and next access delay
2-1	1	0	
2-1	0	0	
3-1	1	1	Any given value. But delay is inserted only below. ● RSPCK clock delay of the 1st frame ● SSL negation delay and next access delay of the last frame
3-2	0	1	

Note 1. Whether the setting value of following bits are valid or not depends on the setting value of the SPCMD.SPNDEN bit. (Refer to section 30.2.6. SPCMDm : RSPI Command Register (m = 0 to 7).)
The SPDECR.SCKDL[2:0] bits: RSPCK delay
The SPDECR.SLNDL[2:0] bits: SSL negate delay
The SPDECR.SPNDL[2:0] bits: Next access delay

< Setting / operation example > (Motorola SPI, BFDS = 1 Case)

SPCMD0.SSLKP = 1 → Burst transfer / no interframe delay between 0 and 1 (SSL keep active)

SPCMD1.SSLKP = 1 → Burst transfer / no interframe delay between 1 and 2 (SSL keep active)

SPCMD2.SSLKP = 1 → Burst transfer / no interframe delay between 2 and 3 (SSL keep active))

SPCMD3.SSLKP = 1 → Burst transfer / no interframe delay between 3 and 4 (SSL keep active)

SPCMD4.SSLKP = 0 → do not Burst Transfer, and inactive SSL. (BFDS setting is invalid because it does not Burst Transfer.)

SPCMD5.SSLKP = 1 → Burst transfer / no interframe delay between 5 and 6 (SSL keep active)

SPCMD6.SSLKP = 1 → Burst transfer / no interframe delay between 6 and 7 (SSL keep active)

在偶校验模式下，奇偶校验位被确定为1（奇偶校验位+发送字符或接收字符）之和为偶数。同样，在奇校验模式下，奇偶校验位被确定为使得1（奇偶校验位+发送字符或接收字符）之和变为奇数。SPOE位只有在SPCR中的SPPE位设置为1时才有效。

PTE bit (Parity Self-Diagnosis Enable)

该位用于启用或禁用奇偶校验电路的自诊断，以确认奇偶校验功能是否正常。

SCKASE位（RSPCK自动停止功能使能）

该位用于启用或禁用RSPCK自动停止功能。当此功能使能时，RSPCK时钟在主机模式下数据接收期间发生溢出错误之前立即停止。有关详细信息，请参阅第30.3.10.1节。溢出错误。

BFDS位（突发传输帧之间延迟选择）

该位控制是否在突发传输帧之间插入延迟时间。

对于SPCMDn.SSLKP位设置为1的帧，在主模式(SPCR.MSTR=1)下有效。

在从机模式下，该位应设置为0。传输帧之间的SSL延迟控制的使用如下所示。请参阅第30.3.12.1节。详细的主模式操作。

1. Non-burst transmits
2.帧间延迟突发传输
   2-1。从第一帧到最后一帧
   2-2。最后一帧
3.帧间无延迟的突发传输
   3-1。从第一帧到最后一帧
   3-2。最后一帧

Table 30.3 传输帧之间使用SSL延迟控制（主模式）

	SPCMDn. SSLKP bit	SPCR.BF DS bit	SSL延迟控制寄存器*1 （RSPCK时钟延迟、SSL否定延迟、下一次访问延迟）
1	0	0	任何给定的值。您可以根据对RSPCK时钟延迟、SSL否定延迟和下一次访问延迟的设置来控制每个延迟值
2-1	1	0	
2-1	0	0	
3-1	1	1	任何给定的值。但是延迟只在下面插入。● 第一帧的RSPCK时钟延迟 ● 最后一帧的SSL否定延迟和下一次访问延迟
3-2	0	1	

注1.以下位的设置值是否有效取决于SPCMD.SPNDEN位的设置值。（请参阅第30.2.6节。SPCMDm：RSPI命令寄存器（m=0到7）。）SPDECR.SCKDL[2:0]位：RSPCK延迟
SPDECR.SLNDL[2:0]位：SSL否定延迟SPDECR.SPNDL[2:0]位：下一次访问延迟

<设置操作示例>(MotorolaSPI BFDS=1Case)

SPCMD0.SSLKP=1→Bursttransfernointerframedelaybetween0and1(SSLkeepactive)

SPCMD1.SSLKP=1→Bursttransfernointerframedelaybetween1and2(SSLkeepactive)

SPCMD2.SSLKP=1→Bursttransfernointerframedelaybetween2and3(SSLkeepactive))

SPCMD3.SSLKP=1→Bursttransfernointerframedelaybetween3and4(SSLkeepactive)

SPCMD4.SSLKP=0→不BurstTransfer和非活动SSL。（BFDS设置无效，因为它不Burst Transfer.)

SPCMD5.SSLKP=1→Bursttransfernointerframedelaybetween5and6(SSLkeepactive)

SPCMD6.SSLKP=1→Bursttransfernointerframedelaybetween6and7(SSLkeepactive)

SPCMD7.SSLKP = 0 → do not Burst Transfer, and inactive SSL. (BFDS setting is invalid because it does not Burst Transfer.)

MODFEN bit (Mode Fault Error Detection Enable)

This bit is used to enable or disable detection of a mode fault error. (See section 30.3.10. Error Detection.) The RSPI determines SSL0 pin input or output direction according to the combination of the MODFEN and MSTR bits. (See section 30.3.2. Controlling the SPI Pins.)

SPEIE bit (RSPI Error Interrupt Enable)

This bit is used to enable or disable an RSPI error interrupt request when the RSPI detects a mode fault error or an underrun error and sets the MODF flag in the RSPI status register (SPSR) to 1, when the RSPI detects an overrun error and sets the OVRF flag in SPSR to 1, or when the RSPI detects a parity error and sets the PERF flag in SPSR to 1. (See section 30.3.10. Error Detection)

SPRIE bit (RSPI Receive Buffer Full Interrupt Enable)

This bit is used to enable or disable a receive buffer full interrupt request of the RSPI.

SPIIE bit (RSPI Idle Interrupt Enable)

This bit is used to enable or disable an idle interrupt request of the RSPI after the RSPI detects the idle state and sets the IDLNF flag in the RSPI status register (SPSR) to 0.

SPDRES bit (RSPI receive data ready error select)

When a receive data ready is detected (SPSR.SPDRF = 1), select whether to use SPRI interrupt request or SPEI interrupt request.

SPTIE bit (RSPI Transmit Buffer Empty Interrupt Enable)

This bit is used to enable or disable a transmit buffer empty interrupt request of the RSPI.

A transmit buffer empty interrupt request at the beginning of transmission is generated by setting the SPE bit to 1 simultaneously when or after the SPTIE bit is set to 1. Note that a transmit buffer empty interrupt is generated while the SPTIE bit is 1 even though RSPI functions are disabled (SPE bit = 0).

CENDIE bit (RSPI Communication End Interrupt Enable)

This bit controls generation of a communication end interrupt request.

SPMS bit (RSPI Mode Select)

This bit is used to select SPI operation (4-wire) or clock synchronous operation (3-wire).

For clock synchronous operation, the SSL pin is not used but three pins RSPCK, MOSI, and MISO are used for communication. When SPMS = 1 (clock synchronous operation (3-wire)), the setting of the SPFRF bit is invalid.

To perform clock synchronous operation in master mode (SPCR.MSTR = 1), the CPHA bit in the RSPI command register (SPCMD) can be set to 0 or 1. To perform clock synchronous operation in slave mode (SPCR.MSTR = 0), set the CPHA bit to 1. If this bit is set to 0 for clock synchronous operation in slave mode (SPCR.MSTR = 0), subsequent operation is not guaranteed.

The communication status according to the settings of the MSTR bit, TXMD [1:0] bits, SPFRF bit, and SPMS bit of the RSPI control register (SPCR) as follows.

Table 30.4 RSPI Communication Status (1 of 2)

SPCR.MSTR	SPCR.TXMD[1]	SPCR.TXMD[0]	SPCR.SPFRF	SPCR.SPMS	Communication Status	Communication Status No
1	0	0	0	0	Transmit-Receive Master / Motorola SPI / SPI operation (4-wire)	1-(1)
1	0	0	1	0	Transmit-Receive Master / TI-SSP / SPI operation (4-wire)	1-(2)
1	0	0	—	1	Transmit-Receive Master /Clock synchronous operation (3-wire)	1-(3)
1	0	1	0	0	Transmit only Master / Motorola SPI / SPI operation (4-wire)	1-(4)
1	0	1	1	0	Transmit only Master / TI-SSP / SPI operation (4-wire)	1-(5)

SPCMD7.SSLKP=0→不BurstTransfer，且SSL处于非活动状态。（BFDS设置无效，因为它不Burst Transfer.)

MODFEN位（模式故障错误检测使能）

该位用于启用或禁用模式故障错误检测。（请参阅第30.3.10节。错误检测。）RSPI根据MODFEN和MSTR位的组合确定SSL0引脚的输入或输出方向。（请参阅第30.3.2节。控制SPI引脚。）

SPEIE位（RSPI错误中断使能）

该位用于在RSPI检测到模式故障错误或欠载错误并将RSPI状态寄存器(SPSR)中的MODF标志设置为1时启用或禁用RSPI错误中断请求，当RSPI检测到溢出错误并设置SPSR中的OVRF标志为1，或者当RSPI检测到奇偶校验错误并将SPSR中的PERF标志设置为1时。（参见第30.3.10节。

错误检测）

SPRIE位（RSPI接收缓冲器满中断使能）

该位用于启用或禁用RSPI的接收缓冲区满中断请求。

SPIIE位（RSPI空闲中断允许）

该位用于在RSPI检测到空闲状态并设置RSPI后启用或禁用RSPI的空闲中断请求
RSPI状态寄存器(SPSR)中的IDLNF标志为0。

SPDRES位（RSPI接收数据就绪错误选择）

当检测到接收数据就绪时（SPSR.SPDRF=1），选择是使用SPRI中断请求还是SPEI中断请求。

SPTIE位（RSPI发送缓冲区空中断使能）

该位用于启用或禁用RSPI的发送缓冲区空中断请求。

当SPTIE位设置为1时或之后，同时将SPE位设置为1，可在发送开始时产生发送缓冲区空中断请求。请注意，即使RSPI为1，也会在SPTIE位为1时产生发送缓冲区空中断功能被禁用（SPE位=0）。

CENDIE位（RSPI通信结束中断使能）

该位控制通信结束中断请求的产生。

SPMS位（RSPI模式选择）

该位用于选择SPI操作（4线）或时钟同步操作（3线）。

对于时钟同步操作，不使用SSL引脚，而是使用三个引脚RSPCK、MOSI和MISO进行通信。当SPMS=1（时钟同步操作（3线））时，SPFRF位的设置无效。

要在主机模式下执行时钟同步操作(SPCR.MSTR=1)，可以将RSPI命令寄存器(SPCMD)中的CPHA位设置为0或1。要在从机模式下执行时钟同步操作(SPCR.MSTR=0)，将CPHA位设置为1。如果该位设置为0以在从机模式下进行时钟同步操作（SPCR.MSTR=0），则无法保证后续操作。

根据MSTR位、TXMD[1:0]位、SPFRF位和SPMS位设置的通信状态
RSPI控制寄存器（SPCR）如下。

Table 30.4 RSPI通信状态(1of2)

SPCR.MSTR	SPCR.TXMD[1]	SPCR.TXMD[0]	SPCR.SPFRF	SPCR.SPMS	通讯状态	Communication状态否
1	0	0	0	0	发送接收主MotorolaSPISPI操作（4线）	1-(1)
1	0	0	1	0	发送-接收主控TI-SSPSPI操作（4线）	1-(2)
1	0	0	—	1	发送接收主时钟同步操作（3线）	1-(3)
1	0	1	0	0	仅发送MasterMotorolaSPISPI操作（4线）	1-(4)
1	0	1	1	0	仅发送主TI-SSPSPI操作（4线）	1-(5)

Table 30.4 RSPI Communication Status (2 of 2)

SPCR. MSTR	SPCR.TXMD[1]	SPCR.TXMD[0]	SPCR. SPFRF	SPCR. SPMS	Communication Status	Communication Status No
1	0	1	—	1	Transmit only Master /Clock synchronous operation (3-wire)	1-(6)
1	1	—	0	0	Receive only Master / Motorola SPI / SPI operation (4-wire)	1-(7)
1	1	—	1	0	Receive only Master / TI-SSP / SPI operation (4-wire)	1-(8)
1	1	—	—	1	Receive only Master /Clock synchronous operation (3-wire)	1-(9)
0	0	0	0	0	Transmit-Receive Slave / Motorola SPI / SPI operation (4-wire) (default)	0-(1)
0	0	0	1	0	Transmit-Receive Slave / TI-SSP / SPI operation (4-wire)	0-(2)
0	0	0	—	1	Transmit-Receive Slave /Clock synchronous operation (3-wire)	0-(3)
0	0	1	0	0	Transmit only Slave / Motorola SPI / SPI operation (4-wire)	0-(4)
0	0	1	1	0	Transmit only Slave / TI-SSP / SPI operation (4-wire)	0-(5)
0	0	1	—	1	Transmit only Slave /Clock synchronous operation (3-wire)	0-(6)
0	1	—	0	0	Receive only Slave / Motorola SPI / SPI operation (4-wire)	0-(7)
0	1	—	1	0	Receive only Slave / TI-SSP / SPI operation (4-wire)	0-(8)
0	1	—	—	1	Receive only Slave /Clock synchronous operation (3-wire)	0-(9)

SPFRF bit (RSPI Frame Format Select)

This bit selects the communication protocol.

The format of the RSPI terminal (RSPCK, SSL0 to 7) can be set according to the set communication protocol.

When SPMS = 1 (clock synchronous operation (3-wire)), this bit is invalid because SSL is not used.

TXMD[1:0] bit (Communication Mode Select)

This bit is used to select the transmit-receive, transmit-only, and receive-only serial communication.

When TXMD[1:0] is set to 01 for communication, transmit-only is performed without reception.

When TXMD[1] is set to 1 for communication, receive-only is performed without transmission.

When TXMD[1:0] is set to 01 for communication, a receive buffer full interrupt request cannot be used.

When TXMD[1] is set to 1 for communication, a transmit buffer empty interrupt request cannot be used.

(See section 30.3.6. Communication Operating Mode.)

MSTR bit (RSPI Master/Slave Mode Select)

This bit is used to select master mode or slave mode of the RSPI. The RSPI determines input/output directions of pins RSPCK, MOSI, MISO, and SSL1 to SSL3 according to the MSTR bit setting.

BPEN bit (Synchronization Circuit Bypass Enable)

This bit selects whether to enable or disable the synchronization bypass function. This bit can be used to bypass the synchronization circuit only when the same clock is input to the bus clock (PCLK) and operation clock (TCLK).

Table 30.4 RSPI通信状态（2之2）

SPCR. MSTR	SPCR.TXMD[1]	SPCR.TXMD[0]	SPCR. SPFRF	SPCR. SPMS	通讯状态	Communication 状态否
1	0	1	—	1	仅发送主时钟同步操作（3线）	1-(6)
1	1	—	0	0	仅接收MasterMotorolaSPISPI操作（4线）	1-(7)
1	1	—	1	0	仅接收主TI-SSPSPI操作（4线）	1-(8)
1	1	—	—	1	仅接收主时钟同步操作（3线）	1-(9)
0	0	0	0	0	发送-接收从机MotorolaSPISPI操作（4线）（默认）	0-(1)
0	0	0	1	0	发送-接收从TI-SSPSPI操作（4线）	0-(2)
0	0	0	—	1	发送接收从时钟同步操作（3线）	0-(3)
0	0	1	0	0	仅发送从机MotorolaSPISPI操作（4线）	0-(4)
0	0	1	1	0	仅发送从TI-SSPSPI操作（4线）	0-(5)
0	0	1	—	1	仅发送从时钟同步操作（3线）	0-(6)
0	1	—	0	0	仅接收从机MotorolaSPISPI操作（4线）	0-(7)
0	1	—	1	0	仅接收从TI-SSPSPI操作（4线）	0-(8)
0	1	—	—	1	仅接收从时钟同步操作（3线）	0-(9)

SPFRF位（RSPI帧格式选择）

该位选择通信协议。

RSPI终端的格式（RSPCK，SSL0到7）可以根据设置的通信协议进行设置。

当SPMS=1（时钟同步操作（3线））时，该位无效，因为没有使用SSL。

TXMD[1:0]位（通信模式选择）

该位用于选择发送-接收、仅发送和仅接收串行通信。

当TXMD[1:0]设置为01进行通信时，只执行发送而不接收。

当TXMD[1]设置为1进行通信时，只执行接收而不发送。

当TXMD[1:0]设置为01进行通信时，不能使用接收缓冲区满中断请求。

当TXMD[1]设置为1进行通信时，不能使用发送缓冲区空中断请求。

（参见第30.3.6节。通信操作模式。）

MSTR位（RSPI主从模式选择）

该位用于选择RSPI的主模式或从模式。RSPI确定引脚的输入输出方向
根据MSTR位设置，RSPCK、MOSI、MISO和SSL1到SSL3。

BPEN位（同步电路旁路使能）

该位选择是启用还是禁用同步旁路功能。只有当总线时钟（PCLK）和操作时钟（TCLK）输入相同的时钟时，该位才能用于绕过同步电路。

30.2.4 SPCR2 : RSPI Control Register 2

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SPDRC[7:0]								RMSTTG	RMEDTG	—	RMFM[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	RMFM[4:0]	Frame processing count setting in Master Receive only The number of received frames can be adjusted in master receive only. 0x00: This function is not used*1 0x01: Automatically stop communication after processing 1 received frame ⋮ 0x1F: Automatically stop communication after processing 31 received frames	R/W
5	—	This bit is read as 0. The write value should be 0.	R
6	RMEDTG	End Trigger in Master Receive only 1: Receive End (Writable only when Master Receive only) Reading value is always 0	W
7	RMSTTG	Start Trigger in Master Receive only 1: Receive Start (Writable only when Master Receive only) Reading value is always 0	W
15:8	SPDRC[7:0]	RSPI received data ready detect adjustment 0x0: Disable receive data ready detection function 0x1: Performs reception data ready judgment after 1 TCLK ⋮ 0xFF Performs reception data ready judgment after 255 TCLK	R/W
16	SPLP	RSPI Loopback 0: Normal mode 1: Loopback mode (inverted transmit data = receive data)	R/W
17	SPLP2	RSPI Loopback 2 0: Normal mode 1: Loopback mode (transmit data = receive data)	R/W
19:18	—	These bits are read as 0. The write value should be 0.	R
20	MOIFV	MOSI Idle Fixed Value 0: The fixed value of MOSI idle = 0. 1: The fixed value of MOSI idle = 1.	R/W
21	MOIFE	MOSI Idle Fixed Value Enable 0: The MOSI output value is the last data of previous transfer. 1: The MOSI output value is the set MOIFV bit value.	R/W
31:22	—	These bits are read as 0. The write value should be 0.	R

Note 1. Refer to SW flow in the Figure 30.66.

RMFM[4:0] bit (Frame processing count setting in Master Receive only)

The number of received frames can be adjusted when operating in master receive only. Valid only when the master mode (SPCR.MSTR = 1) and the communication operation mode select bits (SPCR.TXMD [1:0]) are 10b.

30.2.4 SPCR2：RSPI控制寄存器2

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SPDRC[7:0]								RMSTTG	RMEDTG	—	RMFM[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	RMFM[4:0]	仅主接收中的帧处理计数设置 接收帧数只能在主接收中调整。 0x00：未使用此功能*1 0x01：处理1个接收帧后自动停止通信 ⋮ 0x1F：处理31个接收帧后自动停止通信	R/W
5	—	该位读取为0。写入值应为0。	R
6	RMEDTG	仅在主接收中结束触发 1：接收结束 （仅在MasterReceiveonly时可写）读取值 始终为0	W
7	RMSTTG	仅在主接收中启动触发 1：接收开始 （仅在MasterReceiveonly时可写）读取值 始终为0	W
15:8	SPDRC[7:0]	RSPI接收数据就绪检测调整 0x0：禁用接收数据就绪检测功能0x1：在1个TCLK后执行接收数据就绪判断 ⋮ 0xFF255TCLK后进行接收数据就绪判断	R/W
16	SPLP	RSPI Loopback 0：正常模式1：环回模式（反转发送数据=接收数据）	R/W
17	SPLP2	RSPI Loopback 2 0：正常模式1：环回模式（发送数据=接收数据）	R/W
19:18	—	这些位被读取为0。写入值应为0。	R
20	MOIFV	MOSI空闲固定值 0：MOSIidle的固定值=0。1：MOSIidle的固定值=1。	R/W
21	MOIFE	MOSI空闲固定值启用 0：MOSI输出值为上一次传输的最后一个数据。1：MOSI输出值为设置的MOIFV位值。	R/W
31:22	—	这些位被读取为0。写入值应为0。	R

注1.参考图30.66中的SW流程。

RMFM[4:0]位（仅在主接收中设置帧处理计数）

仅在主接收模式下操作时，可以调整接收帧的数量。仅当主机模式(SPCR.MSTR=1)和通信操作模式选择位(SPCR.TXMD[1:0])为10b时有效。

Only the start bit in master mode reception automatically stops communication after starts frame processing according to the value set in this bit after reception starts.

If the RMFM [4:0] bits are rewritten while the SPE bit of the RSPI control register (SPCR) is 1, subsequent operations are not guaranteed.

RMEDTG bit (End Trigger in Master Receive only)

This bit is used to end reception when master receive only. Valid only when the master mode (SPCR.MSTR = 1) and the communication mode select bits (SPCR.TXMD [1:0]) are 10b.

RMSTTG bit (Start Trigger in Master Receive only)

This bit is used to start reception when master receive only. Valid only when the master mode (SPCR.MSTR = 1) and the communication mode select bits (SPCR.TXMD [1:0]) are 10b.

Writing 1 to this bit during reception is not accepted. Write again after reception is completed.

SPDRC[7:0] bit (RSPI received data ready detect adjustment)

The receive data ready detection function can be disabled or, if used, the period until detection can be set from 1 to 255 TCLK.

The value set in the SPDRC [7:0] bits is used to 1 set the SPDRF flag. For details, see the description of SPDRF in section 30.2.9. SPSR : SPI Status Register.

If the set value is changed while the SPE bit is 1, subsequent operations are not guaranteed.

SPLP bit (RSPI Loopback)

When the SPLP bit is set to 1, the RSPI shuts down the route between the MISO pin and the shift register (when the MSTR bit in the RSPI control register is 1) or shuts down the route between the MOSI pin and the shift register, inverts the input route value in the shift register, and then connects the route to the output route (when the MSTR bit in the RSPI control register is 0) (loopback mode).

SPLP2 bit (RSPI Loopback 2)

When the SPLP2 bit is set to 1, the RSPI shuts down the route between the MISO pin and the shift register (when the MSTR bit in the RSPI control register is 1) or shuts down the route between MOSI pin and the shift register and then connects the route to the output route without inverting the input route value in the shift register (when the MSTR bit in the RSPI control register is 0) (loopback mode). If this bit is set to 1 together with the SPLP bit, setting this bit takes precedence.

MOIFV bit (MOSI Idle Fixed Value)

This bit is used to select the MOSI pin output value during the SSL negation period (including SSL retention period in burst transfer) when the MOIFE bit is 1 in master mode.

If this bit is modified with the SPE bit in the RSPI control register (SPCR) set to 1, subsequent operation is not guaranteed.

MOIFE bit (MOSI Idle Fixed Value Enable)

This bit is used for the RSPI in master mode to fix the MOSI output value during the SSL negation period (including SSL retention period in burst transfer). When MOIFE bit = 0, the RSPI outputs the last data of the previous serial transfer to MOSI during the SSL negation period. When MOIFE bit = 1, the RSPI outputs the fixed MOIFV bit value to MOSI.

If this bit is modified with the SPE bit in the RSPI control register (SPCR) set to 1, subsequent operation is not guaranteed.

只有主机模式接收的起始位在接收开始后根据该位中设置的值开始帧处理后自动停止通信。

如果在RSPI控制寄存器(SPCR)的SPE位为1时重写RMFM[4:0]位，则无法保证后续操作。

RMEDTG位（仅限主接收中的结束触发）

当主机只接收时，该位用于结束接收。仅当主机模式(SPCR.MSTR=1)和通信模式选择位(SPCR.TXMD[1:0])为10b时有效。

RMSTTG位（仅在主接收中启动触发）

该位用于仅在主机接收时开始接收。仅当主机模式(SPCR.MSTR=1)和通信模式选择位(SPCR.TXMD[1:0])为10b时有效。

接收期间不接受向该位写入1。接收完成后再次写入。

SPDRC[7:0]位（RSPI接收数据就绪检测调整）

可以禁用接收数据就绪检测功能，或者，如果使用，可以将检测前的周期设置为1到255 TCLK.

SPDRC[7:0]位中设置的值用于将SPDRF标志设置为1。详见30.2.9节对SPDRF的描述。SPSR：SPI状态寄存器。

如果在SPE位为1时更改设置值，则无法保证后续操作。

SPLP bit (RSPI Loopback)

当SPLP位设置为1时，RSPI关闭MISO引脚和移位寄存器之间的路由（当RSPI控制寄存器中的MSTR位为1时）或关闭MOSI引脚和移位寄存器之间的路由，将移位寄存器中的输入路由值取反，然后将路由连接到输出路由（当RSPI控制寄存器中的MSTR位为0时）（环回模式）。

SPLP2 bit (RSPI Loopback 2)

当SPLP2位设置为1时，RSPI关闭MISO引脚和移位寄存器之间的路由（当RSPI控制寄存器中的MSTR位为1时）或关闭MOSI引脚和移位寄存器之间的路由，然后将路由连接到输出路由，而不反转移位寄存器中的输入路由值（当RSPI控制寄存器中的MSTR位为0时）（环回模式）。如果该位与SPLP位一起设置为1，则设置该位优先。

MOIFV位（MOSI空闲固定值）

该位用于在主模式下MOIFE位为1时选择SSL否定期间（包括突发传输中的SSL保持期间）的MOSI引脚输出值。

如果将该位修改为将RSPI控制寄存器(SPCR)中的SPE位设置为1，则无法保证后续操作。

MOIFE位（MOSI空闲固定值启用）

该位用于主模式下的RSPI，用于在SSL否定期间（包括突发传输中的SSL保留期间）固定MOSI输出值。当MOIFE位=0时，RSPI在SSL否定期间将上一次串行传输的最后一个数据输出到MOSI。当MOIFE位=1时，RSPI将固定的MOIFV位值输出到MOSI。

如果将该位修改为将RSPI控制寄存器(SPCR)中的SPE位设置为1，则无法保证后续操作。

30.2.5 SPCR3 : RSPI Control Register 3

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	SPSLN[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SPBR[7:0]								—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
Value after reset:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSL0P	SSL0 Signal Polarity [In the Motorola-SPI case] 0: The SSL0 signal is active low (0). 1: The SSL0 signal is active high (1). [In the TI-SSP case] 0: The SSL0 signal is active high (1). 1: The SSL0 signal is active low (0).	R/W
1	SSL1P	SSL1 Signal Polarity [In the Motorola-SPI case] 0: The SSL1 signal is active low (0). 1: The SSL1 signal is active high (1). [In the TI-SSP case] 0: The SSL1 signal is active high (1). 1: The SSL1 signal is active low (0).	R/W
2	SSL2P	SSL2 Signal Polarity [In the Motorola-SPI case] 0: The SSL2 signal is active low (0). 1: The SSL2 signal is active high (1). [In the TI-SSP case] 0: The SSL2 signal is active high (1). 1: The SSL2 signal is active low (0).	R/W
3	SSL3P	SSL3 Signal Polarity [In the Motorola-SPI case] 0: The SSL3 signal is active low (0). 1: The SSL3 signal is active high (1). [In the TI-SSP case] 0: The SSL3 signal is active high (1). 1: The SSL3 signal is active low (0).	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R
15:8	SPBR[7:0]	SPI Bit Rate	R/W
23:16	—	These bits are read as 0. The write value should be 0.	R

30.2.5 SPCR3：RSPI控制寄存器3

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	SPSLN[2:0]			—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SPBR[7:0]								—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
重置后的值：	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSL0P	SSL0信号极性[在Motorola-SPI案例中] 0：SSL0信号低电平有效(0)。1：SSL0信号为高电平有效(1)。 [In the TI-SSP case] 0：SSL0信号为高电平有效(1)。1：SSL0信号低电平有效(0)。	R/W
1	SSL1P	SSL1信号极性[在Motorola-SPI案例中] 0：SSL1信号低电平有效(0)。1：SSL1信号为高电平有效(1)。 [In the TI-SSP case] 0：SSL1信号为高电平有效(1)。1：SSL1信号低电平有效(0)。	R/W
2	SSL2P	SSL2信号极性[在Motorola-SPI案例中] 0：SSL2信号低电平有效(0)。1：SSL2信号为高电平有效(1)。 [In the TI-SSP case] 0：SSL2信号为高电平有效(1)。1：SSL2信号低电平有效(0)。	R/W
3	SSL3P	SSL3信号极性[在Motorola-SPI案例中] 0：SSL3信号低电平有效(0)。1：SSL3信号为高电平有效(1)。 [In the TI-SSP case] 0：SSL3信号为高电平有效(1)。1：SSL3信号低电平有效(0)。	R/W
7:4	—	这些位被读取为0。写入值应为0。	R
15:8	SPBR[7:0]	SPI比特率	R/W
23:16	—	这些位被读取为0。写入值应为0。	R

Bit	Symbol	Function	R/W
26:24	SPSLN[2:0]	RSPI Sequence Length Registers SPCMD0 to SPCMD7 to be referenced and reference sequence are changed according to the set sequence length. Relationship among this bit value, sequence length, and SPCMD0 to SPCMD7 to be referenced by the RSPI are shown above. The RSPI in slave mode always references SPCMD0. 0 0 0: Sequence Length is 1 (Referenced SPCMDn, n = 0→0→…) 0 0 1: Sequence Length is 2 (Referenced SPCMDn, n = 0→1→0→…) 0 1 0: Sequence Length is 3 (Referenced SPCMDn, n = 0→1→2→0→…) 0 1 1: Sequence Length is 4 (Referenced SPCMDn, n = 0→1→2→3→0→…) 1 0 0: Sequence Length is 5 (Referenced SPCMDn, n = 0→1→2→3→4→0→…) 1 0 1: Sequence Length is 6 (Referenced SPCMDn, n = 0→1→2→3→4→5→0→…) 1 1 0: Sequence Length is 7 (Referenced SPCMDn, n = 0→1→2→3→4→5→6→0→…) 1 1 1: Sequence Length is 8 (Referenced SPCMDn, n = 0→1→2→3→4→5→6→7→0→…)	R/W
31:27	—	These bits are read as 0. The write value should be 0.	R

SSLiP bits (SSL Signal Polarity Bits)

These bits are used to specify the polarity of SSL signals. The set SSLiP bit (i = 3 to 0) values indicate the active polarity of SSLi signals.

If any of these SSLiP bits is modified with the SPE bit in the RSPI control register (SPCR) set to 1, subsequent operation is not guaranteed.

*SSL0 is different from SSL1-SSL3. When slave or multi-master, it functions as an input.

For details, refer to Single Master/Single Slave (This MCU = Slave), and Multi-Master/Multi-Slave (This MCU = Master).

SPBR[7:0] bit (SPI Bit Rate)

The RSPI bit rate bits (SPBR) is used to set the bit rate in master mode. If SPBR is modified while the MSTR bit in the RSPI control register (SPCR) and the MSTR bit are 1, subsequent operation is not guaranteed.

When the RSPI is used in slave mode, the bit rate depends on the input clock bit rate regardless of the SPCMD.BRDV setting. (Specify a bit rate that meets electrical characteristics.).

The bit rate is determined by a combination of the set SPBR value and the set BRDV[1:0] bits value in the RSPI command register (SPCMD0 to SPCMD7).

The bit rate is calculated by the following expression, where n is the set SPBR value (0 to 255) and N is the set BRDV[1:0] bits value (0 to 3).

$$\text{Bit rate} = \frac{f(\text{TCLK})}{2 \times (n+1) \times 2^N}$$

The following table shows an example of correspondence between bit rates and set values of SPBR and BRDV[1:0].

Table 30.5 Corresponding Between Bit Rates and Set Values (Example)

SPBR Value (n)	BRDV Value (N)	Division Ratio	Bit Rate				
			TCLK = 32 MHz	TCLK = 36 MHz	TCLK = 40 MHz	TCLK = 50 MHz	TCLK = 120MHz
0	0	2	16.0 Mbps	18.0 Mbps	20.0 Mbps	25.0 Mbps	60.0Mbps
1	0	4	8.00 Mbps	9.00 Mbps	10.0 Mbps	12.5 Mbps	30.0Mbps
2	0	6	5.33 Mbps	6.00 Mbps	6.67 Mbps	8.33 Mbps	20.0Mbps
3	0	8	4.00 Mbps	4.50 Mbps	5.00 Mbps	6.25 Mbps	15.0Mbps
4	0	10	3.20 Mbps	3.60 Mbps	4.00 Mbps	5.00 Mbps	12.0Mbps
5	0	12	2.67 Mbps	3.00 Mbps	3.33 Mbps	4.16 Mbps	10.0Mbps
5	1	24	1.33 Mbps	1.50 Mbps	1.67 Mbps	2.08 Mbps	5.0Mbps
5	2	48	677 kbps	750 kbps	833 kbps	1.04 Mbps	2.5Mbps
5	3	96	333 kbps	375 kbps	417 kbps	521 kbps	1.25Mbps
255	3	4096	7.81 kbps	8.80 kbps	9.78 kbps	12.2 kbps	29.3kbps

Bit	Symbol	Function	R/W
26:24	SPSLN[2:0]	RSPI序列长度 参考的寄存器SPCMD0到SPCMD7和参考序列根据设置的序列长度改变。该位值、序列长度和RSPI引用的SPCMD0到SPCMD7之间的关系如上所示。从机模式下的RSPI始终参考SPCMD0。 000：序列长度为1（参考SPCMDn，n=0→0→…）001：序列长度为2（参考SPCMDn，n=0→1→0→…）010：序列长度为3（参考SPCMDn，n=0→1→2→0→…）011：序列长度为4（参考SPCMDn，n=0→1→2→3→0→…）100：序列长度为5（参考SPCMDn，n=0→1→2→3→4→0→…）101：序列长度为6（参考SPCMDn，n=0→1→2→3→4→5→0→…）110：序列长度为7（参考SPCMDn，n=0→1→2→3→4→5→6→0→…）111：序列长度为8（参考SPCMDn，n=0→1→2→3→4→5→6→7→0→…）	R/W
31:27	—	这些位被读取为0。写入值应为0。	R

SSLiP位（SSL信号极性位）

这些位用于指定SSL信号的极性。设置SSLiP位（i=3到0）值表示的有效极性
SSLi signals.

如果在将RSPI控制寄存器(SPCR)中的SPE位设置为1的情况下修改了这些SSLiP位中的任何一个，则无法保证后续操作。

*SSL0与SSL1-SSL3不同。当从机或多主机时，它用作输入。

详情请参考单主单从（本MCU=从）和多主多从（本MCU=主）。

SPBR[7:0] bit (SPI Bit Rate)

RSPI比特率位(SPBR)用于设置主机模式下的比特率。如果SPBR被修改，而MSTR位在RSPI控制寄存器（SPCR）和MSTR位为1，不保证后续操作。

当RSPI在从机模式下使用时，比特率取决于输入时钟比特率，与SPCMD.BRDV设置无关。（指定符合电气特性的比特率。）。

比特率由设置的SPBR值和RSPI命令寄存器（SPCMD0到SPCMD7）中设置的BRDV[1:0]位值的组合确定。

比特率通过以下表达式计算，其中n是设置的SPBR值（0到255），N是设置的BRDV[1:0]位值（0到3）。

$$\text{比特率} = \frac{f(\text{TCLK})}{2 \times (n+1) \times 2^N}$$

下表显示了比特率与SPBR和BRDV[1:0]的设置值之间的对应关系示例。

Table 30.5 比特率与设定值的对应（示例）

SPBR Value (n)	BRDV Value (N)	Division Ratio	比特率				
			TCLK = 32 MHz	TCLK = 36 MHz	TCLK = 40 MHz	TCLK = 50 MHz	TCLK = 120MHz
0	0	2	16.0 Mbps	18.0 Mbps	20.0 Mbps	25.0 Mbps	60.0Mbps
1	0	4	8.00 Mbps	9.00 Mbps	10.0 Mbps	12.5 Mbps	30.0Mbps
2	0	6	5.33 Mbps	6.00 Mbps	6.67 Mbps	8.33 Mbps	20.0Mbps
3	0	8	4.00 Mbps	4.50 Mbps	5.00 Mbps	6.25 Mbps	15.0Mbps
4	0	10	3.20 Mbps	3.60 Mbps	4.00 Mbps	5.00 Mbps	12.0Mbps
5	0	12	2.67 Mbps	3.00 Mbps	3.33 Mbps	4.16 Mbps	10.0Mbps
5	1	24	1.33 Mbps	1.50 Mbps	1.67 Mbps	2.08 Mbps	5.0Mbps
5	2	48	677 kbps	750 kbps	833 kbps	1.04 Mbps	2.5Mbps
5	3	96	333 kbps	375 kbps	417 kbps	521 kbps	1.25Mbps
255	3	4096	7.81 kbps	8.80 kbps	9.78 kbps	12.2 kbps	29.3kbps

Note: The product design department is requested to determine bit rates to be disclosed based on AC specifications.

SPSLN[2:0] bit (RSPI Sequence Length)

These bits are used to set the sequence length for the RSPI in master mode to perform sequence operation. According to the sequence length specified by SPSLN[2:0] bits, the RSPI in master mode changes RSPI command registers 0 to 7 (SPCMD0 to SPCMD7) to be referenced and the reference sequence. For details, see section 30.3.13.1. Master mode operation.

The RSPI in slave mode always references SPCMD0

30.2.6 SPCMDm : RSPI Command Register (m = 0 to 7)

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x14 + 0x04 × m

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	SSLA[2:0]			—	—	—	SPB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	—	—	SSLKP	—	—	—	BRDV[1:0]		CPOL	CPHA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CPHA	RSPCK Phase 0: Data is sampled at an odd edge and changes at an even edge. 1: Data changes at an odd edge and is sampled at an even edge.	R/W
1	CPOL	RSPCK Polarity 0: RSPCK in idle state is 0. 1: RSPCK in idle state is 1.	R/W
3:2	BRDV[1:0]	Bit Rate Division 0 0: The base bit rate is selected. 0 1: Two-divided base bit rate is selected. 1 0: Four-divided base bit rate is selected. 1 1: Eight-divided base bit rate is selected.	R/W
6:4	—	These bits are read as 0. The write value should be 0.	R
7	SSLKP	SSL Signal Level Hold 0: All SSL signals are negated at the end of transfer. 1: SSL signal level is held after the transfer ends until the next access starts.	R/W
11:8	—	These bits are read as 0. The write value should be 0.	R
12	LSBF	RSPI LSB First 0: MSB first 1: LSB first	R/W
13	SPNDEN	RSPI Next-Access Delay Enable 0: Next-access delay is 1RSPCK + 5TCLK 1: Next-access delay is the set value of the RSPI next-access delay register (SPDECR.SPNDL).	R/W
14	SLNDEN	SSL Negation Delay Setting Enable 0: [Master] SSL negation delay is 1RSPCK. [Slave in the TI-SSP] SSL negation delay is 1TCLK 1: SSL negation delay is the set value of the slave select negation delay register (SPDECR.SLNDL).	R/W

Note: 请产品设计部门根据AC规范确定要公开的比特率。

SPSLN[2:0]位（RSPI序列长度）

这些位用于设置RSPI在主模式下执行序列操作的序列长度。根据SPSLN[2:0]位指定的序列长度，主模式下的RSPI更改要参考的RSPI命令寄存器0到7（SPCMD0到SPCMD7）和参考序列。有关详细信息，请参阅第30.3.13.1节。主模式操作。

从机模式下的RSPI始终参考SPCMD0

30.2.6 SPCMDm：RSPI命令寄存器（m=0到7）

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x14 + 0x04 × m

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	SSLA[2:0]			—	—	—	SPB[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	—	—	SSLKP	—	—	—	BRDV[1:0]		CPOL	CPHA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CPHA	RSPCK Phase 0：数据在奇数边沿采样，在偶数边沿变化。1：数据在奇边沿变化，在偶边沿采样。	R/W
1	CPOL	RSPCK Polarity 0：空闲状态的RSPCK为0。 1：空闲状态的RSPCK为1。	R/W
3:2	BRDV[1:0]	比特率划分 00：选择基本比特率。01：选择二分基本比特率。10：选择四分基本比特率。11：选择八分基本比特率。	R/W
6:4	—	这些位被读取为0。写入值应为0。	R
7	SSLKP	SSL信号电平保持 0：所有SSL信号在传输结束时被否定。1：传输结束后SSL信号电平保持到下一次访问开始。	R/W
11:8	—	这些位被读取为0。写入值应为0。	R
12	LSBF	RSPI LSB First 0: MSB first 1: LSB first	R/W
13	SPNDEN	RSPI下一次访问延迟启用 0：下一次访问延迟为1RSPCK+5TCLK1：下一次访问延迟为RSPI下一次访问延迟寄存器（SPDECR.SPNDL）的设定值。	R/W
14	SLNDEN	SSL否定延迟设置启用 0：[Master]SSL否定延迟为1RSPCK。 [TI-SSP中的从机]SSL否定延迟为1TCLK 1：SSL否定延迟是从机选择否定延迟寄存器（SPDECR.SLNDL）的设定值。	R/W

Bit	Symbol	Function	R/W
15	SCKDEN	RSPCK Delay Setting Enable [In the Motorola-SPI case] 0: RSPCK delay is 1 RSPCK. 1: RSPCK delay is the set value of the RSPCK delay register (SPDECR.SCKDL). [In the TI-SSP case] 0: RSPCK delay is 0 RSPCK. 1: RSPCK delay is the set value of the RSPCK delay register (SPDECR.SCKDL).	R/W
20:16	SPB[4:0]	RSPI Data Length 0x00 to 0x02: Setting prohibited (Memo: If it is set them, it is same function as 0x03.) 0x03: 4bit 0x04: 5bit 0x05: 6bit ⋮ 0x1E: 31bit 0x1F: 32bit	R/W
23:21	—	These bits are read as 0. The write value should be 0.	R
26:24	SSLA[2:0]	SSL Signal Assertion 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3	R/W
31:27	—	These bits are read as 0. The write value should be 0.	R

The RSPI has eight RSPI command registers (SPCMD0 to SPCMD7) that are used to set the transfer format of the RSPI in master mode. Furthermore, some bits in SPCMD0 are used to set the transfer format of the RSPI in slave mode. The RSPI in master mode sequentially references SPCMD0 to SPCMD7 according to the setting of the SPSLN[2:0] bits in the RSPI Control register 3 (SPCR3), and then performs serial transfer specified in the referenced SPCMD.

RSPI set the SPCMD register before setting data to be transmitted by referencing the SPCMD when the transmit buffer is empty (while the next-transfer data has not been set).

The SPCMD referenced by the RSPI in master mode is indicated by SPCP[2:0] in the RSPI status register (SPSR). If SPCMD0 is modified while the RSPI in slave mode is enabled (SPCR.SPE = 1), subsequent operation is not guaranteed.

CPHA bit (RSPCK Phase)

This bit is used to set the RSPCK phase of the RSPI in master mode or slave mode. To perform data communication between RSPI modules, the same RSPCK phase must be set for both modules.

When SPCR.SPMS = 0 and SPCR.SPFRF = 1 (in TI SSP mode), setting CPHA = 0 is invalid.

CPOL bit (RSPCK Polarity)

This bit is used to set the RSPCK polarity of the RSPI in master mode or slave mode. To perform data communication between RSPI modules, the same RSPCK polarity must be set for both modules.

BRDV[1:0] bit (Bit Rate Division)

This register is used to determine the bit rate with a combination of the set values of the BRDV[1:0] bits and the RSPI bit rate register (SPCR3.SPBR). The set SPBR value determines the base bit rate. The set BRDV[1:0] bits value is used to select undivided, 2-divided, 4-divided, or 8-divided base bit rate. SPCMD0 to SPCMD7 enable setting of different BRDV[1:0] values. This makes it possible to perform serial transfer with a different bit rate for each command.

SSLKP bit (SSL Signal Level Hold)

This bit is used to set whether to hold or negate the SSL signal level of the current command during a period from the SSL negation timing for the current command to the SSL assertion timing for the next command when the RSPI in master mode performs serial transfer. Setting this bit to 1 enables burst transfer in SPI operation master mode. For details, see section 30.3.12.1. Master mode operation.

To use the RSPI in slave mode, set SSLKP bit to 0.

LSBF bit (RSPI LSB First)

This bit is used to set the data format of the RSPI in master mode or slave mode to MSB first or LSB first.

Bit	Symbol	Function	R/W
15	SCKDEN	RSPCK延迟设置启用[在Motorola-SPI情况下] 0：RSPCK延迟为1RSPCK。1：RSPCK延迟是RSPCK延迟寄存器（SPDECR.SCKDL）的设定值。 [In the TI-SSP case] 0：RSPCK延迟为0RSPCK。1：RSPCK延迟是RSPCK延迟寄存器（SPDECR.SCKDL）的设定值。	R/W
20:16	SPB[4:0]	RSPI数据长度0x00到0x02：禁止设置（备注：如果设置了，则与0x03功能相同。） 0x03: 4bit 0x04: 5bit 0x05: 6bit ⋮ 0x1E: 31bit 0x1F: 32bit	R/W
23:21	—	这些位被读取为0。写入值应为0。	R
26:24	SSLA[2:0]	SSL信号断言 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3	R/W
31:27	—	这些位被读取为0。写入值应为0。	R

RSPI有8个RSPI命令寄存器（SPCMD0到SPCMD7），用于设置主模式下RSPI的传输格式。此外，SPCMD0中的一些位用于设置从机模式下RSPI的传输格式。主机模式下的RSPI根据RSPI控制寄存器3(SPCR3)中SPSLN[2:0]位的设置顺序引用SPCMD0到SPCMD7，然后执行引用的SPCMD中指定的串行传输。

当发送缓冲区为空时（下一次传输数据尚未设置），RSPI在设置要发送的数据之前通过引用SPCMD设置SPCMD寄存器。

RSPI在主模式下引用的SPCMD由RSPI状态寄存器(SPSR)中的SPCP[2:0]指示。如果SPCMD0在从机模式下启用RSPI时修改（SPCR.SPE=1），不能保证后续操作。

CPHA bit (RSPCK Phase)

该位用于设置RSPI在主模式或从模式下的RSPCK相位。要在RSPI模块之间进行数据通信，必须为两个模块设置相同的RSPCK相位。

当SPCR.SPMS=0且SPCR.SPFRF=1（在TISSP模式下）时，设置CPHA=0无效。

CPOL bit (RSPCK Polarity)

该位用于设置RSPI在主模式或从模式下的RSPCK极性。要在RSPI模块之间进行数据通信，必须为两个模块设置相同的RSPCK极性。

BRDV[1:0]位（比特率划分）

该寄存器用于结合BRDV[1:0]位和RSPI比特率寄存器(SPCR3.SPBR)的设置值来确定比特率。设置的SPBR值确定基本比特率。设置的BRDV[1:0]位值用于选择未分频、2分频、4分频或8分频基本比特率。SPCMD0到SPCMD7可以设置不同的BRDV[1:0]值。这使得可以为每个命令以不同的比特率执行串行传输。

SSLKP位（SSL信号电平保持）

该位用于设置在主模式下的RSPI执行串行传输时，从当前命令的SSL否定时序到下一条命令的SSL断言时序期间，是保持还是否定当前命令的SSL信号电平。将此位设置为1可在SPI操作主机模式下启用突发传输。有关详细信息，请参阅第30.3.12.1节。主模式操作。

要在从机模式下使用RSPI，请将SSLKP位设置为0。

LSBF bit (RSPI LSB First)

该位用于设置RSPI在主模式或从模式下的数据格式为MSB优先或LSB优先。

SPNDEN bit (RSPI Next-Access Delay Enable)

This bit is used to set the period (next-access delay) after the RSPI in master mode inactivates the SSL signal at the end of serial transfer until it enables SSL signal assertion of the next access. When SPNDEN bit = 0, the RSPI sets the next-access delay to 1 RSPCK + 5TCLK. When SPNDEN bit = 1, the RSPI inserts the next-access delay in accordance with the RSPI next-access delay register (SPDECR.SPNDL) setting.

To use the RSPI in slave mode, set SPNDEN bit to 0.

SLNDEN bit (SSL Negation Delay Setting Enable)

[In the Motorola-SPI case]

This bit is used to set the period (SSL negation delay) after the RSPI in master mode stops RSPCK oscillation until it inactivates the SSL signal. When SLNDEN bit = 0, the RSPI sets the SSL negation delay to 1 RSPCK. When SLNDEN bit = 1, the RSPI negates the SSL signal with the RSPCK delay in accordance with the slave select negation delay register (SPDECR.SLNDL) setting.

To use the RSPI in slave mode, set SLNDEN bit to 0.

[In the TI-SSP case]

This bit is used to set the period from when the master mode RSPI stops RSPCK oscillation to when the OE signal is inactivated, or when the slave mode RSPI detects the last edge of RSPCK and then negates the OE signal. When the SLNDEN bit is 0, the SSL negate delay is 1 RSPCK in master mode and 1 TCLK in slave mode. When SLNDEN bit = 1, the RSPI negates the SSL signal with the RSPCK delay in accordance with the slave select negation delay register (SPDECR.SLNDL) setting.

When using RSPI in slave mode except TI SSP setting, set the SLNDEN bit to 0.

SCKDEN bit (RSPCK Delay Setting Enable)

[In the Motorola-SPI case]

This bit is used to set the period (RSPCK delay) after the RSPI in master mode activates the SSL signal until it oscillates RSPCK. When SCKDEN bit = 0, the RSPI sets the RSPCK delay to 1 RSPCK. When SCKDEN bit = 1, the RSPI starts RSPCK oscillation with the RSPCK delay in accordance with the RSPCK delay register (SPDECR.SCKDL) setting.

To use the RSPI in slave mode, set SCKDEN bit to 0.

[In the TI-SSP case]

This bit is used to set the period from the start of assertion of the SSL signal to the RSPCK oscillation (RSPCK delay) and the period of the SSL signal to negation by the RSPI in master mode. When SCKDEN bit = 0, the RSPI does not sets the RSPCK delay. When SCKDEN bit = 1, the RSPI starts RSPCK oscillation with the RSPCK delay in accordance with the RSPCK delay register (SPDECR.SPCKDL) setting.

To use the RSPI in slave mode, set SCKDEN bit to 0.

SPB[4:0] bit (RSPI Data Length)

These bits are used to set the transfer data length of the RSPI in master mode or slave mode.

SSLA[2:0] bit (SSL Signal Assertion)

These bits are used to control SSL signal assertion for the RSPI in master mode to perform serial transfer. The set SSLA[2:0] bits value controls assertion of the SSL3 to SSL0 signals. The signal polarity when the SSL signal is asserted depends on the set value of the RSPI slave select polarity register (SPCR3.SSLiP). When SSLA[2:0] bits are set to 000 in multi-master mode, serial transfer is performed with all SSL signals negated (because SSL0 is input).

To use the RSPI in slave mode, set SSLA[2:0] bits to 000.

SPNDEN位（RSPI下一次访问延迟使能）

该位用于设置在主模式下的RSPI在串行传输结束时停用SSL信号之后的周期（下一次访问延迟），直到它启用下一次访问的SSL信号断言。当SPNDEN位=0时，RSPI将下一次访问延迟设置为1RSPCK+5TCLK。当SPNDEN位=1时，RSPI根据RSPI下一次访问延迟寄存器(SPDECR.SPNDL)的设置插入下一次访问延迟。

要在从机模式下使用RSPI，请将SPNDEN位设置为0。

SLNDEN位（SSL否定延迟设置启用）

[In the Motorola-SPI case]

该位用于设置在主模式下的RSPI停止RSPCK振荡直到它停用SSL信号之后的周期（SSL否定延迟）。当SLNDEN位=0时，RSPI将SSL否定延迟设置为1RSPCK。当SLNDEN位=1时，RSPI根据从机选择否定延迟寄存器(SPDECR.SLNDL)的设置，使用RSPCK延迟否定SSL信号。

要在从机模式下使用RSPI，请将SLNDEN位设置为0。

[In the TI-SSP case]

该位用于设置从主模式RSPI停止RSPCK振荡到OE信号无效，或从模式RSPI检测到RSPCK的最后一个边沿然后取消OE信号的周期。当SLNDEN位为0时，SSL否定延迟在主机模式下为1个RSPCK，在从机模式下为1个TCLK。当SLNDEN位=1时，RSPI根据从机选择否定延迟寄存器(SPDECR.SLNDL)的设置，使用RSPCK延迟否定SSL信号。

在除TISSP设置之外的从模式下使用RSPI时，将SLNDEN位设置为0。

SCKDEN位（RSPCK延迟设置使能）

[In the Motorola-SPI case]

该位用于设置在主模式下的RSPI激活SSL信号之后直到其振荡RSPCK的周期（RSPCK延迟）。当SCKDEN位=0时，RSPI将RSPCK延迟设置为1RSPCK。当SCKDEN位=1时，RSPI启动
根据RSPCK延迟寄存器(SPDECR.SCKDL)设置，具有RSPCK延迟的RSPCK振荡。

要在从机模式下使用RSPI，请将SCKDEN位设置为0。

[In the TI-SSP case]

该位用于设置从SSL信号断言开始到RSPCK振荡（RSPCK延迟）的周期，以及SSL信号在主模式下被RSPI否定的周期。当SCKDEN位=0时，RSPI不设置RSPCK延迟。当SCKDEN位=1时，RSPI根据RSPCK延迟启动RSPCK振荡

RSPCK延迟寄存器(SPDECR.SPCKDL)设置。

要在从机模式下使用RSPI，请将SCKDEN位设置为0。

SPB[4:0]位（RSPI数据长度）

这些位用于设置RSPI在主模式或从模式下的传输数据长度。

SSLA[2:0]位（SSL信号断言）

这些位用于控制主模式下RSPI的SSL信号断言以执行串行传输。套装
SSLA[2:0]位值控制SSL3到SSL0信号的断言。SSL信号有效时的信号极性取决于RSPI从机选择极性寄存器(SPCR3.SSLiP)的设置值。当SSLA[2:0]位在多主机模式下设置为000时，串行传输在所有SSL信号取反的情况下执行（因为输入了SSL0）。

要在从机模式下使用RSPI，请将SSLA[2:0]位设置为000。

30.2.7 SPDCR : RSPI Data Control Register

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SPFC[1:0]		—	—	—	SINV	SPRDTD	—	—	BYSW
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BYSW	Byte Swap Operating Mode Select 0: Byte Swap OFF 1: Byte Swap ON	R/W
2:1	—	These bits are read as 0. The write value should be 0.	R/W
3	SPRDTD	RSPI Receive Data or Transmit Data Select 0: The SPDR reads the receive buffer. 1: The SPDR reads the transmit buffer	R/W
4	SINV	Serial data invert bit 0: Not invert serial data 1: Invert serial data.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R
9:8	SPFC[1:0]	Frame Count 0 0: 1 frame 0 1: 2 frame 1 0: 3 frame 1 1: 4 frame	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R

The RSPI data control register (SPDCR) controls the data format.

If the value set in this register is changed while the SPE bit is 1, subsequent operations are not guaranteed.

BYSW bit (Byte Swap Operating Mode Select)

It is a setting bit, that is to swap a transmit/receive data in byte units. A data after byte swap is different by a data length (setting of SPCMD.SPB[4:0]).

When byte swap, A data length (setting of SPB[4:0]) must be set to 32bit or 16bit. Other case of data length (i.e. 4 to 15, 17 to 31-bit length), byte swap is not guaranteed. For the arrangement of data before and after swapping data lengths of 32 bits and 16 bits, see section 30.3.4.3. Byte Swap Transmission and section 30.3.4.4. Byte Swap Reception.

When the parity function set to valid, the behavior is not guaranteed.

SPRDTD bit (RSPI Receive Data or Transmit Data Select)

This bit is used to select receive buffer or transmit buffer from which the RSPI data register (SPDR) value is read.

When the transmit buffer is read, the value that was written to SPDR immediately before is read.

SINV bit (Serial data invert bit)

This bit is used to invert transmit data and receive data.

When the SINV bit is set to 1, transmit buffer (SPTX) data is inverted to invert transmit data and receive data, and then the inverted data is stored in the receive buffer (SPRX). The parity bit is the value corresponding to the inverted transmission/reception data.

30.2.7 SPDCR:RSPI数据控制寄存器

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SPFC[1:0]		—	—	—	SINV	SPRDTD	—	—	BYSW
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BYSW	字节交换操作模式选择 0：字节交换关闭1 ：字节交换开启	R/W
2:1	—	这些位被读取为0。写入值应为0。	R/W
3	SPRDTD	RSPI接收数据或发送数据选择 0：SPDR读取接收缓冲区。1：SPDR读取发送缓冲区	R/W
4	SINV	串行数据反转位 0：不反转串行数据1： 反转串行数据。	R/W
7:5	—	这些位被读取为0。写入值应为0。	R
9:8	SPFC[1:0]	帧数 0 0: 1 frame 0 1: 2 frame 1 0: 3 frame 1 1: 4 frame	R/W
31:10	—	这些位被读取为0。写入值应为0。	R

RSPI数据控制寄存器(SPDCR)控制数据格式。

如果在SPE位为1时更改此寄存器中设置的值，则无法保证后续操作。

BYSW位（字节交换操作模式选择）

它是一个设置位，即以字节为单位交换一个发送接收数据。字节交换后的数据因数据长度不同（SPCMD.SPB[4:0]的设置）。

字节交换时，A数据长度（SPB[4:0]的设置）必须设置为32位或16位。数据长度的其他情况（即4到15、17到31位长度），不保证字节交换。关于交换32位和16位数据长度前后的数据排列，请参见第30.3.4.3节。字节交换传输和第30.3.4.4节。字节交换接收。

当奇偶校验函数设置为有效时，行为不被保证。

SPRDTD位（RSPI接收数据或发送数据选择）

该位用于选择从中读取RSPI数据寄存器(SPDR)值的接收缓冲区或发送缓冲区。

读取发送缓冲区时，会读取之前写入SPDR的值。

SINV位（串行数据反转位）

该位用于反转发送数据和接收数据。

当SINV位设置为1时，发送缓冲器(SPTX)数据反转以反转发送数据和接收数据，然后将反转后的数据存储在接收缓冲器(SPRX)中。奇偶校验位是对应于反转的发送接收数据的值。

SPFC[1:0] bit (Frame Count)

Used for the condition to set the CENDF flag in slave receive only mode.

For details on the CENDF flag setting conditions, refer to section 30.2.9. SPSR : SPI Status Register.

Note that this bit is invalid except in the slave receive only mode.

30.2.8 SPDCR2 : RSPI Data Control Register 2

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x44

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TTRG[1:0]		—	—	—	—	—	—	RTRG[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	RTRG[1:0]	Receive FIFO threshold setting 0 0: threshold 0 0 1: threshold 1 1 0: threshold 2 1 1: threshold 3	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R
9:8	TTRG[1:0]	Transmission FIFO threshold setting 0 0: threshold 0 0 1: threshold 1 1 0: threshold 2 1 1: threshold 3	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

RSPI data control register 2 (SPDCR2) controls the FIFO threshold. If the value set in this register is changed while the SPE bit is 1, subsequent operations are not guaranteed.

RTRG[1:0] bit (Receive FIFO threshold setting)

Set the receive FIFO threshold.

When the number of data stored in the receive FIFO > the number of frames set by RTRG[1:0], the receive buffer full flag is set.

TTRG[1:0] bit (Transmission FIFO threshold setting)

Set the transmit FIFO threshold.

When the number of empty stages in the transmit FIFO > the number of frames set in TTRG[1:0], the transmit buffer empty flag is set.

SPFC[1:0] bit (Frame Count)

用于在从机仅接收模式下设置CENDF标志的条件。

有关CENDF标志设置条件的详细信息，请参阅第30.2.9节。SPSR：SPI状态寄存器。

请注意，除从机仅接收模式外，该位无效。

30.2.8 SPDCR2：RSPI数据控制寄存器2

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x44

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TTRG[1:0]		—	—	—	—	—	—	RTRG[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	RTRG[1:0]	接收FIFO阈值设置 0 0: threshold 0 0 1: threshold 1 1 0: threshold 2 1 1: threshold 3	R/W
7:2	—	这些位被读取为0。写入值应为0。	R
9:8	TTRG[1:0]	传输FIFO阈值设置 0 0: threshold 0 0 1: threshold 1 1 0: threshold 2 1 1: threshold 3	R/W
31:10	—	这些位被读取为0。写入值应为0。	R/W

RSPI数据控制寄存器2(SPDCR2)控制FIFO阈值。如果在SPE位为1时更改此寄存器中设置的值，则无法保证后续操作。

RTRG[1:0]位（接收FIFO阈值设置）

设置接收FIFO阈值。

当接收FIFO中存储的数据数>RTRG[1:0]设置的帧数时，设置接收缓冲区满标志。

TTRG[1:0]位（传输FIFO阈值设置）

设置发送FIFO阈值。

当发送FIFO中的空级数>TTRG[1:0]中设置的帧数时，设置发送缓冲区空标志。

30.2.9 SPSR : SPI Status Register

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SPRF	CENDF	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF	SPDRF	—	—	—	—	—	—	—
Value after reset:	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	SPECM[2:0]			—	SPCP[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	These bits are read as 0. The write value should be 0.	R
10:8	SPCP[2:0]	RSPI Command Pointer 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
11	—	This bit is read as 0. The write value should be 0.	R
14:12	SPECM[2:0]	RSPI Error Command 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
22:15	—	These bits are read as 0. The write value should be 0.	R
23	SPDRF	RSPI Receive Data Ready Flag 0: Receive data ready not detected 1: Receive data ready detected	R
24	OVRF	Overrun Error Flag 0: No overrun error is present. 1: An overrun error is present.	R
25	IDLNF	RSPI Idle Flag 0: The RSPI is in the idle state. 1: The RSPI is in the transfer state.	R
26	MODF	Mode Fault Error Flag 0: Neither mode fault error nor underrun error is present. 1: A mode fault error or underrun error is present.	R
27	PERF	Parity Error Flag 0: No parity error is present. 1: A parity error is present.	R
28	UDRF	Underrun Error Flag This bit indicates error status in combination with the MODF flag. 0: When MODF=0, neither mode fault error nor underrun error is present. When MODF=1, a mode fault error is present. 1: When MODF=0, neither mode fault error nor underrun error is present. When MODF=1, an underrun error is present.	R

30.2.9 SPSR：SPI状态寄存器

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SPRF	CENDF	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF	SPDRF	—	—	—	—	—	—	—
重置后的值：	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	SPECM[2:0]			—	SPCP[2:0]			—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	这些位被读取为0。写入值应为0。	R
10:8	SPCP[2:0]	RSPI命令指针 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
11	—	该位读取为0。写入值应为0。	R
14:12	SPECM[2:0]	RSPI错误命令 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
22:15	—	这些位被读取为0。写入值应为0。	R
23	SPDRF	RSPI接收数据就绪标志 0：未检测到接收数据就绪1：检测到接收数据就绪	R
24	OVRF	溢出错误标志 0：不存在溢出错误。1：存在溢出错误。	R
25	IDLNF	RSPI空闲标志 0：RSPI处于空闲状态。1：RSPI处于传输状态。	R
26	MODF	模式故障错误标志 0：不存在模式故障错误和欠载错误。1：存在模式故障错误或欠载错误。	R
27	PERF	奇偶校验错误标志 0：不存在奇偶校验错误。1：存在奇偶校验错误。	R
28	UDRF	欠载错误标志 该位与MODF标志一起指示错误状态。 0：MODF=0时，既不存在模式故障错误，也不存在欠载错误。当MODF=1时，存在模式故障错误。 1：当MODF=0时，既不存在模式故障错误，也不存在欠载错误。当MODF=1时，存在欠载错误。	R

Bit	Symbol	Function	R/W
29	SPTEF	RSPI Transmit Buffer Empty Flag 0: The number of empty stages in the transmit FIFO ≤ the value set in SPDCR2.TTRG 1: The number of empty stages in the transmit FIFO > the value set in SPDCR2.TTRG	R
30	CENDF	Communication End Flag 0: The RSPI is not communicating or communicating. 1: The RSPI communication completed.	R
31	SPRF	RSPI Receive Buffer Full Flag 0: The number of data stored in the receive FIFO ≤ number of frames set by the SPDCR2.RTRG bit. 1: The number of data stored in the receive FIFO > number of frames set by the SPDCR2.RTRG bit.	R

The RSPI status register (SPSR) stores flags that indicate RSPI's operating status.

SPCP[2:0] bit (RSPI Command Pointer)

These bits indicate RSPI command registers 0 to 7 (SPCMD0 to SPCMD7) indicated by the current pointer in the RSPI sequence control. For details about the RSPI sequence control, see section 30.3.13.1. Master mode operation.

SPECM[2:0] bit (RSPI Error Command)

These bits indicate RSPI command registers 0 to 7 (SPCMD0 to SPCMD7) indicated by the command pointer (SPCP[2:0] bits) when an error was detected in the RSPI sequence control. The RSPI updates the SPECM[2:0] bits value only when an error is detected. When no error is present (OVRF, MODF, and PERF flags in SPSR are 0), the SPECM[2:0] bits value has no meaning. For the RSPI's error detection function, see section 30.3.10. Error Detection. For the RSPI's sequence control, see section 30.3.13.1. Master mode operation.

SPDRF bit (RSPI Receive Data Ready Flag)

During communication (SPCR.SPE = 1), a certain period of time has elapsed while the number of data stored in the reception FIFO ≤ the reception FIFO threshold.

This bit is set to 0 when the reception operation is not performed (SPCR.TXMD [1:0] = 01b).

[Setting (to 1) condition]

All the following two conditions are met.

- SPCR2.SPDRC[7:0] ≠ 00h.
- After the receive FIFO has been written, when the number of data stored in the receive FIFO ≤ the receive FIFO threshold and the value set by SPDRC [7:0] has elapsed

[Clearing (to 0) condition]

- When 1 is written to the SPSRC.SPDRFC bit.

OVRF bit (Overrun Error Flag)

This flag indicates whether an overrun error is present. When the RSPCK clock auto-stop function is enabled (SPCR.SCKASE bit = 1) in master mode (SPCR.MSTR bit = 1), no overrun error occurs and, therefore, this flag is not set to 1. For details, see section 30.3.10.1. Overrun errors.

[Setting (to 1) condition]

When serial transfer is completed in one of the following two conditions with data stored in the receive FIFO for the number of FIFO stages.

- The SPCR.TXMD[1:0] bits = 00b. (transmit-receive mode)
- The SPCR.TXMD[1:0] bits =10b. (receive only)

[Clearing (to 0) condition]

- When 1 is written to the SPSRC.OVRFC bit.

Bit	Symbol	Function	R/W
29	SPTEF	RSPI发送缓冲区空标志 0：发送FIFO中的空级数≤SPDCR2.TTRG中设置的值 1：发送FIFO中的空级数>SPDCR2.TTRG中设置的值	R
30	CENDF	通讯结束标志 0：RSPI不通信或不通信。1：RSPI通信完成。	R
31	SPRF	RSPI接收缓冲区满标志 0：接收FIFO中存储的数据数量≤SPDCR2.RTRG位设置的帧数。 1：接收FIFO中存储的数据数>SPDCR2.RTRG位设置的帧数。	R

RSPI状态寄存器(SPSR)存储指示RSPI操作状态的标志。

SPCP[2:0]位（RSPI命令指针）

这些位指示由RSPI序列控制中的当前指针指示的RSPI命令寄存器0到7（SPCMD0到SPCMD7）。关于RSPI序列控制的详细信息，请参见30.3.13.1节。主模式操作。

SPECM[2:0]位（RSPI错误命令）

当在RSPI序列控制中检测到错误时，这些位指示由命令指针（SPCP[2:0]位）指示的RSPI命令寄存器0到7（SPCMD0到SPCMD7）。RSPI仅在检测到错误时更新SPECM[2:0]位的值。当不存在错误时（SPSR中的OVRF、MODF和PERF标志为0），SPECM[2:0]位值没有意义。关于RSPI的错误检测功能，请参见第30.3.10节。错误检测。对于RSPI的序列控制，请参见第30.3.13.1节。主模式操作。

SPDRF位（RSPI接收数据就绪标志）

在通信过程中（SPCR.SPE=1），接收FIFO中存储的数据数量≤接收FIFO阈值时，经过一定时间。

当不执行接收操作时（SPCR.TXMD[1:0]=01b），该位设置为0。

[Setting (to 1) condition]

满足以下两个条件。

- SPCR2.SPDRC[7:0] ≠ 00h.

●写入接收FIFO后，当接收FIFO中存储的数据数量≤接收FIFO阈值且SPDRC[7:0]设置的值已过去时

[Clearing (to 0) condition]

●当1写入SPSRC.SPDRFC位时。

OVRF位（溢出错误标志）

此标志指示是否存在溢出错误。当在主机模式（SPCR.MSTR位=1）下启用RSPCK时钟自动停止功能（SPCR.SCKASE位=1）时，不会发生溢出错误，因此，该标志不设置为1。详细信息请参见第30.3.10.1节。溢出错误。

[Setting (to 1) condition]

当串行传输在以下两种条件之一中完成时，数据存储在接收FIFO中的FIFO级数。

●SPCR.TXMD[1:0]位=00b。（收发模式）

●SPCR.TXMD[1:0]位=10b。（仅接收）

[Clearing (to 0) condition]

●当1写入SPSRC.OVRFC位时。

IDLNF bit (RSPI Idle Flag)

This flag indicates transfer status of the RSPI.

[Setting (to 1) condition]

[Transmit-Receive, Transmit-only Master mode]

- None of the clearing (to 0) conditions (Transmit-Receive / Transmit-only in Master mode) below is met.

[Receive-only Master mode]

- When 1 is written to RMSTTG of SPCR2.

[Slave mode]

- The SPE bit in SPCR is 1 (RSPI function enabled).

[Clearing (to 0) conditions]

Communication status: 1-(1) to (6) * For details of communication status, see Table 30.4.

[Transmit-Receive, Transmit-only Master mode]

Any of the following two conditions is met.

- The SPE bit in SPCR is 0 (RSPI initialization).
- All the following three conditions are met.
  - The next transfer data is not set in the transmission buffer (SPTXn, n = 0 to 3)
  - The SPCP bits in SPSR are 000 (at the beginning of sequence control).
  - The Operation completed until the next access delay (the master main state machine has transitioned to the idle state)

[Receive-only Master mode]

Communication status: 1-(7) to (9)

Any of the following two conditions is met.

- The SPE bit in SPCR is 0 (RSPI initialization).
- Any of the following 3 conditions is met.
  When RMFM [4:0] = 0x0, after writing 1 to RMEDTG, operation completed until the next access delay (the master main state machine has transitioned to the idle state)
  When RMFM [4:0] ≠ 0x0, after writing 1 to RMEDTG, operation completed until the next access delay (the master main state machine has transitioned to the idle state)
  When RMFM [4:0] ≠ 0x0, the operation is completed up to the next access delay after processing is completed for the number of received frames set in RMFM [4:0] (the master main state machine has transitioned to the idle state)

[Slave mode]

Communication status: 0-(1) to (9)

- The SPE bit in SPCR is 0 (RSPI initialization).

MODF bit (Mode Fault Error Flag)

This flag indicates whether a mode fault error or an underrun error is present. The UDRF flag allows you to see which error (mode fault error or underrun error) has occurred.

[Setting (to 1) condition]

[Multi-master mode]

- The SSL0 pin input level becomes active level while the SPCR.MSTR bit = 1 (master mode) and the SPCR.MODFEN bit = 1 (mode fault error detection enabled), and then the RSPI has detected a mode fault error.

[Slave, Motorola-SPI mode]

Any of the following two conditions is met.

IDLNF位（RSPI空闲标志）

该标志指示RSPI的传输状态。

[Setting (to 1) condition]

[Transmit-Receive, Transmit-only Master mode]

●不满足以下清零条件（Transmit-ReceiveTransmit-onlyinMastermode）。

[Receive-only Master mode]

●当SPCR2的RMSTTG写入1时。

[Slave mode]

●SPCR中的SPE位为1（RSPI功能使能）。

[Clearing (to 0) conditions]

通信状态：1-(1)～(6)*通信状态详见表30.4。

[Transmit-Receive, Transmit-only Master mode]

满足以下两个条件中的任何一个。

●SPCR中的SPE位为0（RSPI初始化）。

●满足以下三个条件。

下一个传输数据未设置在传输缓冲区中（SPTXn，n=0到3）

SPSR中的SPCP位为000（在序列控制的开头）。

操作完成，直到下一次访问延迟（主主状态机已转换为空闲状态）

[Receive-only Master mode]

通讯状态：1-（7）至（9）

满足以下两个条件中的任何一个。

●SPCR中的SPE位为0（RSPI初始化）。

●满足以下3个条件中的任何一个。

当RMFM[4:0]=0x0时，向RMEDTG写1后，操作完成，直到下一次访问延迟（主主状态机已转变为空闲状态）当RMFM[4:0]≠0x0时，向1后写入RMEDTG，操作完成，直到下一次访问延迟（主主状态机已转变为空闲状态）当RMFM[4:0]≠0x0时，处理完成后操作完成到下一次访问延迟的次数在RMFM[4:0]中设置的接收帧（主主状态机已转换到空闲状态）

[Slave mode]

通讯状态：0-(1)到(9)

●SPCR中的SPE位为0（RSPI初始化）。

MODF位（模式故障错误标志）

该标志指示是否存在模式故障错误或欠载错误。UDRF标志允许您查看发生了哪个错误（模式故障错误或欠载错误）。

[Setting (to 1) condition]

[Multi-master mode]

●当SPCR.MSTR位=1（主机模式）和SPCR.MODFEN位=1（启用模式故障错误检测）时SSL0引脚输入电平变为有效电平，然后RSPI检测到模式故障错误。

[Slave, Motorola-SPI mode]

满足以下两个条件中的任何一个。

- The SSL0 pin is negated before the RSPCK cycles necessary for data transfer end while the SPCR.MSTR bit = 0 (slave mode), SPCR.SPFRF bit = 0 (Motorola-SPI) and the SPCR.MODFEN bit = 1 (mode fault error detection enabled), and then the RSPI has detected a mode fault error.
- Serial transfer is started before transmit data output becomes ready while the SPCR.SPE bit = 1 (RSPI function enabled), and then the RSPI has detected an underrun error.

[Slave, TI-SSP mode]

Any of the following two conditions is met.

- The SSL0 pin is asserted before the RSPCK cycles necessary for data transfer end while the SPCR.MSTR bit = 0 (slave mode), SPCR.SPFRF bit = 1 (TI-SSP) and the SPCR.MODFEN bit = 1 (mode fault error detection enabled), and then the RSPI has detected a mode fault error.
- Serial transfer is started before transmit data output becomes ready while the SPCR.SPE bit = 1 (RSPI function enabled), and then the RSPI has detected an underrun error.

The SSL signal active level depends on the SPCR3.SSLiP bits (SSL signal polarity bits).

[Clearing (to 0) condition]

- When 1 is written to the SPSRC.MODFC bit.

PERF bit (Parity Error Flag)

This flag indicates whether a parity error is present.

[Setting (to 1) condition]

When the serial transfer ends and a parity error is detected with the SPPE bit of SPCR set to 1 under any of the following 2 conditions.

- The SPCR.TXMD[1:0] bit = 00b. (transmit-receive master mode or transmit-receive slave mode)
- The SPCR.TXMD[1:0] bit = 10b. (receive-only master mode or receive-only slave mode)

[Clearing (to 0) condition]

- When 1 is written to the SPSRC.PERFC bit.

UDRF bit (Underrun Error Flag)

This flag indicates that a mode fault error or an underrun error is present.

[Setting (to 1) condition]

- Serial transfer is started before transmit data output becomes ready while the SPCR.MSTR bit = 0 and the SPCR.TXMD[1:0] bit = 00b or 01b (transmit-receive slave mode or transmit-only slave mode) and the SPCR.SPE bit = 1 (RSPI function enabled), and then the RSPI has detected an underrun error.

[Clearing (to 0) condition]

- When 1 is written to the SPSRC.UDRFC bit.

SPTEF bit (RSPI Transmit Buffer Empty Flag)

This flag indicates the transmit buffer (SPTX) status in the RSPI data register (SPDR).

[Setting (to 1) condition]

Any of the following 3 conditions is met.

- The SPE bit is set to 0 (RSPI initialization).
- When the number of empty transmission FIFO stages > the value set in SPDCR2.TTRG [1:0].
- When 1 is written to SPFCR.SPFRST.

[Clearing (to 0) condition]

Any of the following two conditions is met.

●当SPCR.MSTR位=0（从模式）、SPCR.SPFRF位=0（摩托罗拉-SPI）和SPCR.MODFEN位=1（模式故障）时，SSL0引脚在数据传输结束所需的RSPCK周期之前被否定错误检测启用），然后RSPI检测到模式故障错误。

●当SPCR.SPE位=1（RSPI功能使能）时，在发送数据输出准备好之前开始串行传输，然后RSPI检测到欠载错误。

[Slave, TI-SSP mode]

满足以下两个条件中的任何一个。

●当SPCR.MSTR位=0（从模式）、SPCR.SPFRF位=1(TI-SSP)和SPCR.MODFEN位=1（模式故障）时，SSL0引脚在数据传输所需的RSPCK周期结束之前被置位错误检测启用），然后RSPI检测到模式故障错误。

●当SPCR.SPE位=1（RSPI功能使能）时，在发送数据输出准备好之前开始串行传输，然后RSPI检测到欠载错误。

SSL信号有效电平取决于SPCR3.SSLiP位（SSL信号极性位）。

[Clearing (to 0) condition]

●当1写入SPSRC.MODFC位时。

PERF位（奇偶校验错误标志）

该标志指示是否存在奇偶校验错误。

[Setting (to 1) condition]

当串行传输结束并且在以下2个条件中的任何一个条件下检测到奇偶校验错误且SPCR的SPPE位设置为1时。

●SPCR.TXMD[1:0]位=00b。（发送-接收主模式或发送-接收从模式）

●SPCR.TXMD[1:0]位=10b。（只接收主模式或只接收从模式）

[Clearing (to 0) condition]

●当1写入SPSRC.PERFC位时。

UDRF位（欠载错误标志）

该标志指示存在模式故障错误或欠载错误。

[Setting (to 1) condition]

●当SPCR.MSTR位=0且发送数据输出就绪时串行传输开始
SPCR.TXMD[1:0]位=00b或01b（发送接收从模式或仅发送从模式）且SPCR.SPE位=1（启用RSPI功能），然后RSPI检测到欠载错误。

[Clearing (to 0) condition]

●当1写入SPSRC.UDRFC位时。

SPTEF位（RSPI发送缓冲区空标志）

该标志指示RSPI数据寄存器(SPDR)中的发送缓冲区(SPTX)状态。

[Setting (to 1) condition]

满足以下3个条件中的任何一个。

●SPE位设置为0（RSPI初始化）。

●当空传输FIFO级数>SPDCR2.TTRG[1:0]中设置的值时。

●当1写入SPFCR.SPFRST时。

[Clearing (to 0) condition]

满足以下两个条件中的任何一个。

- At the time of final access when transmission data is written to SPDR (SPTXn, n = 0 to 3) in one processing routine using DTC / DMAC.
- When 1 is written to the SPSRC.SPTEFC bit.

Writing a value to the SPDR register is enabled only while the SPTEF flag = 1. If a value is written to the SPDR register while the SPTEF flag = 0, transmit buffer data is not updated.

CENDF bit (Communication End Flag)

This flag indicates communication end status of RSPI. It turns 1 at communication end and turns 0 at starting next communication.

[Setting (to 1) condition]

Transmit-Receive / Transmit-only Master mode

Communication status: 1-(1) to (6) * For details of communication status, see Table 30.4.

The following 3 conditions are met.

- The next transfer data is not set in the transmission buffer (SPTXn, n = 0 to 3)
- The SPSR.SPCP[2:0] are 3'b000. (It means the head of the sequential control.)
- Operation completed until the next access delay (the master main state machine has transitioned to the idle state)

Receive-only Master mode

Communication status: 1-(7) to (9)

Any of the following 3 conditions is met.

- When RMFM [4:0] = 0x0, after writing 1 to RMEDTG, operation completed until the next access delay (the master main state machine has transitioned to the idle state)
- When RMFM [4:0] ≠ 0x0, after writing 1 to RMEDTG, operation completed until the next access delay (the master main state machine has transitioned to the idle state)
- When RMFM [4:0] ≠ 0x0, the operation is completed up to the next access delay after processing is completed for the number of received frames set in RMFM [4:0] (the master main state machine has transitioned to the idle state)

Transmit-receive / transmit-only slave, Motorola-SPI mode @ SPI serial communication (4-wire: the SPCR.SPMS bit is 0)

Communication status: 0-(1), (4)

The following 3 conditions are met.

- The next transfer data is not set in the transmission buffer
- The transmission shift register is empty. (It means RSPI does not do serial transfer.)
- SSL0 was negated.

Transmit-receive / transmit-only slave, TI-SSP mode @ SPI serial communication (4-wire: the SPCR.SPMS bit is 0)

Communication status: 0-(2), (5)

The following 3 conditions are met.

- The next transfer data is not set in the transmission buffer
- The transmission shift register is empty. (It means RSPI does not do serial transfer.)
- When the SSL negate delay is completed.

Transmit-receive / transmit only slave mode @ clock synchronous (3-wire: the SPCR.SPMS bit is 1)

Communication status: 0-(3), (6)

The following 3 conditions are met.

- The next transfer data is not set in the transmission buffer
- The transmission shift register is empty. (It means RSPI does not do serial transfer.)
- The last even edge of RSPCK of the frame was detected. (When the SPCMD.CPHA bit is 1.)

●在使用DTCDMAC的一个处理程序中将传输数据写入SPDR(SPTXn n=0至3)的最终访问时。

●当向SPSRC.SPTEFC位写入1时。

仅当SPTEF标志=1时才允许将值写入SPDR寄存器。如果在SPTEF标志=0时将值写入SPDR寄存器，则不会更新发送缓冲区数据。

CENDF位（通信结束标志）

该标志指示RSPI的通信结束状态。通讯结束时变为1，开始下一次通讯时变为0。

[Setting (to 1) condition]

发送-接收仅发送主模式

通信状态：1-(1)～(6)*通信状态详见表30.4。

满足以下3个条件。

●下一个传输数据未设置在传输缓冲区中（SPTXn，n=0到3）

●SPSR.SPCP[2:0]为3'b000。（表示顺序控制的头部。）

●操作完成，直到下一次访问延迟（主主状态机已转换为空闲状态）

仅接收主模式

通讯状态：1-（7）至（9）

满足以下3个条件中的任何一个。

●当RMFM[4:0]=0x0时，向RMEDTG写入1后，操作完成，直到下一次访问延迟（主主状态机已转换为空闲状态）

●当RMFM[4:0]≠0x0时，向RMEDTG写1后，操作完成，直到下一次访问延迟（主主状态机已转移到空闲状态）

●RMFM[4:0]≠0x0时，在处理完成RMFM[4:0]中设置的接收帧数后直到下一个访问延迟完成操作（主主状态机已转换为空闲状态）

Transmit-receive仅发送从机，Motorola-SPI模式@SPI串行通信（4线：SPCR.SPMS位为0）

Communication status: 0-(1), (4)

满足以下3个条件。

●下一个传输数据未设置在传输缓冲区中

●传输移位寄存器为空。（这意味着RSPI不进行串行传输。）

●SSL0被否定。

发送-接收仅发送从机，TI-SSP模式@SPI串行通信（4线：SPCR.SPMS位为0）

Communication status: 0-(2), (5)

满足以下3个条件。

●下一个传输数据未设置在传输缓冲区中

●传输移位寄存器为空。（这意味着RSPI不进行串行传输。）

●SSL否定延迟完成时。

发送-接收仅发送从模式@时钟同步（3线：SPCR.SPMS位为1）

Communication status: 0-(3), (6)

满足以下3个条件。

●下一个传输数据未设置在传输缓冲区中

●传输移位寄存器为空。（这意味着RSPI不进行串行传输。）

●检测到帧RSPCK的最后一个偶数边缘。（当SPCMD.CPHA位为1时。）

Receive only slave, Motorola-SPI mode @ SPI serial communication (4-wire: the SPCR.SPMS bit is 0)

Communication status: 0-(7)

The following condition is met.

- SSL0 input was negated after getting frames for SPDCR.SPFC set value in the receive buffer.

Receive only slave, TI-SSP mode @ SPI serial communication (4-wire: the SPCR.SPMS bit is 0)

Communication status: 0-(8)

The following condition is met.

- SSL0 negate delay is completed after getting frames for SPDCR.SPFC set value in the receive buffer.

Receive only slave mode @ clock synchronous (3-wire: the SPCR.SPMS bit is 1)

Communication status: 0-(9)

The following condition is met.

- The last even edge of RSPCK of the Last frame received for SPFC sets value. (When the SPCMD.CPHA bit is 1.)

[Clearing (to 0) condition]

Transmit-Receive / Transmit-only Master mode

Communication status: 1-(1) to (6)

Any of the following 2 conditions is met.

- The next transmit data was written to the transmit buffer (SPTX).
- When 1 is written to the SPSRC.CENDFC bit.

Receive -only Master mode

Communication status: 1-(7) to (9)

Any of the following 2 conditions is met.

- When 1 is written to the SPCR2.RMSTTG bit with SPE = 1.
- When 1 is written to the SPSRC.CENDFC bit.

Transmit-receive / transmit only slave mode

Communication status: 0-(1) to (6)

Satisfy one of following.

- The next transmit data was written to the transmit buffer (SPTX).
- When 1 is written to the SPSRC.CENDFC bit.

Receive only slave mode @ SPI serial communication (4-wire: the SPCR.SPMS bit is 0)

Communication status: 0-(7) to (8)

Satisfy one of following.

- SSL0 assertion of next data was detected.
- When 1 is written to the SPSRC.CENDFC bit.

Receive only slave mode @ clock synchronous (3-wire: the SPCR.SPMS bit is 1)

Communication status: 0-(9)

Satisfy one of following.

- The first edge of RSPCK of the next data was detected.
- When 1 is written to the SPSRC.CENDFC bit.

仅接收从机，Motorola-SPI模式@SPI串行通信（4线：SPCR.SPMS位为0）

Communication status: 0-(7)

满足以下条件。

●在接收缓冲区中获得SPDCR.SPFC设置值的帧后，SSL0输入被否定。

仅接收从机，TI-SSP模式@SPI串行通信（4线：SPCR.SPMS位为0）

Communication status: 0-(8)

满足以下条件。

●SSL0negatedelay在接收缓冲区中获得SPDCR.SPFC设置值的帧后完成。

仅接收从模式@时钟同步（3线：SPCR.SPMS位为1）

Communication status: 0-(9)

满足以下条件。

●SPFC接收的Last帧的RSPCK的最后一个偶数边设置值。（当SPCMD.CPHA位为1时。）

[Clearing (to 0) condition]

发送-接收仅发送主模式

通讯状态：1-(1)到(6)

满足以下2个条件中的任何一个。

●下一个发送数据被写入发送缓冲区(SPTX)。

●当1写入SPSRC.CENDFC位时。

仅接收主模式

通讯状态：1-（7）至（9）

满足以下2个条件中的任何一个。

●当SPE=1时向SPCR2.RMSTTG位写入1。

●当1写入SPSRC.CENDFC位时。

发送-接收仅发送从模式

通讯状态：0-(1)到(6)

满足以下之一。

●下一个发送数据被写入发送缓冲区(SPTX)。

●当1写入SPSRC.CENDFC位时。

仅接收从机模式@SPI串行通信（4线：SPCR.SPMS位为0）

通讯状态：0-(7)到(8)

满足以下之一。

●检测到下一个数据的SSL0断言。

●当1写入SPSRC.CENDFC位时。

仅接收从模式@时钟同步（3线：SPCR.SPMS位为1）

Communication status: 0-(9)

满足以下之一。

●检测到下一个数据的RSPCK的第一个边沿。

●当1写入SPSRC.CENDFC位时。

SPRF bit (RSPI Receive Buffer Full Flag)

This flag indicates the receive buffer (SPRX) status in the RSPI data register (SPDR).

[Setting (to 1) condition]

When the number of data stored in the receive FIFO > the number of frames set in the SPDCR2.RTRG [1:0] bits in Transmit-Receive, receive-only mode. However, the SPRF flag does not change from 0 to 1 while the OVRF flag = 1. (See section 30.3.10. Error Detection.)

[Clearing (to 0) condition]

Any of the following 3 conditions is met.

- At the last access when read data is read from SPDR (SPRXn, n = 0 to 3) in one processing routine using DTC / DMAC
- When 1 is written to the SPSRC.SPRFC bit
- When 1 is written to the SPFCR.SPFRST bit

30.2.10 SPTFSR : RSPI Transfer FIFO Status Register

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x58

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	TFDN[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
2:0	TFDN[2:0]	Transmit FIFO data empty stage number 0 0 0: Number of empty stages 0 ⋮ 1 0 0: Number of empty stages 4	R
31:3	—	These bits are read as 0. The write value should be 0.	R

TFDN[2:0] bit (Transmit FIFO data empty stage number)

Displays the number of empty transmission FIFO stages. By clearing the SPCR.SPE bit, TFDN[2:0] will be the initial value after reset (= all empty).

30.2.11 SPRFSR : RSPI Receive FIFO Status Register

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x5C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	RFDN[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

SPRF位（RSPI接收缓冲区满标志）

该标志指示RSPI数据寄存器(SPDR)中的接收缓冲区(SPRX)状态。

[Setting (to 1) condition]

当接收FIFO中存储的数据数量>中设置的SPDCR2.RTRG[1:0]位中的帧数时
发送-接收，仅接收模式。但是，当OVRF标志=1时，SPRF标志不会从0变为1。（请参阅第30.3.10节。错误检测。）

[Clearing (to 0) condition]

满足以下3个条件中的任何一个。

●在使用DTCDMAC的一个处理例程中从SPDR(SPRXn n=0到3)读取读取数据时的最后一次访问

●当1写入SPSRC.SPRFC位时

●当1写入SPFCR.SPFRST位时

30.2.10 SPTFSR:RSPI传输FIFO状态寄存器

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x58

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	TFDN[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
2:0	TFDN[2:0]	发送FIFO数据空阶段号 000：空级数0 ⋮ 100：空级数4	R
31:3	—	这些位被读取为0。写入值应为0。	R

TFDN[2:0]位（发送FIFO数据空阶段号）

显示空传输FIFO阶段的数量。通过清除SPCR.SPE位，TFDN[2:0]将是复位后的初始值（=全部为空）。

30.2.11 SPRFSR:RSPI接收FIFO状态寄存器

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x5C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	RFDN[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
2:0	RFDN[2:0]	Receive FIFO data store stage number 0 0 0: Number of store stages 0 ⋮ 1 0 0: Number of store stages 4	R
31:3	—	These bits are read as 0. The write value should be 0.	R

RFDN[2:0] bit (Receive FIFO data store stage number)

Displays the number of stores receive FIFO stages. RFDN [2:0] is cleared by clearing the SPCR.SPE bit.

30.2.12 SPPSR : RSPI Polling Register

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x60

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SPEPS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPEPS	RSPI Poling Status 0: SPCR.SPE is 0 1: SPCR.SPE is 1	R
31:1	—	These bits are read as 0. The write value should be 0.	R

SPEPS bit (RSPI Poling Status)

This bit selects whether to enable or disable the synchronization bypass function. This bit can be used to bypass the synchronization circuit only when the same clock is input to the bus clock (PCLK) and operation clock (TCLK).

30.2.13 SPSRC : RSPI Status Clear Register

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x68

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SPRFC	CENDFC	SPTEFC	UDRFC	PERFC	MODFC	—	OVRFC	SPDRFC	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
22:0	—	These bits are read as 0. The write value should be 0.	R
23	SPDRFC	RSPI Receive Data Ready Flag Clear The RSPI receive data ready flag can be cleared by writing 1. When read, 0 is read.	W

Bit	Symbol	Function	R/W
2:0	RFDN[2:0]	接收FIFO数据存储阶段号 000：存储级数0 ⋮ 100：存储级数4	R
31:3	—	这些位被读取为0。写入值应为0。	R

RFDN[2:0]位（接收FIFO数据存储阶段编号）

显示存储接收FIFO阶段的数量。RFDN[2:0]通过清零SPCR.SPE位来清零。

30.2.12 SPPSR:RSPI轮询寄存器

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x60

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SPEPS
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPEPS	RSPI轮询状态 0: SPCR.SPE is 0 1: SPCR.SPE is 1	R
31:1	—	这些位被读取为0。写入值应为0。	R

SPEPS位（RSPI轮询状态）

该位选择是启用还是禁用同步旁路功能。只有当总线时钟（PCLK）和操作时钟（TCLK）输入相同的时钟时，该位才能用于绕过同步电路。

30.2.13 SPSRC:RSPI状态清除寄存器

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x68

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SPRFC	CENDFC	SPTEFC	UDRFC	PERFC	MODFC	—	OVRFC	SPDRFC	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
22:0	—	这些位被读取为0。写入值应为0。	R
23	SPDRFC	RSPI接收数据就绪标志清零 RSPI接收数据就绪标志可以通过写1来清零。读时，读0。	W

Bit	Symbol	Function	R/W
24	OVRFC	Overrun Error Flag Clear By writing 1, the Overrun Error Flag can be cleared. Reading value is always 0.	W
25	—	This bit is read as 0. The write value should be 0.	R
26	MODFC	Mode Fault Error Flag Clear By writing 1, the Mode Fault Error Flag can be cleared. Reading value is always 0.	W*1
27	PERFC	Parity Error Flag Clear By writing 1, the Parity Error Flag can be cleared. Reading value is always 0.	W
28	UDRFC	Underrun Error Flag Clear By writing 1, the Underrun Error Flag can be cleared. Reading value is always 0.	W*2
29	SPTEFC	RSPI Transmit Buffer Empty Flag Clear By writing 1, the RSPI Transmit Buffer Empty Flag can be cleared. Reading value is always 0.	W
30	CENDFC	Communication End Flag Clear By writing 1, the Communication End Flag can be cleared. Reading value is always 0.	W
31	SPRFC	RSPI Receive Buffer Full Flag Clear By writing 1, the RSPI Receive Buffer Full Flag can be cleared. Reading value is always 0.	W

Note 1. Before setting MODFC and UDRFC, make sure that SPSR.MODF and UDRF are set to 1.
Note 2. When clearing the UDRF flag, clear the MODF flag at the same time (MODFC = 1).

The RSPI status clear register (SPSRC) is a register that clears the status flag (SPSR) that indicates the operating status of RSPI.

30.2.14 SPFCR : RSPI FIFO Clear Register

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x6C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SPFRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPFRST	RSPI FIFO clear By writing 1, the pointer in the FIFO and the stored data are initialized. Reading value is always 0.	W
31:1	—	These bits are read as 0. The write value should be 0.	R

The FIFO clear register (SPFCR) is used to clear the FIFO.

If SPFCR is rewritten while the SPE bit of the RSPI control register (SPCR) is 1, subsequent operations are not guaranteed.

SPFRST bit (RSPI FIFO clear)

Initializing the pointer and stored data in the transmit / receive FIFO by writing 1

30.3 Operation

In this section, the serial transfer period refers to the period from the beginning of driving valid data to the fetching of the final valid data.

Bit	Symbol	Function	R/W
24	OVRFC	溢出错误标志清除 通过写入1，可以清除溢出错误标志。读数值始终为0。	W
25	—	该位读取为0。写入值应为0。	R
26	MODFC	模式故障错误标志清除 通过写入1，可以清除模式故障错误标志。读数值始终为0。	W*1
27	PERFC	奇偶校验错误标志清除 通过写入1，可以清除奇偶校验错误标志。读数值始终为0。	W
28	UDRFC	欠载错误标志清除 通过写入1，可以清除欠载错误标志。读数值始终为0。	W*2
29	SPTEFC	RSPI发送缓冲区空标志清除 通过写1，可以清除RSPI发送缓冲区空标志。读数值始终为0。	W
30	CENDFC	通讯结束标志清除 通过写入1，可以清除通信结束标志。读数值始终为0。	W
31	SPRFC	RSPI接收缓冲器满标志清除 通过写1，可以清除RSPI接收缓冲区满标志。读数值始终为0。	W

注意1.在设置MODFC和UDRFC之前，请确保SPSR.MODF和UDRF设置为1。
注2.清除UDRF标志时，同时清除MODF标志（MODFC=1）。

RSPI状态清除寄存器(SPSRC)是用于清除状态标志(SPSR)的寄存器，该状态标志指示RSPI.

30.2.14 SPFCR:RSPIFIFO清除寄存器

Base address: SPI_Bn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x6C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SPFRST
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPFRST	RSPI FIFO clear 通过写1，初始化FIFO中的指针和存储的数据。读数值始终为0。	W
31:1	—	这些位被读取为0。写入值应为0。	R

FIFO清除寄存器(SPFCR)用于清除FIFO。

如果在RSPI控制寄存器(SPCR)的SPE位为1时重写SPFCR，则无法保证后续操作。

SPFRST bit (RSPI FIFO clear)

通过写入1初始化发送接收FIFO中的指针和存储的数据

30.3 Operation

在本节中，串行传输周期是指从开始驱动有效数据到获取最终有效数据的周期。

30.3.1 Overview of SPI Operation

The SPI is capable of synchronous serial transfers in the following modes:

- Slave mode (SPI operation)
- Single master mode (SPI operation)
- Multi-master mode (SPI operation)
- Slave mode (clock synchronous operation)
- Master mode (clock synchronous operation)

The SPI mode can be selected by using the MSTR, MODFEN, SPMS, and SPFRF bits in SPCR. Table 30.6 lists the relationship between SPI modes and SPCR settings, and a description of each mode.

Table 30.6 Relationship between SPCR settings and SPI modes (1 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1
SPFRF bit setting	valid	valid	valid	Invalid	Invalid
RSPCKn pins	Input	Output	Output/Hi-Z	Input	Output
MOSIn pin	Input	Output	Output/Hi-Z	Input	Output
MISOn pin	Output/Hi-Z	Input	Input	Output	Input
SSLn0 pins	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 pins	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	Supported	—	—
Max transfer rate	TCLK/2	TCLK/2	TCLK/2	TCLK/2	TCLK/2
Clock source	RSPCK input	On-chip baud rate generator	On-chip baud rate generator	RSPCK input	On-chip baud rate generator
Clock polarity	Two				
Clock phase	Two*6	Two*6	Two*6	One (CPHA = 1)	Two
Transfer data length	4 to 32 bits				
Burst transfer	Possible (CPHA = 1)	Possible (CPHA = 0, 1)	Possible (CPHA = 0, 1)	—	—
RSPCK delay control	Not supported	Supported	Supported	Not supported	Supported
SSL negation delay control	Not supported*7	Supported	Supported	Not supported	Supported
Next-access delay control	Not supported	Supported	Supported	Not supported	Supported
Transfer trigger	SSL input active or RSPCK oscillation	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)	RSPCK oscillation	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)
Sequence control	Not supported	Supported	Supported	Not supported	Supported
Transmit buffer empty detection	Supported*5				
Receive buffer full detection	Supported*2				
Overrun error detection	Supported*2	Supported*2 *4	Supported*2 *4	Supported*2	Supported*2

30.3.1 SPI操作概述

SPI能够在以下模式下进行同步串行传输：

●从机模式（SPI操作）

●单主模式（SPI操作）

- Multi-master mode (SPI operation)

●从机模式（时钟同步操作）

●主模式（时钟同步操作）

可以使用SPCR中的MSTR、MODFEN、SPMS和SPFRF位选择SPI模式。表30.6列出了SPI模式和SPCR设置之间的关系，以及每种模式的说明。

Table 30.6 SPCR设置和SPI模式之间的关系(1of2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	从机（时钟同步操作）	主控（时钟同步操作）
MSTR位设置	0	1	1	0	1
MODFEN位设置	0 or 1	0	1	0	0
SPMS位设置	0	0	0	1	1
SPFRF位设置	valid	valid	valid	Invalid	Invalid
RSPCKn pins	Input	Output	Output/Hi-Z	Input	Output
MOSIn pin	Input	Output	Output/Hi-Z	Input	Output
MISOn pin	Output/Hi-Z	Input	Input	Output	Input
SSLn0 pins	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1到SSLn3引脚	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL极性改变功能	Supported	Supported	Supported	—	—
最大传输率	TCLK/2	TCLK/2	TCLK/2	TCLK/2	TCLK/2
时钟源	RSPCK input	片上波特率发生器	片上波特率发生器	RSPCK input	片上波特率发生器
时钟极性	Two				
时钟相位	Two*6	Two*6	Two*6	One (CPHA = 1)	Two
传输数据长度	4到32位				
突发传输	Possible (CPHA = 1)	Possible (CPHA = 0, 1)	Possible (CPHA = 0, 1)	—	—
RSPCK延迟控制	不支持	Supported	Supported	不支持	Supported
SSL否定延迟控制	不支持*7	Supported	Supported	不支持	Supported
下一次访问延迟控制	不支持	Supported	Supported	不支持	Supported
转移触发	SSL输入有效或RSPCK振荡	在产生发送缓冲区空中断请求时写入发送缓冲区(SPTEF=1)	在产生发送缓冲区空中断请求时写入发送缓冲区(SPTEF=1)	RSPCK oscillation	在产生发送缓冲区空中断请求时写入发送缓冲区(SPTEF=1)
顺序控制	不支持	Supported	Supported	不支持	Supported
发送缓冲区空检测	Supported*5				
接收缓冲区满检测	Supported*2				
溢出错误检测	Supported*2	Supported*2 *4	Supported*2 *4	Supported*2	Supported*2

Table 30.6 Relationship between SPCR settings and SPI modes (2 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
Parity error detection	Supported*3 *2				
Mode fault error detection	Supported (MODFEN = 1)	Not supported	Supported	Not supported	Not supported
Underrun error detection	Supported*5	Not supported	Not supported	Supported*5	Not supported

Note 1. This function is not supported in this mode.
Note 2. When SPI is transmit-master mode or transmit-slave mode (refer to Table 30.4), detection of receive buffer full, overrun error, and parity error are not performed.
Note 3. When the SPCR.SPPE bit is 0, parity error detection is not performed.
Note 4. When the SPCR.SCKASE bit is 1, overrun error detection does not proceed.
Note 5. When SPI is receive only slave mode, none of transmit buffer empty and underrun error is detected.
Note 6. CPHA = 0 is invalid in TI SSP mode. (If it is set, the operation is the same as when CPHA = 1.)
Note 7. Supported only in TI SSP mode.

30.3.2 Controlling the SPI Pins

Based on the settings of the MSTR, MODFEN, and SPMS bits in SPCR and the PmnPFS.NCODR bit for I/O Ports, the SPI can switch pin states. Table 30.7 lists the relationship between pin states and bit settings. Setting the PmnPFS.NCODR bit for an I/O port to 0 selects the CMOS output. Setting it to 1 selects the open-drain output. The I/O port settings must follow this relationship.

Table 30.7 Relationship between pin states and bit settings (1 of 2)

Mode	Pin	Pin state*2	
		PmnPFS.NCODR bit for I/O ports = 0	PmnPFS.NCODR bit for I/O ports = 1
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3	CMOS output	Open-drain output
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLn0	Input	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOn	Input	Input
Slave mode (SPI operation) (MSTR = 0, SPMS = 0)	RSPCKn	Input	Input
	SSLn0	Input	Input
	SSLn1 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
Master mode (clock synchronous operation) (MSTR = 1, MODFEN = 0, SPMS = 1)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input

Table 30.6 SPCR设置和SPI模式之间的关系(2of2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	从机（时钟同步操作）	主控（时钟同步操作）
奇偶校验错误检测	Supported*3 *2				
模式故障错误检测	Supported (MODFEN = 1)	不支持	Supported	不支持	不支持
欠载错误检测	Supported*5	不支持	不支持	Supported*5	不支持

注1.此模式不支持此功能。
注2.当SPI为发送主模式或发送从模式时（参见表30.4），不执行接收缓冲区满、溢出错误和奇偶校验错误的检测。

注3.当SPCR.SPPE位为0时，不执行奇偶校验错误检测。
注4.当SPCR.SCKASE位为1时，不进行溢出错误检测。
注5.当SPI为仅接收从机模式时，不会检测到发送缓冲区为空和欠载错误。
注6.CPHA=0在TISSP模式下无效。（如果已设置，则操作与CPHA=1时相同。）
注7.仅在TISSP模式下受支持。

30.3.2 控制SPI引脚

根据SPCR中的MSTR、MODFEN和SPMS位以及IO端口的PmnPFS.NCODR位的设置，SPI可以切换引脚状态。表30.7列出了引脚状态和位设置之间的关系。将IO端口的PmnPFS.NCODR位设置为0可选择CMOS输出。将其设置为1选择开漏输出。IO端口设置必须遵循这种关系。

Table 30.7 引脚状态和位设置之间的关系(1of2)

Mode	Pin	引脚状态*2	
		IO端口的PmnPFS.NCODR位=0	IO端口的PmnPFS.NCODR位=1
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3	CMOS output	Open-drain output
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLn0	Input	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOn	Input	Input
从机模式（SPI操作）（MSTR=0，SPMS=0）	RSPCKn	Input	Input
	SSLn0	Input	Input
	SSLn1 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
主模式（时钟同步操作）（MSTR=1，MODFEN=0，SPMS=1）	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input

Table 30.7 Relationship between pin states and bit settings (2 of 2)

Mode	Pin	Pin state*2	
		PmnPFS.NCODR bit for I/O ports = 0	PmnPFS.NCODR bit for I/O ports = 1
Slave mode (clock synchronous operation) (MSTR = 0, SPMS = 1)	RSPCKn	Input	Input
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn	CMOS output	Open-drain output

Note 1. This function is not supported in this mode.
Note 2. SPI settings are not reflected in multiplexed pins for which the SPI function is not selected.
Note 3. Motorola-SPI: When SSLn0 is at the active level, the pin state is Hi-Z. Whether or not the input signal is at the active level determines the setting of the SPCR3.SSL0P bit.
TI-SSP: From when SSL0 is at the active level until communication is completed, the pin state is Hi-Z under the condition SPCR.SPE = 1.
Note 4. Motorola-SPI: When SSLn0 is at the non-active level or the SPCR.SPE bit is 0, the pin state is Hi-Z. Whether or not the input signal is at the active level determines the setting of the SPCR3.SSL0P bit.
TI-SSP: When SSL0 is except the communication period or when the SPE bit of SPCR is 0 (assertion after SPE = 1 and communication is completed), the pin status changes to Hi-Z.
Note 5. These pins are available for use as I/O port pins.

The SPI in single-master mode (SPI operation) or multi-master mode (SPI operation) determines the MOSI signal values during the SSL negation period (including the SSL retention period during a burst transfer) based on the MOIFE and MOIFV bit settings in SPCR2, as listed in Table 30.8.

Table 30.8 MOSI signal value determination during SSL negation

MOIFE bit	MOIFV bit	MOSIn signal value during SSL negation
0	0, 1	Final data from previous transfer
1	0	Low
1	1	High

30.3.3 SPI System Configuration Examples

This configuration example describes that 0 level of SSL0n signals is active level.

When connecting and using in a multi-slave or multi-master mode, the transfer format of the connected device should be unified to either Motorola-SPI or TI-SSP.

30.3.3.1 Single-master/single-slave with the MCU as a master

Figure 30.6 shows a single-master/single-slave SPI system configuration example where the MCU is used as a master. In the single-master/single-slave configuration, the SSLni outputs of the MCU (master) are not used. The SSL input of the SPI slave is fixed to the low level, and the SPI slave is maintained in the selected state.*1

Note 1. In the transfer format configured when the SPCMDm.CPHA bit is 0, the SSL signal for some slave devices cannot be fixed to an active level. In this case, always connect the SSLni output of the MCU to the SSL input of the slave device.

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signal.

Table 30.7 引脚状态和位设置之间的关系(2of2)

Mode	Pin	引脚状态*2	
		IO端口的PmnPFS.NCODR位=0	IO端口的PmnPFS.NCODR位=1
从机模式（时钟同步操作）（ MSTR=0，SPMS=1）	RSPCKn	Input	Input
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn	CMOS output	Open-drain output

注1.此模式不支持此功能。
注2.SPI设置不反映在未选择SPI功能的复用引脚中。
注3.Motorola-SPI：当SSLn0处于有效电平时，引脚状态为Hi-Z。输入信号是否处于有效电平决定了SPCR3.SSL0P位的设置。TI-SSP：从SSL0处于活动电平到通信完成，引脚状态为Hi-Z条件

SPCR.SPE = 1.
注4.Motorola-SPI：当SSLn0为无效电平或SPCR.SPE位为0时，引脚状态为Hi-Z。输入信号是否处于有效电平决定了SPCR3.SSL0P位的设置。TI-SSP：当SSL0在通信周期之外或SPCR的SPE位为0时（SPE=1后断言，通信完成），引脚状态变为Hi-Z。

注5.这些引脚可用作IO端口引脚。

单主机模式（SPI操作）或多主机模式（SPI操作）下的SPI根据中的MOIFE和MOIFV位设置确定SSL否定期间（包括突发传输期间的SSL保留期间）的MOSI信号值SPCR2，如表30.8中所列。

Table 30.8 SSL否定期间的MOSI信号值确定

MOIFE bit	MOIFV bit	SSL否定期间的MOSIn信号值
0	0, 1	上次传输的最终数据
1	0	Low
1	1	High

30.3.3 SPI系统配置示例

此配置示例描述了SSL0n信号的0电平为活动电平。

在多从机或多主机模式下连接使用时，连接设备的传输格式应统一为Motorola-SPI或TI-SSP。

30.3.3.1 单主单从单片机为主

图30.6显示了单主单从SPI系统配置示例，其中MCU用作主机。在单主单从配置中，不使用MCU（主）的SSLni输出。SPI从机的SSL输入固定为低电平，SPI从机保持在选中状态。*1

注1.在SPCMDm.CPHA位为0时配置的传输格式中，某些从设备的SSL信号不能固定为有效电平。在这种情况下，请始终将MCU的SSLni输出连接到从设备的SSL输入。

MCU（主控）驱动RSPCKn和MOSIn信号。SPI从机驱动MISO信号。

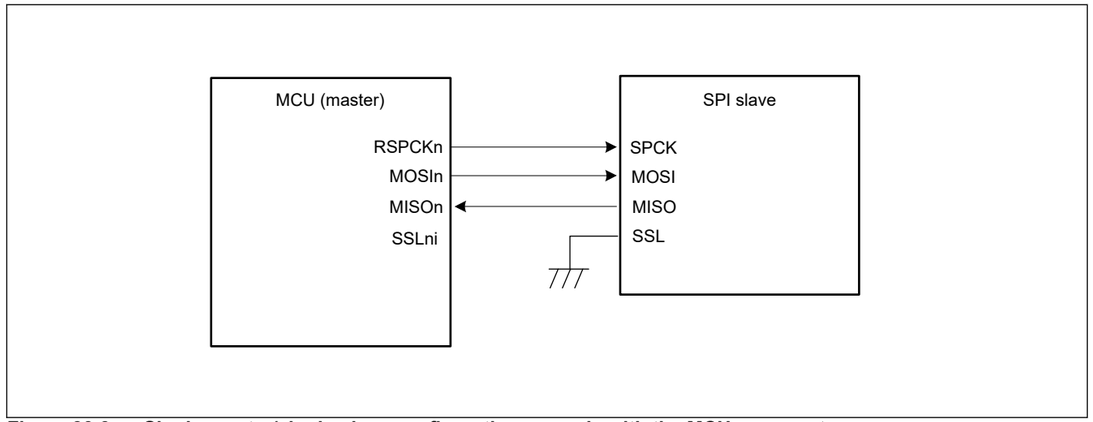


Figure 30.6 Single-master/single-slave configuration example with the MCU as a master

30.3.3.2 Single-master/single-slave with the MCU as a slave

Figure 30.7 shows a single-master/single-slave SPI system configuration example where the MCU is used as a slave. When the MCU operates as a slave, the SSLn0 pin is used as SSL input. The SPI master drives the RSPCK and MOSI signals. The MCU (slave) drives the MISOn signal.*1

Note 1. When SSLn0 is at a non-active level, the pin state is Hi-Z.

In the single-slave configuration when the SPCMDm.CPHA bit is set to 1, the SPCR.SPFRF bit is set to 0, and SPCR.SPMS is set to 0, the SSLn0 input of the MCU (slave) is fixed to the low level and the MCU (slave) is maintained in the selected state. This enables serial transfer execution (Figure 30.8). However, the communication end interrupt does not output when SSL0 input is fixed as Figure 30.8.

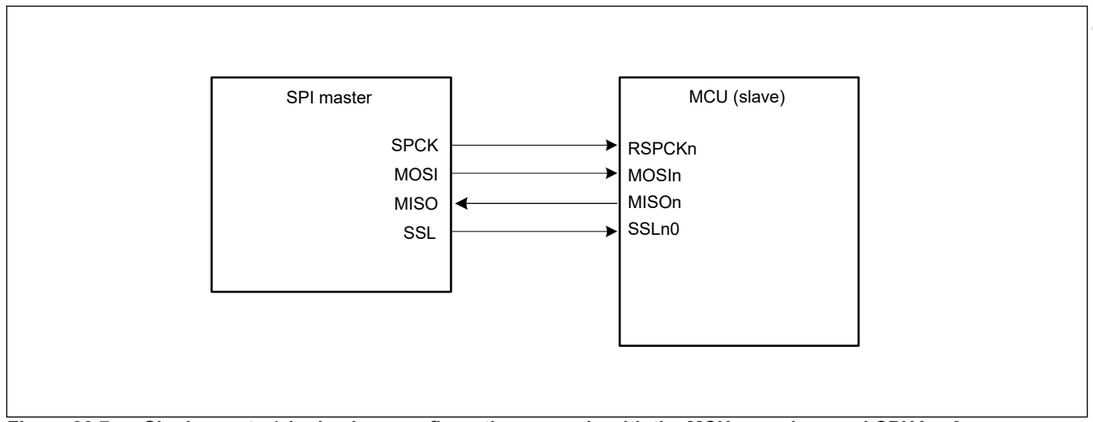


Figure 30.7 Single-master/single-slave configuration example with the MCU as a slave and CPHA = 0

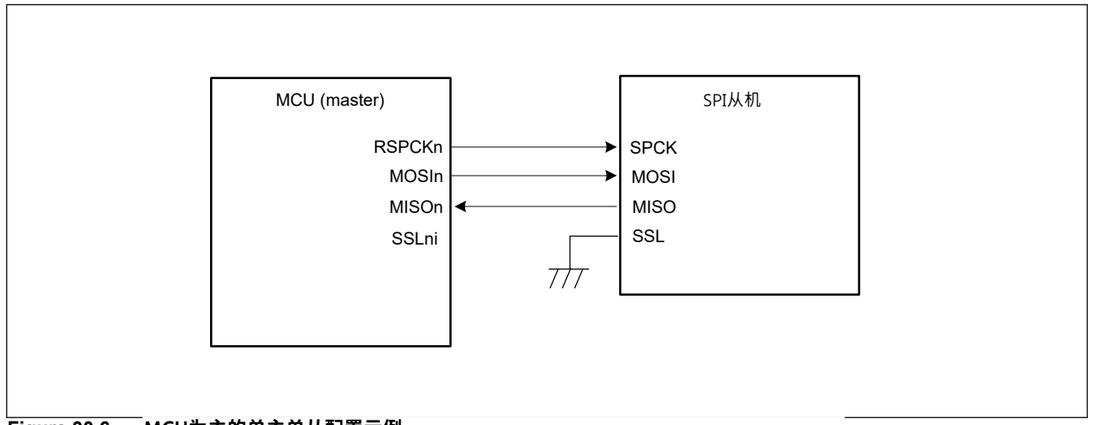


Figure 30.6 MCU为主的单主单从配置示例

30.3.3.2 单主单从单片机作为从机

图30.7显示了单主单从SPI系统配置示例，其中MCU用作从机。当MCU作为从机运行时，SSLn0引脚用作SSL输入。SPI主机驱动RSPCK和MOSI信号。MCU（从机）驱动MIOn信号。*1

注1.当SSLn0处于非活动电平时，引脚状态为Hi-Z。

在单从配置中，当SPCMDm.CPHA位设置为1时，SPCR.SPFRF位设置为0，并且SPCR.SPMS设置为0，MCU（从机）的SSLn0输入固定为低电平，MCU（从机）保持在选择状态。这将启用串行传输执行（图30.8）。但是，如图30.8那样固定SSL0输入时，不输出通信结束中断。

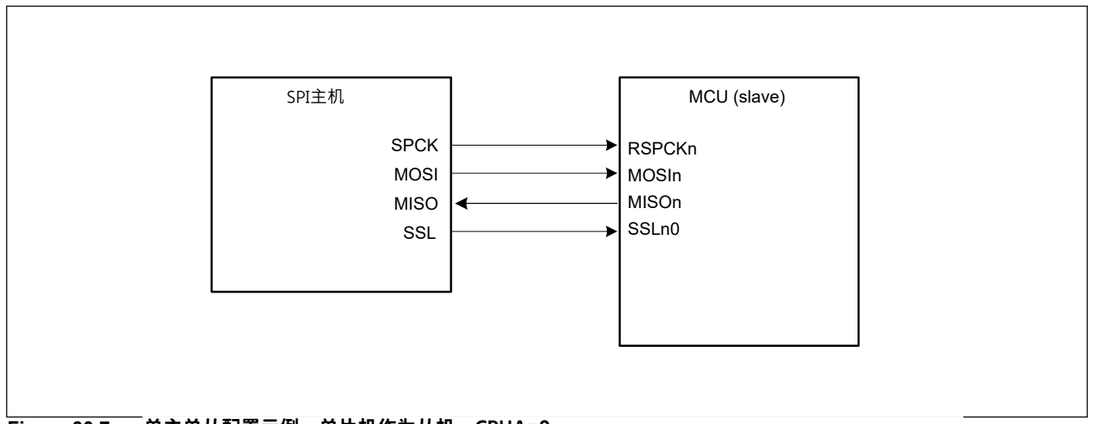


Figure 30.7 单主单从配置示例，单片机作为从机，CPHA=0

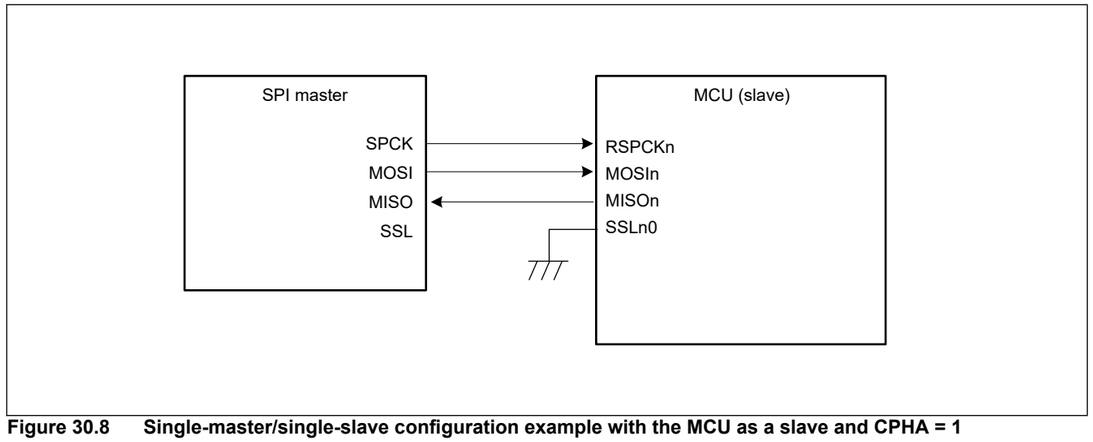


Figure 30.8 Single-master/single-slave configuration example with the MCU as a slave and CPHA = 1

30.3.3.3 Single-master/multi-slave with the MCU as a master

Figure 30.9 shows a single-master/multi-slave SPI system configuration example where the MCU is used as a master. In this example, the SPI system includes the MCU (master) and four slaves (SPI slave 0 to SPI slave 3).

The RSPCKn and MOSIn outputs of the MCU (master) are connected to the RSPCK and MOSI inputs of SPI slaves 0 to 3. The MISO outputs of SPI slaves 0 to 3 are all connected to the MISOn input of the MCU (master). The SSLn0 to SSLn3 outputs of the MCU (master) are connected to the SSL inputs of SPI slaves 0 to 3, respectively.

The MCU (master) drives the RSPCKn, MOSIn, and SSLn0 to SSLn3 signals. Of the SPI slaves 0 to 3, the slave that receives low-level input into the SSL input drives the MISO signal.

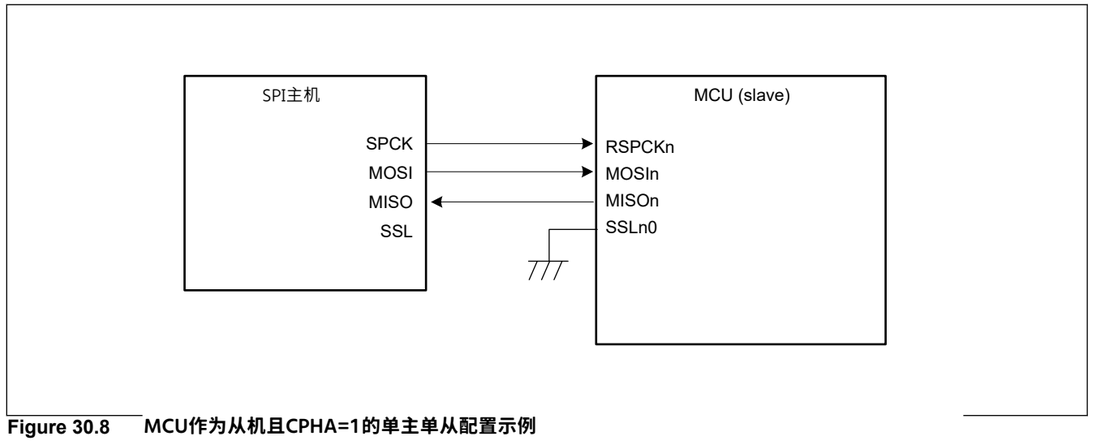


Figure 30.8 MCU作为从机且CPHA=1的单主单从配置示例

30.3.3.3 单主多从，单片机为主

图30.9显示了单主多从SPI系统配置示例，其中MCU用作主控。在本例中，SPI系统包括MCU（主机）和四个从机（SPI从机0到SPI从机3）。

MCU（主机）的RSPCKn和MOSIn输出连接到SPI从机0到3的RSPCK和MOSI输入。
SPI从机0到3的MISO输出都连接到MCU（主机）的MISOn输入。MCU（主机）的SSLn0到SSLn3输出分别连接到SPI从机0到3的SSL输入。

MCU（主控）驱动RSPCKn、MOSIn和SSLn0到SSLn3信号。在SPI从机0到3中，接收到SSL输入的低电平输入的从机驱动MISO信号。

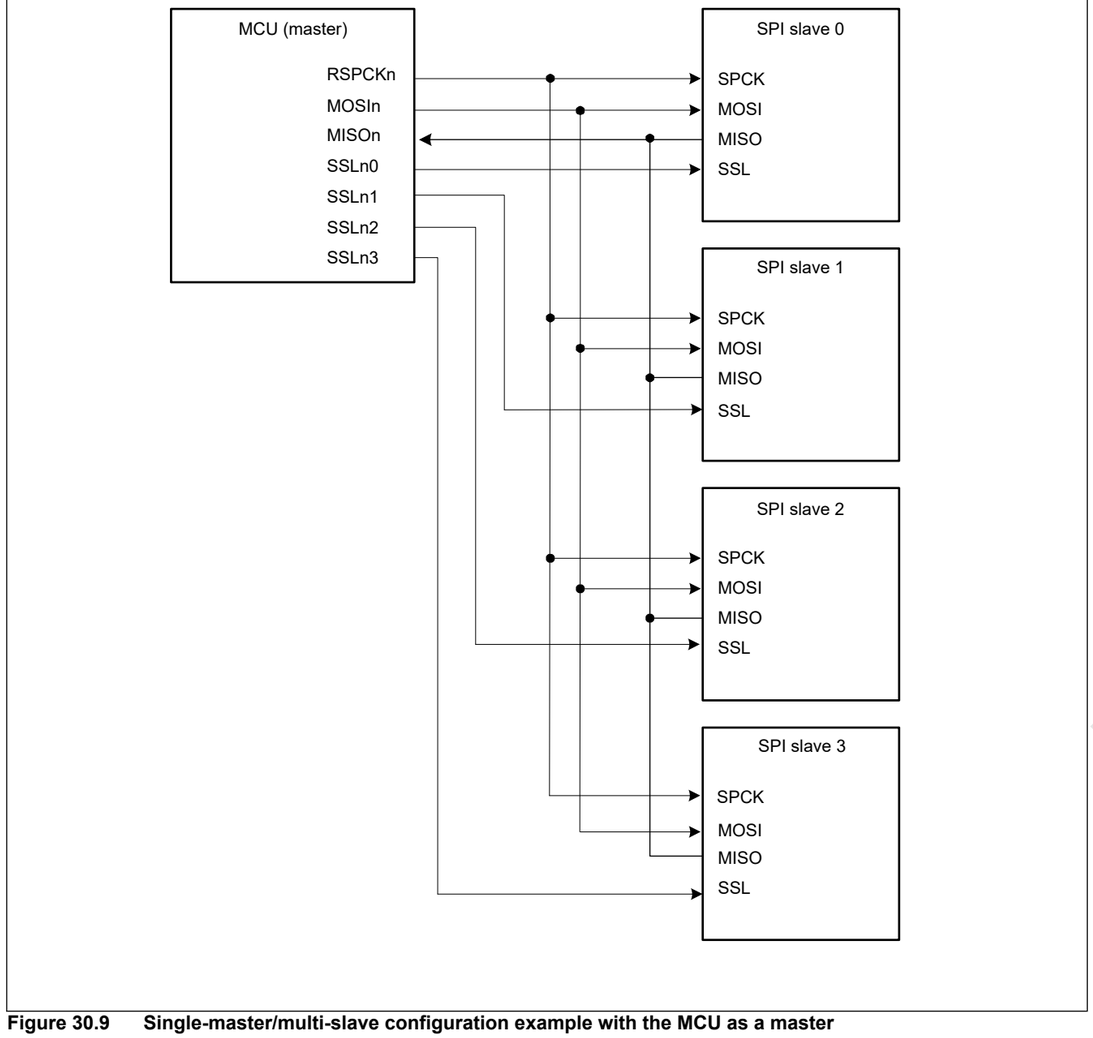


Figure 30.9 Single-master/multi-slave configuration example with the MCU as a master

30.3.3.4 Single-master/multi-slave with the MCU as a slave

Figure 30.10 shows a single-master/multi-slave SPI system configuration example where the MCU is used as a slave. In this example, the SPI system includes an SPI master and two MCUs (slaves X and Y).

The SPCK and MOSI outputs of the SPI master are connected to the RSPCKn and MOSIn inputs of the MCUs (slaves X and Y). The MISOn outputs of the MCUs (slaves X and Y) are all connected to the MISO input of the SPI master. The SSLX and SSLY outputs of the SPI master are connected to the SSLn0 inputs of the MCUs (slaves X and Y, respectively).

The SPI master drives the SPCK, MOSI, SSLX, and SSLY signals. Of the MCUs (slaves X and Y), the slave that receives low-level input into the SSLn0 input drives the MISOn signal.

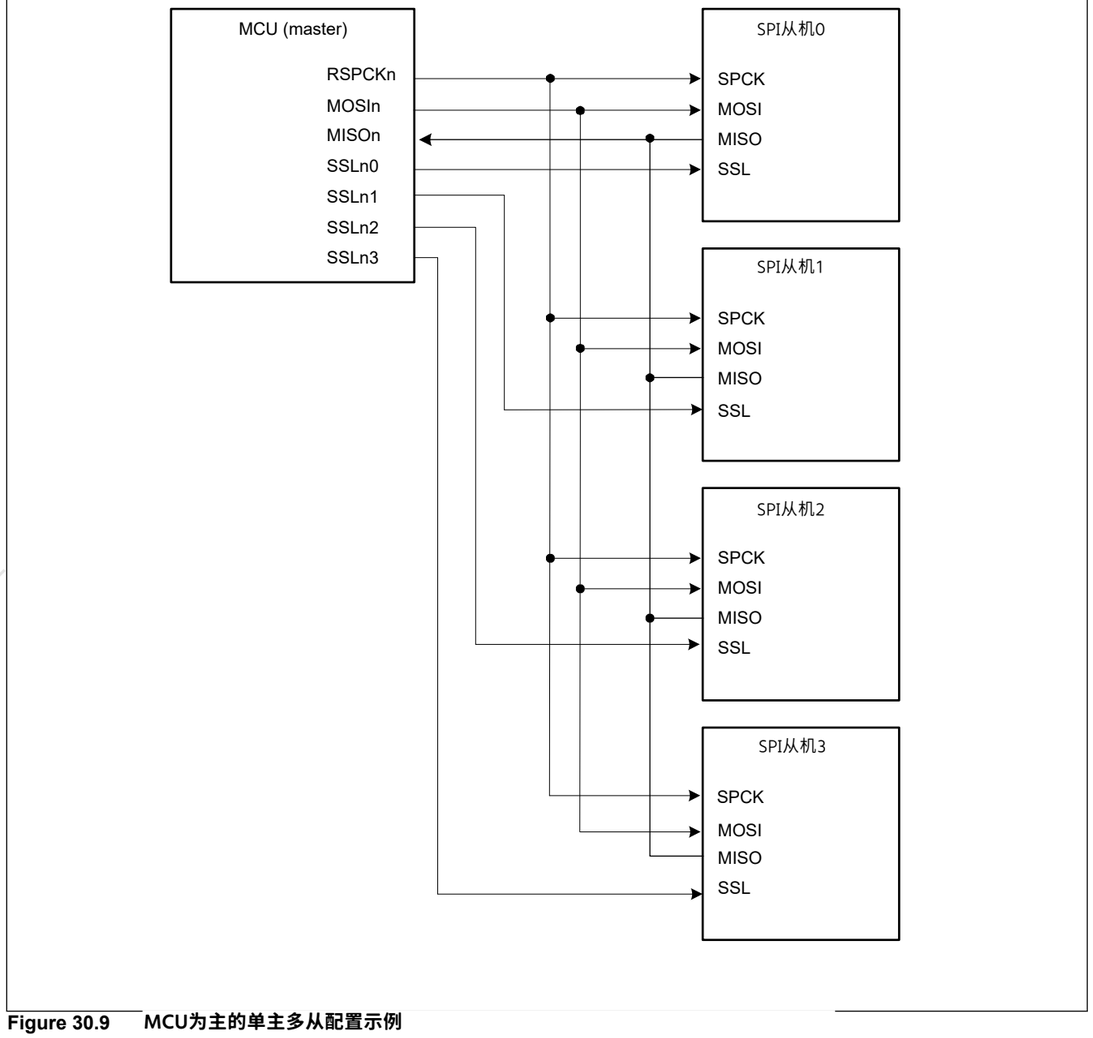


Figure 30.9 MCU为主的单主多从配置示例

30.3.3.4 单主多从，单片机作为从机

图30.10显示了单主多从SPI系统配置示例，其中MCU用作从设备。在本例中，SPI系统包括一个SPI主控和两个MCU（从属X和Y）。

SPI主机的SPCK和MOSI输出连接到MCU（从机X和Y）的RSPCKn和MOSIn输入。MCU（从机X和Y）的MISOn输出都连接到SPI主机的MISO输入。SPI主机的SSLX和SSLY输出连接到MCU的SSLn0输入（分别为从机X和Y）。

SPI主机驱动SPCK、MOSI、SSLX和SSLY信号。在MCU（从机X和Y）中，接收到SSLn0输入的低电平输入的从机驱动MISOn信号。

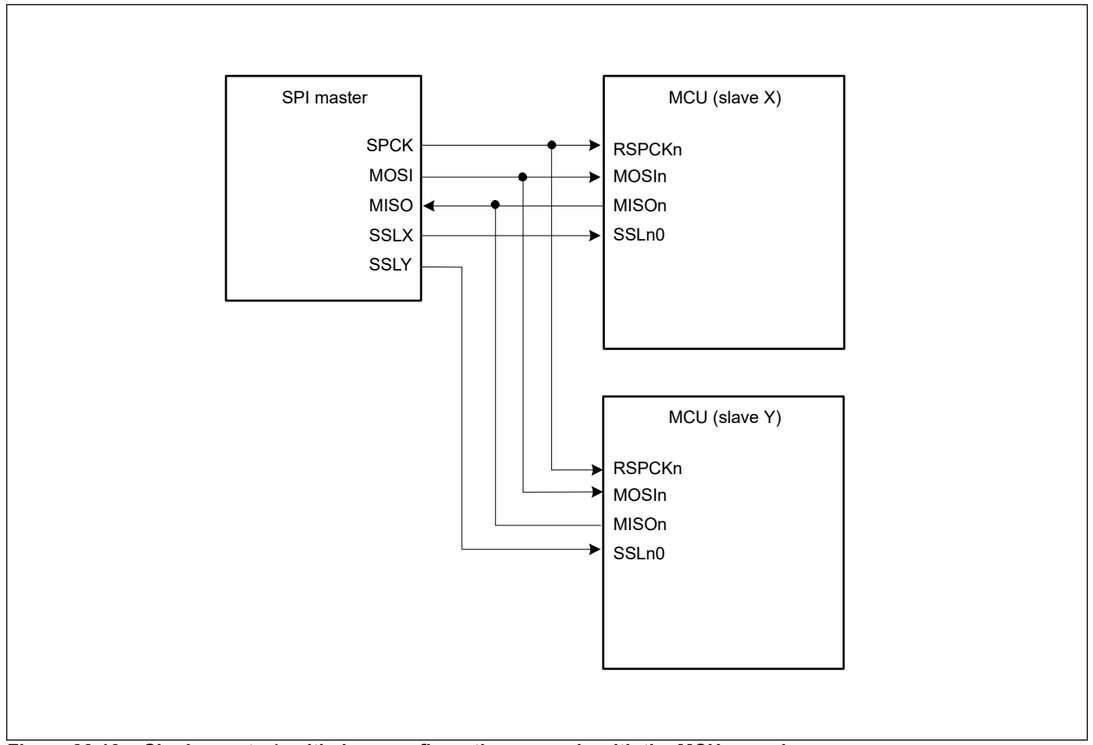


Figure 30.10 Single-master/multi-slave configuration example with the MCU as a slave

30.3.3.5 Multi-master/multi-slave with the MCU as a master

Figure 30.11 shows a multi-master/multi-slave SPI system configuration example where the MCU is used as a master. In this example, the SPI system includes two MCUs (masters X and Y) and two SPI slaves (SPI slaves 1 and 2).

The RSPCKn and MOSIn outputs of the MCUs (masters X and Y) are connected to the RSPCK and MOSI inputs of SPI slaves 1 and 2. The MISO outputs of SPI slaves 1 and 2 are connected to the MISOn inputs of the MCUs (masters X and Y). Any generic port Y output from the MCU (master X) is connected to the SSLn0 input of the MCU (master Y). Any generic port X output of the MCU (master Y) is connected to the SSLn0 input of the MCU (master X). The SSLn1 and SSLn2 outputs of the MCUs (masters X and Y) are connected to the SSL inputs of the SPI slaves 1 and 2. In this configuration example, because the system can be comprised solely of SSLn0 input, and SSLn1 and SSLn2 outputs for slave connections, the SSLn3 output of the MCU is not required.

The MCU drives the RSPCKn, MOSIn, SSLn1, and SSLn2 signals when the SSLn0 input level is high. When the SSLn0 input level is low, the MCU detects a mode fault error, sets RSPCKn, MOSIn, SSLn1, and SSLn2 to Hi-Z, and releases the SPI bus directly to the other master. Of the SPI slaves 1 and 2, the slave that receives low-level input into the SSL input drives the MISO signal.

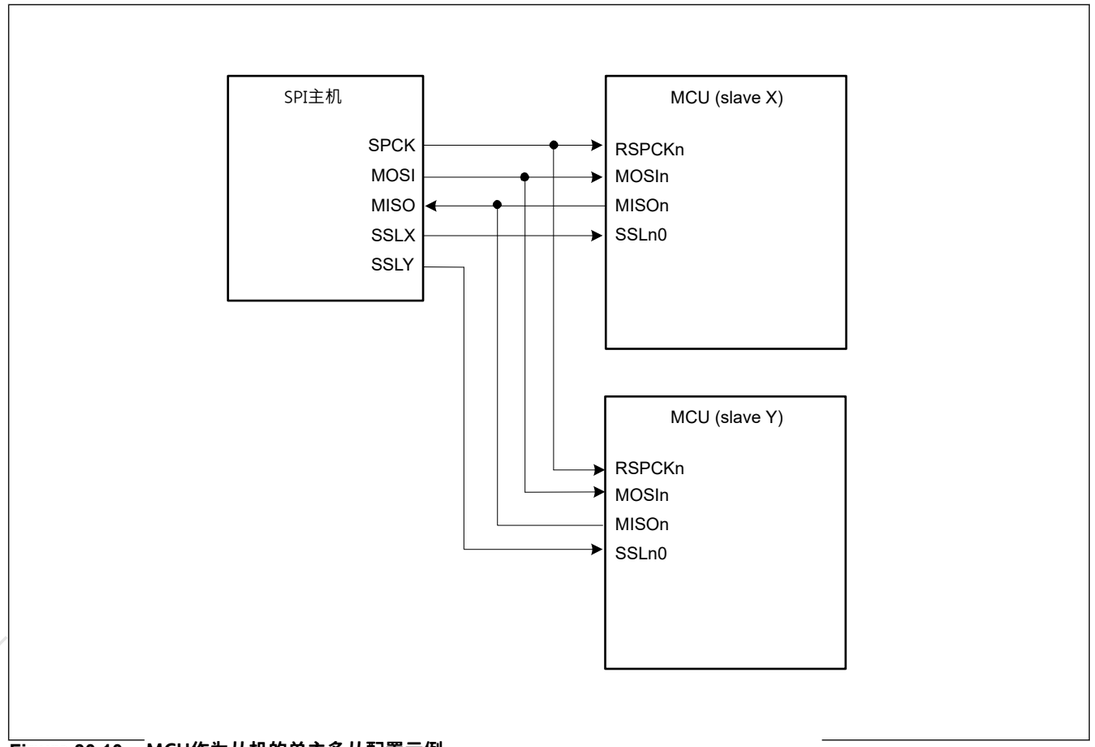


Figure 30.10 MCU作为从机的单主多从配置示例

30.3.3.5 以单片机为主的多主多从

图30.11显示了一个多主机多从机SPI系统配置示例，其中MCU用作主机。在此示例中，SPI系统包括两个MCU（主X和Y）和两个SPI从机（SPI从机1和2）。

MCU（主机X和Y）的RSPCKn和MOSIn输出连接到SPI从机1和2的RSPCK和MOSI输入。SPI从机1和2的MISO输出连接到MCU（主机X）的MISOn输入和Y)。来自MCU（主X）的任何通用端口Y输出都连接到MCU（主Y）的SSLn0输入。MCU（主设备Y）的任何通用端口X输出都连接到MCU（主设备X）的SSLn0输入。MCU（主机X和Y）的SSLn1和SSLn2输出连接到SPI从机1和2的SSL输入。在此配置示例中，因为系统可以仅由SSLn0输入和SSLn1和SSLn2输出组成从连接，不需要MCU的SSLn3输出。

当SSLn0输入电平为高电平时，MCU驱动RSPCKn、MOSIn、SSLn1和SSLn2信号。当SSLn0输入电平为低时，MCU检测到模式故障错误，将RSPCKn、MOSIn、SSLn1和SSLn2设置为Hi-Z，并将SPI总线直接释放到另一个主控。在SPI从机1和2中，接收到SSL输入的低电平输入的从机驱动MISO信号。

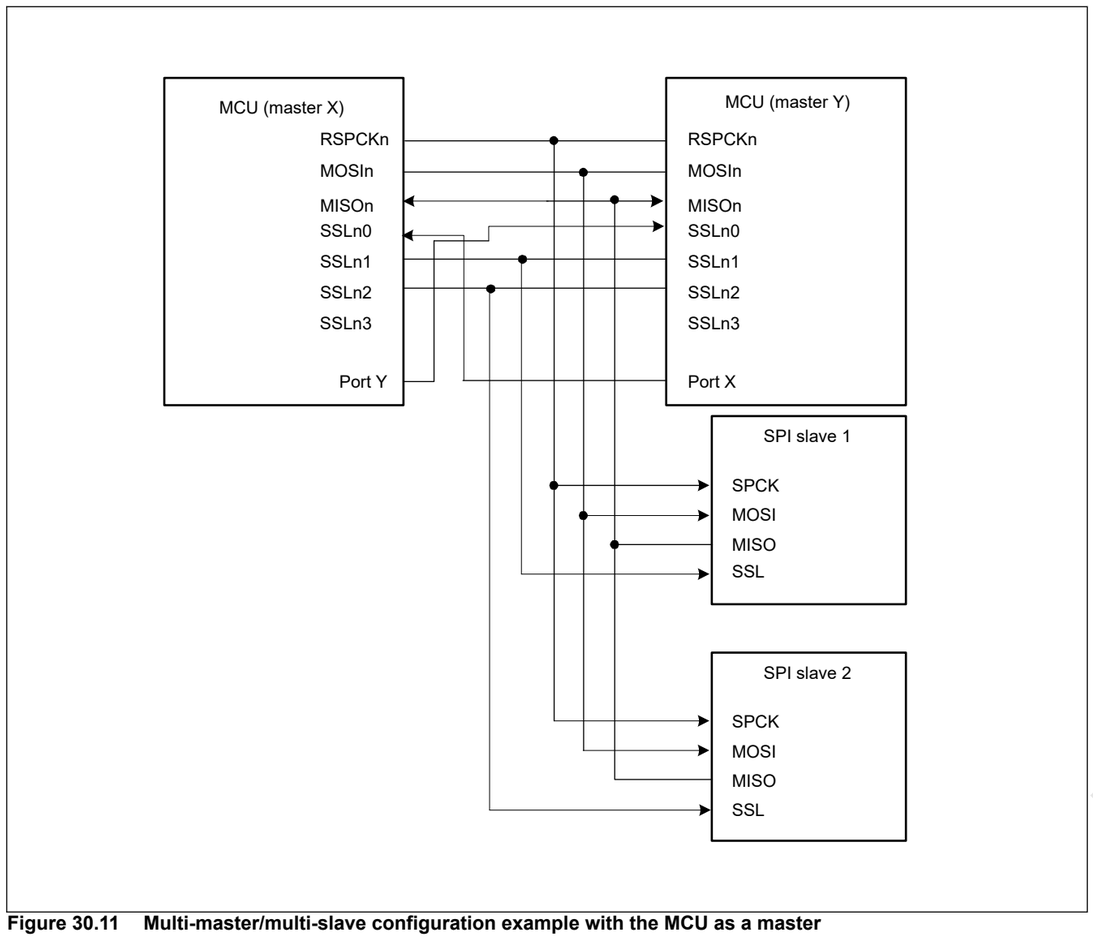


Figure 30.11 Multi-master/multi-slave configuration example with the MCU as a master

When setting TI SSP, enter the following levels for port X and port Y.

- Start of communication: the value of SPCR3.SSL0P of the other master.
- End of communication: the inverted value of SPCR3.SSL0P of the other master.

30.3.3.6 Master and slave in clock synchronous mode with the MCU configured as a master

Figure 30.12 shows a master and slave in clock synchronous mode configuration example where the MCU is used as a master. In this configuration, SSLni of the MCU (master) are not used.

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signal.

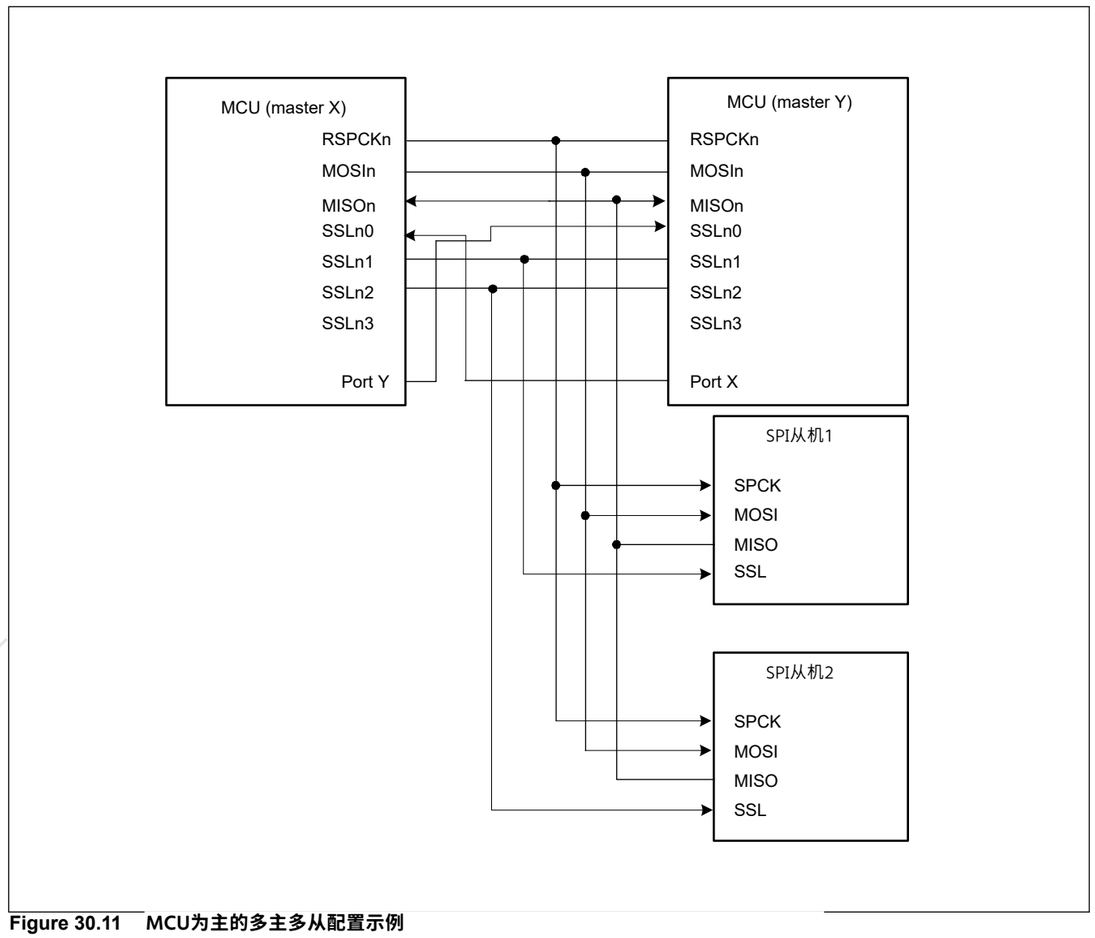


Figure 30.11 MCU为主的多主多从配置示例

设置TISSP时，为端口X和端口Y输入以下级别。

- ●通信开始：其他主站的SPCR3.SSL0P的值。
- ●通信结束：对方主站SPCR3.SSL0P的取反值。

30.3.3.6 主从时钟同步模式，MCU配置为主

图30.12显示了时钟同步模式下的主机和从机配置示例，其中MCU用作主机。在此配置中，不使用MCU（主）的SSLni。

MCU（主控）驱动RSPCKn和MOSIn信号。SPI从机驱动MISO信号。

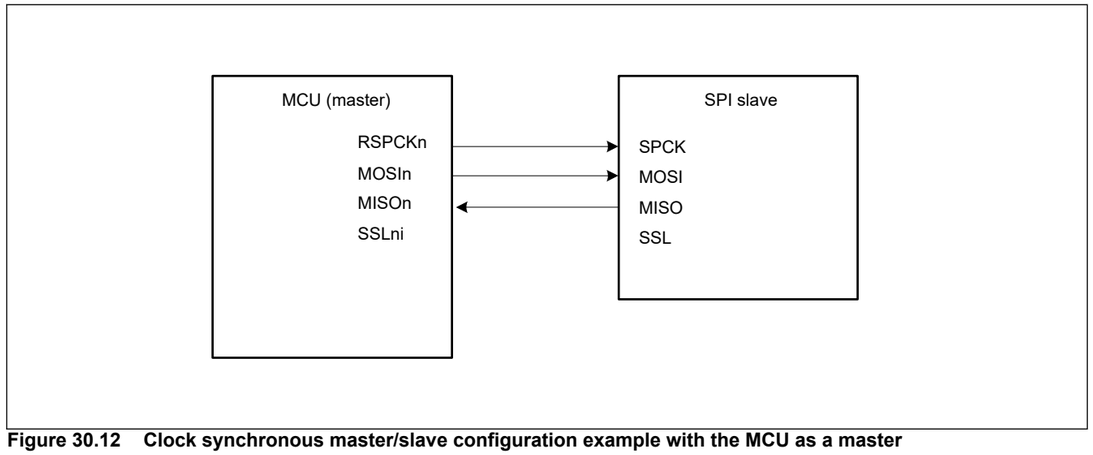


Figure 30.12 Clock synchronous master/slave configuration example with the MCU as a master

30.3.3.7 Master and slave in clock synchronous mode with the MCU as a slave

Figure 30.13 shows a master and slave in clock synchronous mode configuration example where the MCU is used as a slave. When the MCU operates as a slave (clock synchronous operation), the MCU (slave) drives the MISOn signal and the SPI master drives the SPCK and MOSI signals. In addition, SSLn0 to SSLn3 of the MCU (slave) are not used.

The MCU (slave) can only execute serial transfers in the single-slave configuration when the SPCMDm.CPHA bit is set to 1.

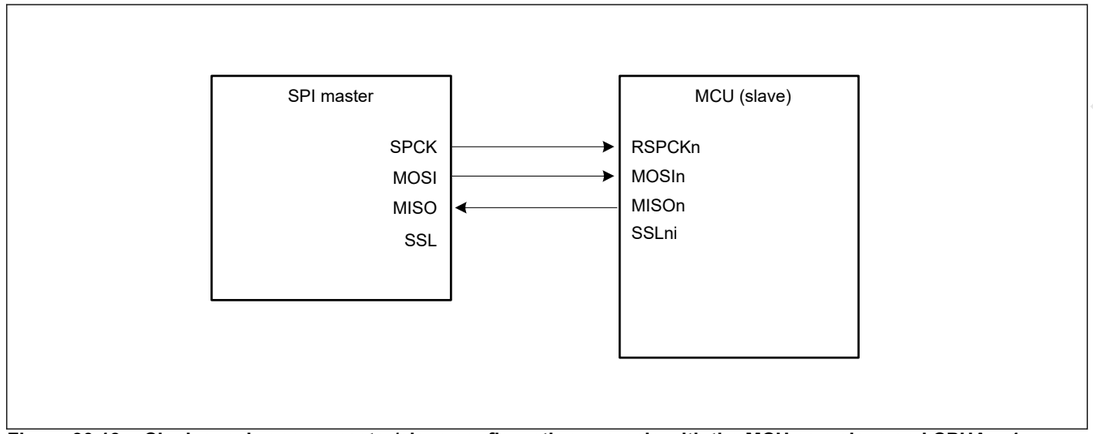


Figure 30.13 Clock synchronous master/slave configuration example with the MCU as a slave and CPHA = 1

30.3.4 Data Formats

The data format of the SPI depends on the settings in SPI Command Register m (SPCMDm) and the parity enable bit in SPI Control Register (SPCR.SPPE). Regardless of whether the MSB or LSB is first, the SPI treats the range from the LSB bit in the SPI Data Register (SPDR) to the bit associated with the selected data length, as transfer data.

This section shows the format of one frame of data before or after transfer.

Data format with parity disabled

When parity is disabled, transmission or reception of data proceeds with the length in bits selected in the SPI data length setting in SPI Command Register m (SPCMDm.SPB[4:0]).

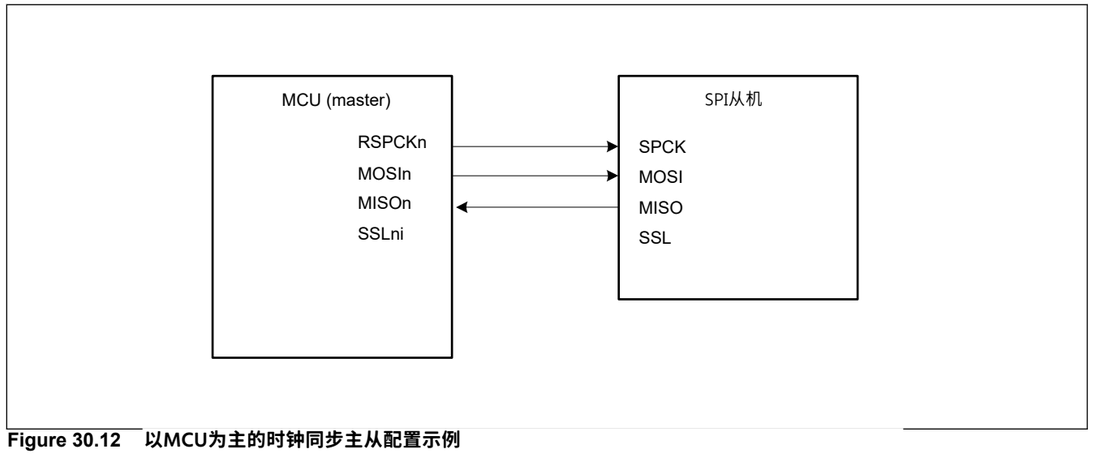


Figure 30.12 以MCU为主的时钟同步主从配置示例

30.3.3.7 主从时钟同步模式，单片机作为从机

图30.13显示了时钟同步模式下的主机和从机配置示例，其中MCU用作从机。当MCU作为从机运行时（时钟同步操作），MCU（从机）驱动MIOn信号，SPI主机驱动SPCK和MOSI信号。此外，不使用MCU（从机）的SSLn0到SSLn3。

当SPCMDm.CPHA位设置为1时，MCU（从机）只能在单从机配置中执行串行传输。

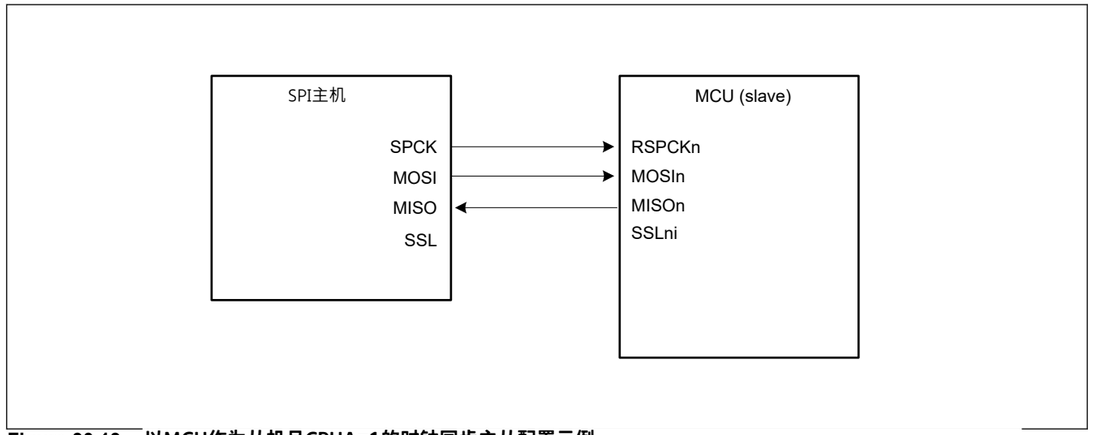


Figure 30.13 以MCU作为从机且CPHA=1的时钟同步主从配置示例

30.3.4 数据格式

SPI的数据格式取决于SPI命令寄存器m(SPCMDm)中的设置和SPI控制寄存器(SPCR.SPPE)中的奇偶校验使能位。无论是MSB还是LSB在前，SPI都会将SPI数据寄存器(SPDR)中的LSB位到与所选数据长度相关的位的范围视为传输数据。

本节显示传输前后一帧数据的格式。

禁用奇偶校验的数据格式

当奇偶校验被禁用时，数据的发送或接收将按照在SPI命令寄存器m(SPCMDm.SPB[4:0])的SPI数据长度设置中选择的位长度进行。

Data format with parity enabled

When parity is enabled, transmission or reception of data proceeds with the length in bits selected in the SPI data length setting in SPI Command Register m (SPCMDm.SPB[4:0]). In this case, however, the last bit is a parity bit.

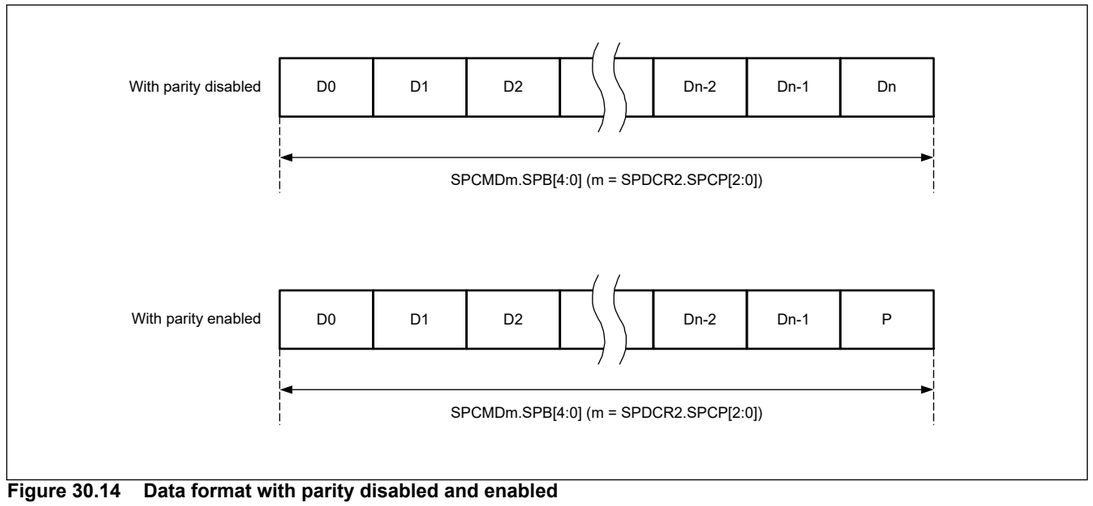


Figure 30.14 Data format with parity disabled and enabled

30.3.4.1 Operation when parity is disabled (SPCR.SPPE = 0)

When parity is disabled, data for transmission is copied to the shift register with no pre-processing. This section describes the connection between the SPI Data Register (SPDR) and the shift register in terms of the combination of MSB- or LSB-first order and data length.

(1) MSB-first transfer with 32-bit data

Figure 30.15 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, a SPI data length of 32 bits, and MSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register from T31 to T30, and continuing to T00.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R31 to R00 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

启用奇偶校验的数据格式

启用奇偶校验时，数据的发送或接收将按照在SPI命令寄存器m(SPCMDm.SPB[4:0])的SPI数据长度设置中选择的位长度进行。然而，在这种情况下，最后一位是奇偶校验位。

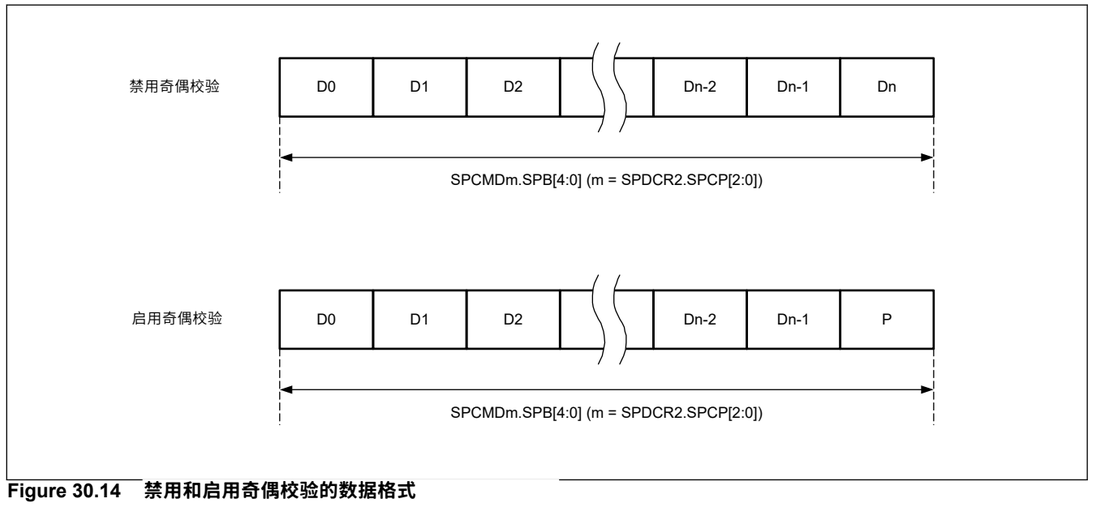


Figure 30.14 禁用和启用奇偶校验的数据格式

30.3.4.1 禁用奇偶校验时的操作(SPCR.SPPE=0)

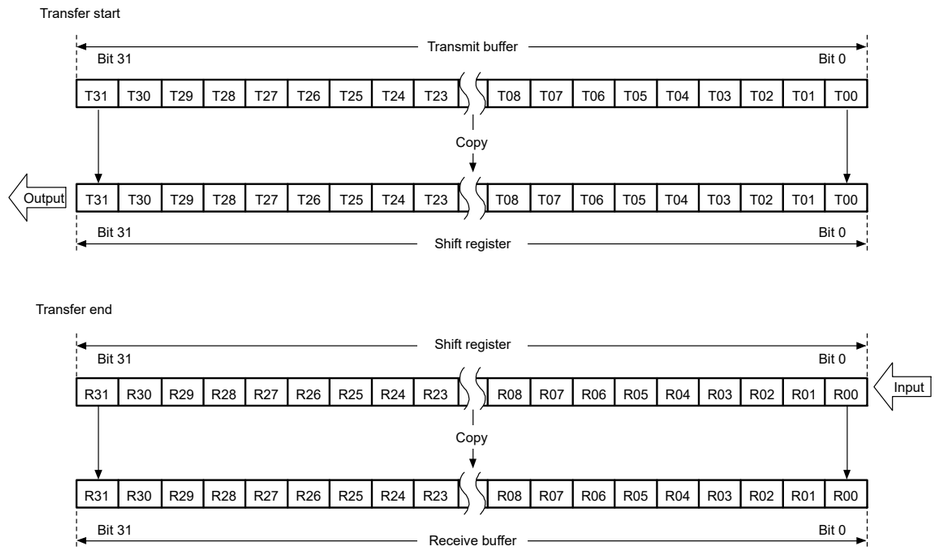
当奇偶校验被禁用时，用于传输的数据被复制到移位寄存器而不进行预处理。本节从MSB或LSBfirstorder和数据长度的组合来描述SPI数据寄存器(SPDR)和移位寄存器之间的连接。

(1) 32位数据的MSB优先传输

图30.15显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用的传输中的操作，a SPI数据长度为32位，且MSB优先选择。

在发送过程中，发送缓冲器当前级的T31到T00位被复制到移位寄存器。发送数据从移位寄存器从T31移出到T30，并继续到T00。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需的RSPCK周期数后收集R31至R00位时，将移位寄存器中的值复制到接收缓冲区。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

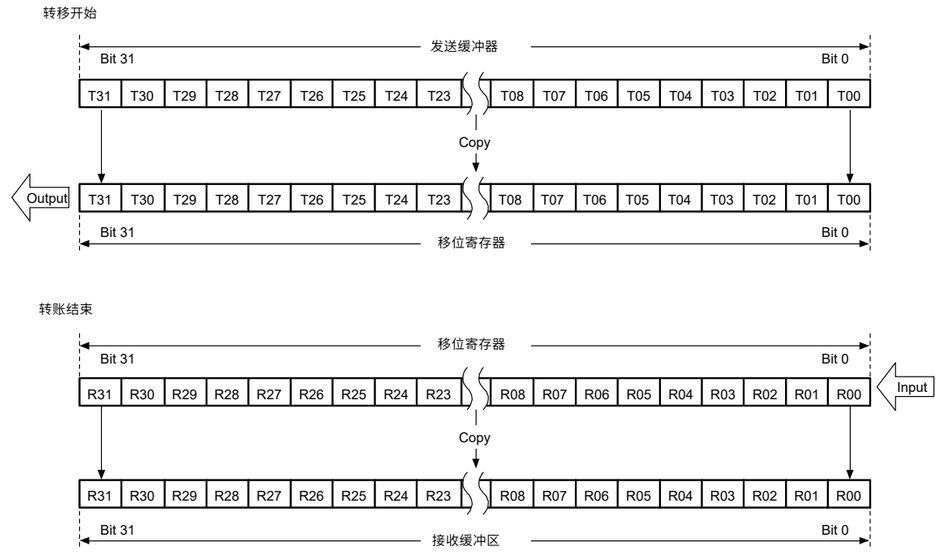
Figure 30.15 MSB-first transfer with 32-bit data and parity disabled

(2) MSB-first transfer with 24-bit data

Figure 30.16 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, an SPI data length of 24 bits for an example that is not 32 bits, and MSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register from T23 to T22, and continuing to T00.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R23 to R00 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

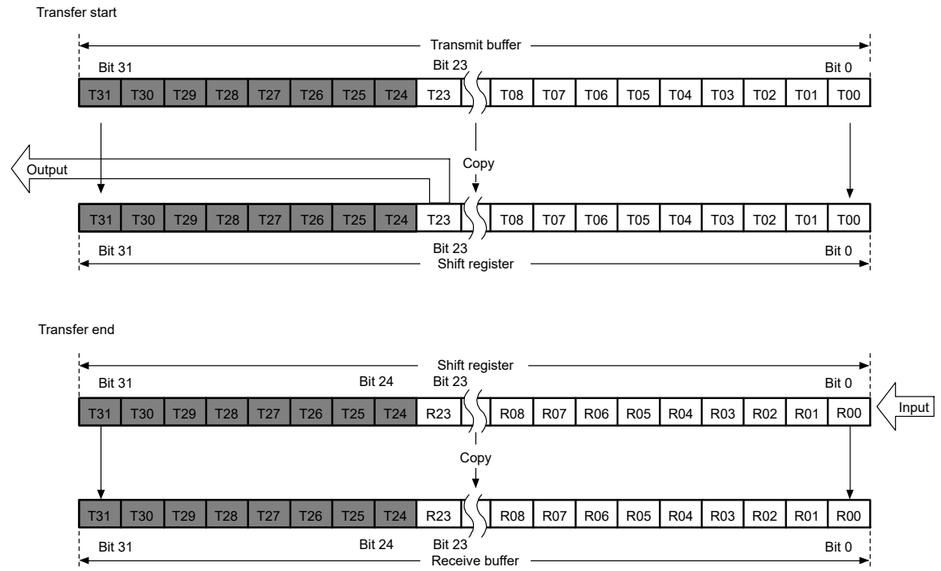
Figure 30.15 禁用32位数据和奇偶校验的MSB优先传输

(2) 24位数据的MSB优先传输

图30.16显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用的传输中的操作，
以24位SPI数据长度为例，即不是32位，并且选择MSB优先。

在发送过程中，来自发送缓冲器当前阶段的低24位（T23到T00）被复制到移位寄存器。
发送的数据从移位寄存器从T23移出到T22，并继续到T00。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需数量的RSPCK周期后，当R23到R00位被收集时，移位寄存器中的值被复制到接收缓冲区。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

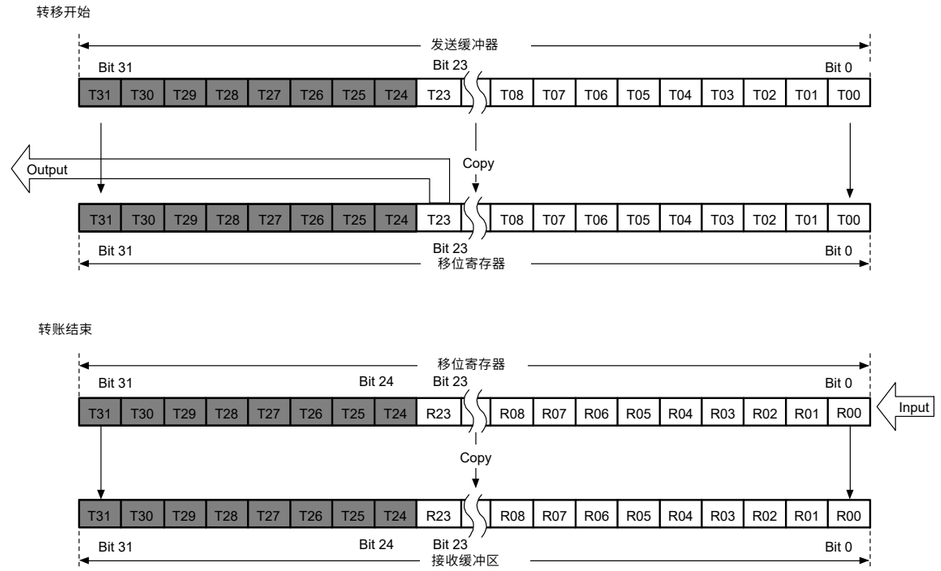
Figure 30.16 MSB-first transfer with 24-bit data and parity disabled

(3) LSB-first transfer with 32-bit data

Figure 30.17 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are reordered bit-by-bit to obtain the order T00 to T31 for copying to the shift register. Data for transmission is shifted out from the shift register in order from T00 to T01, and continuing to T31.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R00 to R31 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

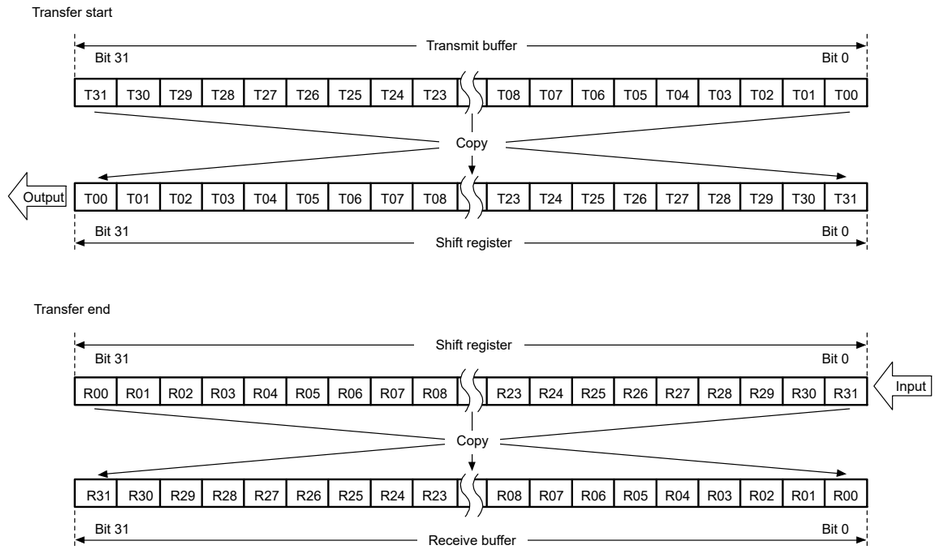
Figure 30.16 禁用24位数据和奇偶校验的MSB优先传输

(3) 32位数据的LSB优先传输

图30.17显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用的传输中的操作，
SPI数据长度为32位，并选择LSB-first。

在传输过程中，传输缓冲器当前级的位T31到T00被逐位重新排序，以获得用于复制到移位寄存器的顺序T00到T31。传输的数据从移位寄存器中按顺序从T00移出到T01，并继续到T31。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需数量的RSPCK周期后收集R00至R31位时，将移位寄存器中的值复制到接收缓冲区。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

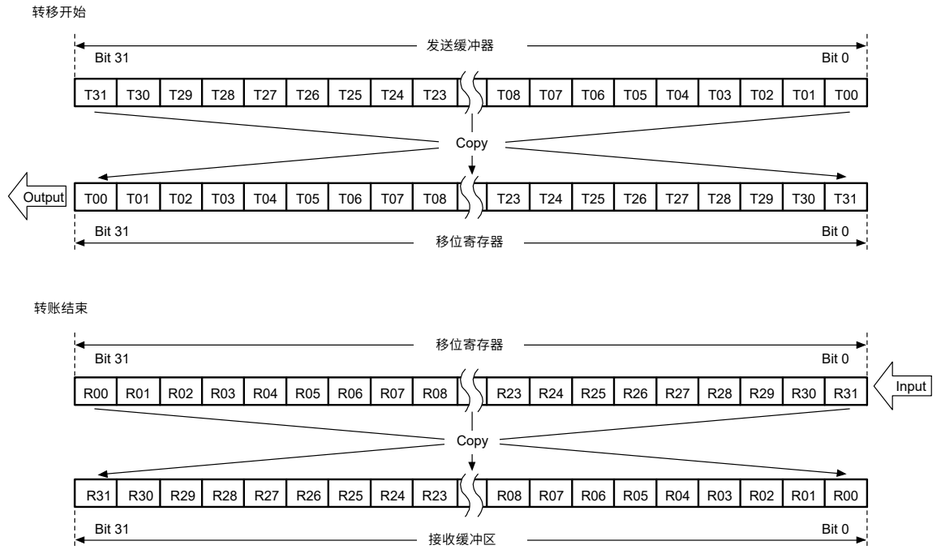
Figure 30.17 LSB-first transfer with 32-bit data and parity disabled

(4) LSB-first transfer with 24-bit data

Figure 30.18 shows the operation of the SPI Data Register (SPDR) and the shift register in transfers with parity disabled, an SPI data length of 24 bits for an example that is not 32, and LSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are reordered bit-by-bit to obtain the order T00 to T23 for copying to the shift register. Data for transmission is shifted out from the shift register from T00 to T01, and continuing to T23.

In reception, received data is shifted in bit-by-bit through bit[8] of the shift register. When the R00 to R23 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

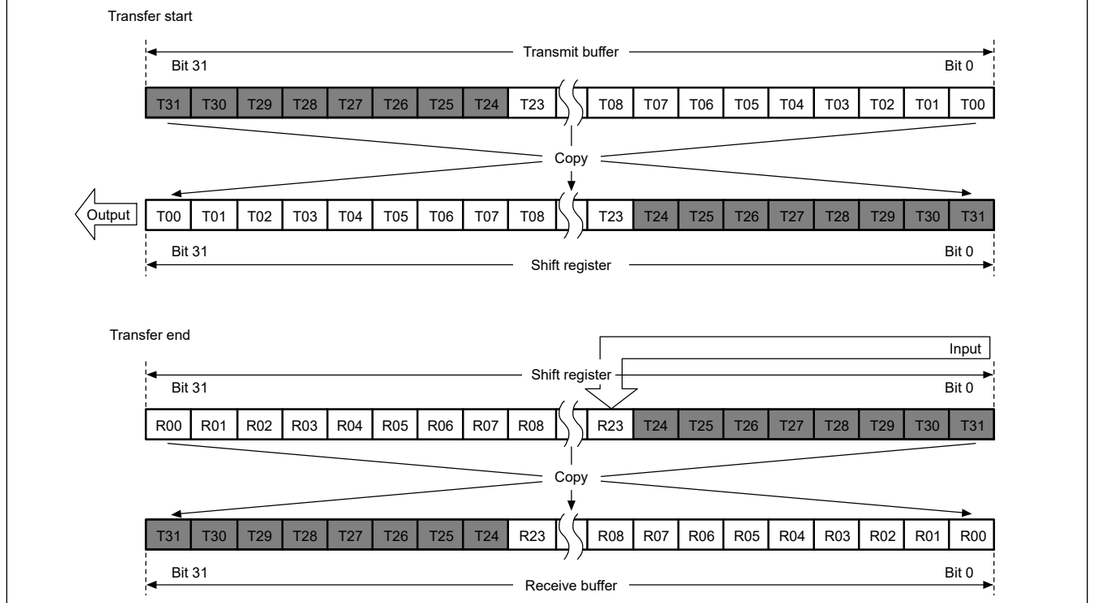
Figure 30.17 LSB优先传输，32位数据和奇偶校验禁用

(4) 24位数据的LSB优先传输

图30.18显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用的传输中的操作，一个SPI数据长度为24位，例如不是32位，并且选择LSB优先。

发送时，将发送缓冲器当前级的低24位（T23到T00）逐位重新排序，得到T00到T23的顺序，用于复制到移位寄存器。发送的数据从移位寄存器从T00移出到T01，并继续到T23。

在接收中，接收到的数据通过移位寄存器的bit[8]逐位移位。在输入所需的RSPCK周期数后收集R00至R23位时，将移位寄存器中的值复制到接收缓冲区。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 30.18 LSB-first transfer with 24-bit data and parity disabled

30.3.4.2 Operation when parity is enabled (SPCR.SPPE = 1)

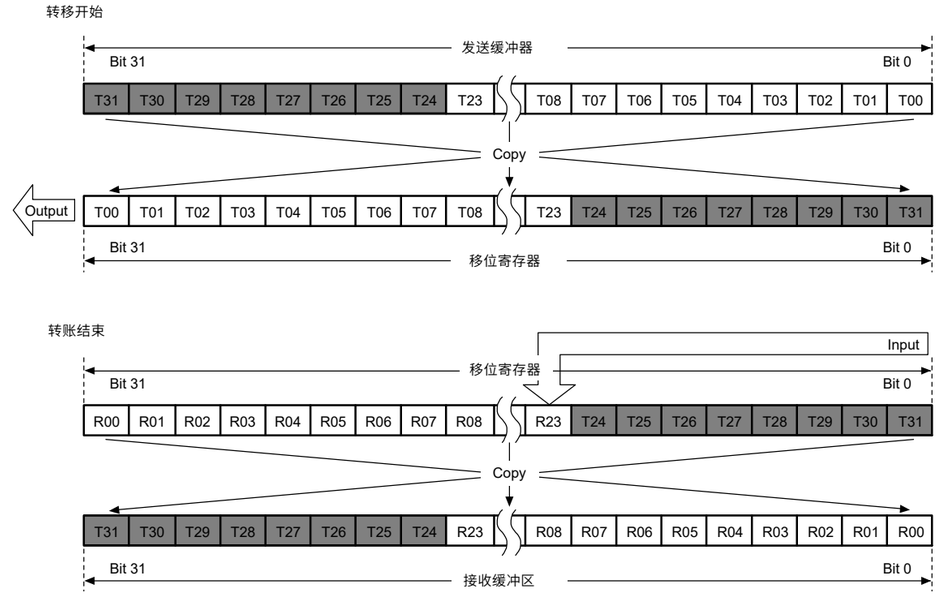
When parity is enabled, the lowest-order bit of the data for transmission becomes a parity bit. Hardware calculates the value of the parity bit.

(1) MSB-first transfer with 32-bit data

Figure 30.19 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, an SPI data length of 32 bits, and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T31 to T01. This replaces the final bit, T00, and the whole value is copied to the shift register. Data is transmitted in the order T31, T30, …, T01, and P.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R31 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R31 to P is checked for parity.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

Figure 30.18 LSB优先传输，24位数据和奇偶校验禁用

30.3.4.2 启用奇偶校验时的操作(SPCR.SPPE=1)

启用奇偶校验时，传输数据的最低位变为奇偶校验位。硬件计算奇偶校验位的值。

(1) 32位数据的MSB优先传输

图30.19显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，
SPI数据长度为32位，且MSB优先选择。

在传输中，奇偶校验位(P)的值是从位T31到T01计算的。这将替换最后一位T00，并将整个值复制到移位寄存器。数据按T31、T30、……、T01和P的顺序传输。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需数量的RSPCK周期后收集R31至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，会检查从R31到P的数据的奇偶性。

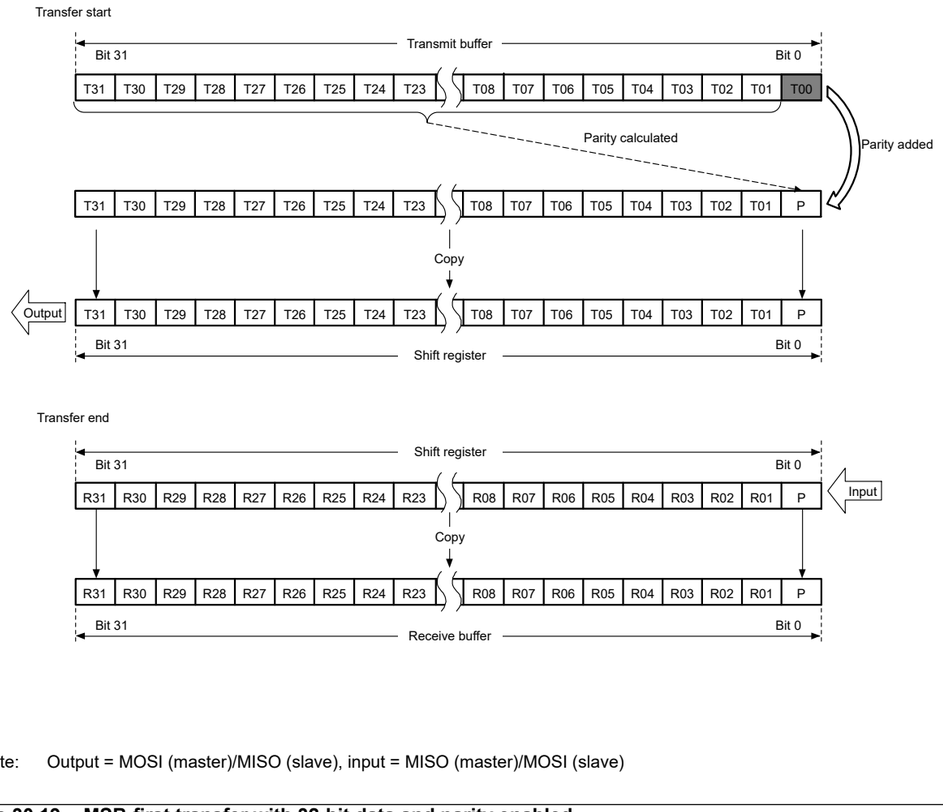


Figure 30.19 MSB-first transfer with 32-bit data and parity enabled

(2) MSB-first transfer with 24-bit data

Figure 30.20 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, a SPI data length of 24 bits, and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T23 to T01. This replaces the final bit, T00, and the whole value is copied to the shift register. Data is transmitted in the order T23, T22, …, T01, and P.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R23 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R23 to P is checked for parity.

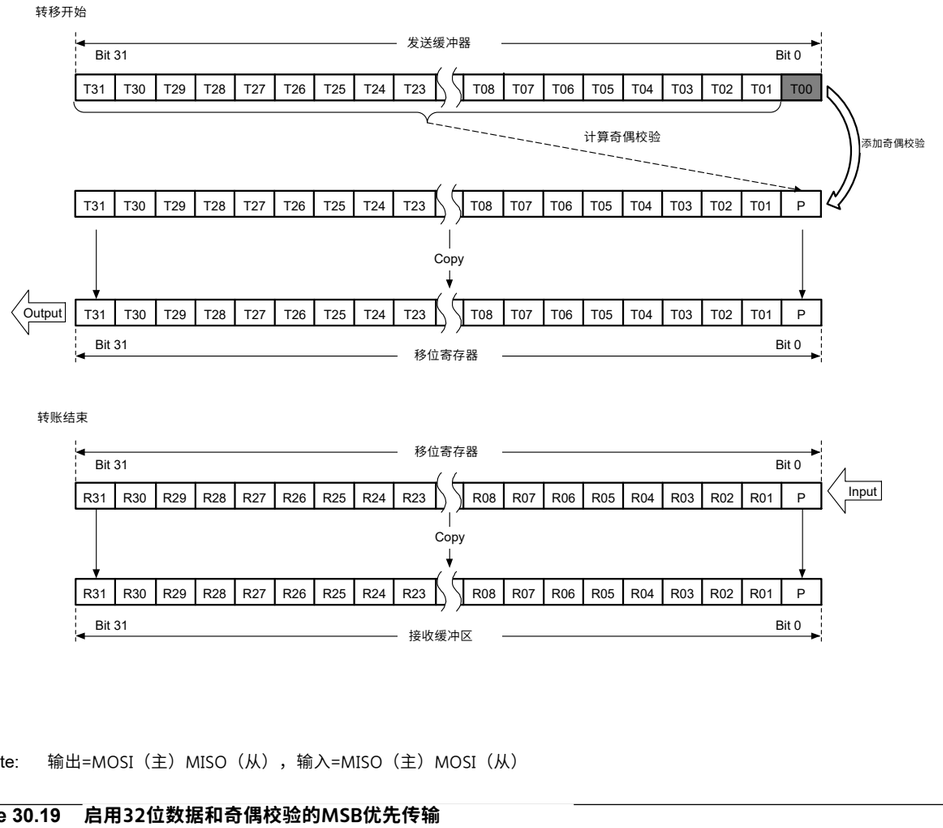


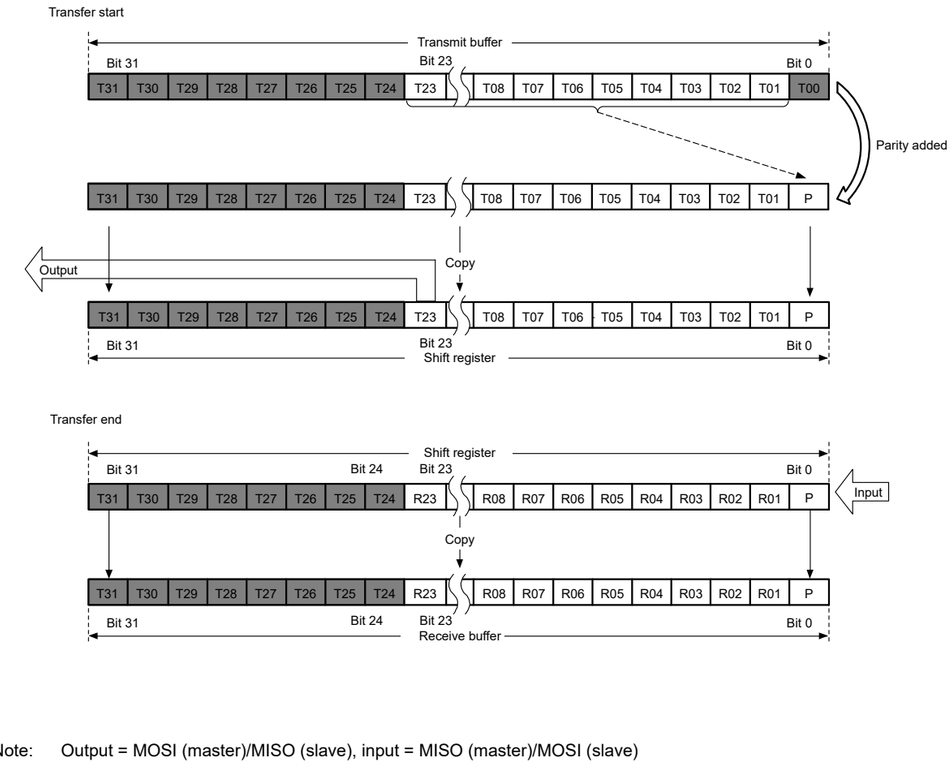
Figure 30.19 启用32位数据和奇偶校验的MSB优先传输

(2) 24位数据的MSB优先传输

图30.20显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，a SPI数据长度为24位，且MSB优先选择。

在传输中，奇偶校验位(P)的值是从位T23到T01计算的。这将替换最后一位T00，并将整个值复制到移位寄存器。数据按T23、T22、……、T01和P的顺序传输。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需数量的RSPCK周期后收集R23至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，会检查从R23到P的数据的奇偶性。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

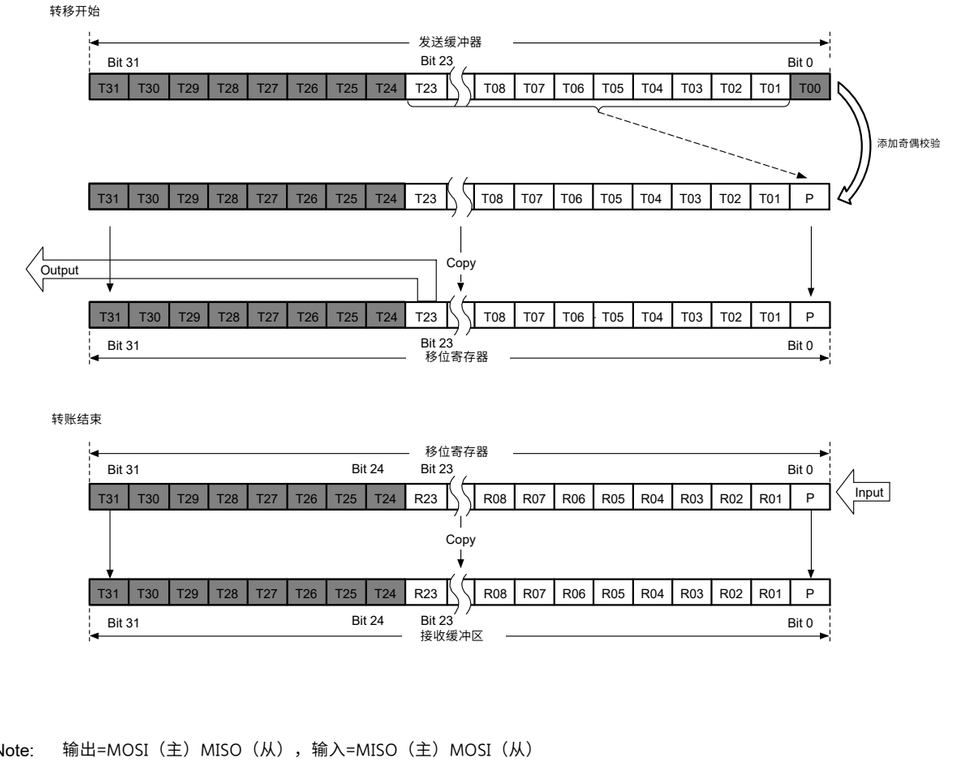
Figure 30.20 MSB-first transfer with 24-bit data and parity enabled

(3) LSB-first transfer with 32-bit data

Figure 30.21 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T30 to T00. This replaces the final bit, T31, and the whole value is copied to the shift register. Data is transmitted in the order T00, T01, …, T30, and P.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R00 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P is checked for parity.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

Figure 30.20 启用24位数据和奇偶校验的MSB优先传输

(3) 32位数据的LSB优先传输

图30.21显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，SPI数据长度为32位，并选择LSB-first。

在传输中，奇偶校验位(P)的值是从位T30到T00计算的。这将替换最后一位T31，并将整个值复制到移位寄存器。数据按T00、T01、……、T30和P的顺序传输。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需数量的RSPCK周期后收集R00至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，会检查从R00到P的数据的奇偶性。

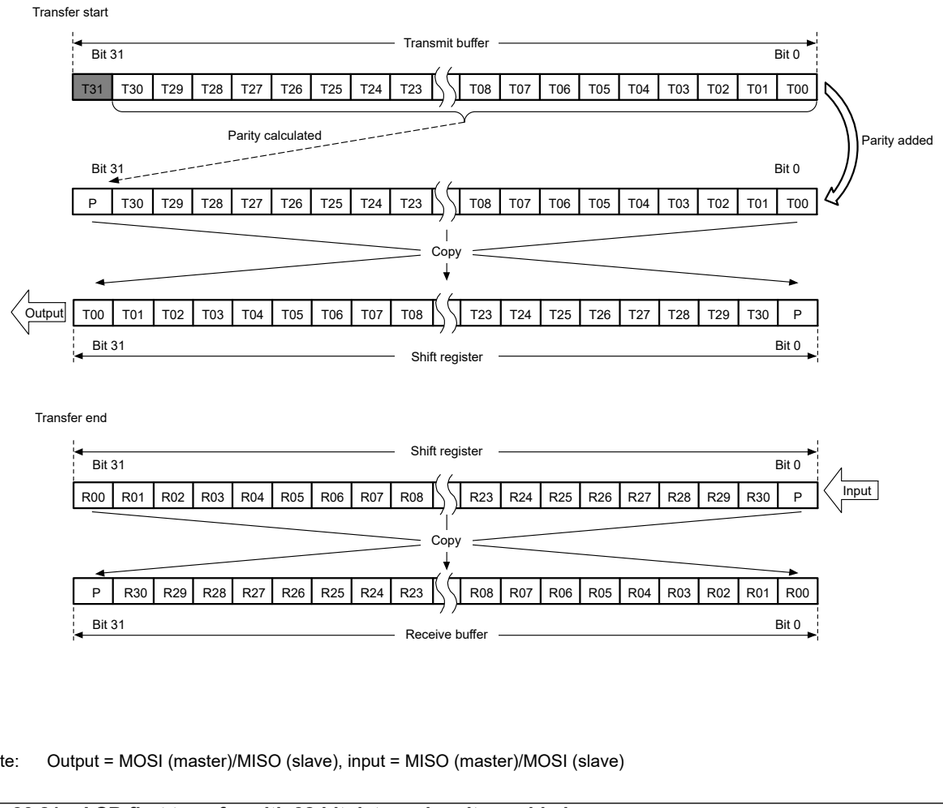


Figure 30.21 LSB-first transfer with 32-bit data and parity enabled

(4) LSB-first transfer with 24-bit data

Figure 30.22 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, a SPI data length of 24 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T22 to T00. This replaces the final bit, T23, and the whole value is copied to the shift register. Data is transmitted in the order T00, T01, …, T22, and P.

In reception, received data is shifted in bit-by-bit through bit[8] of the shift register. When the R00 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P is checked for parity.

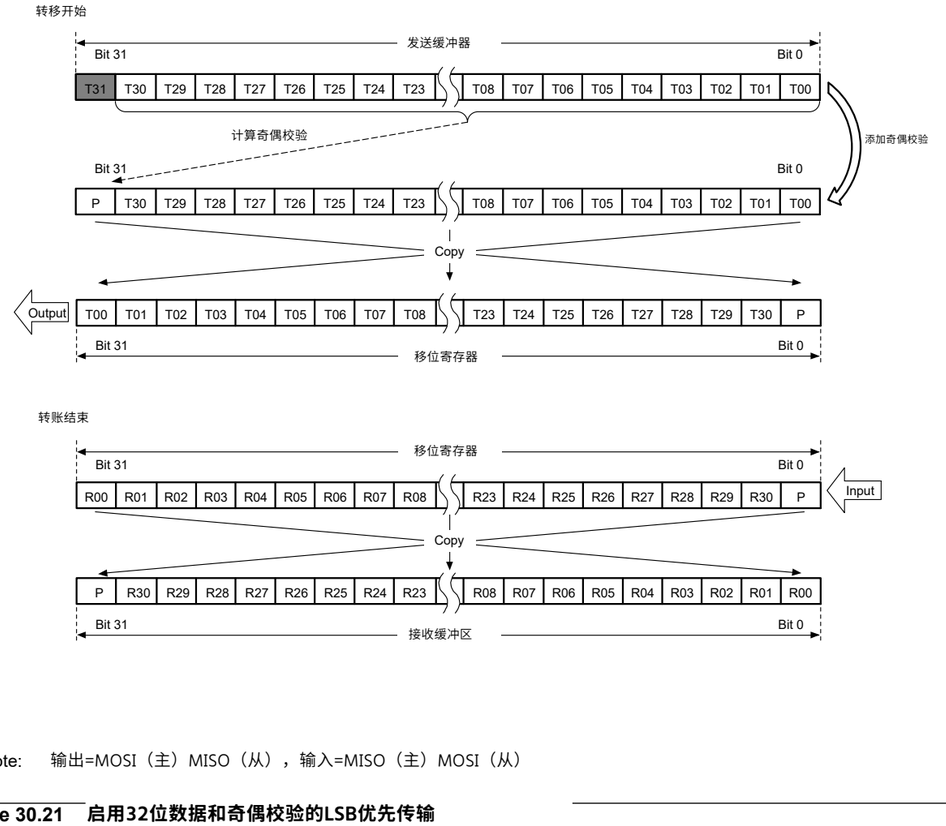


Figure 30.21 启用32位数据和奇偶校验的LSB优先传输

(4) 24位数据的LSB优先传输

图30.22显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，a SPI数据长度为24位，并选择LSB优先。

在传输中，奇偶校验位(P)的值是从位T22到T00计算的。这将替换最后一位T23，并将整个值复制到移位寄存器。数据按T00、T01、……、T22和P的顺序传输。

在接收中，接收到的数据通过移位寄存器的bit[8]逐位移位。在输入所需数量的RSPCK周期后收集R00至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，会检查从R00到P的数据的奇偶性。

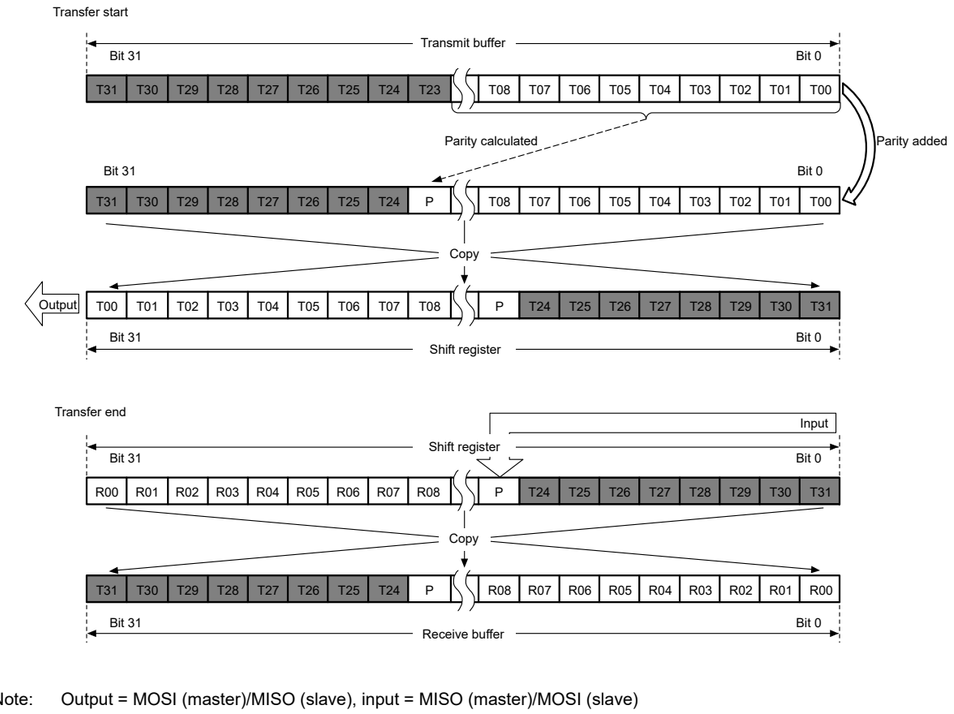


Figure 30.22 LSB-first transfer with 24-bit data and parity enabled

30.3.4.3 Byte Swap Transmission

When byte swapping is enabled, the data in the transmission buffer, swapped in 8-bit units, is copied to the shift register. Figure 30.23 shows the relationship between the SPDR (transmit buffer) and the shift register when transferring data with a 32-bit data length, using a combination of MSB / LSB first and with / without byte swap.

(1) MSB-first transfer. (When the byte swap is disabled.)

Data (Byte3 [T31 to T24] to Byte0 [T07 to T00]) in the transmit buffer are copied to the shift register.

Bit values in the shift register are shifted and transmitted in the order of T31 → T30 → … → T00 as transmit data.

(2) MSB-first transfer. (When the byte swap is enabled.)

Byte values of the transmit buffer (Byte3 [T31 to T24] to Byte0 [T07 to T00]) are reversed in byte units and are copied to the shift register in the order of Byte0 [T07 to T00] to Byte3 [T31 to T24].

Bit values in the shift register are shifted and transmitted in the order of T07 → T06 → … → T00 → T15 → T14 → … → T08 → T23 → T22 → … → T16 → T31 → T30 → … → T24 as transmit data.

(3) LSB-first transfer. (When the byte swap is disabled.)

Bit values of the transmit buffer (Byte3 [T31 to T24] to Byte0 [T07 to T00]) are reversed in bit units and are copied to the shift register in the order of Byte0 [T00 to T07] to Byte3 [T24 to T31].

Bit values in the shift register are shifted and transmitted in the order of T00 → T01 → … → T31 as transmit data.

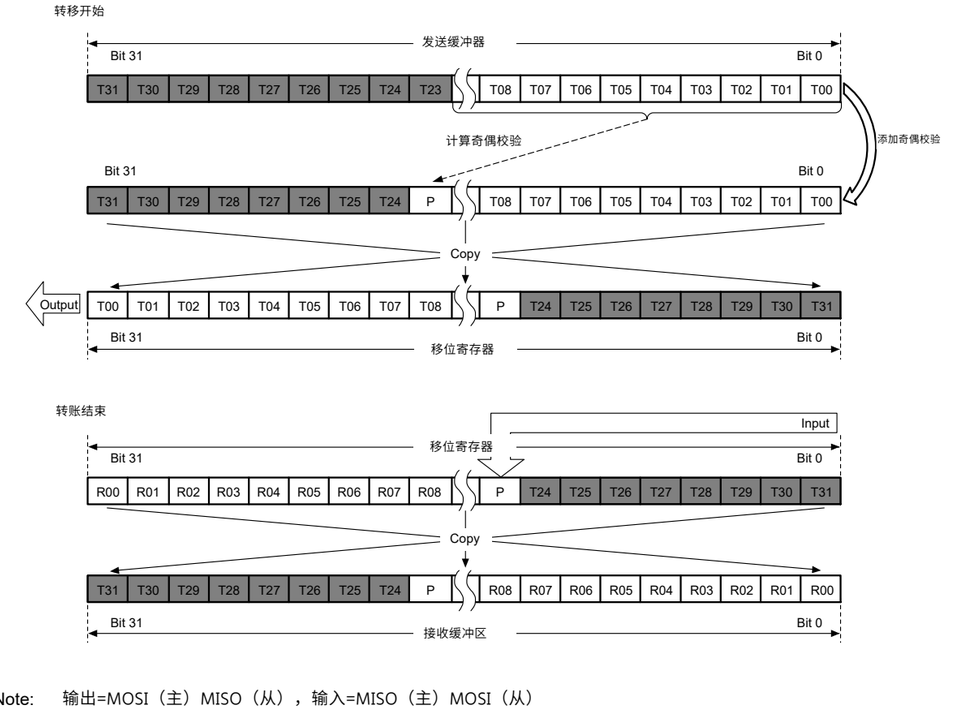


Figure 30.22 启用24位数据和奇偶校验的LSB优先传输

30.3.4.3 字节交换传输

当启用字节交换时，传输缓冲区中的数据以8位为单位进行交换，被复制到移位寄存器中。
图30.23显示了传输32位数据长度的数据时SPDR（发送缓冲区）和移位寄存器之间的关系，使用MSBLSB在前和不进行字节交换的组合。

(1) MSB优先传输。（禁用字节交换时。）

发送缓冲器中的数据（Byte3[T31到T24]到Byte0[T07到T00]）被复制到移位寄存器。

移位寄存器中的位值按照T31→T30→…→T00的顺序移位和传输，作为传输数据。

(2) MSB优先传输。（启用字节交换时。）

发送缓冲区的字节值（Byte3[T31到T24]到Byte0[T07到T00]）以字节为单位反转，并按照Byte0[T07到T00]到Byte3[T31到T24]的顺序复制到移位寄存器.

移位寄存器中的位值按照T07→T06→…→T00→T15→T14→…→的顺序移位传输
T08→T23→T22→…→T16→T31→T30→…→T24作为传输数据。

(3) LSB优先传输。（禁用字节交换时。）

发送缓冲区的位值（Byte3[T31到T24]到Byte0[T07到T00]）以位为单位反转，并按照Byte0[T00到T07]到Byte3[T24到T31]的顺序复制到移位寄存器.

移位寄存器中的位值按照T00→T01→…→T31的顺序移位和发送，作为发送数据。

(4) LSB-first transfer. (When the byte swap is enabled.)

Bit values of each byte of the transmit buffer (Byte3 [T31 to T24] to Byte0 [T07 to T00]) are reversed in bit units and are copied to the shift register in the order of Byte3 [T24 to T31] to Byte0 [T00 to T07].

Bit values in the shift register are shifted and transmitted in the order of T24 → T25 → … → T31 → T16 → T17 → … → T23 → T08 → T09 → … → T15 → T00 → T01 → … → T07 as transmit data.

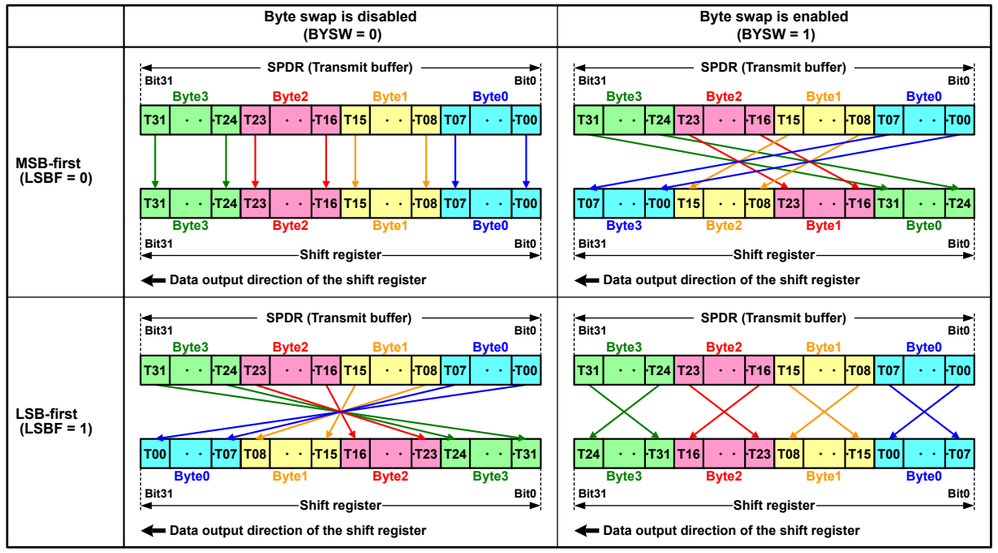


Figure 30.23 Byte swap with MSB/LSB transfer (32bit)

Figure 30.24 shows the relationship between the SPDR (transmit buffer) and the shift register when transferring data with a 16-bit data length, using a combination of MSB / LSB first and with / without byte swap.

1. MSB-first transfer. (When the byte swap is disabled.)
   The transmission buffer data (Byte1 [T15 to T08] to Byte0 [T07 to T00]) is stored in the shift register as Byte1 [T15 to T08] to Byte0 [T07 to T00], Byte1 [T15 to T08] to Byte0 [T07 to T00]. Transmission data is transmitted by shifting the value of the shift register in the order of T15 → T14 → … T00.
2. MSB-first transfer. (When the byte swap is enabled.)
   The data (Byte1 [T15 to T08] to Byte0 [T07 to T00]) of the transmission buffer is replaced in byte units, and Byte0 [T07 to T00] to Byte1 [T15 to T08] and Byte0 [T07 to T00] to Byte1 are stored in the shift register. Sort and copy in the order of [T15 to T08]. The transmission data is transmitted by shifting the value of the shift register in the order of T07 → T06 → … T00 →→ T15 → T14 → … T08.
3. LSB-first transfer. (When the byte swap is disabled.)
   The data (Byte1 [T15 to T08] to Byte0 [T07 to T00]) of the transmission buffer is replaced in bit units, and Byte0 [T00 to T07] to Byte1 [T08 to T15] and Byte0 [T00 to T07] to Byte1 are stored in the shift register. Sort and copy in the order of [T08 to T15]. The transmission data is transmitted by shifting the value of the shift register in the order of T00 → T01 → … T15.
4. LSB-first transfer. (When the byte swap is enabled.)
   The data (Byte1 [T15 to T08] to Byte0 [T07 to T00]) of the transmission buffer is replaced in units of bits for each byte, and the data is rearranged and copied to the shift register in the order of Byte1 [T08 to T15] to Byte0 [T00 to T07]. The transmission data shifts the value of the shift register in the order of T08 → T09 → … T15 → T00 → T01 → … T07 and transmits.

(4) LSB优先传输。（启用字节交换时。）

发送缓冲区（Byte3[T31到T24]到Byte0[T07到T00]）的每个字节的位值以位为单位反转，并按照Byte3[T24到T31]到Byte0[T00]的顺序复制到移位寄存器到T07]。

移位寄存器中的位值按照T24→T25→…→T31→T16→T17→…→的顺序进行移位和传输
T23→T08→T09→…→T15→T00→T01→…→T07作为传输数据。

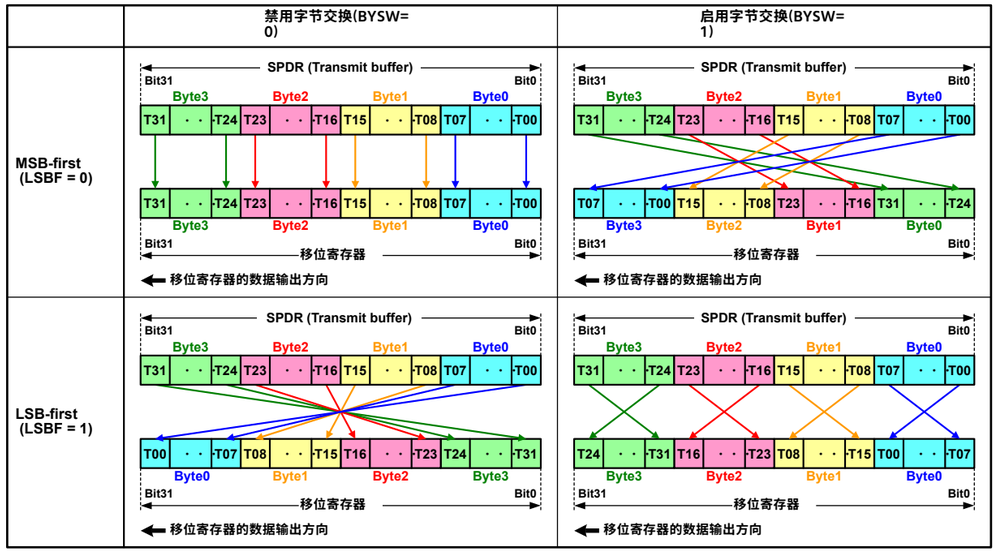


Figure 30.23 带MSBLSB传输的字节交换（32位）

图30.24显示了传输16位数据长度的数据时SPDR（发送缓冲区）和移位寄存器之间的关系，使用MSBLSB在前和不进行字节交换的组合。

1.MSB优先传输。（禁用字节交换时。）
发送缓冲数据（Byte1[T15toT08]toByte0[T07toT00]）作为Byte1[T15toT08]toByte0[T07toT00]、Byte1[T15toT08]toByte0[T07]存储在移位寄存器中到T00]。传输数据通过按T15→T14→…T00的顺序移位移位寄存器的值来传输。

2.MSB优先传输。（启用字节交换时。）
传输缓冲区的数据（Byte1[T15toT08]toByte0[T07toT00]）以字节为单位替换，Byte0[T07toT00]toByte1[T15toT08]和Byte0[T07toT00]toByte1存储在移位寄存器中。按【T15到T08】的顺序排序和复制。传输数据通过移位寄存器的值按照T07→T06→…T00→→T15→T14→…T08的顺序进行移位来传输。

3.LSB优先传输。（禁用字节交换时。）
传输缓冲区的数据（Byte1[T15toT08]toByte0[T07toT00]）以位为单位替换，Byte0[T00toT07]toByte1[T08toT15]和Byte0[T00toT07]toByte1存储在移位寄存器中。按照【T08到T15】的顺序排序和复制。传输数据通过按T00→T01→…T15的顺序移位移位寄存器的值来传输。

4.LSB优先传输。（启用字节交换时。）
发送缓冲器的数据（Byte1[T15～T08]～Byte0[T07～T00]）以每个字节为单位进行置换，按照Byte1[T08～T08～T15]到字节0[T00到T07]。发送数据按照T08→T09→…T15→T00→T01→…T07的顺序对移位寄存器的值进行移位后发送。

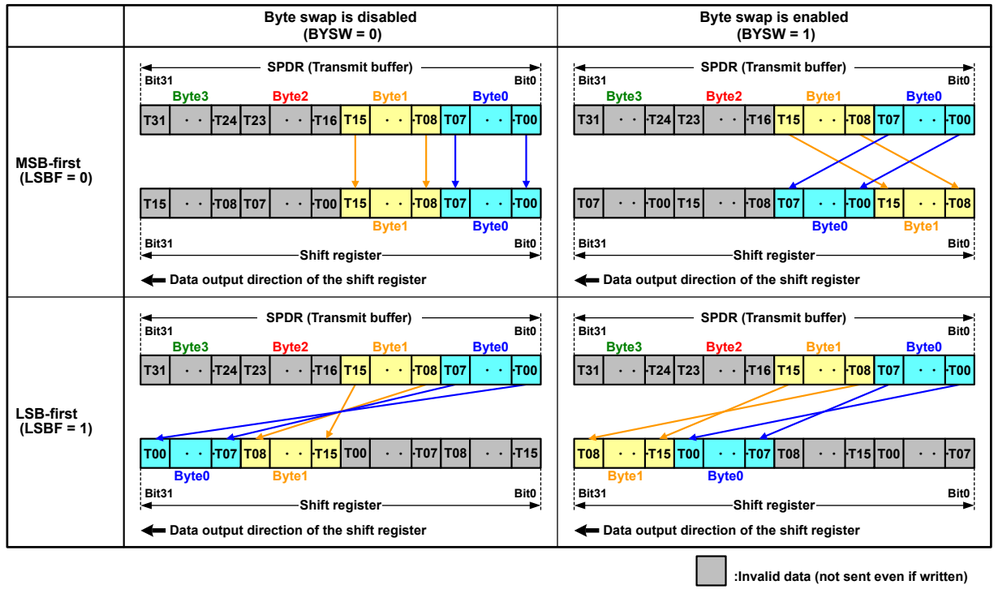


Figure 30.24 Byte swap with MSB/LSB transfer (16bit)

Note: 1. When using the byte swap, set 16 bits or 32 bits to the data length (SPCMDm.SPB[4:0] setting). If setting the other length, the behavior is not guaranteed.
2. When the byte swap is valid, set the parity function as invalid (SPCR.SPPE bit = 0). If setting the parity function as valid (SPPE bit = 1), the behavior is not guaranteed.
3. Set SPDCR.BYSW bit, when SPCR.SPE bit is 0. If rewriting BYSW bit, when SPE bit is 1, the behavior after it is not guaranteed.

30.3.4.4 Byte Swap Reception

When byte swap is enabled, the data in the shift register, swapped in 8-bit units, is copied to the receive buffer. Figure 30.25 shows the relationship between the shift register and SPDR (reception buffer) when transferring data with a 32-bit data length, using a combination of MSB / LSB first and with / without byte swap.

(1) MSB-first transfer. (When the byte swap is disabled.)

The first received data (R31) is stored in bit 0 of the shift register, and received data is shifted in the order of R31 → R30 → … → R00.

When necessary RSPCK cycles are input and data is stored from Byte3 [R31 to R24] to Byte0 [R07 to R00], the shift register value is copied to the receive buffer.

(2) MSB-first transfer. (When the byte swap is enabled.)

The first received data (R07) is stored in bit 0 of the shift register, and received data is shifted in the order of R07 → R06 → … → R00 → R15 → R14 → … → R08 → R23 → R22 → … → R16 → R31 → R30 → … → R24.

When necessary RSPCK cycles are input and data is stored from Byte0 [R07 to R00] to Byte3 [R31 to R24], byte values in the shift register are reversed in byte units and are copied to the receive buffer in the order of Byte3 [R31 to R24] to Byte0 [R07 to R00].

(3) LSB-first transfer. (When the byte swap is disabled.)

The first received data (R00) is stored in bit 0 of the shift register, and received data is shifted in the order of R00 → R01 → … → R31.

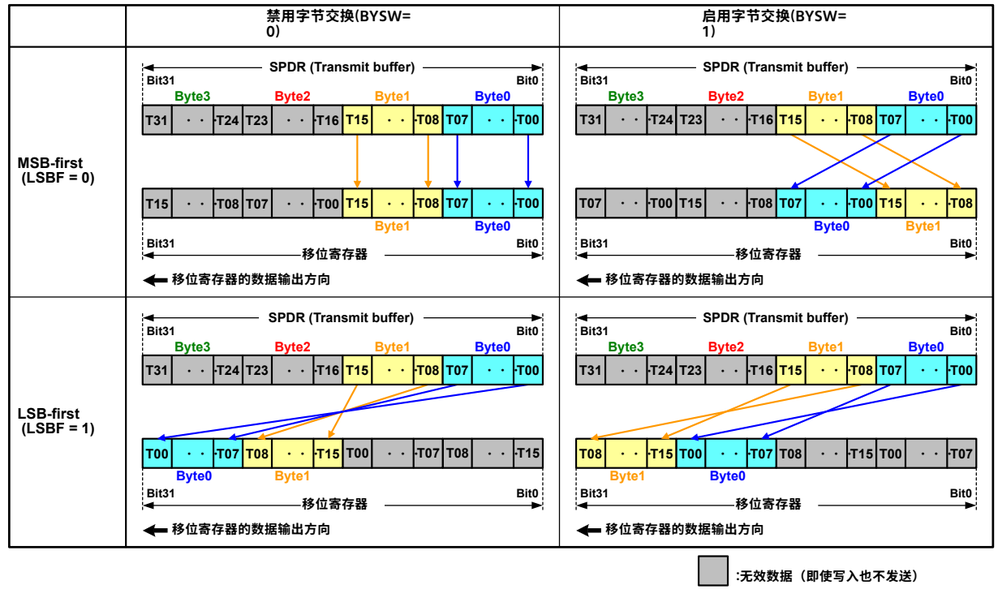


Figure 30.24 带MSBLSB传输的字节交换（16位）

Note: 1.使用字节交换时，将数据长度设置为16位或32位（SPCMDm.SPB[4:0]设置）。如果设置其他长度，则无法保证行为。2.当字节交换有效时，将奇偶校验功能设置为无效（SPCR.SPPE位=0）。如果将奇偶校验功能设置为有效（SPPE位=1），则无法保证行为。3.当SPCR.SPE位为0时，设置SPDCR.BYSW位。如果重写BYSW位，当SPE位为1时，不保证之后的行为。

30.3.4.4 字节交换接收

当字节交换使能时，移位寄存器中的数据以8位为单位进行交换，被复制到接收缓冲区。图30.25显示了在传输32位数据长度的数据时移位寄存器和SPDR（接收缓冲区）之间的关系，使用MSBLSB在前和不进行字节交换的组合。

(1) MSB优先传输。（禁用字节交换时。）

第一个接收到的数据（R31）存储在移位寄存器的第0位，接收到的数据按照R31→R30→…→R00的顺序进行移位。

当输入必要的RSPCK周期并将数据从Byte3[R31到R24]存储到Byte0[R07到R00]时，移位寄存器值被复制到接收缓冲区。

(2) MSB优先传输。（启用字节交换时。）

第一个接收到的数据（R07）存放在移位寄存器的第0位，接收到的数据按照R07→R06→…→R00→R15→R14→…→R08→R23→R22→…→R16→的顺序移位R31→R30→…→R24。

当输入必要的RSPCK周期并将数据从Byte0[R07到R00]到Byte3[R31到R24]存储时，移位寄存器中的字节值以字节为单位反转，并按Byte3[R31的顺序复制到接收缓冲区到R24]到字节0[R07到R00]。

(3) LSB优先传输。（禁用字节交换时。）

第一个接收到的数据（R00）存放在移位寄存器的第0位，接收到的数据按照R00→R01→…→R31的顺序移位。

When necessary RSPCK cycles are input and data is stored from Byte0 [R00 to R07] to Byte3 [R24 to R31], bit values in the shift register are reversed in bit units and are copied to the receive buffer in the order of Byte3 [R31 to R24] to Byte0 [R07 to R00].

(4) LSB-first transfer. (When the byte swap is enabled.)

The first received data (R24) is stored in bit 0 of the shift register, and received data is shifted in the order of R24 → R25 → … → R31 → R16 → R17 → … → R23 → R08 → R09 → … → R15 → R00 → R01 → … → R07.

When necessary RSPCK cycles are input and data is stored from Byte3 [R24 to R31] to Byte0 [R00 to R07], bit values of each byte in the shift register are reversed in bit units and are copied to the receive buffer in the order of Byte3 [R31 to R24] to Byte0 [R07 to R00].

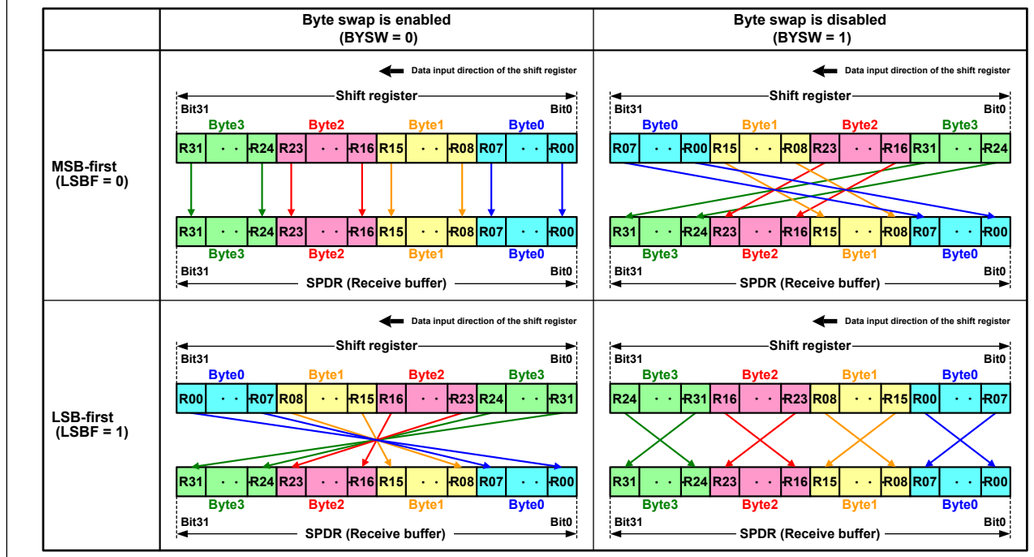


Figure 30.25 Byte swap with MSB/LSB transfer (32bit)

Figure 30.26 shows the relationship between the shift register and SPDR (reception buffer) when transferring data with a 16-bit data length, using a combination of MSB / LSB first and with / without byte swap.

1. MSB-first transfer. (When the byte swap is disabled.)
   The first data (R15) is stored in bit 0 of the shift register, and the received data is shifted for each data in the order of R15 → R14 → … R00. When necessary RSPCK is input and the data is accumulated, the value of the shift register (Byte3 [R31 to R24] to Byte0 [R07 to R00]) is copied to the reception buffer as it is.
2. MSB-first transfer. (When the byte swap is enabled.)
   The first data (R07) is stored in bit 0 of the shift register, and the received data is shifted for each data in the order of R07 → R06 → … R00 → R15 → R14 → … R08. When the necessary RSPCK is input and the data is accumulated, the values of the shift register (Byte0 [R07-R00]-Byte1 [R15-R08]) are replaced in byte units, and Byte3[R31-R24]-Byte0 [R07- R00].
3. LSB-first transfer. (When the byte swap is disabled.)
   The first data (R00) is stored in bit 15 of the shift register, and the received data is shifted for each data in the order of R00 → R01 → … R07 → R08 → R09 → … R15. When the necessary RSPCK is input and the data is accumulated, the values of the shift register (Byte0 [R00 to R07] to Byte1 [R08 to R15]) are exchanged in bit units, and Byte3 [R31 to R24] to Byte0 [R07-R00] in order.
4. LSB-first transfer. (When the byte swap is enabled.)
   The first data (R08) is stored in bit 15 of the shift register, and the received data is shifted for each data in the order of R08 → R09 → … R15 → R00 → R01 → … R15. When the necessary RSPCK is input and the data is accumulated, the

当输入必要的RSPCK周期并将数据从Byte0[R00到R07]到Byte3[R24到R31]存储时，移位寄存器中的位值以位为单位反转，并按Byte3[R31的顺序复制到接收缓冲区到R24]到字节0[R07到R00]。

(4) LSB优先传输。（启用字节交换时。）

第一个接收到的数据（R24）存放在移位寄存器的第0位，接收到的数据按R24→R25→…→R31→R16→R17→…→R23→R08→R09→…→R15→的顺序移位R00→R01→…→R07。

当输入必要的RSPCK周期并将数据从Byte3[R24到R31]到Byte0[R00到R07]存储时，移位寄存器中每个字节的位值以位为单位反转并按顺序复制到接收缓冲区字节3[R31到R24]到字节0[R07到R00]。

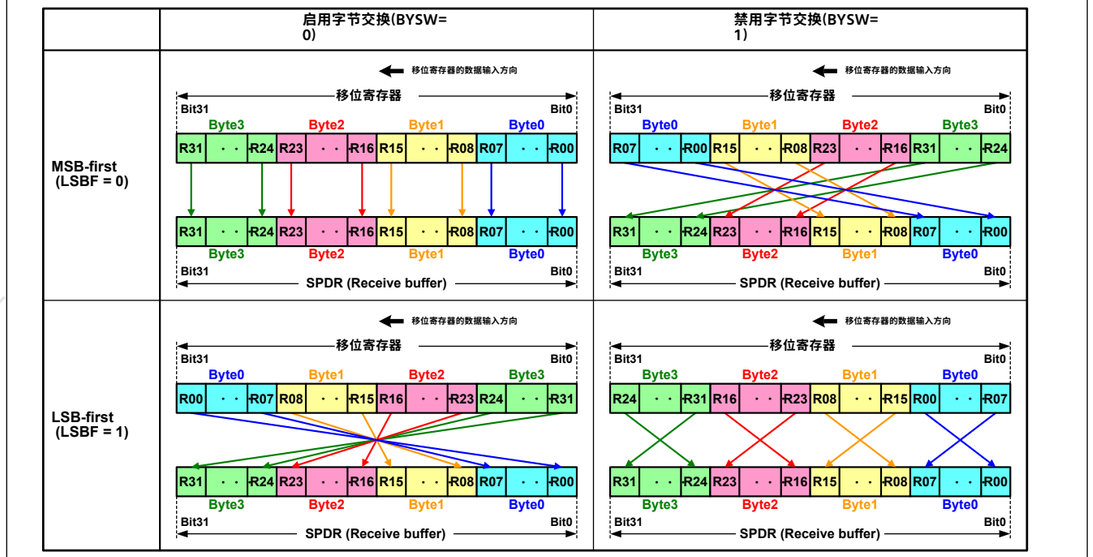


Figure 30.25 带MSBLSB传输的字节交换（32位）

图30.26显示了在传输16位数据长度的数据时移位寄存器和SPDR（接收缓冲区）之间的关系，使用MSBLSB在前和不进行字节交换的组合。

1.MSB优先传输。（禁用字节交换时。）
第一个数据(R15)存储在移位寄存器的位0中，接收到的数据按R15→R14→…R00的顺序对每个数据进行移位。当输入必要的RSPCK并累积数据时，移位寄存器的值(Byte3[R31到R24]到Byte0[R07到R00])被原样复制到接收缓冲区。

2.MSB优先传输。（启用字节交换时。）
第一个数据（R07）存储在移位寄存器的第0位，接收到的数据按每个数据的顺序移位
R07→R06→…R00→R15→R14→…R08。当输入必要的RSPCK并累加数据时，移位寄存器（Byte0[R07-R00]-Byte1[R15-R08]）的值以字节为单位替换，Byte3[R31-R24]-Byte0[R07R00]。

3.LSB优先传输。（禁用字节交换时。）
第一个数据（R00）存储在移位寄存器的第15位，接收到的数据按R00→R01→…R07→R08→R09→…R15的顺序对每个数据进行移位。当输入必要的RSPCK并累积数据时，移位寄存器的值（Byte0[R00到R07]到Byte1[R08到R15]）以位为单位进行交换，并且Byte3[R31到R24]到Byte0[R07-R00]的顺序。

4.LSB优先传输。（启用字节交换时。）
第一个数据（R08）存储在移位寄存器的第15位，接收到的数据按每个数据的顺序移位
R08→R09→…R15→R00→R01→…R15。当输入必要的RSPCK并累积数据时，

values of the shift register (Byte1 [R08 to R15] to Byte0 [R00 to R07]) are replaced in byte units for each byte, and Byte3 [R31 to R24] is stored in the reception buffer. Sort and copy in the order of Byte0 [R07 to R00].

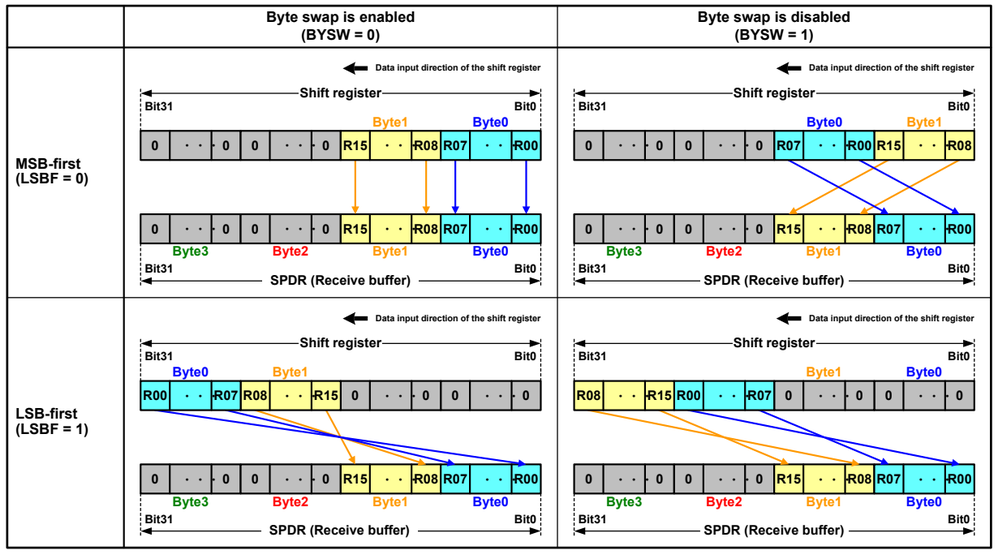


Figure 30.26 Byte swap with MSB/LSB transfer(16bit)

Note: 1. When using the byte swap, set 16 bits or 32 bits to the data length (SPCMDm.SPB[4:0] setting). If setting the other length, the behavior is not guaranteed.
2. When the byte swap is valid, set the parity function as invalid (SPCR.SPPE bit = 0). If setting the parity function as valid (SPPE bit = 1), the behavior is not guaranteed.
3. Set SPDCR.BYSW bit, when SPCR.SPE bit is 0. If rewriting BYSW bit, when SPE bit is 1, the behavior after it is not guaranteed.

30.3.5 Transfer Formats

30.3.5.1 When CPHA = 0

Figure 30.27 shows an example transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 0. Do not perform clock synchronous operation (SPCR.SPMS = 1) when the SPI operates in slave mode (SPCR.MSTR = 0) and the CPHA bit is 0. In Figure 30.27, RSPCKn (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMDm.CPOL bit is 0, and RSPCKn (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI settings. For details, see section 30.3.2. Controlling the SPI Pins.

When the SPCMDm.CPHA bit is 0, the driving of valid data to the MOSIn and MISOn signals begins at an SSLni signal assertion. The first RSPCKn signal change that occurs after the SSLni signal assertion becomes the first transfer data fetch. After this, data is sampled every 1 RSPCK cycle. The change timing for MOSIn and MISOn signals is 1/2 RSPCK cycles after the transfer data fetch timing. The CPOL bit setting does not affect the RSPCK signal operation timing as it only affects the signal polarity.

t1 denotes the RSPCK delay, the period from an SSLni signal assertion to RSPCKn oscillation. t2 denotes the SSL negation delay, the period from the termination of RSPCKn oscillation to an SSLni signal negation. t3 denotes the next-access delay, the period in which SSLni signal assertion is suppressed for the next transfer after the end of serial transfer. t1, t2, and t3 are controlled by a master device running on the SPI system. For a description of t1, t2, and t3 when the SPI is in master mode, see section 30.3.12.1. Master mode operation.

[In the Motorola-SPI case]

移位寄存器(Byte1[R08到R15]到Byte0[R00到R07])的值以每个字节为单位进行替换，并将Byte3[R31到R24]存储在接收缓冲区中。按照Byte0[R07到R00]的顺序排序和复制。

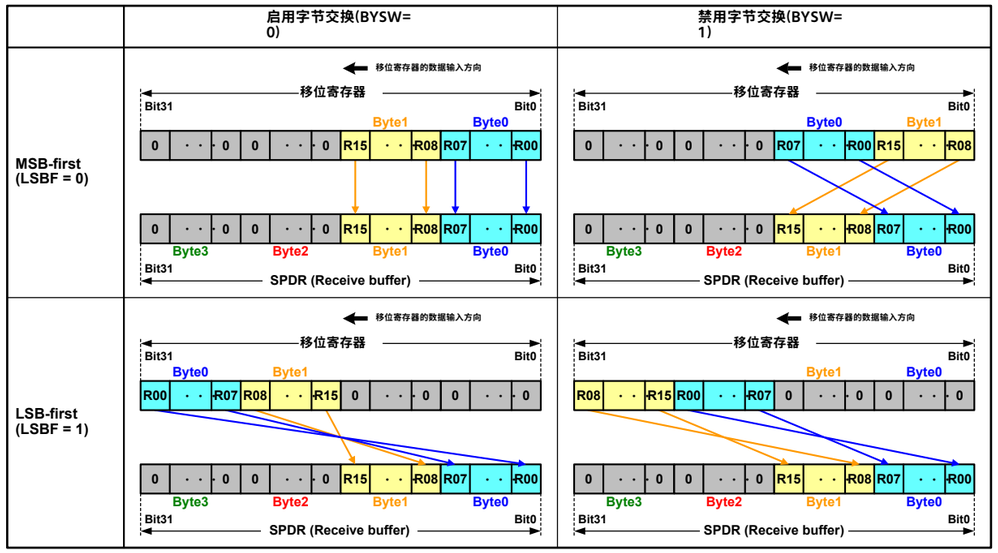


Figure 30.26 带MSBLSB传输的字节交换（16位）

Note: 1.使用字节交换时，将数据长度设置为16位或32位（SPCMDm.SPB[4:0]设置）。如果设置其他长度，则无法保证行为。2.当字节交换有效时，将奇偶校验功能设置为无效（SPCR.SPPE位=0）。如果将奇偶校验功能设置为有效（SPPE位=1），则无法保证行为。3.当SPCR.SPE位为0时，设置SPDCR.BYSW位。如果重写BYSW位，当SPE位为1时，不保证之后的行为。

30.3.5 传输格式

30.3.5.1 When CPHA = 0

图30.27显示了当SPCMDm.CPHA位为0时串行传输8位数据的示例传输格式。当SPI在从机模式下运行时（SPCR.MSTR=0)且CPHA位为0。在图30.27中，RSPCKn(CPOL=0)表示SPCMDm.CPOL位为0时的RSPCKn信号波形，RSPCKn(CPOL=1)表示CPOL位为0时的RSPCKn信号波形1.采样时序表示SPI将串行传输数据取入移位寄存器的时序。信号的IO方向取决于SPI设置。有关详细信息，请参阅第30.3.2节。控制SPI引脚。

当SPCMDm.CPHA位为0时，将有效数据驱动到MOSIn和MISOn信号开始于SSLni信号断言。在SSLni信号断言之后发生的第一个RSPCKn信号变化成为第一次传输数据获取。此后，每1个RSPCK周期对数据进行采样。MOSIn和MISOn信号的变化时序是传输数据获取时序之后的12RSPCK周期。CPOL位设置不影响RSPCK信号操作时序，因为它只影响信号极性。

t1表示RSPCK延迟，即从SSLni信号断言到RSPCKn振荡的周期。t2表示SSL否定延迟，即从RSPCKn振荡终止到SSLni信号否定的周期。t3表示下一次访问延迟，即在串行传输结束后为下一次传输抑制SSLni信号断言的时间段。t1、t2和t3由在SPI系统上运行的主设备控制。有关SPI处于主模式时的t1、t2和t3的说明，请参见第30.3.12.1节。主模式操作。

[In the Motorola-SPI case]

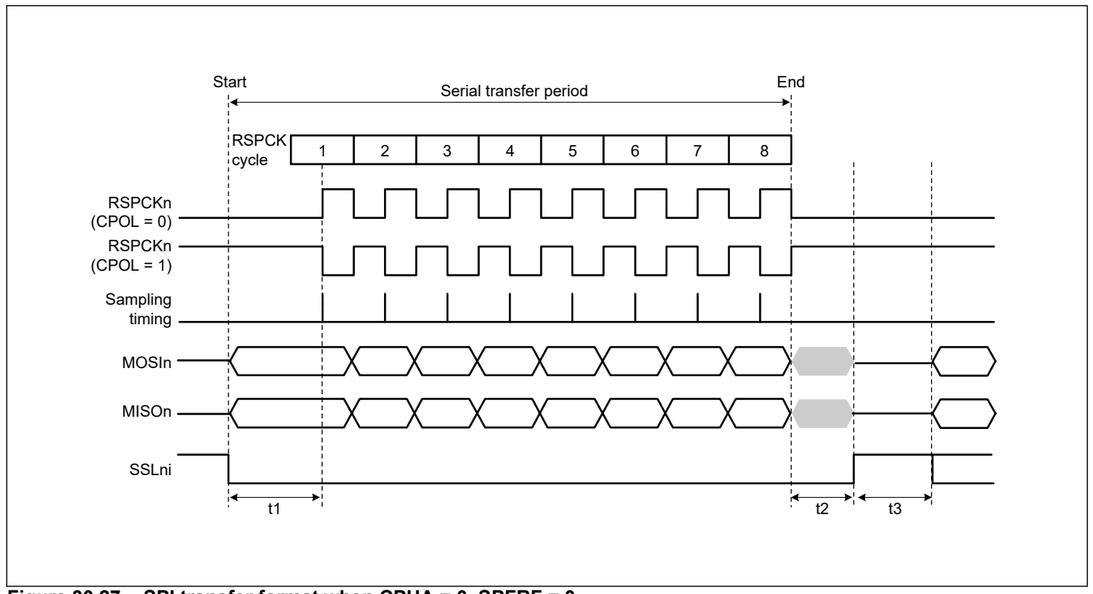


Figure 30.27 SPI transfer format when CPHA = 0, SPFRF = 0

[In TI-SSP case]

Not supported in CPHA = 0

30.3.5.2 When CPHA = 1

Figure 30.28 shows an example transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 1. However, when the SPCR.SPMS bit is 1, the SSLni signals are not used, and only the three signals RSPCKn, MOSIn, and MISOn handle communications. In Figure 30.28, RSPCK (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMDm.CPOL bit is 0 and RSPCK (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI mode (master or slave mode). For details, see section 30.3.2. Controlling the SPI Pins.

When the SPCMDm.CPHA bit is 1, the driving of invalid data to the MISOn signal begins at an SSLni signal assertion. The output of valid data to the MOSIn and MISOn signals begins at the first RSPCKn signal change that occurs after the SSLni signal assertion. After this, data is updated every 1 RSPCK cycle. The transfer data fetch timing is 1/2 RSPCK cycles after the data update timing. The SPCMDm.CPOL bit setting does not affect the RSPCKn signal operation timing. It only affects the signal polarity.

t1, t2, and t3 are the same as those when CPHA = 0. For a description of t1, t2, and t3 when the SPI of the MCU is in master mode, see section 30.3.12.1. Master mode operation.

[In the Motorola-SPI case]

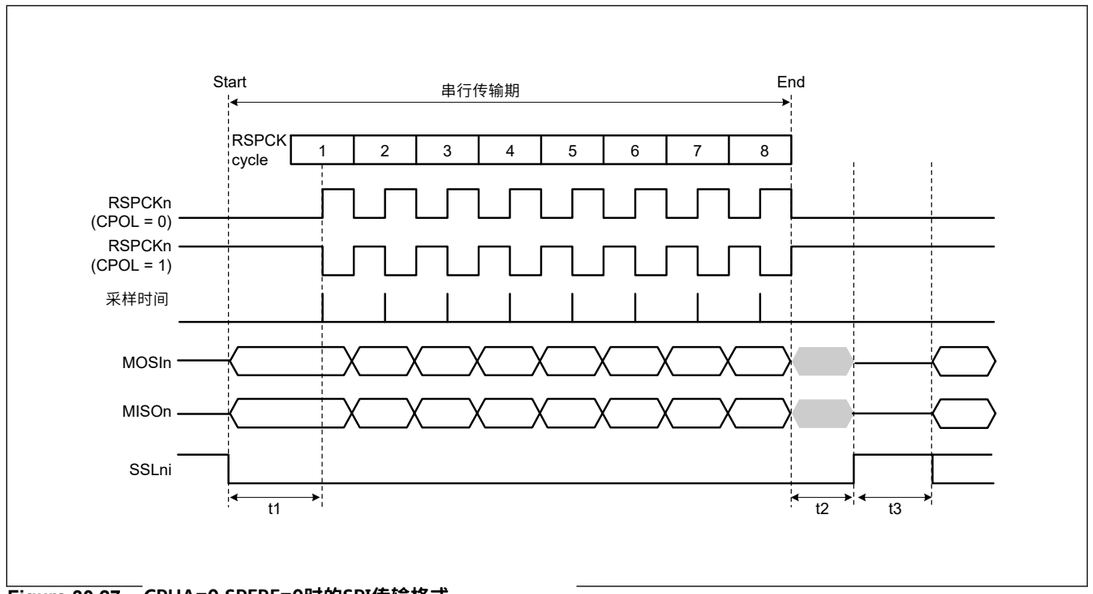


Figure 30.27 CPHA=0 SPFRF=0时的SPI传输格式

[In TI-SSP case]

CPHA不支持=0

30.3.5.2 When CPHA = 1

图30.28显示了当SPMDm.CPHA位为1时串行传输8位数据的示例传输格式。
但是，当SPCR.SPMS位为1时，不使用SSLni信号，只有RSPCKn、MOSIn和MISON处理通信。在图30.28中，RSPCK(CPOL=0)表示SPCMDm.CPOL位为0时的RSPCKn信号波形，RSPCK(CPOL=1)表示CPOL位为1时的RSPCKn信号波形。SPI将串行传输数据提取到移位寄存器中。信号的IO方向取决于SPI模式（主模式或从模式）。有关详细信息，请参阅第30.3.2节。控制SPI引脚。

当SPCMDm.CPHA位为1时，将无效数据驱动到MIOn信号开始于SSLni信号断言。在SSLni信号置位后发生的第一个RSPCKn信号变化时，开始向MOSIn和MISOn信号输出有效数据。此后，每1个RSPCK周期更新一次数据。传输数据获取时序是数据更新时序之后的12个RSPCK周期。SPCMDm.CPOL位设置不影响RSPCKn信号操作时序。它只影响信号极性。

t1、t2、t3与CPHA=0时相同。MCU的SPI为主机模式时t1、t2、t3的说明见30.3.12.1节。主模式操作。

[In the Motorola-SPI case]

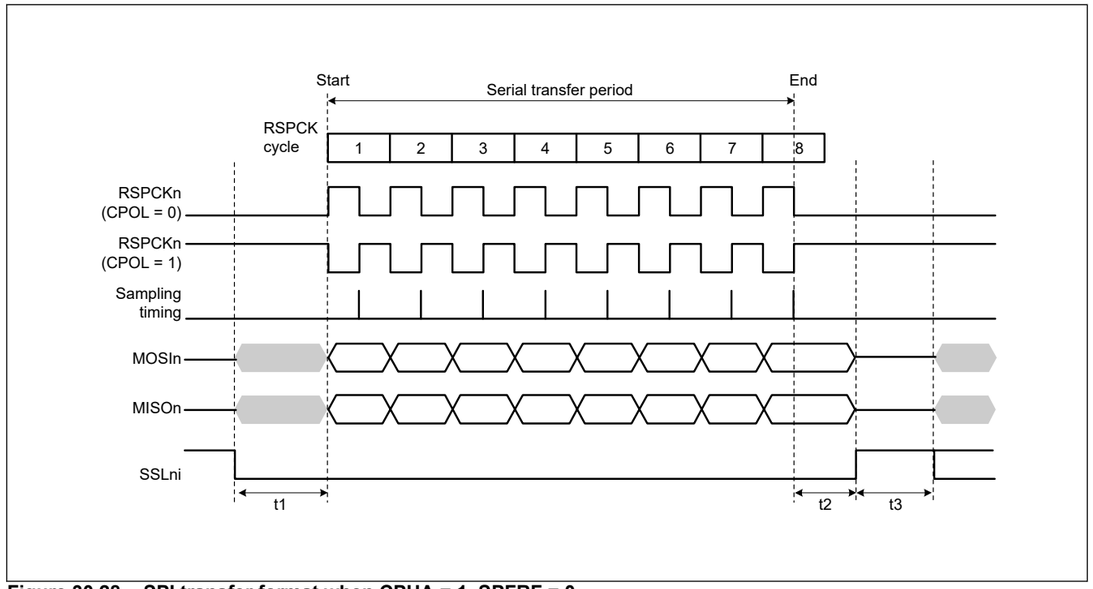


Figure 30.28 SPI transfer format when CPHA = 1, SPFRF = 0

[In the TI-SSP case]

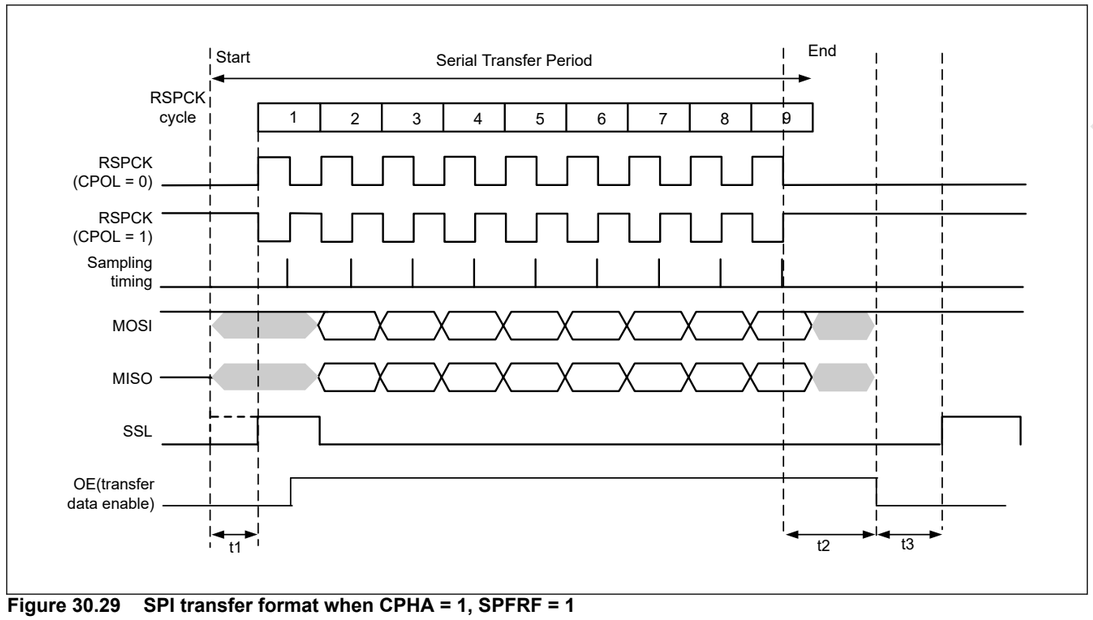


Figure 30.29 SPI transfer format when CPHA = 1, SPFRF = 1

30.3.6 Communication Operating Mode

Transmit-Receive serial communication, transmit-only operation, and Receive-only operation are selected by setting the Communication Mode Select bits (TXMD [1:0]) of the RSPI control register (SPCR).

SPDR access described in Figure 30.30, Figure 30.31, Figure 30.32 shows an access to the RSPI data register (SPDR). W shows a write cycle.

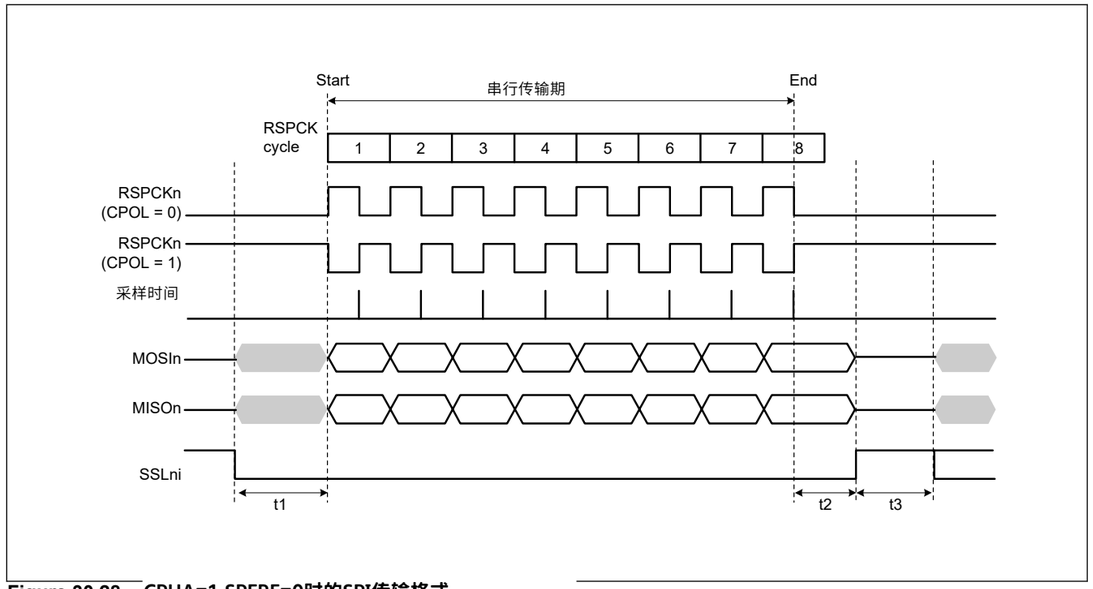


Figure 30.28 CPHA=1 SPFRF=0时的SPI传输格式

[In the TI-SSP case]

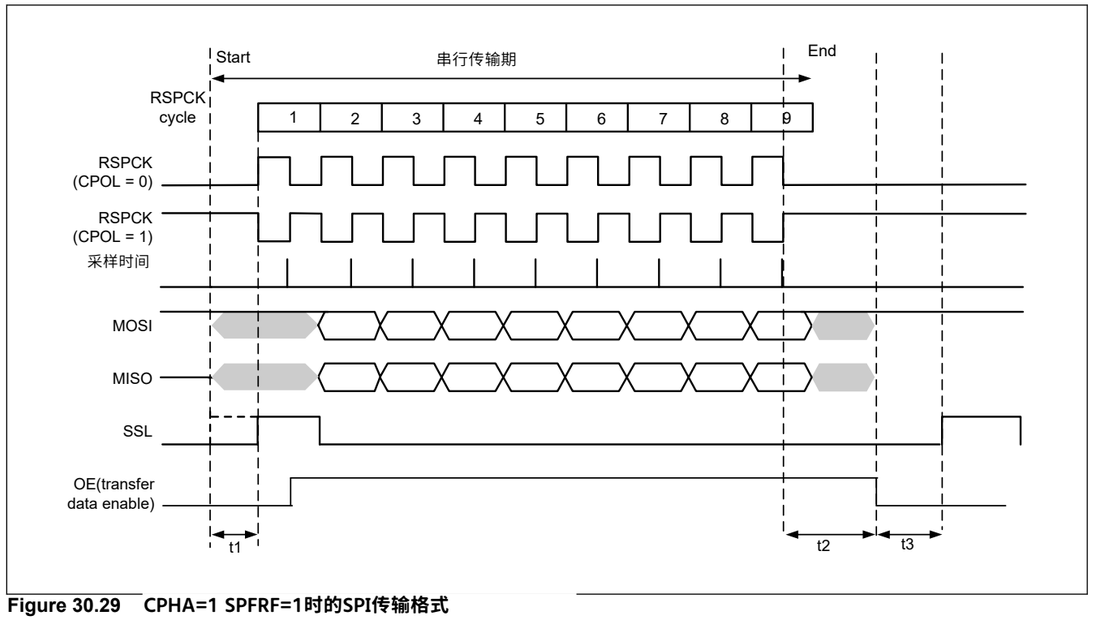


Figure 30.29 CPHA=1 SPFRF=1时的SPI传输格式

30.3.6 通讯操作模式

发送–接收串行通信、仅发送操作和仅接收操作通过设置选择
RSPI控制寄存器(SPCR)的通信模式选择位(TXMD[1:0])。

图30.30、图30.31、图30.32中描述的SPDR访问显示了对RSPI数据寄存器(SPDR)的访问。W表示写周期。

30.3.6.1 Transmit-Receive Serial Communication (TXMD[1:0] = 00b)

Figure 30.30 shows an example of operation when the communication mode select bit (TXMD[1:0]) in the RSPI control register (SPCR) is set to 00b. In the example in Figure 30.30, the RSPI performs 8-bit data serial transfer with the settings of RTRG = FIFO stage - 1, TTRG = 0 in the RSPI data control register 2 (SPDCR2), CPHA in the RSPI command register (SPCMDm) = 1, and CPOL in SPCMD = 0. Numbers under the RSPCK waveform show the number of RSPCK cycles (number of transfer bits).

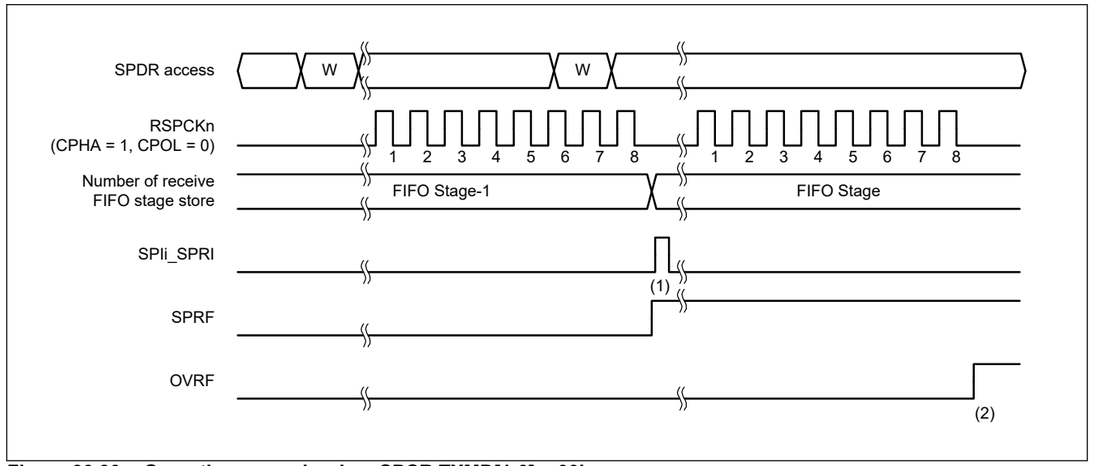


Figure 30.30 Operation example when SPCR.TXMD[1:0] = 00b

The operation of the flags at timings (1) and (2) in Figure 30.30 is as follows:

1. When serial transfer ends while the number of SPDR receive buffer store matches the number of frames set in SPDCR2.RTRG, the SPI generates a receive buffer full interrupt request (SPIi_SPRI), the SPI sets the SPSR.SPRF flag to 1, and copies the received data in the shift register to the receive buffer.
2. When serial transfer ends with data for the number of FIFO stages stored in the SPDR receive buffer, the SPI sets the SPSR.OVRF flag to 1, and discards the received data in the shift register. For details about the operation of the SPSR.OVRF flag, see section 30.3.10.1. Overrun errors.

In Transmit-Receive serial communication (TXMD[1:0] = 00b), transmit data is transmitted and receive data is received. Therefore, the SPRF flag and the OVRF flag are set to 1 at timings (1) and (2) respectively.

30.3.6.2 Transmit-Only Serial Communications (TXMD[1:0] = 01b)

Figure 30.31 shows an example of operation when the communication mode select bit (TXMD[1:0]) in the SPI control register (SPCR) is set to 01b. In this example, the SPI performs an 8-bit serial transfer when the SPDCR2.TTRG is 0, the SPDCR2.RTRG is 0, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

30.3.6.1 发送-接收串行通信（TXMD[1:0]=00b）

图30.30显示了将RSPI控制寄存器(SPCR)中的通信模式选择位(TXMD[1:0])设置为00b时的操作示例。在图30.30的示例中，RSPI执行8位数据串行传输，设置RTRG=FIFO阶段1，RSPI数据控制寄存器2(SPDCR2)中的TTRG=0，RSPI命令寄存器(SPCMDm)中的CPHA=1，SPCMD中的CPOL=0。RSPCK波形下的数字表示RSPCK周期数（传输位数）。

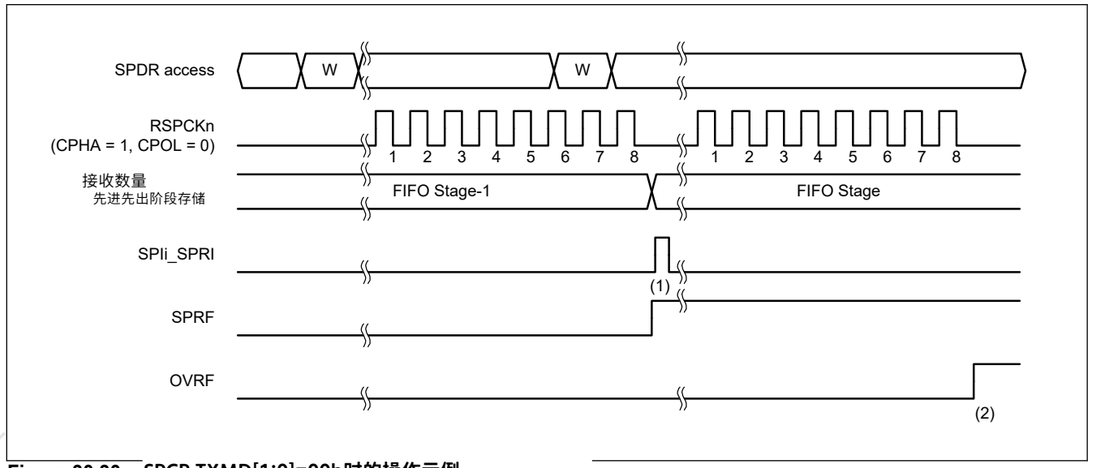


Figure 30.30 SPCR.TXMD[1:0]=00b时的操作示例

图30.30中时间(1)和(2)的标志操作如下：

1.当串行传输结束，而SPDR接收缓冲存储的数量与设置的帧数匹配时
SPDCR2.RTRG，SPI产生接收缓冲区满中断请求（SPIi_SPRI），SPI将SPSR.SPRF标志置1，并将接收到的移位寄存器中的数据复制到接收缓冲区。

2.当串行传输以存储在SPDR接收缓冲区中的FIFO级数的数据结束时，SPI将SPSR.OVRF标志设置为1，并丢弃移位寄存器中的接收数据。有关操作的详细信息
SPSR.OVRF标志，参见第30.3.10.1节。溢出错误。

在发送-接收串行通信(TXMD[1:0]=00b)中，发送数据并接收接收数据。
因此，SPRF标志和OVRF标志分别在时间(1)和(2)被设置为1。

30.3.6.2 仅发送串行通信（TXMD[1:0]=01b）

图30.31显示了当SPI控制寄存器(SPCR)中的通信模式选择位(TXMD[1:0])设置为01b时的操作示例。在本例中，当SPDCR2.TTRG为0、SPDCR2.RTRG为0、SPCMDm.CPHA位为1、SPCMDm.CPOL位为0时，SPI执行8位串行传输。为RSPCKn给出的数字波形中的表示RSPCK周期数，如传输比特数。

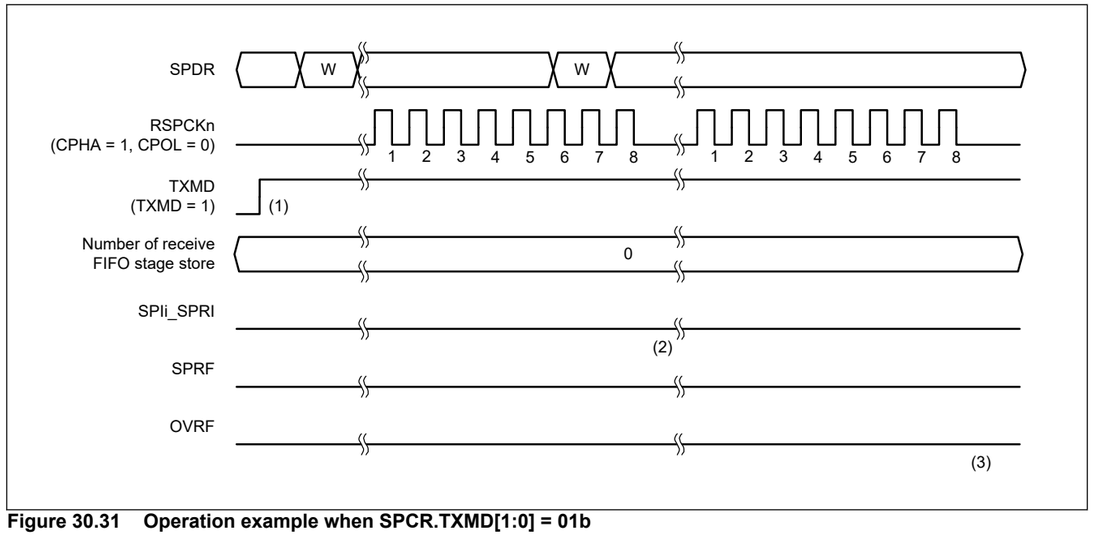


Figure 30.31 Operation example when SPCR.TXMD[1:0] = 01b

The operation of the flags at timings (1) to (3) in Figure 30.31 is as follows:

1. Make sure there is no data left in the receive buffer (the SPSR.SPRF flag is 0) and the SPSR.OVRF flag is 0 before entering transmit-only mode (SPCR.TXMD[1:0] = 01b).
2. When a serial transfer ends without receiving data in the receiving FIFO of SPDR, if the transmit-only mode is selected (SPCR.TXMD[1:0] = 01b), the SPSR.SPRF flag retains the value of 0, and the SPI does not copy the data in the shift register to the receive buffer.
3. Because the receive buffer of SPDR does not hold data that was received in the previous serial transfer, even when a serial transfer ends, the SPSR.OVRF flag retains the value of 0, and the data in the shift register is not copied to the receive buffer.

In transmit-only mode (SPCR.TXMD[1:0] = 01b), the SPI transmits data but does not receive data. Therefore, the SPSR.SPRF and SPSR.OVRF flags remain 0 at timings (1) to (3).

30.3.6.3 Receive-Only Serial Communication (TXMD[1:0] = 10b)

Figure 30.32 shows an example of operation when the communication mode select bit (TXMD[1]) in the RSPI control register (SPCR) is set to 1. In the example in Figure 30.32, the SPI performs 8-bit data serial transfer with the settings of TTRG = FIFO stage - 1, RTRG = 0 in the SPI data control register 2 (SPDCR2), CPHA in the SPI command register (SPCMD) = 1, and CPOL in SPCMD = 0. Numbers under the RSPCK waveform show the number of RSPCK cycles (number of transfer bits).

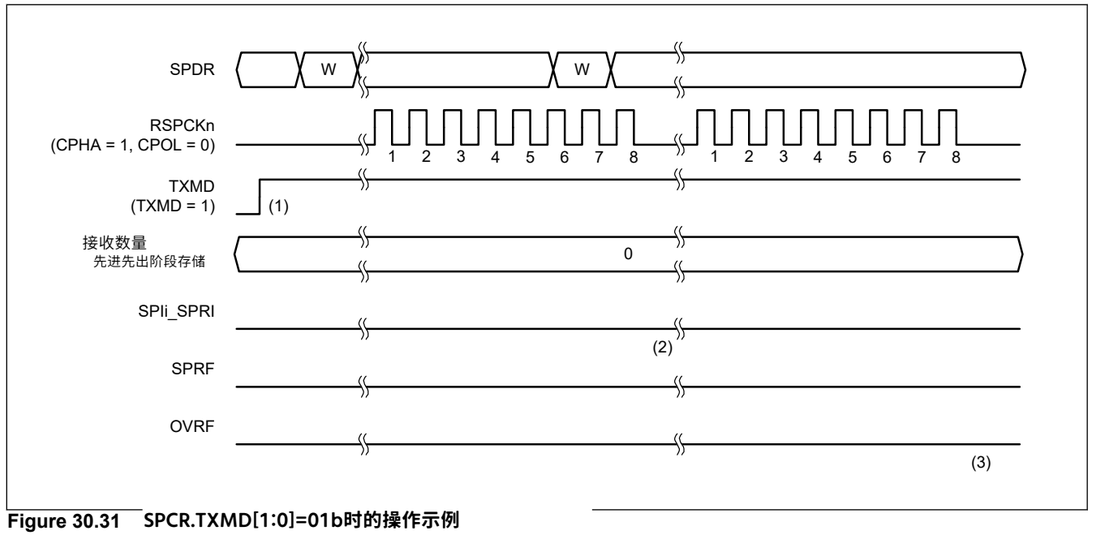


Figure 30.31 SPCR.TXMD[1:0]=01b时的操作示例

图30.31中时间(1)到(3)的标志操作如下：

1.在进入仅发送模式(SPCR.TXMD[1:0]=01b)之前，确保接收缓冲区中没有剩余数据（SPSR.SPRF标志为0）且SPSR.OVRF标志为0。

2.当串行传输结束而在SPDR的接收FIFO中没有接收到数据时，如果选择了仅发送模式（SPCR.TXMD[1:0]=01b），则SPSR.SPRF标志保持值为0，并且SPI不会将移位寄存器中的数据复制到接收缓冲区。

3、因为SPDR的接收缓冲区中没有保存上一次串行传输接收到的数据，所以即使一次串行传输结束，SPSR.OVRF标志保持值0，移位寄存器中的数据不会被复制到接收缓冲区。

在仅发送模式(SPCR.TXMD[1:0]=01b)中，SPI发送数据但不接收数据。因此，SPSR.SPRF和SPSR.OVRF标志在时间(1)到(3)保持为0。

30.3.6.3 仅接收串行通信（TXMD[1:0]=10b）

图30.32显示了将RSPI控制寄存器(SPCR)中的通信模式选择位(TXMD[1])设置为1时的操作示例。在图30.32的示例中，SPI执行8位数据串行传输TTRG=FIFOstage1 RTRG=0intheSPIdatacontrolregister2(SPDCR2) CPHAintheSPIcommandregister(SPCMD)=1 andCPOLinSPCMD=0.RSPCK波形下的数字表示RSPCK周期（传输位数）。

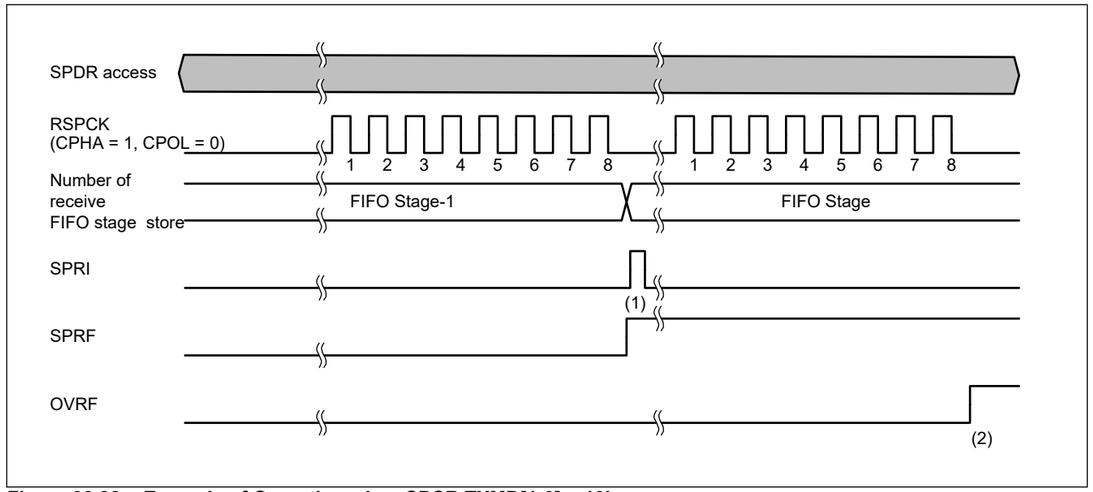


Figure 30.32 Example of Operation when SPCR.TXMD[1:0] = 10b

The following describes operation of flags at timings (1) and (2) in the figure above.

(1) When serial transfer ends while the number of SPDR receive buffer store matches the number of frames set in SPDCR2.RTRG, the SPI generates a receive buffer full interrupt request SPRI (setting the SPSR.SPRF flag to 1) and copies the received data in the shift register to the receive buffer

(2) When serial transfer ends with data for the number of FIFO stages store d in the SPDR receive buffer, the SPI sets the OVRF flag in the SPI status register (SPSR) to 1 and discards the received data in the shift register.

30.3.7 Transmit Buffer Empty and Receive Buffer Full Interrupts

Figure 30.33 show examples of operation of the transmit buffer empty interrupt (SPIi_SPTI) and the receive buffer full interrupt (SPIi_SPRI). The SPDR register accesses shown in these figures indicate the conditions of access to the register, where W denotes a write cycle and R a read cycle. In Figure 30.33, the SPI performs an 8-bit serial transfer when SPCR.TXMD[1:0] bits are 00b, the SPDCR2.TTRG bit is 0, the SPDCR2.RTRG bit is 0, the SPCMDm.CPHA bit is 0, and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

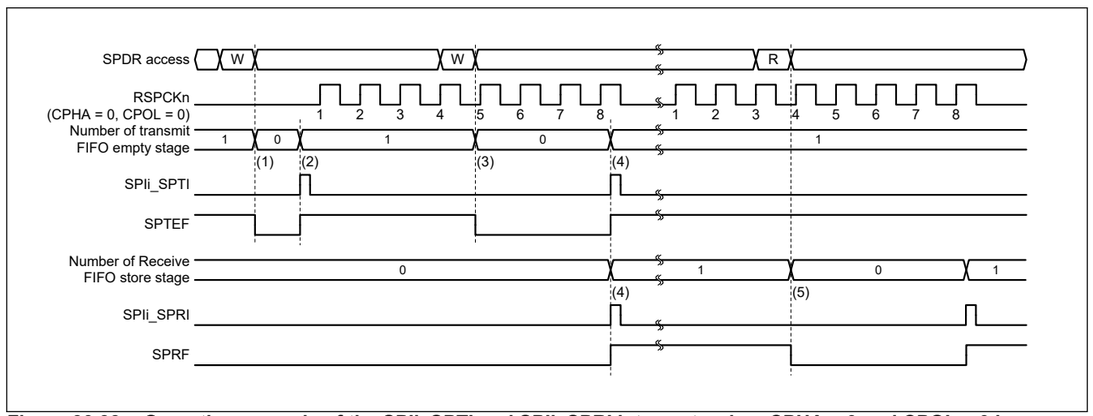


Figure 30.33 Operation example of the SPIi_SPTI and SPIi_SPRI interrupts when CPHA = 0 and CPOL = 0 in master mode

The operation of the SPI at timings (1) to (5) in Figure 30.33 is as follows:

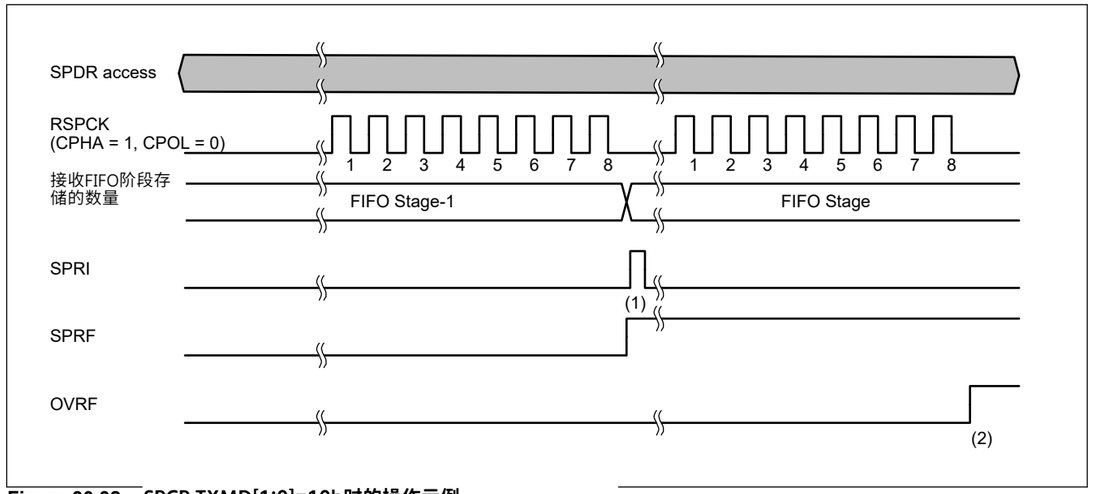


Figure 30.32 SPCR.TXMD[1:0]=10b时的操作示例

下面描述在上图中的时间(1)和(2)的标志的操作。

(1)当串行传输结束而SPDR接收缓冲存储的数量与SPDCR2.RTRG中设置的帧数匹配时，SPI产生一个接收缓冲区满中断请求SPRI（将SPSR.SPRF标志设置为1）并复制接收到的移位寄存器中的数据到接收缓冲区

(2)当串行传输在SPDR接收缓冲区中存储FIFO级数d的数据结束时，SPI将SPI状态寄存器(SPSR)中的OVRF标志设置为1，并丢弃移位寄存器中的接收数据。

30.3.7 发送缓冲区空和接收缓冲区满中断

图30.33显示了发送缓冲区空中断(SPIi_SPTI)和接收缓冲区满中断(SPIi_SPRI)的操作示例。这些图中显示的SPDR寄存器访问表示访问寄存器的条件，其中W表示写周期，R表示读周期。在图30.33中，当SPCR.TXMD[1:0]位为00b、SPDCR2.TTRG位为0、SPDCR2.RTRG位为0、SPCMDm.CPHA位为0时，SPI执行8位串行传输，SPCMDm.CPOL位为0。波形中为RSPCKn给出的数字表示RSPCK周期数，例如传输的位数。

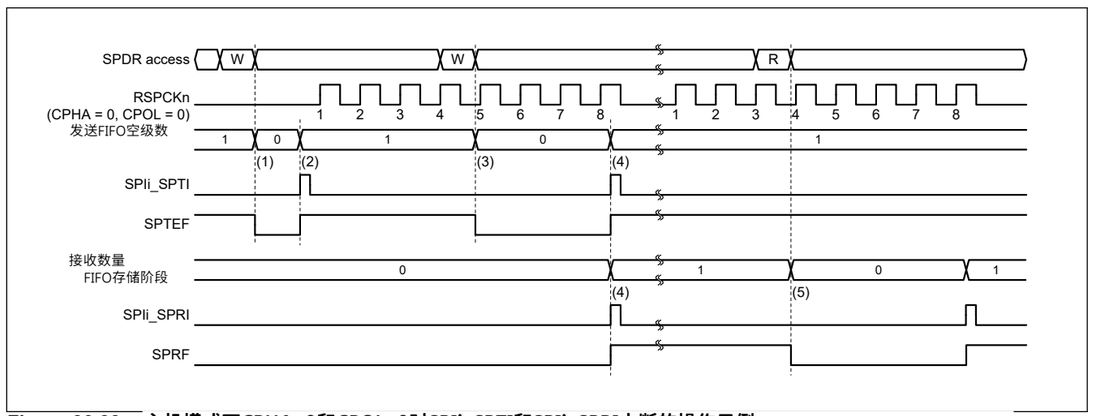


Figure 30.33 主机模式下CPHA=0和CPOL=0时SPIi_SPTI和SPIi_SPRI中断的操作示例

SPI在图30.33中时序(1)到(5)的操作如下：

1. When transmit data is written to SPDR with the transmit buffer of SPDR is before the next transfer data is set, the SPI writes data to the transmit buffer. When transmit data is written to SPDR in one processing routine using DTC / DMAC, the SPSR.SPTEF flag is cleared to 0 at the last access.
2. If the shift register is empty, the SPI copies the data in the transmit buffer to the shift register. At this time, if transmit FIFO empty stage number > TTRG value, then the SPI generates a transmit buffer empty interrupt request (SPIi_SPTI), and sets the SPSR.SPTEF flag to 1. How a serial transfer is started depends on the SPI mode. For details, see section 30.3. Operation, and section 30.3.13. Clock Synchronous Operation.
3. When transmit data is written to SPDR either by the transmit buffer empty interrupt routine, or by the processing of the transmit buffer empty using the SPTEF flag, the SPI writes data to the transmit buffer. When the transmit data is written to SPDR in one processing routine using DTC / DMAC, the SPTEF flag is cleared to 0 at the last access. Because the data being transferred serially is stored in the shift register, the SPI does not copy the data in the transmit buffer to the shift register.
4. When the serial transfer ends with the receive buffer of SPDR > FIFO stage number, the SPI copies the receive data in the shift register to the receive buffer, generates a receive buffer full interrupt request (SPIi_SPRI), and sets the SPRF flag to 1. Because the shift register becomes empty on completion of the serial transfer, if the next transfer data is set in the transmit FIFO before the serial transfer ended, the SPI sets the SPTEF flag to 1 and copies data in the transmit buffer to the shift register. Even when received data is not copied from the shift register to the receive buffer in an overrun error status, on completion of the serial transfer, the SPI determines that the shift register is empty, so data transfer from the transmit buffer to the shift register is enabled.
5. When SPDR is read either by the receive buffer full interrupt routine or processing of the receive buffer full interrupt using the SPRF flag, the receive data can be read. If the received data is read from SPDR in one processing routine using DTC / DMAC, the SPRF flag is cleared to 0 at the last access.

When transmit data is written to the SPDR register while no empty stages in the transmit FIFO, the SPI does not update data in the transmit buffer. When writing to SPDR, always use either a transmit buffer empty interrupt request or check the empty or processing of the transmit buffer empty interrupt using the SPTEF flag. To use a transmit buffer empty interrupt, set the SPTIE bit in SPCR to 1. If the SPI function is disabled (the SPCR.SPE bit is 0), set the SPTIE bit to 0.

When serial transfer ends while data is stored in the receive FIFO for the number of FIFO stages, the SPI does not copy data from the shift register to the receive buffer, and it detects an overrun error (see section 30.3.10. Error Detection). To prevent a receive data overrun error, read the received data using a receive buffer full interrupt request before the next serial transfer ends. To use an SPI receive buffer full interrupt, set the SPCR.SPRIE bit to 1.

Transmission and reception interrupts or the associated IELSRn.IR flags (where n is the interrupt vector number) in the ICU can be used to confirm the states of the transmit and receive buffers.

Similarly, the SPTEF and SPRF flags can be used to confirm the states of the transmit and receive buffers. See section 12, Interrupt Controller Unit (ICU) for the interrupt vector numbers.

30.3.8 Idle Interrupt

The idle interrupt during master mode operation is when the SPCP [2:0] of the RSPI status register (SPSR) becomes 000b (start of sequence control), the IDLNF flag in the RSPI status register (SPSR) is set to 1 and an idle interrupt request is made during master mode operation. An interrupt request is also made by clearing the SPCR.SPE bit to 0.

[In the Motorola-SPI case]

Figure 30.34 shows an example of idle interrupt operation during normal operation.

1.当发送数据写入SPDR时，SPDR的发送缓冲区在下一次传输数据设置之前，SPI将数据写入发送缓冲区。在使用DTCDMAC的一个处理例程中将发送数据写入SPDR时，SPSR.SPTEF标志在最后一次访问时被清除为0。

2.如果移位寄存器为空，SPI将发送缓冲区中的数据复制到移位寄存器中。这时，如果传输FIFO空级数>TTRG值，然后SPI产生一个发送缓冲区空中断请求（SPIi_SPTI），并将SPSR.SPTEF标志设置为1。如何启动串行传输取决于SPI模式。有关详细信息，请参阅第30.3节。操作，以及第30.3.13节。时钟同步操作。

3.当发送数据被发送缓冲区空中断程序写入SPDR时，或者通过使用SPTEF标志处理发送缓冲区空时，SPI将数据写入发送缓冲区。在使用DTCDMAC的一个处理例程中将发送数据写入SPDR时，SPTEF标志在最后一次访问时被清除为0。由于串行传输的数据存储在移位寄存器中，因此SPI不会将发送缓冲区中的数据复制到移位寄存器中。

4.当串行传输以SPDR>FIFO级数的接收缓冲区结束时，SPI将移位寄存器中的接收数据复制到接收缓冲区，产生接收缓冲区满中断请求（SPIi_SPRI），并将SPRF标志设置为1.由于串行传输完成后移位寄存器变为空，如果在串行传输结束前发送FIFO中设置了下一个传输数据，则SPI将SPTEF标志设置为1，并将发送缓冲区中的数据复制到移位登记。即使在溢出错误状态下没有将接收到的数据从移位寄存器复制到接收缓冲区，在串行传输完成时，SPI会确定移位寄存器为空，因此从发送缓冲区到移位寄存器的数据传输是启用。

5.当接收缓冲区满中断程序或接收缓冲区满中断处理读取SPDR时使用SPRF标志，可以读取接收数据。如果在一个使用DTCDMAC的处理例程中从SPDR读取接收到的数据，则SPRF标志在最后一次访问时被清除为0。

当发送数据写入SPDR寄存器且发送FIFO中没有空级时，SPI不会更新发送缓冲区中的数据。写入SPDR时，始终使用发送缓冲区空中断请求或使用SPTEF标志检查发送缓冲区空中断的空或处理。要使用发送缓冲区空中断，请将SPCR中的SPTIE位设置为1。如果禁用SPI功能（SPCR.SPE位为0），请将SPTIE位设置为0。

当串行传输结束而数据存储在接收FIFO中达到FIFO级数时，SPI不会将数据从移位寄存器复制到接收缓冲区，它会检测到溢出错误（参见第30.3.10节。错误检测）.为防止接收数据溢出错误，请在下一次串行传输结束前使用接收缓冲区满中断请求读取接收数据。要使用SPI接收缓冲区满中断，请将SPCR.SPRIE位设置为1。

ICU中的发送和接收中断或相关的IELSRn.IR标志（其中n是中断向量号）可用于确认发送和接收缓冲区的状态。

类似地，SPTEF和SPRF标志可用于确认发送和接收缓冲区的状态。见第12节，用于中断向量编号的中断控制器单元(ICU)。

30.3.8 空闲中断

主机模式操作期间的空闲中断是当RSPI状态寄存器(SPSR)的SPCP[2:0]变为000b（序列控制开始）时，RSPI状态寄存器(SPSR)中的IDLNF标志设置为1，并且空闲中断请求是在主模式操作期间发出的。也可通过将SPCR.SPE位清0来发出中断请求。

[In the Motorola-SPI case]

图30.34显示了正常操作期间的空闲中断操作示例。

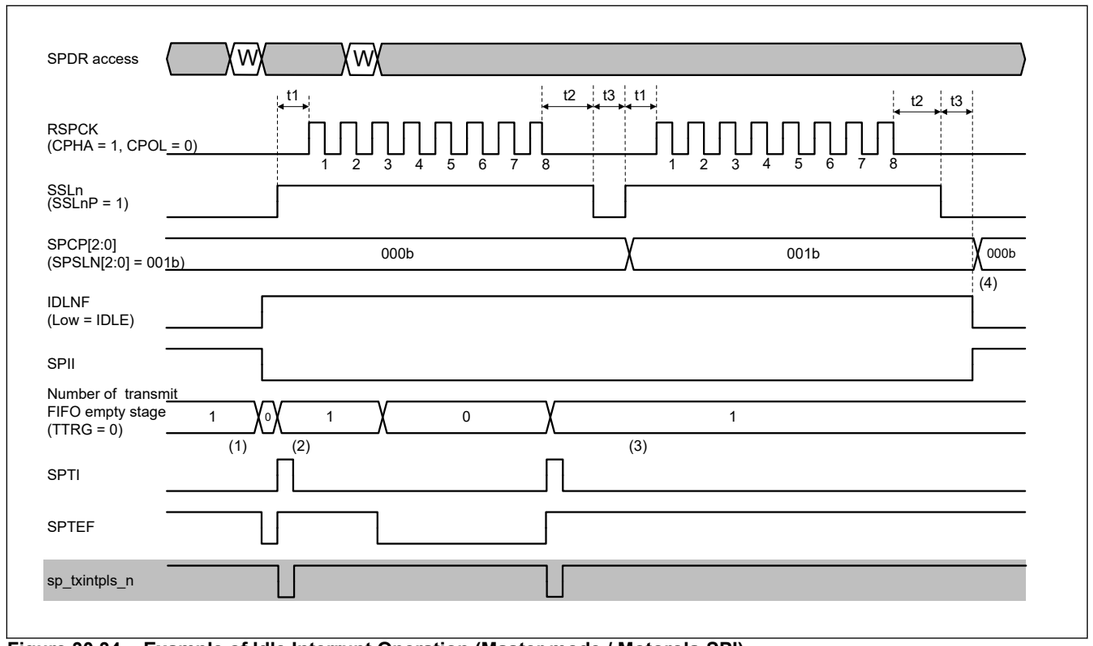


Figure 30.34 Example of Idle Interrupt Operation (Master mode / Motorola-SPI)

1. At the start of transmission, if the next transfer data is not set in the transmission buffer, the IDLNF flag is 0 (IDLE). Writing transmit data makes sets the IDLNF flag to 1 (BUSY). When the SPIIE bit in the RSPI control register (SPCR) is set to 1 before transmit data is written, interrupt processing is required before transmission start. For this reason, set the SPIIE bit to 0 before starting transmission.
2. After transmission has started, the IDLNF flag remains 1 (BUSY) regardless of the transmit buffer state.
3. The SPCP[2:0] bits change the command to the next command the end of t3 cycle. When the next command is not 000b, the IDLNF flag remains unchanged even when the next transmit data has not been written.
4. The IDLNF flag is cleared to 0 (IDLE) the end of t3 cycle because the next command is 000b and the next transmit data is not present. When the SPIIE bit is 1 currently, an SPII interrupt is output.

[In the TI-SSP case]

Figure 30.35 shows an example of idle interrupt operation during normal operation.

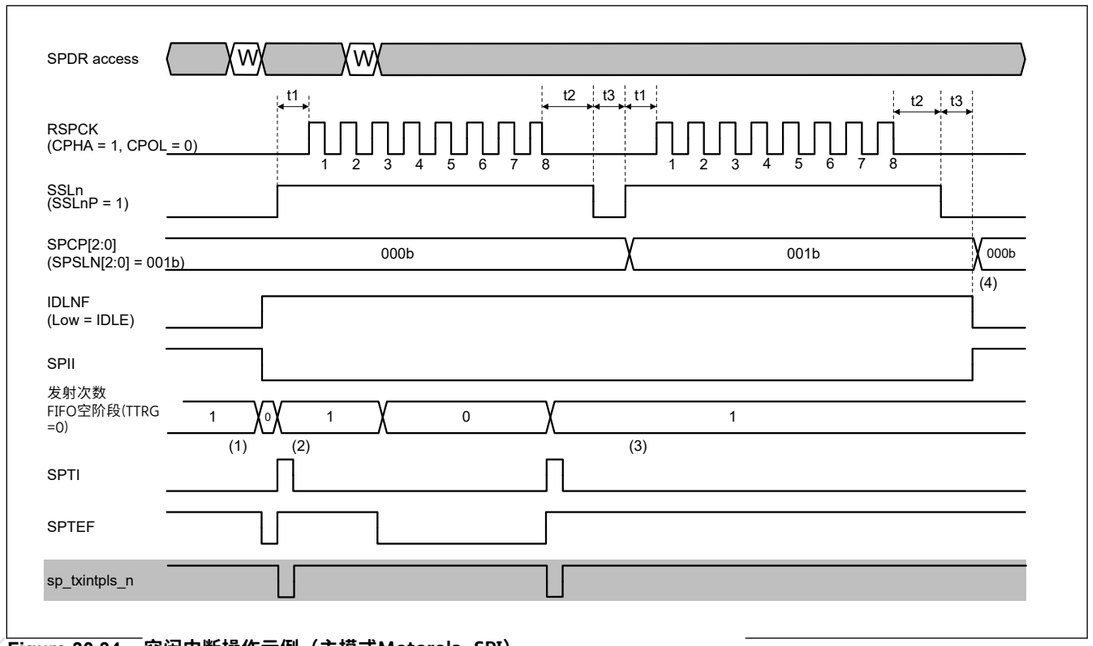


Figure 30.34 空闲中断操作示例（主模式Motorola-SPI）

1.在传输开始时，如果传输缓冲区中没有设置下一个传输数据，则IDLNF标志为0（IDLE）。写入发送数据会使IDLNF标志设置为1(BUSY)。如果在写入发送数据之前将RSPI控制寄存器(SPCR)中的SPIIE位设置为1，则需要在发送开始前进行中断处理。因此，在开始发送之前将SPIIE位设置为0。

2.发送开始后，IDLNF标志保持为1(BUSY)，与发送缓冲区状态无关。

3.SPCP[2:0]位在t3周期结束时将命令更改为下一个命令。当下一个命令不是000b时，即使没有写入下一个发送数据，IDLNF标志也保持不变。

4.IDLNF标志在t3周期结束时被清除为0(IDLE)，因为下一个命令是000b并且下一个发送数据不存在。当前SPIIE位为1时，输出SPII中断。

[In the TI-SSP case]

图30.35显示了正常操作期间的空闲中断操作示例。

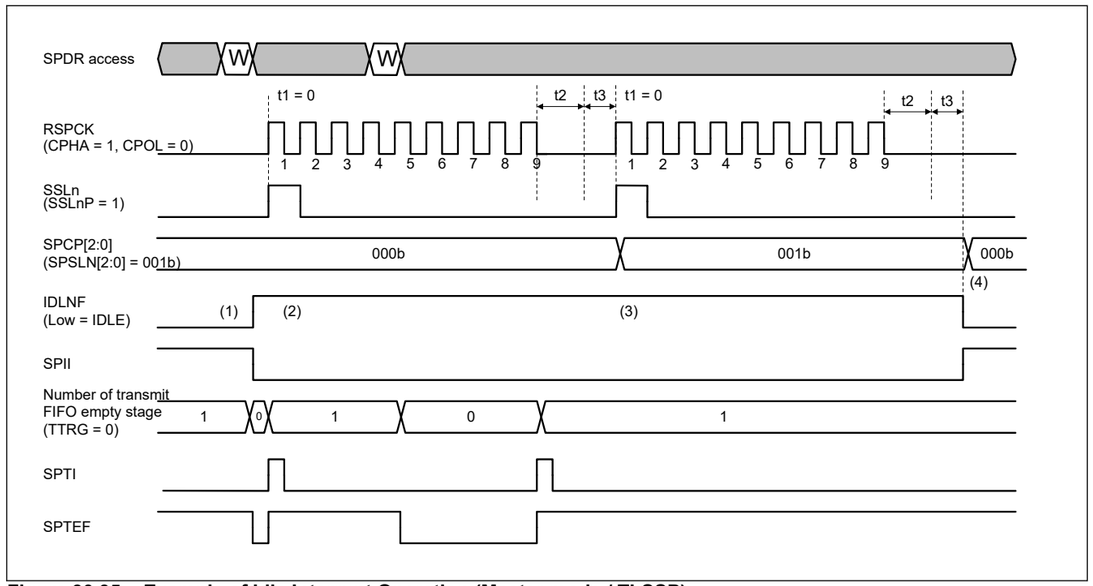


Figure 30.35 Example of Idle Interrupt Operation (Master mode / TI-SSP)

1. At the start of transmission, if the next transfer data is not set in the transmission buffer, the IDLNF flag is 0 (IDLE). Writing transmit data makes sets the IDLNF flag to 1 (BUSY). When the SPIIE bit in the RSPI control register (SPCR) is set to 1 before transmit data is written, interrupt processing is required before transmission start. For this reason, set the SPIIE bit to 0 before starting transmission.
2. After transmission has started, the IDLNF flag remains 1 (BUSY) regardless of the transmit buffer state.
3. The SPCP[2:0] bits change the command to the next command the end of t3 cycle. When the next command is not 000b, the IDLNF flag remains unchanged even when the next transmit data has not been written.
4. The IDLNF flag is cleared to 0 (IDLE) the end of t3 cycle because the next command is 000b and the next transmit data is not present. When the SPIIE bit is 1 currently, an SPII interrupt is output.

30.3.9 Communication End Interrupt

30.3.9.1 Transmit-Receive/Transmit in Master Mode

Refer to the description of the CENDF bit in section 30.2.9. SPSR : SPI Status Register for the setting / clearing conditions of the communication completion flag during Transmit-Receive/Transmit-only in Master Mode.

[In the Motorola-SPI case]

Figure 30.36 shows an example of communication end interrupt operation during transmit-receive/transmit master mode.

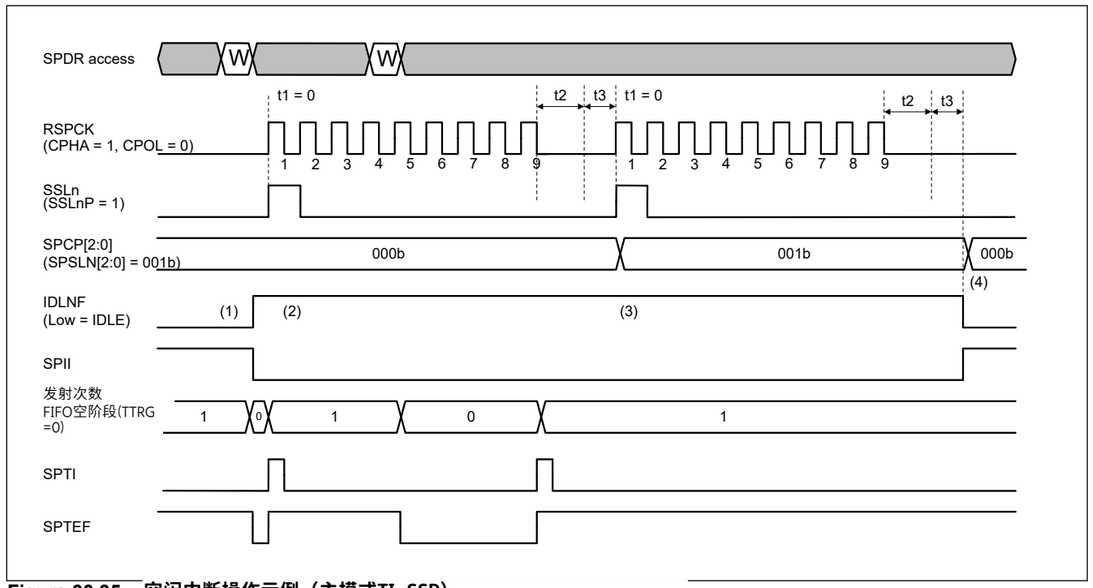


Figure 30.35 空闲中断操作示例（主模式TI-SSP）

1.在传输开始时，如果传输缓冲区中没有设置下一个传输数据，则IDLNF标志为0（IDLE）。
写入发送数据会使IDLNF标志设置为1(BUSY)。如果在写入发送数据之前将RSPI控制寄存器(SPCR)中的SPIIE位设置为1，则需要在发送开始前进行中断处理。因此，在开始发送之前将SPIIE位设置为0。

2.发送开始后，IDLNF标志保持为1(BUSY)，与发送缓冲区状态无关。

3.SPCP[2:0]位在t3周期结束时将命令更改为下一个命令。当下一个命令不是000b时，即使没有写入下一个发送数据，IDLNF标志也保持不变。

4.IDLNF标志在t3周期结束时被清除为0(IDLE)，因为下一个命令是000b并且下一个发送数据不存在。当前SPIIE位为1时，输出SPII中断。

30.3.9 通讯结束中断

30.3.9.1 主控模式下的发送-接收发送

请参阅第30.2.9节中对CENDF位的描述。SPSR:SPI状态寄存器，用于在主模式下发送-接收仅发送期间设置通信完成标志的清除条件。

[In the Motorola-SPI case]

图30.36显示了发送-接收发送主机模式下的通信结束中断操作示例。

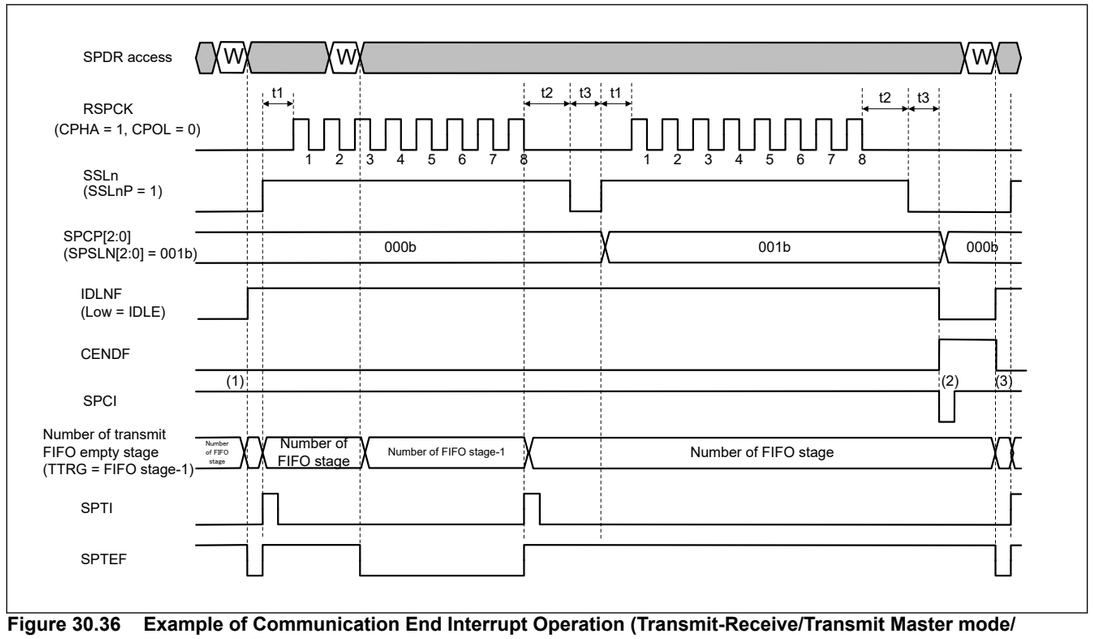


Figure 30.36 Example of Communication End Interrupt Operation (Transmit-Receive/Transmit Master mode/ Motorola-SPI)

1. The CENDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the end of t3 cycle, because the next command is 000b and there is no next transmit data, and then the SPCI interrupt output when the CENDIE bit is 1.
3. The CENDF flag is cleared when the next transmission data is written to the transmit buffer (SPTX). Or when 1 is written to the SPSRC.CENDFC bit, then the CENDF flag is 0.

[In the TI-SSP case]

Figure 30.37 shows an example of communication end interrupt operation during transmit-receive/transmit-only master mode.

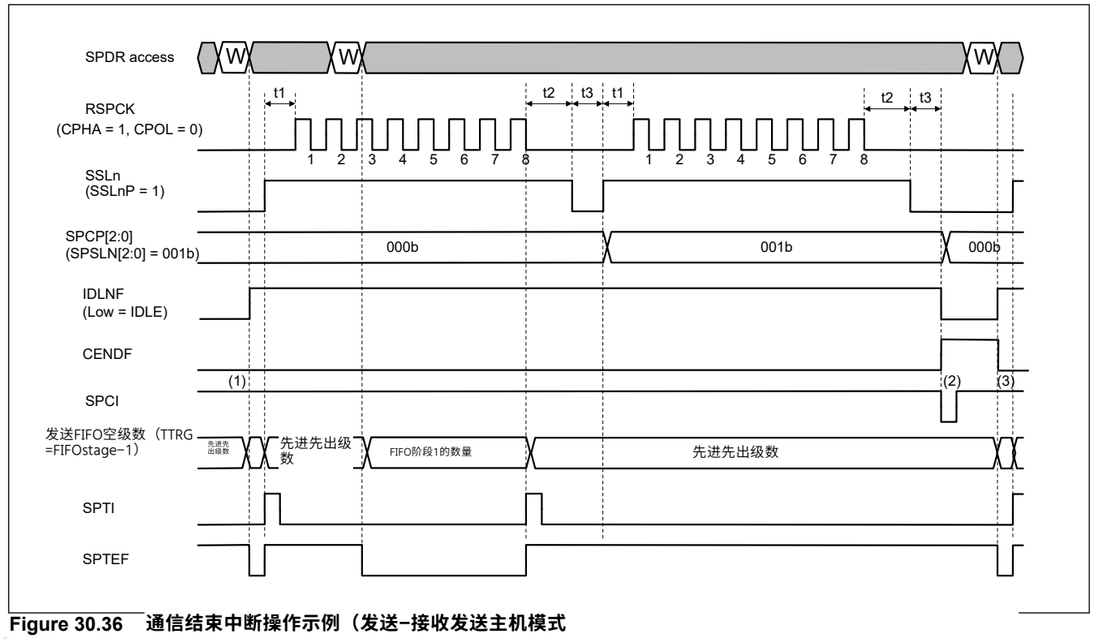


Figure 30.36 通信结束中断操作示例（发送-接收发送主机模式 Motorola-SPI)

1、通信开始前CENDF标志为0，SPCI的电平为1，在通信过程中一直保持。

2.CENDF标志在t3周期结束时为1（通信结束），因为下一条命令为000b，没有下一条发送数据，当CENDIE位为1时SPCI中断输出。

3.CENDF标志在下一个发送数据写入发送缓冲区（SPTX）时被清除。或者当向SPSRC.CENDFC位写入1时，CENDF标志为0。

[In the TI-SSP case]

图30.37显示了在发送-接收仅发送主机模式期间通信结束中断操作的示例。

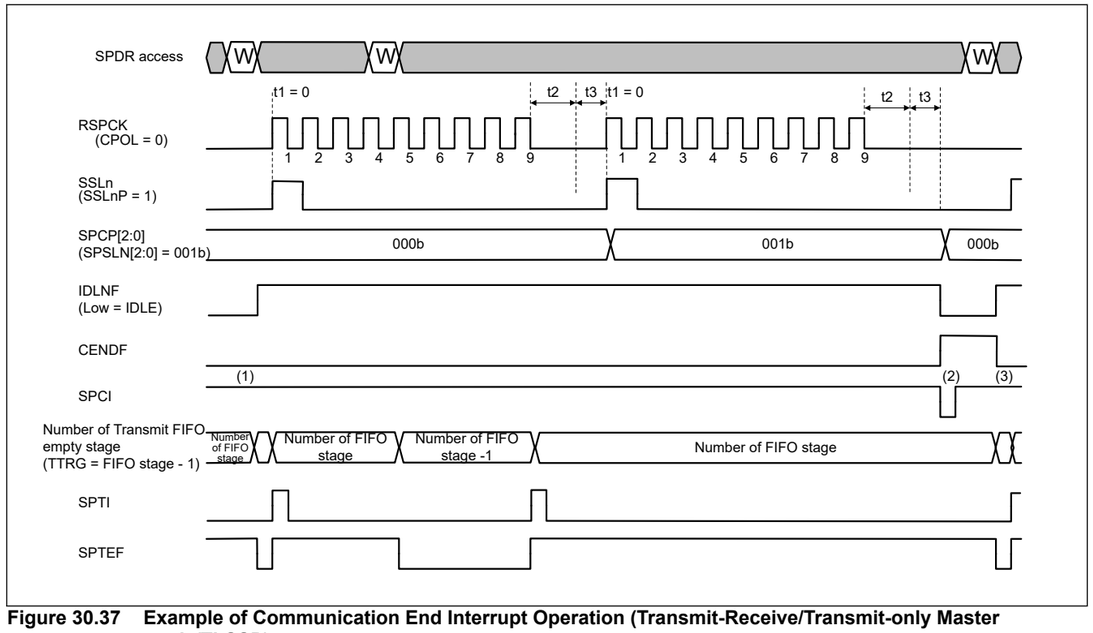


Figure 30.37 Example of Communication End Interrupt Operation (Transmit-Receive/Transmit-only Master mode/TI-SSP)

1. The CENDF flag is 0 and the level of SPCI is 1 before communication start. And these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the end of t3 cycle, because the next command is 000b and there is no next transmit data. And then the SPCI interrupt outputs with PCLK 1 cycle width if the CENDIE bit is 1.
3. The CENDF flag is cleared when the next transmission data is written to the transmit buffer (SPTX). Or when 1 is written to the SPSRC.CENDFC bit, then the CENDF flag is 0.

In slave mode operation, the output timing of the communication end interrupt is deferent due to the value of the SPCR.SPMS bit (RSPI mode select bit), and the clear timing of the communication end interrupt is deferent due to the communication mode (transmit-receive or transmit-only or receive-only).

30.3.9.2 Receive-only in Master Mode

Refer to the description of the CENDF bit in section 30.2.9. SPSR : SPI Status Register for the setting / clearing conditions of the communication completion flag during Receive-only in Master Mode.

Figure 30.38 shows an example of communication end interrupt operation during receive-only master mode at RMFM[4:0] = 0.

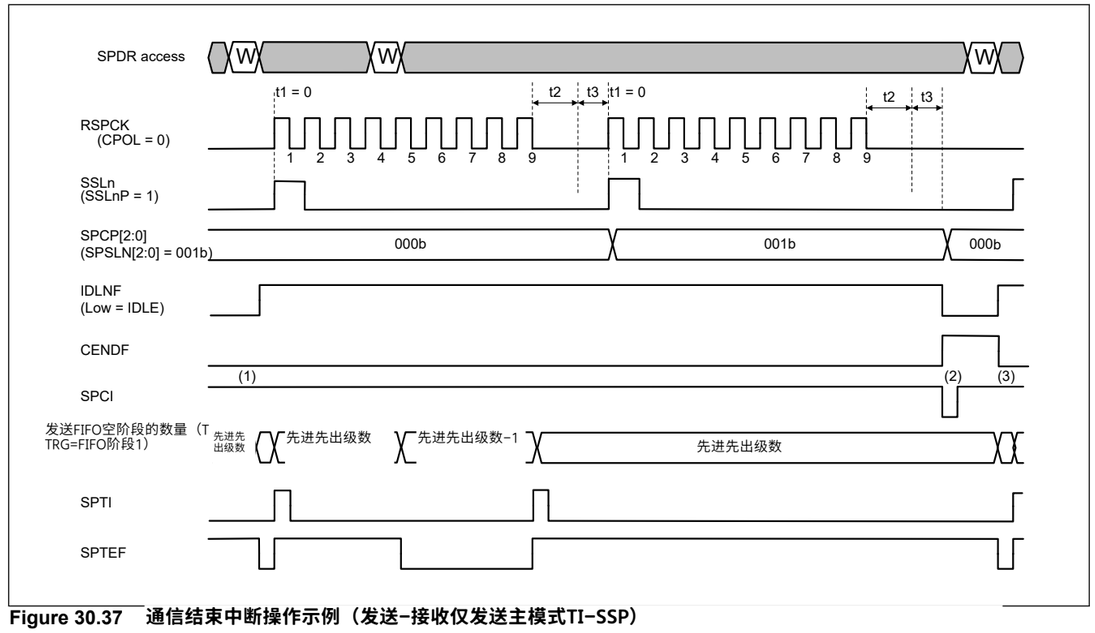


Figure 30.37 通信结束中断操作示例（发送-接收仅发送主模式TI-SSP）

1.CENDF标志位为0，SPCI的电平在通信开始前为1。而这些在交流过程中一直保持着。

2.CENDF标志在t3周期结束时为1（通信结束），因为下一个命令是000b，并且没有下一个传输数据。如果CENDIE位为1，则SPCI中断以PCLK1个周期宽度输出。

3.CENDF标志在下一个发送数据写入发送缓冲区（SPTX）时被清除。或者当向SPSRC.CENDFC位写入1时，CENDF标志为0。

在从模式操作中，通信结束中断的输出时序是不同的，因为SPCR.SPMS位（RSPI模式选择位），通信结束中断的清除时序因通信模式（发送-接收或仅发送或仅接收）而异。

30.3.9.2 主控模式下仅接收

请参阅第30.2.9节中对CENDF位的描述。SPSR:SPI状态寄存器，用于在主模式下仅接收期间设置通信完成标志的清除条件。

图30.38显示了RMFM[4:0]=0时仅接收主机模式下的通信结束中断操作示例。

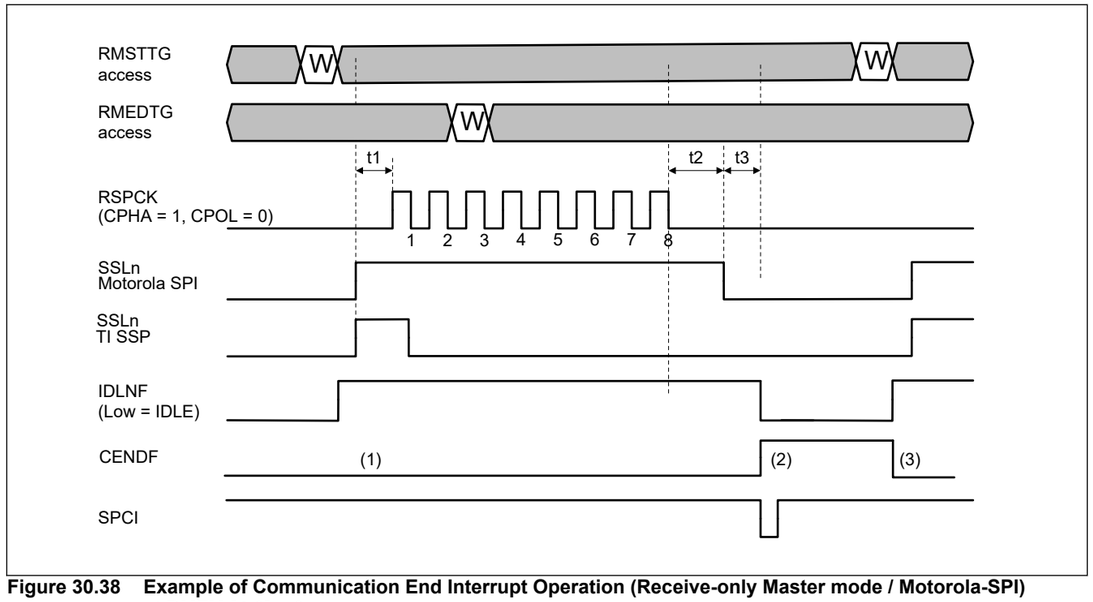


Figure 30.38 Example of Communication End Interrupt Operation (Receive-only Master mode / Motorola-SPI) at RMFM [4:0] = 0

1. The CENDF flag is 0 and the level of SPCI is 1 before communication start. And these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the end of t3 cycle, by writing 1 to RMEDTG during the communication frame. And then the SPCI interrupt outputs with PCLK 1 cycle width if the CENDIE bit is 1.
3. The CENDF flag is cleared when writing 1 to RMSTTG. Or when 1 is written to the SPSRC.CENDFC bit, then the CENDF flag is 0.

Figure 30.39 shows an example of communication end interrupt operation during receive-only master mode at RMFM[4:0] ≠ 0.

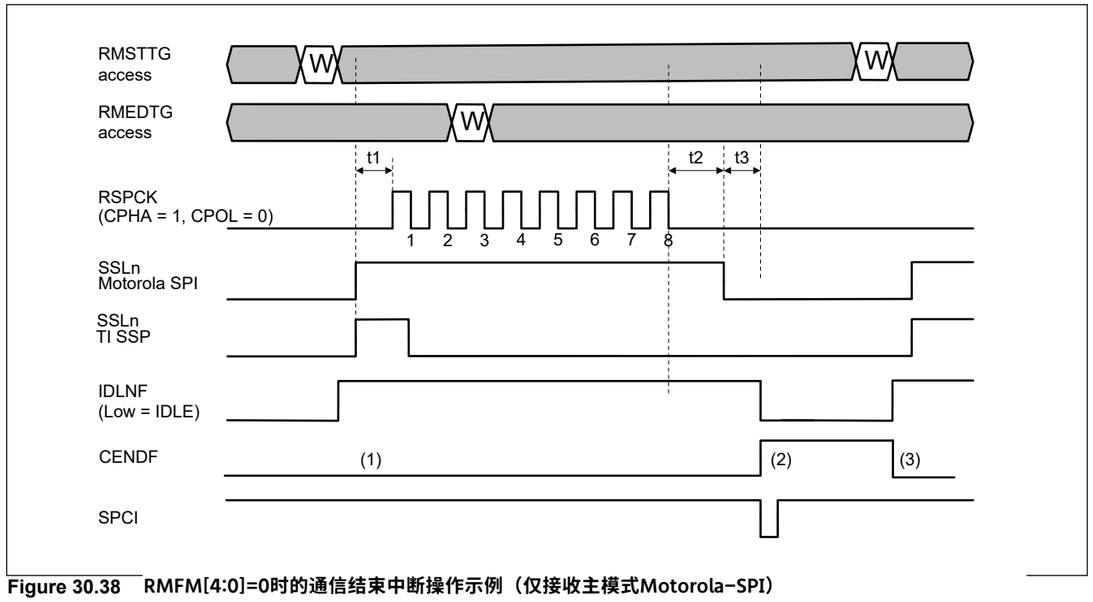


Figure 30.38 RMFM[4:0]=0时的通信结束中断操作示例（仅接收主模式Motorola-SPI）

1.CENDF标志位为0，SPCI的电平在通信开始前为1。而这些在交流过程中一直保持着。

2.通过在通信帧期间向RMEDTG写入1，CENDF标志将在t3周期结束时为1（通信结束）。如果CENDIE位为1，则SPCI中断以PCLK1个周期宽度输出。

3.向RMSTTG写入1时清除CENDF标志。或者当向SPSRC.CENDFC位写入1时，CENDF标志为0。

图30.39显示了RMFM[4:0]≠0时仅接收主机模式期间的通信结束中断操作示例。

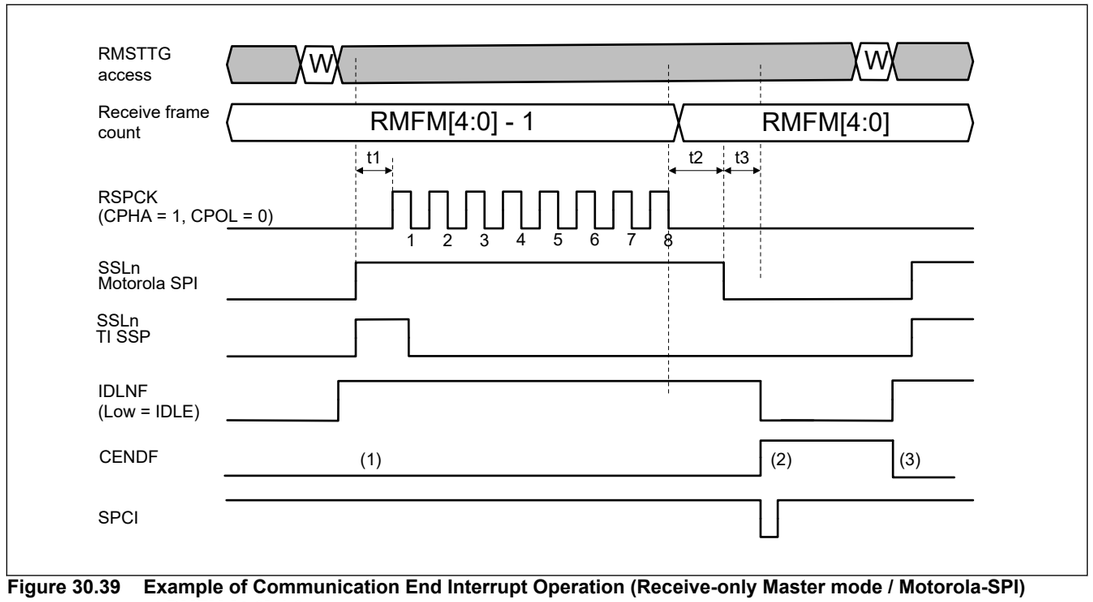


Figure 30.39 Example of Communication End Interrupt Operation (Receive-only Master mode / Motorola-SPI) at RMFM [4:0] ≠ 0

1. The CENDF flag is 0 and the level of SPCI is 1 before communication start. And these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the end of t3 cycle, after receiving the number of frames set by RMFM [4:0]. And then the SPCI interrupt outputs with PCLK 1 cycle width if the CENDIE bit is 1.
3. The CENDF flag is cleared when writing 1 to RMSTTG. Or when 1 is written to the SPSRC.CENDFC bit, then the CENDF flag is 0.

30.3.9.3 Transmit-Receive/Transmit in Slave Mode on SPI Operation (4-wire)

Refer to the description of the CENDF bit in section 30.2.9. SPSR : SPI Status Register for the setting / clearing conditions of the communication completion flag during Transmit-Receive/Transmit-only in Slave Mode (4-wire).

[In the Motorola-SPI case]

Figure 30.40 shows an example of communication end interrupt operation during transmit-receive/transmit slave mode on SPI operation.

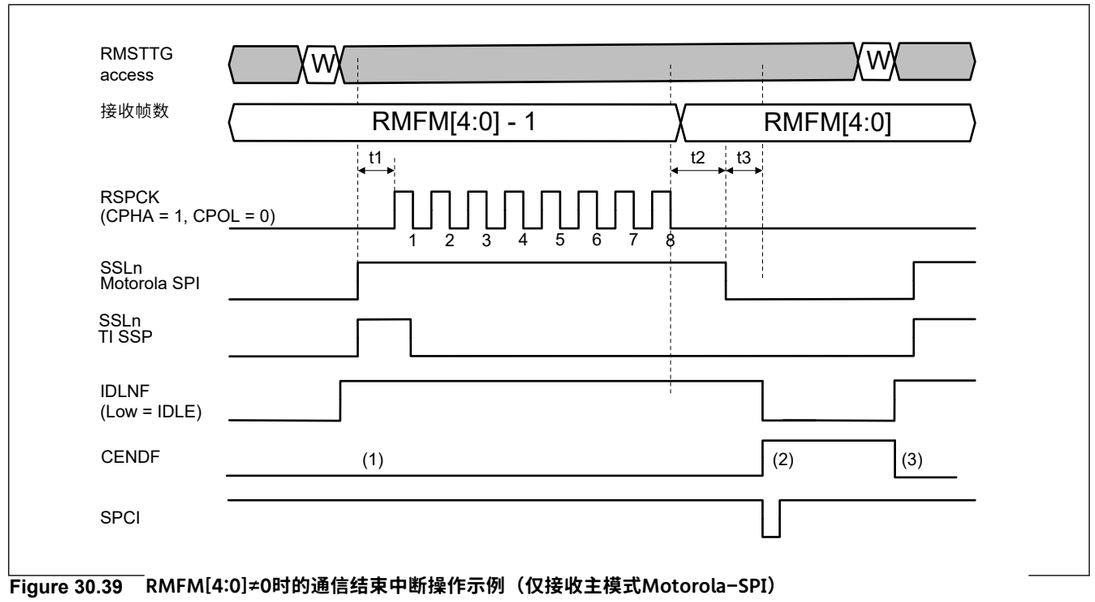


Figure 30.39 RMFM[4:0]≠0时的通信结束中断操作示例（仅接收主模式Motorola-SPI）

1.CENDF标志位为0，SPCI的电平在通信开始前为1。而这些在交流过程中一直保持着。

2.CENDF标志将在t3周期结束时为1（通信结束），接收到RMFM[4:0]设置的帧数。如果CENDIE位为1，则SPCI中断以PCLK1个周期宽度输出。

3.向RMSTTG写入1时清除CENDF标志。或者当向SPSRC.CENDFC位写入1时，CENDF标志为0。

30.3.9.3 SPI操作（4线）从模式下的发送-接收发送

请参阅第30.2.9节中对CENDF位的描述。SPSR:SPI状态寄存器，用于在从模式（4线）下发送-接收仅发送期间设置通信完成标志的清除条件。

[In the Motorola-SPI case]

图30.40显示了在发送-接收发送从模式开启期间的通信结束中断操作示例
SPI操作。

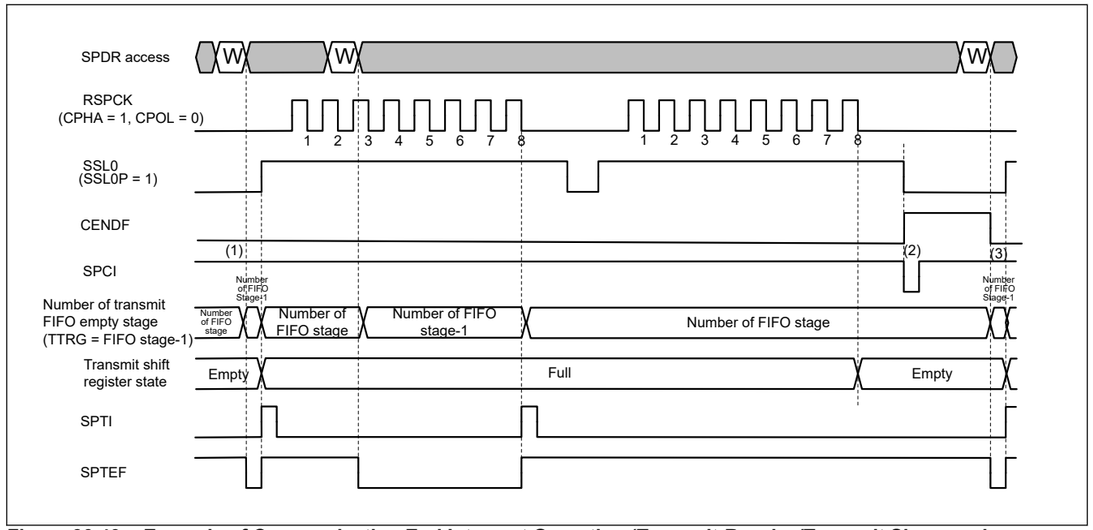


Figure 30.40 Example of Communication End Interrupt Operation (Transmit-Receive/Transmit Slave mode on SPI Operation/Motorola-SPI)

1. The CENDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the timing of SSL0 negate, when the next transfer data is not set in the transmit FIFO and the transmit shift register is empty. And then the SPCI interrupt outputs with PCLK 1 cycle width if the CENDIE bit is 1.
3. The CENDF flag is cleared when the next transmission data is written to the transmit buffer (SPTX). Or when 1 is written to the SPSRC.CENDFC bit, then the CENDF flag is 0.

[In the TI-SSP case]

Figure 30.41 shows an example of communication end interrupt operation during transmit-receive/transmit-only slave mode on SPI operation.

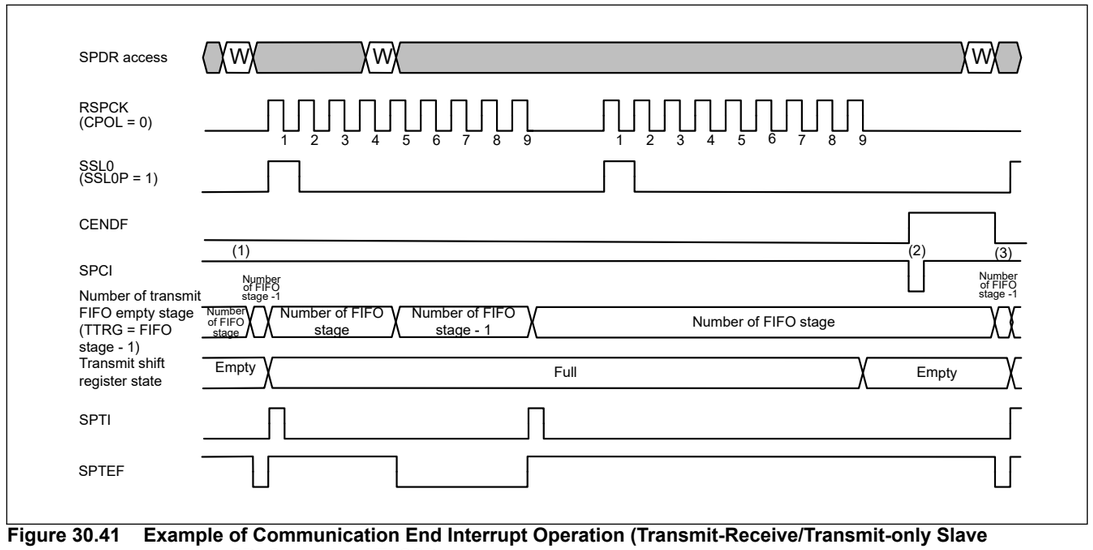


Figure 30.41 Example of Communication End Interrupt Operation (Transmit-Receive/Transmit-only Slave mode on SPI Operation / TI-SSP)

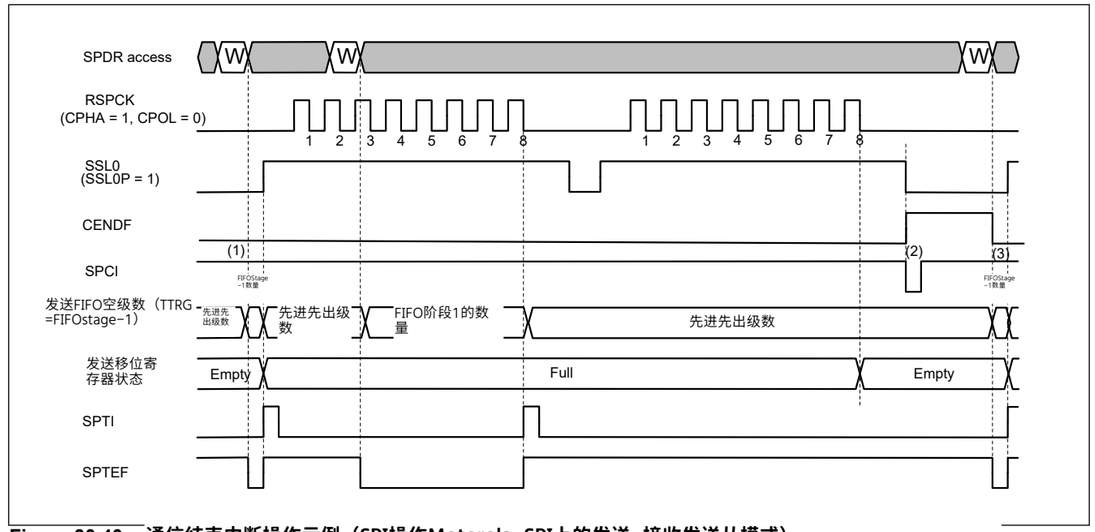


Figure 30.40 通信结束中断操作示例（SPI操作Motorola-SPI上的发送-接收发送从模式）

1、通信开始前CENDF标志为0，SPCI的电平为1，在通信过程中一直保持。

2.CENDF标志将在SSL0否定时为1（通信结束），此时发送FIFO中未设置下一个传输数据且发送移位寄存器为空。如果CENDIE位为1，则SPCI中断以PCLK1个周期宽度输出。

3.CENDF标志在下一个发送数据写入发送缓冲区（SPTX）时被清除。或者当向SPSRC.CENDFC位写入1时，CENDF标志为0。

[In the TI-SSP case]

图30.41显示了在SPI操作上的发送-接收仅发送从机模式期间的通信结束中断操作示例。

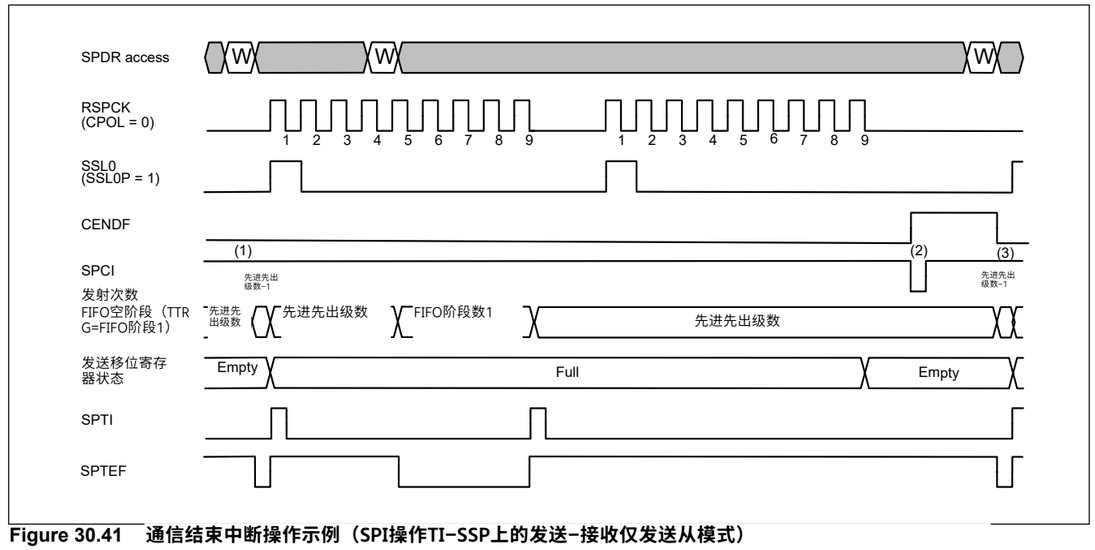


Figure 30.41 通信结束中断操作示例（SPI操作TI-SSP上的发送-接收仅发送从模式）

1. The CENDF flag is 0 and the level of SPCI is 1 before communication start. And these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the RSPCK last data bit sampling, when the next transfer data is not set in the transmit FIFO and the transmit shift register is empty. And then the SPCI interrupt outputs with PCLK 1 cycle width if the CENDIE bit is 1.
3. The CENDF flag is cleared when the next transmission data is written to the transmit buffer (SPTX). Or when 1 is written to the SPSRC.CENDFC bit, then the CENDF flag is 0.

30.3.9.4 Receive Only in Slave Mode on SPI Operation (4-wire)

Refer to the description of the CENDF bit in section 30.2.9. SPSR : SPI Status Register for the setting / clearing conditions of the communication completion flag during Receive-only in Slave Mode (4-wire).

[In the Motorola-SPI case]

Figure 30.42 shows an example of communication end interrupt operation during receive only slave mode on SPI operation (4-wire).

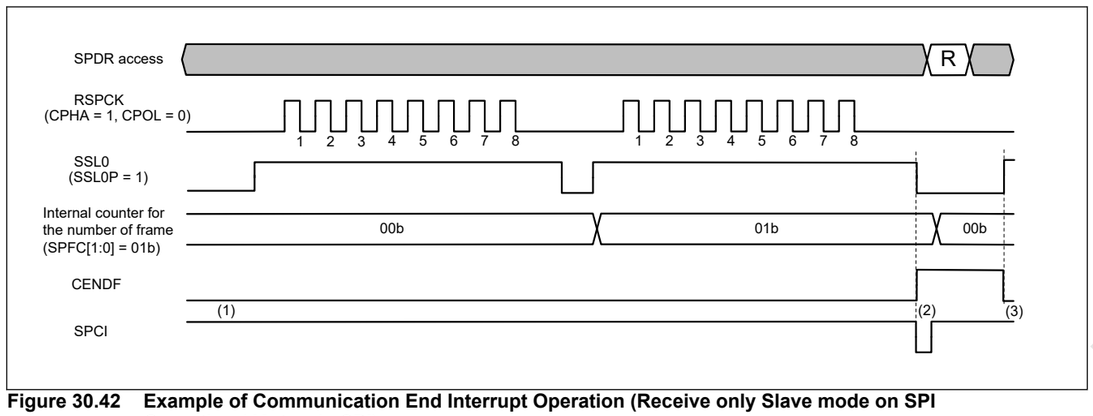


Figure 30.42 Example of Communication End Interrupt Operation (Receive only Slave mode on SPI Operation / Motorola-SPI)

1. The CENDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.
2. After store the frames for the RSPI data control register (SPDCR) SPFC set value in the receive buffer, the CENDF flag becomes 1 (communication completed) at the timing of SSL0 negation. And then the SPCI interrupt outputs with PCLK 1 cycle width if the CENDIE bit is 1.
3. The CENDF flag is cleared at the SSL0 assert when the next transmission start. Or when 1 is written to the SPSRC.CENDFC bit, then the CENDF flag is 0.

[In the TI-SSP case]

Figure 30.43 shows an example of communication end interrupt operation during receive only slave mode on SPI operation (4-wire).

1.CENDF标志位为0，SPCI的电平在通信开始前为1。而这些在交流过程中一直保持着。

2.当发送FIFO中没有设置下一个传输数据且发送移位寄存器为空时，CENDF标志将在RSPCK最后一个数据位采样时为1（通信结束）。如果CENDIE位为1，则SPCI中断以PCLK1个周期宽度输出。

3.CENDF标志在下一个发送数据写入发送缓冲区（SPTX）时被清除。或者当向SPSRC.CENDFC位写入1时，CENDF标志为0。

30.3.9.4 SPI操作时仅在从模式下接收（4线）

请参阅第30.2.9节中对CENDF位的描述。SPSR：SPI状态寄存器，用于在从模式（4线）仅接收期间设置通信完成标志的清除条件。

[In the Motorola-SPI case]

图30.42显示了SPI操作（4线）上仅接收从机模式期间的通信结束中断操作示例。

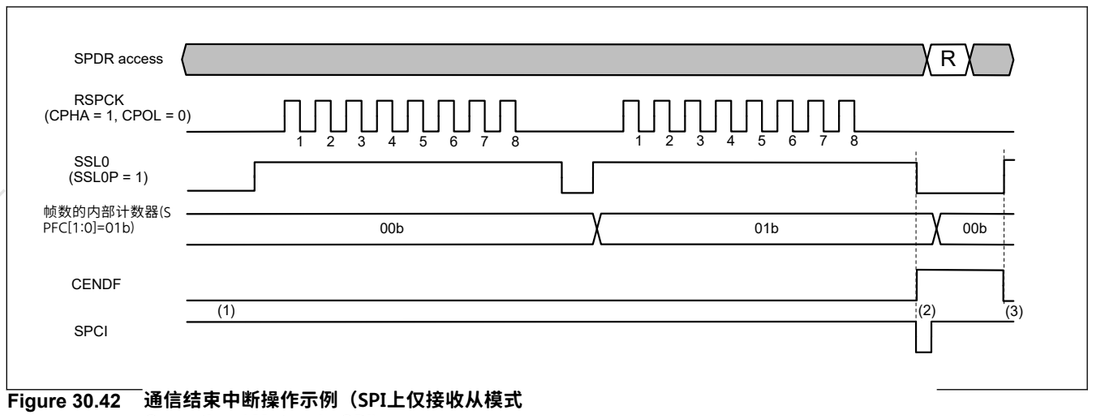


Figure 30.42 通信结束中断操作示例（SPI上仅接收从模式 Operation / Motorola-SPI)

1、通信开始前CENDF标志为0，SPCI的电平为1，在通信过程中一直保持。

2.将RSPI数据控制寄存器(SPDCR)SPFC设置值的帧存储在接收缓冲器中后，CENDF标志在SSL0否定时变为1（通信完成）。如果CENDIE位为1，则SPCI中断以PCLK1个周期宽度输出。

3.CENDF标志在下一次传输开始时在SSL0断言处被清除。或者当向SPSRC.CENDFC位写入1时，CENDF标志为0。

[In the TI-SSP case]

图30.43显示了SPI操作（4线）上仅接收从机模式期间的通信结束中断操作示例。

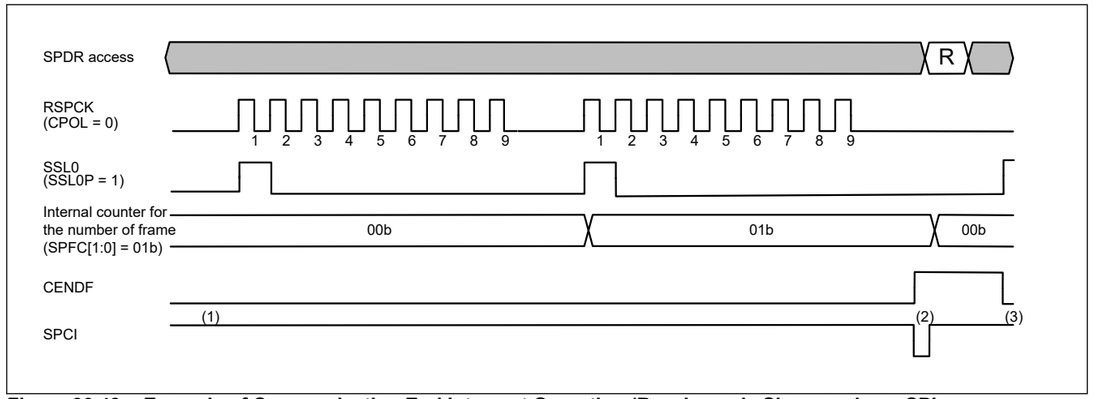


Figure 30.43 Example of Communication End Interrupt Operation (Receive-only Slave mode on SPI Operation / TI-SSP)

1. The CENDF flag is 0 and the level of SPCI is 1 before communication start. And these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the RSPCK last data bit sampling, when the last frame transmission ends. And then the SPCI interrupt outputs with PCLK 1 cycle width if the CENDIE bit is 1.
3. The CENDF flag is cleared at the SSL0 assert when the next transmission start. Or when 1 is written to the SPSRC.CENDFC bit, then the CENDF flag is 0.

30.3.9.5 Transmit-Receive/Transmit in Slave Mode on Clock Synchronous Operation (3-wire)

Refer to the description of the CENDF bit in section 30.2.9. SPSR : SPI Status Register for the setting / clearing conditions of the communication completion flag during Transmit-Receive/Transmit-only in Slave Mode on Clock Synchronous (3-wire).

Figure 30.44 shows an example of communication end interrupt operation during transmit-receive/transmit slave mode on clock synchronous operation (3-wire).

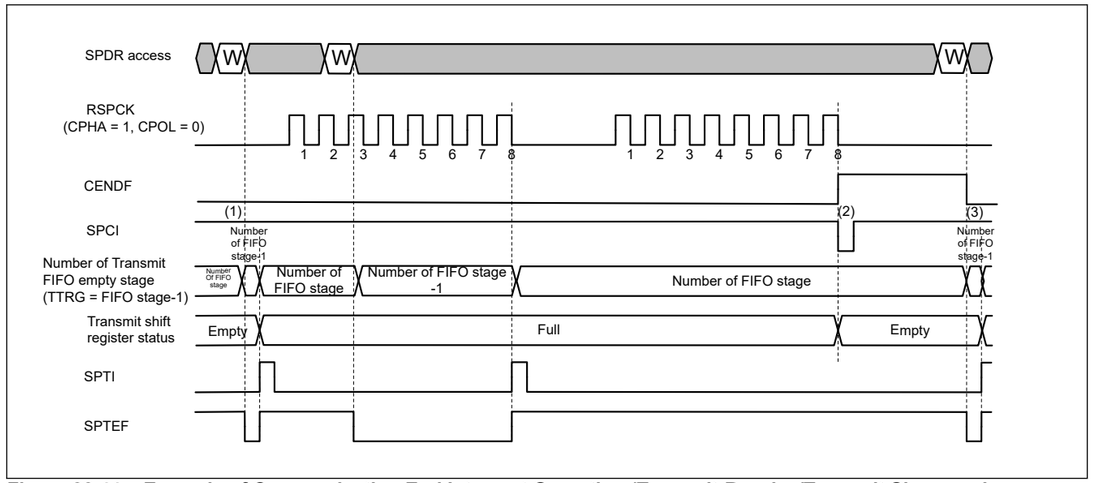


Figure 30.44 Example of Communication End Interrupt Operation (Transmit-Receive/Transmit Slave mode on Clock Synchronous Operation)

1. The CENDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.

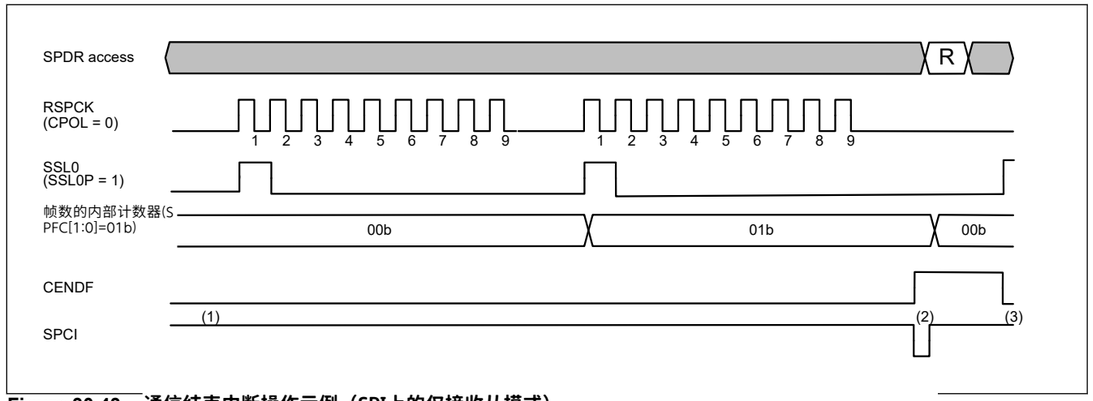


Figure 30.43 通信结束中断操作示例（SPI上的仅接收从模式）Operation / TI-SSP)

1.CENDF标志位为0，SPCI的电平在通信开始前为1。而这些在交流过程中一直保持着。

2.当最后一帧传输结束时，在RSPCK最后一个数据位采样时，CENDF标志将为1（通信结束）。如果CENDIE位为1，则SPCI中断以PCLK1个周期宽度输出。

3.CENDF标志在下一次传输开始时在SSL0断言处被清除。或者当向SPSRC.CENDFC位写入1时，CENDF标志为0。

30.3.9.5 在时钟同步操作（3线）的从模式下发送-接收发送

请参阅第30.2.9节中对CENDF位的描述。SPSR:SPI状态寄存器，用于在时钟同步（3线）从机模式下的Transmit-ReceiveTransmit-only期间设置通信完成标志的清除条件。

图30.44显示了在时钟同步操作（3线）的发送-接收发送从机模式期间通信结束中断操作的示例。

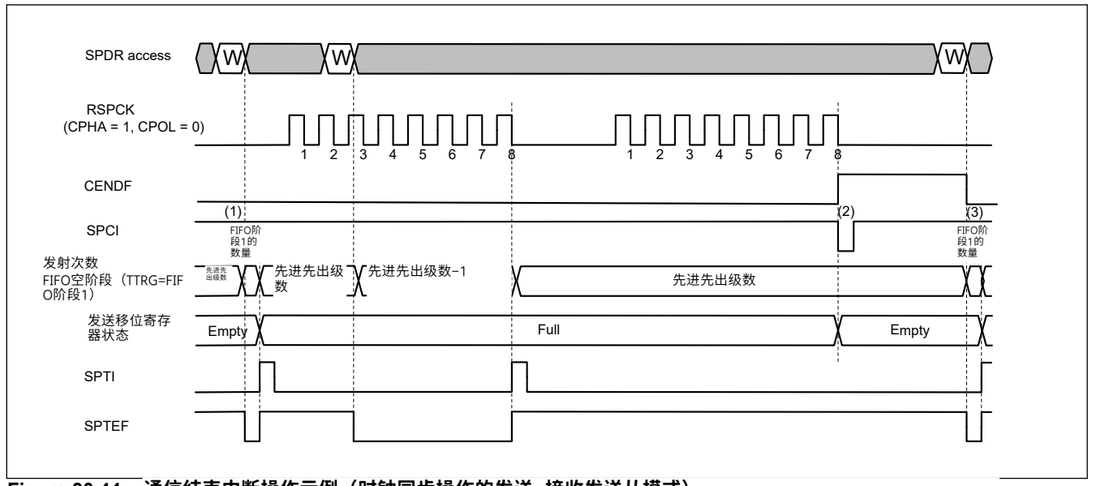


Figure 30.44 通信结束中断操作示例（时钟同步操作的发送-接收发送从模式）

1、通信开始前CENDF标志为0，SPCI的电平为1，在通信过程中一直保持。

2. When the next transfer data is not set in the transmit FIFO and the transmit shift register is empty, then the SPCI interrupt outputs with PCLK 1 cycle width if the CENDIE bit is 1.
3. The CENDF flag is cleared when the next transmission data is written to the transmit buffer (SPTX). Or when 1 is written to the SPSRC.CENDFC bit, then the CENDF flag is 0.

30.3.9.6 Receive Only in Slave Mode on Clock Synchronous Operation (3-wire)

Refer to the description of the CENDF bit in section 30.2.9. SPSR : SPI Status Register for the setting / clearing conditions of the communication completion flag during Receive -only in Slave Mode on Clock Synchronous (3-wire).

Figure 30.45 shows an example of communication end interrupt operation during receive only slave mode on clock synchronous operation.

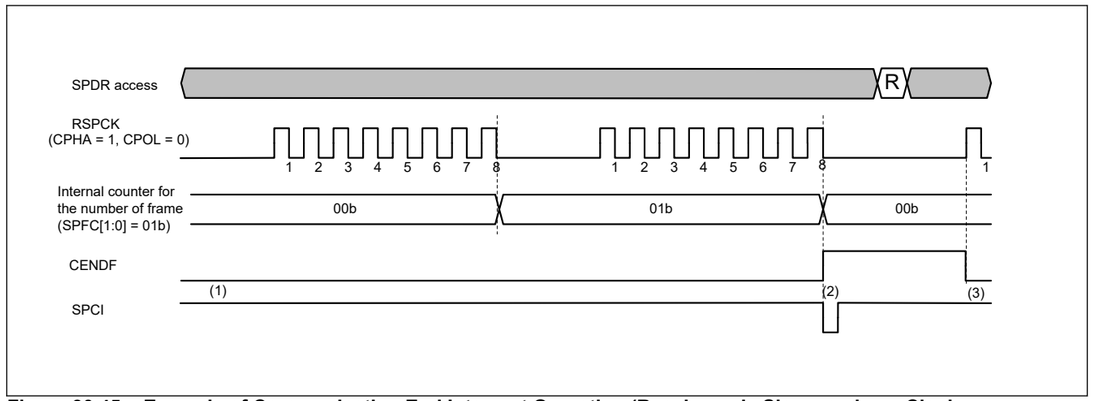


Figure 30.45 Example of Communication End Interrupt Operation (Receive-only Slave mode on Clock Synchronous Operation)

1. The CENDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.
2. The CENDF flag is set to 1 (communication completed) at the timing of the last data bit sampling of RSPCK in the last frame communication when the last frame of the RSPI data control register (SPDCR) SPFC set value is received. And then the SPCI interrupt outputs with PCLK 1 cycle width if the CENDIE bit is 1.
3. The CENDF flag is cleared at the first edge of RSPCK for the next transmission. Or when 1 is written to the SPSRC.CENDFC bit, then the CENDF flag is 0.

30.3.9.7 Common Operation

In this chapter, the operation common to each mode / area option communication in section 30.3.9.1. Transmit-Receive/ Transmit in Master Mode to section 30.3.9.6. Receive Only in Slave Mode on Clock Synchronous Operation (3-wire) is explained. When the enable of RSPI communication end interrupt (CENDIE) is 0, at the time of communication completion, a flag of communication end (CENDF) is set and an event of communication end (sp_elccend) is output, but no interrupt is output. However, if the enable of communication end interrupt (CENDIE) is set to 1 before clearing the flag of communication end (CENDF) while the enable of RSPI function (SPE) is 1, the communication end interrupt is output.

2.当发送FIFO中没有设置下一次传输数据且发送移位寄存器为空时，如果CENDIE位为1，则SPCI中断输出PCLK1个周期宽度。

3.CENDF标志在下一个发送数据写入发送缓冲区（SPTX）时被清除。或者当向SPSRC.CENDFC位写入1时，CENDF标志为0。

30.3.9.6 在时钟同步操作（3线）上仅在从模式下接收

请参阅第30.2.9节中对CENDF位的描述。SPSR:SPI状态寄存器，用于在时钟同步（3线）从机模式下仅接收期间设置通信完成标志的清除条件。

图30.45显示了时钟同步操作下仅接收从机模式期间的通信结束中断操作示例。

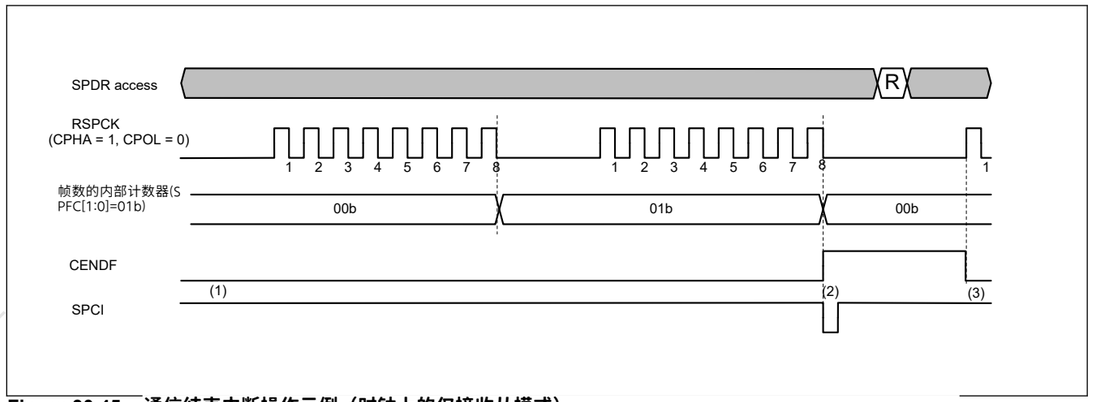


Figure 30.45 通信结束中断操作示例（时钟上的仅接收从模式）

1、通信开始前CENDF标志为0，SPCI的电平为1，在通信过程中一直保持。

2.在接收到RSPI数据控制寄存器(SPDCR)SPFC设置值的最后一帧时，在最后一帧通信中RSPCK的最后一个数据位采样定时将CENDF标志设置为1（通信完成）。如果CENDIE位为1，则SPCI中断以PCLK1个周期宽度输出。

3.CENDF标志在RSPCK的第一个边沿被清除以进行下一次传输。或者当向SPSRC.CENDFC位写入1时，CENDF标志为0。

30.3.9.7 常用操作

在本章中，30.3.9.1节中的每个模式区域选项通信的通用操作。发送-接收在主模式下发送到第30.3.9.6节。解释了时钟同步操作（3线）时仅在从模式下接收。当RSPI通信结束中断（CENDIE）使能为0时，通信完成时，设置通信结束标志（CENDF）并输出通信结束事件（sp_elccend），但不输出中断。但是，如果在清除通信结束标志（CENDF）之前将通信结束中断（CENDIE）的使能设置为1，而RSPI功能（SPE）的使能为1，则输出通信结束中断。

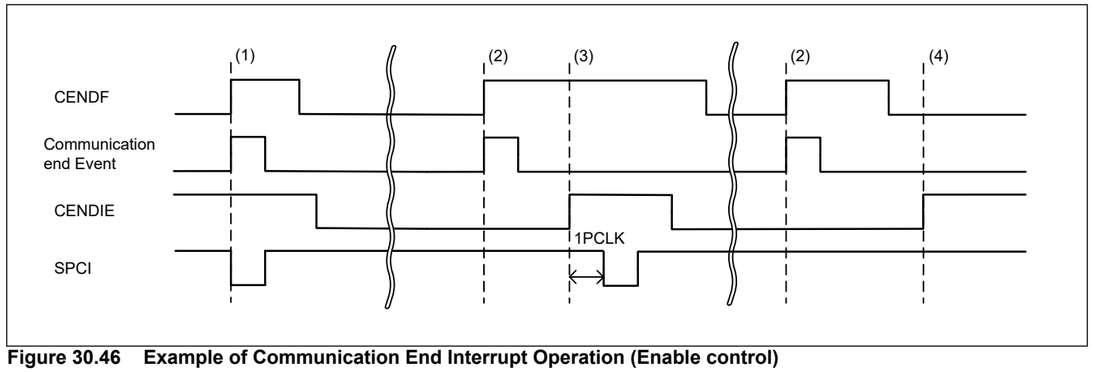


Figure 30.46 Example of Communication End Interrupt Operation (Enable control)

1. When the enable of RSPI communication end interrupt (CENDIE) is 1, at the time of communication completion, the following three are the same timing.
   - A flag of communication end (CENDF)
   - An event of communication end (sp_elccend)
   - The communication end interrupt
2. When the enable of RSPI communication end interrupt (CENDIE) is 0, at the time of communication completion, the following two are the same timing, but no interrupt.
   - A flag of communication end (CENDF)
   - An event of communication end (sp_elccend)
3. After (2), if the enable of communication end interrupt (CENDIE) is set when the enable of RSPI function (SPE) and the flag of communication end (CENDF) are 1, the communication end interrupt is output after 1 PCLKUSCIx.
4. After (2), even if the enable of communication end interrupt (CENDIE) is set when the enable of RSPI function (SPE) or the flag of communication end (CENDF) is 0, the communication end interrupt is not output.

30.3.10 Error Detection

In normal SPI serial transfers, data written to the transmit buffer of SPDR is transmitted, and received data can be read from the receive buffer of SPDR. If access is made to SPDR, an abnormal transfer might occur, depending on the status of the transmit or receive buffer or the status of the SPI at the beginning or end of serial transfer.

If an abnormal transfer occurs, the SPI detects the event as an underrun error, overrun error, parity error, or mode fault error. Table 30.9 lists the relationship between non-normal transfer operations and the SPI error detection function.

Table 30.9 Relationship between non-normal transfer operations and SPI error detection (1 of 2)

Operation	Occurrence condition	SPI operation	Error detection
1	SPDR is written while no empty stages in the transmit FIFO.	• The contents of the transmit buffer are kept • Write data is missing	None
2	SPDR is read while no data stored in receive FIFO.	The contents of the receive buffer and previously received data are output.	None
3	Serial transfer is started in slave mode when the SPI is not able to transmit data.	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the MISOn output signal is stopped • SPI function is disabled	Underrun error
4	Serial transfer ends when data is stored in the receive FIFO for the number of FIFO stages.	• Keeps the contents of the receive FIFO • Missing receive data	Overrun error

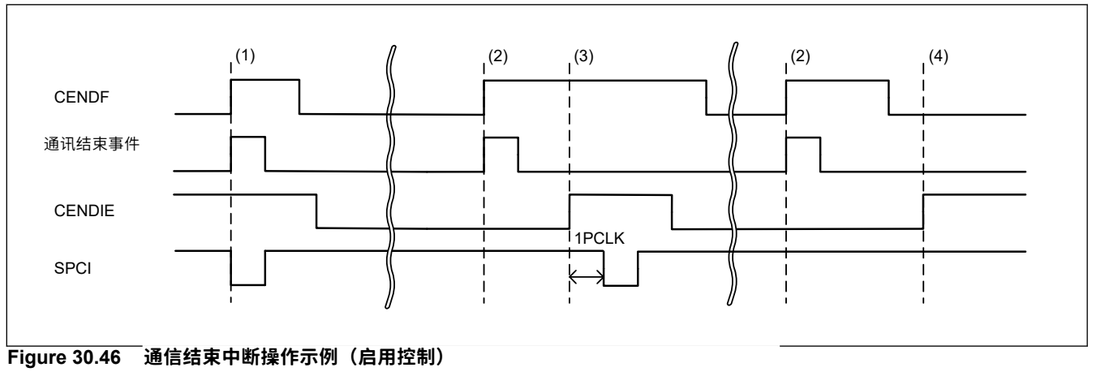


Figure 30.46 通信结束中断操作示例（启用控制）

1、当RSPI通讯结束中断（CENDIE）使能为1时，通讯完成时，以下三个是相同的时序。

- ●通讯结束标志（CENDF）
- ●通信结束事件（sp_elccend）
- ●通讯结束中断

2、当RSPI通讯结束中断（CENDIE）使能为0时，通讯完成时，以下两者时序相同，但无中断。

- ●通讯结束标志（CENDF）
- ●通信结束事件（sp_elccend）

3.（2）之后，如果在RSPI功能（SPE）使能和通信结束标志（CENDF）为1的情况下设置通信结束中断（CENDIE）使能，则在1个PCLKUSCIx后输出通信结束中断。

4.(2)后，即使在RSPI功能(SPE)使能或通信结束标志(CENDF)为0时设置通信结束中断(CENDIE)使能，也不输出通信结束中断。

30.3.10 错误检测

在正常的SPI串行传输中，写入SPDR的发送缓冲区的数据被发送，接收到的数据可以从SPDR的接收缓冲区中读取。如果访问SPDR，可能会发生异常传输，具体取决于发送或接收缓冲区的状态或串行传输开始或结束时SPI的状态。

如果发生异常传输，SPI会将事件检测为欠载错误、溢出错误、奇偶校验错误或模式故障错误。
表30.9列出了非正常传输操作和SPI错误检测功能之间的关系。

Table 30.9 非正常传输操作与SPI错误检测之间的关系(1of2)

Operation	发生条件	SPI操作	错误检测
1	在发送FIFO中没有空阶段时写入SPDR。	• 发送缓冲区的内容被保留 • 写入数据丢失	None
2	SPDR被读取，而没有数据存储在接收中FIFO.	输出接收缓冲区的内容和先前接收的数据。	None
3	当SPI无法传输数据时，串行传输在从模式下启动。	• 串行传输被暂停 • 发送或接收数据丢失 • MIOn输出信号的驱动停止 • SPI功能被禁用	Underrun error
4	当数据存储在接收FIFO中达到FIFO级数时，串行传输结束。	• 保留接收FIFO的内容 • 缺少接收数据	溢出错误

Table 30.9 Relationship between non-normal transfer operations and SPI error detection (2 of 2)

Operation	Occurrence condition	SPI operation	Error detection
5	An incorrect parity bit is received during full-duplex synchronous serial communication with the parity function enabled in following mode: ● Transmit-receive master mode ● Receive-only master mode ● Transmit-receive slave mode ● Receive-only slave mode	The parity error flag is asserted	Parity error
6	The SSLn0 input signal is asserted when the serial transfer is idle in multi-master mode.	● Driving of the RSPCKn, MOSIn, SSLn1 to SSLn3 output signals is stopped ● SPI function is disabled	Mode fault error
7	The SSLn0 input signal is asserted during serial transfer in multi-master mode.	● Serial transfer is suspended ● Transmit or receive data is missing ● Driving of the RSPCKn, MOSIn, SSLn1 to SSLn3 output signals is stopped ● SPI function is disabled	Mode fault error
8	[In the Motorola-SPI case] The SSLn0 input signal is negated during serial transfer in slave mode.	● Serial transfer is suspended ● Transmit or receive data is missing ● Driving of the MISOn output signal is stopped ● SPI function is disabled	Mode fault error
9	[In the TI-SSP case] The SSL0 input signal is asserted during serial transfer in slave mode.	● Serial transfer is suspended ● Transmit or receive data is missing ● Driving of the MISOn output signal is stopped ● SPI function is disabled	Mode fault error
10	After data is stored in the receive FIFO with SPDRES = 1, the number of stored data is less than the threshold value and no receive data is written for the set value of SPDRC [7:0]	Assert the receive data ready flag	Receive data ready

In operation 1 described in Table 30.9, the SPI does not detect an error. To prevent data omission during writes to SPDR, the writes to SPDR must be executed using a transmit buffer empty interrupt request (when the SPSR.SPTEF flag is 1).

Similarly, the SPI does not detect an error in operation 2. To prevent extraneous data from being read, SPDR read must be executed with an SPI receive buffer full interrupt request (when the SPSR.SPRF flag is 1).

For information on the other errors, see the following sections:

- Underrun error, indicated in operation 3, see section 30.3.10.4. Underrun errors
- Overrun error, indicated in operation 4, see section 30.3.10.1. Overrun errors
- Parity error, indicated in operation 5, see section 30.3.10.2. Parity errors
- Mode fault error, indicated in operations 6 to 8, see section 30.3.10.3. Mode fault errors
- For the transmit and receive interrupts, see section 30.3.7. Transmit Buffer Empty and Receive Buffer Full Interrupts.
- For the reception data ready in operations 10, see section 30.3.10.5. Received data ready.

30.3.10.1 Overrun errors

If a serial transfer ends when the receive buffer of SPDR is full, the SPI detects an overrun error and sets the SPSR.OVRF flag to 1. When the OVRF flag is 1, the SPI does not copy data from the shift register to the receive buffer, so the data prior to the error occurrence is retained in the receive buffer. To set the OVRF flag to 0, issue a system reset or 1 is written to the SPSRC.OVRFC bit.

Figure 30.47 shows an example of operation of the OVRF and SPRF flags. The SPSR and SPDR accesses shown in Figure 30.47 indicate the condition of accesses to the SPSR and SPDR register, where W denotes a write cycle, and R a read cycle. In this example, the SPI performs an 8-bit serial transfer when SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

Table 30.9 非正常传输操作与SPI错误检测之间的关系(2of2)

Operation	发生条件	SPI操作	错误检测
5	全双工同步串行通信时接收到错误的奇偶校验位，并在以下模式下启用奇偶校验功能：● 收发主模式 ● 只接收主模式 ● 收发从模式 ● 只接收从模式	奇偶错误标志被置位	奇偶校验错误
6	当串行传输在多主模式下空闲时，SSLn0输入信号被置位。	● 将RSPCKn、MOSIn、SSLn1驱动到SSLn3输出信号停止 ● SPI功能被禁用	模式故障错误
7	SSLn0输入信号在多主机模式下的串行传输期间被置位。	● 串行传输被暂停 ● 发送或接收数据丢失 ● 将RSPCKn、MOSIn、SSLn1驱动到SSLn3输出信号停止 ● SPI功能被禁用	模式故障错误
8	[在Motorola-SPI的情况下]SSLn0输入信号在从模式下的串行传输期间被否定。	● 串行传输被暂停 ● 发送或接收数据丢失 ● MIOn输出信号的驱动停止 ● SPI功能被禁用	模式故障错误
9	[在TI-SSP情况下]SSL0输入信号在从模式下的串行传输期间被断言。	● 串行传输被暂停 ● 发送或接收数据丢失 ● MIOn输出信号的驱动停止 ● SPI功能被禁用	模式故障错误
10	数据存储在接收FIFO中后SPDRES=1，存储数据个数小于阈值，SPDRC[7:0]设定值不写入接收数据	置位接收数据就绪标志	接收数据就绪

在表30.9中描述的操作1中，SPI未检测到错误。为防止写入SPDR期间数据遗漏，必须使用发送缓冲区空中断请求（当SPSR.SPTEF标志为1时）执行对SPDR的写入。

同样，SPI不会检测到操作2中的错误。为防止读取无关数据，必须使用SPI接收缓冲区满中断请求（当SPSR.SPRF标志为1时）执行SPDR读取。

有关其他错误的信息，请参阅以下部分：

●欠载错误，在操作3中指示，参见第30.3.10.4节。欠载错误

●超限错误，在操作4中显示，参见第30.3.10.1节。溢出错误

●奇偶校验错误，在操作5中指示，请参阅第30.3.10.2节。奇偶校验错误

●模式故障错误，在操作6到8中指示，参见第30.3.10.3节。模式故障错误

●关于发送和接收中断，参见30.3.7节。发送缓冲区空和接收缓冲区满中断。

●关于操作10中准备好的接收数据，请参见30.3.10.5节。接收数据就绪。

30.3.10.1 溢出错误

如果串行传输在SPDR的接收缓冲区已满时结束，则SPI检测到溢出错误并将SPSR.OVRF标志设置为1。当OVRF标志为1时，SPI不会将数据从移位寄存器复制到接收缓冲区，因此错误发生之前的数据保留在接收缓冲区中。要将OVRF标志设置为0，请发出系统复位或将1写入SPSRC.OVRFC位。

图30.47显示了OVRF和SPRF标志的操作示例。图30.47所示的SPSR和SPDR访问表示访问SPSR和SPDR寄存器的条件，其中W表示写周期，R表示读周期。在本例中，当SPCMDm.CPHA位为1且SPCMDm.CPOL位为0时，SPI执行8位串行传输。

波形中为RSPCKn给出的数字表示RSPCK周期数，例如传输的位数。

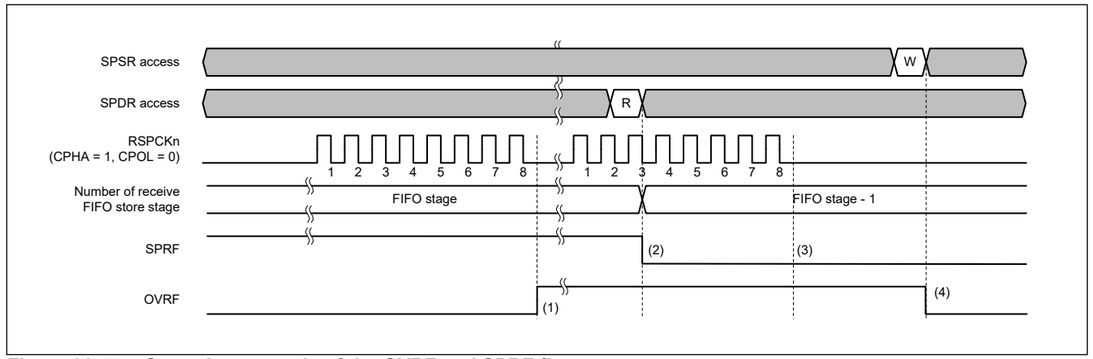


Figure 30.47 Operation example of the OVRF and SPRF flags

The operation of the flags at timings (1) to (4) in Figure 30.47 is as follows:

1. When serial transfer ends while data is stored for the number of FIFO stages, the RSPI detects an overrun error and sets the OVRF flag to 1. The RSPI does not copy shift register data to the receive buffer. The RSPI does not detect a parity error even when SPPE = 1. In master mode, the RSPI copies the value of pointer to the RSPI command register (SPCMDm) to the SPECM[2:0] bits in the RSPI status register (SPSR).
2. When SPDR is read, the SPI outputs the data in the receive buffer. At this time, the SPRF flag is cleared to 0 at the last access when the received data is read from SPDR in one processing routine using DTC / DMAC.
3. If the serial transfer ends with the OVRF flag set to 1 (overrun error occurred), the SPI does not copy data in the shift register to the receive buffer (the SPRF flag does not set to 1). A receive buffer full interrupt is not generated. Even when the SPPE bit is 1, parity errors are not detected. In an overrun error state when the SPI does not copy the received data from the shift register to the receive buffer, on termination of the serial transfer, the SPI determines that the shift register is empty. This enables data transfer from the transmit buffer to the shift register.
4. When 1 is written to the SPSRC.OVRFC bit, the SPSR.OVRF flag is cleared.

The occurrence of an overrun can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. When executing a serial transfer, you must ensure that overrun errors are detected early, for example by reading SPSR immediately after SPDR is read.

If an overrun error occurs and the OVRF flag sets to 1, normal reception operations cannot be performed until the OVRF flag is set to 0.

When the RSPCK auto-stop function is enabled (SPCR.SCKASE = 1) in master mode, an overrun error does not occur. Figure 30.48 and Figure 30.49 show the clock stop waveform when a serial transfer continues while the receive buffer is full in master mode.

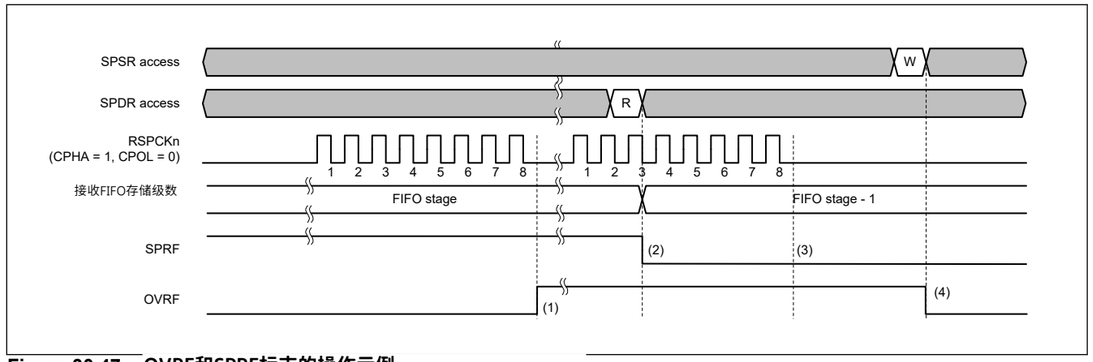


Figure 30.47 OVRF和SPRF标志的操作示例

图30.47中时间(1)到(4)的标志操作如下：

1.当串行传输结束而数据存储到FIFO级数时，RSPI检测到溢出错误并将OVRF标志设置为1。RSPI不会将移位寄存器数据复制到接收缓冲区。即使SPPE=1，RSPI也不会检测到奇偶校验错误。在主模式下，RSPI将指向RSPI命令寄存器(SPCMDm)的指针的值复制到RSPI状态寄存器(SPSR)中的SPECM[2:0]位.

2.读取SPDR时，SPI输出接收缓冲区中的数据。此时，当在一个使用DTCDMAC的处理程序中从SPDR读取接收到的数据时，SPRF标志在最后一次访问时被清除为0。

3.如果串行传输结束时OVRF标志设置为1（发生溢出错误），则SPI不会将移位寄存器中的数据复制到接收缓冲区（SPRF标志不设置为1）。不产生接收缓冲区满中断。即使SPPE位为1，也不会检测到奇偶校验错误。在SPI未将接收到的数据从移位寄存器复制到接收缓冲区的溢出错误状态下，在串行传输终止时，SPI确定移位寄存器为空。这使数据能够从发送缓冲器传输到移位寄存器。

4.当向SPSRC.OVRFC位写入1时，SPSR.OVRF标志被清除。

可以通过读取SPSR或使用SPI错误中断并读取SPSR来检查溢出的发生。
执行串行传输时，必须确保及早检测到溢出错误，例如在读取SPDR后立即读取SPSR。

如果发生溢出错误并且OVRF标志设置为1，则在OVRF标志设置为0之前无法执行正常接收操作。

在主机模式下启用RSPCK自动停止功能(SPCR.SCKASE=1)时，不会发生溢出错误。
图30.48和图30.49显示了在主机模式下接收缓冲器已满时串行传输继续时的时钟停止波形。

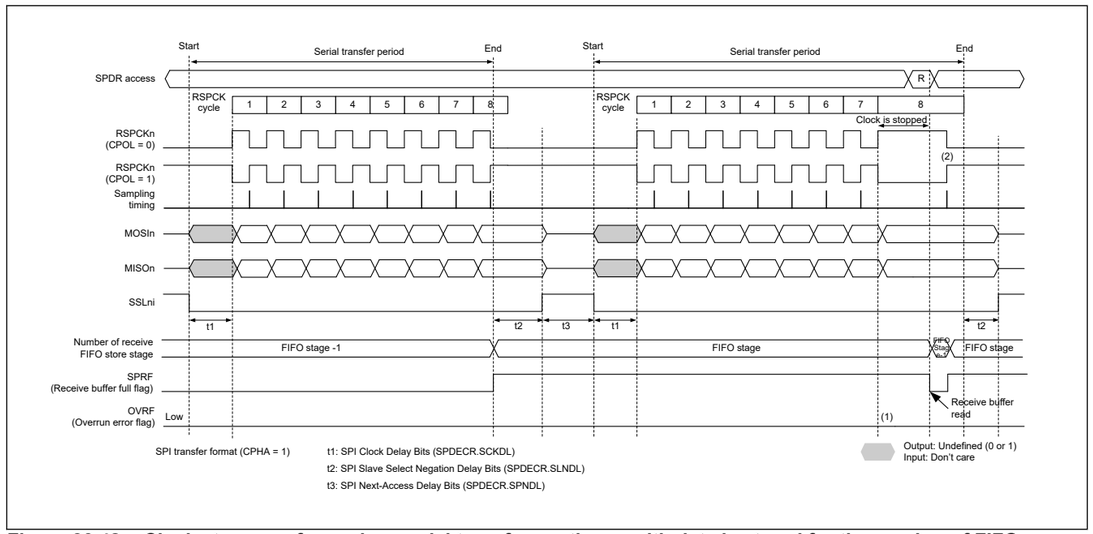


Figure 30.48 Clock stop waveform when serial transfer continues with data is stored for the number of FIFO stages in master mode (CPHA = 1)

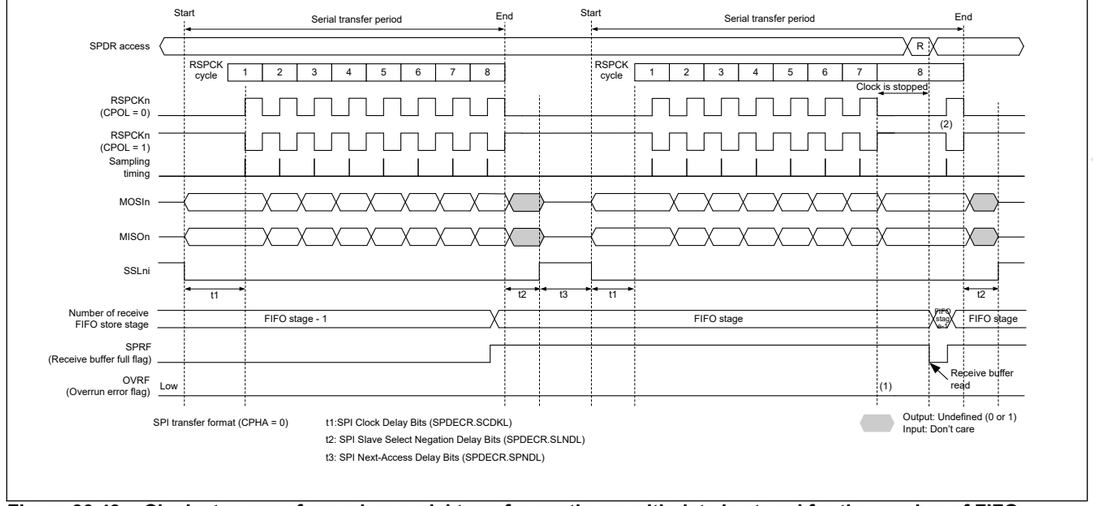


Figure 30.49 Clock stop waveform when serial transfer continues with data is stored for the number of FIFO stages in master mode (CPHA = 0)

The operation of the flags at timings (1) and (2) in Figure 30.48 and Figure 30.49 is as follows:

1. While data is stored in the receive FIFO for the number of FIFO stages, the RSPCK clock is deactivated and no overrun error occurs.
2. If SPDR is read while the clock is stopped, data in the receive buffer can be read. The RSPCK clock restarts.

Overrun error does not occur when RSPCK automatic stop function is enabled for transfer with no delay of between frames during burst transfer in master mode. Figure 30.50 and Figure 30.51 show the clock stop waveform, when there is no delay between frames at burst transfer and the serial transfer continues in the data is stored in the receive FIFO for the number of FIFO stages.

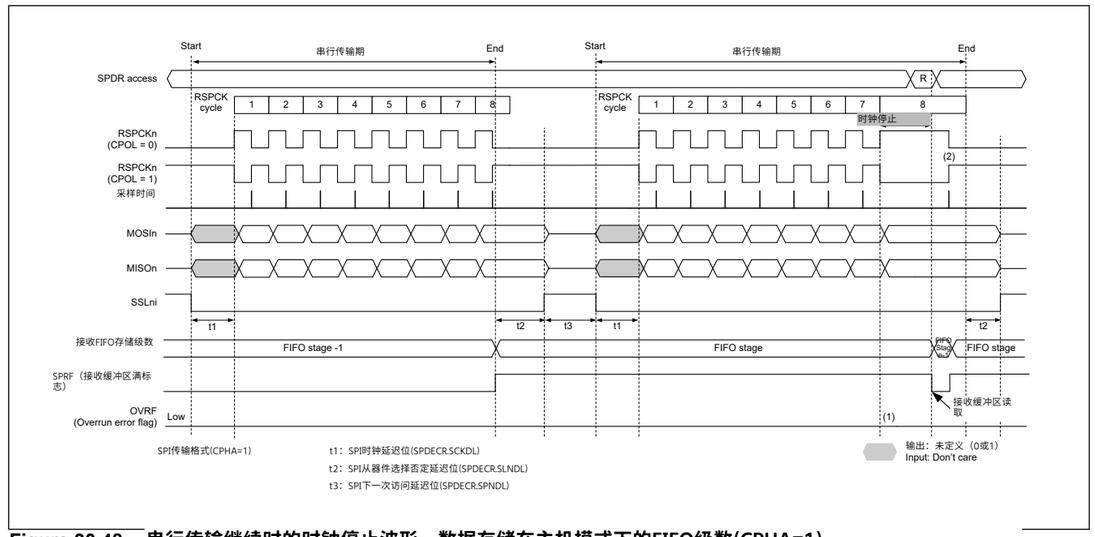


Figure 30.48 串行传输继续时的时钟停止波形，数据存储在主机模式下的FIFO级数(CPHA=1)

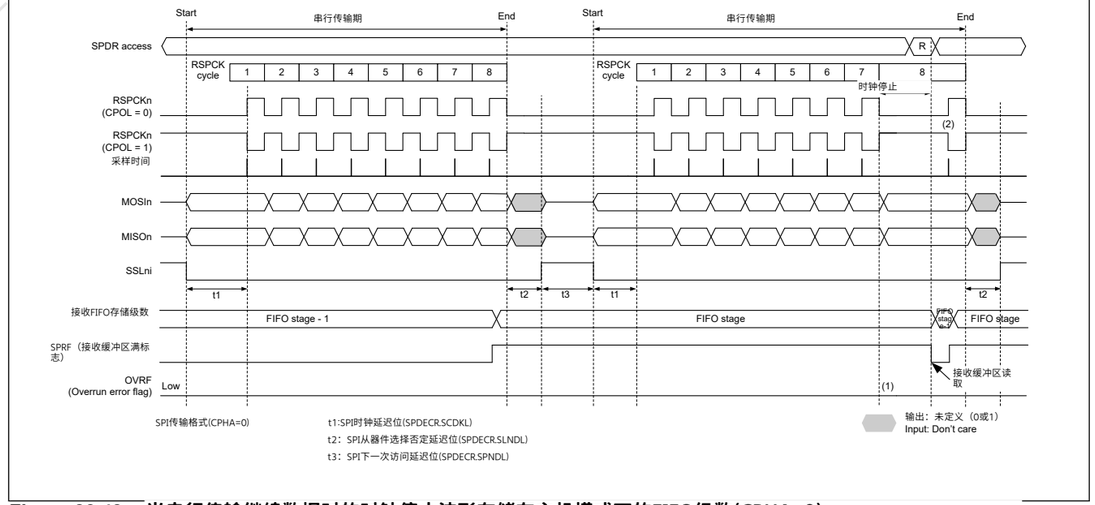


Figure 30.49 当串行传输继续数据时的时钟停止波形存储在主机模式下的FIFO级数(CPHA=0)

图30.48和图30.49中时序（1）和（2）的标志操作如下：

1.当数据存储在接收FIFO中达到FIFO级数时，RSPCK时钟被禁用并且不会发生溢出错误。

2.如果在时钟停止时读取SPDR，则可以读取接收缓冲区中的数据。RSPCK时钟重新启动。

在主模式下的突发传输期间，如果传输启用RSPCK自动停止功能且帧之间没有延迟，则不会发生溢出错误。图30.50和图30.51显示了时钟停止波形，当突发传输的帧之间没有延迟并且串行传输继续时，数据存储在接收FIFO中的FIFO级数。

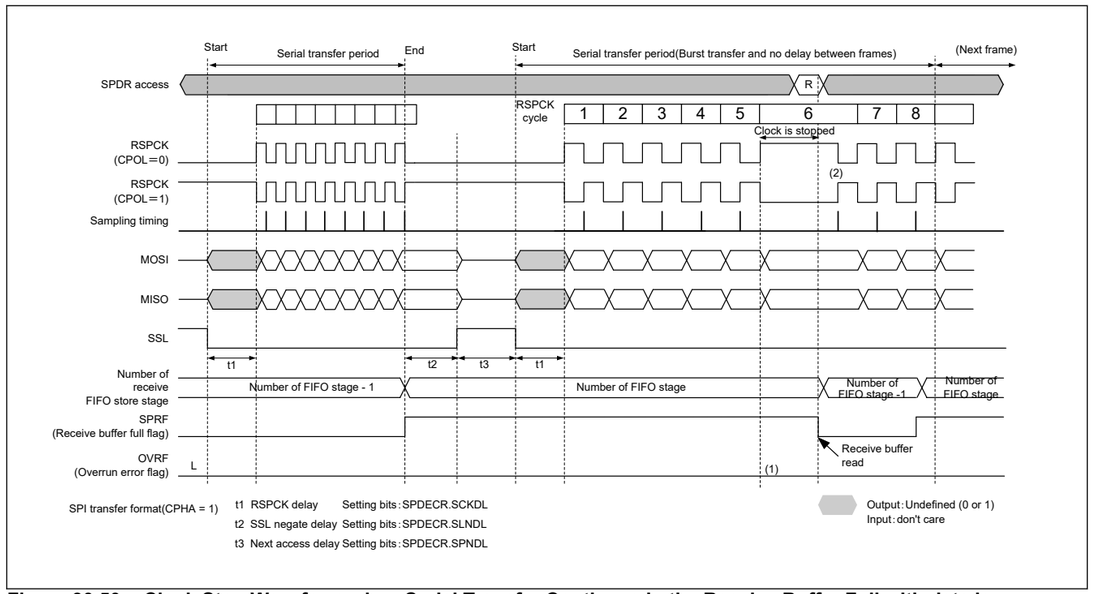


Figure 30.50 Clock Stop Waveform when Serial Transfer Continues in the Receive Buffer Full with data is stored for the number of FIFO stages (at burst transfer and no delay between frames CPHA = 1)

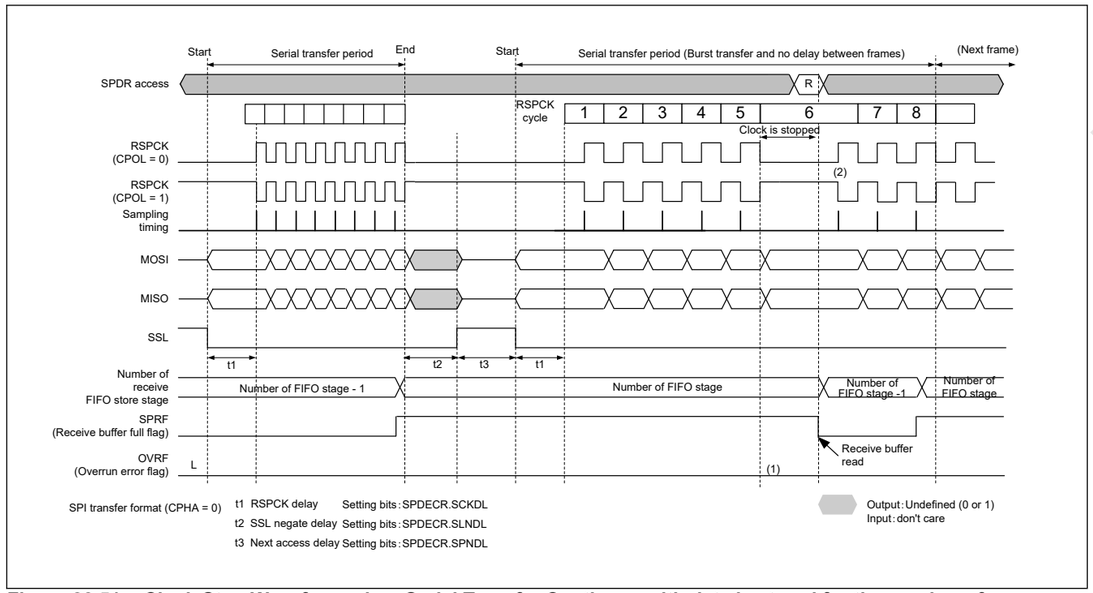


Figure 30.51 Clock Stop Waveform when Serial Transfer Continues with data is stored for the number of FIFO stages in Master Mode (at burst transfer and no delay between frames CPHA = 0)

The following describes operation of flags at timings (1) and (2) in the figure above.

1. While the data is stored for the number of FIFO stages, the RSPCK clock is deactivated and no overrun error occurs.
2. Receive buffer data can be read by reading SPDR during clock stop. After the receive buffer data has been read the RSPCK clock restarts.

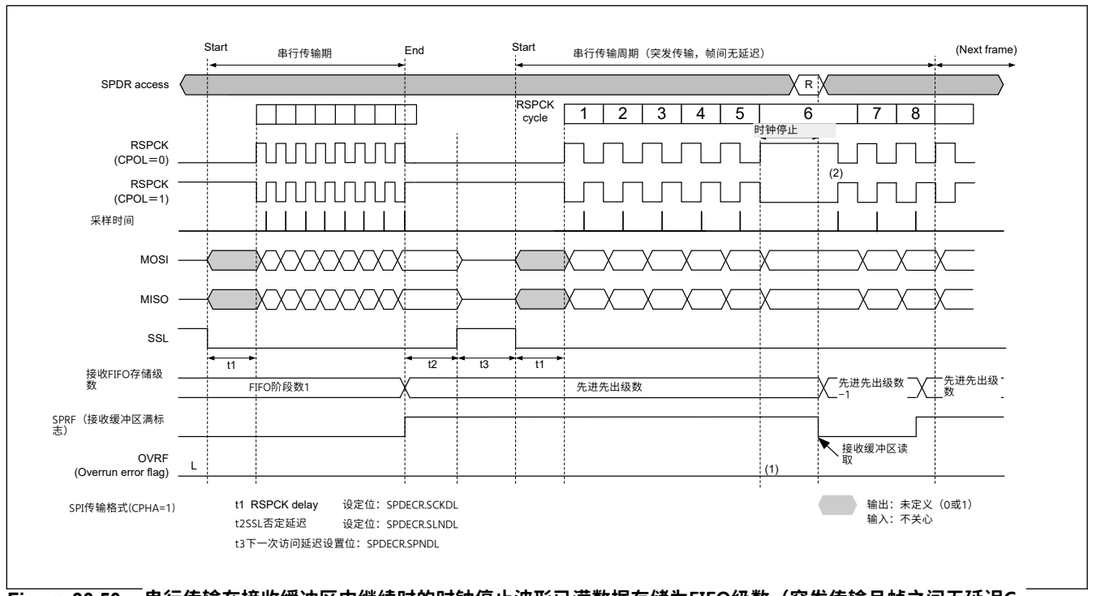


Figure 30.50 串行传输在接收缓冲区中继续时的时钟停止波形已满数据存储为FIFO级数（突发传输且帧之间无延迟CPHA=1）

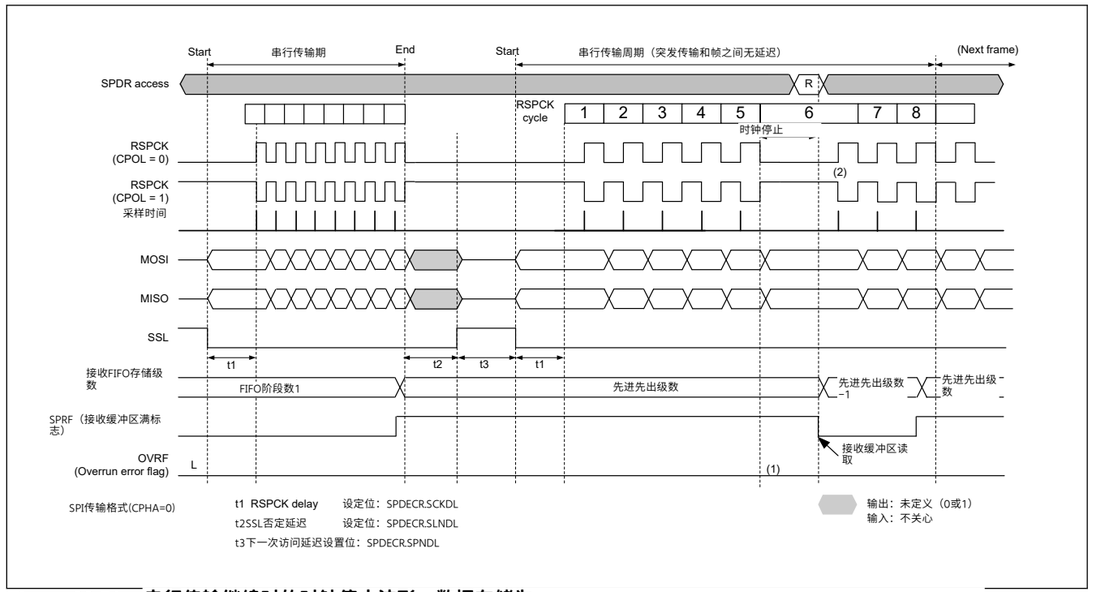


Figure 30.51 串行传输继续时的时钟停止波形，数据存储为主模式下的FIFO阶段（突发传输且帧之间无延迟CPHA=0）

下面描述在上图中的时间(1)和(2)的标志的操作。

1.当数据按FIFO级数存储时，RSPCK时钟被停用，不会发生溢出错误。

2.在时钟停止时，可以通过读取SPDR来读取接收缓冲数据。读取接收缓冲区数据后，RSPCK时钟重新启动。

30.3.10.2 Parity errors

After transfer in transmit-receive or receive-only master mode, transmit-receive slave mode or receive only slave mode while the SPPE bit in the RSPI control register (SPCR) is 1, the RSPI checks occurrence of a parity error. When the RSPI detects a parity error in received data, the PERF flag in the RSPI status register (SPSR) is set to 1. While the OVRF flag is 1, the RSPI does not copy shift register data to the receive buffer. Therefore, parity error in received data is not detected. To clear the PERF flag in SPSR to 0, issue a system reset or 1 is written to the SPSRC.PERFC bit.

Figure 30.52 shows an example of operation of the OVRF and PERF flags. The SPSR access shown in Figure 30.52 indicates the condition of access to the register, where W denotes a write cycle, and R a read cycle. In this example, full-duplex serial communication is performed while the SPCR.SPPE bit is 1. The SPI performs an 8-bit serial transfer when SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

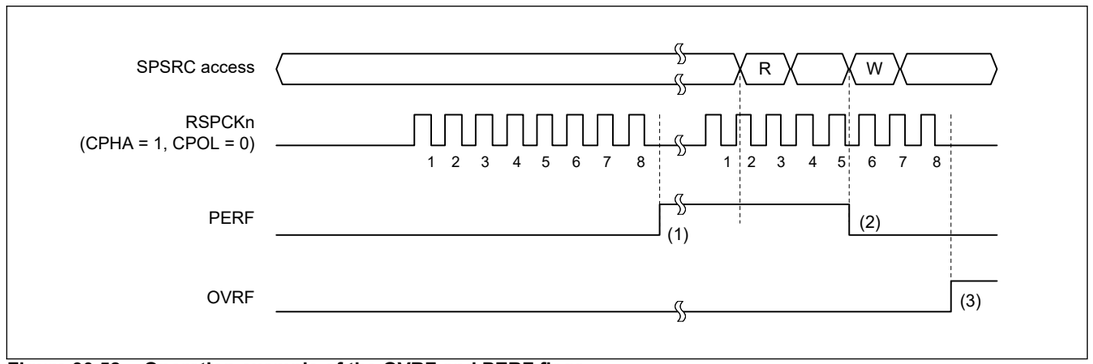


Figure 30.52 Operation example of the OVRF and PERF flags

The operation of the flags at timings (1) to (3) in Figure 30.52 is as follows:

1. When the RSPI does not detect an overrun error and terminates the serial transfer, the RSPI copies shift register data to the receive buffer. When the RSPI checks the received data and detects a parity error at this time, the PERF flag is set to 1. In master mode, the RSPI copies the value of pointer to the RSPI command register (SPCMDm) to the SPECM[2:0] bits in the RSPI Data control register 2 (SPDCR2).
2. When 1 is written to the SPSRC.PERFC bit, then clear the PERF flag.
3. When the SPI detects an overrun error and serial transfer is terminated, the data in the shift register is not copied to the receive buffer. The SPI does not perform parity error detection at this time.

Parity errors can be checked for by either reading the SPSR register or using an SPI error interrupt and reading the SPSR register. When executing a serial transfer, such checks are required to ensure early detection of parity errors. When the SPI is used in master mode, the pointer value to the SPCMDm register at the occurrence of the error can be checked by reading the SPDCR2.SPECM[2:0] bits.

30.3.10.3 Mode fault errors

The SPI operates in multi-master mode when the SPCR.MSTR bit is 1, the SPCR.SPMS bit is 0, and the SPCR.MODFEN bit is 1.

If the active level is input for the SSL0 input signal of the SPI in multi-master mode, the SPI detects a mode fault error regardless of the status of the serial transfer, and sets the SPSR.MODF flag to 1.

On detecting the mode fault error, the SPI copies the value of the pointer to SPCMD to the SPECM[2:0] bits.

The active level of the SSLn0 signal is determined by the SPCR3.SSL0P bit.

When the MSTR bit is 0, the SPI operates in slave mode.

When the RSPI's MODFEN bit = 1 and the SPMS bit = 0 in slave mode, if the SSL0 input signal is negated during the serial transfer period (from valid data drive start to final valid data latch), the RSPI detects a mode fault error, while any of the following 2 conditions is met.

30.3.10.2 奇偶校验错误

当RSPI控制寄存器(SPCR)中的SPPE位为1时，在发送-接收或仅接收主机模式、发送-接收从机模式或仅接收从机模式下传输后，RSPI会检查奇偶校验错误的发生。当RSPI在接收到的数据中检测到奇偶校验错误时，RSPI状态寄存器(SPSR)中的PERF标志设置为1。当OVRF标志为1时，RSPI不会将移位寄存器数据复制到接收缓冲区。因此，未检测到接收数据中的奇偶校验错误。要将SPSR中的PERF标志清除为0，请发出系统复位或将1写入SPSRC.PERFC位。

图30.52显示了OVRF和PERF标志的操作示例。图30.52所示的SPSR访问表示访问寄存器的条件，其中W表示写周期，R表示读周期。在本例中，当SPCR.SPPE位为1时执行全双工串行通信。当SPCMDm.CPHA位为1且SPCMDm.CPOL位为0时，SPI执行8位串行传输。波形表示RSPCK周期数，例如传输的位数。

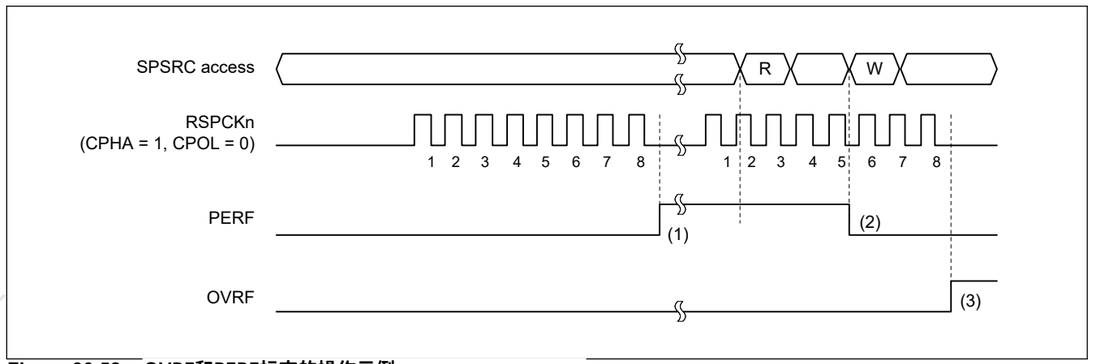


Figure 30.52 OVRF和PERF标志的操作示例

图30.52中时序(1)到(3)的标志操作如下：

1.当RSPI未检测到溢出错误并终止串行传输时，RSPI将移位寄存器数据复制到接收缓冲区。当RSPI此时检查接收到的数据并检测到奇偶校验错误时，PERF标志设置为1。在主机模式下，RSPI将指向RSPI命令寄存器（SPCMDm）的指针的值复制到SPECM[2:0]RSPI数据控制寄存器2(SPDCR2)中的位。

2.当SPSRC.PERFC位写入1时，清除PERF标志。

3.当SPI检测到溢出错误并终止串行传输时，移位寄存器中的数据不会复制到接收缓冲区。此时SPI不执行奇偶校验错误检测。

可以通过读取SPSR寄存器或使用SPI错误中断并读取SPSR寄存器来检查奇偶校验错误。在执行串行传输时，需要进行此类检查以确保及早发现奇偶校验错误。当SPI用于主机模式时，可以通过读取SPDCR2.SPECM[2:0]位来检查发生错误时指向SPCMDm寄存器的指针值。

30.3.10.3 模式故障错误

当SPCR.MSTR位为1、SPCR.SPMS位为0、SPCR.MODFEN位为1时，SPI工作在多主机模式。

如果在多主机模式下为SPI的SSL0输入信号输入有效电平，则无论串行传输的状态如何，SPI都会检测到模式故障错误，并将SPSR.MODF标志设置为1。

在检测到模式故障错误时，SPI将指向SPCMD的指针的值复制到SPECM[2:0]位。

SSLn0信号的有效电平由SPCR3.SSL0P位决定。

当MSTR位为0时，SPI工作在从机模式。

在从机模式下，当RSPI的MODFEN位=1且SPMS位=0时，如果在串行传输期间（从有效数据驱动开始到最终有效数据锁存）否定SSL0输入信号，则RSPI检测到模式故障错误，同时满足以下2个条件中的任何一个。

When the MSTR bit = 1, SPMS bit = 0, and MODFEN bit = 1 in the RSPI control register (SPCR), the RSPI operates in multi-master mode. When an active level is input to the SSL0 input signal of the RSPI in multi-master mode, the RSPI detects a mode fault error regardless of serial transfer status and sets the MODF flag in the RSPI status register (SPSR) to 1. When a mode fault error is detected, the RSPI copies the value of pointer to the RSPI command register (SPCMD) to the SPECM[2:0] bits in the RSPI status register (SPSR). The SSL0 signal active level depends on the SSL0P bit in the RSPI SSLi signal polarity bit (SPCR3.SSLiP) (i = 0 to 3).

While the MSTR bit is 0, the RSPI operates in slave mode. When the RSPI's MODFEN bit = 1 and the SPMS bit = 0 in slave mode, if the SSL0 input signal is negated during the serial transfer period (from valid data drive start to final valid data latch), the RSPI detects a mode fault error while any of the following 2 conditions is met.

[In the Motorola-SPI case]

When the SSL0 input signal is negated while serial data transfer.

[In the TI-SSP case]

When the SSL0 input signal is asserted while serial data transfer. However, during burst transfer, no error is detected even if the SSL0 input signal is asserted during the last bit of frame.

When the RSPI detects a mode fault error, it stops driving output signals and clears the SPE bit in the SPCR register. When the SPE bit is cleared, the RSPI function is disabled (as described in section 30.3.12. SPI Operation). In a multi-master configuration, the mastership can be released by stopping driving output signals and disabling the RSPI function by using a mode fault error.

Whether a mode fault error is present can be checked by reading SPSR or by reading an RSPI error interrupt and SPSR. To detect a mode fault error without using an RSPI error interrupt, poll SPSR. When the RSPI is used in master mode, the pointer value to SPCMD when an error is present can be checked by reading the SPECM[2:0] bits in SPSR.

While the MODF flag = 1, the RSPI ignores writing 1 to the SPE bit. To enable the RSPI function after a mode fault error is detected, clear the MODF flag to 0 without fail.

30.3.10.4 Underrun errors

While the SPI is operating in slave mode (SPCR.MSTR bit = 0) and the communication mode select bit (TXMD[1:0]) in the RSPI control register (SPCR) is set to 00b or 01b, if serial transfer is started before transmit data output is ready with the SPCR.SPE bit set to 1 (SPI function enabled), the SPI detects an underrun error and sets the SPSR.MODF and SPSR.UDRF flags to 1.

On detecting an underrun error, the SPI stops the driving of output signals and clears the SPCR.SPE bit to 0 (see section 30.3.11. Initializing the SPI).

The occurrence of underrun errors can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. Detecting underrun errors without using the SPI error interrupt requires polling of SPSR.

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of an underrun error, the MODF flag must be set to 0.

30.3.10.5 Received data ready

When SPCR.TXMD[1:0] = 00b, 01b, or 11b, and SPCR2.SPDRC[7:0] ≠ 0x00, after receiving data in the receive FIFO during communication (SPE = 1), SPDR.SPDRF flag is set to 1 when the received data is not stored even after the number of received FIFOs is equal to or less than ≤ the threshold value and the value set in SPDRC[7:0] has elapsed.

When the receive data ready is detected, the interrupt and event link output can be selected as SPRI or SPEI with the SPCR.SPDRES bit.

Figure 30.53 shows an example of reception data ready detection operation.

当RSPI控制寄存器(SPCR)中的MSTR位=1、SPMS位=0和MODFEN位=1时，RSPI工作在多主机模式。在多主机模式下，当向RSPI的SSL0输入信号输入有效电平时，无论串行传输状态如何，RSPI都会检测到模式故障错误，并将RSPI状态寄存器(SPSR)中的MODF标志设置为1。当检测到模式故障错误时，RSPI将指向RSPI命令寄存器(SPCMD)的指针的值复制到RSPI状态寄存器(SPSR)中的SPECM[2:0]位。SSL0信号有效电平取决于RSPI中的SSL0P位

SSLi信号极性位(SPCR3.SSLiP)(i=0到3)。

当MSTR位为0时，RSPI工作在从机模式。在从机模式下，当RSPI的MODFEN位=1且SPMS位=0时，如果在串行传输期间（从有效数据驱动开始到最终有效数据锁存）否定SSL0输入信号，则RSPI检测到模式故障错误，同时满足以下2个条件中的任何一个。

[In the Motorola-SPI case]

当串行数据传输时SSL0输入信号被否定时。

[In the TI-SSP case]

当SSL0输入信号在串行数据传输时被置位。然而，在突发传输过程中，即使SSL0输入信号在帧的最后一位被置位，也不会检测到错误。

当RSPI检测到模式故障错误时，它会停止驱动输出信号并清除SPCR寄存器中的SPE位。当SPE位清零时，RSPI功能被禁用（如第30.3.12.SPI操作部分所述）。在多主机配置中，可以通过停止驱动输出信号和使用模式故障错误禁用RSPI功能来释放主机权限。

可以通过读取SPSR或读取RSPI错误中断和SPSR来检查是否存在模式故障错误。要在不使用RSPI错误中断的情况下检测模式故障错误，请轮询SPSR。当RSPI用于主机模式时，当出现错误时指向SPCMD的指针值可以通过读取SPSR中的SPECM[2:0]位来检查。

当MODF标志=1时，RSPI忽略将1写入SPE位。要在检测到模式故障错误后启用RSPI功能，请务必将MODF标志清零。

30.3.10.4 Underrun errors

当SPI在从机模式下运行（SPCR.MSTR位=0）并且RSPI控制寄存器(SPCR)中的通信模式选择位(TXMD[1:0])设置为00b或01b时，如果串行传输开始在发送数据输出准备好之前
SPCR.SPE位设置为1（启用SPI功能），SPI检测到欠载错误并将SPSR.MODF和SPSR.UDRF标志设置为1。

检测到欠载错误时，SPI停止驱动输出信号并将SPCR.SPE位清零（参见第30.3.11节。初始化SPI）。

可以通过读取SPSR或使用SPI错误中断并读取
SPSR。在不使用SPI错误中断的情况下检测欠载错误需要轮询SPSR。

当MODF标志为1时，向SPE位写入1会被SPI忽略。要在检测到欠载错误后启用SPI功能，MODF标志必须设置为0。

30.3.10.5 接收数据就绪

当SPCR.TXMD[1:0]=00b、01b或11b且SPCR2.SPDRC[7:0]≠0x00时，在通信期间（SPE=1）接收到接收FIFO中的数据后，设置SPDR.SPDRF标志即使在接收到的FIFO的数量等于或小于≤阈值并且在SPDRC[7:0]中设置的值已经过去后，接收到的数据仍为1。

当检测到接收数据就绪时，中断和事件链接输出可以选择为SPRI或SPEI
SPCR.SPDRES bit.

图30.53显示了接收数据就绪检测操作的示例。

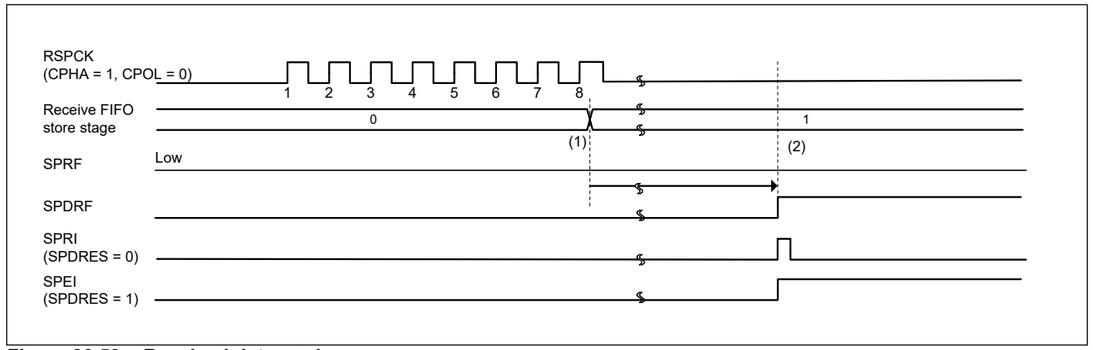


Figure 30.53 Received data ready

The following describes the operation at the timings indicated by (1) and (2) in the figure.

(1) Store the received data in the receive FIFO. SPRF is 0, because receive FIFO store stage ≤ RTRG.

(2) Set SPDRF and assert SPRI or SPEI because there is no writing to the receive FIFO for the amount of SPDRFC [7:0] set from above (1).

30.3.11 Initializing the SPI

If 0 is written to the SPCR.SPE bit or if the SPI sets the SPE bit to 0 because it detected a mode fault error or an underrun error, the SPI disables the SPI function and initializes some of the module functions. When a system reset is generated, the SPI initializes all of the module functions. This section describes initialization by clearing of the SPCR.SPE bit and by a system reset.

30.3.11.1 Initialization by clearing of the SPCR.SPE bit

When the SPCR.SPE bit is set to 0, the SPI initializes by:

- Suspending any serial transfer that is being executed
- Stopping the driving of output signals (Hi-Z) in slave mode
- Initializing the internal state of the SPI
- Initializing the transmit buffer of the SPI (the SPSR.STEF flag sets to 1)

Initialization by clearing of the SPE bit does not initialize the control bits of the SPI. For this reason, the SPI can be started in the same transfer mode in use prior to initialization when the SPE bit is set to 1 again.

The SPSR.CENDF, SPSR.SPRF, SPSR.OVRF, SPSR.MODF, SPSR.PERF, and SPSR.UDRF flags are not initialized, and the value of the SPDCR2.SPECM[2:0] and SPDCR2.SPCP[2:0] bits are not initialized. Therefore, even after the SPI is initialized, data from the receive buffer can be read to check the communication completion status and the error status during an SPI transfer.

The transmit buffer is initialized to an empty state (the SPSR.SPTEF flag sets to 1). Therefore, if the SPCR.SPTIE bit is set to 1 after SPI initialization, a transmit buffer empty interrupt is generated. To disable any transmit buffer empty interrupts when the SPI is initialized, write 0 to the SPTIE bit simultaneously while writing 0 to the SPE bit.

30.3.11.2 Initialization by system reset

A system reset completely initializes the SPI by initializing all SPI control bits, status bits, and data registers, in addition to meeting the requirements described in section 30.3.11.1. Initialization by clearing of the SPCR.SPE bit.

30.3.12 SPI Operation

30.3.12.1 Master mode operation

The only difference between single- and multi-master mode operation is the use of mode fault error detection (see section 30.3.10. Error Detection). In single-master mode, the SPI does not detect mode fault errors whereas in multi-master mode, it does. This section explains operations that are common to both modes.

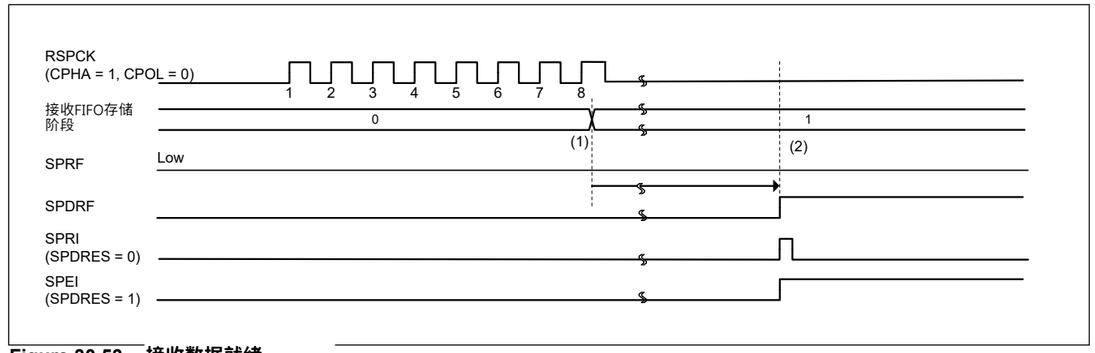


Figure 30.53 接收数据就绪

下面说明图中(1)和(2)所示定时的操作。

(1)将接收到的数据存入接收FIFO。SPRF为0，因为接收FIFO存储阶段≤RTRG。

(2)设置SPDRF并断言SPRI或SPEI，因为对于从上面(1)设置的SPDRFC[7:0]量，没有写入接收FIFO。

30.3.11 初始化SPI

如果将0写入SPCR.SPE位，或者如果SPI由于检测到模式故障错误或欠载错误而将SPE位设置为0，则SPI将禁用SPI功能并初始化一些模块功能。当产生系统复位时，SPI初始化所有模块功能。本节介绍通过清除SPCR.SPE位和系统复位进行的初始化。

30.3.11.1 通过清除SPCR.SPE位进行初始化

当SPCR.SPE位设置为0时，SPI通过以下方式初始化：

●暂停任何正在执行的串行传输

●从机模式下停止驱动输出信号（Hi-Z）

●初始化SPI的内部状态

●初始化SPI的发送缓冲区（SPSR.STEF标志设置为1）

通过清除SPE位进行的初始化不会初始化SPI的控制位。因此，当SPE位再次设置为1时，SPI可以在初始化之前以相同的传输模式启动。

SPSR.CENDF、SPSR.SPRF、SPSR.OVRF、SPSR.MODF、SPSR.PERF和SPSR.UDRF标志未初始化，SPDCR2.SPECM[2:0]和SPDCR2.SPCP[2的值：0]位未初始化。因此，即使在SPI初始化之后，也可以从接收缓冲区读取数据，以检查SPI传输期间的通信完成状态和错误状态。

发送缓冲区初始化为空状态（SPSR.SPTEF标志设置为1）。因此，如果SPCR.SPTIE位在SPI初始化后设置为1，则会产生发送缓冲区空中断。要在SPI初始化时禁用任何发送缓冲区空中断，请同时将0写入SPTIE位，同时将0写入SPE位。

30.3.11.2 通过系统复位初始化

除了满足第30.3.11.1节中描述的要求外，系统复位还通过初始化所有SPI控制位、状态位和数据寄存器来完全初始化SPI。通过清除SPCR.SPE位进行初始化。

30.3.12 SPI操作

30.3.12.1 主模式操作

单主机模式和多主机模式操作之间的唯一区别是使用模式故障错误检测（请参阅第30.3.10节。错误检测）。在单主机模式下，SPI不检测模式故障错误，而在多主机模式下，它可以。本节介绍两种模式共有的操作。

(1) Starting a serial transfer

When data is written to the RSPI data register (SPDR) while the next transfer data is not set in the transmit FIFO, the RSPI updates the transmit buffer (SPTXn,n = 0 to 3) data in SPDR. When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR, the SPI copies data from the transmit buffer to the shift register and starts serial transfer. On copying transmit data to the shift register, the SPI changes the status of the shift register to full. On termination of the serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

The polarity of the SSLni output pins depends on the SPCR3.SSLnP (n = 0 to 3) bits settings. For details on the SPI transfer format, see section 30.3.5. Transfer Formats.

(2) Terminating a serial transfer

[Except Receive-only in Master Mode]

After the RSPI detects the RSPCK edge corresponding to the final sampling timing regardless of the CPHA bit value in the RSPI command register (SPCMD), the RSPI terminates serial transfer. When the number of data stored in the receive FIFO is less than the number of FIFO stages, data is copied from the shift register to the receive buffer in the RSPI data register (SPDR) after serial transfer.

The final sampling timing varies depending on the bit length of transfer data. In master mode, the SPI data length depends on the SPCMDm.SPB[4:0] bit settings. The polarity of the SSLni output pin depends on the SPCR3.SSLnP (n = 0 to 3) bits settings. For details on the SPI transfer format, see section 30.3.5. Transfer Formats.

[Receive-only in Master Mode]

When any of the following 2 conditions is met, then RSPI terminating the serial transfer.

- After the RSPI detects the RSPCK edge corresponding to the final sampling timing regardless of the CPHA bit value in the RSPI command register (SPCMD), the RSPI terminates serial transfer.
- When writing SPCR2.RMEDTG = 1 during the serial transfer period, RSPI terminating the serial transfer.

When the number of data stored in the receive FIFO is less than the number of FIFO stages, data is copied from the shift register to the receive buffer in the RSPI data register (SPDR) after serial transfer.

The final sampling timing varies depending on the transfer data bit length. The data length of the RSPI in master mode depends on the set value of the SPB[4:0] bits in the RSPI command register (SPCMD). The SSL output signal polarity depends on the set RSPI SSLi signal polarity bit (SPCR3.SSLiP) (i = 0 to 3) value. For details about the RSPI transfer format, see section 30.3.5. Transfer Formats.

(3) Sequence control

The transfer format in master mode is determined as follows.

The transfer format used in master mode is determined by the SPCR3, SPCMDm, and SPDECR registers.

The SPCR3.SPSLN[2:0] bits determine the sequence configuration for serial transfers that are executed by the SPI in master mode. The following items are set in the SPCMDm register:

- SSLni pin output signal value
- MSB- or LSB-first
- Data length
- Some of the bit rate settings
- RSPCK polarity and phase
- Whether SPDECR.SCKDL is to be referenced
- Whether SPDECR.SLNDL is to be referenced
- Whether SPDECR.SPNDL is to be referenced

SPCR3.SPBR holds some of the bit rate settings, including SPDECR.SCKDL (SPI clock delay), SPDECR.SLNDL (SSL negation delay), and SPDECR.SPNDL (next-access delay).

Based on the sequence length assigned in SPCR3.SPSLN, the SPI makes up a sequence comprised of a part or all of the SPCMDm register. The SPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this

(1) 开始串行传输

当数据写入RSPI数据寄存器(SPDR)而下一次传输数据未设置在发送FIFO中时，RSPI会更新SPDR中的发送缓冲区(SPTXn n=0至3)数据。当SPDCR.SPFC[1:0]位中设置的帧数写入SPDR后移位寄存器为空时，SPI将数据从发送缓冲区复制到移位寄存器并开始串行传输。在将发送数据复制到移位寄存器时，SPI将移位寄存器的状态更改为已满。在串行传输终止时，它将移位寄存器的状态更改为空。无法引用移位寄存器的状态。

SSLni输出引脚的极性取决于SPCR3.SSLnP（n=0到3）位设置。有关SPI传输格式的详细信息，请参见第30.3.5节。传输格式。

(2) 终止串行传输

[除了在主模式下仅接收]

在RSPI检测到与最终采样时序对应的RSPCK边沿后，无论RSPI命令寄存器(SPCMD)中的CPHA位值如何，RSPI都会终止串行传输。当接收FIFO中存储的数据数小于FIFO级数时，串行传输后数据从移位寄存器复制到RSPI数据寄存器(SPDR)中的接收缓冲区。

最终的采样时序根据传输数据的位长而变化。在主机模式下，SPI数据长度取决于SPMDm.SPB[4:0]位设置。SSLni输出引脚的极性取决于SPCR3.SSLnP（n=0到3）位设置。有关SPI传输格式的详细信息，请参见第30.3.5节。传输格式。

[仅在主模式下接收]

当满足以下2个条件中的任何一个时，RSPI将终止串行传输。

●无论RSPI命令寄存器（SPCMD）中的CPHA位值如何，RSPI检测到最终采样时序对应的RSPCK边沿后，RSPI终止串行传输。

●在串行传输期间写入SPCR2.RMEDTG=1时，RSPI终止串行传输。

当接收FIFO中存储的数据数小于FIFO级数时，串行传输后数据从移位寄存器复制到RSPI数据寄存器(SPDR)中的接收缓冲区。

最终的采样时间因传输数据位长而异。主机模式下RSPI的数据长度取决于RSPI命令寄存器(SPCMD)中SPB[4:0]位的设置值。SSL输出信号极性取决于设置的RSPISSLi信号极性位(SPCR3.SSLiP)(i=0to3)值。有关RSPI传输格式的详细信息，请参见30.3.5节。传输格式。

(3) 顺序控制

主机模式下的传输格式如下确定。

主机模式中使用的传输格式由SPCR3、SPCMDm和SPDECR寄存器决定。

SPCR3.SPSLN[2:0]位确定由SPI在主模式下执行的串行传输的序列配置。在SPCMDm寄存器中设置以下项目：

●SSLni管脚输出信号值

- MSB- or LSB-first

●数据长度

●一些比特率设置

●RSPCK极性和相位

●SPDECR.SCKDL是否被引用

●SPDECR.SLNDL是否被引用

●SPDECR.SPNDL是否被引用

SPCR3.SPBR保存一些比特率设置，包括SPDECR.SCKDL（SPI时钟延迟）、SPDECR.SLNDL（SSL否定延迟）和SPDECR.SPNDL（下一次访问延迟）。

根据SPCR3.SPSLN中分配的序列长度，SPI组成一个序列，由部分或全部
SPMDm寄存器。SPI包含一个指向构成序列的SPCMDm寄存器的指针。这个的价值

pointer can be checked by reading the SPDCR2.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the SPI function is enabled, the SPI loads the pointer to the commands in SPCMD0, and incorporates the SPCMD0 settings into the transfer format at the beginning of serial transfer. The SPI increments the pointer each time the next-access delay period for a data transfer ends. On completion of the serial transfer that corresponds to the final command in the sequence, the SPI sets the pointer to SPCMD0, and in this way the sequence is executed repeatedly.

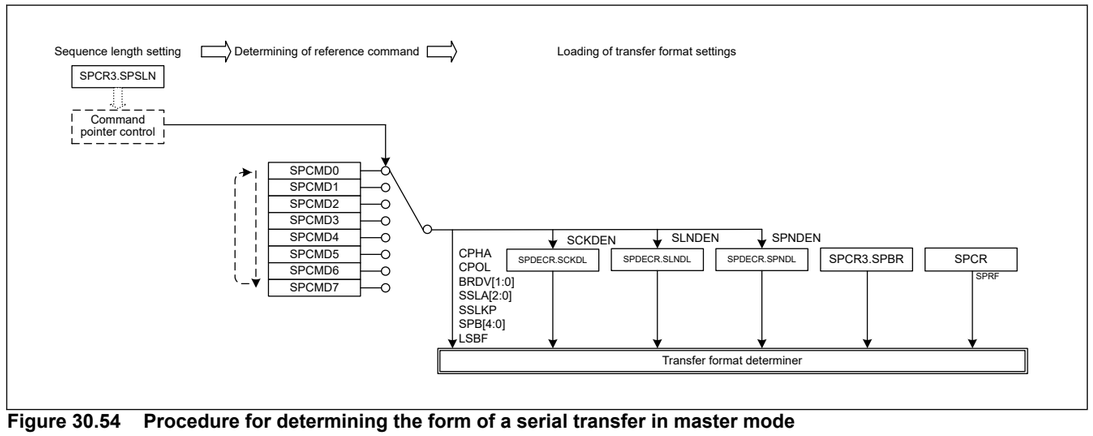


Figure 30.54 Procedure for determining the form of a serial transfer in master mode

In this section, a frame is the combination of the data in SPDR and the settings in SPCMDm.

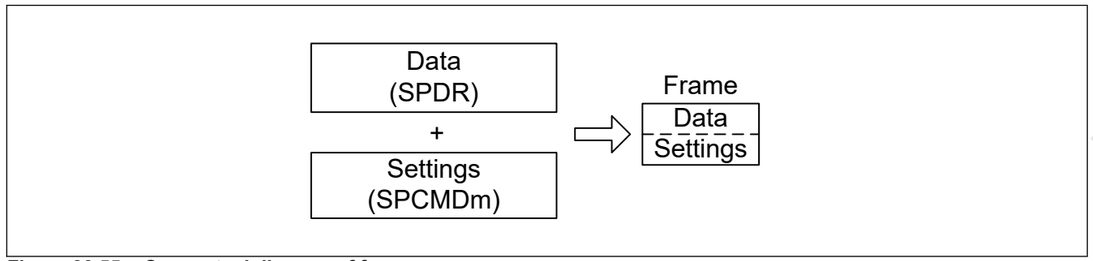


Figure 30.55 Conceptual diagram of frames

Figure 30.56 shows the correspondence between the commands and the transmit and receive buffers in the sequence of operations specified by the settings.

可以通过读取SPDCR2.SPCP[2:0]位来检查指针。当SPCR.SPE位设置为1且SPI功能使能时，SPI加载指向SPCMD0中命令的指针，并在串行传输开始时将SPCMD0设置合并到传输格式中。每次数据传输的下一个访问延迟周期结束时，SPI都会递增指针。在完成对应于序列中最后一个命令的串行传输后，SPI将指针设置为SPCMD0，并以此方式重复执行序列。

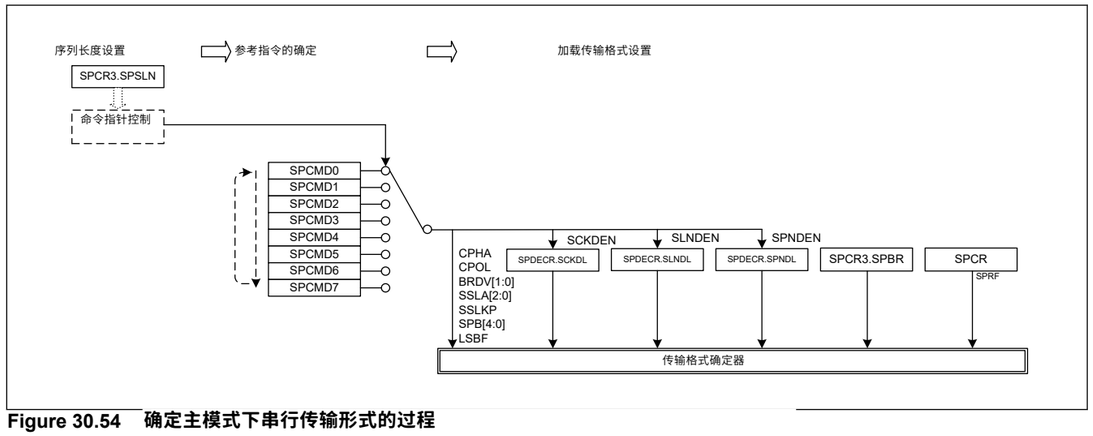


Figure 30.54 确定主模式下串行传输形式的过程

在本节中，帧是SPDR中的数据和SPMDm中的设置的组合。

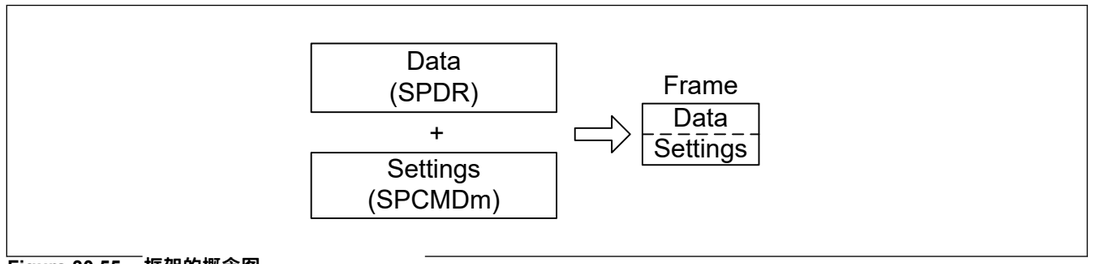


Figure 30.55 框架的概念图

图30.56显示了命令与设置指定的操作顺序中的发送和接收缓冲区之间的对应关系。

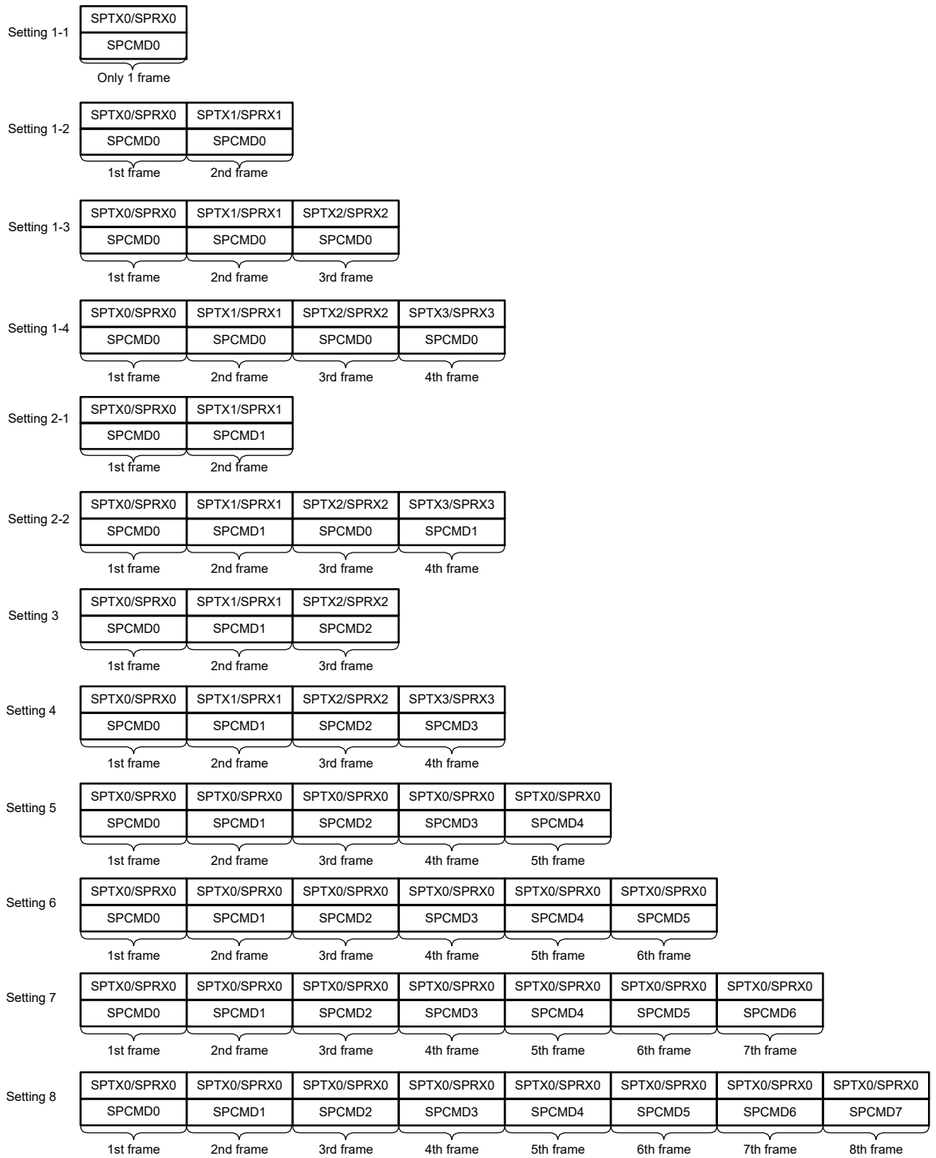


Figure 30.56 Correspondence between SPI Command Register and transmit and receive buffers in sequence operations

(4) Burst transfers

This section describes burst transfer during transmit-receive / transmit-only operation.

[In the Motorola-SPI case]

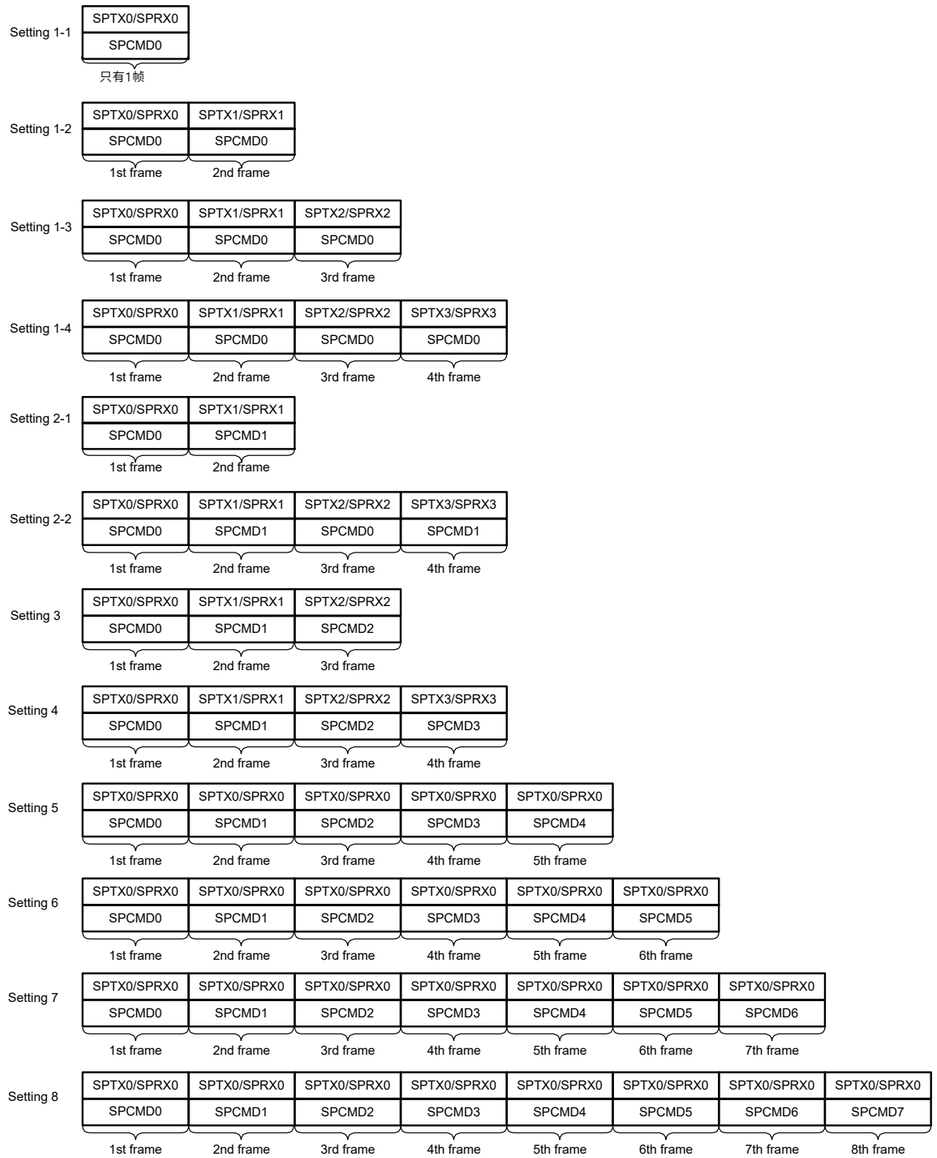


Figure 30.56 顺序操作中SPI命令寄存器与发送接收缓冲区的对应关系

(4) 突发传输

本节描述了发送–接收仅发送操作期间的突发传输。

[In the Motorola-SPI case]

If the SPCMDm.SSLKP bit that the SPI references during the current serial transfer is 1, the SPI maintains the SSLni signal level during the serial transfer until the beginning of the SSLni signal assertion for the next serial transfer. If the SSLni signal level for the next serial transfer is the same as the SSLni signal level for the current serial transfer, the SPI can execute continuous serial transfers while keeping the SSLni signal assertion status (burst transfer).

- When Between Burst Transfer Frames Delay Select bit (BFDS) of SPI control register (SPCR) is 0.

Figure 30.57 shows an example of an SSLni signal operation for a burst transfer that is implemented using the SPCMD0 and SPCMD1 register settings. This section describes SPI operations (1) to (8) shown in Figure 30.57.

Note: The polarity of the SSLni output signal depends on the SPCR3.SSLnP (n = 0 to 3) bits settings.

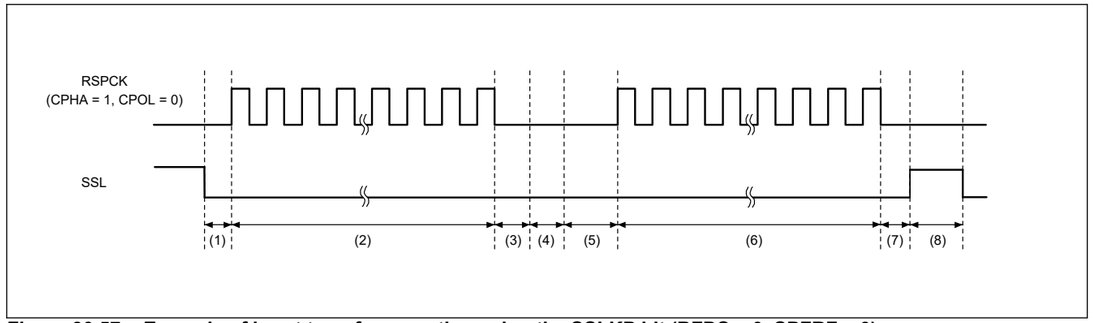


Figure 30.57 Example of burst transfer operation using the SSLKP bit (BFDS = 0, SPFRF = 0)

The SPI operation at times (1) to (8) in the figure is as follows:

1. Based on the SPCMD0 settings, the SPI asserts the SSLni signal and inserts RSPCK delays.
2. The SPI executes serial transfers in accordance with the SPCMD0 settings.
3. The SPI inserts an SSL negation delay.
4. Because the SPCMD0.SSLKP bit is 1, the SPI keeps the SSLni signal value specified in SPCMD0. This period additionally continues for 5 TCLK cycles (at minimum) that is the same as the next-access delay time of SPCMD0. If the shift register is empty after the passage of the minimum period, this period is sustained until the transmit data is stored in the shift register for the next transfer.
5. Based on the SPCMD1 settings, the SPI asserts the SSLni signal and inserts RSPCK delays.
6. The SPI executes serial transfers in accordance with the SPCMD1 settings.
7. Insert SSL negate delay.
8. Because the SPCMD1.SSLKP bit is 0, the SPI negates the SSLni signal. In addition, a next-access delay is inserted in accordance with SPCMD1.

If the SSLni signal output settings in the SPCMDm register where 1 is assigned to the SSLKP bit are different from the SSLni signal output settings in the SPCMDm register to be used in the next transfer, the SPI switches the SSLni signal status to SSLni signal assertion as shown in (5) in Figure 30.57. This corresponds to the command for the next transfer.

Note: If such an SSLni signal switching occurs, the slaves that drive the MISOn signal compete, and collision of signal levels might occur.

The SPI in master mode references the SSLni signal operation within the module when the SSLKP bit is not used. When the SPCMDm.CPHA bit is 0, the SPI can accurately start serial transfers by using the SSLni signal assertion for the next transfer that is detected internally.

- When Between Burst Transfer Frames Delay Select bit (BFDS) of SPI control register (SPCR) is 1.

Figure 30.58 shows an example of SSL signal operation when burst transfer is achieved by using the settings of SPCMD0 and SPCMD1. The following describes SPI operations of (1) to (6) shown in Figure 30.58. The SSL output signal polarity depends on the set SPCR3.SSLnP (n = 0 to 3) value.

如果SPI在当前串行传输期间引用的SPCMDm.SSLKP位为1，则SPI在串行传输期间保持SSLni信号电平，直到下一次串行传输的SSLni信号断言开始。如果下一次串行传输的SSLni信号电平与当前串行传输的SSLni信号电平相同，则SPI可以在保持SSLni信号断言状态（突发传输）的同时执行连续串行传输。

●当SPI控制寄存器(SPCR)的突发传输帧之间延迟选择位(BFDS)为0时。

图30.57显示了使用SPCMD0和SPCMD1寄存器设置实现的突发传输的SSLni信号操作示例。本节介绍图30.57所示的SPI操作(1)至(8)。

Note: SSLni输出信号的极性取决于SPCR3.SSLnP（n=0到3）位设置。

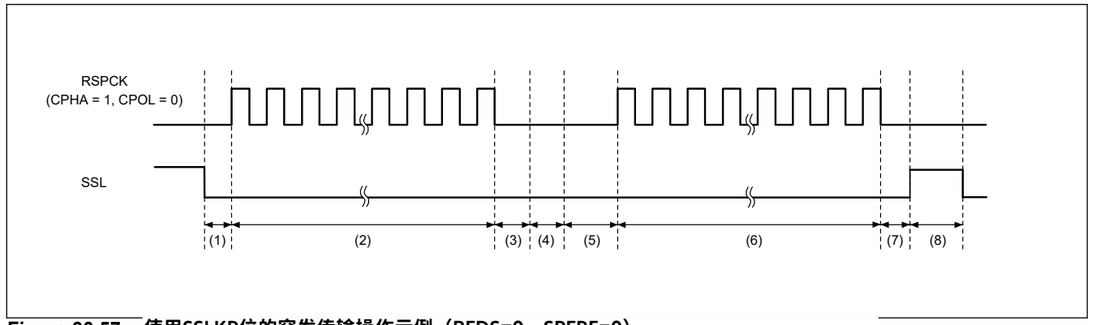


Figure 30.57 使用SSLKP位的突发传输操作示例（BFDS=0，SPFRF=0）

图中（1）到（8）时刻的SPI操作如下：

1.基于SPCMD0设置，SPI断言SSLni信号并插入RSPCK延迟。

2.SPI根据SPMD0设置执行串行传输。

3.SPI插入SSL否定延迟。

4.由于SPCMD0.SSLKP位为1，SPI保持SPCMD0中指定的SSLni信号值。这一时期
额外持续5个TCLK周期（至少），这与SPMD0的下一次访问延迟时间相同。如果在经过最小周期后移位寄存器为空，则该周期一直持续到发送数据存储在移位寄存器中以供下一次传输。

5.基于SPCMD1设置，SPI断言SSLni信号并插入RSPCK延迟。

6.SPI根据SPMD1设置执行串行传输。

7.插入SSL否定延迟。

8.由于SPCMD1.SSLKP位为0，SPI否定SSLni信号。此外，根据SPMD1插入下一个访问延迟。

如果SPCMDm寄存器中的SSLni信号输出设置（其中1分配给SSLKP位）与SPCMDm寄存器中用于下一次传输的SSLni信号输出设置不同，则SPI将SSLni信号状态切换为SSLni信号断言，如下所示如图30.57（5）所示。这对应于下一次传输的命令。

Note: 如果发生这种SSLni信号切换，驱动MISon信号的从机竞争，可能会发生信号电平冲突。

当不使用SSLKP位时，主模式下的SPI参考模块内的SSLni信号操作。当。。。的时候
SPCMDm.CPHA位为0，SPI可以通过使用SSLni信号断言来准确启动串行传输，以进行内部检测到的下一次传输。

●当SPI控制寄存器(SPCR)的突发传输帧之间延迟选择位(BFDS)为1时。

图30.58显示了使用SPCMD0和SPCMD1的设置实现突发传输时SSL信号操作的示例。下面描述图30.58所示的(1)到(6)的SPI操作。SSL输出信号极性取决于设置的SPCR3.SSLnP(n=0to3)值。

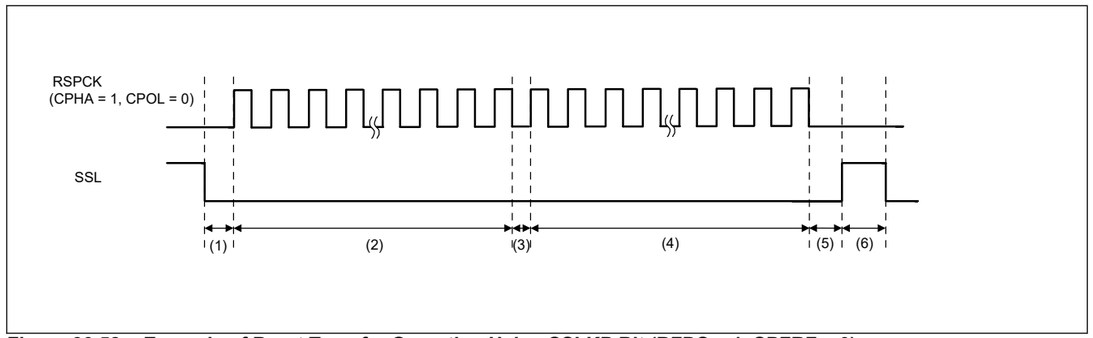


Figure 30.58 Example of Burst Transfer Operation Using SSLKP Bit (BFDS = 1, SPFRF = 0)

1. Assert the SSL signal and insert an RSPCK delay according to SPCMD0. The RSPCK delay is inserted only the first frame of burst transmission.
2. Perform serial transfer according to SPCMD0. Wait last clock until the next transmit data is stored in the shift register, if the shift register is empty during RSPCK negate period between frames.
3. The value of SSL signal according to SPCMD0 was hold, because the SPCMD0.SSLKP bit is 1. RSPCK negate period between frames is 0.5RSPCK, if the shift register is not empty.
4. Perform serial transfer according to SPCMD1.
5. Insert SSL negate delay for the last frame.
6. The SSL signal is negated because the SSLKP bit in SPCMD1 is 0. Furthermore, the next-access delay is inserted according to SPCMD1.

[In the TI-SSP case]

RSPI asserts the SSL signal for one cycle at the start of serial transfer.

Serial transfer can be executed continuously by asserting the SSL signal for one cycle at the start of the next serial transfer (burst transfer).

- When the SSL signal level holding bit (SSLKP) of the RSPI command register (SPCMD) is 1 and the burst transfer frame delay selection bit (BFDS) of the RSPI control register (SPCR) is 1, SPCMD0 to SPCMD1 are shown in Figure 30.59. The following shows an example of SSL signal operation and serial data MISO / MOSI when burst transfer is realized using the settings. The SSL output signal polarity depends on the set RSPI SSLi signal polarity bit (SPCR3.SSLiP) (i = 0 to 3) value.

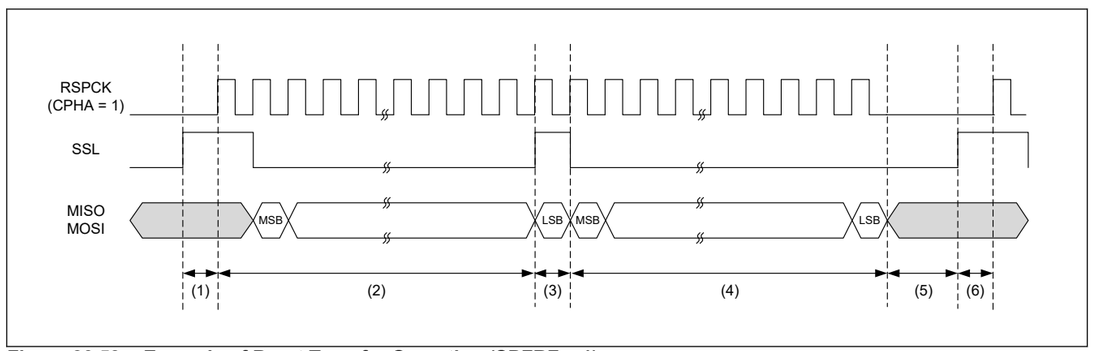


Figure 30.59 Example of Burst Transfer Operation (SPFRF = 1)

1. Assert the SSL signal and insert an RSPCK delay according to SPCMD0. The RSPCK delay is inserted only the first frame of burst transmission.
2. Perform serial transfer according to SPCMD0.

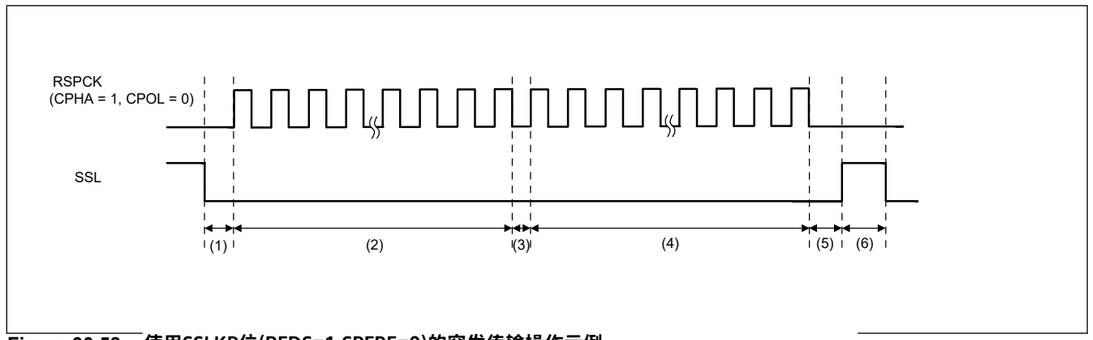


Figure 30.58 使用SSLKP位(BFDS=1 SPFRF=0)的突发传输操作示例

1.置位SSL信号并根据SPMD0插入一个RSPCK延迟。RSPCK延迟仅插入突发传输的第一帧。

2.根据SPMD0进行串行传输。如果在帧之间的RSPCK否定周期内移位寄存器为空，则等待最后一个时钟，直到下一个发送数据存储在移位寄存器中。

3.SPCMD0的SSL信号的值被保持，因为SPCMD0.SSLKP位为1。如果移位寄存器不为空，则帧间的RSPCK否定周期为0.5RSPCK。

4.根据SPMD1进行串行传输。

5.为最后一帧插入SSL否定延迟。

6.SSL信号被取反，因为SPCMD1中的SSLKP位为0。另外，根据SPCMD1插入下一个访问延迟。

[In the TI-SSP case]

RSPI在串行传输开始时将SSL信号置为一个周期。

通过在下一次串行传输（突发传输）开始时将SSL信号置为一个周期，可以连续执行串行传输。

●当RSPI命令寄存器(SPCMD)的SSL信号电平保持位(SSLKP)为1且突发传输时

RSPI控制寄存器（SPCR）的帧延迟选择位（BFDS）为1，SPCMD0到SPCMD1如图30.59所示。以下是使用设置实现突发传输时SSL信号操作和串行数据MISOMOSI的示例。SSL输出信号极性取决于设置的RSPISSLi信号极性位(SPCR3.SSLiP)(i=0to3)值。

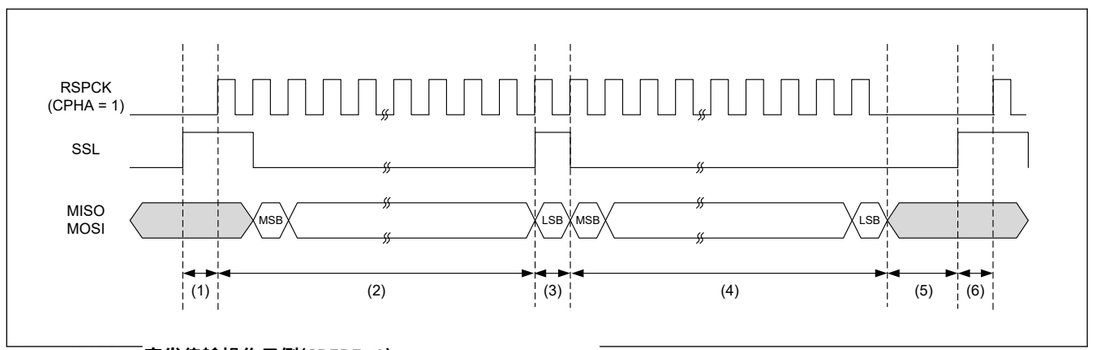


Figure 30.59 突发传输操作示例(SPFRF=1)

1.置位SSL信号并根据SPMD0插入一个RSPCK延迟。RSPCK延迟仅插入突发传输的第一帧。

2.根据SPMD0进行串行传输。

3. Final data transfer and SSL assertion are performed simultaneously. If the shift register is empty during the RSPCK negation period between frames, wait for the output of the last clock until the transmission data for the next transfer is stored in the shift register.
4. Perform serial transfer according to SPCMD1.
5. Insert OE negate delay for the last frame.
6. Insert the next access delay according to SPCMD1.

If the SSL signal output setting in SPCMD with the SSLKP bit set to 1 differs from the SSL signal output setting in SPCMD to be used for the next transfer, the RSPI changes the SSL signal state when the SSL signal corresponding to the next-transfer command is asserted ((5)). Note that, if an SSL signal change like this takes place, slaves that drive the MISO signal may conflict with each other, which may cause collision of signal level.

This section describes burst transfer during receive-only operation.

[In the Motorola-SPI case]

When the SSLKP bit in the RSPI command register (SPCMD), which the RSPI references in the current serial transfer, is 1, the RSPI retains the SSL signal level during serial transfer until the SSL signal assertion of the next serial transfer starts. When the SSL signal level in the next serial transfer is the same as the SSL signal level in the current serial transfer, the RSPI can continuously perform serial transfer while holding the SSL signal assertion status (burst transfer).

- When Between Burst Transfer Frames Delay Select bit (BFDS) of RSPI control register (SPCR) is 0.

Figure 30.60 shows an example of SSL signal operation when burst transfer is achieved by using the settings of SPCMD0 and SPCMD1. The following describes RSPI operations of (1) to (8) shown in Figure 30.60. The SSL output signal polarity depends on the set RSPI SSLi signal polarity bit (SPCR3.SSLiP) (i = 0 to 3) value.

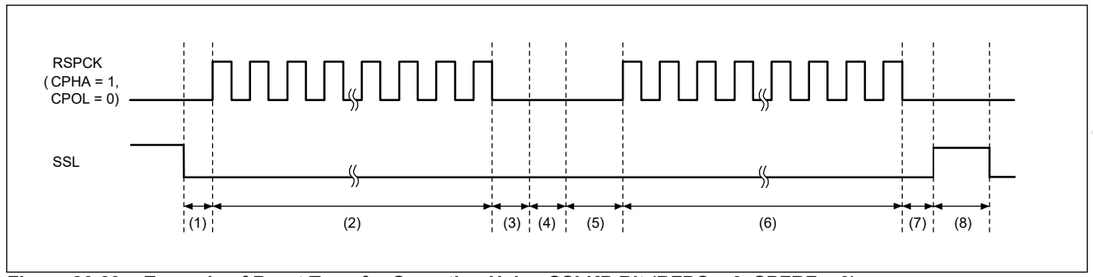


Figure 30.60 Example of Burst Transfer Operation Using SSLKP Bit (BFDS = 0, SPFRF = 0)

1. Assert the SSL signal and insert an RSPCK delay according to SPCMD0.
2. Perform serial transfer according to SPCMD0.
3. Insert an SSL negation delay.
4. The SSL signal value in SPCMD0 is retained because the SSLKP bit in SPCMD0 is 1. This period additionally continues for 5 TCLK cycles (at minimum) that is the same as the next-access delay time of SPCMD0.
5. Assert the SSL signal and insert an RSPCK delay according to SPCMD1.
6. Perform serial transfer according to SPCMD1.
7. Insert SSL negate delay.
8. The SSL signal is negated because the SSLKP bit in SPCMD1 is 0. Furthermore, the next-access delay is inserted according to SPCMD1.

If the SSL signal output setting and the SSL signal output setting between SPCMDs used for burst transfer are different, RSPI switches the SSL signal state when the SSL signal corresponding to the next transfer command is asserted ((5)). Note that, if an SSL signal change like this takes place, slaves that drive the MISO signal may conflict with each other, which may cause collision of signal level.

The RSPI in master mode references the SSL signal operation in the module when SSLKP is not used.

3.最终数据传输和SSL断言同时进行。如果在帧之间的RSPCK否定期间移位寄存器为空，则等待最后一个时钟的输出，直到下一次传输的传输数据存储在移位寄存器中。

4.根据SPMD1进行串行传输。

5.为最后一帧插入OE否定延迟。

6.根据SPMD1插入下一个访问延迟。

如果SPCMD中SSLKP位设置为1的SSL信号输出设置与SPCMD中用于下一次传输的SSL信号输出设置不同，则当与nexttransfer命令对应的SSL信号被断言时，RSPI会更改SSL信号状态((5))。请注意，如果发生这样的SSL信号变化，驱动MISO信号的从机可能会相互冲突，从而可能导致信号电平冲突。

本节介绍仅接收操作期间的突发传输。

[In the Motorola-SPI case]

当当前串行传输中RSPI引用的RSPI命令寄存器(SPCMD)中的SSLKP位为1时，RSPI在串行传输期间保持SSL信号电平，直到下一次串行传输的SSL信号断言开始。当下一次串行传输的SSL信号电平与当前串行传输的SSL信号电平相同时，

RSPI可以在保持SSL信号断言状态的同时连续执行串行传输（突发传输）。

●当RSPI控制寄存器(SPCR)的突发传输帧之间延迟选择位(BFDS)为0时。

图30.60显示了使用SPCMD0和SPCMD1的设置实现突发传输时SSL信号操作的示例。下面描述图30.60所示(1)到(8)的RSPI操作。SSL输出信号极性取决于设置的RSPISSLi信号极性位(SPCR3.SSLiP)(i=0to3)值。

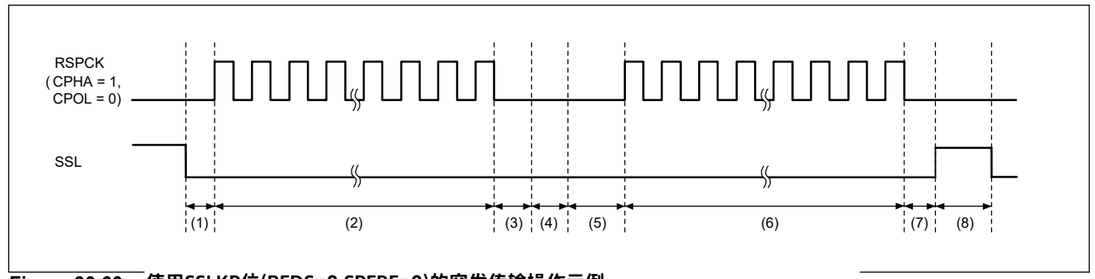


Figure 30.60 使用SSLKP位(BFDS=0 SPFRF=0)的突发传输操作示例

1.置位SSL信号并根据SPMD0插入一个RSPCK延迟。

2.根据SPMD0进行串行传输。

3.插入SSL否定延迟。

4.SPCMD0中的SSL信号值被保留，因为SPCMD0中的SSLKP位为1。此周期额外持续5个TCLK周期（至少），与SPCMD0的下一次访问延迟时间相同。

5.置位SSL信号并根据SPMD1插入一个RSPCK延迟。

6.根据SPMD1进行串行传输。

7.插入SSL否定延迟。

8.SSL信号被取反，因为SPCMD1中的SSLKP位为0。此外，根据SPCMD1插入下一个访问延迟。

如果用于突发传输的SPCMD之间的SSL信号输出设置和SSL信号输出设置不同，则当与下一个传输命令对应的SSL信号被断言时，RSPI切换SSL信号状态((5))。请注意，如果发生这样的SSL信号变化，驱动MISO信号的从机可能会相互冲突，从而可能导致信号电平冲突。

不使用SSLKP时，主模式下的RSPI参考模块中的SSL信号操作。

Even when the CPHA bit in SPCMD is 0, the RSPI can accurately start serial transfer by using the nexttransfer SSL signal assertion detected internally. For this reason, burst transfer in master mode is enabled regardless of the set CPHA bit value. (See section 30.3.11. Initializing the SPI.)

- When Between Burst Transfer Frames Delay Select bit (BFDS) of RSPI control register (SPCR) is 1.

Figure 30.61 shows an example of SSL signal operation when burst transfer is achieved by using the settings of SPCMD0 and SPCMD1. The following describes RSPI operations of (1) to (6) shown in Figure 30.61. The SSL output signal polarity depends on the set RSPI SSLi signal polarity bit (SPCR3.SSLiP) (i = 0 to 3) value.

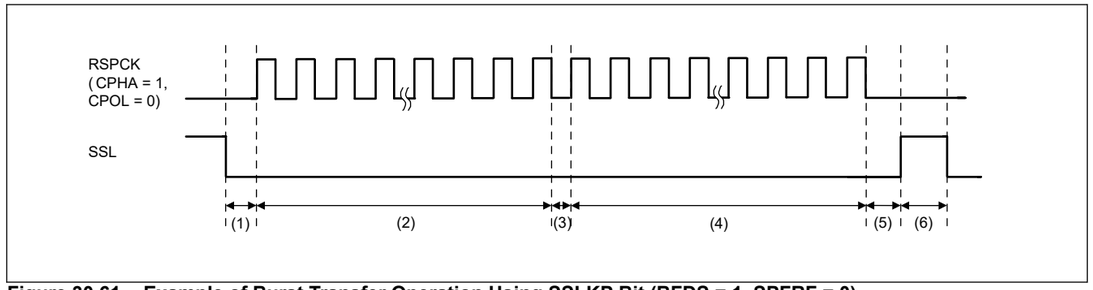


Figure 30.61 Example of Burst Transfer Operation Using SSLKP Bit (BFDS = 1, SPFRF = 0)

1. Assert the SSL signal and insert an RSPCK delay according to SPCMD0.
   The RSPCK delay is inserted only the first frame of burst transmission.
2. Perform serial transfer according to SPCMD0.
3. Since it is not the last frame, the SSL signal value at SPCMD0 is retained. RSPCK negation between frames is 0.5RSPCK for the next frame.
4. Perform serial transfer according to SPCMD1.
5. Insert SSL negate delay for the last frame.
6. The SSL signal is negated. Furthermore, the next-access delay is inserted according to SPCMD1.

Note: Last frame: Frame set by RMFM [4: 0] bits when SPCR2.RMFM [4: 0] ≠ 00h
Or, a frame in which SPCR2.RMEDTG = 1 has been accepted.

[In the TI-SSP case]

RSPI asserts the SSL signal for one cycle at the start of serial transfer.

Serial transfer can be executed continuously by asserting the SSL signal for one cycle at the start of the next serial transfer (burst transfer).

- When the SSL signal level holding bit (SSLKP) of the RSPI command register (SPCMD) is 1 and the burst transfer frame delay selection bit (BFDS) of the RSPI control register (SPCR) is 1, SPCMD0 to SPCMD1 are shown in Figure 30.62. The following shows an example of SSL signal operation and serial data MISO / MOSI when burst transfer is realized using the settings. The SSL output signal polarity depends on the set RSPI SSLi signal polarity bit (SPCR3.SSLiP) (i = 0 to 3) value.

即使SPCMD中的CPHA位为0，RSPI也可以通过使用内部检测到的nexttransferSSL信号断言准确地启动串行传输。因此，无论设置的CPHA位值如何，都会启用主模式下的突发传输。（参见第30.3.11节。初始化SPI。）

●当RSPI控制寄存器(SPCR)的BurstTransferFrames延迟选择位(BFDS)为1时。

图30.61显示了使用SPCMD0和SPCMD1的设置实现突发传输时SSL信号操作的示例。下面描述图30.61所示(1)到(6)的RSPI操作。SSL输出信号极性取决于设置的RSPISSLi信号极性位(SPCR3.SSLiP)(i=0to3)值。

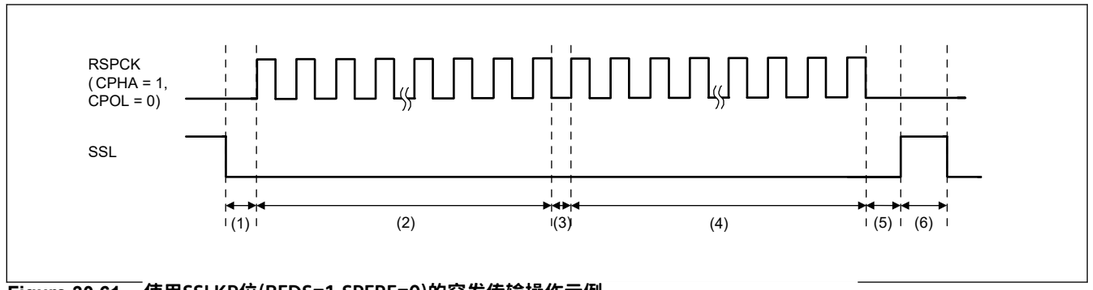


Figure 30.61 使用SSLKP位(BFDS=1 SPFRF=0)的突发传输操作示例

1.置位SSL信号并根据SPMD0插入一个RSPCK延迟。RSPCK延迟仅插入
突发传输的第一帧。

2.根据SPMD0进行串行传输。

3.由于不是最后一帧，所以保留了SPCMD0处的SSL信号值。帧之间的RSPCK否定是下一帧的0.5RSPCK。

4.根据SPMD1进行串行传输。

5.为最后一帧插入SSL否定延迟。

6.SSL信号被否定。此外，根据SPMD1插入下一个访问延迟。

Note: 最后一帧：当SPCR2.RMFM[4:0]≠00h时，由RMFM[4:0]位设置的帧
或者，已接受SPCR2.RMEDTG=1的帧。

[In the TI-SSP case]

RSPI在串行传输开始时将SSL信号置为一个周期。

通过在下一次串行传输（突发传输）开始时将SSL信号置为一个周期，可以连续执行串行传输。

●当RSPI命令寄存器(SPCMD)的SSL信号电平保持位(SSLKP)为1且突发传输时
RSPI控制寄存器（SPCR）的帧延迟选择位（BFDS）为1，SPCMD0到SPCMD1如图30.62所示。以下是使用设置实现突发传输时SSL信号操作和串行数据MISOMOSI的示例。SSL输出信号极性取决于设置的RSPISSLi信号极性位(SPCR3.SSLiP)(i=0to3)值。

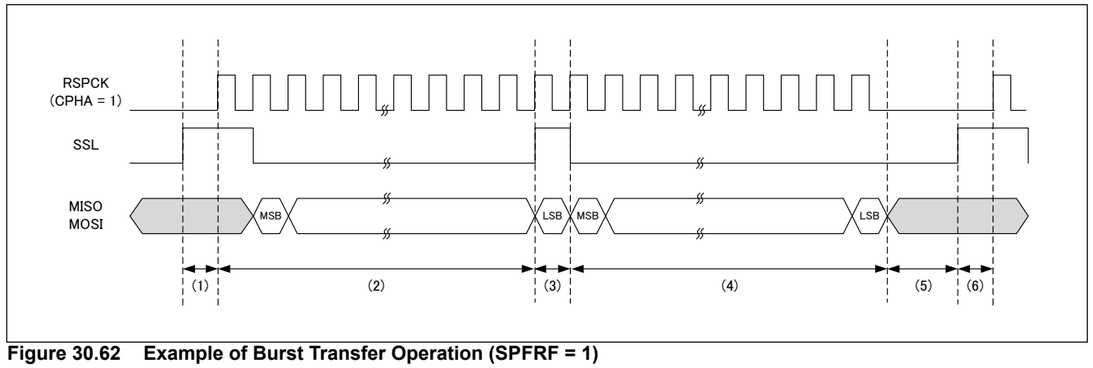


Figure 30.62 Example of Burst Transfer Operation (SPFRF = 1)

1. Assert the SSL signal and insert an RSPCK delay according to SPCMD0. The RSPCK delay is inserted only the first frame of burst transmission.
2. Perform serial transfer according to SPCMD0.
3. Final data transfer and SSL assertion are performed simultaneously.
4. Perform serial transfer according to SPCMD1.
5. Insert OE negate delay for the last frame.
6. Insert the next access delay according to SPCMD1.

Note: Last frame: Frame set by RMFM [4:0] bits when SPCR2.RMFM [4:0] ≠ 00h
Or, a frame in which SPCR2.RMEDTG = 1 has been accepted.
If the SSL signal output setting between the SPCMDs used for burst transfer differs from the SSL signal output setting, RSPI switches the SSL signal state when the SSL signal corresponding to the next transfer command is asserted (5). Note that, if an SSL signal change like this takes place, slaves that drive the MISO signal may conflict with each other, which may cause collision of signal level.

(5) RSPCK delay (t1)

The RSPCK delay value of the SPI in master mode depends on the SPCMDm.SCKDEN bit setting and the SPDECR.SCKDL[2:0] bits setting. The SPI determines the SPCMDm register to be referenced during a serial transfer by pointer control, and determines an RSPCK delay using the SPCMDm.SCKDEN bit and SPDECR.SCKDL[2:0] bits, as listed in Table 30.10. For a definition of RSPCK delay, see section 30.3.5. Transfer Formats.

RSPCK delay insert to only the first frame of burst transmission, when transmit without “Between Burst Transfer Frames Delay”. (The SPCMD.SSLKP bit is 1 and the SPCR.BFDS bit is 1.)

Table 30.10 Relationship between the SPCMDm.SCKDEN bit, SPDECR.SCKDL[2:0] bits, and RSPCK delay

SPCMDm.SCKDEN bit	SPDECR.SCKDL[2:0] bits	RSPCK delay	
		Motorola-SPI	TI-SSP
0	000b to 111b	1 RSPCK	0 RSPCK
1	000	1 RSPCK	1 RSPCK
	001	2 RSPCK	2 RSPCK
	010	3 RSPCK	3 RSPCK
	011	4 RSPCK	4 RSPCK
	100	5 RSPCK	5 RSPCK
	101	6 RSPCK	6 RSPCK
	110	7 RSPCK	7 RSPCK
	111	8 RSPCK	8 RSPCK

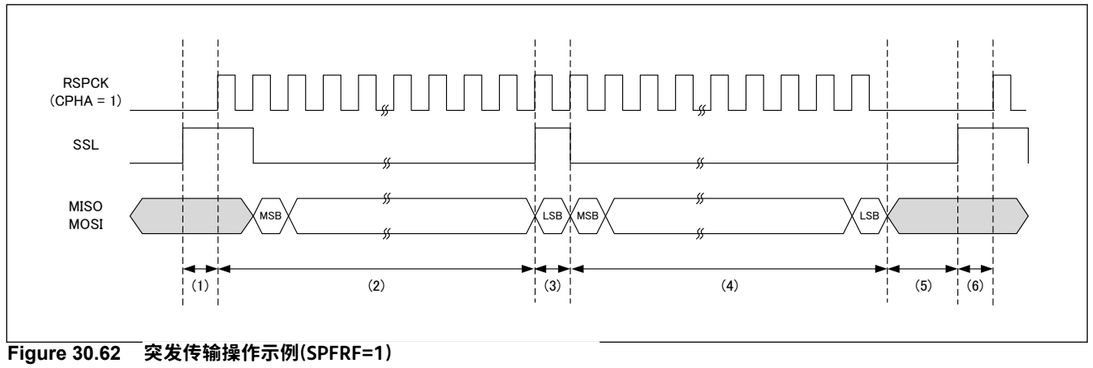


Figure 30.62 突发传输操作示例(SPFRF=1)

1.置位SSL信号并根据SPMD0插入一个RSPCK延迟。RSPCK延迟仅插入突发传输的第一帧。

2.根据SPMD0进行串行传输。

3.最终数据传输和SSL断言同时进行。

4.根据SPMD1进行串行传输。

5.为最后一帧插入OE否定延迟。

6.根据SPMD1插入下一个访问延迟。

Note: 最后一帧：当SPCR2.RMFM[4:0]≠00h时，由RMFM[4:0]位设置的帧或者，已接受SPCR2.RMEDTG=1的帧。
如果用于突发传输的SPCMD之间的SSL信号输出设置与SSL信号输出设置不同，则当对应于下一个传输命令的SSL信号被断言时，RSPI切换SSL信号状态(5)。请注意，如果发生这样的SSL信号变化，驱动MISO信号的从机可能会相互冲突，从而可能导致信号电平冲突。

(5) RSPCK delay (t1)

主机模式下SPI的RSPCK延迟值取决于SPMDm.SCKDEN位设置和SPDECR.SCKDL[2:0]位设置。SPI通过指针控制确定串行传输期间要引用的SPCMDm寄存器，并使用SPCMDm.SCKDEN位和SPDECR.SCKDL[2:0]位确定RSPCK延迟，如表30.10中所列。有关RSPCK延迟的定义，请参见第30.3.5节。传输格式。

当没有“BetweenBurstTransferFrames”传输时，RSPCK延迟仅插入到突发传输的第一帧延迟”。（SPCMD.SSLKP位为1，SPCR.BFDS位为1。）

Table 30.10 SPMDm.SCKDEN位、SPDECR.SCKDL[2:0]位和RSPCK延迟之间的关系

SPCMDm.SCKDEN bit	SPDECR.SCKDL[2:0] bits	RSPCK delay	
		Motorola-SPI	TI-SSP
0	000b to 111b	1 RSPCK	0 RSPCK
1	000	1 RSPCK	1 RSPCK
	001	2 RSPCK	2 RSPCK
	010	3 RSPCK	3 RSPCK
	011	4 RSPCK	4 RSPCK
	100	5 RSPCK	5 RSPCK
	101	6 RSPCK	6 RSPCK
	110	7 RSPCK	7 RSPCK
	111	8 RSPCK	8 RSPCK

(6) SSL negation delay (t2)

The SSL negation delay value of the SPI in master mode depends on the SPCMDm.SLNDEN bit setting and the SPDECR.SLNDL[2:0] bits setting. The SPI determines the SPCMDm register to be referenced by pointer control during a serial transfer, and determines an SSL negation delay using the SPCMDm.SLNDEN bit and SPDECR.SLNDL[2:0] bits, as listed in Table 30.11. For a definition of SSL negation delay, see section 30.3.5. Transfer Formats.

An SSL negation delay is inserted to only the last frame of the burst transmission, that is, transmit without between burst transfer frames delay. (SPCMD.SSLKP bit is 1 and SPCR.BFDS bit is 1).

Table 30.11 Relationship between the SPCMDm.SLNDEN bit, SPDECR.SLNDL[2:0] bits, and SSL negation delay

SPCMDm.SLNDEN bit	SPDECR.SLNDL[2:0] bits	SSL negation delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(7) Next-access delay (t3)

The next-access delay value of the SPI in master mode depends on the SPCMDm.SPNDEN bit setting and the SPDECR.SPNDL[2:0] bits setting. The SPI determines the SPCMDm register to be referenced during serial transfer by pointer control, and then determines a next-access delay during serial transfer using the SPCMDm.SPNDEN bit and SPDECR.SPNDL[2:0] bits, as listed in Table 30.12. For a definition of next-access delay, see section 30.3.5. Transfer Formats.

A next-Access delay is inserted to only the last frame of the burst transmission, that is, transmit without between burst transfer frames delay. (SPCMD.SSLKP bit is 1 and SPDR.BFDS bit is 1).

Table 30.12 Relationship between the SPCMDm.SPNDEN bit, SPDECR.SPNDL[2:0] bits, and next-access delay

SPCMDm.SPNDEN bit	SPDECR.SPNDL[2:0] bits	Next-access delay
0	000b to 111b	1 RSPCK + 5 TCLK
1	000b	1 RSPCK + 5 TCLK
	001b	2 RSPCK + 5 TCLK
	010b	3 RSPCK + 5 TCLK
	011b	4 RSPCK + 5 TCLK
	100b	5 RSPCK + 5 TCLK
	101b	6 RSPCK + 5 TCLK
	110b	7 RSPCK + 5 TCLK
	111b	8 RSPCK + 5 TCLK

(8) Initialization flow

Figure 30.63 shows an example of SPI initialization flow when the SPI is in master mode. For information on how to set up the Interrupt Controller Unit (ICU), DMAC and I/O ports, see the descriptions given in the individual blocks.

(6) SSL否定延迟(t2)

主模式下SPI的SSL否定延迟值取决于SPMDm.SLNDEN位设置和SPDECR.SLNDL[2:0]位设置。SPI确定串行传输期间指针控制要引用的SPCMDm寄存器，并使用SPCMDm.SLNDEN位和SPDECR.SLNDL[2:0]位确定SSL否定延迟，如表30.11中所列。有关SSL否定延迟的定义，请参阅第30.3.5节。传输格式。

仅在突发传输的最后一帧中插入SSL否定延迟，即在突发传输帧之间没有延迟的传输。（SPCMD.SSLKP位为1，SPCR.BFDS位为1）。

Table 30.11 SPCMDm.SLNDEN位、SPDECR.SLNDL[2:0]位和SSL否定延迟之间的关系

SPCMDm.SLNDEN bit	SPDECR.SLNDL[2:0] bits	SSL否定延迟
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(7) Next-access delay (t3)

主机模式下SPI的下一次访问延迟值取决于SPMDm.SPNDEN位设置和SPDECR.SPNDL[2:0]位设置。SPI通过指针控制确定串行传输期间要引用的SPCMDm寄存器，然后使用SPCMDm.SPNDEN位和SPDECR.SPNDL[2:0]位确定串行传输期间的下一次访问延迟，如表30.12中所列。有关下一次访问延迟的定义，请参见第30.3.5节。转移

Formats.

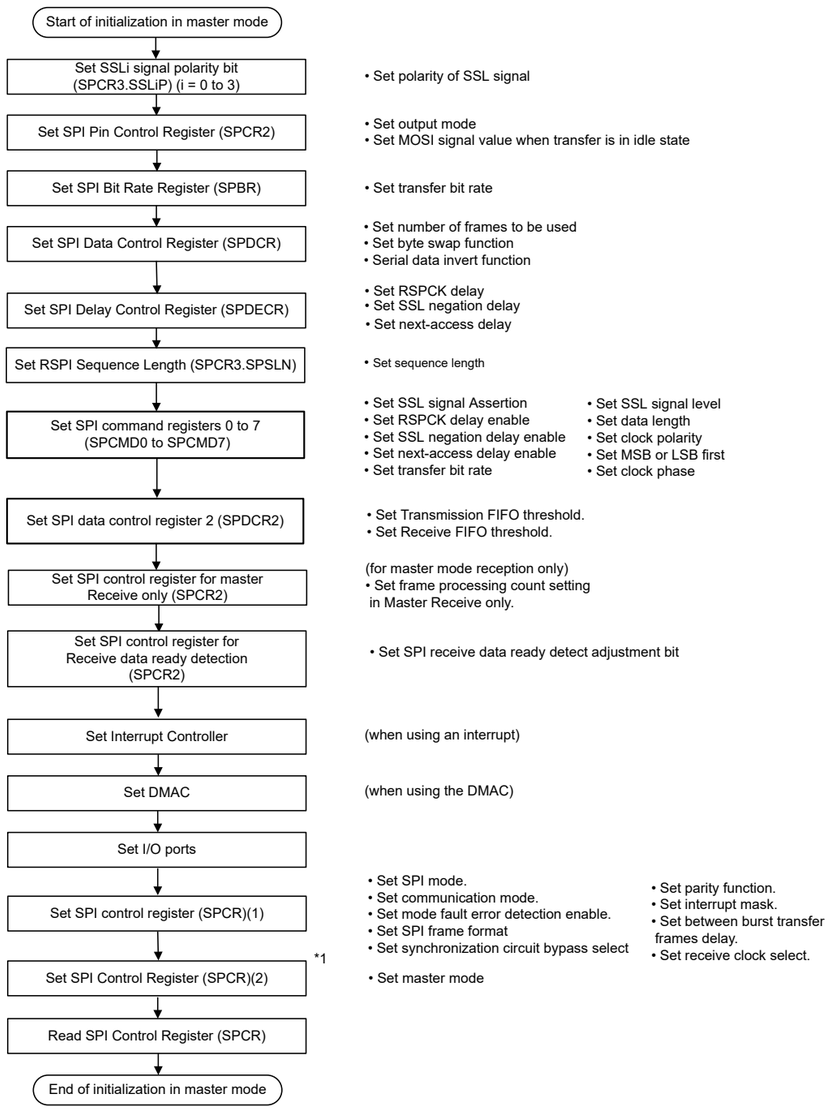
仅在突发传输的最后一帧中插入下一个访问延迟，即在突发传输帧之间没有延迟进行传输。（SPCMD.SSLKP位为1，SPDR.BFDS位为1）。

Table 30.12 SPMDm.SPNDEN位、SPDECR.SPNDL[2:0]位和下一次访问延迟之间的关系

SPCMDm.SPNDEN bit	SPDECR.SPNDL[2:0] bits	Next-access delay
0	000b to 111b	1 RSPCK + 5 TCLK
1	000b	1 RSPCK + 5 TCLK
	001b	2 RSPCK + 5 TCLK
	010b	3 RSPCK + 5 TCLK
	011b	4 RSPCK + 5 TCLK
	100b	5 RSPCK + 5 TCLK
	101b	6 RSPCK + 5 TCLK
	110b	7 RSPCK + 5 TCLK
	111b	8 RSPCK + 5 TCLK

(8) 初始化流程

图30.63显示了SPI处于主机模式时的SPI初始化流程示例。有关如何设置中断控制器单元(ICU)、DMAC和IO端口的信息，请参见各个块中给出的说明。



Note 1. Regarding the setting of the SPI control register(SPCR), leave an interval of 1TCLK between setting(1) (initial setting other than MSTR bit) and setting(2) (MSTR setting).

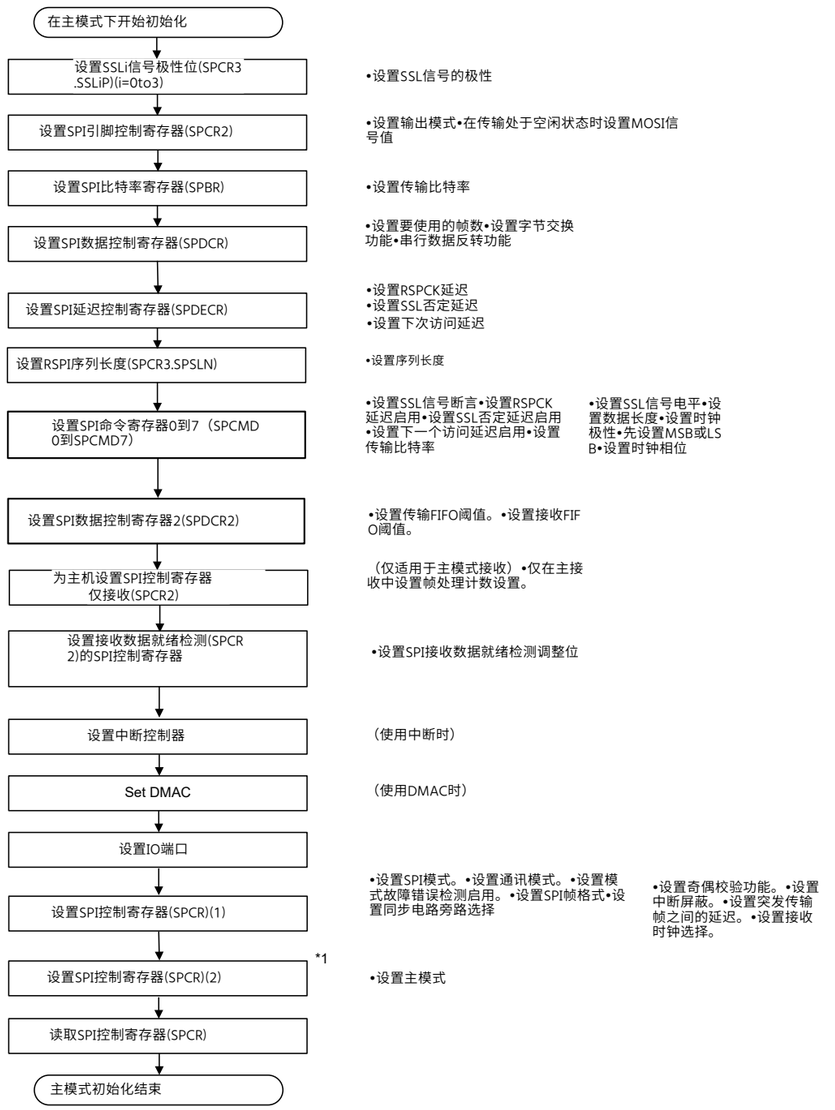
Figure 30.63 Example of initialization flow in master mode for SPI operation

(9) Software processing flow

Figure 30.64 to Figure 30.67 show examples of the software processing flow.

Transmit processing flow

When transmitting data, with the SPIi_SPII or SPCI interrupt enabled, the CPU is notified of the completion of data transmission after the last data write for transmission.



注1.关于SPI控制寄存器（SPCR）的设置，在设置（1）（MSTR位以外的初始设置）和设置（2）（MSTR设置）之间留出1TCLK的间隔。

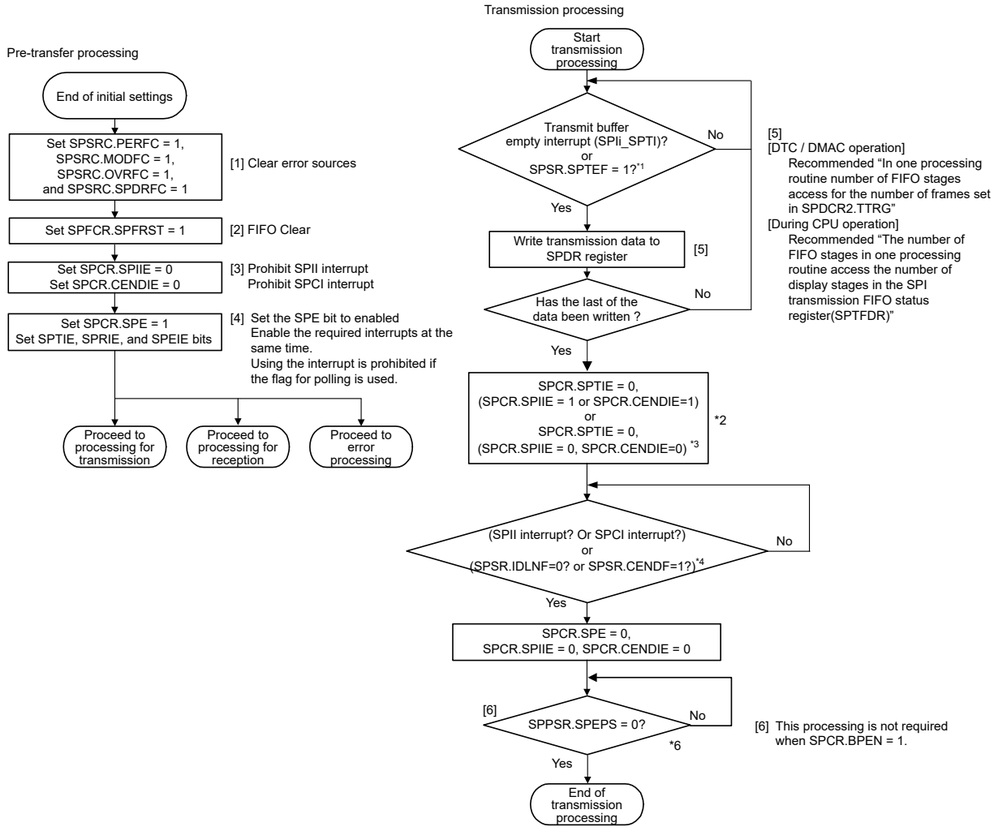
Figure 30.63 SPI操作的主模式初始化流程示例

(9) 软件处理流程

图30.64至图30.67显示了软件处理流程的示例。

传输处理流程

发送数据时，在SPIi_SPII或SPCI中断使能的情况下，在最后一次发送数据写入后通知CPU数据发送完成。

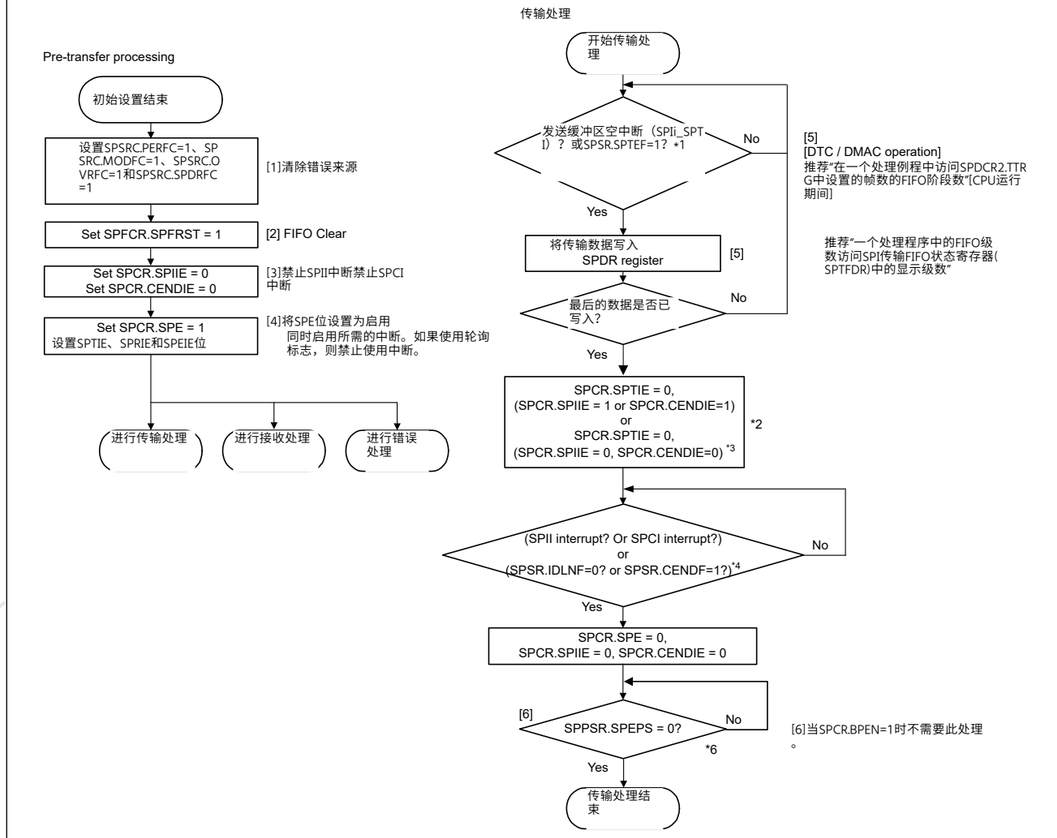


Note 1. Proceed to process of writing data for transmission after reading SPSR.SPTEF flag is 1, if the user uses the flag for polling.
Note 2. The user can know the communication end by SPII interrupt (IDLNF flag) or SPCI interrupt (CENDF flag). Please use either SPII interrupt (IDLNF flag) or SPCI interrupt (CENDF flag).
Note 3. Set SPII interrupt prohibited (SPCR.SPIIE = 0) and SPCI interrupt prohibited (SPCR.CENDIE = 0), if the user uses the flag for polling.
Note 4. Wait more than 1 PCLK, after writing data for transmission to SPDR, and before starting polling of SPSR.IDLNF or SPSR.CENDF, if the user uses the flag for polling.
Note 5. During CPU operation, Write 1 to SPI transmit buffer empty flag clear bit (SPSRC.SPTEFC) after one processing routine.
Note 6. When setting to 0 in slave mode and SPCR.BPEN = 0, check that SPPSR.SPEPS has become 0.(Not required when BPEN = 1.)

Figure 30.64 Transmission flow in master mode

Receive processing flow

The SPI has receive only operation in slave mode.



注1.如果用户使用该标志进行轮询，则读取SPSR.SPTEF标志为1后，继续写入发送数据处理。

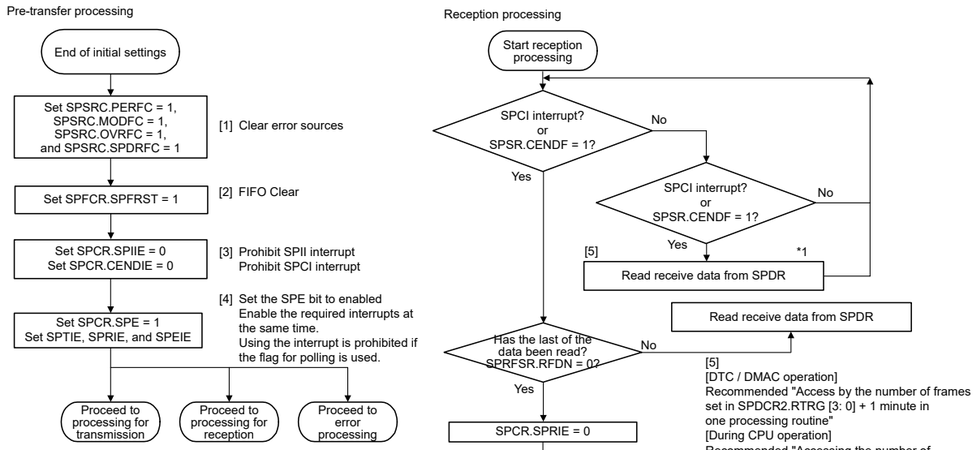
注2.用户可以通过SPII中断（IDLNF标志）或SPCI中断（CENDF标志）知道通讯结束。请使用SPII中断（IDLNF标志）或SPCI中断（CENDF标志）。
注3.如果用户使用该标志进行轮询，则设置SPII中断禁止(SPCR.SPIIE=0)和SPCI中断禁止(SPCR.CENDIE=0)。

注4.等待超过1个PCLK，在写入数据以传输到SPDR之后，在开始轮询SPSR.IDLNF或之前SPSR.CENDF，如果用户使用该标志进行轮询。
注5.在CPU运行期间，在一个处理程序后将1写入SPI发送缓冲区空标志清除位(SPSRC.SPTEFC)。
注6.在从机模式下设置为0且SPCR.BPEN=0时，请检查SPPSR.SPEPS是否已变为0。（当BPEN = 1.)

Figure 30.64 主模式下的传输流

接收处理流程

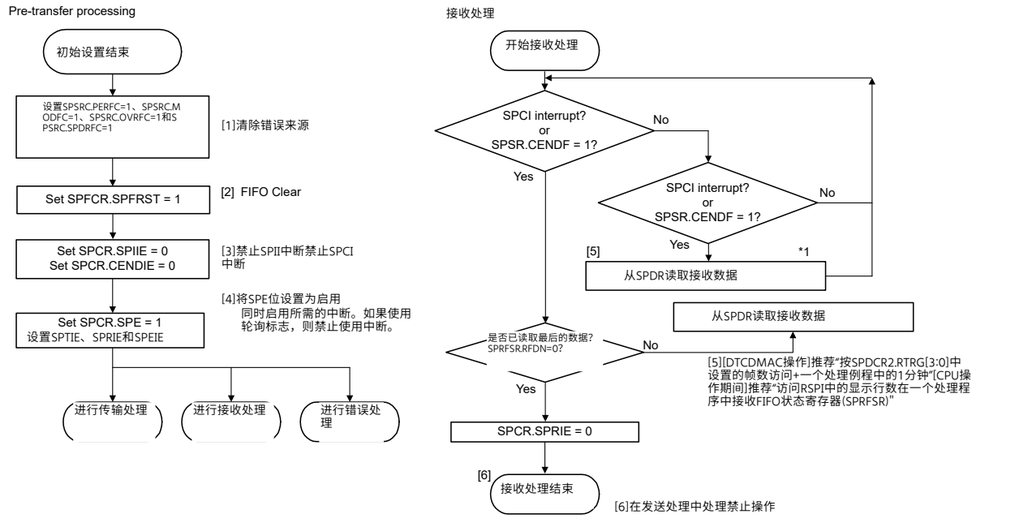
SPI在从机模式下仅接收操作。



Note 1. During CPU operation, write 1 to the SPSCLR.SPRFC bit (RSPI receive buffer full flag clear bit) after one processing routine.

Figure 30.65 Reception flow in master mode

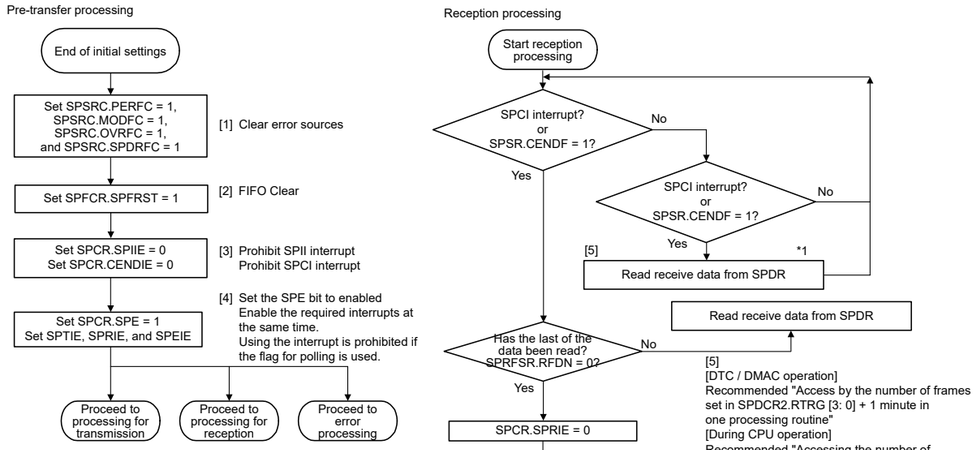
Receive only processing flow in master mode



注1.在CPU运行期间，在一个处理程序后将1写入SPSCLR.SPRFC位（RSPI接收缓冲区满标志清除位）。

Figure 30.65 主模式下的接收流程

在主模式下仅接收处理流



Note 1. The end of communication can be determined by the SPCI interrupt (CENDF flag). Use the SPCI interrupt (CENDF flag).
Note 2. Disable SPCI interrupt (SPCR.CENDIE = 0) during flag polling.
Note 3. A communication completion interrupt at reception only operation (Master) occurs at a predetermined timing under any of the following conditions.
- Frame number processing set by RMFM completed (RMFM [4:0] ≠ 0x0)
- RMEDTG = 1, when processing of the number of frames set by RMFM is not completed (including RMFM [4:0] = 0x0)

Note 4. Internal trigger is also cleared.
Note 5. During CPU operation, write 1 to the RSPI receive buffer full flag clear bit (SPSRC.SPRFC) after one processing routine.

Figure 30.66 Software Processing Flowchart in Master Mode (Reception-only)

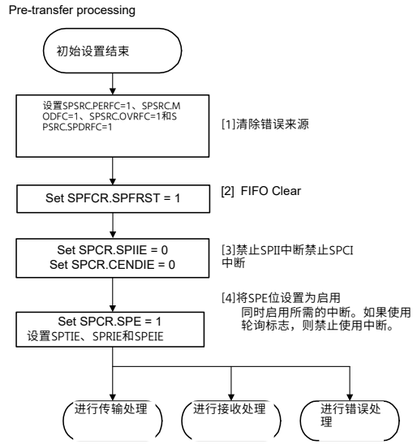
Error processing flow

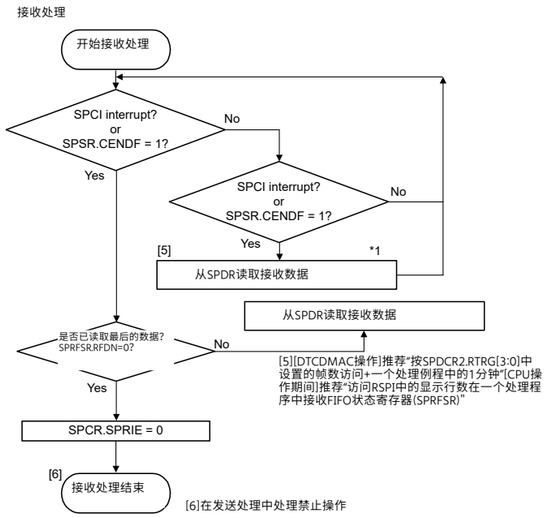
The SPI detects the following errors:

- Mode fault error
- Underrun error
- Overrun error
- Parity error

When a mode fault error is generated, the SPCR.SPE bit is automatically cleared, stopping operations for transmission and reception. For errors from other sources, the SPCR.SPE bit is not cleared and operations for transmission and reception continue. Therefore, Renesas recommends clearing the SPCR.SPE bit to stop operations for errors other than mode fault errors. Not doing so leads to updating of the SPDCR2.SPECM[2:0] bits.

When an error is detected using an interrupt, clear the ICU.IELSRn.IR flag in the error processing routine. If this is not done, the ICU.IELSRn.IR flag might continue to indicate the SPIi_SPTI or SPIi_SPRI interrupt request. If the SPIi_SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the SPI.





注1.通信结束可以由SPCI中断（CENDF标志）决定。使用SPCI中断（CENDF标志）。
注2.在标志轮询期间禁用SPCI中断(SPCR.CENDIE=0)。
注3.仅接收操作（主机）的通信完成中断在以下任何条件下在预定时间发生。●

由RMFM设置的帧号处理完成(RMFM[4:0]≠0x0)
- RMEDTG=1，当RMFM设置的帧数处理未完成时（包括RMFM[4:0]=0x0）

注4.内部触发也被清除。
注5.在CPU运行期间，在一个处理程序后将1写入RSPI接收缓冲区满标志清除位(SPSRC.SPRFC)。

Figure 30.66 主控模式下的软件处理流程图（仅接收）

错误处理流程

SPI检测到以下错误：

●模式故障错误
- Underrun error

●超限错误
●奇偶校验错误

当产生模式故障错误时，SPCR.SPE位自动清零，停止发送和接收操作。对于其他来源的错误，SPCR.SPE位不会被清除，发送和接收操作会继续。因此，瑞萨建议清除SPCR.SPE位以停止除模式故障错误以外的错误操作。不这样做会导致更新SPDCR2.SPECM[2:0]位。

当使用中断检测到错误时，清除错误处理例程中的ICU.IELSRn.IR标志。如果不这样做，ICU.IELSRn.IR标志可能会继续指示SPIi_SPTI或SPIi_SPRI中断请求。如果指示了SPIi_SPRI中断请求，则读取接收缓冲区并初始化SPI中的定序器。

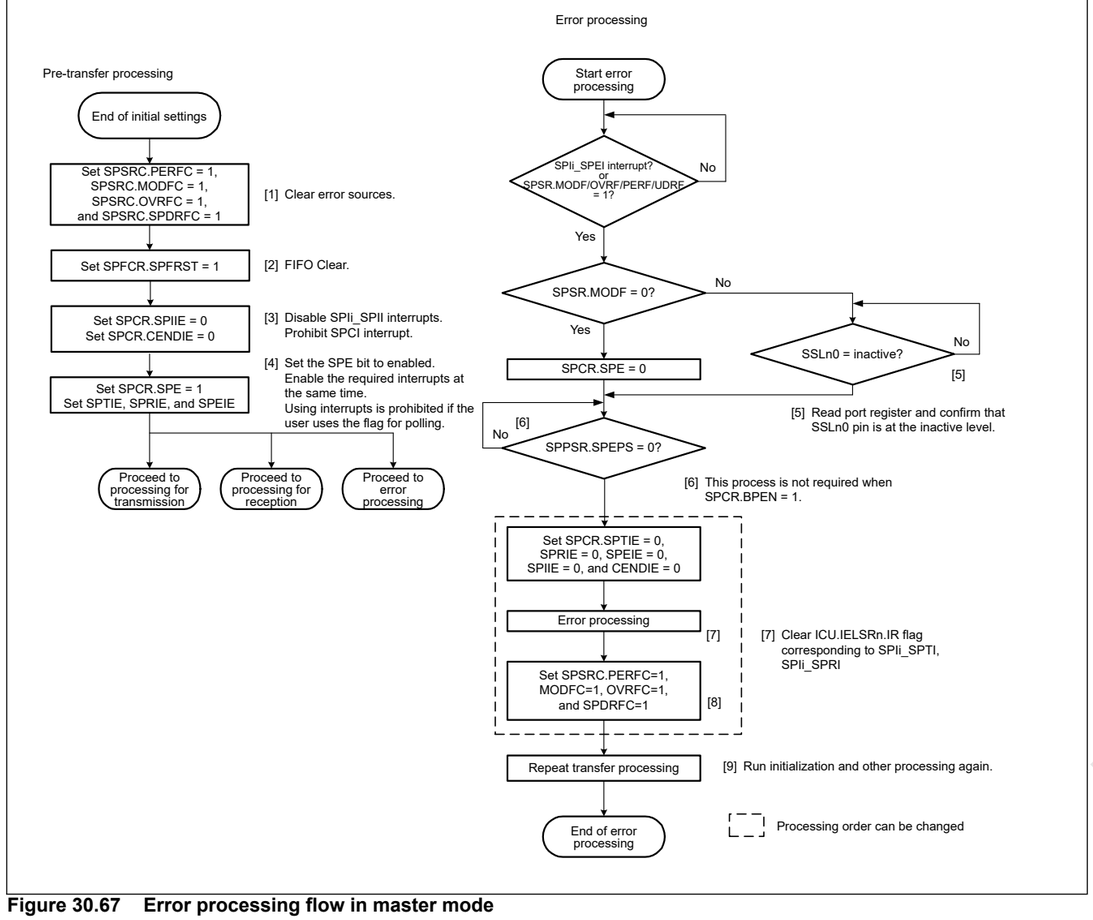


Figure 30.67 Error processing flow in master mode

30.3.12.2 Slave mode operation

(1) Starting a serial transfer

When the SPCMD0.CPHA bit is 0, if the SPI detects an SSLn0 input signal assertion, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 0, the assertion of the SSLn0 input signal triggers the start of a serial transfer.

When the CPHA bit is 1, if the SPI detects the first RSPCKn edge in an SSLn0 signal asserted condition, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 1, the first RSPCKn edge in an SSLn0 signal asserted condition triggers the start of a serial transfer.

Regardless of the CPHA bit setting, the SPI drives the MISOn output signal on SSLn0 signal assertion. The data that is output by the SPI is either valid or invalid, depending on the CPHA bit setting.

For details on the SPI transfer format, see section 30.3.5. Transfer Formats. The polarity of the SSLn0 input signal depends on the SPCR3.SSL0P setting.

(2) Terminating a serial transfer

Regardless of the SPCMD0.CPHA bit setting, the SPI terminates the serial transfer after detecting an RSPCKn edge corresponding to the final sampling timing. When the number of data stored in the receive FIFO is less than the number of FIFO stages, on termination of serial transfer, the SPI copies received data from the shift register to the receive buffer of the SPDR register. On termination of a serial transfer, the SPI changes the status of the shift register to empty, regardless of the

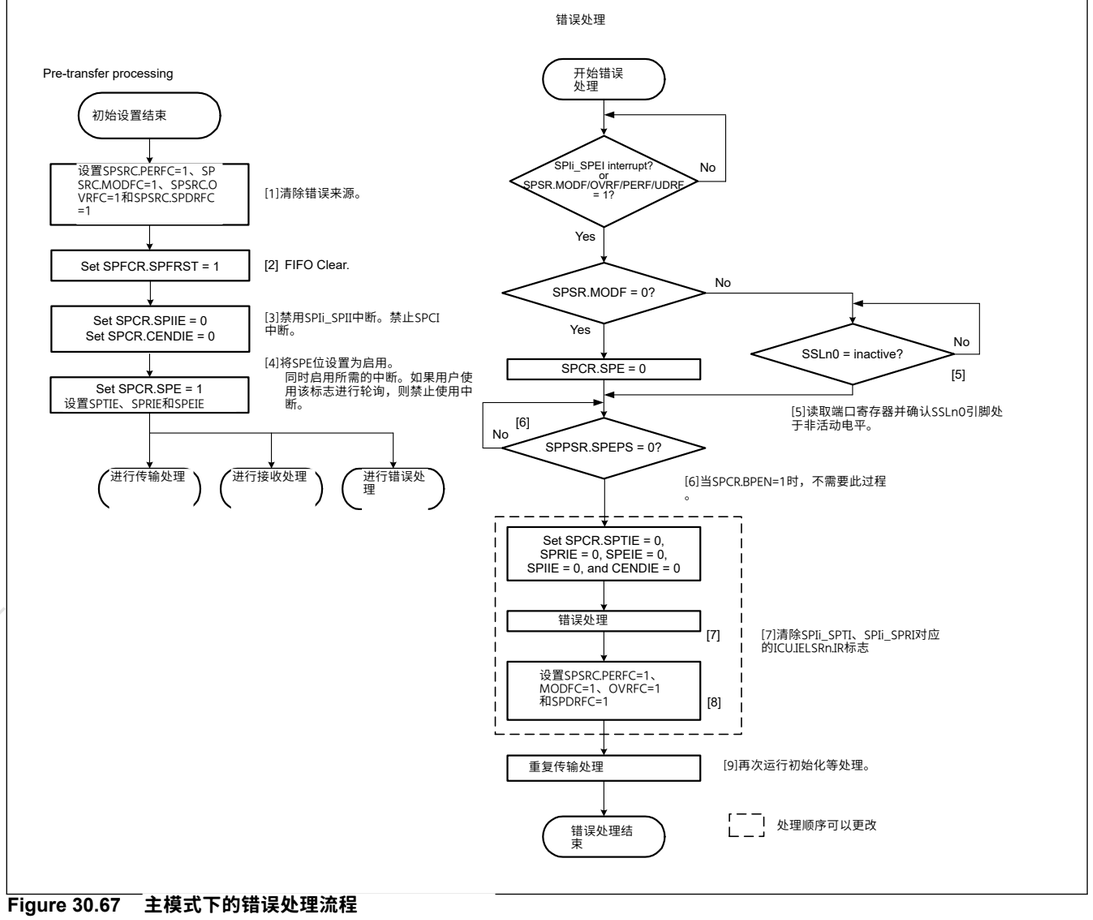


Figure 30.67 主模式下的错误处理流程

30.3.12.2 从模式操作

(1) 开始串行传输

当SPCMD0.CPHA位为0时，如果SPI检测到SSLn0输入信号断言，它必须将有效数据驱动到MISOn输出信号。因此，当CPHA位为0时，SSLn0输入信号的断言触发串行传输的开始。

当CPHA位为1时，如果SPI在SSLn0信号置位条件下检测到第一个RSPCKn边沿，它必须将有效数据驱动到MISOn输出信号。因此，当CPHA位为1时，SSLn0信号断言条件中的第一个RSPCKn边沿触发串行传输的开始。

无论CPHA位设置如何，SPI都会在SSLn0信号置位时驱动MIOn输出信号。SPI输出的数据是有效还是无效，取决于CPHA位设置。

有关SPI传输格式的详细信息，请参见第30.3.5节。传输格式。SSLn0输入信号的极性取决于SPCR3.SSL0P设置。

(2) 终止串行传输

无论SPCMD0.CPHA位设置如何，SPI在检测到对应于最终采样时序的RSPCKn边沿后终止串行传输。当接收FIFO中存储的数据数量小于FIFO级数时，在串行传输终止时，SPI将接收到的数据从移位寄存器复制到SPDR寄存器的接收缓冲区。在串行传输终止时，SPI将移位寄存器的状态更改为空，而不管

receive buffer state. A mode fault error occurs if the SPI detects an SSLn0 input signal negation from the beginning of serial transfer to the end of serial transfer (see section 30.3.10. Error Detection).

The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length is determined by the SPCMD0.SPB[4:0] bits setting. The polarity of the SSLn0 input signal is determined by the SPCR3.SSL0P bit setting. For details on the SPI transfer format, see section 30.3.5. Transfer Formats.

(3) Notes on single-slave operations

[In the Motorola-SPI case]

If the SPCMD0.CPHA bit is 0, the SPI starts serial transfers when it detects the assertion edge for an SSLn0 input signal. In the configuration shown in Figure 30.8, if the SPI is used in single-slave mode, the SSLn0 signal is fixed at an active state. Therefore, when the CPHA bit is set to 0, the SPI cannot correctly start a serial transfer. For the SPI to correctly execute transmit and receive operations in slave mode when the SSLn0 input signal is fixed at an active state, the CPHA bit must be set to 1. Do not fix the SSLn0 input signal if there is a requirement for setting the CPHA bit to 0.

[In the TI-SSP case]

When RSPI is used as a single slave in the configuration shown in the Figure 30.7, the SSL0 input signal is always fixed to the inactive state, so the SPI cannot start the serial transfer.

When using a single slave, use the configuration shown in the example in Figure 30.6.

(4) Burst transfer

[In the Motorola-SPI case]

If the SPCMD0.CPHA bit is 1, continuous serial transfer (burst transfer) can be executed while retaining the assertion state for the SSLn0 input signal. When the CPHA bit is 1, the serial transfer period is the period from the first RSPCKn edge to the sampling timing for the reception of the final bit in an SSLn0 signal active state. Even when the SSLn0 input signal remains at the active level, the SPI can accommodate burst transfers, because it can detect the start of an access.

When the CPHA bit is 0, the second and subsequent serial transfers during burst transfer cannot be executed correctly.

[In the TI-SSP case]

In serial transfer, data transfer starts after the SSL input signal is asserted for RSPCK 1 cycle. Since frame transfer starts from the SSL input signal, SSL must be asserted between frames.

(5) Initialization flow

Figure 30.68 shows an example of initialization flow for SPI operation when the SPI is in slave mode. For a description of how to set up the ICU, DTC, and I/O ports, see the descriptions given in the individual blocks.

接收缓冲区状态。如果SPI从串行传输开始到串行传输结束检测到SSLn0输入信号取反，则会发生模式故障错误（请参阅第30.3.10节。错误检测）。

最终的采样时序根据传输数据的位长而变化。在从机模式下，SPI数据长度由SPCMD0.SPB[4:0]位设置决定。SSLn0输入信号的极性由SPCR3.SSL0P位设置决定。有关SPI传输格式的详细信息，请参见第30.3.5节。传输格式。

(3) 单从操作注意事项

[In the Motorola-SPI case]

如果SPCMD0.CPHA位为0，则SPI在检测到SSLn0输入信号的断言边沿时开始串行传输。在图30.8所示的配置中，如果SPI用于单从模式，则SSLn0信号固定在激活状态。因此，当CPHA位设置为0时，SPI无法正确启动串行传输。当SSLn0输入信号固定为活动状态时，为了使SPI在从模式下正确执行发送和接收操作，CPHA位必须设置为1。如果需要设置CPHA，请不要固定SSLn0输入信号位为0。

[In the TI-SSP case]

在图30.7所示的配置中，当RSPI用作单从机时，SSL0输入信号始终固定为非活动状态，因此SPI无法启动串行传输。

使用单从机时，请使用图30.6示例中所示的配置。

(4) 突发传输

[In the Motorola-SPI case]

如果SPCMD0.CPHA位为1，则可以执行连续串行传输（突发传输），同时保持SSLn0输入信号的断言状态。当CPHA位为1时，串行传输周期是从第一个RSPCKn边沿到SSLn0信号有效状态下接收最后一个位的采样时序的周期。即使SSLn0输入信号保持在有效电平，SPI也可以适应突发传输，因为它可以检测访问的开始。

当CPHA位为0时，突发传输期间的第二次和后续串行传输无法正确执行。

[In the TI-SSP case]

在串行传输中，数据传输在SSL输入信号被断言为RSPCK1个周期后开始。由于帧传输从SSL输入信号开始，因此必须在帧之间断言SSL。

(5) 初始化流程

图30.68显示了SPI处于从模式时SPI操作的初始化流程示例。有关如何设置ICU、DTC和IO端口的说明，请参见各个块中给出的说明。

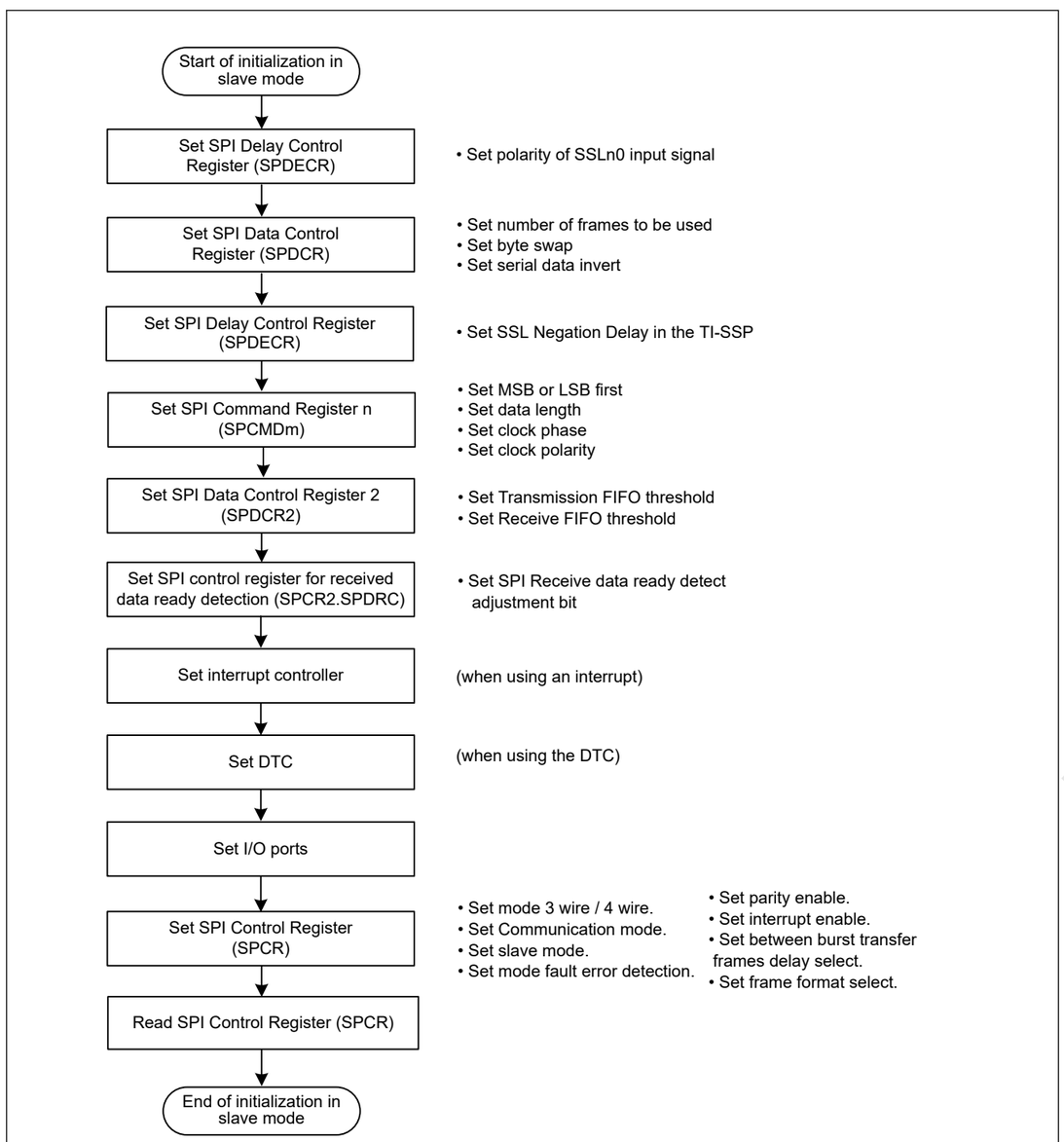


Figure 30.68 Example initialization flow in slave mode for SPI operation

(6) Software processing flow

Figure 30.69 to Figure 30.72 show examples of the flow of software processing.

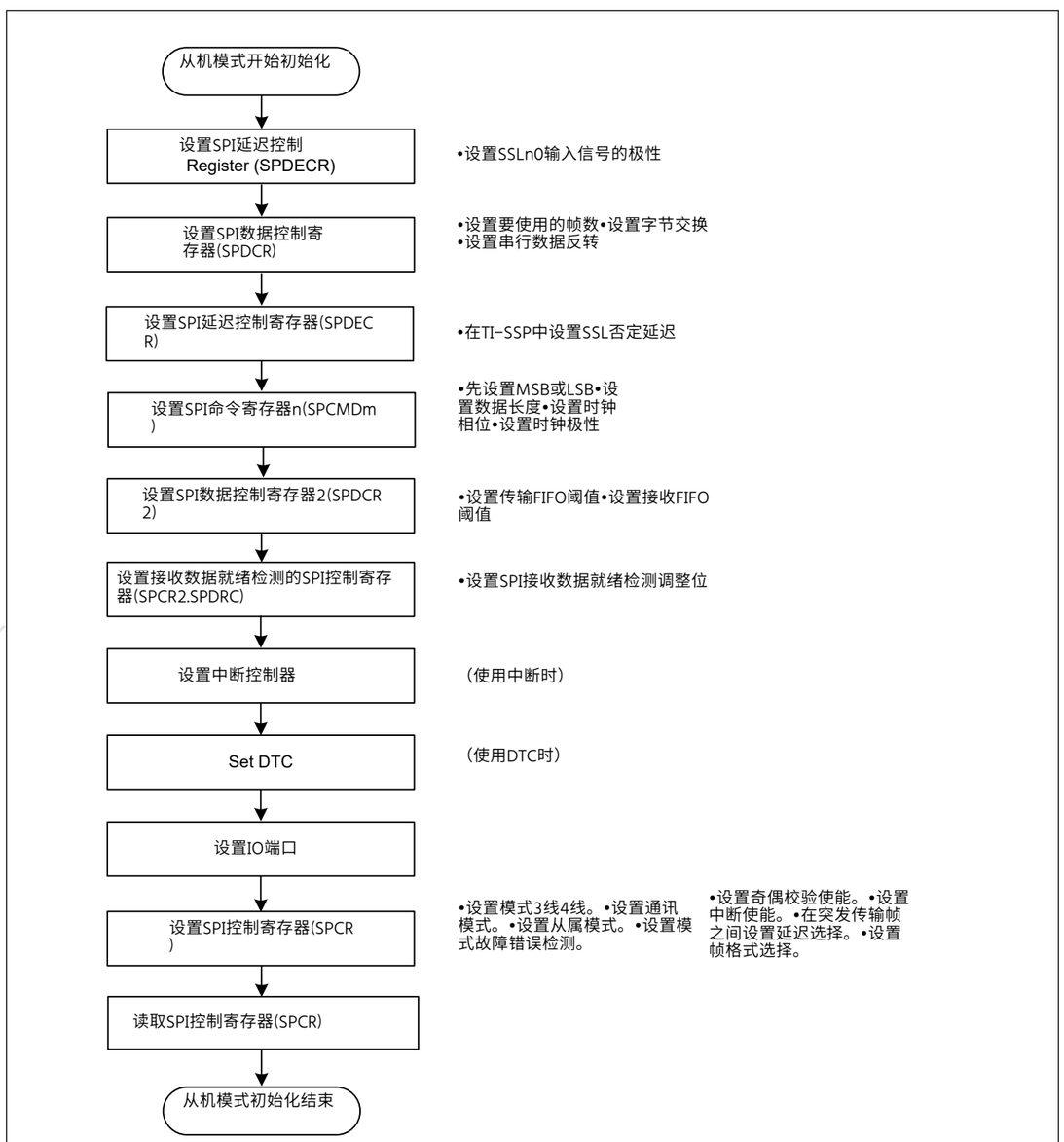
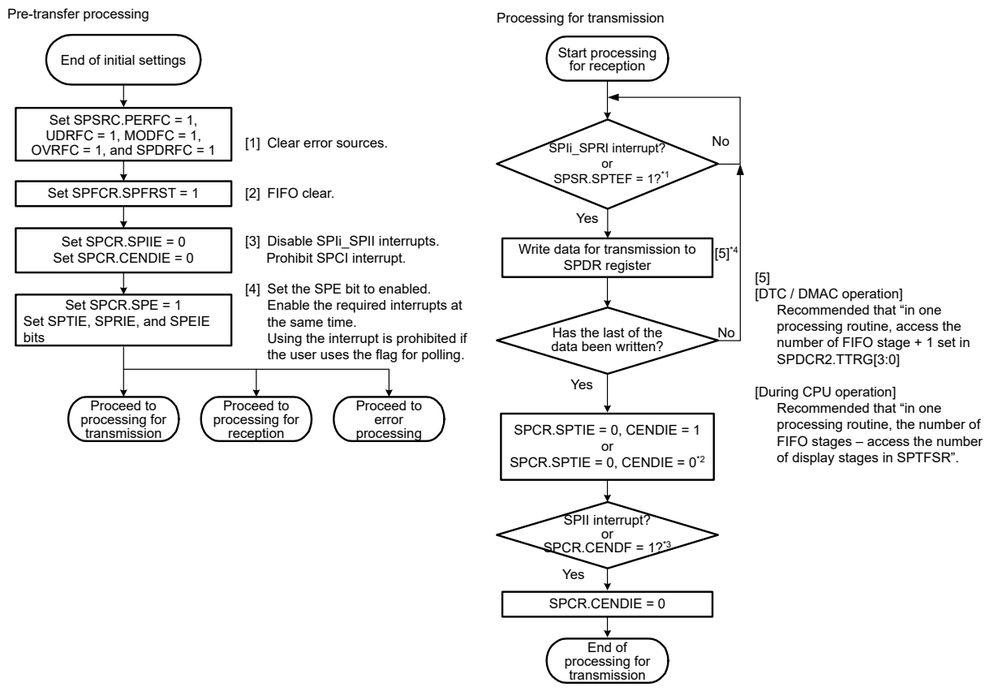


Figure 30.68 SPI操作的从模式初始化流程示例

(6) 软件处理流程

图30.69至图30.72显示了软件处理流程的示例。

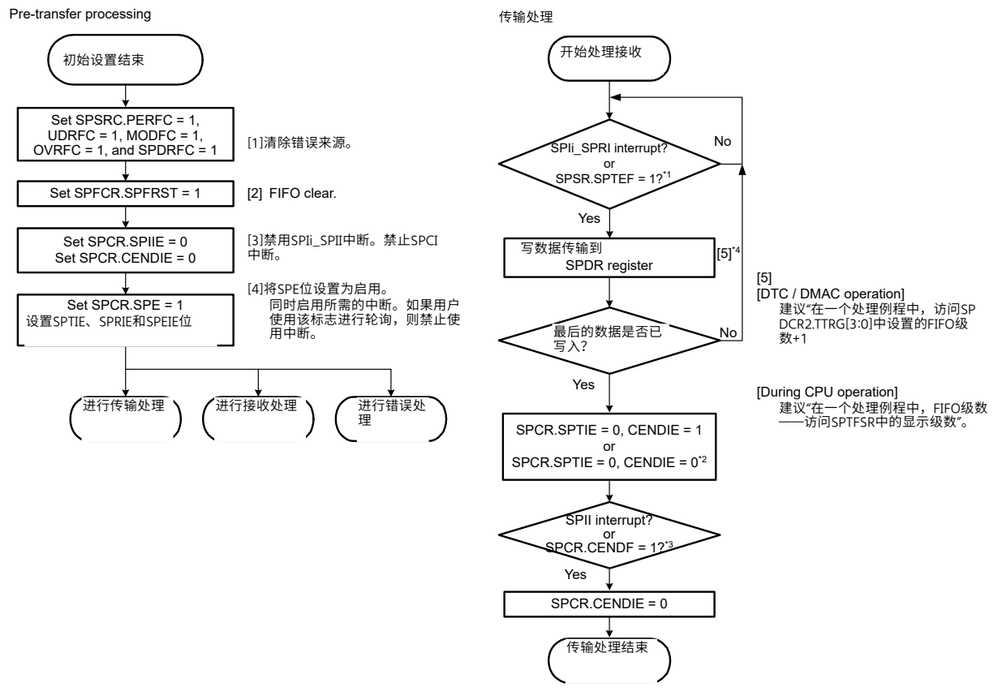
Transmit processing flow



Note 1. Before writing data for transmission to SPDR register, check the transmit buffer empty interrupt by reading SPSR.SPTEF flag, if the flag for polling is used.
Note 2. Set SPCI interrupt prohibited (SPCR.CENDIE = 0), if the user uses the flag for polling.
Note 3. Wait more than 1 PCLK, after writing data for transmission to SPDR, and before starting polling of SPSR.IDLNF or SPSR.CENDF, if the user uses the flag for polling.
Note 4. During CPU operation, Write 1 to RSPI transmit buffer empty flag clear bit (SPSRC.SPTEFC) after one processing routine.

Figure 30.69 Transmission flow in slave mode

传输处理流程

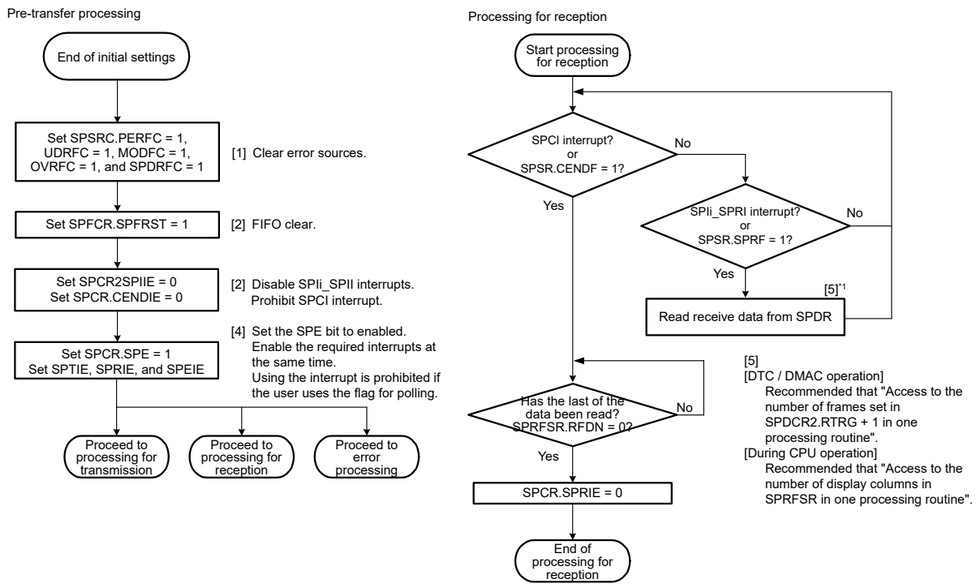


注1.在将数据写入SPDR寄存器之前，如果使用轮询标志，请通过读取SPSR.SPTEF标志检查发送缓冲区空中断。

注2.如果用户使用该标志进行轮询，则设置SPCI中断禁止(SPCR.CENDIE=0)。
注3.等待超过1个PCLK，在写入数据以传输到SPDR之后，在开始轮询SPSR.IDLNF或之前SPSR.CENDF，如果用户使用该标志进行轮询。
注4.在CPU运行期间，在一个处理程序后将1写入RSPI发送缓冲区空标志清除位(SPSRC.SPTEFC)。

Figure 30.69 从模式下的传输流

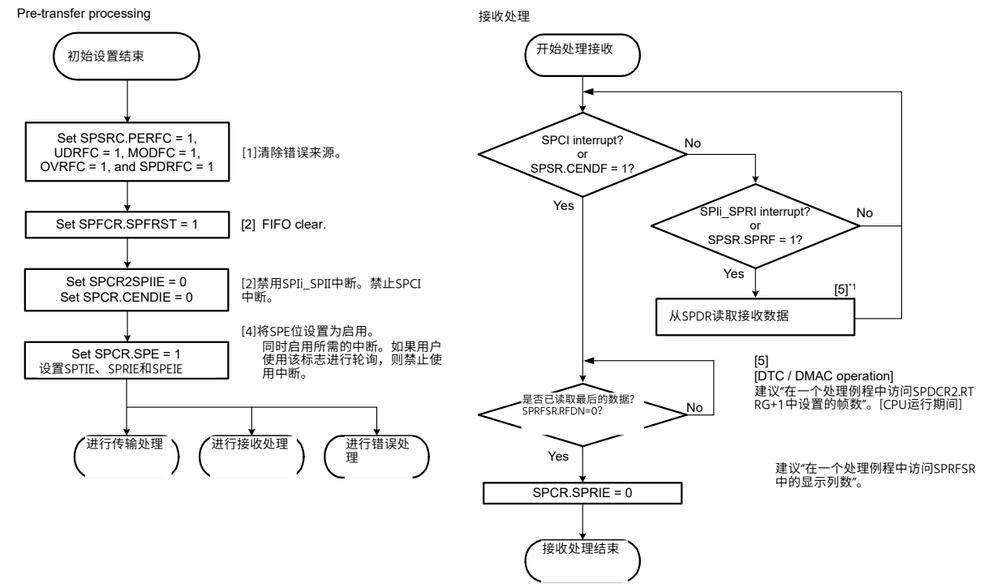
Receive processing flow



Note 1. During CPU operation, Write 1 to the RSPI receive buffer full flag clear bit (SPSRC.SPTEFC) after one processing routine.

Figure 30.70 Reception flow in slave mode

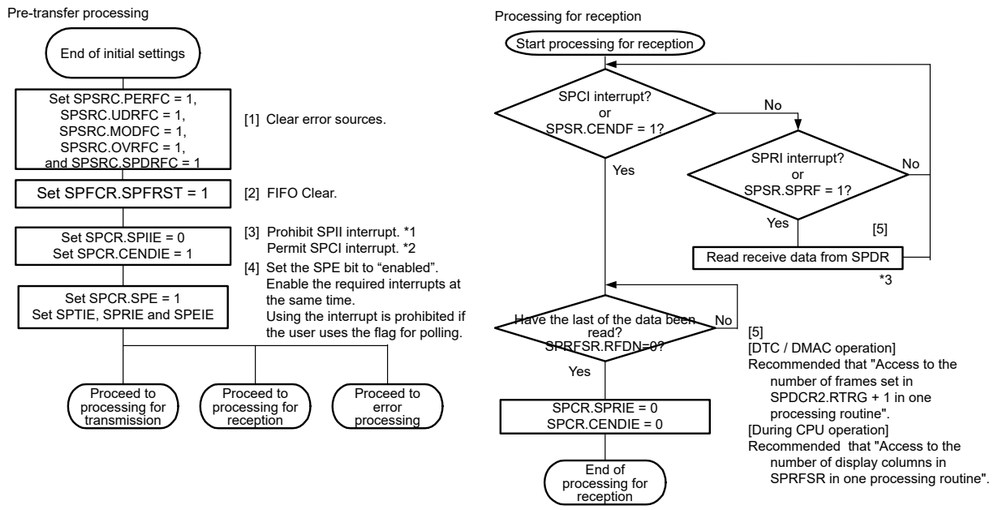
接收处理流程



注1.在CPU运行期间，在一个处理程序后将1写入RSPI接收缓冲区满标志清除位(SPSRC.SPTEFC)。

Figure 30.70 从机模式下的接收流程

Master Reception-only processing flow



Note 1. The end of communication can be determined by the SPCI interrupt (CENDF flag). Use the SPCI interrupt (CENDF flag).
Note 2. Disable the SPCI interrupt (SPCR.CENDIE = 0) during flag polling.
Note 3. During CPU operation, Write 1 to the RSPI receive buffer full flag clear bit (SPSRC.SPTEFC) after one processing routine.

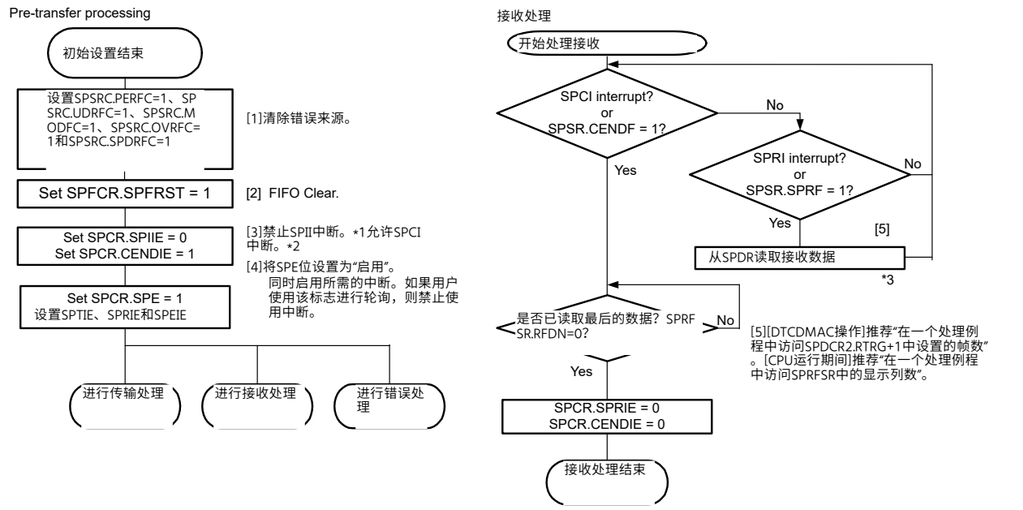
Figure 30.71 Software Processing Flowchart in Master Mode (Reception-only)

Error processing flow

In slave mode operation, even when a mode fault error is generated, the SPSR.MODF flag can be cleared regardless of the state of the SSLn0 pin.

When an error is detected by using an interrupt, clear the ICU.IELSRn.IR flag in the error processing routine. If this is not done, the ICU.IELSRn.IR flag might continue to indicate the SPIi_SPTI or SPIi_SPRI interrupt request. If the SPIi_SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the SPI.

主接收处理流程



注1.通信结束可以由SPCI中断（CENDF标志）决定。使用SPCI中断（CENDF标志）。
注2.在标志轮询期间禁用SPCI中断(SPCR.CENDIE=0)。
注3.在CPU运行期间，在一个处理程序后将1写入RSPI接收缓冲区满标志清除位(SPSRC.SPTEFC)。

Figure 30.71 主控模式下的软件处理流程图（仅接收）

错误处理流程

在从模式操作中，即使产生了模式故障错误，SPSR.MODF标志也可以被清除，而与SSLn0引脚的状态无关。

当使用中断检测到错误时，清除错误处理例程中的ICU.IELSRn.IR标志。如果不这样做，ICU.IELSRn.IR标志可能会继续指示SPIi_SPTI或SPIi_SPRI中断请求。如果指示了SPIi_SPRI中断请求，则读取接收缓冲区并初始化SPI中的定序器。

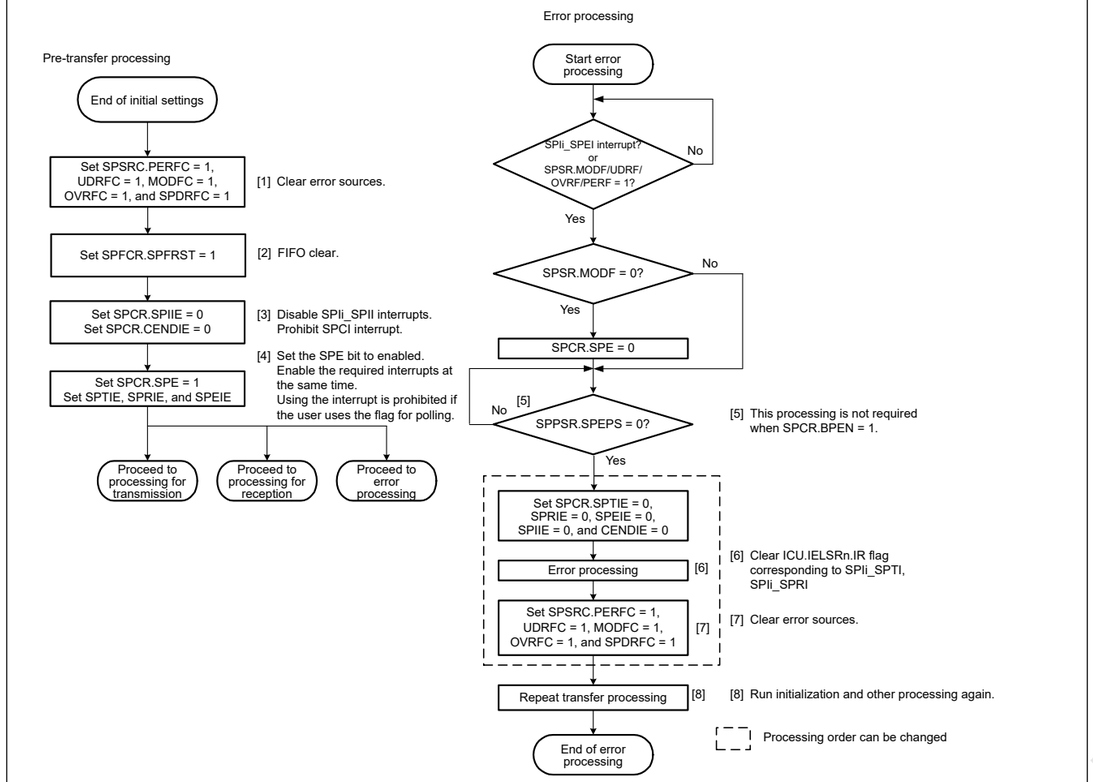


Figure 30.72 Error processing flow for slave mode

30.3.13 Clock Synchronous Operation

Setting the SPCR.SPMS bit to 1 selects clock synchronous operation of the SPI. In clock synchronous operation, the SSLni pin is not used, and the RSPCKn, MOSIn, and MISOn pins handle communications. All SSLni pins are available as I/O port pins.

Although clock synchronous operation does not require the use of the SSLni pin, operation of the module is the same as in SPI operation. In both master mode and slave mode operations, communications can be performed with the same flow as in SPI operation. However, mode fault errors are not detected, because the SSLni pin is not used.

Additionally, do not perform operation if clock synchronous operation is enabled when the SPCMDm.CPHA bit is set to 0 in slave mode (SPCR.MSTR = 0).

30.3.13.1 Master mode operation

(1) Starting serial transfer

When data is written to the RSPI data register (SPDR) while the next transfer data is not set in the transmit FIFO, the RSPI updates the transmit buffer (SPTXn, n = 0 to 3) data in SPDR.While the shift register is empty, the RSPI copies transmit buffer data to the shift register to start serial transfer. After the RSPI copies transmit data to the shift register, it changes the shift register status to full. Upon completion of serial transfer, the RSPI changes the shift register status to empty. The shift register status cannot be monitored.

For details about the RSPI transfer format, see section 30.3.5. Transfer Formats. In clock synchronous operation, however, the SSL0 output signal is not used for communication.

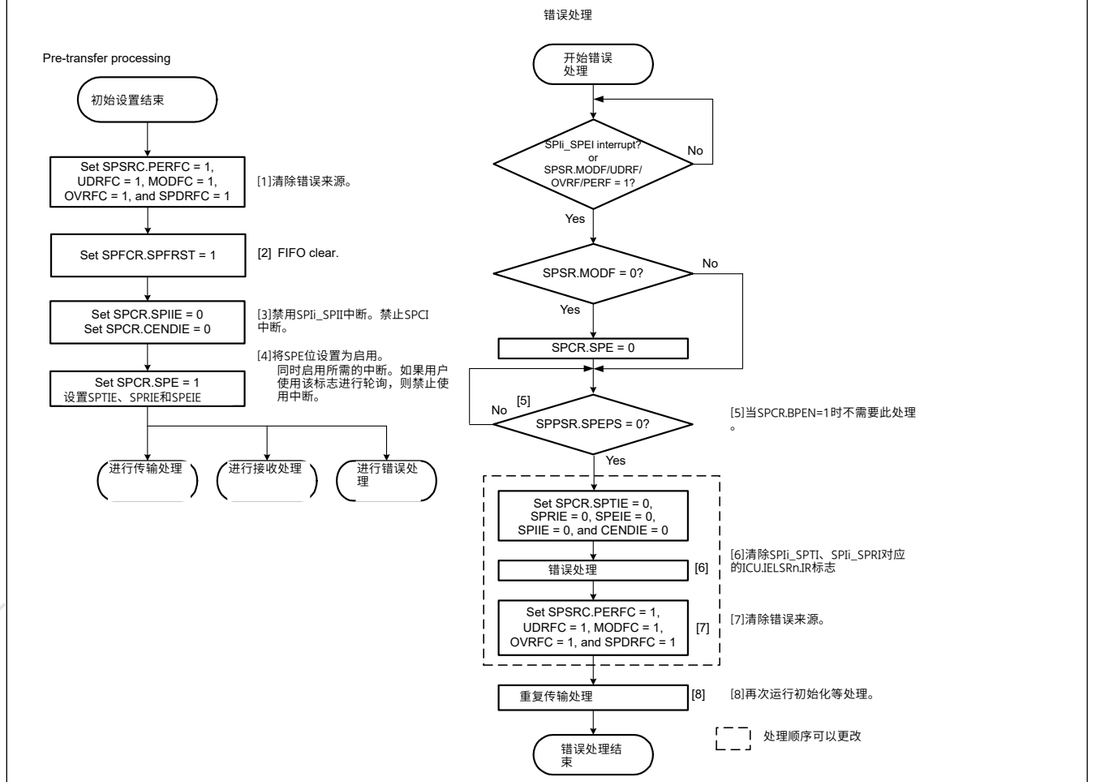


Figure 30.72 从机模式的错误处理流程

30.3.13 时钟同步操作

将SPCR.SPMS位设置为1可选择SPI的时钟同步操作。在时钟同步操作中，不使用SSLni引脚，而RSPCKn、MOSIn和MISOn引脚处理通信。所有SSLni引脚都可用作IO端口引脚。

虽然时钟同步操作不需要使用SSLni引脚，但模块的操作与SPI操作相同。在主模式和从模式操作中，可以使用与在相同的流程中执行通信
SPI操作。但是，未检测到模式故障错误，因为未使用SSLni引脚。

此外，如果在从模式(SPCR.MSTR=0)下SPCMDm.CPHA位设置为0时使能时钟同步操作，则不要执行操作。

30.3.13.1 主模式操作

(1) 开始串行传输

当数据写入RSPI数据寄存器(SPDR)而下一次传输数据未设置在发送FIFO中时，RSPI更新SPDR中的发送缓冲区(SPTXn n=0到3)数据。而移位寄存器为空，RSPI将传输缓冲区数据复制到移位寄存器以开始串行传输。RSPI将发送数据复制到移位寄存器后，将移位寄存器状态更改为满。串行传输完成后，RSPI将移位寄存器状态更改为空。无法监控移位寄存器状态。

有关RSPI传输格式的详细信息，请参见30.3.5节。传输格式。然而，在时钟同步操作中，SSL0输出信号不用于通信。

(2) Terminating serial transfer

The SPI terminates the serial transfer after transmitting an RSPCKn edge corresponding to the sampling timing. If the number of data stored in the receive FIFO < the number of FIFO stages, on termination of serial transfer, the SPI copies data from the shift register to the receive buffer of the SPI Data Register (SPDR).

The final sampling timing varies depending on the bit length of transfer data. In master mode, the SPI data length depends on the SPCMDm.SPB[4:0] bits setting. Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 30.3.5. Transfer Formats.

(3) Sequence control

The transfer format used in master mode is determined by the SPCR3, SPCMDm, and SPDECR registers. Although the SSLni signals are not output in clock synchronous operation, these settings are valid.

The SPCR3.SPSLN[2:0] bits determine the sequence configuration for serial transfers that are executed by the SPI in master mode. The following parameters are specified in the SPCMDm register:

- SSLni output signal value
- MSB or LSB first
- Data length
- Some of the bit rate settings
- RSPCKn polarity and phase
- Whether SPDECR.SCKDL is to be referenced
- Whether SPDECR.SLNDL is to be referenced
- Whether SPDECR.SPNDL is to be referenced

SPCR3.SPBR holds some of the bit rate settings such as SPDECR.SCKDL, an SPI clock delay value, SPDECR.SLNDL, an SSL negation delay, and SPDECR.SPNDL, a next-access delay value.

Based on the sequence length that is assigned to SPCR3, the SPI makes up a sequence comprised of a part or all of SPCMDm register. The SPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPDCR2.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the SPI function is enabled, the SPI loads the pointer to the commands in SPCMD0 register, and incorporates the SPCMD0 register setting into the transfer format at the beginning of serial transfer. The SPI increments the pointer each time the next-access delay period for a data transfer ends. On completion of the serial transfer that corresponds to the final command comprising the sequence, the SPI sets the pointer to the SPCMD0 register, and in this manner the sequence is executed repeatedly.

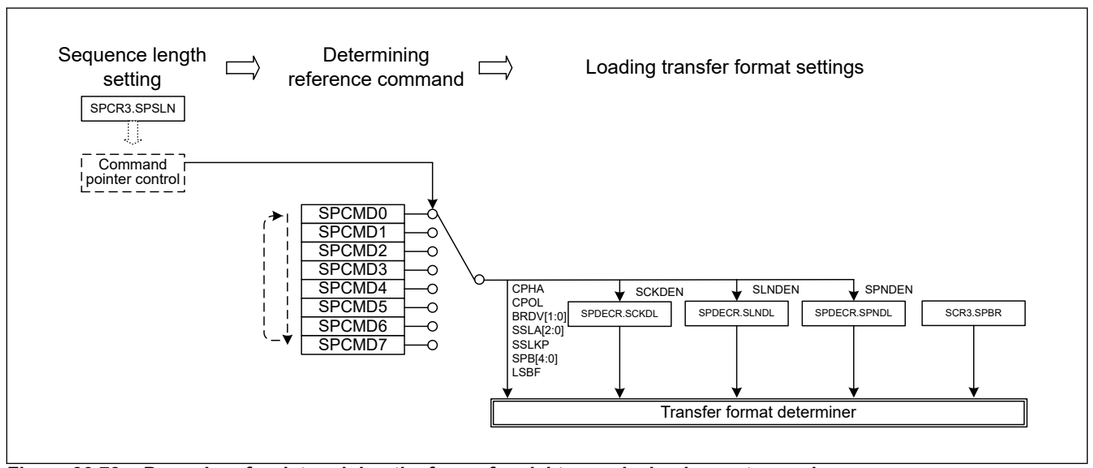


Figure 30.73 Procedure for determining the form of serial transmission in master mode

In this section, a frame is the combination of the data (SPDR) and the settings (SPCMDm).

(2) 终止串行传输

SPI在发送对应于采样时序的RSPCKn边沿后终止串行传输。如果接收FIFO中存储的数据数量<FIFO级数，则在串行传输终止时，SPI将数据从移位寄存器复制到SPI数据寄存器(SPDR)的接收缓冲区。

最终的采样时序根据传输数据的位长而变化。在主模式下，SPI数据长度取决于SPMDm.SPB[4:0]位设置。在没有SSLn0输出信号的情况下进行时钟同步操作的传输。有关SPI传输格式的详细信息，请参见第30.3.5节。传输格式。

(3) 顺序控制

主机模式中使用的传输格式由SPCR3、SPCMDm和SPDECR寄存器决定。虽然
时钟同步操作中不输出SSLni信号，这些设置有效。

SPCR3.SPSLN[2:0]位确定由SPI在主模式下执行的串行传输的序列配置。SPCMDm寄存器中指定了以下参数：

- SSLni输出信号值
- MSB或LSB在前
- 数据长度
- 一些比特率设置
- RSPCKn极性和相位
- SPDECR.SCKDL是否被引用
- SPDECR.SLNDL是否被引用
- SPDECR.SPNDL是否被引用

SPCR3.SPBR保存一些比特率设置，例如SPDECR.SCKDL，一个SPI时钟延迟值，SPDECR.SLNDL，一个SSL否定延迟和SPDECR.SPNDL，下一次访问延迟值。

根据分配给SPCR3的序列长度，SPI组成一个由部分或全部组成的序列
SPMDm寄存器。SPI包含一个指向构成序列的SPCMDm寄存器的指针。该指针的值可以通过读取SPDCR2.SPCP[2:0]位来检查。当SPCR.SPE位设置为1且SPI功能使能时，SPI将指针加载到SPCMD0寄存器中的命令，并在串行传输开始时将SPCMD0寄存器设置合并到传输格式中。每次数据传输的下一个访问延迟周期结束时，SPI都会递增指针。在完成对应于包含序列的最终命令的串行传输后，SPI将指针设置为SPMD0寄存器，并以这种方式重复执行序列。

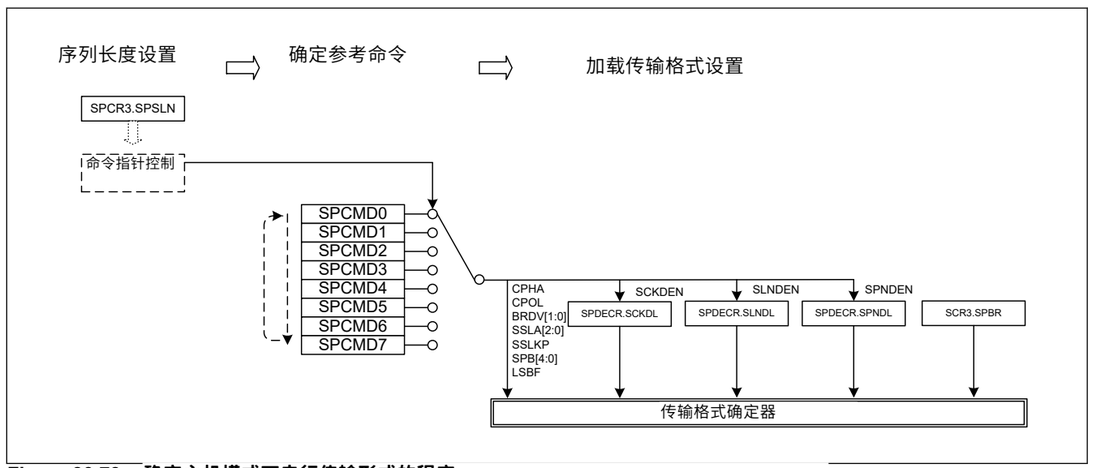


Figure 30.73 确定主机模式下串行传输形式的程序

在本节中，帧是数据(SPDR)和设置(SPCMDm)的组合。

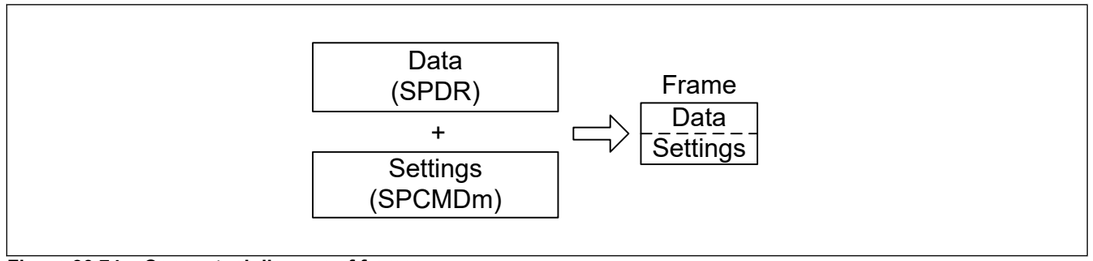


Figure 30.74 Conceptual diagram of frames

Figure 30.75 shows the relationship between the command and the transmit and receive buffers in the sequence of operations specified by the settings.

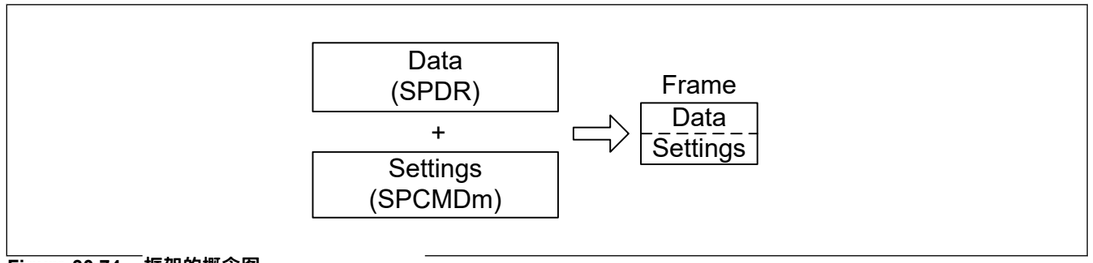


Figure 30.74 框架的概念图

图30.75显示了命令与设置指定的操作顺序中的发送和接收缓冲区之间的关系。

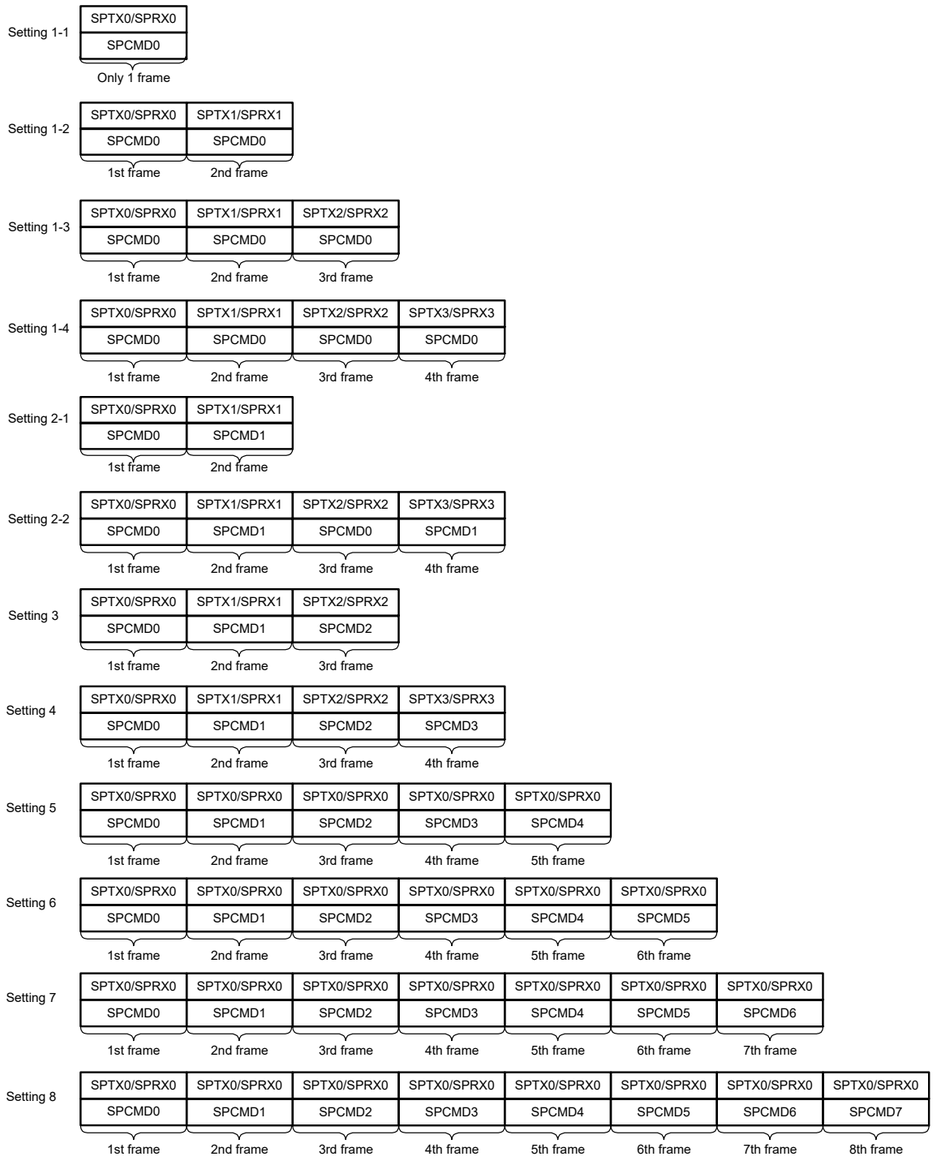


Figure 30.75 Correspondence between SPI Command Register and transmit and receive buffers in sequence operations

(4) Initialization flow

Figure 30.76 shows an example of initialization flow for clock synchronous operation when the SPI is used in master mode. For information on how to set up the ICU, DMAC or DTC, and I/O ports, see the descriptions given in the individual blocks.

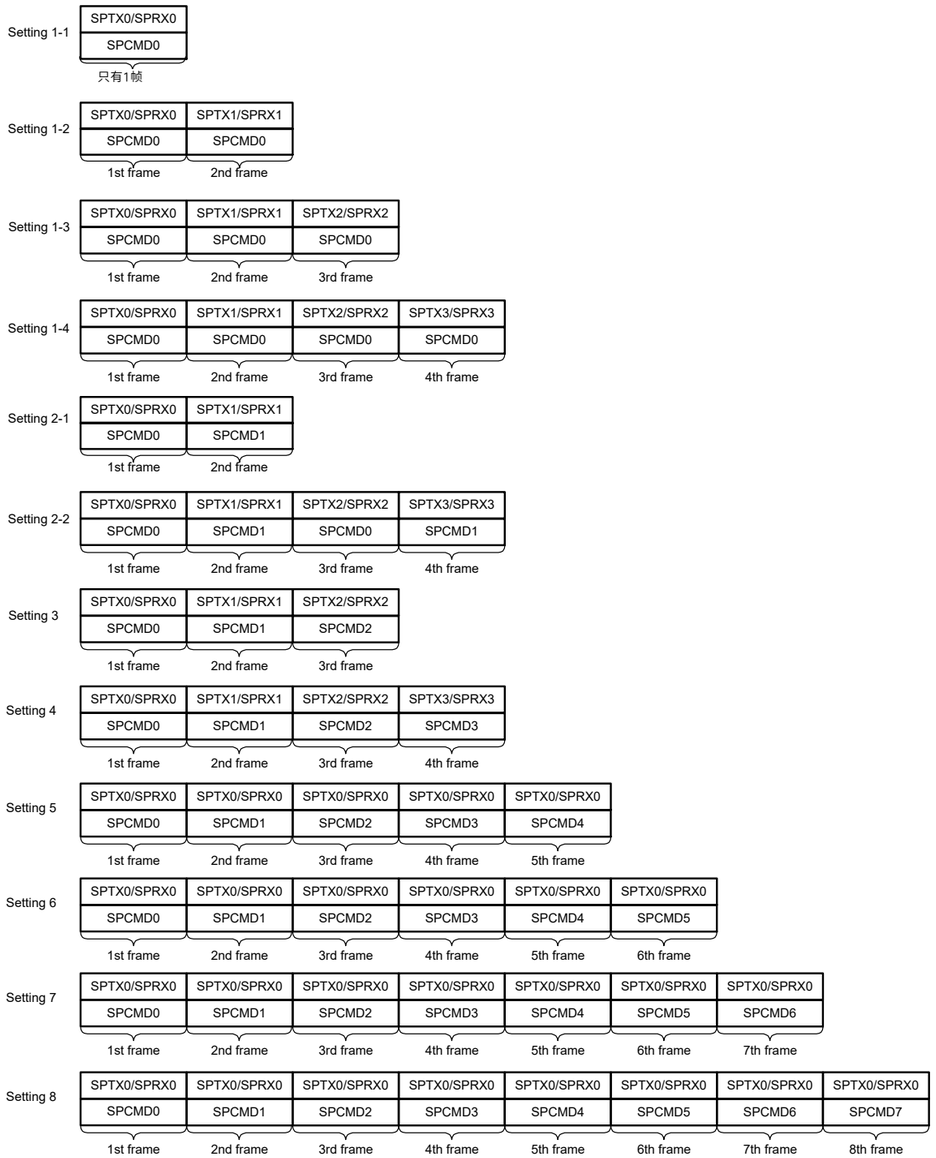


Figure 30.75 顺序操作中SPI命令寄存器与发送接收缓冲区的对应关系

(4) 初始化流程

图30.76显示了在主模式下使用SPI时时钟同步操作的初始化流程示例。
有关如何设置ICU、DMAC或DTC以及IO端口的信息，请参阅各个块中给出的说明。

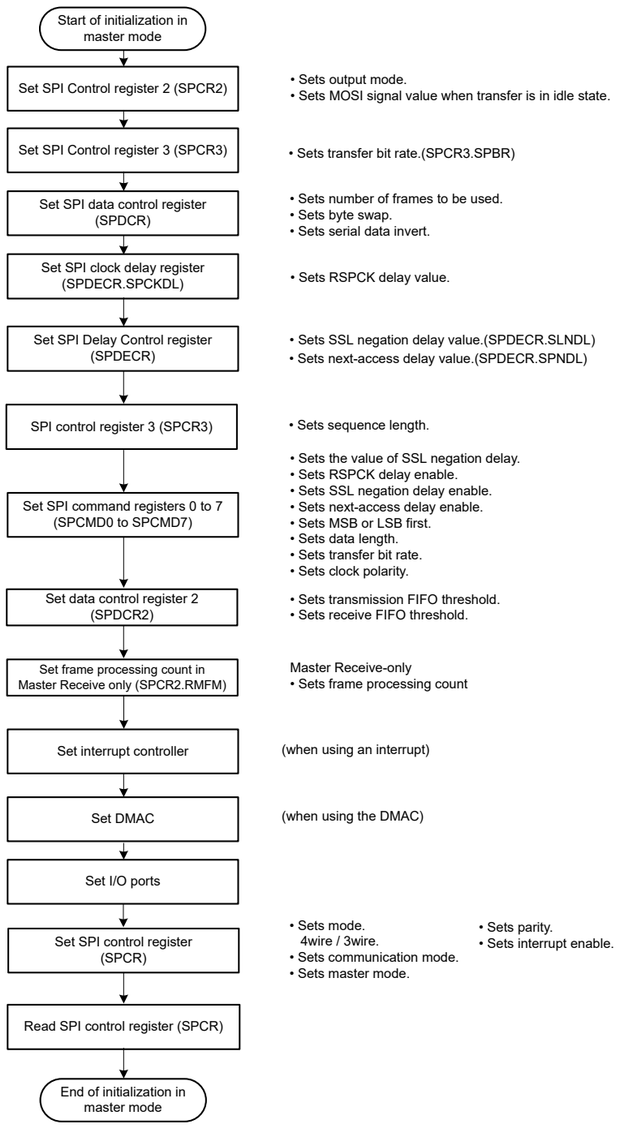


Figure 30.76 Example of initialization flow in master mode for clock synchronous operation

(5) Software processing flow

Software processing during clock synchronous master operation is the same as that for SPI master operation. For details, see (9) Software processing flow in section 30.3.12.1. Master mode operation. Mode fault errors do not occur in clock synchronous operation.

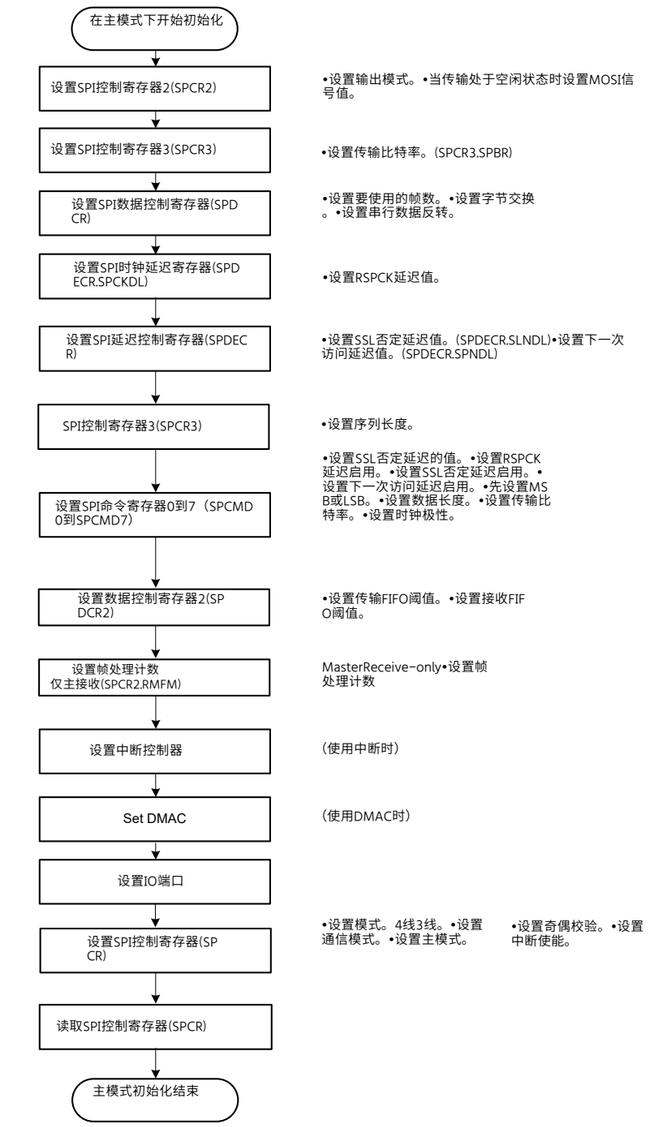


Figure 30.76 时钟同步操作的主模式初始化流程示例

(5) 软件处理流程

时钟同步主机操作期间的软件处理与SPI主机操作相同。详见30.3.12.1节（9）软件处理流程。主模式操作。时钟同步操作中不会发生模式故障错误。

30.3.13.2 Slave mode operation

(1) Starting serial transfer

When the SPCR.SPMS bit is 1, the first RSPCKn edge triggers the start of a serial transfer in the SPI, and the SPI drives the MISOn output signal. The SSL0 input signal is not used in clock synchronous operation. For details on the SPI transfer format, see section 30.3.5. Transfer Formats.

(2) Terminating serial transfer

The SPI terminates the serial transfer after detecting an RSPCKn edge corresponding to the final sampling timing. When the number of data stored in the receive FIFO < the number of FIFO stages, on termination of serial transfer, the SPI copies received data from the shift register to the receive buffer of the SPDR register. On termination of a serial transfer, the SPI changes the status of the shift register to empty regardless of the receive buffer.

The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length depends on the SPCMD0.SPB[4:0] bits setting. For details on the SPI transfer format, see section 30.3.5. Transfer Formats.

(3) Initialization flow

Figure 30.77 shows an example of initialization flow for clock synchronous operation when the SPI is used in slave mode. For a description of how to set up the ICU, DTC, and I/O ports, see the descriptions given in the individual blocks.

30.3.13.2 从模式操作

(1) 开始串行传输

当SPCR.SPMS位为1时，第一个RSPCKn边沿触发SPI中串行传输的开始，并且SPI驱动MISon输出信号。SSL0输入信号不用于时钟同步操作。有关SPI传输格式的详细信息，请参见第30.3.5节。传输格式。

(2) 终止串行传输

SPI在检测到对应于最终采样时序的RSPCKn边沿后终止串行传输。当接收FIFO中存储的数据数<FIFO级数时，在串行传输终止时，SPI将接收到的数据从移位寄存器复制到SPDR寄存器的接收缓冲区。在串行传输终止时，SPI将移位寄存器的状态更改为空，而与接收缓冲区无关。

最终的采样时序根据传输数据的位长而变化。在从机模式下，SPI数据长度取决于SPCMD0.SPB[4:0]位设置。有关SPI传输格式的详细信息，请参见第30.3.5节。传输格式。

(3) 初始化流程

图30.77显示了在从模式下使用SPI时时钟同步操作的初始化流程示例。
有关如何设置ICU、DTC和IO端口的说明，请参见各个块中给出的说明。

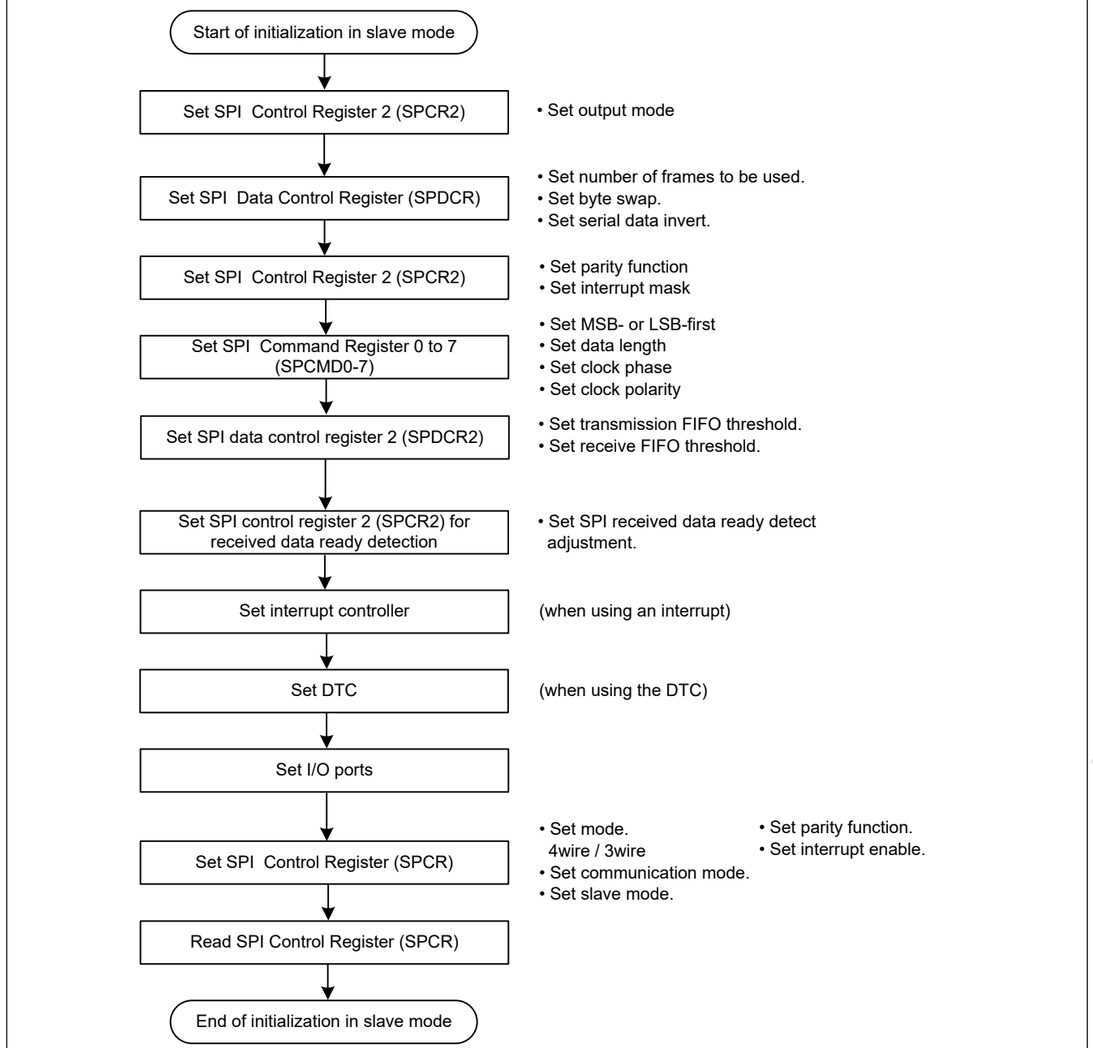


Figure 30.77 Example of initialization flow in slave mode for clock synchronous operation

(4) Software processing flow

Software processing during clock synchronous slave operation is the same as that for SPI slave operation. For details, see (6)Software processing flow. Mode fault errors do not occur in clock synchronous mode.

30.3.14 Loopback Mode

When 1 is written to the SPCR2.SPLP2 bit or SPCR2.SPLP bit, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, or between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects the input and output paths of the shift register, establishing a loopback mode. The SPI does not shut off the path between the MOSIn pin and the shift register if the SPCR.MSTR bit is 1, or between the MISOn pin and the shift register if the SPCR.MSTR bit is 0. This is called loopback mode. When a serial transfer is executed in loopback mode, the transmit data for the SPI or the reversed transmit data becomes the received data for the SPI.

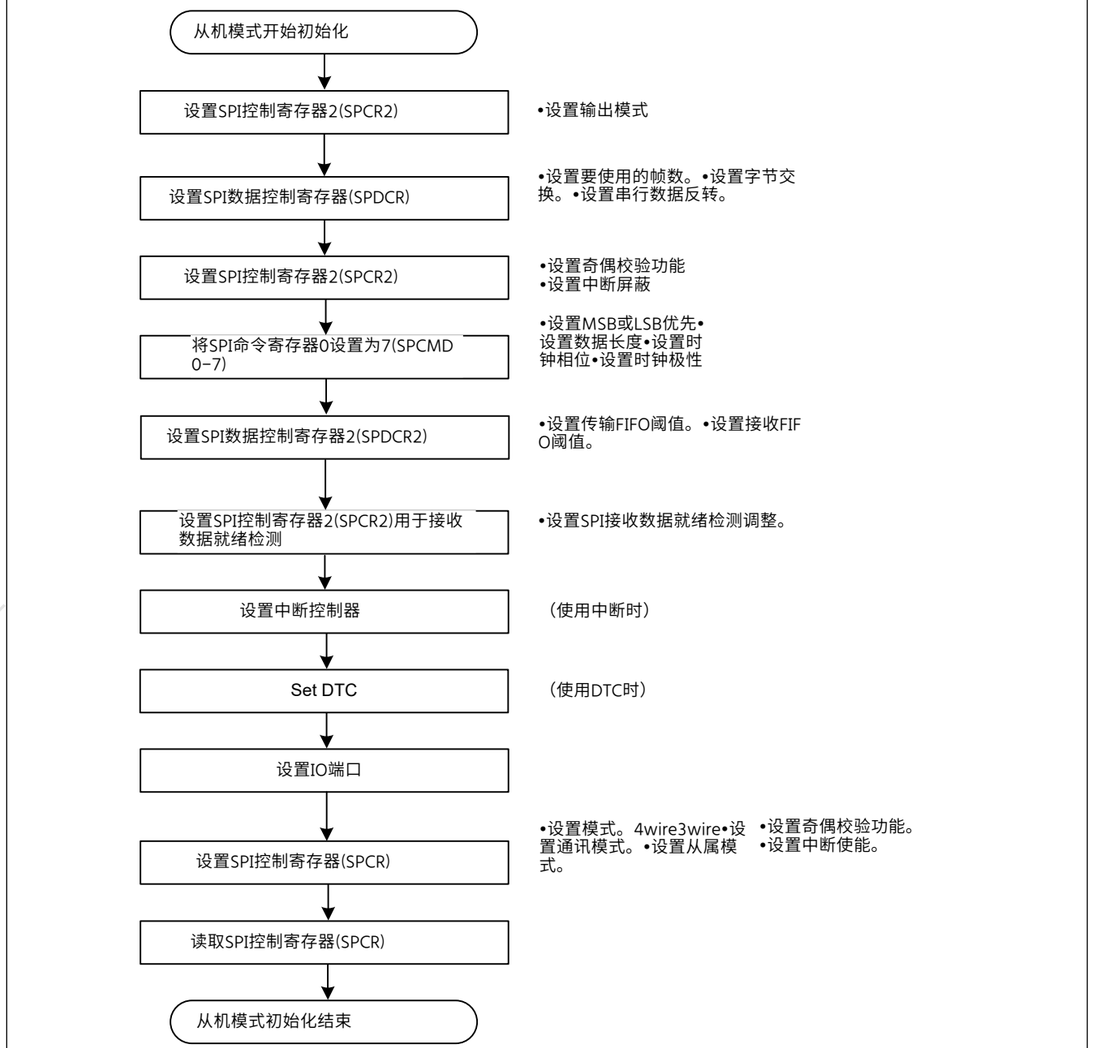


Figure 30.77 时钟同步操作的从模式初始化流程示例

(4) 软件处理流程

时钟同步从机操作期间的软件处理与SPI从机操作相同。详见（6）软件处理流程。时钟同步模式下不会发生模式故障错误。

30.3.14 Loopback Mode

当SPCR2.SPLP2位或SPCR2.SPLP位写入1时，如果SPCR.MSTR位为1，则SPI关闭MISOn引脚和移位寄存器之间的路径，或者如果SPCR.MSTR位为0，连接移位寄存器的输入和输出路径，建立环回模式。如果SPCR.MSTR位为1，SPI不关闭MOSIn引脚和移位寄存器之间的路径，如果SPCR.MSTR位为0，则SPI不关闭MISOn引脚和移位寄存器之间的路径。这称为环回模式。当在环回模式下执行串行传输时，SPI的发送数据或反向发送数据将成为SPI的接收数据。

Table 30.13 lists the relationship between the SPLP2 and SPLP bits and the received data. Figure 30.78 shows the configuration of the shift register I/O paths when the SPI in master mode is set to loopback mode (SPCR2.SPLP2 = 0, SPCR2.SPLP = 1).

Table 30.13 SPLP2 and SPLP bit settings and received data

SPCR2.SPLP2 bit	SPCR2.SPLP bit	Received data
0	0	Input data from the MOSIn pin or MISOn pin
0	1	Inverted transmit data
1	0	Transmit data
1	1	Transmit data

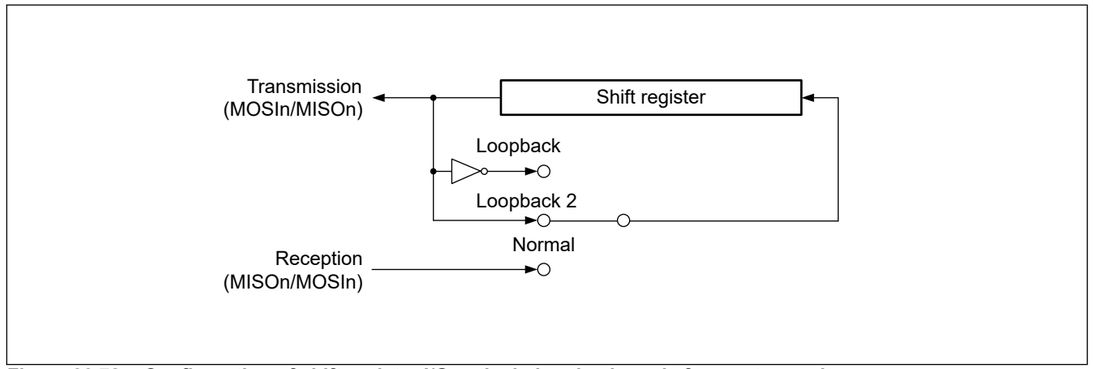


Figure 30.78 Configuration of shift register I/O paths in loopback mode for master mode

30.3.15 Self-Diagnosis of Parity Bit Function

The parity circuit consists of a parity bit adding unit used for transmit data and an error detecting unit used for received data. To detect defects in the parity bit adding unit and error detecting unit, the parity circuit performs self-diagnosis as shown in Figure 30.79.

表30.13列出了SPLP2和SPLP位与接收数据之间的关系。图30.78显示了当主模式下的SPI设置为环回模式（SPCR2.SPLP2=0，SPCR2.SPLP=1）时移位寄存器IO路径的配置。

Table 30.13 SPLP2和SPLP位设置和接收数据

SPCR2.SPLP2 bit	SPCR2.SPLP bit	接收数据
0	0	从MOSIn引脚或MIOn引脚输入数据
0	1	反相传输数据
1	0	传输数据
1	1	传输数据

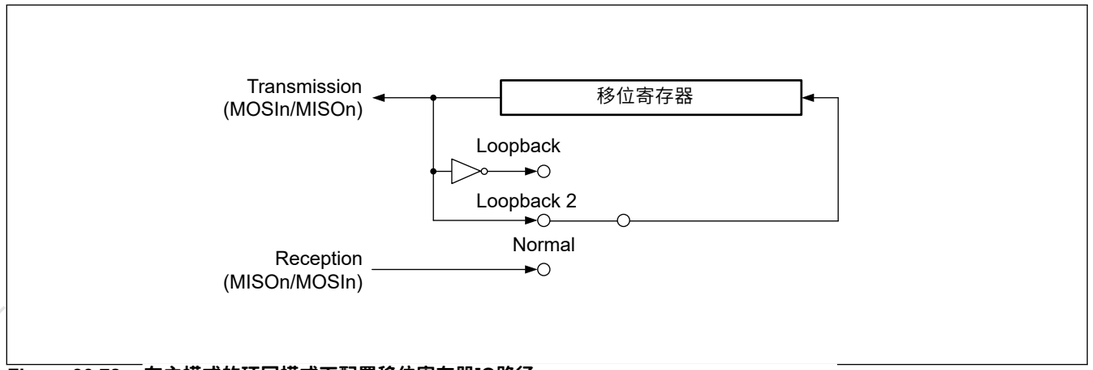


Figure 30.78 在主模式的环回模式下配置移位寄存器IO路径

30.3.15 奇偶校验位功能自诊断

奇偶校验电路由用于发送数据的奇偶校验位添加单元和用于接收数据的错误检测单元组成。为了检测奇偶校验位添加单元和错误检测单元中的缺陷，奇偶校验电路执行自诊断，如图所示Figure 30.79.

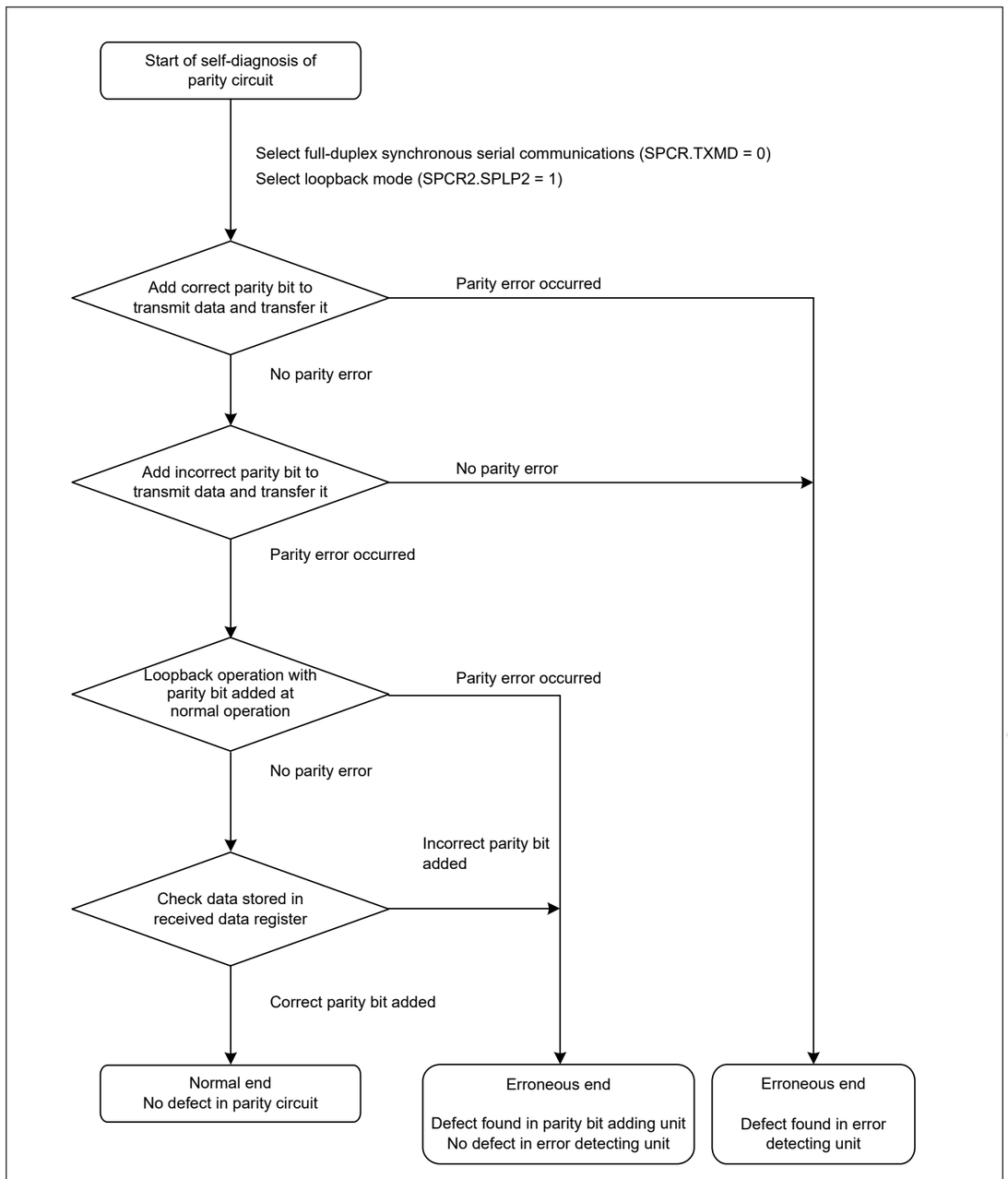


Figure 30.79 Self-diagnosis flow for parity circuit

30.3.16 Interrupt Sources

The SPI has the following interrupt sources:

- Receive buffer full
- Transmit buffer empty

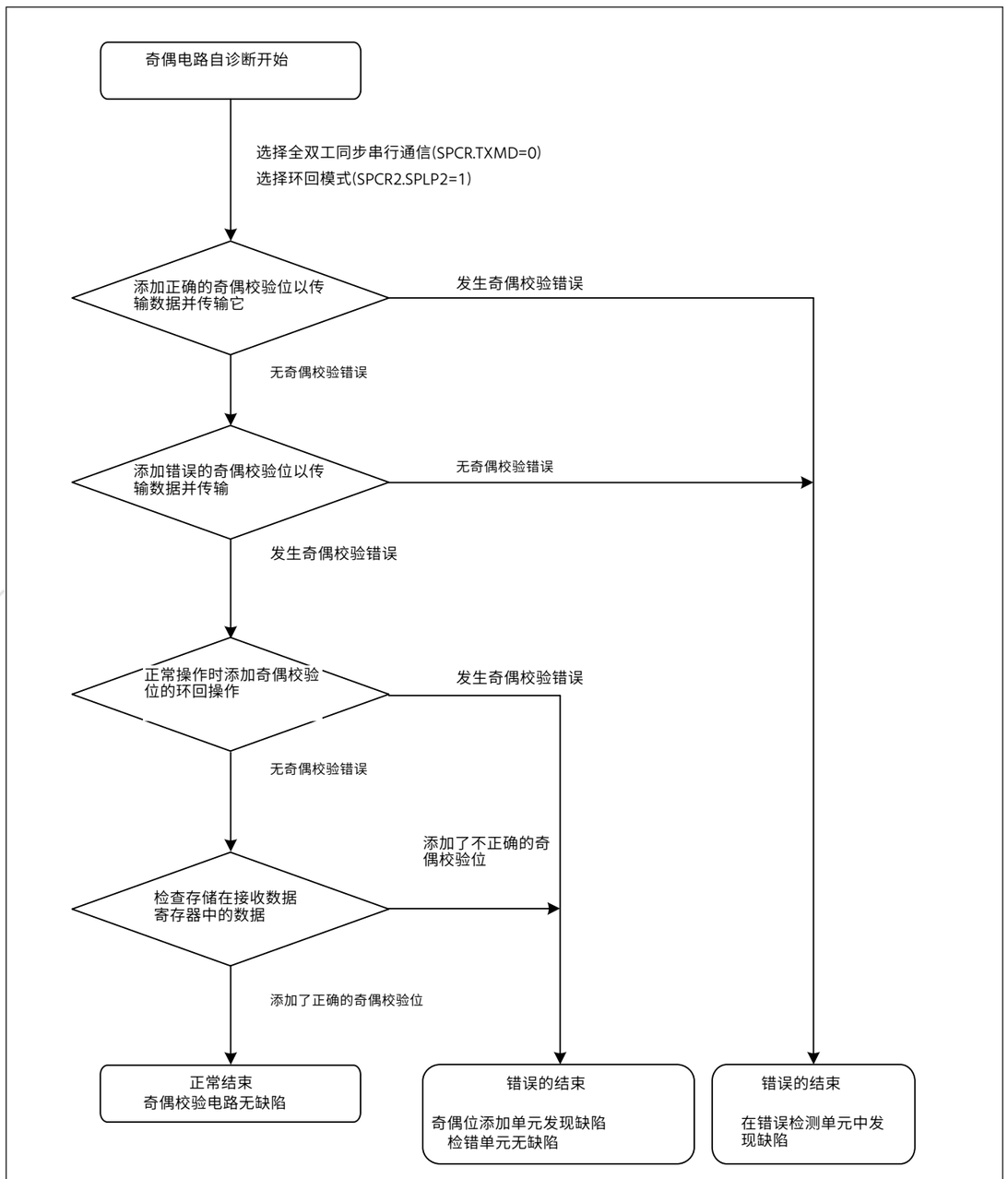


Figure 30.79 奇偶校验电路的自诊断流程

30.3.16 中断源

SPI有以下中断源：

- 接收缓冲区已满
- 发送缓冲区空

- SPI error (mode-fault, underrun, overrun, or parity error)
- SPI idle
- Communication-end

The DMAC or DTC can be activated by the receive buffer full or transmit buffer empty interrupt to perform data transfer.

Because the vector address for the SPIi_SPEI (SPI error interrupt) is allocated to interrupt requests on mode-fault, underrun, overrun, and parity errors, the actual interrupt source must be determined from the flags. Interrupt sources for the SPI are listed in Table 30.14. An interrupt is generated on satisfaction of one of the interrupt conditions in Table 30.14. Clear the receive buffer full and transmit buffer empty sources through a data transfer.

When using the DMAC or DTC to perform data transmission and reception, you must first set up the DMAC or DTC to be in a transfer-enabled status before setting the SPI. For information on setting up the DMAC or DTC, see section 15, DMA Controller (DMAC) and section 16, Data Transfer Controller (DTC).

If the conditions for generating a transmit buffer empty or receive buffer full interrupt occur while the ICU.IELSRn.IR flag is 1, the interrupt is not output as a request for the ICU but is retained internally (the capacity for retention is one request per source). A retained interrupt request is output when the ICU.IELSRn.IR flag becomes 0. A retained interrupt request is automatically discarded when it is output as an actual interrupt request. The interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) for an internally retained interrupt request can also be set to 0.

Table 30.14 SPI interrupt sources

Interrupt source	Symbol	Interrupt condition	DTC/DMAC activation
Receive buffer full	SPIi_SPRI	The receive buffer becomes full (SPSR.SPRF flag is 1) while the SPCR.SPRIE bit is 1 or The receive data become ready (SPSR.SPDRF flag is 1) while the SPCR.SPDRES bit is 0	Possible
Transmit buffer empty	SPIi_SPTI	The transmit buffer becomes empty (SPSR.SPTEF flag is 1) while the SPCR.SPTIE bit is 1	Possible
SPI error (mode-fault, underrun, overrun, or parity error)	SPIi_SPEI	The SPSR.MODF, OVRF,or PERF flag sets to 1, or the SPSR.SPDRES and SPDRF flag set to 1 while the SPCR.SPEIE bit is 1	Impossible
SPI idle	SPIi_SPII	The SPSR.IDLNF flag sets to 0 while the SPCR.SPIIE bit is 1	Impossible
Communication-end	SPIi_SPCEND	CENDIE = 1 and CENDF = 1	Impossible

30.4 Event Link Controller Event Output

The Event Link Controller (ELC) can produce the following event output signals:

- Receive buffer full event output
- Transmit buffer empty event output
- Mode-fault, underrun, overrun, or parity error event output
- SPI idle event output
- Transmission-completed event output

The event link output signal is output regardless of the interrupt enable bit setting.

30.4.1 Receive Buffer Full Event Output

When the number of data stored in the receive FIFO > the threshold value, or when the number of data stored in the receive FIFO ≤ the threshold value and SPDRES = 0 has elapsed after writing to the receive FIFO, and the SPDRC [7:0] has elapsed outputs an event.

30.4.2 Transmit Buffer Empty Event Output

An event is output when the number of empty transmission FIFO stage > the threshold or when the SPCR.SPE bit changes from 0 to 1.

●SPI错误（模式故障、欠载、溢出或奇偶校验错误）

●SPI空闲

- Communication-end

DMAC或DTC可由接收缓冲区满或发送缓冲区空中断激活以执行数据传输。

由于SPIi_SPEI（SPI错误中断）的向量地址分配给模式错误、欠载、溢出和奇偶校验错误的中断请求，因此必须根据标志确定实际中断源。表30.14列出了SPI的中断源。满足表30.14中的中断条件之一时会产生中断。通过数据传输清除接收缓冲区满和发送缓冲区空源。

使用DMAC或DTC进行数据收发时，必须先将DMAC或DTC设置为传输使能状态，然后再设置SPI。有关设置DMAC或DTC的信息，请参阅第15节，DMA控制器(DMAC)和第16节，数据传输控制器(DTC)。

如果在ICU.IELSRn.IR标志为1时发生发送缓冲区空或接收缓冲区满中断的条件，则该中断不会作为对ICU的请求输出，而是在内部保留（保留容量为每个请求一个请求）资源）。当ICU.IELSRn.IR标志变为0时，输出保留中断请求。当作为实际中断请求输出时，自动丢弃保留中断请求。内部保留中断请求的中断使能位（SPCR.SPTIE或SPCR.SPRIE位）也可以设置为0。

Table 30.14 SPI中断源

中断源	Symbol	中断条件	DTC/DMAC activation
接收缓冲区已满	SPIi_SPRI	SPCR.SPRIE位为1时接收缓冲器变满（SPSR.SPRF标志为1）或SPCR.SPDRES位为0时接收数据准备好（SPSR.SPDRF标志为1）	Possible
发送缓冲区为空	SPIi_SPTI	当SPCR.SPTIE位为1时，发送缓冲区变为空（SPSR.SPTEF标志为1）	Possible
SPI错误（模式错误、欠载、溢出或奇偶校验错误）	SPIi_SPEI	SPSR.MODF、OVRF或PERF标志设置为1，或者SPSR.SPDRES和SPDRF标志设置为1，而SPCR.SPEIE位为1	Impossible
SPI空闲	SPIi_SPII	SPSR.IDLNF标志设置为0，而SPCR.SPIIE位为1	Impossible
Communication-end	SPIi_SPCEND	CENDIE = 1 and CENDF = 1	Impossible

30.4 事件链接控制器事件输出

事件链接控制器(ELC)可以产生以下事件输出信号：

●接收缓冲区满事件输出

●发送缓冲区空事件输出

●模式故障、欠载、溢出或奇偶校验错误事件输出

●SPI空闲事件输出

●传输完成事件输出

无论中断允许位设置如何，都会输出事件链接输出信号。

30.4.1 接收缓冲区满事件输出

当接收FIFO中存储的数据数量>阈值时，或者当接收中存储的数据数量FIFO≤阈值且SPDRES=0在写入接收FIFO后已过，并且SPDRC[7:0]已过输出事件。

30.4.2 发送缓冲区空事件输出

当空传输FIFO级数>阈值或SPCR.SPE位从0变为1时，输出事件。

30.4.3 Mode-Fault, Underrun, Overrun, Parity Error, or received data ready Event Output

This event signal is output when mode-fault, underrun, overrun, or parity error is detected. See section 30.5.4. Constraints on Mode-Fault, Underrun, Overrun, Parity Error, or Receive Data Ready Event Output if using this event signal.

(1) Mode-fault

Table 30.15 lists the conditions for occurrence of a mode-fault event.

Table 30.15 Conditions for mode-fault occurrence

SPI mode	SPCR.MODFEN bit	SSLn0 pin	Remarks
SPI operation (SPMS = 0) Slave (SPCR.MSTR = 0) Motorola (SPCR.SPFRF = 0)	1	Not active	Event is output only when the SSLn0 pin is deactivated during transmission
SPI operation (SPMS = 0) Slave (SPCR.MSTR = 0) Motorola (SPCR.SPFRF = 1)	1	active	Event is output only when the SSLn0 pin is activated during transmission

(2) Underrun

This event signal is output in response to an underrun when a serial transfer starts while the transmission data is not ready, and the value of the SPCR.MSTR bit is 0 and the SPCR.SPE bit is 1. Under these conditions, the MODF and UDRF flags are set to 1.

(3) Overrun

This event signal is output in response to an overrun when a serial transfer completes while the receive buffer contains unread data and the value of the SPCR.TXMD[1:0] bits are 00b, 10b, or 11b. Under these conditions, the OVRF flag is set to 1.

(4) Parity error

This event signal is output in response to a parity error detected on completion of a serial transfer while the value of the SPPE bit in SPCR is 1.

(5) Receive Data Ready

When TXMD[1:0] of SPCR = 00b or 10b and SPDRES = 1 as the receive data ready event output condition, the number of data stored in the receive FIFO is received after writing the receive FIFO. An event will be output when the set value of SPDRC[7:0] has elapsed while the number is less than the FIFO threshold.

30.4.4 SPI Idle Event Output

(1) In master mode

In Transmit-Receive / Transmit-only master mode, an event is output when the IDLNF flag in SPSR changes from 1 to 0.

The IDLNF flag changes from 1 to 0 only when either of the conditions 1) and 2) below is met.

1. The SPE bit in SPCR is cleared to 0 (RSPI initialized) during transmission.
2. All of the following three conditions are met.
   - The transmit buffer (SPTXn, n = 0 to 3) is empty (next transfer data has not been set).
   - The SPSR bit in SPCR is 000 (at the start of sequence control).
   - Operation completed until the next access delay (when the master main state machine transitions to the idle state).

In receive only master mode

Any of the following 2 conditions is met.

1. SPE bit of SPCR is 0 (RSPI initialization)
2. When any of the following is met
   - When RMFM [4:0] = 0x0, after writing 1 to RMEDTG, operation completed until the next access delay (when the master main state machine transitions to the idle state).

30.4.3 模式故障、欠载、溢出、奇偶校验错误或接收数据就绪事件输出

当检测到模式故障、欠载、溢出或奇偶校验错误时，输出此事件信号。请参阅第30.5.4节。如果使用此事件信号，则限制模式故障、欠载、溢出、奇偶校验错误或接收数据就绪事件输出。

(1) Mode-fault

表30.15列出了模式故障事件发生的条件。

Table 30.15 模式故障发生的条件

SPI模式	SPCR.MODFEN bit	SSLn0 pin	Remarks
SPI操作(SPMS=0)从机(SPCR.MSTR=0) Motorola (SPCR.SPFRF = 0)	1	不活跃	只有在传输过程中禁用SSLn0引脚时才会输出事件
SPI操作(SPMS=0)从机(SPCR.MSTR=0) Motorola (SPCR.SPFRF = 1)	1	active	只有在传输过程中激活SSLn0引脚时才会输出事件

(2) Underrun

当串行传输开始而传输数据尚未准备好，并且SPCR.MSTR位的值为0且SPCR.SPE位为1时，输出此事件信号以响应欠载。在这些条件下，MODF和UDRF标志设置为1。

(3) Overrun

当串行传输完成而接收缓冲区包含未读数据且SPCR.TXMD[1:0]位的值为00b、10b或11b时，输出此事件信号以响应溢出。在这些条件下，OVRF标志设置为1。

(4) 奇偶校验错误

该事件信号是响应在串行传输完成时检测到的奇偶校验错误而输出的，而
SPCR中的SPPE位为1。

(5) 接收数据就绪

当SPCR的TXMD[1:0]=00b或10b且SPDRES=1作为接收数据就绪事件输出条件时，在写入接收FIFO后接收存储在接收FIFO中的数据数量。当SPDRC[7:0]的设置值已过且数量小于FIFO阈值时，将输出事件。

30.4.4 SPI空闲事件输出

(1) 在主模式

在Transmit-ReceiveTransmit-onlymaster模式下，当SPSR中的IDLNF标志从1变为0时输出事件。

仅当满足以下条件1)和2)中的任何一个时，IDLNF标志才会从1变为0。

1.SPCR中的SPE位在传输过程中被清零（RSPI初始化）。

2.满足以下三个条件。

- ●发送缓冲区（SPTXn，n=0到3）为空（未设置下一次传输数据）。
- ●SPCR中的SPSR位为000（序列控制开始时）。
- ●操作完成，直到下一次访问延迟（当主主状态机转换到空闲状态时）。

在仅接收主模式下

满足以下2个条件中的任何一个。

1.SPCR的SPE位为0（RSPI初始化）

2.满足以下任何一项时

- ●当RMFM[4:0]=0x0时，向RMEDTG写1后，操作完成，直到下一次访问延迟（当主主状态机转换到空闲状态时）。

- When RMFM [4:0] ≠ 0x0, after writing 1 to RMEDTG, operation completed until the next access delay (when the master main state machine transitions to the idle state).
- When RMFM [4:0] ≠ 0x0, the RSPI internal sequencer transitions to the idle state after operation completed until the next access delay (when the master main state machine transitions to the idle state).

(2) In slave mode

In slave mode, an event is output when the SPCR.SPE bit is set to 0 (SPI is initialized).

30.4.5 Communication End Event Output

In master mode, an event is output when the IDLNF flag (RSPI idle flag) changes from 1 to 0. In slave mode, an event occurs with conditions shown in Table 30.16 and Table 30.17

Table 30.16 Communication End Event Generating Conditions (transmit-receive/transmit slave mode)

	Transmit Buffer Status	Shift Register Status	Others
SPI operation (SPMS = 0, SPFRF = 0)	Empty	Empty	SSL0 input is negated
SPI operation (SPMS = 0, SPFRF = 1)	Empty	Empty	SSL negation delay completed
Clock synchronous operation (SPMS = 1)	Empty	Empty	The last even edge of RSPCK of last data was detected (CPHA = 1)

Table 30.17 Communication End Event Generating Conditions (receive only slave mode)

	Others
SPI operation (SPMS = 0, SPFRF = 0)	After storing the frames corresponding to the SPFC setting value in the receive buffer, negate SSL0 input.
SPI operation (SPMS = 0, SPFRF = 1)	After storing the frames corresponding to the SPFC setting value in the receive buffer, SSL negation delay completed
Clock synchronous operation (SPMS = 1)	RSPCK last even edge detection when receiving the last frame for the SPFC set value (CPHA = 1)

Regardless of master mode or slave mode, no event is output when 0 is written to the SPCR.SPE bit during transmission or when the SPCR.SPE bit is cleared due to a mode fault error or an underrun error.

A communication end event is output at the following timing. The communication end event output timing in master operation is omitted because it is output at the same timing as an idle event.

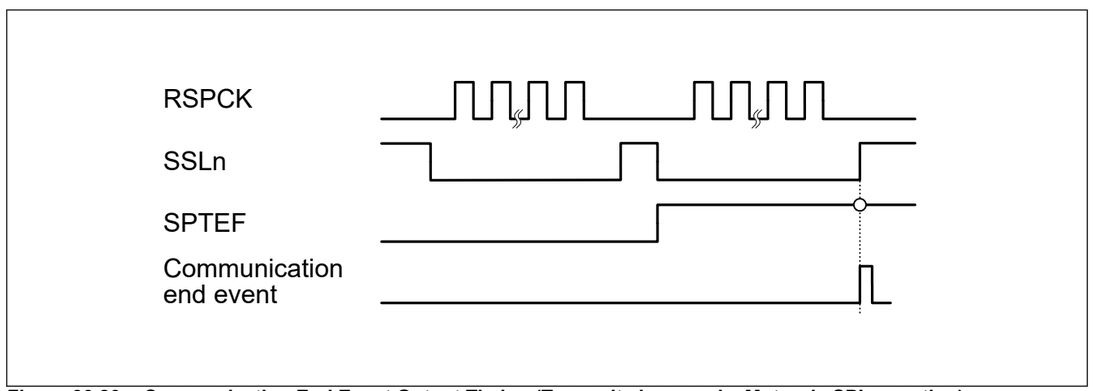


Figure 30.80 Communication End Event Output Timing (Transmit slave mode, Motorola SPI operation)

●当RMFM[4:0]≠0x0时，向RMEDTG写入1后，操作完成，直到下一次访问延迟（当主主状态机转换到空闲状态时）。

●当RMFM[4:0]≠0x0时，RSPI内部定序器在操作完成后转换到空闲状态，直到下一次访问延迟（当主主状态机转换到空闲状态时）。

(2) 在从模式

在从机模式下，当SPCR.SPE位设置为0（SPI初始化）时，会输出一个事件。

30.4.5 通讯结束事件输出

在主机模式下，当IDLNF标志（RSPI空闲标志）从1变为0时输出事件。在从机模式下，事件发生的条件如表30.16和表30.17所示

Table 30.16 通信结束事件发生条件（发送-接收发送从模式）

	发送缓冲区状态	移位寄存器状态	Others
SPI操作（SPMS=0，SPFRF = 0)	Empty	Empty	SSL0输入被否定
SPI操作（SPMS=0，SPFRF = 1)	Empty	Empty	SSL否定延迟已完成
时钟同步操作(SPMS=1)	Empty	Empty	检测到最后一个数据的RSPCK的最后一个偶边沿(CPHA=1)

Table 30.17 通信结束事件发生条件（仅接收从模式）

	Others
SPI操作（SPMS=0，SPFRF=0）	将与SPFC设置值对应的帧存储到接收缓冲区后，否定SSL0输入。
SPI操作（SPMS=0，SPFRF=1）	将对应于SPFC设置值的帧存储到接收缓冲区后，SSL否定延迟完成
时钟同步操作(SPMS=1)	当接收到SPFC设定值的最后一帧时，RSPCK最后一个偶边沿检测(CPHA=1)

无论主模式还是从模式，在传输过程中向SPCR.SPE位写入0或由于模式故障错误或欠载错误而清除SPCR.SPE位时，不输出任何事件。

在以下定时输出通信结束事件。主操作中的通信结束事件输出时序被省略，因为它与空闲事件在相同的时序输出。

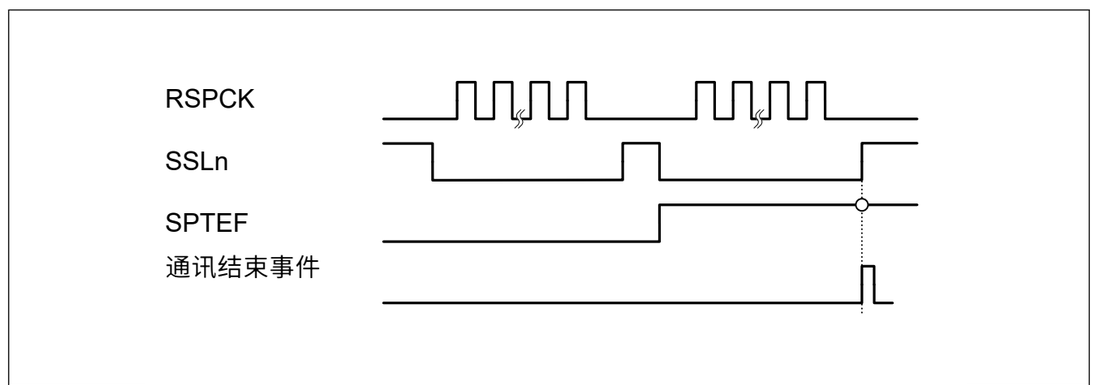


Figure 30.80 通信结束事件输出时序（发送从机模式，摩托罗拉SPI操作）

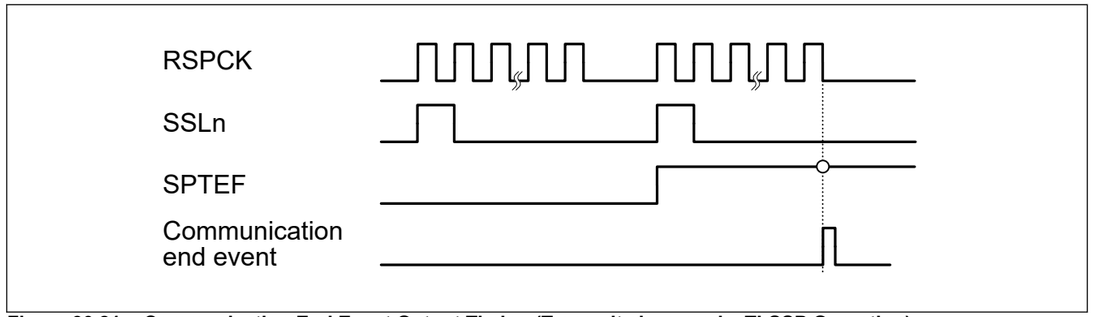


Figure 30.81 Communication End Event Output Timing (Transmit slave mode, TI-SSP Operation)

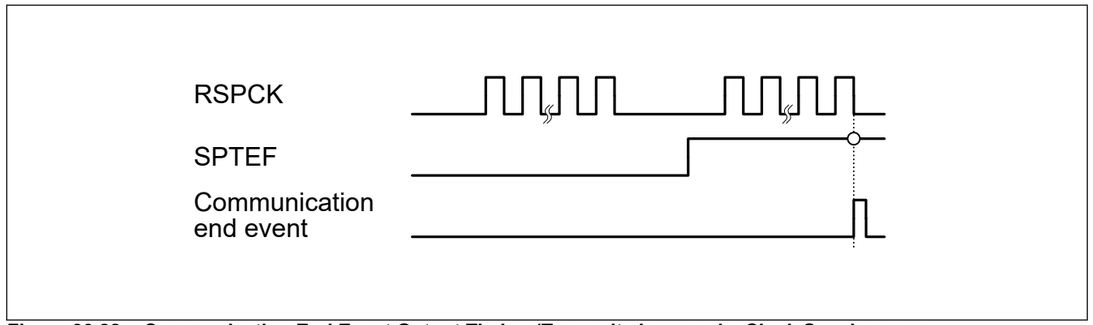


Figure 30.82 Communication End Event Output Timing (Transmit slave mode, Clock Synchronous Operation)

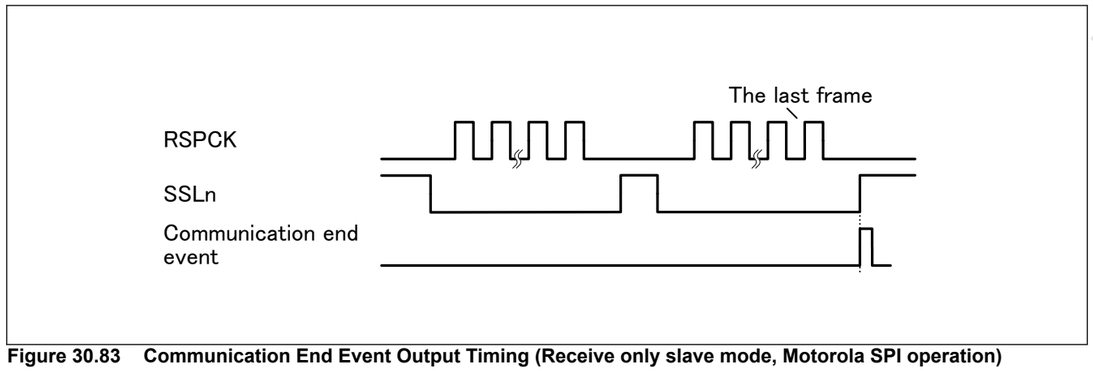


Figure 30.83 Communication End Event Output Timing (Receive only slave mode, Motorola SPI operation)

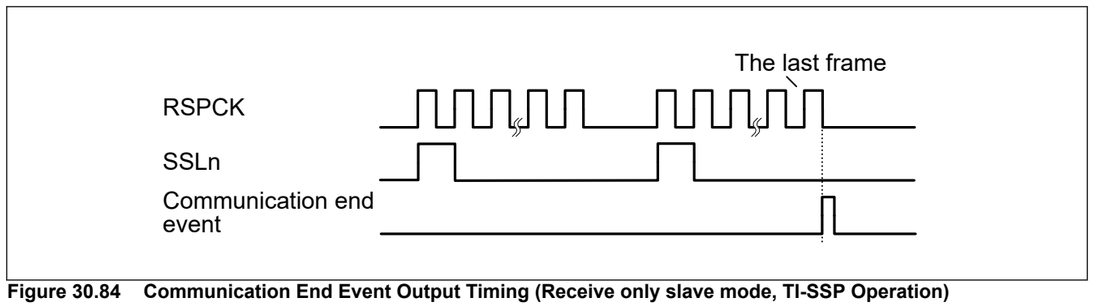


Figure 30.84 Communication End Event Output Timing (Receive only slave mode, TI-SSP Operation)

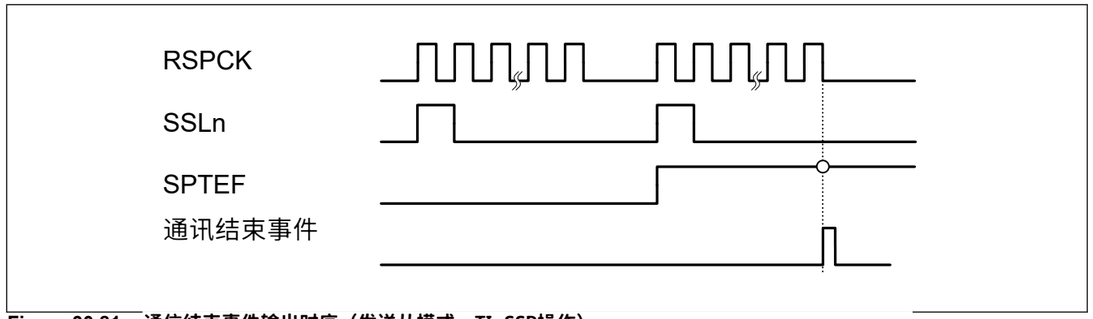


Figure 30.81 通信结束事件输出时序（发送从模式，TI-SSP操作）

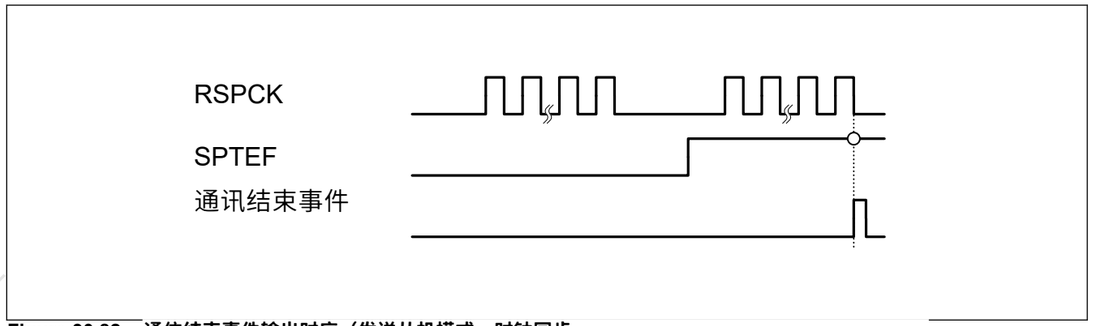


Figure 30.82 通信结束事件输出时序（发送从机模式，时钟同步 Operation)

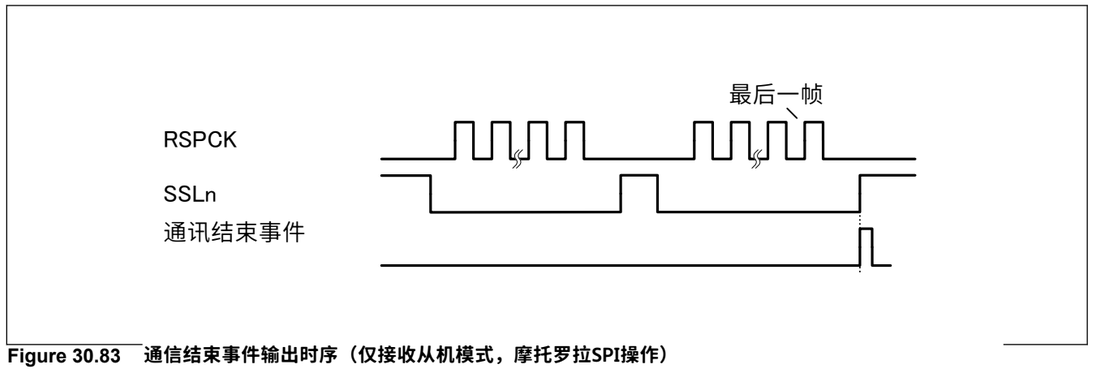


Figure 30.83 通信结束事件输出时序（仅接收从机模式，摩托罗拉SPI操作）

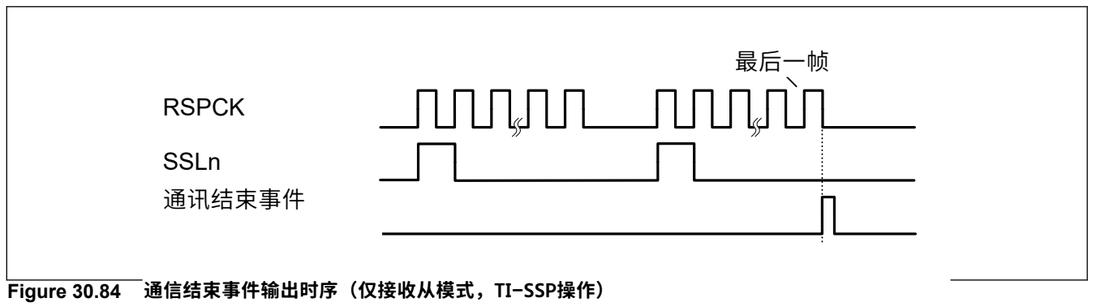


Figure 30.84 通信结束事件输出时序（仅接收从模式，TI-SSP操作）

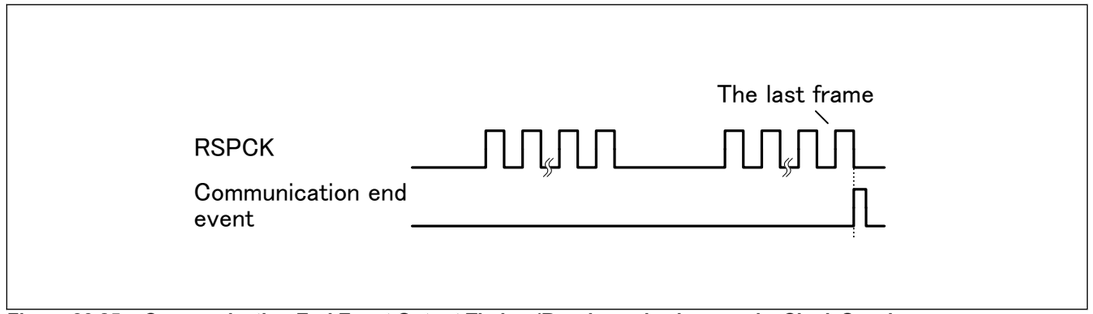


Figure 30.85 Communication End Event Output Timing (Receive only slave mode, Clock Synchronous Operation)

30.4.6 Synchronization bypass function

This IP has an internal clock (PCLK) and an operation clock (TCLK), and each has its own operation circuit. Therefore, a synchronization circuit is inserted between the signals between different clocks, and a signal delay between different clocks requires a synchronization delay time (2 to 3 PCLK or 2 to 3 TCLK).

However, the synchronization circuit can be bypassed by the BPEN = 1 of the RSPI control register (SPCR) only when the same clock is input as the internal bus clock and the operation clock. In this case, the synchronization delay time is excluded, and responsiveness is improved.

In addition, this IP has a synchronization circuit between the communication clock (RSPCK) and the operation clock (TCLK), but this synchronization circuit cannot be bypassed.

30.5 Usage Notes

30.5.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable the SPI operation. The SPI is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details on the Module Stop Control Register B, see section 10, Low Power Modes.

30.5.2 Constraint on Low-Power Functions

When using the module-stop function and entering a low-power mode other than Sleep mode, set the SPCR.SPE bit to 0 before completing communication.

30.5.3 Constraints on Starting Transfer

If the ICU.IELSRn.IR flag is 1 when transfer starts, the interrupt request is internally retained, which can lead to unanticipated behavior of the ICU.IELSRn.IR flag.

To prevent this, use the following procedure to clear interrupt requests before enabling operations (by setting the SPCR.SPE bit to 1):

1. Confirm that transfer stopped (the SPCR.SPE bit is 0).
2. Set the associated interrupt enable bit (SPCR.SPTIE bit or SPCR.SPRIE bit) to 0.
3. Read the associated interrupt enable bit (SPCR.SPTIE bit or SPCR.SPRIE bit) and confirm that its value is 0.
4. Set the ICU.IELSRn.IR flag to 0.

30.5.4 Constraints on Mode-Fault, Underrun, Overrun, Parity Error, or Receive Data Ready Event Output

Using the mode-fault, underrun, overrun, parity error, or receive data ready event is prohibited if the SPI is in multi-master mode (when the SPCR.SPMS bit is 0, the SPCR.MSTR bit is 1, and the SPCR.MODFEN bit is 1).

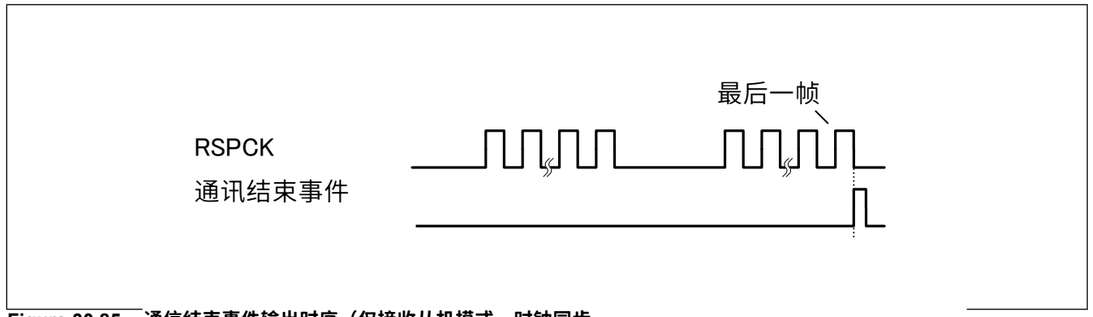


Figure 30.85 通信结束事件输出时序（仅接收从机模式，时钟同步 Operation)

30.4.6 同步旁路功能

这个IP有一个内部时钟（PCLK）和一个操作时钟（TCLK），每个都有自己的操作电路。因此，在不同时钟之间的信号之间插入同步电路，不同时钟之间的信号延迟需要同步延迟时间（2到3个PCLK或2到3个TCLK）。

但是，只有当输入与内部总线时钟和操作时钟相同的时钟时，才能通过RSPI控制寄存器(SPCR)的BPEN=1绕过同步电路。在这种情况下，排除了同步延迟时间，提高了响应性。

另外，这个IP在通信时钟（RSPCK）和工作时钟（TCLK）之间有一个同步电路，但是这个同步电路是不能绕过的。

30.5 使用说明

30.5.1 模块停止状态的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用SPI操作。SPI在复位后最初停止。释放模块停止状态可以访问寄存器。有关模块停止控制寄存器B的详细信息，请参见第10节，低功耗模式。

30.5.2 对低功耗功能的限制

当使用模块停止功能并进入除睡眠模式以外的低功耗模式时，在完成通信之前将SPCR.SPE位设置为0。

30.5.3 开始传输的限制

如果ICU.IELSRn.IR标志在传输开始时为1，则内部保留中断请求，这可能导致ICU.IELSRn.IR标志的意外行为。

为防止这种情况发生，请使用以下程序在使能操作之前清除中断请求（通过将SPCR.SPE位设置为1）：

1.确认传输停止（SPCR.SPE位为0）。

2.将相关的中断使能位（SPCR.SPTIE位或SPCR.SPRIE位）设置为0。

3.读取相关的中断使能位（SPCR.SPTIE位或SPCR.SPRIE位）并确认其值为0。

4.将ICU.IELSRn.IR标志设置为0。

30.5.4 模式故障、欠载、溢出、奇偶校验错误或接收数据的约束就绪事件输出

如果SPI处于多主模式（当SPCR.SPMS位为0，SPCR.MSTR位为1，并且SPCR.MODFEN位为1)。

30.5.5 Constraints on the SPSR.SPRF and SPSR.SPTEF Flags

If the polling flags, SPRF and SPTEF, are used, using the interrupts is prohibited, and you must set the SPCR.SPRIE and SPCR.SPTIE bits to 0. Either the interrupts or the flags can be used, but not both.

30.5.5 SPSR.SPRF和SPSR.SPTEF标志的约束

如果使用轮询标志SPRF和SPTEF，则禁止使用中断，您必须设置SPCR.SPRIE和SPCR.SPTIE位为0。可以使用中断或标志，但不能同时使用。

31. Cyclic Redundancy Check (CRC)

31.1 Overview

The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows to monitor the access to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.

Table 31.1 lists the CRC calculator specifications and Figure 31.1 shows a block diagram.

Table 31.1 CRC calculator specifications

Item	Description	
Data size	8-bit	32-bit
Data for CRC calculation*1	CRC code generated for data in 8n-bit units (where n is a natural number)	CRC code generated for data in 32n-bit units (where n is a natural number)
CRC processor unit	Operation executed on 8 bits in parallel	Operation executed on 32 bits in parallel
CRC generating polynomial	One of three generating polynomials that is selectable: [8-bit CRC] • $X^8 + X^2 + X + 1$ (CRC-8) [16-bit CRC] • $X^{16} + X^{15} + X^2 + 1$ (CRC-16) • $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT).	One of two generating polynomials that is selectable: [32-bit CRC] • $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C).
CRC calculation switching	The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication	
Module-stop function	Module-stop state can be set to reduce power consumption	
CRC snoop	Monitor reads from and writes to a certain register address	
TrustZone Filter	Security attribution can be set	

Note 1. This function cannot divide data used in CRC calculations. Write data in 8-bit or 32-bit units.

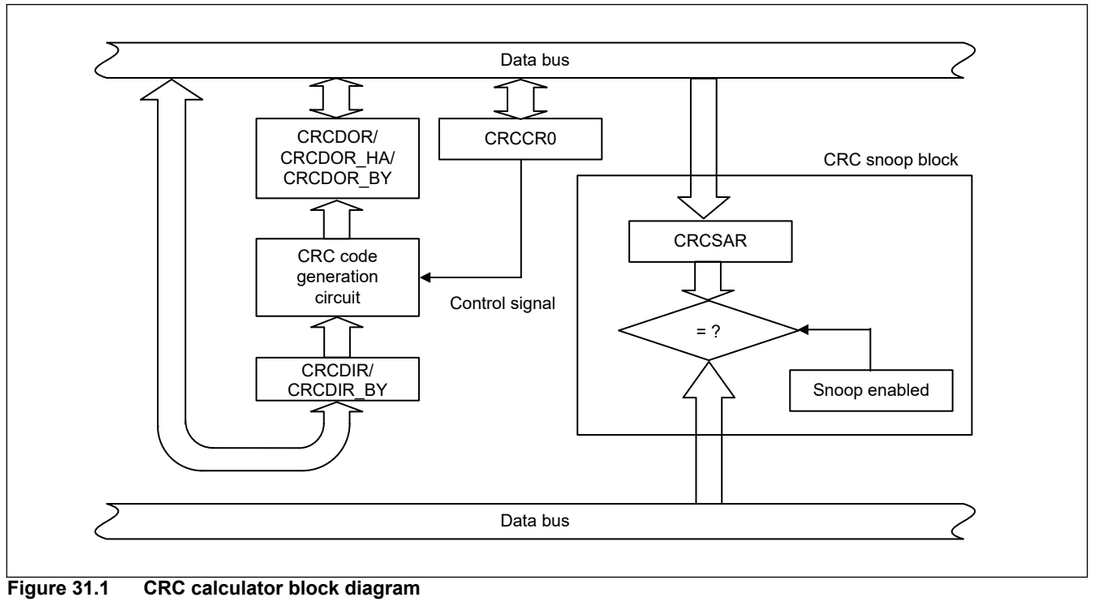


Figure 31.1 CRC calculator block diagram

31. 循环冗余校验(CRC)

31.1 Overview

循环冗余校验(CRC)生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外，还可以使用各种CRC生成多项式。snoop功能允许监视对特定地址的访问。此功能在需要在某些事件中自动生成CRC代码的应用中很有用，例如监视对串行发送缓冲区的写入和从串行接收缓冲区的读取。

表31.1列出了CRC计算器规格，图31.1显示了框图。

Table 31.1 CRC计算器规格

Item	Description	
数据大小	8-bit	32-bit
CRC计算数据*1	为8n位单元中的数据生成的CRC码（其中n是自然数）	为32n位单元中的数据生成的CRC码（其中n是自然数）
CRC处理器单元	在8位上并行执行的操作	在32位上并行执行的操作
CRC生成多项式	可选择的三个生成多项式之一：[8位CRC]● [16-bit CRC] • $X^{16} + X^{15} + X^2 + 1$ (CRC-16) • $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT).	可选择的两个生成多项式之一：[32位CRC]● $X^{11} +$ $X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C).
CRC计算切换	CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信	
Module-stop function	可设置模块停止状态以降低功耗	
CRC snoop	监视器读取和写入某个寄存器地址	
TrustZone Filter	可设置安全属性	

注1.此功能不能除以CRC计算中使用的数据。以8位或32位为单位写入数据。

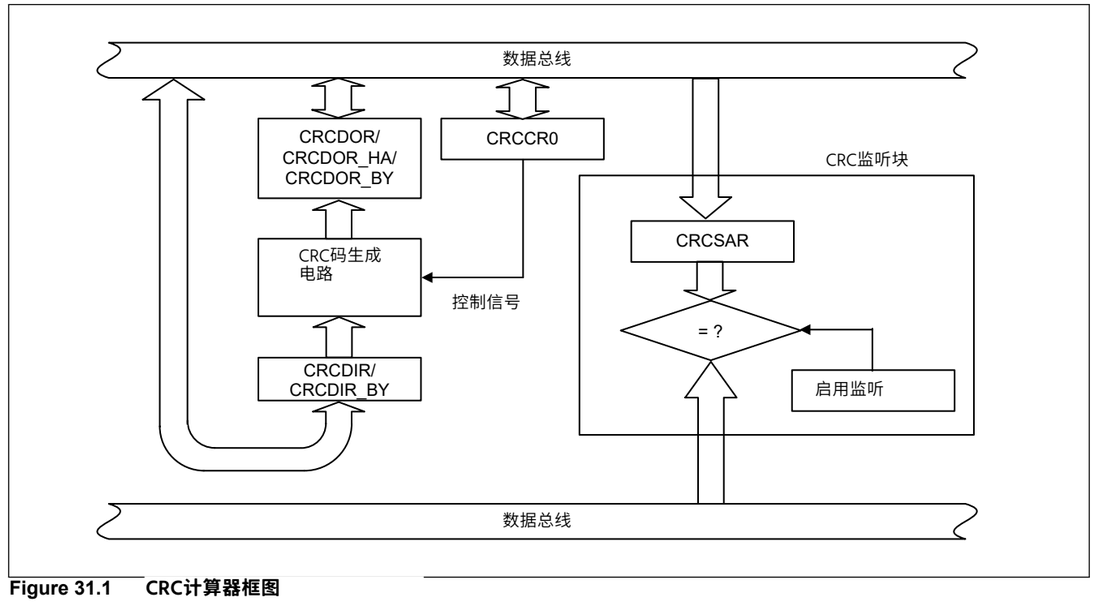


Figure 31.1 CRC计算器框图

31.2 Register Descriptions

31.2.1 CRCCR0 : CRC Control Register 0

Base address: CRC = 0x4010_8000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DORCLR	LMS	—	—	—	GPS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	GPS[2:0]	CRC Generating Polynomial Switching 0 0 1: 8-bit CRC-8 ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC-32C ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) Others: No calculation is executed	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	LMS	CRC Calculation Switching 0: Generate CRC code for LSB-first communication 1: Generate CRC code for MSB-first communication	R/W
7	DORCLR	CRCDOR/CRCDOR_HA/CRCDOR_BY Register Clear 0: No effect 1: Clear the CRCDOR/CRCDOR_HA/CRCDOR_BY register	W

GPS[2:0] bits (CRC Generating Polynomial Switching)

The GPS[2:0] bits select the CRC generating polynomial.

LMS bit (CRC Calculation Switching)

The LMS bit selects the bit order of generated CRC code. Transmit the lower byte of the CRC code first for LSB-first communication and the upper byte first for MSB-first communication. For details on transmitting and receiving CRC code, see section 31.3. Operation.

DORCLR bit (CRCDOR/CRCDOR_HA/CRCDOR_BY Register Clear)

Write 1 to the DORCLR bit to set the CRCDOR/CRCDOR_HA/CRCDOR_BY register to 0x00000000. This bit is read as 0. Only 1 can be written to it.

31.2.2 CRCCR1 : CRC Control Register 1

Base address: CRC = 0x4010_8000

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CRCSEN	CRCSWR	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W

31.2 注册说明

31.2.1 CRCCR0:CRC控制寄存器0

Base address: CRC = 0x4010_8000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DORCLR	LMS	—	—	—	GPS[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	GPS[2:0]	CRC生成多项式切换 0 0 1: 8-bit CRC-8 ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC-32C ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 其他：不执行计算	R/W
5:3	—	这些位被读取为0。写入值应为0。	R/W
6	LMS	CRC计算切换 0：生成LSB优先通信的CRC代码1：生成MSB优先通信的CRC代码	R/W
7	DORCLR	CRCDORCRCDOR_HACRCDOR_BY寄存器清零 0：无效1：清除CRCDORCRCDOR_HACRCDOR_BY寄存器	W

GPS[2:0]位（CRC生成多项式切换）

GPS[2:0]位选择CRC生成多项式。

LMS位（CRC计算切换）

LMS位选择生成的CRC码的位顺序。对于LSB在先的通信，首先发送CRC码的低字节，对于MSB在先的通信，首先发送高字节。有关发送和接收CRC码的详细信息，请参见第31.3节。手术。

DORCLR位（CRCDORCRCDOR_HACRCDOR_BY寄存器清零）

将1写入DORCLR位以将CRCDORCRCDOR_HACRCDOR_BY寄存器设置为0x00000000。该位读为0。只能写入1。

31.2.2 CRCCR1：CRC控制寄存器1

Base address: CRC = 0x4010_8000

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CRCSEN	CRCSWR	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
6	CRCSWR	Snoop-On-Write/Read Switch 0: Snoop-on-read 1: Snoop-on-write	R/W
7	CRCSEN	Snoop Enable 0: Disabled 1: Enabled	R/W

CRCSWR bit (Snoop-On-Write/Read Switch)

The CRCSWR bit selects the direction of access in the CRC snoop function.

When this bit is set to 0 (initial value), the CRC snoop operation to read a specific register is enabled. Similarly, when this bit is set to 1, the CRC snoop operation to write a specific register is enabled.

CRCSEN bit (Snoop Enable)

When the CRCSEN bit is set to 1, the CRC snoop operation is enabled. When this bit is set to 0, the CRC snoop operation is disabled.

31.2.3 CRCDIR/CRCDIR_BY : CRC Data Input Register

Base address: CRC = 0x4010_8000

Offset address: 0x04

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC input data The CRCDIR register is a 32-bit read/write register to write data for CRC-32 or CRC-32C calculation. The CRCDIR_BY (CRCDIR[31:24]) is an 8-bit read/write register to write data for CRC-8, CRC-16, or CRC-CCITT calculation.	R/W

31.2.4 CRCDOR/CRCDOR_HA/CRCDOR_BY : CRC Data Output Register

Base address: CRC = 0x4010_8000

Offset address: 0x08

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC output data The CRCDOR register is a 32-bit read/write register for CRC-32 or CRC-32C calculation. The CRCDOR_HA (CRCDOR[31:16]) register is a 16-bit read/write register for CRC-16 or CRC-CCITT calculation. The CRCDOR_BY (CRCDOR[31:24]) register is an 8-bit read/write register for CRC-8 calculation. Because its initial value is 0x00000000, rewrite the CRCDOR/CRCDOR_HA/CRCDOR_BY register to perform the calculations using a value other than the initial value. Data written to the CRCDIR/CRCDIR_BY register is CRC calculated and the result is stored in the CRCDOR/CRCDOR_HA/CRCDOR_BY register. If the CRC code is calculated following the transferred data and the result is 0x00000000, there is no CRC error.	R/W

Bit	Symbol	Function	R/W
6	CRCSWR	Snoop-On-Write/Read Switch 0: Snoop-on-read 1: Snoop-on-write	R/W
7	CRCSEN	侦听启用 0：禁用1： 启用	R/W

CRCSWR bit (Snoop-On-Write/Read Switch)

CRCSWR位选择CRC探听功能中的访问方向。

当该位设置为0（初始值）时，启用读取特定寄存器的CRC监听操作。类似地，当该位设置为1时，将启用写入特定寄存器的CRC侦听操作。

CRCSEN bit (Snoop Enable)

当CRCSEN位设置为1时，启用CRC侦听操作。当该位设置为0时，CRC监听操作被禁用。

31.2.3 CRCDIRCRCDIR_BY:CRC数据输入寄存器

Base address: CRC = 0x4010_8000

Offset address: 0x04

Bit position:	31																												0
Bit field:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC输入数据 CRCDIR寄存器是一个32位读写寄存器，用于写入数据以进行CRC-32或CRC-32C计算。CRCDIR_BY(CRCDIR[31:24])是一个8位读写寄存器，用于为CRC-8、CRC-16或CRC-CCITT计算写入数据。	R/W

31.2.4 CRCDORCRCDOR_HACRCDOR_BY:CRC数据输出寄存器

Base address: CRC = 0x4010_8000

Offset address: 0x08

Bit position:	31																												0
Bit field:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC输出数据 CRCDOR寄存器是一个32位读写寄存器，用于CRC-32或CRC-32C计算。CRCDOR_HA(CRCDOR[31:16])寄存器是用于CRC-16或 CRC-CCITT calculation. CRCDOR_BY(CRCDOR[31:24])寄存器是一个用于CRC-8计算的8位读写寄存器。由于其初始值为0x00000000，因此重写CRCDORCRCDOR_HACRCDOR_BY寄存器以使用初始值以外的值执行计算。写入CRCDIRCRCDIR_BY寄存器的数据经过CRC计算，结果存储在CRCDORCRCDOR_HACRCDOR_BY寄存器中。如果在传输数据之后计算CRC码，结果为0x00000000，则没有CRC错误。	R/W

31.2.5 CRCSAR : Snoop Address Register

Base address: CRC = 0x4010_8000

Offset address: 0x0C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	CRCSA[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CRCSA[13:0]	Register Snoop Address These bits store the TDR or RDR address in the SCI module to snoop	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

CRCSA[13:0] bits (Register Snoop Address)

The CRCSA[13:0] bits specify the lower address 14 bits of the register monitored by the CRC snoop operation.

Only the following addresses can be used for the CRCSA[13:0] bits:

- 0x4011_8004: SCI0.TDR, 0x4011_8000:SCI0.RDR
- 0x4011_8104: SCI1.TDR, 0x4011_8100:SCI1.RDR
- 0x4011_8204: SCI2.TDR, 0x4011_8200:SCI2.RDR
- 0x4011_8304: SCI3.TDR, 0x4011_8300:SCI3.RDR
- 0x4011_8404: SCI4.TDR, 0x4011_8400:SCI4.RDR
- 0x4011_8904: SCI9.TDR, 0x4011_8900:SCI9.RDR

31.3 Operation

31.3.1 Basic Operation

The CRC calculator generates CRC codes for use in LSB-first or MSB-first transfer.

The following examples show CRC code generation for input data (0xF0) using the 16-bit CRC-CCITT generating polynomial ($X^{16} + X^{12} + X^5 + 1$). In these examples, the value of the CRC Data Output Register (CRCDOR_HA) is cleared before CRC calculation.

When an 8-bit CRC (with the polynomial $X^8 + X^2 + X + 1$) is in use, the valid bits of the CRC code are obtained in CRCDOR_BY. When a 32-bit CRC is in use, the valid bits of the CRC code are obtained in CRCDOR.

Figure 31.2 and Figure 31.3 show the LSB-first and MSB-first data transmission examples respectively. Figure 31.4 and Figure 31.5 show the LSB-first and MSB-first data reception examples.

31.2.5 CRCSAR:监听地址寄存器

Base address: CRC = 0x4010_8000

Offset address: 0x0C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	CRCSA[13:0]													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CRCSA[13:0]	注册监听地址 这些位存储SCI模块中的TDR或RDR地址以进行监听	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W

CRCSA[13:0]位（寄存器监听地址）

CRCSA[13:0]位指定由CRC侦听操作监视的寄存器的低地址14位。

CRCSA[13:0]位只能使用以下地址：

- 0x4011_8004: SCI0.TDR, 0x4011_8000:SCI0.RDR
- 0x4011_8104: SCI1.TDR, 0x4011_8100:SCI1.RDR
- 0x4011_8204: SCI2.TDR, 0x4011_8200:SCI2.RDR
- 0x4011_8304: SCI3.TDR, 0x4011_8300:SCI3.RDR
- 0x4011_8404: SCI4.TDR, 0x4011_8400:SCI4.RDR
- 0x4011_8904: SCI9.TDR, 0x4011_8900:SCI9.RDR

31.3 Operation

31.3.1 基本操作

CRC计算器生成用于LSB优先或MSB优先传输的CRC代码。

以下示例显示了使用16位CRC-CCITT生成多项式(X16+X12+X5+1)为输入数据(0xF0)生成CRC码。在这些示例中，CRC数据输出寄存器(CRCDOR_HA)的值在CRC计算之前被清除。

当使用8位CRC（多项式X8+X2+X+1）时，CRC码的有效位在CRCDOR_BY。使用32位CRC时，在CRCDOR中获取CRC码的有效位。

图31.2和图31.3分别显示了LSB-first和MSB-first数据传输示例。图31.4和图31.5显示了LSB优先和MSB优先的数据接收示例。

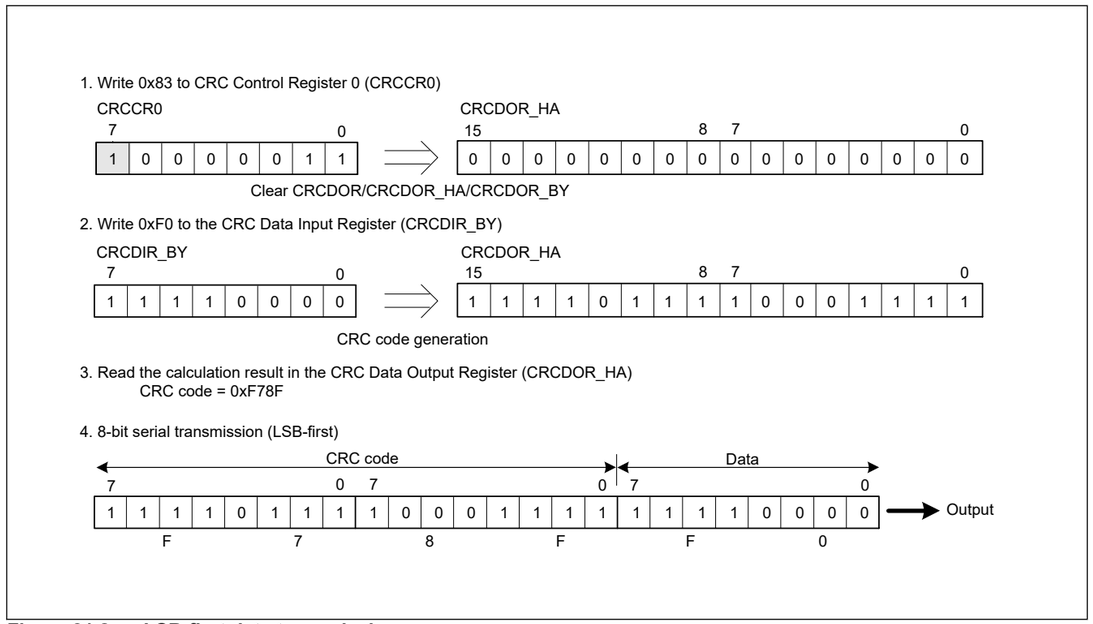


Figure 31.2 LSB-first data transmission

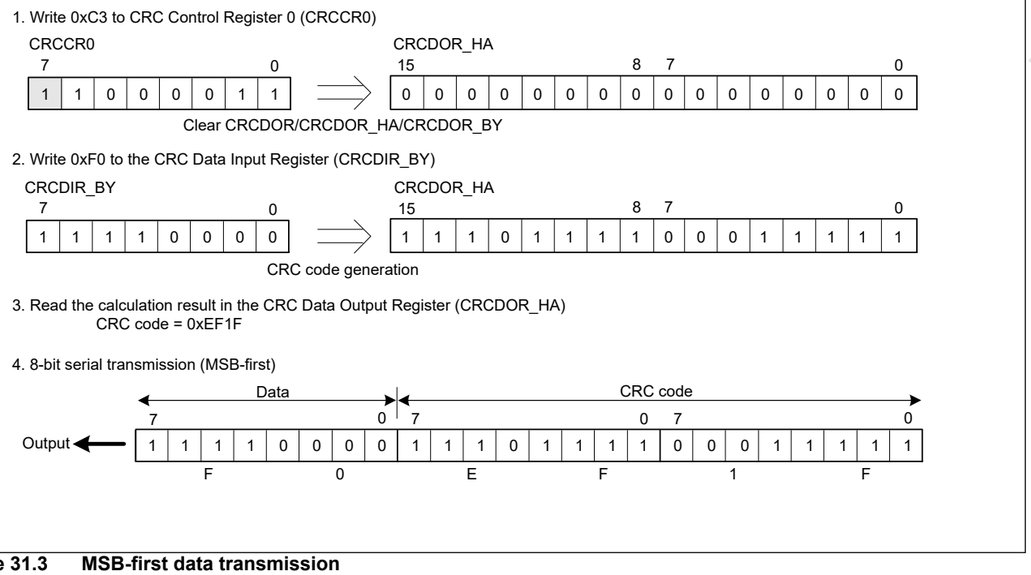


Figure 31.3 MSB-first data transmission

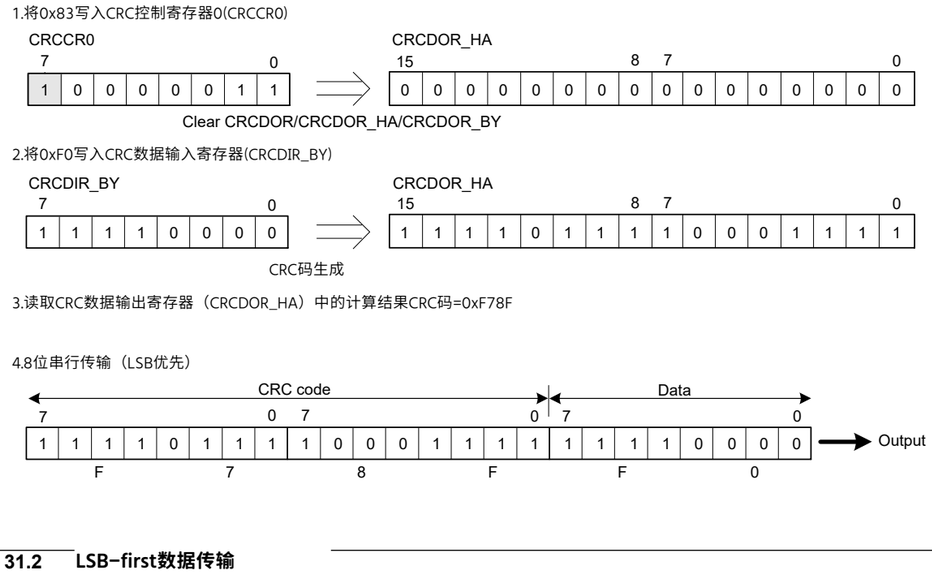


Figure 31.2 LSB−first数据传输

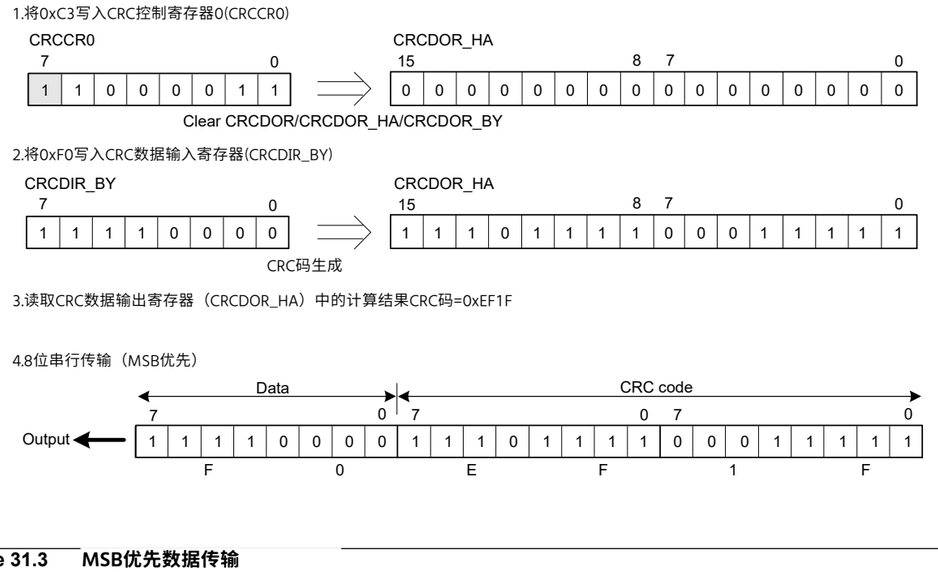
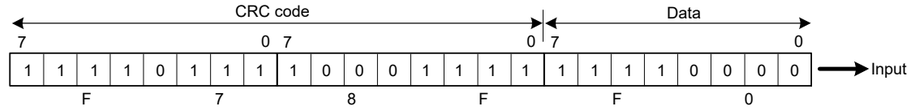
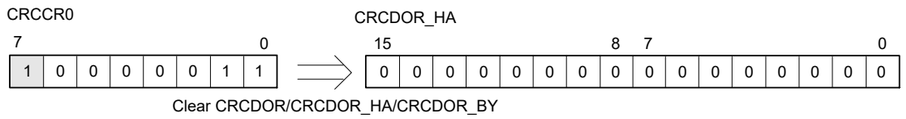


Figure 31.3 MSB优先数据传输

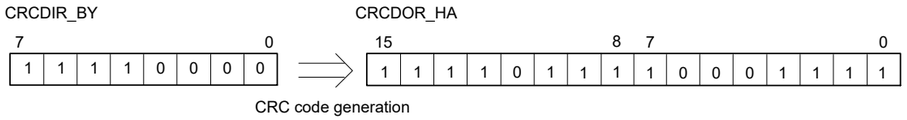
1. 8-bit serial reception (LSB-first)



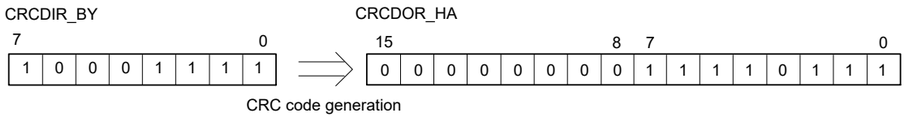
2. Write 0x83 to the CRC Control Register 0 (CRCCR0)



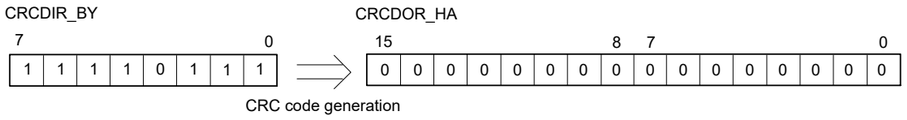
3. Write 0xF0 to the CRC Data Input Register (CRCDIR_BY)



4. Write 0x8F to the CRC Data Input Register (CRCDIR_BY)



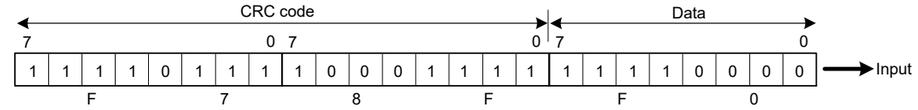
5. Write 0xF7 to the CRC Data Input Register (CRCDIR_BY)



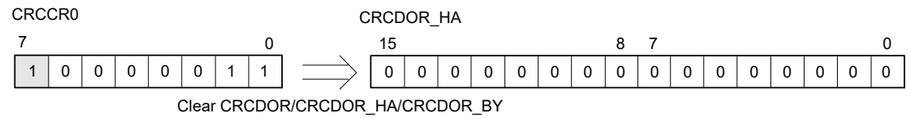
6. Read the calculation result in the CRC Data Output Register (CRCDOR_HA)
CRC code = 0x0000 → no error

Figure 31.4 LSB-first data reception

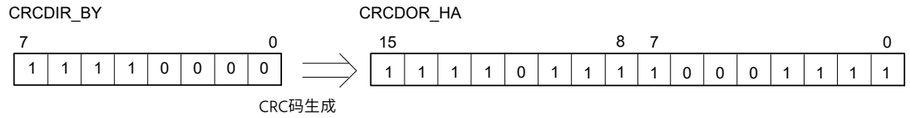
1.8位串行接收（LSB优先）



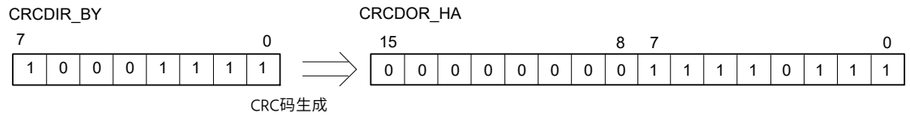
2.将0x83写入CRC控制寄存器0(CRCCR0)



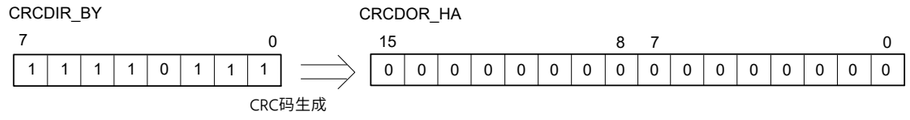
3.将0xF0写入CRC数据输入寄存器(CRCDIR_BY)



4.将0x8F写入CRC数据输入寄存器(CRCDIR_BY)



5.将0xF7写入CRC数据输入寄存器(CRCDIR_BY)



6.读取CRC数据输出寄存器（CRCDOR_HA）中的计算结果CRC码=0x0000→无错误

Figure 31.4 LSB-first数据接收

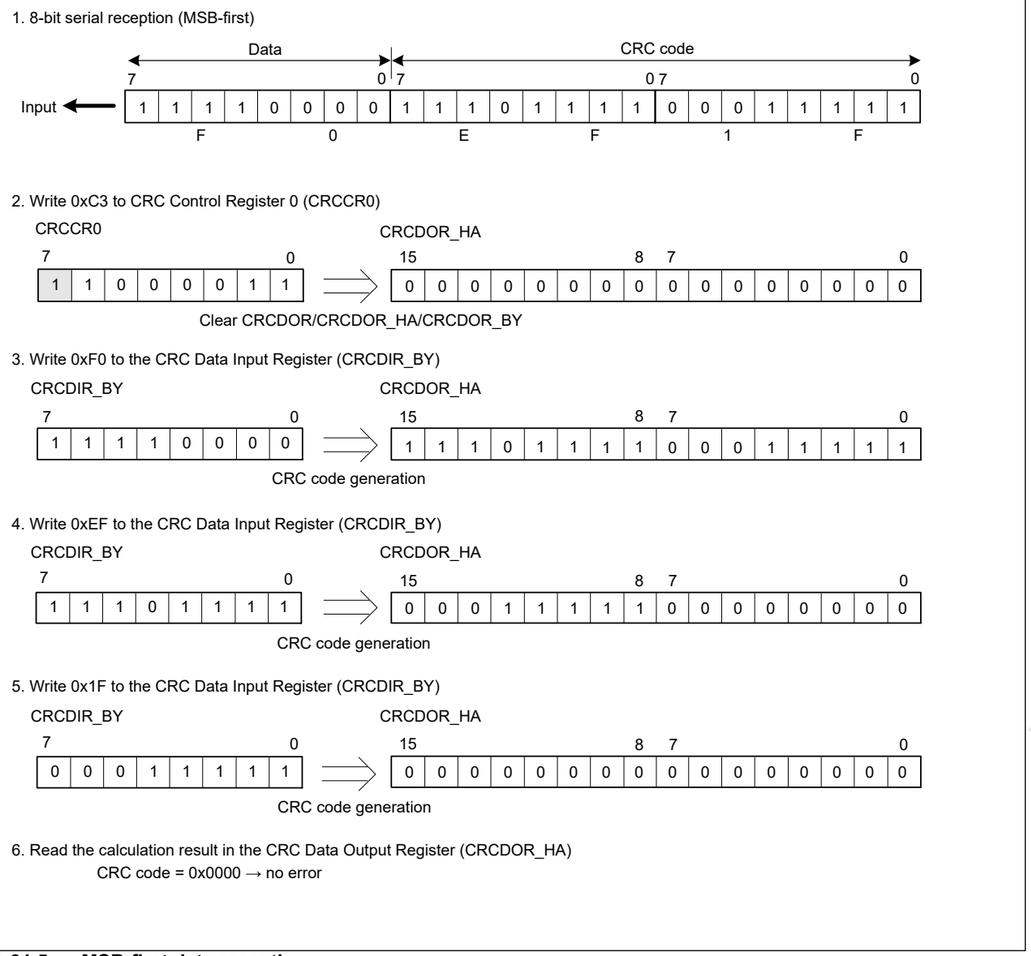


Figure 31.5 MSB-first data reception

31.3.2 CRC Snoop Function

The CRC snoop function monitors reads from and writes to a specific register and performs CRC calculation on the monitored data automatically. Because the CRC snoop function recognizes writes to and reads from a specific register address as a trigger to automatically perform CRC calculation, there is no need to write data to the CRCDIR register. All I/O register specified in the section 31.2.5. CRCSAR : Snoop Address Register are subject to the CRC snoop. The CRC snoop is useful in monitoring writes to the SCIn.TDR (n = 0 to 4, 9) register, and reads from the SCIn.RDR (n = 0 to 4, 9) register.

To use this function, write the lower address 14 bits of a specific register to bits CRCSA13 to CRCSA0 in the CRCSAR register, and set CRCSEN bit in the CRCCR1 register to 1. Then, set the CRCSWR bit in the CRCCR1 register to 1 to enable snooping on writes to the target register, or set the CRCSWR bit in the CRCCR1 register to 0 to enable snooping on reads from the target register. It is possible that access to a target I/O register may be executed before the CRCSWR bit write completed. In this case, the data is not stored in the CRCDIR register. To avoid this issue, before accessing I/O register, read back the CRCSWR bit that was written to confirm that the write completed.

When both the CRCSEN and CRCSWR bits are set to 1, and data is written to a target register in a bus master module such as the CPU, DMAC, and DTC, the CRC calculator stores the data in the CRCDIR register and performs CRC calculation. Similarly, when the CRCSEN bit is set to 1, CRCSWR bit to 0, and data is read from a target register in a bus master

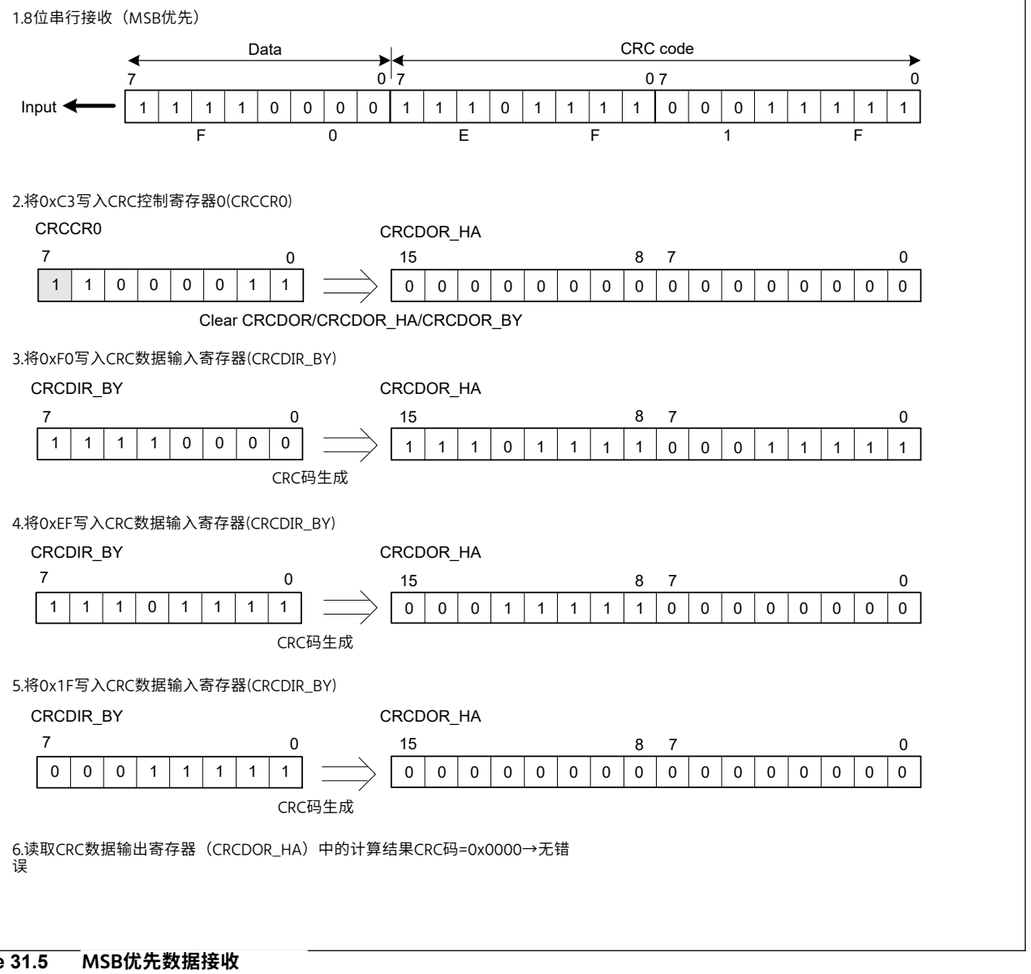


Figure 31.5 MSB优先数据接收

31.3.2 CRC监听功能

CRCsnoop功能监视对特定寄存器的读取和写入，并自动对监视的数据执行CRC计算。由于CRCsnoop功能将特定寄存器地址的写入和读取识别为触发以自动执行CRC计算，因此无需将数据写入CRCDIR寄存器。第31.2.5节中指定的所有IO寄存器。CRCSAR:SnoopAddressRegister受CRCsnoop影响。CRCsnoop在监视对SCIn.TDR(n=0到4 9)寄存器的写入以及从SCIn.RDR(n=0到4 9)寄存器中读取时很有用。

要使用此功能，将特定寄存器的低地址14位写入CRCSAR寄存器中的位CRCSA13到CRCSA0，并将CRCCR1寄存器中的CRCSEN位设置为1。然后，将CRCCR1寄存器中的CRCSWR位设置为1以启用对目标寄存器的写入进行监听，或者将CRCCR1寄存器中的CRCSWR位设置为0以启用对目标寄存器读取的监听。可能在CRCSWR位写入完成之前执行对目标IO寄存器的访问。在这种情况下，数据不存储在CRCDIR寄存器中。为避免此问题，在访问IO寄存器之前，请回读已写入的CRCSWR位以确认写入已完成。

当CRCSEN和CRCSWR位都设置为1，并且数据被写入总线主模块（如CPU、DMAC和DTC）中的目标寄存器时，CRC计算器将数据存储在CRCDIR寄存器中并执行CRC计算。类似地，当CRCSEN位设置为1时，CRCSWR位设置为0，并且从总线主机中的目标寄存器读取数据

module such as the CPU, DMAC, and DTC, the CRC calculator stores the data in the CRCDIR register and performs CRC calculations.

When the CRC code is generated by using CRC-8, CRC-16, and CRC-CCITT generating polynomial, the target register is accessed in 1 byte (8 bits). Similarly, when the CRC code is generated by using CRC-32 and CRC-32C generating polynomial, the target register is accessed in words (32 bits).

When CPU is halted, CRC snoop operation is invalid.

31.4 Usage Notes

31.4.1 Settings for the Module-Stop State

The Module Stop Control Register C (MSTPCRC) can enable or disable CRC calculator operation. The CRC calculator is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

31.4.2 Note on Transmission

The transmission sequence for the CRC code differs based on whether the transmission is LSB-first or MSB-first. Figure 31.6 shows an LSB-first and MSB-first data transmission.

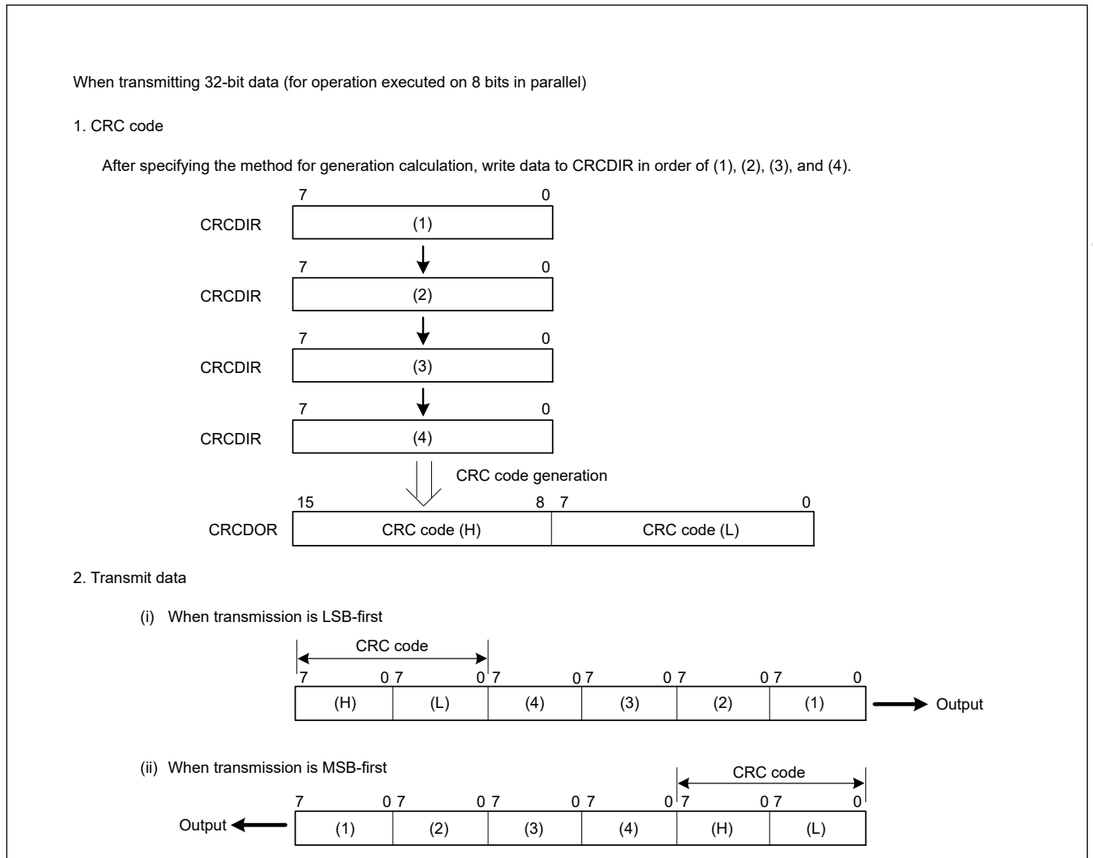


Figure 31.6 LSB-first and MSB-first data transmission

CPU、DMAC和DTC等模块，CRC计算器将数据存储在CRCDIR寄存器中并执行CRC计算。

当使用CRC-8、CRC-16和CRC-CCITT生成多项式生成CRC码时，以1个字节（8位）访问目标寄存器。类似地，当使用CRC-32和CRC-32C生成多项式生成CRC码时，以字（32位）访问目标寄存器。

当CPU停止时，CRCsnoop操作无效。

31.4 使用说明

31.4.1 模块停止状态的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用CRC计算器操作。CRC计算器在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

31.4.2 传输注意事项

CRC码的传输顺序根据传输是LSB在先还是MSB在先而有所不同。图31.6显示了LSB优先和MSB优先的数据传输。

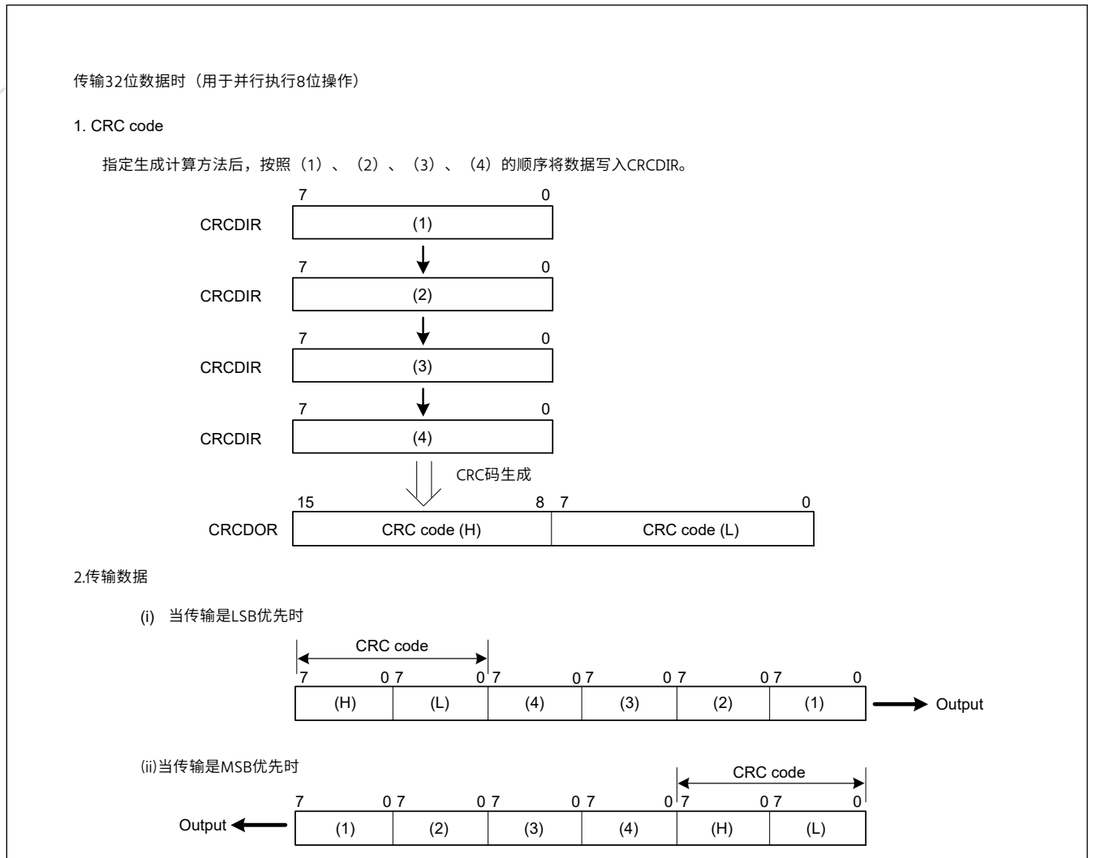


Figure 31.6 LSB-first和MSB-first数据传输

32. Trigonometric Function Unit (TFU)

32.1 Overview

An trigonometric Function Unit (TFU) handles the high-speed calculation of sinf, cosf, atan2f, and hypotf functions.

For details, refer to the manual for the functions using TFU.

The ICLK is used as the operating clock for the TFU.

Table 32.1 lists the specifications of the TFU.

Table 32.1 TFU specifications

Item	Description				
Arithmetic Processing	Calculation of sine, cosine, arctangent, and $\sqrt{x^2+y^2}$ • A sine and cosine can be simultaneously calculated. • An arctangent and $\sqrt{x^2+y^2}$ can be simultaneously calculated.				
Range and Unit of Values	**Arithmetic Processing**	**I/O**		**Range**	**Unit**
	Calculating sine	Input	Angle θ	$-float\_max \le \theta \le float\_max$ *1	radian
		Output	$\sin\theta$	$-1.0 \le \sin\theta \le 1.0$	—
	Calculating cosine	Input	Angle θ	$-float\_max \le \theta \le float\_max$ *1	radian
		Output	$\cos\theta$	$-1.0 \le \cos\theta \le 1.0$	—
	Calculating arctangent	Input	x and y coordinates	$-float\_max \le x \le float\_max$ *1 $-float\_max \le y \le float\_max$ *1	—
		Output	$\arctan(y/x)$	$-\pi \le \arctan(y/x) \le \pi$	radian
	Calculating $\sqrt{x^2+y^2}$	Input	x and y coordinates	$-float\_max \le x \le float\_max$ *1 $-float\_max \le y \le float\_max$ *1	—
		Output	$\sqrt{x^2+y^2}$	$0 \le \sqrt{x^2+y^2} \le \infty$	—
Data Type for Processing	Single-precision floating-point				
Number of cycles for calculation	Sine: 14 Cosine: 14 Arctangent: 14 $\sqrt{x^2+y^2}$: 14 + α*2				

Note 1. float_max is the maximum value that can be expressed as single-precision floating-point: $(2 - 2^{-23}) \times 2^{127}$.

Note 2. α is the number of cycles it takes for software to multiply to obtain result.

32. 三角函数单元(TFU)

32.1 Overview

三角函数单元(TFU)处理sinf、cosf、atan2f和hypotf函数的高速计算。

有关详细信息，请参阅使用TFU的功能的手册。

ICLK用作TFU的工作时钟。

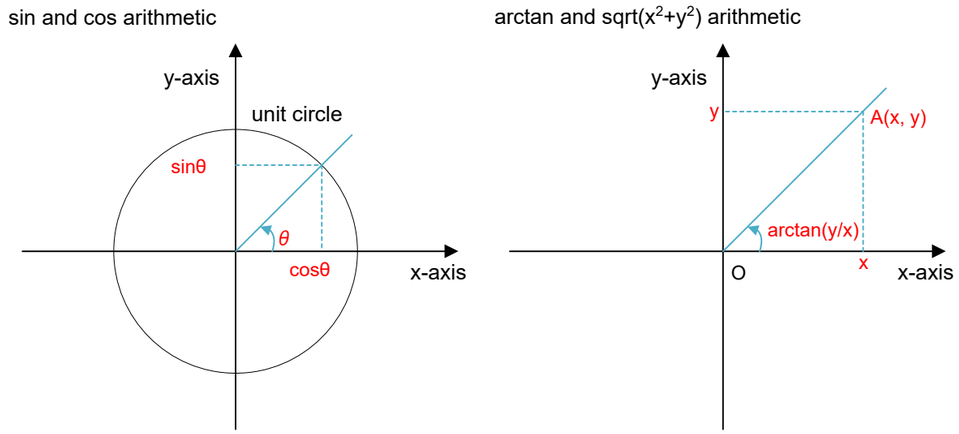
表32.1列出了TFU的规格。

Table 32.1 TFU specifications

Item	Description				
算术处理	计算正弦、余弦、反正切和x2+y2 可以同时计算正弦和余弦。 可以同时计算反正切和x2+y2。				
范围和单位	**算术处理**	**I/O**		**Range**	**Unit**
	计算正弦	Input	Angle θ	$-float\_max \le \theta \le float\_max$ *1	radian
		Output	$\sin\theta$	$-1.0 \le \sin\theta \le 1.0$	—
	计算余弦	Input	Angle θ	$-float\_max \le \theta \le float\_max$ *1	radian
		Output	$\cos\theta$	$-1.0 \le \cos\theta \le 1.0$	—
	Calculating arctangent	Input	x和y坐标	$-float\_max \le x \le float\_max$ *1 $-float\_max \le y \le float\_max$ *1	—
		Output	$\arctan(y/x)$	$-\pi \le \arctan(y/x) \le \pi$	radian
	Calculating $\sqrt{x^2+y^2}$	Input	x和y坐标	$-float\_max \le x \le float\_max$ *1 $-float\_max \le y \le float\_max$ *1	—
		Output	$\sqrt{x^2+y^2}$	$0 \le \sqrt{x^2+y^2} \le \infty$	—
数据类型 Processing	Single-precision floating-point				
计算周期数	Sine: 14 Cosine: 14 Arctangent: 14 $\sqrt{x^2+y^2}$: 14 + α*2				

注1.float_max是可以表示为单精度浮点的最大值：(2 2 23)×2127。

注2.α是软件乘以得到结果所需的周期数。



Note: sin and cos arithmetic:
Operation to find sinθ and cosθ, which are the triangular ratios of the input angle values θ.
arctan arithmetic:
Operation to find the angle value between the vector OA (O is the origin and A is the point indicated by the input coordinates x and y) and the positive part of the x-axis.
sqrt(x^2+y^2) arithmetic:
Operation to find the distance from the point A indicated by the input coordinates x and y to the origin O.
Note: By multiplying the TFU output result sqrt(x^2+y^2) by the constant k,
the distance between OA ($\sqrt{x^2+y^2}$) can be obtained. for details about k, see section 32.3.1. Arithmetic Processing.

Figure 32.1 Explanation for operations

32.1.1 Precautions on Use of the Arithmetic Unit for Trigonometric Functions

This section describes precautions on use of the Arithmetic Unit for Trigonometric functions.

32.1.1.1 General Precautions

When using TFU, recursive call is prohibited.

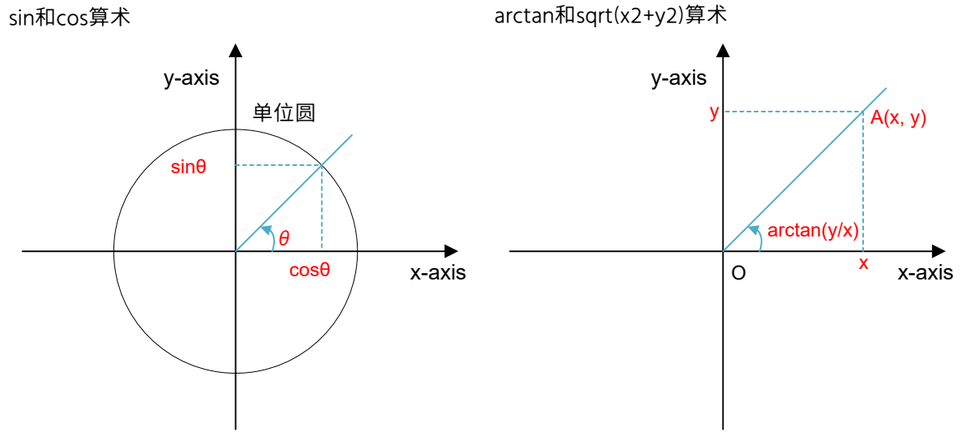
32.2 Register Descriptions

32.2.1 TRGSTS : Trigonometric Status Register

Base address: TFU = 0x4002_1000
Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ERRF	BSYF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BSYF	Calculation in progress flag 0: No calculating 1: Calculating	R
1	ERRF	Input error flag 0: No input error occurred 1: Input error occurred	R



Note: sin和cos算术：
求sinθ和cosθ的操作，它们是输入角度值θ的三角比。反正切算术：

求向量OA（O是原点，A是输入坐标x和y所指示的点）与x轴正部分之间的角度值的操作。sqrt(x2+y2)算术：

求输入坐标x和y指示的点A到原点O的距离的操作。
Note: 通过将TFU输出结果sqrt(x2+y2)乘以常数k，
可以得到OA(x2+y2)之间的距离。有关k的详细信息，请参见第32.3.1节。算术处理。

Figure 32.1 操作说明

32.1.1 三角函数使用算术单位的注意事项

本节介绍使用三角函数算术单元的注意事项。

32.1.1.1 一般注意事项

使用TFU时，禁止递归调用。

32.2 注册说明

32.2.1 TRGSTS:三角状态寄存器

Base address: TFU = 0x4002_1000
Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ERRF	BSYF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BSYF	计算中标志 0：不计算1：计算	R
1	ERRF	输入错误标志 0：未发生输入错误1：发生输入错误	R

Bit	Symbol	Function	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R

Note: Writing to this register is invalid.

BSYF bit (Calculation in progress flag)

The BSYF bit specifies the calculation in progress flag.

[Setting condition]

- When calculation started

[Clearing condition]

- When calculation completed

ERRF bit (Input error flag)

The ERRF bit specifies the input error flag.

[Setting condition]

- When input error occurred. For details on input error, see Table 32.6.

[Clearing condition]

- When the next calculation started

32.2.2 SCDT0 : Sine Cosine Data Register 0

Base address: TFU = 0x4002_1000

Offset address: 0x10

Bit position: 31 … 0

Bit field: SCDT0[31:0]

Value after reset: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
31:0	SCDT0[31:0]	Sine Cosine Data Register 0 (single-precision floating-point)	R/W

For the sincos operation, the SCDT0 register is dedicated for the output value cosθ of the trigonometric function unit. See Table 32.2 for detail. Writing to this register during operation is prohibited.

Writing to this register is prohibited even during the arctan/sqrt operation.

If read access is made to this register during the calculation, the result is read after the calculation is completed. At this time, the bus access is forced to wait until the channel process is completed.

See Table 32.2 for how to use this register.

32.2.3 SCDT1 : Sine Cosine Data Register 1

Base address: TFU = 0x4002_1000

Offset address: 0x14

Bit position: 31 … 0

Bit field: SCDT1[31:0]

Value after reset: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
31:0	SCDT1[31:0]	Sine Cosine Data Register 1 (single-precision floating-point)	R/W

Bit	Symbol	Function	R/W
7:2	—	这些位被读取为0。写入值应为0。	R

Note: 写入该寄存器无效。

BSYF位（计算中标志）

BSYF位指定计算进行中标志。

[Setting condition]

●计算开始时

[Clearing condition]

●计算完成时

ERRF位（输入错误标志）

ERRF位指定输入错误标志。

[Setting condition]

●发生输入错误时。有关输入错误的详细信息，请参见表32.6。

[Clearing condition]

●下次计算开始时

32.2.2 SCDT0:正余弦数据寄存器0

Base address: TFU = 0x4002_1000

Offset address: 0x10

Bit position: 31 … 0

Bit field: SCDT0[31:0]

重置后的值: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
31:0	SCDT0[31:0]	正弦余弦数据寄存器0（单精度浮点）	R/W

对于sincos运算，SCDT0寄存器专用于三角函数单元的输出值cosθ。看详细信息见表32.2。禁止在操作期间写入该寄存器。

即使在arctansqrt操作期间，也禁止写入该寄存器。

如果在计算过程中对该寄存器进行读访问，则在计算完成后读取结果。此时，总线访问被迫等待，直到通道过程完成。

有关如何使用该寄存器的信息，请参见表32.2。

32.2.3 SCDT1：正弦余弦数据寄存器1

Base address: TFU = 0x4002_1000

Offset address: 0x14

Bit position: 31 … 0

Bit field: SCDT1[31:0]

重置后的值: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
31:0	SCDT1[31:0]	正弦余弦数据寄存器1（单精度浮点）	R/W

For the sincos operation, the SCDT1 register is shared for the input angle value θ and the output value sinθ of the trigonometric function unit. See Table 32.2 for detail. Writing to this register during operation is prohibited.

Writing to this register is prohibited even during the arctan/sqrt operation.

If read access is made to this register during the calculation, the result is read after the calculation is completed. At this time, the bus access is forced to wait until the channel process is completed.

See Table 32.2 for how to use this register.

Table 32.2 Input/Output value of SCDT0 and SCDT1

Register	Input value	Output value
SCDT0	—	cosθ
SCDT1	Angle θ	sinθ

32.2.4 ATDT0 : Arctangent Data Register 0

Base address: TFU = 0x4002_1000

Offset address: 0x18

Bit position:	31																													0
Bit field:	ATDT0[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	ATDT0[31:0]	Arctangent Data Register 0 (single-precision floating-point)	R/W

For the arctan/sqrt operation, the ATDT0 register is shared for the input coordinates value x and the sqrt(x^2+y^2) output value of the trigonometric function unit. See Table 32.3 for detail. Writing to this register during operation is prohibited.

Writing to this register is prohibited even during the sincos operation.

If read access is made to this register during the calculation, the result is read after the calculation is completed. At this time, the bus access is forced to wait until the channel process is completed.

See Table 32.3 for how to use this register.

32.2.5 ATDT1 : Arctangent Data Register 1

Base address: TFU = 0x4002_1000

Offset address: 0x1C

Bit position:	31																													0
Bit field:	ATDT1[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	ATDT1[31:0]	Arctangent Data Register 1 (single-precision floating-point)	R/W

For the arctan/sqrt operation, the ATDT1 register is shared for the input coordinates value y and the arctan(y/x) output value of the trigonometric function unit. See Table 32.3 for detail. Writing to this register during operation is prohibited.

Writing to this register is prohibited even during the sincos operation.

If read access is made to this register during the calculation, the result is read after the calculation is completed. At this time, the bus access is forced to wait until the channel process is completed.

See Table 32.3 for how to use this register.

对于sincos运算，SCDT1寄存器为三角函数单元的输入角度值θ和输出值sinθ共享。详见表32.2。禁止在操作期间写入该寄存器。

即使在arctansqrt操作期间，也禁止写入该寄存器。

如果在计算过程中对该寄存器进行读访问，则在计算完成后读取结果。此时，总线访问被迫等待，直到通道过程完成。

有关如何使用该寄存器的信息，请参见表32.2。

Table 32.2 输入SCDT0和SCDT1的输出值

Register	输入值	产值
SCDT0	—	cosθ
SCDT1	Angle θ	sinθ

32.2.4 ATDT0：反正切数据寄存器0

Base address: TFU = 0x4002_1000

Offset address: 0x18

Bit position:	31																													0
Bit field:	ATDT0[31:0]																													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	ATDT0[31:0]	反正切数据寄存器0（单精度浮点）	R/W

对于arctansqrt运算，ATDT0寄存器为三角函数单元的输入坐标值x和sqrt(x2+y2)输出值共享。详见表32.3。禁止在操作期间写入该寄存器。

即使在sincos操作期间，也禁止写入该寄存器。

如果在计算过程中对该寄存器进行读访问，则在计算完成后读取结果。此时，总线访问被迫等待，直到通道过程完成。

有关如何使用该寄存器的信息，请参见表32.3。

32.2.5 ATDT1：反正切数据寄存器1

Base address: TFU = 0x4002_1000

Offset address: 0x1C

Bit position:	31																													0
Bit field:	ATDT1[31:0]																													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	ATDT1[31:0]	反正切数据寄存器1（单精度浮点）	R/W

对于arctansqrt运算，ATDT1寄存器为三角函数单元的输入坐标值y和arctan(yx)输出值共享。详见表32.3。禁止在操作期间写入该寄存器。

即使在sincos操作期间，也禁止写入该寄存器。

如果在计算过程中对该寄存器进行读访问，则在计算完成后读取结果。此时，总线访问被迫等待，直到通道过程完成。

有关如何使用该寄存器的信息，请参见表32.3。

Table 32.3 Input/Output value of ATDT0 and ATDT1

Register	Input value	Output value
ATDT0	Input coordinates x	sqrt(x^2+y^2)
ATDT1	Input coordinates y	arctan(y/x)

32.3 Operation

32.3.1 Arithmetic Processing

The trigonometric arithmetic unit has two arithmetic operations, the sincos operation and the arctan/sqrt operation. See Table 32.4 for detail.

Table 32.4 Arithmetic processing

Arithmetic	Input value	Output value
sincos	Angle value θ	cosθ and sinθ
arctan/sqrt	Coordinates x and y	arctan(y/x) and sqrt(x^2+ y^2)

The arithmetic formula for sqrt(x^2+ y^2) is:

$$\mathrm{sqrt}(x^2 + y^2) = \frac{\sqrt{x^2 + y^2}}{k}$$

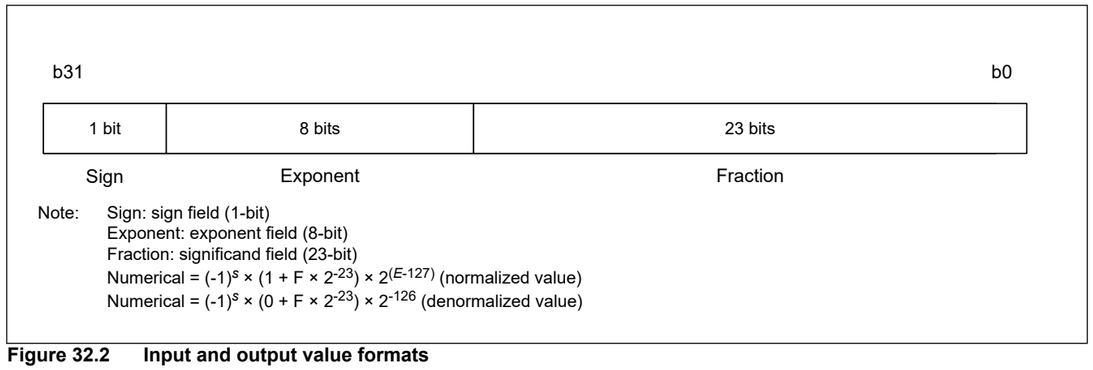
The value of scaling factor k is:

$$k = \prod_{i=0}^{\infty} \frac{1}{\sqrt{1 + 2^{-2i}}} \fallingdotseq 0.607252935008881256 1694$$

32.3.2 Input and Output Value Formats

The input/output values of TFU support only single-precision floating-point as shown in Table 32.5.

- Floating-point
  Support single-precision floating-point specified by the IEEE754 standard.
  - Single-precision floating-point



Note: Sign: sign field (1-bit)
Exponent: exponent field (8-bit)
Fraction: significand field (23-bit)
Numerical = $(-1)^s \times (1 + F \times 2^{-23}) \times 2^{(E-127)}$ (normalized value)
Numerical = $(-1)^s \times (0 + F \times 2^{-23}) \times 2^{-126}$ (denormalized value)

Figure 32.2 Input and output value formats

Table 32.5 Support single-precision floating-point (1 of 2)

S	E	F	Numerical
Any value	0 < E < 255	Any value	$(-1)^s \times 1.F \times 2^{(E-127)}$ (normalized value — Normal Numbers)
Any value	E = 0	F > 0	$(-1)^s \times 0.F \times 2^{-126}$ (denormalized value — Subnormal Numbers)
S = 0	E = 0	F = 0	$(-1)^0 \times 0.0$ (positive zero — +0)

Table 32.3 输入ATDT0和ATDT1的输出值

Register	输入值	产值
ATDT0	输入坐标x	sqrt(x^2+y^2)
ATDT1	输入坐标y	arctan(y/x)

32.3 Operation

32.3.1 算术处理

三角算术单元有两个算术运算，sincos运算和arctansqrt运算。看详细信息见表32.4。

Table 32.4 算术处理

算术输入值		产值
sincos	角度值θ	cosθ和sinθ
arctan/sqrt	坐标x和yarctan(yx)和	sqrt(x2+y2)

sqrt(x2+y2)的算术公式为：

$$\mathrm{sqrt}(x^2 + y^2) = \frac{\sqrt{x^2 + y^2}}{k}$$

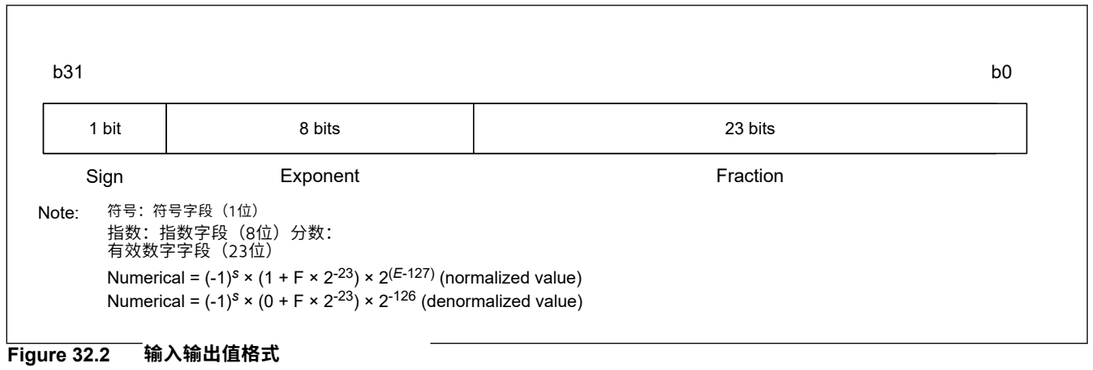
比例因子k的值为：

$$k = \prod_{i=0}^{\infty} \frac{1}{\sqrt{1 + 2^{-2i}}} \fallingdotseq 0.607252935008881256 1694$$

32.3.2 输入和输出值格式

TFU的输入输出值仅支持单精度浮点，如表32.5所示。

- Floating-point
  支持IEEE754标准规定的单精度浮点。
  - Single-precision floating-point



Note: 符号：符号字段（1位）
指数：指数字段（8位）分数：
有效数字字段（23位）
Numerical = $(-1)^s \times (1 + F \times 2^{-23}) \times 2^{(E-127)}$ (normalized value)
Numerical = $(-1)^s \times (0 + F \times 2^{-23}) \times 2^{-126}$ (denormalized value)

Figure 32.2 输入输出值格式

Table 32.5 支持单精度浮点（1of2）

S	E	F	Numerical
任何值	0 < E < 255	任何值	(−1)s×1.F×2(E127)（归一化值−普通数）
任何值	E = 0	F > 0	(−1)s×0.F×2−126（非规格化值−次正规数）
S = 0	E = 0	F = 0	$(-1)^0 \times 0.0$ (positive zero — +0)

Table 32.5 Support single-precision floating-point (2 of 2)

S	E	F	Numerical
S = 1	E = 0	F = 0	$(-1)^{-1}$ × 0.0 (negative zero — -0)
S = 0	E = 255	F = 0	(positive infinity — +∞)
S = 1	E = 255	F = 0	(negative infinity — -∞)
Any value	E = 255	$2^{22} > F > 0$	(non-number — SNaN: Signaling Not a Number)
Any value	E = 255	$F \geq 2^{22}$	(non-number — QNaN: Quiet Not a Number)

32.3.3 Relationship Between Input and Output Values for Sincos Operation

When the input values in the sincos operation are ±0, ±∞, SNaN (Signaling Not a Number), and QNaN (Quiet Not a Number), a fixed value is output as shown in Table 32.6.

Table 32.6 Relationship between special input value and its output value (for sincos operation)

Input (*θ*)	Output (cos)	Output (sin)
-∞	QNaN	QNaN
-0	+1	-0
+0	+1	+0
+∞	QNaN	QNaN
SNaN/QNaN	QNaN	QNaN

Note: The output value of QNaN is 0xffc0_0000.

32.3.4 Relationship Between Input and Output Values for Arctan Operation

When either the input values x or y in the arctan operation are ±0, ±∞, SNaN (Signaling Not a Number), and QNaN (Quiet Not a Number), a fixed value is output as shown in Table 32.7.

If both input values are ±0, it is determined as an input error.

Table 32.7 Relationship between special input value and its output value (for arctan operation)

x / y	-∞	Negative value	-0	+0	Positive value	+∞	SNaN/QNaN
-∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
Negative value	QNaN	—	-π/2	-π/2	—	QNaN	QNaN
-0	QNaN	-π	QNaN*1	QNaN*1	-0	QNaN	QNaN
+0	QNaN	+π	QNaN*1	QNaN*1	+0	QNaN	QNaN
Positive value	QNaN	—	+π/2	+π/2	—	QNaN	QNaN
+∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
SNaN/QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN

Note 1. An input error occurs for the special input value, and the input error flag (TRGSTS.ERRF) is set.

32.3.5 Relationship Between Input and Output Values for sqrt Operation

When either the input values x or y in the sqrt operation are ±0, ±∞, SNaN (Signaling Not a Number), and QNaN (Quiet Not a Number), or when both x and y are ± 0, a fixed value is output as shown in Table 32.8.

If both input values are ±0, it is determined as an input error.

Table 32.5 支持单精度浮点(2of2)

S	E	F	Numerical
S = 1	E = 0	F = 0	$(-1)^{-1}$ × 0.0 (negative zero — -0)
S = 0	E = 255	F = 0	(positive infinity — +∞)
S = 1	E = 255	F = 0	(negative infinity — -∞)
任何值	E = 255	$2^{22} > F > 0$	（非数字——SNaN：发信号通知不是数字）
任何值	E = 255	$F \geq 2^{22}$	（非数字——QNaN：安静的不是数字）

32.3.3 正余弦运算的输入值和输出值之间的关系

当sincos运算中的输入值为±0、±∞、SNaN（SignalingNotaNumber）和QNaN（QuietNota Number），输出一个固定值，如表32.6所示。

Table 32.6 特殊输入值与其输出值的关系（用于sincos运算）

Input (*θ*)	Output (cos)	Output (sin)
-∞	QNaN	QNaN
-0	+1	-0
+0	+1	+0
+∞	QNaN	QNaN
SNaN/QNaN	QNaN	QNaN

Note: QNaN的输出值为0xffc0_0000。

32.3.4 反正切运算的输入值和输出值之间的关系

当arctan运算中的输入值x或y为±0、±∞、SNaN（SignalingNotaNumber）和QNaN（Quiet NotaNumber），则输出固定值，如表32.7所示。

如果两个输入值都是±0，则确定为输入错误。

Table 32.7 特殊输入值与其输出值之间的关系（用于arctan运算）

x / y	-∞	负值	-0	+0	正值	+∞	SNaN/QNaN
-∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
负值	QNaN	—	-π/2	-π/2	—	QNaN	QNaN
-0	QNaN	-π	QNaN*1	QNaN*1	-0	QNaN	QNaN
+0	QNaN	+π	QNaN*1	QNaN*1	+0	QNaN	QNaN
正值	QNaN	—	+π/2	+π/2	—	QNaN	QNaN
+∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
SNaN/QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN

注1.特殊输入值发生输入错误，并设置输入错误标志(TRGSTS.ERRF)。

32.3.5 sqrt操作的输入和输出值之间的关系

当sqrt运算中的输入值x或y为±0、±∞、SNaN（SignalingNotaNumber）和QNaN（Quiet NotaNumber），或者当x和y均为±0时，输出固定值，如表32.8所示。

如果两个输入值都是±0，则确定为输入错误。

Table 32.8 Relationship between special input value and its output value (for sqrt(x^2+y^2) operation)

x / y	-∞	Negative value	-0	+0	Positive value	+∞	SNaN/QNaN
-∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
Negative value	QNaN	—	—	—	—	QNaN	QNaN
-0	QNaN	—	+0*1	+0*1	—	QNaN	QNaN
+0	QNaN	—	+0*1	+0*1	—	QNaN	QNaN
Positive value	QNaN	—	—	—	—	QNaN	QNaN
+∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
SNaN/QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN

Note 1. An input error occurs for the special input value, and the input error flag (TRGSTS.ERRF) is set.

32.3.6 Procedure for Trigonometric Function Operation

Figure 32.3 shows the procedure for sincos operation. There are two procedures. The advantages and disadvantages of each are shown in Table 32.9.

Figure 32.4 shows the procedure for arctan operation. There are two procedures. The advantages and disadvantages of each are shown in Table 32.9.

Table 32.9 Advantages and disadvantages of sincos and arctan operations

Method	Advantages	Disadvantages
Procedure 1	Not occupy the bus	Operation end determination is required by checking TRGSTS.BSY
Procedure 2	Operation end determination is not required by checking TRGSTS.BSY (reduced number of execution cycles)	Waiting for the number of execution cycles is required to read the result of the operation

Table 32.8 特殊输入值与其输出值的关系（对于sqrt(x2+y2)操作）

x / y	-∞	负值	-0	+0	正值	+∞	SNaN/QNaN
-∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
负值	QNaN	—	—	—	—	QNaN	QNaN
-0	QNaN	—	+0*1	+0*1	—	QNaN	QNaN
+0	QNaN	—	+0*1	+0*1	—	QNaN	QNaN
正值	QNaN	—	—	—	—	QNaN	QNaN
+∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
SNaN/QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN

注1.特殊输入值发生输入错误，并设置输入错误标志(TRGSTS.ERRF)。

32.3.6 三角函数运算过程

图32.3显示了sincos操作的过程。有两个程序。每种方法的优缺点如表32.9所示。

图32.4显示了arctan操作的过程。有两个程序。每种方法的优缺点如表32.9所示。

Table 32.9 sincos和arctan运算的优缺点

Method	Advantages	Disadvantages
程序1不占用总线		通过检查需要确定操作结束 TRGSTS.BSY
程序2不需要	通过检查来确定操作结束 TRGSTS.BSY（减少执行周期数）	需要等待执行周期数才能读取操作结果

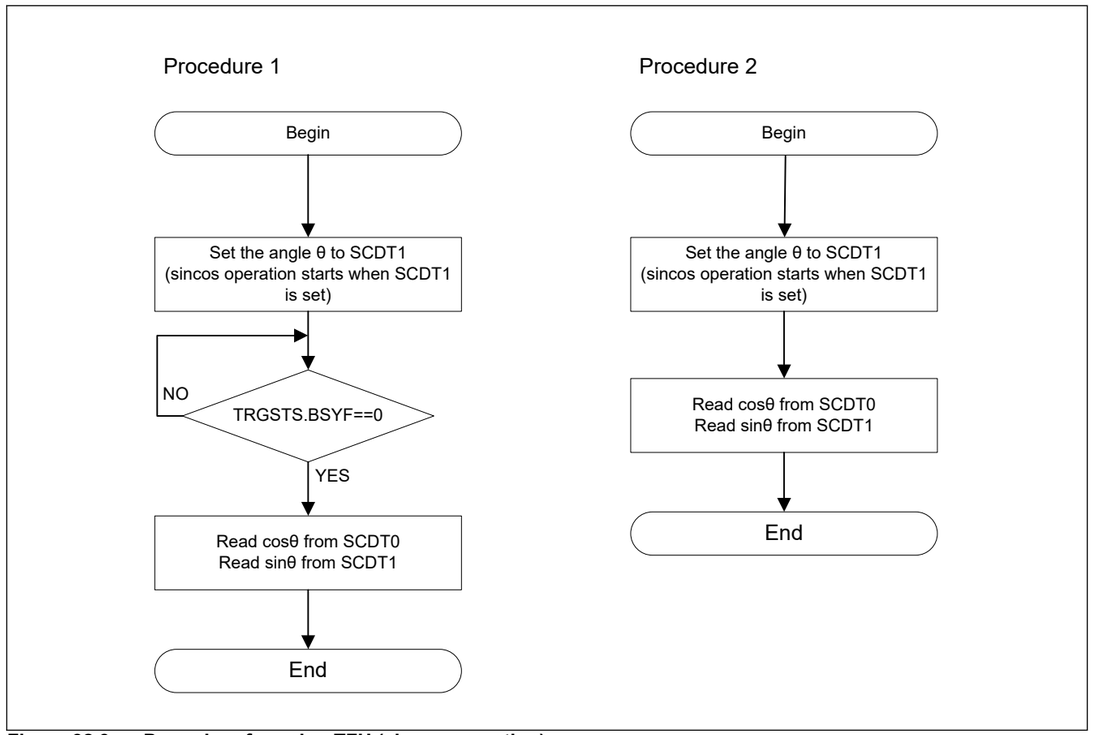


Figure 32.3 Procedure for using TFU (sincos operation)

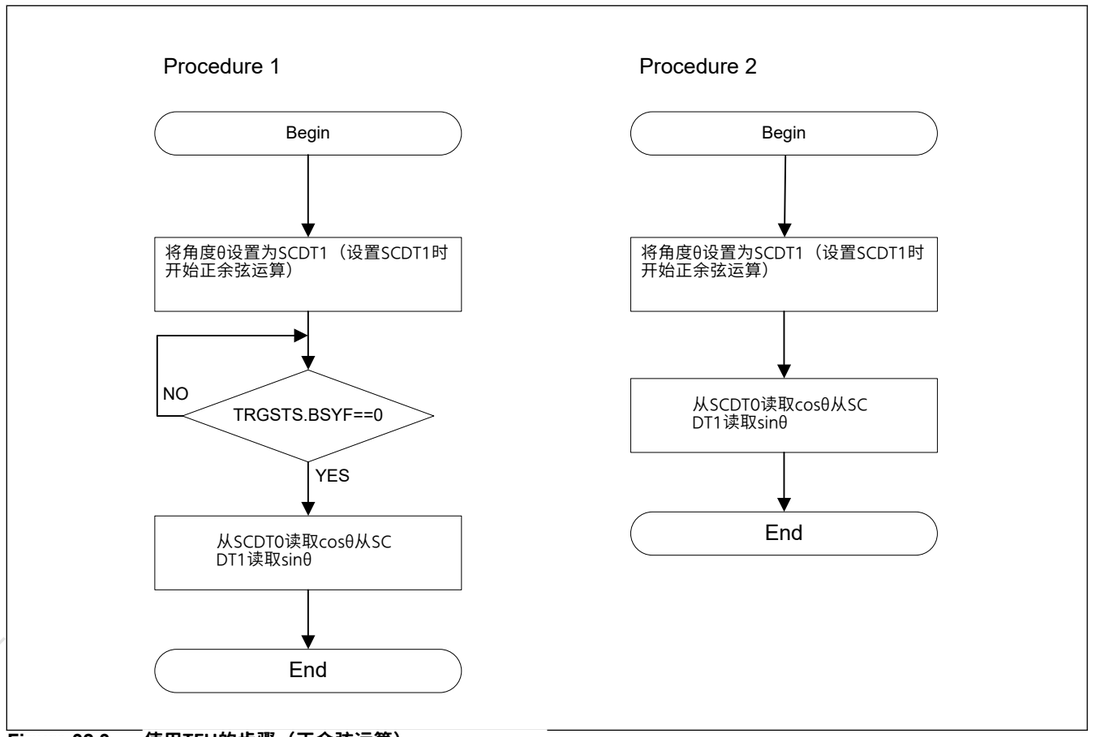


Figure 32.3 使用TFU的步骤（正余弦运算）

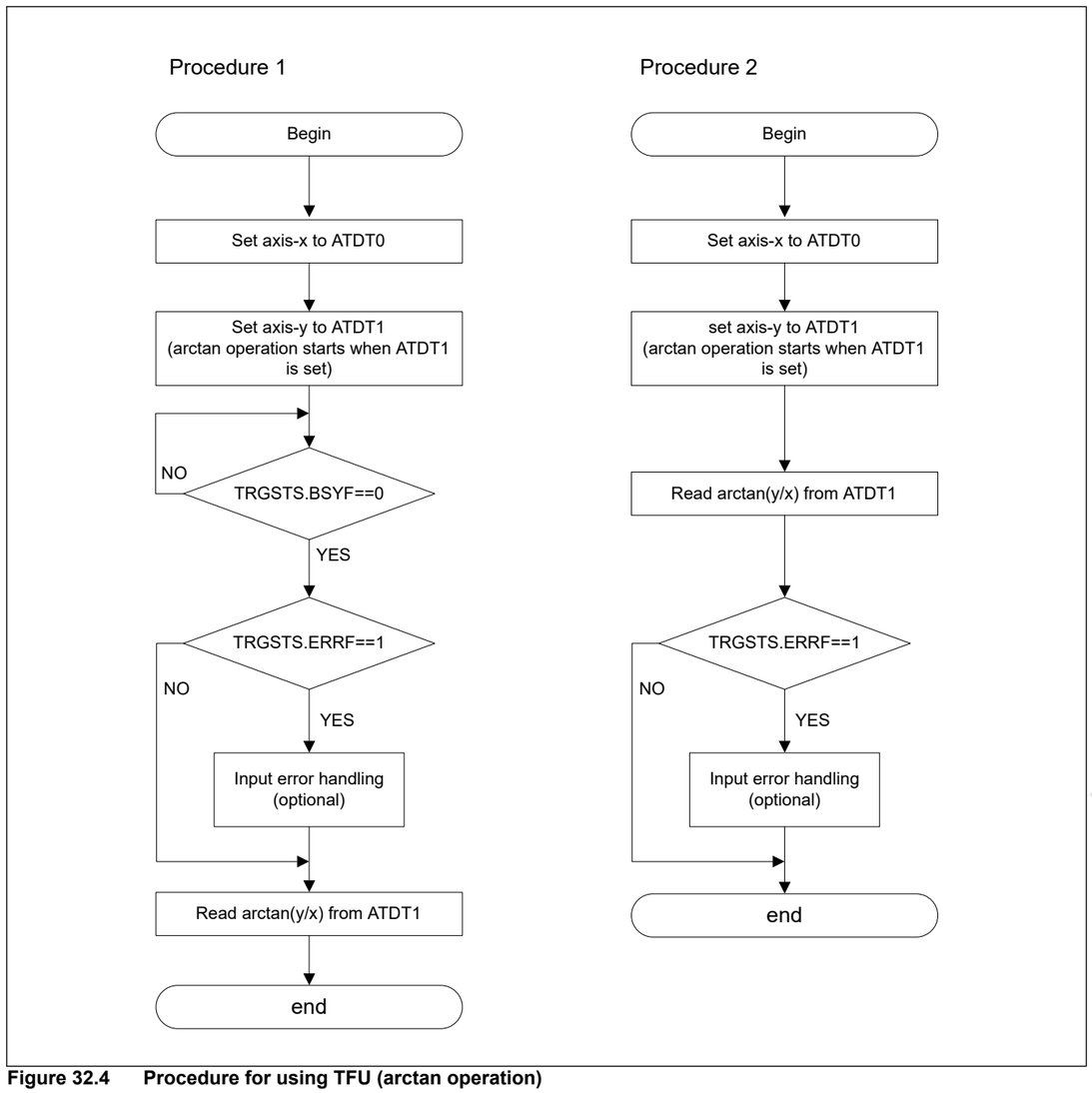


Figure 32.4 Procedure for using TFU (arctan operation)

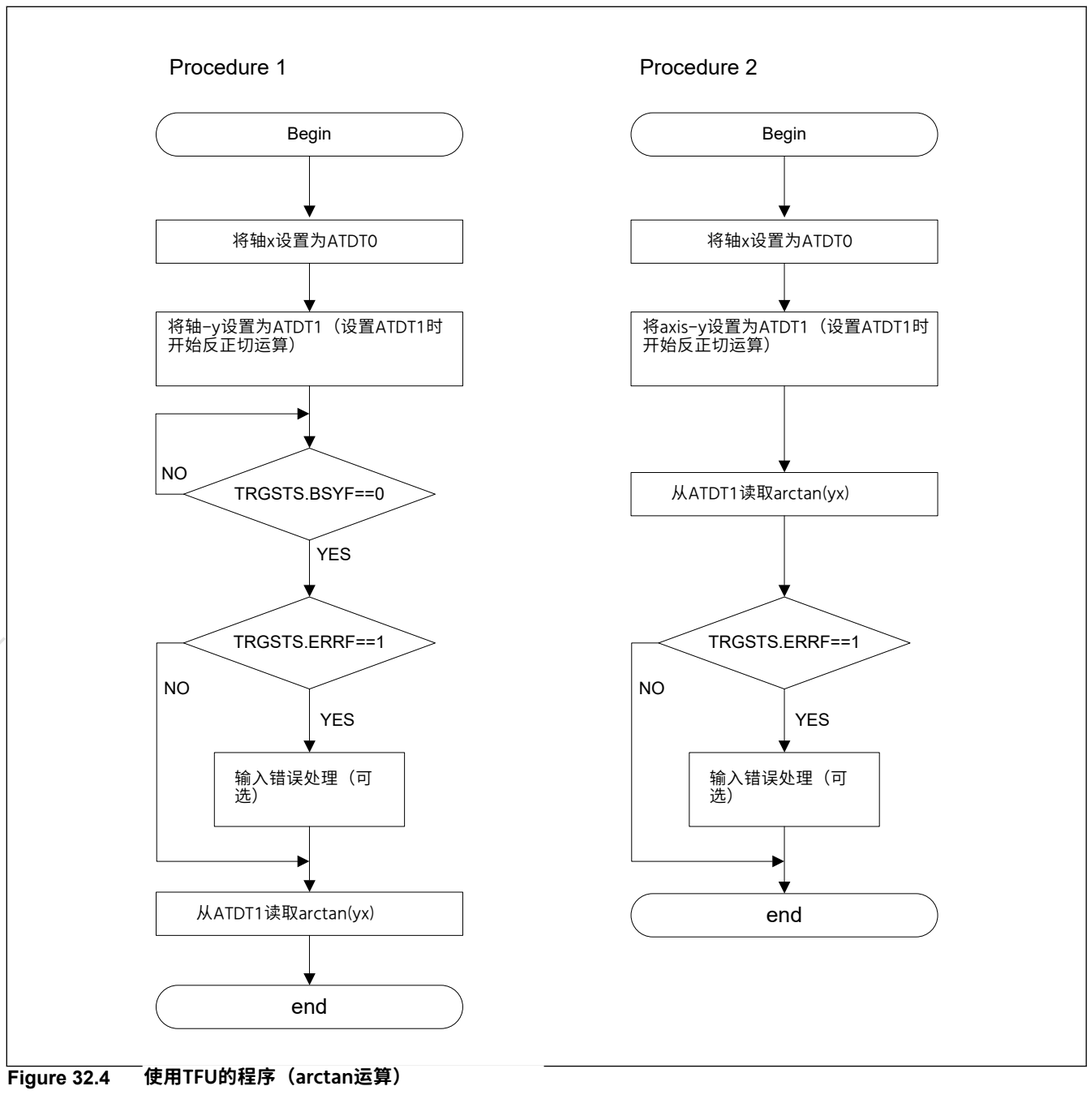


Figure 32.4 使用TFU的程序（arctan运算）

33. IIR Filter Accelerator (IIRFA)

33.1 Overview

This IIR filter accelerator performs cascade connected Direct form II transposed biquad IIR (Infinite Impulse Response) filter operation as shown in Figure 33.1.

One biquad IIR filter operation is called a stage. Cascade connected stages are called channels.

The following settings are available:

- Any number of stages up to 32 stages can be connected.
- The stages to be cascade connected can be selected for each channel.
- The coefficients (a_1, a_2, b_0, b_1, b_2) and delay data (D_0, D_1) can be set for each stage.

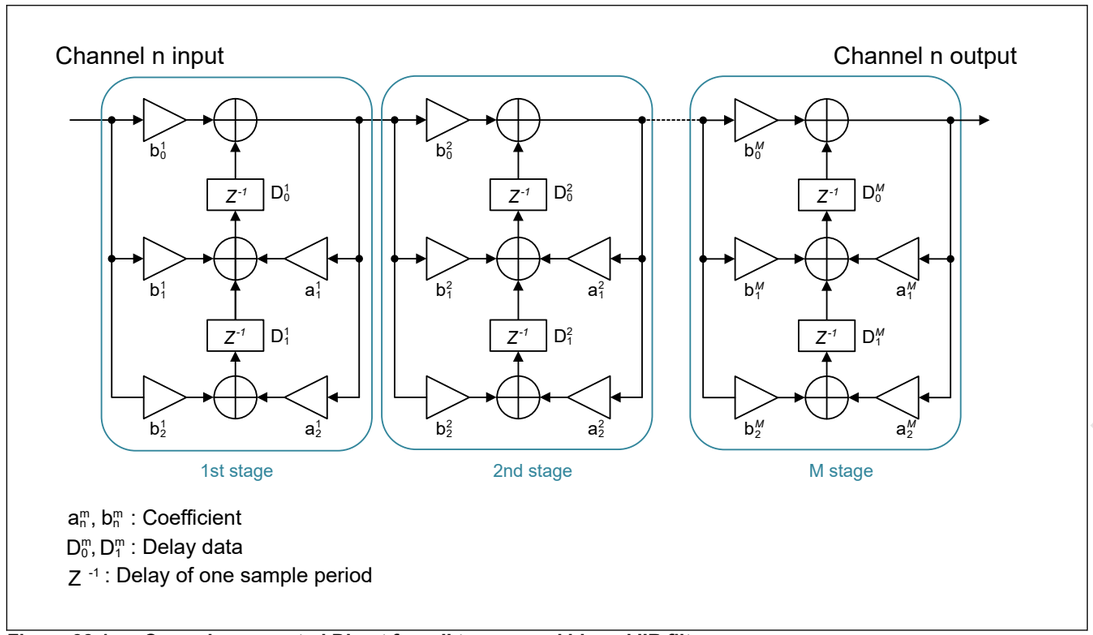


Figure 33.1 Cascade connected Direct form II transposed biquad IIR filter

Table 33.1 shows the specification of the IIR filter accelerator.

Table 33.1 IIR filter accelerator specification (1 of 2)

Parameter	Description
Operation processing	biquad IIR filter
Data type	Single precision floating-point defined in the IEEE754 standard (Negative denormalized numbers are treated as −0, positive denormalized numbers as +0, and NaN (Not a number) as ∞.)
Rounding mode	Round to nearest, round toward zero.
Maximum number of stages	32
Operation circuit	Multiple channels can be processed by time-slicing and one channel can be operated at the same time.
Number of I/O channels	16 channels
Number of cascade connected stages	1 to 32 stages can be connected per channel.
Number of operation cycles	2 cycles per stage until completion of output preparation

33. IIR滤波器加速器(IIRFA)

33.1 Overview

该IIR滤波器加速器执行级联连接的直接形式II转置双二阶IIR（无限脉冲响应）滤波器操作，如图33.1所示。

一个双二阶IIR滤波器操作称为阶段。级联连接的阶段称为通道。

可以使用以下设置：

●最多可连接32个阶段。

●可以为每个通道选择要级联的级。

●可以为每个阶段设置系数（a1，a2，b0，b1，b2）和延迟数据（D0，D1）。

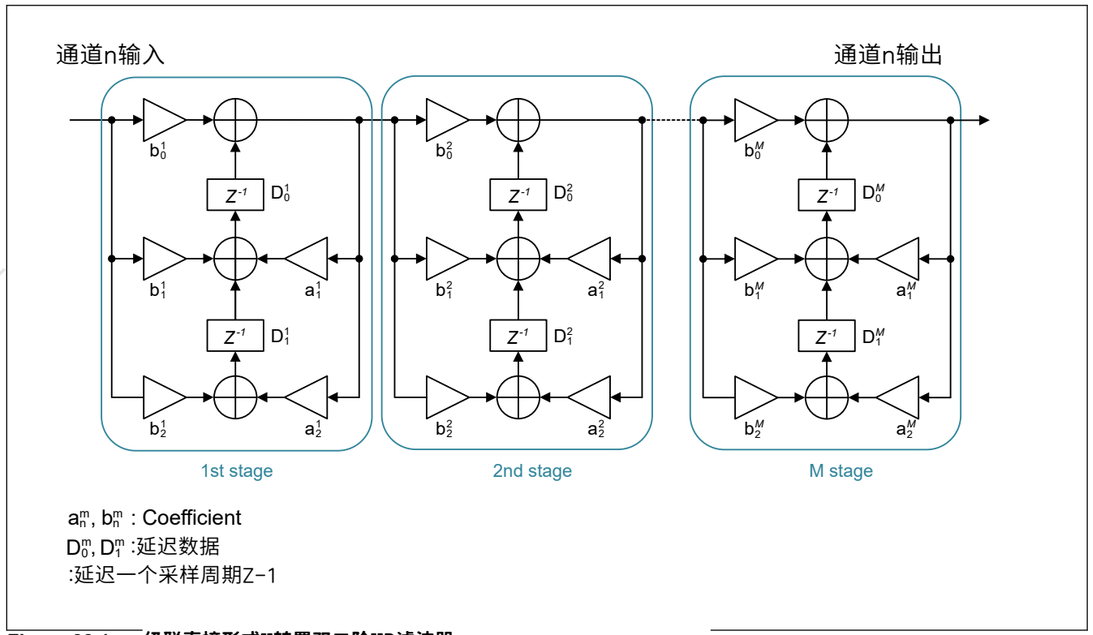


Figure 33.1 级联直接形式II转置双二阶IIR滤波器

表33.1显示了IIR滤波器加速器的规格。

Table 33.1 IIR滤波器加速器规范(1of2)

Parameter	Description
操作处理	biquad IIR filter
数据类型	IEEE754标准中定义的单精度浮点数（负的非规范化数字被视为−0，正的非规范化数字被视为+0，NaN（非数字）被视为∞。）
舍入模式	四舍五入到最近，向零四舍五入。
最大级数	32
运算电路	可分时处理多通道，可同时操作一个通道。
输入输出通道数	16 channels
级联级数	每个通道可连接1至32级。
操作周期数	每阶段2个周期，直到完成输出准备

Table 33.1 IIR filter accelerator specification (2 of 2)

Parameter	Description
Interrupt	• The following interrupt can be generated – Output data preparation completion interrupt – Process completion interrupt – Operation error interrupt • ECC error interrupts can be generated.
Coefficient/delay data storage area	The coefficient and delay data are retained in local RAM and error correction and detection can be performed by ECC. (with 1-bit error correction and 2-bit error detection)

33.2 Register Descriptions

33.2.1 Register List

Table 33.2 lists the I/O registers.

The meaning of the R/W column in the subsequent register descriptions is as follows:

R/W: Indicates that the read and write access operations are possible.
R: Indicates that only the read access operation is possible. The write access operation is ignored.
W: Indicates that the write access operation is possible. Unless otherwise specified, the read value is the value after reset.

Table 33.2 I/O register list (base address: IIRFA = 0x4002_0000) (1 of 2)

Register name	Symbol	Access width	Value after reset	Offset address	R/W
Channel processing status register	IIRCPRCS	32	0x00000000	0x000	R
Channel processing completion flag register	IIRCPRCFF	32	0x00000000	0x004	R
Output data preparation completion flag register	IIRORDYF	32	0x00000000	0x008	R
Operation error flag register	IIRCERRF	32	0x00000000	0x00C	R
Operation control register	IIROPCNT	32	0x00000000	0x010	R/W
ECC control register	IIRECCCNT	32	0x00000000	0x020	R/W
ECC interrupt enable register	IIRECCINT	32	0x00000000	0x028	R/W
ECC error flag register	IIRECCEF	32	0x00000000	0x030	R
ECC error flag clear register	IIRECCEFCLR	32	0x00000000	0x034	W
ECC 1-bit error address register	IIRESEADR	32	0x00000000	0x038	R
ECC 2-bit error address register	IIREDEADR	32	0x00000000	0x03C	R
Channel n input register (n = 0 to 15)	IIRCHnINP	32	Undefined	0x100 + 0x10 × n	W
Channel n output register (n = 0 to 15)	IIRCHnOUT	32	0x00000000	0x104 + 0x10 × n	R
Channel n control register (n = 0 to 15)	IIRCHnCNT	32	0x00000000	0x108 + 0x10 × n	R/W
Channel n interrupt enable register (n = 0 to 15)	IIRCHnINT	8	0x00	0x10C + 0x10 × n	R/W
Channel n status register (n = 0 to 15)	IIRCHnSTS	8	0x00	0x10D + 0x10 × n	R
Channel n flag clear register (n = 0 to 15)	IIRCHnFCLR	8	0x00	0x10E + 0x10 × n	W
Stage m coefficient b0 register (m = 0 to 31)	IIRSTGmB0	32	Undefined	0x400 + 0x20 × m	R/W
Stage m coefficient b1 register (m = 0 to 31)	IIRSTGmB1	32	Undefined	0x404 + 0x20 × m	R/W
Stage m coefficient b2 register (m = 0 to 31)	IIRSTGmB2	32	Undefined	0x408 + 0x20 × m	R/W
Stage m coefficient a1 register (m = 0 to 31)	IIRSTGmA1	32	Undefined	0x40C + 0x20 × m	R/W
Stage m coefficient a2 register (m = 0 to 31)	IIRSTGmA2	32	Undefined	0x410 + 0x20 × m	R/W
Stage m delay data D0 register (m = 0 to 31)	IIRSTGmD0	32	Undefined	0x414 + 0x20 × m	R/W

Table 33.1 IIR滤波器加速器规范(2of2)

Parameter	Description
Interrupt	• 可以产生以下中断 – 输出数据准备完成中断 – 进程完成中断 – 操作错误中断 • 可以产生ECC错误中断。
系数延迟数据存储区	系数和延迟数据保留在本地RAM中，可以通过ECC执行纠错和检测。（具有1位纠错和2位错误检测）

33.2 注册说明

33.2.1 注册列表

表33.2列出了IO寄存器。

后续寄存器说明中RW列的含义如下：

RW：表示可以进行读写访问操作。
R：表示只能进行读访问操作。写访问操作被忽略。
W：表示可以进行写访问操作。除非另有说明，否则读取的值为复位后的值。

Table 33.2 IO寄存器列表（基地址：IIRFA=0x4002_0000）（1of2）

注册名称	Symbol	存取宽度	重置后的值	偏移地址	R/W
通道处理状态寄存器	IIRCPRCS	32	0x00000000	0x000	R
通道处理完成标志寄存器	IIRCPRCFF	32	0x00000000	0x004	R
输出数据准备完成标志寄存器	IIRORDYF	32	0x00000000	0x008	R
操作错误标志寄存器	IIRCERRF	32	0x00000000	0x00C	R
操作控制寄存器	IIROPCNT	32	0x00000000	0x010	R/W
ECC控制寄存器	IIRECCCNT	32	0x00000000	0x020	R/W
ECC中断使能寄存器	IIRECCINT	32	0x00000000	0x028	R/W
ECC错误标志寄存器	IIRECCEF	32	0x00000000	0x030	R
ECC错误标志清除寄存器	IIRECCEFCLR	32	0x00000000	0x034	W
ECC1位错误地址寄存器	IIRESEADR	32	0x00000000	0x038	R
ECC2位错误地址寄存器	IIREDEADR	32	0x00000000	0x03C	R
通道n输入寄存器（n=0到15）	IIRCHnINP	32	Undefined	0x100 + 0x10 × n	W
通道n输出寄存器（n=0到15）	IIRCHnOUT	32	0x00000000	0x104 + 0x10 × n	R
通道n控制寄存器（n=0到15）	IIRCHnCNT	32	0x00000000	0x108 + 0x10 × n	R/W
通道n中断使能寄存器（n=0到15）	IIRCHnINT	8	0x00	0x10C + 0x10 × n	R/W
通道n状态寄存器（n=0到15）	IIRCHnSTS	8	0x00	0x10D + 0x10 × n	R
通道n标志清除寄存器（n=0到15）	IIRCHnFCLR	8	0x00	0x10E + 0x10 × n	W
阶段m系数b0寄存器（m=0到31）	IIRSTGmB0	32	Undefined	0x400 + 0x20 × m	R/W
阶段m系数b1寄存器（m=0到31）	IIRSTGmB1	32	Undefined	0x404 + 0x20 × m	R/W
阶段m系数b2寄存器（m=0到31）	IIRSTGmB2	32	Undefined	0x408 + 0x20 × m	R/W
阶段m系数a1寄存器（m=0到31）	IIRSTGmA1	32	Undefined	0x40C + 0x20 × m	R/W
阶段m系数a2寄存器（m=0到31）	IIRSTGmA2	32	Undefined	0x410 + 0x20 × m	R/W
阶段m延迟数据D0寄存器（m=0到31）	IIRSTGmD0	32	Undefined	0x414 + 0x20 × m	R/W

Table 33.2 I/O register list (base address: IIRFA = 0x4002_0000) (2 of 2)

Register name	Symbol	Access width	Value after reset	Offset address	R/W
Stage m delay data D1 register (m = 0 to 31)	IIRSTGmD1	32	Undefined	0x418 + 0x20 × m	R/W

Note: The register cannot be accessed with an access width other than that described.

33.2.1.1 IIRCPRCS : Channel Processing Status Register

Base address: IIRFA = 0x4002_0000

Offset address: 0x000

Bit position:	31																15															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPRCS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CPRCS[15:0]	Channel processing status bit Bit 0 corresponds to channel 0, bit 1 to channel 1, …, and bit 15 to channel 15. 0: The channel processing of the corresponding channel is not being performed. 1: The channel processing of the corresponding channel is being performed.	R
31:16	—	These bits are read as 0.	R

When the CPRCS[n] bit is read, IIRCHnSTS.CPRCS flag value is read (n = 0 to 15).

33.2.1.2 IIRCPRCFF : Channel Processing Completion Flag Register

Base address: IIRFA = 0x4002_0000

Offset address: 0x004

Bit position:	31																15															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPRCFF[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CPRCFF[15:0]	Channel processing completion flag Bit 0 corresponds to channel 0, bit 1 to channel 1, …, and bit 15 to channel 15. 0: The channel processing of the corresponding channel is not completed. 1: The channel processing of the corresponding channel is completed.	R
31:16	—	These bits are read as 0.	R

When the CPRCFF[n] bit is read, IIRCHnSTS.CPRCFF flag value is read (n = 0 to 15).

33.2.1.3 IIRORDYF : Output Data Preparation Completion Flag Register

Base address: IIRFA = 0x4002_0000

Offset address: 0x008

Bit position:	31																15															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ORDYF[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 33.2 IO寄存器列表（基址：IIRFA=0x4002_0000）（2of2）

注册名称	Symbol	存取宽度	重置后的值	偏移地址	R/W
阶段m延迟数据D1寄存器（m=0到31）	IIRSTGmD1	32	Undefined	0x418 + 0x20 × m	R/W

Note: 不能以上述以外的访问宽度访问该寄存器。

33.2.1.1 IIRCPRCS：通道处理状态寄存器

Base address: IIRFA = 0x4002_0000

Offset address: 0x000

Bit position:	31																15															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPRCS[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CPRCS[15:0]	通道处理状态位 位0对应通道0，位1对应通道1，……，位15对应通道15。 0：不进行对应通道的通道处理。1：正在执行相应通道的通道处理。	R
31:16	—	这些位读为0。	R

当读取CPRCS[n]位时，读取IIRCHnSTS.CPRCS标志值（n=0到15）。

33.2.1.2 IIRCPRCFF:通道处理完成标志寄存器

Base address: IIRFA = 0x4002_0000

Offset address: 0x004

Bit position:	31																15															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPRCFF[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CPRCFF[15:0]	通道处理完成标志 位0对应通道0，位1对应通道1，……，位15对应通道15。 0：对应通道的通道处理未完成。1：对应通道的通道处理完成。	R
31:16	—	这些位读为0。	R

当读取CPRCFF[n]位时，读取IIRCHnSTS.CPRCFF标志值（n=0到15）。

33.2.1.3 IIRORDYF:输出数据准备完成标志寄存器

Base address: IIRFA = 0x4002_0000

Offset address: 0x008

Bit position:	31																15															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ORDYF[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ORDYF[15:0]	Output data preparation completion flag Bit 0 corresponds to channel 0, bit 1 to channel 1, …, and bit 15 to channel 15. 0: The output data preparation of the corresponding channel is not completed. 1: The output data preparation of the corresponding channel is completed.	R
31:16	—	These bits are read as 0.	R

When the ORDYF[n] bit is read, IIRCHnSTS.ORDYF flag value is read (n = 0 to 15).

33.2.1.4 IIRCERRF : Operation Error Flag Register

Base address: IIRFA = 0x4002_0000

Offset address: 0x00C

Bit position:	31															15															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CERRF[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CERRF[15:0]	Operation error flag Bit 0 corresponds to channel 0, bit 1 to channel 1, …, and bit 15 to channel 15. 0: No operation error has occurred in the corresponding channel. 1: An operation error has occurred in the corresponding channel.	R
31:16	—	These bits are read as 0.	R

When the CERRF[n] bit is read, IIRCHnSTS.CERRF flag value is read (n = 0 to 15).

33.2.1.5 IIROPCNT : Operation Control Register

Base address: IIRFA = 0x4002_0000

Offset address: 0x010

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	RND[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	RND[2:0]	Setting for the rounding mode for addition and multiplication 0 0 0: Round to nearest 0 0 1: Round toward zero Others: Setting prohibited.	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

The IIROPCNT register switches the rounding mode for addition and multiplication results during channel processing.

Set this register before starting the channel processing. When this register is rewritten during channel processing, the change does not affect the channel processing that is being executed. The change affects from the next channel processing.

Bit	Symbol	Function	R/W
15:0	ORDYF[15:0]	输出数据准备完成标志 位0对应通道0，位1对应通道1，……，位15对应通道15。 0：对应通道的输出数据准备未完成。1：对应通道的输出数据准备完成。	R
31:16	—	这些位读为0。	R

当读取ORDYF[n]位时，读取IIRCHnSTS.ORDYF标志值（n=0到15）。

33.2.1.4 IIRCERRF:操作错误标志寄存器

Base address: IIRFA = 0x4002_0000

Offset address: 0x00C

Bit position:	31															15															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CERRF[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CERRF[15:0]	操作错误标志 位0对应通道0，位1对应通道1，……，位15对应通道15。 0：对应通道未发生操作错误。1：对应通道发生操作错误。	R
31:16	—	这些位读为0。	R

当读取CERRF[n]位时，读取IIRCHnSTS.CERRF标志值（n=0到15）。

33.2.1.5 IIROPCNT:操作控制寄存器

Base address: IIRFA = 0x4002_0000

Offset address: 0x010

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	RND[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	RND[2:0]	设置加法和乘法的舍入模式 000：四舍五入到最接近的001：四舍五入到零 其他：禁止设置。	R/W
31:3	—	这些位被读取为0。写入值应为0。	R/W

IIROPCNT寄存器在通道处理期间切换加法和乘法结果的舍入模式。

在开始通道处理之前设置该寄存器。在通道处理期间重写该寄存器时，更改不会影响正在执行的通道处理。该更改影响下一个通道处理。

33.2.1.6 IIRECCCNT : ECC Control Register

Base address: IIRFA = 0x4002_0000

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ECCWBDIS	ECCMD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECCMD	ECC setting bit 0: The ECC error detection/correction function is disabled. 1: The ECC error detection/correction function is enabled.	R/W
1	ECCWBDIS	ECC-corrected data write-back disable bit 0: The error-corrected data write-back is enabled. 1: The error-corrected data write-back is disabled.	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

This register sets the ECC error detection/correction function.

Set this register before starting the channel processing. If the value is changed during the channel processing, operation is not guaranteed.

ECCMD bit (ECC setting bit)

The ECCMD bit enables or disables the error detection/correction function.

If the ECC error detection/correction function is enabled, the ECC code is updated when data is written to the coefficient/delay data storage area.

If the ECC error detection/correction function is disabled, the ECC code is not updated when data is written to the coefficient/delay data storage area.

ECCWBDIS bit (ECC-corrected data write-back disable bit)

The ECCWBDIS bit controls the ECC 1-bit error-corrected data write-back when the ECC error detection/correction function is enabled.

33.2.1.7 IIRECCINT : ECC Interrupt Enable Register

Base address: IIRFA = 0x4002_0000

Offset address: 0x028

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EDEIE	ESEIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

33.2.1.6 IIRECCCNT:ECC控制寄存器

Base address: IIRFA = 0x4002_0000

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ECCWBDIS	ECCMD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECCMD	ECC设置位 0：ECC检错校正功能关闭。1：ECC检错校正功能使能。	R/W
1	ECCWBDIS	ECC校正数据回写禁用位 0：启用纠错数据回写。1：禁止纠错数据回写。	R/W
31:2	—	这些位被读取为0。写入值应为0。	R/W

该寄存器设置ECC错误检测校正功能。

在开始通道处理之前设置该寄存器。如果在通道处理过程中更改该值，则无法保证操作。

ECCMD位（ECC设置位）

ECCMD位启用或禁用错误检测校正功能。

如果启用ECC错误检测校正功能，则在将数据写入系数延迟数据存储区时更新ECC代码。

如果禁用ECC错误检测校正功能，则在将数据写入系数延迟数据存储区时不会更新ECC代码。

ECCWBDIS位（ECC校正数据回写禁用位）

ECCWBDIS位控制ECC纠错功能启用时ECC1位纠错数据的回写。

33.2.1.7 IIRECCINT:ECC中断使能寄存器

Base address: IIRFA = 0x4002_0000

Offset address: 0x028

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EDEIE	ESEIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESEIE	ECC 1-bit error interrupt enable bit 0: The generation of ECC 1-bit error interrupt requests is disabled. 1: The generation of ECC 1-bit error interrupt requests is enabled.	R/W
1	EDEIE	ECC 2-bit error interrupt enable bit 0: The generation of ECC 2-bit error interrupt requests is disabled. 1: The generation of ECC 2-bit error interrupt requests is enabled.	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

ESEIE bit (ECC 1-bit error interrupt enable bit)

The ESEIE bit enables or disables the ECC 1-bit error interrupt requests (IIRFA_ERR) when the IIRECCEF.ESEF flag is 1.

EDEIE bit (ECC 2-bit error interrupt enable bit)

The EDEIE bit enables or disables the ECC 2-bit error interrupt requests (IIRFA_ERR) when the IIRECCEF.EDEF flag is 1.

33.2.1.8 IIRECCEF : ECC Error Flag Register

Base address: IIRFA = 0x4002_0000

Offset address: 0x030

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EDEF	ESEF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESEF	ECC 1-bit error flag 0: No 1-bit ECC error is detected. 1: 1-bit ECC error is detected.	R
1	EDEF	ECC 2-bit error flag 0: No 2-bit ECC error is detected. 1: 2-bit ECC error is detected.	R
31:2	—	These bits are read as 0.	R

ESEF bit (ECC 1-bit error flag)

[Setting condition]

- 1-bit ECC error is detected.

[Clearing condition]

- When 1 is written to the IIRECCEFCLR.ESEFCLR bit.

Note: When the setting condition and clearing condition occur at the same time, the clearing condition takes precedence.

EDEF bit (ECC 2-bit error flag)

[Setting condition]

- 2-bit ECC error is detected.

[Clearing condition]

- When 1 is written to the IIRECCEFCLR.EDEFCLR bit.

Bit	Symbol	Function	R/W
0	ESEIE	ECC1位错误中断使能位 0：禁止产生ECC1位错误中断请求。1：使能产生ECC1位错误中断请求。	R/W
1	EDEIE	ECC2位错误中断使能位 0：禁止产生ECC2位错误中断请求。1：使能产生ECC2位错误中断请求。	R/W
31:2	—	这些位被读取为0。写入值应为0。	R/W

ESEIE位（ECC1位错误中断使能位）

当IIRECCEF.ESEF标志为1时，ESEIE位启用或禁用ECC1位错误中断请求(IIRFA_ERR)。

EDEIE位（ECC2位错误中断使能位）

当IIRECCEF.EDEF标志为1时，EDEIE位启用或禁用ECC2位错误中断请求(IIRFA_ERR)。

33.2.1.8 IIRECCEF:ECC错误标志寄存器

Base address: IIRFA = 0x4002_0000

Offset address: 0x030

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EDEF	ESEF
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESEF	ECC1位错误标志 0：未检测到1位ECC错误。1：检测到1位ECC错误。	R
1	EDEF	ECC2位错误标志 0：未检测到2位ECC错误。1：检测到2位ECC错误。	R
31:2	—	这些位读为0。	R

ESEF位（ECC1位错误标志）

[Setting condition]

●检测到1位ECC错误。

[Clearing condition]

●当向IIRECCEFCLR.ESEFCLR位写入1时。

Note: 当设置条件和清零条件同时出现时，清零条件优先。

EDEF位（ECC2位错误标志）

[Setting condition]

●检测到2位ECC错误。

[Clearing condition]

●当向IIRECCEFCLR.EDEFCLR位写入1时。

Note: When the setting condition and clearing condition occur at the same time, the clearing condition takes precedence.

33.2.1.9 IIRECCEFCLR : ECC Error Flag Clear Register

Base address: IIRFA = 0x4002_0000

Offset address: 0x034

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EDEFCLR	ESEFCLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESEFCLR	ECC 1-bit error flag clear bit 0: No effect 1: Clears the ESEF flag of the IIRECCEF register.	W
1	EDEFCLR	ECC 2-bit error status flag clear bit 0: No effect 1: Clears the EDEF flag of the IIRECCEF register.	W
31:2	—	The write value should be 0.	W

The IIRECCEFCLR register clears the ESEF and EDEF flags of the IIRECCEF register.

33.2.1.10 IIRESEADR : ECC 1-bit Error Address Register

Base address: IIRFA = 0x4002_0000

Offset address: 0x038

Bit position:	31	10	0
Bit field:	—	SEADR[10:0]	
Value after reset:	0	0	0

Bit	Symbol	Function	R/W
10:0	SEADR[10:0]	Error address Retains a part of the address of the coefficient/delay data that has detected an ECC 1-bit error. The address to be retained is from bit 10 to bit 2. The lower 2 bits are always 0.	R
31:11	—	These bits are read as 0.	R

A part of the address of the coefficient/delay data that has detected an ECC 1-bit error is retained. When an ECC 1-bit error is detected in a state where the IIRECCEF.ESEF flag is 0, the SEADR[10:0] bits are updated. When the IIRECCEF.ESEF flag is 1, the SEADR[10:0] bits are not updated.

When the base address (IIRFA) is added to the value of this register, the address of the I/O register corresponding to the coefficient/delay data that has detected an ECC 1-bit error is obtained.

Note: 当设置条件和清零条件同时出现时，清零条件优先。

33.2.1.9 IIRECCEFCLR:ECC错误标志清除寄存器

Base address: IIRFA = 0x4002_0000

Offset address: 0x034

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EDEFCLR	ESEFCLR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESEFCLR	ECC1位错误标志清除位 0：无效1：清除IIRECCEF寄存器的ESEF标志。	W
1	EDEFCLR	ECC2位错误状态标志清除位 0：无效1：清除IIRECCEF寄存器的EDEF标志。	W
31:2	—	写入值应为0。	W

IIRECCEFCLR寄存器清除IIRECCEF寄存器的ESEF和EDEF标志。

33.2.1.10 IIRESEADR:ECC1位错误地址寄存器

Base address: IIRFA = 0x4002_0000

Offset address: 0x038

Bit position:	31	10	0
Bit field:	—	SEADR[10:0]	
重置后的值:	0	0	0

Bit	Symbol	Function	R/W
10:0	SEADR[10:0]	错误地址 保留已检测到ECC1位错误的系数延迟数据的部分地址。要保留的地址是从第10位到第2位。低2位始终为0。	R
31:11	—	这些位读为0。	R

保留检测到ECC1位错误的系数延迟数据的部分地址。当在IIRECCEF.ESEF标志为0的状态下检测到ECC1位错误时，更新SEADR[10:0]位。当IIRECCEF.ESEF标志为1时，SEADR[10:0]位不更新。

当基地址（IIRFA）被加到这个寄存器的值上时，得到与检测到ECC1位错误的系数延迟数据对应的IO寄存器的地址。

33.2.1.11 IIREDEADR : ECC 2-bit Error Address Register

Base address: IIRFA = 0x4002_0000

Offset address: 0x03C

Bit position:	31																				10										0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DEADR[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	DEADR[10:0]	Error address Retains a part of the address of the coefficient/delay data that has detected an ECC 2-bit error. The address to be retained is from bit 10 to bit 2. The lower 2 bits are always 0.	R
31:11	—	These bits are read as 0.	R

A part of the address of the coefficient/delay data that has detected an ECC 2-bit error is retained. When an ECC 2-bit error is detected in a state where the IIRECCEF.EDEF flag is 0, the DEADR[10:0] bits are updated. When the IIRECCEF.EDEF flag is 1, the DEADR[10:0] bits are not updated.

When the base address (IIRFA) is added to the value of this register, the address of the I/O register corresponding to the coefficient/delay data that has detected an ECC 2-bit error is obtained.

33.2.1.12 IIRCHnINP : Channel n Input Register (n = 0 to 15)

Base address: IIRFA = 0x4002_0000

Offset address: 0x100 + 0x10 × n

Bit position:	31																														0
Bit field:																															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	n/a	Input data (single precision floating-point) setting of channel n The channel processing of channel n is started.	W

Set the input data to this register. When a value is written to this register, the channel processing of channel n is started.

The read value is undefined when a read access to this register is performed.

If a write access to this register is performed during the channel processing of any channel, bus access is forced to wait until the channel processing is completed. A value is written to this register after the channel processing is complete.

33.2.1.13 IIRCHnOUT : Channel n Output Register (n = 0 to 15)

Base address: IIRFA = 0x4002_0000

Offset address: 0x104 + 0x10 × n

Bit position:	31																														0
Bit field:																															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Output data (single precision floating-point) of channel n	R

33.2.1.11 IIREDEADR:ECC2位错误地址寄存器

Base address: IIRFA = 0x4002_0000

Offset address: 0x03C

Bit position:	31																				10										0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DEADR[10:0]										
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	DEADR[10:0]	错误地址 保留检测到ECC2位错误的系数延迟数据的部分地址。要保留的地址是从第10位到第2位。 低2位始终为0。	R
31:11	—	这些位读为0。	R

保留检测到ECC2位错误的系数延迟数据的部分地址。当在IIRECCEF.EDEF标志为0的状态下检测到ECC2位错误时，更新DEADR[10:0]位。当IIRECCEF.EDEF标志为1时，不更新DEADR[10:0]位。

当基地址（IIRFA）被加到这个寄存器的值上时，得到与检测到ECC2位错误的系数延迟数据对应的IO寄存器的地址。

33.2.1.12 IIRCHnINP：通道n输入寄存器（n=0到15）

Base address: IIRFA = 0x4002_0000

Offset address: 0x100 + 0x10 × n

Bit position:	31																														0
Bit field:																															
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	n/a	通道n的输入数据（单精度浮点）设置 开始通道n的通道处理。	W

将输入数据设置到该寄存器。当一个值被写入该寄存器时，通道n的通道处理开始。

执行对该寄存器的读访问时，读取的值未定义。

如果在任何通道的通道处理期间对该寄存器进行写访问，则总线访问将被强制等待，直到通道处理完成。通道处理完成后会向该寄存器写入一个值。

33.2.1.13 IIRCHnOUT：通道n输出寄存器（n=0到15）

Base address: IIRFA = 0x4002_0000

Offset address: 0x104 + 0x10 × n

Bit position:	31																														0
Bit field:																															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	通道n的输出数据（单精度浮点）	R

This register reads the output data of channel n.

If a read access is performed to this register before the output data preparation of channel n is completed, bus access is forced to wait until the output data preparation is completed. The value is read after the output data preparation is complete.

33.2.1.14 IIRCHnCNT : Channel n Control Register (n = 0 to 15)

Base address: IIRFA = 0x4002_0000

Offset address: 0x108 + 0x10 × n

Bit position:	31																													0
Bit field:	STGSEL[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	STGSEL[31:0]	Stage selection bit The stage to be used for channel n is selected. Bit 0 corresponds to stage 0, bit 1 to stage 1, ..., and bit 31 to stage 31. 0: The corresponding stage is not used for channel n. 1: The corresponding stage is used for channel n.	R/W

This register selects the stage to use for channel n.

Set the stage to be used using this register before starting the channel processing. Operation is not guaranteed when the channel processing of channel n is started with the setting that does not use any stage, that is, the value of this register is 0.

When multiple stages are selected, the cascade connected biquad IIR filter operation is performed for the selected stages. In this case, the operation of the stages is performed in ascending order of stage number.

Note:
- Writing 1 to the bit corresponding to the stage used for another channel is ignored. The stage with the same number cannot be used between different channels.
- Whether 1 is written to the bit corresponding to the stage used for another channel can be determined by reading the IIRCHnCNT immediately after writing to the IIRCHnCNT and checking whether the written value matches with the read value. When not matched, this means that 1 is written to the bit corresponding to the stage used for another channel.
- Do not rewrite the corresponding IIRCHnCNT register during the channel processing of channel n. Operation is not guaranteed if the bit is rewritten.

33.2.1.15 IIRCHnINT : Channel n Interrupt Enable Register (n = 0 to 15)

Base address: IIRFA = 0x4002_0000

Offset address: 0x10C + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CERRIE	ORDYIE	CPRCFIE	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	CPRCFIE	Channel processing completion interrupt enable bit 0: The generation of channel processing completion interrupt requests is disabled. 1: The generation of channel processing completion interrupt requests is enabled.	R/W
2	ORDYIE	Output data preparation completion interrupt enable bit 0: The generation of output data preparation completion interrupt requests is disabled. 1: The generation of output data preparation completion interrupt requests is enabled.	R/W

该寄存器读取通道n的输出数据。

如果在通道n的输出数据准备完成之前对该寄存器执行读访问，则总线访问将被强制等待，直到输出数据准备完成。输出数据准备完成后读取该值。

33.2.1.14 IIRCHnCNT：通道n控制寄存器（n=0到15）

Base address: IIRFA = 0x4002_0000

Offset address: 0x108 + 0x10 × n

Bit position:	31																													0
Bit field:	STGSEL[31:0]																													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	STGSEL[31:0]	阶段选择位 选择用于通道n的阶段。位0对应于阶段0，位1对应于阶段1，……，位31对应于阶段31。 0：对应级不用于通道n。1：对应级用于通道n。	R/W

该寄存器选择用于通道n的阶段。

在开始通道处理之前使用该寄存器设置要使用的阶段。当通道n的通道处理以不使用任何阶段的设置启动时，不保证操作，即该寄存器的值为0。

选择多个阶段时，将对所选阶段进行级联连接的BiquadIIR滤波器操作。在这种情况下，阶段的操作按阶段编号的升序执行。

Note:
- ●将1写入对应于用于另一个通道的阶段的位将被忽略。不同通道之间不能使用相同编号的阶段。
- ●是否将1写入对应于用于另一个通道的阶段的位可通过以下方式确定
  写入IIRCHnCNT后立即读取IIRCHnCNT，并检查写入的值是否与读取的值匹配。当不匹配时，这意味着将1写入与用于另一个通道的阶段相对应的位。
- 在通道n的通道处理过程中，不要重写相应的IIRCHnCNT寄存器。如果该位被重写，则无法保证操作。

33.2.1.15 IIRCHnINT：通道n中断使能寄存器（n=0到15）

Base address: IIRFA = 0x4002_0000

Offset address: 0x10C + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CERRIE	ORDYIE	CPRCFIE	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	该位读取为0。写入值应为0。	R/W
1	CPRCFIE	通道处理完成中断使能位 0：禁止生成通道处理完成中断请求。1：使能通道处理完成中断请求的产生。	R/W
2	ORDYIE	输出数据准备完成中断使能位 0：禁止产生输出数据准备完成中断请求。 1：允许产生输出数据准备完成中断请求。	R/W

Bit	Symbol	Function	R/W
3	CERRIE	Operation error interrupt enable bit 0: The generation of operation error interrupt requests is disabled. 1: The generation of operation error interrupt requests is enabled.	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

CPRCFIE bit (Channel processing completion interrupt enable bit)

The CPRCFIE bit enables or disables the channel processing completion interrupt requests of channel n when the IRCHnSTS.CPRCFF flag is 1.

ORDYIE bit (Output data preparation completion interrupt enable bit)

The ORDYIE bit enables or disables the output data preparation completion interrupt requests of channel n when the IIRCHnSTS.ORDYF flag is 1.

CERRIE bit (Operation error interrupt enable bit)

The CERRIE bit enables or disables the operation error interrupt requests of channel n when the IIRCHnSTS.CERRF flag is 1.

33.2.1.16 IIRCHnSTS : Channel n Status Register (n = 0 to 15)

Base address: IIRFA = 0x4002_0000

Offset address: 0x10D + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CERRF	ORDYF	CPRCFF	CPRCS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CPRCS	Channel processing status flag 0: The channel processing is not being performed. 1: The channel processing is being performed.	R
1	CPRCFF	Channel processing completion flag 0: The channel processing is not completed. 1: The channel processing is completed.	R
2	ORDYF	Output data preparation completion flag 0: The output data preparation is not completed. 1: The output data preparation is completed.	R
3	CERRF	Operation error flag 0: No operation error has occurred. 1: An operation error has occurred.	R
7:4	—	These bits are read as 0.	R

CPRCS bit (Channel processing status flag)

[Setting condition]

- The channel processing of channel n is started.

[Clearing condition]

- The channel processing of channel n is completed.

Note: When the setting condition and clearing condition occur at the same time, the setting condition takes precedence.

CPRCFF bit (Channel processing completion flag)

[Setting condition]

- The channel processing of channel n is completed.

Bit	Symbol	Function	R/W
3	CERRIE	操作错误中断使能位 0：禁止产生操作错误中断请求。1：允许产生操作错误中断请求。	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

CPRCFIE位（通道处理完成中断使能位）

CPRCFIE位启用或禁用通道n的通道处理完成中断请求，当IRCHnSTS.CPRCFF标志为1。

ORDYIE位（输出数据准备完成中断使能位）

ORDYIE位允许或禁止通道n的输出数据准备完成中断请求，当IIRCHnSTS.ORDYF标志为1。

CERRIE位（操作错误中断使能位）

当IIRCHnSTS.CERRF标志为1时，CERRIE位启用或禁用通道n的操作错误中断请求。

33.2.1.16 IIRCHnSTS：通道n状态寄存器（n=0到15）

Base address: IIRFA = 0x4002_0000

Offset address: 0x10D + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CERRF	ORDYF	CPRCFF	CPRCS
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CPRCS	通道处理状态标志 0：不进行通道处理。1：正在执行通道处理。	R
1	CPRCFF	通道处理完成标志 0：通道处理未完成。1：通道处理完成。	R
2	ORDYF	输出数据准备完成标志 0：输出数据准备未完成。1：输出数据准备完成。	R
3	CERRF	操作错误标志 0：未发生操作错误。1：发生操作错误。	R
7:4	—	这些位读为0。	R

CPRCS位（通道处理状态标志）

[Setting condition]

●开始通道n的通道处理。

[Clearing condition]

●通道n的通道处理完成。

Note: 当设置条件和清除条件同时出现时，设置条件优先。

CPRCFF位（通道处理完成标志）

[Setting condition]

●通道n的通道处理完成。

[Clearing condition]

- When 1 is written to the IIRCHnFCLR.CPRCFFCLR bit or the channel processing of channel n is started.

Note: When the setting condition and clearing condition occur at the same time, the clearing condition takes precedence.

ORDYF bit (Output data preparation completion flag)

[Setting condition]

- The output data preparation of channel n is completed.

[Clearing condition]

- The IIRCHnOUT register is read or the channel processing of channel n is started.

Note: When the setting condition and clearing condition occur at the same time, the clearing condition takes precedence.

CERRF bit (Operation error flag)

[Setting condition]

- An operation error occurs when the output data preparation of channel n is completed.

[Clearing condition]

- When 1 is written to the IIRCHnFCLR.CERRFCLR bit.

Note: When the setting condition and clearing condition occur at the same time, the clearing condition takes precedence.

33.2.1.17 IIRCHnFCLR : Channel n Flag Clear Register (n = 0 to 15)

Base address: IIRFA = 0x4002_0000

Offset address: 0x10E + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CERRFCLR	—	CPRCFFCLR	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	The write value should be 0.	W
1	CPRCFFCLR	Channel processing completion flag clear bit 0: No effect 1: Clears the CPRCFF flag of the IIRCHnSTS register.	W
2	—	The write value should be 0.	W
3	CERRFCLR	Operation error flag clear bit 0: No effect 1: Clears the CERRF flag of the IIRCHnSTS register.	W
7:4	—	The write value should be 0.	W

This register clears the CERRF and CPRCFF flags of the IIRCHnSTS register.

[Clearing condition]

●当IIRCHnFCLR.CPRCFFCLR位写入1或通道n的通道处理开始时。

Note: 当设置条件和清零条件同时出现时，清零条件优先。

ORDYF位（输出数据准备完成标志）

[Setting condition]

●通道n的输出数据准备完成。

[Clearing condition]

●读取IIRCHnOUT寄存器或启动通道n的通道处理。

Note: 当设置条件和清零条件同时出现时，清零条件优先。

CERRF位（操作错误标志）

[Setting condition]

●通道n的输出数据准备完成时发生操作错误。

[Clearing condition]

●当IIRCHnFCLR.CERRFCLR位写入1时。

Note: 当设置条件和清零条件同时出现时，清零条件优先。

33.2.1.17 IIRCHnFCLR：通道n标志清除寄存器（n=0到15）

Base address: IIRFA = 0x4002_0000

Offset address: 0x10E + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CERRFCLR	—	CPRCFFCLR	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	写入值应为0。	W
1	CPRCFFCLR	通道处理完成标志清除位 0：无效1：清除IIRCHnSTS寄存器的CPRCFF标志。	W
2	—	写入值应为0。	W
3	CERRFCLR	操作错误标志清除位 0：无效1：清除IIRCHnSTS寄存器的CERRF标志。	W
7:4	—	写入值应为0。	W

该寄存器清除IIRCHnSTS寄存器的CERRF和CPRCFF标志。

33.2.1.18 IIRSTGmB0 : Stage m Coefficient b0 Register (m = 0 to 31)

Base address: IIRFA = 0x4002_0000

Offset address: 0x400 + 0x20 × m

Bit position:	31																												0
Bit field:																													
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	n/a	Coefficient data (single precision floating-point) of stage m	R/W

Each register corresponds to the coefficient data with the same symbol as shown in Figure 33.2.

If an access to this register is performed during the channel processing of any channel, bus access is forced to wait until the channel process is completed. A write access or read access is performed after the channel processing is complete.

When a write access to this register is performed, the write value is saved to the coefficient/delay data storage area. When a read access to this register is performed, the read value is read from the coefficient/delay data storage area.

33.2.1.19 IIRSTGmB1 : Stage m Coefficient b1 Register (m = 0 to 31)

Base address: IIRFA = 0x4002_0000

Offset address: 0x404 + 0x20 × m

Bit position:	31																												0
Bit field:																													
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	n/a	Coefficient data (single precision floating-point) of stage m	R/W

Each register corresponds to the coefficient data with the same symbol as shown in Figure 33.2.

If an access to this register is performed during the channel processing of any channel, bus access is forced to wait until the channel process is completed. A write access or read access is performed after the channel processing is complete.

When a write access to this register is performed, the write value is saved to the coefficient/delay data storage area. When a read access to this register is performed, the read value is read from the coefficient/delay data storage area.

33.2.1.20 IIRSTGmB2 : Stage m Coefficient b2 Register (m = 0 to 31)

Base address: IIRFA = 0x4002_0000

Offset address: 0x408 + 0x20 × m

Bit position:	31																												0
Bit field:																													
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	n/a	Coefficient data (single precision floating-point) of stage m	R/W

Each register corresponds to the coefficient data with the same symbol as shown in Figure 33.2.

If an access to this register is performed during the channel processing of any channel, bus access is forced to wait until the channel process is completed. A write access or read access is performed after the channel processing is complete.

33.2.1.18 IRSTGmB0:阶段m系数b0寄存器(m=0到31)

Base address: IIRFA = 0x4002_0000

Offset address: 0x400 + 0x20 × m

Bit position:	31																												0
Bit field:																													
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	n/a	第m阶段的系数数据（单精度浮点）	R/W

每个寄存器对应的系数数据具有相同的符号，如图33.2所示。

如果在任何通道的通道处理过程中访问该寄存器，则总线访问被强制等待，直到通道处理完成。在通道处理完成后执行写访问或读访问。

当对该寄存器执行写访问时，写入值将保存到系数延迟数据存储区。当对该寄存器进行读访问时，从系数延迟数据存储区中读取读值。

33.2.1.19 IRSTGmB1:阶段m系数b1寄存器(m=0到31)

Base address: IIRFA = 0x4002_0000

Offset address: 0x404 + 0x20 × m

Bit position:	31																												0
Bit field:																													
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	n/a	第m阶段的系数数据（单精度浮点）	R/W

每个寄存器对应的系数数据具有相同的符号，如图33.2所示。

如果在任何通道的通道处理过程中访问该寄存器，则总线访问被强制等待，直到通道处理完成。在通道处理完成后执行写访问或读访问。

当对该寄存器执行写访问时，写入值将保存到系数延迟数据存储区。当对该寄存器进行读访问时，从系数延迟数据存储区中读取读值。

33.2.1.20 IRSTGmB2:阶段m系数b2寄存器(m=0到31)

Base address: IIRFA = 0x4002_0000

Offset address: 0x408 + 0x20 × m

Bit position:	31																												0
Bit field:																													
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	n/a	第m阶段的系数数据（单精度浮点）	R/W

每个寄存器对应的系数数据具有相同的符号，如图33.2所示。

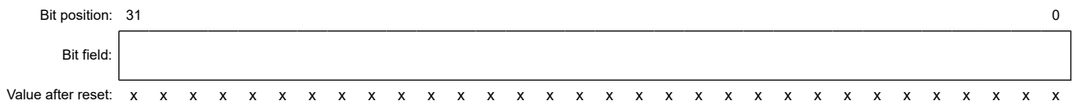
如果在任何通道的通道处理过程中访问该寄存器，则总线访问被强制等待，直到通道处理完成。在通道处理完成后执行写访问或读访问。

When a write access to this register is performed, the write value is saved to the coefficient/delay data storage area. When a read access to this register is performed, the read value is read from the coefficient/delay data storage area.

33.2.1.21 IIRSTGmA1 : Stage m Coefficient a1 Register (m = 0 to 31)

Base address: IIRFA = 0x4002_0000

Offset address: 0x40C + 0x20 × m



Bit	Symbol	Function	R/W
31:0	n/a	Coefficient data (single precision floating-point) of stage m	R/W

Each register corresponds to the coefficient data with the same symbol as shown in Figure 33.2.

If an access to this register is performed during the channel processing of any channel, bus access is forced to wait until the channel process is completed. A write access or read access is performed after the channel processing is complete.

When a write access to this register is performed, the write value is saved to the coefficient/delay data storage area. When a read access to this register is performed, the read value is read from the coefficient/delay data storage area.

33.2.1.22 IIRSTGmA2 : Stage m Coefficient a2 Register (m = 0 to 31)

Base address: IIRFA = 0x4002_0000

Offset address: 0x410 + 0x20 × m

Bit	Symbol	Function	R/W
31:0	n/a	Coefficient data (single precision floating-point) of stage m	R/W

Each register corresponds to the coefficient data with the same symbol as shown in Figure 33.2.

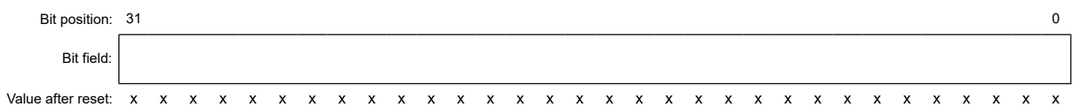
If an access to this register is performed during the channel processing of any channel, bus access is forced to wait until the channel process is completed. A write access or read access is performed after the channel processing is complete.

When a write access to this register is performed, the write value is saved to the coefficient/delay data storage area. When a read access to this register is performed, the read value is read from the coefficient/delay data storage area.

33.2.1.23 IIRSTGmD0 : Stage m Delay Data D0 Register (m = 0 to 31)

Base address: IIRFA = 0x4002_0000

Offset address: 0x414 + 0x20 × m



Bit	Symbol	Function	R/W
31:0	n/a	Delay data (single precision floating-point) of stage m	R/W

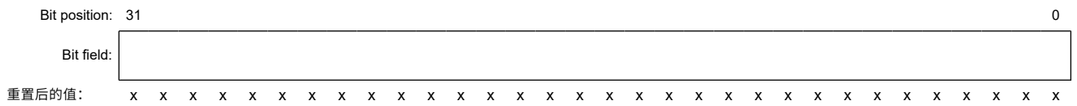
Each register corresponds to the delay data with the same symbol as shown in Figure 33.2.

当对该寄存器执行写访问时，写入值将保存到系数延迟数据存储区。当对该寄存器进行读访问时，从系数延迟数据存储区中读取读值。

33.2.1.21 IRSTGmA1:阶段m系数a1寄存器(m=0到31)

Base address: IIRFA = 0x4002_0000

Offset address: 0x40C + 0x20 × m



Bit	Symbol	Function	R/W
31:0	n/a	第m阶段的系数数据（单精度浮点）	R/W

每个寄存器对应的系数数据具有相同的符号，如图33.2所示。

如果在任何通道的通道处理过程中访问该寄存器，则总线访问被强制等待，直到通道处理完成。在通道处理完成后执行写访问或读访问。

当对该寄存器执行写访问时，写入值将保存到系数延迟数据存储区。当对该寄存器进行读访问时，从系数延迟数据存储区中读取读值。

33.2.1.22 IRSTGmA2:阶段m系数a2寄存器(m=0到31)

Base address: IIRFA = 0x4002_0000

Offset address: 0x410 + 0x20 × m

Bit	Symbol	Function	R/W
31:0	n/a	第m阶段的系数数据（单精度浮点）	R/W

每个寄存器对应的系数数据具有相同的符号，如图33.2所示。

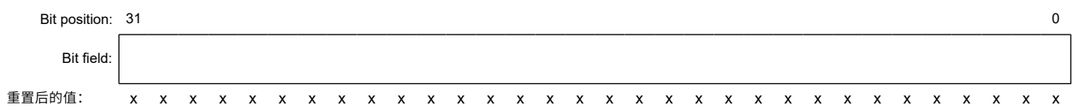
如果在任何通道的通道处理过程中访问该寄存器，则总线访问被强制等待，直到通道处理完成。在通道处理完成后执行写访问或读访问。

当对该寄存器执行写访问时，写入值将保存到系数延迟数据存储区。当对该寄存器进行读访问时，从系数延迟数据存储区中读取读值。

33.2.1.23 IRSTGmD0:阶段m延迟数据D0寄存器(m=0到31)

Base address: IIRFA = 0x4002_0000

Offset address: 0x414 + 0x20 × m



Bit	Symbol	Function	R/W
31:0	n/a	阶段m的延迟数据（单精度浮点）	R/W

每个寄存器对应的延迟数据具有相同的符号，如图33.2所示。

The value of the delay data D0 register is updated when the operation of the stage corresponding to the register is executed.

If an access to this register is performed during the channel processing of any channel, bus access is forced to wait until the channel process is completed. A write access or read access is performed after the channel processing is complete.

When a write access to this register is performed, the write value is saved to the coefficient/delay data storage area. When a read access to this register is performed, the read value is read from the coefficient/delay data storage area.

33.2.1.24 IIRSTGmD1 : Stage m Delay Data D1 Register (m = 0 to 31)

Base address: IIRFA = 0x4002_0000

Offset address: 0x418 + 0x20 × m

Bit position:	31																												0
Bit field:																													
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	n/a	Delay data (single precision floating-point) of stage m	R/W

Each register corresponds to the delay data with the same symbol as shown in Figure 33.2.

The value of the delay data D1 register is updated when the operation of the stage corresponding to the register is executed.

If an access to this register is performed during the channel processing of any channel, bus access is forced to wait until the channel process is completed. A write access or read access is performed after the channel processing is complete.

When a write access to this register is performed, the write value is saved to the coefficient/delay data storage area. When a read access to this register is performed, the read value is read from the coefficient/delay data storage area.

33.3 Operation

33.3.1 Overview

IIRFA has a cascade connected biquad IIR (Infinite Impulse Response) filter operation function.

The formula for the transfer function of cascade connected M biquad IIR filters is as follows:

$$H(z) = \prod_{m=1}^{M} \frac{b_0^m + b_1^m z^{-1} + b_2^m z^{-2}}{1 - a_1^m z^{-1} - a_2^m z^{-2}}$$

b_0^m , b_1^m , and b_2^m , are feed-forward coefficients, and a a_1^m and a_2^m are feed-back coefficients.

The operation for each biquad IIR filter is defined by the following difference equation:

$$y(n) = b_0x(n) + b_1x(n-1) + b_2x(n-2) + a_1y(n-1) + a_2y(n-2)$$

$x(n)$ is input data, $y(n)$ is output data, $x(n-1)$ and $y(n-1)$ are input data and output data of 1 sample period delay, and $x(n-2)$ and $y(n-2)$ are input data and output data of 2 sample period delay.

IIRFA performs the cascade connected Direct form II transposed biquad IIR filter operation shown in Figure 33.2.

One biquad IIR filter operation is called a stage. Any number of stages up to 32 stages that are cascade connected are called channels.

延迟数据D0寄存器的值在该寄存器对应的级的操作被执行时被更新。

如果在任何通道的通道处理过程中访问该寄存器，则总线访问被强制等待，直到通道处理完成。在通道处理完成后执行写访问或读访问。

当对该寄存器执行写访问时，写入值将保存到系数延迟数据存储区。当对该寄存器进行读访问时，从系数延迟数据存储区中读取读值。

33.2.1.24 IRSTGmD1:阶段m延迟数据D1寄存器(m=0到31)

Base address: IIRFA = 0x4002_0000

Offset address: 0x418 + 0x20 × m

Bit position:	31																												0
Bit field:																													
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	n/a	阶段m的延迟数据（单精度浮点）	R/W

每个寄存器对应的延迟数据具有相同的符号，如图33.2所示。

延迟数据D1寄存器的值在执行该寄存器对应的级的操作时被更新。

如果在任何通道的通道处理过程中访问该寄存器，则总线访问被强制等待，直到通道处理完成。在通道处理完成后执行写访问或读访问。

当对该寄存器执行写访问时，写入值将保存到系数延迟数据存储区。当对该寄存器进行读访问时，从系数延迟数据存储区中读取读值。

33.3 Operation

33.3.1 Overview

IIRFA具有级联双二阶IIR（InfiniteImpulseResponse）滤波器运算功能。

级联M个双二阶IIR滤波器的传递函数公式如下：

$$H(z) = \prod_{m=1}^{M} \frac{b_0^m + b_1^m z^{-1} + b_2^m z^{-2}}{1 - a_1^m z^{-1} - a_2^m z^{-2}}$$

b_0^m Lb_1^m L　　b^m 是前馈系数，aa1　　a^m是反馈系数。

每个双二阶IIR滤波器的操作由以下差分方程定义：

$$y(n) = b_0x(n) + b_1x(n-1) + b_2x(n-2) + a_1y(n-1) + a_2y(n-2)$$

x(n)是输入数据，y(n)是输出数据，x(n−1)和y(n−1)是1个采样周期延迟的输入数据和输出数据，x(n−2)和y(n−2)是2个采样周期延迟的输入数据和输出数据。

IIRFA执行图33.2所示的级联直接形式II转置双二阶IIR滤波器操作。

一个双二阶IIR滤波器操作称为阶段。级联连接的多达32个级的任意数量的级称为通道。

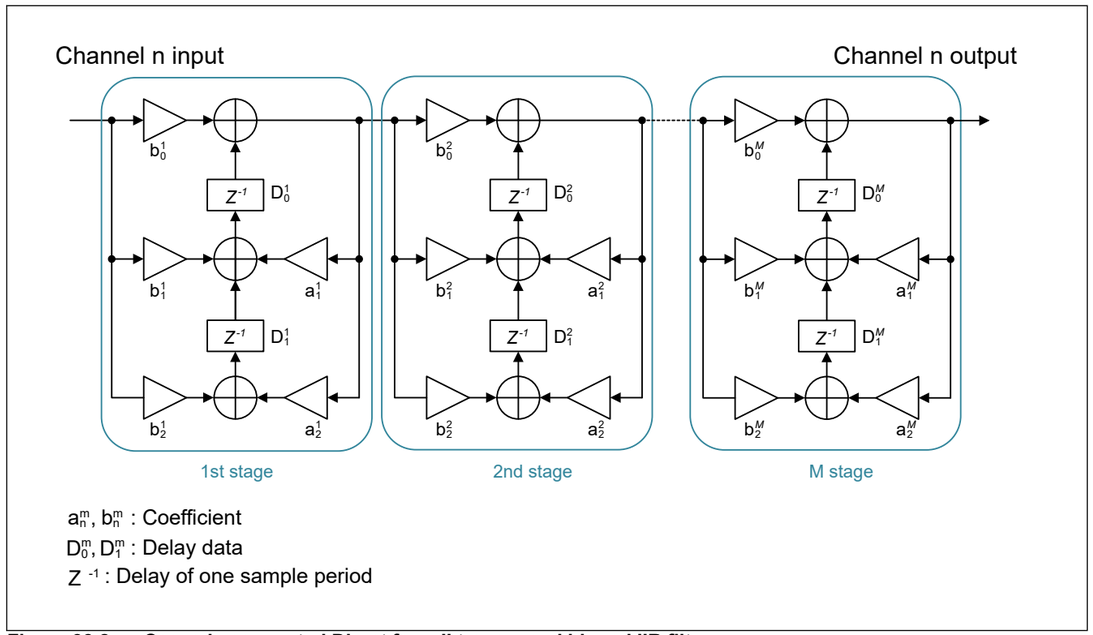


Figure 33.2 Cascade connected Direct form II transposed biquad IIR filter

The stages to be cascade connected can be selected for each channel. In addition, the coefficient (a_1, a_2, b_0, b_1, b_2) and delay data (D_0, D_1) can be set for each stage.

Figure 33.3 shows an example of stage selection for each channel. In this example, channel 0 performs the cascade connected biquad IIR filter operation for stage 0, stage 2, and stage 3. For the operation, see section 33.3.2. Channel Processing Operation.

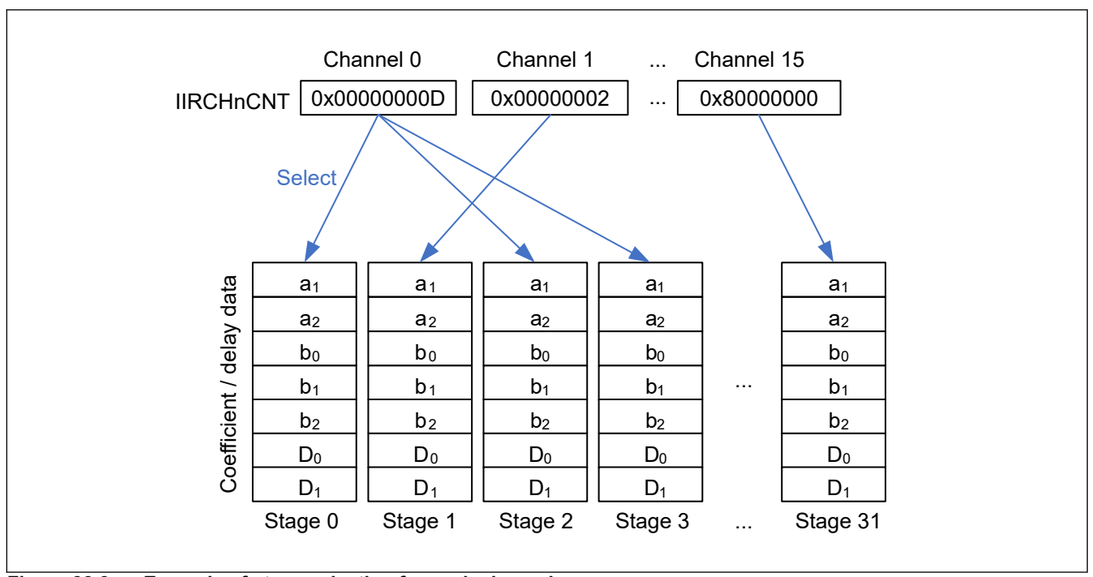


Figure 33.3 Example of stage selection for each channel

The coefficient and delay data for each stage are stored to the coefficient/delay data storage area. The coefficient/delay data storage area has an error detection/correction function by ECC. When the ECC error detection/correction function is

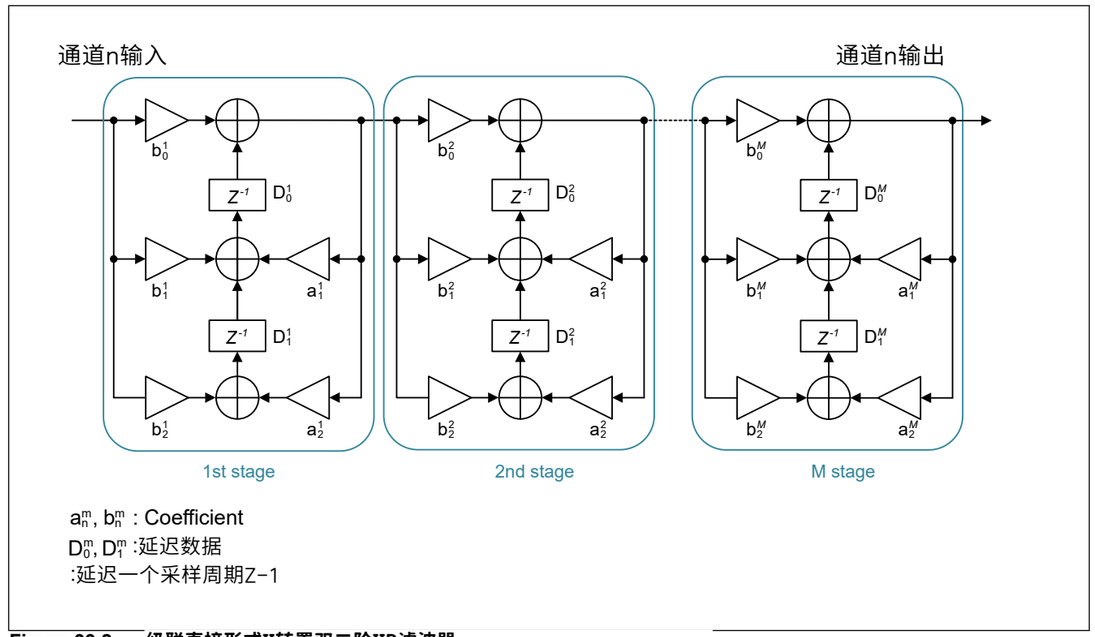


Figure 33.2 级联直接形式II转置双二阶IIR滤波器

可以为每个通道选择要级联的级。此外，可以为每个阶段设置系数（a1，a2，b0，b1，b2）和延迟数据（D0，D1）。

图33.3显示了每个通道的阶段选择示例。在此示例中，通道0对第0级、第2级和第3级执行级联连接的双二阶IIR滤波器操作。有关操作，请参阅第33.3.2节。通道处理操作。

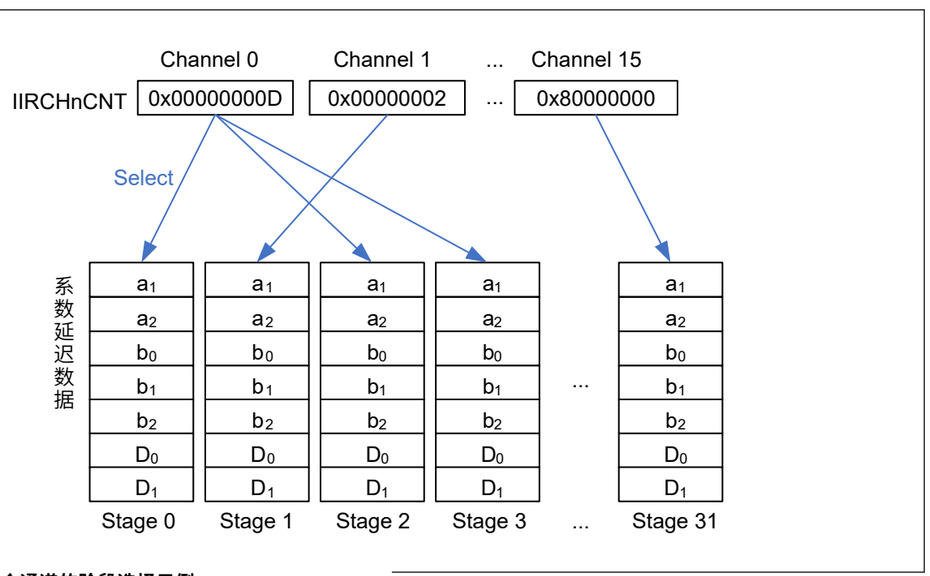


Figure 33.3 每个通道的阶段选择示例

每一级的系数和延迟数据存储到系数延迟数据存储区。系数延迟数据存储区具有ECC检错校正功能。当ECC检错校正功能为

enabled (IIRECCCNT.ECCMD = 1), an error that has occurred in the data in the coefficient/delay data storage area can be detected and corrected. For details on the ECC error, see section 33.3.4. Operation on ECC Error Detection.

The I/O data, stage coefficient/delay data are retained in the single precision floating-point format specified in the IEEE754 standard. For details on the single precision floating-point, see Figure 33.4.

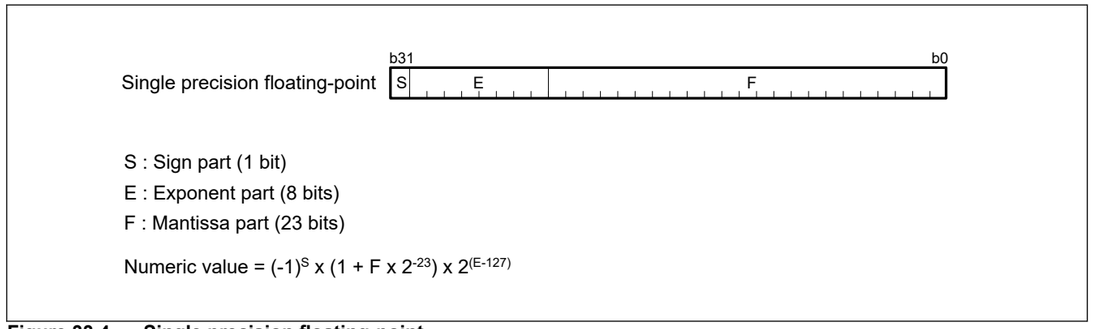


Figure 33.4 Single precision floating-point

The single precision floating-point format supports the following values:

- 0 < E < 255 (normal numbers)
- E = 0 and F = 0 (signed zero)
- E = 0 and F > 0 (denormalized numbers)
- E = 255 and F = 0 (infinity)
- E = 255 and F > 0 (NaN: Not a Number)
  MSB of F is 0. (SNaN: Signaling NaN)
  MSB of F is 1. (QNaN: Quiet NaN)

IIRFA treats the input as +0 if a positive denormalized number is input, −0 if a negative denormalized number is input, and infinity if a NaN (Not a Number) is input.

IIRFA performs addition and multiplication of single precision floating-points multiple times in the cascade connected biquad IIR filter operation. If the result of each addition and multiplication is a positive denormalized number, it is treated as +0. If the result is a negative denormalized number, it is treated as -0. If the result is a NaN (Not a Number), it is treated as infinity. In addition, the rounding mode for each addition and multiplication result can be selected by IIROPCNT.

Note: The output data of channel n may be infinity depending on the channel processing. At this time, an operation error occurs. For details on the operation error, see section 33.3.3. Operation When an Operation Error Occurs.

33.3.2 Channel Processing Operation

Channel processing is a series of operations that are executed when a write access is performed to the input register of a channel. Operations for all stages used by the channel are performed sequentially during the channel processing. If the output data operation is completed in the middle of the channel processing (before the IIRCHnSTS.CPRFF flag is 1), the IIRCHnSTS.ORDYF flag is 1 and the output data (IIRCHnOUT register) can be read.

Figure 33.5 shows an example of channel processing operation.

1. Input data is written.
   When input data is written to the IIR channel n input register (IIRCHnINP), the IIR filter operation is performed in accordance with the setting of the IIR channel n control register (IIRCHnCNT). At this time, the IIRCHnSTS.CPRCS bit is 1. In addition, the delay data registers for stage m (IIRSTGmD0, IIRSTGmD1) used for the operation are updated by the operation result.
2. Operation of the output data is completed.
   When the operation of the output data is completed, the IIRCHnSTS.ORDYF flag is 1 and the operation result is stored to the IIR channel n output register (IIRCHnOUT).
3. Output data is read.
   When the value is read from the IIRCHnOUT register, the IIRCHnSTS.ORDYF flag is 0.

启用（IIRECCCNT.ECCMD=1），可以检测和纠正系数延迟数据存储区域中的数据中发生的错误。有关ECC错误的详细信息，请参阅第33.3.4节。ECC错误检测操作。

IO数据、级系数延迟数据以IEEE754标准中规定的单精度浮点格式保留。有关单精度浮点的详细信息，请参见图33.4。

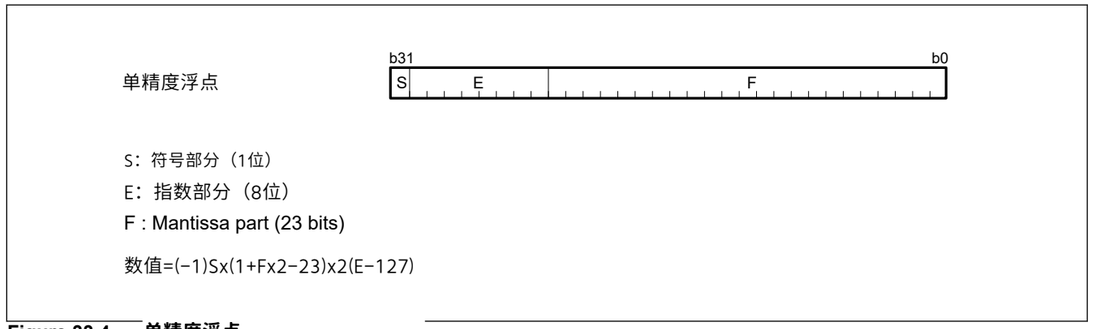


Figure 33.4 单精度浮点

单精度浮点格式支持以下值：

- 0 < E < 255 (normal numbers)
- E = 0 and F = 0 (signed zero)
- E = 0 and F > 0 (denormalized numbers)
- E = 255 and F = 0 (infinity)
- ●E=255且F>0（NaN：非数字）
  F的MSB为0。(SNaN:SignalingNaN)
  F的MSB为1。（QNaN：安静的NaN）

如果输入一个正的非规范化数字，则IIRFA将输入视为+0，如果输入一个负的非规范化数字，则将输入视为−0，如果输入NaN（非数字），则将其视为无穷大。

IIRFA在级联双二阶IIR滤波器操作中多次执行单精度浮点的加法和乘法。如果每次加法和乘法的结果是正的非规格化数，则将其视为+0。如果结果是负的非规范化数字，则将其视为−0。如果结果是NaN（不是数字），则将其视为无穷大。此外，可以通过IIROPCNT选择每个加法和乘法结果的舍入模式。

Note: 取决于通道处理，通道n的输出数据可能是无穷大的。此时，发生操作错误。有关操作错误的详细信息，请参阅第33.3.3节。发生操作错误时的操作。

33.3.2 通道处理操作

通道处理是在对通道的输入寄存器执行写访问时执行的一系列操作。通道使用的所有阶段的操作在通道处理期间顺序执行。如果输出数据操作在通道处理过程中完成（在IIRCHnSTS.CPRFF标志为1之前），则IIRCHnSTS.ORDYF标志为1，并且可以读取输出数据（IIRCHnOUT寄存器）。

图33.5显示了通道处理操作的示例。

1.写入输入数据。
当输入数据写入IIR通道n输入寄存器(IIRCHnINP)时，将根据IIR通道n控制寄存器(IIRCHnCNT)的设置执行IIR滤波器操作。此时，IIRCHnSTS.CPRCS位为1。另外，用于运算的阶段m的延迟数据寄存器（IIRSTGmD0，IIRSTGmD1）由运算结果更新。

2.输出数据的操作完成。
当输出数据的运算完成时，IIRCHnSTS.ORDYF标志为1，运算结果存入IIR通道n输出寄存器（IIRCHnOUT）。

3.读取输出数据。
当从IIRCHnOUT寄存器读取值时，IIRCHnSTS.ORDYF标志为0。

4. Channel processing is completed.
   When the channel processing is completed, the IIRCHnSTS.CPRCFF flag is 1. In addition, the IIRCHnSTS.CPRCS bit is 0.

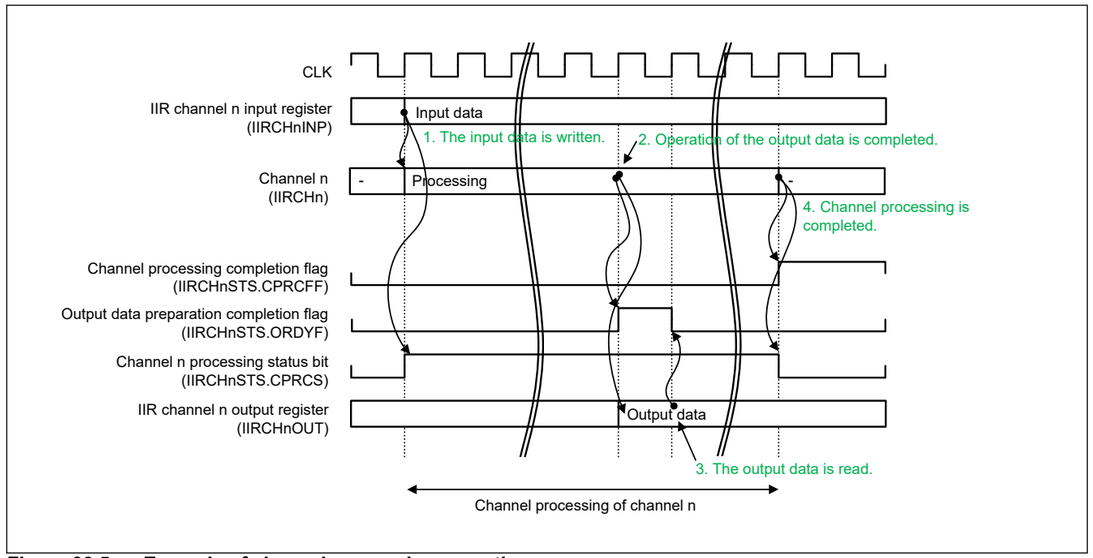


Figure 33.5 Example of channel processing operation

Note: The maximum number of channels that can be processed at the same time is 1. If a write access to the IIRCHnINP register is performed during the channel processing of any channel, bus access is forced to wait until the channel processing that is being performed is completed.

33.3.3 Operation When an Operation Error Occurs

An operation error shows that the result of the cascade connected biquad IIR filter operation is infinity. If the value of the IIR channel n output register (IIRCHnOUT) is positive or negative infinity, an operation error occurs at the same time as when the output data preparation is completed. If an operation error occurs, the IIRCHnSTS.CERRF flag is 1.

A positive infinity and a negative infinity are collectively referred to as infinity or ∞. In addition, +∞ indicates positive infinity and −∞ indicates negative infinity.

The value of the IIRCHnOUT register is the value that is obtained by performing the addition and multiplication of single precision floating-points multiple times. When the result of any addition or multiplication is infinity, this value is propagated and the value of the IIRCHnOUT register ultimately becomes infinity.

The following examples show the conditions in which the result of the addition and multiplication becomes infinity.

(1) An overflow occurs in the addition or multiplication.

If the result of addition or multiplication exceeds the maximum finite value represented by a single precision floating-point, an overflow occurs. If an overflow occurs, the result of the relevant addition or multiplication becomes infinity.

(2) The input value of the addition or multiplication includes SNaN, QNaN, or infinity.

When the input value of the addition or multiplication includes SNaN, QNaN, or infinity, the result of the relevant addition or multiplication becomes infinity.

Table 33.3 and Table 33.4 show the calculation results for input values at the time of addition and multiplication.

4.通道处理完成。
当通道处理完成时，IIRCHnSTS.CPRCFF标志为1。此外，IIRCHnSTS.CPRCS位为0。

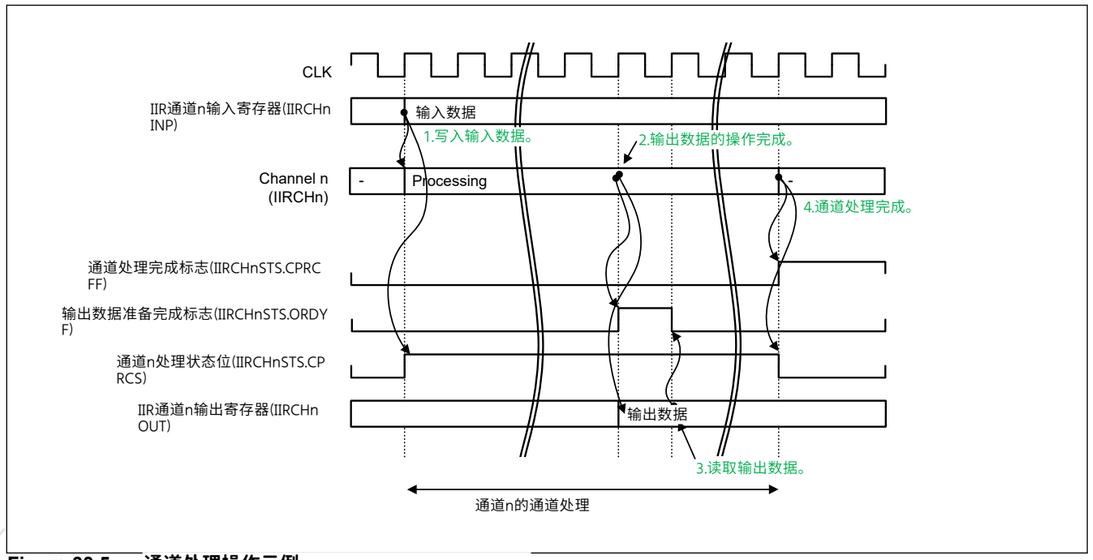


Figure 33.5 通道处理操作示例

Note: 可同时处理的最大通道数为1。如果在任何通道的通道处理过程中对IIRCHnINP寄存器进行写访问，总线访问将被强制等待，直到正在执行的通道处理完成.

33.3.3 发生操作错误时的操作

运算错误表明级联双二阶IIR滤波器运算的结果为无穷大。如果IIR通道n输出寄存器(IIRCHnOUT)的值为正或负无穷大，则在输出数据准备完成的同时发生操作错误。如果发生操作错误，则IIRCHnSTS.CERRF标志为1。

正无穷大和负无穷大统称为无穷大或∞。此外，+∞表示正无穷大，−∞表示负无穷大。

IIRCHnOUT寄存器的值是单精度浮点数多次加法和乘法得到的值。当任何加法或乘法的结果为无穷大时，该值被传播，IIRCHnOUT寄存器的值最终变为无穷大。

以下示例显示了加法和乘法的结果变为无穷大的条件。

(1)加法或乘法发生溢出。

如果加法或乘法的结果超过单精度浮点表示的最大有限值，则会发生溢出。如果发生溢出，相关加法或乘法的结果将变为无穷大。

(2)加法或乘法的输入值包括SNaN、QNaN或无穷大。

当加法或乘法的输入值包括SNaN、QNaN或无穷大时，相关加法或乘法的结果变为无穷大。

表33.3和表33.4显示了加法和乘法时输入值的计算结果。

Table 33.3 Calculation results for input values at the time of addition (x + y)

		y				
		Normal number	+0, +Denormalized number	−0, −Denormalized number	+∞, +SNaN, +QNaN	−∞, −SNaN, −QNaN
x	Normal number	Addition*1			+∞	−∞
	+0, +Denormalized number	Addition*1	+0		+∞	−∞
	−0, −Denormalized number	Addition*1	+0	−0	+∞	−∞
	+∞, +SNaN, +QNaN	+∞				
	+∞, +SNaN, −QNaN	−∞			+∞	−∞

Note 1. If an overflow occurs, the calculation result is +∞ or −∞.

Table 33.4 Calculation results for input values at the time of multiplication (x × y)

		y					
		+Normal number	−Normal number	+0, +Denormalized number	−0, −Denormalized number	+∞, +SNaN, +QNaN	−∞, −SNaN, −QNaN
x	+Normal number	Multiplication*1				+∞	−∞
	−Normal number	Multiplication*1				−∞	+∞
	+0, +Denormalized number	Multiplication*1		+0	−0	+∞	
	−0, −Denormalized number	Multiplication*1		−0	+0	+∞	
	+∞, +SNaN, +QNaN	+∞	−∞	+∞			−∞
	+∞, +SNaN,−QNaN	−∞	+∞			−∞	+∞

Note 1. If an overflow occurs, the calculation result is +∞ or −∞.

33.3.4 Operation on ECC Error Detection

The coefficient/delay data storage area has an ECC error detection/correction function and a corrected data write-back function.

The ECC specification is SEC-DED (Single-Error Correction/Double-Error Detection). A 7-bit ECC code is generated for one coefficient/delay data (32-bit data).

(1) ECC error detection function

This ECC error detection function detects the ECC error (ECC 1-bit error, ECC 2-bit error) if an error occurs in the data in the coefficient/delay data storage area. An ECC error is detected when a read access to the coefficient/delay data register is performed and when the coefficient/delay data is used during the channel processing.

An ECC error may be detected multiple times during one channel processing. Table 33.5 shows the conditions for detecting an ECC error.

Table 33.5 Conditions for detecting an ECC error

ECC error detection/correction function	Number of bits for the error that occurred	ECC error
Enable (IIRECCCNT.ECCMD = 1)	0 bits	No ECC error is detected.
	1 bit	An ECC 1-bit error is detected.
	2 bits	An ECC 2-bit error is detected.
	3 bits or more	Whether an ECC error is detected is undefined.
Disable (IIRECCCNT.ECCMD = 0)	Don't Care	No ECC error is detected.

Table 33.3 加法时输入值的计算结果(x+y)

		y				
		正常号码	+0, +Denormalized number	−0, −Denormalized number	+∞, +SNaN, +QNaN	−∞, −SNaN, −QNaN
x	正常号码	Addition*1			+∞	−∞
	+0, +Denormalized number	Addition*1	+0		+∞	−∞
	−0, −Denormalized number	Addition*1	+0	−0	+∞	−∞
	+∞, +SNaN, +QNaN	+∞				
	+∞, +SNaN, −QNaN	−∞			+∞	−∞

注1.如果发生溢出，则计算结果为+∞或−∞。

Table 33.4 乘法时输入值的计算结果(x×y)

		y					
		+Normal number	−Normal number	+0, +Denormalized number	−0, −Denormalized number	+∞, +SNaN, +QNaN	−∞, −SNaN, −QNaN
x	+Normal number	Multiplication*1				+∞	−∞
	−Normal number	Multiplication*1				−∞	+∞
	+0, +Denormalized number	Multiplication*1		+0	−0	+∞	
	−0, −Denormalized number	Multiplication*1		−0	+0	+∞	
	+∞, +SNaN, +QNaN	+∞	−∞	+∞			−∞
	+∞, +SNaN,−QNaN	−∞	+∞			−∞	+∞

注1.如果发生溢出，则计算结果为+∞或−∞。

33.3.4 ECC错误检测操作

系数延迟数据存储区具有ECC错误检测校正功能和校正数据回写功能。

ECC规范是SEC-DED（单纠错双错误检测）。为一个系数延迟数据（32位数据）生成一个7位ECC码。

(1) ECC错误检测功能

此ECC错误检测功能在系数延迟数据存储区域中的数据发生错误时检测ECC错误（ECC1位错误、ECC2位错误）。当执行对系数延迟数据寄存器的读取访问以及在通道处理期间使用系数延迟数据时，检测到ECC错误。

在一个通道处理期间，可能会多次检测到ECC错误。表33.5显示了检测ECC错误的条件。

Table 33.5 检测ECC 错误的条件

ECC错误检测校正功能	发生错误的位数	ECC error
Enable (IIRECCCNT.ECCMD = 1)	0 bits	未检测到ECC错误。
	1 bit	检测到ECC1位错误。
	2 bits	检测到ECC2位错误。
	3位或更多	是否检测到ECC错误未定义。
Disable (IIRECCCNT.ECCMD = 0)	Don't Care	未检测到ECC错误。

When an ECC 1-bit error is detected, the IIRECCEF.ESEF flag is 1. When an ECC 2-bit error is detected, the IIRECCEF.EDEF flag is 1.

(2) ECC error correction function

The ECC error correction function corrects errors in the values read from the coefficients/delayed data register or the data used for the operation. When an ECC 1-bit error is detected, the error correction is performed.

(3) Corrected data write-back function

The corrected data write-back function writes back the value after an ECC error correction to the data in the coefficient/ delay data storage area. If the ECC error correction is performed when the corrected data write-back function is enabled (IIRECCCNT.ECCWBDIS = 0), the corrected data is written back.

When the ECC error correction is performed during the channel processing, the channel processing continues using the data after ECC error correction. At this time, the number of channel processing cycles is not extended.

When the corrected data is written back during the channel processing, the channel processing continues. At this time, the number of channel processing cycles is extended in accordance with the number of write-back times.

33.3.5 Operating Procedure

33.3.5.1 Initial Settings

Perform the initial settings of IIRFA before use. Table 33.6 shows an example of the initial setting procedure.

When the ECC error detection/correction function is enabled (IIRECCCNT.ECCMD = 1), write the initial values to all coefficient/delay data registers of all stages. The data in the coefficient/delay data storage area is undefined when the power is turned on. Therefore, when the ECC error detection/correction function is enabled (IIRECCCNT.ECCMD = 1), if the data is read from the coefficient/delay data storage area without initializing or if the channel processing is started without initializing, an ECC error occurs.

Table 33.6 Example of initialization procedures

Step	Description	Register to be set
1	Set the ECC function of the coefficient/delay data storage area.	IIRECCCNT
2	Set what stages are to be cascade connected for use in each channel.	IIRCHnCNT
3	Set the initial values (single precision floating-points) to the coefficient/ delay data registers.	IIRSTGmB0, IIRSTGmB1, IIRSTGmB2,IIRSTGmA1, IIRSTGmA2, IIRSTGmD0, IIRSTGmD1
4	Enable or disable the ECC error interrupt and channel n interrupt.	IIRECCINT IIRCHnINT

33.3.5.2 Procedure for Channel Processing Execution

This section shows an example procedure of the channel process execution.

There are three methods to execute the channel processing. The difference between the three methods is the procedure for output data reading after the channel processing starts.

Table 33.7 shows the procedure for output data reading of each method.

Table 33.7 Procedure for output data reading of each method

	Single data processing	Multiple data processing
Method 1	Read without waiting for output data preparation completion.	
Method 2	Read after polling the output data preparation completion flag.	Read after polling the channel processing completion flag.
Method 3	Read after accepting the output data preparation completion interrupt.	Read after accepting the channel processing completion interrupt.

The single data processing and multiple data processing classify the channel processing procedure in accordance with the number of data to be processed. Single data processing means that the channel processing is performed for one input value

当检测到ECC1位错误时，IIRECCEF.ESEF标志为1。当检测到ECC2位错误时，IIRECCEF.EDEF标志为1。

(2) ECC纠错功能

ECC纠错功能纠正从系数延迟数据寄存器读取的值或用于操作的数据中的错误。当检测到ECC1位错误时，执行纠错。

(3) 修正数据回写功能

修正数据回写功能将ECC纠错后的值回写到系数延迟数据存储区域的数据中。如果在启用更正数据回写功能时执行ECC纠错（IIRECCCNT.ECCWBDIS=0），则回写更正数据。

当在信道处理过程中进行ECC纠错时，信道处理继续使用ECC纠错后的数据。此时，通道处理周期数不延长。

当在通道处理期间写回校正数据时，通道处理继续。此时，通道处理周期数根据回写次数而延长。

33.3.5 运作程序

33.3.5.1 初始设置

使用前执行IIRFA的初始设置。表33.6显示了初始设置过程的示例。

当ECC错误检测校正功能使能时（IIRECCCNT.ECCMD=1），将初始值写入所有阶段的所有系数延迟数据寄存器。上电时系数延迟数据存储区中的数据未定义。因此，当启用ECC错误检测校正功能时（IIRECCCNT.ECCMD=1），如果在未初始化的情况下从系数延迟数据存储区读取数据，或者如果在未初始化的情况下启动通道处理，则会发生ECC错误。

Table 33.6 初始化程序示例

Step	Description	要设置的注册
1	设置系数延迟数据存储区的ECC功能。	IIRECCCNT
2	设置要级联连接的级以在每个通道中使用。	IIRCHnCNT
3	将初始值（单精度浮点）设置到系数延迟数据寄存器。	IIRSTGmB0, IIRSTGmB1, IIRSTGmB2,IIRSTGmA1, IIRSTGmA2, IIRSTGmD0, IIRSTGmD1
4	启用或禁用ECC错误中断和通道n中断。	IIRECCINT IIRCHnINT

33.3.5.2 通道处理执行程序

本节显示了通道处理执行的示例过程。

有三种方法来执行通道处理。三种方法的区别在于通道处理开始后读取输出数据的过程。

表33.7显示了每种方法的输出数据读取过程。

Table 33.7 各方法的输出数据读取步骤

	单一数据处理	多数据处理
Method 1	无需等待输出数据准备完成即可读取。	
Method 2	轮询输出数据准备完成标志后读取。	轮询通道处理完成标志后读取。
Method 3	接受输出数据准备完成中断后读取。	接受通道处理完成中断后读取。

单数据处理和多数据处理根据要处理的数据数量对通道处理过程进行分类。单数据处理是指对一个输入值进行通道处理

and no other channel processing is performed after the processing is completed. Multiple data processing means that the channel processing is performed consecutively for multiple input values.

Method 2 and method 3 have different procedures for single data processing and multiple data processing. IIRFA completes the output data preparation before the channel processing is completed. Therefore, to reduce the number of cycles, the procedure for single data processing is to read the output data when the output data preparation is completed, instead of when the channel processing is completed.

Points to note for methods 1, 2, and 3 are as follows:

- Method 1
  - Since the flag determination processing is not required, the overhead is small.
  - When a read access to the IIRCHnOUT register is performed, bus access is forced to wait until the output data preparation is completed.
  - The input value can be written to the IIRCHnINP register and a read access to the IIRCHnOUT register can be performed with DMA.
- Method 2
  - Since the flag determination processing is required, the overhead is large.
  - When a read access to the IIRCHnOUT register is performed, bus access is not forced to wait.
- Method 3
  - The overhead is relatively large due to processing at the time of interrupt acceptance.
  - When a read access to the IIRCHnOUT register is performed, bus access is not forced to wait.
  - After the channel processing starts, the CPU can perform other process until the output data preparation completion interrupt or the channel processing completion interrupt occurs.

In accordance with the number of stages used for the channel processing, the number of cycles increases from the start of the channel processing to the completion of output data preparation and channel processing. Therefore, the recommended method may vary depending on the number of stages to be used.

Method 1 is recommended when the number of stages used for the channel processing is small. When this method is used, the bus is occupied until the output data preparation is completed. Therefore, bus access to other bus master that uses the same bus is forced to wait. In addition, the CPU does not accept any interrupt while the bus access is waited.

Methods 2 and 3 are recommended when the number of stages used for the channel processing is large. When these methods are used, the overhead is large due to the flag determination processing or interrupt processing. Therefore, when the number of stages used for the channel processing is small, the effect of the overhead is large.

Figure 33.6, Table 33.7, and Figure 33.8 show an example procedure for each method.

处理完成后不进行其他通道处理。多数据处理是指对多个输入值连续进行通道处理。

方法2和方法3对单数据处理和多数据处理的过程不同。IIRFA在通道处理完成之前完成输出数据准备。因此，为了减少周期数，单个数据处理的过程是在输出数据准备完成时读取输出数据，而不是在通道处理完成时读取。

方法一、二、三的注意事项如下：

- Method 1

  由于不需要标志确定处理，因此开销很小。

  当对IIRCHnOUT寄存器执行读访问时，总线访问被强制等待，直到输出数据准备完成。

  可以将输入值写入IIRCHnINP寄存器，并且可以使用DMA执行对IIRCHnOUT寄存器的读取访问。

- Method 2

  由于需要标志确定处理，因此开销很大。

  当对IIRCHnOUT寄存器执行读访问时，总线访问不会被强制等待。

- Method 3

  由于接受中断时的处理，开销比较大。

  当对IIRCHnOUT寄存器执行读访问时，总线访问不会被强制等待。

  通道处理开始后，CPU可以进行其他处理，直到输出数据准备完成中断或通道处理完成中断发生。

根据用于通道处理的阶段数，从通道处理开始到输出数据准备和通道处理完成的周期数增加。因此，推荐的方法可能会根据要使用的阶段数而有所不同。

当用于通道处理的阶段数较少时，建议使用方法1。使用这种方法时，总线一直被占用，直到输出数据准备完成。因此，对使用同一总线的其他总线主机的总线访问被迫等待。此外，在等待总线访问期间，CPU不接受任何中断。

当用于通道处理的阶段数较大时，建议使用方法2和3。当使用这些方法时，由于标志确定处理或中断处理，开销很大。因此，当用于信道处理的级数较少时，开销的影响较大。

图33.6、表33.7和图33.8显示了每种方法的示例过程。

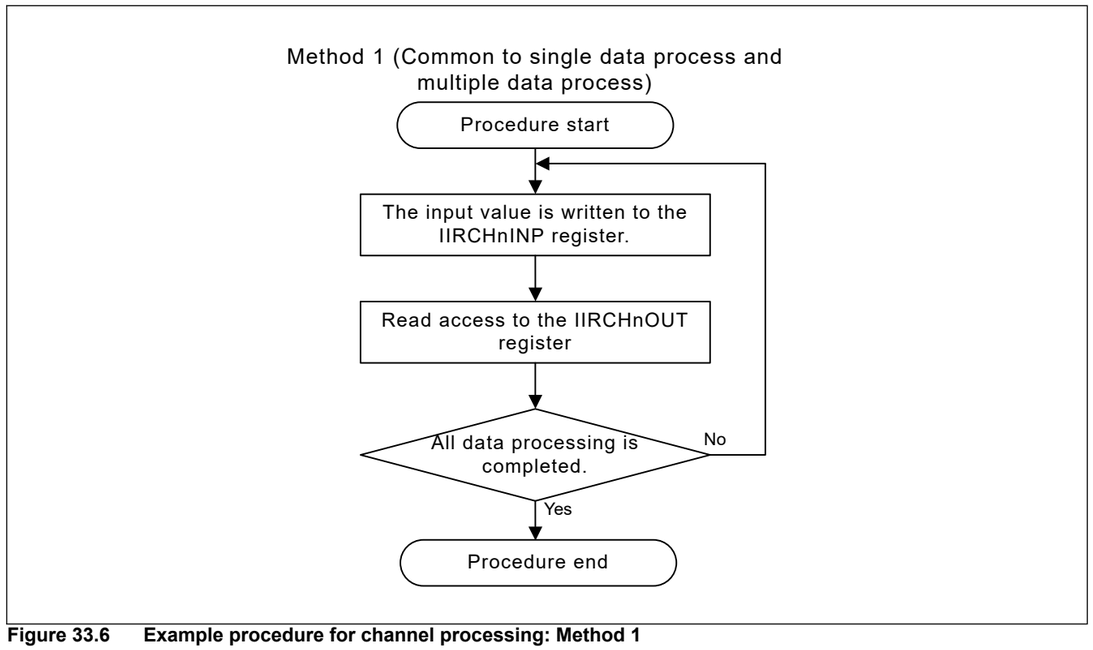


Figure 33.6 Example procedure for channel processing: Method 1

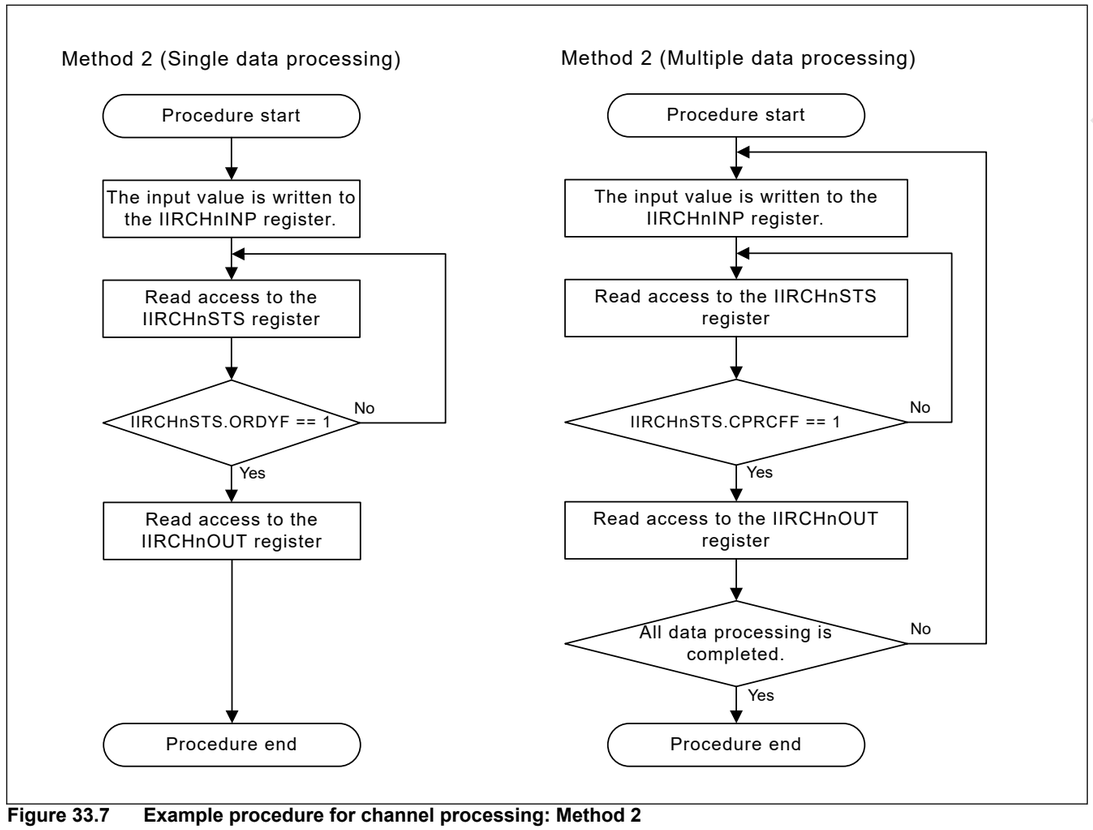


Figure 33.7 Example procedure for channel processing: Method 2

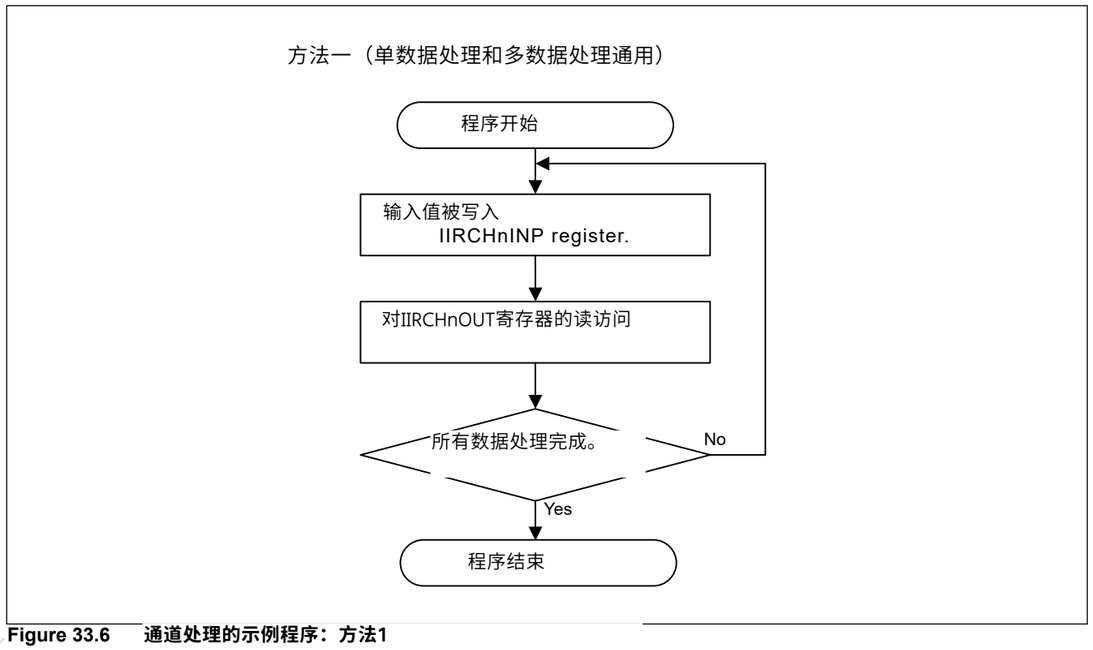


Figure 33.6 通道处理的示例程序：方法1

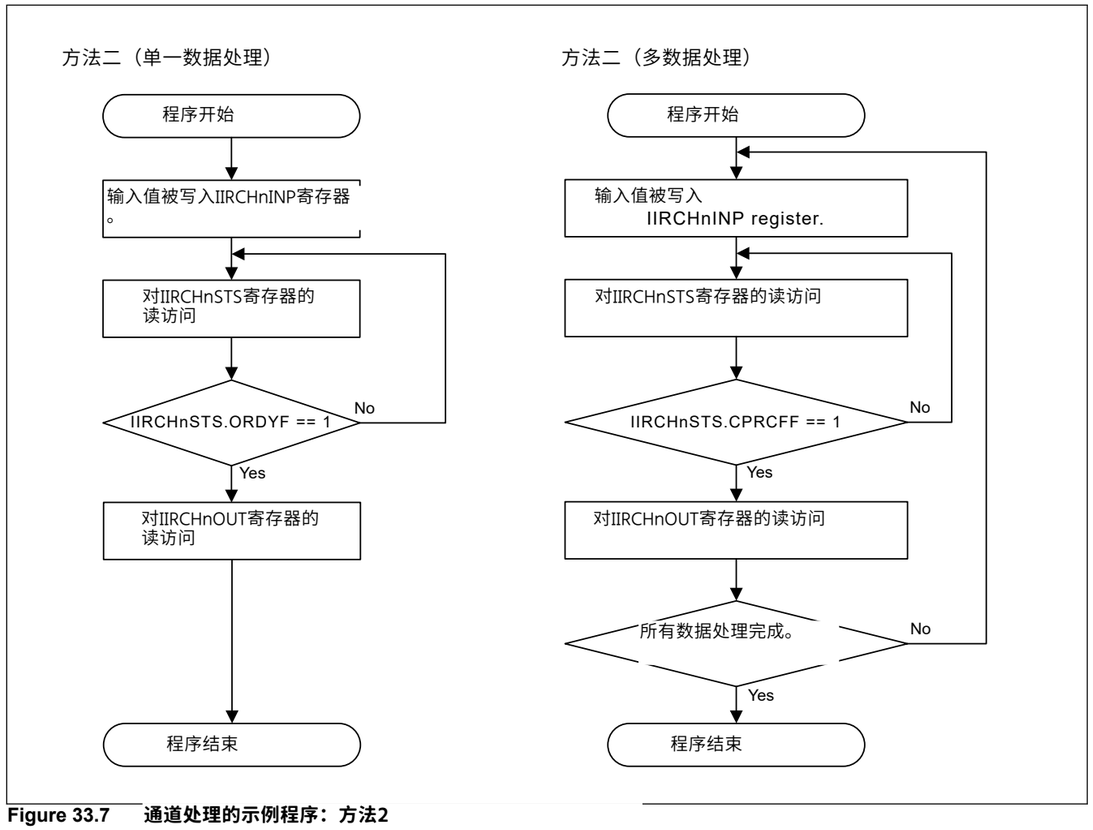
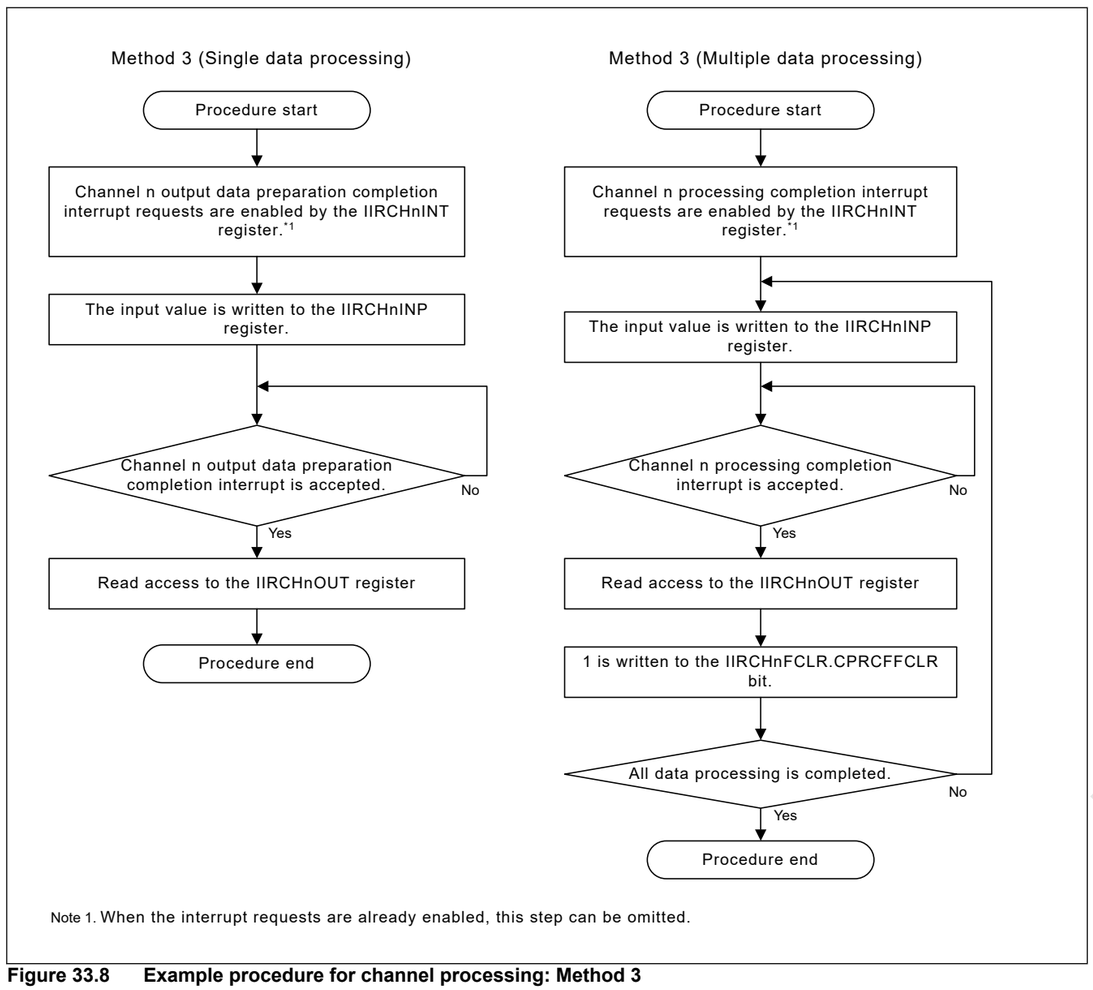


Figure 33.7 通道处理的示例程序：方法2



Note 1. When the interrupt requests are already enabled, this step can be omitted.

Figure 33.8 Example procedure for channel processing: Method 3

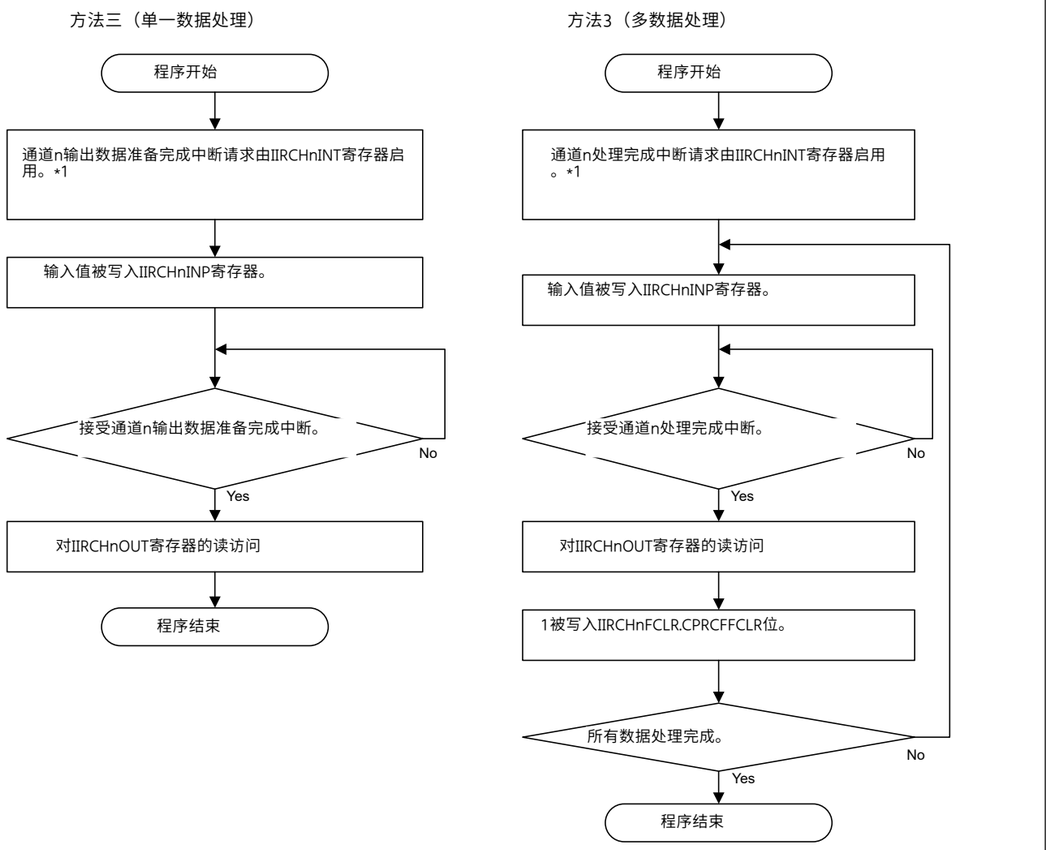
33.3.5.3 Procedure for Intentionally Detecting ECC Errors

This section describes the procedure for intentionally detecting ECC errors (ECC 1-bit error, ECC 2-bit error). To check the behavior of a software routine after an ECC error is detected, perform these procedures.

If the ECC error detection/correction function is disabled (IIRECCCNT.ECCMD = 0), any data can be written to the coefficient/delay data register without updating the ECC code when data is written to the coefficient/delay data register. Therefore, the data error occurrence status of the coefficient/delay data storage area can be reproduced by reversing an appropriate bit of the coefficient/delay data. After the corrupted data has been generated, a read access to the coefficient/delay data register is performed to detect an ECC 1-bit error or ECC 2-bit error in accordance with the number of reversed bits.

The following steps show an example procedure.

1. Perform the initial settings with the ECC error detection/correction function enabled (IIRECCCNT.ECCMD = 1).
2. Write any data to a coefficient/delay data register in any stage.
3. Disable the ECC error detection/correction function (IIRECCCNT.ECCMD = 0).
4. Write a value to detect an ECC 1-bit error or ECC 2-bit error to the address to which data is written in step 2.



注1.当中断请求已经使能时，此步骤可以省略。

Figure 33.8 通道处理的示例程序：方法3

33.3.5.3 有意检测ECC错误的过程

本节介绍有意检测ECC错误（ECC1位错误、ECC2位错误）的过程。要在检测到ECC错误后检查软件例程的行为，请执行以下过程。

如果禁用ECC错误检测校正功能（IIRECCCNT.ECCMD=0），则在将数据写入系数延迟数据寄存器时，可以将任何数据写入系数延迟数据寄存器而无需更新ECC代码。因此，可以通过反转系数延迟数据的适当位来再现系数延迟数据存储区的数据错误发生状态。在生成损坏数据后，对系数延迟数据寄存器执行读取访问，以根据反转的位数检测ECC1位错误或ECC2位错误。

以下步骤显示了一个示例过程。

1.在启用ECC错误检测校正功能(IIRECCCNT.ECCMD=1)的情况下执行初始设置。

2.在任何阶段将任何数据写入系数延迟数据寄存器。

3.禁用ECC错误检测校正功能（IIRECCCNT.ECCMD=0）。

4.将检测ECC1位错误或ECC2位错误的值写入步骤2中写入数据的地址。

Example: When 0x00000000 is written in step 2, writing 0x00000001 reproduces a state where a 1-bit error occurs in the coefficient/delay data and writing 0x00000003 reproduces a state where a 2-bit error occurs in the coefficient/delay data.

5. Enable the ECC error detection/correction function (IIRECCCNT.ECCMD = 1).
6. Read the data from the address to which data is written in steps 2 and 4.
   At this time, an ECC 1-bit error or ECC 2-bit error is detected depending on the value of the data written in steps 2 and 4.

33.4 Interrupt Sources

Table 33.8 shows a list of interrupt sources.

Table 33.8 Interrupt sources

Name	Interrupt source	Interrupt flag	Interrupt generation condition
IIRFA_ORDYn (n = 0 to 2)	Channel n output data preparation is completed.	IIRCHnSTS.ORDYF	IIRCHnSTS.ORDYF = 1 and IIRCHnINT.ORDYIE = 1
IIRFA_ORDY3 (m = 3 to 15)	Output data preparation is completed in any of channel m.	IIRCHmSTS.ORDYF	IIRCHmSTS.ORDYF = 1 and IIRCHmINT.ORDYIE = 1
IIRFA_CPRCFn (n = 0 to 2)	Channel n processing is completed.	IIRCHnSTS.CPRCFF	IIRCHnSTS.CPRCFF = 1 and IIRCHnINT.OPRCFIE = 1
IIRFA_CPRCF3 (m = 3 to 15)	Processing is completed in any of channel m.	IIRCHmSTS.CPRCFF	IIRCHmSTS.CPRCFF = 1 and IIRCHmINT.CPRCFIE = 1
IIRFA_ERR (x = 0 to 15)	An operation error has occurred in any of channel.	IIRCHxSTS.CERRF	IIRCHxSTS.CERRF = 1 and IIRCHxINT.CERRIE = 1
	An ECC 1-bit error has occurred.	IIRECCEF.ESEF	IIRECCEF.ESEF = 1 and IIRECCINT.ESEIE = 1
	An ECC 2-bit error has occurred.	IIRECCEF.EDEF	IIRECCEF.EDEF = 1 and IIRECCINT.EDEIE = 1

IIRFA_ORDY3 is an output data preparation completion interrupt of wire-ORed channels 3 to 15. To check the channel in which an interrupt is generated, see section 33.2.1.3. IIRORDYF : Output Data Preparation Completion Flag Register.

IIRFA_CPRCF3 is an processing completion interrupt of wire-ORed channels 3 to 15. To check the channel in which an interrupt is generated, see section 33.2.1.2. IIRCPRCFF : Channel Processing Completion Flag Register.

IIRFA_ERR is a wire-ORed interrupt for the all channel of operation error, ECC 1-bit error, and ECC 2-bit error. To check which error interrupts are generated, see section 33.2.1.4. IIRCERRF : Operation Error Flag Register, and section 33.2.1.8. IIRECCEF : ECC Error Flag Register.

示例：当在步骤2中写入0x00000000时，写入0x00000001会再现在系数延迟数据中出现1位错误的状态，写入0x00000003会再现在系数延迟数据中出现2位错误的状态。

5.启用ECC错误检测校正功能（IIRECCCNT.ECCMD=1）。

6.从步骤2和4中写入数据的地址读取数据。
此时，根据在步骤2和4中写入的数据值检测ECC1位错误或ECC2位错误。

33.4 中断源

表33.8显示了中断源列表。

Table 33.8 中断源

Name	中断源	中断标志	中断产生条件
IIRFA_ORDYn (n = 0 to 2)	通道n输出数据准备完成。	IIRCHnSTS.ORDYF	IIRCHnSTS.ORDYF = 1 and IIRCHnINT.ORDYIE = 1
IIRFA_ORDY3 (m = 3 to 15)	在任何通道m中完成输出数据准备。	IIRCHmSTS.ORDYF	IIRCHmSTS.ORDYF = 1 and IIRCHmINT.ORDYIE = 1
IIRFA_CPRCFn (n = 0 to 2)	通道n处理完成。	IIRCHnSTS.CPRCFF	IIRCHnSTS.CPRCFF = 1 and IIRCHnINT.OPRCFIE = 1
IIRFA_CPRCF3 (m = 3 to 15)	处理在任何通道m中完成。	IIRCHmSTS.CPRCFF	IIRCHmSTS.CPRCFF = 1 and IIRCHmINT.CPRCFIE = 1
IIRFA_ERR (x = 0 to 15)	任一通道发生操作错误。	IIRCHxSTS.CERRF	IIRCHxSTS.CERRF = 1 and IIRCHxINT.CERRIE = 1
	发生ECC1位错误。	IIRECCEF.ESEF	IIRECCEF.ESEF = 1 and IIRECCINT.ESEIE = 1
	发生ECC2位错误。	IIRECCEF.EDEF	IIRECCEF.EDEF = 1 and IIRECCINT.EDEIE = 1

IIRFA_ORDY3是线或通道3到15的输出数据准备完成中断。要检查产生中断的通道，请参见第33.2.1.3节。IIRORDYF：输出数据准备完成标志寄存器。

IIRFA_CPRCF3是线或通道3到15的处理完成中断。要检查产生中断的通道，请参见第33.2.1.2节。IIRCPRCFF：通道处理完成标志寄存器。

IIRFA_ERR是针对所有通道的操作错误、ECC1位错误和ECC2位错误的线或中断。要检查生成了哪些错误中断，请参阅第33.2.1.4节。IIRCERRF：操作错误标志寄存器，以及第33.2.1.8节。IIRECCEF：ECC错误标志寄存器。

34. Boundary Scan

34.1 Overview

The boundary scan function provides a serial I/O interface based on the JTAG (Joint Test Action Group), IEEE Std.1149.1, and IEEE Standard Test Access Port and Boundary Scan Architecture. Table 34.1 lists the boundary scan specifications, Figure 34.1 shows a block diagram, and Table 34.2 lists the I/O pins.

Table 34.1 Boundary scan specifications

Parameter	Specifications
Execution condition	Boundary scan must be executed when the RES pin is driven low.
Test modes	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode

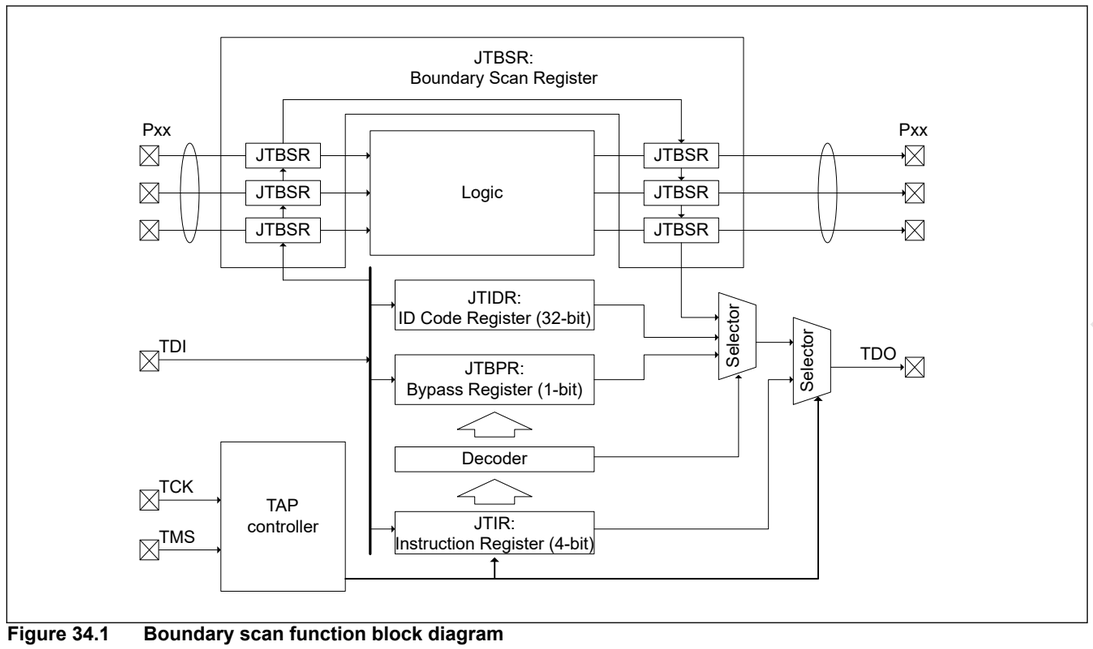


Figure 34.1 Boundary scan function block diagram

Table 34.2 Boundary scan I/O pins

Pin name	I/O	Description
TCK	Input	Test clock input pin Clock signal for boundary scan. The input clock duty cycle is 50% when the boundary scan function is used.
TMS	Input	Test mode select pin
TDI	Input	Test data input pin
TDO	Output	Test data output pin

Note: This device does not support the TRST pin for the JTAG interface.

34.2 Register Descriptions

Table 34.3 lists the boundary scan registers.

34. 边界扫描

34.1 Overview

边界扫描功能提供基于JTAG（联合测试行动组）、IEEEStd.1149.1和IEEE标准测试访问端口和边界扫描架构的串行IO接口。表34.1列出了边界扫描规范，图34.1显示了框图，表34.2列出了IO引脚。

Table 34.1 边界扫描规格

Parameter	Specifications
执行条件	当RES引脚驱动为低电平时，必须执行边界扫描。
测试模式	• 旁路模式 • EXTEST mode • SAMPLE/PRELOAD mode • 钳位模式 • HIGHZ mode • IDCODE mode

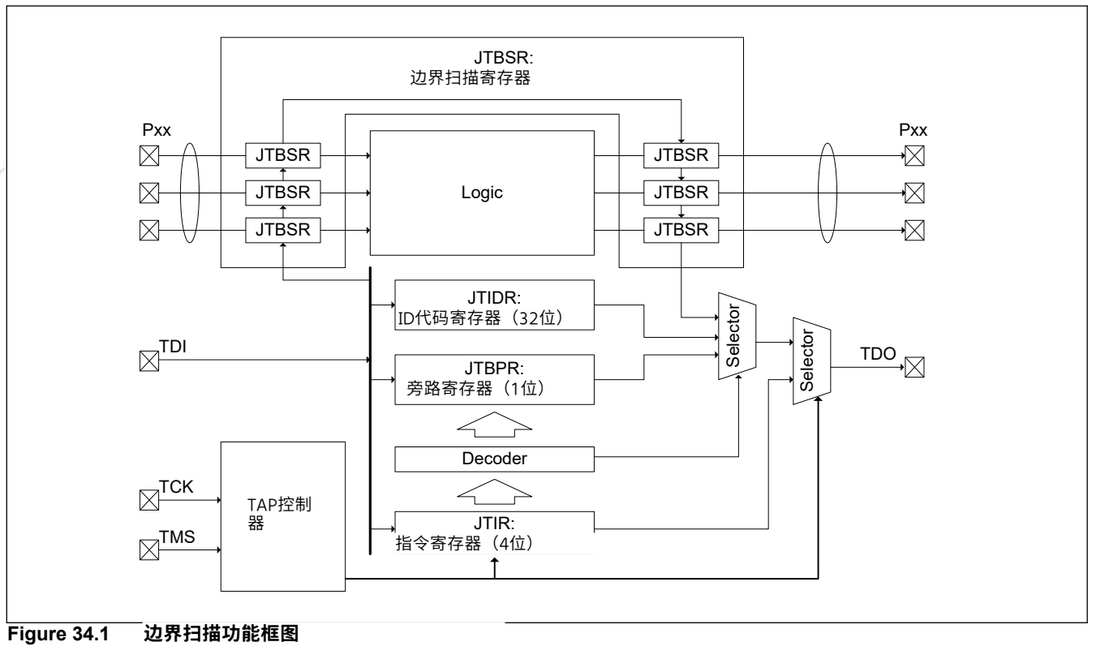


Figure 34.1 边界扫描功能框图

Table 34.2 边界扫描IO引脚

引脚名称	I/O	Description
TCK	Input	测试时钟输入引脚 边界扫描的时钟信号。使用边界扫描功能时，输入时钟占空比为50%。
TMS	Input	测试模式选择引脚
TDI	Input	测试数据输入引脚
TDO	Output	测试数据输出引脚

Note: 该器件不支持JTAG接口的TRST引脚。

34.2 注册说明

表34.3列出了边界扫描寄存器。

Table 34.3 Boundary scan registers

Register name	Symbol	Value after reset
Instruction Register	JTIR	0xE
ID Code Register	JTIDR	0x0841_F447
Bypass Register	JTBPR	Undefined
Boundary Scan Register	JTBSR	Undefined

Usage notes for the boundary scan registers:

- Instructions can be input to the Instruction Register (JTIR) through the TDI pin by serial transfer.
- The Bypass Register (JTBPR), which is a 1-bit register, is connected between the TDI and TDO pins in BYPASS mode.
- The Boundary Scan Register (JTBSR), which is configured according to the BSDL description, is connected between the TDI and TDO pins when test data is being shifted in.

Table 34.4 shows the availability of serial transfer for the registers.

Table 34.4 Serial transfer for registers

Register name	Serial input	Serial output
Instruction Register (JTIR)	Available	Available
ID Code Register (JTIDR)	Available	Available
Bypass Register (JTBPR)	Available	Available
Boundary Scan Register (JTBSR)	Available	Available

34.2.1 JTIR : Instruction Register

Bit	Symbol	Function	R/W
3:0	TS[3:0]	Test Bit Set The command configuration for these bits	—

TS[3:0]	Instruction
0x0	EXTEST
0x1	SAMPLE/PRELOAD
0x3	IDCODE (Renesas code)
0x5	CLAMP
0x6	HIGHZ
0xF	BYPASS
Others	Reserved

JTAG instructions can be transferred to the JTIR register by serial input from the TDI pin. The JTIR register is initialized when a power-on reset occurs, or when the TAP controller is in the Test-Logic-Reset state.

34.2.2 JTIDR : ID Code Register

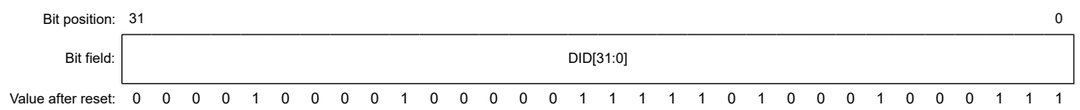


Table 34.3 边界扫描寄存器

注册名称	Symbol	重置后的值
指令寄存器	JTIR	0xE
ID代码寄存器	JTIDR	0x0841_F447
绕过寄存器	JTBPR	Undefined
边界扫描寄存器	JTBSR	Undefined

边界扫描寄存器的使用说明：

●指令可以通过串行传输的方式通过TDI引脚输入指令寄存器（JTIR）。

●BypassRegister(JTBPR)是一个1位寄存器，在BYPASS模式下连接在TDI和TDO引脚之间。

●根据BSDL描述配置的边界扫描寄存器(JTBSR)在测试数据移入时连接在TDI和TDO引脚之间。

表34.4显示了寄存器串行传输的可用性。

Table 34.4 寄存器的串行传输

注册名称	串行输入	串行输出
指令寄存器(JTIR)	Available	Available
ID代码寄存器(JTIDR)	Available	Available
旁路寄存器(JTBPR)	Available	Available
边界扫描寄存器(JTBSR)	Available	Available

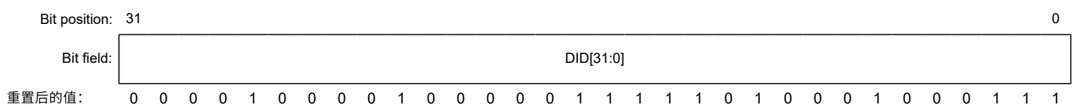
34.2.1 JTIR:指令寄存器

Bit	Symbol	Function	R/W
3:0	TS[3:0]	测试位组 这些位的命令配置	—

TS[3:0]	Instruction
0x0	EXTEST
0x1	SAMPLE/PRELOAD
0x3	IDCODE (Renesas code)
0x5	CLAMP
0x6	HIGHZ
0xF	BYPASS
Others	Reserved

JTAG指令可以通过TDI引脚的串行输入传输到JTIR寄存器。当发生上电复位或TAP控制器处于Test-Logic-Reset状态时，JTIR寄存器被初始化。

34.2.2 JTIDR:ID代码寄存器



Bit	Symbol	Function	R/W
31:0	DID[31:0]	Device ID These bits store the fixed value that indicates the device IDCODE (0x0841_F447).	—

The JTIDR register data is output from the TDO pin when the IDCODE instruction is executed. After a reset release, the DID[31:0] of JTIDR changes into the Arm® debug code. See the *Arm® CoreSight™ SoC-400 Technical Reference Manual* (ARM DDI 0480F).

34.2.3 JTBPR : Bypass Register

The JTBPR register is a 1-bit register and is connected between the TDI and TDO pins when the JTIR register is set to BYPASS mode. The JTBPR register cannot be read from or written to by the CPU.

34.2.4 JTBSR : Boundary Scan Register

The JTBSR register is a shift register for controlling the external input and output pins of this device, and is distributed across the pads. To apply the JTBSR register in boundary-scan testing, issue the EXTEST, SAMPLE/PRELOAD, CLAMP, and HIGHZ instructions. The BSDL file describes the associations between the JTBSR register bits and the pins of this device. The value after reset is undefined.

34.3 Operation

During a reset, the JTAG ports, TCK, TMS, TDI, and TDO, are assigned as default pin functions. The TCK, TMS, and TDI pins are pulled up by the pull-up resistors. Boundary scan testing can be executed after the setup time elapses when POR is negated and RES is driven low.

34.3.1 TAP Controller

Figure 34.2 shows the state transition diagram of the TAP controller. All transitions are controlled by the TMS signal.

Bit	Symbol	Function	R/W
31:0	DID[31:0]	设备ID 这些位存储指示设备IDCODE(0x0841_F447)的固定值。	—

执行IDCODE指令时，从TDO引脚输出JTIDR寄存器数据。复位释放后，
JTIDR的DID[31:0]更改为Arm®调试代码。请参阅Arm®CoreSight SoC-400技术参考手册(ARMDDI0480F)。

34.2.3 JTBPR:旁路寄存器

JTBPR寄存器是一个1位寄存器，当JTIR寄存器设置为
旁路模式。CPU无法读取或写入JTBPR寄存器。

34.2.4 JTBSR:边界扫描寄存器

JTBSR寄存器是一个移位寄存器，用于控制该器件的外部输入和输出引脚，分布在各个焊盘上。要在边界扫描测试中应用JTBSR寄存器，请发出EXTEST、SAMPLEPRELOAD、CLAMP和HIGHZ指令。BSDL文件描述了JTBSR寄存器位和该器件引脚之间的关联。复位后的值未定义。

34.3 Operation

在复位期间，JTAG端口、TCK、TMS、TDI和TDO被分配为默认引脚功能。TCK、TMS和TDI引脚由上拉电阻上拉。当POR被否定并且RES被驱动为低电平时，可以在设置时间过去后执行边界扫描测试。

34.3.1 水龙头控制器

图34.2显示了TAP控制器的状态转换图。所有转换都由TMS信号控制。

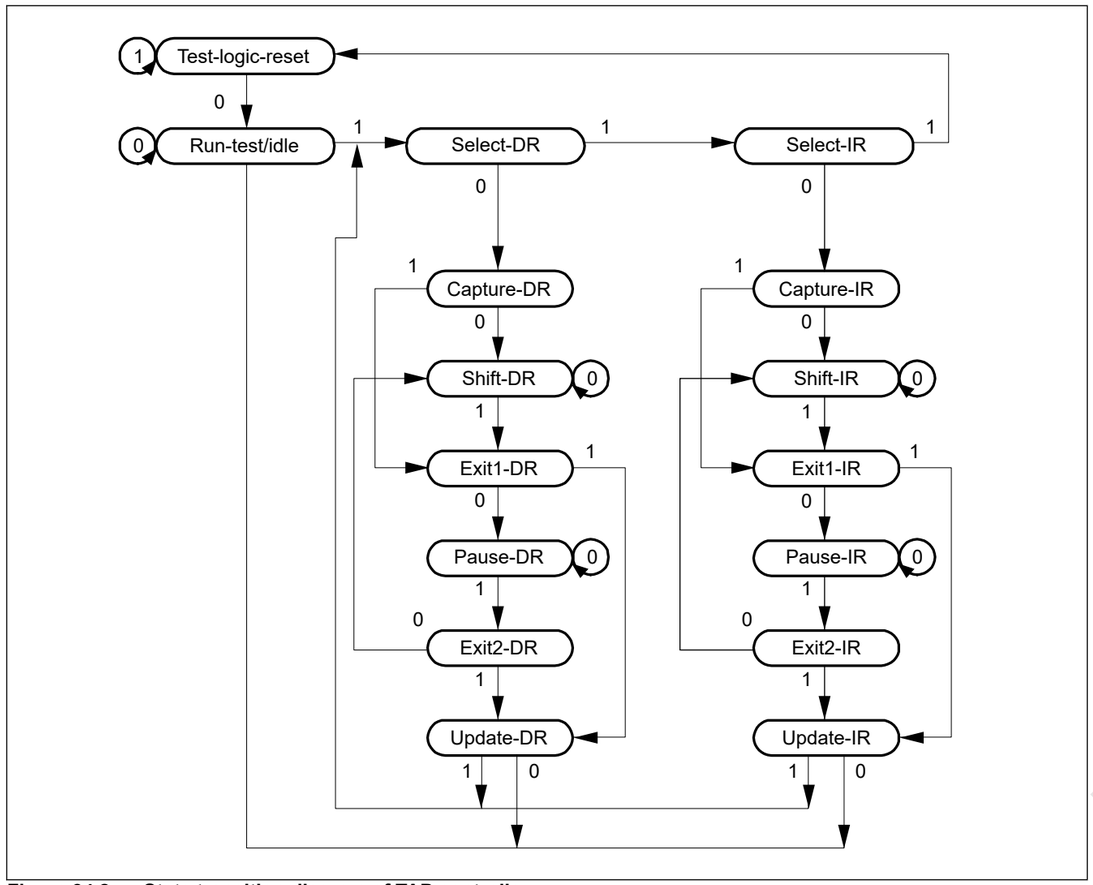


Figure 34.2 State transition diagram of TAP controller

34.3.2 Commands

(1) BYPASS

The BYPASS instruction drives the Bypass Register (JTBPR). This instruction shortens the shift path, facilitating the transfer of serial data to other LSIs on a printed circuit board at higher speeds. While this instruction is being executed, the test circuit has no effect on the system circuits.

The JTBPR register is connected between the TDI and TDO pins. Bypass operation is initiated from the Shift-DR operation. The TDO is low in the first clock cycle in the Shift-DR state. In the subsequent clock cycles, values input to the TDI pin are output from the TDO pin.

(2) EXTEST

The EXTEST instruction is used to test external circuits when this device is installed on the printed circuit board. If this instruction is executed, output pins are used to output test data (specified in the SAMPLE/PRELOAD instruction) from the Boundary Scan Register (JTBSR) to the other devices, and input pins are used to input the test result.

(3) SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction is used to input data from the internal circuits of this device to the JTBSR register, output data from the scan path, and reload the data to the scan path. While this instruction is executed, input signals are directly input to this device and output signals are also directly output to the external circuits. This device system circuit is not affected by this instruction.

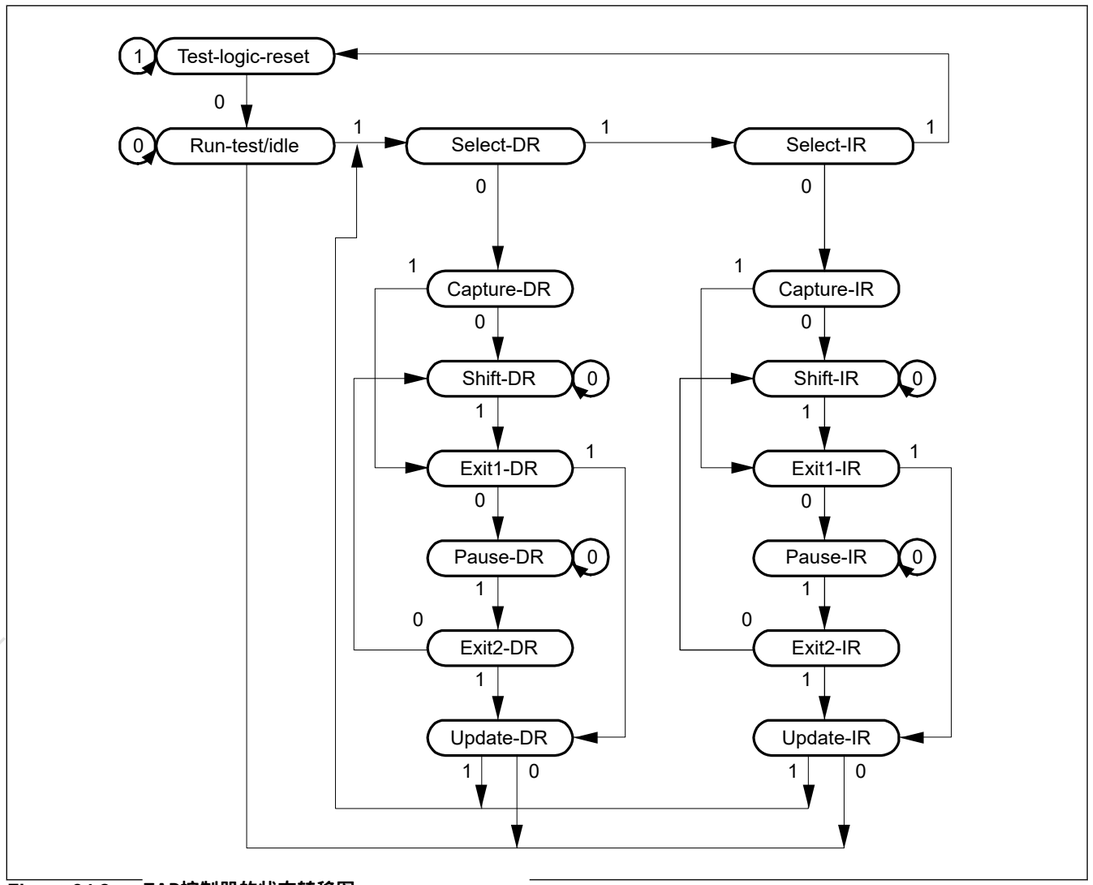


Figure 34.2 TAP控制器的状态转移图

34.3.2 Commands

(1) BYPASS

BYPASS指令驱动旁路寄存器(JTBPR)。该指令缩短了移位路径，便于将串行数据以更高的速度传输到印刷电路板上的其他LSI。在执行该指令时，测试电路对系统电路没有影响。

JTBPR寄存器连接在TDI和TDO引脚之间。旁路操作从Shift-DR操作开始。TDO在Shift-DR状态的第一个时钟周期内为低电平。在随后的时钟周期中，输入到TDI引脚的值从TDO引脚输出。

(2) EXTEST

当本设备安装在印刷电路板上时，EXTEST指令用于测试外部电路。如果执行该指令，输出引脚用于将测试数据（在SAMPLEPRELOAD指令中指定）从边界扫描寄存器(JTBSR)输出到其他设备，输入引脚用于输入测试结果。

(3) SAMPLE/PRELOAD

SAMPLEPRELOAD指令用于将数据从本器件内部电路输入到JTBSR寄存器，从扫描路径输出数据，并将数据重新加载到扫描路径。执行该指令时，输入信号直接输入到本设备，输出信号也直接输出到外部电路。本设备系统电路不受本指令影响。

In SAMPLE operation, the JTBSR register latches a snapshot of the data transferred from the input pins to the internal circuit or data transferred from the internal circuit to the output pins. The latched data is read from the scan path. The JTBSR register latches the data snapshot on the rising edge of the TCK pin in the Capture-DR state. The data snapshot is only transferred from the internal circuit to the output pins during a reset.

In PRELOAD operation, the initial value is written from the scan path to the parallel output latch of the JTBSR register prior to the EXTEST instruction execution. If EXTEST is executed without executing this PRELOAD operation, undefined values are output from the beginning to the end (transfer to the output latch) of the EXTEST sequence. (In the EXTEST instruction, output parallel latches are always output to the output pins.)

(4) IDCODE

When the IDCODE instruction is selected, the ID Code Register (JTIDR) value is output to the TDO pin in the Shift-DR state of the TAP controller. In this case, the JTIDR register value is output LSB-first. During this instruction execution, the test circuit does not affect the system circuit.

(5) CLAMP

When the CLAMP instruction is selected, output pins output the JTBSR register value that was specified in the SAMPLE/PRELOAD instruction in advance. While the CLAMP instruction is selected, the status of the JTBSR register is maintained regardless of the TAP controller state.

The JTBPR register is connected between the TDI and TDO pins, leading to the same operation as when the BYPASS instruction is selected.

(6) HIGHZ

When the HIGHZ instruction is selected, all output pins enter high-impedance state. While the HIGHZ instruction is selected, the JTBSR register is maintained regardless of the state of the TAP controller.

The JTBPR register is connected between the TDI and TDO pins, leading to the same operation as when the BYPASS instruction is selected.

34.4 Usage Notes

The boundary scan function is subject to the following constraints:

- The boundary scan must be executed when the RES pin is driven low
- Serial data input/output is in LSB order, as shown in Figure 34.3

在SAMPLE操作中，JTBSR寄存器锁存从输入引脚传输到内部电路的数据或从内部电路传输到输出引脚的数据的快照。从扫描路径读取锁存的数据。在Capture-DR状态下，JTBSR寄存器在TCK引脚的上升沿锁存数据快照。数据快照仅在复位期间从内部电路传输到输出引脚。

在PRELOAD操作中，在执行EXTEST指令之前，将初始值从扫描路径写入JTBSR寄存器的并行输出锁存器。如果在不执行此PRELOAD操作的情况下执行EXTEST，则从EXTEST序列的开头到结尾（传输到输出锁存器）输出未定义的值。（在EXTEST指令中，输出并行锁存器始终输出到输出引脚。）

(4) IDCODE

WhentheIDCODEinstructionisselected theIDCodeRegister(JTIDR)valueisoutputtotheTDOpinintheShift-DRstateoftheTAPcontroller.在这种情况下，JTIDR寄存器值首先输出LSB。在该指令执行期间，测试电路不影响系统电路。

(5) CLAMP

选择夹具指令时，输出引脚输出样品中指定的JTBSR寄存器值
预先PRELOAD指令。选择CLAMP指令时，无论TAP控制器状态如何，都将保持JTBSR寄存器的状态。

JTBPR寄存器连接在TDI和TDO引脚之间，导致与选择BYPASS指令时相同的操作。

(6) HIGHZ

选择Highz指令时，所有输出引脚都输入高阻抗状态。选择HIGHZ指令时，无论TAP控制器的状态如何，都会保持JTBSR寄存器。

JTBPR寄存器连接在TDI和TDO引脚之间，导致与选择BYPASS指令时相同的操作。

34.4 使用说明

边界扫描函数受以下约束：

- RES引脚拉低时必须执行边界扫描
- 串行数据输入输出为LSB顺序，如图34.3所示

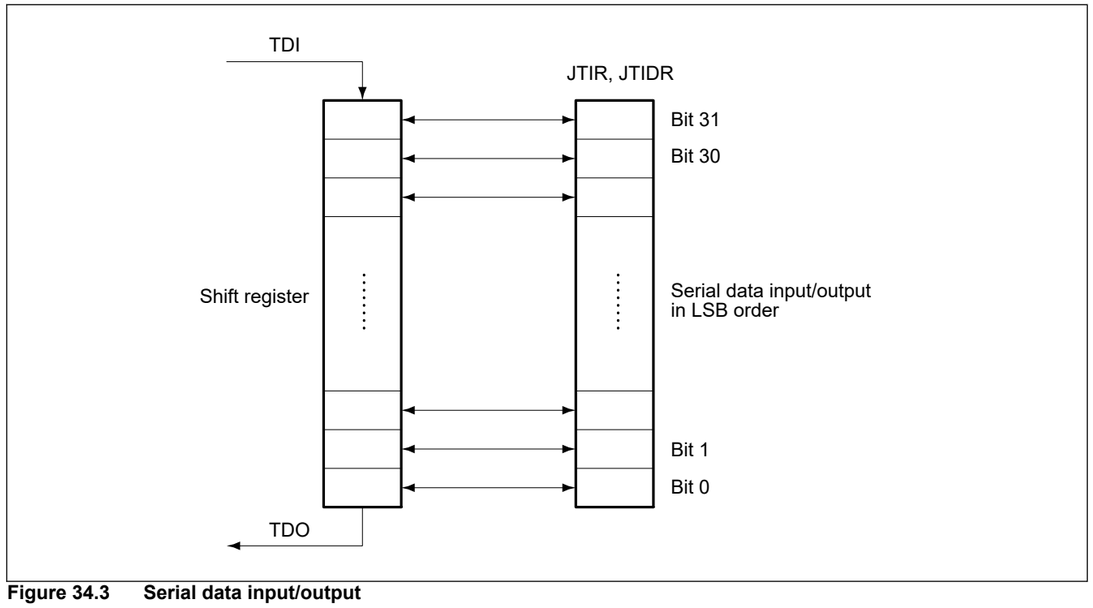


Figure 34.3 Serial data input/output

The following pins cannot be boundary-scanned:

- Power supply pins (VCC, VCL, VSS, AVCC0, AVSS0)
- Analog reference pins (AVREFH0, AVREFL0)
- Clock pins (EXTAL, XTAL)
- Reset pin (RES)
- The boundary-scan pins (TCK, TMS, TDI, and TDO).

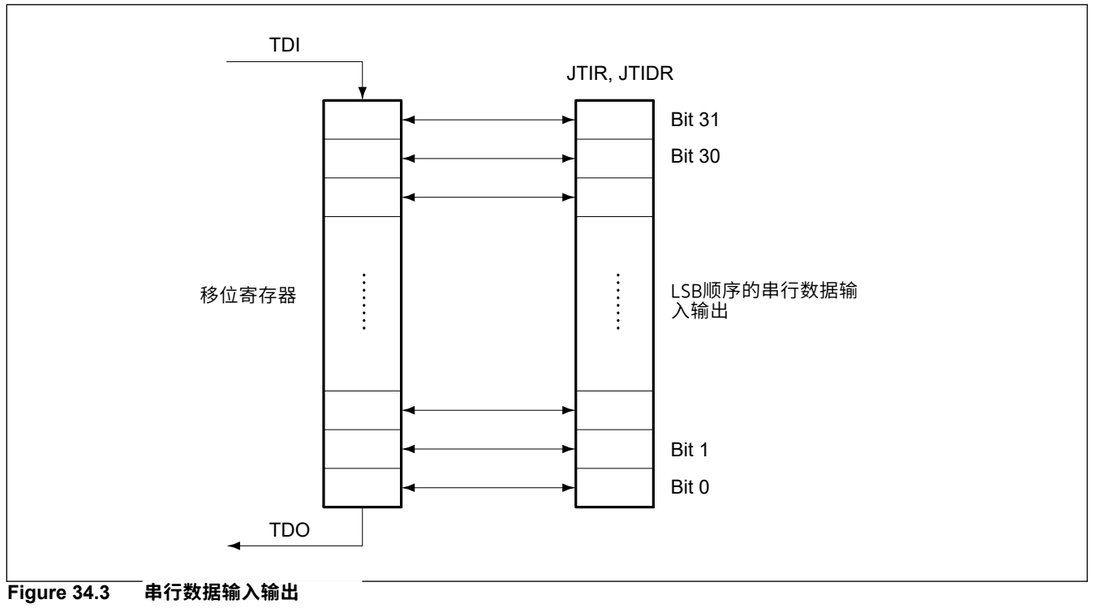


Figure 34.3 串行数据输入输出

以下引脚不能进行边界扫描：

●电源引脚（VCC、VCL、VSS、AVCC0、AVSS0）

●模拟参考引脚（AVREFH0、AREFL0）

●时钟引脚（EXTAL、XTAL）

●复位引脚（RES）

●边界扫描引脚（TCK、TMS、TDI和TDO）。

35. Secure Cryptographic Engine (SCE5)

This is the SCE5_B version of the SCE5 peripheral module.

SCE5_B is referred to as SCE5 in this chapter.

35.1 Overview

The Secure Cryptographic Engine (SCE5) consists of the access management circuit, encryption engine, and random number generation circuit. In combination with the SCE5 library, the SCE5 can prevent eavesdropping (to maintain confidentiality), falsification of information (to ensuret integrity), and impersonation (to verify authenticity).

Because key information required for encryption and decryption is stored only in the SCE5 and all accesses from the outside can be blocked, SCE5 enables building a more robust security system.

Table 35.1 lists the SCE5 specifications. Figure 35.1 shows the SCE5 block diagram.

Table 35.1 SCE5 specifications

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE5 due to a tampered program or CPU runaway, this circuit blocks all subsequent accesses and stops data output from the SCE5
Encryption engine	AES: Compliant with NIST FIPS PUB 197 • Key length: 128 or 256 bits • Data block size: 128 bits • Encryption usage modes ECB, CBC, CTR: Compliant with NIST SP 800-38A CMAC: Compliant with NIST SP 800-38B GCM: Compliant with NIST SP 800-38D XTS: Compliant with NIST SP 800-38E GCTR • Throughput for 128-bit data 44 PCLKA cycles for 128-bit key 61 PCLKA cycles for 256-bit key*1 AES-GCM • AES-GCM is realized by combining AES-GCTR and GHASH. Key management • Wrapped keys are only valid within the SCE5
Random number generation	32-bit true random number generation circuit
Hardware Unique Key	• A read-only, 128-bit Hardware Unique Key (HUK). • Key derivation functions (KDFs) combine the Hardware Unique Key with the key generation information. The derived keys implement the key wrapping for user key secure storage. • The HUK uniqueness prevents the illicit cloning and copying of keys to another MCU of the MCU group. • The HUK itself is stored in wrapped (encrypted, non-plain) format in an isolated memory area. Therefore it is protected from illicit access and copy.
Unique ID	• A read-only, 128-bit ID unique to an MCU (Unique ID) is accessible from the access management circuit. • Key derivation functions (KDFs) combine the Unique ID with the key generation information. Such derived keys are used to unwrap the HUK within the SCE boundary.
Low power consumption	Setting of the module-stop state is possible

Note 1. This does not include the overhead of calling SCE5 library functions.

35. 安全加密引擎(SCE5)

这是SCE5外设模块的SCE5_B版本。

SCE5_B在本章中称为SCE5。

35.1 Overview

安全密码引擎（SCE5）由访问管理电路、加密引擎和随机数生成电路组成。结合SCE5库，SCE5可以防止窃听（以保持机密性）、伪造信息（以确保完整性）和假冒（以验证真实性）。

由于加密和解密所需的关键信息仅存储在SCE5中，并且可以阻止来自外部的所有访问，因此SCE5可以构建更强大的安全系统。

表35.1列出了SCE5规范。图35.1显示了SCE5框图。

Table 35.1 SCE5 specifications

Parameter	Specifications
访问控制	访问管理电路● 如果由于程序被篡改或CPU失控而导致对SCE5的非正常访问，该电路将阻止所有后续访问并停止从SCE5输出数据
加密引擎	AES：符合NISTFIPSPUB197● 密钥长度：128或256位 • 数据块大小：128位 • 加密使用模式 ECB、CBC、CTR：符合NISTSP800-38A CMAC：符合NISTSP800-38BGCM：符合NISTSP800-38DXTS：符合NISTSP800-38E GCTR • 128位数据的吞吐量128位密钥的4 4个PCLKA周期256位密钥的61个PCLKA周期*1 AES-GCM • AES-GCM是通过结合AES-GCTR和GHASH实现的。 密钥管理● 封装的密钥仅在SCE5内有效
随机数生成	32位真随机数产生电路
硬件唯一密钥	• 只读的128位硬件唯一密钥(HUK)。 • 密钥派生函数(KDF)将硬件唯一密钥与密钥生成信息相结合。派生密钥实现了用户密钥安全存储的密钥包装。 • HUK唯一性可防止将密钥非法克隆和复制到MCU组的另一个MCU。 • HUK本身以封装（加密，非纯）格式存储在隔离的内存区域中。因此，它受到保护，免受非法访问和复制。
唯一身份	• MCU唯一的只读128位ID（唯一ID）可从访问管理电路访问。 • 密钥派生函数(KDF)将唯一ID与密钥生成信息相结合。此类派生密钥用于在SCE边界内解开HUK。
低功耗	可以设置模块停止状态

注1.这不包括调用SCE5库函数的开销。

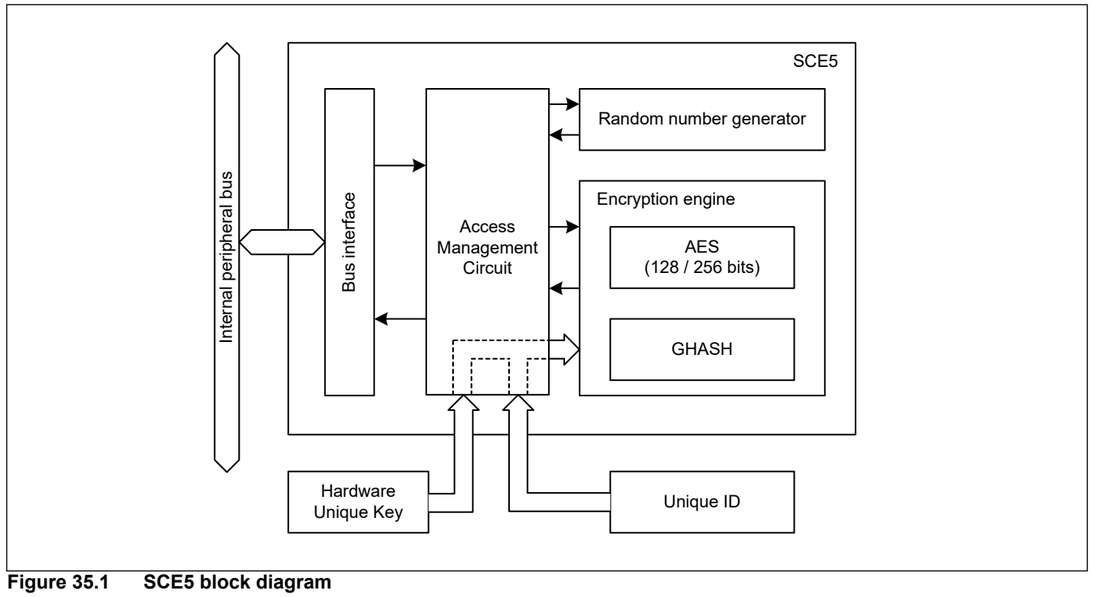


Figure 35.1 SCE5 block diagram

35.2 Operation

35.2.1 Encryption Engine

Figure 35.2 shows conceptual diagram of the encryption engine installed in the SCE5.

The encryption engine uses the key generation information, and converts the plaintext data to ciphertext or ciphertext data to plaintext through the hardware.

The encryption/decryption process can be completed without exposing the key data and the process's intermediate data to the outside of the SCE5.

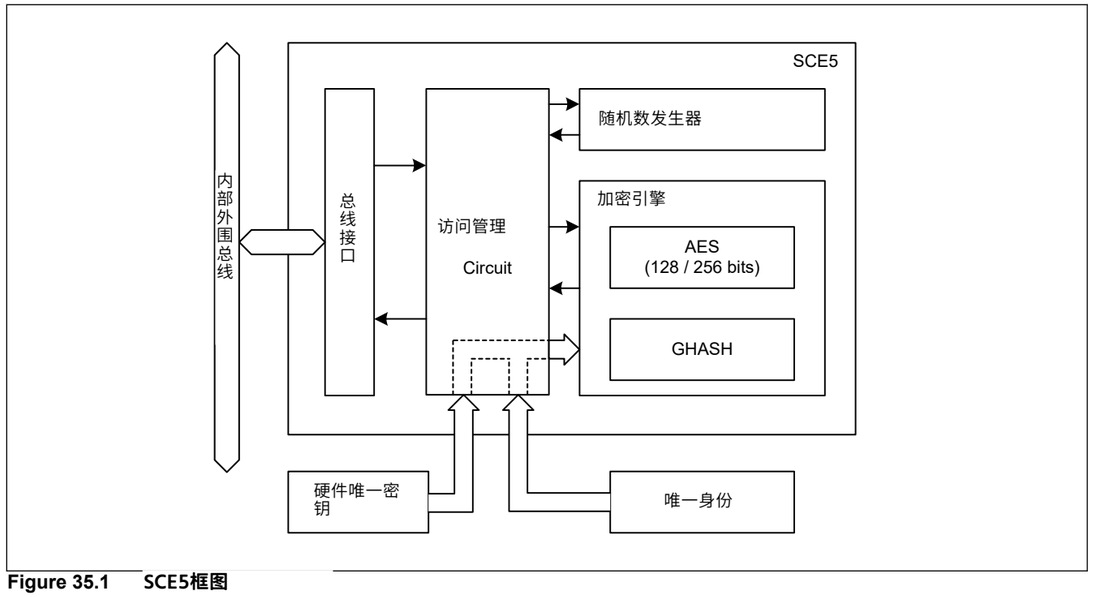


Figure 35.1 SCE5框图

35.2 Operation

35.2.1 加密引擎

图35.2显示了安装在SCE5中的加密引擎的概念图。

加密引擎使用密钥生成信息，通过硬件将明文数据转换为密文或将密文数据转换为明文。

加密解密过程可以在不将密钥数据和过程的中间数据暴露在SCE5外部的情况下完成。

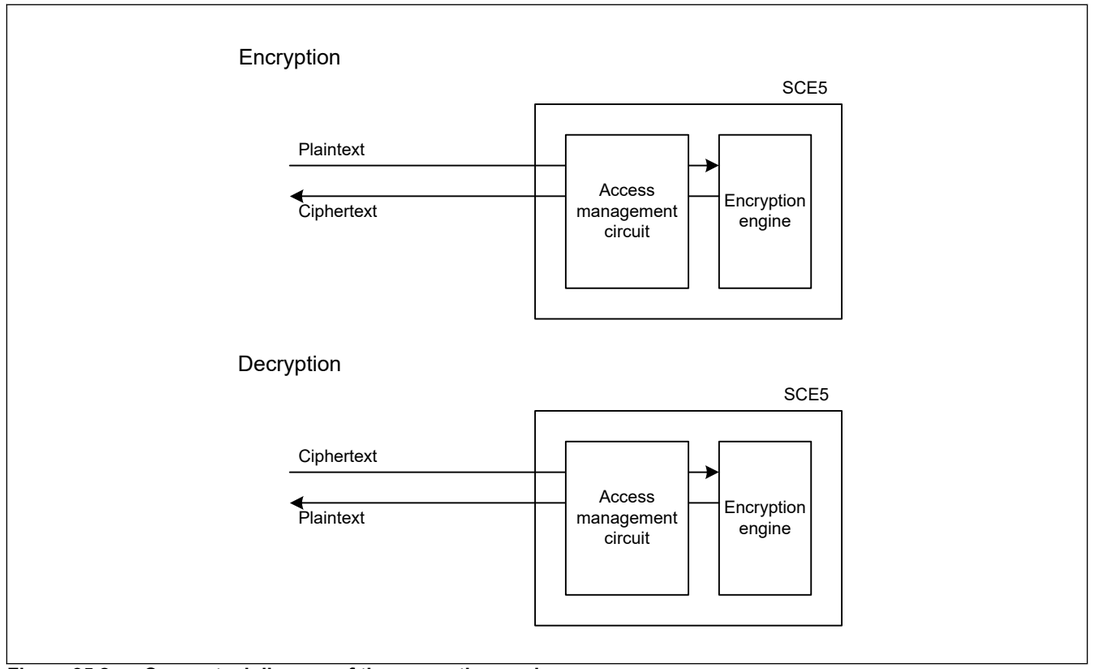


Figure 35.2 Conceptual diagram of the encryption engine

35.2.2 Encryption and Decryption

Follow the procedure below to encrypt and decrypt the data:

1. Enter the key generation information to the SCE5 and restore the key data.
2. Enter the target data to the SCE5. Plaintext data is converted to ciphertext and ciphertext data to plaintext.
3. Read the converted data.

The encryption engine has input and output buffers, and can perform encryption/decryption in parallel with data input/output.

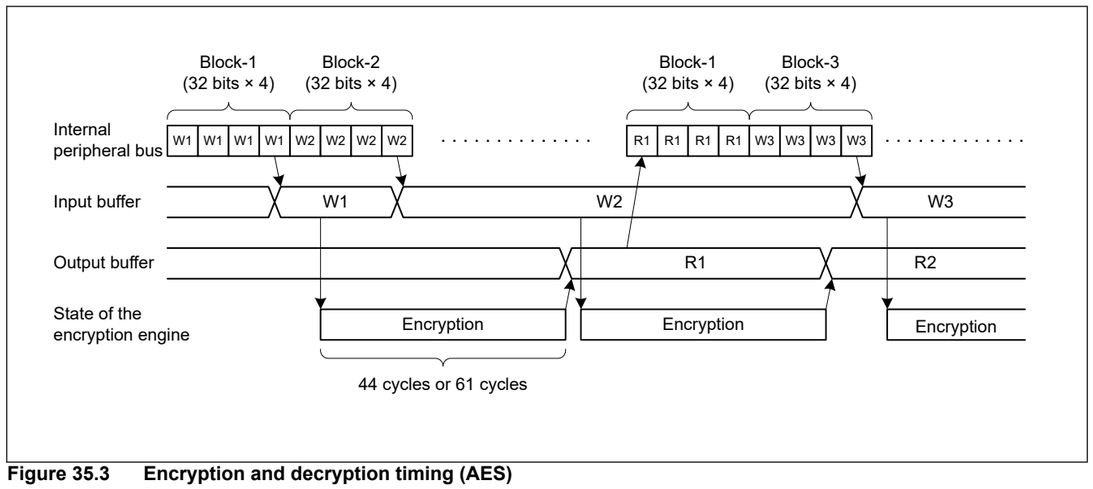


Figure 35.3 Encryption and decryption timing (AES)

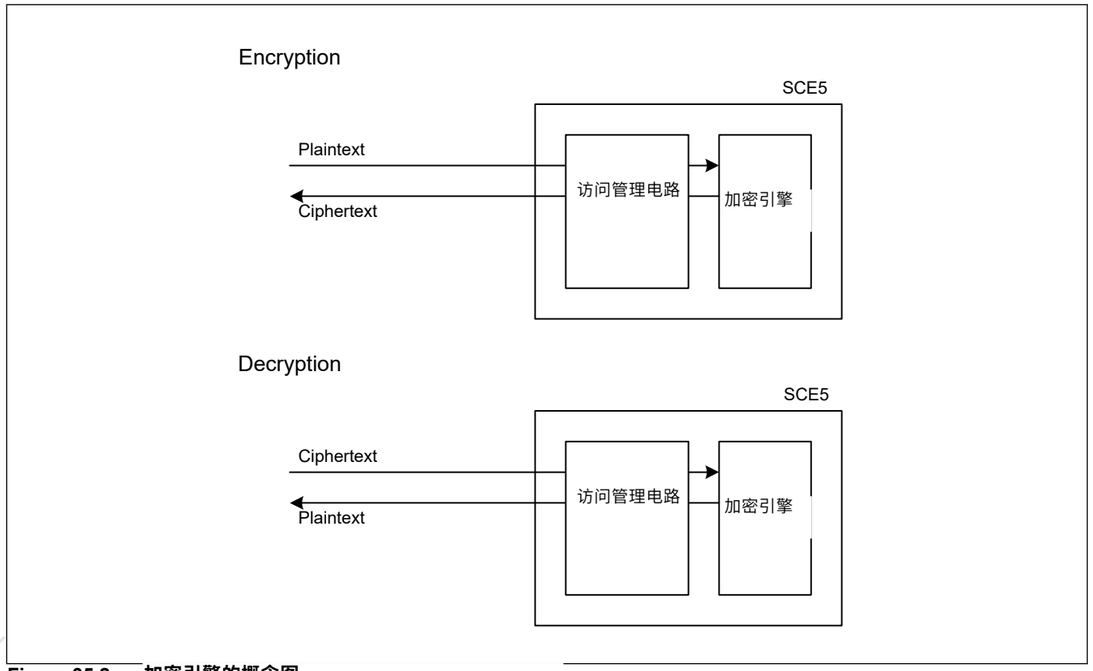


Figure 35.2 加密引擎的概念图

35.2.2 加密和解密

请按照以下步骤对数据进行加密和解密：

1.将密钥生成信息输入SCE5，恢复密钥数据。

2.将目标数据输入到SCE5。明文数据转换为密文，密文数据转换为明文。

3.读取转换后的数据。

加密引擎具有输入和输出缓冲区，可以与数据输入输出并行进行加密解密。

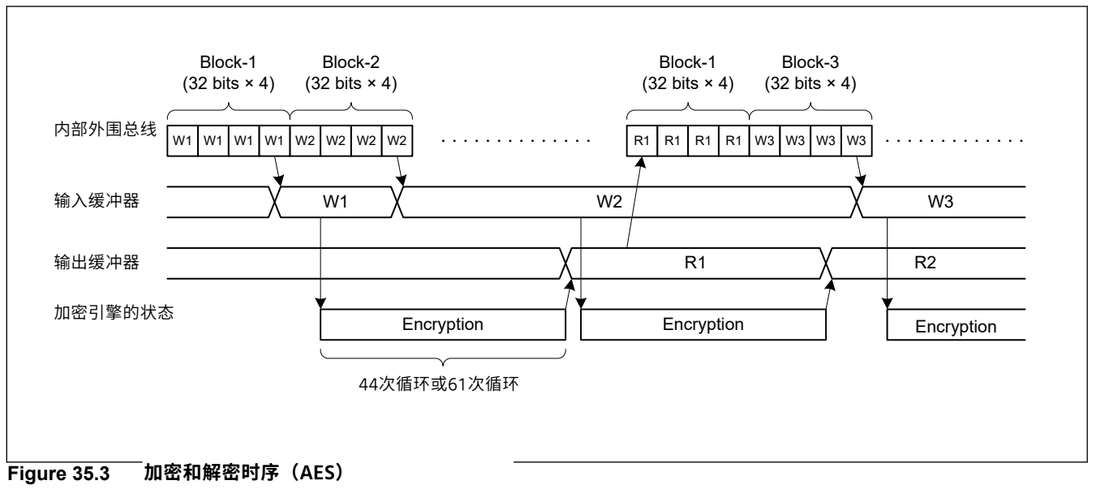


Figure 35.3 加密和解密时序（AES）

35.3 Usage Notes

35.3.1 Software Standby Mode

When the software standby mode is entered while the encryption engine is in process, proper processing cannot be resumed after the software standby mode is exited. The software standby mode should therefore be entered while the encryption engine is not running.

35.3.2 Module-Stop Function Setting

SCE5 operation can be disabled or enabled using Module Stop Control Register C (MSTPCRC). The SCE5 module is initially stopped after reset. Releasing the module-stop state enables access to the registers.

35.3 使用说明

35.3.1 软件待机模式

当加密引擎正在运行时进入软件待机模式时，退出软件待机模式后无法恢复正常处理。因此，应在加密引擎未运行时进入软件待机模式。

35.3.2 模块停止功能设置

可以使用模块停止控制寄存器C(MSTPCRC)禁用或启用SCE5操作。SCE5模块在复位后最初停止。释放模块停止状态可以访问寄存器。

36. 12-Bit A/D Converter (ADC)

This is the ADC_B version of the ADC peripheral module.

ADC_B is referred to as ADC in this chapter.

36.1 Overview

This MCU contains two units of 12-bit successive approximation A/D Converters. The A/D converter unit 0 (ADC0) can select up to 21 channels of analog inputs. The A/D converter unit 1 (ADC1) can select up to 17 channels of analog inputs. The temperature sensor, internal reference voltage, and D/A converters can be A/D-converted by A/D converter unit 0 or unit 1. A/D conversion data can be selected from 16-bit, 14-bit, 12-bit, and 10-bit length data formats.

The ADC has the following features.

- Resolution: 12-bit
- Fast conversion: Up to 6.25 Msps (0.16 µs per channel) (when A/D conversion clock ADCLK = 50 MHz)
- Input Channels: Up to 29 analog input channels
- Self-calibration Function
- Built-in Channel-dedicated sample-and-hold circuit (SH)
- Built-in Programmable Gain Amplifier (PGA)

Table 36.1 shows the ADC specifications, and Table 36.2 shows the ADC I/O pins.

Table 36.1 ADC specifications (1 of 2)

Item	Description
Number of units	Two units (unit 0 and unit 1)
Input channels	• Up to 29 analog input channels – A/D Converter Unit 0: Up to 21 analog input channels – A/D Converter Unit 1: Up to 17 analog input channels – 9 analog input channels are shared by A/D Converter Unit 0 and Unit 1
Extended Analog Function	Self-diagnosis, temperature sensor, internal reference voltage, D/A converter (DA0 to DA3)
A/D conversion method	Successive approximation method
Resolution of A/D converter	12-bits
Conversion time	0.16 µs per channel (when A/D conversion clock ADCLK = 50 MHz).
A/D conversion clock	The A/D conversion clock (ADCLK) can be set by selecting the clock source and the division ratio as follows: • The clock source: the peripheral module clock PCLKC*1, the peripheral module clock PCLKA*1, the GPT clock GPTCLK*1. • The division ratio: 1/2/3/4/5/6/7/8 A/D conversion clock (ADCLK) can operate between 25 MHz at a minimum and 60 MHz at a maximum.
A/D conversion data	• A/D conversion results are stored in data register or FIFO. • A/D conversion results are available in 16-, 14-, 12-, and 10-bit data formats.
Operating modes	• Single Scan mode – Assign any selected analog input or analog channel of the extended analog function to any scan group*2, and convert the selected analog input only once per scan group for A/D conversion. – By selecting the scan start conditions for each scan group individually, A/D conversion for each scan group can be started at different times. • Continuous Scan Mode – Assign any selected analog input or analog channel of the extended analog function to any scan group*2 and repeat A/D conversion in scan group units.
Conditions for A/D conversion start	• Software trigger (for simultaneous activation of scan group: max. 9 triggers) • Software trigger (for individual scan group activation: up to 9 triggers) • Trigger from Event Link Controller: 6 triggers • Triggers from GPT: 20 triggers • External trigger input: 2 triggers (ADTRGn input (n = 0, 1))

36. 12-Bit A/D Converter (ADC)

这是ADC外设模块的ADC_B版本。

ADC_B在本章中称为ADC。

36.1 Overview

该MCU包含两个12位逐次逼近模数转换器单元。AD转换器单元0(ADC0)最多可以选择21个模拟输入通道。AD转换器单元1(ADC1)最多可以选择17个模拟输入通道。温度传感器、内部参考电压和DA转换器可通过AD转换器单元0或单元1进行AD转换。AD转换数据可选择16位、14位、12位和10位长度数据格式。

ADC具有以下特性。

- Resolution: 12-bit
- ●快速转换：高达6.25Msps（每通道0.16µs）（当AD转换时钟ADCLK=50MHz时）
- ●输入通道：最多29个模拟输入通道
- Self-calibration Function
- Built-in Channel-dedicated sample-and-hold circuit (SH)
- ●内置可编程增益放大器（PGA）

表36.1显示了ADC规格，表36.2显示了ADCIO引脚。

Table 36.1 ADC规格(1of2)

Item	Description
单位数量	两个单元（单元0和单元1）
输入通道	• 多达29个模拟输入通道 – AD转换器单元0：最多21个模拟输入通道 – AD转换器单元1：最多17个模拟输入通道 – 9个模拟输入通道由AD转换器单元0和单元1共享
扩展模拟功能	自诊断、温度传感器、内部参考电压、DA转换器（DA0至DA3）
AD转换方式	逐次逼近法
AD转换器的分辨率	12-bits
转换时间	每通道0.16µs（当AD转换时钟ADCLK=50MHz时）。
AD转换时钟	AD转换时钟（ADCLK）可以通过选择时钟源和分频比来设置，如下所示：● 时钟源：外设模块时钟PCLKC*1、外设模块时钟PCLKA*1、 GPT clock GPTCLK*1. • 分频比：12345678 D转换时钟(ADCLK)可以在最小25MHz和最大60MHz之间运行。
AD转换数据	• AD转换结果存储在数据寄存器或FIFO中。 • AD转换结果以16、14、12和10位数据格式提供。
操作模式	• 单次扫描模式 – 将任何选择的模拟输入或扩展模拟功能的模拟通道分配到任何扫描组*2，并且每个扫描组仅将选择的模拟输入转换一次以进行AD转换。 – 通过单独选择每个扫描组的扫描开始条件，可以在不同的时间开始每个扫描组的AD转换。 • 连续扫描模式 – 将任何选择的模拟输入或扩展模拟功能的模拟通道分配给任何扫描组*2并以扫描组为单位重复AD转换。
AD转换开始的条件	• 软件触发（用于同时激活扫描组：最多9个触发） • 软件触发（用于单个扫描组激活：最多9个触发） • 来自事件链接控制器的触发器：6个触发器 • GPT触发器：20个触发器 • 外部触发输入：2个触发（ADTRGn输入(n=0 1)）

Table 36.1 ADC specifications (2 of 2)

Item	Description
Functions	● Virtual Channel function (37 virtual channels) ● Scan Group function (up to 9 scan groups) ● Variable sampling time (select from 16 tables per virtual channel) ● Channel-dedicated sample-and-hold circuit (SH) (3 SH units for A/D Converter Unit 0, 3 SH units for A/D Converter Unit 1) (Constant sampling can be set) ● Self-diagnosis function for A/D Converter ● Selectable A/D-converted value addition mode or average mode ● Analog input disconnection detection assist function (discharge function/precharge function) ● Selectable the data format from 16- / 14- / 12- / 10-bit. ● Limiter Clip Function (Up to 8 tables) ● Compare Match Function (Up to 8 tables) ● Self-calibration function ● User's Gain adjustment function ● User's Offset adjustment function ● Built-in FIFO (8 stages per each scan group) ● Multiple A/D converters Unit-to-unit synchronous operation function
Programmable Gain Amplifier (PGA)	● Analog input signals can be amplified by programmable gain amplifier (PGA), and A/D conversion can be performed. (3 PGA for A/D Converter Unit 0, 1 PGA for A/D Converter Unit 1) ● Support the single-ended input or the pseudo-differential input ● Monitor function via pin for PGA output
Interrupt sources	● A/D scan end interrupt – Generates the interrupt requests and the ELC events at the end of A/D scan operation for the scan group i (ADC_ADIi (i = 0 to 4)). The interrupt requests are independent for each scan group. – Generates the interrupt request and the ELC event at the end of A/D scan operation for any of the scan groups 5 to 8 (ADC_ADI5678). The interrupt request is shared for scan groups 5 to 8. ● FIFO data read request interrupt – Generates the interrupt requests when the number of available stages of FIFO for the scan group i becomes less than the specified value (ADC_FIFOREQi (i = 0 to 4)). The interrupt requests are independent for each scan group. – Generates the interrupt request or the ELC event when the number of available stages of FIFO for any of the scan groups 5 to 8 becomes less than the specified value (ADC_FIFOREQ5678). The interrupt request is shared for scan group 5 to 8. ● FIFO data overflow interrupt – Generates the interrupt request when the overflow occurs in any of the FIFO for the scan groups 0 to 8 (ADC_FIFOOVF). ● Limiter Clip interrupt – Generates the interrupt request when the limiter clip using the limiter tables 0 to 7 is occurred for A/D conversion results (ADC_LIMCLPI). ● Compare Match interrupt – Generates the interrupt requests when the compare match using the compare match tables j are occurred for A/D conversion results (ADC_CMPIj (j = 0 to 3)). The interrupt requests are independent for each compare match table. ● Composite Compare Match interrupt – Generates the interrupt requests and the ELC events when the compare match of the composite condition using compare match tables 0 to 7 occurs (ADC_CCMPMm (m = 0, 1)). ● A/D Converter Error interrupt – Generates the interrupt requests when the operational error is detected in A/D converter Unit j (ADC_ERRj (j = 0, 1)). ● A/D Conversion Overflow interrupt – Generates the interrupt request when the A/D conversion result overflow is occurred (ADC_RESOVFj (j = 0,1)) The interrupt requests are independent for A/D converter unit j. ● A/D Converter calibration end interrupt – Generates the interrupt requests at the end of calibration operation of A/D converter unit j (ADC_CALENDj (j = 0, 1)).
	● Trigger Input – Scan can be started by the trigger from the ELC. ● Event Generation – An event is generated at the end of each scan operation for the scan group 0 to 4. – An event is generated at the end of scan operation for any of the scan group 5 to 8. – An event is generated when Complex Compare Match is occurred.
Reference Voltage	VREFH0 is the analog reference voltage. VREFL0 is the analog reference ground.
Module-stop function	Module-stop state can be set to reduce power consumption.*3

Table 36.1 ADC规格（2个中的2个）

Item	Description
Functions	● 虚拟通道功能（37个虚拟通道） ● 扫描组功能（最多9个扫描组） ● 可变采样时间（从每个虚拟通道16个表中选择） ● 通道专用采样保持电路（SH）（AD转换器单元0为3个SH单元，AD转换器单元1为3个SH单元）（可设置恒定采样） ● AD转换器的自诊断功能 ● 可选择AD转换值加法模式或平均模式 ● 模拟输入断线检测辅助功能（放电功能预充电功能） ● 可选择16141210位的数据格式。 ● 限制器剪辑功能（最多8个表） ● 比较匹配功能（最多8个表） ● Self-calibration function ● 用户增益调节功能 ● 用户偏移调整功能 ● 内置FIFO（每个扫描组8个阶段） ● 多个AD转换器单元间同步操作功能
可编程增益放大器(PGA)	● 模拟输入信号可以通过可编程增益放大器（PGA）进行放大，并且可以进行A/D转换。（3个PGA用于AD转换器单元0，1个PGA用于AD转换器单元1） ● 支持单端输入或伪差分输入 ● 通过PGA输出引脚监控功能
中断源	● AD扫描结束中断 – 在扫描组i(ADC_ADIi(i=0to4))的AD扫描操作结束时生成中断请求和ELC事件。每个扫描组的中断请求是独立的。 – 在扫描组5到8(ADC_ADI5678)中的任何一个的AD扫描操作结束时生成中断请求和ELC事件。扫描组5到8共享中断请求。 ● FIFO数据读取请求中断 – 当扫描组i的可用FIFO级数小于指定值(ADC_FIFOREQi(i=0到4))时，生成中断请求。每个扫描组的中断请求是独立的。 – 当可用级数达到时产生中断请求或ELC事件 任何扫描组5到8的FIFO变得小于指定值(ADC_FIFOREQ5678)。中断请求为扫描组5到8共享。 ● FIFO数据溢出中断 – 当扫描组0到8(ADC_FIFOOVF)的任何FIFO发生溢出时生成中断请求。 ● 限制器剪辑中断 – 当AD转换结果(ADC_LIMCLPI)发生使用限制器表0至7的限制器剪辑时，生成中断请求。 ● 比较匹配中断 – 当AD转换结果(ADC_CMPIj(j=0to3))发生使用比较匹配表j的比较匹配时产生中断请求。中断请求对于每个比较匹配表都是独立的。 ● 复合比较匹配中断 – 当使用比较匹配表0到7的复合条件比较匹配发生时（ADC_CCMPMm(m=0 1)），生成中断请求和ELC事件。 ● AD转换器错误中断 – 当在AD转换器单元j(ADC_ERRj(j=0 1))中检测到操作错误时产生中断请求。 ● AD转换溢出中断 – 发生AD转换结果溢出时产生中断请求(ADC_RESOVFj(j=0 1))中断请求独立于AD转换单元j。 ● AD转换器校准结束中断 – 在AD转换器单元j(ADC_CALENDj(j=0 1))的校准操作结束时生成中断请求。
	● 触发输入 – 可以通过ELC的触发器启动扫描。 ● 事件生成 – 在扫描组0到4的每个扫描操作结束时生成一个事件。 – 对于扫描组5到8中的任何一个，扫描操作结束时都会生成一个事件。 – 发生复杂比较匹配时会生成一个事件。
参考电压	VREFH0是模拟参考电压。VREFL0是模拟 参考地。
Module-stop function	可设置模块停止状态以降低功耗。*3

Note 1. For details, refer to section 8, Clock Generation Circuit.
Note 2. Up to 8 channels can be assigned per scan group.
Note 3. For details, refer to section 10, Low Power Modes.

Table 36.2 ADC I/O pins

Pin name	I/O	Function
AVCC0	Input	Analog block power supply pin
AVSS0	Input	Analog block power supply ground pin
VREFH0	Input	Analog reference voltage supply pin
VREFL0	Input	Analog reference ground pin
AN000 to AN028	Input	Analog input pins
PGAIN0 to PGAIN3	Input	Analog input pins for Programmable Gain Amplifier
PGAVSS0 to PGAVSS3	Input	Reference ground input pins for Programmable Gain Amplifier
PGAOUT0 to PGAOUT3	Output	Voltage Monitor pins for Programmable Gain Amplifier
SHIN0 to SHIN2, SHIN4 to SHIN6	Input	Analog input pins for Channel-dedicated sample-and-hold circuit
ADTRG0, ADTRG1	Input	External trigger input pin for starting A/D conversion, Active Low.

Figure 36.1 shows the block diagram of ADC. Figure 36.2 shows the Analog Channel Structure for A/D Converter Unit 0. Figure 36.3 shows the Analog Channel Structure for A/D Converter Unit 1.

注1.有关详细信息，请参阅第8节，时钟生成电路。
注2.每个扫描组最多可以分配8个通道。注3.有关详细信息，
请参阅第10节，低功耗模式。

Table 36.2 ADC I/O pins

引脚名称	I/O	Function
AVCC0	Input	模拟模块电源引脚
AVSS0	Input	模拟模块电源接地引脚
VREFH0	Input	模拟参考电压电源引脚
VREFL0	Input	模拟参考接地引脚
AN000 to AN028	Input	模拟输入引脚
PGAIN0 to PGAIN3	Input	可编程增益放大器的模拟输入引脚
PGAVSS0 to PGAVSS3	Input	可编程增益放大器的参考地输入引脚
PGAOUT0 to PGAOUT3	Output	可编程增益放大器的电压监视器引脚
SHIN0 to SHIN2, SHIN4 to SHIN6	Input	通道专用采样保持电路的模拟输入引脚
ADTRG0, ADTRG1	Input	用于启动AD转换的外部触发输入引脚，低电平有效。

图36.1显示了ADC的框图。图36.2显示了AD转换器单元0的模拟通道结构。
图36.3显示了AD转换器单元1的模拟通道结构。

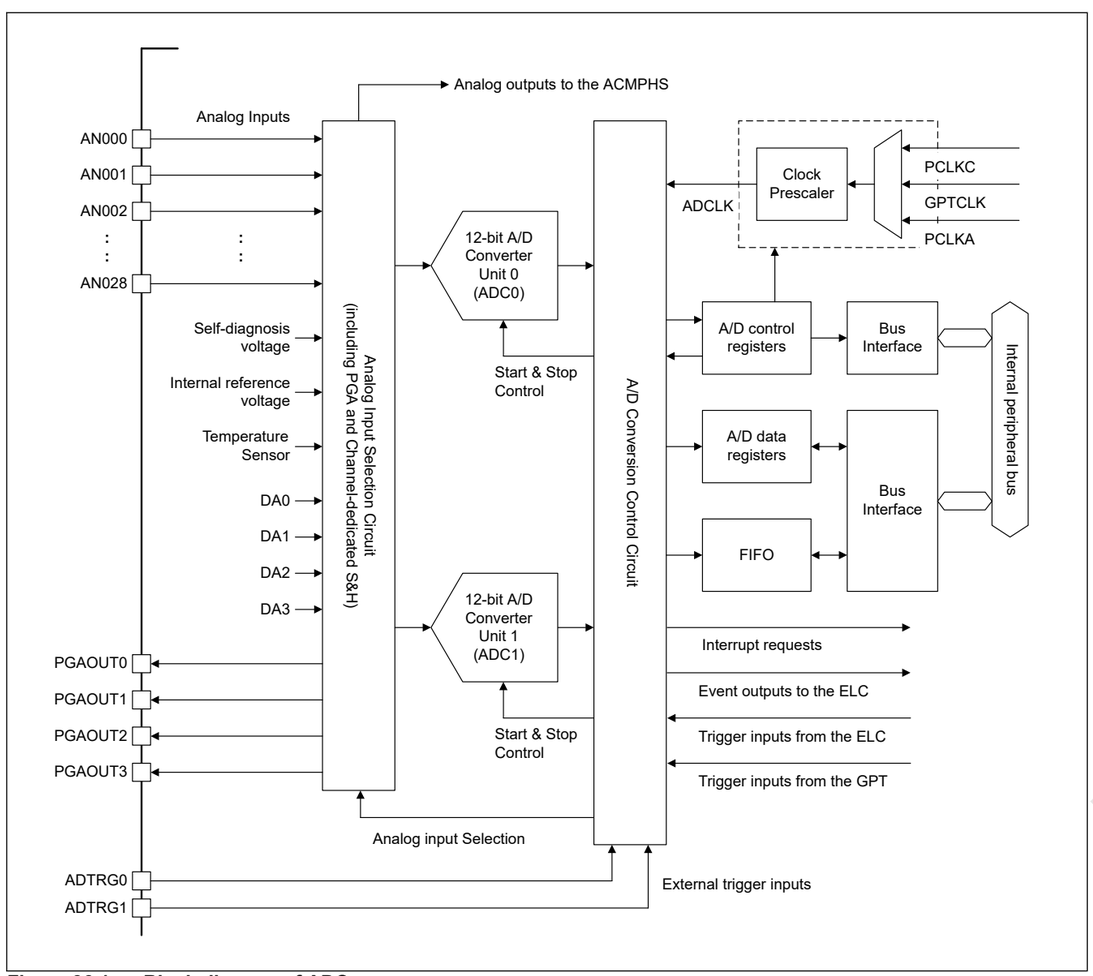


Figure 36.1 Block diagram of ADC

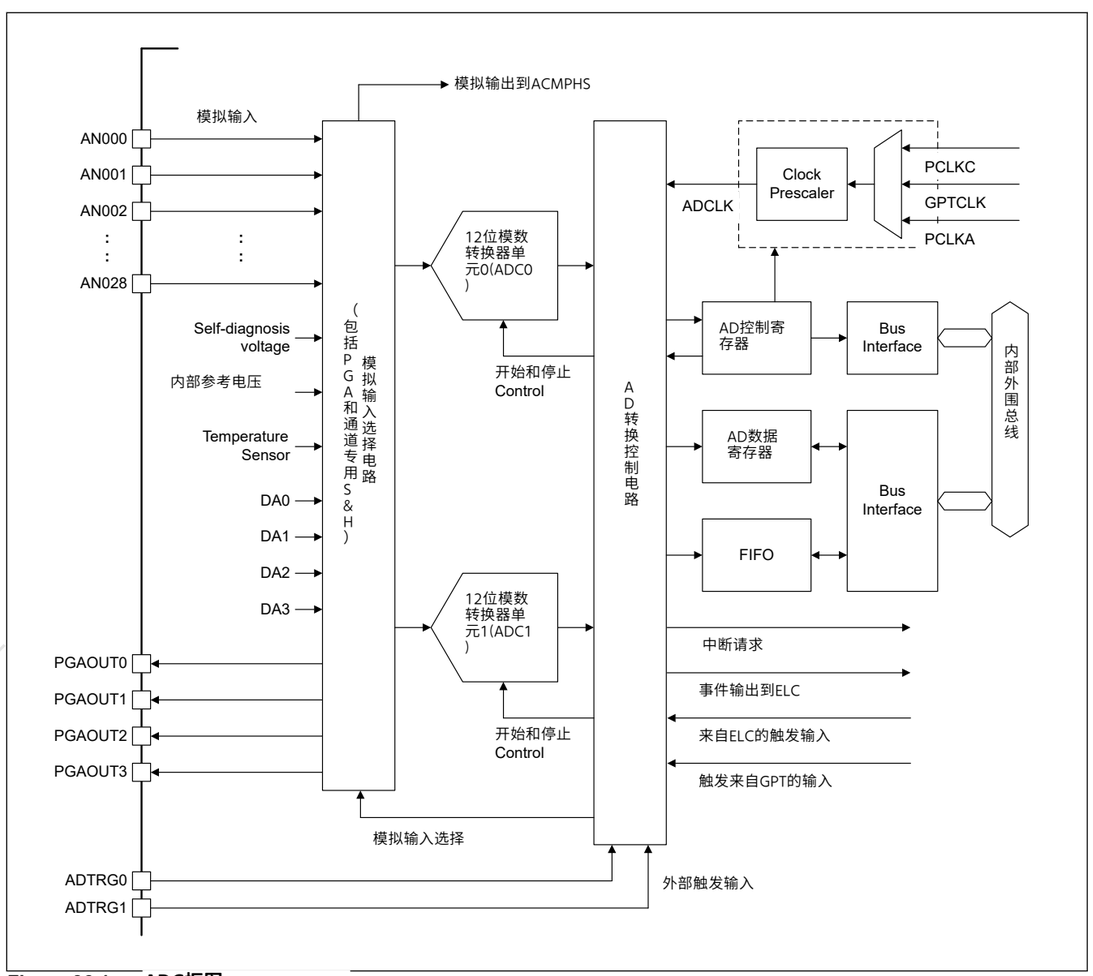


Figure 36.1 ADC框图

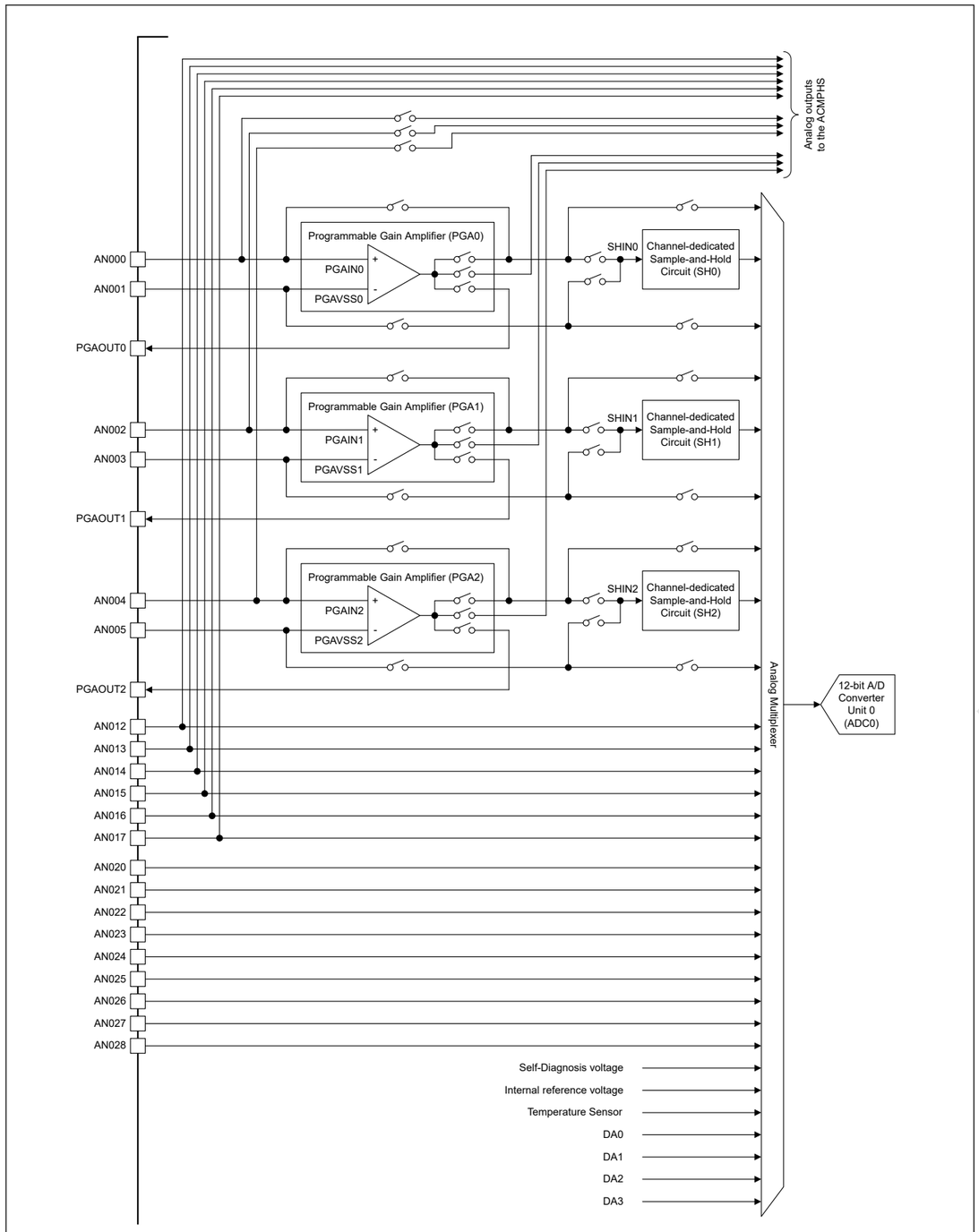


Figure 36.2 Analog Channel Structure for A/D Converter Unit 0

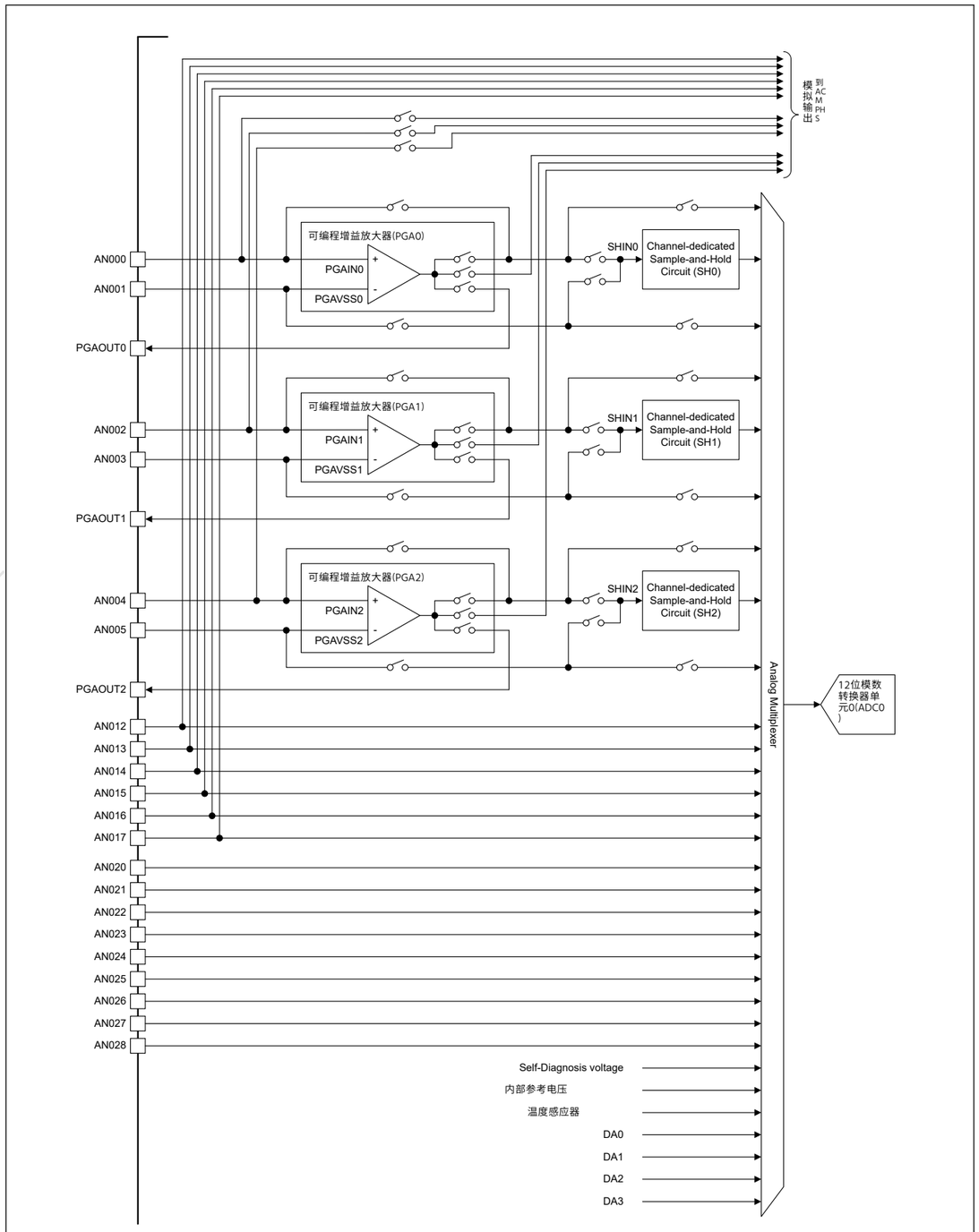


Figure 36.2 AD转换器单元0的模拟通道结构

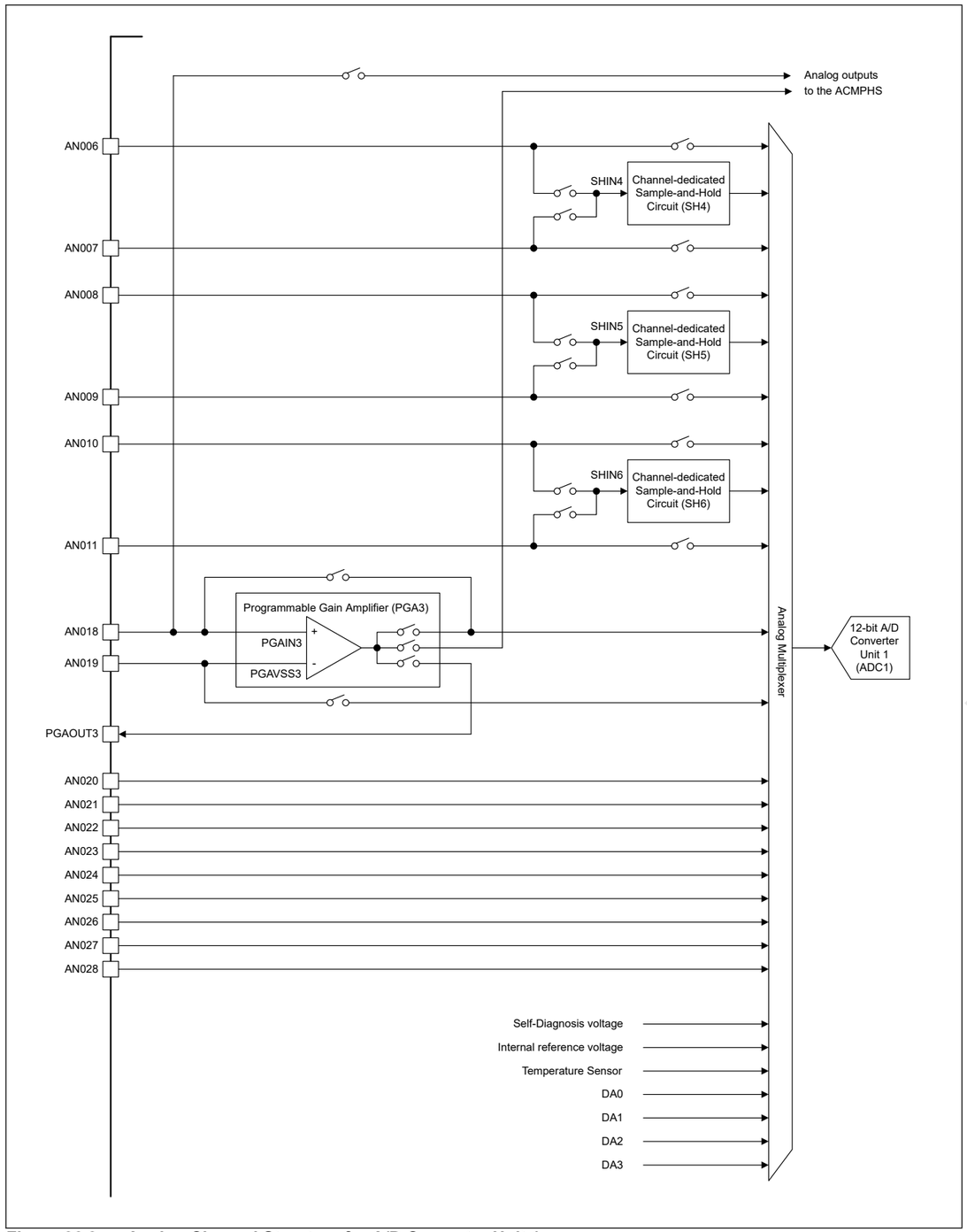


Figure 36.3 Analog Channel Structure for A/D Converter Unit 1

Table 36.3 shows the ADC channel configuration of the analog inputs.

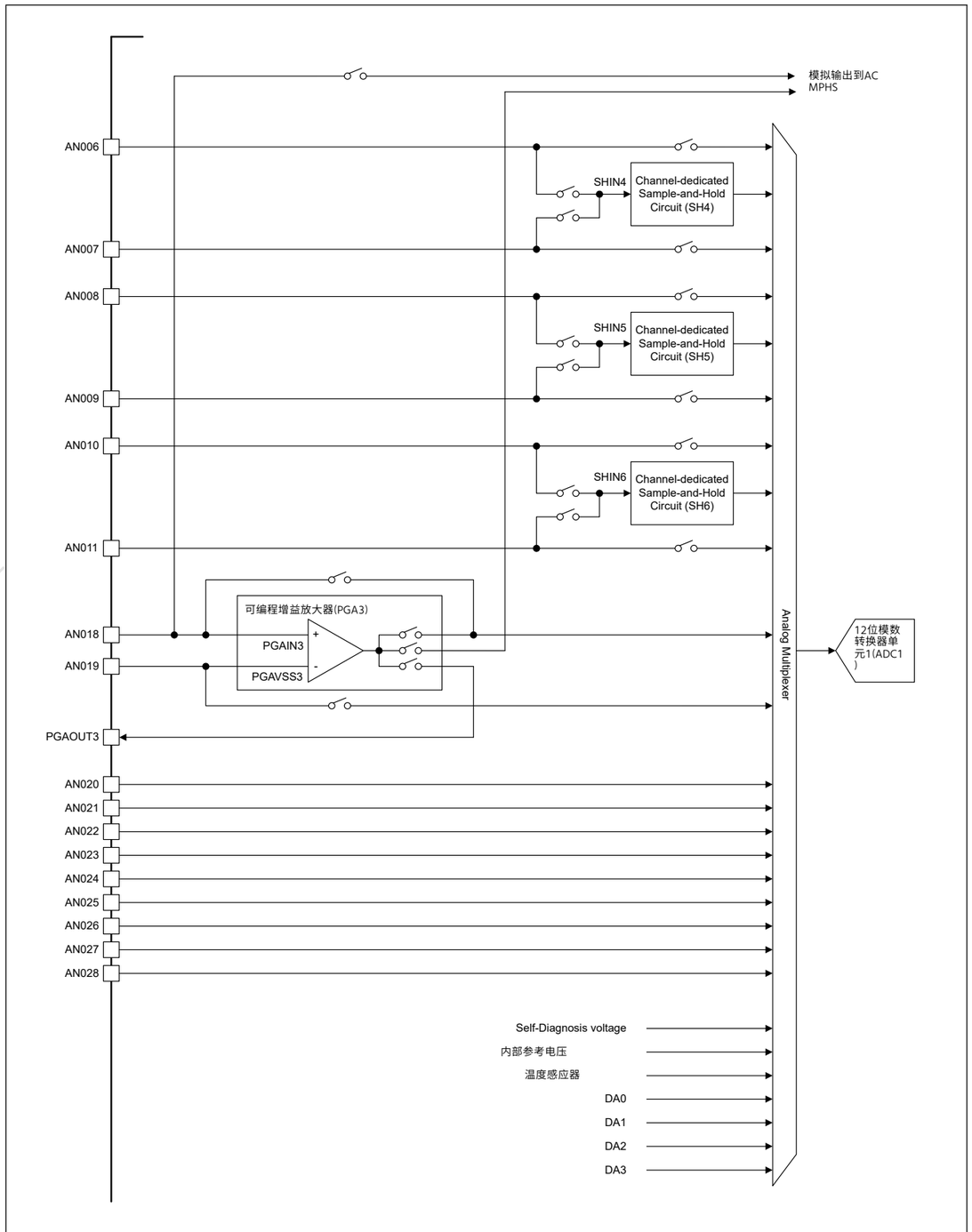


Figure 36.3 AD转换器单元1的模拟通道结构

表36.3显示了模拟输入的ADC通道配置。

Table 36.3 ADC channel configuration of the analog inputs

Analog Channel Number	Source of Analog Signal			A/D Converter	
	Analog Input	Programmable Gain Amplifier	Channel-dedicated Sample-and-Hold Circuit	Unit 0	Unit 1
0	AN000	PGAIN0	SHIN0*3	✓	—
1	AN001*2	PGAVSS0		✓	—
2	AN002	PGAIN1	SHIN1*3	✓	—
3	AN003*2	PGAVSS1		✓	—
4	AN004	PGAIN2	SHIN2*3	✓	—
5	AN005*2	PGAVSS2		✓	—
6	AN006	—	SHIN4*3	—	✓
7	AN007	—		—	✓
8	AN008	—	SHIN5*3	—	✓
9	AN009	—		—	✓
10	AN010	—	SHIN6*3	—	✓
11	AN011	—		—	✓
12	AN012	—	—	✓	—
13	AN013	—	—	✓	—
14	AN014	—	—	✓	—
15	AN015	—	—	✓	—
16	AN016	—	—	✓	—
17	AN017	—	—	✓	—
18	AN018	PGAIN3	—	—	✓
19	AN019*2	PGAVSS3	—	—	✓
20	AN020*1	—	—	✓	✓
21	AN021*1	—	—	✓	✓
22	AN022*1	—	—	✓	✓
23	AN023*1	—	—	✓	✓
24	AN024*1	—	—	✓	✓
25	AN025*1	—	—	✓	✓
26	AN026*1	—	—	✓	✓
27	AN027*1	—	—	✓	✓
28	AN028*1	—	—	✓	✓

Note 1. Do not convert the same signal source from both A/D converter Unit 0 and Unit 1.
Note 2. Only when the Programmable Gain Amplifier (PGA) is disabled and PGA is set to single-ended input, the ANx can be used for A/D conversion as an analogue input channel. When PGA is enabled, it works as PGAVSS pin; Do not perform A/D conversion of ANx. Regardless of the PGA enable/disable setting, when the PGA is set to a pseudo-differential input, A/D conversion of the ANx is not possible.
Note 3. The one Channel-dedicated Sample-and-Hold Circuit is shared from the two analog channels.

Table 36.4 shows the ADC channel configuration of the extended analog function.

Table 36.4 ADC channel configuration of the extended analog function (1 of 2)

Analog Channel Number	Source of Analog Signal*1	A/D Converter	
		Unit 0	Unit 1
96	Self-diagnosis	✓	✓
97	Temperature Sensor	✓	✓

Table 36.3 模拟输入的ADC通道配置

模拟通道号	模拟信号源			A/D Converter	
	模拟输入	可编程增益 Amplifier	Channel-dedicated Sample-and-Hold Circuit	Unit 0	Unit 1
0	AN000	PGAIN0	SHIN0*3	✓	—
1	AN001*2	PGAVSS0		✓	—
2	AN002	PGAIN1	SHIN1*3	✓	—
3	AN003*2	PGAVSS1		✓	—
4	AN004	PGAIN2	SHIN2*3	✓	—
5	AN005*2	PGAVSS2		✓	—
6	AN006	—	SHIN4*3	—	✓
7	AN007	—		—	✓
8	AN008	—	SHIN5*3	—	✓
9	AN009	—		—	✓
10	AN010	—	SHIN6*3	—	✓
11	AN011	—		—	✓
12	AN012	—	—	✓	—
13	AN013	—	—	✓	—
14	AN014	—	—	✓	—
15	AN015	—	—	✓	—
16	AN016	—	—	✓	—
17	AN017	—	—	✓	—
18	AN018	PGAIN3	—	—	✓
19	AN019*2	PGAVSS3	—	—	✓
20	AN020*1	—	—	✓	✓
21	AN021*1	—	—	✓	✓
22	AN022*1	—	—	✓	✓
23	AN023*1	—	—	✓	✓
24	AN024*1	—	—	✓	✓
25	AN025*1	—	—	✓	✓
26	AN026*1	—	—	✓	✓
27	AN027*1	—	—	✓	✓
28	AN028*1	—	—	✓	✓

注1.不要从AD转换器单元0和单元1转换相同的信号源。
注2.只有当可编程增益放大器(PGA)被禁用且PGA设置为单端输入时，ANx才能作为模拟输入通道用于AD转换。当PGA使能时，它作为PGAVSS引脚工作；不要执行ANx的AD转换。无论PGA启用禁用设置如何，当PGA设置为伪差分输入时，ANx的AD转换是不可能的。

注3.一个通道专用的采样保持电路由两个模拟通道共享。

表36.4显示了扩展模拟功能的ADC通道配置。

Table 36.4 扩展模拟功能的ADC通道配置(1of2)

模拟频道 Number	模拟信号源*1	A/D Converter	
		Unit 0	Unit 1
96	Self-diagnosis	✓	✓
97	温度感应器	✓	✓

Table 36.4 ADC channel configuration of the extended analog function (2 of 2)

Analog Channel Number	Source of Analog Signal*1	A/D Converter	
		Unit 0	Unit 1
98	Internal reference voltage	✓	✓
101	D/A Converter channel 0	✓	✓
102	D/A Converter channel 1	✓	✓
103	D/A Converter channel 2	✓	✓
104	D/A Converter channel 3	✓	✓

Note 1. Do not convert the same signal source from both A/D converter Unit 0 and Unit 1.

36.2 Register Descriptions

36.2.1 System

36.2.1.1 ADCLKENR : A/D Conversion Clock Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CLKEN	ADCLK Operating Enable bit 0: Stop ADCLK 1: Operating enable ADCLK	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

The ADCLKENR register controls the A/D conversion clock (ADCLK) to operate or stop.

36.2.1.2 ADCLKSR : A/D Conversion Clock Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKSR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 36.4 扩展模拟功能的ADC通道配置(2of2)

模拟频道 Number	模拟信号源*1	A/D Converter	
		Unit 0	Unit 1
98	内部参考电压	✓	✓
101	DA转换器通道0	✓	✓
102	DA转换器通道1	✓	✓
103	DA转换器通道2	✓	✓
104	DA转换器通道3	✓	✓

注1.不要从AD转换器单元0和单元1转换相同的信号源。

36.2 注册说明

36.2.1 System

36.2.1.1 ADCLKENR:AD转换时钟使能寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CLKEN	ADCLK操作使能位 0：停止ADCLK1：使能ADCLK	R/W
31:1	—	这些位被读取为0。写入值应为0。	R/W

ADCLKENR寄存器控制AD转换时钟(ADCLK)操作或停止。

36.2.1.2 ADCLKSR:AD转换时钟状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKSR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CLKSR	ADCLK status bit 0: ADCLK is stopped 1: ADCLK is operating	R
31:1	—	These bits are read as 0.	R

The ADCLKSR register indicates that A/D conversion clock (ADCLK) is stop or operating.

36.2.1.3 ADCLKCR : A/D Conversion Clock Control Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18		16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	DIVR[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CLKSEL[1:0]	ADCLK Clock Source Select 0 0: Peripheral Module Clock C (PCLKC) 0 1: GPT clock (GPTCLK) 1 0: Peripheral Module Clock A (PCLKA) 0 1: Setting prohibited	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
18:16	DIVR[2:0]	Clock Division Ratio Select 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/3 0 1 1: 1/4 1 0 0: 1/5 1 0 1: 1/6 1 1 0: 1/7 1 1 1: 1/8	R/W
31:19	—	These bits are read as 0. The write value should be 0.	R/W

The ADCLKCR register selects the frequency of A/D conversion clock (ADCLK). The frequency of ADCLK should be set within the range specified in the section 46, Electrical Characteristics.

CLKSEL[1:0] bits (ADCLK Clock Source Select)

CLKSEL[1:0] bits select the clock source of A/D conversion clock (ADCLK).

DIVR[2:0] bits (Clock Division Ratio Select)

DIVR[2:0] bits select the division ratio for the clock source selected by CLKSEL[1:0] bits. The clock divided by the clock source selected by CLKSEL[1:0] bits at the ratio set by DIVR[2:0] bits becomes the A/D conversion operating clock (ADCLK).

Bit	Symbol	Function	R/W
0	CLKSR	ADCLK状态位 0：ADCLK停止1：ADC LK正在运行	R
31:1	—	这些位读为0。	R

ADCLKSR寄存器指示AD转换时钟(ADCLK)停止或运行。

36.2.1.3 ADCLKCR:AD转换时钟控制寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18		16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	DIVR[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKSEL[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CLKSEL[1:0]	ADCLK时钟源选择 00：外设模块时钟C(PCLKC)01：GPT时钟(GPTCLK)10：外设模块时钟A(PCLKA)01： 禁止设置	R/W
15:2	—	这些位被读取为0。写入值应为0。	R/W
18:16	DIVR[2:0]	时钟分频比选择 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/3 0 1 1: 1/4 1 0 0: 1/5 1 0 1: 1/6 1 1 0: 1/7 1 1 1: 1/8	R/W
31:19	—	这些位被读取为0。写入值应为0。	R/W

ADCLKCR寄存器选择AD转换时钟(ADCLK)的频率。ADCLK的频率应设置在第46节“电气特性”中指定的范围内。

CLKSEL[1:0]位（ADCLK时钟源选择）

CLKSEL[1:0]位选择AD转换时钟(ADCLK)的时钟源。

DIVR[2:0]位（时钟分频比选择）

DIVR[2:0]位选择由CLKSEL[1:0]位选择的时钟源的分频比。由CLKSEL[1:0]位选择的时钟源以DIVR[2:0]位设置的比率分频的时钟成为AD转换操作时钟(ADCLK)。

36.2.1.4 ADSYCR : A/D Converter Synchronous Operation Control Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x00C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADSY DIS1	ADSY DIS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	ADSYCYC[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
10:0	ADSYCYC[10:0]	Synchronous Operation Period Cycle These bits should be set in the range from 2 to 1023. The settings of 0 or 1 are prohibited.	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W
16	ADSYDIS0	ADC0 Synchronous Operation Select 0: Enable ADC0 synchronous operation 1: Disable ADC0 synchronous operation	R/W
17	ADSYDIS1	ADC1 Synchronous Operation Select 0: Enable ADC1 synchronous operation 1: Disable ADC1 synchronous operation	R/W
31:18	—	These bits are read as 0. The write value should be 0.	R/W

The ADSYCR register controls the Synchronous operation function.

ADSYCYC[10:0] bits (Synchronous Operation Period Cycle)

These bits are selected the Synchronous operation period cycles.

These bits set in the range from 2 to 1023 regardless of whether the synchronous operation function is used or not.

The settings of 0 or 1 are prohibited.

ADSYDIS0 bit (ADC0 Synchronous Operation Select)

ADSYDIS0 bit selects enable/disable the synchronous operation of ADC0. If the synchronous operation is enabled, the ADC0 operates synchronously with other A/D converter that has synchronous operation enabled.

ADSYDIS1 bit (ADC1 Synchronous Operation Select)

ADSYDIS1 bit selects enables/disables to the synchronous operation of ADC1. If the synchronous operation is enabled, the ADC1 operates synchronously with other A/D converter that has synchronous operation enabled.

36.2.1.4 ADSYCR:AD转换器同步操作控制寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x00C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADSY DIS1	ADSY DIS0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	ADSYCYC[10:0]										
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
10:0	ADSYCYC[10:0]	同步操作周期Cycle这些位应设置在2到1023的范围内 。 禁止设置0或1。	R/W
15:11	—	这些位被读取为0。写入值应为0。	R/W
16	ADSYDIS0	ADC0同步操作选择 0：启用ADC0同步操作1：禁用ADC0同 步操作	R/W
17	ADSYDIS1	ADC1同步操作选择 0：使能ADC1同步操作1：禁止ADC1同 步操作	R/W
31:18	—	这些位被读取为0。写入值应为0。	R/W

ADSYCR寄存器控制同步操作功能。

ADSYCYC[10:0]位（同步操作周期）

这些位选择同步操作周期周期。

无论是否使用同步运算功能，这些位都设置在2到1023的范围内。

禁止设置0或1。

ADSYDIS0位（ADC0同步操作选择）

ADSYDIS0位选择使能禁用ADC0的同步操作。如果启用同步操作，则ADC0与其他已启用同步操作的AD转换器同步操作。

ADSYDIS1位（ADC1同步操作选择）

ADSYDIS1位选择启用禁用ADC1的同步操作。如果启用同步操作，则ADC1与其他已启用同步操作的AD转换器同步操作。

36.2.1.5 ADERINTCR : A/D Conversion Error Interrupt Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADEIE1	ADEIE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADEIE0	ADC0 A/D Conversion Error Interrupt Enable 0: Disable A/D conversion error interrupt for ADC0 1: Enable A/D conversion error interrupt for ADC0	R/W
1	ADEIE1	ADC1 A/D Conversion Error Interrupt Enable 0: Disable A/D conversion error interrupt for ADC1 1: Enable A/D conversion error interrupt for ADC1	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

The ADERINTCR register controls the enable/disable to the A/D conversion error interrupt.

36.2.1.6 ADOVFINTCR : A/D Conversion Overflow Interrupt Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x024

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADOVFIE1	ADOVFIE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADOVFIE0	ADC0 A/D Conversion Overflow Interrupt Enable 0: Disable A/D conversion Overflow Interrupt Enable for ADC0 1: Enable A/D conversion Overflow Interrupt Enable for ADC0	R/W
1	ADOVFIE1	ADC1 A/D Conversion Overflow Interrupt Enable 0: Disable A/D conversion Overflow Interrupt Enable for ADC1 1: Enable A/D conversion Overflow Interrupt Enable for ADC1	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

The ADOVFINTCR register controls the enable/disable to the A/D conversion overflow interrupt.

36.2.1.5 ADERINTCR:AD转换错误中断使能寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADEIE1	ADEIE0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADEIE0	ADC0AD转换错误中断使能 0：禁止ADC0的AD转换错误中断1：使能ADC0的AD转换错误中断	R/W
1	ADEIE1	ADC1AD转换错误中断使能 0：禁止ADC1的AD转换错误中断1：使能ADC1的AD转换错误中断	R/W
31:2	—	这些位被读取为0。写入值应为0。	R/W

ADERINTCR寄存器控制AD转换错误中断的使能禁用。

36.2.1.6 ADOVFINTCR:AD转换溢出中断使能寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x024

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADOVFIE1	ADOVFIE0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADOVFIE0	ADC0AD转换溢出中断使能 0：禁止ADC0的AD转换溢出中断使能1：使能ADC0的AD转换溢出中断使能	R/W
1	ADOVFIE1	ADC1AD转换溢出中断使能 0：禁止ADC1的AD转换溢出中断使能1：使能ADC1的AD转换溢出中断使能	R/W
31:2	—	这些位被读取为0。写入值应为0。	R/W

ADOVFINTCR寄存器控制AD转换溢出中断的使能禁用。

36.2.1.7 ADCALINTCR : Calibration interrupt Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x028

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CALENDIE1	CALENDIE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 0. The write value should be 0.	R/W
16	CALENDIE0	ADC0 Calibration End Interrupt Enable 0: Disable Calibration End Interrupt for ADC0 1: Enable Calibration End Interrupt for ADC0	R/W
17	CALENDIE1	ADC1 Calibration End Interrupt Enable 0: Disable Calibration End Interrupt for ADC1 1: Enable Calibration End Interrupt for ADC1	R/W
31:18	—	These bits are read as 0. The write value should be 0.	R/W

The ADCALINTCR register controls the enable/disable to the Calibration Request Interrupt and the Calibration End Interrupt.

36.2.1.8 ADMDR : A/D Converter Mode Selection Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x040

Bit position:	31	11	8	3	0
Bit field:	—	ADMD1[3:0]	—	ADMD0[3:0]	
Value after reset:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				

Bit	Symbol	Function	R/W
3:0	ADMD0[3:0]	ADC0 Mode Selection 0x0: Single scan mode 0x1: Continuous scan mode Others: Setting prohibited	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
11:8	ADMD1[3:0]	ADC1 Mode Selection 0x0: Single scan mode 0x1: Continuous scan mode Others: Setting prohibited	R/W
31:12	—	These bits are read as 0. The write value should be 0.	R/W

The ADMDR register selects the operating mode.

36.2.2 Scan Group

36.2.1.7 ADCALINTCR:校准中断使能寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x028

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CALENDIE1	CALENDIE0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	这些位被读取为0。写入值应为0。	R/W
16	CALENDIE0	ADC0校准结束中断使能 0：禁止ADC0的校准结束中断1：使能ADC0的校准结束中断	R/W
17	CALENDIE1	ADC1校准结束中断使能 0：禁止ADC1的校准结束中断1：使能ADC1的校准结束中断	R/W
31:18	—	这些位被读取为0。写入值应为0。	R/W

ADCALINTCR寄存器控制校准请求中断和校准结束的使能禁用Interrupt.

36.2.1.8 ADMDR:AD转换器模式选择寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x040

Bit position:	31	11	8	3	0
Bit field:	—	ADMD1[3:0]	—	ADMD0[3:0]	
重置后的值:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				

Bit	Symbol	Function	R/W
3:0	ADMD0[3:0]	ADC0模式选择 0x0：单次扫描模式0x1：连续扫描模式 其他：禁止设置	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
11:8	ADMD1[3:0]	ADC1模式选择 0x0：单次扫描模式0x1：连续扫描模式 其他：禁止设置	R/W
31:12	—	这些位被读取为0。写入值应为0。	R/W

ADMDR寄存器选择工作模式。

36.2.2 扫描组

36.2.2.1 ADGSPCR : A/D Group scan Priority Control Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x044

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	GRP1	LGRRS1	RSCN1	PGS1	—	—	—	—	GRP0	LGRRS0	RSCN0	PGS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PGS0	ADC0 Group Priority Control Setting 0: ADC0 operation is without group priority control 1: ADC0 operation is with group priority control	R/W
1	RSCN0	ADC0 Group Priority Control Setting 2 0: Set when PGS0 is set to 0. 1: Set when PGS0 is set to 1.	R/W
2	LGRRS0	ADC0 Group Priority Control Setting 3 0: Set when PGS0 is set to 0. 1: Set when PGS0 is set to 1.	R/W
3	GRP0	ADC0 Group Priority Control Setting 4 0: Set the following case: ● When PGS0 is set to 0 ● When PGS0 is set to 1 and ADC0 is Single scan mode.*1 1: Set when PGS0 is set to 1 and ADC0 is Continuous scan mode.	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	PGS1	ADC1 Group Priority Control Setting 0: ADC1 operation is without group priority control 1: ADC1 operation is with group priority control	R/W
9	RSCN1	ADC1 Group Priority Control Setting 2 0: Set when PGS1 is set to 0. 1: Set when PGS1 is set to 1.	R/W
10	LGRRS1	ADC1 Group Priority Control Setting 3 0: Set when PGS1 is set to 0. 1: Set when PGS1 is set to 1.	R/W
11	GRP1	ADC1 Group Priority Control Setting 4 0: Set the following case: ● When PGS1 is set to 0 ● When PGS1 is set to 1 and ADC1 is Single scan mode.*1 1: Set when PGS1 is set to 1 and ADC1 is Continuous scan mode.	R/W
31:12	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. To perform the group priority operation by assigning 3 or more scan groups to the A/D converter Unit n (n = 0, 1), GRPn must be set to 1.

The ADGSPCR register controls the group priority operation to each A/D converter. For details on setting this register, see section 36.3.16. Group Priority Operation.

36.2.2.1 ADGSPCR:AD组扫描优先控制寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x044

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	GRP1	LGRRS1	RSCN1	PGS1	—	—	—	—	GRP0	LGRRS0	RSCN0	PGS0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PGS0	ADC0组优先控制设置 0：ADC0操作无组优先控制1：ADC0操作有组优先控制	R/W
1	RSCN0	ADC0组优先控制设置2 0：当PGS0设置为0时设置。1 ：当PGS0设置为1时设置。	R/W
2	LGRRS0	ADC0组优先控制设置3 0：当PGS0设置为0时设置。1 ：当PGS0设置为1时设置。	R/W
3	GRP0	ADC0组优先控制设置4 0：设置以下情况：● 当PGS0设置为0时 ● 当PGS0设置为1且ADC0为单次扫描模式时。*1 1：当PGS0设置为1且ADC0为连续扫描模式时设置。	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	PGS1	ADC1组优先控制设置 0：ADC1操作无组优先控制1：ADC1操作有组优先控制	R/W
9	RSCN1	ADC1组优先控制设置2 0：当PGS1设置为0时设置。1 ：当PGS1设置为1时设置。	R/W
10	LGRRS1	ADC1组优先控制设置3 0：当PGS1设置为0时设置。1 ：当PGS1设置为1时设置。	R/W
11	GRP1	ADC1组优先控制设置4 0：设置以下情况：● 当PGS1设置为0时 ● 当PGS1设置为1且ADC1为单次扫描模式时。*1 1：当PGS1设置为1且ADC1为连续扫描模式时设置。	R/W
31:12	—	这些位被读取为0。写入值应为0。	R/W

注1.通过将3个或更多扫描组分配给AD转换器单元n(n=0 1)来执行组优先操作，必须将GRPn设置为1。

ADGSPCR寄存器控制每个AD转换器的组优先级操作。有关设置该寄存器的详细信息，请参阅第36.3.16节。集团优先经营。

36.2.2.2 ADSGER : Scan Group Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x048

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SGREn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SGREn	Scan Group n Enable 0: Disable the scan group n 1: Enable the scan group n	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 8

The ADSGER register selects the enable/disable to each scan group.

SGREn bit (Scan Group n Enable bit) (n = 0 to 8)

SGREn selects the enable/disable to the scan group n. When SGREn is set to 1, A/D conversion with the scan group n is available. When SGREn is set to 0, A/D conversion with the scan group n is not available, even if the trigger corresponding to the scan group n is input.

36.2.2.3 ADSGCR0 : Scan Group Control Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0x04C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	SGADS3[1:0]		—	—	—	—	—	—	SGADS2[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SGADS1[1:0]		—	—	—	—	—	—	SGADS0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SGADS0[1:0]	Scan Group 0 A/D Converter Selection 0 0: Select ADC0 0 1: Select ADC1 Others: Setting prohibited	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
9:8	SGADS1[1:0]	Scan Group 1 A/D Converter Selection 0 0: Select ADC0 0 1: Select ADC1 Others: Setting prohibited	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W

36.2.2.2 ADSGER：扫描组启用寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x048

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SGREn								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SGREn	扫描组n启用 0：禁用扫描组n1：启用扫描组n	R/W
31:9	—	这些位被读取为0。写入值应为0。	R/W

Note: n = 0 to 8

ADSGER寄存器为每个扫描组选择启用禁用。

SGREn位（扫描组n启用位）（n=0到8）

SGREn选择对扫描组n启用禁用。当SGREn设置为1时，可以使用扫描组n进行AD转换。当SGREn设置为0时，即使输入了与扫描组n对应的触发器，也无法使用扫描组n进行AD转换。

36.2.2.3 ADSGCR0：扫描组控制寄存器0

Base address: ADC_B = 0x4017_0000

Offset address: 0x04C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	SGADS3[1:0]		—	—	—	—	—	—	SGADS2[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SGADS1[1:0]		—	—	—	—	—	—	SGADS0[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SGADS0[1:0]	扫描组0AD转换器选择 0 0: Select ADC0 0 1: Select ADC1 其他：禁止设置	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
9:8	SGADS1[1:0]	扫描组1AD转换器选择 0 0: Select ADC0 0 1: Select ADC1 其他：禁止设置	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
17:16	SGADS2[1:0]	Scan Group 2 A/D Converter Selection 0 0: Select ADC0 0 1: Select ADC1 Others: Setting prohibited	R/W
23:18	—	These bits are read as 0. The write value should be 0.	R/W
25:24	SGADS3[1:0]	Scan Group 3 A/D Converter Selection 0 0: Select ADC0 0 1: Select ADC1 Others: Setting prohibited	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

The ADSGCR0 register selects which A/D Converter is used for each scan group.

36.2.2.4 ADSGCR1 : Scan Group Control Register 1

Base address: ADC_B = 0x4017_0000

Offset address: 0x050

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	SGADS7[1:0]		—	—	—	—	—	—	SGADS6[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SGADS5[1:0]		—	—	—	—	—	—	SGADS4[1:0]	

Bit	Symbol	Function	R/W
1:0	SGADS4[1:0]	Scan Group 4 A/D Converter Selection 0 0: Select ADC0 0 1: Select ADC1 Others: Setting prohibited	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
9:8	SGADS5[1:0]	Scan Group 5 A/D Converter Selection 0 0: Select ADC0 0 1: Select ADC1 Others: Setting prohibited	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
17:16	SGADS6[1:0]	Scan Group 6 A/D Converter Selection 0 0: Select ADC0 0 1: Select ADC1 Others: Setting prohibited	R/W
23:18	—	These bits are read as 0. The write value should be 0.	R/W
25:24	SGADS7[1:0]	Scan Group 7 A/D Converter Selection 0 0: Select ADC0 0 1: Select ADC1 Others: Setting prohibited	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

The ADSGCR1 register selects which A/D Converter is used for each scan group.

Bit	Symbol	Function	R/W
17:16	SGADS2[1:0]	扫描组2AD转换器选择 0 0: Select ADC0 0 1: Select ADC1 其他：禁止设置	R/W
23:18	—	这些位被读取为0。写入值应为0。	R/W
25:24	SGADS3[1:0]	扫描组3AD转换器选择 0 0: Select ADC0 0 1: Select ADC1 其他：禁止设置	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

ADSGCR0寄存器选择用于每个扫描组的AD转换器。

36.2.2.4 ADSGCR1：扫描组控制寄存器1

Base address: ADC_B = 0x4017_0000

Offset address: 0x050

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	SGADS7[1:0]		—	—	—	—	—	—	SGADS6[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SGADS5[1:0]		—	—	—	—	—	—	SGADS4[1:0]	

Bit	Symbol	Function	R/W
1:0	SGADS4[1:0]	扫描组4AD转换器选择 0 0: Select ADC0 0 1: Select ADC1 其他：禁止设置	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
9:8	SGADS5[1:0]	扫描组5AD转换器选择 0 0: Select ADC0 0 1: Select ADC1 其他：禁止设置	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W
17:16	SGADS6[1:0]	扫描组6AD转换器选择 0 0: Select ADC0 0 1: Select ADC1 其他：禁止设置	R/W
23:18	—	这些位被读取为0。写入值应为0。	R/W
25:24	SGADS7[1:0]	扫描组7AD转换器选择 0 0: Select ADC0 0 1: Select ADC1 其他：禁止设置	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

ADSGCR1寄存器选择用于每个扫描组的AD转换器。

36.2.2.5 ADSGCR2 : Scan Group Control Register 2

Base address: ADC_B = 0x4017_0000

Offset address: 0x054

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGADS8[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SGADS8[1:0]	Scan Group 8 A/D Converter Selection 0 0: Select ADC0 0 1: Select ADC1 Others: Setting prohibited	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

The ADSGCR2 register selects which A/D Converter is used for each scan group.

36.2.2.6 ADINTCR : Scan End Interrupt Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x05C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ADIEn									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	ADIEn	Scan Group n Scan End Interrupt Enable 0: Disable Scan End interrupt 1: Enable Scan End interrupt	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 8

The ADINTCR register enables/disables the Scan End interrupt.

36.2.2.5 ADSGCR2：扫描组控制寄存器2

Base address: ADC_B = 0x4017_0000

Offset address: 0x054

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGADS8[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SGADS8[1:0]	扫描组8AD转换器选择 0 0: Select ADC0 0 1: Select ADC1 其他：禁止设置	R/W
31:2	—	这些位被读取为0。写入值应为0。	R/W

ADSGCR2寄存器选择用于每个扫描组的AD转换器。

36.2.2.6 ADINTCR:扫描结束中断使能寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x05C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ADIEn									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	ADIEn	扫描组n扫描结束中断使能 0：禁用扫描结束中断1：启用扫描结束中断	R/W
31:10	—	这些位被读取为0。写入值应为0。	R/W

Note: n = 0 to 8

ADINTCR寄存器启用禁用扫描结束中断。

36.2.2.7 ADTRGEXTn : External Trigger Enable Register n (n = 0 to 8)

Base address: ADC_B = 0x4017_0000

Offset address: 0x0C0 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRGEXT1	TRGEXT0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TRGEXT0	External Trigger Input 0 (ADTRG0) Enable 0: Disable ADTRG0 1: Enable ADTRG0	R/W
1	TRGEXT1	External Trigger Input 1 (ADTRG1) Enable 0: Disable ADTRG1 1: Enable ADTRG1	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

The ADTRGEXTn register enables/disables the External Trigger input 0 and 1 (ADTRG0 and ADTRG1) as the starting conditions for A/D conversion of scan group n.

36.2.2.8 ADTRGELCn : ELC Trigger Enable Register n (n = 0 to 8)

Base address: ADC_B = 0x4017_0000

Offset address: 0x0C4 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	TRGELCm					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	TRGELCm	ELC Trigger m Enable 0: Disable ELC Trigger m 1: Enable ELC Trigger m	R/W
31:6	—	These bits are read as 0. The write value should be 0.	R/W

Note: m = 0 to 5

The ADTRGELCn register enables/disables the ELC Trigger m as the starting conditions for A/D conversion of scan group n.

36.2.2.7 ADTRGEXTn：外部触发使能寄存器n（n=0到8）

Base address: ADC_B = 0x4017_0000

Offset address: 0x0C0 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRGEXT1	TRGEXT0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TRGEXT0	外部触发输入0(ADTRG0)使能 0：禁用ADTRG01： 启用ADTRG0	R/W
1	TRGEXT1	外部触发输入1(ADTRG1)启用 0：禁用ADTRG11： 启用ADTRG1	R/W
31:2	—	这些位被读取为0。写入值应为0。	R/W

ADTRGEXTn寄存器使能禁用外部触发输入0和1（ADTRG0和ADTRG1）作为扫描组n的AD转换的开始条件。

36.2.2.8 ADTRGELCn:ELC触发使能寄存器n(n=0到8)

Base address: ADC_B = 0x4017_0000

Offset address: 0x0C4 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	TRGELCm					
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	TRGELCm	ELC触发器m启用 0：禁用ELC触发m1：启 用ELC触发m	R/W
31:6	—	这些位被读取为0。写入值应为0。	R/W

Note: m = 0 to 5

ADTRGELCn寄存器启用禁用ELC触发器m作为扫描组n的AD转换的启动条件。

36.2.2.9 ADTRGGPTn : GPT Trigger Enable Register n (n = 0 to 8)

Base address: ADC_B = 0x4017_0000

Offset address: 0x0C8 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	TRGGPTBm									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TRGGPTAm									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	TRGGPTAm	GPT channel m A/D Conversion Starting Request A Enable 0: Disable the A/D conversion stating request A from GPT channel m 1: Enable the A/D conversion stating request A from GPT channel m	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
25:16	TRGGPTBm	GPT channel m A/D Conversion Starting Request B Enable 0: Disable the A/D conversion stating request B from GPT channel m 1: Enable the A/D conversion stating request B from GPT channel m	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

Note: m = 0 to 9

The ADTRGGPTn register enables/disables the A/D Conversion Starting Request A/B from GPT channel m as the starting conditions for A/D conversion of scan group n.

36.2.2.10 ADTRGENR : A/D Conversion Start Trigger Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	STTRGENn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STTRGENn	Scan Group n A/D Conversion Start Trigger Enable 0: Disable the A/D conversion start trigger 1: Enable the A/D conversion start trigger	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 8

The ADTRGENR register enables/disables the trigger from the peripheral modules for starting the A/D conversion of Scan group n. The triggers for each scan group are selected in the ADTRGEXTn, ADTRGELCn, and ADTRGGPTn registers.

STTRGENn bit (Scan Group n A/D Conversion Start Trigger Enable)

STTRGENn selects whether the trigger inputs from the peripheral module, which are selected in the ADTRGEXTn, ADTRGELCn, and ADTRGGPTn registers, is used for the A/D conversion start condition.

36.2.2.9 ADTRGGPTn：GPT触发使能寄存器n（n=0到8）

Base address: ADC_B = 0x4017_0000

Offset address: 0x0C8 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	TRGGPTBm									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TRGGPTAm									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	TRGGPTAm	GPT通道mAD转换启动请求A使能 0：禁止来自GPT通道m的AD转换启动请求A1：使能来自GPT通道m的AD转换启动请求A	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W
25:16	TRGGPTBm	GPT通道mAD转换启动请求B使能 0：禁止来自GPT通道m的AD转换启动请求B1：使能来自GPT通道m的AD转换启动请求B	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

Note: m = 0 to 9

ADTRGGPTn寄存器使能禁用来自GPT通道m的AD转换启动请求AB作为扫描组n的AD转换的启动条件。

36.2.2.10 ADTRGENR:AD转换开始触发使能寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xC08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	STTRGENn								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STTRGENn	扫描组nAD转换启动触发使能 0：禁止AD转换启动触发1：使能AD转换启动触发	R/W
31:9	—	这些位被读取为0。写入值应为0。	R/W

Note: n = 0 to 8

ADTRGENR寄存器使能禁用来自外围模块的触发，以启动扫描组n的AD转换。在ADTRGEXTn、ADTRGELCn和ADTRGGPTn寄存器中选择每个扫描组的触发器。

STTRGENn位（扫描组nAD转换启动触发使能）

STTRGENn选择是否来自外围模块的触发输入，在ADTRGEXTn中选择，ADTRGELCn和ADTRGGPTn寄存器用于AD转换开始条件。

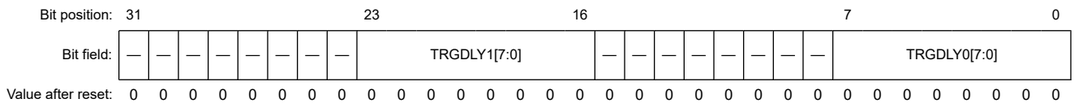
When STTRGENn bit is set to 1, the A/D conversion of scan group n can be started by trigger inputs from the peripheral module.

When STTRGENn bit is set to 0, the A/D conversion of scan group n cannot be started by trigger inputs from the peripheral module. In this setting, the A/D conversion of scan group n can be only started by writing to the ADSYSTR or ADSTRn registers.

36.2.2.11 ADTRGDLR0 : A/D Conversion Start Trigger Delay Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0x1C0



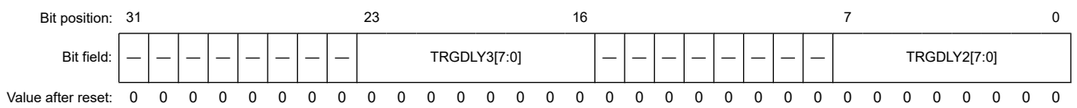
Bit	Symbol	Function	R/W
7:0	TRGDLY0[7:0]	Scan Group 0 Trigger Input Delay Configuration	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W
23:16	TRGDLY1[7:0]	Scan Group 1 Trigger Input Delay Configuration	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

The ADTRGDLR0 register controls the input delay added to the External trigger inputs, ELC triggers and GPT triggers which are the stating conditions for the A/D conversion of each scan group. The input delay value is given as the register setting value × the cycle of the A/D conversion clock (ADCLK).

36.2.2.12 ADTRGDLR1 : A/D Conversion Start Trigger Delay Register 1

Base address: ADC_B = 0x4017_0000

Offset address: 0x1C4



Bit	Symbol	Function	R/W
7:0	TRGDLY2[7:0]	Scan Group 2 Trigger Input Delay Configuration	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W
23:16	TRGDLY3[7:0]	Scan Group 3 Trigger Input Delay Configuration	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

The ADTRGDLR1 register controls the input delay added to the External trigger inputs, ELC triggers and GPT triggers which are the starting conditions for the A/D conversion of each scan group. The input delay value is given as the register setting value × the cycle of the A/D conversion clock (ADCLK).

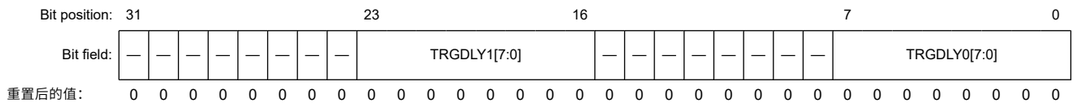
当STTRGENn位设置为1时，扫描组n的AD转换可以通过来自外围模块的触发输入来启动。

当STTRGENn位设置为0时，扫描组n的AD转换不能由外围模块的触发输入启动。在此设置中，扫描组n的AD转换只能通过写入ADSYSTR或ADSTRn寄存器来启动。

36.2.2.11 ADTRGDLR0:AD转换开始触发延迟寄存器0

Base address: ADC_B = 0x4017_0000

Offset address: 0x1C0



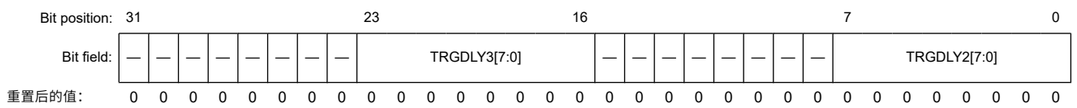
Bit	Symbol	Function	R/W
7:0	TRGDLY0[7:0]	扫描组0触发输入延迟配置	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W
23:16	TRGDLY1[7:0]	扫描组1触发输入延迟配置	R/W
31:24	—	这些位被读取为0。写入值应为0。	R/W

ADTRGDLR0寄存器控制添加到外部触发输入、ELC触发和GPT触发的输入延迟，它们是每个扫描组AD转换的启动条件。输入延迟值以寄存器设置值×AD转换时钟(ADCLK)的周期给出。

36.2.2.12 ADTRGDLR1:AD转换开始触发延迟寄存器1

Base address: ADC_B = 0x4017_0000

Offset address: 0x1C4



Bit	Symbol	Function	R/W
7:0	TRGDLY2[7:0]	扫描组2触发输入延迟配置	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W
23:16	TRGDLY3[7:0]	扫描组3触发输入延迟配置	R/W
31:24	—	这些位被读取为0。写入值应为0。	R/W

ADTRGDLR1寄存器控制添加到外部触发输入、ELC触发和GPT触发的输入延迟，它们是每个扫描组AD转换的开始条件。输入延迟值以寄存器设置值×AD转换时钟(ADCLK)的周期给出。

36.2.2.13 ADTRGDLR2 : A/D Conversion Start Trigger Delay Register 2

Base address: ADC_B = 0x4017_0000

Offset address: 0x1C8

Bit position:	31								23								16								7								0
Bit field:	—	—	—	—	—	—	—	—	TRGDLY5[7:0]								—	—	—	—	—	—	—	—	TRGDLY4[7:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TRGDLY4[7:0]	Scan Group 4 Trigger Input Delay Configuration	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W
23:16	TRGDLY5[7:0]	Scan Group 5 Trigger Input Delay Configuration	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

The ADTRGDLR2 register controls the input delay added to the External trigger inputs, ELC triggers and GPT triggers which are the starting conditions for the A/D conversion of each scan group. The input delay value is given as the register setting value × the cycle of the A/D conversion clock (ADCLK).

36.2.2.14 ADTRGDLR3 : A/D Conversion Start Trigger Delay Register 3

Base address: ADC_B = 0x4017_0000

Offset address: 0x1CC

Bit position:	31								23								16								7								0
Bit field:	—	—	—	—	—	—	—	—	TRGDLY7[7:0]								—	—	—	—	—	—	—	—	TRGDLY6[7:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TRGDLY6[7:0]	Scan Group 6 Trigger Input Delay Configuration	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W
23:16	TRGDLY7[7:0]	Scan Group 7 Trigger Input Delay Configuration	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

The ADTRGDLR3 register controls the input delay added to the External trigger inputs, ELC triggers and GPT triggers which are the starting conditions for the A/D conversion of each scan group. The input delay value is given as the register setting value × the cycle of the A/D conversion clock (ADCLK).

36.2.2.15 ADTRGDLR4 : A/D Conversion Start Trigger Delay Register 4

Base address: ADC_B = 0x4017_0000

Offset address: 0x1D0

Bit position:	31																								7								0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRGDLY8[7:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TRGDLY8[7:0]	Scan Group 8 Trigger Input Delay Configuration	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

36.2.2.13 ADTRGDLR2:AD转换开始触发延迟寄存器2

Base address: ADC_B = 0x4017_0000

Offset address: 0x1C8

Bit position:	31								23								16								7								0
Bit field:	—	—	—	—	—	—	—	—	TRGDLY5[7:0]								—	—	—	—	—	—	—	—	TRGDLY4[7:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TRGDLY4[7:0]	扫描组4触发输入延迟配置	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W
23:16	TRGDLY5[7:0]	扫描组5触发输入延迟配置	R/W
31:24	—	这些位被读取为0。写入值应为0。	R/W

ADTRGDLR2寄存器控制添加到外部触发输入、ELC触发和GPT触发的输入延迟，它们是每个扫描组AD转换的开始条件。输入延迟值以寄存器设置值×AD转换时钟(ADCLK)的周期给出。

36.2.2.14 ADTRGDLR3:AD转换开始触发延迟寄存器3

Base address: ADC_B = 0x4017_0000

Offset address: 0x1CC

Bit position:	31								23								16								7								0
Bit field:	—	—	—	—	—	—	—	—	TRGDLY7[7:0]								—	—	—	—	—	—	—	—	TRGDLY6[7:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TRGDLY6[7:0]	扫描组6触发输入延迟配置	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W
23:16	TRGDLY7[7:0]	扫描组7触发输入延迟配置	R/W
31:24	—	这些位被读取为0。写入值应为0。	R/W

ADTRGDLR3寄存器控制添加到外部触发输入、ELC触发和GPT触发的输入延迟，它们是每个扫描组AD转换的开始条件。输入延迟值以寄存器设置值×AD转换时钟(ADCLK)的周期给出。

36.2.2.15 ADTRGDLR4:AD转换开始触发延迟寄存器4

Base address: ADC_B = 0x4017_0000

Offset address: 0x1D0

Bit position:	31																								7								0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRGDLY8[7:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TRGDLY8[7:0]	扫描组8触发输入延迟配置	R/W
31:8	—	这些位被读取为0。写入值应为0。	R/W

The ADTRGDLR4 register controls the input delay added to the External trigger inputs, ELC triggers and GPT triggers which are the starting conditions for the A/D conversion of each scan group. The input delay value is given as the register setting value × the cycle of the A/D conversion clock (ADCLK).

36.2.3 Virtual Channel

36.2.3.1 ADCHCRn : A/D Conversion Channel Configuration Register n (n = 0 to 36)

Base address: ADC_B = 0x4017_0000

Offset address: 0x600 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	SSTSEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	AINMD	CNVCS[6:0]							—	—	—	SGSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	SGSEL[4:0]	Scan Group Selection 0x00: Not select any scan group 0x01: Select the scan group 0 0x02: Select the scan group 1 0x03: Select the scan group 2 0x04: Select the scan group 3 ⋮ 0x09: Select the scan group 8 Others: Setting prohibited	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
14:8	CNVCS[6:0]	A/D Conversion Channel Selection 0x00: AN000 0x01: AN001 ⋮ 0x1C: AN028 0x60: Self-diagnosis 0x61: Temperature sensor 0x62: Internal reference voltage 0x65: D/A converter channel 0 0x66: D/A converter channel 1 0x67: D/A converter channel 2 0x68: D/A converter channel 3 Others: Setting prohibited	R/W
15	AINMD	Analog Input mode selection bit 0: Set when CNVCS[6:0] is selected other than the Self-diagnosis (0x60). 1: selected the Self-diagnosis (0x60).	R/W
19:16	SSTSEL[3:0]	Sampling State Table Selection 0x0: Select the sampling state table 0 0x1: Select the sampling state table 1 0x2: Select the sampling state table 2 0x3: Select the sampling state table 3 ⋮ 0xF: Select the sampling state table 15	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The ADCHCRn register selects the Virtual channel configuration for A/D conversion.

ADTRGDLR4寄存器控制添加到外部触发输入、ELC触发和GPT触发的输入延迟，它们是每个扫描组AD转换的开始条件。输入延迟值以寄存器设置值×AD转换时钟(ADCLK)的周期给出。

36.2.3 虚拟通道

36.2.3.1 ADCHCRn:AD转换通道配置寄存器n(n=0到36)

Base address: ADC_B = 0x4017_0000

Offset address: 0x600 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	SSTSEL[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	AINMD	CNVCS[6:0]							—	—	—	SGSEL[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	SGSEL[4:0]	扫描组选择 0x00：不选择任何扫描组0x01：选择扫描组00x02：选择扫描组1 0x03：选择扫描组20x04：选择扫描组3 ⋮ 0x09：选择扫描组8 其他：禁止设置	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
14:8	CNVCS[6:0]	AD转换通道选择 0x00: AN000 0x01: AN001 ⋮ 0x1C：AN0280x60：自诊断0x61：温度传感器0x62：内部参考电压0x65：DA转换器通道00x66：DA转换器通道10x67：DA转换器通道20x68：DA转换器通道3 其他：禁止设置	R/W
15	AINMD	模拟输入模式选择位 0：选择CNVC[6：0]时设置除自诊断（0x60）以外。1：选择自诊断（0x60）。	R/W
19:16	SSTSEL[3:0]	采样状态表选择 0x0：选择采样状态表00x1：选择采样状态表10x2：选择采样状态表20x3：选择采样状态表3 ⋮ 0xF：选择采样状态表15	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

ADCHCRn寄存器选择用于AD转换的虚拟通道配置。

SGSEL[4:0] bits (Scan Group Selection)

SGSEL[4:0] bits select which scan group to assign the selected channel in CNVCS[6:0]. If SGSEL[4:0] is set to 0x00, the channel selected by CNVCS[6:0] is not available for A/D conversion. If SGSEL[4:0] is set to other than 0x00, the channel selected by CNVCS[6:0] is available for A/D conversion in the scan operation of the scan group corresponding to the setting value.

Up to 8 A/D conversion channels can be assigned per scan group. Do not assign more than 9 A/D conversion channCNVCS[6:0]els per scan group.

CNVCS[6:0] bits (A/D Conversion Channel Selection)

CNVCS[6:0] bits select the analog signal source for the A/D conversion. CNVCS[6:0] bits should be set for the channel number corresponding to the Analog Input or the Extended Analog function.

To A/D convert the channel selected by CNVCS[6:0] bits, it should be assigned to one of the scan groups by SGSEL[4:0] bits.

AINMD bits (Analog Input mode selection bit)

The AINMD bit should be set when self-diagnosis is performed.

When the self-diagnosis channel is selected (CNVCS[6:0] bits are 0x60), set the AINMD bit to 1.

Otherwise, the AINMD bit should be set to 0.

SSTSEL[3:0] bits (Sampling State Table Selection)

SSTSEL[3:0] bits select the sampling state table for A/D conversion of the analog signal source selected by the CNVCS[6:0] bits. The number of sampling states is the value set in the selected sampling state table.

36.2.3.2 ADDOPCRAn : A/D Conversion Data Operation Control A Register n (n = 0 to 36)

Base address: ADC_B = 0x4017_0000

Offset address: 0x604 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	OFSETSEL[3:0]				—	—	—	—	GAINSEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 0. The write value should be 0.	R/W
19:16	GAINSEL[3:0]	User Gain Table Selection 0x0: Not use the User Gain Table 0x1: Use the User Gain Table 0 0x2: Use the User Gain Table 1 0x3: Use the User Gain Table 2 ⋮ 0x8: Use the User Gain Table 7 0x9 to Others: Setting prohibited	R/W
23:20	—	These bits are read as 0. The write value should be 0.	R/W

SGSEL[4:0]位（扫描组选择）

SGSEL[4:0]位选择在CNVCS[6:0]中分配所选通道的扫描组。如果SGSEL[4:0]设置为0x00，则CNVCS[6:0]选择的通道不可用于AD转换。如果SGSEL[4:0]设置为0x00以外，则CNVCS[6:0]选择的通道在与设置值对应的扫描组的扫描操作中可用于AD转换。

每个扫描组最多可以分配8个AD转换通道。不要为每个扫描组分配超过9个AD转换通道CNVCS[6:0]e
ls。

CNVCS[6:0]位（AD转换通道选择）

CNVCS[6:0]位选择AD转换的模拟信号源。CNVCS[6:0]位应设置为对应于模拟输入或扩展模拟功能的通道号。

要将CNVCS[6:0]位选择的通道进行AD转换，应通过SGSEL[4:0]位将其分配到扫描组之一。

AINMD位（模拟输入模式选择位）

执行自诊断时应 设置AINMD位。

Whentheself-diagnosischannelisselected(CNVCS[6:0]bitsare0x60) settheAINMDbitto1.

否则，AINMD位应设置为0。

SSTSEL[3:0]位（采样状态表选择）

SSTSEL[3:0]位选择采样状态表，用于对所选择的模拟信号源进行AD转换
CNVCS[6:0]位。采样状态的数量是在选择的采样状态表中设置的值。

36.2.3.2 ADDOPCRAn:AD转换数据操作控制A寄存器n(n=0到36)

Base address: ADC_B = 0x4017_0000

Offset address: 0x604 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	OFSETSEL[3:0]				—	—	—	—	GAINSEL[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	这些位被读取为0。写入值应为0。	R/W
19:16	GAINSEL[3:0]	用户增益表选择 0x0：不使用用户增益表0x1：使用用户增益表00x2：使用用户增益表10x3：使用用户增益表2 ⋮ 0x8：使用用户增益表7 0x9 to Others: 禁止设定	R/W
23:20	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
27:24	OFSETSEL[3:0]	User Offset Table Selection 0x0: Not use the User Offset Table 0x1: Use the User Offset Table 0 0x2: Use the User Offset Table 1 0x3: Use the User Offset Table 2 ⋮ 0x8: Use the User Offset Table 7 Others: Setting prohibited	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

Note: m = 0, 1

The ADDOPCRAn register is one of the registers that selects the data calculation function to the A/D conversion data of virtual channel n.

GAINSEL[3:0] bits (User Gain Table Selection)

GAINSEL[3:0] bits select the User Gain Table for adjusting the A/D conversion data of virtual channel n.

When GAINSEL[3:0] bits are set to 0x0, no gain adjustment is performed. When GAINSEL[3:0] bits are set to any of 0x1 to 0x8, the gain adjustment is performed according to the User Gain Table selected by GAINSEL[3:0] bits.

OFSETSEL[3:0] bits (User Offset Table Selection)

OFSETSEL[3:0] bits select the User Offset Table for adjusting the A/D conversion data of virtual channel n. When OFSETSEL[3:0] bits are set to 0x0, no gain adjustment is performed. When OFSETSEL[3:0] bits are set to any of 0x1 to 0x8, the offset adjustment is performed according to the User Offset Table selected by OFSETSEL[3:0] bits.

36.2.3.3 ADDOPCRBn : A/D Conversion Data Operation Control B Register n (n = 0 to 36)

Base address: ADC_B = 0x4017_0000

Offset address: 0x608 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	CMPTBLEm							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	ADC[3:0]				—	—	—	—	—	—	AVEMD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	AVEMD[1:0]	Addition/Averaging Mode Selection 0 0: Not use Addition/Averaging mode 0 1: Addition mode 1 0: Averaging mode 1 1: Setting prohibited	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
27:24	OFSETSEL[3:0]	用户偏移表选择 0x0：不使用用户偏移表0x1：使用用户偏移表00x2：使用用户偏移表10x3：使用用户偏移表2 ⋮ 0x8：使用用户偏移表7 其他：禁止设置	R/W
31:28	—	这些位被读取为0。写入值应为0。	R/W

Note: m = 0, 1

ADDOPCRAn寄存器是选择对虚拟通道n的AD转换数据进行数据计算功能的寄存器之一。

GAINSEL[3:0]位（用户增益表选择）

GAINSEL[3:0]位选择用户增益表，用于调整虚拟通道n的AD转换数据。

当GAINSEL[3:0]位设置为0x0时，不执行增益调整。当GAINSEL[3:0]位设置为0x1到0x8中的任何一个时，增益调整根据GAINSEL[3:0]位选择的用户增益表执行。

OFSETSEL[3:0]位（用户偏移表选择）

OFSETSEL[3:0]位选择用于调整虚拟通道n的AD转换数据的用户偏移表。什么时候OFSETSEL[3:0]位设置为0x0，不执行增益调整。当OFSETSEL[3:0]位设置为0x1到0x8中的任何一个时，根据由OFSETSEL[3:0]位选择的用户偏移表执行偏移调整。

36.2.3.3 ADDOPCRBn:AD转换数据操作控制B寄存器n(n=0到36)

Base address: ADC_B = 0x4017_0000

Offset address: 0x608 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	CMPTBLEm							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	ADC[3:0]				—	—	—	—	—	—	AVEMD[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	AVEMD[1:0]	加法平均模式选择 00：不使用加法平均模式01：加法模式10：平均模式11：禁止设置	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
11:8	ADC[3:0]	Addition/Averaging Times Selection 0x0: 1-time conversion (no addition, same as normal conversion) 0x1: 2-time conversion (1 addition) 0x3: 4-time conversion (3 additions) 0x4: 8-time conversion (7 additions) 0x5: 16-time conversion (15 additions) 0x6: 32-time conversion (31 additions) 0x7: 64-time conversion (63 additions) 0x8: 128-time conversion (127 additions) 0x9: 256-time conversion (255 additions) 0xA: 512-time conversion (511 additions) 0xB: 1024-time conversion (1023 additions) Others: Setting prohibited	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
23:16	CMPTBLEm	Compare Match Enable 0: Disable the compare match with the Compare Match Table m 1: Enable the compare match with the Compare Match Table m	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

Note: m = 0 to 7

The ADDOPCRBn register is one of the registers that selects the data calculation function to the A/D conversion data of virtual channel n.

AVEMD[1:0] bits (Addition/Averaging Mode Selection)

AVEMD[1:0] bits select the addition mode or the averaging mode for the A/D conversion of virtual channel n. When ADMD[1:0] bits are set to 00b, the addition/averaging operation is not performed. When ADMD[1:0] bits are set to 01b or 10b, the addition/averaging operation is performed according to the setting value of ADC[3:0] bits.

ADC[3:0] bits (Addition/Averaging Times Selection)

ADC[3:0] bits select the number of times of addition/averaging for the A/D conversion of virtual channel n. If the addition mode or the averaging mode is selected in AVEMD[1:0] bits, the A/D conversion is performed a number of times according to the setting value of ADC[3:0] bits.

CMPTBLEm bits (Compare Match Enable) (m = 0 to 7)

CMPTBLEm bits enable/disable the compare match with the compare match table m for the A/D conversion data of virtual channel n.

36.2.3.4 ADDOPCRCn : A/D Conversion Data Operation Control C Register n (n = 0 to 36)

Base address: ADC_B = 0x4017_0000

Offset address: 0x60C + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	SIGNSEL	—	—	ADPRC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	LIMTBLS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
11:8	ADC[3:0]	加法平均次数选择 0x0：1次转换（无加法，与普通转换相同）0x1：2次转换（1次加法）0x3：4次转换（3次加法）0x4：8次转换（7次加法）0x5：16次转换（15次加法）0x6：32次转换（31次加法）0x7：64次转换（63次加法）0x8：128次转换（127次加法）0x9：256次转换（255次加法）0xA：512次转换（511次加法）0xB：1024次转换（1023次加法） 其他：禁止设置	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W
23:16	CMPTBLEm	比较匹配启用 0：禁用与比较匹配表m的比较匹配1：启用与比较匹配表m的比较匹配	R/W
31:24	—	这些位被读取为0。写入值应为0。	R/W

Note: m = 0 to 7

ADDOPCRBn寄存器是选择对虚拟通道n的AD转换数据进行数据计算功能的寄存器之一。

AVEMD[1:0]位（加法平均模式选择）

AVEMD[1:0]位选择虚拟通道n的AD转换的加法模式或平均模式。什么时候ADMD[1:0]位设置为00b，不执行加法平均操作。当ADMD[1:0]位设置为01b或10b时，根据ADC[3:0]位的设置值进行加法平均运算。

ADC[3:0]位（加法平均次数选择）

ADC[3:0]位选择虚拟通道n的A/D转换的加法平均次数。如果在AVEMD[1:0]位中选择了加法模式或平均模式，则AD转换根据ADC[3:0]位的设置值进行多次。

CMPTBLEm位（比较匹配使能）（m=0到7）

CMPTBLEm位使能禁用与比较匹配表m的比较匹配，用于虚拟通道n的AD转换数据。

36.2.3.4 ADDOPCRCn:AD转换数据操作控制C寄存器n(n=0到36)

Base address: ADC_B = 0x4017_0000

Offset address: 0x60C + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	SIGNSEL	—	—	ADPRC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	LIMTBLS[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	LIMTBLS[3:0]	Limiter Clip Table Selection 0x0: Not use the Limiter Clip Table 0x1: Use the Limiter Clip Table 0 0x2: Use the Limiter Clip Table 1 0x3: Use the Limiter Clip Table 2 ⋮ 0x8: Use the Limiter Clip Table 7 Others: Setting prohibited	R/W
15:4	—	These bits are read as 0. The write value should be 0.	R/W
17:16	ADPRC[1:0]	A/D Conversion Data Format Selection 0 0: Store the A/D conversion result as 16-bit data format 0 1: Store the A/D conversion result as 14-bit data format 1 0: Store the A/D conversion result as 12-bit data format 1 1: Store the A/D conversion result as 10-bit data format	R/W
19:18	—	These bits are read as 0. The write value should be 0.	R/W
20	SIGNSEL	A/D Conversion Data Sign Selection 0: Set when A/D conversion of the self-diagnosis channel is performed 1: Set when A/D conversion of the channel other than the self-diagnosis is performed	R/W
31:21	—	These bits are read as 0. The write value should be 0.	R/W

The ADDOPCRCn register is one of the registers that selects the data calculation function to the A/D conversion data of virtual channel n.

LIMTBLS[3:0] bits (Limiter Clip Table Selection)

LIMTBLS[3:0] bits select the limiter clip table for clipping the A/D conversion data of virtual channel n. When LIMTBLS[3:0] bits are set to 0x0, the A/D conversion data is not clipped. When LIMTBLS[3:0] bits are set to any of 0x1 to 0x8, the A/D conversion data is clipped according to the limiter clip table selected by LIMTBLS[3:0] bits.

ADPRC[1:0] bits (A/D Conversion Data Format Selection)

ADPRC[1:0] bits select the data length of A/D conversion data. The A/D conversion data of virtual channel n is stored to the A/D Data Register or the FIFO with selected data length.

SIGNSEL bit (A/D Conversion Data Sign Selection)

SIGNSEL bit must be set to 0 when A/D conversion of the self-diagnosis channel is performed.

SIGNSEL bit must be set to 1 when A/D conversion of the channel other than the self-diagnosis is performed.

36.2.4 A/D Conversion Configuration

36.2.4.1 ADSGDCRn : Scan Group Diagnosis Function Control Register n (n = 0 to 8)

Base address: ADC_B = 0x4017_0000

Offset address: 0x200 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	ADNDIS[3:0]				—	—	ADDISN	ADDISP	—	—	—	ADDISEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	DIAGVAL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	LIMTBLS[3:0]	限制器剪辑表选择 0x0：不使用限制器剪辑表0x1：使用限制器剪辑表00x2：使用限制器剪辑表10x3：使用限制器剪辑表2 ⋮ 0x8：使用限制器剪辑表7 其他：禁止设置	R/W
15:4	—	这些位被读取为0。写入值应为0。	R/W
17:16	ADPRC[1:0]	AD转换数据格式选择 00：将AD转换结果存储为16位数据格式01：将AD转换结果存储为14位数据格式10：将AD转换结果存储为12位数据格式11：存储AD转换结果作为10位数据格式	R/W
19:18	—	这些位被读取为0。写入值应为0。	R/W
20	SIGNSEL	AD转换数据符号选择 0：自诊断通道进行AD转换时置位1：自诊断以外的通道进行AD转换时置位	R/W
31:21	—	这些位被读取为0。写入值应为0。	R/W

ADDOPCRCn寄存器是选择对虚拟通道n的AD转换数据进行数据计算功能的寄存器之一。

LIMTBLS[3:0]位（限制器剪辑表选择）

LIMTBLS[3:0]位选择限幅器削波表，用于削波虚拟通道n的AD转换数据。什么时候LIMTBLS[3:0]位设置为0x0，AD转换数据不被剪裁。当LIMTBLS[3:0]位设置为0x1到0x8中的任何一个时，AD转换数据将根据LIMTBLS[3:0]位选择的限制器剪辑表进行剪辑。

ADPRC[1:0]位（AD转换数据格式选择）

ADPRC[1:0]位选择AD转换数据的数据长度。虚拟通道n的AD转换数据以选定的数据长度存储到AD数据寄存器或FIFO。

SIGNSEL位（AD转换数据符号选择）

进行自诊断通道的AD转换时，SIGNSEL位必须设置为0。

进行自诊断以外的通道的AD转换时，SIGNSEL位必须设置为1。

36.2.4 AD转换配置

36.2.4.1 ADSGDCRn：扫描组诊断功能控制寄存器n（n=0至8）

Base address: ADC_B = 0x4017_0000

Offset address: 0x200 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	ADNDIS[3:0]				—	—	ADDISN	ADDISP	—	—	—	ADDISEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	DIAGVAL[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	DIAGVAL[2:0]	Self-diagnosis Mode Selection 0 0 0: Set when any Self-diagnosis channel are not included. Setting prohibited when any Self-diagnosis channels are included. 1 0 0: Self-diagnosis mode 1 1 0 1: Self-diagnosis mode 2 1 1 0: Self-diagnosis mode 3 Others: Setting prohibited	R/W
15:3	—	These bits are read as 0. The write value should be 0.	R/W
16	ADDISEN	Disconnection Detection Assist Enable 0: Disable the Disconnection Detection Assist function 1: Enable the Disconnection Detection Assist function	R/W
19:17	—	These bits are read as 0. The write value should be 0.	R/W
20	ADDISP	Disconnection Detection Assist Mode Selection (for the even-numbered analog channel) 0: Discharge 1: Precharge	R/W
21	ADDISN	Disconnection Detection Assist Mode Selection (for the odd-numbered analog channel) 0: Discharge 1: Precharge	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W
27:24	ADNDIS[3:0]	Disconnection Detection Assist Period 0x0: Setting prohibited when the Disconnection Detection Assist function is enabled 0x1: Setting prohibited 0x2: Setting prohibited Others: The number of states for the discharge or precharge period	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The ADSGDCRn register controls the diagnosis function at the scanning operation of scan group n.

DIAGVAL[2:0] bits (Self-diagnosis Mode Selection)

DIAGVAL[2:0] bits select the self-diagnosis mode for A/D converter.

DIAGVAL[2:0]bits must be set to 000b when the scan group n is not included any virtual channel that selected the self-diagnosis channel. DIAGVAL[2:0] bits must be set to 100b, 101b or 110b when the scan group n is including the virtual channel that selected the self-diagnosis channel.

ADDISEN bit (Disconnection Detection Assist Enable)

ADDISEN bit enables/disables the disconnection detection assist function. When ADDISEN bit is set to 0, the disconnection detection assist operation is not performed. When ADDISEN bit is set to 1, the disconnection detection assist operation according to the setting of ADDISP bit and ADDISN bit is performed at the scanning operation of scan group n.

ADDISP bit / ADDISN bit (Disconnection Detection Assist Mode Selection)

ADDISP bit and ADDISN bit select the discharge/precharge operation for the disconnection detection.

ADDISP bit selects the discharge/precharge operation for the even-numbered analog channel.

ADDISN bit selects the discharge/precharge operation for the odd-numbered analog channel.

ADNDIS[3:0] bits (Disconnection Detection Assist Period)

ADNDIS[3:0] bits select the discharge/precharge period. When the disconnection detection assist function is disabled (ADDISEN = 0), ADNDIS[3:0] should be set to 0x0. When the disconnection detection assist function is enabled (ADDISEN = 1),ADNDIS[3:0] should be set to a number between 0x3 and 0xF as the number of state for the discharge/precharge period.

Bit	Symbol	Function	R/W
2:0	DIAGVAL[2:0]	自诊断模式选择 000：不包含任何自诊断通道时置位。 包含自诊断通道时禁止设置。 1 0 0: Self-diagnosis mode 1 1 0 1: Self-diagnosis mode 2 1 1 0: Self-diagnosis mode 3 其他：禁止设置	R/W
15:3	—	这些位被读取为0。写入值应为0。	R/W
16	ADDISEN	断线检测辅助启用 0：关闭断线检测辅助功能1：开启断线检测辅助功能	R/W
19:17	—	这些位被读取为0。写入值应为0。	R/W
20	ADDISP	断线检测辅助模式选择（偶数模拟通道） 0: Discharge 1: Precharge	R/W
21	ADDISN	断线检测辅助模式选择（奇数模拟通道） 0: Discharge 1: Precharge	R/W
23:22	—	这些位被读取为0。写入值应为0。	R/W
27:24	ADNDIS[3:0]	断线检测辅助期间 0x0：断线检测辅助功能有效时禁止设置0x1：禁止设置0x2：禁止设置 其他：放电或预充电期的状态数	R/W
31:28	—	这些位被读取为0。写入值应为0。	R/W

ADSGDCRn寄存器在扫描组n的扫描操作中控制诊断功能。

DIAGVAL[2:0]位（自诊断模式选择）

DIAGVAL[2:0]位选择AD转换器的自诊断模式。

当扫描组n不包括任何选择自诊断通道的虚拟通道时，DIAGVAL[2:0]位必须设置为000b。当扫描组n包含选择自诊断通道的虚拟通道时，DIAGVAL[2:0]位必须设置为100b、101b或110b。

ADDISEN位（断线检测辅助使能）

ADDISEN位启用禁用断线检测辅助功能。当ADDISEN位设置为0时，不执行断线检测辅助操作。当ADDISEN位设置为1时，根据ADDISP位和ADDISN位的设置，在扫描组n的扫描操作中执行断线检测辅助操作。

ADDISP位ADDISN位（断线检测辅助模式选择）

ADDISP位和ADDISN位选择放电预充电操作以进行断线检测。

ADDISP位选择偶数模拟通道的放电预充电操作。

ADDISN位选择奇数模拟通道的放电预充电操作。

ADNDIS[3:0]位（断线检测辅助周期）

ADNDIS[3:0]位选择放电预充电周期。当断线检测辅助功能被禁用（ADDISEN=0）时，ADNDIS[3:0]应设置为0x0。当断线检测辅助功能启用时（ADDISEN=1），ADNDIS[3:0]应设置为0x3和0xF之间的数字作为放电预充电期的状态数。

36.2.4.2 ADSSTR0 : Sampling State Table Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0x240

Bit position:	31						25									16									9								0
Bit field:	—	—	—	—	—	—	SST1[9:0]									—	—	—	—	—	—	SST0[9:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	

Bit	Symbol	Function	R/W
9:0	SST0[9:0]	Sampling State Table 0 These bits set the sampling time in the range from 2 to 1023 states.	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
25:16	SST1[9:0]	Sampling State Table 1 These bits set the sampling time in the range from 2 to 1023 states.	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

The ADSSTR0 register selects the sampling time at the A/D conversion that is using each sampling state table.

36.2.4.3 ADSSTR1 : Sampling State Table Register 1

Base address: ADC_B = 0x4017_0000

Offset address: 0x244

Bit position:	31						25									16									9								0
Bit field:	—	—	—	—	—	—	SST3[9:0]									—	—	—	—	—	—	SST2[9:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	

Bit	Symbol	Function	R/W
9:0	SST2[9:0]	Sampling State Table 2 These bits set the sampling time in the range from 2 to 1023 states.	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
25:16	SST3[9:0]	Sampling State Table 3 These bits set the sampling time in the range from 2 to 1023 states.	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

The ADSSTR1 register selects the sampling time at the A/D conversion that is using each sampling state table.

36.2.4.4 ADSSTR2 : Sampling State Table Register 2

Base address: ADC_B = 0x4017_0000

Offset address: 0x248

Bit position:	31						25									16									9								0
Bit field:	—	—	—	—	—	—	SST5[9:0]									—	—	—	—	—	—	SST4[9:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	

Bit	Symbol	Function	R/W
9:0	SST4[9:0]	Sampling State Table 4 These bits set the sampling time in the range from 2 to 1023 states.	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W

36.2.4.2 ADSSTR0：采样状态表寄存器0

Base address: ADC_B = 0x4017_0000

Offset address: 0x240

Bit position:	31						25									16									9								0
Bit field:	—	—	—	—	—	—	SST1[9:0]									—	—	—	—	—	—	SST0[9:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	

Bit	Symbol	Function	R/W
9:0	SST0[9:0]	采样状态表0 这些位在2到1023个状态范围内设置采样时间。	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W
25:16	SST1[9:0]	采样状态表1 这些位在2到1023个状态范围内设置采样时间。	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

ADSSTR0寄存器选择使用每个采样状态表的AD转换时的采样时间。

36.2.4.3 ADSSTR1：采样状态表寄存器1

Base address: ADC_B = 0x4017_0000

Offset address: 0x244

Bit position:	31						25									16									9								0
Bit field:	—	—	—	—	—	—	SST3[9:0]									—	—	—	—	—	—	SST2[9:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	

Bit	Symbol	Function	R/W
9:0	SST2[9:0]	采样状态表2 这些位在2到1023个状态范围内设置采样时间。	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W
25:16	SST3[9:0]	采样状态表3 这些位在2到1023个状态范围内设置采样时间。	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

ADSSTR1寄存器选择使用每个采样状态表的AD转换时的采样时间。

36.2.4.4 ADSSTR2：采样状态表寄存器2

Base address: ADC_B = 0x4017_0000

Offset address: 0x248

Bit position:	31						25									16									9								0
Bit field:	—	—	—	—	—	—	SST5[9:0]									—	—	—	—	—	—	SST4[9:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	

Bit	Symbol	Function	R/W
9:0	SST4[9:0]	采样状态表4 这些位在2到1023个状态范围内设置采样时间。	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
25:16	SST5[9:0]	Sampling State Table 5 These bits set the sampling time in the range from 2 to 1023 states.	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

The ADSSTR2 register selects the sampling time at the A/D conversion that is using each sampling state table.

36.2.4.5 ADSSTR3 : Sampling State Table Register 3

Base address: ADC_B = 0x4017_0000

Offset address: 0x24C

Bit position:	31						25									16									9								0
Bit field:	—	—	—	—	—	—	SST7[9:0]									—	—	—	—	—	—	SST6[9:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	

Bit	Symbol	Function	R/W
9:0	SST6[9:0]	Sampling State Table 6 These bits set the sampling time in the range from 2 to 1023 states.	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
25:16	SST7[9:0]	Sampling State Table 7 These bits set the sampling time in the range from 2 to 1023 states.	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

The ADSSTR3 register selects the sampling time at the A/D conversion that is using each sampling state table.

36.2.4.6 ADSSTR4 : Sampling State Table Register 4

Base address: ADC_B = 0x4017_0000

Offset address: 0x250

Bit position:	31						25									16									9								0
Bit field:	—	—	—	—	—	—	SST9[9:0]									—	—	—	—	—	—	SST8[9:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	

Bit	Symbol	Function	R/W
9:0	SST8[9:0]	Sampling State Table 8 These bits set the sampling time in the range from 2 to 1023 states.	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
25:16	SST9[9:0]	Sampling State Table 9 These bits set the sampling time in the range from 2 to 1023 states.	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

The ADSSTR4 register selects the sampling time at the A/D conversion that is using each sampling state table.

Bit	Symbol	Function	R/W
25:16	SST5[9:0]	采样状态表5 这些位在2到1023个状态范围内设置采样时间。	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

ADSSTR2寄存器选择使用每个采样状态表的AD转换时的采样时间。

36.2.4.5 ADSSTR3：采样状态表寄存器3

Base address: ADC_B = 0x4017_0000

Offset address: 0x24C

Bit position:	31						25									16									9								0
Bit field:	—	—	—	—	—	—	SST7[9:0]									—	—	—	—	—	—	SST6[9:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	

Bit	Symbol	Function	R/W
9:0	SST6[9:0]	采样状态表6 这些位在2到1023个状态范围内设置采样时间。	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W
25:16	SST7[9:0]	采样状态表7 这些位在2到1023个状态范围内设置采样时间。	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

ADSSTR3寄存器选择使用每个采样状态表的AD转换时的采样时间。

36.2.4.6 ADSSTR4：采样状态表寄存器4

Base address: ADC_B = 0x4017_0000

Offset address: 0x250

Bit position:	31						25									16									9								0
Bit field:	—	—	—	—	—	—	SST9[9:0]									—	—	—	—	—	—	SST8[9:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	

Bit	Symbol	Function	R/W
9:0	SST8[9:0]	采样状态表8 这些位在2到1023个状态范围内设置采样时间。	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W
25:16	SST9[9:0]	采样状态表9 这些位在2到1023个状态范围内设置采样时间。	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

ADSSTR4寄存器选择使用每个采样状态表的AD转换时的采样时间。

36.2.4.7 ADSSTR5 : Sampling State Table Register 5

Base address: ADC_B = 0x4017_0000

Offset address: 0x254

Bit position:	31						25										16										9										0
Bit field:	—	—	—	—	—	—	SST11[9:0]										—	—	—	—	—	—	SST10[9:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0				

Bit	Symbol	Function	R/W
9:0	SST10[9:0]	Sampling State Table 10 These bits set the sampling time in the range from 2 to 1023 states.	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
25:16	SST11[9:0]	Sampling State Table 11 These bits set the sampling time in the range from 2 to 1023 states.	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

The ADSSTR5 register selects the sampling time at the A/D conversion that is using each sampling state table.

36.2.4.8 ADSSTR6 : Sampling State Table Register 6

Base address: ADC_B = 0x4017_0000

Offset address: 0x258

Bit position:	31						25										16										9										0
Bit field:	—	—	—	—	—	—	SST13[9:0]										—	—	—	—	—	—	SST12[9:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0				

Bit	Symbol	Function	R/W
9:0	SST12[9:0]	Sampling State Table 12 These bits set the sampling time in the range from 2 to 1023 states.	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
25:16	SST13[9:0]	Sampling State Table 13 These bits set the sampling time in the range from 2 to 1023 states.	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

The ADSSTR6 register selects the sampling time at the A/D conversion that is using each sampling state table.

36.2.4.9 ADSSTR7 : Sampling State Table Register 7

Base address: ADC_B = 0x4017_0000

Offset address: 0x25C

Bit position:	31						25										16										9										0
Bit field:	—	—	—	—	—	—	SST15[9:0]										—	—	—	—	—	—	SST14[9:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0				

Bit	Symbol	Function	R/W
9:0	SST14[9:0]	Sampling State Table 14 These bits set the sampling time in the range from 2 to 1023 states.	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W

36.2.4.7 ADSSTR5：采样状态表寄存器5

Base address: ADC_B = 0x4017_0000

Offset address: 0x254

Bit position:	31						25										16										9										0
Bit field:	—	—	—	—	—	—	SST11[9:0]										—	—	—	—	—	—	SST10[9:0]														
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0				

Bit	Symbol	Function	R/W
9:0	SST10[9:0]	采样状态表10 这些位在2到1023个状态范围内设置采样时间。	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W
25:16	SST11[9:0]	采样状态表11 这些位在2到1023个状态范围内设置采样时间。	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

ADSSTR5寄存器选择使用每个采样状态表的AD转换时的采样时间。

36.2.4.8 ADSSTR6：采样状态表寄存器6

Base address: ADC_B = 0x4017_0000

Offset address: 0x258

Bit position:	31						25										16										9										0
Bit field:	—	—	—	—	—	—	SST13[9:0]										—	—	—	—	—	—	SST12[9:0]														
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0				

Bit	Symbol	Function	R/W
9:0	SST12[9:0]	采样状态表12 这些位在2到1023个状态范围内设置采样时间。	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W
25:16	SST13[9:0]	采样状态表13 这些位在2到1023个状态范围内设置采样时间。	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

ADSSTR6寄存器选择使用每个采样状态表的AD转换时的采样时间。

36.2.4.9 ADSSTR7：采样状态表寄存器7

Base address: ADC_B = 0x4017_0000

Offset address: 0x25C

Bit position:	31						25										16										9										0
Bit field:	—	—	—	—	—	—	SST15[9:0]										—	—	—	—	—	—	SST14[9:0]														
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0				

Bit	Symbol	Function	R/W
9:0	SST14[9:0]	采样状态表14 这些位在2到1023个状态范围内设置采样时间。	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
25:16	SST15[9:0]	Sampling State Table 15 These bits set the sampling time in the range from 2 to 1023 states.	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

The ADSSTR7 register selects the sampling time at the A/D conversion that is using each sampling state table.

36.2.4.10 ADCNVSTR : A/D Conversion State Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x260

Bit position:	31																		13					8		5				0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CST1[5:0]					—	—	CST0[5:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
5:0	CST0[5:0]	A/D Converter Unit 0 (ADC0) A/D successive approximation time configuration These bits set the successive approximation time in the range from 3 to 63 states.	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
13:8	CST1[5:0]	A/D Converter Unit 1 (ADC1) A/D successive approximation time configuration These bits set the successive approximation time in the range from 3 to 63 states.	R/W
31:14	—	These bits are read as 0. The write value should be 0.	R/W

The ADCNVSTR register specifies the A/D successive approximation time, which required by the A/D converter Unit 0 or Unit 1 to convert the sampled analog input to the digital value, in the number of cycles based on A/D conversion clock (ADCLK). The A/D successive approximation time does not include the sampling time of the analog input.

The A/D successive approximation time must be set to meet the value specified in section 46, Electrical Characteristics. If the successive approximation time is set to a value over the range specified for the electrical characteristics, the A/D conversion result is not guaranteed. In addition, the A/D successive approximation time for each A/D converter should be set to be the same. (Set the same value to CST0[5:0] bits and CST1[5:0] bits).

36.2.5 S&H, PGA and Others

36.2.5.1 ADSHCR0 : Channel-Dedicated Sample-and-Hold Circuit Control Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0x280

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SHEN2	SHEN1	SHEN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
25:16	SST15[9:0]	采样状态表15 这些位在2到1023个状态范围内设置采样时间。	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

ADSSTR7寄存器选择使用每个采样状态表的AD转换时的采样时间。

36.2.4.10 ADCNVSTR:AD转换状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x260

Bit position:	31																		13					8		5				0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CST1[5:0]					—	—	CST0[5:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
5:0	CST0[5:0]	AD转换器单元0(ADC0) AD逐次逼近时间配置 这些位在3到63个状态范围内设置逐次逼近时间。	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
13:8	CST1[5:0]	AD转换器单元1(ADC1) AD逐次逼近时间配置 这些位在3到63个状态范围内设置逐次逼近时间。	R/W
31:14	—	这些位被读取为0。写入值应为0。	R/W

ADCNVSTR寄存器指定AD逐次逼近时间，这是AD转换器单元0或
单元1将采样的模拟输入转换为数字值，其周期数基于AD转换时钟(ADCLK)。AD逐次逼近时间不包括模拟输入的采样时间。

AD逐次逼近时间必须设置为满足第46节“电气特性”中规定的值。如果将逐次逼近时间设置为超出电气特性指定范围的值，则无法保证AD转换结果。此外，每个AD转换器的AD逐次逼近时间应设置为相同。（将相同的值设置为CST0[5:0]位和CST1[5:0]位）。

36.2.5 S&H、PGA等

36.2.5.1 ADSHCR0：通道专用采样保持电路控制寄存器0

Base address: ADC_B = 0x4017_0000

Offset address: 0x280

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SHEN2	SHEN1	SHEN0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SHEN0	Channel-Dedicated Sample-and-Hold Circuit Unit 0 Select 0: Bypass the circuit unit 0 1: Use the circuit unit 0	R/W
1	SHEN1	Channel-Dedicated Sample-and-Hold Circuit Unit 1 Select 0: Bypass the circuit unit 1 1: Use the circuit unit 1	R/W
2	SHEN2	Channel-Dedicated Sample-and-Hold Circuit Unit 2 Select 0: Bypass the circuit unit 2 1: Use the circuit unit 2	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

The ADSHCR0 register controls the Channel-Dedicated Sample-and-Hold circuits (unit 0, unit 1 and unit 2) connected to the A/D converter unit 0 (ADC0).

SHENn bit (Channel-Dedicated Sample-and-Hold Circuit Bypass Select) (n = 0 to 2)

The SHENn bit selects whether to use or bypass the Channel-Dedicated Sample-and-Hold circuits unit n. When the SHENn bit is set to 0, the Channel-dedicated Sample-and-Hold circuits unit n is disabled.

If A/D conversion of analog input channel to which the Channel-Dedicated Sample-and-Hold circuit unit n is performed, the Channel-Dedicated Sample-and-Hold circuit is not used and is bypassed.

When the SHENn bit is set to 1, the Channel-Dedicated Sample-and-Hold circuits unit n is enabled. In this case, A/D conversion of analog input channel to which the Channel-Dedicated Sample-and-Hold circuit unit n is performed with the Channel-Dedicated Sample-and-Hold circuit used.

36.2.5.2 ADSHCR1 : Channel-Dedicated Sample-and-Hold Circuit Control Register 1

Base address: ADC_B = 0x4017_0000

Offset address: 0x28C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SHEN6	SHEN5	SHEN4
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SHEN4	Channel-Dedicated Sample-and-Hold Circuit Unit 4 Select 0: Bypass the circuit unit 4 1: Use the circuit unit 4	R/W
1	SHEN5	Channel-Dedicated Sample-and-Hold Circuit Unit 5 Select 0: Bypass the circuit unit 5 1: Use the circuit unit 5	R/W
2	SHEN6	Channel-Dedicated Sample-and-Hold Circuit Unit 6 Select 0: Bypass the circuit unit 6 1: Use the circuit unit 6	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

The ADSHCR1 register controls the Channel-Dedicated Sample-and-Hold circuits (unit 4, unit 5 and unit 6) connected to the A/D converter unit 1 (ADC1).

Bit	Symbol	Function	R/W
0	SHEN0	通道专用采样保持电路单元0选择 0：绕过电路单元01：使用电路单元0	R/W
1	SHEN1	通道专用采样保持电路单元1选择 0：绕过电路单元11：使用电路单元1	R/W
2	SHEN2	通道专用采样保持电路单元2选择 0：绕过电路单元21：使用电路单元2	R/W
31:3	—	这些位被读取为0。写入值应为0。	R/W

ADSHCR0寄存器控制连接到AD转换器单元0(ADC0)的通道专用采样保持电路（单元0、单元1和单元2）。

SHENn位（通道专用采样保持电路旁路选择）（n=0至2）

SHENn位选择是使用还是绕过通道专用采样保持电路单元n。当SHENn位设置为0时，通道专用的采样保持电路单元n被禁用。

如果对通道专用采样保持电路单元n执行的模拟输入通道进行AD转换，则
通道专用的采样保持电路未使用并被旁路。

当SHENn位设置为1时，通道专用采样保持电路单元n被使能。在这种情况下，通道专用采样保持电路单元n使用的通道专用采样保持电路对其执行模拟输入通道的AD转换。

36.2.5.2 ADSHCR1：通道专用采样保持电路控制寄存器1

Base address: ADC_B = 0x4017_0000

Offset address: 0x28C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SHEN6	SHEN5	SHEN4
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SHEN4	通道专用采样保持电路单元4选择 0：绕过电路单元41：使用电路单元4	R/W
1	SHEN5	通道专用采样保持电路单元5选择 0：绕过电路单元51：使用电路单元5	R/W
2	SHEN6	通道专用采样保持电路单元6选择 0：绕过电路单元61：使用电路单元6	R/W
31:3	—	这些位被读取为0。写入值应为0。	R/W

ADSHCR1寄存器控制连接到AD转换器单元1(ADC1)的通道专用采样保持电路（单元4、单元5和单元6）。

SHENn bit (Channel-Dedicated Sample-and-Hold Circuit Bypass Select) (n = 4 to 6)

The SHENn bit selects whether to use or bypass the Channel-Dedicated Sample-and-Hold circuits unit n. When the SHENn bit is set to 0, the Channel-dedicated Sample-and-Hold circuits unit n is disabled.

If A/D conversion of analog input channel to which the Channel-Dedicated Sample-and-Hold circuit unit n is performed, the Channel-Dedicated Sample-and-Hold circuit is not used and is bypassed.

When the SHENn bit is set to 1, the Channel-Dedicated Sample-and-Hold circuits unit n is enabled. In this case, A/D conversion of analog input channel to which the Channel-Dedicated Sample-and-Hold circuit unit n is performed with the Channel-Dedicated Sample-and-Hold circuit used.

36.2.5.3 ADSHSTR0 : Channel-Dedicated Sample & Hold Circuit State Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0x288

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SHHST[2:0]			—	—	—	—	—	—	—	—	SHSST[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
7:0	SHSST[7:0]	Channel-Dedicated Sample-and-Hold Circuit Unit 0 to 2 Sampling Time Setting These bits set the sampling time in the range from 4 to 255 states.	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W
18:16	SHHST[2:0]	Channel-Dedicated Sample-and-Hold Circuit Unit 0 to 2 Hold Mode Switching Time Setting These bits set the hold mode switching time in the range from 2 to 7 states.	R/W
31:19	—	These bits are read as 0. The write value should be 0.	R/W

The ADSHSTR0 register specifies the sampling time and the hold mode switching time for the Channel-Dedicated Sample-and-Hold circuits (unit 0, unit 1, and unit 2) connected to the A/D converter unit 0 (ADC0). The value set in this register should be set to meet the value specified in section 46, Electrical Characteristics.

36.2.5.4 ADSHSTR1 : Channel-Dedicated Sample & Hold Circuit State Register 1

Base address: ADC_B = 0x4017_0000

Offset address: 0x294

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SHHST[2:0]			—	—	—	—	—	—	—	—	SHSST[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
7:0	SHSST[7:0]	Channel-Dedicated Sample-and-Hold Circuit Unit 4 to 6 Sampling Time Setting These bits set the sampling time in the range from 4 to 255 states.	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W
18:16	SHHST[2:0]	Channel-Dedicated Sample-and-Hold Circuit Unit 4 to 6 Hold Mode Switching Time Setting These bits set the hold mode switching time in the range from 2 to 7 states.	R/W
31:19	—	These bits are read as 0. The write value should be 0.	R/W

SHENn位（通道专用采样保持电路旁路选择）（n=4至6）

SHENn位选择是使用还是绕过通道专用采样保持电路单元n。当SHENn位设置为0时，通道专用的采样保持电路单元n被禁用。

如果对通道专用采样保持电路单元n执行的模拟输入通道进行AD转换，则
通道专用的采样保持电路未使用并被旁路。

当SHENn位设置为1时，通道专用采样保持电路单元n被使能。在这种情况下，通道专用采样保持电路单元n使用的通道专用采样保持电路对其执行模拟输入通道的AD转换。

36.2.5.3 ADSHSTR0：通道专用采样和保持电路状态寄存器0

Base address: ADC_B = 0x4017_0000

Offset address: 0x288

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SHHST[2:0]			—	—	—	—	—	—	—	—	SHSST[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
7:0	SHSST[7:0]	通道专用采样保持电路单元0至2 采样时间设置 这些位在4到255个状态范围内设置采样时间。	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W
18:16	SHHST[2:0]	通道专用采样保持电路单元0至2 保持模式切换时间设置 这些位在2到7个状态范围内设置保持模式切换时间。	R/W
31:19	—	这些位被读取为0。写入值应为0。	R/W

ADSHSTR0寄存器指定连接到AD转换器单元0(ADC0)的通道专用采样保持电路（单元0、单元1和单元2）的采样时间和保持模式切换时间。该寄存器中设置的值应设置为符合第46节“电气特性”中指定的值。

36.2.5.4 ADSHSTR1：通道专用采样和保持电路状态寄存器1

Base address: ADC_B = 0x4017_0000

Offset address: 0x294

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SHHST[2:0]			—	—	—	—	—	—	—	—	SHSST[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
7:0	SHSST[7:0]	通道专用采样保持电路单元4至6 采样时间设置 这些位在4到255个状态范围内设置采样时间。	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W
18:16	SHHST[2:0]	通道专用采样保持电路单元4至6 保持模式切换时间设置 这些位在2到7个状态范围内设置保持模式切换时间。	R/W
31:19	—	这些位被读取为0。写入值应为0。	R/W

The ADSHSTR1 register specifies the sampling time and the hold mode switching time for the Channel-Dedicated Sample-and-Hold circuits (unit 4, unit 5, and unit 6) connected to the A/D converter unit 1 (ADC1). The value set in this register should be set to meet the value specified in section 46, Electrical Characteristics.

36.2.5.5 ADPGACRn : Programmable Gain Amplifier Control Register n (n = 0 to 3)

Base address: ADC_B = 0x4017_0000

Offset address: 0x2C0 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	PGAGAIN[3:0]				—	—	PGADG[1:0]		—	—	—	PGAGEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	PGAENAMP	PGASEL1	PGADEN	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1*1	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	PGADEN	PGA Unit n Input Mode Select*1 0: Single-ended Input mode 1: Pseudo Differential Input mode	R/W
2	PGASEL1	PGA Unit n Transit Enable 0: Not output the signal in a path through the PGA 1: Output the signal in a path through the PGA	R/W
3	PGAENAMP	PGA Unit n Enable 0: Disable the PGA 1: Enable the PGA	R/W
15:4	—	These bits are read as 0. The write value should be 0.	R/W
16	PGAGEN	PGA Unit n Gain Setting Enable 0: Disable gain setting 1: Enable gain setting	R/W
19:17	—	These bits are read as 0. The write value should be 0.	R/W
21:20	PGADG[1:0]	PGA Unit n Differential Input Gain Setting When PGA is Single-ended Input mode, set 00b. When PGA is Pseudo Differential Input mode, select the following values: 0 0: × 1.500 0 1: × 2.333 1 0: × 4.000 1 1: × 5.667	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W

ADSHSTR1寄存器指定连接到AD转换器单元1(ADC1)的通道专用采样保持电路（单元4、单元5和单元6）的采样时间和保持模式切换时间。该寄存器中设置的值应设置为符合第46节“电气特性”中指定的值。

36.2.5.5 ADPGACRn：可编程增益放大器控制寄存器n（n=0至3）

Base address: ADC_B = 0x4017_0000

Offset address: 0x2C0 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	PGAGAIN[3:0]				—	—	PGADG[1:0]		—	—	—	PGAGEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	PGAENAMP	PGASEL1	PGADEN	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1*1	0

Bit	Symbol	Function	R/W
0	—	该位读取为0。写入值应为0。	R/W
1	PGADEN	PGA单元n输入模式选择*1 0：单端输入模式1：伪差分输入模式	R/W
2	PGASEL1	PGA单元n传输启用 0：不通过PGA的路径输出信号1：通过PGA的路径输出信号	R/W
3	PGAENAMP	PGA单元n启用 0：禁用PGA1：启用PGA	R/W
15:4	—	这些位被读取为0。写入值应为0。	R/W
16	PGAGEN	PGA单元n增益设置启用 0：禁用增益设置1：启用增益设置	R/W
19:17	—	这些位被读取为0。写入值应为0。	R/W
21:20	PGADG[1:0]	PGA单元n差分输入增益设置 当PGA为单端输入模式时，设置为00b。 当PGA为伪差分输入模式时，选择以下值： 0 0: × 1.500 0 1: × 2.333 1 0: × 4.000 1 1: × 5.667	R/W
23:22	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
27:24	PGAGAIN[3:0]	PGA Unit n Gain Setting 0x00: × 2.000 (PGA is Single-ended Input mode) Setting prohibited (PGA is Pseudo Differential Input mode) 0x01: × 2.500 (PGA is Single-ended Input mode) × 1.500 (PGA is Pseudo Differential Input mode) 0x02: × 2.667 (PGA is Single-ended Input mode) Setting prohibited (PGA is Pseudo Differential Input mode) 0x03: × 2.857 (PGA is Single-ended Input mode) Setting prohibited (PGA is Pseudo Differential Input mode) 0x04: × 3.077 (PGA is Single-ended Input mode) Setting prohibited (PGA is Pseudo Differential Input mode) 0x05: × 3.333 (PGA is Single-ended Input mode) × 2.333 (PGA is Pseudo Differential Input mode) 0x06: × 3.636 (PGA is Single-ended Input mode) Setting prohibited (PGA is Pseudo Differential Input mode) 0x07: × 4.000 (PGA is Single-ended Input mode) Setting prohibited (PGA is Pseudo Differential Input mode) 0x08: × 4.444 (PGA is Single-ended Input mode) Setting prohibited (PGA is Pseudo Differential Input mode) 0x09: × 5.000 (PGA is Single-ended Input mode) × 4.000 (PGA is Pseudo Differential Input mode) 0x0A: × 5.714 (PGA is Single-ended Input mode) Setting prohibited (PGA is Pseudo Differential Input mode) 0x0B: × 6.667 (PGA is Single-ended Input mode) × 5.667 (PGA is Pseudo Differential Input mode) 0x0C: × 8.000 (PGA is Single-ended Input mode) Setting prohibited (PGA is Pseudo Differential Input mode) 0x0D: × 10.000 (PGA is Single-ended Input mode) Setting prohibited (PGA is Pseudo Differential Input mode) 0x0E: × 13.333 (PGA is Single-ended Input mode) Setting prohibited (PGA is Pseudo Differential Input mode) 0x0F: Setting prohibited	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The initial value after reset depends on the user setting of Option Function Select Register 1 in Option Setting Memory.

The ADPGACRn register controls the Programmable Gain Amplifier Unit n.

PGADEN bit (PGA Unit n Input Mode Select)

PGADEN bit selects the Single-ended Input mode or the Pseudo Differential Input mode for PGA unit n.

PGASEL1 bit (PGA Unit n Transit Enable)

PGASEL1 bit controls the output of the PGA unit n.

PGAENAMP bit (PGA Unit n Enable)

PGAENAMP controls the power-on of the amplifier in the PGA unit n. When 1 is set to the PGAENAMP bit, the amplifier in the PGA unit n is enabled.

PGAGEN bit (PGA Unit n Gain Setting Enable)

PGAGEN bit enables or disables the gain setting for PGA unit n.

PGADG[1:0] bits (PGA Unit n Differential Input Gain Setting)

PGADG[1:0] bits specify the gain of the amplifier in the PGA Unit n in Pseudo Differential Input mode. These bits are used in combination with PGAGAIN[3:0].

PGAGAIN[3:0] bits (PGA Unit n Gain Setting)

PGAGAIN[3:0] bits specify the gain of the amplifier in the PGA Unit n. In Pseudo Differential Input mode (PGADEN = 1 and PGAGEN = 1), these bits are used in combination with PGADG[1:0].

Bit	Symbol	Function	R/W
27:24	PGAGAIN[3:0]	PGA单元n增益设置 0x00：×2.000（PGA为单端输入模式） 设置禁止（PGA为伪差分输入模式） 0x01：×2.500（PGA为单端输入模式） ×1.500（PGA为伪差分输入模式） 0x02：×2.667（PGA为单端输入模式） 设置禁止（PGA为伪差分输入模式） 0x03：×2.857（PGA为单端输入模式） 设置禁止（PGA为伪差分输入模式） 0x04：×3.077（PGA为单端输入模式） 设置禁止（PGA为伪差分输入模式） 0x05：×3.333（PGA为单端输入模式） ×2.333（PGA为伪差分输入模式） 0x06：×3.636（PGA为单端输入模式） 设置禁止（PGA为伪差分输入模式） 0x07：×4.000（PGA为单端输入模式） 设置禁止（PGA为伪差分输入模式） 0x08：×4.444（PGA为单端输入模式） 设置禁止（PGA为伪差分输入模式） 0x09：×5.000（PGA为单端输入模式） ×4.000（PGA为伪差分输入模式） 0x0A：×5.714（PGA为单端输入模式） 设置禁止（PGA为伪差分输入模式） 0x0B：×6.667（PGA为单端输入模式） ×5.667（PGA为伪差分输入模式） 0x0C：×8.000（PGA为单端输入模式） 设置禁止（PGA为伪差分输入模式） 0x0D：×10.000（PGA为单端输入模式） 设置禁止（PGA为伪差分输入模式） 0x0E：×13.333（PGA为单端输入模式） 设置禁止（PGA为伪差分输入模式） 0x0F：禁止设置	R/W
31:28	—	这些位被读取为0。写入值应为0。	R/W

注1.复位后的初始值取决于选项设置存储器中选项功能选择寄存器1的用户设置。

ADPGACRn寄存器控制可编程增益放大器单元n。

PGADEN位（PGA单元n输入模式选择）

PGADEN位选择PGA单元n的单端输入模式或伪差分输入模式。

PGASEL1位（PGA单元n传输使能）

PGASEL1位控制PGA单元n的输出。

PGAENAMP位（PGA单元n启用）

PGAENAMP控制PGA单元n中放大器的通电。当PGAENAMP位设置为1时，启用PGA单元n中的放大器。

PGAGEN位（PGA单元n增益设置使能）

PGAGEN位启用或禁用PGA单元n的增益设置。

PGADG[1:0]位（PGA单元n差分输入增益设置）

PGADG[1:0]位指定伪差分输入模式下PGA单元n中放大器的增益。这些位与PGAGAIN[3:0]结合使用。

PGAGAIN[3:0]位（PGA单元n增益设置）

PGAGAIN[3:0]位指定PGA单元n中放大器的增益。在伪差分输入模式下（PGADEN=1和PGAGEN=1），这些位与PGADG[1:0]结合使用。

36.2.5.6 ADPGAMONCR : Programable Gain Amp Monitor Output Control Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x300

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	MONSEL3	MONSEL2	MONSEL1	MONSEL0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	PGAMON[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	PGAMON[2:0]	PGA Monitor Signal Selection 0x0: Not select monitor signal (Hi-Z) 0x1: PGA output Others: Setting prohibited	R/W
15:3	—	These bits are read as 0. The write value should be 0.	R/W
16	MONSEL0	PGA Unit 0 Monitor Output Enable 0: Disable monitor output 1: Enable monitor output	R/W
17	MONSEL1	PGA Unit 1 Monitor Output Enable 0: Disable monitor output 1: Enable monitor output	R/W
18	MONSEL2	PGA Unit 2 Monitor Output Enable 0: Disable monitor output 1: Enable monitor output	R/W
19	MONSEL3	PGA Unit 3 Monitor Output Enable 0: Disable monitor output 1: Enable monitor output	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The ADPGAMONCR register controls the PGA monitor output function for the PGA analog input and output signals.

PGAMON[2:0] bits (PGA Monitor Signal Selection)

PGAMON[2:0] bits select which analog signal is output from the I/O port pin. This setting is applied to all of the PGA units.

MONSELn bit (PGA Monitor Output Setting) (n = 0 to 3)

MONSELn bit enables or disables the monitor output function of the PGA unit n. When the MONSELn bit is set to 0, no analog signal for the PGA unit n is monitored out. When the MONSELn is set to 1, the analog signal selected by PGAMON[2:0] for the PGA unit n can be monitored on the I/O port pin.

Note: It is also required to configure the I/O ports. For details, see section 18, I/O Ports.

36.2.5.7 ADREFCR : Internal Reference Voltage Monitor Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x320

Bit position:	31	…	1	0
Bit field:	—	…	—	VDE
Value after reset:	0	…	0	0

36.2.5.6 ADPGAMONCR:可编程增益放大器监视器输出控制寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x300

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	MONSEL3	MONSEL2	MONSEL1	MONSEL0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	PGAMON[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	PGAMON[2:0]	PGA监视器信号选择 0x0：不选择监控信号（Hi-Z）0x1：PGA输出 其他：禁止设置	R/W
15:3	—	这些位被读取为0。写入值应为0。	R/W
16	MONSEL0	PGA单元0监视器输出使能 0：禁用监控输出1：启用监控输出	R/W
17	MONSEL1	PGA单元1监视器输出使能 0：禁用监控输出1：启用监控输出	R/W
18	MONSEL2	PGA单元2监视器输出使能 0：禁用监控输出1：启用监控输出	R/W
19	MONSEL3	PGA单元3监视器输出使能 0：禁用监控输出1：启用监控输出	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

ADPGAMONCR寄存器控制PGA模拟输入和输出信号的PGA监视器输出功能。

PGAMON[2:0]位（PGA监视器信号选择）

PGAMON[2:0]位选择从IO端口引脚输出的模拟信号。此设置适用于所有PGA单元。

MONSELn位（PGA监视器输出设置）（n=0至3）

MONSELn位启用或禁用PGA单元n的监视输出功能。当MONSELn位设置为0时，不会监测到PGA单元n的模拟信号。当MONSELn设置为1时，由PGAMON[2:0]为PGA单元n选择的模拟信号可以在IO端口引脚上进行监视。

Note: 还需要配置IO端口。有关详细信息，请参阅第18节，IO端口。

36.2.5.7 ADREFCR:内部参考电压监视器使能寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x320

Bit position:	31	…	1	0
Bit field:	—	…	—	VDE
重置后的值:	0	…	0	0

Bit	Symbol	Function	R/W
0	VDE	Internal Reference Voltage A/D Conversion Select 0: Disable A/D conversion of internal reference voltage 1: Enable A/D conversion of internal reference voltage	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

The ADREFCR register controls the function of the internal reference voltage circuit. When the A/D conversion of the internal reference voltage is performed, the VDE bit must be set to 1.

36.2.6 Self-Calibration

36.2.6.1 ADCALSTCR : A/D Converter Self-Calibration State Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x264

Bit position:	31									21						16						9								0
Bit field:	—	—	—	—	—	—	—	—	—	CALADCST[5:0]						—	—	—	—	—	—	CALADSST[9:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
9:0	CALADSST[9:0]	A/D Converter Self-Calibration Sampling Time Configuration These bits set the sampling time in the range from 2 to 1023 states.	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
21:16	CALADCST[5:0]	A/D Converter Self-Calibration Successive Approximation Time Configuration. These bits set the successive approximation time in the range from 3 to 63 states.	R/W
31:22	—	These bits are read as 0. The write value should be 0.	R/W

The ADCALSTCR register specifies the sampling and the A/D successive approximation times at the self-calibration operation for all A/D converter (ADC0, ADC1). The sampling time and successive approximation time should be set by the number of clock cycles based on the A/D conversion clock (ADCLK) to meet the values specified in section 46, Electrical Characteristics.

36.2.6.2 ADCALSHCR : Channel-Dedicated Sample & Hold Circuit Self-Calibration State Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x2B0

Bit position:	31												18	16								7								0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	CALSHHST[2:0]		—	—	—	—	—	—	—	CALSHSST[7:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
7:0	CALSHSST[7:0]	Channel-Dedicated Sample & Hold Circuit Self-Calibration Sampling Time Configuration These bits set the sampling time in the range from 5 to 255 states.	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
0	VDE	内部参考电压AD转换选择 0：禁止内部参考电压AD转换1：使能内部参考电压AD转换	R/W
31:1	—	这些位被读取为0。写入值应为0。	R/W

ADREFCR寄存器控制内部参考电压电路的功能。当执行内部参考电压的AD转换时，VDE位必须设置为1。

36.2.6 Self-Calibration

36.2.6.1 ADCALSTCR:AD转换器自校准状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x264

Bit position:	31									21						16						9								0
Bit field:	—	—	—	—	—	—	—	—	—	CALADCST[5:0]						—	—	—	—	—	—	CALADSST[9:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
9:0	CALADSST[9:0]	AD转换器自校准采样时间配置 这些位在2到1023个状态范围内设置采样时间。	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W
21:16	CALADCST[5:0]	AD转换器自校准逐次逼近时间配置。 这些位在3到63个状态范围内设置逐次逼近时间。	R/W
31:22	—	这些位被读取为0。写入值应为0。	R/W

ADCALSTCR寄存器指定所有AD转换器（ADC0、ADC1）在自校准操作中的采样和AD逐次逼近时间。采样时间和逐次逼近时间应由基于AD转换时钟(ADCLK)的时钟周期数设置，以满足第46节“电气特性”中规定的值。

36.2.6.2 ADCALSHCR：通道专用采样和保持电路自校准状态 Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x2B0

Bit position:	31												18	16								7								0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	CALSHHST[2:0]		—	—	—	—	—	—	—	CALSHSST[7:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
7:0	CALSHSST[7:0]	通道专用采样保持电路自校准采样时间配置 这些位在5到255个状态范围内设置采样时间。	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
18:16	CALSHHST[2:0]	Channel-Dedicated Sample & Hold Circuit Self-Calibration Hold Mode Switching Time Configuration These bits set the hold mode switching time in the range from 2 to 7 states.	R/W
31:19	—	These bits are read as 0. The write value should be 0.	R/W

The ADCALSHCR register specifies the sampling time and the hold mode switching time at the self-calibration operation for all Channel-dedicated sample-and-hold circuits (SH0 to SH2, SH4 to SH6). The sampling time and the hold mode switching time should be set by the number of clock cycles based on the A/D conversion clock (ADCLK) to meet the values specified in section 46, Electrical Characteristics.

36.2.6.3 ADUOFTRn : User Offset Table Register n (n = 0 to 7)

Base address: ADC_B = 0x4017_0000

Offset address: 0x360 + 0x04 × n

Bit position:	31															15														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UOFSET[15:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	UOFSET[15:0]	User Offset Table n 0x7FFF: + 32767 0x7FFE: + 32766 ⋮ 0x0002: + 2 0x0001: + 1 0x0000: 0 (without user offset) 0xFFFF: - 1 0xFFFE: - 2 ⋮ 0x8001: - 32767 0x8000: - 32768	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The ADUOFTRn register specifies the offset value in the User Offset Table n.

36.2.6.4 ADUGTRn : User Gain Table Register n (n = 0 to 7)

Base address: ADC_B = 0x4017_0000

Offset address: 0x380 + 0x04 × n

Bit position:	31								23																				0
Bit field:	—	—	—	—	—	—	—	—	UGAIN[23:0]																				
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
23:0	UGAIN[23:0]	User Gain Table n These bits set the gain value to be multiplied by the A/D conversion result. b23-b22: Integer part of gain b21-b0: Fractional part of gain	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

The ADUGTRn register specifies the gain value in the User Gain Table n.

36.2.7 Limiter Clip Function

Bit	Symbol	Function	R/W
18:16	CALSHHST[2:0]	通道专用采样和保持电路自校准保持模式切换时间 Configuration 这些位在2到7个状态范围内设置保持模式切换时间。	R/W
31:19	—	这些位被读取为0。写入值应为0。	R/W

ADCALSHCR寄存器指定所有通道专用采样保持电路（SH0至SH2、SH4至SH6）在自校准操作时的采样时间和保持模式切换时间。采样时间和保持模式切换时间应由基于AD转换时钟(ADCLK)的时钟周期数设置，以满足第46节"电气特性"中规定的值。

36.2.6.3 ADUOFTRn：用户偏移表寄存器n（n=0到7）

Base address: ADC_B = 0x4017_0000

Offset address: 0x360 + 0x04 × n

Bit position:	31															15														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UOFSET[15:0]														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	UOFSET[15:0]	用户偏移表n0x7FFF:+327670 x7FFE:+32766 0x0002:+20x00 01:+10x0000:0（无用户偏移 ）0xFFFF:10xFFFE:2 0x8001:3 27670x8000:32768	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

ADUOFTRn寄存器指定用户偏移表n中的偏移值。

36.2.6.4 ADUGTRn：用户增益表寄存器n（n=0到7）

Base address: ADC_B = 0x4017_0000

Offset address: 0x380 + 0x04 × n

Bit position:	31								23																				0
Bit field:	—	—	—	—	—	—	—	—	UGAIN[23:0]																				
重置后的值:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
23:0	UGAIN[23:0]	用户增益表n 这些位设置要乘以AD转换结果的增益值。b23-b22：增益的整数部分b21-b0：增益的小数部分	R/W
31:24	—	这些位被读取为0。写入值应为0。	R/W

ADUGTRn寄存器指定用户增益表n中的增益值。

36.2.7 限制器剪辑功能

36.2.7.1 ADLIMINTCR : Limiter Clip Interrupt Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x3A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LIMIEn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LIMIEn	Limiter Clip Interrupt n Enable bit 0: Disable the Limiter clip interrupt n 1: Enable the Limiter clip interrupt n	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 8

The ADLIMINTCR register enables/disables the Limiter clip interrupt n.

36.2.7.2 ADLIMTRn : Limiter Clip Table Register n (n = 0 to 7)

Base address: ADC_B = 0x4017_0000

Offset address: 0x3A4 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	LIMU[15:0]																LIML[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	LIML[15:0]	Limiter clip table n : Lower-side limit value	R/W
31:16	LIMU[15:0]	Limiter clip table n : Upper-side limit value	R/W

The ADLIMTRn register specifies the lower- and upper-side limit value of the limiter clip table n.

36.2.7.3 ADLIMGRSR : Limiter Clip Scan Group Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LIMGRFn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

36.2.7.1 ADLIMINTCR:限制器剪辑中断使能寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x3A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LIMIEn								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LIMIEn	限制器剪辑中断n使能位 0：禁用Limiter剪辑中断n1：启用Limiter剪辑中断n	R/W
31:9	—	这些位被读取为0。写入值应为0。	R/W

Note: n = 0 to 8

ADLIMINTCR寄存器启用禁用限制器剪辑中断n。

36.2.7.2 ADLIMTRN:限制器剪辑表寄存器n(n=0到7)

Base address: ADC_B = 0x4017_0000

Offset address: 0x3A4 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	LIMU[15:0]																LIML[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	LIML[15:0]	限制器剪辑表n：下限限制值	R/W
31:16	LIMU[15:0]	限制器剪辑表n：上限值	R/W

ADLIMTRn寄存器指定限制器剪辑表n的下限值和上限值。

36.2.7.3 ADLIMGRSR：限制器剪辑扫描组状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xD28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LIMGRFn								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LIMGRFn	Scan Group n Limiter Clip Flag 0: Limiter clip for scan group n is not detected 1: Limiter clip for scan group n is detected	R
31:9	—	These bits are read as 0.	R

Note: n = 0 to 8

The ADLIMGRSR register indicates whether the limiter clip occurred in the scanning operation for scan group n. Each flag can be cleared in the ADLIMGRSCR.

36.2.7.4 ADLIMCHSR0 : Limiter Clip Channel Status Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD2C

Bit position:	31			28																								0
Bit field:	—	—	—	LIMCHFn																								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	LIMCHFn	Analog Channel No. n : Limiter Clip Flag bit 0: Limiter clip is not detected 1: Limiter clip is detected	R
31:29	—	These bits are read as 0.	R

Note: n = 0 to 28

The ADLIMCHSR0 register indicates whether the limiter clip occurred when the A/D conversion for the analog channel n is performed. Each flag can be cleared in ADLIMCHSCR0.

36.2.7.5 ADLIMEXSR : Extended Analog Limiter Clip Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LIMEXF8	LIMEXF7	LIMEXF6	LIMEXF5	—	—	LIMEXF2	LIMEXF1	LIMEXF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	LIMEXF0	Self-Diagnosis Channel : Limiter Clip Flag bit 0: Limiter clip is not detected 1: Limiter clip is detected	R
1	LIMEXF1	Temperature Sensor Channel : Limiter Clip Flag bit 0: Limiter clip is not detected 1: Limiter clip is detected	R
2	LIMEXF2	Internal Reference Voltage Channel : Limiter Clip Flag bit 0: Limiter clip is not detected 1: Limiter clip is detected	R
4:3	—	These bits are read as 0.	R

Bit	Symbol	Function	R/W
8:0	LIMGRFn	扫描组n限制器剪辑标志 0：未检测到扫描组n的限制器剪辑1：检测到扫描组n的限制器剪辑	R
31:9	—	这些位读为0。	R

Note: n = 0 to 8

ADLIMGRSR寄存器指示限制器剪辑是否发生在扫描组n的扫描操作中。每个标志都可以在ADLIMGRSCR中清除。

36.2.7.4 ADLIMCHSR0：限制器剪辑通道状态寄存器0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD2C

Bit position:	31			28																								0
Bit field:	—	—	—	LIMCHFn																								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	LIMCHFn	模拟通道编号n：限幅器剪辑标志位 0：未检测到限幅剪辑1：检测到限幅剪辑	R
31:29	—	这些位读为0。	R

Note: n = 0 to 28

ADLIMCHSR0寄存器指示在对模拟通道n执行AD转换时是否发生限幅器削波。每个标志都可以在ADLIMCHSCR0中清除。

36.2.7.5 ADLIMEXSR:扩展模拟限制器剪辑状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xD38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LIMEXF8	LIMEXF7	LIMEXF6	LIMEXF5	—	—	LIMEXF2	LIMEXF1	LIMEXF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	LIMEXF0	自诊断通道：限幅剪辑标志位 0：未检测到限幅剪辑1：检测到限幅剪辑	R
1	LIMEXF1	温度传感器通道：限制器削波标志位 0：未检测到限幅剪辑1：检测到限幅剪辑	R
2	LIMEXF2	内部参考电压通道：限幅器削波标志位 0：未检测到限幅剪辑1：检测到限幅剪辑	R
4:3	—	这些位读为0。	R

Bit	Symbol	Function	R/W
5	LIMEXF5	D/A Converter 0 Channel : Limiter Clip Flag bit 0: Limiter clip is not detected 1: Limiter clip is detected	R
6	LIMEXF6	D/A Converter 1 Channel : Limiter Clip Flag bit 0: Limiter clip is not detected 1: Limiter clip is detected	R
7	LIMEXF7	D/A Converter 2 Channel : Limiter Clip Flag bit 0: Limiter clip is not detected 1: Limiter clip is detected	R
8	LIMEXF8	D/A Converter 3 Channel : Limiter Clip Flag bit 0: Limiter clip is not detected 1: Limiter clip is detected	R
31:9	—	These bits are read as 0.	R

The ADLIMEXSR register indicates whether the limiter clip occurred when the A/D conversion for the extended analog function (which channel no. is 96 to 98, 101 to 104) is performed. Each flag can be cleared in the ADLIMEXSCR.

36.2.7.6 ADLIMGRSCR : Limiter Clip Scan Group Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD3C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LIMGRCn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LIMGRCn	Scan Group n Limiter Clip Flag Clear 0: No effect 1: ADLIMGRSR.LIMGRFn is cleared	W
31:9	—	The write value should be 0.	W

Note: n = 0 to 8

The ADLIMGRSCR register clears the limiter clip flag for scan group n (ADLIMGRSR.LIMGRFn).

36.2.7.7 ADLIMCHSCR0 : Limiter Clip Channel Status Clear Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD40

Bit position:	31			28																										0
Bit field:	—	—	—	LIMCHCn																										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	LIMCHCn	Analog Channel No. n Limiter Clip Flag Clear bit 0: No effect 1: ADLIMCHSR0.LIMCHFn is cleared	W

Bit	Symbol	Function	R/W
5	LIMEXF5	DA转换器0通道：限幅器剪辑标志位 0：未检测到限幅剪辑1：检测到限幅剪辑	R
6	LIMEXF6	DA转换器1通道：限幅器剪辑标志位 0：未检测到限幅剪辑1：检测到限幅剪辑	R
7	LIMEXF7	DA转换器2通道：限幅器剪辑标志位 0：未检测到限幅剪辑1：检测到限幅剪辑	R
8	LIMEXF8	DA转换器3通道：限幅器剪辑标志位 0：未检测到限幅剪辑1：检测到限幅剪辑	R
31:9	—	这些位读为0。	R

ADLIMEXSR寄存器指示在执行扩展模拟功能（通道号为96至98、101至104）的AD转换时是否发生限幅器削波。每个标志都可以在ADLIMEXSCR中清除。

36.2.7.6 ADLIMGRSCR：限制器剪辑扫描组状态清除寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xD3C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LIMGRCn								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LIMGRCn	扫描组n限制器剪辑标志清除 0：无效1：ADLIMGRSR.LIMGRFn清零	W
31:9	—	写入值应为0。	W

Note: n = 0 to 8

ADLIMGRSCR寄存器清除扫描组n的限制器剪辑标志(ADLIMGSR.LIMGRFn)。

36.2.7.7 ADLIMCHSCR0：限制器剪辑通道状态清除寄存器0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD40

Bit position:	31			28																										0
Bit field:	—	—	—	LIMCHCn																										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	LIMCHCn	模拟通道编号n限制器削波标志清除位 0：无效1：ADLIMCHSR0.LIMCHFn清零	W

Bit	Symbol	Function	R/W
31:29	—	The write value should be 0.	W

Note: n = 0 to 28

The ADLIMCHSCR0 register clears the limiter clip flag for the analog channel n (ADLIMCHSR0.LIMCHFn).

36.2.7.8 ADLIMEXSCR : Extended Analog Limiter Clip Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD4C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LIMEXF8	LIMEXF7	LIMEXF6	LIMEXF5	—	—	LIMEXF2	LIMEXF1	LIMEXF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	LIMEXF0	Self-Diagnosis Channel : Limiter Clip Flag Clear 0: No effect 1: ADLIMEXSR.LIMEXF0 is cleared	W
1	LIMEXF1	Temperature Sensor Channel : Limiter Clip Flag Clear 0: No effect 1: ADLIMEXSR.LIMEXF1 is cleared	W
2	LIMEXF2	Internal Reference Voltage Channel : Limiter Clip Flag Clear 0: No effect 1: ADLIMEXSR.LIMEXF2 is cleared	W
4:3	—	The write value should be 0.	W
5	LIMEXF5	D/A Converter 0 Channel : Limiter Clip Flag Clear 0: No effect 1: ADLIMEXSR.LIMEXF5 is cleared	W
6	LIMEXF6	D/A Converter 1 Channel : Limiter Clip Flag Clear 0: No effect 1: ADLIMEXSR.LIMEXF6 is cleared	W
7	LIMEXF7	D/A Converter 2 Channel : Limiter Clip Flag Clear 0: No effect 1: ADLIMEXSR.LIMEXF7 is cleared	W
8	LIMEXF8	D/A Converter 3 Channel : Limiter Clip Flag Clear 0: No effect 1: ADLIMEXSR.LIMEXF8 is cleared	W
31:9	—	The write value should be 0.	W

The ADLIMCHEXSCR0 register clears the limiter clip flag for the extended analog function.

36.2.8 Compare Match Function

Bit	Symbol	Function	R/W
31:29	—	写入值应为0。	W

Note: n = 0 to 28

ADLIMCHSCR0寄存器清除模拟通道n(ADLIMCHSR0.LIMCHFn)的限制器削波标志。

36.2.7.8 ADLIMEXSCR：扩展模拟限制器剪辑状态清除寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xD4C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LIMEXF8	LIMEXF7	LIMEXF6	LIMEXF5	—	—	LIMEXF2	LIMEXF1	LIMEXF0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	LIMEXF0	自诊断通道：限制器剪辑标志清除 0：无效1：ADLIMEXSR.LIMEXF0清零	W
1	LIMEXF1	温度传感器通道：限制器剪辑标志清除 0：无效1：ADLIMEXSR.LIMEXF1清零	W
2	LIMEXF2	内部参考电压通道：限制器削波标志清除 0：无效1：ADLIMEXSR.LIMEXF2清零	W
4:3	—	写入值应为0。	W
5	LIMEXF5	DA转换器0通道：限制器剪辑标志清除 0：无效1：ADLIMEXSR.LIMEXF5清零	W
6	LIMEXF6	DA转换器1通道：限制器剪辑标志清除 0：无效1：ADLIMEXSR.LIMEXF6清零	W
7	LIMEXF7	DA转换器2通道：限制器剪辑标志清除 0：无效1：ADLIMEXSR.LIMEXF7清零	W
8	LIMEXF8	DA转换器3通道：限制器剪辑标志清除 0：无效1：ADLIMEXSR.LIMEXF8清零	W
31:9	—	写入值应为0。	W

ADLIMCHEXSCR0寄存器清除扩展模拟功能的限制器剪辑标志。

36.2.8 比较匹配函数

36.2.8.1 ADCMPENR : Compare Match Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x400

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	CMPENn							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CMPENn	Compare Match n Enable 0: Disable the compare match n 1: Enable the compare match n	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 7

The ADCMPENR register enables/disables the compare match n.

36.2.8.2 ADCMPINTCR : Compare Match Interrupt Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x404

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	CMPIEn			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CMPIEn	Compare Match Interrupt n Enable 0: Disable the Compare Match interrupt n 1: Enable the Compare Match interrupt n	R/W
31:4	—	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 3

The ADCMPINTCR register enables/disables the Compare Match interrupt n.

36.2.8.1 ADCMPENR:比较匹配使能寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x400

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	CMPENn							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CMPENn	比较匹配n启用 0：禁用比较匹配n1：启用比较匹配n	R/W
31:8	—	这些位被读取为0。写入值应为0。	R/W

Note: n = 0 to 7

ADCMPENR寄存器使能禁用比较匹配n。

36.2.8.2 ADCMPINTCR:比较匹配中断使能寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x404

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	CMPIEn			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CMPIEn	比较匹配中断n使能 0：禁止比较匹配中断n1：使能比较匹配中断n	R/W
31:4	—	这些位被读取为0。写入值应为0。	R/W

Note: n = 0 to 3

ADCMPINTCR寄存器使能禁用比较匹配中断n。

36.2.8.3 ADCCMPCRn : Composite Compare Match Configuration Register n (n = 0, 1)

Base address: ADC_B = 0x4017_0000

Offset address: 0x408 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	CCMPTBLm							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CCMPCND[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CCMPCND[1:0]	Composite Compare Match Condition Selection 0 0: Logical disjunction (OR) conditions 0 1: Logical conjunction (AND) conditions 1 0: Logical exclusive disjunction (EXOR) conditions 1 1: Setting prohibited	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
23:16	CCMPTBLm	Composite Compare Match Condition Table Selection 0: Not use the Compare Match Table m 1: Use the Compare Match table m	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

Note: m = 0 to 7

The ADCCMPCRn register configures the conditions for the Composite Compare Match interrupt n.

CCMPCND[1:0] bits (Composite Compare Match Condition Selection)

CCMPCND[1:0] bits select the generating condition for the Composite Compare Match interrupt n.

CCMPTBLm bits (Composite Compare Match Condition Table Selection)

CCMPTBLm bits select whether to use or not to use the Compare Match table m as the generating conditions of the Composite Compare Match interrupt.

36.2.8.4 ADCMPMDR0 : Compare Match Mode Selection Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0x448

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	CMPMD3[1:0]		—	—	—	—	—	—	CMPMD2[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPMD1[1:0]		—	—	—	—	—	—	CMPMD0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

36.2.8.3 ADCCMPCRn：复合比较匹配配置寄存器n(n=0 1)

Base address: ADC_B = 0x4017_0000

Offset address: 0x408 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	CCMPTBLm							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CCMPCND[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CCMPCND[1:0]	复合比较匹配条件选择 00：逻辑或（OR）条件01：逻辑与（AND）条件10 ：逻辑异或（EXOR）条件11：禁止设置	R/W
15:2	—	这些位被读取为0。写入值应为0。	R/W
23:16	CCMPTBLm	复合比较匹配条件表选择 0：不使用比较匹配表m1：使用比较匹 配表m	R/W
31:24	—	这些位被读取为0。写入值应为0。	R/W

Note: m = 0 to 7

ADCCMPCRn寄存器配置复合比较匹配中断n的条件。

CCMPCND[1:0]位（复合比较匹配条件选择）

CCMPCND[1:0]位选择复合比较匹配中断n的产生条件。

CCMPTBLm位（复合比较匹配条件表选择）

CCMPTBLm位选择是否使用比较匹配表m作为生成条件
复合比较匹配中断。

36.2.8.4 ADCMPMDR0：比较匹配模式选择寄存器0

Base address: ADC_B = 0x4017_0000

Offset address: 0x448

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	CMPMD3[1:0]		—	—	—	—	—	—	CMPMD2[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPMD1[1:0]		—	—	—	—	—	—	CMPMD0[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CMPMD0[1:0]	Compare Match 0 : Match Mode Selection 0 0: Generate the match when more than high-side level 0 1: Generate the match when less than low-side level 1 0: Generate the match when more than high-side level or less than low-side level 1 1: Generate the match when it is in the range from low-side level to high-side level	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
9:8	CMPMD1[1:0]	Compare Match 1 : Match Mode Selection 0 0: Generate the match when more than high-side level 0 1: Generate the match when less than low-side level 1 0: Generate the match when more than high-side level or less than low-side level 1 1: Generate the match when it is in the range from low-side level to high-side level	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
17:16	CMPMD2[1:0]	Compare Match 2 : Match Mode Selection 0 0: Generate the match when more than high-side level 0 1: Generate the match when less than low-side level 1 0: Generate the match when more than high-side level or less than low-side level 1 1: Generate the match when it is in the range from low-side level to high-side level	R/W
23:18	—	These bits are read as 0. The write value should be 0.	R/W
25:24	CMPMD3[1:0]	Compare Match 3 : Match Mode Selection 0 0: Generate the match when more than high-side level 0 1: Generate the match when less than low-side level 1 0: Generate the match when more than high-side level or less than low-side level 1 1: Generate the match when it is in the range from low-side level to high-side level	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

The ADCMPMDR0 register selects the generating condition of each compare match event.

36.2.8.5 ADCMPMDR1 : Compare Match Mode Selection Register 1

Base address: ADC_B = 0x4017_0000

Offset address: 0x44C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	CMPMD7[1:0]		—	—	—	—	—	—	CMPMD6[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPMD5[1:0]		—	—	—	—	—	—	CMPMD4[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CMPMD4[1:0]	Compare Match 4 : Match Mode Selection 0 0: Generate the match when more than high-side level 0 1: Generate the match when less than low-side level 1 0: Generate the match when more than high-side level or less than low-side level 1 1: Generate the match when it is in the range from low-side level to high-side level	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
9:8	CMPMD5[1:0]	Compare Match 5 : Match Mode Selection 0 0: Generate the match when more than high-side level 0 1: Generate the match when less than low-side level 1 0: Generate the match when more than high-side level or less than low-side level 1 1: Generate the match when it is in the range from low-side level to high-side level	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
1:0	CMPMD0[1:0]	比较匹配0：匹配模式选择 00：高于高端电平时产生匹配01：低于低端电平时产生匹配10：高于高端电平或低于低端电平时产生匹配11：产生处于从低位电平到高位电平范围内的匹配	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
9:8	CMPMD1[1:0]	比较匹配1：匹配模式选择 00：高于高端电平时产生匹配01：低于低端电平时产生匹配10：高于高端电平或低于低端电平时产生匹配11：产生处于从低位电平到高位电平范围内的匹配	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W
17:16	CMPMD2[1:0]	比较匹配2：匹配模式选择 00：高于高端电平时产生匹配01：低于低端电平时产生匹配10：高于高端电平或低于低端电平时产生匹配11：产生处于从低位电平到高位电平范围内的匹配	R/W
23:18	—	这些位被读取为0。写入值应为0。	R/W
25:24	CMPMD3[1:0]	比较匹配3：匹配模式选择 00：高于高端电平时产生匹配01：低于低端电平时产生匹配10：高于高端电平或低于低端电平时产生匹配11：产生处于从低位电平到高位电平范围内的匹配	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

ADCMPMDR0寄存器选择每个比较匹配事件的产生条件。

36.2.8.5 ADCMPMDR1：比较匹配模式选择寄存器1

Base address: ADC_B = 0x4017_0000

Offset address: 0x44C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	CMPMD7[1:0]		—	—	—	—	—	—	CMPMD6[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPMD5[1:0]		—	—	—	—	—	—	CMPMD4[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CMPMD4[1:0]	比较匹配4：匹配模式选择 00：高于高端电平时产生匹配01：低于低端电平时产生匹配10：高于高端电平或低于低端电平时产生匹配11：产生处于从低位电平到高位电平范围内的匹配	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
9:8	CMPMD5[1:0]	比较匹配5：匹配模式选择 00：高于高端电平时产生匹配01：低于低端电平时产生匹配10：高于高端电平或低于低端电平时产生匹配11：产生处于从低位电平到高位电平范围内的匹配	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
17:16	CMPMD6[1:0]	Compare Match 6 : Match Mode Selection 0 0: Generate the match when more than high-side level 0 1: Generate the match when less than low-side level 1 0: Generate the match when more than high-side level or less than low-side level 1 1: Generate the match when it is in the range from low-side level to high-side level	R/W
23:18	—	These bits are read as 0. The write value should be 0.	R/W
25:24	CMPMD7[1:0]	Compare Match 7 : Match Mode Selection 0 0: Generate the match when more than high-side level 0 1: Generate the match when less than low-side level 1 0: Generate the match when more than high-side level or less than low-side level 1 1: Generate the match when it is in the range from low-side level to high-side level	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

The ADCMPMDR1 register selects the generating condition of each compare match event.

36.2.8.6 ADCMPTBRn : Compare Match Table Register n (n = 0 to 7)

Base address: ADC_B = 0x4017_0000

Offset address: 0x458 + 0x04 × n

Bit position:	31															16	15													0
Bit field:	CMPTBH[15:0]																CMPTBL[15:0]														
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPTBL[15:0]	Compare Match Table n : Low-side level Set CMPTBH > CMPTBL	R/W
31:16	CMPTBH[15:0]	Compare Match Table n : High-side level Set CMPTBH > CMPTBL	R/W

The ADCMPTBRn register specifies the low-side level and the high-side level for the Compare Match Table n.

36.2.8.7 ADCMPTBSR : Compare Match Table Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	CMPTBFn							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CMPTBFn	Compare Match Table n Match Flag 0: Match event with compare match table n is not detected 1: Match event with compare match table n is detected	R
31:8	—	These bits are read as 0.	R

Note: n = 0 to 7

Bit	Symbol	Function	R/W
17:16	CMPMD6[1:0]	比较匹配6：匹配模式选择 00：高于高端电平时产生匹配01：低于低端电平时产生匹配10：高于高端电平或低于低端电平时产生匹配11：产生处于从低位电平到高位电平范围内的匹配	R/W
23:18	—	这些位被读取为0。写入值应为0。	R/W
25:24	CMPMD7[1:0]	比较匹配7：匹配模式选择 00：高于高端电平时产生匹配01：低于低端电平时产生匹配10：高于高端电平或低于低端电平时产生匹配11：产生处于从低位电平到高位电平范围内的匹配	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

ADCMPMDR1寄存器选择每个比较匹配事件的产生条件。

36.2.8.6 ADCMPTBRn：比较匹配表寄存器n（n=0到7）

Base address: ADC_B = 0x4017_0000

Offset address: 0x458 + 0x04 × n

Bit position:	31															16	15													0
Bit field:	CMPTBH[15:0]																CMPTBL[15:0]														
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPTBL[15:0]	比较匹配表n：低端电平 Set CMPTBH > CMPTBL	R/W
31:16	CMPTBH[15:0]	比较匹配表n：高侧电平 Set CMPTBH > CMPTBL	R/W

ADCMPTBRn寄存器指定比较匹配表n的低端电平和高端电平。

36.2.8.7 ADCMPTBSR:比较匹配表状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xD00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	CMPTBFn							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CMPTBFn	比较匹配表n匹配标志 0：未检测到与比较匹配表n的匹配事件1：检测到与比较匹配表n的匹配事件	R
31:8	—	这些位读为0。	R

Note: n = 0 to 7

The ADCMPTBSR register indicates whether the match event with the Compare Match Table n occurred during the A/D conversion. Each flag can be cleared in the ADCMPTBSCR.

36.2.8.8 ADCMPTBSCR : Compare Match Table Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	CMPTBCn							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CMPTBCn	Compare Match Table n : Match Flag Clear 0: No effect 1: ADCMPTBSR.CMPTBFn is cleared	W
31:8	—	The write value should be 0.	W

Note: n = 0 to 7

The ADCMPTBSCR register clears the match flag for the compare match n (ADCMPTBSR.CMPTBFn).

36.2.8.9 ADCMPCHSR0 : Compare Match Channel Status Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD08

Bit position:	31	28	0
Bit field:	—	—	—	CMPCHFn
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	CMPCHFn	Analog Channel No. n : Compare Match Flag 0: Compare match is not detected 1: Compare match is detected	R
31:29	—	These bits are read as 0.	R

Note: n = 0 to 28

The ADCMPCHSR0 register indicates whether the compare match event for the Analog Channel No. n is detected. Each flag can be cleared in ADCMPCHSCR0.

ADCMPTBSR寄存器指示在AD转换期间是否发生了与比较匹配表n的匹配事件。每个标志都可以在ADCMPTBSCR中清除。

36.2.8.8 ADCMPTBSCR:比较匹配表状态清除寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xD04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	CMPTBCn							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CMPTBCn	比较匹配表n：匹配标志清除 0：无效1：ADCMPTBSR.CMPTBFn清零	W
31:8	—	写入值应为0。	W

Note: n = 0 to 7

ADCMPTBSCR寄存器清除比较匹配n(ADCMPTBSR.CMPTBFn)的匹配标志。

36.2.8.9 ADCMPCHSR0：比较匹配通道状态寄存器0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD08

Bit position:	31	28	0
Bit field:	—	—	—	CMPCHFn
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	CMPCHFn	模拟通道编号n：比较匹配标志 0：未检测到比较匹配1：检测到比较匹配	R
31:29	—	这些位读为0。	R

Note: n = 0 to 28

ADCMPCHSR0寄存器指示是否检测到模拟通道编号n的比较匹配事件。每个标志都可以在ADCMPCHSCR0中清除。

36.2.8.10 ADCMPEXSR : Extended Analog Compare Match Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPEXF8	CMPEXF7	CMPEXF6	CMPEXF5	—	—	CMPEXF2	CMPEXF1	CMPEXF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPEXF0	Self-Diagnosis Channel : Compare Match Flag 0: Compare match is not detected 1: Compare match is detected	R
1	CMPEXF1	Temperature Sensor Channel : Compare Match Flag 0: Compare match is not detected 1: Compare match is detected	R
2	CMPEXF2	Internal Reference Voltage Channel : Compare Match Flag 0: Compare match is not detected 1: Compare match is detected	R
4:3	—	These bits are read as 0.	R
5	CMPEXF5	D/A Converter 0 Channel : Compare Match Flag 0: Compare match is not detected 1: Compare match is detected	R
6	CMPEXF6	D/A Converter 1 Channel : Compare Match Flag 0: Compare match is not detected 1: Compare match is detected	R
7	CMPEXF7	D/A Converter 2 Channel : Compare Match Flag 0: Compare match is not detected 1: Compare match is detected	R
8	CMPEXF8	D/A Converter 3 Channel : Compare Match Flag 0: Compare match is not detected 1: Compare match is detected	R
31:9	—	These bits are read as 0.	R

The ADCMPEXSR register indicates whether the compare match event for the extended analog function channel is detected. Each flag can be cleared in ADCMPEXSCR.

36.2.8.11 ADCMPCHSCR0 : Compare Match Channel Status Clear Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	CMPCHCn												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPCHCn															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

36.2.8.10 ADCMPEXSR：扩展模拟比较匹配状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xD14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPEXF8	CMPEXF7	CMPEXF6	CMPEXF5	—	—	CMPEXF2	CMPEXF1	CMPEXF0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPEXF0	自诊断通道：比较匹配标志 0：未检测到比较匹配1：检测到比较匹配	R
1	CMPEXF1	温度传感器通道：比较匹配标志 0：未检测到比较匹配1：检测到比较匹配	R
2	CMPEXF2	内部参考电压通道：比较匹配标志 0：未检测到比较匹配1：检测到比较匹配	R
4:3	—	这些位读为0。	R
5	CMPEXF5	DA转换器0通道：比较匹配标志 0：未检测到比较匹配1：检测到比较匹配	R
6	CMPEXF6	DA转换器1通道：比较匹配标志 0：未检测到比较匹配1：检测到比较匹配	R
7	CMPEXF7	DA转换器2通道：比较匹配标志 0：未检测到比较匹配1：检测到比较匹配	R
8	CMPEXF8	DA转换器3通道：比较匹配标志 0：未检测到比较匹配1：检测到比较匹配	R
31:9	—	这些位读为0。	R

ADCMPEXSR寄存器指示是否检测到扩展模拟功能通道的比较匹配事件。每个标志都可以在ADCMPEXSCR中清除。

36.2.8.11 ADCMPCHSCR0：比较匹配通道状态清除寄存器0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	CMPCHCn												
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPCHCn															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	CMPCHCn	Analog Channel No. n : Compare Match Flag Clear bit 0: No effect 1: ADCMPCHSR0.CMPCHFn is cleared	W
31:29	—	The write value should be 0.	W

Note: n = 0 to 28

The ADCMPCHSCR0 register clears the compare match flag for the Analog Channel No.n (ADCMPCHSR0.CMPCHFn).

36.2.8.12 ADCMPEXSCR : Extended Analog Compare Match Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD24

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPEXC	CMPEXC7	CMPEXC6	CMPEXC5	—	—	CMPEXC2	CMPEXC1	CMPEXC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPEXC0	Self-Diagnosis Channel : Compare Match Flag Clear bit 0: No effect 1: ADCMPEXSR.CMPCHF0 is cleared	W
1	CMPEXC1	Temperature Sensor Channel : Compare Match Flag Clear bit 0: No effect 1: ADCMPEXSR.CMPCHF1 is cleared	W
2	CMPEXC2	Internal Reference Voltage Channel : Compare Match Flag Clear bit 0: No effect 1: ADCMPEXSR.CMPCHF2 is cleared	W
4:3	—	The write value should be 0.	W
5	CMPEXC5	D/A Converter 0 Channel : Compare Match Flag Clear bit 0: No effect 1: ADCMPEXSR.CMPCHF5 is cleared	W
6	CMPEXC6	D/A Converter 1 Channel : Compare Match Flag Clear bit 0: No effect 1: ADCMPEXSR.CMPCHF6 is cleared	W
7	CMPEXC7	D/A Converter 2 Channel : Compare Match Flag Clear bit 0: No effect 1: ADCMPEXSR.CMPCHF7 is cleared	W
8	CMPEXC8	D/A Converter 3 Channel : Compare Match Flag Clear bit 0: No effect 1: ADCMPEXSR.CMPCHF8 is cleared	W
31:9	—	The write value should be 0.	W

The ADCMPEXSCR register clears the compare match flag for the Extended Analog Function Channel (ADCMPEXSR.CMPEXFn).

36.2.9 Start and Stop Control of A/D Conversion

Bit	Symbol	Function	R/W
28:0	CMPCHCn	模拟通道编号n：比较匹配标志清除位 0：无效1：ADCMPCHSR0.CMPCHFn清零	W
31:29	—	写入值应为0。	W

Note: n = 0 to 28

ADCMPCHSCR0寄存器清除模拟通道No.n(ADCMPCHSR0.CMPCHFn)的比较匹配标志。

36.2.8.12 ADCMPEXSCR：扩展模拟比较匹配状态清除寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xD24

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPEXC	CMPEXC7	CMPEXC6	CMPEXC5	—	—	CMPEXC2	CMPEXC1	CMPEXC0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPEXC0	自诊断通道：比较匹配标志清除位 0：无效1：ADCMPEXSR.CMPCHF0清零	W
1	CMPEXC1	温度传感器通道：比较匹配标志清除位 0：无效1：ADCMPEXSR.CMPCHF1清零	W
2	CMPEXC2	内部参考电压通道：比较匹配标志清除位 0：无效1：ADCMPEXSR.CMPCHF2清零	W
4:3	—	写入值应为0。	W
5	CMPEXC5	DA转换器0通道：比较匹配标志清零位 0：无效1：ADCMPEXSR.CMPCHF5清零	W
6	CMPEXC6	DA转换器1通道：比较匹配标志清除位 0：无效1：ADCMPEXSR.CMPCHF6清零	W
7	CMPEXC7	DA转换器2通道：比较匹配标志清除位 0：无效1：ADCMPEXSR.CMPCHF7清零	W
8	CMPEXC8	DA转换器3通道：比较匹配标志清除位 0：无效1：ADCMPEXSR.CMPCHF8清零	W
31:9	—	写入值应为0。	W

ADCMPEXSCR寄存器清除扩展模拟功能通道(ADCMPEXSR.CMPEXFn)的比较匹配标志。

36.2.9 AD转换的启动和停止控制

36.2.9.1 ADCALSTR : A/D Converter Self-calibration Start Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	ADCALST1[2:0]*1			—	—	—	—	—	ADCALST0[2:0]*1		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ADCALST0[2:0]*1	A/D Converter Unit 0 (ADC0) Self-calibration Start Control bits [Function of each bit] b0: Start bit of the internal circuit calibration b1: Start bit of the gain and offset calibration b2: Start bit of the Channel-dedicated Sample-and-Hold circuit calibration [Write value] 0: No effect (not start the calibration) 1: Start the calibration	W
7:3	—	The write value should be 0.	W
10:8	ADCALST1[2:0]*1	A/D Converter Unit 1 (ADC1) Self-calibration Start Control bits [Function of each bit] b0: Start bit of the internal circuit calibration b1: Start bit of the gain and offset calibration b2: Start bit of the Channel-dedicated Sample-and-Hold circuit calibration [Write value] 0: No effect (not start the calibration) 1: Start the calibration	W
31:11	—	The write value should be 0.	W

Note 1. To perform a calibration operation, write 1 to each of the calibration start bits simultaneously.

The ADCALSTR register controls the start of the Self-calibration for each A/D converter.

ADCALSTm[2:0] bits (A/D converter Unit m (ADCm) Self-calibration Start Control bits) (m = 0, 1)

ADCALSTm[2:0] bits control the start of the Self-calibration operation of the A/D converter Unit m. When any bit of ADCALSTm[2:0] is set to 1, the Self-calibration operation corresponding to each bit is started. When multiple bits of ADCALSTm[2:0] are set to 1 simultaneously, each self-calibration operation is performed in the order as following:

1. Internal circuit calibration
2. A/D converter gain/offset calibration
3. Channel-specific sample and hold circuit gain/offset calibration

Note: The Self-calibration operation corresponding to the bits set to 0 in ADCALSTm[2:0] is skipped.

ADCALSTm[2:0] bits must be written when all A/D converters are stopped (ADSR.ADACTm = 0 and ADSR.CALACTm = 0);

Writing to ADCALSTm[2:0] bits are prohibited when A/D converters are operating.

36.2.9.1 ADCALSTR:AD转换器自校准启动寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xC00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	ADCALST1[2:0]*1			—	—	—	—	—	ADCALST0[2:0]*1		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ADCALST0[2:0]*1	AD转换器单元0(ADC0)自校准启动控制位[各个位的功能] b0：内部电路校准起始位 b1：增益和偏移校准的起始位 b2：通道专用采样保持电路校准的起始位[写入值] 0：无效（不开始校准）1：开始校准	W
7:3	—	写入值应为0。	W
10:8	ADCALST1[2:0]*1	AD转换器单元1(ADC1)自校准启动控制位[各个位的功能] b0：内部电路校准起始位 b1：增益和偏移校准的起始位 b2：通道专用采样保持电路校准的起始位[写入值] 0：无效（不开始校准）1：开始校准	W
31:11	—	写入值应为0。	W

注1.要执行校准操作，请同时向每个校准起始位写入1。

ADCALSTR寄存器控制每个AD转换器自校准的开始。

ADCALSTm[2:0]位（AD转换器单元m(ADCm)自校准启动控制位） （m=0 1）

ADCALSTm[2:0]位控制AD转换器单元m的自校准操作的开始。当ADCALSTm[2:0]的任何一位设置为1时，将启动每个位对应的自校准操作。当多个位
ADCALSTm[2:0]同时置1，每次自校准操作按如下顺序执行：

1.内部电路校准

2.AD转换器增益偏移校准

3.通道特定的采样保持电路增益偏移校准

Note: 与ADCALSTm[2:0]中设置为0的位对应的自校准操作被跳过。

当所有AD转换器停止时（ADSR.ADACTm=0和ADSR.CALACTm=0），必须写入ADCALSTm[2:0]位；

当AD转换器工作时，禁止写入ADCALSTm[2:0]位。

36.2.9.2 ADSYSTR : A/D Conversion Synchronous Software Start Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ADSYSTn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	ADSYSTn	Scan Group n : A/D Conversion start 0: No effect 1: Start the A/D conversion of scan group n	W
31:9	—	The write value should be 0.	W

Note: n = 0 to 8

The ADSYSTR register controls the start of the A/D conversion of scan group n. This register is used to start the A/D conversions of several scan groups simultaneously by software.

ADSYSTn bit (Scan Group n : A/D Conversion start)

ADSYSTn bit controls the start of the A/D conversion of scan group n. When ADSYSTn bit is set to 1, the A/D conversion of scan group n is started. Setting 0 to ADSYSTn bit has no effect on the operation. Set 1 simultaneously to the ADSYSTn bit of the scan group to start A/D conversion simultaneously.

36.2.9.3 ADSTRn : A/D Conversion Software Start Register n (n = 0 to 8)

Base address: ADC_B = 0x4017_0000

Offset address: 0xC20 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADST	Scan Group n A/D Conversion Start 0: No effect 1: Start the A/D conversion of scan group n	W
31:1	—	The write value should be 0.	W

The ADSTRn register controls the start of the A/D conversion of scan group n. This register is used to start the A/D conversion of a scan group by software.

If A/D conversions of several scan groups are to be started simultaneously by software, the ADSYSTR register should be used.

36.2.9.2 ADSYSTR:AD转换同步软件启动寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xC10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ADSYSTn								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	ADSYSTn	扫描组n：AD转换开始 0：无效1：开始扫描组n的AD转换	W
31:9	—	写入值应为0。	W

Note: n = 0 to 8

ADSYSTR寄存器控制扫描组n的AD转换的开始。该寄存器用于通过软件同时启动多个扫描组的AD转换。

ADSYSTn位（扫描组n：AD转换开始）

ADSYSTn位控制扫描组n的AD转换的开始。当ADSYSTn位设置为1时，开始扫描组n的AD转换。将ADSYSTn位设置为0对操作没有影响。同时将扫描组的ADSYSTn位设置为1，以同时启动AD转换。

36.2.9.3 ADSTRn:AD转换软件启动寄存器n(n=0到8)

Base address: ADC_B = 0x4017_0000

Offset address: 0xC20 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADST	扫描组nAD转换开始 0：无效1：开始扫描组n的AD转换	W
31:1	—	写入值应为0。	W

ADSTRn寄存器控制扫描组n的AD转换的开始。该寄存器用于通过软件启动一个扫描组的AD转换。

如果要通过软件同时启动多个扫描组的AD转换，则应使用ADSYSTR寄存器。

ADST bit (Scan Group n A/D Conversion Start)

ADST bit controls the start of the A/D conversion of scan group n. When ADSYSTn bit is set to 1, the A/D conversion of the scan group n is started. Setting 0 to ADST bit has no effect on the operation.

36.2.9.4 ADSTOPR : A/D Conversion Stop Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC60

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ADSTOP1	—	—	—	—	—	—	—	ADSTOP0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADSTOP0	A/D Converter Unit 0 Force Stop bit 0: No effect 1: Force stop the operation of A/D converter unit 0	W
7:1	—	The write value should be 0.	W
8	ADSTOP1	A/D Converter Unit 1 Force Stop bit 0: No effect 1: Force stop the operation of A/D converter unit 1	W
31:9	—	The write value should be 0.	W

The ADSTOPR register forces each A/D converter to stop the operation. When the A/D converter is stopped with this register, the A/D conversion results with that A/D converter are not guaranteed.

ADSTOP0 bit (A/D Converter Unit 0 Force Stop bit)

ADSTOP0 bit forces the A/D converter unit 0 to stop the A/D conversion operation. Setting 0 to ADSTOP0 bit has no effect on the operation. When ADSTOP0 is set to 1, the A/D converter unit 0 is forced to stop the operation. If the A/D converter unit 0 is forced to stop, the A/D conversion results with the A/D converter unit 0 are not guaranteed.

ADSTOP1 bit (A/D Converter Unit 1 Force Stop bit)

ADSTOP1 bit forces the A/D converter unit 1 to stop the A/D conversion operation. Setting 0 to ADSTOP1 bit has no effect on the operation. When ADSTOP1 is set to 1, the A/D converter unit 1 is forced to stop the operation. If the A/D converter unit 1 is forced to stop, the A/D conversion results with the A/D converter unit 1 are not guaranteed.

36.2.10 Status Registers

ADST位（扫描组nAD转换开始）

ADST位控制扫描组n的AD转换的开始。当ADSYSTn位设置为1时，开始扫描组n的AD转换。将ADST位设置为0对操作没有影响。

36.2.9.4 ADSTOPR:AD转换停止寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xC60

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ADSTOP1	—	—	—	—	—	—	—	ADSTOP0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADSTOP0	AD转换器单元0强制停止位 0：无效1：强制停止AD转换单元的运行0	W
7:1	—	写入值应为0。	W
8	ADSTOP1	AD转换器单元1强制停止位 0：无效1：强制停止AD转换器单元1的运行	W
31:9	—	写入值应为0。	W

ADSTOPR寄存器强制每个AD转换器停止操作。当使用该寄存器停止AD转换器时，不能保证使用该AD转换器的AD转换结果。

ADSTOP0位（AD转换器单元0强制停止位）

ADSTOP0位强制AD转换器单元0停止AD转换操作。将ADSTOP0位设置为0对操作没有影响。当ADSTOP0设置为1时，AD转换器单元0被强制停止操作。如果强制停止AD转换器单元0，则无法保证AD转换器单元0的AD转换结果。

ADSTOP1位（AD转换器单元1强制停止位）

ADSTOP1位强制AD转换器单元1停止AD转换操作。将ADSTOP1位设置为0对操作没有影响。当ADSTOP1设置为1时，AD转换器单元1被强制停止操作。如果强制停止AD转换器单元1，则无法保证AD转换器单元1的AD转换结果。

36.2.10 状态寄存器

36.2.10.1 ADSR : A/D Conversion Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC80

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CALACT1	CALACT0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADACT1	ADACT0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADACT0	A/D Converter Unit 0 (ADC0) A/D Conversion Status 0: ADC0 is not in A/D conversion 1: ADC0 is in A/D conversion	R
1	ADACT1	A/D Converter Unit 1 (ADC1) A/D Conversion Status 0: ADC1 is not in A/D conversion 1: ADC1 is in A/D conversion	R
15:2	—	These bits are read as 0.	R
16	CALACT0	A/D Converter Unit 0 (ADC0) : Calibration Status 0: ADC0 is not in the calibration operation 1: ADC0 is in the calibration operation	R
17	CALACT1	A/D Converter Unit 1 (ADC1) : Calibration Status 0: ADC1 is not in the calibration operation 1: ADC1 is in the calibration operation	R
31:18	—	These bits are read as 0.	R

The ADSR register indicates the status for each A/D converter operation.

36.2.10.2 ADGRSR : Scan Group Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC84

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ACTGRn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	ACTGRn*1	Scan Group n Status 0: Scan group n is idle 1: Scan group n is in the scanning operation	R
31:9	—	These bits are read as 0.	R

Note: n = 0 to 8

Note 1. In the Group Priority Operation, if the scanning operation of a low priority group is interrupted, the ACTGRn bit of the corresponding scan group is set to 1.

The ADGRSR register indicates the operating status for each scan group.

36.2.10.1 ADSR:AD转换状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xC80

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CALACT1	CALACT0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADACT1	ADACT0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADACT0	AD转换器单元0(ADC0)AD转换状态 0：ADC0未进行AD转换1：ADC0正在进行AD转换	R
1	ADACT1	AD转换器单元1(ADC1)AD转换状态 0：ADC1未进行AD转换1：ADC1正在进行AD转换	R
15:2	—	这些位读为0。	R
16	CALACT0	AD转换器单元0(ADC0)：校准状态 0：ADC0未进行校准操作1：ADC0正在进行校准操作	R
17	CALACT1	AD转换器单元1(ADC1)：校准状态 0：ADC1不在校准操作中1：ADC1在校准操作中	R
31:18	—	这些位读为0。	R

ADSR寄存器指示每个AD转换器操作的状态。

36.2.10.2 ADGRSR:扫描组状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xC84

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ACTGRn								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	ACTGRn*1	扫描组n状态 0：扫描组n空闲1：扫描组n正在扫描操作中	R
31:9	—	这些位读为0。	R

Note: n = 0 to 8

注1.在组优先级操作中，如果低优先级组的扫描操作被中断，则相应扫描组的ACTGRn位设置为1。

ADGRSR寄存器指示每个扫描组的操作状态。

36.2.10.3 ADSCANENDSR : Scan End Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SCENDFn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SCENDFn*1	Scan Group n Scan End Flag 0: Scan group n has not been scanned 1: End of scan for scan group n is detected	R
31:9	—	These bits are read as 0.	R

Note: n = 0 to 8

Note 1. If the A/D conversion operation is stopped with the ADSTOPR register, the SCANENDFn bit of the scan group in which the scan operation was stopped is not changed. (It is not set to 1)

The ADSCANENDSR register indicates whether the scanning operation for each scan group has been done. Each flag can be cleared in ADSCANENDSCR register.

36.2.10.4 ADSCANENDSCR : Scan End Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD54

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SCENDCn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SCENDCn	Scan Group n Scan End Flag Clear 0: No effect 1: ADSCANENDSR.SCENDFn is cleared	W
31:9	—	The write value should be 0.	W

Note: n = 0 to 8

The ADSCANENDSCR register clears the scan end flag for the scan group n.

36.2.10.3 ADSCANENDSR:扫描结束状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xD50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SCENDFn								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SCENDFn*1	扫描组n扫描结束标志 0：未扫描扫描组n1：检测到扫描组n扫描结束	R
31:9	—	这些位读为0。	R

Note: n = 0 to 8

注1.如果通过ADSTOPR寄存器停止AD转换操作，则停止扫描操作的扫描组的SCANENDFn位不会改变。（未设置为1）

ADSCANENDSR寄存器指示每个扫描组的扫描操作是否已完成。每个标志都可以在ADSCANENDSCR寄存器中清除。

36.2.10.4 ADSCANENDSCR:扫描结束状态清除寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xD54

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SCENDCn								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SCENDCn	扫描组n扫描结束标志清除 0：无效1：ADSCANENDSR.SCENDFn清零	W
31:9	—	写入值应为0。	W

Note: n = 0 to 8

ADSCANENDSCR寄存器清除扫描组n的扫描结束标志。

36.2.10.5 ADERSR : A/D Conversion Error Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC88

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADERF1	ADERF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADERF0	A/D Converter Unit 0 (ADC0) Error Flag 0: Error is not detected 1: Error is detected	R
1	ADERF1	A/D Converter Unit 1 (ADC1) Error Flag 0: Error is not detected 1: Error is detected	R
31:2	—	These bits are read as 0.	R

The ADERSR register indicates whether the operating error has occurred in each A/D converter. Each flag can be cleared in ADERSCR register.

The A/D conversion data is not guaranteed in the A/D converter operation with an error detected.

36.2.10.6 ADERSCR : A/D Conversion Error Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC8C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADERCLR1	ADERCLR0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADERCLR0	A/D Converter Unit 0 Error Flag Clear 0: No effect 1: ADERSR.ADERF0 is cleared	W
1	ADERCLR1	A/D Converter Unit 1 Error Flag Clear 0: No effect 1: ADERSR.ADERF1 is cleared	W
31:2	—	The write value should be 0.	W

The ADERSCR register clears the error flag for A/D converter unit 0 or unit 1.

36.2.10.5 ADERSR:AD转换错误状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xC88

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADERF1	ADERF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADERF0	AD转换器单元0(ADC0)错误标志 0：未检测到错误1：检测到错误	R
1	ADERF1	AD转换器单元1(ADC1)错误标志 0：未检测到错误1：检测到错误	R
31:2	—	这些位读为0。	R

ADERSR寄存器指示每个AD转换器是否发生操作错误。每个标志都可以在ADERSCR register.

在检测到错误的AD转换器操作中不能保证AD转换数据。

36.2.10.6 ADERSCR:AD转换错误状态清除寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xC8C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADERCLR1	ADERCLR0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADERCLR0	AD转换器单元0错误标志清除 0：无效1：ADERSR.ADERF0清零	W
1	ADERCLR1	AD转换器单元1错误标志清除 0：无效1：ADERSR.ADERF1清零	W
31:2	—	写入值应为0。	W

ADERSCR寄存器清除AD转换器单元0或单元1的错误标志。

36.2.10.7 ADCALENDSR : A/D Converter Calibration End Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC98

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CALENDF1	CALENDF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CALENDF0	A/D Converter Unit 0 Calibration End flag 0: End of the calibration is not detected 1: End of the calibration is detected	R
1	CALENDF1	A/D Converter Unit 1 Calibration End flag 0: End of the calibration is not detected 1: End of the calibration is detected	R
31:2	—	These bits are read as 0.	R

The ADCALENDSR register indicates the end of the calibration operation for the A/D converter unit 0 or unit 1. Each flag can be cleared in ADCALENDSCR register.

36.2.10.8 ADCALENDSCR : A/D Converter Calibration End Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC9C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CALENDC1	CALENDC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CALENDC0	A/D Converter Unit 0 Calibration End Flag Clear 0: No effect 1: ADCALENDSR.CALENDF0 is cleared	W
1	CALENDC1	A/D Converter Unit 1 Calibration End Flag Clear 0: No effect 1: ADCALENDSR.CALENDF1 is cleared	W
31:2	—	The write value should be 0.	W

The ADCALENDSCR register clears the Calibration End flag for the A/D converter unit 0 or unit 1.

36.2.10.7 ADCALENDSR:AD转换器校准结束状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xC98

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CALENDF1	CALENDF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CALENDF0	AD转换器单元0校准结束标志 0：未检测到校准结束1：检测到校准结束	R
1	CALENDF1	AD转换器单元1校准结束标志 0：未检测到校准结束1：检测到校准结束	R
31:2	—	这些位读为0。	R

ADCALENDSR寄存器指示AD转换器单元0或单元1校准操作的结束。每个标志都可以在ADCALENDSCR寄存器中清除。

36.2.10.8 ADCALENDSCR:AD转换器校准结束状态清除寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xC9C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CALENDC1	CALENDC0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CALENDC0	AD转换器单元0校准结束标志清除 0：无效1：ADCALENDSR.CALENDF0清零	W
1	CALENDC1	AD转换器单元1校准结束标志清除 0：无效1：ADCALENDSR.CALENDF1清零	W
31:2	—	写入值应为0。	W

ADCALENDSCR寄存器清除AD转换器单元0或单元1的校准结束标志。

36.2.10.9 ADOVFERSR : A/D Conversion Overflow Error Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xCA0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADOVFEF1	ADOVFEF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADOVFEF0	A/D Converter Unit 0 (ADC0) Overflow Error Flag 0: ADC0 overflow error is not detected 1: ADC0 overflow error is detected	R
1	ADOVFEF1	A/D Converter Unit 1 (ADC1) Overflow Error Flag 0: ADC1 overflow error is not detected 1: ADC1 overflow error is detected	R
31:2	—	These bits are read as 0.	R

The ADOVFERSR register indicates whether the overflow error has occurred in an A/D conversion using A/D converter unit 0 or unit 1. Each flag can be cleared in ADOVFERSCR register.

36.2.10.10 ADOVFCHSR0 : A/D Conversion Overflow Channel Status Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xCA4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	OFVCHFn																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	OFVCHFn	Analog Channel No. n : Overflow Flag 0: Overflow is not detected 1: Overflow is detected	R
31:29	—	These bits are read as 0.	R

Note: n = 0 to 28

The ADOVFCHSR0 register indicates whether the overflow has occurred in the A/D conversion of the analog channel n. Each flag can be cleared in ADOVFCHSCR0 register.

36.2.10.9 ADOVFERSR:AD转换溢出错误状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xCA0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADOVFEF1	ADOVFEF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADOVFEF0	AD转换器单元0(ADC0)溢出错误标志 0：未检测到ADC0溢出错误1：检测到ADC0溢出错误	R
1	ADOVFEF1	AD转换器单元1(ADC1)溢出错误标志 0：未检测到ADC1溢出错误1：检测到ADC1溢出错误	R
31:2	—	这些位读为0。	R

ADOVFERSR寄存器指示在使用AD转换器单元0或单元1的AD转换中是否发生溢出错误。可以在ADOVFERSCR寄存器中清除每个标志。

36.2.10.10 ADOVFCHSR0:AD转换溢出通道状态寄存器0

Base address: ADC_B = 0x4017_0000

Offset address: 0xCA4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	OFVCHFn																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	OFVCHFn	模拟通道编号n：溢出标志 0：未检测到溢出1：检测到溢出	R
31:29	—	这些位读为0。	R

Note: n = 0 to 28

ADOVFCHSR0寄存器指示模拟通道n的AD转换是否发生溢出。
每个标志都可以在ADOVFCHSCR0寄存器中清除。

36.2.10.11 ADOVFEXSR : Extended Analog A/D Conversion Overflow Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xCB0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OVFEXF8	OVFEXF7	OVFEXF6	OVFEXF5	—	—	OVFEXF2	OVFEXF1	OVFEXF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OVFEXF0	Self-Diagnosis Channel : Overflow Flag bit 0: Overflow is not detected 1: Overflow is detected	R
1	OVFEXF1	Temperature Sensor Channel : Overflow Flag bit 0: Overflow is not detected 1: Overflow is detected	R
2	OVFEXF2	Internal Reference Voltage Channel : Overflow Flag bit 0: Overflow is not detected 1: Overflow is detected	R
4:3	—	These bits are read as 0.	R
5	OVFEXF5	D/A Converter 0 Channel : Overflow Flag bit 0: Overflow is not detected 1: Overflow is detected	R
6	OVFEXF6	D/A Converter 1 Channel : Overflow Flag bit 0: Overflow is not detected 1: Overflow is detected	R
7	OVFEXF7	D/A Converter 2 Channel : Overflow Flag bit 0: Overflow is not detected 1: Overflow is detected	R
8	OVFEXF8	D/A Converter 3 Channel : Overflow Flag bit 0: Overflow is not detected 1: Overflow is detected	R
31:9	—	These bits are read as 0.	R

The ADOVFEXSR register indicates whether the overflow occurred when the A/D conversion for the extended analog function is performed. Each flag can be cleared in ADOVFEXSCR.

36.2.10.12 ADOVFERSCR : A/D Conversion Overflow Error Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xCB4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADOVFEC1	ADOVFEC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

36.2.10.11 ADOVFEXSR:扩展模拟AD转换溢出状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xCB0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OVFEXF8	OVFEXF7	OVFEXF6	OVFEXF5	—	—	OVFEXF2	OVFEXF1	OVFEXF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OVFEXF0	自诊断通道：溢出标志位 0：未检测到溢出1：检测到溢出	R
1	OVFEXF1	温度传感器通道：溢出标志位 0：未检测到溢出1：检测到溢出	R
2	OVFEXF2	内部参考电压通道：溢出标志位 0：未检测到溢出1：检测到溢出	R
4:3	—	这些位读为0。	R
5	OVFEXF5	DA转换器0通道：溢出标志位 0：未检测到溢出1：检测到溢出	R
6	OVFEXF6	DA转换器1通道：溢出标志位 0：未检测到溢出1：检测到溢出	R
7	OVFEXF7	DA转换器2通道：溢出标志位 0：未检测到溢出1：检测到溢出	R
8	OVFEXF8	DA转换器3通道：溢出标志位 0：未检测到溢出1：检测到溢出	R
31:9	—	这些位读为0。	R

ADOVFEXSR寄存器指示执行扩展模拟功能的AD转换时是否发生溢出。每个标志都可以在ADOVFEXSCR中清除。

36.2.10.12 ADOVFERSCR:AD转换溢出错误状态清除寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xCB4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADOVFEC1	ADOVFEC0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADOVFEC0	A/D Converter Unit 0 (ADC0) Overflow Error Flag Clear 0: No effect 1: ADOVFERSR.ADOVFEF0 is cleared	W
1	ADOVFEC1	A/D Converter Unit 1 (ADC1) Overflow Error Flag Clear 0: No effect 1: ADOVFERSR.ADOVFEF1 is cleared	W
31:2	—	The write value should be 0.	W

The ADOVFERSCR register clears the Overflow Error flag for the A/D converter unit 0 or unit 1.

36.2.10.13 ADOVFCHSCR0 : A/D Conversion Overflow Channel Status Clear Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xCB8

Bit position:	31			28																										0
Bit field:	—	—	—	OVFCHCn																										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	OVFCHCn	Analog Channel No. n : Overflow Flag Clear 0: No effect 1: ADOVFCHSR0.OVFCHFn is cleared	W
31:29	—	The write value should be 0.	W

Note: n = 0 to 28

The ADOVFCHSCR0 register clears the Overflow flag for the analog channel n.

36.2.10.14 ADOVFEXSCR : Extended Analog A/D Conversion Overflow Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xCC4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OVFEXC8	OVFEXC7	OVFEXC6	OVFEXC5	—	—	OVFEXC2	OVFEXC1	OVFEXC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OVFEXC0	Self-Diagnosis Channel : Overflow Flag Clear 0: No effect 1: ADOVFEXSR.OVFEXF0 is cleared	W
1	OVFEXC1	Temperature Sensor Channel : Overflow Flag Clear 0: No effect 1: ADOVFEXSR.OVFEXF1 is cleared	W

Bit	Symbol	Function	R/W
0	ADOVFEC0	AD转换器单元0(ADC0)溢出错误标志清除 0：无效1：ADOVFERSR.ADOVFEF0清零	W
1	ADOVFEC1	AD转换器单元1(ADC1)溢出错误标志清除 0：无效1：ADOVFERSR.ADOVFEF1清零	W
31:2	—	写入值应为0。	W

ADOVFERSCR寄存器清除AD转换器单元0或单元1的溢出错误标志。

36.2.10.13 ADOVFCHSCR0:AD转换溢出通道状态清除寄存器0

Base address: ADC_B = 0x4017_0000

Offset address: 0xCB8

Bit position:	31			28																										0
Bit field:	—	—	—	OVFCHCn																										
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	OVFCHCn	模拟通道编号n：溢出标志清除 0：无效1：ADOVFCHSR0.OVFCHFn清零	W
31:29	—	写入值应为0。	W

Note: n = 0 to 28

ADOVFCHSCR0寄存器清除模拟通道n的溢出标志。

36.2.10.14 ADOVFEXSCR:扩展模拟AD转换溢出状态清除 Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xCC4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OVFEXC8	OVFEXC7	OVFEXC6	OVFEXC5	—	—	OVFEXC2	OVFEXC1	OVFEXC0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OVFEXC0	自诊断通道：溢出标志清除 0：无效1：ADOVFEXSR.OVFEXF0清零	W
1	OVFEXC1	温度传感器通道：溢出标志清除 0：无效1：ADOVFEXSR.OVFEXF1清零	W

Bit	Symbol	Function	R/W
2	OVFEXC2	Internal Reference Voltage Channel : Overflow Flag Clear 0: No effect 1: ADOVFEXSR.OVFEXF2 is cleared	W
4:3	—	The write value should be 0.	W
5	OVFEXC5	D/A Converter 0 Channel : Overflow Flag Clear 0: No effect 1: ADOVFEXSR.OVFEXF5 is cleared	W
6	OVFEXC6	D/A Converter 1 Channel : Overflow Flag Clear 0: No effect 1: ADOVFEXSR.OVFEXF6 is cleared	W
7	OVFEXC7	D/A Converter 2 Channel : Overflow Flag Clear 0: No effect 1: ADOVFEXSR.OVFEXF7 is cleared	W
8	OVFEXC8	D/A Converter 3 Channel : Overflow Flag Clear 0: No effect 1: ADOVFEXSR.OVFEXF8 is cleared	W
31:9	—	The write value should be 0.	W

The ADOVFEXSCR register clears the overflow flag for the extended analog function channels.

36.2.11 FIFO

36.2.11.1 ADFIFOCR : FIFO Control Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x4C0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FIFOENn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOENn	Scan Group n FIFO Enable 0: Disable scan group n FIFO function 1: Enable scan group n FIFO function	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 8

The ADFIFOCR register enables/disables the FIFO function of scan group n.

FIFOENn bit (Scan Group n FIFO Enable)

FIFOENn bit enables or disables the FIFO function of scan group n. When the FIFOENn is set to 1, the FIFO function of scan group n is enabled, and the result of A/D conversion is stored to the FIFO. When the FIFOENn is set to 0, the FIFO function of scan group n is disabled.

The A/D conversion result can also be read from the A/D data or extended data registers.

Bit	Symbol	Function	R/W
2	OVFEXC2	内部参考电压通道：溢出标志清除 0：无效1：ADOVFEXSR.OVFEXF2清零	W
4:3	—	写入值应为0。	W
5	OVFEXC5	DA转换器0通道：溢出标志清除 0：无效1：ADOVFEXSR.OVFEXF5清零	W
6	OVFEXC6	DA转换器1通道：溢出标志清除 0：无效1：ADOVFEXSR.OVFEXF6清零	W
7	OVFEXC7	DA转换器2通道：溢出标志清除 0：无效1：ADOVFEXSR.OVFEXF7清零	W
8	OVFEXC8	DA转换器3通道：溢出标志清除 0：无效1：ADOVFEXSR.OVFEXF8清零	W
31:9	—	写入值应为0。	W

ADOVFEXSCR寄存器清除扩展模拟功能通道的溢出标志。

36.2.11 FIFO

36.2.11.1 ADFIFOCR：先进先出控制寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x4C0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FIFOENn								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOENn	扫描组nFIFO启用 0：禁用扫描组nFIFO功能1：启用扫描组nFIFO功能	R/W
31:9	—	这些位被读取为0。写入值应为0。	R/W

Note: n = 0 to 8

ADFIFOCR寄存器使能禁用扫描组n的FIFO功能。

FIFOENn位（扫描组nFIFO启用）

FIFOENn位启用或禁用扫描组n的FIFO功能。当FIFOENn置1时，使能扫描组n的FIFO功能，并将AD转换的结果存入FIFO。当FIFOENn设置为0时，扫描组n的FIFO功能被禁用。

AD转换结果也可以从AD数据或扩展数据寄存器中读取。

36.2.11.2 ADFIFOINTCR : FIFO Interrupt Control Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x4C4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FIFOIEn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOIEn	Scan Group n FIFO Interrupt Enable 0: Disable scan group n FIFO interrupt 1: Enable scan group n FIFO interrupt	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 8

The ADFIFOINTCR register enables/disables the FIFO data read request interrupt and FIFO overflow interrupt for scan group n.

36.2.11.3 ADFIFOINTLR0 : FIFO Interrupt Generation Level Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0x4C8

Bit position:	31											19				16											3			0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	FIFOILV1[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOILV0[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOILV0[3:0]	Scan Group 0 FIFO Interrupt Output Timing Setting These bits set the generation timing of FIFO interrupt. The FIFO data read request interrupt is generated when the number of available FIFO stages falls below the value set by these bits. Set a value in the range from 0 to 7. Setting a value in the range from 8 to 15 is prohibited.	R/W
15:4	—	These bits are read as 0. The write value should be 0.	R/W
19:16	FIFOILV1[3:0]	Scan Group 1 FIFO Interrupt Output Timing Setting These bits set the generation timing of FIFO interrupt. The FIFO data read request interrupt is generated when the number of available FIFO stages falls below the value set by these bits. Set a value in the range from 0 to 7. Setting a value in the range from 8 to 15 is prohibited.	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The ADFIFOINTLR0 register specifies the generation timing of the FIFO data read request interrupt for the scan group 0 and 1.

36.2.11.2 ADFIFOINTCR:FIFO中断控制寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0x4C4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FIFOIEn								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOIEn	扫描组nFIFO中断使能 0：禁用扫描组nFIFO中断1：启用扫描组nFIFO中断	R/W
31:9	—	这些位被读取为0。写入值应为0。	R/W

Note: n = 0 to 8

ADFIFOINTCR寄存器使能禁用扫描组n的FIFO数据读取请求中断和FIFO溢出中断。

36.2.11.3 ADFIFOINTLR0：FIFO中断生成级别寄存器0

Base address: ADC_B = 0x4017_0000

Offset address: 0x4C8

Bit position:	31											19				16											3			0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	FIFOILV1[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOILV0[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOILV0[3:0]	扫描组0FIFO中断输出时序设置 这些位设置FIFO中断的产生时序。 当可用FIFO级数低于这些位设置的值时，将产生FIFO数据读取请求中断。请在0到7的范围内设置值。禁止在8到15的范围内设置值。	R/W
15:4	—	这些位被读取为0。写入值应为0。	R/W
19:16	FIFOILV1[3:0]	扫描组1FIFO中断输出时序设置 这些位设置FIFO中断的产生时序。 当可用FIFO级数低于这些位设置的值时，将产生FIFO数据读取请求中断。请在0到7的范围内设置值。禁止在8到15的范围内设置值。	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

ADFIFOINTLR0寄存器指定扫描组0和1的FIFO数据读取请求中断的产生时序。

36.2.11.4 ADFIFOINTLR1 : FIFO Interrupt Generation Level Register 1

Base address: ADC_B = 0x4017_0000

Offset address: 0x4CC

Bit position:	31												19		16										3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	FIFOILV3[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOILV2[3:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOILV2[3:0]	Scan Group 2 FIFO Interrupt Output Timing Setting These bits set the generation timing of FIFO interrupt. The FIFO data read request interrupt is generated when the number of available FIFO stages falls below the value set by these bits. Set a value in the range from 0 to 7. Setting a value in the range from 8 to 15 is prohibited.	R/W
15:4	—	These bits are read as 0. The write value should be 0.	R/W
19:16	FIFOILV3[3:0]	Scan Group 3 FIFO Interrupt Output Timing Setting These bits set the output timing of scan group 3 FIFO interrupt. The FIFO data read request interrupt is generated when the number of available FIFO stages falls below the value set by these bits. Set a value in the range from 0 to 7. Setting a value in the range from 8 to 15 is prohibited.	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The ADFIFOINTLR1 register specifies the generation timing of the FIFO data read request interrupt for the scan group 2 and 3.

36.2.11.5 ADFIFOINTLR2 : FIFO Interrupt Generation Level Register 2

Base address: ADC_B = 0x4017_0000

Offset address: 0x4D0

Bit position:	31												19		16										3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	FIFOILV5[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOILV4[3:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOILV4[3:0]	Scan Group 4 FIFO Interrupt Output Timing Setting These bits set the generation timing of FIFO interrupt. The FIFO data read request interrupt is generated when the number of available FIFO stages falls below the value set by these bits. Set a value in the range from 0 to 7. Setting a value in the range from 8 to 15 is prohibited.	R/W
15:4	—	These bits are read as 0. The write value should be 0.	R/W
19:16	FIFOILV5[3:0]	Scan Group 5 FIFO Interrupt Output Timing Setting These bits set the generation timing of FIFO interrupt. The FIFO data read request interrupt is generated when the number of available FIFO stages falls below the value set by these bits. Set a value in the range from 0 to 7. Setting a value in the range from 8 to 15 is prohibited.	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The ADFIFOINTLR2 register specifies the generation timing of the FIFO data read request interrupt for the scan group 4 and 5.

36.2.11.4 ADFIFOINTLR1：FIFO中断生成级别寄存器1

Base address: ADC_B = 0x4017_0000

Offset address: 0x4CC

Bit position:	31												19		16										3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	FIFOILV3[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOILV2[3:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOILV2[3:0]	扫描组2FIFO中断输出时序设置 这些位设置FIFO中断的产生时序。 当可用FIFO级数低于这些位设置的值时，将产生FIFO数据读取请求中断。请在0到7的范围内设置值。禁止在8到15的范围内设置值。	R/W
15:4	—	这些位被读取为0。写入值应为0。	R/W
19:16	FIFOILV3[3:0]	扫描组3FIFO中断输出时序设置 这些位设置扫描组3FIFO中断的输出时序。 当可用FIFO级数低于这些位设置的值时，将产生FIFO数据读取请求中断。请在0到7的范围内设置值。禁止在8到15的范围内设置值。	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

ADFIFOINTLR1寄存器指定扫描组2和3的FIFO数据读取请求中断的产生时序。

36.2.11.5 ADFIFOINTLR2：FIFO中断生成级别寄存器2

Base address: ADC_B = 0x4017_0000

Offset address: 0x4D0

Bit position:	31												19		16										3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	FIFOILV5[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOILV4[3:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOILV4[3:0]	扫描组4FIFO中断输出时序设置 这些位设置FIFO中断的产生时序。 当可用FIFO级数低于这些位设置的值时，将产生FIFO数据读取请求中断。请在0到7的范围内设置值。禁止在8到15的范围内设置值。	R/W
15:4	—	这些位被读取为0。写入值应为0。	R/W
19:16	FIFOILV5[3:0]	扫描组5FIFO中断输出时序设置 这些位设置FIFO中断的产生时序。 当可用FIFO级数低于这些位设置的值时，将产生FIFO数据读取请求中断。请在0到7的范围内设置值。禁止在8到15的范围内设置值。	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

ADFIFOINTLR2寄存器指定扫描组4和5的FIFO数据读取请求中断的产生时序。

36.2.11.6 ADFIFOINTLR3 : FIFO Interrupt Generation Level Register 3

Base address: ADC_B = 0x4017_0000

Offset address: 0x4D4

Bit position:	31												19			16											3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	FIFOILV7[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOILV6[3:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOILV6[3:0]	Scan Group 6 FIFO Interrupt Output Timing Setting These bits set the generation timing of FIFO interrupt. The FIFO data read request interrupt is generated when the number of available FIFO stages falls below the value set by these bits. Set a value in the range from 0 to 7. Setting a value in the range from 8 to 15 is prohibited.	R/W
15:4	—	These bits are read as 0. The write value should be 0.	R/W
19:16	FIFOILV7[3:0]	Scan Group 7 FIFO Interrupt Output Timing Setting These bits set the generation timing of FIFO interrupt. The FIFO data read request interrupt is generated when the number of available FIFO stages falls below the value set by these bits. Set a value in the range from 0 to 7. Setting a value in the range from 8 to 15 is prohibited.	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The ADFIFOINTLR3 register specifies the generation timing of the FIFO data read request interrupt for the scan group 6 and 7.

36.2.11.7 ADFIFOINTLR4 : FIFO Interrupt Generation Level Register 4

Base address: ADC_B = 0x4017_0000

Offset address: 0x4D8

Bit position:	31																										3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FIFOILV8[3:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOILV8[3:0]	Scan Group 8 FIFO Interrupt Output Timing Setting These bits set the generation timing of FIFO interrupt. The FIFO data read request interrupt is generated when the number of available FIFO stages falls below the value set by these bits. Set a value in the range from 0 to 7. Setting a value in the range from 8 to 15 is prohibited.	R/W
31:4	—	These bits are read as 0. The write value should be 0.	R/W

The ADFIFOINTLR4 register specifies the generation timing of the FIFO data read request interrupt for the scan group 8.

36.2.11.8 ADFIFOSR0 : FIFO Status Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xCD0

Bit position:	31												19			16											3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	FIFOST1[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOST0[3:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

36.2.11.6 ADFIFOINTLR3：FIFO中断生成级别寄存器3

Base address: ADC_B = 0x4017_0000

Offset address: 0x4D4

Bit position:	31												19			16											3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	FIFOILV7[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOILV6[3:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOILV6[3:0]	扫描组6FIFO中断输出时序设置 这些位设置FIFO中断的产生时序。 当可用FIFO级数低于这些位设置的值时，将产生FIFO数据读取请求中断。请在0到7的范围内设置值。禁止在8到15的范围内设置值。	R/W
15:4	—	这些位被读取为0。写入值应为0。	R/W
19:16	FIFOILV7[3:0]	扫描组7FIFO中断输出时序设置 这些位设置FIFO中断的产生时序。 当可用FIFO级数低于这些位设置的值时，将产生FIFO数据读取请求中断。请在0到7的范围内设置值。禁止在8到15的范围内设置值。	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

ADFIFOINTLR3寄存器指定扫描组6和7的FIFO数据读取请求中断的产生时序。

36.2.11.7 ADFIFOINTLR4：FIFO中断生成级别寄存器4

Base address: ADC_B = 0x4017_0000

Offset address: 0x4D8

Bit position:	31																										3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FIFOILV8[3:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOILV8[3:0]	扫描组8FIFO中断输出时序设置 这些位设置FIFO中断的产生时序。 当可用FIFO级数低于这些位设置的值时，将产生FIFO数据读取请求中断。请在0到7的范围内设置值。禁止在8到15的范围内设置值。	R/W
31:4	—	这些位被读取为0。写入值应为0。	R/W

ADFIFOINTLR4寄存器指定扫描组8的FIFO数据读取请求中断的产生时序。

36.2.11.8 ADFIFOSR0：FIFO状态寄存器0

Base address: ADC_B = 0x4017_0000

Offset address: 0xCD0

Bit position:	31												19			16											3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	FIFOST1[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOST0[3:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOST0[3:0]	Number of Available Stages in FIFO for Scan Group 0	R
15:4	—	These bits are read as 0.	R
19:16	FIFOST1[3:0]	Number of Available Stages in FIFO for Scan Group 1	R
31:20	—	These bits are read as 0.	R

The ADFIFOSR0 register indicates the number of available stages in FIFO for scan group 0 and 1.

36.2.11.9 ADFIFOSR1 : FIFO Status Register 1

Base address: ADC_B = 0x4017_0000

Offset address: 0xCD4

Bit position:	31												19		16												3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	FIFOST3[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOST2[3:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOST2[3:0]	Number of Available Stages in FIFO for Scan Group 2	R
15:4	—	These bits are read as 0.	R
19:16	FIFOST3[3:0]	Number of Available Stages in FIFO for Scan Group 3	R
31:20	—	These bits are read as 0.	R

The ADFIFOSR1 register indicates the number of available stages in FIFO for scan group 2 and 3.

36.2.11.10 ADFIFOSR2 : FIFO Status Register 2

Base address: ADC_B = 0x4017_0000

Offset address: 0xCD8

Bit position:	31												19		16												3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	FIFOST5[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOST4[3:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOST4[3:0]	Number of Available Stages in FIFO for Scan Group 4	R
15:4	—	These bits are read as 0.	R
19:16	FIFOST5[3:0]	Number of Available Stages in FIFO for Scan Group 5	R
31:20	—	These bits are read as 0.	R

The ADFIFOSR2 register indicates the number of available stages in FIFO for scan group 4 and 5.

36.2.11.11 ADFIFOSR3 : FIFO Status Register 3

Base address: ADC_B = 0x4017_0000

Offset address: 0xCDC

Bit position:	31												19		16												3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	FIFOST7[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOST6[3:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOST0[3:0]	扫描组0的FIFO中可用阶段数	R
15:4	—	这些位读为0。	R
19:16	FIFOST1[3:0]	扫描组1的FIFO中可用阶段数	R
31:20	—	这些位读为0。	R

ADFIFOSR0寄存器指示FIFO中用于扫描组0和1的可用级数。

36.2.11.9 ADFIFOSR1：FIFO状态寄存器1

Base address: ADC_B = 0x4017_0000

Offset address: 0xCD4

Bit position:	31												19		16												3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	FIFOST3[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOST2[3:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOST2[3:0]	扫描组2的FIFO中可用阶段数	R
15:4	—	这些位读为0。	R
19:16	FIFOST3[3:0]	扫描组3的FIFO中可用阶段数	R
31:20	—	这些位读为0。	R

ADFIFOSR1寄存器指示FIFO中用于扫描组2和3的可用级数。

36.2.11.10 ADFIFOSR2：FIFO状态寄存器2

Base address: ADC_B = 0x4017_0000

Offset address: 0xCD8

Bit position:	31												19		16												3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	FIFOST5[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOST4[3:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOST4[3:0]	扫描组4的FIFO中可用阶段数	R
15:4	—	这些位读为0。	R
19:16	FIFOST5[3:0]	扫描组5的FIFO中可用阶段数	R
31:20	—	这些位读为0。	R

ADFIFOSR2寄存器指示FIFO中用于扫描组4和5的可用级数。

36.2.11.11 ADFIFOSR3：FIFO状态寄存器3

Base address: ADC_B = 0x4017_0000

Offset address: 0xCDC

Bit position:	31												19		16												3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	FIFOST7[3:0]				—	—	—	—	—	—	—	—	—	—	—	FIFOST6[3:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOST6[3:0]	Number of Available Stages in FIFO for Scan Group 6	R
15:4	—	These bits are read as 0.	R
19:16	FIFOST7[3:0]	Number of Available Stages in FIFO for Scan Group 7	R
31:20	—	These bits are read as 0.	R

The ADFIFOSR3 register indicates the number of available stages in FIFO for scan group 6 and 7.

36.2.11.12 ADFIFOSR4 : FIFO Status Register 4

Base address: ADC_B = 0x4017_0000

Offset address: 0xCE0

Bit position:	31																										3	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FIFOST8[3:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOST8[3:0]	Number of Available Stages in FIFO for Scan Group 8	R
31:4	—	These bits are read as 0.	R

The ADFIFOSR4 register indicates the number of available stages in FIFO for scan group 8.

36.2.11.13 ADFIFODCR : FIFO Data Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xCF0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FIFODCn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFODCn	Scan Group n FIFO Data Clear 0: No effect 1: Clear the data of scan group n FIFO	W
31:9	—	The write value should be 0.	W

Note: n = 0 to 8

The ADFIFODCR register clears the data in FIFO for each scan group.

FIFODCn bit (Scan Group n FIFO Data Clear)

FIFODCn bit clears the data in FIFO for scan group n. Writing 1 to the FIFODCn clears the data in the FIFO of scan group n. Writing 0 has no effect on the operation, and the data in FIFO is not cleared.

Bit	Symbol	Function	R/W
3:0	FIFOST6[3:0]	扫描组6的FIFO中可用阶段数	R
15:4	—	这些位读为0。	R
19:16	FIFOST7[3:0]	扫描组7的FIFO中可用阶段数	R
31:20	—	这些位读为0。	R

ADFIFOSR3寄存器指示FIFO中用于扫描组6和7的可用级数。

36.2.11.12 ADFIFOSR4：FIFO状态寄存器4

Base address: ADC_B = 0x4017_0000

Offset address: 0xCE0

Bit position:	31																										3	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FIFOST8[3:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
3:0	FIFOST8[3:0]	扫描组8的FIFO中可用阶段数	R
31:4	—	这些位读为0。	R

ADFIFOSR4寄存器指示扫描组8的FIFO中可用级数。

36.2.11.13 ADFIFODCR:FIFO数据清除寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xCF0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FIFODCn								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFODCn	扫描组nFIFO数据清除 0：无效1：清除扫描组nFIFO的数据	W
31:9	—	写入值应为0。	W

Note: n = 0 to 8

ADFIFODCR寄存器为每个扫描组清除FIFO中的数据。

FIFODCn位（扫描组nFIFO数据清除）

FIFODCn位清除扫描组n的FIFO中的数据。将1写入FIFODCn将清除扫描组n的FIFO中的数据。写0对操作没有影响，FIFO中的数据不会被清除。

36.2.11.14 ADFIFOERSR : FIFO Error Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xCF4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	FIFOFLFn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FIFOOVFn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOOVFn	Scan Group n FIFO Overflow Flag 0: No overflow 1: FIFO overflow is detected	R
15:9	—	These bits are read as 0.	R
24:16	FIFOFLFn	Scan Group n FIFO Data Read Request Flag 0: FIFO Data Read Request is not detected. 1: FIFO Data Read Request is detected.	R
31:25	—	These bits are read as 0.	R

Note: n = 0 to 8

The ADFIFOERSR register indicates the status of the FIFO. Each flag can be cleared in ADFIFOERSCR.

FIFOOVFn bit (Scan Group n FIFO Overflow Flag)

FIFOOVFn bit indicates whether the overflow occurred in the FIFO of the scan group n.

When FIFOOVFn bit is 0, an overflow is not detected in the FIFO. When FIFOOVFn is 1, an overflow occurred in the FIFO and the A/D conversion result cannot be stored to the FIFO. FIFOOVFn can be cleared in ADFIFOERSCR.

FIFOFLFn bit (Scan Group n FIFO Data Read Request Flag)

FIFOFLFn indicates whether a FIFO data read request in scan group n has been detected. The setting and clearing conditions of FIFOFLFn are shown as follows:

[Setting condition]

When the condition of ADFIFOSRm.FIFOSTn[3:0] ≤ ADFIFOINTLRm.FIFOILVn[3:0] is detected.

[Clearing condition]

When ADFIFOERSCR.FIFOFLCn is written to 1 under the condition of ADFIFOSRm.FIFOSTn[3:0] > ADFIFOINTLRm.FIFOILVn[3:0].

When the condition of ADFIFOSRm.FIFOSTn[3:0] > ADFIFOINTLRm.FIFOILVn[3:0] is occurred by the read access to ADFIFODRn register with DMAC or DTC.

Note: m = 0 to 4, n = 0 to 8

36.2.11.14 ADFIFOERSR:FIFO错误状态寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xCF4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	FIFOFLFn								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FIFOOVFn								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOOVFn	扫描组nFIFO溢出标志 0：无溢出1：检测到FIFO溢出	R
15:9	—	这些位读为0。	R
24:16	FIFOFLFn	扫描组nFIFO数据读取请求标志 0：未检测到FIFO数据读取请求。1：检测到FIFO数据读取请求。	R
31:25	—	这些位读为0。	R

Note: n = 0 to 8

ADFIFOERSR寄存器指示FIFO的状态。每个标志都可以在ADFIFOERSCR中清除。

FIFOOVFn位（扫描组nFIFO溢出标志）

FIFOOVFn位指示扫描组n的FIFO是否发生溢出。

当FIFOOVFn位为0时，在FIFO中未检测到溢出。当FIFOOVFn为1时，发生溢出FIFO和AD转换结果不能存储到FIFO。FIFOOVFn可以在ADFIFOERSCR中清零。

FIFOFLFn位（扫描组nFIFO数据读取请求标志）

FIFOFLFn指示是否检测到扫描组n中的FIFO数据读取请求。FIFOFLFn的设置和清除条件如下所示：

[Setting condition]

当检测到ADFIFOSRm.FIFOSTn[3:0]≤ADFIFOINTLRm.FIFOILVn[3:0]的条件时。

[Clearing condition]

当ADFIFOSRm.FIFOSTn[3:0]条件下ADFIFOERSCR.FIFOFLCn写入1> ADFIFOINTLRm.FIFOILVn[3:0].

当ADFIFOSRm.FIFOSTn[3:0]>ADFIFOINTLRm.FIFOILVn[3:0]的条件发生在读访问AFIFODDRn寄存器与DMAC或DTC。

Note: m = 0 to 4, n = 0 to 8

36.2.11.15 ADFIFOERSCR : FIFO Error Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xCF8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	FIFOFLCn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FIFOOVFCn								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOOVFCn	Scan Group n FIFO Overflow Flag Clear 0: No effect 1: ADFIFOERSR.FIFOOVFn is cleared	W
15:9	—	The write value should be 0.	W
24:16	FIFOFLCn	Scan Group n FIFO Data Read Request Flag Clear 0: No effect 1: ADFIFOERSR.FIFOFLFn is cleared	W
31:25	—	The write value should be 0.	W

Note: n = 0 to 8

ADFIFOERSCR clears the FIFO overflow flags and the FIFO data read request flags for scan group n.

36.2.12 Data Register

36.2.12.1 ADDRn : A/D Data Register n (n = 0 to 28)

Base address: ADC_B = 0x4017_0000

Offset address: 0x1000 + 0x04 × n

Bit position:	31															15														0
Bit field:	ERR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DATA[15:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DATA[15:0]	A/D conversion data	R
30:16	—	These bits are read as 0.	R
31	ERR	A/D conversion data error status 0: No error (the A/D conversion data is valid) 1: Error is detected (the A/D conversion data is not guaranteed)	R

The ADDRn registers are read-only registers to read A/D conversion results.

DATA[15:0] bits (A/D conversion data)

DATA[15:0] bits indicate the data of the A/D conversion result for the analog input channel n.

The data format of the A/D conversion results is determined by the setting of the virtual channel m (m = 0 to 36) to which the analog input channel n is assigned.

36.2.11.15 ADFIFOERSCR:FIFO错误状态清除寄存器

Base address: ADC_B = 0x4017_0000

Offset address: 0xCF8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	FIFOFLCn								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FIFOOVFCn								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOOVFCn	扫描组nFIFO溢出标志清除 0：无效1：ADFIFOERSR.FIFOOVFn清零	W
15:9	—	写入值应为0。	W
24:16	FIFOFLCn	扫描组nFIFO数据读取请求标志清除 0：无效1：ADFIFOERSR.FIFOFLFn清零	W
31:25	—	写入值应为0。	W

Note: n = 0 to 8

ADFIFOERSCR清除扫描组n的FIFO溢出标志和FIFO数据读取请求标志。

36.2.12 数据寄存器

36.2.12.1 ADDRn:AD数据寄存器n(n=0到28)

Base address: ADC_B = 0x4017_0000

Offset address: 0x1000 + 0x04 × n

Bit position:	31															15														0
Bit field:	ERR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DATA[15:0]														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DATA[15:0]	AD转换数据	R
30:16	—	这些位读为0。	R
31	ERR	AD转换数据错误状态 0：无错误（AD转换数据有效）1：检测到错误（不保证AD转换数据）	R

ADDRn寄存器是只读寄存器，用于读取AD转换结果。

DATA[15:0]位（AD转换数据）

DATA[15:0]位表示模拟输入通道n的A/D转换结果数据。

AD转换结果的数据格式由分配了模拟输入通道n的虚拟通道m（m=0至36）的设置决定。

ERR bit (A/D conversion data error status)

ERR bit indicates the error status in the A/D conversion for the analog input channel n.

When the ERR bit is 0, the A/D conversion data is valid. When the ERR bit is 1, the A/D conversion data is invalid, and the accuracy of the A/D conversion data is not guaranteed.

36.2.12.2 ADEXDRn : A/D Extended Analog Data Register n (n = 0 to 2, 5 to 8)

Base address: ADC_B = 0x4017_0000

Offset address: 0x1180 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ERR	—	—	—	—	DIAGSR[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DATA[15:0]	A/D conversion data	R
23:16	—	These bits are read as 0.	R
26:24	DIAGSR[2:0]*1	Self-Diagnosis Status*1	R
30:27	—	These bits are read as 0.	R
31	ERR	A/D Conversion Error Status 0: No error (the A/D conversion data is valid) 1: Error is detected (the A/D conversion data is not guaranteed)	R

Note 1. Only the ADEXDR0 register has the DIAGSR[2:0] bits. The DIAGSR[2:0] bits in the ADEXDRn register except for the ADEXDR0 register are reserved bits.

The ADEXDRn registers are read-only registers to read A/D conversion results of the extended analog function. The ADEXDRn registers and the extended analog functions are as follows:

- ADEXDR0 : Self-diagnosis
- ADEXDR1 : Temperature sensor
- ADEXDR2 : Internal reference voltage
- ADEXDR5 : D/A converter ch0 output
- ADEXDR6 : D/A converter ch1 output
- ADEXDR7 : D/A converter ch2 output
- ADEXDR8 : D/A converter ch3 output

DATA[15:0] bits (A/D conversion data)

DATA[15:0] bits indicate the data of the A/D conversion result for the extended analog function channel. The data format of the A/D conversion results is determined by the setting of the virtual channel m (m = 0 to 36) to which the extended analog function channel is assigned.

DIAGSR[2:0] bits (Self-Diagnosis Status)

DIAGSR[2:0] bits indicate the voltage setting of the self-diagnosis channel. DIAGSR[2:0] bits indicate the setting value in ADSGDCRm.DIAGVAL[2:0] bits (m = 0 to 8). DIAGSR[2:0] bits are only available in ADEXDR0. DIAGSR[2:0] bits in ADEXDRn except ADEXDR0 are reserved.

ERR bit (A/D Conversion Error Status)

ERR bit indicates the error status in the A/D conversion for the extended analog functions.

ERR位（AD转换数据错误状态）

ERR位指示模拟输入通道n的AD转换中的错误状态。

当ERR位为0时，AD转换数据有效。当ERR位为1时，AD转换数据无效，无法保证AD转换数据的准确性。

36.2.12.2 ATEXDRn:AD扩展模拟数据寄存器n(n=0到2 5到8)

Base address: ADC_B = 0x4017_0000

Offset address: 0x1180 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ERR	—	—	—	—	DIAGSR[2:0]			—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DATA[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DATA[15:0]	AD转换数据	R
23:16	—	这些位读为0。	R
26:24	DIAGSR[2:0]*1	Self-Diagnosis Status*1	R
30:27	—	这些位读为0。	R
31	ERR	AD转换错误状态 0：无错误（AD转换数据有效）1：检测到错误（不保证AD转换数据）	R

注1.只有ADEXDR0寄存器有DIAGSR[2:0]位。ADEXDRn寄存器中的DIAGSR[2:0]位（ADEXDR0寄存器除外）是保留位。

ADEXDRn寄存器是只读寄存器，用于读取扩展模拟功能的AD转换结果。这
ATEXDRn寄存器和扩展模拟功能如下：

- ADEXDR0 : Self-diagnosis
- ●ATEXDR1：温度传感器
- ●ATEXDR2：内部参考电压
- ●ATEXDR5:DA转换器ch0输出
- ●ATEXDR6:DA转换器ch1输出
- ●ATEXDR7:DA转换器ch2输出
- ●ATEXDR8:DA转换器ch3输出

DATA[15:0]位（AD转换数据）

DATA[15:0]位表示扩展模拟功能通道的AD转换结果数据。AD转换结果的数据格式由分配了扩展模拟功能通道的虚拟通道m（m=0至36）的设置决定。

DIAGSR[2:0] bits (Self-Diagnosis Status)

DIAGSR[2:0]位指示自诊断通道的电压设置。DIAGSR[2:0]位指示ADSGDCRm.DIAGVAL[2:0]位（m=0到8）中的设置值。DIAGSR[2:0]位仅在ADEXDR0中可用。DIAGSR[2:0]位
除了ATEXDR0之外的AEXDRn被保留。

ERR位（AD转换错误状态）

ERR位指示扩展模拟功能的AD转换中的错误状态。

When the ERR bit is 0, the A/D conversion data is valid. When the ERR bit is 1, the A/D conversion data is invalid, and the accuracy of the A/D conversion data is not guaranteed.

36.2.12.3 ADFIFODRn : FIFO Data Register n (n = 0 to 8)

Base address: ADC_B = 0x4017_0000

Offset address: 0x1200 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ERR	CH[6:0]							—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DATA[15:0]	A/D Conversion Data	R
23:16	—	These bits are read as 0.	R
30:24	CH[6:0]	A/D Conversion Channel Number	R
31	ERR	A/D Conversion Data Error Status 0: No error (the A/D conversion data is valid) 1: Error is detected (the A/D conversion data is not guaranteed)	R

The ADFIFODRn register is used to read data stored in the FIFO of scan group n.

DATA[15:0] bits (A/D Conversion Data)

DATA[15:0] bits are read-only bits that read the A/D conversion data stored in the scan group n FIFO.

CH[6:0] bits (A/D Conversion Channel Number)

CH[6:0] bits indicate the channel number of the A/D conversion data that is read from the DATA[15:0] bits.

ERR bit (A/D Conversion Data Error Status)

ERR bit indicates the error status in the A/D conversion data of the analog channel indicated by CH[6:0] bits.

When the ERR bit is 0, the A/D conversion data is valid. When the ERR bit is 1, the A/D conversion data is invalid, and the accuracy of the A/D conversion data is not guaranteed.

36.3 Operation

36.3.1 A/D Conversion clock

A/D conversion clock (ADCLK) is the operation clock of ADC. The A/D converters (ADC0 and ADC1) are operated and controlled by ADCLK as the basic clock. Figure 36.4 shows clock structure of ADC.

ADCLK is generated from the clock source and the division ratio selected in ADCLKCR register. The frequency of ADCLK should be set so that PCLKA ≥ ADCLK. Also, the frequency of ADCLK should be set so that it is within the guaranteed operating range specified in the electrical characteristics. For more details, refer to section 46, Electrical Characteristics.

当ERR位为0时，AD转换数据有效。当ERR位为1时，AD转换数据无效，无法保证AD转换数据的准确性。

36.2.12.3 AFIFODDRn：FIFO数据寄存器n（n=0到8）

Base address: ADC_B = 0x4017_0000

Offset address: 0x1200 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ERR	CH[6:0]							—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DATA[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DATA[15:0]	AD转换数据	R
23:16	—	这些位读为0。	R
30:24	CH[6:0]	AD转换通道号	R
31	ERR	AD转换数据错误状态 0：无错误（AD转换数据有效）1：检测到错误（不保证AD转换数据）	R

AFIFODDRn寄存器用于读取存储在扫描组n的FIFO中的数据。

DATA[15:0]位（AD转换数据）

DATA[15:0]位是只读位，用于读取存储在扫描组nFIFO中的AD转换数据。

CH[6:0]位（AD转换通道号）

CH[6:0]位指示从DATA[15:0]位读取的AD转换数据的通道号。

ERR位（AD转换数据错误状态）

ERR位指示由CH[6:0]位指示的模拟通道的AD转换数据中的错误状态。

当ERR位为0时，AD转换数据有效。当ERR位为1时，AD转换数据无效，无法保证AD转换数据的准确性。

36.3 Operation

36.3.1 AD转换时钟

D转换时钟(ADCLK)是ADC的操作时钟。AD转换器（ADC0和ADC1）由作为基本时钟的ADCLK操作和控制。图36.4显示了ADC的时钟结构。

ADCLK由时钟源和在ADCLKCR寄存器中选择的分频比生成。ADCLK的频率应设置为PCLKA≥ADCLK。此外，ADCLK的频率应设置在电气特性规定的保证工作范围内。有关详细信息，请参阅第46节，电气特性。

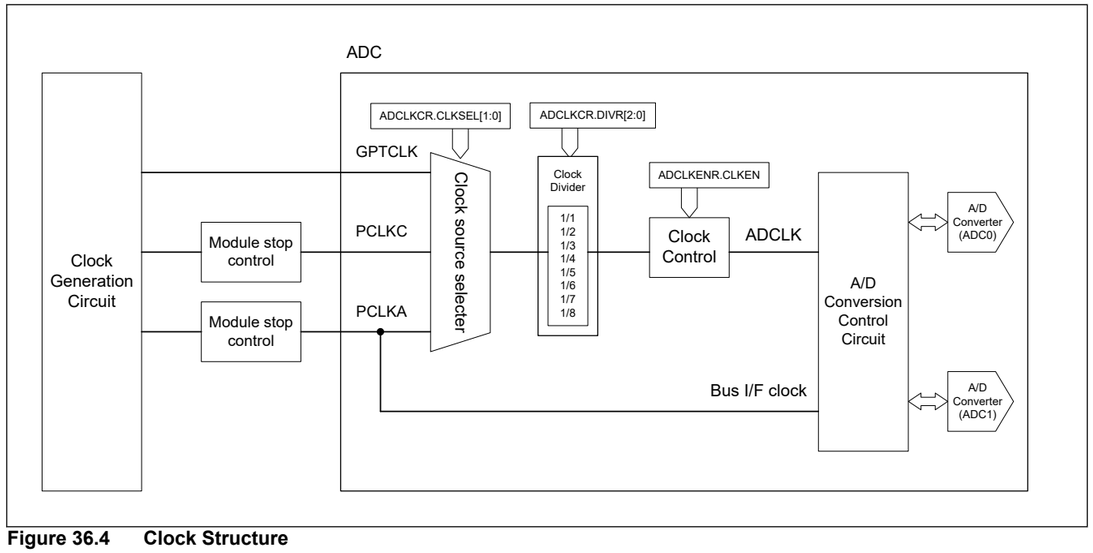


Figure 36.4 Clock Structure

36.3.2 Analog Channel

The analog channel is the source of the analog signal that is targeted for A/D conversion. The analog channels consist of the following elements:

- Analog input channels: A/D conversion channels for the analog input from MCU's I/O pin as the signal source.
- Extended analog channels: A/D conversion channels for the source of the analog signal inside the MCU.

To perform A/D conversion for the analog channels, assignments to the virtual channel and scan group are required. For each element, refer to each item.

36.3.3 Virtual Channel

The virtual channel is a group of registers that stores the A/D conversion configurations for a single analog channel. The virtual channels can be specified the analog channels for A/D conversion, the settings for A/D conversion, the data processing method, the assignment to scan groups, and so on.

To perform the A/D conversion of the analog channel, the analog channel should be assigned to any of the virtual channels. Then that virtual channel should be assigned to one of the scan groups. Refer to Figure 36.5 for the relationship between the analog channels and the virtual channels and scan groups. Figure 36.6 shows the A/D conversion order in Figure 36.5 settings.

The virtual channel can be assigned to only one scan group. When performing the A/D conversion on one analog channel in the different scan group, or when performing the A/D conversion several times within the same scan group, assign several virtual channels to one analog channel.

When performing the A/D conversion more than once using more than one virtual channel within the same scan group for the same analog channel, use the FIFO function in combination. When the FIFO function is not used, the A/D data register (ADDRn (n = 0 to 28)) or the A/D extended analog data register (ADEXDRm (m = 0 to2, 5 to 8)) stores only the data of the last A/D conversion in a scanning operation.

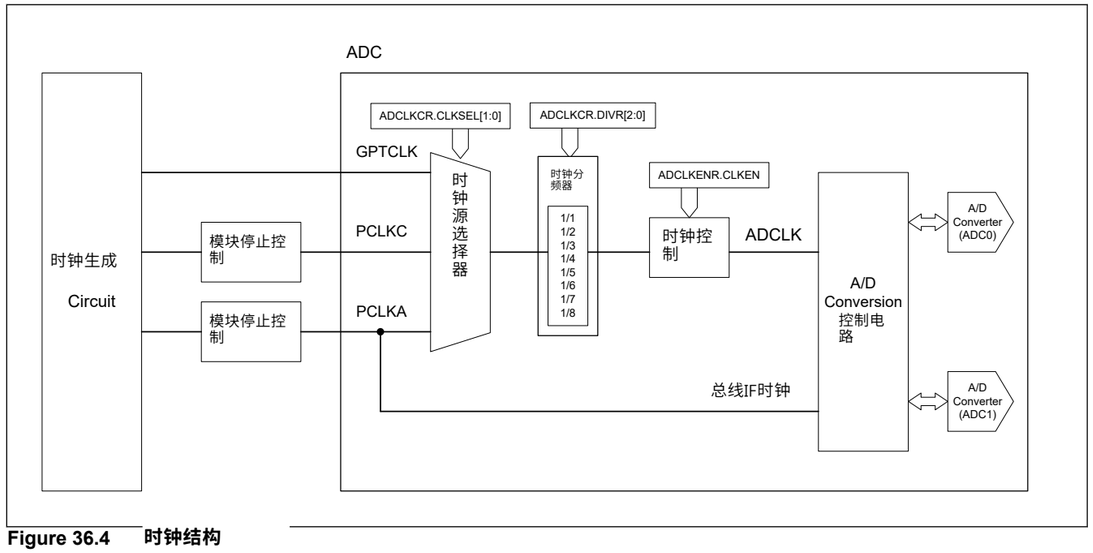


Figure 36.4 时钟结构

36.3.2 模拟频道

模拟通道是AD转换目标的模拟信号源。模拟通道由以下元素组成：

●模拟输入通道：单片机IO引脚作为信号源的模拟输入的AD转换通道。

●扩展模拟通道：MCU内部模拟信号源的D转换通道。

要对模拟通道执行AD转换，需要分配到虚拟通道和扫描组。对于每个元素，请参阅每个项目。

36.3.3 虚拟通道

虚拟通道是一组寄存器，用于存储单个模拟通道的AD转换配置。虚拟通道可以指定用于AD转换的模拟通道、AD转换的设置、数据处理方法、扫描组的分配等。

要执行模拟通道的AD转换，应将模拟通道分配给任何虚拟通道。然后应该将该虚拟通道分配给扫描组之一。模拟通道与虚拟通道和扫描组的关系见图36.5。图36.6显示了图36.5中的AD转换顺序设置。

虚拟通道只能分配给一个扫描组。对不同扫描组中的1个模拟通道进行AD转换时，或在同一扫描组内进行多次AD转换时，将多个虚拟通道分配给1个模拟通道。

使用同一扫描组内的多个虚拟通道对同一模拟通道进行多次AD转换时，请组合使用FIFO功能。不使用FIFO功能时，AD数据寄存器（ADDRn(n=0to28)）或AD扩展模拟数据寄存器（ADEXDRm(m=0to2 5to8)）只存储最后一个AD的数据扫描操作中的转换。

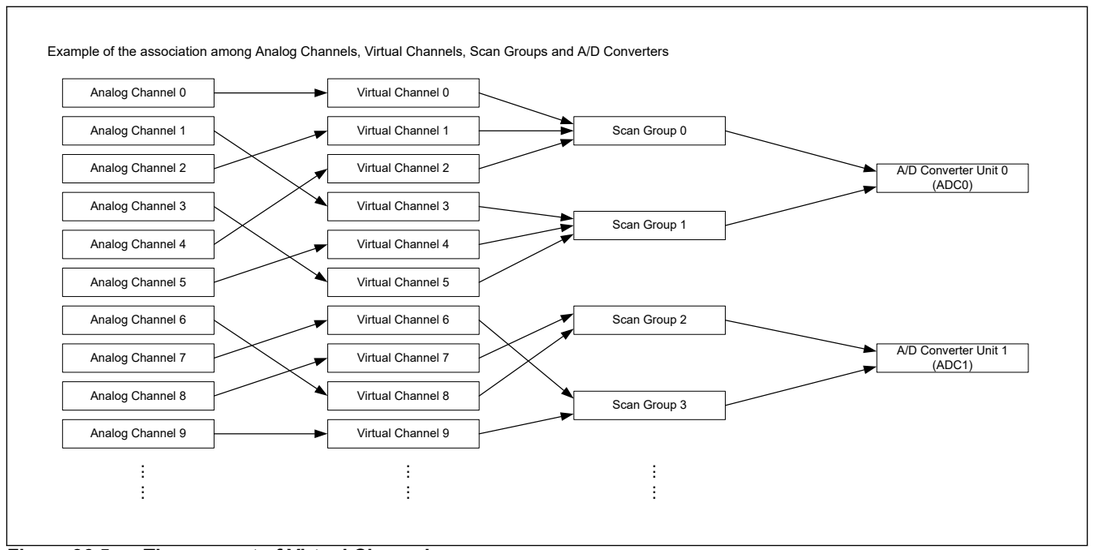


Figure 36.5 The concept of Virtual Channel

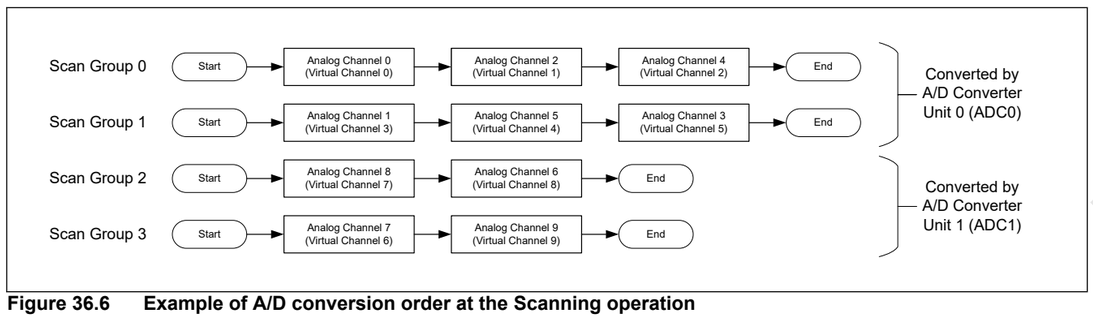


Figure 36.6 Example of A/D conversion order at the Scanning operation

36.3.4 Scan Group

The scan group is a group of the analog channels where the A/D conversions are performed on one scanning operation. To perform the A/D conversion using the scan group, configure the following steps:

- Assign the analog channel for the A/D conversion to the virtual channel.
- Assign the virtual channel to the scan group.
- Assign the scan group to A/D Converter.

Refer to Figure 36.5 and Figure 36.6 for the relationship among the analog channels, the virtual channels, and the scan groups.

A scan group can be assigned up to 8 virtual channels. If more than 9 virtual channels are assigned to a scan group, the 1st to 8th virtual channels in ascending order of the virtual channel number are targeted for A/D conversion, and the 9th and subsequent channels are not targeted for A/D conversion.

Notes on the scan groups

The virtual channels assigned to one scan group should be assigned the analog channels that can be converted by the same A/D converter. If any analog channels cannot be converted by the specified A/D converter are included, the A/D conversion result of those channels are undefined.

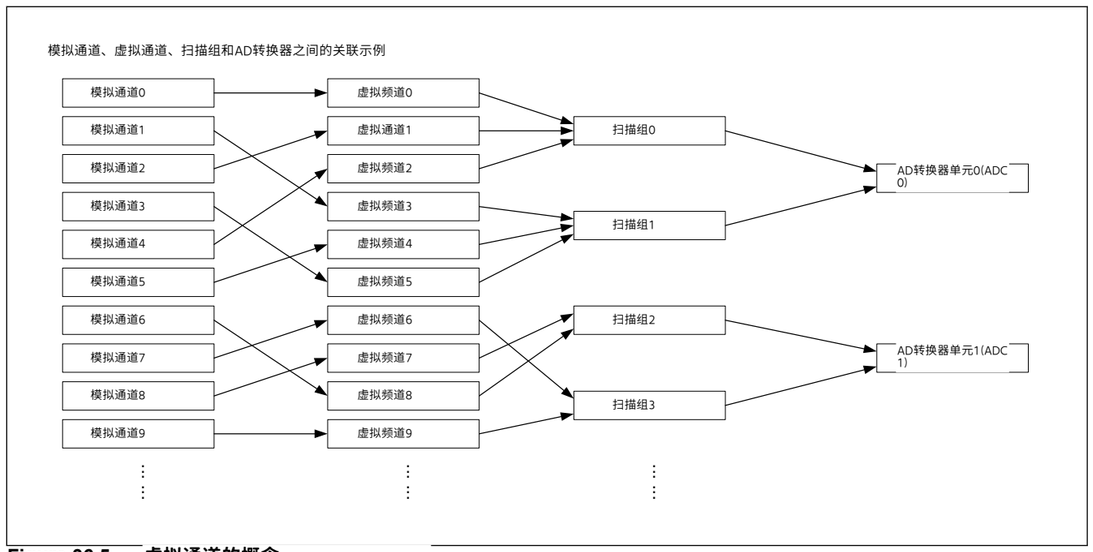


Figure 36.5 虚拟通道的概念

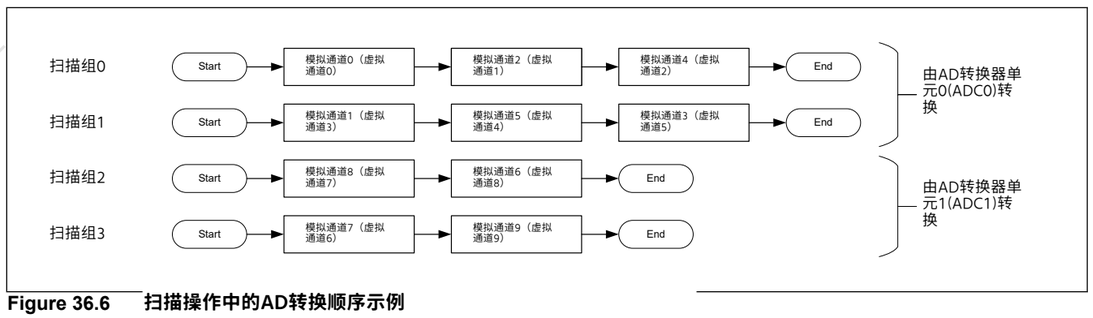


Figure 36.6 扫描操作中的AD转换顺序示例

36.3.4 扫描组

扫描组是一组模拟通道，其中对一次扫描操作执行AD转换。要使用扫描组执行AD转换，请配置以下步骤：

●将AD转换的模拟通道分配给虚拟通道。
●将虚拟通道分配给扫描组。
●将扫描组分配给模数转换器。

模拟通道、虚拟通道和扫描组之间的关系请参见图36.5和图36.6。

一个扫描组最多可以分配8个虚拟通道。如果为扫描组分配了9个以上的虚拟通道，则按虚拟通道编号升序排列的第1到第8个虚拟通道将成为AD转换的目标，而第9和后续通道将不作为AD转换的目标。

关于扫描组的说明

分配给一个扫描组的虚拟通道应分配可以由同一扫描组转换的模拟通道
一个D转换器。如果包含指定的AD转换器不能转换的模拟通道，则这些通道的AD转换结果是不确定的。

36.3.5 Scanning Operation

The scanning operation is the operation of sequential A/D conversion for the analog channels. The modes of the scanning operation are the followings:

- Single Scan mode
  - In single scan mode, one scan group is scanned once for each A/D converter start trigger input.
  - Each time an A/D conversion start trigger is input, A/D conversion is performed once for each analog channel assigned to that scan group.
- Continuous Scan mode
  - The continuous scan mode repeats the scanning operation of one scan group.
  - When an A/D conversion start trigger is input, A/D conversion of each analog channel assigned to that scan group is repeated until A/D conversion stop processing is performed.

The scanning operations are performed on a scan group basis. When the scanning operation is started, A/D conversion is performed for each analog channel based on the virtual channel setting. If 2 or more scan group assigned to the same A/D Converter are started at the same time, the scanning operation of the group with the smallest scan group number is started.

The A/D conversion order of the analog channel in the scanning operation is the ascending order of the virtual channel numbers assigned to the scan group. (The channels with the lowest virtual channel numbers are performed the A/D conversion at the forward end of the scan group. The channels with larger virtual channel numbers are performed the A/D conversion at the backward of the scan group.)

Refer to Figure 36.5 and Figure 36.6 for the relationship of the conversion order of the respective analog channel in the scanning operation.

36.3.5.1 Single Scan mode

Table 36.5 and Figure 36.7 show the operation example in Single Scan mode.

Table 36.5 Example of the scanning operation in Single Scan mode

Step	Operation
1	When a software trigger or a trigger from a peripheral module is input, the scanning operation of the scan group corresponding to the trigger is started.
2	Each time an A/D conversion of one analog channel is completed, A/D conversion result is stored to the data register (ADDRi (i = 0 to 28), ADEXDRj (j = 0 to 2, 5 to 8)). If FIFO is used, the A/D conversion result is also stored to the FIFO data register (ADFIFODRk (k = 0 to 8)).
3	If the Scan End Interrupt is enabled, the Scan End Interrupt corresponding to that scan group is generated when the A/D conversion of all virtual channels assigned to that scan group is completed.
4	During the scanning operation, ADGRSR.ACTGRn (n = 0 to 8) bit corresponding to that scan group is set to 1. ADSR.ADACTm (m = 0, 1) bit corresponding to the A/D Converter performing the A/D conversion is also set to 1. When scanning operation is complete, each bit is cleared to 0 and A/D Converter enters standby.

36.3.5 扫描操作

扫描操作是模拟通道的顺序AD转换操作。扫描操作的模式如下：

●单次扫描模式

在单次扫描模式下，每个AD转换器启动触发输入扫描一个扫描组一次。

每次输入AD转换开始触发时，对分配给该扫描组的每个模拟通道执行一次AD转换。

●连续扫描模式

连续扫描模式重复一个扫描组的扫描操作。

当输入AD转换开始触发时，将重复分配给该扫描组的每个模拟通道的AD转换，直到执行AD转换停止处理。

扫描操作以扫描组为基础进行。当开始扫描操作时，根据虚拟通道设置对每个模拟通道进行AD转换。如果同时启动分配给同一AD转换器的2个或多个扫描组，则开始扫描组号最小的组的扫描操作。

扫描操作中模拟通道的AD转换顺序是分配给扫描组的虚拟通道号的升序。（虚拟通道号最小的通道在扫描组的前端进行AD转换。虚拟通道号较大的通道在扫描组的后端进行AD转换。）

扫描操作中各模拟通道的转换顺序关系请参考图36.5和图36.6。

36.3.5.1 单次扫描模式

表36.5和图36.7显示了单次扫描模式下的操作示例。

Table 36.5 单次扫描模式下的扫描操作示例

Step	Operation
1	当输入软件触发或来自外围模块的触发时，触发对应的扫描组的扫描操作开始。
2	每次完成一个模拟通道的AD转换，AD转换结果被存储到数据寄存器（ADDRi（i=0到28）、ADEXDRj（j=0到2、5到8））。如果使用FIFO，AD转换结果也存储到FIFO数据寄存器（AFIFODRk(k=0to8)）。
3	如果启用了扫描结束中断，则当分配给该扫描组的所有虚拟通道的AD转换完成时，将产生与该扫描组对应的扫描结束中断。
4	在扫描操作期间，对应于该扫描组的ADGRSR.ACTGRn（n=0到8）位设置为1。 对应于执行AD转换的AD转换器的ADSR.ADACTm(m=0 1)位也设置为1。 扫描操作完成后，每个位都被清零，AD转换器进入待机状态。

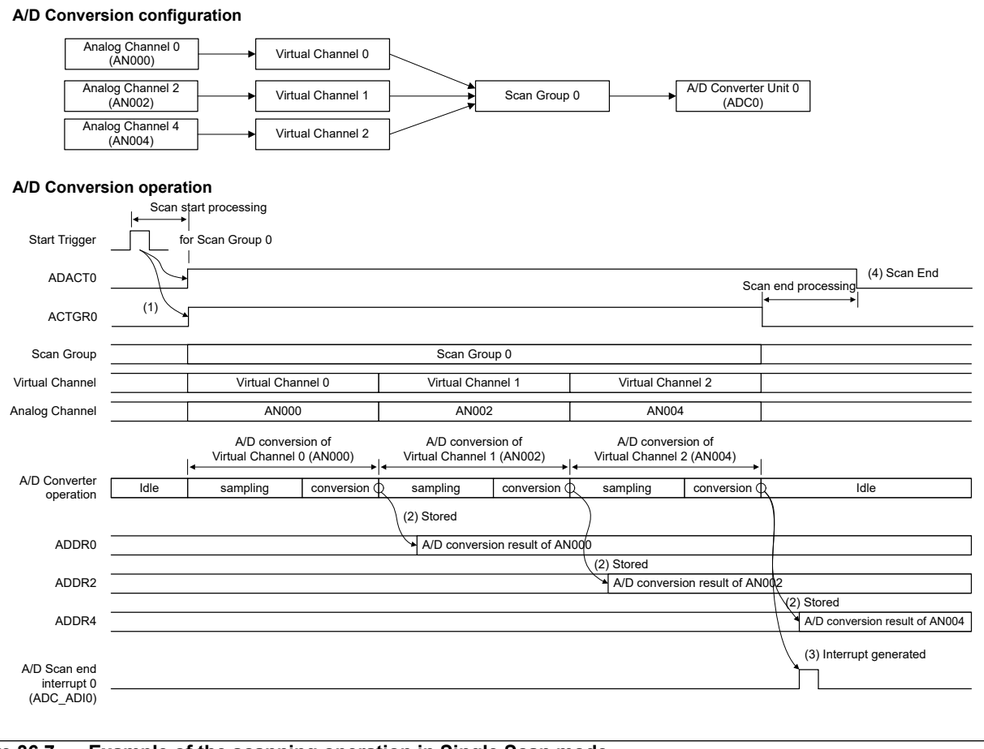


Figure 36.7 Example of the scanning operation in Single Scan mode

36.3.5.2 Continuous Scan mode

Table 36.6 and Figure 36.8 show the operation example in Continuous Scan mode.

Table 36.6 Example of the scanning operation in Continuous Scan mode

Step	Operation
1	When a software trigger or a trigger from a peripheral module is input, the scanning operation of the scan group corresponding to the trigger is started. When scanning operation starts, ADGRSR.ACTGRn (n = 0 to 8) corresponding to that scan group is set to 1. ADSR.ADACTm (m = 0, 1) bit corresponding to the A/D Converter performing the A/D conversion is also set to 1.
2	Each time an A/D conversion of one analog channel is completed, A/D conversion result is stored to the data register (ADDRi (i = 0 to 28), ADEXDRj (j = 0 to 2, 5 to 8)). If FIFO is used, the A/D conversion result is also stored to the FIFO data register (ADFIFODRk (k = 0 to 8)).
3	If the Scan End Interrupt is enabled, the Scan End Interrupt corresponding to that scan group is generated when the A/D conversion of all virtual channels assigned to that scan group is completed.
4	Step 2 and Step 3 are repeated until the A/D conversion stop process is performed, and scanning operation continues. To stop A/D conversion, follow section 36.5.4. Force stops the A/D conversion operation.

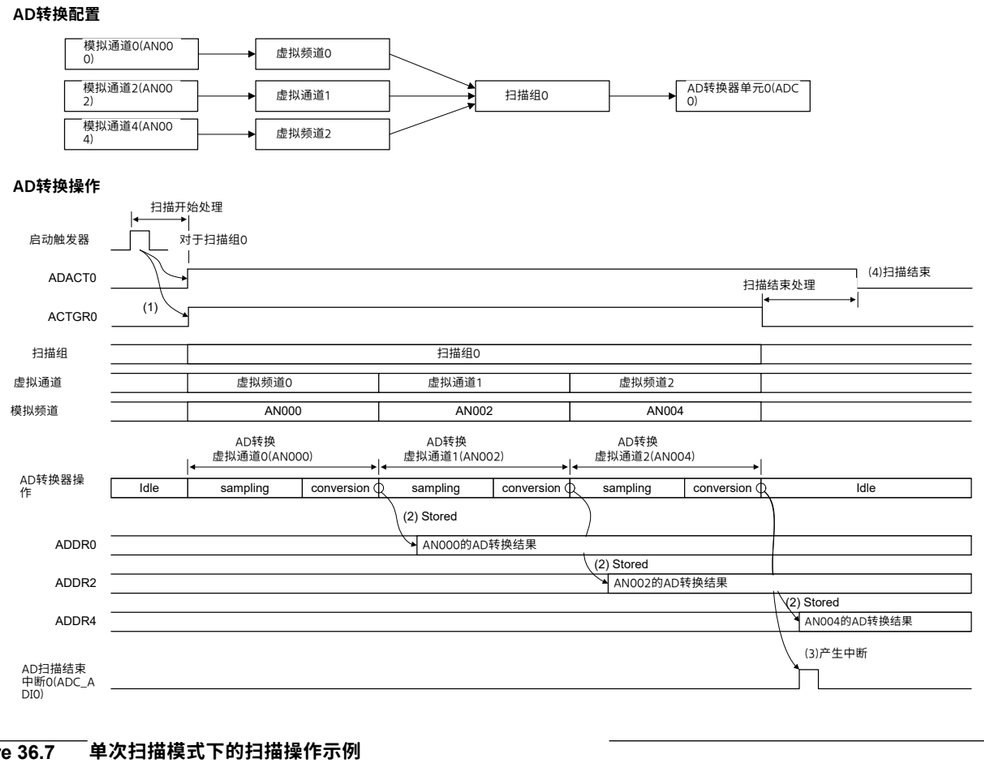


Figure 36.7 单次扫描模式下的扫描操作示例

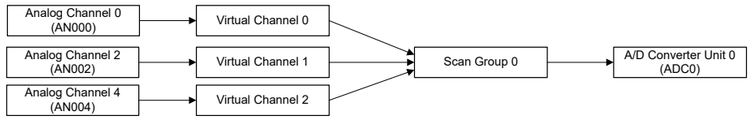
36.3.5.2 连续扫描模式

表36.6和图36.8显示了连续扫描模式下的操作示例。

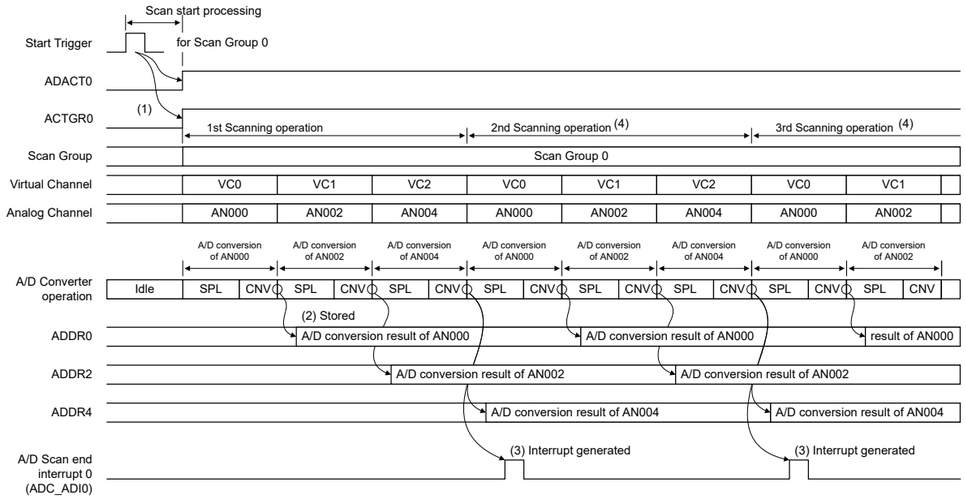
Table 36.6 连续扫描模式下的扫描操作示例

Step	Operation
1	当输入软件触发或来自外围模块的触发时，触发对应的扫描组的扫描操作开始。当扫描操作开始时，对应于该扫描组的ADGRSR.ACTGRn（n=0到8）设置为1。 对应于执行AD转换的AD转换器的ADSR.ADACTm(m=0 1)位也设置为1。
2	每次完成一个模拟通道的AD转换，AD转换结果被存储到数据寄存器（ADDRi（i=0到28）、ADEXDRj（j=0到2、5到8））。如果使用FIFO，AD转换结果也存储到FIFO数据寄存器（AFIFODRk(k=0to8)）。
3	如果启用了扫描结束中断，则当分配给该扫描组的所有虚拟通道的AD转换完成时，将产生与该扫描组对应的扫描结束中断。
4	重复步骤2和步骤3直到执行AD转换停止过程，并继续扫描操作。 要停止AD转换，请遵循第36.5.4节。强制停止AD转换操作。

A/D Conversion configuration



A/D Conversion operation



Note: VC: Virtual Channel SPL: Sampling state CNV: Conversion state

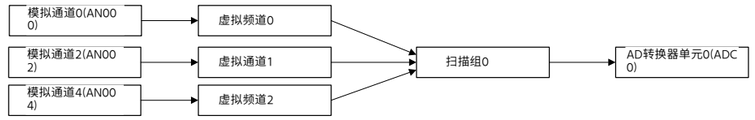
Figure 36.8 Example of the scanning operation in Continuous Scan mode

36.3.6 Self-Calibration

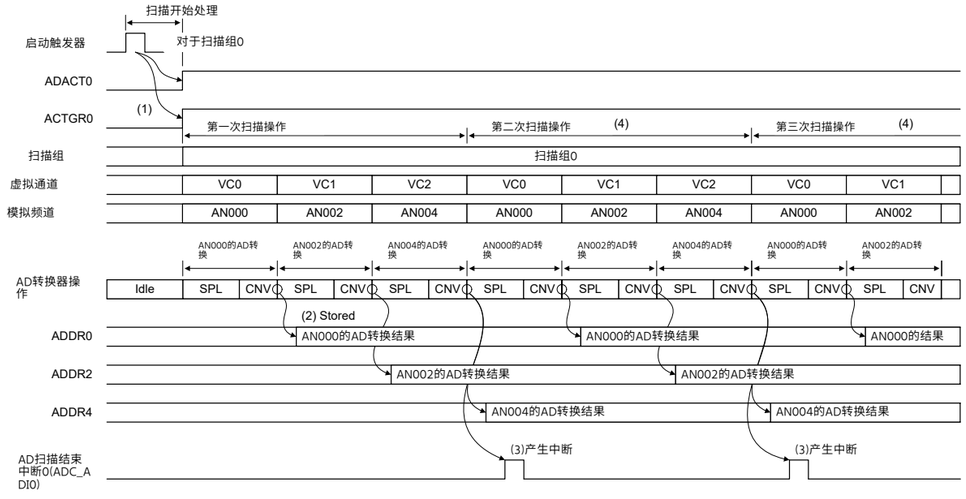
ADC has a built-in Self-Calibration function. Self-Calibration function is used to calibrate the variations of characteristics caused by the chip-by-chip variations. Self-Calibration function has the following operations.

1. Internal Circuit Calibration
   - Adjusts the operation of A/D Converter's internal circuitry.
2. Gain and Offset Calibration
   - Measure the A/D Converter's Gain Error and Offset Error.
   - The calibration processing of the A/D conversion result based on the measured error data is performed after the A/D conversion.
     For more details, refer to section 36.4.2.1. Gain Error and Offset Error Calibration.
   - This Self-Calibration should be performed after Internal-circuit Self-Calibration is completed.
3. Channel-dedicated sample-and-hold circuit Gain and Offset Calibration
   - Measure the Gain Error and the Offset Error when using the Channel-dedicated sample-and-hold circuit.
   - The calibration processing of the A/D conversion result based on the measured error data is performed after the A/D conversion.
     For more details, refer to section 36.4.2.1. Gain Error and Offset Error Calibration.
   - This Self-Calibration should be performed after A/D Converter Gain/Offset Self-Calibration is completed.

AD转换配置



AD转换操作



Note: VC：虚拟通道SPL：采样状态CNV：转换状态

Figure 36.8 连续扫描模式下的扫描操作示例

36.3.6 Self-Calibration

ADC具有内置的自校准功能。自校准功能用于校准因芯片变化引起的特性变化。自校准功能具有以下操作。

1.内部电路校准

●调整AD转换器内部电路的操作。

2.增益和偏移校准

●测量AD转换器的增益误差和失调误差。

●基于测得的误差数据对AD转换结果的校准处理是在AD转换之后进行的。有关详细信息，请参阅第36.4.2.1节。增益误差和偏移误差校准。

●此自校准应在内部电路自校准完成后进行。

3.通道专用采样保持电路增益和偏移校准

●使用通道专用采样保持电路测量增益误差和偏移误差。

●基于测得的误差数据对AD转换结果的校准处理是在AD转换之后进行的。有关详细信息，请参阅第36.4.2.1节。增益误差和偏移误差校准。

●此自校准应在AD转换器增益偏移自校准完成后执行。

36.3.6.1 Conditions under which Self-Calibration is required

The conditions under which Self-Calibration is required are shown in Table 36.7. Under the conditions shown in Table 36.7, Self-Calibration should be performed before using the A/D converter. If A/D Converter is operating, stop all A/D Converters and perform the Self-Calibration again. If the required Self-Calibration is not performed, the A/D conversion result is not guaranteed.

Table 36.7 List of conditions under which Self-calibration should be performed

Conditions under which Self-Calibration is required	Internal-circuit Calibration	Gain/Offset Calibration	Channel-dedicated sample-and-hold circuit Gain and Offset Calibration *1
After reset release	✓	✓	✓
After releasing the module stop	✓	✓	✓
When returning from Software Standby mode or Deep Software Standby mode	✓	✓	✓
When changed the ADCLK setting (When clock source or frequency is changed)	✓	✓	✓
When changed the operating mode of the AD converter (When changed ADMDR.ADMDm bit (m = 0, 1))	✓	✓	—
When changed A/D successive approximation time (When changed ADCNVSTR.CSTm bit (m = 0, 1))	✓	✓	—
When changed the operation setting of the Channel-dedicated sample-and-hold circuit *1	—	—	✓

Note: ✓: Self-calibration should be performed.
—: Self-calibration is not required.
Note 1. When any of ADSHCRm.SHENn bits are set to 1, perform the Channel-dedicated Sample-and-Hold circuits Self-Calibration (m = 0, 1. n = 0 to 2, 4 to 6). Not required if the Channel-dedicated sample-and-hold circuits are not used.

36.3.6.2 Self-Calibration procedure

Table 36.8 shows the Self-Calibration procedures.

Table 36.8 Procedure for Self-Calibration (1 of 2)

No.	Step	Description
1	Disable trigger input	Disables the trigger input from the peripheral module. (Write ADTRGENR.STTRGENn = 0)
2	Waiting for all A/D Converters to stop	Check that all A/D converters are stopped. If AD conversion is operating wait until the A/D converter stops by either of the following: ● Wait until all A/D conversions are complete ● Force the A/D converter to stop the operation using the ADSTOPR register. For details on forced stopping of A/D conversion operation, refer to section 36.5.4. Force stops the A/D conversion operation.
3	Setting the number of states for Self-Calibration	Set the number of states for the Self-Calibration of A/D Converter to ADCALSTCR register. The values in ADCALSTCR register are commonly used for ADC0 and ADC1. Set the value to be set in ADCALSTCR register to satisfy the range defined in section 46, Electrical Characteristics.
4	Clearing the Error Status Flag	If error flags are detected, clear them before performing the Self-Calibration. (A/D Converter error flag, A/D Converter overflow flag, etc.)
5	Performing the Self-Calibration for ADC0	Performs the Self-Calibration for ADC0. ● Internal-circuit Calibration ● Gain/Offset Calibration After starting the Self-Calibration, wait until it is completed.
6	Performing the Self-Calibration for ADC1	Performs the Self-Calibration for ADC1 in the same as Step 5.

36.3.6.1 需要自校准的条件

需要自校准的条件如表36.7所示。在表36.7所示条件下，
使用AD转换器前应进行自校准。如果AD转换器正在运行，请停止所有AD
转换器并再次执行自校准。如果未执行所需的自校准，则无法保证AD转换结果。

Table 36.7 应执行自校准的条件列表

需要自校准的条件	Internal-circuit Calibration	Gain/Offset Calibration	通道专用采样保持电路增益和偏移 Calibration *1
复位释放后	✓	✓	✓
释放模块后停止	✓	✓	✓
从软件待机模式或深度软件待机模式返回时	✓	✓	✓
更改ADCLK设置时（更改时钟源或频率时）	✓	✓	✓
当改变AD转换器的操作模式时（当改变ADMDR.ADMDm位(m=0 1)）	✓	✓	—
当改变AD逐次逼近时间(当改变ADCNVSTR.CSTm位(m=0 1))	✓	✓	—
更改通道专用采样保持电路的操作设置时*1	—	—	✓

Note: ：应进行自校准。—：不需要自校准。
注1.当任何ADSHCRm.SHENn位设置为1时，执行通道专用采样保持电路自校准（m=0、1。n=0到2、4到6）。如果不使用通道专用的采样保持电路，则不需要。

36.3.6.2 Self-Calibration procedure

表36.8显示了自校准程序。

Table 36.8 自校准程序(1of2)

No.	Step	Description
1	禁用触发输入	禁用来自外围模块的触发输入。（写ADTRGENR.STTRGENn=0）
2	等待所有AD转换器停止	检查所有AD转换器是否已停止。 如果AD转换正在运行，请等待AD转换器通过以下任一方式停止：● 等到所有AD转换完成 ● 使用ADSTOPR寄存器强制AD转换器停止操作。 关于强制停止AD转换操作的详细内容，请参阅36.5.4项。 强制停止AD转换操作。
3	设置Self的状态数 Calibration	将AD转换器自校准的状态数设置到ADCALSTCR寄存器。ADCALSTCR寄存器中的值通常用于ADC0和ADC1。设置要在ADCALSTCR寄存器中设置的值，以满足第46节“电气特性”中定义的范围。
4	清除错误状态标志	如果检测到错误标志，请在执行自校准之前清除它们。（广告转换器错误标志、AD转换器溢出标志等）
5	为ADC0执行自校准	执行ADC0的自校准。● ● Gain/Offset Calibration 启动自校准后，等待它完成。
6	为ADC1执行自校准	与步骤5相同，对ADC1执行自校准。

Table 36.8 Procedure for Self-Calibration (2 of 2)

No.	Step	Description
7	Setting the Self-Calibration of Channel-dedicated sample-and-hold circuit *1	Make settings for Self-Calibration of Channel-dedicated sample-and-hold circuit. Enable Channel-dedicated sample-and-hold circuit. *2 Sets the number of states for channel-dedicated sample-and-hold Self-Calibration (ADCALSTCR register *3 and ADCALSHCR register).
8	Performing Channel-dedicated sample-and-hold circuit Self-Calibration for SH0 0 to SH2. *1	Performs the Self-Calibration for Channel-dedicated sample-and-hold circuit (SH0 to SH2) connected to ADC0. ● Channel-dedicated sample-and-hold circuit Gain/Offset Calibration After starting Self-Calibration, wait until it is completed.
9	Performing Channel-dedicated sample-and-hold circuit Self-Calibration for SH4 to SH6 *1	Performs the Self-Calibration for Channel-dedicated sample-and-hold circuit (SH4 to SH6) connected to ADC1 in the same as Step 8.
10	Error Status Check *4	Check for errors in Self-Calibration. If no operating error occurs, Self-Calibration is complete.

Note: In order to increase the effectiveness of Self-Calibration, it is recommended to perform Self-Calibration for the A/D converters one by one.
Note 1. Not required if the Channel-dedicated sample-and-hold circuits are not used.
Note 2. Enable all Channel-dedicated sample-and-hold circuits connected to ADCm (m = 0, 1).
Note 3. When the Self-Calibration the channel-dedicated sample-and-hold circuitry, the number of sampling states at the Self-Calibration of the A/D converter (ADCALSTCR.CALASSST[9:0] bits) may also need to be changed. Set the value that satisfies the electrical characteristics.
Note 4. If the A/D Converter Error is detected by the Self-Calibration, it may be set outside the operation guaranteed range specified in the electric characteristics. Check the operation setting.

36.3.6.3 Restrictions on Self-Calibration

(1) Prohibition of the scanning operation during Self-Calibration

Do not start the scanning operation during Self-Calibration. When performing the scanning operation, start the scanning operation after Self-Calibration is completed. Operation is not guaranteed when the scanning operation is started during Self-Calibration.

(2) Prohibition of additional writes to the ADCALSTR register during Self-Calibration

After the Self-Calibration is started, writing to ADCALSTR register is prohibited until Self-Calibration is completed. Write to ADCALSTR register after Self-Calibration is completed. Operation is not guaranteed if this restriction is violated.

(3) Prohibition of forcibly stop during Self-Calibration

Do not force stop with the ADSTOPR register during Self-Calibration. Even if the A/D conversion operation is to be stopped forcibly due to a system error or exception handling, be sure to wait until the Self-Calibration is complete. Operation is not guaranteed when forced to stop during Self-Calibration.

(4) Restrictions on Self-Calibration for Channel-dedicated sample-and-hold circuit

To perform the Self-Calibration for the Channel-dedicated sample-and-hold circuit, all Channel-dedicated sample-and-hold circuits connected to the A/D converter should be enabled as follows.

- For ADC0: Set 1 for ADSHCR0.SHEN0 to SHEN2 bit
- For ADC1: Set 1 for ADSHCR1.SHEN4 to SHEN6 bit

If there is a Channel-dedicated sample-and-hold circuit that is not used, set it to disabled (ADSHCRm.SHENn = 0 (m = 0, 1. n = 0 to 2, 4 to 6) after Self-Calibration completes.

Operation is not guaranteed when the Self-Calibration for the Channel-dedicated sample-and-hold circuit is performed while any Channel-dedicated sample-and-hold circuit are disabled.

(5) Restrictions on the Self-Calibration

Self-calibration should be performed for the A/D converters one by one. During the Self-Calibration operation, the other A/D converters should be in idle (not in scan operation or Self-Calibration operation).

Table 36.8 自校准程序（2之2）

No.	Step	Description
7	设置通道专用采样保持电路的自校准*1	对通道专用采样保持电路的自校准进行设置。 启用通道专用的采样保持电路。*2 设置通道专用采样保持自校准的状态数（ADCALSTCR寄存器*3和ADCALSHCR寄存器）。
8	对SH00到SH2执行通道专用的采样和保持电路自校准。*1	执行通道专用采样保持电路的自校准（SH0至SH2)连接到ADC0。● 通道专用采样保持电路增益偏移校准 开始自校准后，等待它完成。
9	执行SH4至SH6的通道专用采样和保持电路自校准*1	执行通道专用采样保持电路的自校准（SH4至SH6)与步骤8相同，连接到ADC1。
10	错误状态检查*4	检查自校准中的错误。 如果没有发生操作错误，则自校准完成。

Note: 为了提高自校准的有效性，建议对AD转换器逐一进行自校准。

注1.如果不使用通道专用的采样保持电路，则不需要。
注2.使能所有连接到ADCm的通道专用采样保持电路(m=0 1)。
注3.当对通道专用的采样保持电路进行自校准时，ADC转换器的自校准时的采样状态数（ADCALSTCR.CALASSST[9:0]位）可能也需要更改.设置满足电气特性的值。

注4.如果通过自校准检测到AD转换器错误，则可能设置在电气特性规定的操作保证范围之外。检查操作设置。

36.3.6.3 自校准的限制

(1) 自校准期间禁止扫描操作

请勿在自校准期间启动扫描操作。执行扫描操作时，请在自校准完成后开始扫描操作。在自校准期间开始扫描操作时，无法保证操作。

(2) 在自校准期间禁止对ADCALSTR寄存器进行额外的写入

自校准开始后，在自校准完成之前，禁止写入ADCALSTR寄存器。自校准完成后写入ADCALSTR寄存器。如果违反此限制，则无法保证操作。

(3) 自校准期间禁止强行停止

在自校准期间不要使用ADSTOPR寄存器强制停止。即使由于系统错误或异常处理而强制停止AD转换操作，也请务必等到自校准完成。在自校准期间强制停止时无法保证操作。

(4) 通道专用采样保持电路自校准的限制

要对通道专用采样保持电路执行自校准，连接到AD转换器的所有通道专用采样保持电路应启用如下。

●对于ADC0：将ADSHCR0.SHEN0到SHEN2位设置为1
●对于ADC1：将ADSHCR1.SHEN4到SHEN6位设置为1

如果有一个未使用的通道专用采样保持电路，则在自校准完成后将其设置为禁用(ADSHCRm.SHENn=0(m=0 1.n=0to2 4to6).

在禁用任何通道专用采样和保持电路的情况下执行通道专用采样保持电路的自校准时，不能保证操作。

(5) 自校准的限制

应对AD转换器一一进行自校准。在自校准操作期间，其他AD转换器应处于空闲状态（不在扫描操作或自校准操作中）。

If this restriction is violated, the A/D conversion accuracy will be degraded due to noise during the self-calibration operation. In this case, the A/D Converter characteristics are not guaranteed.

In addition, in order to enhance the effect of Self-Calibration, Self-Calibration operation should be performed under conditions with as little noise as possible.

(6) Restrictions on setting of the number of status for Self-Calibration

The number of states to be set in the ADCALSTCR and ADCALSHCR registers should be set to satisfy the values specified in the Electrical Characteristics. In addition, the number of states involved in Self-calibration should be set to satisfy the following restrictions.

If these restrictions are violated, A/D conversion results are not guaranteed.

[Restrictions on setting of ADCALSTCR register]

- ADCALSTCR.CALADSST[9:0] bits
  - According to the type of Self-Calibration, set the values to satisfy those specified in the electrical characteristics.
  - If the setting value differs according to the type of Self-Calibration, change the register setting value for each Self-Calibration.
- ADCALSTCR.CALADCST[5:0] bits
  - Set the same value as ADCNVSTR.CSTm[5:0] (m = 0, 1) bits.
    (ADCALSTCR.CALADCST[9:0] = ADCNVSTR.CSTm[5:0])

[Restrictions on setting of ADCALSHCR register] (only when Channel-dedicated sample-and-hold circuit is used)

- ADCALSHCR.CALSHSST[7:0] bits
  - Set the value equal to the value of the ADSHSTRm.SHSST[7:0] bits plus 1 (m = 0, 1).
    (ADCALSHCR.CALSHSST[7:0] = ADSHSTRm.SHSST[7:0] + 1)
  - If the setting values of ADSHSTR0.SHSST[7:0] and ADSHSTR1.SHSST[7:0] are different, change the register setting values of CALSHSST[7:0] for each Self-Calibration of ADC0 (SH0 to SH2) and ADC1 (SH4 to SH6).
- ADCALSHCR.CALSHHST[2:0] bits
  - Set the same value as ADSHSTRm.SHHST[2:0] (m = 0, 1) bits.

36.3.7 Analog Input Channel

For the correspondence between the analog input pins and the analog channel numbers, the A/D converters, Programmable Gain Amplifier, and Channel-dedicated sample-and-hold circuit, refer to Table 36.3.

36.3.8 Extended Analog Function

Extended Analog Function performs A/D conversion on the internal signal source of MCU. The available sources for Extended Analog Function are shown in the following:

- Self-diagnosis voltage
- Internal Reference Voltage
- Temperature Sensor
- D/A Converter Output (Internal Output Path to ACMPHS)

36.3.9 Self-diagnosis Function

This A/D converter has a built-in self-diagnosis function. The self-diagnosis function inputs the self-diagnosis voltage to the A/D converter and performs A/D conversion. The A/D conversion result of the self-diagnosis voltage can be used to confirm that the A/D converter is operating normally.

36.3.9.1 Self-diagnosis Configuration

The procedure for self-diagnosis of the A/D converter is shown in the following:

如果违反此限制，则AD转换精度将因自校准操作期间的噪声而降低。在这种情况下，不能保证AD转换器的特性。

此外，为了增强自校准的效果，自校准操作应在噪声尽可能小的条件下进行。

(6) 自校准状态数设置限制

在ADCALSTCR和ADCALSHCR寄存器中设置的状态数应设置为满足电气特性中指定的值。此外，Self-calibration中涉及的状态数应设置为满足以下限制。

如果违反这些限制，则无法保证AD转换结果。

[ADCALSTCR寄存器的设置限制]

- ADCALSTCR.CALADSST[9:0] bits
  根据自校准的类型，设置值以满足电气特性中规定的值。
  如果设置值因Self-Calibration类型而异，请更改每个SelfCalibration的寄存器设置值。
- ADCALSTCR.CALADCST[5:0] bits
  设置与ADCNVSTR.CSTm[5:0](m=0 1)位相同的值。（ADCALSTCR.CALADCST[9:0]=ADCNVSTR.CSTm[5:0]）

[ADCALSHCR寄存器的设置限制]（仅当使用通道专用采样保持电路时）

- ADCALSHCR.CALSHSST[7:0] bits
  将该值设置为等于ADSHSTRm.SHSST[7:0]位的值加1(m=0 1)。（ADCALSHCR.CALSHSST[7:0]=ADSHSTRm.SHSST[7:0]+1）
  如果ADSHSTR0.SHSST[7:0]和ADSHSTR1.SHSST[7:0]的设置值不同，请更改每次ADC0自校准（SH0至SH2）的CALSHSST[7:0]寄存器设置值和ADC1（SH4至SH6）。
- ADCALSHCR.CALSHHST[2:0] bits
  设置与ADSHSTRm.SHHST[2:0](m=0 1)位相同的值。

36.3.7 模拟输入通道

对于模拟输入引脚和模拟通道号之间的对应关系，AD转换器，可编程增益放大器和通道专用的采样保持电路，请参见表36.3。

36.3.8 扩展模拟功能

扩展模拟功能对MCU的内部信号源进行AD转换。可用的资源
扩展模拟功能如下所示：

- Self-diagnosis voltage

●内部参考电压

●温度传感器

●DA转换器输出（到ACMPHS的内部输出路径）

36.3.9 Self-diagnosis Function

该AD转换器具有内置自诊断功能。自诊断功能将自诊断电压输入到AD转换器并执行AD转换。自诊断电压的AD转换结果可用于确认AD转换器工作正常。

36.3.9.1 Self-diagnosis Configuration

AD转换器的自诊断程序如下所示：

1. Assign the self-diagnosis channel to one of the virtual channels and configure the virtual channel.
2. Assign the virtual channel for which the self-diagnosis channel has been selected to one of the scan groups.
3. Set the self-diagnosis voltage in the ADSGDCRn.DIAGVAL[2:0] (n = 0 to 8) bits corresponding to the scan group assigned in 2. above.
4. When the scan group to which the self-diagnosis channel is assigned is started the scanning and A/D conversion of the self-diagnosis channel is started, the self-diagnosis operation is executed.

Table 36.9 shows the operation setting when the self-diagnosis function is used. When using the self-diagnosis function, follow the settings in Table 36.9. If self-diagnosis operation is performed with the settings other than those shown in Table 36.9, the self-diagnosis result (A/D conversion result) is not guaranteed.

Table 36.9 Operation setting and expected value when self-diagnosis function is used

Self-diagnosis mode	Register setting value				Expected value of A/D conversion data *1 *2
	ADSGDCRx	ADCHCRy		ADDOPCRCy	
	DIAGVAL[2:0]	CNVCS[6:0]	AINMD	SIGNSEL	
Self-diagnosis mode 1	100b	0x60	1	1	0x0000 *3
Self-diagnosis mode 2	101b	0x60	1	1	0x8000 *4
Self-diagnosis mode 3	110b	0x60	1	1	0x7FFF *5

Note: x = 0 to 8, y = 0 to 36
Note 1. The expected value is the ideal A/D converter result stored in ADEXDR0.DATA[15:0] or ADFIFODRx.DATA[15:0].
Note 2. The A/D conversion data is the value when 16-bit data format (ADDOPCRn.ADPRC[1:0] = 00b) is selected.
Note 3. The expected value of A/D conversion is the signed data. The A/D conversion result becomes 0x0001 (+1) or more when a positive accuracy error occurs in A/D conversion, and becomes 0xFFFF (-1) or less when a negative accuracy error occurs.
Note 4. When an accuracy error occurs in A/D conversion, the A/D conversion result is a value greater than or equal to 0x8000.
Note 5. When an accuracy error occurs in A/D conversion, the A/D conversion result is less than or equal to 0x7FFF.

36.3.9.2 Notes on self-diagnosis function

(1) Notes on performing the Self-Diagnosis

The data register (ADEXDR0) to store the self-diagnosis result is shared by all A/D converters. When performing the self-diagnosis, ADEXDR0 register is overwritten by the result of the later self-diagnosis operation. If self-diagnosis operations of ADC0 and ADC1 are performed simultaneously, a conflict occurs when the self-diagnosis result is stored in ADEXDR0 register, and the self-diagnosis result of either ADC0 or ADC1 is lost. In addition, the value in the ADEXDR0 register cannot distinguish the data has been converted by which A/D converter.

To avoid this problem, it is recommended to perform self-diagnosis in one of the following methods:

[Recommended operation when self-diagnosis function is used]

- Perform self-diagnosis for each A/D converter one by one.
  - In order to distinguish which A/D converter's self-diagnosis result when reading the data register, please schedule the self-diagnosis operation of each A/D converter to be exclusive.
- Use FIFO function for scan groups that include self-diagnosis channels.
  - By using FIFO, it is possible to distinguish indirectly the A/D conversion result for that scan group was converted by which A/D converter. This mechanism makes it possible to distinguish which A/D converter's self-diagnosis result.

(2) Notes on data format during self-diagnosis

When self-diagnosis is performed, if a data format other than 16-bit length is set, an overflow occurs due to A/D conversion data rounding, and the A/D conversion data error is detected. To perform self-diagnosis, select the 16-bit data format.

36.3.10 Internal Reference Voltage

ADC can perform A/D conversion of Internal Reference Voltage. Internal Reference Voltage outputs a constant voltage that is independent of the power supply voltage (VCC, VSS, AVCC, AVSS, VREFH0 and VREFL0). The monitoring of Internal

1.将自诊断通道分配给其中一个虚拟通道并配置虚拟通道。
2.将已选择自诊断通道的虚拟通道分配给其中一个扫描组。
3.在ADSGDCRn.DIAGVAL[2:0](n=0到8)位中设置自诊断电压，对应于上面2.中分配的扫描组。
4.当分配自诊断通道的扫描组开始扫描并开始自诊断通道的A/D转换时，执行自诊断操作。

表36.9显示了使用自诊断功能时的操作设置。使用自诊断功能时，请按照表36.9中的设置。如果以表36.9所示设置以外的设置执行自诊断操作，则不能保证自诊断结果（AD转换结果）。

Table 36.9 使用自诊断功能时的动作设定及期望值

Self-diagnosis mode	注册设定值				AD转换数据的期望值
	ADSGDCRx	ADCHCRy		ADDOPCRCy	
	DIAGVAL[2:0]	CNVCS[6:0]	AINMD	SIGNSEL	
Self-diagnosis mode 1	100b	0x60	1	1	0x0000 *3
Self-diagnosis mode 2	101b	0x60	1	1	0x8000 *4
Self-diagnosis mode 3	110b	0x60	1	1	0x7FFF *5

Note: x = 0 to 8, y = 0 to 36
注1.预期值是存储在ADEXDR0.DATA[15:0]或ADFIFODRx.DATA[15:0]中的理想AD转换器结果。
注2.AD转换数据是选择16位数据格式(ADDOPCRn.ADPRC[1:0]=00b)时的值。
注3.AD转换的期望值是有符号数据。当AD转换出现正精度误差时，AD转换结果变为0x0001(+1)或更大，而当出现负精度误差时，AD转换结果变为0xFFFF(−1)或更小。
注4.当AD转换出现精度误差时，AD转换结果为大于等于0x8000的值。
注5.当AD转换出现精度误差时，AD转换结果小于等于0x7FFF。

36.3.9.2 自诊断功能注意事项

(1) 执行自诊断的注意事项

存储自诊断结果的数据寄存器（ADEXDR0）由所有AD转换器共享。执行自诊断时，ADEXDR0寄存器被后面的自诊断操作的结果覆盖。如果同时进行ADC0和ADC1的自诊断操作，则在ADEXDR0寄存器中存储自诊断结果时会发生冲突，ADC0或ADC1的自诊断结果会丢失。另外，ADEXDR0寄存器中的值无法区分数据是由哪个A/D转换器转换的。

为避免此问题，建议通过以下方法之一进行自诊断：

[使用自诊断功能时的推荐操作]

●对每个AD转换器逐一进行自诊断。

为了在读取数据寄存器时区分哪个AD转换器的自诊断结果，请将每个AD转换器的自诊断操作安排为独占。

●对包含自诊断通道的扫描组使用FIFO功能。

通过使用FIFO，可以间接区分该扫描组的AD转换结果是由哪个AD转换器转换的。这种机制可以区分哪个AD转换器的自诊断结果。

(2) 自诊断时数据格式的注意事项

执行自诊断时，如果设置了16位长度以外的数据格式，则由于AD转换数据舍入而发生溢出，并检测到AD转换数据错误。要执行自诊断，请选择16位数据格式。

36.3.10 内部参考电压

ADC可以对内部参考电压进行AD转换。内部参考电压输出与电源电压（VCC、VSS、AVCC、AVSS、VREFH0和VREFL0）无关的恒定电压。内部监控

Reference Voltage can be used to detect variations in the analog reference supply voltage (VREFH0 and VREFL0) and abnormalities or faults in the system.

When performing A/D conversion of Internal Reference Voltage, it is required to set the Internal Reference Voltage Monitor Enable Register (ADREFCR) and assign the analog channel of Internal Reference Voltage to any of the virtual channels. Refer to Table 36.4 for the correspondence between Internal Reference Voltage function and the analog channels. For the sampling time when A/D conversion of Internal Reference Voltage is performed, refer to section 46, Electrical Characteristics.

36.3.11 Temperature Sensor

ADC can perform A/D conversion of Temperature Sensor. The chip temperature can be estimated from the A/D conversion result of Temperature Sensor. For more details on Temperature Sensor, refer to section 38, Temperature Sensor (TSN).

When A/D conversion of Temperature Sensor is performed, Temperature Sensor should be configured and the analog channel of Temperature Sensor should be assigned to any of the virtual channels. Refer to Table 36.4 for the correspondence between Temperature Sensor and analog channels. For the sampling time when A/D conversion of Temperature Sensor is performed, refer to section 46, Electrical Characteristics.

36.3.12 D/A Converter

ADC can perform A/D conversion of the voltage that the D/A converter is outputting to the internal module (ACMPHS). When the output of the D/A converter is used for the reference input voltage of High-Speed Analog Comparator (ACMPHS), this function can be used to monitor the output voltage of the D/A converter. For details of the D/A converter function, refer to section 37, 12-Bit D/A Converter (DAC12).

When A/D conversion is performed on the output of D/A converter (DA0 to DA3) (output to ACMPHS), the D/A converter should be configured and the analog channel of the D/A converter should be assigned to one of the virtual channels. For the sampling time when A/D conversion is performed on the D/A converter output voltage, refer to section 46, Electrical Characteristics.

36.3.13 Programmable Gain Amplifier

ADC has built-in Programmable Gain Amplifier (PGA). The PGA amplifies an external analog input signal and outputs it to A/D converter, Channel-dedicated sample-and-hold circuit, and High-Speed Analog Comparator (ACMPHS).

36.3.13.1 Configuration and Operation of PGA

The PGAs are able to select the single-ended input or the pseudo-differential input per unit. Figure 36.9 shows the internal configuration of the PGA in the single-ended input mode and the pseudo differential input mode.

(1) Single-ended input

In single-ended input mode, PGA amplifies the input from PGAIN pin with the specified gain. The gain is set with ADPGACRn.PGAGAIN[3:0] (n = 0 to 3) bits. Settable gains are ×2.000 to ×13.333. Table 36.10 shows the calculation formula of PGA output voltage.

When operating the PGA in single-ended input mode, PGAIN should be connected to the signal source and PGAVSS should be connected to the analog ground (AVSS0). The input voltage to PGAIN must not exceed the range specified in the Electrical Characteristics.

(2) Pseudo-differential input

In pseudo differential input mode, PGA amplifies the difference between PGAIN pin and PGAVSS pin with the specified gain and output the voltage obtained by adding the offset of AVCC×0.5 level. The gain is set by ADPGACRn.PGAGAIN[3:0] (n = 0 to 3) bits and ADPGACRn.PGADG[1:0] (n = 0 to 3) bits. Settable gains are ×1.500, ×2.333, ×4.000, and ×5.667. Set the same gain value to PGAGAIN[3:0] bits and PGADG[1:0] bits. Table 36.10 shows the calculation formula of PGA output voltage.

When operating the PGA in Pseudo Differential Input Mode, PGAIN should be connected to the signal source, and PGAVSS should be connected to the reference ground of the signal source. The inputs to PGAIN and PGAVSS pins must not exceed the range specified in the Electrical Characteristics.

参考电压可用于检测模拟参考电源电压（VREFH0和VREFL0）的变化以及系统中的异常或故障。

对内部参考电压进行A/D转换时，需要设置内部参考电压监视器
启用寄存器(ADREFCR)并将内部参考电压的模拟通道分配给任何虚拟通道。内部参考电压功能与模拟通道的对应关系见表36.4。关于内部参考电压进行AD转换时的采样时间，请参阅第46节，电气特性。

36.3.11 温度感应器

ADC可以对温度传感器进行AD转换。芯片温度可以通过温度传感器的AD转换结果来估算。有关温度传感器的更多详细信息，请参阅第38节，温度传感器(TSN)。

进行温度传感器的AD转换时，应配置温度传感器，并将温度传感器的模拟通道分配给任何虚拟通道。温度传感器与模拟通道的对应关系见表36.4。关于温度传感器进行AD转换时的采样时间，请参阅第46节，电气特性。

36.3.12 D/A Converter

ADC可以对DA转换器输出到内部模块(ACMPHS)的电压进行AD转换。
当DA转换器的输出用作高速模拟比较器(ACMPHS)的参考输入电压时，该功能可用于监控DA转换器的输出电压。有关DA转换器功能的详细信息，请参阅第37节，12位DA转换器(DAC12)。

当对数模转换器（DA0到DA3）的输出（输出到ACMPHS）执行数模转换时，应配置数模转换器，并将数模转换器的模拟通道分配给虚拟通道之一。关于DA转换器输出电压进行AD转换时的采样时间，请参阅第46节，电气特性。

36.3.13 可编程增益放大器

ADC具有内置的可编程增益放大器(PGA)。PGA放大外部模拟输入信号并将其输出到
AD转换器、通道专用采样保持电路和高速模拟比较器(ACMPHS)。

36.3.13.1 PGA的配置和操作

PGA能够为每个单元选择单端输入或伪差分输入。图36.9显示了PGA在单端输入模式和伪差分输入模式下的内部配置。

(1) Single-ended input

在单端输入模式下，PGA以指定的增益放大来自PGAIN引脚的输入。增益设置为
ADPGACRn.PGAGAIN[3:0]（n=0到3）位。可设置的增益为×2.000至×13.333。PGA输出电压的计算公式如表36.10所示。

在单端输入模式下操作PGA时，PGAIN应连接到信号源，PGAVSS应连接到模拟地（AVSS0）。PGAIN的输入电压不得超过电气特性中规定的范围。

(2) Pseudo-differential input

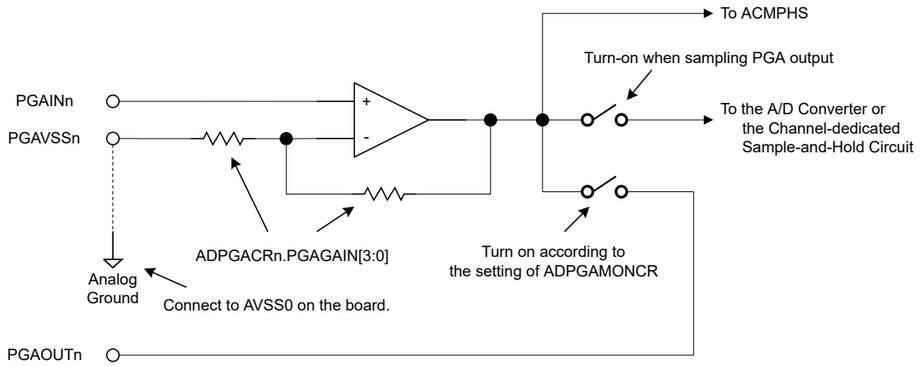
在伪差分输入模式下，PGA将PGAIN引脚和PGAVSS引脚之间的差值以规定的增益放大，并输出加上AVCC×0.5电平的偏移后的电压。增益由ADPGACRn.PGAGAIN[3:0]（n=0到3）位和ADPGACRn.PGADG[1:0]（n=0到3）位设置。可设置的增益为×1.500、×2.333、×4.000和×5.667。将相同的增益值设置为PGAGAIN[3:0]位和PGADG[1:0]位。PGA输出电压的计算公式如表36.10所示。

在伪差分输入模式下操作PGA时，应将PGAIN连接到信号源，并且
PGAVSS应连接到信号源的参考地。PGAIN和PGAVSS引脚的输入不得超过电气特性中指定的范围。

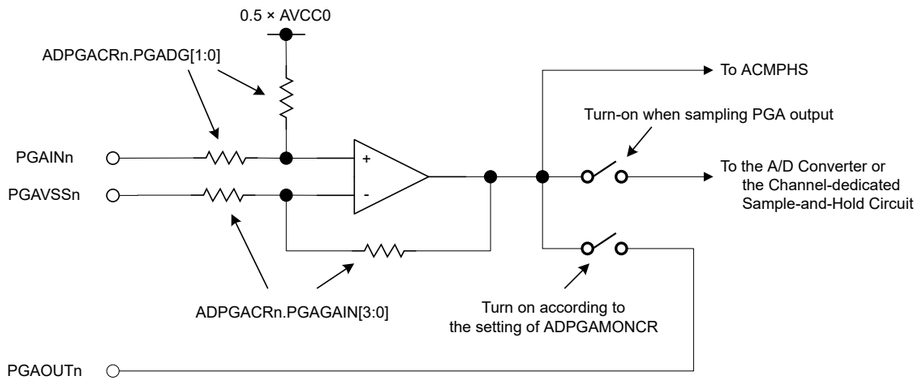
(3) PGA output

The analog signal amplified by PGA can be used with A/D converter, Channel-dedicated sample-and-hold circuit, and High-Speed Analog Comparator. When the PGA output is used by the A/D converter or the Channel-dedicated sample-and-hold circuit, set the analog input channel to which PGAIN pin is assigned to perform A/D conversion.

(1) When PGA is selected as the Single-ended input mode



(2) When PGA is selected as the Pseudo Differential input mode



Note: n = 0 to 3

Figure 36.9 Internal Configuration of PGA

Table 36.10 PGA output voltage

PGA mode	PGA output voltage
Single-ended input	Gain × Vin
Pseudo-differential input	Gain × (Vin – Vs) + AVCC × 0.5

Note: Vin: PGAIN0 to PGAIN3, Vs: PGAVSS0 to PGAVSS3

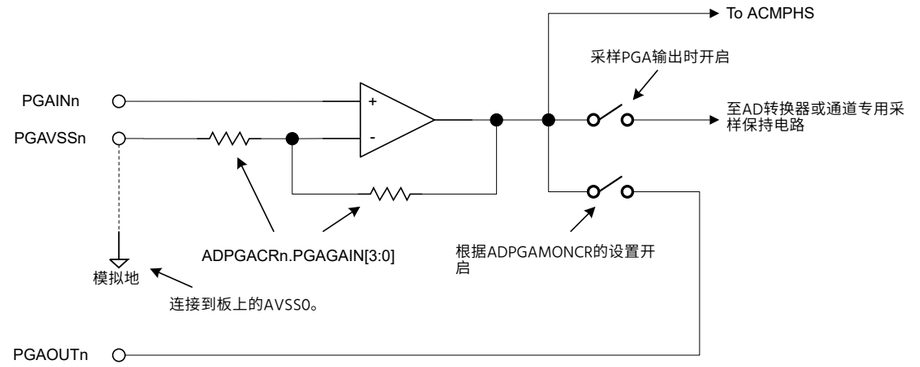
36.3.13.2 PGA operation setting

Table 36.11 shows the combination of the PGA setting and the related functions that can be used.

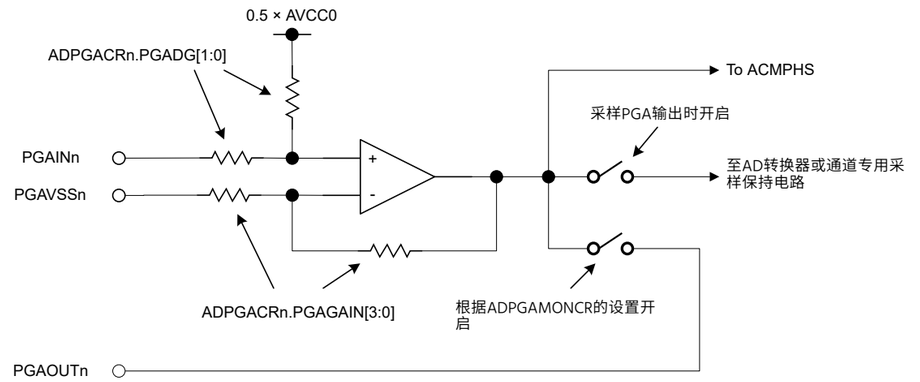
(3) PGA输出

PGA放大后的模拟信号可与A/D转换器、通道专用采样保持电路、High
速度模拟比较器。当PGA输出用于AD转换器或通道专用采样保持电路时，设置PGAIN引脚分配到的模拟输入通道执行AD转换。

(1)WhenPGAisselectedastheSingle-endedinputmode



(2)选择PGA作为伪差分输入模式时



Note: n = 0 to 3

Figure 36.9 PGA的内部配置

Table 36.10 PGA输出电压

PGA模式	PGA输出电压
Single-ended input	增益×Vin
Pseudo-differential input	Gain × (Vin – Vs) + AVCC × 0.5

Note: Vin: PGAIN0 to PGAIN3, Vs: PGAVSS0 to PGAVSS3

36.3.13.2 PGA操作设置

表36.11显示了PGA设置和可以使用的相关功能的组合。

Table 36.11 PGA Settings and Available Related Functions

Use Case	Function				Register Setting						
					PnmPFS	ADPGACRn (n = 0 to 4) *5					
		ACMPHS *1				b27-24	b21-20	b16	b3	b2	b1
	I/O Port	IVCMP3	IVCMP2	ADC	ASEL	PGAGAIN[3:0]	PGADG[1:0]	PGAGEN	PGAENAMP	PGASEL1	PGADEN *3
When using I/O Port	✓	—	—	—	0	0x0	00b	0	0	0	0
When using ACMPHS or ADC (not use PGA) *4	—	—	✓	✓ (ANx)	1	0x0	00b	1	0	0	0
When using PGA Single-ended input	—	✓	✓	✓ (PGA Output)	1	0x0 to 0xE	00b	1	1	1	0
When using PGA Pseudo Differential Input	—	✓	—	✓ (PGA Output)	1	0x1, 0x5, 0x9, 0xB	00b to 11b	1	1	1	1

Note: ✓: Available, —: Not available.
ANx: Analog input channel to which PGAINn or PGAVSSn (n = 0 to 3) is assigned
Note 1. ACMPHS.IVCMP2: When using ANx-input by-passing PGA
ACMPHS.IVCMP3: When PGA are used
Note 2. For details on PnmPFS register settings, refer to section 18, I/O Ports.
Note 3. The value after reset depends on the user-set value of in section 6, Option-Setting Memory.
Note 4. I/O Port and ACMPHS cannot be used at the same time.
I/O Port and ADC cannot be used at the same time.
Note 5. Only the combinations listed in the table can be set to ADPGACRn register.

36.3.13.3 PGA Output Monitor Function

ADC outputs the PGA' internal output to the pin for observation.

To output the PGA's internal output to the pin, ADPGAMONCR register setting and the pin configuration of which PGAOUT function is assigned are required. For more details on the pin configuration, refer to section 18, I/O Ports.

Restrictions on the PGA Output Monitoring Function

The PGA output monitor function (hereinafter referred to as this function) is an auxiliary function for the purpose of program development, debugging, checking operation, and analysis of the MCU, and is not intended to be used in normal operation. When this function is used, the PGA characteristics may deteriorate and unintentional operation may occur due to the effects of load or external noise caused by the terminal output, etc. For these reasons, functions, characteristics, and reliability are not guaranteed when this function is used. When using this function, be sure to give sufficient consideration to the safety of the customer's equipment and system before using it. Also, after the development of your equipment or system is completed, be sure to use the product with this function disabled (no PGA output to the pins).

36.3.13.4 Restrictions on PGA

When using a PGA, observe the following constraints:

(1) Limitations of the analog input path to which PGAIN and PGAVSS are assigned

When PGA is used, the analog input pin assigned to PGAVSS pin cannot be input to A/D conversion or Channel-dedicated sample-and-hold circuit.

Regardless of the PGA is enabled or disabled, if the PGA is set to Pseudo Differential Input Mode, the analog inputs to which PGAIN and PGAVSS are assigned cannot be used by the A/D converter or Channel-dedicated sample-and-hold circuit bypassing the PGA.

(2) Restrictions of the input-voltage range to pins to which PGAIN and PGAVSS are assigned

The inputs to the pins to which PGAIN and PGAVSS are connected must not exceed the range specified in the Electrical Characteristics.

Table 36.11 PGA设置和可用的相关功能

用例	Function				寄存器设置						
					PnmPFS	ADPGACRn (n = 0 to 4) *5					
		ACMPHS *1				b27-24	b21-20	b16	b3	b2	b1
	I/O Port	IVCMP3	IVCMP2	ADC	ASEL	PGAGAIN[3:0]	PGADG[1:0]	PGAGEN	PGAENAMP	PGASEL1	PGADEN *3
使用IO时 Port	✓	—	—	—	0	0x0	00b	0	0	0	0
使用时 ACMPHS或ADC（不使用PGA）*4	—	—	✓	✓ (ANx)	1	0x0	00b	1	0	0	0
使用PGA时 Single-ended input	—	✓	✓	✓ (PGA Output)	1	0x0 to 0xE	00b	1	1	1	0
使用PGA时 伪微分 Input	—	✓	—	✓ (PGA Output)	1	0x1, 0x5, 0x9, 0xB	00b to 11b	1	1	1	1

Note: ：可用，—：不可用。ANx：分配了PGAINn或PGAVSSn（n=0到3）的模拟输入通道
注1.ACMPHS.IVCMP2：使用ANx输入旁路PGA时
ACMPHS.IVCMP3：使用PGA时
注2.有关PnmPFS寄存器设置的详细信息，请参阅第18节，IO端口。
注3.复位后的值取决于第6节选项设置内存中的用户设置值。
注4.IOPort和ACMPHS不能同时使用。
IOPort和ADC不能同时使用。
注5.只有表中列出的组合才能设置到ADPGACRn寄存器。

36.3.13.3 PGA输出监控功能

ADC将PGA的内部输出输出到引脚以供观察。

要将PGA的内部输出输出到引脚，需要ADPGAMONCR寄存器设置和分配PGAOUT功能的引脚配置。有关引脚配置的更多详细信息，请参阅第18节，IO端口。

PGA输出监控功能的限制

PGA输出监控功能（以下简称该功能）是用于单片机的程序开发、调试、检查运行和分析的辅助功能，不打算在正常运行时使用。使用本功能时，由于负载的影响或端子输出引起的外部噪声等的影响，PGA特性可能会劣化，可能会发生误动作。因此，不保证本功能时的功能、特性和可靠性。用过的。使用此功能时，请务必充分考虑客户设备和系统的安全后再使用。此外，在您的设备或系统开发完成后，请务必使用禁用此功能的产品（无PGA输出到引脚）。

36.3.13.4 对PGA的限制

使用PGA时，请注意以下限制：

(1) 分配PGAIN和PGAVSS的模拟输入路径的限制

使用PGA时，分配给PGAVSS引脚的模拟输入引脚不能输入到AD转换或通道专用采样保持电路。

无论PGA是启用还是禁用，如果PGA设置为伪差分输入模式，则分配了PGAIN和PGAVSS的模拟输入不能被AD转换器或绕过PGA的通道专用采样保持电路使用.

(2) 对分配了PGAIN和PGAVSS的引脚的输入电压范围的限制

PGAIN和PGAVSS所连接的引脚的输入不得超过电气规范中规定的范围
Characteristics.

Regardless of whether the PGA is enabled or disabled, when the PGA is configured in single-input mode, do not input a negative voltage to the analog pins to which PGAIN and PGAVSS are assigned.

For details of the voltage that can be applied to the pins, refer to section 46, Electrical Characteristics.

(3) Restrictions on PGA Output Monitor Function

The PGA output monitor function is an auxiliary function for the purpose of program development, debugging, checking operation, and analysis of the MCU, and is not intended to use this function in normal operation. When using this function, the reliability of PGA and its related functions, characteristics, and devices is not guaranteed. For details, refer to section 36.3.13.3. PGA Output Monitor Function.

36.3.14 Channel-Dedicated Sample-and Hold Circuit

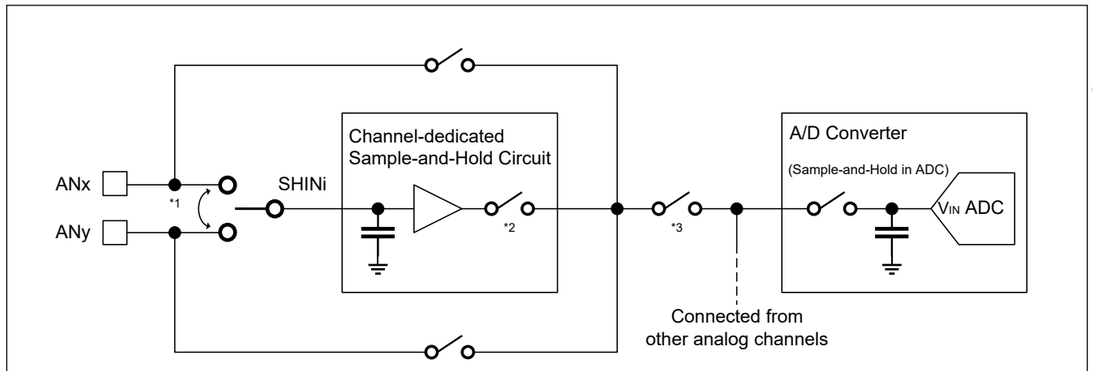
ADC has a built-in Channel-dedicated sample-and-hold circuit. By using multiple Channel-dedicated sample-and-hold circuits, it is possible to sample multiple analog inputs simultaneously. Channel-dedicated sample-and-hold circuit is only available in Single Scan mode.

36.3.14.1 Configuration of Channel-dedicated Sample-and-Hold Circuit

(1) Configuration of Channel-dedicated Sample-and-Hold Circuit without PGA

Figure 36.10 shows the configuration of Channel-dedicated sample-and-hold circuit (SH) and A/D converter to which Programmable Gain Amplifier (PGA) is not connected. For the configuration of the analog channels, refer to Figure 36.2, Figure 36.3, and Table 36.3.

Channel-dedicated sample-and-hold circuit to which PGA is not connected is connected to two analog-input channels. Channel-dedicated sample-and-hold circuit samples and holds only one of the two analog inputs (ANx or ANy) in one scanning operation, and outputs it to the A/D converter.



Note: i: The unit number of Channel-dedicated Sample-and-Hold Circuit
x: Even-numbered analog channel connected to the Channel-dedicated Sample-and-Hold Circuit
y: Odd-numbered analog channel connected to the Channel-dedicated Sample-and-Hold Circuit
Note 1. Turn on when the Channel-dedicated Sample-and-Hold Circuit is enabled and samples ANx or ANy channel.
Note 2. Turn on when the Channel-dedicated Sample-and-Hold Circuit is the holding state.
Note 3. Turn on when the A/D conversion (the sampling state) of ANx, ANy or Channel-dedicated Sample-and-Hold Circuit output.

Figure 36.10 Configuration of Channel-dedicated sample-and-hold circuit (without PGA)

(2) Configuration of Channel-dedicated Sample-and-Hold Circuit with PGA

Figure 36.11 shows the configuration of Channel-dedicated sample-and-hold circuit (SH) and A/D converter to which Programmable Gain Amplifier (PGA) is connected. For the configuration of the analog channels, refer to Figure 36.2, Figure 36.3, and Table 36.3.

无论PGA使能还是禁止，当PGA配置为单输入模式时，不要向分配了PGAIN和PGAVSS的模拟引脚输入负电压。

有关可施加到引脚的电压的详细信息，请参阅第46节，电气特性。

(3) PGA输出监控功能的限制

PGA输出监控功能是用于单片机的程序开发、调试、检查运行和分析的辅助功能，不打算在正常运行时使用该功能。使用此功能时，不保证PGA及其相关功能、特性和器件的可靠性。有关详细信息，请参阅第36.3.13.3节。PGA输出监控功能。

36.3.14 通道专用采样保持电路

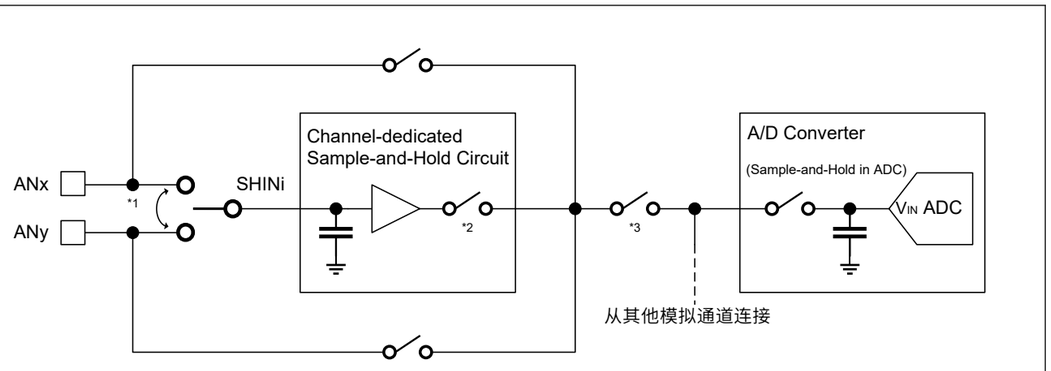
ADC具有内置的通道专用采样保持电路。通过使用多个通道专用的采样保持电路，可以同时采样多个模拟输入。通道专用的采样保持电路仅在单次扫描模式下可用。

36.3.14.1 通道专用采样保持电路的配置

(1) 不带PGA的通道专用采样保持电路的配置

图36.10显示了通道专用采样保持电路(SH)和AD转换器的配置
未连接可编程增益放大器(PGA)。有关模拟通道的配置，请参见图36.2，
图36.3和表36.3。

未连接PGA的通道专用采样保持电路连接到两个模拟输入通道。通道专用采样保持电路在一次扫描操作中仅对两个模拟输入（ANx或ANy）中的一个进行采样和保持，并将其输出到AD转换器。



Note: i：通道专用采样保持电路的单元编号x：连接到通道专用采样保持电路的偶数模拟通道y：连接到通道专用采样和保持电路的奇数模拟通道-保持电路

注1.当通道专用采样保持电路使能并对ANx或ANy通道进行采样时打开。
注2.通道专用采样保持电路处于保持状态时开启。
注3.当ANx、ANy或通道专用采样保持电路输出的AD转换（采样状态）时开启。

Figure 36.10 通道专用采样保持电路的配置（无PGA）

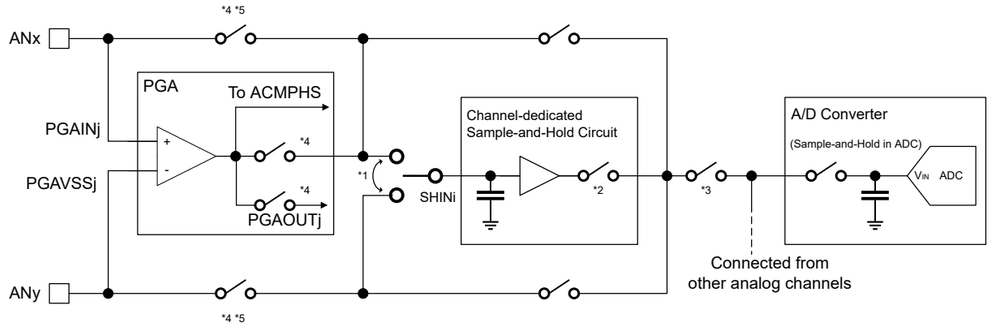
(2) 使用PGA配置通道专用采样保持电路

图36.11显示了通道专用采样保持电路(SH)和连接可编程增益放大器(PGA)的AD转换器的配置。有关模拟通道的配置，请参见图36.2，
图36.3和表36.3。

Channel-dedicated sample-and-hold circuit to which the PGA is connected has two analog paths connected. One path is the output of the PGA or the analog input path from PGAIN that bypassed the PGA, and the other path is the analog input path from PGAVSS that bypassed the PGA.

When PGA is enabled, the analog path of PGAVSS-side cannot be used as an input to Channel-dedicated sample-and-hold circuit and an input to the A/D converter. Only when PGA is disabled and PGA is selected Single-ended input mode, the analog input path of PGAVSS can be used as an input to Channel-dedicated sample-and-hold circuit and an input to the A/D converter.

Channel-dedicated sample-and-hold circuit can sample and hold only one of the two analog inputs (ANx or ANy) in one scanning operation, and output it to the A/D converter.



Note: i: The unit number of Channel-dedicated Sample-and-Hold Circuit
j: The unit number of Programmable Gain Amplifier
x: Even-numbered analog channel connected to the Channel-dedicated Sample-and-Hold Circuit
y: Odd-numbered analog channel connected to the Channel-dedicated Sample-and-Hold Circuit
Note 1. Turn on when the Channel-dedicated Sample-and-Hold Circuit is enabled and samples ANx or ANy channel.
Note 2. Turn on when the Channel-dedicated Sample-and-Hold Circuit is the holding state.
Note 3. Turn on when the A/D conversion (the sampling state) of ANx (PGA bypass or via PGA), ANy (PGA bypass) or Channel-dedicated Sample-and-Hold Circuit output.
Note 4. The turning on/off is depended on the operating setting of the PGA.
Note 5. Turn off whenever the PGA is selected the Pseudo differential input mode.

Figure 36.11 Configuration of Channel-dedicated sample-and-hold circuit (with PGA)

36.3.14.2 Operation of Channel-dedicated Sample-and-Hold Circuit

(1) Basic Operation

The basic operation of Channel-dedicated sample-and-hold circuit is shown in the following and Figure 36.12.

[Operation example]

- A/D converter operation: Single Scan mode (ADC0)
- Channel-dedicated sample-and-hold circuit: SH0 to SH2 are enabled
  - AN000 to AN0005 are subject to A/D conversion using Channel-dedicated sample-and-hold circuit.
- Scan group 0: A/D conversion is performed by assigning a AN000, AN002, AN004, AN020
  - Each analog input is assigned to virtual channels 0 to 3.

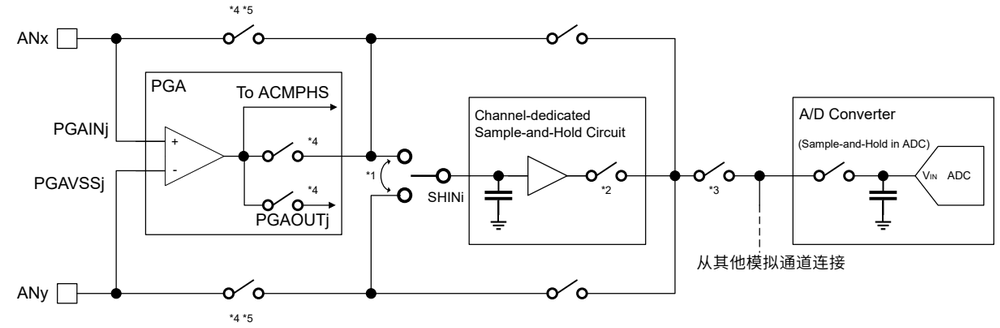
[Operation]

1. The scanning operation of scan group 0 starts when a trigger for scan group 0 is input.
2. Channel-dedicated sample-and-hold circuit (SH0 to SH2) starts sampling the analog inputs (AN000, AN002, AN004) and holds them.
3. A/D conversion is performed on the voltages held by each Channel-dedicated sample-and-hold circuit and on other analog input channels (AN020).

PGA所连接的通道专用采样保持电路连接了两条模拟路径。一条路径是PGA的输出或绕过PGA的PGAIN的模拟输入路径，另一条路径是绕过PGA的PGAVSS的模拟输入路径。

当PGA使能时，PGAVSS侧的模拟路径不能用作通道专用采样保持电路的输入和AD转换器的输入。只有当PGA禁用且PGA选择单端输入模式时，PGAVSS的模拟输入路径才能用作通道专用采样保持电路的输入和AD转换器的输入。

通道专用的采样保持电路可以在一次扫描操作中仅对两个模拟输入（ANx或ANy）中的一个进行采样和保持，并将其输出到AD转换器。



Note: i：通道专用采样保持电路的单元编号j：可编程增益放大器的单元编号x：连接到通道专用采样保持电路的偶数模拟通道y：奇数模拟通道连接到通道专用的采样保持电路

注1.当通道专用采样保持电路使能并对ANx或ANy通道进行采样时打开。
注2.通道专用采样保持电路处于保持状态时开启。
注3.当ANx（PGA旁路或通过PGA）、ANy（PGA旁路）或通道专用采样保持电路输出的AD转换（采样状态）时打开。

注4.开启关闭取决于PGA的操作设置。
注5.当PGA选择伪差分输入模式时关闭。

Figure 36.11 通道专用采样保持电路的配置（带PGA）

36.3.14.2 通道专用采样保持电路的操作

(1) 基本操作

通道专用采样保持电路的基本操作如下和图36.12所示。

[Operation example]

●AD转换器操作：单扫描模式（ADC0）

●通道专用采样保持电路：启用SH0至SH2

AN000至AN0005使用通道专用的采样保持电路进行AD转换。

●扫描组0：通过分配AN000、AN002、AN004、AN020执行AD转换

每个模拟输入都分配给虚拟通道0到3。

[Operation]

1.扫描组0的扫描操作在扫描组0的触发输入时开始。

2.通道专用采样保持电路（SH0至SH2）开始对模拟输入（AN000、AN002、AN004）进行采样并保持它们。

3.对每个通道专用采样保持电路和其他模拟输入通道(AN020)保持的电压进行D转换。

4. When A/D conversion of each channel completes, the A/D conversion result is stored in the corresponding A/D data register n (ADDRn).
5. If Scan End Interrupt in scan group 0 is set to enabled, an Scan End Interrupt occurs.

Note: For analog channels that use Channel-dedicated sample-and-hold circuit, set the virtual channels so that A/D conversion is performed at the beginning of the scan group. For more details, refer to section 36.3.14.3. Restrictions on Channel-dedicated sample-and-hold circuit.

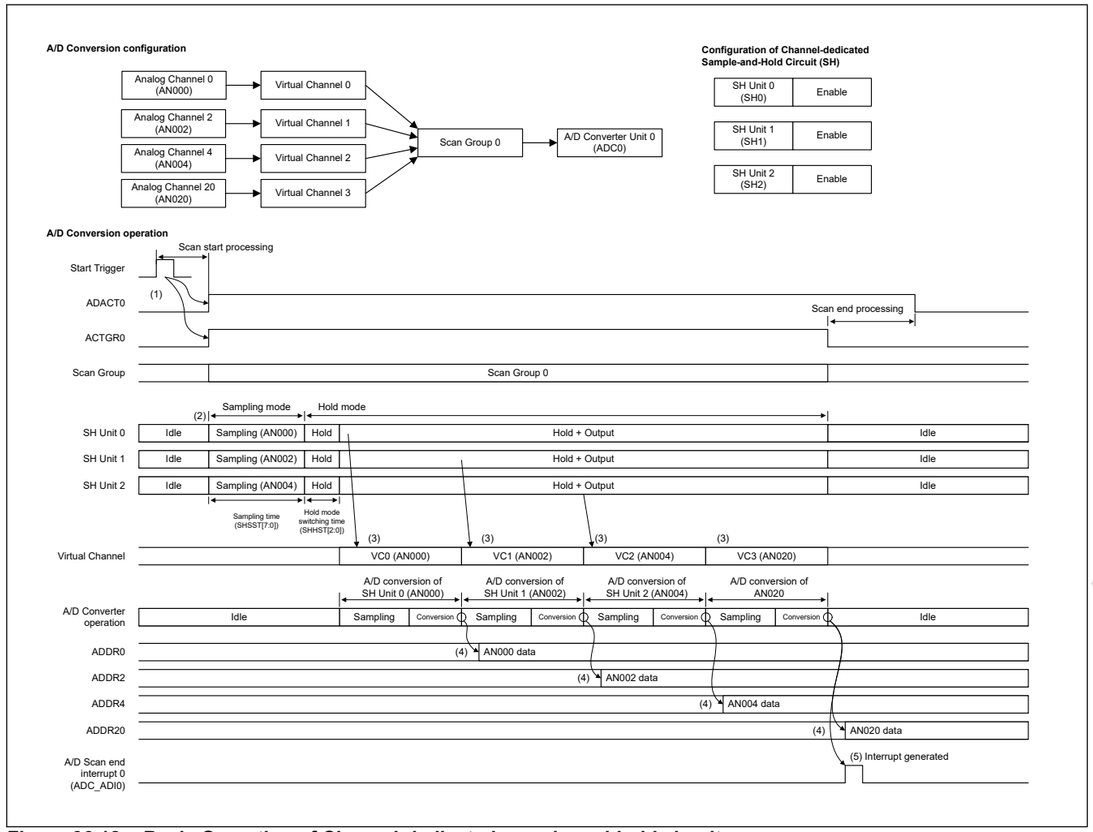


Figure 36.12 Basic Operation of Channel-dedicated sample-and-hold circuit

(2) Operation of the Channel-dedicated Sample-and-Hold Circuit shared with two analog channels

An operation example when A/D conversion is performed on two analog input channels connected to Channel-dedicated sample-and-hold circuit is shown in the following and Figure 36.13.

[Operation example]

- A/D converter operation: Single Scan mode (ADC0)
- Channel-dedicated sample-and-hold circuit: SH0 to SH2 are enabled
  - AN000 to AN0005 are subject to A/D conversion using Channel-dedicated sample-and-hold circuit.
- Scan group 0: Assign AN000, AN002, AN004 (virtual channels use 0 to 2)
- Scan group 1: Assign AN001, AN003, AN005 (virtual channels use 3 to 5)
- After A/D conversion of scan group 0, A/D conversion of scan group 1 is performed.

[Operation]

1. The scanning operation of scan group 0 starts when a trigger for scan group 0 is input.

4、当各通道的AD转换完成后，AD转换结果存入对应的AD数据寄存器n（ADDRn）。

5.如果扫描组0中的扫描结束中断设置为启用，则会发生扫描结束中断。

Note: 对于使用通道专用采样保持电路的模拟通道，设置虚拟通道，以便在扫描组的开头执行AD转换。有关详细信息，请参阅第36.3.14.3节。通道专用采样保持电路的限制。

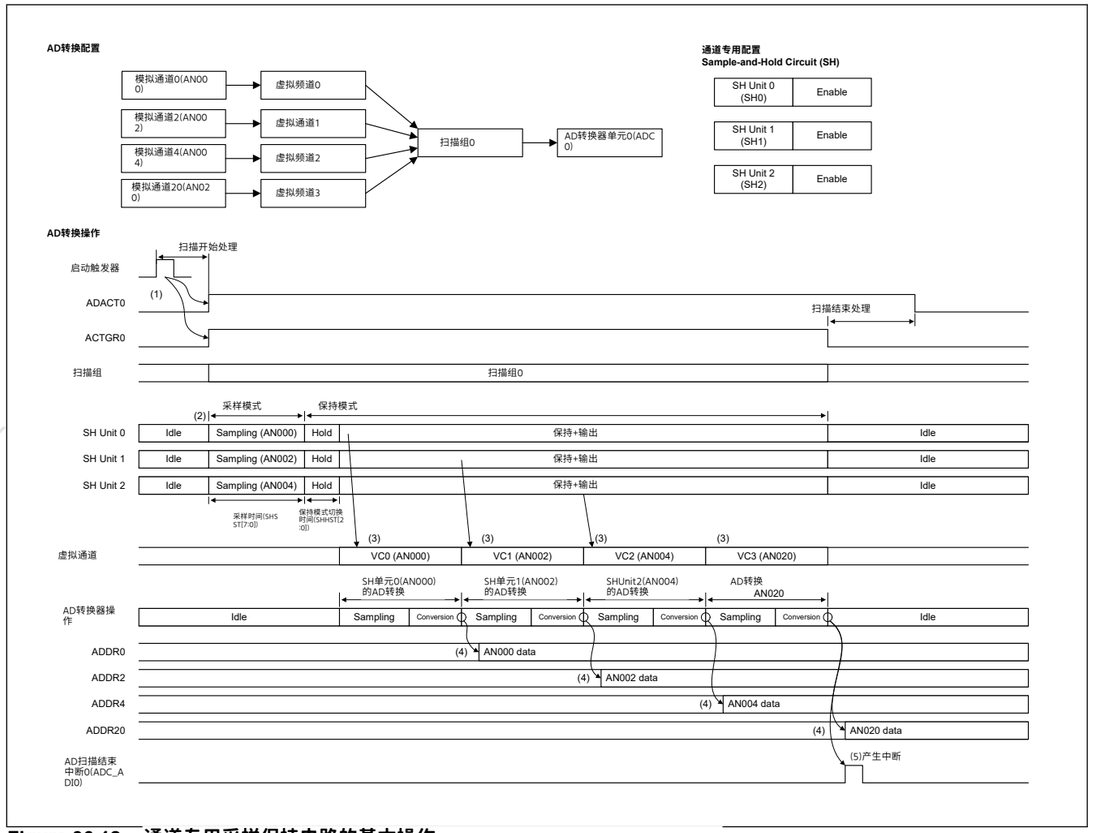


Figure 36.12 通道专用采样保持电路的基本操作

(2) 与两个模拟通道共享的通道专用采样保持电路的操作

下图和图36.13显示了在连接到通道专用采样保持电路的两个模拟输入通道上执行AD转换时的操作示例。

[Operation example]

- ●AD转换器操作：单扫描模式（ADC0）
- ●通道专用采样保持电路：启用SH0至SH2
  - AN000至AN0005使用通道专用的采样保持电路进行AD转换。
- ●扫描组0：分配AN000、AN002、AN004（虚拟通道使用0到2）
- ●扫描组1：分配AN001、AN003、AN005（虚拟通道使用3到5）
- ●扫描组0的AD转换后，进行扫描组1的AD转换。

[Operation]

1.扫描组0的扫描操作在扫描组0的触发输入时开始。

2. Channel-dedicated sample-and-hold circuit (SH0 to SH2) starts sampling the analog inputs (AN000, AN002, AN004) and holds them.
3. A/D conversion is performed on the voltages held by Channel-dedicated sample-and-hold circuit.
4. When A/D conversion of each channel in scan group 0 completes, the A/D conversion result is stored in the corresponding A/D data register n (ADDRn).
5. If Scan End Interrupt in scan group 0 is set to Enabled, an Scan End Interrupt occurs.
6. After scanning of scan group 0 is completed, the scanning operation of scan group 1 starts when a trigger for scan group 1 is input.
7. Channel-dedicated sample-and-hold circuit (SH0 to SH2) starts sampling the analog inputs (AN001, AN003, AN05) and holds them.
8. A/D conversion is performed on the voltages held by Channel-dedicated sample-and-hold circuit.
9. When A/D conversion of each channel in scan group 1 completes, the A/D conversion result is stored in the corresponding A/D data register n (ADDRn).
10. If Scan End Interrupt for scan group 1 is set to Enabled, an Scan End Interrupt occurs.

Note: For analog channels that use Channel-dedicated sample-and-hold circuit, set the virtual channels so that A/D conversion is performed at the beginning of the scan group. For more details, refer to section 36.3.14.3. Restrictions on Channel-dedicated sample-and-hold circuit.

2.通道专用采样保持电路（SH0至SH2）开始对模拟输入（AN000、AN002、AN004）进行采样并保持它们。

3.对通道专用采样保持电路保持的电压进行D转换。

4、扫描组0各通道的A/D转换完成后，A/D转换结果存入对应的A/D数据寄存器n(ADDRn)。

5.如果扫描组0中的扫描结束中断设置为启用，则会发生扫描结束中断。

6.扫描组0的扫描完成后，扫描组1的扫描操作在输入扫描组1的触发时开始。

7.通道专用的采样保持电路（SH0至SH2）开始对模拟输入（AN001、AN003、AN05）进行采样并保持它们。

8.通道专用采样保持电路对保持的电压进行D转换。

9、扫描组1各通道的A/D转换完成后，A/D转换结果存入对应的A/D数据寄存器n(ADDRn)。

10.如果扫描组1的扫描结束中断设置为启用，则会发生扫描结束中断。

Note: 对于使用通道专用采样保持电路的模拟通道，设置虚拟通道，以便在扫描组的开头执行AD转换。有关详细信息，请参阅第36.3.14.3节。通道专用采样保持电路的限制。

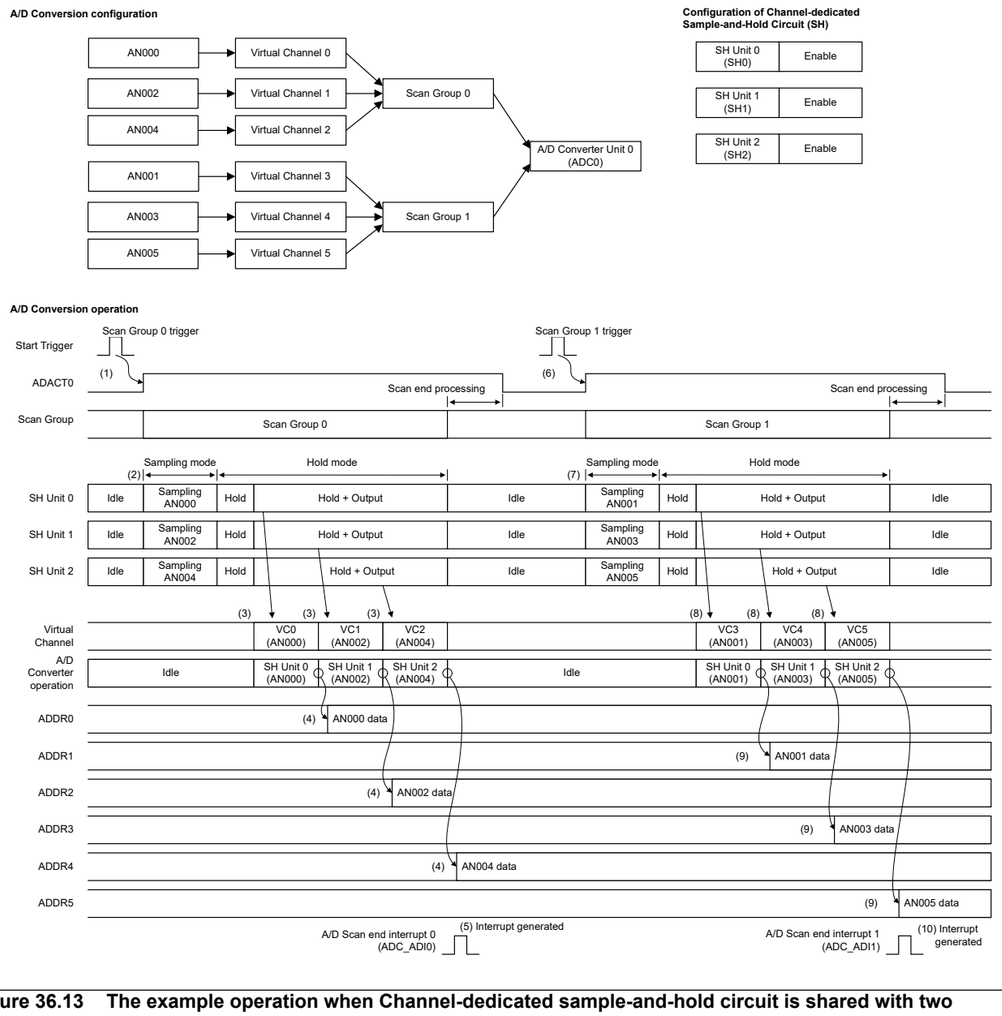


Figure 36.13 The example operation when Channel-dedicated sample-and-hold circuit is shared with two analog channels

36.3.14.3 Restrictions on Channel-dedicated sample-and-hold circuit

When using Channel-dedicated sample-and-hold circuit, observe the following restrictions:

(1) Operating Modes in which channel-dedicated sample-and-hold circuits can be used

Channel-dedicated sample-and-hold circuit is only available in Single Scan mode. Cannot be used in Continuous Scan mode.

(2) Restrictions on Self-Calibration Operation of Channel-dedicated sample-and-hold circuit

Self-Calibration operation is required when Channel-dedicated sample-and-hold circuit is used. For more details on Self-Calibration procedures for Channel-dedicated sample-and-hold circuit and the restrictions on it, refer to section 36.3.6. Self-Calibration.

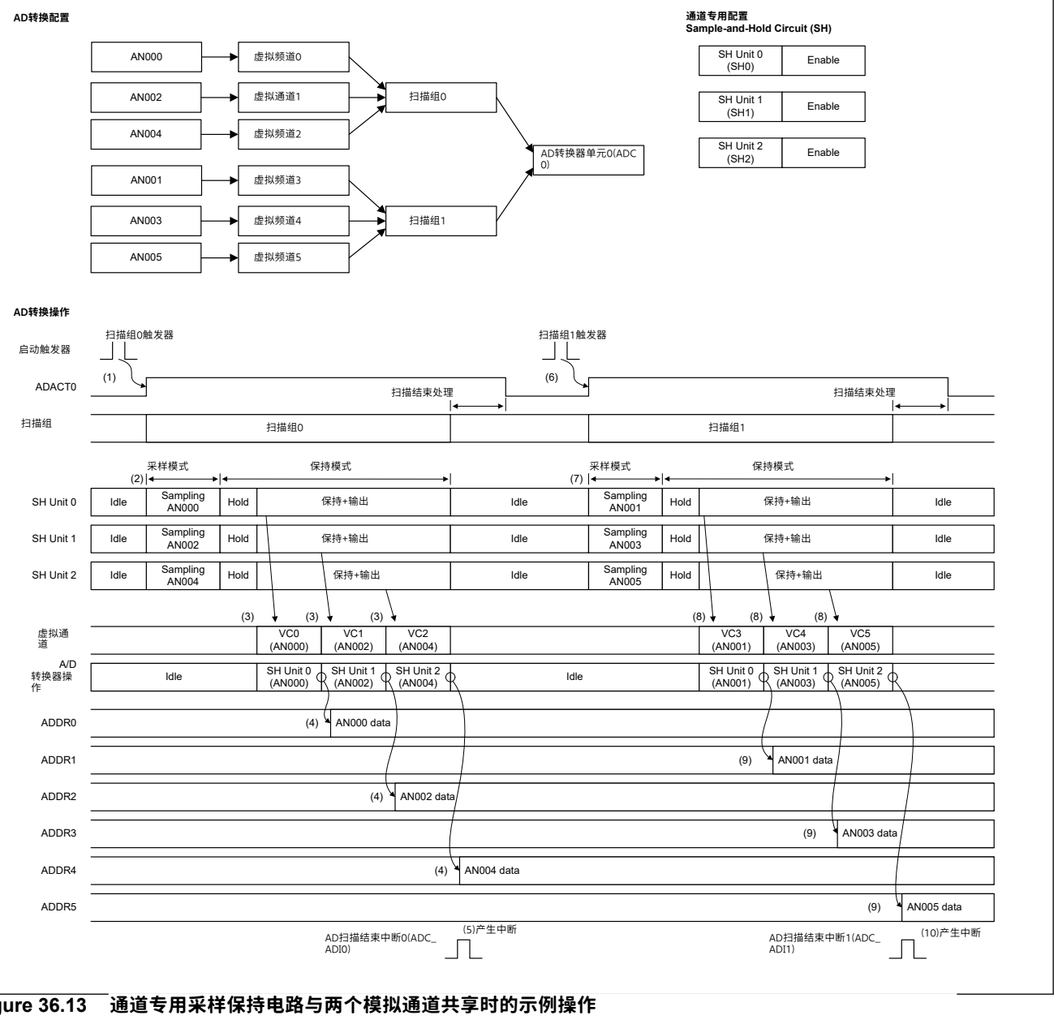


Figure 36.13 通道专用采样保持电路与两个模拟通道共享时的示例操作

36.3.14.3 通道专用采样保持电路的限制

使用通道专用采样保持电路时，请遵守以下限制：

(1) 可以使用通道专用采样保持电路的工作模式

通道专用的采样保持电路仅在单次扫描模式下可用。不能在连续扫描模式下使用。

(2) 通道专用采样保持电路自校准操作的限制

当使用通道专用的采样保持电路时，需要进行自校准操作。有关自我的更多详细信息
通道专用采样保持电路的校准程序及其限制，请参阅第36.3.6节。自己
Calibration.

(3) Restrictions on assigning Virtual Channels and Scan Groups

For analog channels using Channel-dedicated sample-and-hold circuit, assign them to virtual channels so that A/D conversion is performed at the front of the scan group. Specifically, assign an analog channel that uses Channel-dedicated sample-and-hold circuit from the virtual channel that has the smallest virtual channel number among the virtual channels assigned to that scan group. (Assign the analog channels of Channel-dedicated sample-and-hold circuit to the front virtual channels in ascending order of the virtual channel number.)

If this restriction is violated, the operation of Channel-dedicated sample-and-hold circuit and A/D converter is not guaranteed.

(4) Restrictions on analog paths when using Channel-dedicated sample-and-hold circuit

When Channel-dedicated sample-and-hold circuit is enabled, both the even analog channels and the odd-numbered analog channels connected to Channel-dedicated sample-and-hold circuit are performed the A/D conversion with Channel-dedicated sample-and-hold circuit. A/D conversion cannot be performed by bypassing Channel-dedicated sample-and-hold circuit for only one of the analog channels.

Refer also the next restriction related to this restriction.

(5) Prohibition of multiple assignments of Channels Using the Same Channel-dedicated sample-and-hold circuit in the same scan group

It is prohibited to assign more than one virtual channel that uses the same Channel-dedicated sample-and-hold circuit to a single scan group. Specific restrictions are the followings:

[Restrictions]

- The virtual channel whose signal source is selected as the even analog channel connected to Channel-dedicated Sample-and-Hold Circuit and the virtual channel whose signal source is selected as the odd-numbered analog channel must not be assigned to the same scan group.
- It is prohibited to assign the even analog channels or odd-numbered analog channels connected to Channel-dedicated Sample-and-Hold Circuit to multiple virtual channels, and assign them to the same scan group.

Operation is not guaranteed if this restriction is violated.

To avoid this restriction, assign virtual channels that use the same Channel-dedicated Sample-and-Hold Circuit to separate scan groups. This restriction can be avoided by preventing A/D conversion from occurring more than once for the same Channel-dedicated Sample-and-Hold Circuit during one scanning operation.

(6) Restrictions on Group Priority Operation

Channel-dedicated Sample-and-Hold Circuit is not available in Group Priority Operation.

36.3.15 Disconnection Detection Assist Function

Disconnection Detection Assist Function is the function that fixes the charges of the sampling capacitance of the A/D converter to a specified condition prior to starting A/D conversion. This function can be used to detect the wiring disconnection connected to analog input.

Figure 36.14 shows an example operation of A/D conversion when Disconnection Detection Assist Function is used. Figure 36.15 shows an example of the disconnection detection when precharge is selected, and Figure 36.16 shows an example of the disconnection detection when discharge is selected.

(3) 分配虚拟通道和扫描组的限制

对于使用通道专用采样保持电路的模拟通道，将它们分配给虚拟通道，以便在扫描组的前面执行AD转换。具体而言，从分配给该扫描组的虚拟通道中虚拟通道编号最小的虚拟通道分配一个使用通道专用采样保持电路的模拟通道。（将通道专用采样保持电路的模拟通道按虚拟通道编号的升序分配到前面的虚拟通道。）

如果违反此限制，则不能保证通道专用采样保持电路和AD转换器的操作。

(4) 使用通道专用采样保持电路时对模拟路径的限制

当通道专用采样保持电路使能时，连接到通道专用采样保持电路的偶数模拟通道和奇数模拟通道都与通道专用采样保持电路进行模数转换。仅对一个模拟通道绕过通道专用的采样保持电路，无法执行D转换。

另请参阅与此限制相关的下一个限制。

(5) 禁止在同一扫描组中使用同一通道专用采样和保持电路的多个通道分配

禁止将使用同一通道专用采样保持电路的多个虚拟通道分配给单个扫描组。具体限制如下：

[Restrictions]

●信号源选择为偶数模拟通道连接到通道专用采样保持电路的虚拟通道和信号源选择为奇数模拟通道的虚拟通道不能分配到同一个扫描组。

●禁止将连接到通道专用采样保持电路的偶数模拟通道或奇数模拟通道分配给多个虚拟通道，并将它们分配到同一个扫描组中。

如果违反此限制，则无法保证操作。

为避免此限制，请将使用相同通道专用采样保持电路的虚拟通道分配给单独的扫描组。可以通过防止在一次扫描操作期间为同一通道专用采样保持电路多次发生AD转换来避免这种限制。

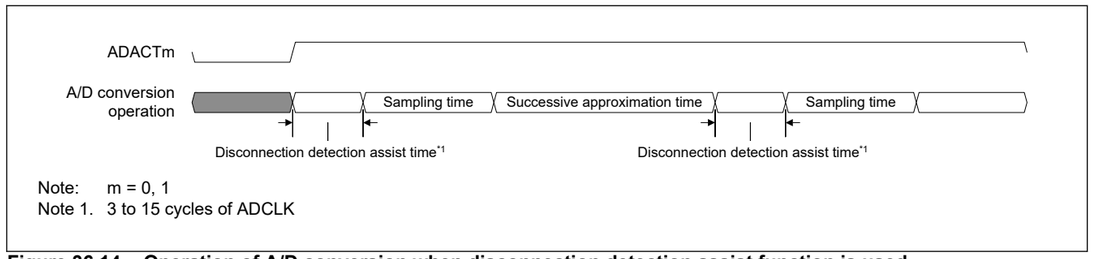
(6) 群组优先操作限制

通道专用的采样保持电路在组优先操作中不可用。

36.3.15 断线检测辅助功能

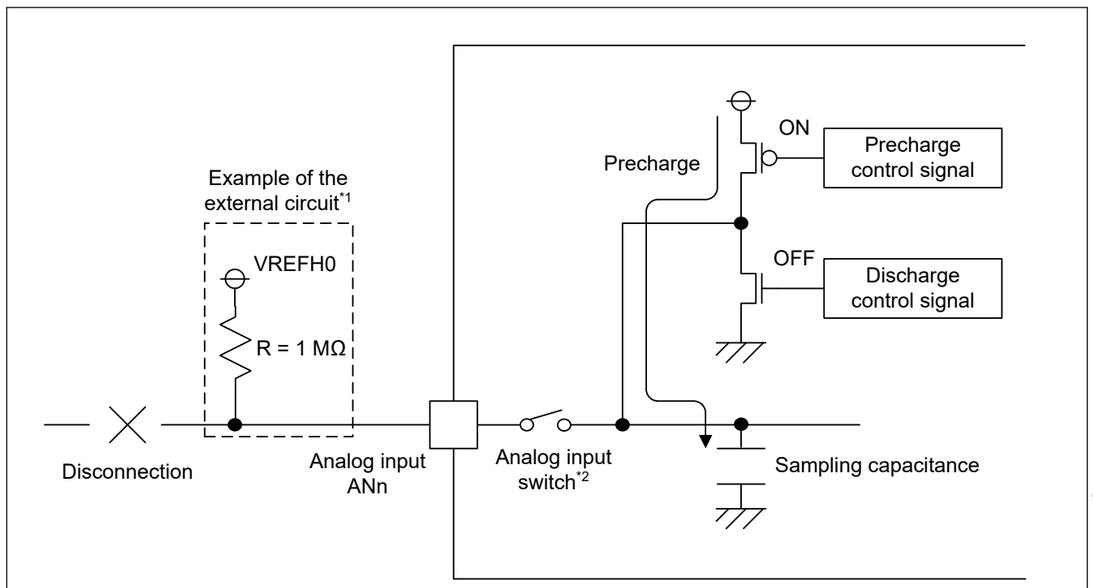
断线检测辅助功能是在开始AD转换之前将AD转换器的采样电容的电荷固定到指定条件的功能。此功能可用于检测连接到模拟输入的接线断开。

图36.14显示了使用断线检测辅助功能时AD转换的示例操作。图36.15显示了选择预充电时的断线检测示例，图36.16显示了选择放电时的断线检测示例。



Note: m = 0, 1
Note 1. 3 to 15 cycles of ADCLK

Figure 36.14 Operation of A/D conversion when disconnection detection assist function is used

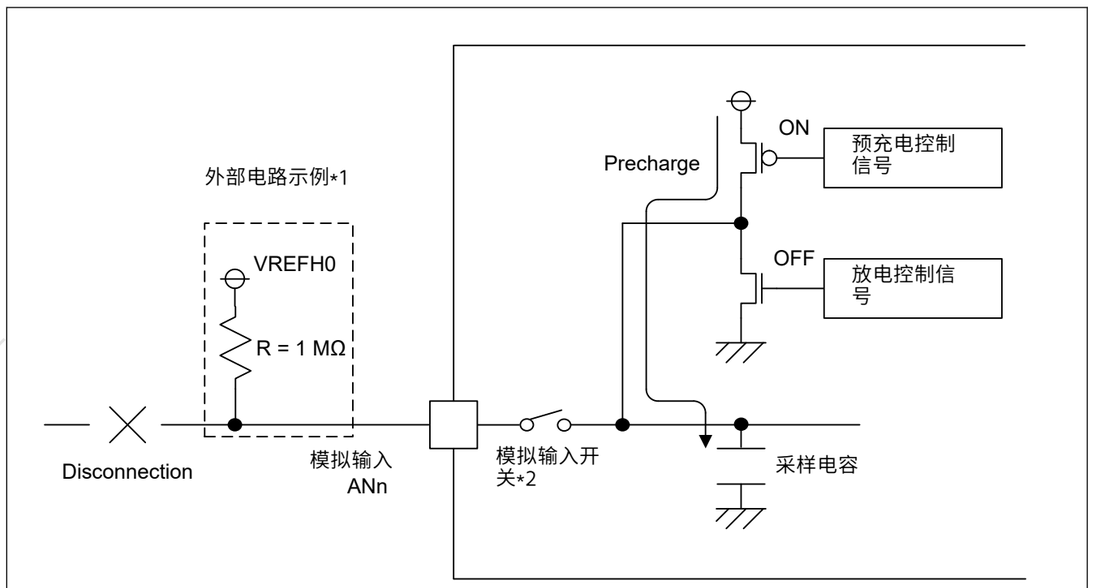


Note 1. The converted result should be used after it is fully evaluated because the result data when disconnection occurs varies depending on the external circuit.
Note 2. Turn off when precharge, and turn on when sampling the Analog input ANn.

Figure 36.15 Example of disconnection detection when precharge is selected

Note: m = 0, 1
注1.ADCLK的3到15个周期

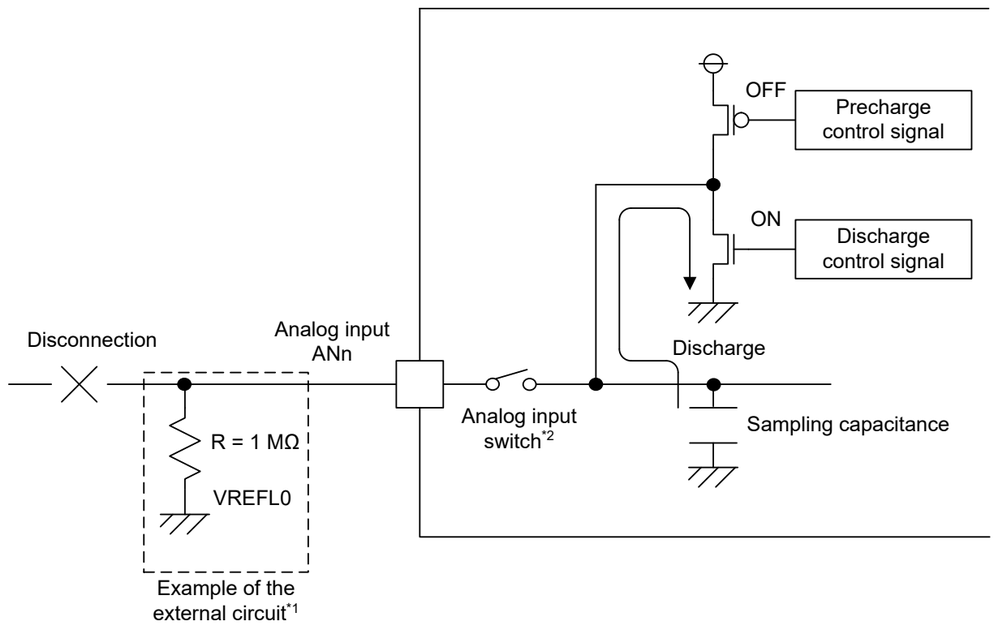
Figure 36.14 使用断线检测辅助功能时的AD转换动作



注1.由于断线时的结果数据因外部电路而异，因此应在充分评估后使用转换结果。

注2.预充电时关闭，对模拟输入ANn进行采样时打开。

Figure 36.15 选择预充电时的断线检测示例



Note 1. The converted result should be used after it is fully evaluated because the result data when disconnection occurs varies depending on the external circuit.
Note 2. Turn off when discharge and turn on when sampling the Analog input ANn.

Figure 36.16 Example of disconnection detection when discharge is selected

36.3.16 Group Priority Operation

Group Priority Operation function is the function that performs the scanning operation (A/D conversion) for a scan group with a higher priority based on the scan group's priority.

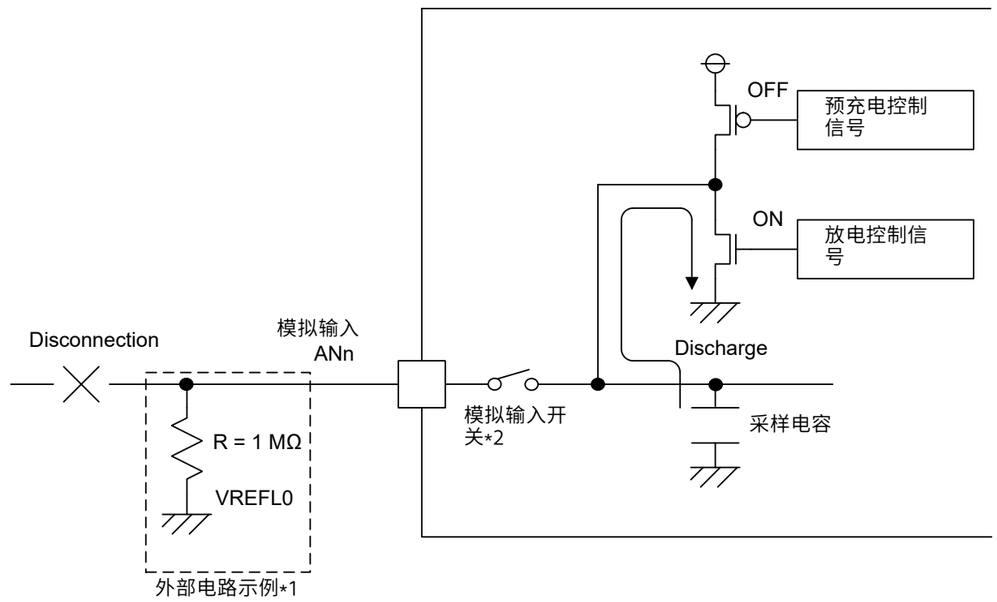
The priority of scan groups is group 0 > group 1 > … > group 8.

Table 36.12 shows the conditions when Group Priority Operation can be used and the corresponding register settings. Set the operation according to Table 36.12.

Table 36.12 Group Priority Operation Usable Conditions and Corresponding Register Settings

Operating Conditions		Group Priority Operation				
Operation mode of A/D Converter	number of scan groups *1	Operation	Setting for ADGSPCR register *2			
			PGSm	RSCNm	LGRRSm	GRPm
Single Scan mode	2 Group	✓	1	1	1	0
	3 Group or more	—	0	0	0	0
Continuous Scan mode	2 Group	✓	1	1	1	1
	3 Group or more	✓	1	1	1	1

Note: ✓: Available, —: Not Available (Prohibited)
m = 0, 1
Note 1. The number of scan groups is the total number of scan groups used for one A/D converter.
Note 2. Settings other than the specified value are prohibited.



注1.由于断线时的结果数据因外部电路而异，因此应在充分评估后使用转换结果。

注2.放电时关闭，对模拟输入ANn进行采样时打开。

Figure 36.16 选择放电时的断线检测示例

36.3.16 集团优先运营

GroupPriorityOperation功能是根据扫描组的优先级，对优先级高的扫描组执行扫描操作（AD转换）的功能。

扫描组的优先级为组0>组1>…>组8。

表36.12显示了可以使用组优先操作的条件和相应的寄存器设置。根据表36.12设置操作。

Table 36.12 组优先操作的可用条件和相应的寄存器设置

运行条件		集团优先运营				
AD的操作模式 Converter	扫描组数*1	Operation	ADGSPCR寄存器的设置*2			
			PGSm	RSCNm	LGRRSm	GRPm
单次扫描模式	2 Group	✓	1	1	1	0
	3组以上	—	0	0	0	0
连续扫描模式	2 Group	✓	1	1	1	1
	3组以上	✓	1	1	1	1

Note: :可用 —:不可用(禁止)m=0 1

注1.扫描组数是用于1个AD转换器的扫描组总数。
注2.禁止指定值以外的设置。

36.3.16.1 Group Priority Operation in Single Scan mode

In Group Priority Operation in Single Scan mode, the single scanning operation is performed for a scan group according to the scan group's priority.

If an A/D conversion start trigger for the high priority group is input during a scanning operation of the low priority group, the scanning operation of the low priority group is interrupted, and the scanning operation of the high priority group is started. After the scanning operation of the high priority group is completed, the scanning operation of the low priority group is resumed.

When an A/D conversion start trigger of the low priority group during a scanning operation of the high priority group is input, the scanning operation of the low priority group is performed after the scanning operation of the high priority group is completed.

Example of the Group Priority Operation in Single Scan mode

Table 36.13 and Figure 36.17 show the example of Group Priority Operation in Single Scan mode when analog channel 0 (AN000) is assigned to scan group 0 (high priority) and analog channel 1 to 3 (AN001 to AN003) are assigned to scan group 1 (low priority).

Table 36.13 Example of the Group Priority Operation in Single Scan mode (2 Groups)

Step	Operation
1	The scanning operation of scan group 1 starts when a trigger for scan group 1 is input.
2	When A/D conversion of each channel in scan group 1 completes, the A/D conversion result is stored in the corresponding A/D data register n (ADDRn).
3	If a trigger for scan group 0 is input during A/D conversion for scan group 1, the scanning operation of scan group 1 is suspended and the scanning operation of scan group 0 is started. *1
4	When A/D conversion of each channel in scan group 0 completes, the A/D conversion result is stored in the corresponding A/D data register n (ADDRn).
5	If Scan End Interrupt in scan group 0 is set to enabled, an Scan End Interrupt occurs.
6	The scanning operation of scan group 1 is resumed after scanning of scan group 0 is completed. The scanning operation is resumed from the A/D conversion incomplete channel. *1
7	When A/D conversion of each channel in scan group 1 completes, the A/D conversion result is stored in the corresponding A/D data register n (ADDRn).
8	If Scan End Interrupt for scan group 1 is set to enable, an Scan End Interrupt occurs.
9	When all scanning operations are completed, ADSR.ADACTm (m = 0, 1) bits are cleared and the A/D converter enters the standby status.

Note 1. The timing of interruption and restart of scanning operation depends on the operating conditions. For more details, refer to section 36.3.16.3. Restrictions on Group Priority Operation.

36.3.16.1 单次扫描模式下的组优先操作

在单次扫描模式下的组优先操作中，根据扫描组的优先级对一个扫描组执行单次扫描操作。

如果在低优先级组的扫描操作期间输入高优先级组的AD转换开始触发，则低优先级组的扫描操作被中断，并且高优先级组的扫描操作开始。高优先级组的扫描操作完成后，重新开始低优先级组的扫描操作。

当在高优先级组的扫描操作期间输入低优先级组的AD转换开始触发时，在高优先级组的扫描操作完成之后执行低优先级组的扫描操作。

单次扫描模式下的组优先操作示例

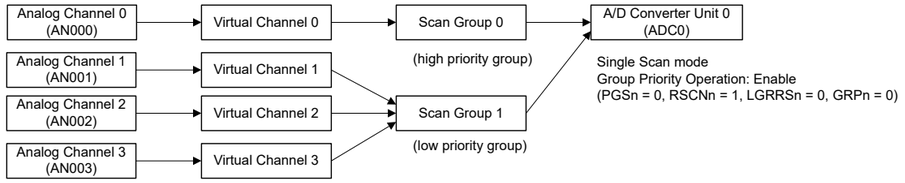
表36.13和图36.17显示了当模拟通道0(AN000)分配给扫描组0（高优先级）并且模拟通道1到3（AN001到AN003）分配给扫描组1时，单次扫描模式下的组优先级操作示例（低优先级）。

Table 36.13 单次扫描模式下的组优先操作示例（2组）

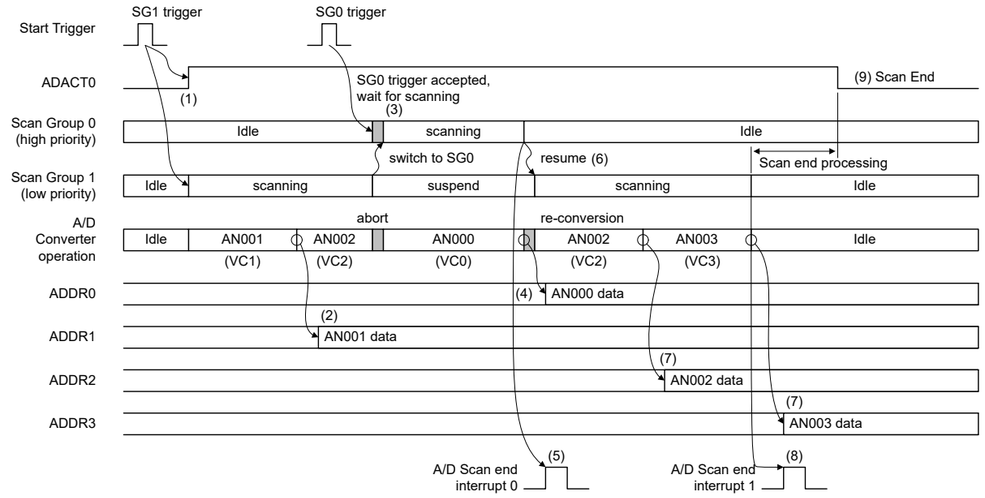
Step	Operation
1	当输入扫描组1的触发器时，扫描组1的扫描操作开始。
2	当扫描组1中各通道的A/D转换完成后，A/D转换结果存入对应的A/D数据寄存器n(ADDRn)。
3	如果在扫描组1的AD转换期间输入了扫描组0的触发信号，则扫描组1的扫描操作暂停，扫描组0的扫描操作开始。*1
4	当扫描组0中各通道的AD转换完成后，AD转换结果存入对应的AD数据寄存器n(ADDRn)。
5	如果扫描组0中的扫描结束中断设置为启用，则会发生扫描结束中断。
6	扫描组0的扫描完成后，扫描组1的扫描操作将恢复。扫描操作从AD转换未完成通道重新开始。*1
7	当扫描组1中各通道的A/D转换完成后，A/D转换结果存入对应的A/D数据寄存器n(ADDRn)。
8	如果扫描组1的扫描结束中断设置为启用，则会发生扫描结束中断。
9	当所有扫描操作完成后，ADSR.ADACTm(m=0 1)位被清零，AD转换器进入待机状态。

注1.扫描操作的中断和重新启动时间取决于操作条件。有关详细信息，请参阅第36.3.16.3节。限制组优先操作。

A/D Conversion configuration



A/D Conversion operation



Note: SG: Scan Group VC: Virtual channel

Figure 36.17 Example of Group Priority Operation in Single Scan mode (2 Groups)

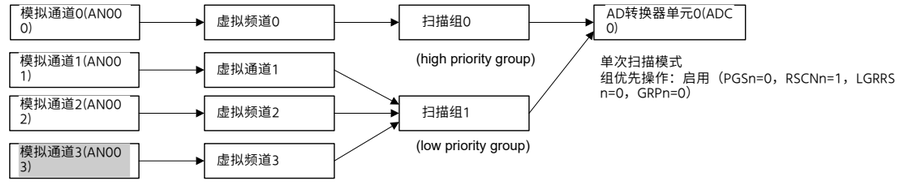
36.3.16.2 Group Priority Operation in Continuous Scan mode

In Group Priority Operation in Continuous Scan mode, the continuous scanning operation is performed for the scan group (continuous-scan group) in which scanning operation was first started. If an A/D conversion start trigger of another scan group (interrupt-scan group) is input during the continuous scanning operation of the continuous-scan group, the following operations are performed according to the priority of the interrupt-scan group.

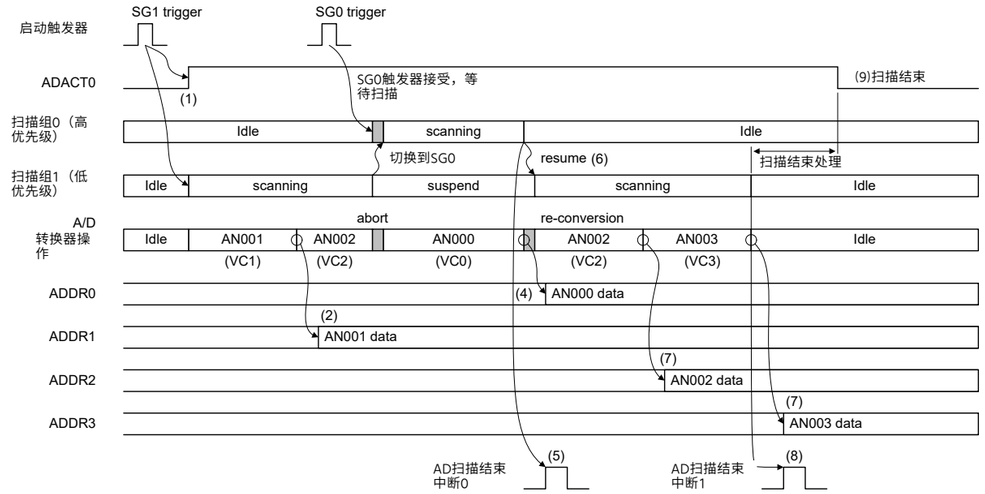
1. Priority: When Interrupt-scan group (high) > Continuous-scan group (low)
   - The scanning operation of the continuous-scan group is interrupted, and the single scanning operation of the interrupt-scan group is started.
   - The continuous scanning operation of the continuous-scan group is restarted after the single scanning operation of the interrupt-scan group is completed.
2. Priority: When Continuous-scan group (high) > Interrupt-scan group (low)
   - This operation is prohibited. Operation is not guaranteed.

   In case 1. above, if an A/D conversion start trigger for another scan group (interrupt-scan group B) is input during the single scanning operation of the interrupt-scan group (interrupt-scan group A), the following operation is performed according to the priority of interrupt-scan group B.
3. Priority: When Interrupt-scan group B (high) > Interrupt-scan group A (middle) > Continuous-scan group (low)

AD转换配置



AD转换操作



Note: SG：扫描组VC：虚拟通道

Figure 36.17 单次扫描模式下的组优先操作示例（2组）

36.3.16.2 连续扫描模式下的组优先操作

在连续扫描模式下的组优先操作中，对首先开始扫描操作的扫描组（连续扫描组）执行连续扫描操作。如果在连续扫描组的连续扫描操作期间输入另一个扫描组（中断扫描组）的AD转换开始触发，则根据中断扫描组的优先级执行以下操作。

1.优先级：当中断扫描组（高）>连续扫描组（低）

- ●连续扫描组的扫描操作被中断，中断扫描组的单次扫描操作开始。
- ●连续扫描组的连续扫描操作在中断扫描组的单次扫描操作完成后重新开始。

2.优先级：当连续扫描组（高）>中断扫描组（低）

- ●禁止该操作。不保证操作。

在上述情况1.中，如果在中断扫描组（中断扫描组A）的单次扫描操作期间输入另一个扫描组（中断扫描组B）的AD转换开始触发，则根据以下操作执行以下操作中断扫描组B的优先级。

3.优先级：当中断扫描组B（高）>中断扫描组A（中）>连续扫描组（低）

- The single scanning operation of interrupt-scan group A is suspended, and the single scanning operation of interrupt-scan group B is started.
- After the single scanning operation of interrupt-scan group B is completed, the single scanning operation of interrupt-scan group A is resumed.
- After the scanning operation of interrupt-scan group A is completed, the continuous scanning operation of the continuous-scan group is resumed.

4. Priority: When interrupt-scan group A (high) > interrupt-scan group B (medium) > continuous-scan group (low)
   - After the single scanning operation of interrupt-scan group A is completed, the single scanning operation of interrupt-scan group B is started.
   - After the single scanning operation of interrupt-scan group B is completed, the continuous scanning operation of the continuous-scan group is resumed.
5. Priority: When interrupt-scan group A (high) > continuous-scan group (medium) > interrupt-scan group (low)
   - This operation is prohibited. Operation is not guaranteed.

Example operations are shown in the followings:

(1) Example of Two-group Priority Operation in Continuous Scan mode

Table 36.14 and Figure 36.18 show the example of Group Priority Operation in Continuous Scan mode when analog channel 0 (AN000) is assigned to scan group 0 (high-priority group) and analog channel 1 to 3 (AN001 to AN003) is assigned to scan group 1 (low-priority group).

Table 36.14 Example of the Group Priority Operation in Continuous Scan mode (2 Groups)

Step	Operation
1	The continuous scanning operation of scan group 1 (low priority group) is started by the trigger input of scan group 1.
2	When A/D conversion of each channel in scan group 1 completes, the A/D conversion result is stored in the corresponding A/D data register n (ADDRn).
3	If a trigger for scan group 0 is input during A/D conversion for scan group 1, the scanning operation of scan group 1 is suspended and scanning operation of scan group 0 is started. *1
4	When A/D conversion of each channel in scan group 0 completes, the A/D conversion result is stored in the corresponding A/D data register n (ADDRn).
5	If Scan End Interrupt in scan group 0 is set to enabled, an Scan End Interrupt occurs.
6	The scanning operation of scan group 1 is resumed after scanning of scan group 0 is completed. The scanning operation is resumed from the A/D conversion incomplete channel. *1
7	When A/D conversion of each channel in scan group 1 completes, the A/D conversion result is stored in the corresponding A/D data register n (ADDRn).
8	If Scan End Interrupt for scan group 1 is set to enabled, an Scan End Interrupt occurs.
9	Scan group 1 continues the continuous scanning operation. *2

Note 1. The timing of interruption and restart of scanning operation depends on the operating conditions. For more details, refer to section 36.3.16.3. Restrictions on Group Priority Operation.
Note 2. To stop the continuous scanning operation, follow the procedures described in section 36.5.4. Force stops the A/D conversion operation.

●中断扫描组A的单次扫描操作暂停，开始中断扫描组B的单次扫描操作。

●中断扫描组B的单次扫描操作完成后，恢复中断扫描组A的单次扫描操作。

●中断扫描组A的扫描操作完成后，恢复连续扫描组的连续扫描操作。

4.优先级：当中断扫描组A（高）>中断扫描组B（中）>连续扫描组（低）

●中断扫描组A的单次扫描操作完成后，开始中断扫描组B的单次扫描操作。

●中断扫描组B的单次扫描操作完成后，恢复连续扫描组的连续扫描操作。

5.优先级：当中断扫描组A（高）>连续扫描组（中）>中断扫描组（低）

●禁止该操作。不保证操作。

示例操作如下所示：

(1) 连续扫描模式下的两组优先操作示例

表36.14和图36.18显示了连续扫描模式下的组优先级操作示例，其中模拟通道0(AN000)分配给扫描组0（高优先级组），模拟通道1到3（AN001到AN003）分配给扫描第1组（低优先级组）。

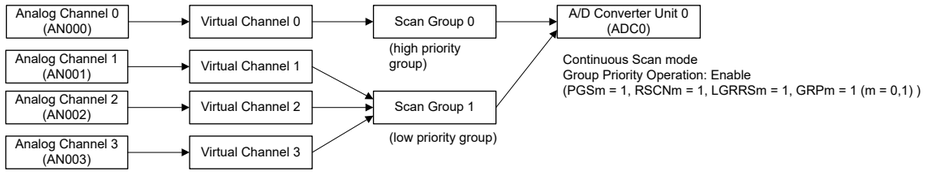
Table 36.14 连续扫描模式下的组优先操作示例（2组）

Step	Operation
1	扫描组1（低优先级组）的连续扫描操作由扫描组1的触发输入开始。
2	当扫描组1中各通道的A/D转换完成后，A/D转换结果存入对应的A/D数据寄存器n(ADDRn)。
3	如果在扫描组1的AD转换期间输入了扫描组0的触发信号，则扫描组1的扫描操作暂停，扫描组0的扫描操作开始。*1
4	当扫描组0中各通道的AD转换完成后，AD转换结果存入对应的AD数据寄存器n(ADDRn)。
5	如果扫描组0中的扫描结束中断设置为启用，则会发生扫描结束中断。
6	扫描组0的扫描完成后，扫描组1的扫描操作将恢复。扫描操作从AD转换未完成通道重新开始。*1
7	当扫描组1中各通道的A/D转换完成后，A/D转换结果存入对应的A/D数据寄存器n(ADDRn)。
8	如果扫描组1的扫描结束中断设置为启用，则会发生扫描结束中断。
9	扫描组1继续连续扫描操作。*2

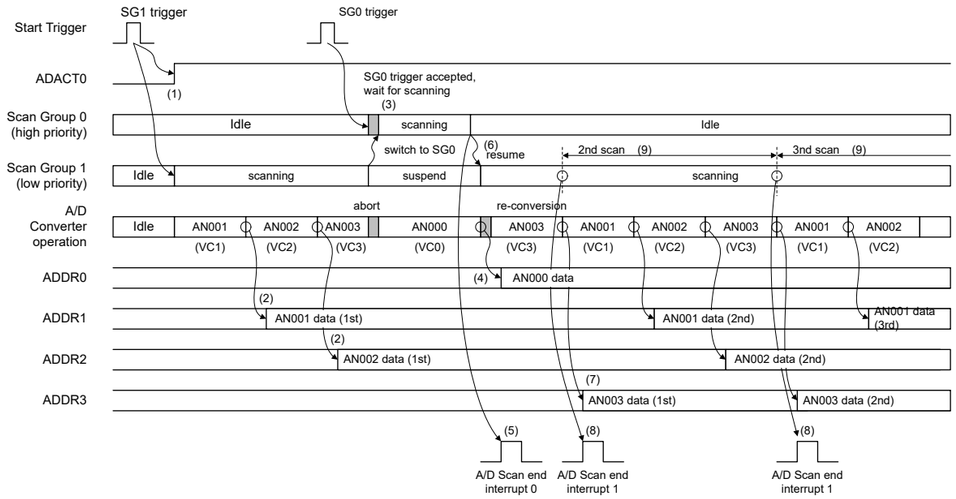
注1.扫描操作的中断和重新启动时间取决于操作条件。有关详细信息，请参阅第36.3.16.3节。限制组优先操作。

注2.要停止连续扫描操作，请按照第36.5.4节中所述的步骤进行操作。强制停止AD转换操作。

A/D Conversion configuration



A/D Conversion operation



Note: SG: Scan Group VC: Virtual channel

Figure 36.18 Example of Group Priority Operation (Continuous Scan mode) (2 groups)

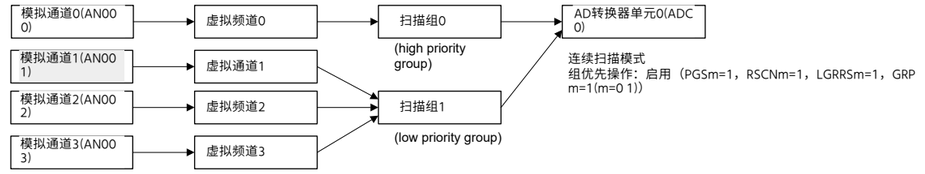
(2) Example of Three-Groups Priority Operation in Continuous Scan mode

Table 36.15 and Figure 36.19 show the example of Group Priority Operation when analog channel 0 (AN000) is assigned to scan group 0 (high priority), analog channels 1 and 2 (AN001 and AN002) are assigned to scan group 1 (middle priority), and analog channel 3 to 5 (AN003 to AN005) are assigned to scan group 2 (low priority).

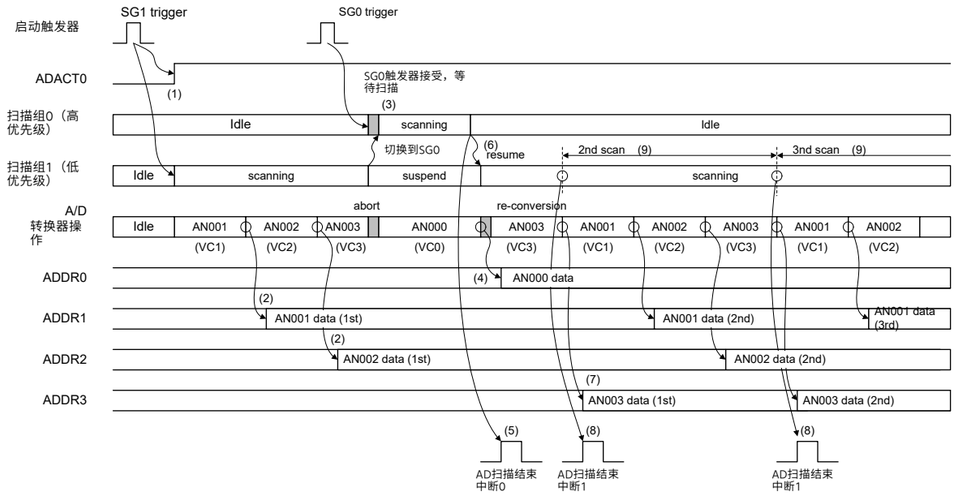
Table 36.15 Example of the Group Priority Operation in Continuous Scan mode (3 Groups) (1 of 2)

Step	Operation
1	The continuous scanning operation of scan group 2 is started by the trigger input of scan group 2.
2	When A/D conversion of each channel in scan group 2 completes, the A/D conversion result is stored in the corresponding A/D data register n (ADDRn).
3	If a trigger for scan group 1 is input during A/D conversion on scan group 2, the scanning operation of scan group 2 is suspended and the scanning operation of scan group 1 is started. *1
4	When A/D conversion of each channel in scan group 1 completes, the A/D conversion result is stored in the corresponding A/D data register n (ADDRn).
5	If a trigger for scan group 0 is input during A/D conversion for scan group 1, the scanning operation of scan group 1 is suspended and the scanning operation of scan group 0 is started. *1
6	When A/D conversion of each channel in scan group 0 completes, the A/D conversion result is stored in the corresponding A/D data register n (ADDRn).
7	If Scan End Interrupt in scan group 0 is set to enabled, an Scan End Interrupt occurs.

AD转换配置



AD转换操作



Note: SG：扫描组VC：虚拟通道

Figure 36.18 组优先操作示例（连续扫描模式）（2组）

(2) 连续扫描模式下的三组优先操作示例

表36.15和图36.19显示了当模拟通道0(AN000)分配给扫描组0（高优先级），模拟通道1和2（AN001和AN002）分配给扫描组1（中优先级）时的组优先级操作示例 模拟通道3至5（AN003至AN005）分配给扫描组2（低优先级）。

Table 36.15 连续扫描模式下的组优先操作示例（3组）（1of2）

Step	Operation
1	扫描组2的连续扫描操作由扫描组2的触发输入启动。
2	当扫描组2中每个通道的AD转换完成后，AD转换结果将存储在相应的AD数据寄存器n(ADDRn)中。
3	如果在扫描组2的AD转换期间输入了扫描组1的触发信号，则扫描组2的扫描操作暂停，扫描组1的扫描操作开始。*1
4	当扫描组1中各通道的A/D转换完成后，A/D转换结果存入对应的A/D数据寄存器n(ADDRn)。
5	如果在扫描组1的AD转换期间输入了扫描组0的触发信号，则扫描组1的扫描操作暂停，扫描组0的扫描操作开始。*1
6	当扫描组0中各通道的AD转换完成后，AD转换结果存入对应的AD数据寄存器n(ADDRn)。
7	如果扫描组0中的扫描结束中断设置为启用，则会发生扫描结束中断。

Table 36.15 Example of the Group Priority Operation in Continuous Scan mode (3 Groups) (2 of 2)

Step	Operation
8	The scanning operation of scan group 1 is resumed after scanning of scan group 0 is completed. The scanning operation is restarted from the A/D conversion incomplete channel. *1
9	When A/D conversion of each channel in scan group 1 completes, the A/D conversion result is stored in the corresponding A/D data register n (ADDRn).
10	If Scan End Interrupt for scan group 1 is set to enabled, an Scan End Interrupt occurs.
11	Scan group 2 is resumed after scanning of scan group 1 is completed. The scanning operation is resumed from the A/D conversion incomplete channel. *1
12	When A/D conversion of each channel in scan group 2 completes, the A/D conversion result is stored in the corresponding A/D data register n (ADDRn).
13	If Scan End Interrupt in scan group 2 is set to enabled, an Scan End Interrupt occurs.
14	Scan group 1 continues the continuous scanning operation. *2

Note 1. The timing of interruption and restart of scanning operation depends on the operating conditions. For more details, refer to section 36.3.16.3. Restrictions on Group Priority Operation.

Note 2. To stop the continuous scanning operation, follow the procedures described in section 36.5.4. Force stops the A/D conversion operation.

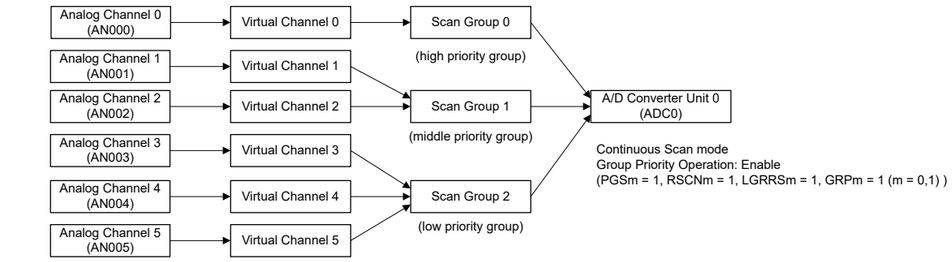
Table 36.15 连续扫描模式下的组优先操作示例（3组）（2of2）

Step	Operation
8	扫描组0的扫描完成后，扫描组1的扫描操作将恢复。扫描操作从AD转换未完成通道重新开始。*1
9	当扫描组1中各通道的A/D转换完成后，A/D转换结果存入对应的A/D数据寄存器n(ADDRn)。
10	如果扫描组1的扫描结束中断设置为启用，则会发生扫描结束中断。
11	扫描组1扫描完成后，扫描组2恢复。扫描操作从AD转换未完成通道重新开始。*1
12	当扫描组2中每个通道的AD转换完成后，AD转换结果将存储在相应的AD数据寄存器n(ADDRn)中。
13	如果扫描组2中的扫描结束中断设置为启用，则会发生扫描结束中断。
14	扫描组1继续连续扫描操作。*2

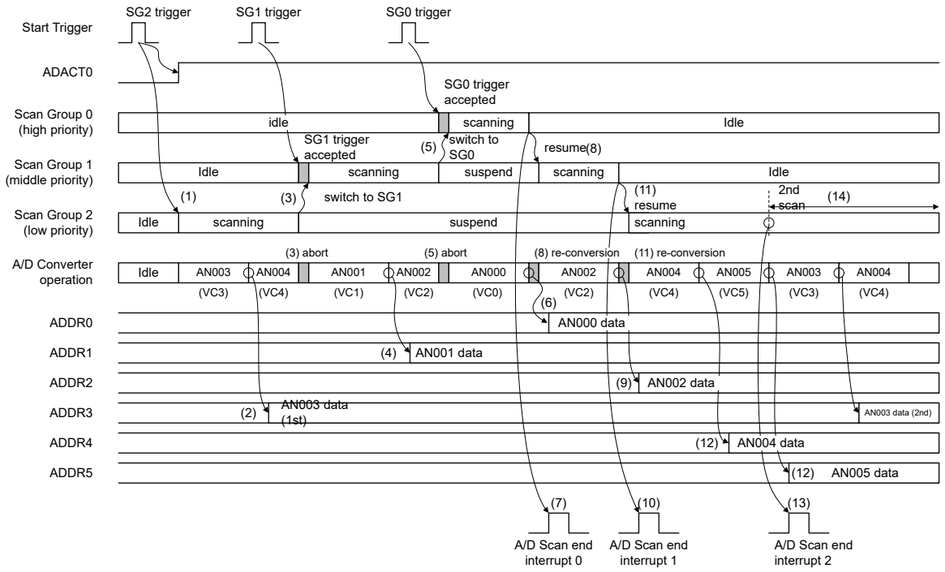
注1.扫描操作的中断和重新启动时间取决于操作条件。有关详细信息，请参阅第36.3.16.3节。限制组优先操作。

注2.要停止连续扫描操作，请按照第36.5.4节中所述的步骤进行操作。强制停止AD转换操作。

A/D Conversion configuration



A/D Conversion operation



Note: SG: Scan Group VC: Virtual channel

Figure 36.19 Example of Group Priority Operation (Continuous Scan mode) (3 groups)

36.3.16.3 Restrictions on Group Priority Operation

(1) Channel-dedicated sample-and-hold circuit Restrictions

Channel-dedicated sample-and-hold circuit is prohibited in Group Priority Operation.

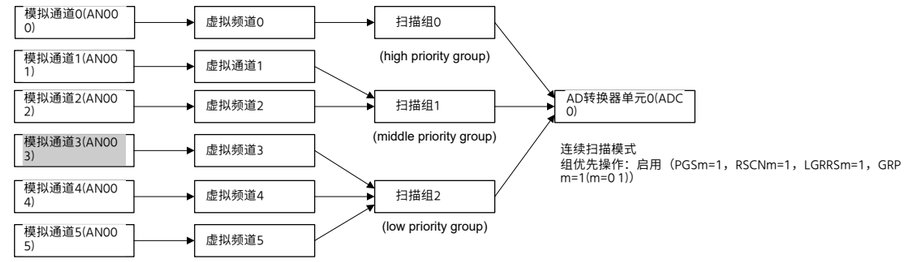
(2) Restrictions on the operation mode and operation setting of the A/D converter

Group Priority Operation in Single Scan mode prohibits the use of three or more scan groups for a single A/D converter. In this case, the operation is not guaranteed.

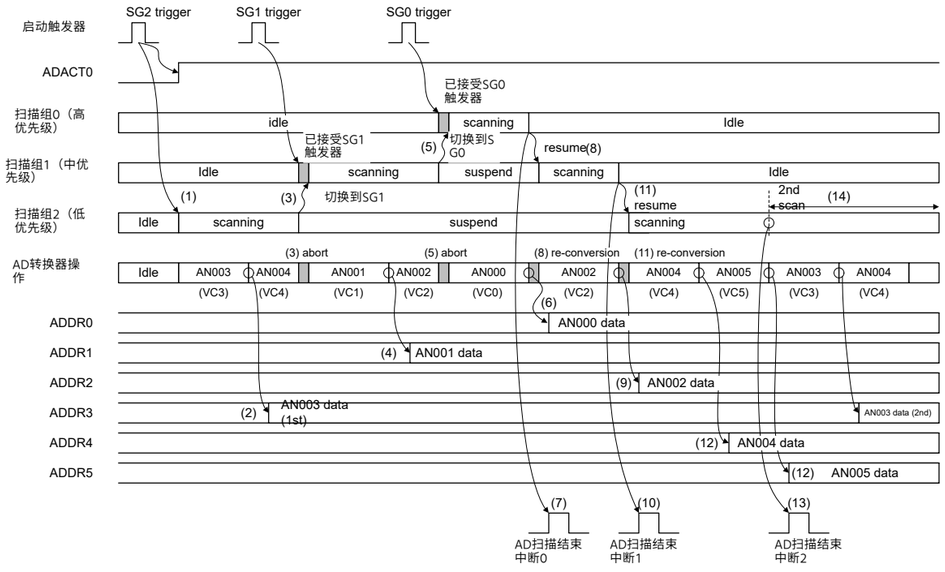
When using three or more scan groups for one A/D converter in Group Priority Operation, use the A/D converter in Continuous Scan mode.

For more details, refer to Table 36.12.

AD转换配置



AD转换操作



Note: SG：扫描组VC：虚拟通道

Figure 36.19 组优先操作示例（连续扫描模式）（3组）

36.3.16.3 群组优先操作限制

(1) 通道专用采样保持电路限制

在组优先操作中禁止使用通道专用的采样保持电路。

(2) AD转换器的操作模式和操作设置的限制

单扫描模式下的组优先操作禁止对单个AD转换器使用三个或更多扫描组。在这种情况下，无法保证操作。

当在组优先操作中为一个AD转换器使用三个或更多扫描组时，在组优先操作中使用AD转换器连续扫描模式。

更多详细信息，请参见表36.12。

(3) Restrictions on Group Priority Operation in Continuous Scan mode

In Group Priority Operation in Continuous Scan mode, do not input A/D conversion start triggers for scan groups that have a lower priority than the scan group that started continuous scanning operation. If this restriction is violated, the operation is not guaranteed.

(4) Restrictions on Trigger Input for the Same Scan Group

Input the A/D converter start triggers for the same scan group in Group Priority Operation for the following periods.

[When Synchronous Operation is disabled (ADSYCR.ADSYDISm = 1)]

- 2 ADCLK + 2 PCLK cycles after the scan end flag is set *1

[When Synchronous Operation is enabled (ADSYCR.ADSYDISm = 0)]

- Synchronous Operation Period cycle × 2 after the scan end flag is set *1

Note: m = 0, 1

Note 1. ADSCANENDSR.SCANENDFn = 1 (n = 0 to 8)

If A/D conversion start triggers are input without waiting for the above period, the A/D conversion start triggers may be lost. To accept A/D conversion start triggers reliably, input triggers at the intervals described above.

(5) Restrictions on Suspend and Resume for Scanning operation of Low-Priority Groups

When an A/D conversion start trigger for the high priority group is input during scanning of the low priority group in Group Priority Operation, the scanning operation of the low priority group is interrupted at the timing shown in the following:

[Scan interruption timing of low priority group]

- When Synchronous Operation is enabled
  - After the A/D converter start trigger of the high-priority group is accepted, the scanning operation of the low-priority group is suspended after waiting until the next Synchronous Operation Period timing.
- When Synchronous Operation is disabled
  - The scanning operation of the low-priority group is immediately suspended after the A/D conversion start trigger of the high-priority group is accepted.

If A/D conversion is being performed on channels for which A/D-Converted Value Addition/Averaging Function is to be used at the timing of scan interruption of a low-priority group, the midway result of A/D-converted value addition/average value at that time is discarded. When the scanning operation of the low-priority group is resumed, A/D conversion is performed again for the number of times specified by A/D-Converted Value Addition/Averaging Function from the beginning.

If the scanning operation is suspended by Group Priority Operation, ADGRSR.ACTGRn (n = 0 to 8) bit of the scanning group remains set to 1.

36.3.17 Synchronous Operation

Synchronous Operation is the function that controls the operations of multiple A/D converters so that they are synchronized.

36.3.17.1 Synchronous Operation Examples

(1) Basic Synchronous Operation

The basic operation of Synchronous Operation is shown in the following.

[Operation example]

- A/D converter Unit 0 (ADC0)
  - Single Scan mode
  - Assign analog channel 0 to 2 (AN000 to AN002) to scan group 0 and perform A/D conversion. (each analog channel allocates virtual channel 0 to 2)

(3) 连续扫描模式下组优先操作的限制

在连续扫描模式下的组优先操作中，对于优先级低于开始连续扫描操作的扫描组的扫描组，不要输入AD转换开始触发。如果违反此限制，则无法保证操作。

(4) 同一扫描组的触发输入限制

在以下时段中，在GroupPriorityOperation中输入同一扫描组的AD转换器启动触发器。

[禁用同步操作时(ADSYCR.ADSYDISm=1)]

●设置扫描结束标志后的2个ADCLK+2个PCLK周期*1

[启用同步操作时(ADSYCR.ADSYDISm=0)]

●设置扫描结束标志后的同步操作周期周期×2*1

Note: m = 0, 1

注1.ADSCANENDSR.SCANENDFn=1（n=0到8）

如果在未等待上述时间的情况下输入AD转换启动触发器，则可能会丢失AD转换启动触发器。要可靠地接受AD转换开始触发，请按上述间隔输入触发。

(5) 低优先级组扫描操作暂停和恢复的限制

在Group中的低优先级组扫描期间输入高优先级组的AD转换启动触发时PriorityOperation，低优先级组的扫描操作在如下所示的时序被中断：

[低优先级组的扫描中断时机]

●启用同步操作时

高优先级组的AD转换器启动触发被接受后，低优先级组的扫描操作在等待下一个SynchronousOperationPeriod时序后暂停。

●当同步操作被禁用时

在接受高优先级组的AD转换开始触发后，立即暂停低优先级组的扫描操作。

如果在低优先级组的扫描中断时对要使用AD转换值相加平均功能的通道执行AD转换，则此时的AD转换值相加平均值的中间结果被丢弃。当低优先级组的扫描操作重新开始时，AD转换从头开始重新执行AD-ConvertedValueAdditionAveragingFunction指定的次数。

如果扫描操作被GroupPriorityOperation暂停，扫描组的ADGRSR.ACTGRn（n=0到8）位保持设置为1。

36.3.17 同步操作

同步操作是控制多个AD转换器的操作以使其同步的功能。

36.3.17.1 同步操作示例

(1) 基本同步操作

同步操作的基本操作如下所示。

[Operation example]

●AD转换器单元0(ADC0)

单次扫描模式

将模拟通道0到2（AN000到AN002）分配给扫描组0并执行AD转换。（每个模拟通道分配虚拟通道0到2）

- A/D converter Unit 1 (ADC1)
  - Single Scan mode
  - Assign analog channel 6 to 8 (AN006 to AN008) to scan group 1 and perform A/D conversion.
    (each analog channel allocates virtual channel 6 to 8)

[Operation]

1. When a trigger of scan group 0 is input, a wait is inserted until the A/D conversion synchronization timing.
2. At the timing of Synchronous Operation Period, the trigger input of scan group 0 is accepted, and the scanning operation of scan group 0 (for ADC0) starts.
3. When a trigger of scan group 1 is input, a wait is inserted until the A/D conversion synchronization timing.
4. At the timing of Synchronous Operation Period, the trigger input of scan group 1 is accepted, and the scanning operation of scan group 1 (for ADC1) starts.
5. During Synchronous Operation, the A/D converter starts the sampling operation in accordance with Synchronous Operation Period.

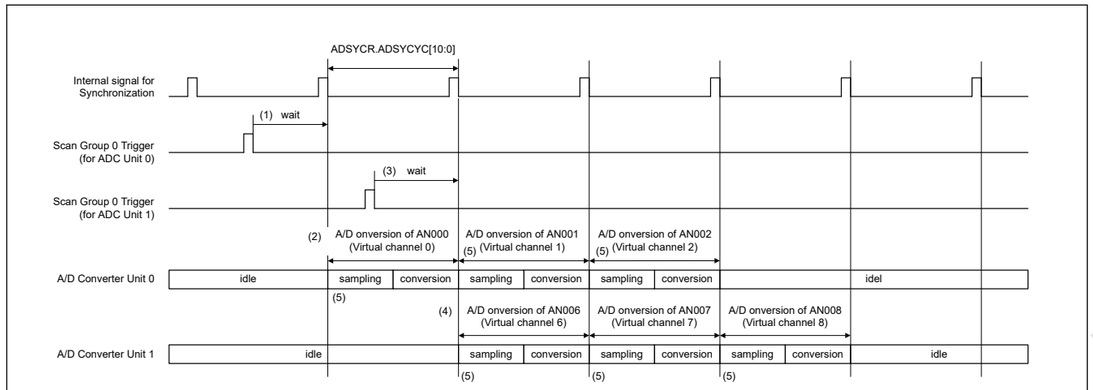


Figure 36.20 Example of Synchronous Operation (Single Scan mode)

(2) Synchronous Operation using with Channel-dedicated sample-and-hold circuit

An example of Synchronous Operation using with Channel-dedicated sample-and-hold circuit is shown in the following.

[Operation example]

- A/D converter Unit 0 (ADC0)
  - Single Scan mode
  - Using Channel-dedicated sample-and-hold circuit Unit 0 to Unit 2 (SH0 to SH2)
  - Assign analog channel 0/2/4 (AN000, AN002, AN004) to scan group 0, and performing A/D conversion using with Channel-dedicated sample-and-hold circuits.
    (each analog channel is assigned to virtual channel 0 to 2)
- A/D converter Unit 1 (ADC1)
  - Single Scan mode
  - Assign analog channel 6 to 8 (AN006 to AN008) to scan group 1 and perform A/D conversion.
    (each analog channel is assigned to virtual channel 6 to 8)

[Operation]

1. When a trigger of scan group 1 is input, a wait is inserted until the A/D conversion synchronization timing.
2. At the timing of Synchronous Operation Period, the trigger input of scan group 1 is accepted, and the scanning operation of scan group 1 (for ADC1) starts.

●AD转换器单元1(ADC1)

单次扫描模式

将模拟通道6到8（AN006到AN008）分配给扫描组1并执行AD转换。（每个模拟通道分配虚拟通道6到8）

[Operation]

1.当输入扫描组0的触发时，插入等待直到AD转换同步时序。

2.在SynchronousOperationPeriod的定时，接受扫描组0的触发输入，扫描组0（ADC0用）的扫描操作开始。

3.当输入扫描组1的触发时，插入等待直到AD转换同步时序。

4.在同步操作周期的时间点，接受扫描组1的触发输入，扫描组1（ADC1用）的扫描操作开始。

5.在同步操作期间，AD转换器按照同步操作周期开始采样操作。

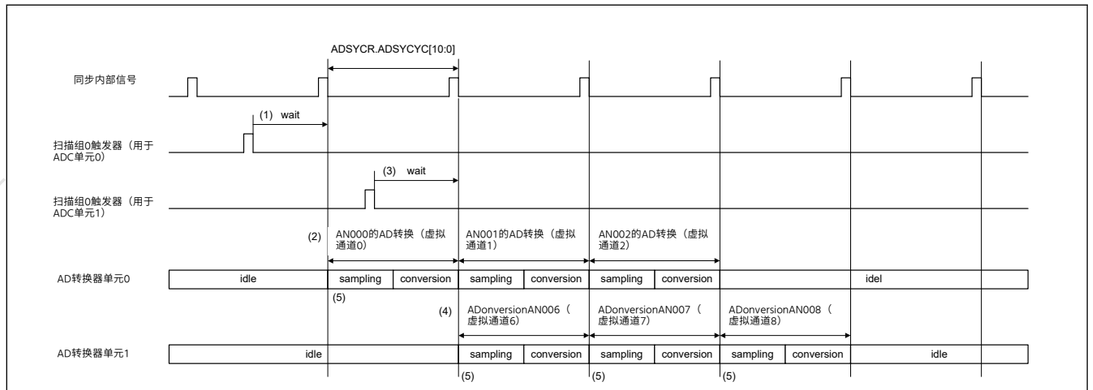


Figure 36.20 同步操作示例（单次扫描模式）

(2) 使用通道专用采样保持电路进行同步操作

使用通道专用采样保持电路的同步操作示例如下所示。

[Operation example]

●AD转换器单元0(ADC0)

单次扫描模式

使用通道专用采样保持电路单元0至单元2（SH0至SH2）

将模拟通道024(AN000 AN002 AN004)分配给扫描组0，并使用通道专用的采样保持电路执行AD转换。（每个模拟通道分配给虚拟通道0到2）

●AD转换器单元1(ADC1)

单次扫描模式

将模拟通道6到8（AN006到AN008）分配给扫描组1并执行AD转换。（每个模拟通道分配给虚拟通道6到8）

[Operation]

1.当输入扫描组1的触发时，插入等待直到AD转换同步时序。

2.在同步操作周期的时间点，接受扫描组1的触发输入，扫描组1（ADC1用）的扫描操作开始。

3. When a trigger of scan group 0 is input, a wait is inserted until the A/D conversion synchronization timing.
4. At the timing of Synchronous Operation Period, the trigger input of scan group 0 is accepted, and the scanning operation of scan group 0 (for ADC0) starts. Channel-dedicated sample-and-hold circuit (SH0 to SH2) samples and holds the analog-channels of AN000 / AN002 / AN004 at the beginning of the scanning operation in scan group 0.
5. After the holding by Channel-dedicated sample-and-hold circuit, A/D converter starts the samplings and the conversions.
6. During Synchronous Operation, Channel-dedicated sample-and-hold circuit and A/D converter starts the sampling operation in accordance with Synchronous Operation Period.

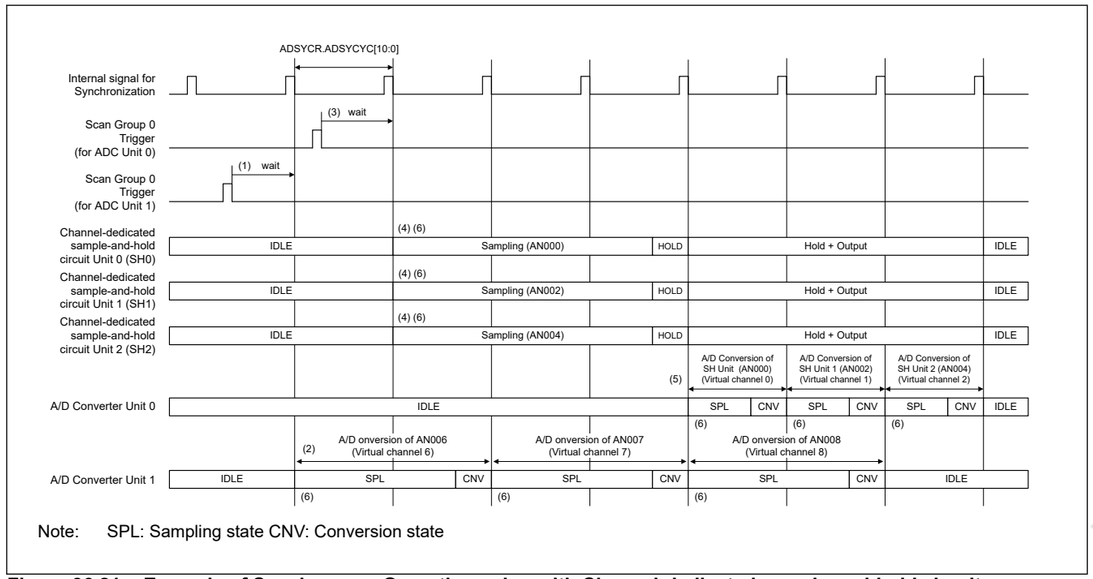


Figure 36.21 Example of Synchronous Operation using with Channel-dedicated sample-and-hold circuit

36.3.17.2 Restrictions on Synchronous Operation

When Synchronous Operation is used, observe the following restrictions. If the following restrictions are violated, operations are not guaranteed.

1. Basic restrictions
   - Set the Synchronous Operation Period so that it is an even number of cycles.
     - ADSYCR.ADSYCYC[10:0] = 2 × i
       (i: Any integer greater than or equal to 1 (i = 1, 2, 3…))
   - Set the Synchronous Operation Period to a value larger than successive approximation time of ADCm (m = 0, 1).
     - ADSYCR.ADSYCYC[10:0] ≥ ADCNVSTR.CSTm[5:0] + 1
       (m = 0, 1)
   - Set so that the sum of the sampling times of the analog channels and successive approximation time of ADCm (m = 0, 1) is an integral multiple of the Synchronous Operation Period.
     - ADSSTRx.SSTy[9:0] + ADCNVSTR.CSTm[5:0] = ADSYCR.ADSYCYC[10:0] × i
       (x = 0 to 7. y = 0 to 15. m = 0, 1. i: Any integer greater than or equal to 1 (i = 1, 2, 3…))
   - Set the Synchronous Operation Period to a value larger than successive approximation time at Self-Calibration.*1
     - ADSYCR.ADSYCYC[10:0] ≥ ADCALSTCR.CALADCST[5:0] + 1
   - Set the sampling time and successive approximation time at Self-Calibration to be integral multiples of the Synchronous Operation Period.*1

3.当输入扫描组0的触发时，插入等待直到AD转换同步时序。

4.在SynchronousOperationPeriod的定时，扫描组0的触发输入被接受，扫描组0（ADC0用）的扫描操作开始。通道专用采样保持电路（SH0至SH2）在扫描组0中的扫描操作开始时对AN000AN002AN004的模拟通道进行采样和保持。

5.通道专用采样保持电路保持后，AD转换器开始采样和转换。

6.在同步操作期间，通道专用的采样保持电路和AD转换器按照同步操作周期开始采样操作。

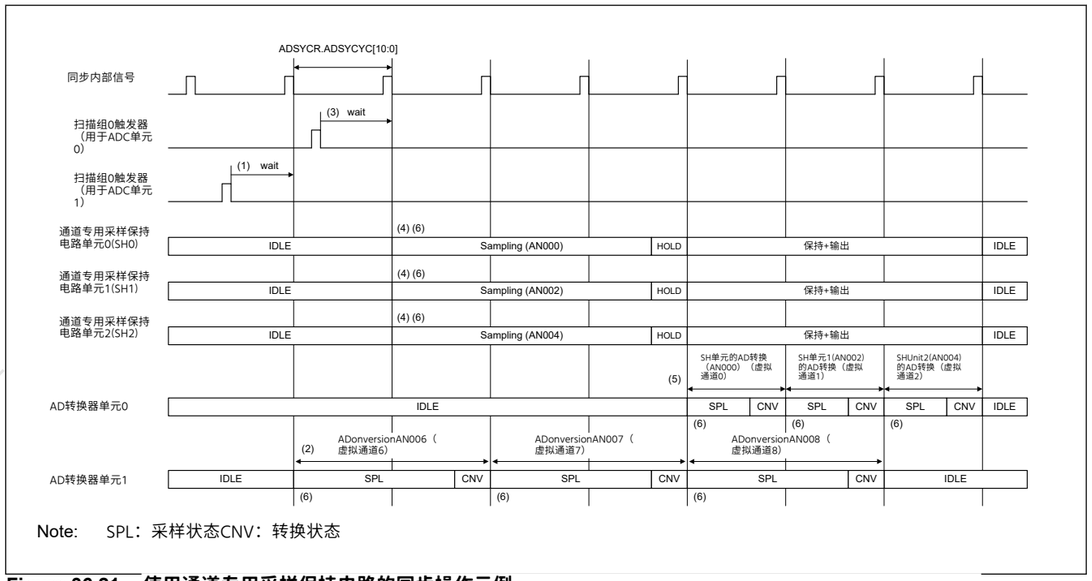


Figure 36.21 使用通道专用采样保持电路的同步操作示例

36.3.17.2 同步操作的限制

使用同步操作时，请遵守以下限制。如果违反以下限制，则无法保证操作。

1.基本限制

- ●将同步操作周期设置为偶数周期。
  - ADSYCR.ADSYCYC[10:0] = 2 × i
    (i:任何大于或等于1的整数(i=1 2 3…))
- ●将SynchronousOperationPeriod设置为大于ADCm的逐次逼近时间(m=0 1)的值。
  - ADSYCR.ADSYCYC[10:0] ≥ ADCNVSTR.CSTm[5:0] + 1
    (m = 0, 1)
- ●设置为模拟通道的采样时间和ADCm(m=0 1)的逐次逼近时间之和为同步操作周期的整数倍。
  - ADSSTRx.SSTy[9:0] + ADCNVSTR.CSTm[5:0] = ADSYCR.ADSYCYC[10:0] × i
    （x=0到7。y=0到15。m=0、1。i：任何大于或等于1的整数（i=1、2、3…））
- ●将同步操作周期设置为大于自校准时的逐次逼近时间的值。*1
  - ADSYCR.ADSYCYC[10:0] ≥ ADCALSTCR.CALADCST[5:0] + 1
- ●将自校准时的采样时间和逐次逼近时间设置为同步操作周期的整数倍。*1

– ADCALSTCR.CALADSST[9:0] + ADCALSTCR.CALADCST[5:0] = ADSYCR.ADSYCYC[10:0] × i
(i: Any integer greater than or equal to 1 (i = 1, 2, 3…))

2. Restrictions when using Channel-dedicated sample-and-hold circuit

- Set the Synchronous Operation Period to a value greater than the hold mode switching time of Channel-dedicated sample-and-hold circuit.
  – ADSYCR.ADSYCYC[10:0] ≥ ADSHSTRm.SHHST[2:0] + 1
  (m = 0, 1)
- Set the sum of Channel-dedicated sample-and-hold circuit sampling time and the hold mode switching time to be an integral multiple of the Synchronous Operation Period.
  – ADSHSTRm.SHSST[7:0] + ADSHSTRm.SHHST[2:0] = ADSYCR.ADSYCYC[10:0] × i
  (i: Any integer greater than or equal to 1 (i = 1, 2, 3…))
- Set the hold mode switching time of Channel-dedicated sample-and-hold circuit so that it is the same as successive approximation time of ADCm (m = 0, 1).
  – ADSHSTRm.SHHST[2:0] = ADCNVSTR.CSTm[5:0]
  (m = 0, 1)
- Set the Synchronous Operation Period to a value greater than the hold mode switching time in Channel-dedicated sample-and-hold circuit's Self-Calibration operation.*1
  – ADSYCR. ADSYCYC[10:0] ≥ ADCALSHCR.CALSHHST[2:0] + 1
- Set so that the sum of Channel-dedicated sample-and-hold circuit sampling time and the hold mode switching time in Self-Calibration operation is an integral multiple of the Synchronous Operation Period.*1
  – ADCALSHCR.CALSHSST[7:0] + ADCALSHCR.CALSHHST[2:0] = ADSYCR.ADSYCYC[10:0] × i
  (i: Any integer greater than or equal to 1 (i = 1, 2, 3…))

3. Restrictions when using Disconnection Detection Assist Function

- Set Disconnection Detection Assist period so that it is the same as the Synchronous Operation Period.
  – ADSGDCRn.ADNDIS[3:0] = ADSYCR.ADSYCYC[10:0]
  (n = 0 to 8)

Note 1. In relation to this restriction, the restrictions on the settings of Self-calibration should be satisfied at the same time. For restrictions on the setting of self-calibration, see section 36.3.6.3. Restrictions on Self-Calibration.

36.4 A/D Conversion Data

This section describes the internal processing for A/D conversion data. For details about the operation of A/D conversion, refer to section 36.3. Operation.

36.4.1 Internal data processing flow

Figure 36.22 shows the internal processing-flow of A/D conversion data.

The A/D conversion data output from the A/D converter is temporarily stored in the data buffer. At this time, A/D conversion data is bit-extended to 16-bit length data for subsequent data processing. (12-bit length data is shifted left by 4 bits and extended to 16-bit length data.) And then, various data processing is performed based on the register setting. If the function that corresponds to each data processing is not used, its data processing is skipped.

ADCALSTCR.CALADSST[9:0]+ADCALSTCR.CALADCST[5:0]=ADSYCR.ADSYCYC[10:0]×i(i:任何大于或等于1的整数(i=1 2 3…))

2.使用通道专用采样保持电路时的限制

●将同步操作周期设置为大于通道专用采样保持电路的保持模式切换时间的值。

– ADSYCR.ADSYCYC[10:0] ≥ ADSHSTRm.SHHST[2:0] + 1
(m = 0, 1)

●将通道专用采样保持电路采样时间和保持模式切换时间之和设置为同步操作周期的整数倍。

ADSHSTRm.SHSST[7:0]+ADSHSTRm.SHHST[2:0]=ADSYCR.ADSYCYC[10:0]×i（i：任何大于或等于1的整数（i=1、2、3…））

●设置通道专用采样保持电路的保持模式切换时间，使其与ADCm的逐次逼近时间(m=0 1)相同。

– ADSHSTRm.SHHST[2:0] = ADCNVSTR.CSTm[5:0]
(m = 0, 1)

●将同步操作周期设置为大于通道专用采样保持电路自校准操作中的保持模式切换时间的值。*1

– ADSYCR. ADSYCYC[10:0] ≥ ADCALSHCR.CALSHHST[2:0] + 1

●设置为使通道专用采样保持电路采样时间和自校准操作中的保持模式切换时间之和为同步操作周期的整数倍。*1

ADCALSHCR.CALSHSST[7:0]+ADCALSHCR.CALSHHST[2:0]=ADSYCR.ADSYCYC[10:0]×i(i:任何大于或等于1的整数(i=1 2 3…))

3.使用断线检测辅助功能时的限制

●设置断线检测辅助周期，使其与同步运行周期相同。

– ADSGDCRn.ADNDIS[3:0] = ADSYCR.ADSYCYC[10:0]
(n = 0 to 8)

注1.关于此限制，需要同时满足Self-calibration的设置限制。
关于自校准设置的限制，请参见第36.3.6.3节。自校准的限制。

36.4 AD转换数据

本节介绍AD转换数据的内部处理。关于AD转换的操作，请参阅36.3节。手术。

36.4.1 内部数据处理流程

图36.22显示了AD转换数据的内部处理流程。

AD转换器输出的AD转换数据暂时存储在数据缓冲器中。此时，AD转换数据被位扩展为16位长度的数据，用于后续的数据处理。（12位长度数据左移4位，扩展为16位长度数据。）然后，根据寄存器设置执行各种数据处理。如果不使用每个数据处理对应的函数，则跳过其数据处理。

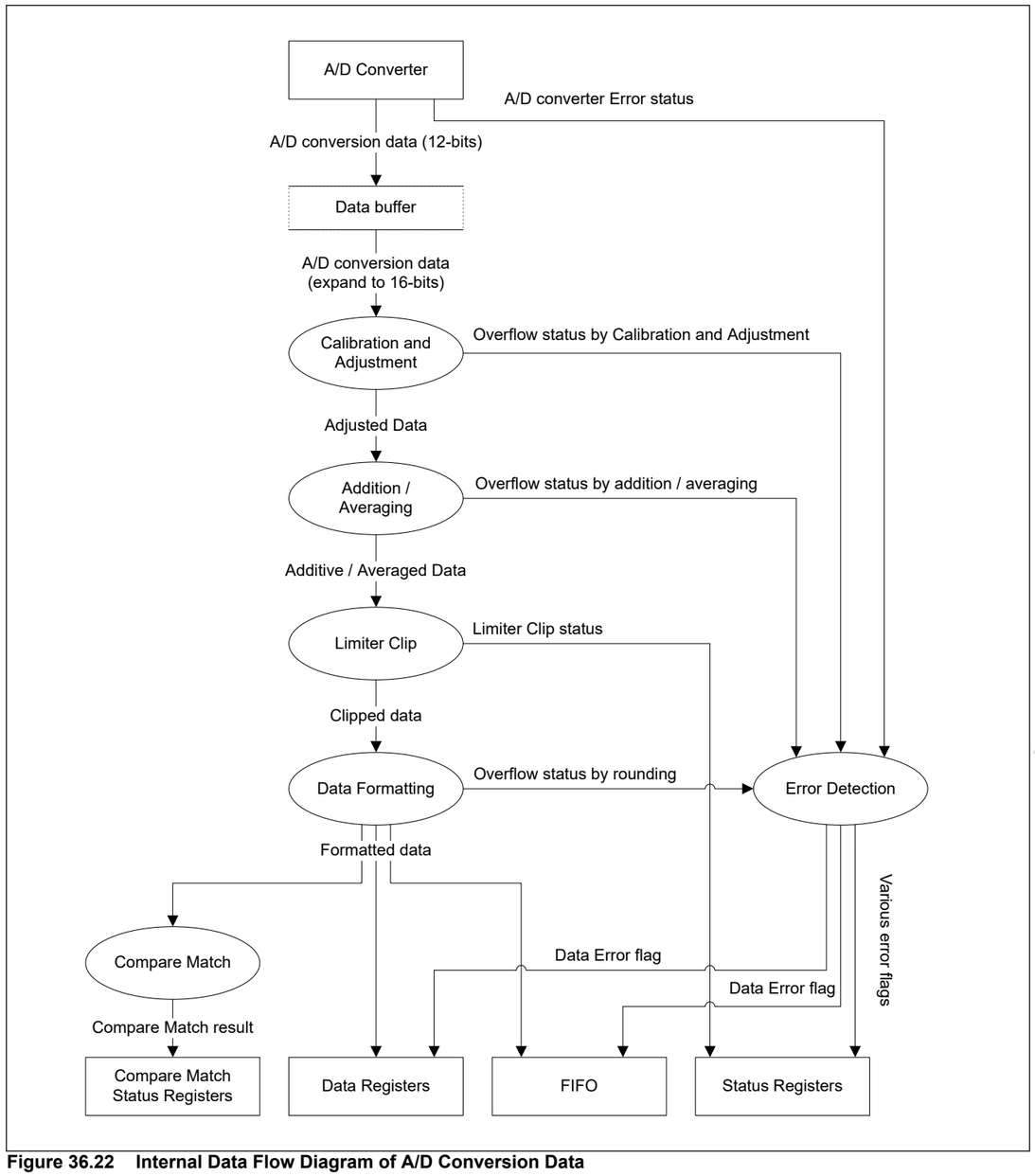


Figure 36.22 Internal Data Flow Diagram of A/D Conversion Data

36.4.2 Calibration and Adjustment

In this process, the following processing is performed for the results output from the A/D converter.

1. Calibrate Gain Error and Offset Error
2. Adjust User's Gain
3. Adjust User's Offset

For details on each process, refer to the each item.

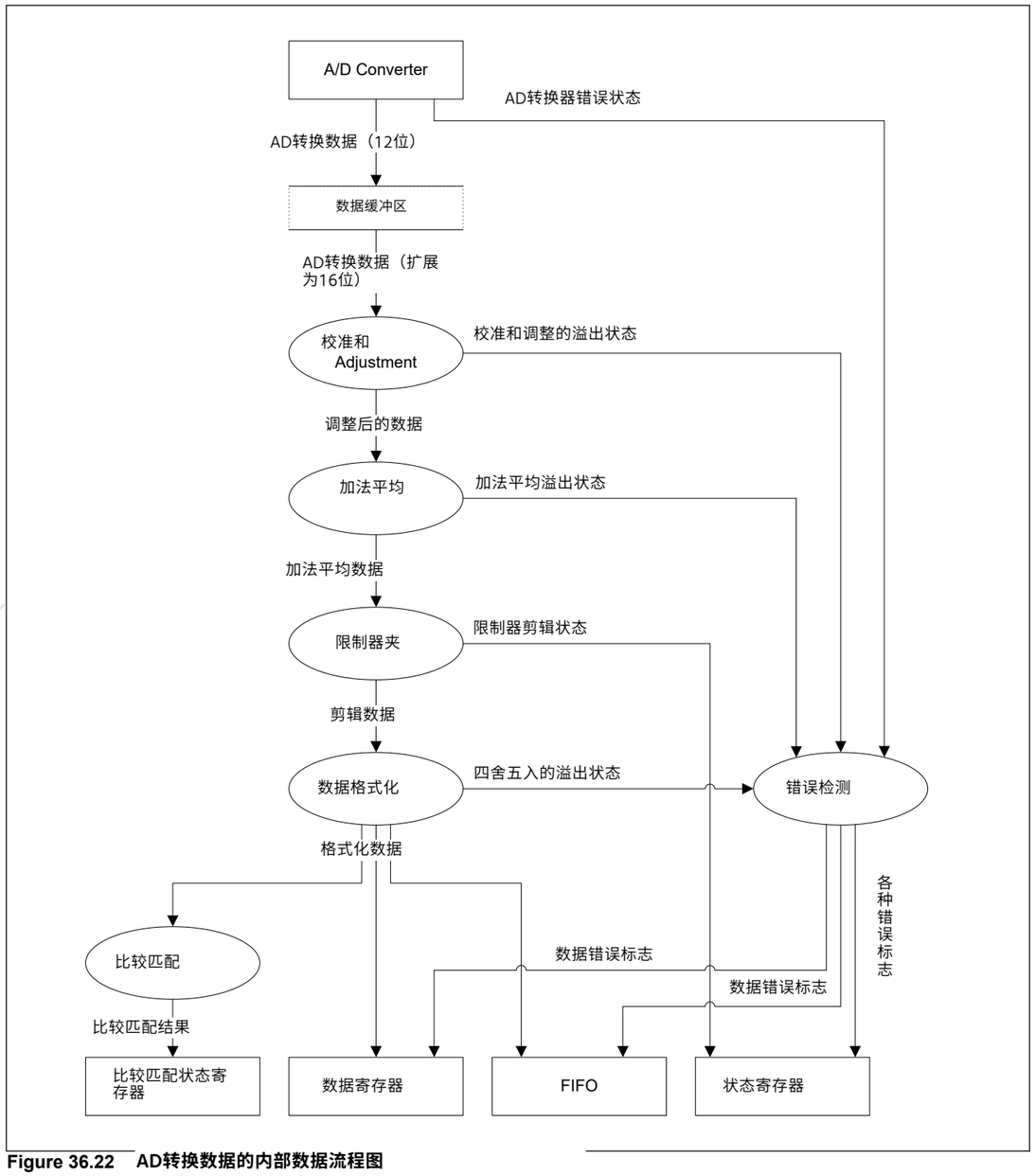


Figure 36.22 AD转换数据的内部数据流程图

36.4.2 校准和调整

在此过程中，对从AD转换器输出的结果执行以下处理。

1.校准增益误差和偏移误差

2.调整用户增益

3.调整用户的偏移量

有关每个过程的详细信息，请参阅每个项目。

36.4.2.1 Gain Error and Offset Error Calibration

This process calibrates the A/D converter's Gain Error and Offset Error due to by chip-by-chip characteristic variations.

Calibration for the A/D converter's Gain Error and Offset Error is performed by calculation based on error data measured inside the ADC by Self-Calibration operation.

36.4.2.2 User's Gain Adjustment

User's Gain adjusting function multiplies the A/D conversion data by an arbitrary coefficient value.

The coefficient value of User's Gain is set in ADUGTRn.UGAIN[23:0] (n = 0 to 7). User's Gain can be set for each virtual channel. The User's Gain Table to be used is selected in ADDOPCRAm.GAINSEL[3:0] (m = 0 to 36). The coefficient value of User's Gain is the sum of the gain corresponding to the bits that are set to 1 in ADUGTRn.UGAIN[23:0]. Table 36.16 shows the gain factors corresponding to the respective bits in ADUGTRn.UGAIN[23:0]. An example of setting User's Gain is shown in Table 36.17. Figure 36.23 shows the relationship between before adjustment (input) and after adjustment (output) to the A/D conversion result when User's Gain adjustment function is used.

The overflow of A/D conversion data may occur when User's Gain adjusting function is used.

Table 36.16 List of gains corresponding to each gain setting bit in User's Gain setting table register

UGAIN[23:16]	Gain value	UGAIN[15:8]	Gain value	UGAIN[7:0]	Gain value
b23	2^{1} = 2.0	b15	2^{-7} = 7.813E-03	b7	2^{-15} = 3.052E-05
b22	2^{0} = 1.0	b14	2^{-8} = 3.906E-03	b6	2^{-16} = 1.526E-05
b21	2^{-1} = 0.5	b13	2^{-9} = 1.953E-03	b5	2^{-17} = 7.629E-06
b20	2^{-2} = 0.25	b12	2^{-10} = 9.766E-04	b4	2^{-18} = 3.815E-06
b19	2^{-3} = 0.125	b11	2^{-11} = 4.883E-04	b3	2^{-19} = 1.907E-06
b18	2^{-4} = 0.0625	b10	2^{-12} = 2.441E-04	b2	2^{-20} = 9.537E-07
b17	2^{-5} = 0.03125	b9	2^{-13} = 1.221E-04	b1	2^{-21} = 4.768E-07
b16	2^{-6} = 1.563E-02	b8	2^{-14} = 6.104E-04	b0	2^{-22} = 2.384E-07

Table 36.17 Example of User's Gain Settings

ADUGTRn.UGAIN[23:0] (n = 0 to 7)	Gain value
0x000000	x0.0000
…	…
0x040000	x0.0625
…	…
0x080000	x0.1250
…	…
0x100000	x0.2500
…	…
0x200000	x0.5000
…	…
0x400000 (initial value)	x1.0000
…	…
0x800000h	x2.0000
…	…
0xFFFFFF	x3.9999

36.4.2.1 增益误差和失调误差校准

该过程校准因芯片特性变化而导致的AD转换器的增益误差和偏移误差。

AD转换器的增益误差和失调误差的校准是根据通过自校准操作在ADC内部测量的误差数据进行计算的。

36.4.2.2 用户增益调整

用户的增益调整功能将AD转换数据乘以任意系数值。

用户增益的系数值在ADUGTRn.UGAIN[23:0]（n=0到7）中设置。可以为每个虚拟通道设置用户增益。要使用的用户增益表在ADDOPCRAm.GAINSEL[3:0]（m=0到36）中选择。用户增益的系数值是ADUGTRn.UGAIN[23:0]中设置为1的位对应的增益之和。表36.16显示了对应于ADUGTRn.UGAIN[23:0]中各个位的增益因子。设置用户增益的示例如表36.17所示。图36.23显示了使用用户增益调整功能时调整前（输入）和调整后（输出）与AD转换结果的关系。

使用用户增益调整功能时，可能会出现AD转换数据溢出。

Table 36.16 用户增益设置表寄存器中每个增益设置位对应的增益列表

UGAIN[23:16]	获得价值	UGAIN[15:8]	获得价值	UGAIN[7:0]	获得价值
b23	2^{1} = 2.0	b15	2^{-7} = 7.813E-03	b7	2^{-15} = 3.052E-05
b22	2^{0} = 1.0	b14	2^{-8} = 3.906E-03	b6	2^{-16} = 1.526E-05
b21	2^{-1} = 0.5	b13	2^{-9} = 1.953E-03	b5	2^{-17} = 7.629E-06
b20	2^{-2} = 0.25	b12	2^{-10} = 9.766E-04	b4	2^{-18} = 3.815E-06
b19	2^{-3} = 0.125	b11	2^{-11} = 4.883E-04	b3	2^{-19} = 1.907E-06
b18	2^{-4} = 0.0625	b10	2^{-12} = 2.441E-04	b2	2^{-20} = 9.537E-07
b17	2^{-5} = 0.03125	b9	2^{-13} = 1.221E-04	b1	2^{-21} = 4.768E-07
b16	2^{-6} = 1.563E-02	b8	2^{-14} = 6.104E-04	b0	2^{-22} = 2.384E-07

Table 36.17 用户增益设置示例

ADUGTRn.UGAIN[23:0] (n = 0 to 7)	获得价值
0x000000	x0.0000
…	…
0x040000	x0.0625
…	…
0x080000	x0.1250
…	…
0x100000	x0.2500
…	…
0x200000	x0.5000
…	…
0x400000 (initial value)	x1.0000
…	…
0x800000h	x2.0000
…	…
0xFFFFFF	x3.9999

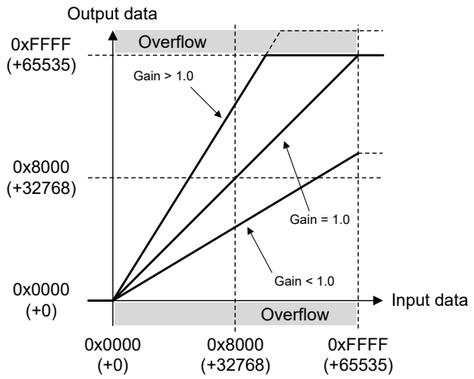


Figure 36.23 User's Gain Adjustment (16-bit data length format)

36.4.2.3 User's Offset Adjustment

User's Offset adjustment function adds or subtracts any constant value to or from the A/D conversion data.

The constant value of User's Offset is set in ADUOFTRn.UOFSET[15:0] (n = 0 to 7). User's Offset can be set for each virtual channel. User's Offset Table to be used is selected in ADDOPCRAm.OFSETSEL[3:0] (m = 0 to 36). Table 36.18 shows the relationship between the register setting value of User's Offset and the offset value. Figure 36.24 shows the relationship between before adjustment (input) and after adjustment (output) to the A/D conversion result when User's Offset adjustment function is used.

When User's Offset adjusting function is used, overflow of A/D conversion data may occur.

Table 36.18 Relationship between User's Offset register value and offset value

ADUOFTRn.UOFSET[15:0] (n = 0 to 7)	Offset value (16bit data length format)
0x7FFF	+32767
0x7FFE	+32766
0x7FFD	+32765
…	…
0x0003	+3
0x0002	+2
0x0001	+1
0x0000 (initial value)	0
0xFFFF	-1
0xFFFE	-2
0xFFFD	-3
…	…
0x8002	-32766
0x8001	-32767
0x8000	-32768

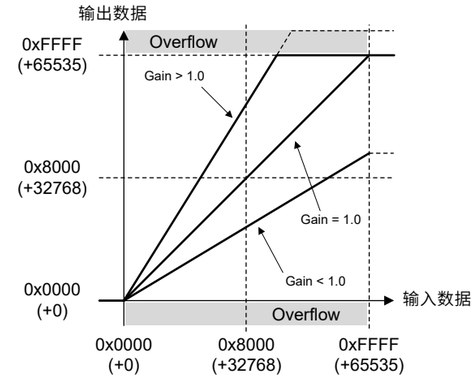


Figure 36.23 用户增益调整（16位数据长度格式）

36.4.2.3 用户偏移调整

用户的偏移调整功能可以在AD转换数据中添加或减去任何常数值。

用户偏移的常数值在ADUOFTRn.UOFSET[15:0]中设置（n=0到7）。可以为每个虚拟通道设置用户偏移量。要使用的用户偏移表在ADDOPCRAm.OFSETSEL[3:0]（m=0到36）中选择。表36.18显示了用户偏移的寄存器设置值和偏移值之间的关系。图36.24显示了使用User'sOffset调整功能时调整前（输入）和调整后（输出）与AD转换结果的关系。

使用User'sOffset调整功能时，可能会发生AD转换数据溢出。

Table 36.18 用户偏移寄存器值与偏移值的关系

ADUOFTRn.UOFSET[15:0] (n = 0 to 7)	偏移值（16bit数据长度格式）
0x7FFF	+32767
0x7FFE	+32766
0x7FFD	+32765
…	…
0x0003	+3
0x0002	+2
0x0001	+1
0x0000 (initial value)	0
0xFFFF	-1
0xFFFE	-2
0xFFFD	-3
…	…
0x8002	-32766
0x8001	-32767
0x8000	-32768

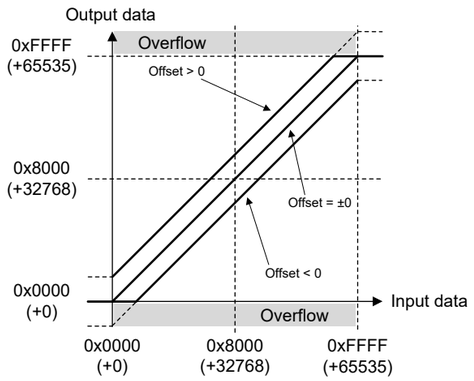


Figure 36.24 User's Offset Adjustment (16-bit data length format)

36.4.3 A/D-Converted Value Addition/Average Function

A/D-Converted Value Addition Function and A/D-Converted Value Averaging Function perform A/D conversion on analog channels continuously for the specified number of times, and calculates the total or the average value of the A/D conversion data.

The A/D-converted value addition/averaging function can be set for each virtual channel in ADDOPCRBn.AVEMD[1:0] (n = 0 to 36) and ADDOPCRBn.ADC[3:0] (n = 0 to 36). When A/D-converted value addition/averaging function is used, the A/D converter repeats A/D conversion of the target analog channels continuously for the specified number of times. After A/D conversion of the number of times specified in ADDOPCRBn.ADC[3:0] bits is completed, the calculated result of the total value or average value is output.

Note: When the A/D-converted value addition/average function is used, overflow of the A/D conversion data may occur. However, in certain conditions, A/D conversion data overflow may not be detected. For details about A/D conversion data overflow, refer to section 36.6.2. A/D conversion overflow.

36.4.4 Limiter Clip Function

Limiter Clip Function is the function to set the upper and lower limits of A/D conversion data. When the A/D conversion data exceeds the specified upper limit value, it is clipped to the upper limit value. If the A/D conversion data falls below the specified lower limit, it is clipped to the lower limit value. Figure 36.25 shows an example of Limiter Clip Function operation.

The upper and lower limits of Limiter Clip Function can be specified in ADLIMTRn.LIMU[15:0] (n = 0 to 7) and ADLIMTRn.LIML[15:0] (n = 0 to 7). The Limiter Clip Function can be selected use or not (enable or disable) for each virtual channel in ADDOPCRCm.LIMTBLS[3:0] (m = 0 to 36).

Limiter Clip Function is processed by 16-bit length. When 14-/12-/10-bit is selected as the data length of the A/D conversion data (when ADDIOCRCm.ADPRC[1:0] = 01b, 10b, or 11b), the rounding to the specified data length is performed after the clipping by Limiter Clip Function. For more details, refer to section 36.4.5. Data Formatting process.

For Limiter Clip Function, the upper limit value should be greater than the lower limit value (ADLIMTRn.LIMU[15:0] > ADLIMTRn.LIML[15:0] (n = 0 to 7)). When the upper limit value is less than or equal to the lower limit value, the A/D conversion data is always 0x0000.

If a limiter clip occurs, the flags are set in the following status registers:

- ADLIMGRSR: The flag is set to the bit corresponding to the scan group where the limiter clip occurred.
- ADLIMCHSR0: If a limiter clip occurs during A/D conversion of an analog input channel, the flag is set to the corresponding bit.
- ADLIMEXSR: If a limiter clip occurs during A/D conversion of Extended Analog Function, the flag is set to the corresponding bit.

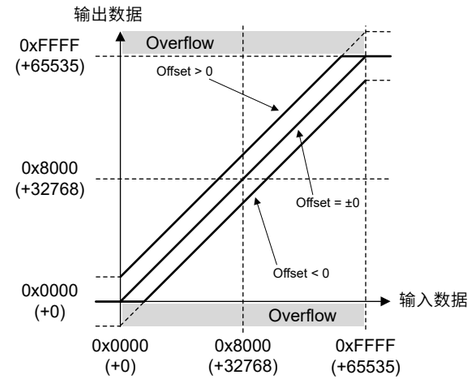


Figure 36.24 用户偏移调整（16位数据长度格式）

36.4.3 一个D转换的增值平均函数

D-ConvertedValueAdditionFunction和AD-ConvertedValueAveragingFunction在模拟通道上连续执行AD转换指定次数，并计算AD转换数据的总和或平均值。

可以在ADDOPCRBn.AVEMD[1:0]（n=0到36）和ADDOPCRBn.ADC[3:0]（n=0到36）中为每个虚拟通道设置AD转换值加法平均功能。使用AD转换值加法平均功能时，AD转换器连续重复目标模拟通道的AD转换指定次数。完成ADDOPCRBn.ADC[3:0]位中指定次数的AD转换后，输出总值或平均值的计算结果。

Note: 使用AD转换值加法平均功能时，可能会发生AD转换数据溢出。
但是，在某些情况下，可能无法检测到AD转换数据溢出。关于AD转换数据溢出的详细内容，请参阅36.6.2节。AD转换溢出。

36.4.4 限制器剪辑功能

限制器剪辑功能是设置AD转换数据的上限和下限的功能。当AD转换数据超过指定的上限值时，将被剪裁到上限值。如果AD转换数据低于指定的下限，则将其裁剪为下限值。图36.25显示了限制器削波功能操作的示例。

限制器削波功能的上限和下限可以在ADLIMTRn.LIMU[15:0]（n=0到7）中指定，并且ADLIMTRN.LIML[15:0]（n=0到7）。可以为ADDOPCRCm.LIMTBLS[3:0](m=0到36)中的每个虚拟通道选择使用或不使用限制器剪辑功能（启用或禁用）。

限制器剪辑功能按16位长度处理。When14-12-10-bitisselectedasthedatalengthoftheADconversiondata(whenADDIOCRCm.ADPRC[1:0]=01b 10b or11b) theroundingtothespecifieddatalengthisperformedaftertheclipping通过限制器剪辑功能。有关详细信息，请参阅第36.4.5节。数据格式化过程。

对于限制器削波功能，上限值应大于下限值(ADLIMTRn.LIMU[15:0]>ADLIMTRn.LIML[15:0](n=0to7))。当上限值小于或等于下限值时，AD转换数据始终为0x0000。

如果发生限制器剪辑，则在以下状态寄存器中设置标志：

- ADLIMGRSR：该标志设置为与发生限制器剪辑的扫描组对应的位。
- ADLIMCHSR0：如果在模拟输入通道的AD转换过程中出现限幅器削波，则将该标志设置为相应的位。
- ADLIMEXSR：如果在扩展模拟功能的AD转换过程中出现限幅器削波，则将该标志设置为相应的位。

To clear the flags in the status registers, write 1 to the corresponding bit in ADLIMGRSCR, ADLIMCHSCR0, ADLIMEXSCR.

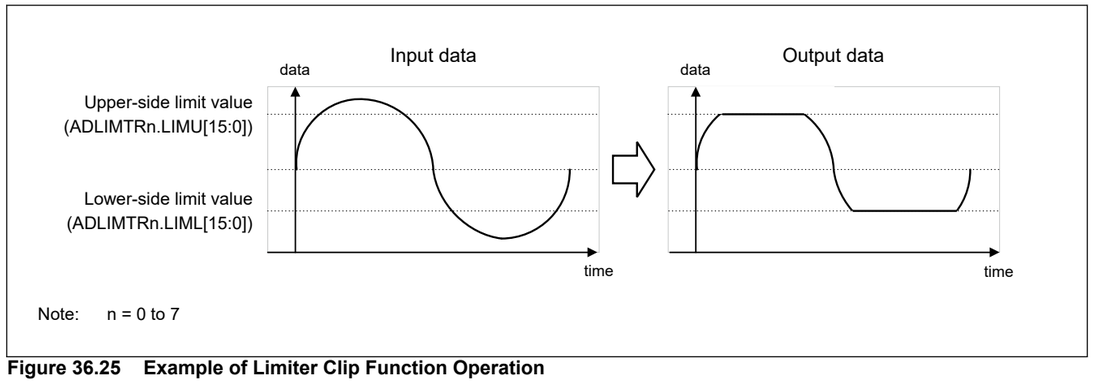


Figure 36.25 Example of Limiter Clip Function Operation

36.4.5 Data Formatting process

This process rounds and formats the A/D conversion data to the specified data format. The data processed in this process is stored to DATA[15:0] bits in A/D data register (ADDRi (i = 0 to 28)), Extended A/D data register (ADEXDRj (j = 0 to 2, 5 to 8)), and FIFO data register (ADFIFODRk (k = 0 to 8)) as the A/D conversion results.

Rounding and formatting of A/D conversion data is performed as the following based on ADDOPCRCn.ADPRC[1:0] (n = 0 to 36) bits setting.

- When 14-/12-/10-bit data format is selected (ADPRC[1:0] = 01b, 10b, 11b)
  - The lower bits are cut based on ADDOPCRCn.ADPRC[1:0] setting.
  - The most significant bit of the digit to be cut is rounded. (round down if 0, round up if 1)
- When 16-bit format is selected (ADPRC[1:0] = 00b)
  - Data length is not rounded.

For more details about the data format that has been processed by this process, refer to section 36.4.6. Data Format.

36.4.6 Data Format

The data format of the A/D conversion result stored to DATA[15:0] bits in A/D data register (ADDRi (i = 0 to 28)), Extended A/D data register (ADEXDRj (j = 0 to 2, 5 to 8)), and FIFO data register (ADFIFODRk (k = 0 to 8)) is described in the following.

Note: The A/D converter in ADC is the 12-bit A/D converter. When 16-bit or 14-bit data format is selected, the lower 4 bits or lower 2 bits of the A/D conversion result are extended bits for data processing. These bits are bit-extended and used internally for error calibration (Self-Calibration) of the A/D converter, User's Gain/offset adjusting function, and A/D-Converted Value Averaging Function.

Even if 16-bit or 14-bit data format is selected, the resolution and accuracy of the A/D converter is not guaranteed.

(1) 16-bits data length format

Table 36.19 shows the alignment of A/D conversion data on 16-bit data format. Figure 36.26 shows the data range for 16-bit data format.

For 16-bit data format, the analog input-voltage (VREFL0 to VREFH0) is A/D-converted within 0x0000 to 0xFFFF.

要清除状态寄存器中的标志，请将1写入ADLIMGRSCR、ADLIMCHSCR0、ADLIMEXSCR.

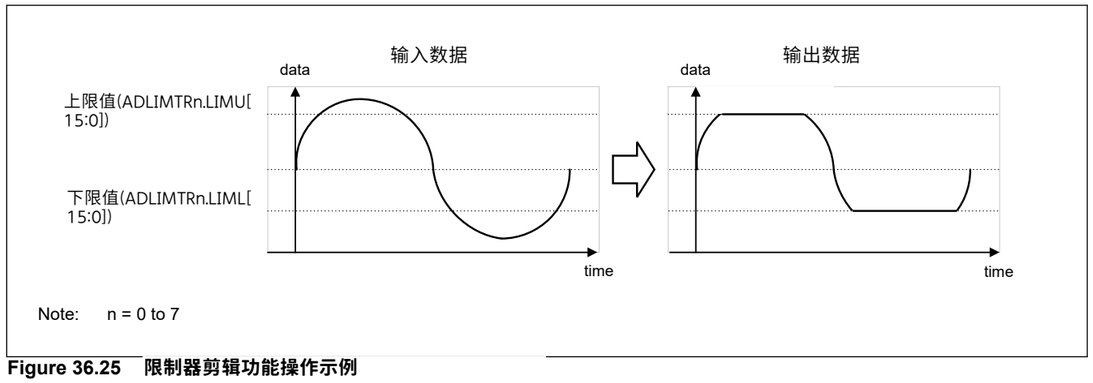


Figure 36.25 限制器剪辑功能操作示例

36.4.5 数据格式化过程

此过程将AD转换数据四舍五入并格式化为指定的数据格式。此过程中处理的数据存储到AD数据寄存器(ADDRi(i=0to28))、扩展AD数据寄存器(AdexDRj(j=0to2 5to8))中的DATA[15:0]位，和FIFO数据寄存器(AFIFODRk(k=0to8))作为AD转换结果。

基于ADDOPCRCn.ADPRC[1:0]（n=0到36）位设置，AD转换数据的舍入和格式化如下所示。

●选择14-12-10位数据格式（ADPRC[1：0]=01B，10B，11B）

根据ADDOPCRCn.ADPRC[1:0]设置切割低位。

要剪切的数字的最高位被四舍五入。（0向下取整，1向上取整）

●选择16位格式时(ADPRC[1:0]=00b)

数据长度未四舍五入。

关于该进程处理的数据格式的更多详细信息，请参见第36.4.6节。数据格式。

36.4.6 数据格式

AD转换结果的数据格式存储到AD数据寄存器(ADDRi(i=0to28))中的DATA[15:0]位，
扩展AD数据寄存器(ATEXDRj(j=0to2 5to8))和FIFO数据寄存器(AFIFODDRk(k=0to8))描述如下。

Note: ADC中的AD转换器是12位AD转换器。When16-bitor14-bitdataformatisselected thelower4bitsorlower2bitsoftheADconversionresultareextendedbitsfordataprocessing.这些位经过位扩展并在内部用于AD转换器的误差校准（自校准）、用户增益偏移调整功能和AD转换值平均功能。

即使选择16位或14位数据格式，也不能保证AD转换器的分辨率和精度。

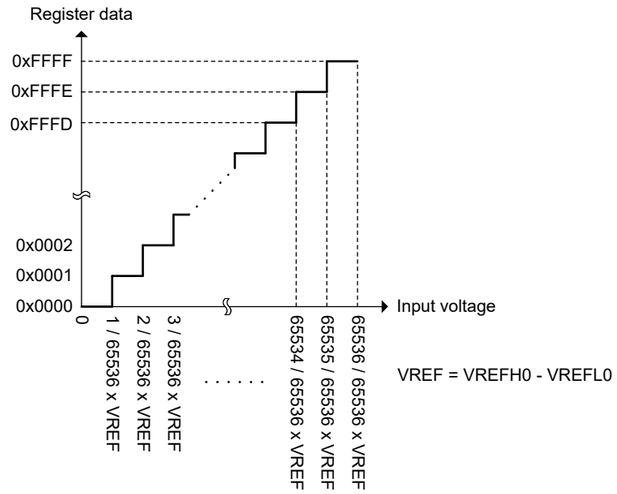
(1) 16位数据长度格式

表36.19显示了16位数据格式的AD转换数据的对齐方式。图36.26显示了16位数据格式的数据范围。

对于16位数据格式，模拟输入电压（VREFL0至VREFH0）在0x0000至0xFFFF范围内进行AD转换。

Table 36.19 Alignment of A/D Conversion Result Data (16-bit Data Length)

Bit position:	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Bit field:	DATA [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R



Note: This figure illustrates the case of the ideal A/D conversion characteristics.

Figure 36.26 Data range of A/D conversion result (16-bit data length)

(2) 14-bits data length format

Table 36.20 shows the alignment of A/D conversion data on 14-bit data format. Figure 36.27 shows the data range for 14-bit data format.

For 14-bit data format, the analog input-voltage (VREFL0 to VREFH0) is A/D-converted within 0x0000 to 0x3FFF.

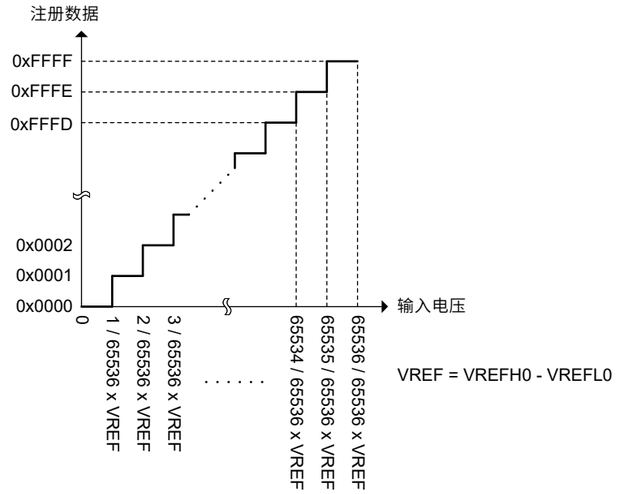
For 14-bit data length, the upper 2 bits (bit15 to bit14) are always 0.

Table 36.20 Alignment of A/D Conversion Result Data (14-bit Data Length)

Bit position:	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Bit field:	0	0	DATA[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.19 AD转换结果数据的对齐（16位数据长度）

Bit position:	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Bit field:	DATA [15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R



Note: 该图说明了理想AD转换特性的情况。

Figure 36.26 AD转换结果的数据范围（16位数据长度）

(2) 14位数据长度格式

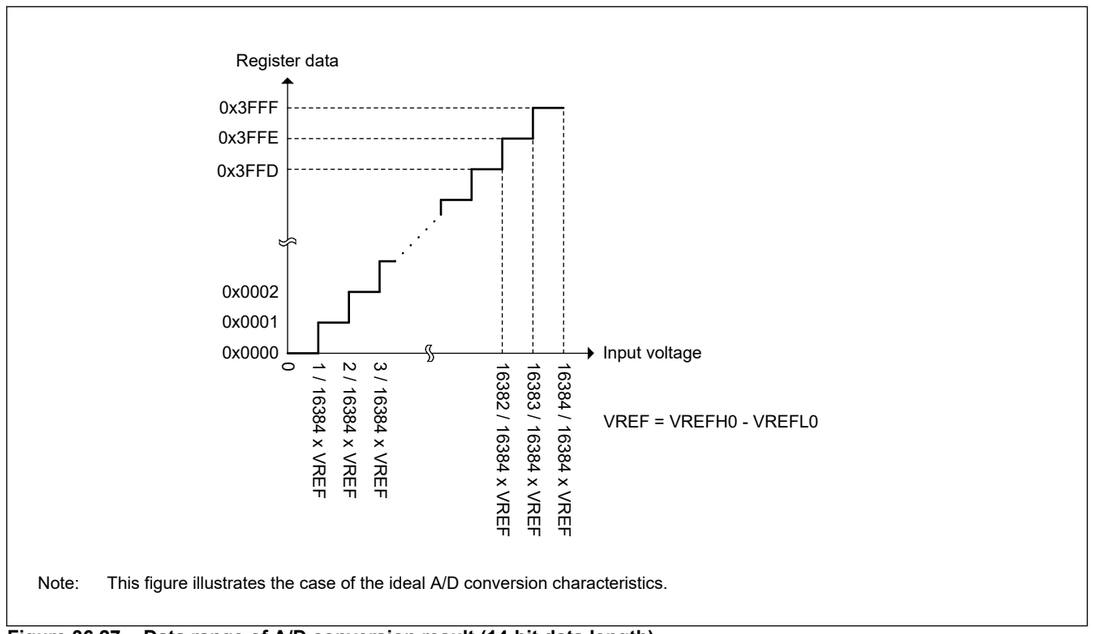
表36.20显示了AD转换数据在14位数据格式上的对齐方式。图36.27显示了14位数据格式的数据范围。

对于14位数据格式，模拟输入电压（VREFL0至VREFH0）在0x0000至0x3FFF范围内进行AD转换。

对于14位数据长度，高2位（bit15到bit14）始终为0。

Table 36.20 AD转换结果数据的对齐（14位数据长度）

Bit position:	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Bit field:	0	0	DATA[13:0]													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R



Note: This figure illustrates the case of the ideal A/D conversion characteristics.

Figure 36.27 Data range of A/D conversion result (14-bit data length)

(3) 12-bits data length format

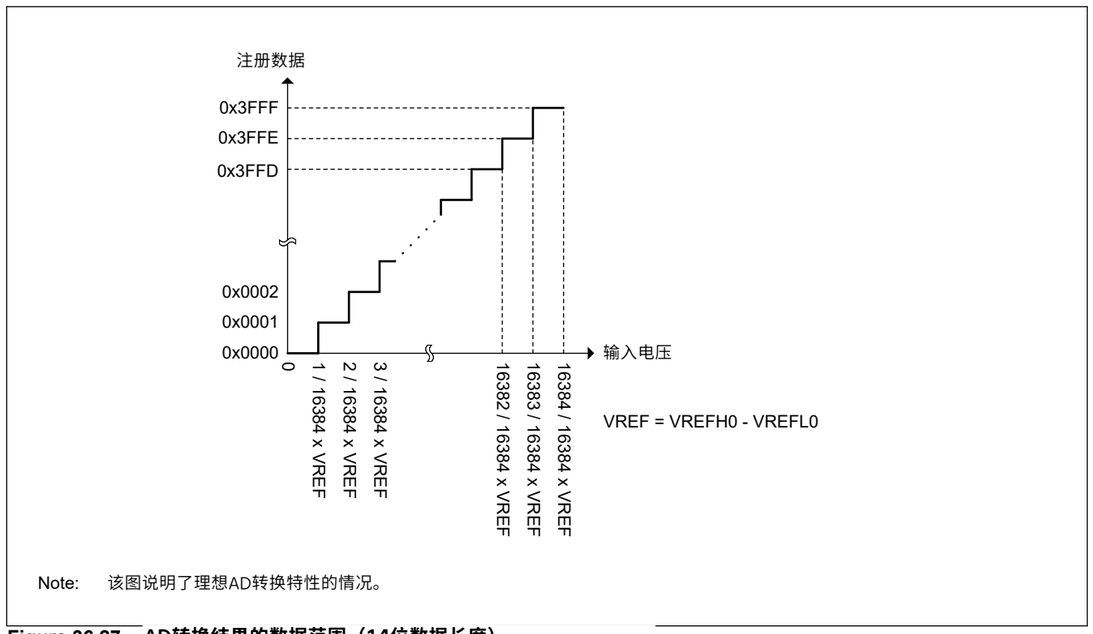
Table 36.21 shows the alignment of A/D conversion data on 12-bit data format. Figure 36.28 shows the data range for 12-bit data format.

For 12-bit data format, the analog input-voltage (VREFL0 to VREFH0) is A/D-converted within 0x0000 to 0x0FFF.

For 12-bit data length, the upper 4 bits (bit15 to bit12) are always 0.

Table 36.21 Alignment of A/D Conversion Result Data (12-bit Data Length)

Bit position:	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Bit field:	0	0	0	0	DATA[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R



Note: 该图说明了理想AD转换特性的情况。

Figure 36.27 AD转换结果的数据范围（14位数据长度）

(3) 12位数据长度格式

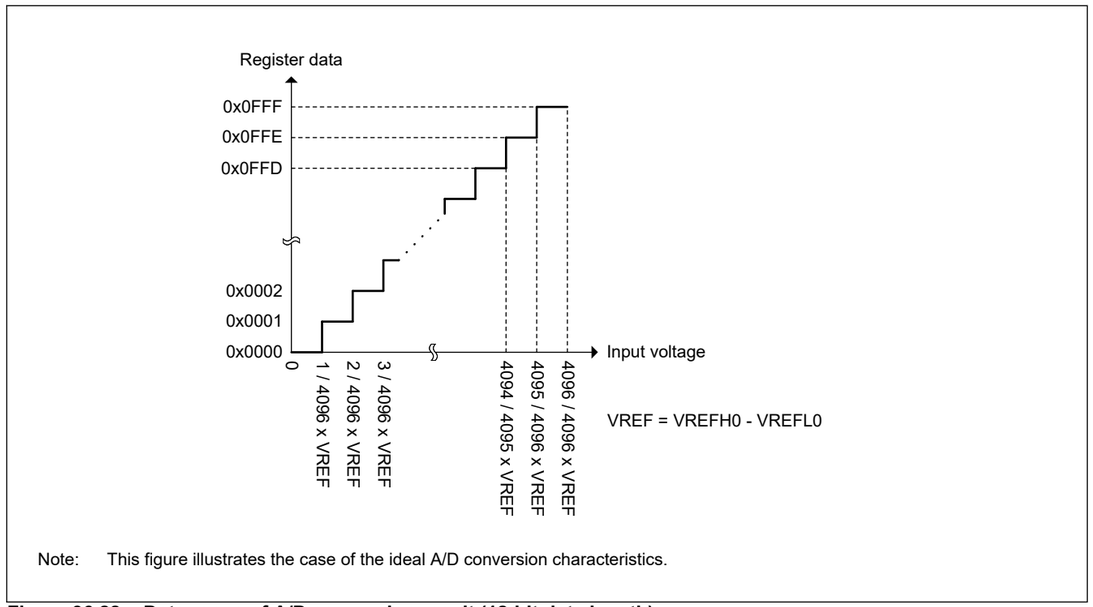
表36.21显示了AD转换数据在12位数据格式上的对齐方式。图36.28显示了12位数据格式的数据范围。

对于12位数据格式，模拟输入电压（VREFL0至VREFH0）在0x0000至0x0FFF范围内进行AD转换。

对于12位数据长度，高4位（bit15到bit12）始终为0。

Table 36.21 AD转换结果数据的对齐（12位数据长度）

Bit position:	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Bit field:	0	0	0	0	DATA[11:0]											
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R



Note: This figure illustrates the case of the ideal A/D conversion characteristics.

Figure 36.28 Data range of A/D conversion result (12-bit data length)

(4) 10-bits data length format

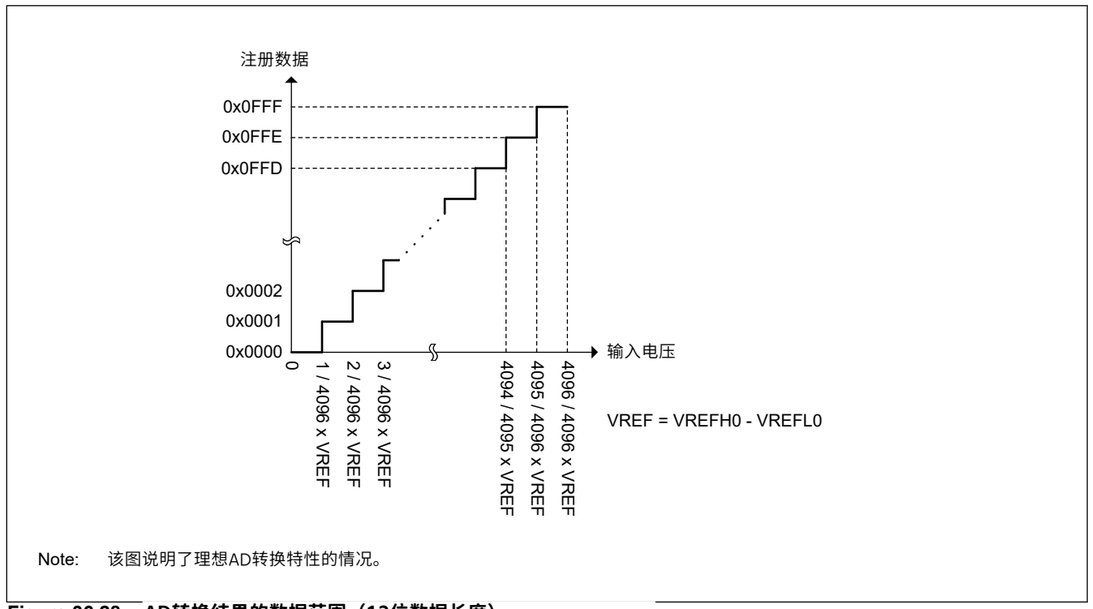
Table 36.22 shows the alignment of A/D conversion data on 10-bit data format. Figure 36.29 shows the data range for 10-bit data format.

For 10-bit data format, the analog input-voltage (VREFL0 to VREFH0) is A/D-converted within 0x0000 to 0x03FF.

For 10-bit data length, the upper 6 bits (bit15 to bit10) are always 0.

Table 36.22 Alignment of A/D Conversion Result Data (10-bit Data Length)

Bit position:	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Bit field:	0	0	0	0	0	0	DATA [9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R



Note: 该图说明了理想AD转换特性的情况。

Figure 36.28 AD转换结果的数据范围（12位数据长度）

(4) 10位数据长度格式

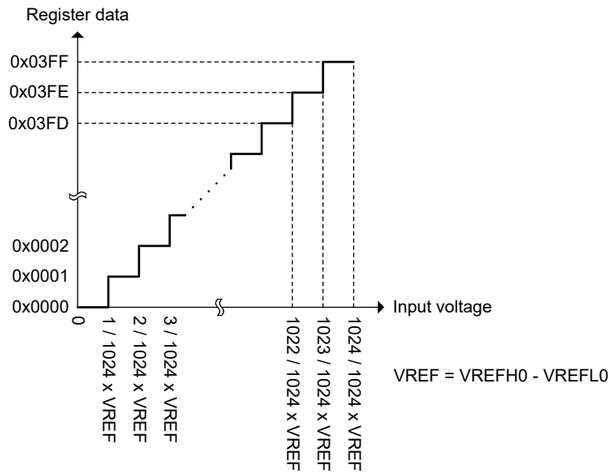
表36.22显示了10位数据格式的AD转换数据的对齐方式。图36.29显示了10位数据格式的数据范围。

对于10位数据格式，模拟输入电压（VREFL0至VREFH0）在0x0000至0x03FF范围内进行AD转换。

对于10位数据长度，高6位（bit15到bit10）始终为0。

Table 36.22 AD转换结果数据的对齐（10位数据长度）

Bit position:	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Bit field:	0	0	0	0	0	0	DATA [9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R



Note: This figure illustrates the case of the ideal A/D conversion characteristics.

Figure 36.29 Data range of A/D conversion result (10-bit data length)

36.4.7 Compare Match Function

36.4.7.1 Compare match

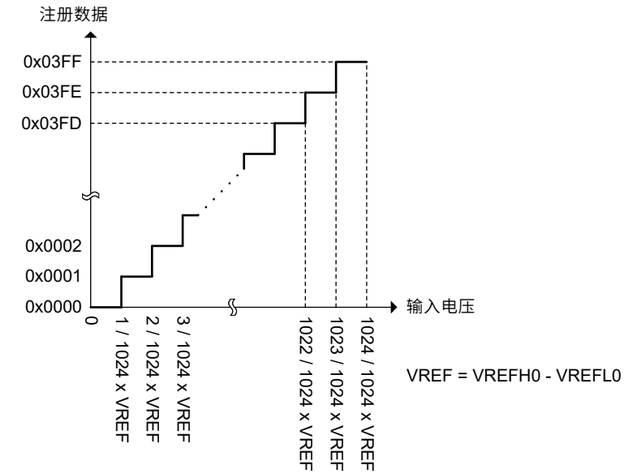
The compare match function compares the A/D conversion result with the reference value set in the compare match table register (ADCMPTBRn (n = 0 to 7). The compare match function compares the A/D conversion data after the data formatting process.

(1) Compare match mode

The comparison mode for detecting the compare match is selected in ADCMPMDRm.CMPMDn[1:0] (m = 0, 1. n = 0 to 7). The comparison mode can be selected from the following four modes.

1. Compare match is detected when the A/D conversion value is greater than or equal to the specified upper limit value.
2. Compare match is detected when the A/D conversion value is less than or equal to the specified lower limit.
3. Compare match is detected when the A/D conversion value is greater than or equal to the specified upper limit value, or less than or equal to the lower limit value.
4. Compare match is detected when the A/D conversion value is within the specified upper and lower limit values (when the value is lower than or equal to the upper limit value and greater than or equal to the lower limit value).

Figure 36.30 shows an example of compare match detection.



Note: 该图说明了理想AD转换特性的情况。

Figure 36.29 AD转换结果的数据范围（10位数据长度）

36.4.7 比较匹配函数

36.4.7.1 比较匹配

比较匹配功能将AD转换结果与比较匹配表寄存器(ADCMPTBRn(n=0to7))中设置的参考值进行比较。比较匹配 功能将经过数据格式化处理后的AD转换数据进行比较。

(1) 比较匹配模式

检测比较匹配的比较模式在ADCMPMDRm.CMPMDn[1:0](m=0 1.n=0to7)中选择。
比较模式可以从以下四种模式中选择。

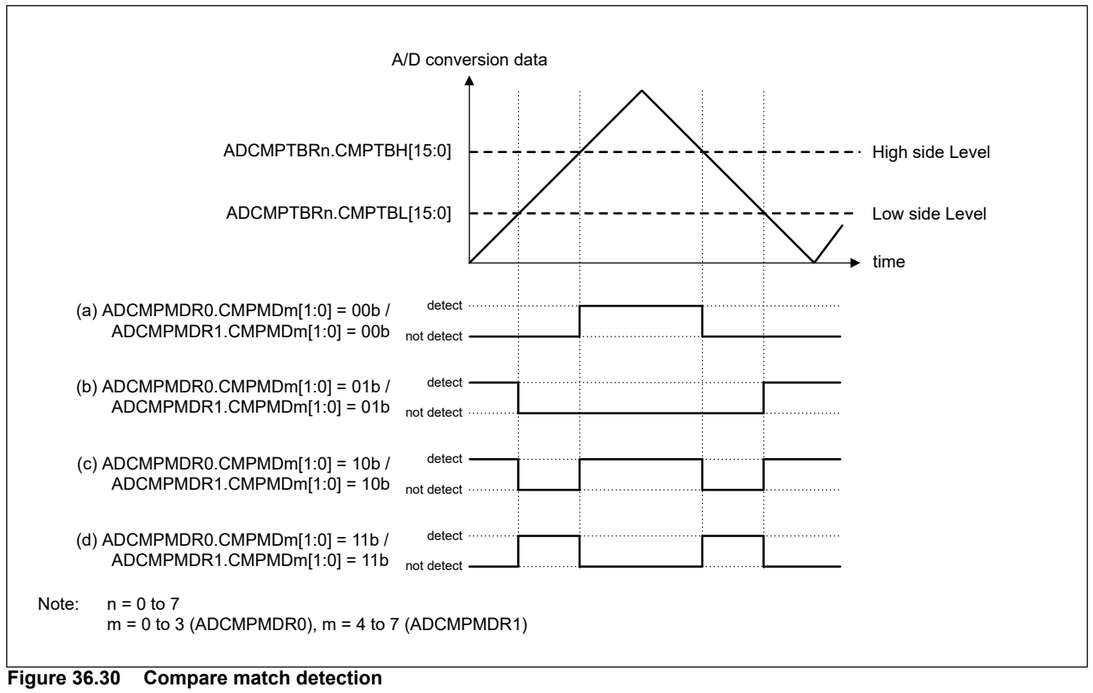
1.当AD转换值大于或等于指定的上限值时，检测到比较匹配。

2.当AD转换值小于或等于指定的下限时，检测到比较匹配。

3.当AD转换值大于或等于指定的上限值或小于或等于下限值时，检测到比较匹配。

4.当AD转换值在指定的上下限值范围内（小于等于上限值且大于等于下限值）时，检测到比较匹配。

图36.30显示了比较匹配检测的示例。



Note: n = 0 to 7
m = 0 to 3 (ADCMPMDR0), m = 4 to 7 (ADCMPMDR1)

Figure 36.30 Compare match detection

(2) Compare match detection

To use the compare match function, enable the compare match table used in ADCMPENR register, and select the compare match table in ADDOPCRBn.CMPTBLEm (n = 0 to 36, m = 0 to 7) for each virtual channel.

When A/D conversion is performed on a virtual channel for which the compare match function is enabled, a compare match is judged based on the A/D conversion result of its channel.

When a compare match is detected, the flags are set in the following status registers:

- ADCMPTBSR: The flag is set to the bit corresponding to the compare match table used when a compare match is detected.
- ADCMPCHSR0: The flag is set to the bit corresponding to the analog input channel that detected the compare match.
- ADCMPEXSR: The flag is set to the bit corresponding to Extended Analog Function where a compare match is detected.

To clear the flag of each status register, write 1 to the corresponding bit of ADCMPTBSCR, ADCMPCHSCR0, ADCMPEXSCR.

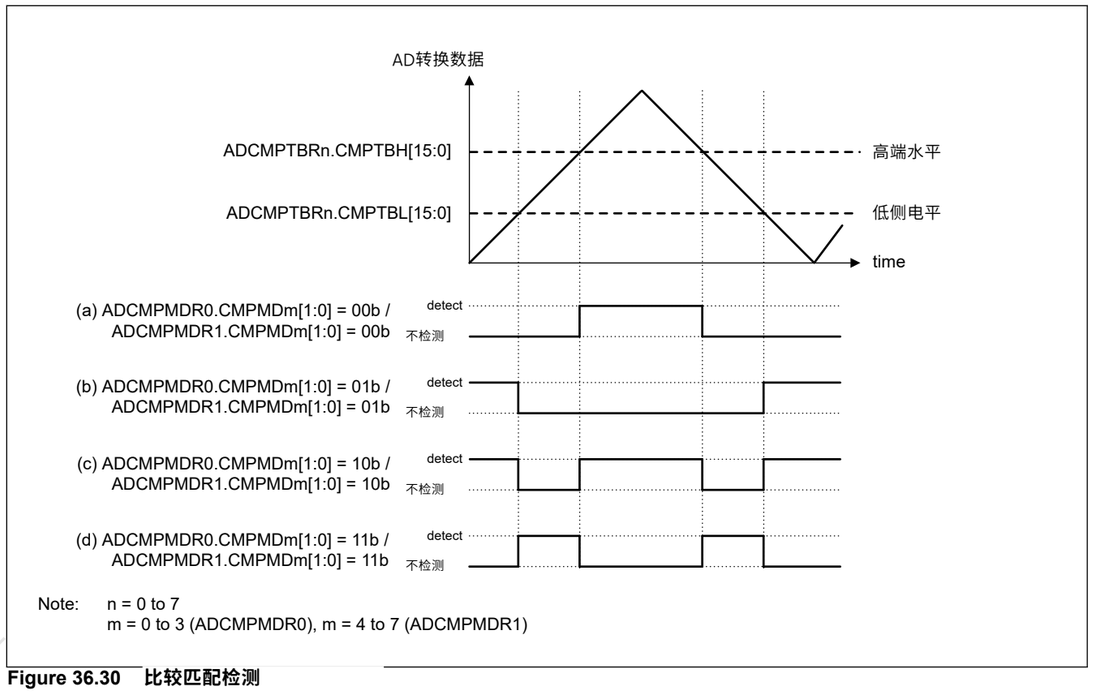
If Compare Match interrupt is enabled in ADCMPINTCR register and a compare match using compare match table 0 to 3 is detected, the corresponding interrupt is generated. Check the compare match of compare match table 4 to 7 in ADCMPTBSR register.

36.4.7.2 Composite Compare Match

The composite compare match function generates interrupts and ELC events by combining the comparison results of multiple compare match tables. The combination and condition of the compare match table for the composite compare match function is set in ADCCMPCR0 or ADCCMPCR1.

Composite Compare Match interrupt is generated when a compare match is detected that matches the specified condition.

Figure 36.31 shows the relationship between composite compare match and compare match function. Table 36.23 shows the relationship between the composite compare match function and the control register.



Note: n = 0 to 7
m = 0 to 3 (ADCMPMDR0), m = 4 to 7 (ADCMPMDR1)

Figure 36.30 比较匹配检测

(2) 比较匹配检测

要使用比较匹配功能，请启用ADCMPENR寄存器中使用的比较匹配表，并在ADDOPCRBn.CMPTBLEm（n=0到36，m=0到7）中为每个虚拟通道选择比较匹配表。

当对启用了比较匹配功能的虚拟通道进行AD转换时，将根据其通道的AD转换结果判断比较匹配。

当检测到比较匹配时，会在以下状态寄存器中设置标志：

●ADCMPTBSR：该标志设置为与检测到比较匹配时使用的比较匹配表对应的位。

●ADCMPCHSR0：该标志设置为与检测到比较匹配的模拟输入通道对应的位。

●ADCMPEXSR：该标志设置为与检测到比较匹配的扩展模拟功能对应的位。

要清除每个状态寄存器的标志，将1写入ADCMPTBSCR的相应位ADCMPCHSCR0，ADCMPEXSCR.

如果在ADCMPINTCR寄存器中使能了比较匹配中断，并且检测到使用比较匹配表0到3的比较匹配，则产生相应的中断。检查ADCMPTBSR寄存器中比较匹配表4到7的比较匹配。

36.4.7.2 复合比较匹配

复合比较匹配功能通过组合多个比较匹配表的比较结果来生成中断和ELC事件。复合比较匹配功能的比较匹配表的组合和条件在ADCCMPCR0或ADCCMPCR1中设置。

当检测到与指定条件匹配的比较匹配时，将产生复合比较匹配中断。

图36.31显示了复合比较匹配和比较匹配函数之间的关系。表36.23显示了复合比较匹配函数和控制寄存器之间的关系。

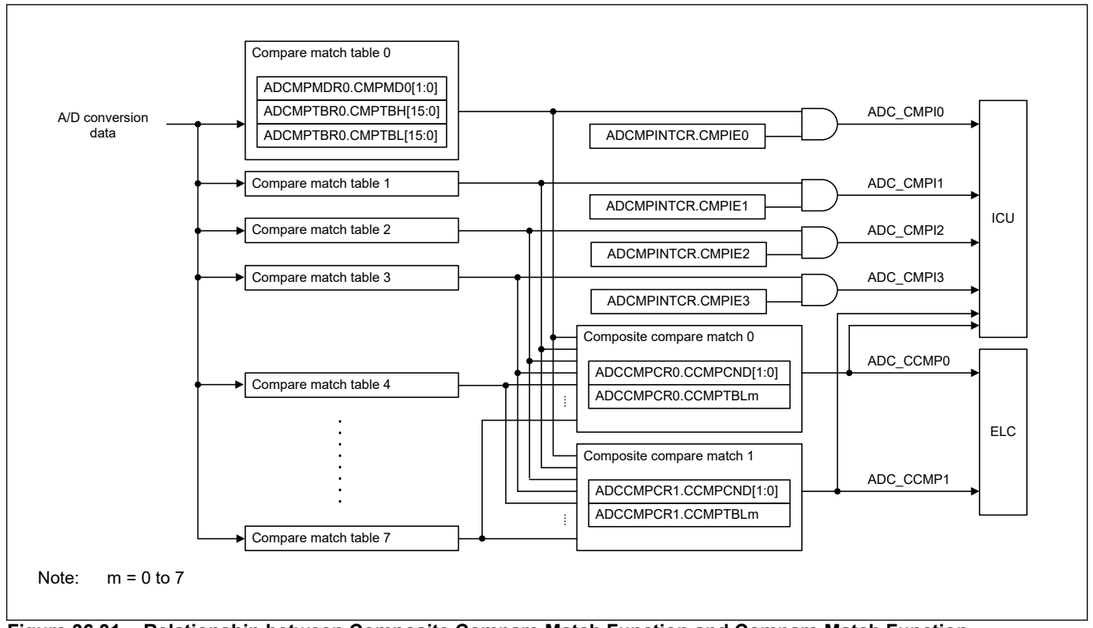


Figure 36.31 Relationship between Composite Compare Match Function and Compare Match Function

Table 36.23 Composite compare match and control register

Function name	Enable composite compare function	Composite compare mode selection	Composite compare match interrupt
Composite compare match 0	ADCMPCR0.CMPTBmSEL0 (m = 0 to 7)	ADCMPCR0.CMPITYPE0[1:0]	ADC_CCMPM0
Composite compare match 1	ADCMPCR1.CMPTBmSEL1 (m = 0 to 7)	ADCMPCR1.CMPITYPE1[1:0]	ADC_CCMPM1

36.4.8 Data Registers

A/D data register (ADDRi (i = 0 to 28)) and Extended A/D data register (ADEXDRj (j = 0 to 2, 5 to 8)) store the A/D conversion data of the analog channels corresponding to each register. These registers are updated (overwritten) when A/D conversion for the analog channel corresponding to each register is completed.

36.4.9 FIFO Function

FIFO consists of 8-stage registers and can hold up to 8 A/D conversion data. One FIFO is implemented for each scan group. The A/D conversion data stored in FIFO can be read from ADFIFODRn register (n = 0 to 8).

FIFO acts as a ring buffer. Writing and reading A/D conversion data to and from FIFO is controlled by the write pointer and read pointer inside FIFO. The block diagram of FIFO is shown in Figure 36.32.

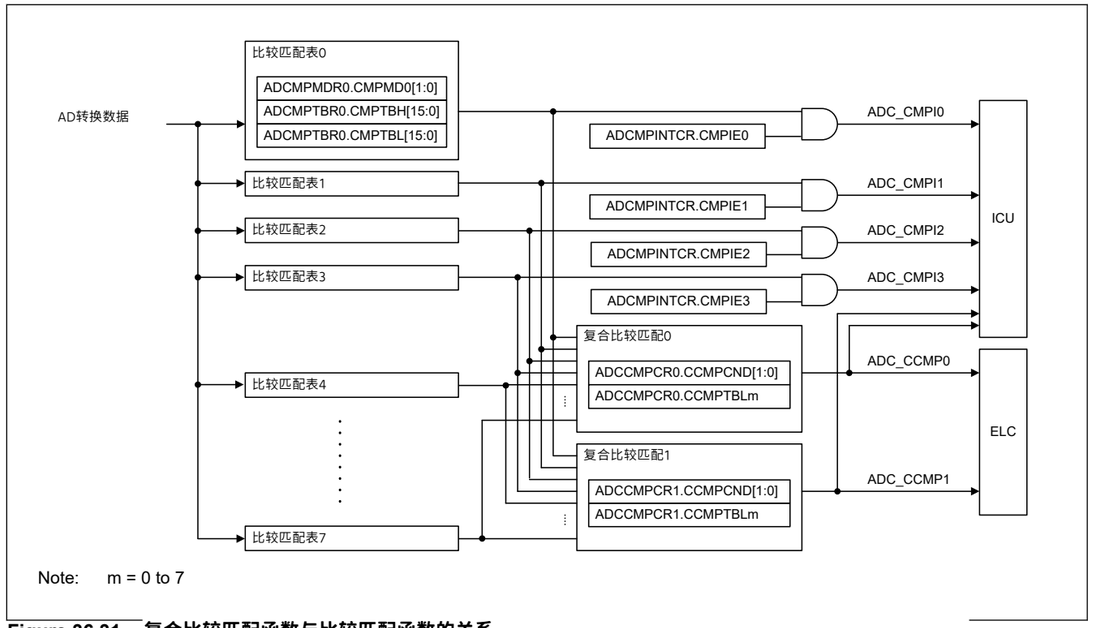


Figure 36.31 复合比较匹配函数与比较匹配函数的关系

Table 36.23 复合比较匹配和控制寄存器

函数名称	启用复合比较功能	复合比较模式选择	复合比较匹配中断
复合比较匹配0	ADCMPCR0.CMPTBmSEL0 (m = 0 to 7)	ADCMPCR0.CMPITYPE0[1:0]	ADC_CCMPM0
复合比较匹配1	ADCMPCR1.CMPTBmSEL1 (m = 0 to 7)	ADCMPCR1.CMPITYPE1[1:0]	ADC_CCMPM1

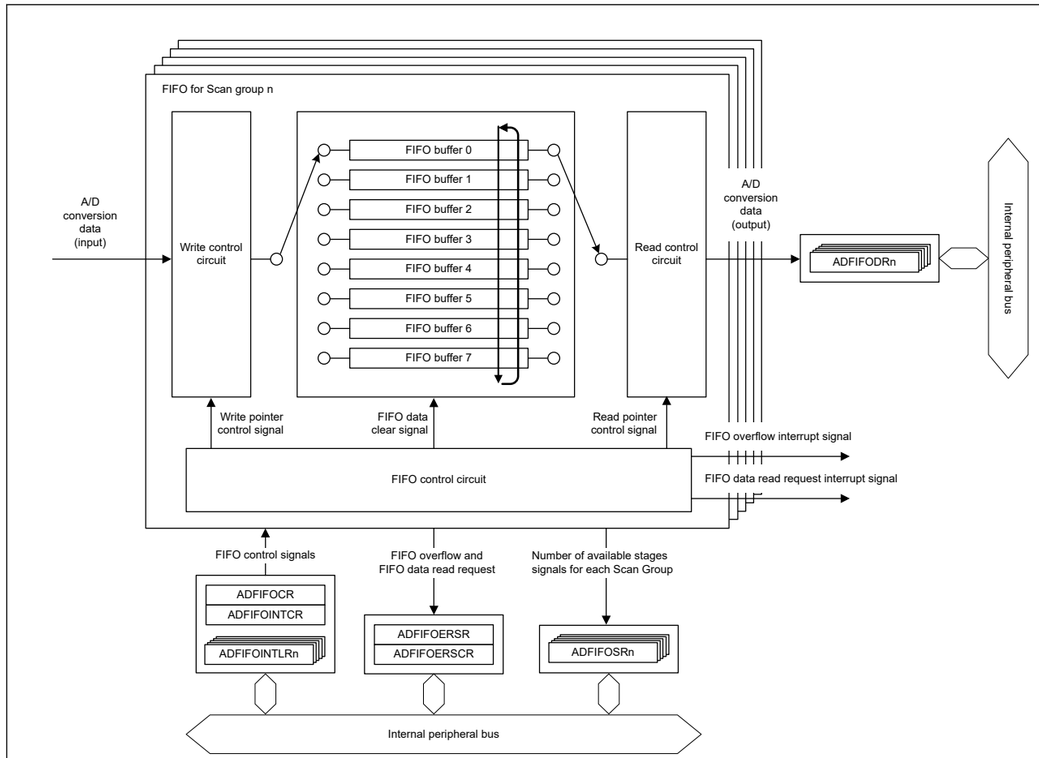
36.4.8 数据寄存器

AD数据寄存器(ADDRi(i=0到28))和扩展AD数据寄存器(ADXDRj(j=0到2 5到8))存储每个寄存器对应的模拟通道的AD转换数据。当每个寄存器对应的模拟通道的AD转换完成时，这些寄存器将被更新（覆盖）。

36.4.9 FIFO Function

FIFO由8级寄存器组成，最多可保存8个AD转换数据。每个扫描组实现一个FIFO。
存储在FIFO中的AD转换数据可以从ADFIFODRn寄存器（n=0到8）中读取。

FIFO充当环形缓冲区。向FIFO写入和读取AD转换数据由FIFO内部的写指针和读指针控制。FIFO的框图如图36.32所示。



Note: n = 0 to 8

Figure 36.32 The block diagram of FIFO

36.4.9.1 Operation when A/D conversion data is read from FIFO

The A/D conversion data is stored sequentially to the register pointed by the write pointer. When A/D conversion data is written to a register in FIFO, the write pointer is switched to the next register. (Write pointer value is increased 1). At this time, the number of available stages (ADFIFOSRm.FIFOSTn[3:0] (m = 0 to 4, n = 0 to 8) bits) is decreased 1.

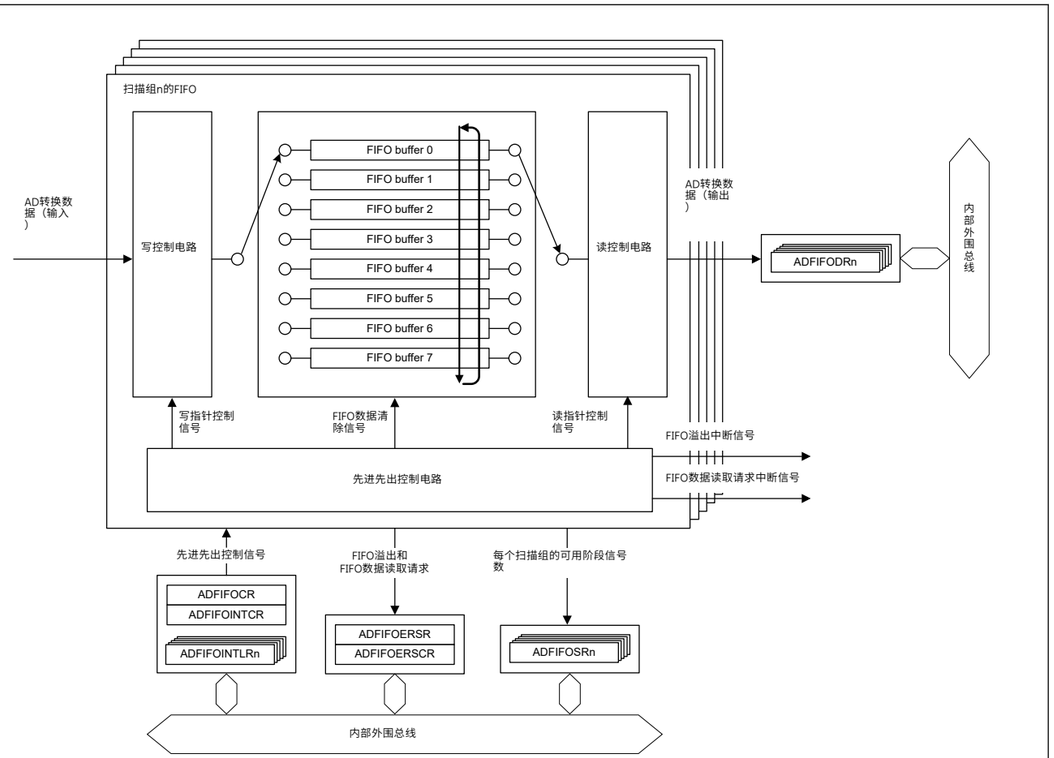
A FIFO overflow occurs when ADFIFOSRm.FIFOSTn[3:0] bits are 0000b and an additional A/D conversion data is written to FIFO. When a FIFO overflow occurs, the A/D converter data is not written and the write pointer does not change.

36.4.9.2 Operation when A/D conversion data is read from FIFO

When A/D conversion data is read from FIFO data register (ADFIFODRn (n = 0 to 8)), the data in the register pointed to by FIFO read pointer is read. When A/D conversion data is read from FIFO, the read pointer is switched to the next register (the read pointer is increased 1). At this time, the number of available stages in FIFO (ADFIFOSRm.FIFOSTn[3:0] (m = 0 to 4, n = 0 to 8) bits) is increased 1.

If FIFO is empty (ADFIFOSRm.FIFOSTn[3:0] bits are 1111b) and the reading from the FIFO is occurred, an invalid data is read. (If FIFO is read after a reset or after FIFO data is cleared, 0x00000000 is read. If data had been written to register in FIFO, the previous data is read.) In addition, the read pointer does not change in the read operation when FIFO is empty.

Read A/D conversion data from FIFO data register (ADFIFODRn) by 32-bit access. For more details, refer to section 36.4.9.5. Usage Notes on FIFO.



Note: n = 0 to 8

Figure 36.32 先进先出的框图

36.4.9.1 从FIFO读取AD转换数据时的操作

AD转换数据依次存储到写指针指向的寄存器中。当AD转换数据写入FIFO中的一个寄存器时，写指针切换到下一个寄存器。（写指针值增加1）。此时，可用级数（ADFIFOSRm.FIFOSTn[3:0]（m=0到4，n=0到8）位）减少1。

当ADFIFOSRm.FIFOSTn[3:0]位为0000b且额外的AD转换数据写入FIFO时，发生FIFO溢出。当发生FIFO溢出时，AD转换器数据不被写入，写指针也不改变。

36.4.9.2 从FIFO读取AD转换数据时的操作

当从FIFO数据寄存器(ADFIFODRn(n=0to8))读取AD转换数据时，寄存器中的数据由FIFO读指针被读取。当从FIFO中读取AD转换数据时，读指针切换到下一个寄存器（读指针加1）。此时，FIFO（ADFIFOSRm.FIFOSTn[3:0]（m=0到4，n=0到8）位）中的可用级数增加1。

如果FIFO为空（ADFIFOSRm.FIFOSTn[3:0]位为1111b）并且发生从FIFO的读取，则读取无效数据。（如果在复位或清除FIFO数据后读取FIFO，则读取0x00000000。如果数据已写入FIFO中的寄存器，则读取之前的数据。）此外，在读取操作时读取指针不会改变FIFO为空。

通过32位访问从FIFO数据寄存器(ADFIFODRn)读取AD转换数据。有关详细信息，请参阅第36.4.9.5节。关于FIFO的使用说明。

36.4.9.3 FIFO data read request and overflow

When A/D conversion data is written to or read from FIFO, the write pointer or read pointer changes. Depending on the state of the write pointer and the read pointer, the number of available stages in FIFO is reflected in ADFIFOSRm.FIFOSTn[3:0] (m = 0 to 4, n = 0 to 8).

FIFO data read request flag is set (ADFIFOERSR.FIFOFLFn = 1) when the number of available stages become less than or equal to the value specified in ADFIFOINTLRm.FIFOLVn[3:0] (m = 0 to 4, n = 0 to 8) bit. If a FIFO data read request occurs, FIFO data read request interrupt can be generated.

When FIFO is full (ADFIFOSRm.FIFOSTn[3:0] bits are 0000b) and additional A/D converter data are written, FIFO overflow error flag is set (ADFIFOERSROOEOOVFn = 1). If a FIFO overflow occurs, FIFO data overflow interrupt can be generated.

36.4.9.4 Clearing FIFO data

The data stored in the registers in FIFO can be cleared by writing to ADFIFODCR.FIFODCn (n = 0 to 8) bit. When writing 1 to ADFIFODCR.FIFODCn bit, the registers, read pointer, and write pointer in FIFO of the scan group corresponding to FIFODCn bit are initialized. Clearing FIFO data should be performed while A/D conversion is not being performed.

36.4.9.5 Usage Notes on FIFO

Reading the A/D conversion data from the FIFO data register (ADFIFODRn (n = 0 to 8)) should be performed with a single 32-bit access; access to each bit of ADFIFODRn, 16-bit read access, and 8-bit read access are prohibited.

Whenever a 32-bit read access is performed from the internal bus to ADFIFODRn, the FIFO reads out the data and changes the FIFO read pointer. If reading access to each bit of ADFIFODRn is performed, the read pointer may advance unintentionally, resulting in loss of A/D conversion data. Also, if 16-bit or 8-bit access is performed, the read pointer will not change and correct data may not be read.

36.4.10 A/D Conversion Data Error detection

The ERR bit in A/D data register (ADDRi (i = 0 to 28)), Extended A/D data register (ADEXDRj (j = 0 to 2, 5 to 8)), and FIFO data register (ADFIFODRk (k = 0 to 8)) is a flag that indicates an A/D conversion data error. An A/D conversion data error indicates that an invalid A/D conversion data has been detected. If an A/D conversion data error occurs (ERR = 1), the A/D conversion data cannot be guaranteed.

A/D conversion data error is generated by the following factors.

- A/D converter error
- A/D conversion overflow

For more details about these errors, refer to section 36.6. Error Detection.

36.5 Start and Stop control of A/D conversion

36.5.1 Software Trigger

A/D conversion of scan group n can be started by writing 1 to ADSTRn.ADST (n = 0 to 8) bit or ADSYSTR.ADSYSTn (n = 0 to 8) bit.

ADSTRn.ADST bit is used to start A/D conversion individually for each scan group. ADSYSTR.ADSYSTn bit is used to start A/D conversion on the scan group assigned to ADC0 or ADC1 at the same time.

Except when Group Priority Operation, if ADC0 or ADC1 is already performing A/D conversion operation for a scan group, writing to ADSTRn.ADST bit or ADSYSTR.ADSYSTn bit to an another scan group that uses that A/D converter is ignored.

36.5.2 Peripheral module Triggers

A/D conversion can be started by triggers from the peripheral modules listed in the followings.

- ELC Trigger
- GPT Trigger

36.4.9.3 FIFO数据读取请求和溢出

当AD转换数据写入FIFO或从FIFO读取时，写指针或读指针会发生变化。根据写指针和读指针的状态，FIFO中可用的级数反映在ADFIFOSRm.FIFOSTn[3:0]（m=0到4，n=0到8）中。

当可用阶段数小于或等于ADFIFOINTLRm.FIFOLVn[3:0]（m=0到4，n=0到8）中指定的值时，设置FIFO数据读取请求标志(ADFIFOERSR.FIFOFLFn=1)）少量。如果发生FIFO数据读取请求，则会产生FIFO数据读取请求中断。

当FIFO已满（ADFIFOSRm.FIFOSTn[3:0]位为0000b）并写入额外的AD转换器数据时，设置FIFO溢出错误标志（ADFIFOERSROOEOOVFn=1）。如果发生FIFO溢出，会产生FIFO数据溢出中断。

36.4.9.4 清除FIFO数据

FIFO寄存器中存储的数据可以通过写入ADFIFODCR.FIFODCn(n=0to8)位来清除。当向ADFIFODCR.FIFODCn位写入1时，初始化FIFODCn位对应的扫描组的FIFO中的寄存器、读指针和写指针。未执行AD转换时应执行清除FIFO数据。

36.4.9.5 先进先出的使用说明

从FIFO数据寄存器(AFIFODRn(n=0to8))读取AD转换数据应使用单个32位访问；禁止访问ADFIFODRn的每一位、16位读访问和8位读访问。

每当从内部总线对AFIFODRn执行32位读取访问时，FIFO都会读取数据并更改FIFO读取指针。如果对ADFIFODDRn的每一位进行读访问，读指针可能会意外前进，导致AD转换数据丢失。此外，如果执行16位或8位访问，则读指针不会改变，并且可能无法读取正确的数据。

36.4.10 AD转换数据错误检测

AD数据寄存器(ADDRi(i=0to28))、扩展AD数据寄存器(AdexDRj(j=0to2 5to8))中的ERR位，以及FIFO数据寄存器(ADFIFODRk(k=0to8))是指示AD转换数据错误的标志。AD转换数据错误表示检测到无效的AD转换数据。如果发生AD转换数据错误(ERR=1)，则无法保证AD转换数据。

D转换数据错误由以下因素产生。

- ●AD转换器错误
- ●AD转换溢出

有关这些错误的更多详细信息，请参阅第36.6节。错误检测。

36.5 AD转换的启动和停止控制

36.5.1 软件触发

可以通过将1写入ADSTRn.ADST（n=0到8）位或ADSYSTR.ADSYSTn（n=0到8）位来启动扫描组n的D转换。

ADSTRn.ADST位用于为每个扫描组单独启动AD转换。ADSYSTR.ADSYSTn位用于同时启动分配给ADC0或ADC1的扫描组的AD转换。

除组优先操作外，如果ADC0或ADC1已经对一个扫描组执行AD转换操作，则忽略向另一个使用该AD转换器的扫描组写入ADSTRn.ADST位或ADSYSTR.ADSYSTn位。

36.5.2 外设模块触发器

D转换可以通过来自下列外围模块的触发器来启动。

- ELC Trigger
- GPT Trigger

- External Trigger (I/O port)

To perform A/D conversion by a trigger from a peripheral module, configure the trigger for each scan group and enable the trigger input from the peripheral module in ADTRGENR register.

36.5.2.1 ELC Trigger

A/D conversion can be started by an event (ELC event) from Event Link Controller. To start A/D conversion using an ELC event, configure the scan group using the ELC event in ADTRGELCn (n = 0 to 8) register and enable the A/D conversion start trigger in ADTRGENR register. Table 36.24 shows the correspondence between ADTRGELCn register and ELC event.

Table 36.24 Correspondence between ELC Trigger Enable Register and ELC Event

Resister bit	Event Name
ADTRGELCn.TRGELC0	ELC_AD00
ADTRGELCn.TRGELC1	ELC_AD01
ADTRGELCn.TRGELC2	ELC_AD02
ADTRGELCn.TRGELC3	ELC_AD10
ADTRGELCn.TRGELC4	ELC_AD11
ADTRGELCn.TRGELC5	ELC_AD12

Note: n = 0 to 8

36.5.2.2 GPT Trigger

A/D conversion can be started by an interrupt source from the general-purpose PWM Timer (GPT). To start A/D conversion using an interrupt source from the GPT, configure the scan group using the GPT interrupt source in ADTRGGPTn (n = 0 to 8) register and enable the A/D conversion start trigger in ADTRGENR register. Table 36.25 shows the correspondence between ADTRGGPTn register and GPT interrupt sources.

Table 36.25 Correspondence between GPT Trigger Enable Registers and GPT Interrupt Sources (1 of 2)

Resister bit	Event Name
ADTRGGPTn.TRGGPTA0	GPT0_ADTRGA
ADTRGGPTn.TRGGPTA1	GPT1_ADTRGA
ADTRGGPTn.TRGGPTA2	GPT2_ADTRGA
ADTRGGPTn.TRGGPTA3	GPT3_ADTRGA
ADTRGGPTn.TRGGPTA4	GPT4_ADTRGA
ADTRGGPTn.TRGGPTA5	GPT5_ADTRGA
ADTRGGPTn.TRGGPTA6	GPT6_ADTRGA
ADTRGGPTn.TRGGPTA7	GPT7_ADTRGA
ADTRGGPTn.TRGGPTA8	GPT8_ADTRGA
ADTRGGPTn.TRGGPTA9	GPT9_ADTRGA
ADTRGGPTn.TRGGPTB0	GPT0_ADTRGB
ADTRGGPTn.TRGGPTB1	GPT1_ADTRGB
ADTRGGPTn.TRGGPTB2	GPT2_ADTRGB
ADTRGGPTn.TRGGPTB3	GPT3_ADTRGB
ADTRGGPTn.TRGGPTB4	GPT4_ADTRGB
ADTRGGPTn.TRGGPTB5	GPT5_ADTRGB
ADTRGGPTn.TRGGPTB6	GPT6_ADTRGB
ADTRGGPTn.TRGGPTB7	GPT7_ADTRGB
ADTRGGPTn.TRGGPTB8	GPT8_ADTRGB

●外部触发（IO端口）

要通过来自外设模块的触发执行AD转换，请为每个扫描组配置触发，并在ADTRGENR寄存器中启用来自外设模块的触发输入。

36.5.2.1 ELC Trigger

D转换可以通过来自EventLinkController的事件（ELC事件）启动。要使用ELC事件启动AD转换，请使用ADTRGELCn(n=0至8)寄存器中的ELC事件配置扫描组，并在ADTRGENR寄存器中启用AD转换启动触发器。ADTRGELCn寄存器与ELC事件的对应关系如表36.24所示。

Table 36.24 ELC触发使能寄存器与ELC事件的对应关系

电阻位	活动名称
ADTRGELCn.TRGELC0	ELC_AD00
ADTRGELCn.TRGELC1	ELC_AD01
ADTRGELCn.TRGELC2	ELC_AD02
ADTRGELCn.TRGELC3	ELC_AD10
ADTRGELCn.TRGELC4	ELC_AD11
ADTRGELCn.TRGELC5	ELC_AD12

Note: n = 0 to 8

36.5.2.2 GPT Trigger

D转换可由通用PWM定时器(GPT)的中断源启动。要使用来自GPT的中断源启动AD转换，请使用ADTRGGPTn(n=0至8)寄存器中的GPT中断源配置扫描组，并在ADTRGENR寄存器中启用AD转换启动触发器。ADTRGGPTn寄存器与GPT中断源的对应关系如表36.25所示。

Table 36.25 GPT触发使能寄存器和GPT中断源之间的对应关系(1of2)

电阻位	活动名称
ADTRGGPTn.TRGGPTA0	GPT0_ADTRGA
ADTRGGPTn.TRGGPTA1	GPT1_ADTRGA
ADTRGGPTn.TRGGPTA2	GPT2_ADTRGA
ADTRGGPTn.TRGGPTA3	GPT3_ADTRGA
ADTRGGPTn.TRGGPTA4	GPT4_ADTRGA
ADTRGGPTn.TRGGPTA5	GPT5_ADTRGA
ADTRGGPTn.TRGGPTA6	GPT6_ADTRGA
ADTRGGPTn.TRGGPTA7	GPT7_ADTRGA
ADTRGGPTn.TRGGPTA8	GPT8_ADTRGA
ADTRGGPTn.TRGGPTA9	GPT9_ADTRGA
ADTRGGPTn.TRGGPTB0	GPT0_ADTRGB
ADTRGGPTn.TRGGPTB1	GPT1_ADTRGB
ADTRGGPTn.TRGGPTB2	GPT2_ADTRGB
ADTRGGPTn.TRGGPTB3	GPT3_ADTRGB
ADTRGGPTn.TRGGPTB4	GPT4_ADTRGB
ADTRGGPTn.TRGGPTB5	GPT5_ADTRGB
ADTRGGPTn.TRGGPTB6	GPT6_ADTRGB
ADTRGGPTn.TRGGPTB7	GPT7_ADTRGB
ADTRGGPTn.TRGGPTB8	GPT8_ADTRGB

Table 36.25 Correspondence between GPT Trigger Enable Registers and GPT Interrupt Sources (2 of 2)

Resister bit	Event Name
ADTRGGPTn.TRGGPTB9	GPT9_ADTRGB

Note: n = 0 to 8

36.5.2.3 External Trigger

A/D conversion can be started by the input from the external trigger pin (ADTRG0 and ADTRG1). To start A/D conversion using an external trigger, configure the scan group using the external trigger in ADTRGEXTn (n = 0 to 8) register and enable the A/D conversion start trigger in ADTRGENR register.

External trigger is active low. Therefore, before using an external trigger (ADTRG0 and ADTRG1), configure the I/O port and input the High level to the external trigger pin.

36.5.3 Trigger Delay

The trigger delay function adds a delay to the A/D conversion start trigger in order to adjust the A/D conversion start timing for each scan group. This function adds a delay to the internal trigger for each scan group generated by accepting an external trigger, ELC trigger or GPT trigger. This function cannot be used to add a delay to a software trigger.

The delay value to be added to the internal trigger is set for each scan group in ADTRGDLRi (i = 0 to 4) register. The delay value to be added is the register setting value × A/D Conversion clock (ADCLK) cycle.

36.5.4 Force stops the A/D conversion operation

The scanning operation of the A/D converter can be forcibly stopped by writing 1 to ADSTOPR.ADSTOPm (m = 0, 1) bit during scanning operation. If the scanning operation is forcibly stopped, the A/D conversion data is not guaranteed.

36.5.4.1 Forced stop procedure

Table 36.26 shows the procedure for forced stop of A/D conversion operation. Observe Table 36.26 when performing the forced stop. If this procedure is violated, the A/D converter may not be able to stop and then it may not operate normally. In that case, a reset is required for recovery.

Table 36.26 Procedure for Forced Stop of A/D conversion operation

No.	Step Name	Description
1	Disable trigger input	Disables the trigger input from the peripheral module. (Write ADTRGENR.STTRGENn = 0)
2	Waiting time	After setting the above Step 1, a wait time is required to safely stop the A/D converter. Proceed to the next processing after the specified waiting time has elapsed. For details on the wait time, refer to section 36.5.4.2. Waiting time after disabling trigger input for forced stop processing.
3	Checking the A/D converter status	Check if the A/D converter is operating after the waiting time of the above Step 2 has elapsed. If the A/D converter is running (ADSR.ADACTm = 1), proceed to Step 4. If the A/D converter is stopped (ADSR.ADACTm = 0), no further processing is required (proceed to Step 6).
4	Forced stop of A/D converter	Forcibly stop the A/D converter by ADSTOPR register. *1 (Write ADSTOPR.ADSTOPm = 1)
5	Waiting for A/D converter to stop	Wait until the A/D converter stops. (ADSR.ADACTm = 0)
6	End	Processing of forced stop is completed.

Note: m = 0, 1, n = 0 to 8
Do not write to ADSYSTR register or ADSTRn register while this forced stop procedure is in progress.
Note 1. Forced stopping during Self-Calibration operation is prohibited. For more details, refer to section 36.3.6. Self-Calibration.

36.5.4.2 Waiting time after disabling trigger input for forced stop processing

In the forced stop procedure shown in Table 36.26, after disabling the trigger input from the peripheral module, a wait time is required to perform the forced stop (Step 2 of Table 36.26). This wait time is the time that must be secured to perform a forced stop safely.

Table 36.25 GPT触发使能寄存器和GPT中断源之间的对应关系(2of2)

电阻位	活动名称
ADTRGGPTn.TRGGPTB9	GPT9_ADTRGB

Note: n = 0 to 8

36.5.2.3 外部触发

通过来自外部触发引脚（ADTRG0和ADTRG1）的输入可以启动D转换。要使用外部触发启动AD转换，请使用ADTRGEXTn(n=0至8)寄存器中的外部触发配置扫描组，并在ADTRGENR寄存器中启用AD转换启动触发。

外部触发低电平有效。因此，在使用外部触发（ADTRG0和ADTRG1）之前，配置IO端口并将高电平输入到外部触发引脚。

36.5.3 触发延迟

触发延迟功能将延迟添加到AD转换开始触发，以便调整每个扫描组的AD转换开始时序。此功能为通过接受外部触发、ELC触发或GPT触发而生成的每个扫描组的内部触发添加延迟。此功能不能用于向软件触发添加延迟。

在ADTRGDLRi(i=0to4)寄存器中为每个扫描组设置要添加到内部触发的延迟值。要添加的延迟值是寄存器设置值×AD转换时钟(ADCLK)周期。

36.5.4 强制停止AD转换操作

在扫描操作期间，通过向ADSTOPR.ADSTOPm(m=0 1)位写入1可以强制停止AD转换器的扫描操作。如果强制停止扫描操作，则无法保证AD转换数据。

36.5.4.1 强制停止程序

表36.26显示了AD转换操作的强制停止程序。执行强制停止时请遵守表36.26。如果违反此程序，AD转换器可能无法停止，然后可能无法正常运行。在这种情况下，需要重置以进行恢复。

Table 36.26 强制停止AD转换操作的步骤

No.	步骤名称	Description
1	禁用触发输入	禁用来自外围模块的触发输入。（写ADTRGENR.STTRGENn=0）
2	等待的时间	设置上述步骤1后，需要等待一段时间才能安全停止AD转换器。经过指定的等待时间后，继续进行下一个处理。有关等待时间的详细信息，请参阅第36.5.4.2节。 强制停止处理禁用触发输入后的等待时间。
3	检查AD转换器状态	在经过上述步骤2的等待时间后，检查AD转换器是否正在运行。如果AD转换器正在运行（ADSR.ADACTm=1），则继续执行步骤4。如果AD转换器停止（ADSR.ADACTm=0），则不需要进一步处理（继续执行步骤6）。
4	AD转换器的强制停止	通过ADSTOPR寄存器强制停止AD转换器。*1 (Write ADSTOPR.ADSTOPm = 1)
5	等待AD转换器停止	等到AD转换器停止。(ADSR.ADACTm=0)
6	End	强制停止处理完成。

Note: m=0 1 n=0到8在此强制停止过程正在进行时不要写入ADSYSTR寄存器或ADSTRn寄存器。

注1.自校准操作期间禁止强制停止。有关详细信息，请参阅第36.3.6节。自校准。

36.5.4.2 强制停止处理的触发输入无效后的等待时间

在表36.26所示的强制停止过程中，在禁用来自外围模块的触发输入后，执行强制停止需要等待时间（表36.26的步骤2）。该等待时间是必须确保安全执行强制停止的时间。

The wait time after disabling the trigger input for forced stop processing is calculated as follows.

[Waiting time after disabling trigger input in forced stop processing]

- When Synchronous Operation is enabled (ADSYCR.ADSYDISm = 0)
  - (ADTRGDLRi.TRGDLYn[7:0] setting value + ADSYCR.ADCSYCYC[10:0] setting value × 2) × t_{ADCLK}
- When Synchronous Operation is disabled (ADSYCR.ADSYDISm = 1)
  - (4 + ADTRGDLRi.TRGDLYn[7:0] setting value) × t_{ADCLK}

Note: i = 0 to 4, n = 0 to 8, m = 0, 1 t_{ADCLK}: ADCLK period

Proceed to the Step 3 process in Table 36.26after the waiting time calculated by the above expressions has elapsed using various timer functions, etc. When the above-mentioned wait time is generated without using the timer function, a wait time can also be generated by reading the status register, etc. multiple times. The number of register reads required is expressed by the following equation:

[Wait time generating by register read]

N_{RD} = (Wait time after disabling trigger input ÷ (t_{PCLK} × N_{RDCYC})) + 1

N_{RD}: Number of register reads required to generate the trigger input disable wait time (truncate after the decimal point)

t_{PCLK}: The period of the Bus I/F clock (PCLKA)

N_{RDCYC}: Minimum number of register read access cycles

For more details, refer to section Appendix 3, I/O Registers.

36.6 Error Detection

36.6.1 A/D converter error

An A/D converter error is detected when an abnormal operation of the A/D converter occurs. If an A/D converter error is detected, the A/D conversion result is not guaranteed.

An A/D converter error occurs in the following cases: However, depending on the operating state of the device, an A/D converter error may not be detected even under the following conditions.

[A/D Converter Error Generation Conditions]

- When A/D conversion is performed without Self-calibration.
- When the operating frequency of ADCLK exceeds the guaranteed operating frequency specified in the electric characteristics.
- When the successive approximation time of the A/D converter exceeds the guaranteed operating range specified in the electric characteristics.
- When an accidental abnormal operation occurs in the A/D converter due to external factors.

If an A/D converter error is detected, the flag is set in ADERSR.ADERFn (n = 0, 1) bit. To clear the A/D converter error flag, write 1 to the corresponding bit in ADERSCR register.

Notes on A/D Converter Error

The A/D converter error is an auxiliary function used to detect abnormal operation of the A/D converter. It does not guarantee reliable operation error detection or normal operation. Even under the A/D converter error occurrence conditions described above, an A/D converter error may not be detected depending on the operating status of the device.

36.6.2 A/D conversion overflow

A/D conversion overflow is detected when A/D conversion data exceeds the range that can be handled in the specified data format. When A/D conversion overflow occurs, the A/D conversion data at that time becomes the upper or lower limit value of the specified data format. For the range that can be handled as A/D conversion data, refer to section 36.4.6. Data Format.

A/D conversion overflow is detected in the following cases:

强制停止处理的触发输入无效后的等待时间计算如下。

[强制停止处理中触发输入无效后的等待时间]

●启用同步操作时(ADSYCR.ADSYDISm=0)

(ADTRGDLRi.TRGDLYn[7:0]设置值+ADSYCR.ADCSYCYC[10:0]设置值×2)×tADCLK

●禁用同步操作时(ADSYCR.ADSYDISm=1)

- (4 + ADTRGDLRi.TRGDLYn[7:0] setting value) × t_{ADCLK}

Note: i=0到4 n=0到8 m=0 1tADCLK:ADCLK周期

使用各种计时器函数等，在通过上述表达式计算的等待时间过去后，继续执行表36.26中的步骤3处理。当不使用计时器函数生成上述等待时间时，也可以通过以下方式生成等待时间多次读取状态寄存器等。所需的寄存器读取次数由以下等式表示：

[通过寄存器读取产生的等待时间]

NRD=(禁用触发输入后的等待时间÷(tPCLK×NRDCYC))+1

NRD：生成触发输入禁用等待时间所需的寄存器读取次数（小数点后截断）

tPCLK:总线IF时钟(PCLKA)的周期

NRDCYC:寄存器读取访问周期的最小数量

有关详细信息，请参阅附录3，IO寄存器部分。

36.6 错误检测

36.6.1 AD转换器错误

当AD转换器发生异常操作时，检测到AD转换器错误。如果检测到AD转换器错误，则无法保证AD转换结果。

在以下情况下会发生AD转换器错误：但是，根据设备的操作状态，即使在以下情况下也可能无法检测到AD转换器错误。

[AD转换器错误产生条件]

●在没有自校准的情况下进行AD转换时。

●ADCLK的工作频率超过电气特性中规定的保证工作频率时。

●AD转换器的逐次逼近时间超过电气特性中规定的保证工作范围时。

●当AD转换器由于外部因素发生意外异常操作时。

如果检测到AD转换器错误，则在ADERSR.ADERFn(n=0 1)位中设置该标志。要清除AD转换器错误标志，将1写入ADERSCR寄存器中的相应位。

AD转换器错误的注意事项

AD转换器错误是用于检测AD转换器异常操作的辅助功能。它不保证可靠的操作错误检测或正常操作。即使在上述AD转换器错误发生条件下，根据设备的操作状态，也可能无法检测到AD转换器错误。

36.6.2 AD转换溢出

当AD转换数据超出指定数据格式可以处理的范围时，将检测到D转换溢出。当发生AD转换溢出时，此时的AD转换数据变为指定数据格式的上限值或下限值。关于可作为AD转换数据处理的范围，请参阅36.4.6项。数据格式。

在以下情况下会检测到D转换溢出：

- When the input to the A/D converter exceeds VREFH0 or falls below VREFL0
- When overflow occurs by the internal processing (calculation) for the A/D conversion data shown in the following:
  - Gain Error and Offset Error Calibration
  - User's Gain/User's Offset adjustment function
  - When using A/D-Converted Value Addition/Averaging Function
  - Data Formatting Process

When an A/D conversion overflow is detected, the flag is set in the following status register:

- ADOVFERSR: The flag is set to the bit corresponding to the A/D converter that detected the A/D conversion overflow.
- ADOVFCHSR0: The flag is set to the bit corresponding to the analog input channel on which A/D conversion overflow is detected.
- ADOVFEXSR: The flag is set to the bit corresponding to the Extended Analog channel on which A/D conversion overflow is detected.

To clear the flags in the status registers, write 1 to the corresponding bit in ADOVFERSCR, ADOVFCHSCR0, ADOVFEXSCR.

Restrictions on A/D conversion overflow

When A/D-Converted Value Addition/Averaging Function is used, A/D conversion overflow is not detected under the following conditions.

- Leading channel of scan group
- Restart channel of the interrupted group in Group Priority Operation

To detect that the A/D conversion data is illegal under these conditions, use Limiter Clip Function or Compare match function.

36.6.3 FIFO overflow

If A/D-converted data is written (added) to FIFO while FIFO is full, a FIFO overflow is detected. For more details about FIFO overflow, refer to section 36.4.9. FIFO Function.

36.7 Procedure for setting up and changing

36.7.1 Initial setup procedure

Table 36.27 shows the initial setup procedure.

Table 36.27 Initial setup procedure (1 of 2)

No.	Step	Description
1	Release module-stop	Release the module-stop bit for ADC in MSTPCR register.
2	I/O port Configuration	Set ASEL bit of the pin used as analog input to 1.
3	Synchronous Operation Configuration	Set the Synchronous operation function. The synchronous operation function is enabled at the initial value of the register after reset release. If the synchronous operation function is not used, be sure to disable the synchronous operation function (ADSYCR.ADSYDISm = 1 (m = 0, 1)).
4	ADCLK Configuration	Set the clock source and division ratio for ADCLK. Then, set ADCLKENR.CKEN bit to 1, and wait for ADCLK to supply (ADCLKSR.CLKSR = 1).
5	A/D conversion configuration	Perform various settings for A/D conversion.
6	Wait for operation stabilization	Wait until the various operating stabilization times specified in the Electrical Characteristics have elapsed.

●当AD转换器的输入超过VREFH0或低于VREFL0时

●当AD转换数据的内部处理（计算）发生溢出时，如下所示：

增益误差和偏移误差校准

–用户增益用户偏移调整功能

使用D转换的增值平均功能时

数据格式化过程

当检测到AD转换溢出时，在以下状态寄存器中设置标志：

●ADOVFERSR：该标志设置为与检测到AD转换溢出的AD转换器对应的位。

●ADOVFCHSR0：该标志设置为与检测到AD转换溢出的模拟输入通道对应的位。

●ADOVFEXSR：该标志设置为与检测到AD转换溢出的扩展模拟通道对应的位。

要清除状态寄存器中的标志，请将1写入ADOVFERSCR、ADOVFCHSCR0、ADOVFEXSCR.

AD转换溢出的限制

使用AD转换值加法平均功能时，在以下条件下不会检测到AD转换溢出。

●扫描组主通道

●GroupPriorityOperation中中断组的重启通道

要在这些条件下检测AD转换数据是非法的，请使用限制器剪辑功能或比较匹配功能。

36.6.3 FIFO overflow

如果在FIFO已满时将AD转换数据写入（添加）到FIFO，则检测到FIFO溢出。有关更多详细信息FIFO溢出，请参阅第36.4.9节。先进先出功能。

36.7 设置和更改程序

36.7.1 初始设置程序

表36.27显示了初始设置过程。

Table 36.27 初始设置程序(1of2)

No.	Step	Description
1	Release module-stop	释放MSTPCR寄存器中ADC的模块停止位。
2	IO口配置	将用作模拟输入的引脚的ASEL位设置为1。
3	同步操作配置	设置同步运行功能。 复位释放后，同步操作功能在寄存器的初始值处使能。如果不使用同步运算功能，请务必禁用同步运算功能(ADSYCR.ADSYDISm=1(m=0 1))。
4	ADCLK Configuration	设置ADCLK的时钟源和分频比。 然后，将ADCLKENR.CKEN位设置为1，并等待ADCLK提供(ADCLKSR.CLKSR=1)。
5	AD转换配置	执行AD转换的各种设置。
6	等待运行稳定	等到电气规范中规定的各种运行稳定时间特征已经过去。

Table 36.27 Initial setup procedure (2 of 2)

No.	Step	Description
7	Self-Calibration	Self-Calibration must be executed prior to starting A/D conversion. Set up for Self-Calibration and execute it. For more details, refer to section 36.3.6. Self-Calibration.
8	Trigger configuration	To start A/D conversion by a trigger from peripheral modules, configure the triggers for each scan group.
9	Start of A/D conversion	When a software trigger or a trigger from peripheral modules is input, A/D conversion (scanning operation) starts.

36.7.2 Procedure for changing ADCLK settings

Table 36.28 shows the procedure for changing ADCLK setting.

Table 36.28 Procedure for changing ADCLK setting

No.	Step	Description
1	Disable trigger input	Disables the trigger input from the peripheral module. (Write ADTRGENR.STTRGENn = 0)
2	Stop A/D conversion	Check that all AD converter is stopped. When A/D conversion is in progress, wait until all A/D conversion is completed or forcibly stop A/D conversion operation. For details about forcibly stop A/D conversion operation, refer to section 36.5.4. Force stops the A/D conversion operation.
3	Stop ADCLK supplies	Set ADCLKENR.CKEN bit to 0. Then, wait for ADCLK to stop (ADCLKSR.CLKSR = 0).
4	Change ADCLK setting	Change the clock-source and the division ratio for ADCLK.
5	Started supplying ADCLK	Set ADCLKENR.CKEN bit to 1, and wait for ADCLK to supply (ADCLKSR.CLKSR = 1).
6	Change the A/D conversion configuration	Change the following settings according to the changed ADCLK frequency. • Successive approximation time for A/D converter • Number of sampling states for A/D conversion • Number of sampling states and hold mode switching states for Channel-dedicated sample-and-hold circuit *1 • Number of states for Self-Calibration operation (A/D converter and Channel-dedicated sample-and-hold circuit *1) • Synchronous Operation Period *2 • Disconnection Detection Assist Period *3 If other settings related to A/D conversion are also to be changed, change them in this step.
7	Wait for operation stabilization	Wait until the various operating stabilization times specified in the section 46, Electrical Characteristics have elapsed.
8	Self-Calibration	Execute Self-Calibration operation prior to starting A/D conversion. For more details, refer to section 36.3.6. Self-Calibration.
9	Trigger configuration	To start A/D conversion by a trigger from peripheral modules, configure the triggers for each scan group.
10	Start of A/D conversion	When a software trigger or a trigger from peripheral modules is input, A/D conversion (scanning operation) starts.

Note 1. Setting is not required when Channel-dedicated sample-and-hold circuit is not used.
Note 2. No change is required when Synchronous Operation setting is disabled (ADSYCR, ADSYDISm = 1 (m = 0, 1))
Note 3. Setting is not required when Disconnection Detection Assist Function is not used.

36.7.3 Procedure for changing the settings of the A/D converter

Table 36.29 shows the procedure for changing the A/D conversion configuration. If there is a change in ADCLK setting, follow the procedures in section 36.7.2. Procedure for changing ADCLK settings.

Table 36.27 初始设置程序（2之2）

No.	Step	Description
7	Self-Calibration	自校准必须在开始AD转换之前执行。 设置自校准并执行它。 有关详细信息，请参阅第36.3.6节。自校准。
8	触发配置	要通过来自外围模块的触发器启动AD转换，请为每个扫描组配置触发器。
9	AD转换开始	当输入软件触发或来自外围模块的触发时，AD转换（扫描操作）开始。

36.7.2 更改ADCLK设置的步骤

表36.28显示了更改ADCLK设置的过程。

Table 36.28 更改ADCLK设置的步骤

No.	Step	Description
1	禁用触发输入	禁用来自外围模块的触发输入。（写ADTRGENR.STTR GENn=0）
2	停止AD转换	检查所有AD转换器是否已停止。 当AD转换正在进行时，等待所有AD转换完成或强制停止AD转换操作。关于强制停止AD转换操作的详细内容，请参阅36.5.4节。 强制停止AD转换操作。
3	停止ADCLK电源	将ADCLKENR.CKEN位设置为0。然后，等待ADCLK停止(ADCL KSR.CLKSR=0)。
4	更改ADCLK设置	更改ADCLK的时钟源和分频比。
5	开始提供ADCLK	将ADCLKENR.CKEN位设置为1，并等待ADCLK提供(ADCLKSR. CLKSR=1)。
6	更改AD转换配置	根据更改后的ADCLK频率更改以下设置。● AD转换器的逐次逼近时间 • AD转换的采样状态数 • 通道专用采样保持电路的采样状态数和保持模式切换状态*1 • 自校准操作的状态数（AD转换器和 Channel-dedicated sample-and-hold circuit *1) • 同步运行期间*2 • 断线检测辅助期间*3 如果还需要更改与AD转换相关的其他设置，请在此步骤中进行更改。
7	等待运行稳定	等到第46节规定的各种运行稳定时间， 电气特性已失效。
8	Self-Calibration	在开始AD转换之前执行自校准操作。有关详细信息，请参阅第36.3.6节。自校准。
9	触发配置	要通过来自外围模块的触发器启动AD转换，请为每个扫描组配置触发器。
10	AD转换开始	当输入软件触发或来自外围模块的触发时，AD转换（扫描操作）开始。

注1.不使用通道专用采样保持电路时无需设置。
注2.禁用同步操作设置时无需更改(ADSYCR ADSYDISm=1(m=0 1))
注3.不使用断线检测辅助功能时无需设定。

36.7.3 更改AD转换器设置的步骤

表36.29显示了更改AD转换配置的过程。如果ADCLK设置发生变化，请按照第36.7.2节中的程序进行。更改AD CLK设置的程序。

Table 36.29 Procedure for changing the settings of the A/D converter

No.	Step	Description
1	Disable trigger input	Disables the trigger input from the peripheral module. (Write ADTRGENR.STTRGENn = 0)
2	Stop A/D conversion	Check that all AD converter is stopped. When A/D conversion is in progress, wait until all A/D conversion is completed or forcibly stop A/D conversion operation. For details about forcibly stop A/D conversion operation, refer to section 36.5.4. Force stops the A/D conversion operation.
3	Change the A/D conversion configuration	Change various settings for A/D conversion. (except the settings for ADCLK)
4	Wait for operation stabilization	Wait until the various operating stabilization times specified in the Electrical Characteristics have elapsed.
5	Self-Calibration	Execute Self-Calibration operation prior to starting A/D conversion. For more details, refer to section 36.3.6. Self-Calibration.
6	Trigger configuration	To start A/D conversion by a trigger from peripheral modules, configure the triggers for each scan group.
7	Start of A/D conversion	When a software trigger or a trigger from peripheral modules is input, A/D conversion (scanning operation) starts.

36.8 Interrupt Sources and ELC Events

Table 36.30 lists ADC interrupt sources or ELC event requests.

For more details about interrupts, refer to section 12, Interrupt Controller Unit (ICU).

For more details about ELC events, refer to section 17, Event Link Controller (ELC).

Table 36.30 Interrupt Sources (1 of 2)

Interrupt request or ELC event	Symbol	Description	Status flag
A/D converter error interrupt	ADC_ERR0	Generated when abnormal operation of ADC0 is detected.	ADERSR.ADERF0
	ADC_ERR1	Generated when abnormal operation of ADC1 is detected.	ADERSR.ADERF1
A/D converter Self-Calibration End interrupt	ADC_CALEND0	Generated when Self-Calibration operation of ADC0 is finished.	ADCALENDSR.CALENDF0
	ADC_CALEND1	Generated when Self-Calibration operation of ADC1 is finished.	ADCALENDSR.CALENDF1
A/D Scan End Interrupt	ADC_ADI0	Generated at the scan end of scan group 0	ADSCANENDSR.SCANENDF0
	ADC_ADI1	Generated at the scan end of scan group 1	ADSCANENDSR.SCANENDF1
	ADC_ADI2	Generated at the scan end of scan group 2	ADSCANENDSR.SCANENDF2
	ADC_ADI3	Generated at the scan end of scan group 3	ADSCANENDSR.SCANENDF3
	ADC_ADI4	Generated at the scan end of scan group 4	ADSCANENDSR.SCANENDF4
	ADC_ADI5678	Generated at the scan end of scan group 5 to 8	ADSCANENDSR.SCANENDF5 ADSCANENDSR.SCANENDF6 ADSCANENDSR.SCANENDF7 ADSCANENDSR.SCANENDF8
Limitter Clip interrupt	ADC_LIMCLPI	Generated when a limiter clip using limiter table 0 to 7 is detected for A/D conversion.	ADLIMGRSR.LIMGRFn ADLIMCHSR0.LIMCHFi ADLIMEXSR.LIMEXFj

Table 36.29 更改AD转换器设置的步骤

No.	Step	Description
1	禁用触发输入	禁用来自外围模块的触发输入。（写ADTRGENR.STTR GENn=0）
2	停止AD转换	检查所有AD转换器是否已停止。 当AD转换正在进行时，等待所有AD转换完成或强制停止AD转换操作。关于强制停止AD转换操作的详细内容，请参阅36.5.4节。 强制停止AD转换操作。
3	更改AD转换配置	更改AD转换的各种设置。（ADCLK的设置除外）
4	等待运行稳定	等到电气规范中规定的各种运行稳定时间 特征已经过去。
5	Self-Calibration	在开始AD转换之前执行自校准操作。 有关详细信息，请参阅第36.3.6节。自校准。
6	触发配置	要通过来自外围模块的触发器启动AD转换，请为每个扫描组配置触发器。
7	AD转换开始	当输入软件触发或来自外围模块的触发时，AD转换（扫描操作）开始。

36.8 中断源和ELC事件

表36.30列出了ADC中断源或ELC事件请求。

有关中断的更多详细信息，请参阅第12节，中断控制器单元(ICU)。

有关ELC事件的更多详细信息，请参阅第17节，事件链接控制器(ELC)。

Table 36.30 中断源(1of2)

中断请求或ELC事件	Symbol	Description	状态标志
AD转换器错误中断	ADC_ERR0	当检测到ADC0工作异常时产生。	ADERSR.ADERF0
	ADC_ERR1	当检测到ADC1工作异常时产生。	ADERSR.ADERF1
A/D converter Self-Calibration 结束中断	ADC_CALEND0	ADC0的自校准操作完成时产生。	ADCALENDSR.CALENDF0
	ADC_CALEND1	ADC1的自校准操作完成时产生。	ADCALENDSR.CALENDF1
AD扫描结束中断	ADC_ADI0	在扫描组0的扫描结束时生成	ADSCANENDSR.SCANENDF0
	ADC_ADI1	在扫描组1的扫描结束时生成	ADSCANENDSR.SCANENDF1
	ADC_ADI2	在扫描组2的扫描结束时生成	ADSCANENDSR.SCANENDF2
	ADC_ADI3	在扫描组3的扫描结束时生成	ADSCANENDSR.SCANENDF3
	ADC_ADI4	在扫描组4的扫描结束时生成	ADSCANENDSR.SCANENDF4
	ADC_ADI5678	在扫描组5到8的扫描结束时生成	ADSCANENDSR.SCANENDF5 ADSCANENDSR.SCANENDF6 ADSCANENDSR.SCANENDF7 ADSCANENDSR.SCANENDF8
限制器剪辑中断	ADC_LIMCLPI	当检测到使用限制器表0到7进行AD转换的限制器剪辑时生成。	ADLIMGRSR.LIMGRFn ADLIMCHSR0.LIMCHFi ADLIMEXSR.LIMEXFj

Table 36.30 Interrupt Sources (2 of 2)

Interrupt request or ELC event	Symbol	Description	Status flag
A/D Conversion Overflow interrupt	ADC_RESOVF0	Generated when the overflow is detected in A/D conversion result with ADC0.	ADOVFERSR.ADOVFEF0 ADOVFCHSR0.OVFCHFi ADOVFEXSR.OVFEXFj
	ADC_RESOVF1	Generated when the overflow is detected in A/D conversion result with ADC1.	ADOVFERSR.ADOVFEF1 ADOVFCHSR0.OVFCHFi ADOVFEXSR.OVFEXFj
Compare Match interrupt	ADC_CMPI0	Generated when a compare match with compare match table 0 is detected.	ADCMPTBSR.CMPTBF0
	ADC_CMPI1	Generated when a compare match with compare match table 1 is detected.	ADCMPTBSR.CMPTBF1
	ADC_CMPI2	Generated when a compare match with compare match table 2 is detected.	ADCMPTBSR.CMPTBF2
	ADC_CMPI3	Generated when a compare match with compare match table 3 is detected.	ADCMPTBSR.CMPTBF3
Composite Compare Match interrupt	ADC_CCMPM0 ADC_CCMPM1	Generated when a composite compare match with combined conditions using Compare match table 0 to 7 is detected.	ADCMPTBSR.CMPTBF0 to ADCMPTBSR.CMPTBF8
FIFO data read request interrupt	ADC_FIFOREQ0	Generated when the number of available stages in FIFO for scan group 0 become less than or equal to the specified value.	ADFIFOSR0.FIFOST0[3:0]
	ADC_FIFOREQ1	Generated when the number of available stages in FIFO for scan group 1 become less than or equal to the specified value.	ADFIFOSR0.FFOST1[3:0]
	ADC_FIFOREQ2	Generated when the number of available stages in FIFO for scan group 2 become less than or equal to the specified value.	ADFIFOSR1.FFOST2[3:0]
	ADC_FIFOREQ3	Generated when the number of available stages in FIFO for scan group 3 become less than or equal to the specified value.	ADFIFOSR1.FFOST3[3:0]
	ADC_FIFOREQ4	Generated when the number of available stages in FIFO for scan group 4 become less than or equal to the specified value.	ADFIFOSR2.FFOST4[3:0]
	ADC_FIFOREQ5678	Generated when the number of available stages in any of FIFO for scan groups 5 to 8 become less than or equal to the specified value.	ADFIFOSR2.FFOST5[3:0] ADFIFOSR3.FFOST6[3:0] ADFIFOSR3.FFOST7[3:0] ADFIFOSR3.FFOST8[3:0]
FIFO data overflow interrupt	ADC_FIFOOVF	Generated when FIFO overflow is detected in any of FIFO for scan group 0 to 8.	ADFIFOERSR.FIFOOVF0 to ADFIFOERSR.FIFOOVF8

Note: i = 0 to 28.
j = 0 to 2, 5 to 8.

(1) A/D Converter Error Interrupt

A/D Converter Error interrupt can be generated when an A/D Converter Error is detected.

A/D Converter Error interrupt (ADC_ERRm (m = 0, 1)) is generated when ADERINTCR.ADEIEm (m = 0, 1) bit is 1 and ADERSR.ADERFm (m = 0, 1) bit is 1.

Table 36.30 中断源(2of2)

中断请求或ELC事件	Symbol	Description	状态标志
AD转换溢出中断	ADC_RESOVF0	ADC0在AD转换结果中检测到溢出时产生。	ADOVFERSR.ADOVFEF0 ADOVFCHSR0.OVFCHFi ADOVFEXSR.OVFEXFj
	ADC_RESOVF1	当使用ADC1在AD转换结果中检测到溢出时产生。	ADOVFERSR.ADOVFEF1 ADOVFCHSR0.OVFCHFi ADOVFEXSR.OVFEXFj
比较匹配中断	ADC_CMPI0	当检测到与比较匹配表0的比较匹配时生成。	ADCMPTBSR.CMPTBF0
	ADC_CMPI1	当检测到与比较匹配表1的比较匹配时生成。	ADCMPTBSR.CMPTBF1
	ADC_CMPI2	当检测到与比较匹配表2的比较匹配时生成。	ADCMPTBSR.CMPTBF2
	ADC_CMPI3	当检测到与比较匹配表3的比较匹配时生成。	ADCMPTBSR.CMPTBF3
复合比较匹配中断	ADC_CCMPM0 ADC_CCMPM1	当使用比较匹配表0到7检测到具有组合条件的复合比较匹配时生成。	ADCMPTBSR.CMPTBF0 to ADCMPTBSR.CMPTBF8
FIFO数据读取请求中断	ADC_FIFOREQ0	当扫描组0的FIFO中的可用阶段数小于或等于指定值时生成。	ADFIFOSR0.FIFOST0[3:0]
	ADC_FIFOREQ1	当扫描组1的FIFO中的可用阶段数小于或等于指定值时生成。	ADFIFOSR0.FFOST1[3:0]
	ADC_FIFOREQ2	当扫描组2的FIFO中的可用阶段数小于或等于指定值时生成。	ADFIFOSR1.FFOST2[3:0]
	ADC_FIFOREQ3	当扫描组3的FIFO中的可用阶段数小于或等于指定值时生成。	ADFIFOSR1.FFOST3[3:0]
	ADC_FIFOREQ4	当扫描组4的FIFO中的可用阶段数小于或等于指定值时生成。	ADFIFOSR2.FFOST4[3:0]
	ADC_FIFOREQ5678	当扫描组5到8的任何FIFO中的可用阶段数小于或等于指定值时生成。	ADFIFOSR2.FFOST5[3:0] ADFIFOSR3.FFOST6[3:0] ADFIFOSR3.FFOST7[3:0] ADFIFOSR3.FFOST8[3:0]
FIFO数据溢出中断	ADC_FIFOOVF	在扫描组0到8的任何FIFO中检测到FIFO溢出时生成。	ADFIFOERSR.FIFOOVF0 to ADFIFOERSR.FIFOOVF8

Note: i = 0 to 28.
j = 0 to 2, 5 to 8.

(1) AD转换器错误中断

当检测到AD转换器错误时，可以生成D转换器错误中断。

当ADERINTCR.ADEIEm(m=0 1)位为1且
ADERSR.ADERFm(m=0 1)位为1。

(2) A/D Converter Self-Calibration End Interrupt

A/D converter Self-Calibration End interrupt can be generated at the end of A/D converter Self-Calibration operation.

A/D converter Self-Calibration End interrupt (ADC_CALENDm (m = 0, 1)) is generated when ADCALINTCR.CALENDIEm (m = 0, 1) bit is 1 and ADCALENDSR.CALENDFm (m = 0, 1) bit is 1.

(3) A/D scan End interrupt

A/D Scan End interrupt can be generated at the end of scanning operation of scan group n (n = 0 to 8).

A/D Scan End interrupt for scan group 0 to 4 (ADC_ADI0 to ADC_ADI4) are generated when ADINTCR.ADIEn (n = 0 to 4) bit is set to 1 and ADSCANENDSR.SCENDFn (n = 0 to 4) bit is set to 1.

A/D Scan End interrupt for scan group 5 to 8 (ADC_ADI5678) is generated when ADINTCR.ADIEn (n = 5 to 8) bit is set to 1 and ADSCANENDSR.SCENDFn (n = 5 to 8) bit is set to 1 is satisfied in any of the scan group 5 to 8.

However, A/D Scan End interrupt is not generated when A/D conversion operation (scanning operation) is forcibly stopped by ADSTOPR register.

(4) Limitter Clip interrupt

Limiter Clip interrupt (ADC_LIMCLPI) can be generated when a limiter clip with limiter table i (i = 0 to 7) is detected.

Limiter Clip interrupt is generated when either ADLIMINTCR.LIMIEi (i = 0 to 7) bit is 1 and ADLIMGRSR.LIMGRFi (i = 0 to 7) bit is 1 is satisfied.

(5) A/D Conversion Overflow interrupt

A/D Conversion Overflow interrupt can be generated when A/D Conversion overflow in the A/D conversion result using ADCm (m = 0, 1) is detected. For details about A/D Conversion overflow, refer to section 36.6.2. A/D conversion overflow.

A/D Conversion Overflow interrupt (ADC_RESOVFm (m = 0, 1)) is generated when ADOVFINTCR.ADOVFIEm (m = 0, 1) bit is 1 and ADOVFERSR.ADOVFEFm (m = 0, 1) bit is 1.

(6) Compare Match interrupt

Compare Match interrupt can be generated when a compare match is detected.

Compare Match interrupt (ADC_CMPIj (j = 0 to 3)) is generated when ADCMPINTCR.CMPIEj (j = 0 to 3) bit is 1 and ADCMPTBSR.CMPTBFj (j = 0 to 3) bit is 1.

There are no interrupts corresponding to the compare match tables 4 to 7.

(7) Composite Compare Match interrupt

Composite Compare Match interrupt (ADC_CCMPMk (k = 0, 1)) can be generated by combining the comparison results of two or more compare match tables. For details about composite compare match, refer to section 36.4.7.2. Composite Compare Match.

(8) FIFO data read request interrupt

FIFO data read request interrupt can be generated when the number of available stages in FIFO become less than or equal to the specified value.

FIFO data read request interrupt for scan group 0 to 4 (ADC_FIFOREQ0 to ADC_FIFOREQ4) are generated when ADFIFOINTCR.FIFOIEn (n = 0 to 4) is set to 1 and ADFIFOSRm.FIFOSTn[3:0] ≤ ADFIFOINTLRm.FIFOLVn[3:0] (m = 0 to 3, n = 0 to 4).

FIFO data read request interrupt for scan group 5 to 8 (ADC_FIFOREQ5678) are generated when the following condition is satisfied in any FIFO for scan group 5 to 8: ADFIFOINTCR.FIFOIEn (n = 5 to 8) is set to 1 and ADFIFOSRm.FIFOSTn[3:0] ≤ ADFIFOINTLRm.FIFOLVn[3:0] (m = 3 to 4, n = 5 to 8)

However, FIFO read request interrupt is not generated while the ADFIFOERSR.FIFOFLFn (n = 0 to 8) bit corresponding to its interrupt source is set to 1.

(9) FIFO data overflow interrupt

FIFO data overflow interrupt (ADC _FIFOOVF) can be generated when a FIFO overflow is detected in any of FIFO in scan groups 0 to 8.

(2) AD转换器自校准结束中断

AD转换器自校准结束中断可以在AD转换器自校准操作结束时产生。

D转换器自校准结束中断(ADC_CALENDm(m=0 1))在以下情况下产生
ADCALINTCR.CALENDIEm(m=0 1)位为1，ADCALENDSR.CALENDFm(m=0 1)位为1。

(3) AD扫描结束中断

在扫描组n（n=0到8）的扫描操作结束时可以产生D扫描结束中断。

当ADINTCR.ADIEn(n=0到4)位设置为1且ADSCANENDSR.SCENDFn(n=0到4)位设置为1时，将生成扫描组0到4（AD C_ADI0到ADC_ADI4）的D扫描结束中断。

当ADINTCR.ADIEn(n=5到8)位设置为1且ADSCANENDSR.SCENDFn(n=5到8)位设置为1时，将产生扫描组5到8(AD C_ADI5678)的D扫描结束中断扫描组5到8中的任何一个。

但是，当ADSTOPR寄存器强制停止AD转换操作（扫描操作）时，不会产生AD扫描结束中断。

(4) 限制器剪辑中断

当检测到带有限制器表i（i=0到7）的限制器剪辑时，可以生成限制器剪辑中断(ADC_LIMCLPI)。

当ADLIMINTCR.LIMIEi(i=0至7)位为1且ADLIMGRSR.LIMGRFi(i=0至7)位为1时，产生限制器剪辑中断。

(5) AD转换溢出中断

当AD转换结果中的AD转换溢出时，可以产生AD转换溢出中断
ADCm(m=0 1)被检测到。关于AD转换溢出的详细内容，请参阅36.6.2节。AD转换溢出。

当ADOVFINTCR.ADOVFIEm(m=0 1)位为1且ADOVFERSR.ADOVFEFm(m=0 1)位为1时，产生D转换溢出中断(ADC_ RESOVFm(m=0 1))。

(6) 比较匹配中断

当检测到比较匹配时，可以产生比较匹配中断。

当ADCMPINTCR.CMPIEj(j=0to3)位为1且
ADCMPTBSR.CMPTBFj(j=0到3)位为1。

没有对应于比较匹配表4到7的中断。

(7) 复合比较匹配中断

综合比较匹配中断(ADC_CCMPMk(k=0 1))可以通过组合两个或多个比较匹配表的比较结果来产生。有关复合比较匹配的详细信息，请参阅第36.4.7.2节。复合比较匹配。

(8) FIFO数据读取请求中断

当FIFO中的可用级数小于或等于指定值时，会产生FIFO数据读取请求中断。

扫描组0到4（ADC_FIFOREQ0到ADC_FIFOREQ4）的FIFO数据读取请求中断在以下情况下产生
ADFIFOINTCR.FIFOIEn（n=0到4）设置为1，并且ADFIFOSRm.FIFOSTn[3:0]≤ADFIFOINTLRm.FIFOLVn[3:0]（m=0到3，n=0到4）。

当扫描组5到8的任何FIFO满足以下条件时，将生成扫描组5到8的FIFO数据读取请求中断(ADC_FIFOREQ5678)：ADFIFOINTCR.FIFOIEn(n=5到8)设置为1且ADFIFOSRm.FIFOSTn[3:0]≤ADFIFOINTLRm.FIFOLVn[3:0]（m=3到4，n=5到8）

但是，当其中断源对应的ADFIFOERSR.FIFOFLFn(n=0至8)位设置为1时，不会产生FIFO读请求中断。

(9) FIFO数据溢出中断

当在扫描组0到8中的任何FIFO中检测到FIFO溢出时，可以生成FIFO数据溢出中断(ADC_FIFOOVF)。

FIFO data overflow interrupt is generated when ADFIFOINTCR.FIFOIEn (n = 0 to 8) bit is 1 and ADFIFOERSR.FIFOOVFn (n = 0 to 8) bit is 1.

36.9 Scan Conversion Time

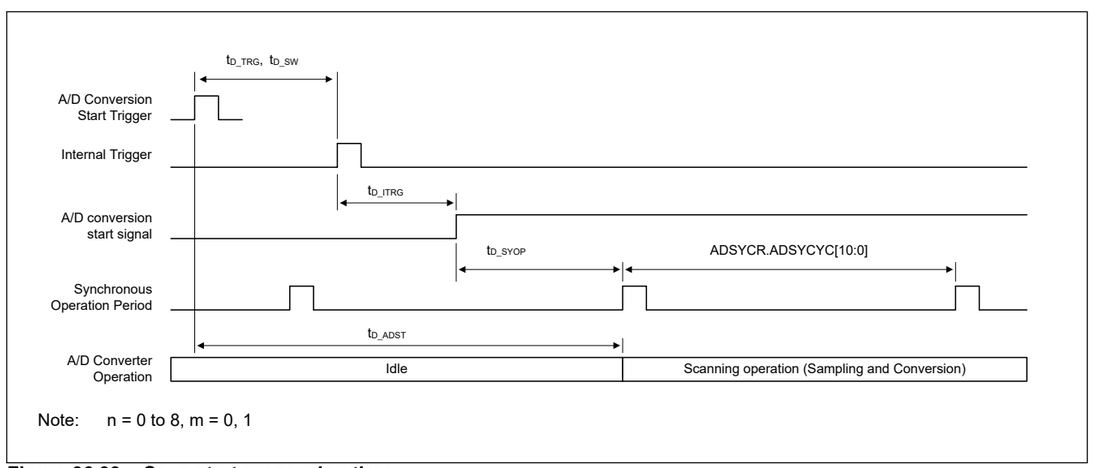
36.9.1 Scan Start Processing Time

The processing time from the input of the A/D conversion start trigger to the start of the scanning operation is shown in Table 36.31 and Figure 36.33.

Table 36.31 Scan start processing time

Item		Symbol	Processing time
Peripheral module trigger input processing time*1		t_{D_TRG}	1 ADSRCCLK + 3 ADCLK + (ADTRGDLRr.TRGDLYn[7:0] + 1) × ADCLK
Software trigger input processing time		t_{D_SW}	[When ADCLK = PCLKA/1]*2 • Number of access cycles to I/O registers*3 + 1 PCLKA [Other than above] • (Number of access cycles to I/O registers*3) + 1 PCLKA + (3 to 4 ADCLK)
Internal Trigger processing time		t_{D_ITRG}	3 ADCLK
Wait Time for Synchronous Operation		t_{D_SYOP}	[When Synchronous Operation is disabled] (ADSYCR.ADSYDISm = 1) • 0 [When Synchronous Operation is enabled] (ADSYCR.ADSYDISm = 0) • 0 to ADSYCR.ADSYCYC[10:0] × ADCLK
Total scan stat processing time	Started by Peripheral Module Trigger	t_{D_ADST}	t_{D_TRG} + t_{D_ITRG} + t_{D_SYOP}
	Started by Software Trigger		t_{D_SW} + t_{D_ITRG} + t_{D_SYOP}

Note: ADSRCCLK: Clock source of ADCLK
n = 0 to 8, m = 0, 1, r = 0 to 4
Note 1. It does not include the input delay time from the source of the peripheral module trigger to ADC.
Note 2. When ADCLKCR.CLKSEL[1:0] = 10b and ADCLKCR.DIVR[2:0] = 000b are set.
Note 3. It is the number of access cycles to ADSTRn register (n = 0 to 8) or ADSYSTR register. For more details about the number of access cycles for I/O registers, refer to section Appendix 3, I/O Registers.



Note: n = 0 to 8, m = 0, 1

Figure 36.33 Scan start processing time

36.9.2 Conversion Processing Time

当ADFIFOINTCR.FIFOIEn(n=0to8)位为1且
ADFIFOERSR.FIFOOVFn（n=0到8）位为1。

36.9 扫描转换时间

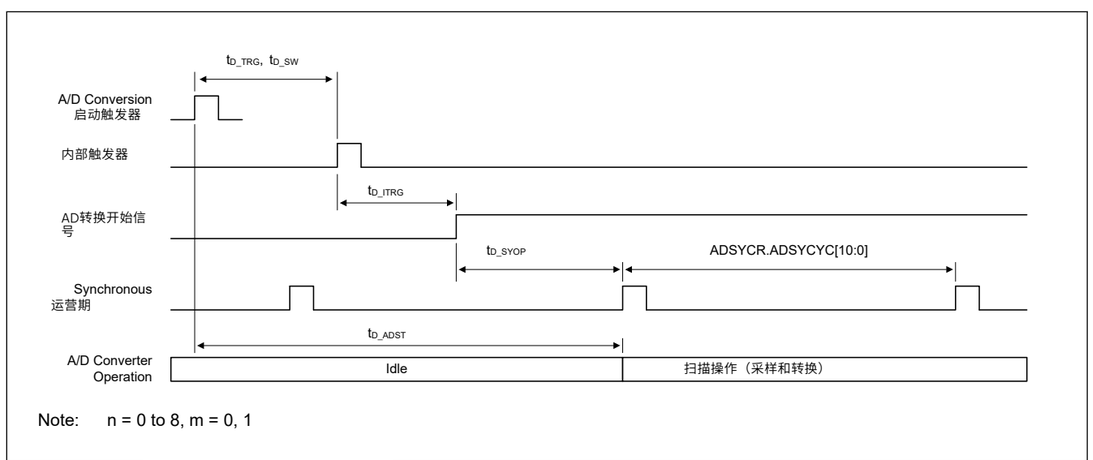
36.9.1 扫描开始处理时间

从输入AD转换开始触发到开始扫描操作的处理时间如图所示
表36.31和图36.33。

Table 36.31 扫描开始处理时间

Item		Symbol	处理时间
外围模块触发输入处理时间*1		t_{D_TRG}	1 ADSRCCLK + 3 ADCLK + (ADTRGDLRr.TRGDLYn[7:0] + 1) × ADCLK
软件触发输入处理时间		t_{D_SW}	[When ADCLK = PCLKA/1]*2 ●IO寄存器的访问周期数*3+1PCLKA[上述以外]● （IO寄存器的访问周期数*3）+1PCLKA+（3到4ADCLK）
内部触发处理时间		t_{D_ITRG}	3 ADCLK
同步操作的等待时间		t_{D_SYOP}	[禁用同步操作时](ADSYCR.ADSYDISm=1) ● 0[启用同步操作时](ADSYCR.ADSYDISm=0) ● LK
总扫描统计处理时间	由外设模块启动 Trigger	t_{D_ADST}	t_{D_TRG} + t_{D_ITRG} + t_{D_SYOP}
	由软件触发启动		t_{D_SW} + t_{D_ITRG} + t_{D_SYOP}

Note: ADSRCCLK：ADCLK的时钟源n=0to8
m=0 1 r=0to4
注1.它不包括从外围模块触发源到ADC的输入延迟时间。
注2.当ADCLKCR.CLKSEL[1:0]=10b且ADCLKCR.DIVR[2:0]=000b设置时。
注3.它是访问ADSTRn寄存器（n=0至8）或ADSYSTR寄存器的周期数。有关IO寄存器访问周期数的更多详细信息，请参阅附录3，IO寄存器部分。



Note: n = 0 to 8, m = 0, 1

Figure 36.33 扫描开始处理时间

36.9.2 转换处理时间

The various processing times in the conversion operation are shown in Table 36.32, Figure 36.34 and Figure 36.35.

Table 36.32 A/D Conversion Processing Time

Item		Symbol	Processing Time
Channel-dedicated sample-and-hold processing time	Sampling time	t_{SH_SPL}	ADSHSTRm.SHSST[7:0] × ADCLK
	Hold mode switching time	t_{SH_HLD}	ADSHSTRm.SHHST[2:0] × ADCLK
Disconnection Detect Assist processing time		t_{DDA}	[When Disconnection Detect Assist Function is disabled] ● 0 [When Disconnection Detect Assist Function is enabled] ● ADSGDCRn.ADNDIS[3:0] × ADCLK
A/D conversion time	Sampling time	t_{AD_SPL}	ADSSTRp.SSTq[9:0] × ADCLK
	Successive approximation time	t_{AD_CNV}	ADCNVSTR.CSTm[5:0] × ADCLK
A/D conversion data processing time	When ADCLK = PCLKA/1 is set*1	t_{ADDP}	[When A/D-Converted Value Addition/Average Function is not used] ● 6 ADCLK + 2 PCLKA [When A/D-Converted Value Addition/Average Function is used] ● 7 ADCLK + 2 PCLKA
	Other than above		[A/D-Converted Value Addition/Average Function is not used] ● 7 ADCLK + (5 to 6 PCLKA) [A/D-Converted Value Addition/Average Function is used] ● 8 ADCLK + (5 to 6 PCLKA)
Total A/D conversion time*3	Channel conversion time*2	t_{ADCH}	$(t_{DDA} + t_{AD\_SPL} + t_{AD\_CNV}) \times N\_ADC \times ADCLK$
	Scan conversion time*4	t_{SCAN}	[When Channel-dedicated sample-and-hold circuit is not used] ● Σt_{ADCH} [When Channel-dedicated sample-and-hold circuit is used] ● $t_{SH\_SPL} + t_{SH\_HLD} + \Sigma t_{ADCH}$

Note: n = 0 to 8, m = 0, 1, p = 0 to 7, q = 0 to 15
N_{ADC}: This value is the number of the times of the addition/averaging according to the setting value of ADDOPCRBx.ADC[3:0] (x = 0 to 36). If A/D-Converted Value Addition/Average Function is not used, This value is 1.
Note 1. When ADCLKCR.CLKSEL[1:0] = 10b and ADCLKCR.DIVR[2:0] = 000b are set.
Note 2. It does not include the Channel-dedicated sample-and-hold processing time.
Note 3. It does not include the A/D conversion data processing time
Note 4. This is the sum of the channel conversion times (t_{ADCH}) that calculated from the conversion settings for each analog channel assigned to the scan group. If Channel-dedicated sample-and-hold circuits are used, Channel-dedicated sample-and-hold processing times (t_{SH_SPL} and t_{SH_HLD}) are also added.

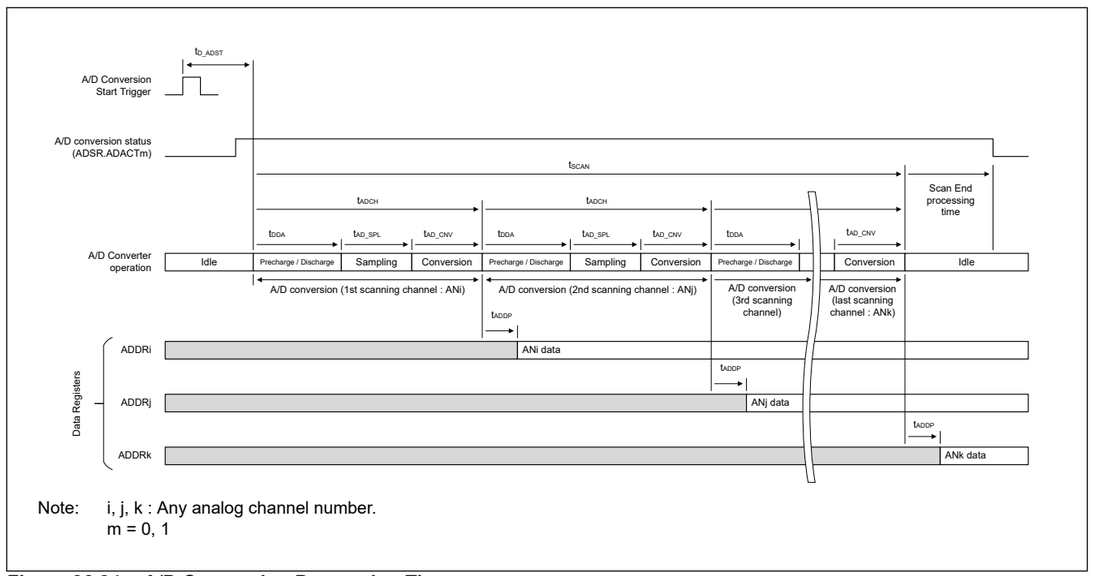
转换操作中的各种处理时间如表36.32、图36.34和图36.35所示。

Table 36.32 AD转换处理时间

Item		Symbol	处理时间
通道专用的采样保持处理时间	采样时间	t_{SH_SPL}	ADSHSTRm.SHSST[7:0] × ADCLK
	保持模式切换时间	t_{SH_HLD}	ADSHSTRm.SHHST[2:0] × ADCLK
断线检测辅助处理时间		t_{DDA}	[断线检测辅助功能无效时]● 0[断线检测辅助功能有效时]●
AD转换时间	采样时间	t_{AD_SPL}	ADSSTRp.SSTq[9:0] × ADCLK
	逐次逼近时间	t_{AD_CNV}	ADCNVSTR.CSTm[5:0] × ADCLK
AD转换数据处理时间	当ADCLK=PCLKA设置为1*1	t_{ADDP}	[不使用D换算值加法平均功能时]● 6ADCLK+2PCLKA[当使用D转换增值平均功能时]●
	上述以外		[不使用D-ConvertedValueAdditiveAverageFunction]● 7ADCLK+(5to6PCLKA)[使用AD-转换增值平均功能]●
AD转换总时间*3	频道转换时间*2	t_{ADCH}	$(t_{DDA} + t_{AD\_SPL} + t_{AD\_CNV}) \times N\_ADC \times ADCLK$
	扫描转换时间*4	t_{SCAN}	[不使用通道专用采样保持电路时]● ΣtADCH[使用通道专用采样保持电路时]●

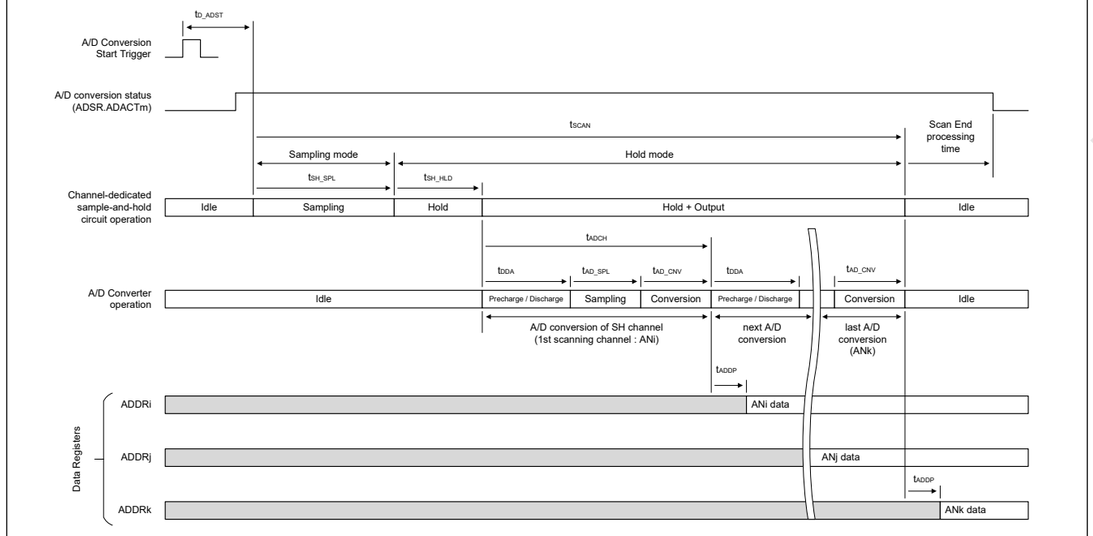
Note: n=0to8 m=0 1 p=0to7 q=0to15NADC:该值是根据ADDOPCRBx.ADC[3:0]（x=0到36）。如果不使用D-ConvertedValueAdditiveAverageFunction，则该值为1。

注1.当ADCLKCR.CLKSEL[1:0]=10b且ADCLKCR.DIVR[2:0]=000b设置时。
注2.它不包括通道专用的采样保持处理时间。
注3.不包括AD转换数据处理时间
注4.这是根据分配给扫描组的每个模拟通道的转换设置计算的通道转换时间(tADCH)的总和。如果使用通道专用的采样保持电路，还增加了通道专用的采样保持处理时间（tSH_SPL和tSH_HLD）。



Note: i, j, k : Any analog channel number.
m = 0, 1

Figure 36.34 A/D Conversion Processing Time

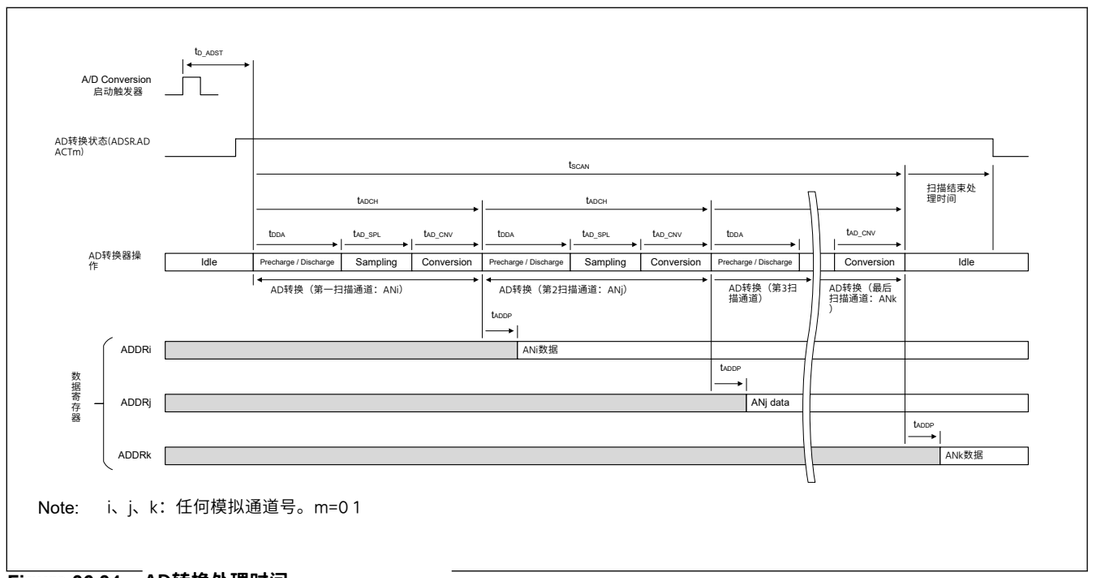


Note: i, j, k : Any analog channel number.
m = 0, 1

Figure 36.35 A/D Conversion Processing Time with Channel-dedicated sample-and-hold circuit

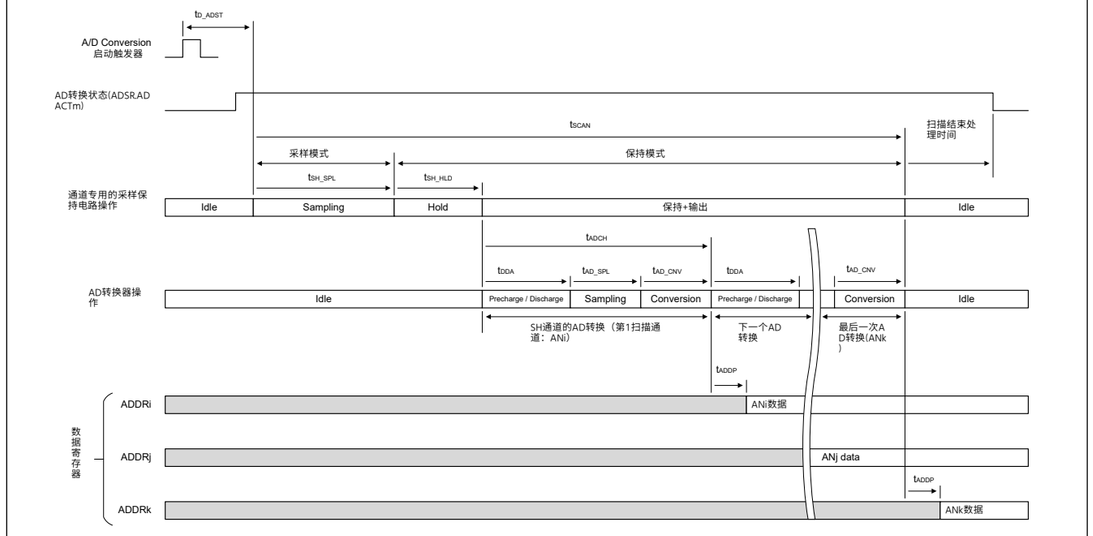
36.9.3 Scan End Processing Time

The scan end processing time and the forcibly stop processing time are shown in Table 36.33, Figure 36.36, Figure 36.37.



Note: i、j、k：任何模拟通道号。m=0 1

Figure 36.34 AD转换处理时间



Note: i、j、k：任何模拟通道号。m=0 1

Figure 36.35 通道专用采样保持电路的AD转换处理时间

36.9.3 扫描结束处理时间

扫描结束处理时间和强制停止处理时间见表36.33、图36.36、图36.37。

Table 36.33 Scan End Processing Time and Forcibly Stop Processing Time

Item		Symbol	Processing Time
Scan end processing time	Until reflected in the status register*1	t_{ED1}	t_{ADDP}
	Until output the FIFO data read request interrupt	t_{ED2}	t_{ED1} + 2 PCLKA
Forcibly Stop processing time	Forcibly stop trigger input processing time	t_{STOP_TRG}	[When ADCLK = PCLKA/1 is set]*2 ● Number of access cycles to I/O registers*3 + 1 PCLKA [Other than above] ● (Number of access cycles to I/O registers*3) + 1 PCLKA + (3 to 4 ADCLK)
	Wait Time for Synchronous Operation	t_{STOP_SYNC}	[When Synchronous Operation is disabled] (ADSYCR.ADSYDISm = 1) ● 0 [When Synchronous Operation is enabled] (ADSYCR.ADSYDISm = 0) ● 0 to ADSYCR.ADSYCYC[10:0] × ADCLK
	Forcibly stop processing time	t_{STOP}	[When ADCLK = PCLKA/1 is set]*2 (ADSYCR.ADSYDISm = 1) ● 4 PCLKA (ADSYCR.ADSYDISm = 0) ● 3 PCLKA [Other than above] (ADSYCR.ADSYDISm = 1) ● 4 PCLKA + (2 to 3 PCLKA) (ADSYCR.ADSYDISm = 0) ● 3 PCLKA + (2 to 3 PCLKA)

Note: m = 0, 1
Note 1. This is the time it takes for ADSCANENDSR.SCANENDFn = 1 (n = 0 to 8) or until an end-of-scan interrupt is generated.
Note 2. When ADCLKCR.CLKSEL[1:0] = 10b and ADCLKCR.DIVR[2:0] = 000b are set.
Note 3. It is the number of access cycles to ADSTOPR register. For more details about the number of access cycles for I/O registers, refer to section Appendix 3, I/O Registers.

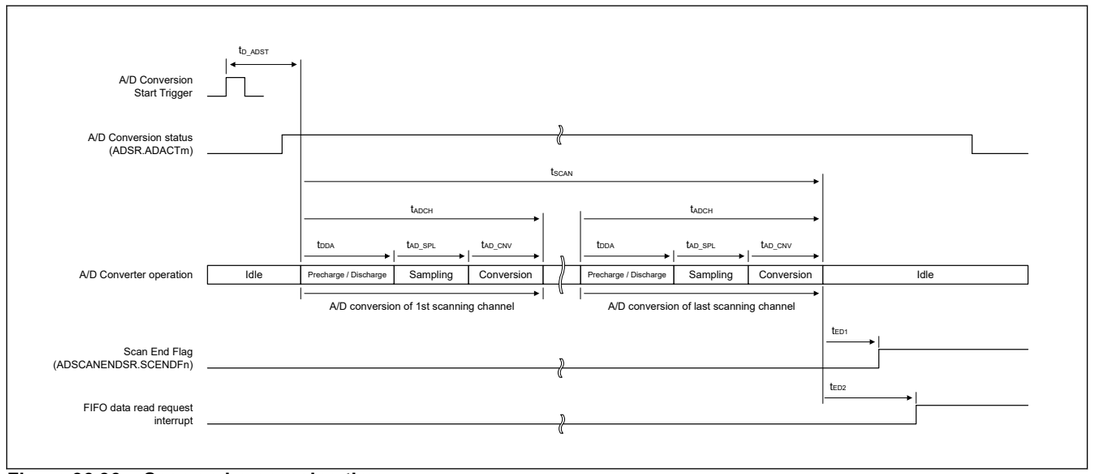


Figure 36.36 Scan end processing time

Table 36.33 扫描结束处理时间和强制停止处理时间

Item		Symbol	处理时间
扫描结束处理时间	直到反映在状态寄存器*1	t_{ED1}	t_{ADDP}
	直到输出FIFO数据读取请求中断	t_{ED2}	t_{ED1} + 2 PCLKA
强制停止处理时间	强制停止触发输入处理时间	t_{STOP_TRG}	[When ADCLK = PCLKA/1 is set]*2 ● IO寄存器的访问周期数*3 + 1 PCLKA [Other than above] ● （IO寄存器的访问周期数*3）+1PCLKA+（3到4ADCLK）
	同步操作的等待时间	t_{STOP_SYNC}	[禁用同步操作时](ADSYCR.ADSYDISm=1) ● 0[启用同步操作时](ADSYCR.ADSYDISm=0) ● LK
	强制停止处理时间	t_{STOP}	[When ADCLK = PCLKA/1 is set]*2 (ADSYCR.ADSYDISm = 1) ● 4 PCLKA (ADSYCR.ADSYDISm = 0) ● 3 PCLKA [Other than above] (ADSYCR.ADSYDISm = 1) ● 4 PCLKA + (2 to 3 PCLKA) (ADSYCR.ADSYDISm = 0) ● 3 PCLKA + (2 to 3 PCLKA)

Note: m = 0, 1
注1.这是ADSCANENDSR.SCANENDFn=1（n=0到8）或直到产生扫描结束中断所需的时间。
注2.当ADCLKCR.CLKSEL[1:0]=10b且ADCLKCR.DIVR[2:0]=000b设置时。
注3.它是访问ADSTOPR寄存器的周期数。有关IO寄存器访问周期数的更多详细信息，请参阅附录3，IO寄存器部分。

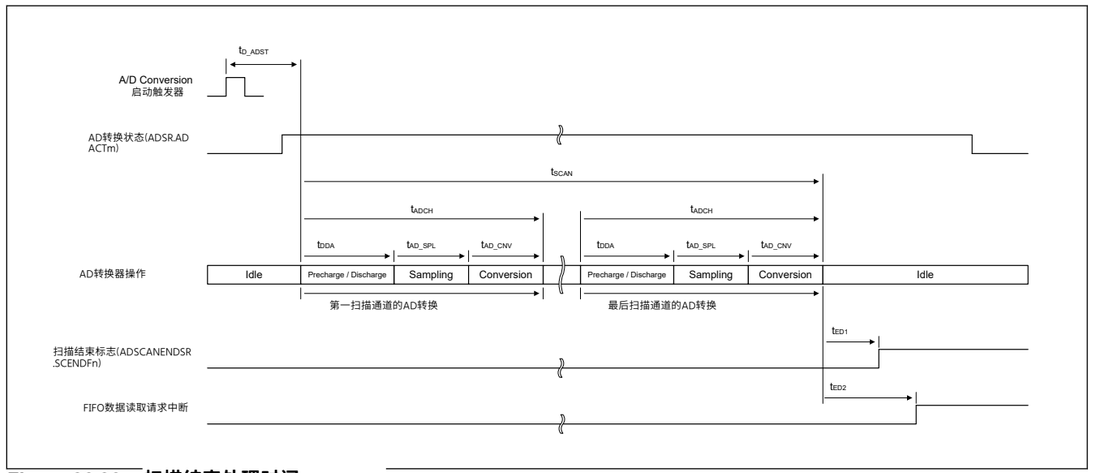
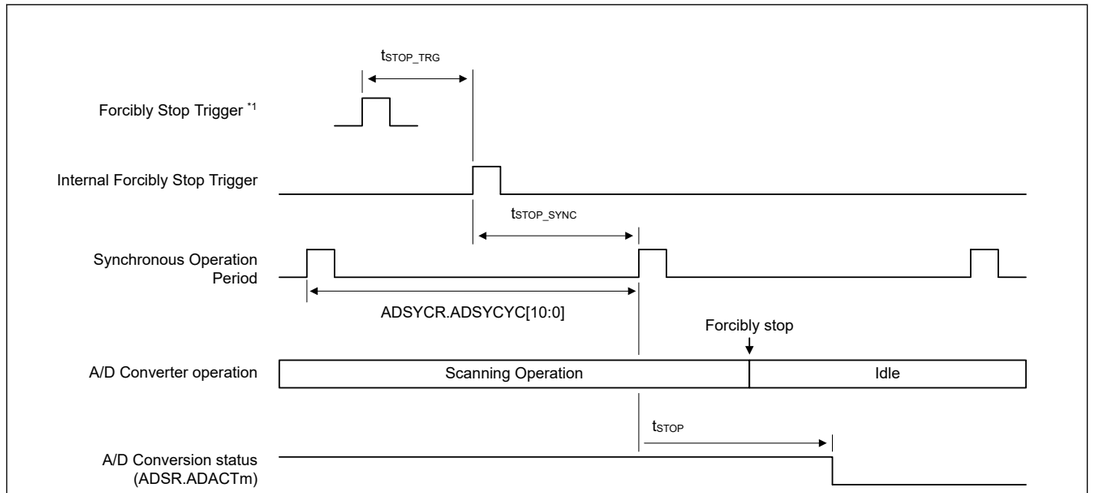


Figure 36.36 扫描结束处理时间



Note 1. It is generated by writting to ADSTOPR.ADSTROPm = 1. (m = 0, 1)

Figure 36.37 Force stop processing time

36.10 Usage Notes

36.10.1 Prohibitation of changing the operation settings during A/D conversion operation

The registers related to the operation setting of the A/D converter should be set while all A/D converters are stopped (ADSR.ADACTm = 0 and ADSR.CALACTm = 0 (m = 0, 1)). Changing (writing) of registers except for those listed below is prohibited during A/D conversion. If the operation setting is changed during A/D conversion, operation is not guaranteed.

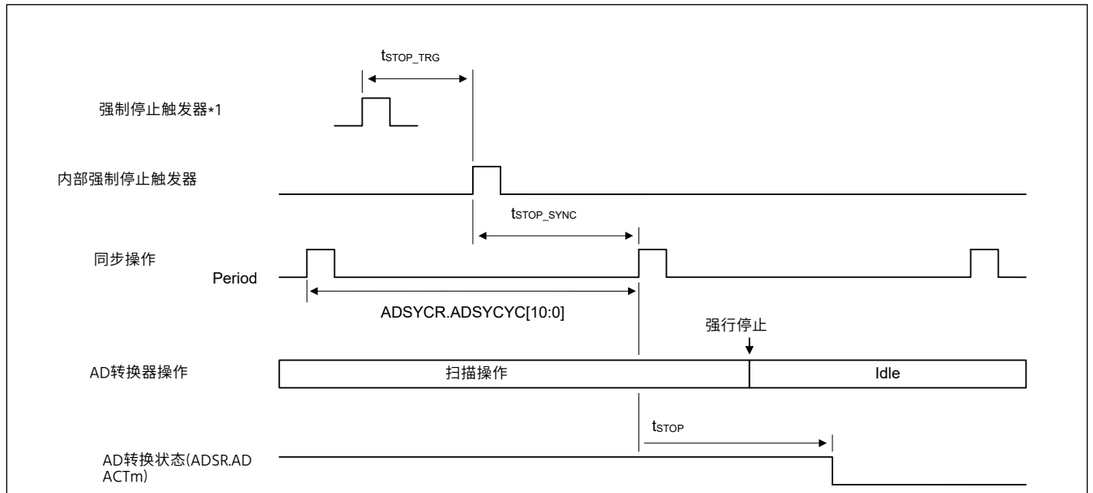
[Registers that can be written while the A/D converter is operating]

- Status Clear Registers
  - Status clear registers related to A/D converter operation (ADERSCR, ADCALSCR, ADCALENDSCR, ADSCANENDSCR)
  - A/D Conversion Overflow Status Clear Registers (ADOVFERSCR, ADOVFCHSCR0, ADOVFEXSCR)
  - Limiter Clip Status Clear Register (ADLIMGRSCR, ADLIMCHSCR0, ADLIMEXSCR)
  - Compare Match Status Clear Register (ADCMPTBSCR, ADCMPCHSCR0, ADCMPEXSCR)
  - FIFO Error Status Clear Register (ADFIFOERSCR)
- Software Trigger Register (ADSYSTR, ADSTRn (n = 0 to 8))
- A/D Converter Stop Register (ADSTOPR)
- A/D Converter Start Trigger Enable Register (ADTRGENR) *1

Note 1. Writing during operation is only permitted for disabling the trigger input (ADTRGENR.STTRGENn = 0 (n = 0 to 8)) in order to stop the A/D conversion. To avoid unintended operation, do not change the trigger input to Enable (ADTRGENR.STTRGENn = 1) during operation.

36.10.2 Usage Notes on Forced Stop of A/D Conversion

If you want to forcibly stop the A/D conversion operation, follow the procedure in section 36.5.4. Force stops the A/D conversion operation.



注1.它是通过写入ADSTOPR.ADSTROPm=1生成的。(m=0 1)

Figure 36.37 强制停止处理时间

36.10 使用说明

36.10.1 禁止在AD转换操作期间更改操作设置

与AD转换器的操作设置相关的寄存器应在所有AD转换器停止时设置（ADSR.ADACTm=0和ADSR.CALACTm=0(m=0 1)）。在AD转换过程中，禁止更改（写入）除以下列出的寄存器之外的寄存器。如果在AD转换期间更改操作设置，则无法保证操作。

[可以在AD转换器运行时写入的寄存器]

●状态清除寄存器

与AD转换器操作相关的状态清除寄存器
(ADERSCR, ADCALSCR, ADCALENDSCR, ADSCANENDSCR)

AD转换溢出状态清除寄存器
(ADOVFERSCR, ADOVFCHSCR0, ADOVFEXSCR)

限制器剪辑状态清除寄存器
(ADLIMGRSCR, ADLIMCHSCR0, ADLIMEXSCR)

比较匹配状态清除寄存器
(ADCMPTBSCR, ADCMPCHSCR0, ADCMPEXSCR)

FIFO错误状态清除寄存器(ADFIF OERSCR)

●软件触发寄存器(ADSYSTR ADSTRn(n=0to8))

●AD转换器停止寄存器(ADSTOPR)

●AD转换器启动触发使能寄存器(ADTRGENR)*1

注1.操作期间写入仅允许禁用触发输入(ADTRGENR.STTRGENn=0(n=0至8))以停止AD转换。为避免意外操作，请勿在操作期间将触发输入更改为启用(ADTRGENR.STTRGENn=1)。

36.10.2 强制停止AD转换的使用说明

如果要强制停止AD转换操作，请按照第36.5.4节中的步骤进行操作。强制停止AD转换操作。

36.10.3 Usage Notes on A/D data registers

When A/D conversion is performed multiple times on the same analog channel, A/D data register (ADDRn (n = 0 to 28) or A/D extended analog data register m (m = 0 to 2, 5 to 8) corresponding to that analog channel is overwritten at the later A/D conversion.

If you intend to keep the data for each A/D conversion for the same analog channel, perform one of the following methods.

- Read out data from registers at each scanning operation
  - At the end of scanning each scan group, read out the A/D conversion data of the analog channel that was subject to A/D conversion from ADDRn or ADEXDRm.
  - This method is effective if A/D conversion of the same analog channel is not performed more than once in the same scan group, and A/D conversion data can be read from the registers before the next scanning operation.
- Use FIFO function to hold data for each A/D conversion
  - By using FIFO, multiple A/D conversion data for the same analog channel can be kept.
  - Read out the A/D conversion data before FIFO overflow.

36.10.4 Settings for the Module-Stop Function

The Module Stop Control Register can enable or disable ADC operation. The ADC is initially stopped after a reset. The registers become accessible on release from the module-stop state.

Also refer to section 36.10.5. Restrictions on Entering and Releasing the Low-Power States in connection with this usage note.

36.10.5 Restrictions on Entering and Releasing the Low-Power States

Before entering the module-stop state or Software Standby mode, be sure to stop A/D conversion. In Addition, configure the A/D conversion not to start during the entering to the low power state.

To operate the A/D converter after the module-stop state or software standby mode is released, wait for the operation stabilization time specified in the Electrical Characteristics, execute Self-Calibration operation, and then start A/D conversion.

Also, when releasing the module-stop state again after entering to the module-stop state, make sure the shutdown time specified in the Electrical Characteristics has elapsed before releasing the module stop state.

Operations are not guaranteed if these restriction are violated.

36.10.6 Notes on board design

(1) Protection Circuit

To prevent the analog input pins from being destroyed by abnormal voltage such as excessive surge, take the following measures.

- Insert a capacitor between AVCC0 and AVSS0 and between VREFH0 and VREFL0.
- Connect a protection circuit to protect the analog input pins.

An example of a protection circuit is shown in Figure 36.38.

(2) Board design to ensure A/D conversion accuracy

In order to ensure the accuracy of A/D conversion, design the board considering the following:

- Analog circuits and digital circuits should be separated from each other as far as possible.
- Analog circuit signal lines and digital circuit signal lines should not intersect or be placed near each other.
- The analog input, analog reference power supply (VREFH0), analog reference ground (VREFL0), and analog power supply (AVCC0) should be separated from digital circuits using the analog ground (AVSS0).
- The analog ground (AVSS0) should be connected to a stable digital ground (VSS) on the board (single-point ground plane connection).

36.10.3 AD数据寄存器的使用注意事项

当对同一模拟通道进行多次AD转换时，对应于该模拟通道的AD数据寄存器(ADDRn(n=0到28)或AD扩展模拟数据寄存器m(m=0到2、5到8)将被覆盖在后来的AD转换。

如果您打算为同一模拟通道保留每次AD转换的数据，请执行以下方法之一。

●在每次扫描操作时从寄存器中读取数据

在每个扫描组扫描结束时，从ADDRn或ADXDRm中读出经过AD转换的模拟通道的AD转换数据。

此方法在同一扫描组中对同一模拟通道的AD转换不超过一次时有效，并且可以在下一次扫描操作之前从寄存器中读取AD转换数据。

●使用FIFO功能保存每次AD转换的数据

通过使用FIFO，可以保存同一模拟通道的多个AD转换数据。

在FIFO溢出之前读出AD转换数据。

36.10.4 模块停止功能的设置

模块停止控制寄存器可以启用或禁用ADC操作。ADC在复位后最初停止。寄存器在从模块停止状态释放时变得可访问。

另请参阅第36.10.5节。与本使用说明有关的进入和释放低功耗状态的限制。

36.10.5 进入和释放低功耗状态的限制

在进入模块停止状态或软件待机模式之前，请务必停止AD转换。此外，配置进入低功耗状态期间不启动AD转换。

要在模块停止状态或软件待机模式解除后操作AD转换器，请等待电气特性中指定的操作稳定时间，执行自校准操作，然后开始AD转换。

另外，在进入模块停止状态后再次解除模块停止状态时，请确保在解除模块停止状态之前已经过了电气特性中指定的关闭时间。

如果违反这些限制，则无法保证操作。

36.10.6 电路板设计注意事项

(1) 保护电路

为防止模拟输入引脚因过大浪涌等异常电压而损坏，请采取以下措施。

●在AVCC0和AVSS0之间以及VREFH0和VREFL0之间插入一个电容。

●连接保护电路以保护模拟输入引脚。

保护电路示例如图36.38所示。

(2) 板卡设计保证AD转换精度

为了保证AD转换的准确性，设计板子时考虑以下几点：

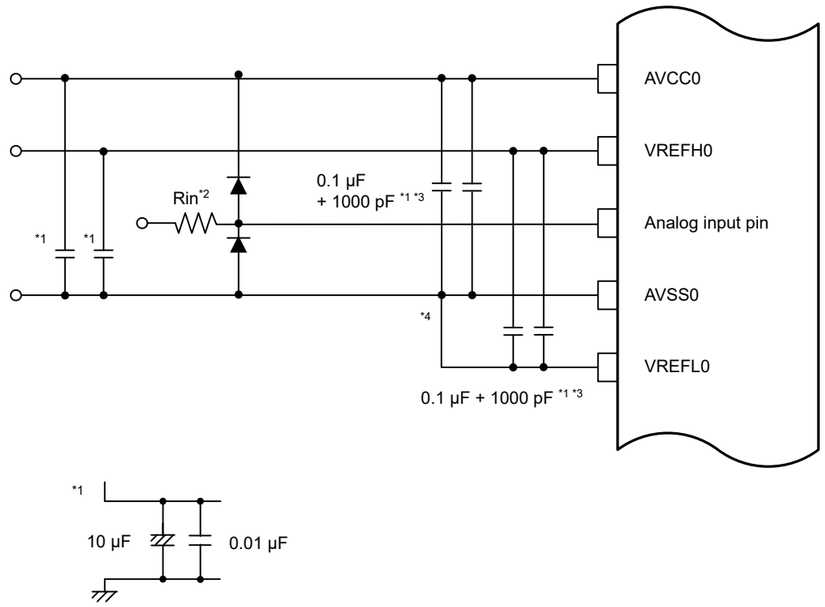
●模拟电路和数字电路应尽量分开。

●模拟电路信号线和数字电路信号线不能交叉或靠近。

●模拟输入、模拟参考电源（VREFH0）、模拟参考地（VREFL0）和模拟电源（AVCC0）应与使用模拟地（AVSS0）的数字电路分开。

●模拟地（AVSS0）应连接到板上稳定的数字地（VSS）（单点地平面连接）。

- Place a capacitor for noise filters between AVCC0 pin and AVSS0 pin and between VREFH0 pin and VREFL0 pin close to the pin and connect them. Also, connect AVSS0 and VREFL0 pins to the analog ground on the board as close to the pins as possible. An example of connection is shown in Figure 36.38.



Note 1. The values shown here are for reference only.
The appropriate values depend on your board design, operating conditions, etc.
Note 2. Rin: Signal source impedance
Note 3. To ensure the better A/D conversion accuracy, these capacitors must be place as close as possible to the appropriate pins.
Note 4. Connect to the analog ground of the board at the position as close as possible to the capacitor for noise filtering that ensure the A/D conversion accuracy.

Figure 36.38 Example of protection circuit and noise prevention

36.10.7 Notes on using analog channels to which the PGA is connected

When using an analog input pin to which a PGA is connected, refer to section 36.3.13.2. PGA operation setting.

36.10.8 Notes on Synchronous Operation

Synchronous Operation function is enabled in the initial state after reset released. If using Synchronous Operation function, follow the restrictions described in section 36.3.17. Synchronous Operation. If Synchronous Operation function is not used, disable Synchronous Operation in ADSYCR register.

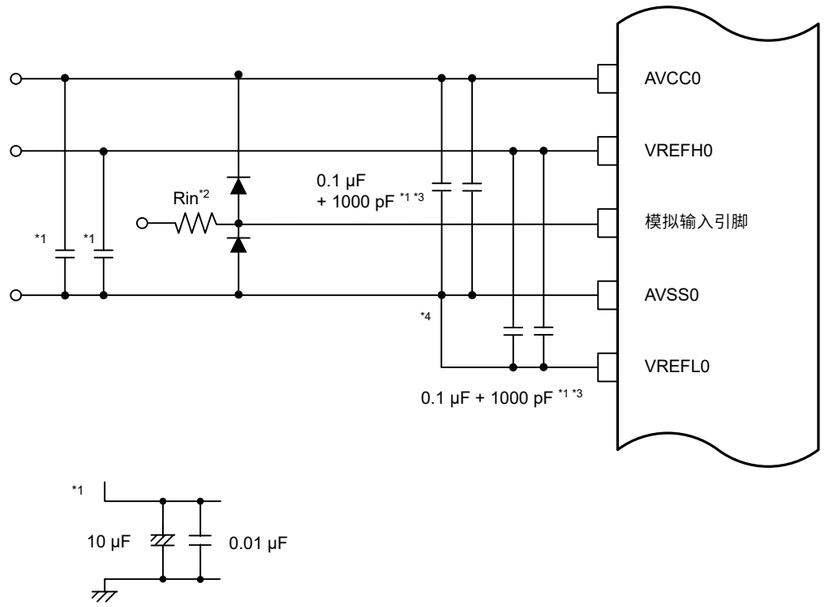
36.10.9 Notes on Channel-dedicated sample-and-hold circuit

When using Channel-dedicated sample-and-hold circuit, follow the restrictions. For more details, refer to section 36.3.14. Channel-Dedicated Sample-and Hold Circuit.

36.10.10 Prohibition of A/D conversions from multiple A/D converter to the same analogue signal source

To avoid degradation of the accuracy of the A/D conversion result, A/D conversion of the same analog channel (same analog signal source) from both ADC0 and ADC1 is prohibited, except for the self-diagnosis channel.

●在AVCC0引脚和AVSS0引脚之间以及VREFH0引脚和VREFL0引脚之间放置一个用于噪声滤波器的电容器靠近引脚并连接它们。此外，将AVSS0和VREFL0引脚连接到电路板上的模拟地，使其尽可能靠近引脚。连接示例如图36.38所示。



注1.此处显示的数值仅供参考。
适当的值取决于您的电路板设计、操作条件等。
注2.Rin：信号源阻抗
注3.为确保更好的AD转换精度，这些电容必须尽可能靠近相应的引脚放置。

注4.在尽可能靠近电容器的位置连接到电路板的模拟地，以确保AD转换精度的噪声过滤。

Figure 36.38 保护电路和噪声防止示例

36.10.7 使用连接PGA的模拟通道的注意事项

使用连接PGA的模拟输入引脚时，请参阅第36.3.13.2节。PGA操作设置。

36.10.8 同步操作注意事项

同步操作功能在复位释放后的初始状态下启用。如果使用同步操作功能，请遵循第36.3.17节中描述的限制。同步操作。如果不使用同步操作功能，请禁用ADSYCR寄存器中的同步操作。

36.10.9 通道专用采样保持电路注意事项

使用通道专用采样保持电路时，请遵守限制条件。有关详细信息，请参阅第36.3.14节。
通道专用采样保持电路。

36.10.10 禁止从多个AD转换器到同一个模拟信号源的AD转换

为避免AD转换结果精度下降，除自诊断通道外，禁止ADC0和ADC1对同一模拟通道（同一模拟信号源）进行AD转换。

If this restriction is violated, the A/D conversion results are not guaranteed because the A/D conversion accuracy of the target analog channel may deteriorate significantly.

36.10.11 Notes on A/D Conversion Start Trigger

A/D conversion start triggers for the same scan group are not accepted until scanning operation of the scan group is completed (in this case, A/D converter start triggers are ignored).

An A/D conversion trigger for the same scan group should be input after the scanning operation of its scan group is completed (ADSCANENDSR.SCANENDFn = 1 (n = 0 to 8)) and after a 6 PCLKA clock cycles or more has elapsed.

36.10.12 Notes on Self-Calibration

Observe the restrictions on Self-Calibration function. For more details, refer to section 36.3.6. Self-Calibration.

36.10.13 Notes on Group Priority Operation

Observe the restrictions when using Group Priority Operation. For more details, refer to section 36.3.16. Group Priority Operation.

36.10.14 Notes on PGA Output Monitor Function

There are restrictions when using the PGA output monitor function. For more details, refer to section 36.3.13. Programmable Gain Amplifier.

如果违反此限制，则无法保证AD转换结果，因为目标模拟通道的AD转换精度可能会显着下降。

36.10.11 AD转换开始触发注意事项

在扫描组的扫描操作完成之前，不接受同一扫描组的AD转换启动触发器（在这种情况下，忽略AD转换器启动触发器）。

在其扫描组的扫描操作完成（ADSCANENDSR.SCANENDFn=1（n=0至8））并且经过6个或更多PCLKA时钟周期后，应输入同一扫描组的AD转换触发。

36.10.12 自校准注意事项

遵守自校准功能的限制。有关详细信息，请参阅第36.3.6节。自校准。

36.10.13 群组优先操作注意事项

使用组优先操作时请遵守限制。有关详细信息，请参阅第36.3.16节。团体优先Operation.

36.10.14 PGA输出监控功能注意事项

使用PGA输出监控功能时有一些限制。有关详细信息，请参阅第36.3.13节。可编程增益放大器。

37. 12-Bit D/A Converter (DAC12)

37.1 Overview

The MCU provides a 12-bit D/A Converter (DAC12) with an output amplifier. Table 37.1 lists the DAC12 specifications, Figure 37.1 shows a block diagram, and Table 37.2 lists the I/O pins.

Table 37.1 DAC12 specifications

Parameter	Specifications
Resolution	12 bits
Output channels	4 channels
Module-stop function	Module-stop state can be set to reduce power consumption
Event link function (input)	The DA0, DA1, DA2 and DA3 conversion can be started on input of an event signal
D/A output amplifier control function	Controls whether the output amplifier (for both amplifier-through and amplifier-bias controls) is used
Destination of D/A output control function	Controls whether the output to the external pin or to the internal modules (ACMPHS) is used
TrustZone Filter	Security attribution can be set

37. 12-Bit D/A Converter (DAC12)

37.1 Overview

MCU提供带输出放大器的12位DA转换器(DAC12)。表37.1列出了DAC12规格，
图37.1显示了框图，表37.2列出了IO引脚。

Table 37.1 DAC12 specifications

Parameter	Specifications
Resolution	12 bits
输出通道	4 channels
Module-stop function	可设置模块停止状态以降低功耗
事件链接功能（输入）	DA0、DA1、DA2和DA3转换可以在输入事件信号时启动
DA输出放大器控制功能	控制是否使用输出放大器（用于放大器直通和放大器偏置控制）
DA输出控制功能的目的地	控制是使用外部引脚还是内部模块(ACMPHS)的输出
TrustZone Filter	可设置安全属性

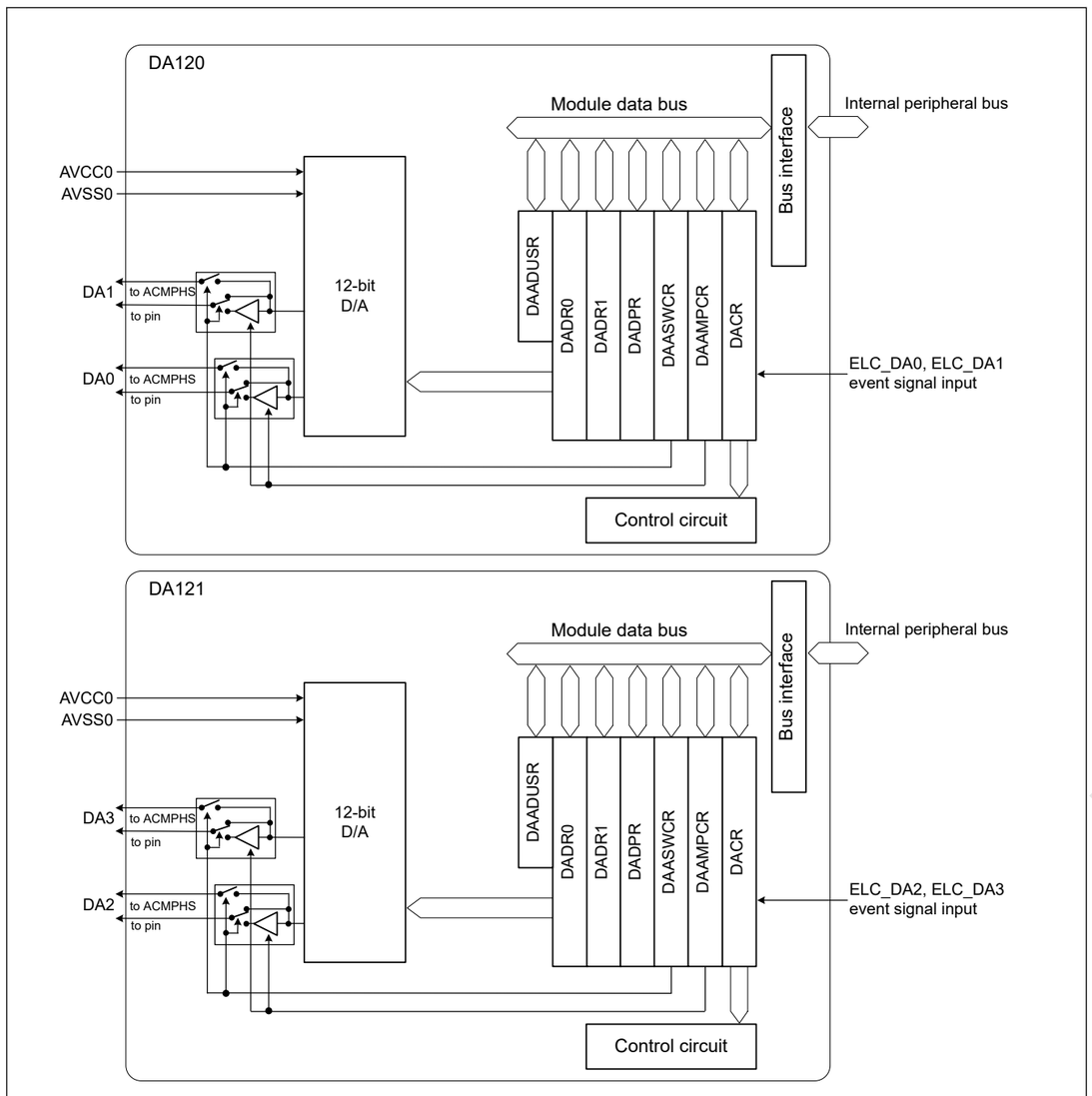


Figure 37.1 DAC12 block diagram

Table 37.2 lists the pin configuration of the DAC12.

Table 37.2 DAC12 I/O pins (1 of 2)

Pin name	I/O	Function
AVCC0	Input	• Analog power and analog reference top voltage supply pin for ADC and DAC12. • Connect to VCC when these modules are not used.
AVSS0	Input	• Analog ground and analog reference ground supply pin for ADC and DAC12. • Connect to VSS when these modules are not used.
DA0	Output	Channel 0 output pin for the analog signals processed by the DAC12
DA1	Output	Channel 1 output pin for the analog signals processed by the DAC12
DA2	Output	Channel 2 output pin for the analog signals processed by the DAC12

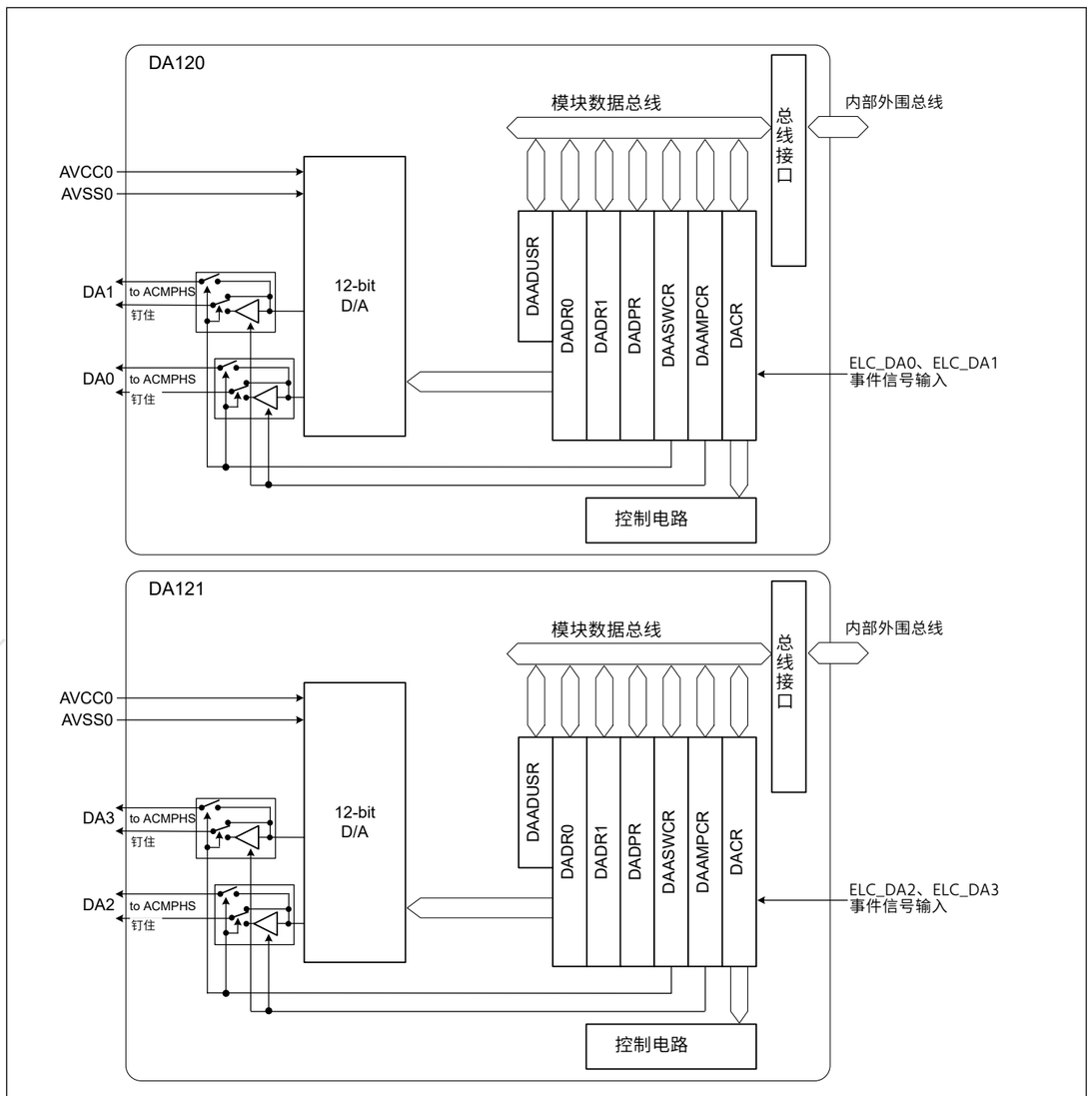


Figure 37.1 DAC12框图

表37.2列出了DAC12的引脚配置。

Table 37.2 DAC12IO引脚（2个中的1个）

引脚名称	I/O	Function
AVCC0	Input	• ADC和DAC12的模拟电源和模拟参考最高电压电源引脚。 • 不使用这些模块时连接到VCC。
AVSS0	Input	• ADC和DAC12的模拟地和模拟参考地电源引脚。 • 不使用这些模块时连接到VSS。
DA0	Output	DAC12处理的模拟信号的通道0输出引脚
DA1	Output	DAC12处理的模拟信号的通道1输出引脚
DA2	Output	DAC12处理的模拟信号的通道2输出引脚

Table 37.2 DAC12 I/O pins (2 of 2)

Pin name	I/O	Function
DA3	Output	Channel 3 output pin for the analog signals processed by the DAC12

37.2 Register Descriptions

37.2.1 DADRn : D/A Data Register n (n = 0, 1)

Base address: DAC12m = 0x4017_2000 + 0x0100 × m (m = 0, 1)

Offset address: 0x00 + 0x02 × n

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DADRn register is 16-bit read/write registers that store data for D/A conversion. When an analog output is enabled, the values in DADRn are converted and output to the analog output pins.

12-bit data can be formatted as left- or right-justified in the DADPR.DPSEL bit setting. In right-justified format (DADPR.DPSEL = 0), the lower 12 bits, [11:0], are valid. In left-justified format (DADPR.DPSEL = 1), the upper 12 bits, [15:4], are valid.

37.2.2 DACR : D/A Control Register

Base address: DAC12m = 0x4017_2000 + 0x0100 × m (m = 0, 1)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAOE1	DAOE0	DAE	—	—	—	—	—
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	—	These bits are read as 1. The write value should be 1.	R/W
5	DAE*1	D/A Enable 0: Control D/A conversion of channels 0 and 1 individually Control D/A conversion of channels 2 and 3 individually 1: Control D/A conversion of channels 0 and 1 collectively Control D/A conversion of channels 2 and 3 collectively	R/W
6	DAOE0	D/A Output Enable 0 0: Disable analog output of channel 0 (DA0) Disable analog output of channel 2 (DA2) 1: Enable D/A conversion of channel 0 (DA0) Enable D/A conversion of channel 2 (DA2)	R/W
7	DAOE1	D/A Output Enable 1 0: Disable analog output of channel 1 (DA1) Disable analog output of channel 3 (DA3) 1: Enable D/A conversion of channel 1 (DA1) Enable D/A conversion of channel 3 (DA3)	R/W

Note 1. This bit controls D/A conversion in combination with the DAOEi bit (i = 0, 1), which controls the output of the conversion results. For details, see Table 37.3.

Table 37.2 DAC12IO引脚（2个中的2个）

引脚名称	I/O	Function
DA3	Output	DAC12处理的模拟信号的通道3输出引脚

37.2 注册说明

37.2.1 DADRn:DA数据寄存器n(n=0 1)

Base address: DAC12m = 0x4017_2000 + 0x0100 × m (m = 0, 1)

Offset address: 0x00 + 0x02 × n

Bit position:	15															0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DADRn寄存器是16位读写寄存器，用于存储用于DA转换的数据。当模拟输出使能时，DADRn中的值被转换并输出到模拟输出引脚。

在DADPR.DPSEL位设置中，12位数据可以被格式化为左对齐或右对齐。在右对齐格式(DADPR.DPSEL=0)中，低12位[11:0]有效。在左对齐格式(DADPR.DPSEL=1)中，高12位[15:4]有效。

37.2.2 DACR:DA控制寄存器

Base address: DAC12m = 0x4017_2000 + 0x0100 × m (m = 0, 1)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAOE1	DAOE0	DAE	—	—	—	—	—
重置后的值:	0	0	0	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	—	这些位被读取为1。写入值应为1。	R/W
5	DAE*1	D/A Enable 0：分别控制通道0和1的DA转换单独控制通道2和3的DA转换 1：统一控制通道0和通道1的DA转换统一控制通道2和通道3的DA转换	R/W
6	DAOE0	DA输出使能0 0：禁用通道0的模拟输出（DA0）禁用通道2的模拟输出（DA2） 1：使能通道0（DA0）的DA转换使能通道2（DA2）的DA转换	R/W
7	DAOE1	DA输出使能1 0：禁用通道1的模拟输出（DA1）禁用通道3的模拟输出（DA3） 1：使能通道1（DA1）的DA转换使能通道3（DA3）的DA转换	R/W

注1.该位与DAOEi位(i=0 1)一起控制DA转换，DAOEi位控制转换结果的输出。详见表37.3。

Table 37.3 D/A conversion controls (m = 0)

DAE	DAOE1	DAOE0	Description
0	0	0	Disable D/A conversion and analog output pins (DA0, DA1)*1
		1	• Enable D/A conversion of channel 0 and disable D/A conversion of channel 1 • Enable analog output of channel 0 (DA0) and disable analog output of channel 1 (DA1)*1
	1	0	• Disable D/A conversion of channel 0 and enable D/A conversion of channel 1 • Disable analog output of channel 0 (DA0)*1 and enable analog output of channel 1 (DA1)
		1	• Enable D/A conversion of channels 0 and 1 • Enable analog output of channels 0 and 1 (DA0, DA1)
1	x	x	• Enable D/A conversion of channels 0 and 1 • Collective enable analog output of channels 0 and 1 (DA0, DA1)

Note: x: Don't care
Note 1. When analog output is disabled, the analog output signal is placed in the Hi-Z state.

Table 37.4 D/A conversion controls (m = 1)

DAE	DAOE1	DAOE0	Description
0	0	0	Disable D/A conversion and analog output pins (DA2, DA3)*1
		1	• Enable D/A conversion of channel 2 and disable D/A conversion of channel 3 • Enable analog output of channel 2 (DA2) and disable analog output of channel 3 (DA3)*1
	1	0	• Disable D/A conversion of channel 2 and enable D/A conversion of channel 3 • Disable analog output of channel 2 (DA2)*1 and enable analog output of channel 3 (DA3)
		1	• Enable D/A conversion of channels 2 and 3 • Enable analog output of channels 2 and 3 (DA2, DA3)
1	x	x	• Enable D/A conversion of channels 2 and 3 • Collective enable analog output of channels 2 and 3 (DA2, DA3)

Note: x: Don't care
Note 1. When analog output is disabled, the analog output signal is placed in the Hi-Z state.

DAE bit (D/A Enable)

The DAE bit controls D/A conversion, amplifier operation, and analog output in combination with the DAOEi bit (i = 0, 1) and the DAAMPCR.DAAMPi bit (i = 0, 1). See Table 37.5.

DAOEi bit (D/A Output Enable i)

The DAOEi bit (i = 0, 1) controls D/A conversion, amplifier operation, and analog output in combination with the DAE bit and DAAMPCR.DAAMPi bit (i = 0, 1). See Table 37.5.

When both the DAOEi bit (i = 0, 1) and DAE bit are 0, D/A conversion of channel i (i = 0, 1) is not processed, and no conversion result is output.

The event link function can be used to set the DAOEi bit to 1. The DAOE0 bit is set to 1 when the event specified in the ELSR12 register of the ELC (ELC_DA0 event) occurs, and output of the D/A conversion results starts. The DAOE1 bit is set to 1 when the event specified in the ELSR13 register of the ELC (ELC_DA1 event) occurs, and output of the D/A conversion results starts.

D/A conversions for channel 2 and 3 are controled by same bits in the register for the address when m = 1.

The setting of the ELC functions for channel 2 and 3 is possible in same manner too.

The event specified in the ELSR28 register of the ELC triggers the set of DAOE0 bit for address of m = 1 and the output of the D/A conversion for channel 2. The event specified in the ELSR29 triggers the set of DAOE1 bit and the output of the D/A conversion for channel 3.

Table 37.3 DA转换控制(m=0)

DAE	DAOE1	DAOE0	Description
0	0	0	禁用DA转换和模拟输出引脚(DA0 DA1)*1
		1	• 启用通道0的DA转换和禁用通道1的DA转换 • 启用通道0(DA0)的模拟输出和禁用通道1(DA1)的模拟输出*1
	1	0	• 禁用通道0的DA转换，启用通道1的DA转换 • 禁用通道0(DA0)*1的模拟输出并启用通道1(DA1)的模拟输出
		1	• 启用通道0和1的DA转换 • 启用通道0和1（DA0、DA1）的模拟输出
1	x	x	• 启用通道0和1的DA转换 • 通道0和1（DA0、DA1）的集体启用模拟输出

Note: x: Don't care
注1.当模拟输出禁用时，模拟输出信号置于Hi-Z状态。

Table 37.4 DA转换控制(m=1)

DAE	DAOE1	DAOE0	Description
0	0	0	禁用DA转换和模拟输出引脚(DA2 DA3)*1
		1	• 启用通道2的DA转换和禁用通道3的DA转换 • 启用通道2(DA2)的模拟输出和禁用通道3(DA3)的模拟输出*1
	1	0	• 禁用通道2的DA转换，启用通道3的DA转换 • 禁用通道2(DA2)*1的模拟输出并启用通道3(DA3)的模拟输出
		1	• 启用通道2和3的DA转换 • 启用通道2和3（DA2、DA3）的模拟输出
1	x	x	• 启用通道2和3的DA转换 • 共同启用通道2和3（DA2、DA3）的模拟输出

Note: x: Don't care
注1.当模拟输出禁用时，模拟输出信号置于Hi-Z状态。

DAE位（DA启用）

DAE位与DAOEi位(i=0 1)和DAAMPCR.DAAMPi位(i=0 1)一起控制DA转换、放大器操作和模拟输出。见表37.5。

DAOEi位（DA输出使能i）

DAOEi位(i=0 1)与DAE位和DAAMPCR.DAAMPi位(i=0 1)一起控制DA转换、放大器操作和模拟输出。见表37.5。

当DAOEi位(i=0 1)和DAE位均为0时，通道i(i=0 1)的DA转换不进行处理，也不输出转换结果。

事件链接功能可用于将DAOEi位设置为1。当在
发生ELC（ELC_DA0事件）的ELSR12寄存器，开始输出DA转换结果。当发生ELC的ELSR13寄存器中指定的事件（ELC_DA1事件）时，DAOE1位设置为1，并开始输出DA转换结果。

当m=1时，通道2和3的DA转换由地址寄存器中的相同位控制。

通道2和3的ELC功能的设置也可以以相同的方式进行。

ELC的ELSR28寄存器中指定的事件触发地址m=1的DAOE0位的设置和通道2的DA转换的输出。ELSR29中指定的事件触发DAOE1位的设置和通道2的输出D通道3的转换。

Table 37.5 D/A conversion and analog output control

DACR		DAAMPCR	DAASWCR	Channel i operation	Amplifier operation of channel i	Analog external output of channel i*1	Analog internal output of channel i*2
DAE	DAOEi	DAAMPi	DAASWi				
0	0	x	x	Stop	Stop	Hi-Z	Hi-Z
0	1	0	0	Run	Stop	Amplifier-through	Hi-Z
0	1	0	1	Run	Stop	Hi-Z	Amplifier-through
0	1	1	0	Run	Run	Amplifier output	Hi-Z
0	1	1	1	Run	Run	Hi-Z	Hi-Z
1	x	0	0	Run	Stop	Amplifier-through	Hi-Z
1	x	0	1	Run	Stop	Hi-Z	Amplifier-through
1	x	1	0	Run	Run	Amplifier output	Hi-Z
1	x	1	1	Run	Run	Hi-Z	Hi-Z

Note: x : Don't care
Note 1. output to pin
Note 2. output to ACMPHS

37.2.3 DADPR : DADRn Format Select Register

Base address: DAC12m = 0x4017_2000 + 0x0100 × m (m = 0, 1)

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSEL	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	DPSEL	DADRn Format Select 0: Right-justified format 1: Left-justified format	R/W

37.2.4 DAAMPCR : D/A Output Amplifier Control Register

Base address: DAC12m = 0x4017_2000 + 0x0100 × m (m = 0, 1)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAAMP1	DAAMP0	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	DAAMP0	Amplifier Control 0 0: Do not use channel 0 output amplifier (m = 0) Do not use channel 2 output amplifier (m = 1) 1: Use channel 0 output amplifier (m = 0) Use channel 2 output amplifier (m = 1)	R/W

Table 37.5 DA转换和模拟输出控制

DACR		DAAMPCR	DAASWCR	通道i操作	通道i的放大器操作	通道i的模拟外部输出*1	通道i的模拟内部输出*2
DAE	DAOEi	DAAMPi	DAASWi				
0	0	x	x	Stop	Stop	Hi-Z	Hi-Z
0	1	0	0	Run	Stop	Amplifier-through	Hi-Z
0	1	0	1	Run	Stop	Hi-Z	Amplifier-through
0	1	1	0	Run	Run	放大器输出	Hi-Z
0	1	1	1	Run	Run	Hi-Z	Hi-Z
1	x	0	0	Run	Stop	Amplifier-through	Hi-Z
1	x	0	1	Run	Stop	Hi-Z	Amplifier-through
1	x	1	0	Run	Run	放大器输出	Hi-Z
1	x	1	1	Run	Run	Hi-Z	Hi-Z

Note: x：不在乎
注1.输出到引脚
注2.输出到ACMPHS

37.2.3 DADPR:DADRn格式选择寄存器

Base address: DAC12m = 0x4017_2000 + 0x0100 × m (m = 0, 1)

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSEL	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	这些位被读取为0。写入值应为0。	R/W
7	DPSEL	DADRn格式选择 0: Right-justified format 1: Left-justified format	R/W

37.2.4 DAAMPCR:DA输出放大器控制寄存器

Base address: DAC12m = 0x4017_2000 + 0x0100 × m (m = 0, 1)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAAMP1	DAAMP0	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	这些位被读取为0。写入值应为0。	R/W
6	DAAMP0	放大器控制0 0：不使用通道0输出放大器（m=0）不使用通道2输出放大器（m=1） 1：使用通道0输出放大器（m=0）使用通道2输出放大器（m=1）	R/W

Bit	Symbol	Function	R/W
7	DAAMP1	Amplifier Control 1 0: Do not use channel 1 output amplifier (m = 0) Do not use channel 3 output amplifier (m = 1) 1: Use channel 1 output amplifier (m = 0) Use channel 3 output amplifier (m = 1)	R/W

The DAAMPCR register selects D/A output with or without using the amplifier.

DAAMP0 bit (Amplifier Control 0)

When the DAAMP0 bit is 0, analog values are output for D/A output of channel 0 (m = 0) and channel 2 (m = 1) without using the amplifier. When the DAAMP0 bit is 1, analog values are output for D/A output of channel 0 (m = 0) and channel 2 (m = 1) through the amplifier.

When both the DACR.DAE and DACR.DAOE0 bits are 0, the amplifier is not used regardless of the setting of the DAAMP0 bit. See Table 37.5 for details.

DAAMP1 bit (Amplifier Control 1)

When the DAAMP1 bit is 0, analog values are output for D/A output of channel 1 (m = 0) and channel 3 (m = 1) without using the amplifier. When the DAAMP1 bit is 1, analog values are output for D/A output of channel 1 (m = 0) and channel 3 (m = 1) through the amplifier.

When both the DACR.DAE and DACR.DAOE1 bits are 0, the amplifier is not used regardless of the setting of the DAAMP1 bit. See Table 37.5 for details.

37.2.5 DAASWCR : D/A Amplifier Stabilization Wait Control Register

Base address: DAC12m = 0x4017_2000 + 0x0100 × m (m = 0, 1)

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAASW1	DAASW0	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5	—	These bits are read as 0. The write value should be 0.	R/W
6	DAASW0	D/A Amplifier Stabilization Wait 0 and D/A internal output control 0: For output to external pin: Amplifier stabilization wait off (output) for channel 0 (m = 0) and channel 2 (m = 1) For output to internal module: Disable output for channel 0 (m = 0) and channel 2 (m = 1) 1: For output to external pin: Amplifier stabilization wait on (high-Z) for channel 0 (m = 0) and channel 2 (m = 1) For output to internal module: Enable output for channel 0 (m = 0) and channel 2 (m = 1)	R/W
7	DAASW1	D/A Amplifier Stabilization Wait 1 and D/A internal output control 0: For output to external pin: Amplifier stabilization wait off (output) for channel 1 (m = 0) and channel 3 (m = 1) For output to internal module: Disable output for channel 1 (m = 0) and channel 3 (m = 1) 1: For output to external pin: Amplifier stabilization wait on (high-Z) for channel 1 (m = 0) and channel 3 (m = 1) For output to internal module: Enable output for channel 1 (m = 0) and channel 3 (m = 1)	R/W

The DAASWCR register controls D/A output with the output amplifier or D/A output for internal modules. This register is used in the initialization procedure to wait for stabilization of the D/A output amplifier. Each bit in DAASWCR should be set to 1 when both the DACR.DAE bit and the DACR.DAOEi (i = 0, 1) bit are 0. See section 37.6.5. Initialization Procedure with the Output Amplifier.

Bit	Symbol	Function	R/W
7	DAAMP1	放大器控制1 0：不使用通道1输出放大器（m=0）不使用通道3输出放大器（m=1） 1：使用通道1输出放大器（m=0）使用通道3输出放大器（m=1）	R/W

DAAMPCR寄存器选择使用或不使用放大器的DA输出。

DAAMP0位（放大器控制0）

当DAAMP0位为0时，不使用放大器输出通道0(m=0)和通道2(m=1)的DA输出的模拟值。当DAAMP0位为1时，通过放大器为通道0(m=0)和通道2(m=1)的DA输出输出模拟值。

当DACR.DAE和DACR.DAOE0位都为0时，无论设置如何都不会使用放大器DAAMP0位。详见表37.5。

DAAMP1位（放大器控制1）

当DAAMP1位为0时，不使用放大器输出通道1(m=0)和通道3(m=1)的DA输出的模拟值。当DAAMP1位为1时，通过放大器为通道1(m=0)和通道3(m=1)的DA输出输出模拟值。

当DACR.DAE和DACR.DAOE1位都为0时，无论设置如何都不会使用放大器DAAMP1位。详见表37.5。

37.2.5 DAASWCR:DA放大器稳定等待控制寄存器

Base address: DAC12m = 0x4017_2000 + 0x0100 × m (m = 0, 1)

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAASW1	DAASW0	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5	—	这些位被读取为0。写入值应为0。	R/W
6	DAASW0	DA放大器稳定等待0和DA内部输出控制 0：输出到外部引脚： 通道0(m=0)和通道2(m=1)的放大器稳定等待关闭（输出） 对于内部模块的输出： 禁用通道0(m=0)和通道2(m=1)的输出 1：输出到外部引脚： 通道0(m=0)和通道2(m=1)的放大器稳定等待(high-Z) 对于内部模块的输出： 启用通道0(m=0)和通道2(m=1)的输出	R/W
7	DAASW1	DA放大器稳定等待1和DA内部输出控制 0：输出到外部引脚： 通道1(m=0)和通道3(m=1)的放大器稳定等待关闭（输出） 对于内部模块的输出： 禁用通道1(m=0)和通道3(m=1)的输出 1：输出到外部引脚： 通道1(m=0)和通道3(m=1)的放大器稳定等待(high-Z) 对于内部模块的输出： 启用通道1(m=0)和通道3(m=1)的输出	R/W

DAASWCR寄存器通过输出放大器控制DA输出或用于内部模块的DA输出。该寄存器在初始化过程中用于等待DA输出放大器的稳定。当DACR.DAE位和DACR.DAOEi(i=0 1)位均为0时，DAASWCR中的每个位都应设置为1。请参见第37.6.5节。输出放大器的初始化程序。

DAASW0 bit (D/A Amplifier Stabilization Wait 0)

Set the DAASW0 bit to 1 in the initialization procedure to wait for the stabilization of the D/A channel 0 and 2 output amplifier. When DAASW0 is set to 1, D/A conversion operates, but the conversion result of D/A is not output from channel 0 to the DA0 pin (m = 0) and channel 2 to the DA2 pin (m = 1). When the DAASW0 bit is 0, the stabilization wait time stops, and the D/A conversion result of channel 0 (m = 0) and channel 2 (m = 1) is output through the output amplifier to the DA0 pin (m = 0) and DA2 pin (m = 1). When the amplifier is not used (DAAMPCR.DAAMP0 bit is 0) and DAASW0 is set to 1, D/A conversion result of channel 0 (m = 0) and channel 2 (m = 1) is output to the internal modules.

DAASW1 bit (D/A Amplifier Stabilization Wait 1)

Set the DAASW1 bit to 1 in the initialization procedure to wait for the stabilization of the D/A channel 1 and 3 output amplifier. When DAASW1 is set to 1, D/A conversion operates, but the conversion result of D/A is not output from channel 1 to the DA1 pin (m = 0) and channel 3 to the DA3 pin (m = 1). When the DAASW1 bit is 0, the stabilization wait time stops, and the D/A conversion result of channel 1 (m = 0) and channel 3 (m = 1) is output through the output amplifier to the DA1 pin (m = 0) and DA3 pin (m = 1). When the amplifier is not used (DAAMPCR.DAAMP1 bit is 0) and DAASW1 is set to 1, D/A conversion result of channel 1 (m = 0) and channel 3 (m = 1) is output to the internal modules.

37.3 Operation

The DAC12 includes D/A conversion circuits for four channels, each of which can operate independently. When the DAOEn bit (n = 0, 1) in DACR is set to 1, DAC12 is enabled and the conversion result is output.

This following example shows D/A conversion on channel 0. Figure 37.2 shows the timing of this operation.

To process D/A conversion on channel 0:

1. Set the data for D/A conversion in the DADR0 register and the data format in the DADPR.DPSEL bit.
2. Set the DACR.DAOE0 bit to 1 to start D/A conversion. The conversion result is output from the analog output pin DA0 after the conversion time t_{DCONV} elapses. The conversion result continues to be output until DADR0 is written to again or the DAOE0 bit is set to 0. The output value (reference) is expressed by the following formula:

$$\frac{\text{Setting in DADR0}}{4096} \times AVCC0$$

3. To start conversion again, write another value to DADR0. The conversion result is output after the conversion time t_{DCONV} elapses.
4. To disable analog output, set the DAOE0 bit to 0.

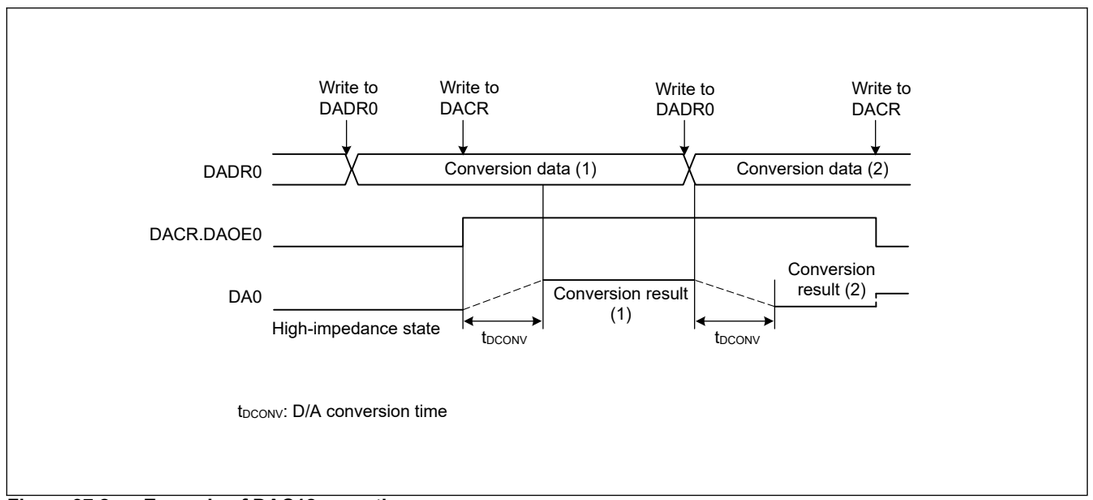


Figure 37.2 Example of DAC12 operation

DAASW0位（DA放大器稳定等待0）

在初始化过程中将DAASW0位设置为1，以等待DA通道0和2输出放大器稳定。当DAASW0设置为1时，DA转换操作，但DA的转换结果不从通道0输出到DA0引脚（m=0）和通道2到DA2引脚（m=1）。当DAASW0位为0时，稳定等待时间停止，通道0（m=0）和通道2（m=1）的DA转换结果通过输出放大器输出到DA0引脚（m=0）和DA2引脚（m=1）。当不使用放大器（DAAMPCR.DAAMP0位为0）且DAASW0设置为1时，将通道0（m=0）和通道2（m=1）的DA转换结果输出到内部模块。

DAASW1位（DA放大器稳定等待1）

在初始化过程中将DAASW1位设置为1，以等待DA通道1和3输出放大器稳定。当DAASW1设置为1时，DA转换操作，但DA的转换结果不从通道1输出到DA1引脚（m=0）和通道3输出到DA3引脚（m=1）。当DAASW1位为0时，稳定等待时间停止，通道1（m=0）和通道3（m=1）的DA转换结果通过输出放大器输出到DA1引脚（m=0）和DA3引脚（m=1）。当不使用放大器（DAAMPCR.DAAMP1位为0）且DAASW1设置为1时，通道1（m=0）和通道3（m=1）的DA转换结果输出到内部模块。

37.3 Operation

DAC12包括四个通道的DA转换电路，每个通道都可以独立工作。当。。。的时候
DACR中的DAOEn位(n=0 1)设置为1，使能DAC12并输出转换结果。

以下示例显示了通道0上的DA转换。图37.2显示了此操作的时序。

在通道0上处理DA转换：

1.在DADR0寄存器中设置用于DA转换的数据，在DADPR.DPSEL位中设置数据格式。

2.将DACR.DAOE0位设置为1以启动DA转换。经过转换时间tDCONV后，转换结果从模拟输出引脚DA0输出。转换结果继续输出，直到再次写入DADR0或将DAOE0位设置为0。输出值（参考值）由以下公式表示：

$$\frac{\text{DADR04096中的设置}}{4096} \times AVCC0$$

3.要再次开始转换，向DADR0写入另一个值。在经过转换时间tDCONV后输出转换结果。

4.要禁用模拟输出，请将DAOE0位设置为0。

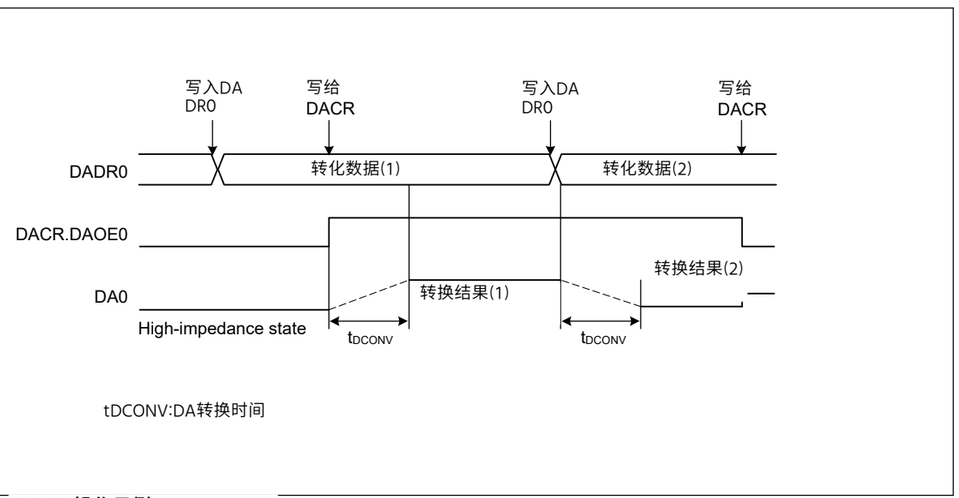


Figure 37.2 DAC12操作示例

37.4 Event Link Operation Setting Procedure

This section describes the procedures used in event link operation.

37.4.1 DA0 Event Link Operation Setting Procedure

To set up DA0 event link operation:

1. Set the DADPR.DPSEL bit and the data for D/A conversion in the DADR0 register.
2. Set the ELC_DA0 event signal to be linked to each peripheral module in the ELSR12 register.
3. Set the ELCR.ELCON bit to 1. This enables event link operation for all modules with the event link function selected.
4. Set the event output source module to activate the event link. After the event is output from the module, the DACR.DAOE0 bit becomes 1, and D/A conversion starts on channel 0.
5. Set the ELSR12 register to 0x0000 to stop event link operation of DAC12 channel 0. All event link operation is stopped when the ELCR.ELCON bit is set to 0.

37.4.2 DA1 Event Link Operation Setting Procedure

To set up DA1 event link operation:

1. Set the DADPR.DPSEL bit and set the data for D/A conversion in the DADR1 register.
2. Set the ELC_DA1 event signal to be linked to each peripheral module in the ELSR13 register.
3. Set the ELCR.ELCON bit to 1. This enables the event link operation for all modules with the event link function selected.
4. Set the event output source module to activate the event link. After the event is output from the module, the DACR.DAOE1 bit is becomes 1, and D/A conversion starts on channel 1.
5. Set the ELSR13 register to 0x0000 to stop event link operation on DAC12 channel 1. All event link operation is stopped when the ELCR.ELCON bit is set to 0.

37.4.3 DA2 Event Link Operation Setting Procedure

To set up DA2 event link operation:

1. Set the DADPR.DPSEL bit and the data for D/A conversion in the DADR0 register.
2. Set the ELC_DA2 event signal to be linked to each peripheral module in the ELSR28 register.
3. Set the ELCR.ELCON bit to 1.
   This enables event link operation for all modules with the event link function selected.
4. Set the event output source module to activate the event link.
   After the event is output from the module, the DACR.DAOE0 bit becomes 1, and D/A conversion starts on channel 2.
5. Set the ELSR28 register to 0x0000 to stop event link operation of DAC12 channel 2.
   All event link operation is stopped when the ELCR.ELCON bit is set to 0.

37.4.4 DA3 Event Link Operation Setting Procedure

To set up DA3 event link operation:

1. Set the DADPR.DPSEL bit and set the data for D/A conversion in the DADR1 register.
2. Set the ELC_DA3 event signal to be linked to each peripheral module in the ELSR29 register.
3. Set the ELCR.ELCON bit to 1.
   This enables the event link operation for all modules with the event link function selected.
4. Set the event output source module to activate the event link.
   After the event is output from the module, the DACR.DAOE1 bit becomes 1, and D/A conversion starts on channel 3.
5. Set the ELSR29 register to 0x0000 to stop event link operation on DAC12 channel 3.
   All event link operation is stopped when the ELCR.ELCON bit is set to 0.

37.4 事件链接操作设置步骤

本节介绍事件链接操作中使用的过程。

37.4.1 DA0事件链接操作设置步骤

设置DA0事件链接操作：

1.设置DADPR.DPSEL位和DADR0寄存器中用于DA转换的数据。

2.在ELSR12寄存器中设置ELC_DA0事件信号链接到每个外围模块。

3.将ELCR.ELCON位设置为1。这将为所有选择了事件链接功能的模块启用事件链接操作。

4.设置事件输出源模块，激活事件链接。模块输出事件后，DACR.DAOE0位变为1，通道0开始DA转换。

5.将ELSR12寄存器设置为0x0000以停止DAC12通道0的事件链接操作。所有事件链接操作在ELCR.ELCON位设置为0时停止。

37.4.2 DA1事件链接操作设置步骤

设置DA1事件链接操作：

1.设置DADPR.DPSEL位并在DADR1寄存器中设置用于DA转换的数据。

2.在ELSR13寄存器中设置ELC_DA1事件信号链接到每个外围模块。

3.将ELCR.ELCON位设置为1。这将为所有选择了事件链接功能的模块启用事件链接操作。

4.设置事件输出源模块，激活事件链接。模块输出事件后，DACR.DAOE1位变为1，通道1开始DA转换。

5.将ELSR13寄存器设置为0x0000以停止DAC12通道1上的事件链接操作。所有事件链接操作在ELCR.ELCON位设置为0时停止。

37.4.3 DA2事件链接操作设置步骤

设置DA2事件链接操作：

1.设置DADPR.DPSEL位和DADR0寄存器中用于DA转换的数据。

2.在ELSR28寄存器中设置ELC_DA2事件信号链接到每个外围模块。

3.将ELCR.ELCON位设置为1。
这将启用所有模块的事件链接操作，并选择了事件链接功能。

4.设置事件输出源模块，激活事件链接。
模块输出事件后，DACR.DAOE0位变为1，通道2开始DA转换。

5.将ELSR28寄存器设置为0x0000以停止DAC12通道2的事件链接操作。所有事件链接操作在ELCR.ELCON位设置为0时停止。

37.4.4 DA3事件链接操作设置步骤

设置DA3事件链接操作：

1.设置DADPR.DPSEL位并在DADR1寄存器中设置用于DA转换的数据。

2.在ELSR29寄存器中设置ELC_DA3事件信号链接到每个外围模块。

3.将ELCR.ELCON位设置为1。
这将启用所有已选择事件链接功能的模块的事件链接操作。

4.设置事件输出源模块，激活事件链接。
模块输出事件后，DACR.DAOE1位变为1，通道3开始DA转换。

5.将ELSR29寄存器设置为0x0000以停止DAC12通道3上的事件链接操作。所有事件链接操作在ELCR.ELCON位设置为0时停止。

37.5 Usage Notes on Event Link Operation

- When the event link function is used, do not use the amplifier output function.
- When the event link function is used, set the DACR.DAE bit to 0.
- When the event specified for the ELC_DA0 event signal is generated while a write to the DACR.DAOE0 bit is performed, the write cycle is stopped, and the generated event takes precedence in setting the bit to 1.
- When the event specified for the ELC_DA1 event signal is generated while a write to the DACR.DAOE1 bit is performed, the write cycle is stopped, and the generated event takes precedence in setting the bit to 1.
- When the event specified for the ELC_DA2 event signal is generated while a write to the DACR.DAOE0 (m = 1) bit is performed, the write cycle is stopped, and the generated event takes precedence in setting the bit to 1.
- When the event specified for the ELC_DA3 event signal is generated while a write to the DACR.DAOE1 (m = 1) bit is performed, the write cycle is stopped, and the generated event takes precedence in setting the bit to 1.

37.6 Usage Notes

37.6.1 Settings for the Module-Stop Function

DAC12 operation can be disabled or enabled using the Module Stop Control Register. The DAC12 is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

37.6.2 DAC12 Operation in the Module-Stop State

When the MCU enters the module-stop state with D/A conversion enabled, the D/A outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current must be reduced in the module-stop state, disable D/A conversion by setting the DACR.DAOE1, DAOE0, and DAE bits to 0.

37.6.3 DAC12 Operation in Software Standby Mode

When the MCU enters Software Standby mode with D/A conversion enabled, the D/A outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current must be reduced in Software Standby mode, disable D/A conversion by setting the DACR.DAOE1, DAOE0, and DAE bits to 0.

37.6.4 Constraint on Entering Deep Software Standby Mode

When the MCU enters Deep Software Standby mode with D/A conversion enabled, the outputs of the DAC12 are placed in a high impedance state.

37.6.5 Initialization Procedure with the Output Amplifier

Use the following initialization procedures with the output amplifier. The example shows the case for channel 0.

To initialize the DAC12 with the output amplifier:

1. Write 0x0000 to the DADR0 register.
2. Set the DAASWCR.DAASW0 bit to 1.
3. Set the DAAMPCR.DAAMP0 bit to 1.
4. Set the DACR.DAE bit or the DACR.DAOE0 bit to 1 to start operation of the amplifier.
5. Clear the DAASWCR.DAASW0 bit to 0 after waiting for the duration of D/A conversion time t_{DCONV}.
6. Write the value to be converted in the DADR0 register.

37.5 事件链接操作使用说明

●使用事件链接功能时，请勿使用放大器输出功能。

●使用事件链接功能时，将DACR.DAE位设置为0。

●如果在执行对DACR.DAOE0位的写入时产生了为ELC_DA0事件信号指定的事件，则写入周期停止，并且产生的事件优先将该位设置为1。

●如果在执行对DACR.DAOE1位的写入时产生了为ELC_DA1事件信号指定的事件，则写入周期停止，并且产生的事件优先将该位设置为1。

●如果在写入DACR.DAOE0(m=1)位的同时生成了为ELC_DA2事件信号指定的事件，则写入周期停止，并且生成的事件优先将该位设置为1。

●如果在执行对DACR.DAOE1(m=1)位的写入时生成了为ELC_DA3事件信号指定的事件，则写入周期停止，并且生成的事件优先将该位设置为1。

37.6 使用说明

37.6.1 模块停止功能的设置

可以使用模块停止控制寄存器禁用或启用DAC12操作。DAC12在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

37.6.2 DAC12在模块停止状态下的操作

当MCU进入模块停止状态并启用DA转换时，DA输出保持不变，模拟电源电流与DA转换时相同。如果在模块停止状态下必须降低模拟电源电流，则通过将DACR.DAOE1、DAOE0和DAE位设置为0来禁用DA转换。

37.6.3 DAC12在软件待机模式下的操作

当MCU进入软件待机模式并启用DA转换时，DA输出保持不变，模拟电源电流与DA转换期间相同。如果在软件待机模式下必须降低模拟电源电流，则通过将DACR.DAOE1、DAOE0和DAE位设置为0来禁用DA转换。

37.6.4 进入深度软件待机模式的限制

当MCU在启用DA转换的情况下进入深度软件待机模式时，DAC12的输出置于高阻抗状态。

37.6.5 输出放大器的初始化程序

对输出放大器使用以下初始化程序。该示例显示了通道0的情况。

使用输出放大器初始化DAC12：

1.将0x0000写入DADR0寄存器。

2.将DAASWCR.DAASW0位设置为1。

3.将DAAMPCR.DAAMP0位设置为1。

4.将DACR.DAE位或DACR.DAOE0位设置为1以启动放大器的操作。

5.等待DA转换时间tDCONV后，将DAASWCR.DAASW0位清零。

6.将要转换的值写入DADR0寄存器。

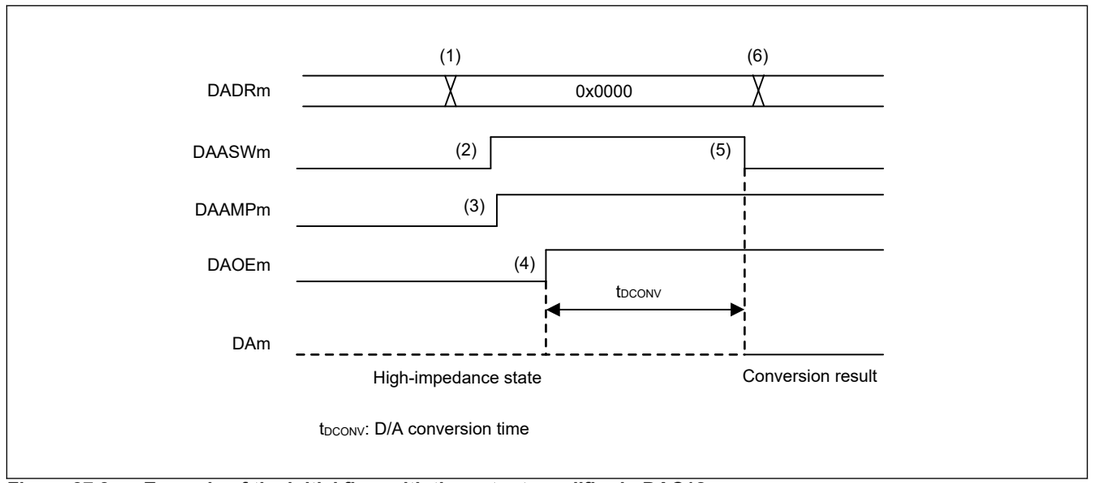


Figure 37.3 Example of the initial flow with the output amplifier in DAC12

While the amplifier is running, clearing the DACR.DAE and DACR.DAOE0 bits to 0 allows the amplifier to stop operation. To use the amplifier again, repeat steps 1 to 6.

37.6.6 Initialization Procedure of the Output to internal modules

Use the following initialization procedures for the output to internal modules.

The example shows the case for channel 0.

1. Set the DAASWCR.DAASW0 bit to 1.
2. Set the DACR.DAE bit or the DACR.DAOE0 bit to 1.
3. Write the value to be converted in the DADR0 register.

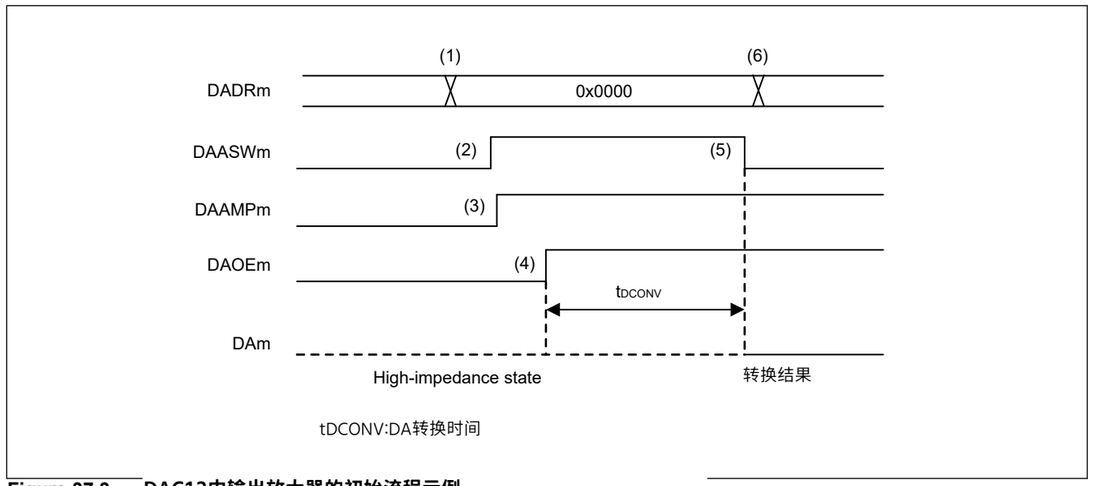


Figure 37.3 DAC12中输出放大器的初始流程示例

在放大器运行时，将DACR.DAE和DACR.DAOE0位清零可让放大器停止运行。
要再次使用放大器，请重复步骤1至6。

37.6.6 输出到内部模块的初始化过程

对内部模块的输出使用以下初始化过程。

该示例显示了通道0的情况。

1.将DAASWCR.DAASW0位设置为1。
2.将DACR.DAE位或DACR.DAOE0位设置为1。
3.将要转换的值写入DADR0寄存器。

38. Temperature Sensor (TSN)

38.1 Overview

The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC for conversion and can be further used by the end application.

Table 38.1 lists the TSN specifications, and Figure 38.1 shows a block diagram.

Table 38.1 TSN specifications

Item	Description
Temperature sensor voltage output	Temperature sensor outputs a voltage to the 12-bit A/D converter
Module-stop function	Module-stop state can be set to reduce power consumption
Temperature sensor calibration data	Reference data measured for each chip at factory shipment is stored in a register
TrustZone Filter	Security attribution can be set

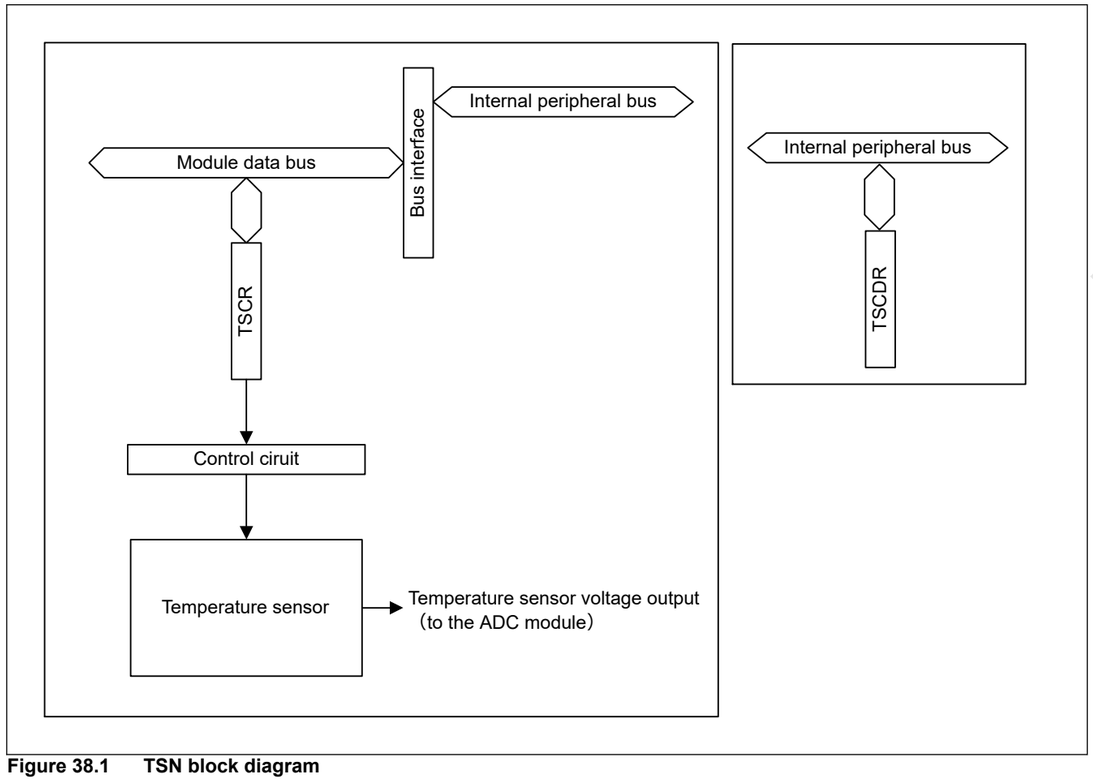


Figure 38.1 TSN block diagram

38. 温度传感器(TSN)

38.1 Overview

片上温度传感器(TSN)确定并监控芯片温度，以确保器件可靠运行。传感器输出与管芯温度成正比的电压，管芯温度与输出电压之间的关系相当线性。输出电压提供给ADC进行转换，并可进一步供最终应用使用。

表38.1列出了TSN规范，图38.1显示了框图。

Table 38.1 TSN specifications

Item	Description
温度传感器电压输出	温度传感器向12位AD转换器输出电压
Module-stop function	可设置模块停止状态以降低功耗
温度传感器校准数据	出厂时为每个芯片测量的参考数据存储在寄存器中
TrustZone Filter	可设置安全属性

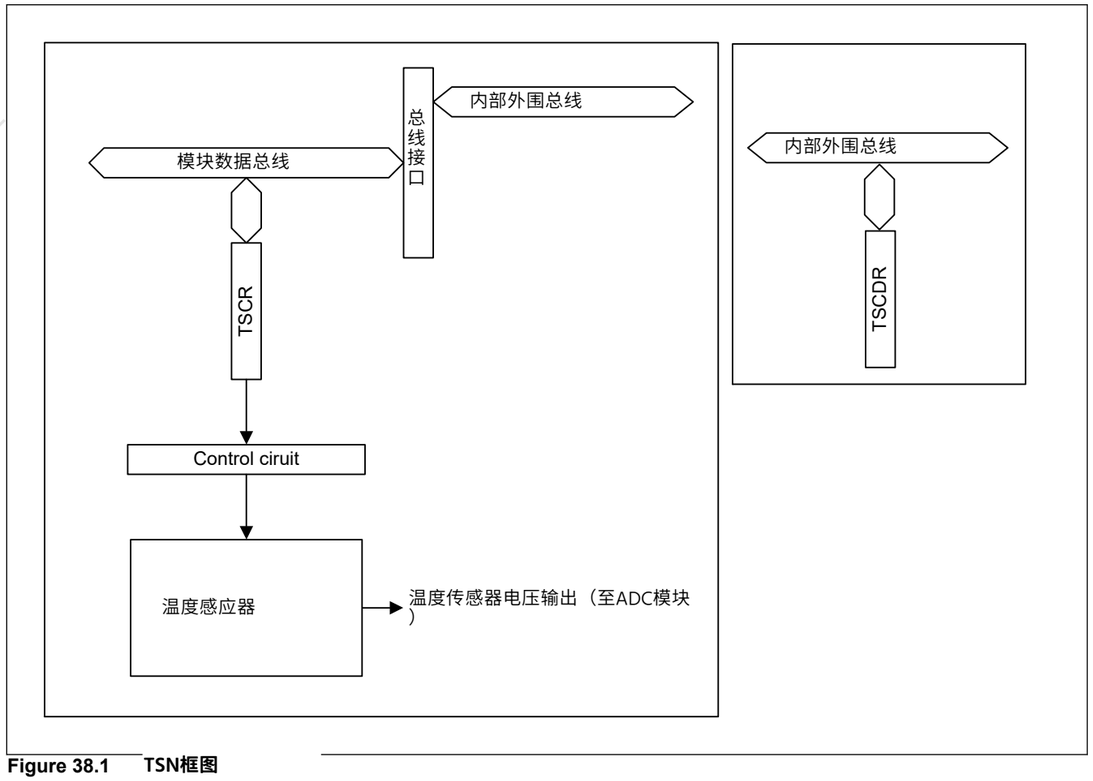


Figure 38.1 TSN框图

38.2 Register Descriptions

38.2.1 TSCR : Temperature Sensor Control Register

Base address: TSN = 0x400F_3000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TSEN	—	—	TSOE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
4	TSOE	Temperature Sensor Output Enable 0: Disable output from the temperature sensor to the ADC 1: Enable output from the temperature sensor to the ADC	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	TSEN	Temperature Sensor Enable 0: Stop the temperature sensor 1: Start the temperature sensor.	R/W

The TSCR is a register which controls the temperature sensor. The timing constraints shown in Figure 38.3 apply to the settings of the TSCR register.

TSOE bit (Temperature Sensor Output Enable)

The TSOE bit enables or disables the temperature sensor output to ADC.

TSEN bit (Temperature Sensor Enable)

The TSEN bit starts or stops the temperature sensor.

38.2.2 TSCDR : Temperature Sensor Calibration Data Register

Base address: TSD = 0x407F_B000

Offset Address: 0x017C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TSCDR[15:0]															
Value after reset:	Chip-specific value															

Bit	Symbol	Function	R/W
15:0	TSCDR[15:0]	Temperature Sensor Calibration Data Chip-specific value	R
31:16	—	These bits are read as 0.	R

The TSCDR register stores temperature sensor calibration data measured for each chip at factory shipment.

Temperature sensor calibration data is the output voltage of the temperature sensor under the conditions Tj = 127°C and AVCC0 = VREFH0 = 3.3 V converted to a digital value by the 12-bit A/D converter.

The TSCDR register is a read-only 32-bit register. Read from this register in 32-bit units.

38.2 注册说明

38.2.1 TSCR：温度传感器控制寄存器

Base address: TSN = 0x400F_3000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TSEN	—	—	TSOE	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	这些位被读取为0。写入值应为0。	R/W
4	TSOE	温度传感器输出使能 0：禁用从温度传感器到ADC的输出1：启用从温度传感器到ADC的输出	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	TSEN	温度传感器启用 0：停止温度传感器1：启动温度传感器。	R/W

TSCR是一个控制温度传感器的寄存器。图38.3所示的时序约束适用于TSCR寄存器的设置。

TSOE位（温度传感器输出使能）

TSOE位启用或禁用温度传感器输出到ADC。

TSEN位（温度传感器使能）

TSEN位启动或停止温度传感器。

38.2.2 TSCDR:温度传感器校准数据寄存器

Base address: TSD = 0x407F_B000

Offset Address: 0x017C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TSCDR[15:0]															
重置后的值：	Chip-specific value															

Bit	Symbol	Function	R/W
15:0	TSCDR[15:0]	温度传感器校准数据 Chip-specific value	R
31:16	—	这些位读为0。	R

TSCDR寄存器存储在出厂时为每个芯片测量的温度传感器校准数据。

温度传感器校准数据是温度传感器在条件Tj=127°C和AVCC0=VREFH0=3.3V通过12位AD转换器转换为数字值。

TSCDR寄存器是一个只读的32位寄存器。以32位为单位从该寄存器中读取。

Temperature sensor calibration data is stored in the lower 12 bits of the TSCDR register.

38.3 Using the Temperature Sensor

The temperature sensor outputs a voltage that varies with the temperature. This voltage is converted to a digital value by the 12-bit A/D converter. To obtain the die temperature, convert this value into the temperature.

38.3.1 Preparation for Using the Temperature Sensor

The ambient temperature (T) is proportional to the temperature sensor voltage output (Vs), so ambient temperature is calculated with the following formula:

T = (Vs - V1) / slope + T1

- T: Ambient temperature of MCU as calculation result (°C)
- Vs: Voltage output by the temperature sensor on temperature measurement (V)
- T1: Temperature experimentally measured at one point (°C)
- V1: Voltage output by the temperature sensor on measurement of T1 (V)
- T2: Temperature experimentally measured at a second point (°C)
- V2: Voltage output by the temperature sensor on measurement of T2 (V)
- Slope: Temperature gradient of the temperature sensor (V / °C), slope = (V2 - V1) / (T2 -T1)

Characteristics vary between sensors, so Renesas recommends measuring two different sample temperatures as follows:

1. Use the 12-bit A/D converter to measure the voltage V1 output by the temperature sensor at temperature T1.
2. Again use the 12-bit A/D converter to measure the voltage V2 output by the temperature sensor at a different temperature T2.
3. Obtain the temperature gradient (slope = (V2 - V1) / (T2 - T1)) from these results.
4. Subsequently, obtain temperatures by substituting the slope into the formula for the temperature characteristic (T = (Vs - V1) / slope + T1).

If you are using the temperature gradient given in section 46, Electrical Characteristics, use the A/D converter to measure the voltage V1 output by the temperature sensor at temperature T1, then calculate the temperature characteristic using the following formula:

T = (Vs - V1) / slope + T1

Note: This method produces less accurate temperatures than measurement at two points.

In this MCU, the TSCDR register stores the temperature value (CAL127) of the temperature sensor measured under the condition Ta = Tj = 127°C and AVCC0 = VREFH0 = 3.3 V. If you use this value as the sample measurement result at the first point, you can omit the preparation before using the temperature sensor.

V1 is calculated from CAL127:

V1 = 3.3 × CAL127 / 4096 [V] (In case of 12 bit accuracy)

Using this value, the measured temperature can be calculated according to the following formula:

T = (Vs - V1) / slope + 127 [°C]

- T: Ambient temperature of MCU as calculation result (°C)
- Vs: Voltage output by the temperature sensor when the temperature is measured (V)
- V1: Voltage output by the temperature sensor when Ta = Tj = 127°C and AVCC0 = VREFH0 = 3.3 V (V)
- Slope: Temperature gradient of the temperature sensor*1 / 1000 (V/°C)

Note 1. See section 46, Electrical Characteristics

38.3.2 Procedures for Using the Temperature Sensor

Figure 38.2 shows the procedure for using the TSN.

温度传感器校准数据存储在TSCDR寄存器的低12位中。

38.3 使用温度传感器

温度传感器输出随温度变化的电压。该电压由12位AD转换器转换为数字值。要获得芯片温度，请将该值转换为温度。

38.3.1 使用温度传感器的准备工作

环境温度(T)与温度传感器电压输出(Vs)成正比，因此使用以下公式计算环境温度：

T = (Vs - V1) / slope + T1

- T：作为计算结果的MCU的环境温度（°C）
- Vs：温度传感器测温时的电压输出（V）
- T1：在某一点实验测量的温度(°C)
- V1：温度传感器在测量T1（V）时输出的电压
- T2：在第二点实验测量的温度(°C)
- V2：温度传感器在测量T2（V）时输出的电压
- 斜率：温度传感器的温度梯度（V°C），斜率=（V2V1）（T2−T1）

传感器的特性各不相同，因此瑞萨电子建议测量两种不同的样品温度，如下所示：

1、使用12位AD转换器测量温度T1时温度传感器输出的电压V1。

2.再次使用12位AD转换器测量温度传感器在不同温度T2下输出的电压V2。

3.从这些结果中获得温度梯度（斜率=(V2V1)(T2T1)）。

4.随后，通过将斜率代入温度特性公式(T=(VsV1)斜率+T1)来获得温度。

如果您使用第46节“电气特性”中给出的温度梯度，请使用AD转换器测量温度传感器在温度T1下输出的电压V1，然后使用以下公式计算温度特性：

T = (Vs - V1) / slope + T1

Note: 这种方法产生的温度不如两点测量准确。

在此MCU中，TSCDR寄存器存储在Ta=Tj=127°C和AVCC0=VREFH0=3.3V条件下测量的温度传感器的温度值(CAL127)。如果您使用此值作为第一次的样本测量结果点，您可以省略使用温度传感器之前的准备工作。

V1由CAL127计算得出：

V1=3.3×CAL1274096[V]（在12位精度的情况下）

使用该值，可根据以下公式计算测得的温度：

T = (Vs - V1) / slope + 127 [°C]

- T：作为计算结果的MCU的环境温度（°C）
- Vs：测温时温度传感器输出的电压（V）
- V1：Ta=Tj=127°C且AVCC0=VREFH0=3.3V(V)时温度传感器输出的电压
- 斜率：温度传感器的温度梯度*11000(V°C)

注1.见第46节，电气特性

38.3.2 使用温度传感器的步骤

图38.2显示了使用TSN的过程。

For details, see section 36, 12-Bit A/D Converter (ADC).

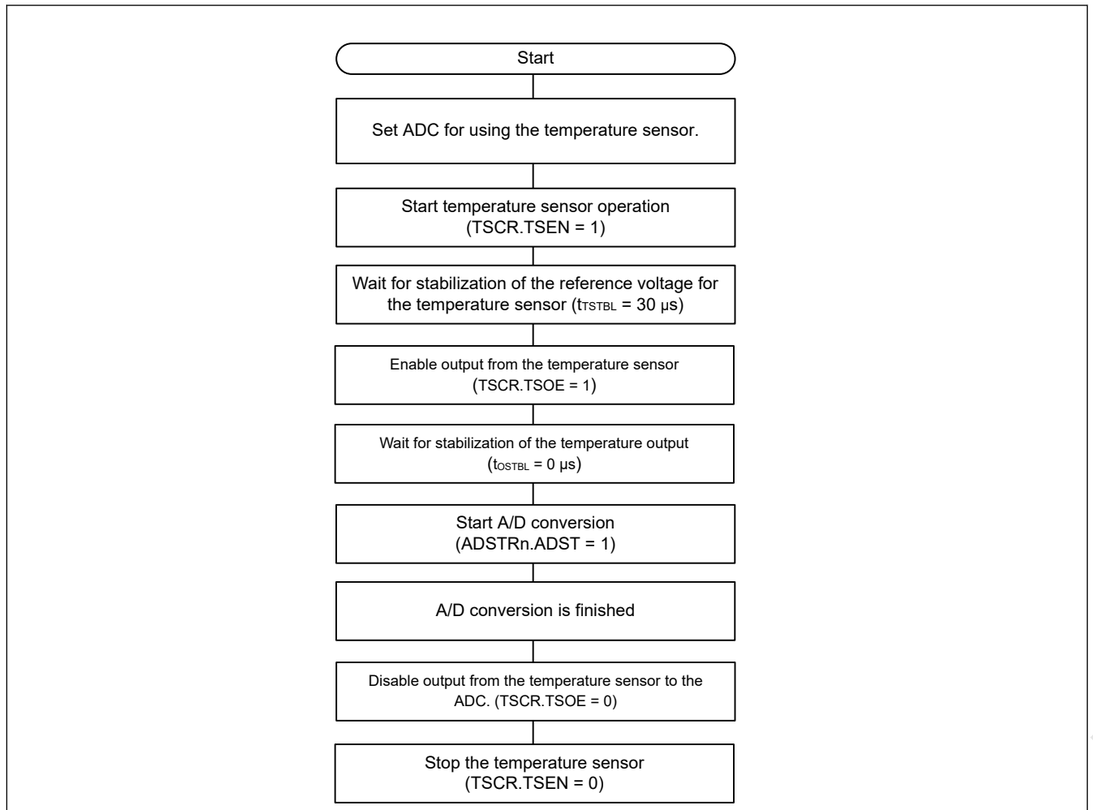


Figure 38.2 Procedure example for using the TSN

Figure 38.3 shows the timing from the start of temperature sensor operation until the completion of A/D conversion when the ADC is in single scan mode (the conversion target is the temperature sensor output only). See section 46, Electrical Characteristics for each time. The sampling time tSPL should be set longer than the value described in section 46, Electrical Characteristics.

有关详细信息，请参阅第36节，12位AD转换器(ADC)。

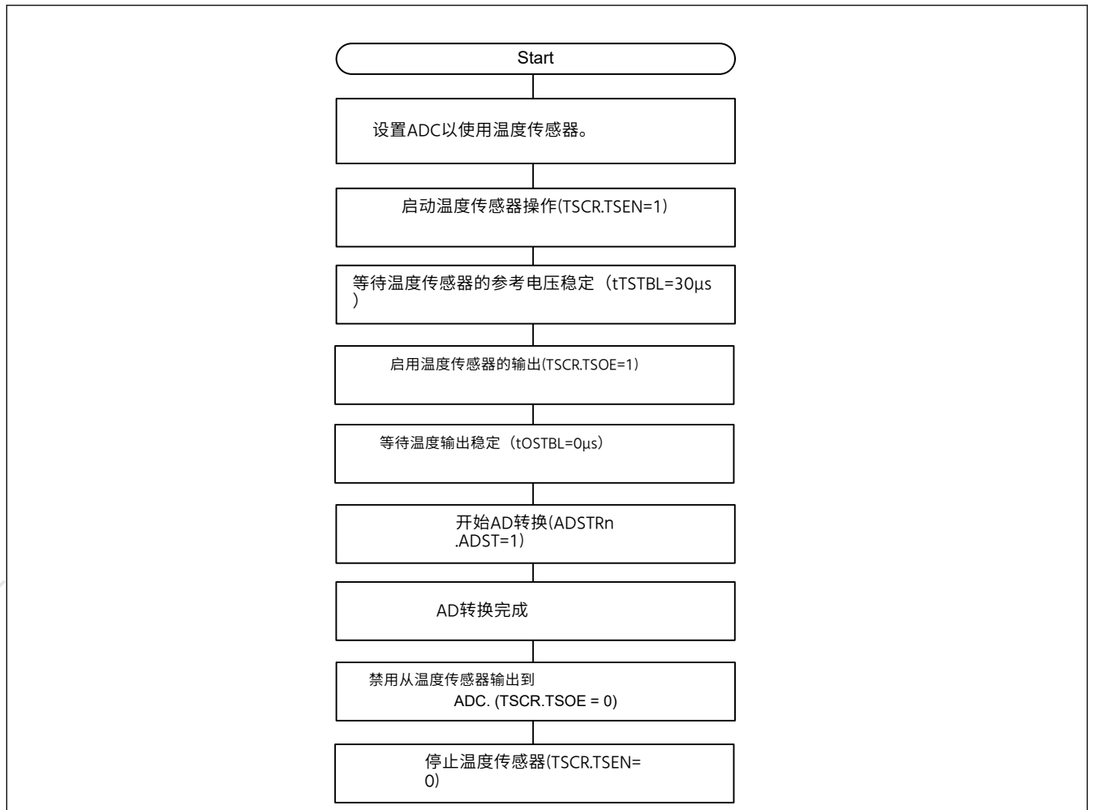


Figure 38.2 使用TSN的过程示例

图38.3显示了当ADC处于单次扫描模式（转换目标仅为温度传感器输出）时，从温度传感器操作开始到AD转换完成的时序。每次参见第46节，电气特性。采样时间tSPL应设置得比第46节"电气"中描述的值长

Characteristics.

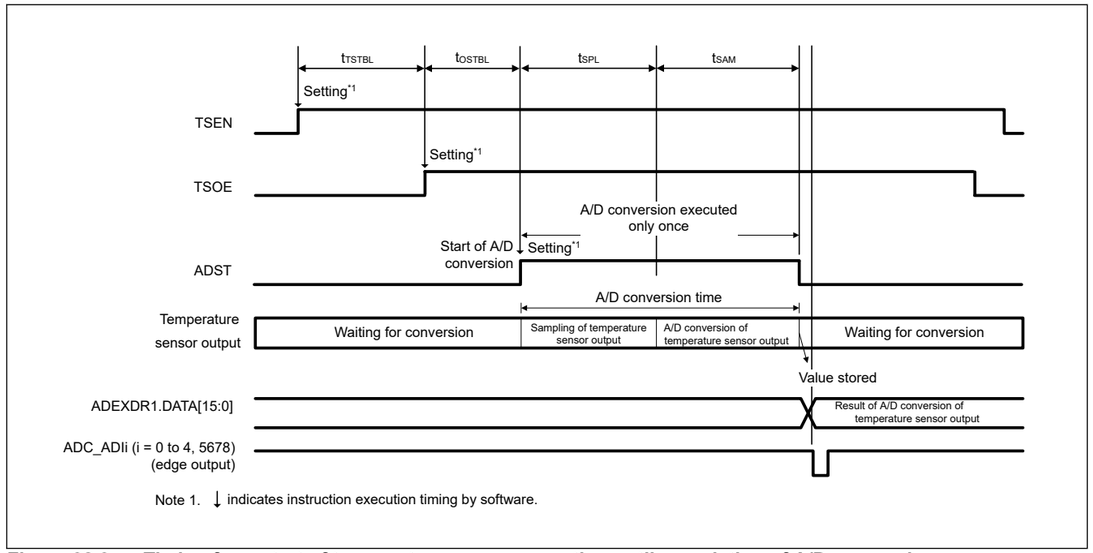


Figure 38.3 Timing from start of temperature sensor operation until completion of A/D conversion

38.4 Usage Notes

38.4.1 Settings for the Module-Stop Function

TSN operation can be disabled or enabled using the associated bit in Module Stop Control Register D (MSTPCRD). The TSN is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

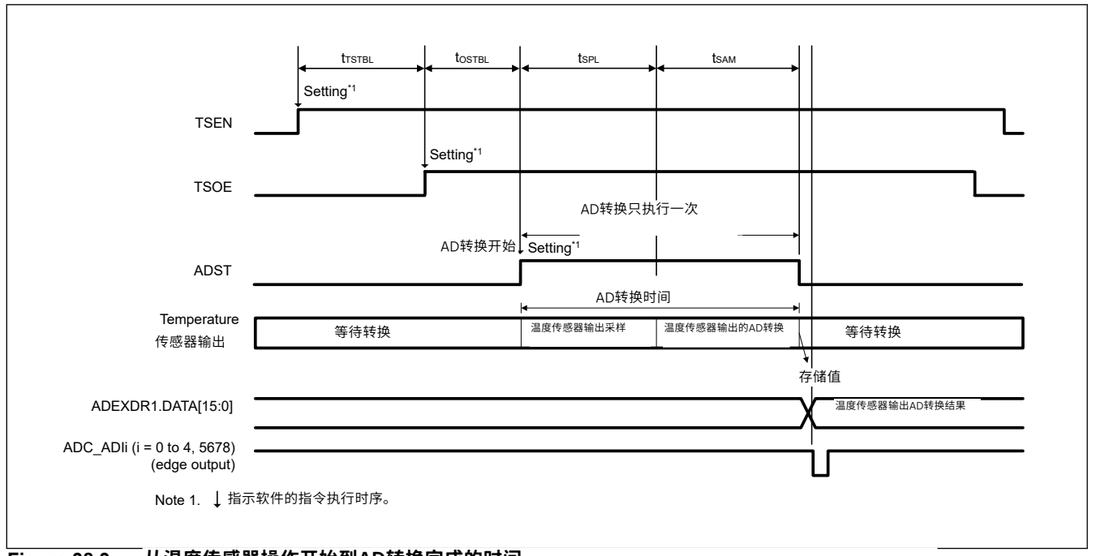


Figure 38.3 从温度传感器操作开始到AD转换完成的时间

38.4 使用说明

38.4.1 模块停止功能的设置

使用模块停止控制寄存器D(MSTPCRD)中的相关位可以禁用或启用TSN操作。TSN在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

39. High-Speed Analog Comparator (ACMPHS)

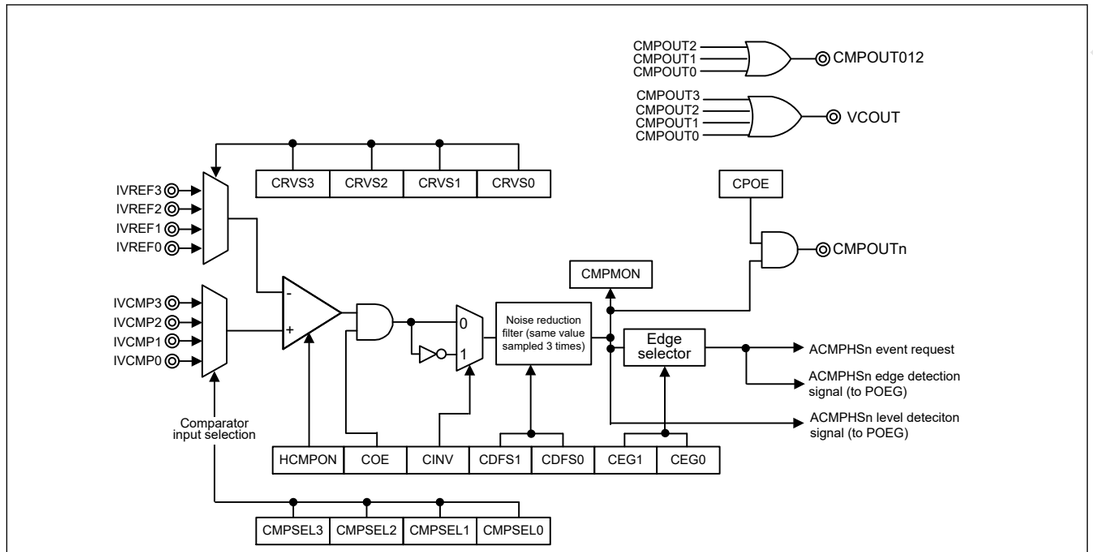
39.1 Overview

The High-Speed Analog Comparator (ACMPHS) can be used to compare a test voltage with a reference voltage and to provide a digital output based on the result of conversion. Both the test voltage and the reference voltage can be provided to the ACMPHS from internal sources (D/A converter output, Programable Gain Amplifire (PGA) output) and an external source. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion.

Table 39.1 lists the ACMPHS specifications, Figure 39.1 shows a block diagram, and Table 39.2 shows the input source configurations.

Table 39.1 ACMPHS specifications

Parameter	Specifications
Number of channels	4 channels: ACMPHSn (n = 0 to 3)
Analog input voltage	• Output from internal PGA • Input from internal A/D converter input pin (one selectable)
Reference voltage	• Output from internal D/A converter • Input from internal A/D converter input pin (one selectable)
ACMPHS output	• Comparison result • Generation of ELC event output • Monitor output from register
Interrupt request signal	• Interrupt request generated on valid edge detection from comparison result • Selectable to rising edge, falling edge, or both edges
Digital filter function	• Selectable to one of three sampling frequencies • Not using the filter function is selectable



Note 1. n = 0 to 3

Figure 39.1 ACMPHS block diagram

39. 高速模拟比较器(ACMPHS)

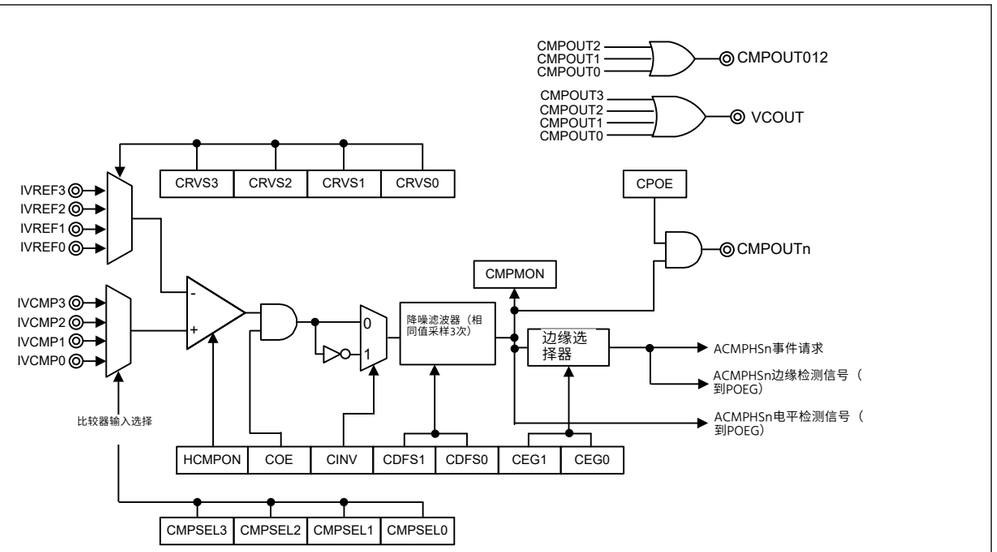
39.1 Overview

高速模拟比较器(ACMPHS)可用于将测试电压与参考电压进行比较，并根据转换结果提供数字输出。测试电压和参考电压都可以从内部源（数模转换器输出、可编程增益放大器(PGA)输出）和外部源提供给ACMPHS。这种灵活性在需要在模拟信号之间执行go-no-go比较而不一定需要AD转换的应用中很有用。

表39.1列出了ACMPHS规范，图39.1显示了框图，表39.2显示了输入源配置。

Table 39.1 ACMPHS specifications

Parameter	Specifications
通道数	4 channels: ACMPHSn (n = 0 to 3)
模拟输入电压	• 内部PGA输出 • 从内部AD转换器输入引脚输入（一个可选）
参考电压	• 来自内部数模转换器的输出 • 从内部AD转换器输入引脚输入（一个可选）
ACMPHS output	• 比较结果 • 生成ELC事件输出 • 监控寄存器的输出
中断请求信号	• 从比较结果中检测到有效边沿时产生中断请求 • 可选择上升沿、下降沿或双沿
数字滤波功能	• 可选择三种采样频率之一 • 可选择不使用过滤功能



注1.n=0至3

Figure 39.1 ACMPHS框图

Table 39.2 Input source configuration of the ACMPHS

Comparator	Reference voltage input source				Analog voltage input source				Output pin
	IVREF3	IVREF2	IVREF1	IVREF0	IVCMP3	IVCMP2	IVCMP1	IVCMP0	
ACMPHS0	DA0	DA3	AN017	AN016	PGA0 output	AN000	—	AN012	VCOUT*1, CMPOUT012*2, CMPOUT0
ACMPHS1	DA1	DA3	AN017	AN016	PGA1 output	AN002	—	AN013	VCOUT*1, CMPOUT012*2, CMPOUT1
ACMPHS2	DA2	DA3	AN017	AN016	PGA2 output	AN004	—	AN014	VCOUT*1, CMPOUT012*2, CMPOUT2
ACMPHS3	DA3	DA2	AN017	AN016	PGA3 output	AN018	—	AN015	VCOUT*1, CMPOUT3

Note 1. ACMPHS0 to ACMPHS3 compare outputs are bundled with the VCOUT pin.
Note 2. ACMPHS0 to ACMPHS2 compare outputs are bundled with the CMPOUT012 pin.

39.2 Register Descriptions

39.2.1 CMPCTL : Comparator Control Register

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 3)
Offset address: 0x000

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HCMPON	CDFS[1:0]		CEG[1:0]		—	COE	CINV
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CINV	Comparator Output Polarity Selection*1 *2 0: Do not invert comparator output 1: Invert comparator output	R/W
1	COE	Comparator Output Enable 0: Disable comparator output (output signal is low level) 1: Enable comparator output	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
4:3	CEG[1:0]	Selection of Valid Edge (Edge Selector) 0 0: Do not detect edge 0 1: Detect rising edge 1 0: Detect falling edge 1 1: Detect both edges	R/W
6:5	CDFS[1:0]	Noise Filter Selection *1 *2 *3 0 0: Do not use noise filter 0 1: Use noise filter sampling frequency of PCLKB/2^3 1 0: Use noise filter sampling frequency of PCLKB/2^4 1 1: Use noise filter sampling frequency of PCLKB/2^5	R/W
7	HCMPON	Comparator Operation Control*4 0: Stop operation (comparator outputs a low-level signal) 1: Enable operation (enables input to the comparator pins)	R/W

Note 1. Disable the ACMPHS output (COE= 0) before changing the CDFS[1:0] and CINV bits.
Note 2. If the CDFS[1:0] and CINV bits are changed, an ACMPHS interrupt request and an ELC event might be generated. Before changing these bits, set the ELSRn register to 0 (the ACMPHS output is not linked). After changing these bits, clear the IR flag in the IELSRn register to 0 to clear the interrupt status.
Note 3. If the CDFS[1:0] bits are changed from 00b (noise filter not used) to a value other than 00b (noise filter used), perform sampling four times and update the filter output, and then use the ACMPHS interrupt request or the ELC event.
Note 4. A stabilization wait time is required to permit ACMPHS operation after enabling it (HCMPON = 1). The operation stabilization wait time for ACMPHS is 300 ns.

Note: Set this register before setting registers in the POEG when using comparator output as a POEG source.

Table 39.2 ACMPHS的输入源配置

Comparator	参考电压输入源				模拟电压输入源				输出引脚
	IVREF3	IVREF2	IVREF1	IVREF0	IVCMP3	IVCMP2	IVCMP1	IVCMP0	
ACMPHS0	DA0	DA3	AN017	AN016	PGA0 output	AN000	—	AN012	VCOUT*1, CMPOUT012*2, CMPOUT0
ACMPHS1	DA1	DA3	AN017	AN016	PGA1 output	AN002	—	AN013	VCOUT*1, CMPOUT012*2, CMPOUT1
ACMPHS2	DA2	DA3	AN017	AN016	PGA2 output	AN004	—	AN014	VCOUT*1, CMPOUT012*2, CMPOUT2
ACMPHS3	DA3	DA2	AN017	AN016	PGA3 output	AN018	—	AN015	VCOUT*1, CMPOUT3

注1.ACMPHS0至ACMPHS3比较输出与VCOUT引脚捆绑在一起。
注2.ACMPHS0到ACMPHS2比较输出与CMPOUT012引脚捆绑在一起。

39.2 注册说明

39.2.1 CMPCTL:比较器控制寄存器

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 3)
Offset address: 0x000

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HCMPON	CDFS[1:0]		CEG[1:0]		—	COE	CINV
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CINV	比较器输出极性选择*1*2 0：不反转比较器输出1：反转比较器输出	R/W
1	COE	比较器输出使能 0：禁止比较器输出（输出信号为低电平）1：使能比较器输出	R/W
2	—	该位读取为0。写入值应为0。	R/W
4:3	CEG[1:0]	有效边的选择（边选择器） 00：不检测边沿01：检测上升沿10：检测下降沿11：检测两个边沿	R/W
6:5	CDFS[1:0]	噪声过滤器选择*1*2*3 00：不使用噪声滤波器01：使用PCLKB的噪声滤波器采样频率23 10：使用PCLKB的噪声滤波器采样频率24 11：使用PCLKB的噪声滤波器采样频率25	R/W
7	HCMPON	比较器操作控制*4 0：停止操作（比较器输出低电平信号）1：使能操作（使能输入到比较器引脚）	R/W

注1.在更改CDFS[1:0]和CINV位之前禁用ACMPHS输出(COE=0)。
注2.如果更改CDFS[1:0]和CINV位，可能会产生ACMPHS中断请求和ELC事件。在更改这些位之前，将ELSRn寄存器设置为0（ACMPHS输出未链接）。更改这些位后，将IELSRn寄存器中的IR标志清零以清除中断状态。

注3.如果CDFS[1:0]位从00b（未使用噪声滤波器）更改为00b以外的值（使用噪声滤波器），执行四次采样并更新滤波器输出，然后使用ACMPHS中断请求或ELC事件。
注4.启用ACMPHS后需要稳定等待时间以允许其运行(HCMPON=1)。ACMPHS的操作稳定等待时间为300ns。

Note: 当使用比较器输出作为POEG源时，在设置POEG中的寄存器之前设置该寄存器。

The CMPCTL register controls the ACMPHS operation, enables or disables the ACMPHS output, selects the noise filter, selects the valid edge of the interrupt signal, and selects the interrupt.

39.2.2 CMPSEL0 : Comparator Input Select Register

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 3)

Offset address: 0x004

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CMPSEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CMPSEL[3:0]	Comparator Input Selection*1 0x0: Do not input 0x1: Select IVCMP0*2 0x2: Setting prohibited*2 0x4: Select IVCMP2*2 0x8: Select IVCMP3*2 Others: Setting prohibited	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Use the following procedure to change the CMPSEL[3:0] bits. Writing a value other than 0x00 while the value of the CMPSEL0 register is not 0x00 is invalid. Writing 1 to two or more bits is also invalid. In both cases, the previous value is retained.
To change the CMPSEL[3:0] bits:
1. Set the CMPCTL.COE bit to 0.
2. Set the CMPSEL0 register to 0x00.
3. Set a new value in the CMPSEL[3:0] bits, with 1 set in only one of the bits.
4. Wait for the input switching stabilization wait time (200 ns).
5. Set the CMPCTL.COE bit to 1.
6. Clear the IR flag in the IELSRn register to clear the interrupt status.

Note 2. For details, see Table 39.2.

39.2.3 CMPSEL1 : Comparator Reference Voltage Select Register

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 3)

Offset address: 0x008

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CRVS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CRVS[3:0]	Reference Voltage Selection*1 0x0: Do not input 0x1: Select IVREF0*2 0x2: Select IVREF1*2 0x4: Select IVREF2*2 0x8: Select IVREF3*2 Others: Setting prohibited	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Use the following procedure to change the CRVS[3:0] bits. Writing a value other than 0x00 while the value of the CMPSEL1 register is not 0x00 is invalid. Writing 1 to two or more bits is also invalid. In both cases, the previous value is retained.
To change the CRVS[3:0] bits:
1. Set the CMPCTL.COE bit to 0.
2. Set the CMPSEL1 register to 0x00.
3. Set a new value to the CRVS[3:0] bits, with 1 set in only one of the bits.
4. Wait for the input switching stabilization wait time (200 ns)

CMPCTL寄存器控制ACMPHS操作，使能或禁用ACMPHS输出，选择噪声滤波器，选择中断信号的有效边沿，选择中断。

39.2.2 CMPSEL0：比较器输入选择寄存器

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 3)

Offset address: 0x004

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CMPSEL[3:0]			
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CMPSEL[3:0]	比较器输入选择*1 0x0：不输入0x1：选择IVCMP0*2 0x2：禁止设置*2 0x4: Select IVCMP2*2 0x8: Select IVCMP3*2 其他：禁止设置	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

注1.使用以下程序更改CMPSEL[3:0]位。CMPSEL0寄存器的值不是0x00时写入0x00以外的值无效。将1写入两位或更多位也是无效的。在这两种情况下，都会保留先前的值。要更改CMPSEL[3:0]位：1.将CMPCTL.COE位设置为0。2.将CMPSEL0寄存器设置为0x00。3.在CMPSEL[3:0]位中设置一个新值，其中一个位设置为1。4.等待输入切换稳定等待时间（200ns）。5.将CMPCTL.COE位设置为1。6.清除IELSRn寄存器中的IR标志以清除中断状态。

注2.详见表39.2。

39.2.3 CMPSEL1：比较器参考电压选择寄存器

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 3)

Offset address: 0x008

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CRVS[3:0]			
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CRVS[3:0]	参考电压选择*1 0x0：不输入0x1：选择IVREF0*2 0x2: Select IVREF1*2 0x4: Select IVREF2*2 0x8: Select IVREF3*2 其他：禁止设置	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

注1.使用以下过程更改CRVS[3:0]位。CMPSEL1寄存器的值不是0x00时写入0x00以外的值无效。将1写入两位或更多位也是无效的。在这两种情况下，都会保留先前的值。要更改CRVS[3:0]位：1.将CMPCTL.COE位设置为0。2.将CMPSEL1寄存器设置为0x00。3.为CRVS[3:0]位设置一个新值，其中一个位设置为1。4.等待输入切换稳定等待时间（200ns）

5. Set the CMPCTL.COE bit to 1.
6. Clear the IR flag in the IELSRn register to clear the interrupt status.

Note 2. For details, see Table 39.2.

39.2.4 CMPMON : Comparator Output Monitor Register

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 3)

Offset address: 0x00C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPMON
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPMON	Comparator Output Monitor*1 0: Comparator output is low 1: Comparator output is high	R
7:1	—	These bits are read as 0. The write value should be 0.	R

Note 1. When ACMPHS operation is enabled (HCMPON = COE = 1) but the noise filter is not in use (CDFS[1:0] = 00b), design the software so that the CMPMON bit is read twice and the values are only used after the two consecutive values match.

39.2.5 CPIOC : Comparator Output Control Register

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 3)

Offset address: 0x010

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CPOE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CPOE	Comparator Output Selection 0: Disable CMPOUTn pin output of the comparator (output signal is low fixed) 1: Enable CMPOUTn pin output of the comparator	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

39.3 Operation

The ACMPHS compares a reference voltage to an analog input voltage. Operation is not guaranteed when the values of registers are changed during ACMPHS operation. Table 39.3 shows the procedures for setting the registers associated with ACMPHS.

Table 39.3 Procedure for setting registers associated with ACMPHSn (n = 0 to 3) (1 of 2)

Step	Register	Bit	Setting
1	Associated MSTPCRD register	MSTPD28 to MSTPD25	0: Input clock supply.
2	Associated pin function control register (PFS)	ASEL	1: Select the function of pins IVREF and IVCMP.
3	Associated D/A convertor		When using the D/A convertor, select in the register.
4	CMPSEL0, CMPSEL1	CMPSEL0 to CMPSEL3, CRVS0 to CRVS3	Select the ACMPHSn input, with 1 set in only one of the bits.
5	CMPCTL	CDFS[1:0], CEG1, CEG0, and CINV	Set up ACMPHSn control.
		HCMPON	1: Enable ACMPHSn operation.

5.将CMPCTL.COE位设置为1。6.清除IELSRn寄存器中的IR标志以清除中断状态。

注2.详见表39.2。

39.2.4 CMPMON:比较器输出监控寄存器

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 3)

Offset address: 0x00C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPMON
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPMON	比较器输出监视器*1 0：比较器输出低1：比较器输出高	R
7:1	—	这些位被读取为0。写入值应为0。	R

注1.当启用ACMPHS操作(HCMPON=COE=1)但未使用噪声滤波器(CDFS[1:0]=00b)时，设计软件时读取CMPMON位两次且值仅在两个连续值匹配后使用。

39.2.5 CPIOC：比较器输出控制寄存器

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 3)

Offset address: 0x010

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CPOE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CPOE	比较器输出选择 0：禁止比较器的CMPOUTn引脚输出（输出信号为低电平固定）1：使能比较器的CMPOUTn引脚输出	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

39.3 Operation

ACMPHS将参考电压与模拟输入电压进行比较。如果在ACMPHS操作期间更改寄存器的值，则无法保证操作。表39.3显示了设置与ACMPHS相关的寄存器的过程。

Table 39.3 设置与ACMPHSn相关的寄存器的过程（n=0到3）（1of2）

Step	Register	Bit	Setting
1	相关的MSTPCRD寄存器	MSTPD28 to MSTPD25	0：输入时钟电源。
2	相关引脚功能控制寄存器(PFS)	ASEL	1：选择引脚IVREF和IVCMP的功能。
3	Associated D/A convertor		使用DA转换器时，在寄存器中选择。
4	CMPSEL0, CMPSEL1	CMPSEL0 to CMPSEL3, CRVS0 to CRVS3	选择ACMPHSn输入，仅其中一位设置为1。
5	CMPCTL	CDFS[1:0], CEG1, CEG0, and CINV	设置ACMPHSn控制。
		HCMPON	1：使能ACMPHSn操作。

Table 39.3 Procedure for setting registers associated with ACMPHSn (n = 0 to 3) (2 of 2)

Step	Register	Bit	Setting
6	Waiting for the ACMPHS stabilization time (minimum 300 ns).		
7	CMPCTL	COE	1: Enable ACMPHSn output.
8	CPIOC	CPOE	Set the CMPOUTn output
	Associated pin function control register (PFS)	PSEL, PMR	Select the ACMPHS port function.
9	IELSRn	IR, IELS[8:0]	When using an interrupt, select the interrupt status flag and the ICU event link.*1
10	ELSRn	ELS[8:0]	When using an ELC, select the event link.*2
11	Operation started		
12	CMPCTL	COE	0: When changing IVREF or IVCMP, to disable ACMPHSn output.
13	CMPSEL1	CRVS0 to CRVS3	Change the CMPSEL1 bits as follows: 1. Set bits CMPSEL1 to 0000 0000b. 2. Set a new value to the CMPSEL1 bits, with 1 set in only one of the bits.
	CMPSEL0	CMPSEL0 to CMPSEL3	Change the CMPSEL0 bits as follows: 1. Set bits CMPSEL0 to 0000 0000b. 2. Set a new value to the CMPSEL0 bits, with 1 set in only one of the bits.
14	Waiting for the ACMPHS switching stabilization time (minimum 200 ns).		
15	CMPCTL	COE	1: Enable ACMPHSn output.
16	Operation restarted		

Note 1. After ACMPHSn is set, an unnecessary interrupt might occur until operation becomes stable, so initialize the interrupt flag.
Note 2. After ACMPHSn is set, an unnecessary interrupt might occur until operation becomes stable, so initialize the event link select.

Figure 39.2 shows an example of ACMPHS operation. The VCOUT output becomes 1 when the analog input voltage is higher than the ACMPHS reference input voltage, and the VCOUT output becomes 0 when the analog input voltage is lower than the reference voltage. When the ACMPHS output changes, an interrupt request and an ELC event are output.

Table 39.3 设置与ACMPHSn相关的寄存器的过程（n=0到3）（2之2）

Step	Register	Bit	Setting
6	等待ACMPHS稳定时间（最少300ns）。		
7	CMPCTL	COE	1：使能ACMPHSn输出。
8	CPIOC	CPOE	设置CMPOUTn输出
	相关引脚功能控制寄存器(PFS)	PSEL, PMR	选择ACMPHS端口功能。
9	IELSRn	IR, IELS[8:0]	使用中断时，选择中断状态标志和ICU事件链接。*1
10	ELSRn	ELS[8:0]	使用ELC时，选择事件链接。*2
11	操作开始		
12	CMPCTL	COE	0：改变IVREF或IVCMP时，禁用ACMPHSn输出。
13	CMPSEL1	CRVS0 to CRVS3	如下更改CMPSEL1位：1.将CMPSEL1位设置为000000 00b。2.为CMPSEL1位设置一个新值，其中一个位设置为1。
	CMPSEL0	CMPSEL0 to CMPSEL3	如下更改CMPSEL0位：1.将CMPSEL0位设置为000000 00b。2.为CMPSEL0位设置一个新值，其中一个位设置为1。
14	等待ACMPHS开关稳定时间（最少200ns）。		
15	CMPCTL	COE	1：使能ACMPHSn输出。
16	操作重新开始		

注1.ACMPHSn置位后，在操作稳定之前可能会发生不必要的中断，因此请初始化中断标志。
注2.设置ACMPHSn后，在操作稳定之前可能会发生不必要的中断，因此请初始化事件链接选择。

图39.2显示了ACMPHS操作的示例。当模拟输入电压高于ACMPHS参考输入电压时，VCOUT输出变为1，当模拟输入电压低于参考电压时，VCOUT输出变为0。当ACMPHS输出改变时，会输出一个中断请求和一个ELC事件。

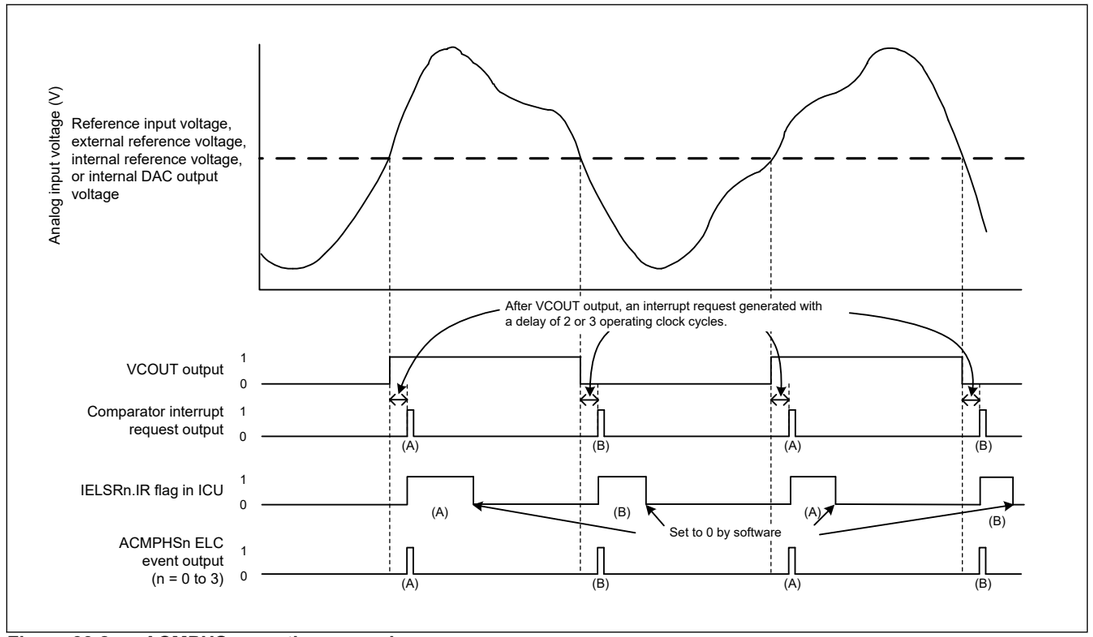


Figure 39.2 ACMPHS operation example

Figure 39.2 applies when CPOE = 1 (pin output enabled), CDFS[1:0] = 00b (filter not used), and CEG1 = CEG0 = 1 (both-edge detection selected). When CINV = 0, CEG0 = 1, and CEG1 = 0 (rising-edge detection selected for non-inversion output signal from the ACMPHS), the IELSR.IR flag changes as shown by (A) only. When CINV = 0, CEG0 = 0, and CEG1 = 1 (falling-edge detection selected for non-inversion output signal from the ACMPHS), the IR flag changes as shown by (B) only.

39.4 Noise Filter

The ACMPHS contains a noise filter. The sampling clock can be selected in the CMPCTL.CDFS[1:0] bits. The comparator output signal is sampled every sampling clock, and if the same value is sampled three times, the noise filter output at the next sampling clock cycle is used as the ACMPHS output.

Figure 39.3 shows the configuration of the noise filter and edge detector, and Figure 39.4 shows an example of noise filter and interrupt operation.

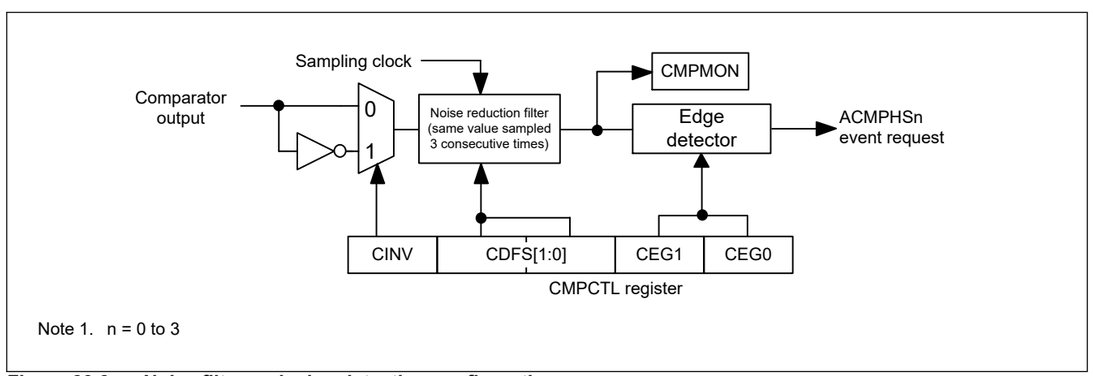


Figure 39.3 Noise filter and edge detection configuration

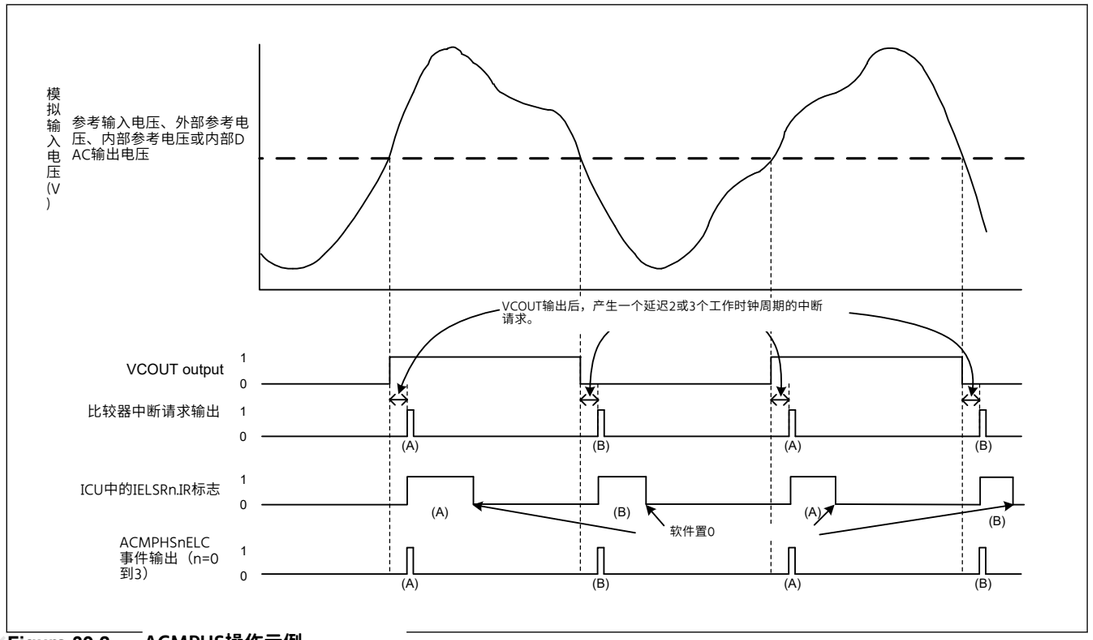


Figure 39.2 ACMPHS操作示例

图39.2适用于CPOE=1（使能引脚输出）、CDFS[1:0]=00b（未使用滤波器）和CEG1=CEG0=1（选择双沿检测）时。当CINV=0、CEG0=1和CEG1=0（为来自ACMPHS的非反相输出信号选择上升沿检测）时，IELSR.IR标志仅如(A)所示变化。当CINV=0、CEG0=0和CEG1=1（为来自ACMPHS的非反相输出信号选择下降沿检测）时，IR标志仅如(B)所示变化。

39.4 噪声过滤器

ACMPHS包含一个噪声滤波器。可以在CMPCTL.CDFS[1:0]位中选择采样时钟。每个采样时钟对比较器输出信号进行采样，如果采样3次相同的值，则将下一个采样时钟周期的噪声滤波器输出作为ACMPHS输出。

图39.3显示了噪声滤波器和边缘检测器的配置，图39.4显示了噪声滤波器和中断操作的示例。

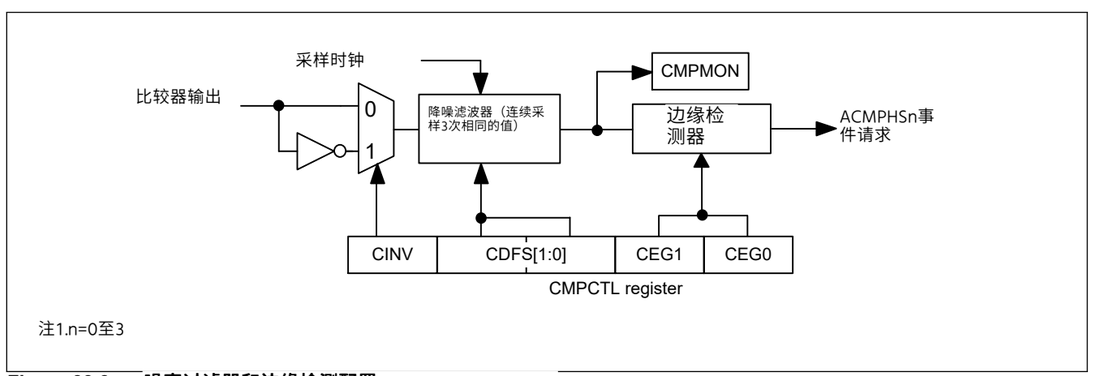


Figure 39.3 噪声过滤器和边缘检测配置

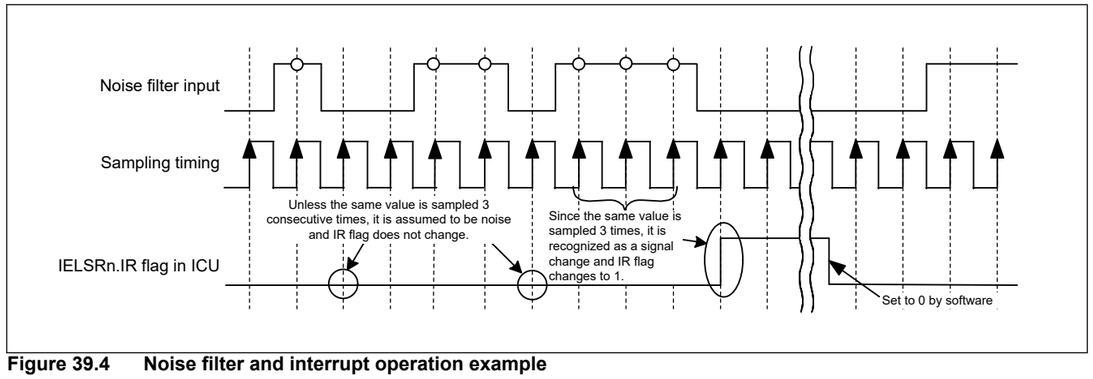


Figure 39.4 Noise filter and interrupt operation example

The operation example in Figure 39.4 applies when the CMPCTL.CDFS[1:0] bits are 01b, 10b, or 11b (noise filter used).

39.5 ACMPHS Interrupts

The ACMPHS generates three interrupt requests from sources ACMPHSn (n = 0 to 3). To use an ACMPHS interrupt, select it in the IELSR register in the Interrupt Controller Unit (ICU).

When using the ACMPHS interrupt through the edge selector, set at least one of the CMPCTL.CEG0 and CMPCTL.CEG1 bits to 1 (to a value other than 00b for no edge selection).

For details on the register settings related to ACMPHS interrupt requests, see section 39.2.1. CMPCTL : Comparator Control Register.

39.6 ACMPHS Output to the Event Link Controller (ELC)

The ELC uses the ACMPHS interrupt request signal as an ELC event signal, enabling link operation for the preset module. To use the ACMPHS ELC event, select them in the ELSR register in the ELC. When using the ELC event request, set at least one of the CMPCTL.CEG0 and CMPCTL.CEG1 bits to 1 (to a value other than 00b for no edge selection).

39.7 ACMPHS Pin Output

The comparison result from the ACMPHS can be output to external pins. Use the CMPCTL.CINV and CPIOC.CPOE bits to set the output polarity (non-inverted or inverted output) and enable or disable output. To output the ACMPHS comparison result to the CMPOUTn (n = 0 to 3), VCOUT and CMPOUT012 output pins, set the associated port mn pin function control register (PmnPFS) in the I/O register. The CMPOUT0 to CMPOUT3 compare outputs are bundled with the VCOUT pin. The CMPOUT0 to CMPOUT2 compare outputs are bundled with the CMPOUT012 pin too.

39.8 Usage Notes

39.8.1 Settings for the Module-Stop Function

ACMPHS operation can be disabled or enabled using the Module Stop Control Register. The ACMPHS is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

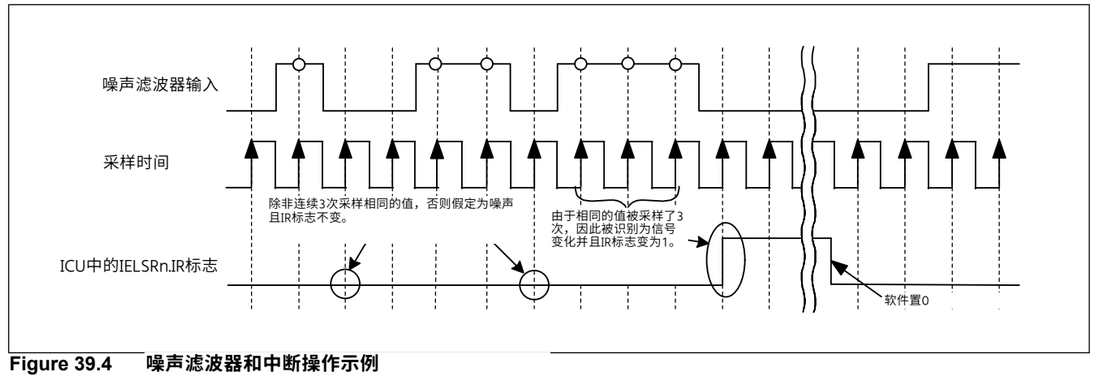


Figure 39.4 噪声滤波器和中断操作示例

图39.4中的操作示例适用于CMPCTL.CDFS[1:0]位为01b、10b或11b（使用噪声滤波器）时。

39.5 ACMPHS Interrupts

ACMPHS从源ACMPHSn（n=0到3）产生三个中断请求。要使用ACMPHS中断，请在中断控制器单元(ICU)的IELSR寄存器中选择它。

通过边沿选择器使用ACMPHS中断时，将CMPCTL.CEG0和CMPCTL.CEG1位中的至少一个设置为1（设置为00b以外的值表示不选择边沿）。

有关与ACMPHS中断请求相关的寄存器设置的详细信息，请参见第39.2.1节。CMPCTL:比较器控制寄存器。

39.6 ACMPHS输出到事件链接控制器(ELC)

ELC使用ACMPHS中断请求信号作为ELC事件信号，为预设模块启用链接操作。
要使用ACMPHSELC事件，请在ELC的ELSR寄存器中选择它们。使用ELC事件请求时，将CMPCTL.CEG0和CMPCTL.CEG1位中的至少一个设置为1（设置为00b以外的值以表示无边沿选择）。

39.7 ACMPHS引脚输出

ACMPHS的比较结果可以输出到外部引脚。使用CMPCTL.CINV和CPIOC.CPOE位设置输出极性（非反相或反相输出）并启用或禁用输出。要将ACMPHS比较结果输出到CMPOUTn（n=0至3）、VCOUT和CMPOUT012输出引脚，请在IO寄存器中设置相关的端口mn引脚功能控制寄存器（PmnPFS）。CMPOUT0到CMPOUT3比较输出与VCOUT引脚捆绑在一起。CMPOUT0到CMPOUT2比较输出也与CMPOUT012引脚捆绑在一起。

39.8 使用说明

39.8.1 模块停止功能的设置

可以使用模块停止控制寄存器禁用或启用ACMPHS操作。ACMPHS在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

40. Data Operation Circuit (DOC)

This is the DOC_B version of the DOC peripheral module.

DOC_B is referred to as DOC in this chapter.

40.1 Overview

The data operation circuit (DOC) is used to compare, add, and subtract 16 or 32-bit data. An interrupt can be generated when the following conditions apply.

- When the 16 or 32-bit compared values match the detection condition
- When the result of 16 or 32-bit data addition overflows
- When the result of 16 or 32-bit data subtraction underflows

Table 40.1 lists the data operation circuit specifications and Figure 40.1 shows a block diagram of the data operation circuit.

Table 40.1 DOC specifications

Item	Description
Data operation function	16 or 32-bit data comparison, comparison to detect data above or below thresholds, and window comparison 16 or 32-bit data addition, and subtraction
Module-stop function	The module-stop state can be set to reduce power consumption.
Interrupts	• The compared values match the detection condition • The result of data addition is greater than 0xFFFF (DOCR.DOBW = 0) or 0xFFFF_FFFF (DOCR.DOBW = 1) • The result of data subtraction is less than 0x0000 (DOCR.DOBW = 0) or 0x0000_0000h (DOCR.DOBW = 1)
Event link function (output)	• The result of data comparison is consistent with detection condition • The result of data addition is greater than 0xFFFF (DOCR.DOBW = 0) or 0xFFFF_FFFF (DOCR.DOBW = 1) • The result of data subtraction is less than 0x0000 (DOCR.DOBW = 0) or 0x0000_0000 (DOCR.DOBW = 1)
TrustZone Filter	Security attribution can be set

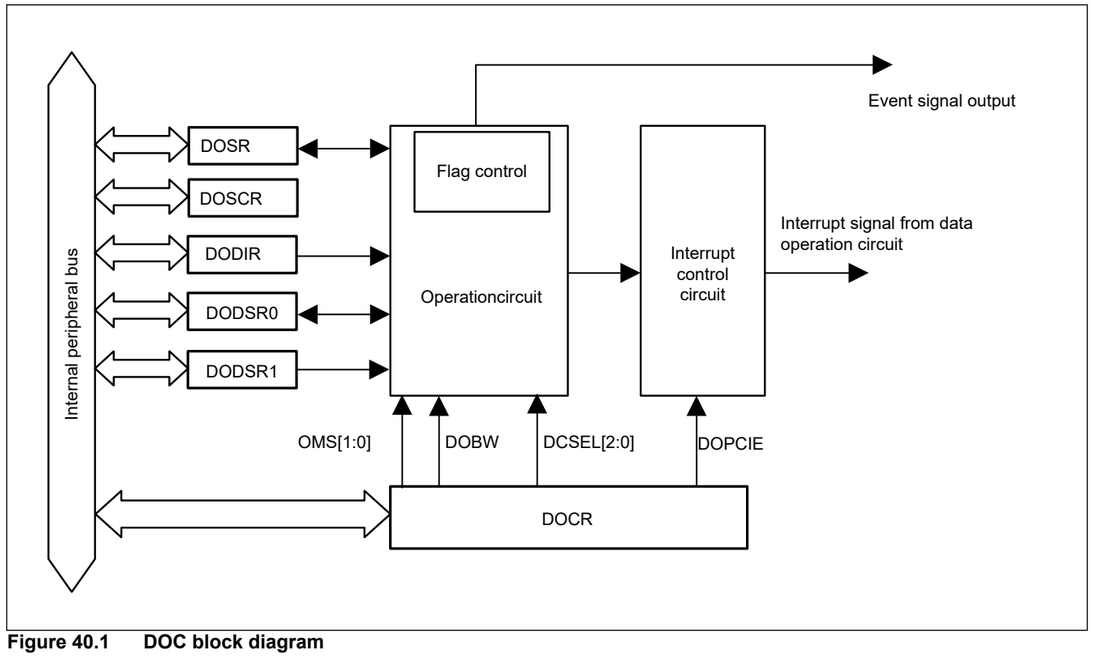


Figure 40.1 DOC block diagram

40. 数据运算电路(DOC)

这是DOC外围模块的DOC_B版本。

DOC_B在本章中称为DOC。

40.1 Overview

数据运算电路(DOC)用于对16位或32位数据进行比较、加法和减法。当以下条件适用时，可以产生中断。

●16位或32位比较值符合检测条件时
●16位或32位数据相加结果溢出时
●16位或32位数据减法的结果下溢时

表40.1列出了数据操作电路的规格，图40.1显示了数据操作电路的框图。

Table 40.1 文档规范

Item	Description
数据运算功能	16或32位数据比较，检测高于或低于阈值的数据的比较，以及窗口比较16或32位数据的加法和减法
Module-stop function	可设置模块停止状态以降低功耗。
Interrupts	• 比较值符合检测条件 • 数据相加结果大于0xFFFF(DOCR.DOBW=0)或0xFFFF_FFFF(DOCR.DOBW=1) • 数据减法的结果小于0x0000(DOCR.DOBW=0)或0x0000_0000h(DOCR.DOBW=1)
事件链接功能（输出）	• 数据比对结果与检测条件一致 • 数据相加结果大于0xFFFF(DOCR.DOBW=0)或0xFFFF_FFFF(DOCR.DOBW=1) • 数据减法的结果小于0x0000(DOCR.DOBW=0)或0x0000_0000(DOCR.DOBW=1)
TrustZone Filter	可设置安全属性

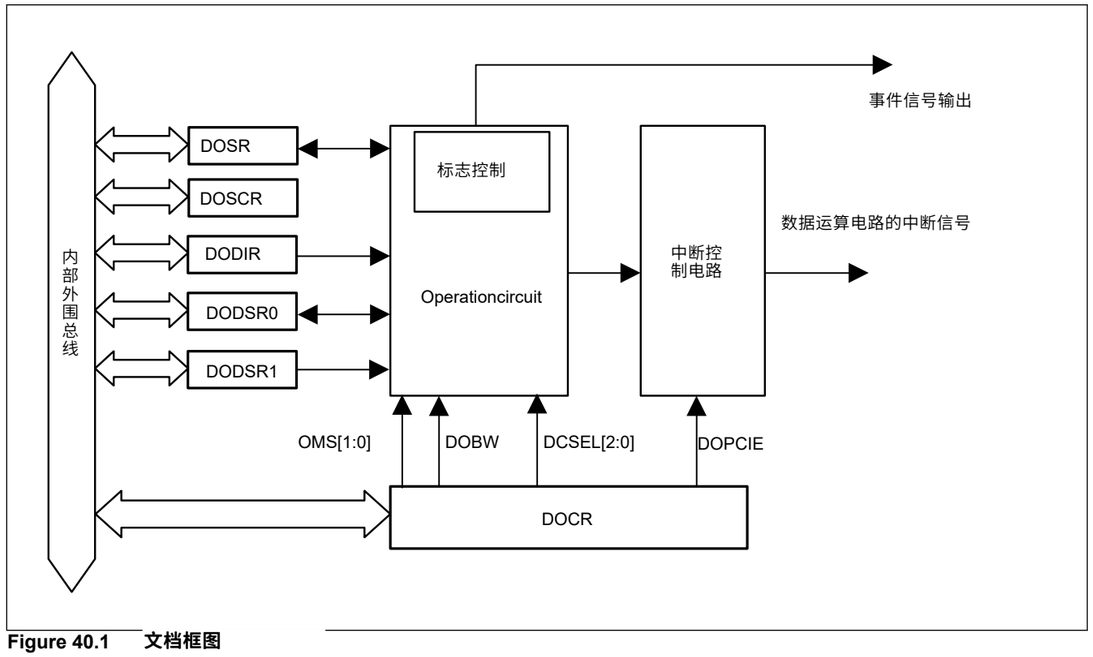


Figure 40.1 文档框图

40.2 DOC Register Descriptions

40.2.1 DOCR : DOC Control Register

Base address: DOC_B = 0x4010_9000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DOPCIE	DCSEL[2:0]			DOBW	—	OMS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	OMS[1:0]	Operating Mode Select 0 0: Data comparison mode 0 1: Data addition mode 1 0: Data subtraction mode 1 1: Setting prohibited	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	DOBW	Data Operation Bit Width Select 0: 16-bit 1: 32-bit	R/W
6:4	DCSEL[2:0]*1	Detection Condition Select 0 0 0: Mismatch (DODSR0 ≠ DODIR) 0 0 1: Match (DODSR0 = DODIR) 0 1 0: Lower (DODSR0 > DODIR) 0 1 1: Upper (DODSR0 < DODIR) 1 0 0: Inside window (DODSR0 < DODIR < DODSR1) 1 0 1: Outside window (DODIR < DODSR0, DODSR1 < DODIR) Others: Setting prohibited	R/W
7	DOPCIE	Data Operation Circuit Interrupt Enable 0: Disables interrupts from the data operation circuit. 1: Enables interrupts from the data operation circuit.	R/W

Note 1. Valid only when data comparison mode is selected.

The DOCR is a register which can set the operation mode of data operation circuit and interrupt enable/disable.

OMS[1:0] bits (Operating Mode Select)

These bits select the operating mode of the data operation circuit.

DOBW bit (Data Operation Bit Width Select)

This bit selects the bit width of data operation.

DCSEL[2:0] bits (Detection Condition Select)

These bits are valid only when data comparison mode is selected.

These bits select the condition for detection in data comparison mode.

DOPCIE bit (Data Operation Circuit Interrupt Enable)

Setting this bit to 1 enables interrupts from the data operation circuit.

40.2 DOC寄存器说明

40.2.1 DOCR:DOC控制寄存器

Base address: DOC_B = 0x4010_9000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DOPCIE	DCSEL[2:0]			DOBW	—	OMS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	OMS[1:0]	操作模式选择 00：数据比较模式01：数据加法模式10：数据减法模式11：禁止设置	R/W
2	—	该位读取为0。写入值应为0。	R/W
3	DOBW	数据操作位宽选择 0: 16-bit 1: 32-bit	R/W
6:4	DCSEL[2:0]*1	检测条件选择 000：不匹配（DODSR0≠DODIR）001：匹配（DODSR0=DODIR）010：下限（DODSR0>DODIR）011：上限（DODSR0<DODIR）100：窗口内（DODSR0<DODIR）<DODSR1)101:窗外(DODIR<DODSR0 DODSR1<DODIR) 其他：禁止设置	R/W
7	DOPCIE	数据操作电路中断使能 0：禁止数据操作电路的中断。1：使能数据操作电路的中断。	R/W

注1.仅在选择数据比较模式时有效。

DOCR是一个寄存器，可以设置数据操作电路的操作模式和中断使能禁止。

OMS[1:0]位（操作模式选择）

这些位选择数据操作电路的操作模式。

DOBW位（数据操作位宽选择）

该位选择数据操作的位宽。

DCSEL[2:0]位（检测条件选择）

这些位仅在选择数据比较模式时有效。

这些位选择数据比较模式下的检测条件。

DOPCIE位（数据操作电路中断允许）

将此位设置为1可启用来自数据操作电路的中断。

40.2.2 DOSR : DOC Flag Status Register

Base address: DOC_B = 0x4010_9000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DOPCF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DOPCF	Data Operation Circuit Flag Indicates the result of an operation.	R
7:1	—	These bits are read as 0. The write value should be 0.	R/W

The DOSR register indicates the status of the data operation.

DOPCF flag (Data Operation Circuit Flag)

[Setting conditions]

- DOCR.OMS[1:0] bits = 00b (Data comparison mode): The compared value matches the detection condition selected by DOCR.DCSEL[2:0] bits
- DOCR.OMS[1:0] bits = 01b (Data addition mode): The result of data addition is greater than FFFFh (DOCR.DOBW = 0) or FFFF_FFFFh (DOCR.DOBW = 1)
- DOCR.OMS[1:0] bits = 10b (Data subtraction mode): The result of data subtraction is less than 0000h (DOCR.DOBW = 0) or 0000_0000h (DOCR.DOBW = 1)

[Clearing condition]

- Writing 1 to the DOSCR.DOPCFCL bit

40.2.3 DOSCR : DOC Flag Status Clear Register

Base address: DOC_B = 0x4010_9000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DOPCFCL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DOPCFCL	DOPCF Clear 0: Maintains the DOPCF flag state. 1: Clears the DOPCF flag.	W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

The DOSCR is a register which can clear the status of data operation. This register is read as 0x00.

DOPCFCL bit (DOPCF Clear)

Setting this bit to 1 clears the DOPCF flag.

40.2.2 DOSR:DOC标志状态寄存器

Base address: DOC_B = 0x4010_9000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DOPCF
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DOPCF	数据运算电路标志 表示操作的结果。	R
7:1	—	这些位被读取为0。写入值应为0。	R/W

DOSR寄存器指示数据操作的状态。

DOPCF标志（数据操作电路标志）

[Setting conditions]

●DOCR.OMS[1:0]bits=00b（数据比较模式）：比较值符合DOCR.DCSEL[2:0]bits选择的检测条件

●DOCR.OMS[1:0]bits=01b（数据相加模式）：数据相加结果大于FFFFh（DOCR.DOBW=0）或FFFF_FFFFh（DOCR.DOBW=1）

●DOCR.OMS[1:0]bits=10b（数据减法模式）：数据减法的结果小于0000h（DOCR.DOBW=0）或0000_0000h（DOCR.DOBW=1）

[Clearing condition]

●向DOSCR.DOPCFCL位写入1

40.2.3 DOSCR:DOC标志状态清除寄存器

Base address: DOC_B = 0x4010_9000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DOPCFCL
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DOPCFCL	DOPCF Clear 0：保持DOPCF标志状态。1：清除DOPCF标志。	W
7:1	—	这些位被读取为0。写入值应为0。	R/W

DOSCR是一个可以清除数据操作状态的寄存器。该寄存器读为0x00。

DOPCFCL bit (DOPCF Clear)

将该位设置为1清除DOPCF标志。

40.2.4 DODIR : DOC Data Input Register

Base address: DOC_B = 0x4010_9000

Offset address: 0x0C

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	It stores data used in the operations. Access the DODIR with the bit width of data operation selected by the DOCR.DOBW bit.	R/W

40.2.5 DODSR0 : DOC Data Setting Register 0

Base address: DOC_B = 0x4010_9000

Offset address: 0x10

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Access the DODSR0 with the bit width of data operation selected by the DOCR.DOBW bit. This register stores data for use as a reference in data comparison mode. When selecting window comparison (DOCR.DCSEL[2:0] = 100b, 101b), set a value less than DODSR1 (DODSR1 > DODSR0). This register also stores the results of operations in data addition and data subtraction modes.	R/W

40.2.6 DODSR1 : DOC Data Setting Register 1

Base address: DOC_B = 0x4010_9000

Offset address: 0x14

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Access the DODSR1 with the bit width of data operation selected by the DOCR.DOBW bit. This register stores data for use as a reference in data comparison mode. When selecting window comparison (DOCR.DCSEL[2:0] = 100b, 101b), set a value greater than DODSR0 (DODSR1 > DODSR0). This register is only used for window comparisons.	R/W

40.3 Operation

40.3.1 Data Comparison Mode

Figure 40.2 to Figure 40.7 shows an example of the steps involved in data comparison mode operation by the data operation circuit.

The following is an example of operation when the bit width of data operation is 32-bit.

40.2.4 DODIR:DOC数据输入寄存器

Base address: DOC_B = 0x4010_9000

Offset address: 0x0C

Bit position:	31																													0
Bit field:																														
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	它存储操作中使用的数据。 使用DOCR.DOBW位选择的数据操作的位宽访问DODIR。	R/W

40.2.5 DODSR0：DOC数据设置寄存器0

Base address: DOC_B = 0x4010_9000

Offset address: 0x10

Bit position:	31																													0
Bit field:																														
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	使用DOCR.DOBW位选择的数据操作的位宽访问DODSR0。该寄存器存储数据以在数据比较模式下用作参考。选择窗口比较时（DOCR.DCSEL[2:0]=100b 101b），设置一个小于DODSR1的值（DODSR1>DODSR0）。该寄存器还存储数据加法和数据减法模式下的运算结果。	R/W

40.2.6 DODSR1：DOC数据设置寄存器1

Base address: DOC_B = 0x4010_9000

Offset address: 0x14

Bit position:	31																													0
Bit field:																														
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	使用DOCR.DOBW位选择的数据操作的位宽访问DODSR1。该寄存器存储数据以在数据比较模式下用作参考。选择窗口比较时（DOCR.DCSEL[2:0]=100b 101b），设置一个大于DODSR0的值（DODSR1>DODSR0）。该寄存器仅用于窗口比较。	R/W

40.3 Operation

40.3.1 数据比较模式

图40.2至图40.7显示了数据操作电路在数据比较模式操作中涉及的步骤示例。

以下是数据操作的位宽为32位时的操作示例。

1. Writing 00b to the DOCR.OMS[1:0] bits selects data comparison mode, and setting the DOCR.DCSEL[2:0] to selects detection condition.
2. The 32-bit reference data is set in DODSR0 and DODSR1.*1
3. 32-bit data for comparison is written to DODIR.
4. If a value written to DODIR match the detection condition set by DOCR.DCSEL[2:0], the DOCR.DOPCF flag is set to 1 and an ELC event is generated. When the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also generated.

Note: The comparison operation is executed only by writing to the DODIR

Note 1. The DODSR1 register setting is required only when window comparison is selected. Set a value greater than DODSR0 (DODSR1 > DODSR0).

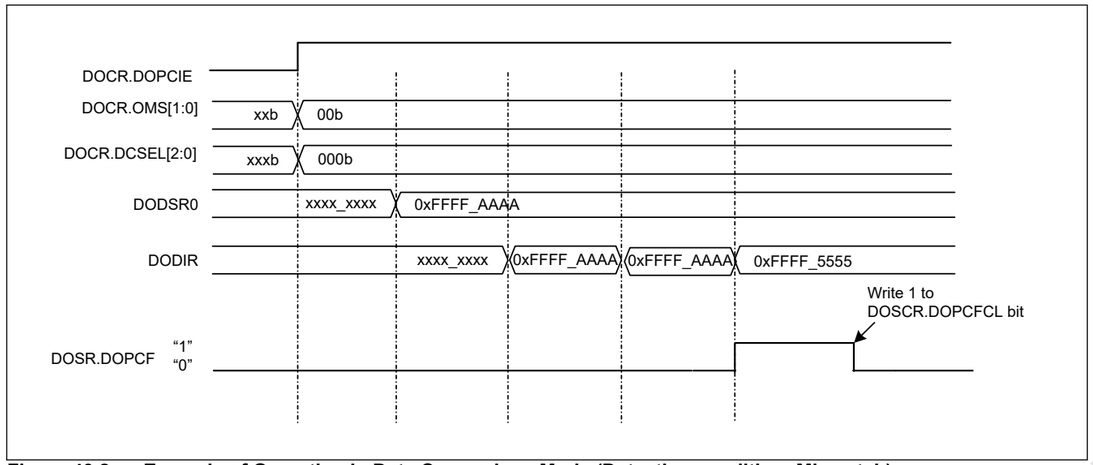


Figure 40.2 Example of Operation in Data Comparison Mode (Detection condition: Mismatch)

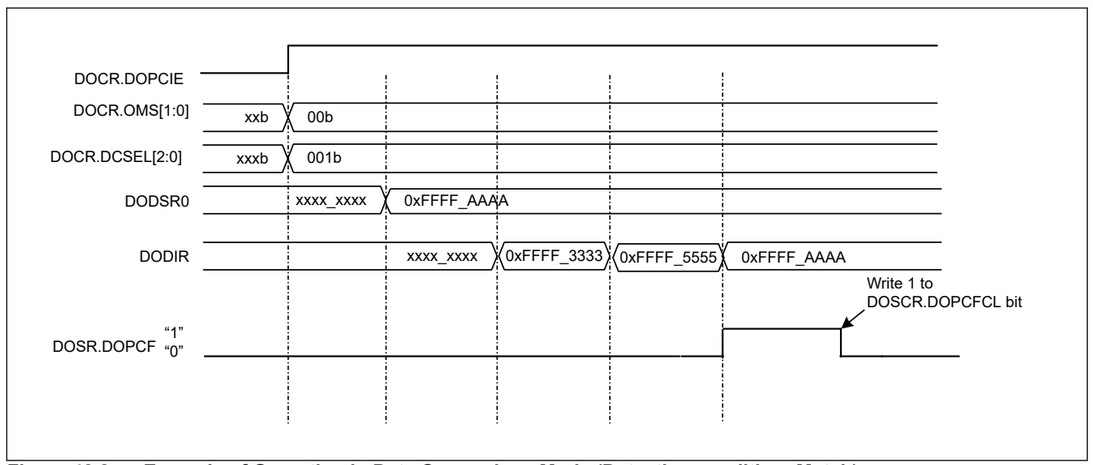


Figure 40.3 Example of Operation in Data Comparison Mode (Detection condition: Match)

1.向DOCR.OMS[1:0]位写入00b选择数据比较模式，并设置DOCR.DCSEL[2:0]选择检测条件。

2.32位参考数据设置在DODSR0和DODSR1中。*1

3.用于比较的32位数据写入DODIR。

4.如果写入DODIR的值与DOCR.DCSEL[2:0]设置的检测条件匹配，则DOCR.DOPCF标志设置为1并生成ELC事件。当DOCR.DOPCIE位为1时，也会产生数据操作电路中断。

Note: 仅通过写入DODIR来执行比较操作

注1.DODSR1寄存器设置仅在选择窗口比较时需要。设置一个大于
DODSR0 (DODSR1 > DODSR0).

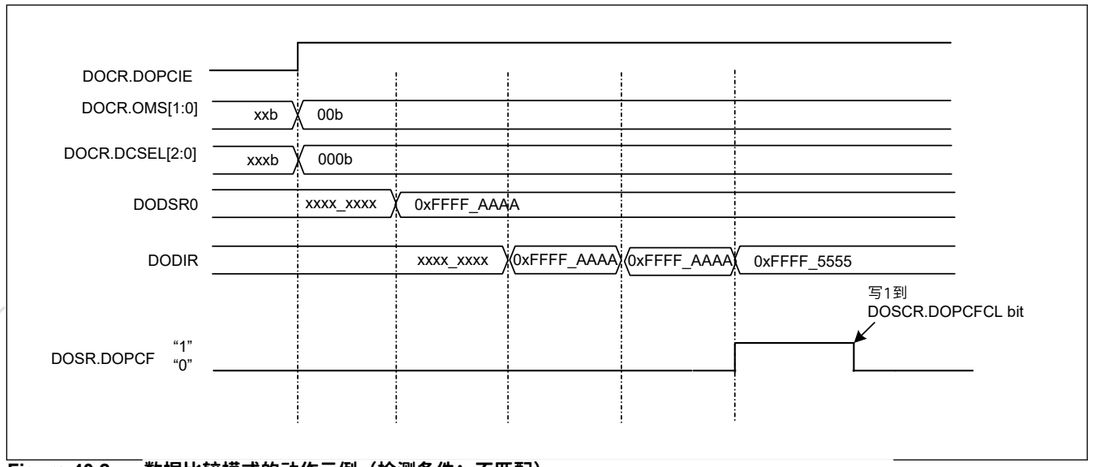


Figure 40.2 数据比较模式的动作示例（检测条件：不匹配）

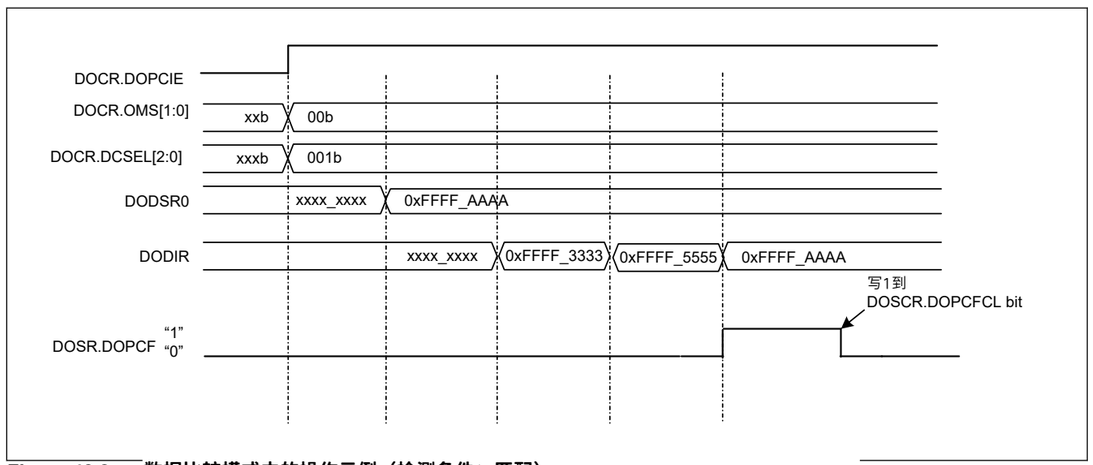


Figure 40.3 数据比较模式中的操作示例（检测条件：匹配）

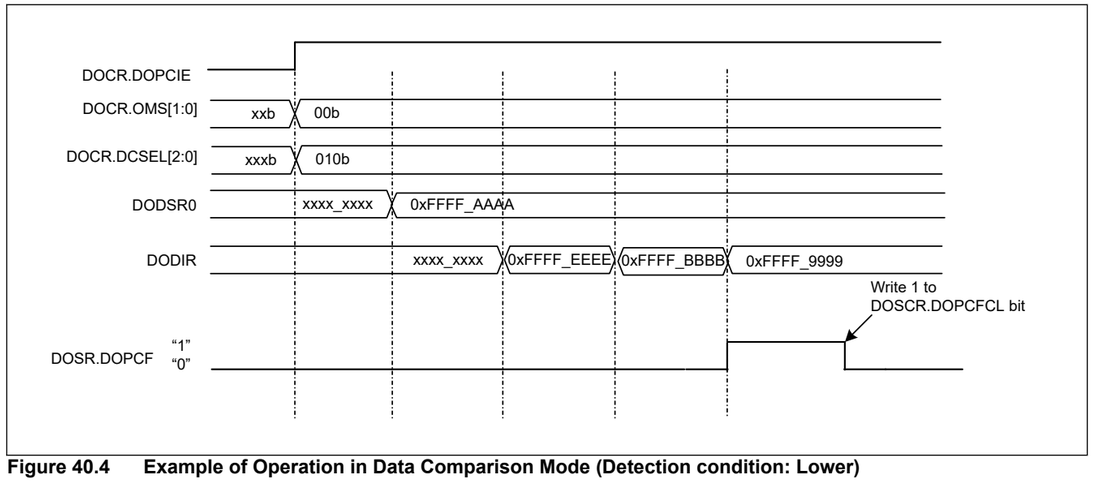


Figure 40.4 Example of Operation in Data Comparison Mode (Detection condition: Lower)

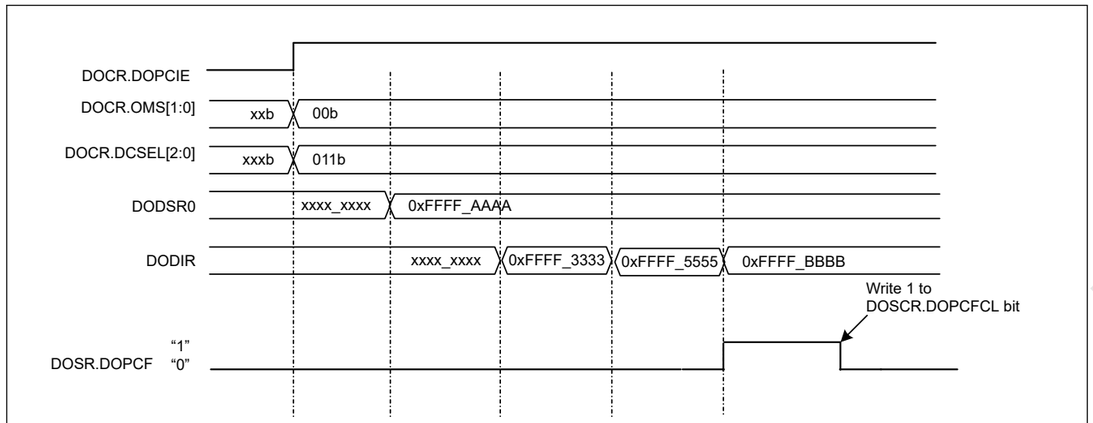


Figure 40.5 Example of Operation in Data Comparison Mode (Detection condition: Upper)

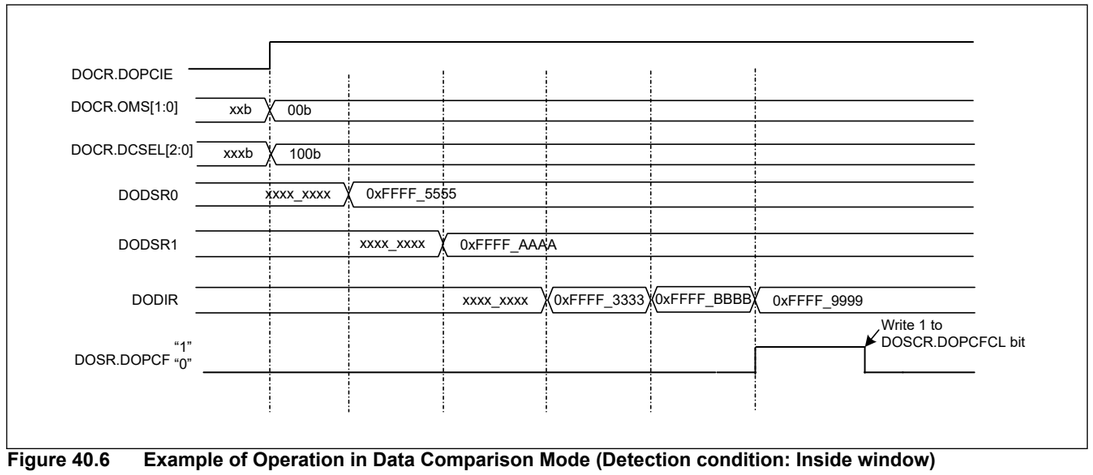


Figure 40.6 Example of Operation in Data Comparison Mode (Detection condition: Inside window)

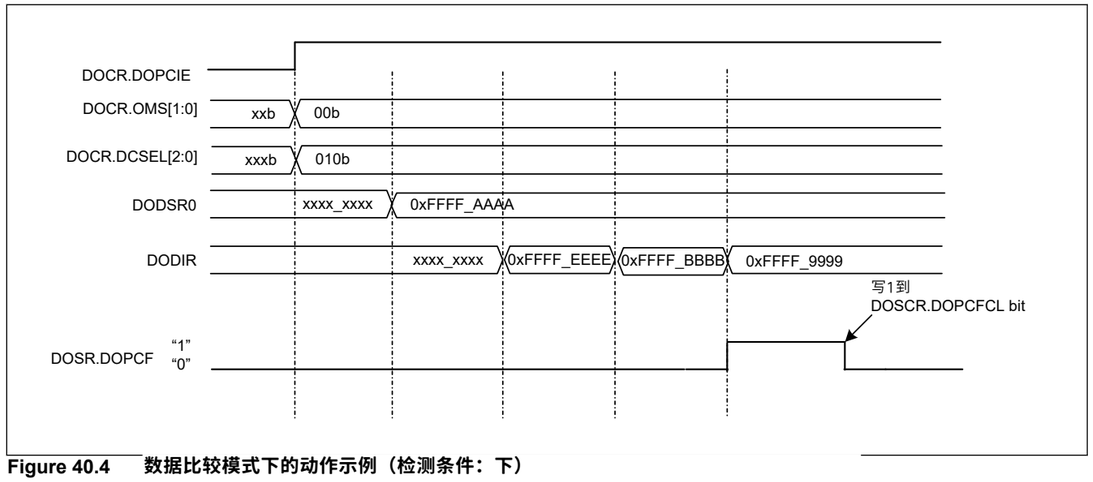


Figure 40.4 数据比较模式下的动作示例（检测条件：下）

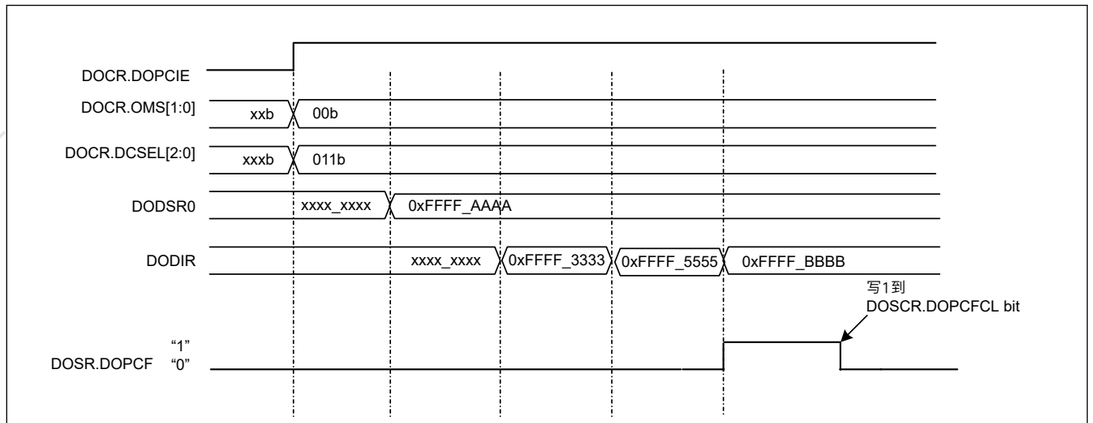


Figure 40.5 数据比较模式的动作示例（检测条件：上）

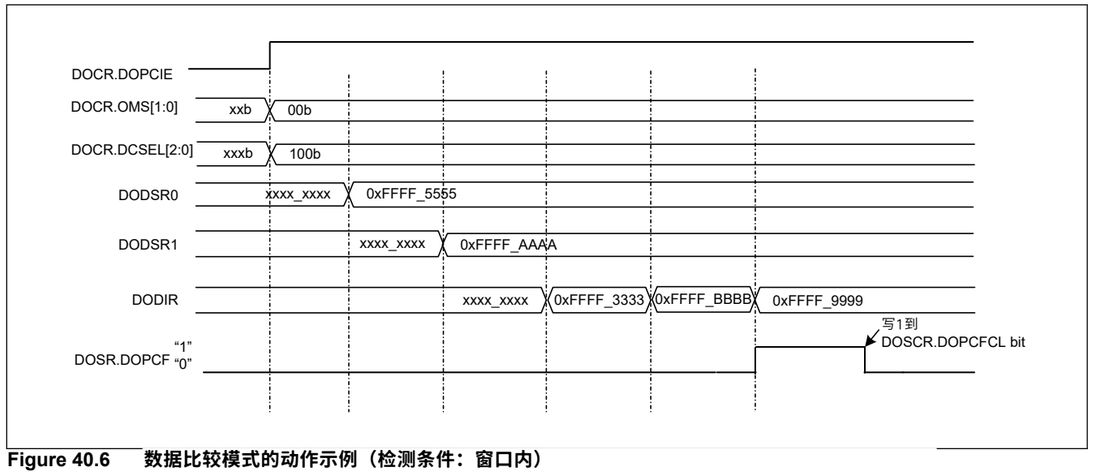


Figure 40.6 数据比较模式的动作示例（检测条件：窗口内）

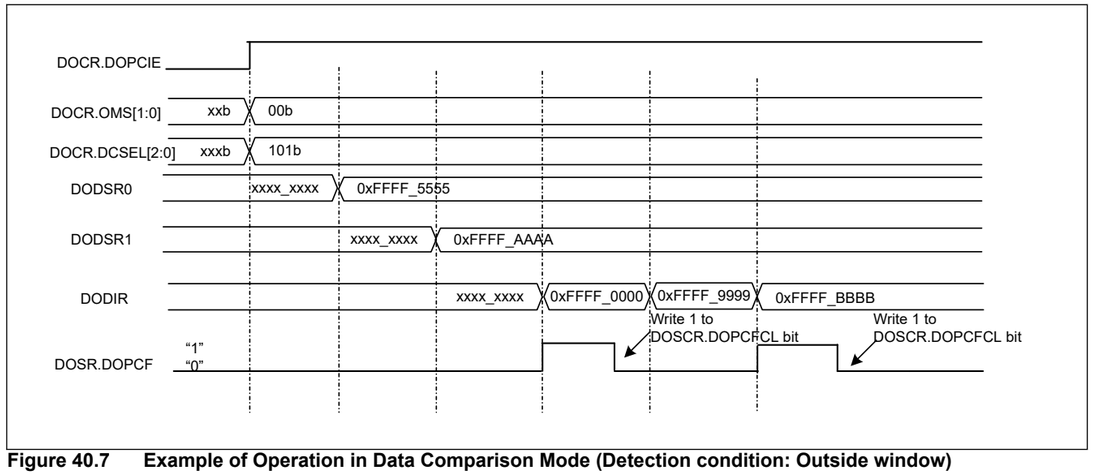


Figure 40.7 Example of Operation in Data Comparison Mode (Detection condition: Outside window)

40.3.2 Data Addition Mode

Figure 40.8 shows an example of the steps involved in data addition mode *1 operation by the data operation circuit.

The following is an example of operation when the bit width of data operation is 32-bit.

1. Writing 01b to the DOCR.OMS[1:0] bits selects data addition mode.
2. 32-bit data is set in the DODSR0 register as the initial value.
3. 32-bit data to be added is written to DODIR. The result of the operation is stored in DODSR0.
4. Writing of 32-bit data continues until all data for addition have been written to DODIR.
5. If the result of an operation is greater than 0xFFFF_FFFF, the DOSR.DOPCF flag is set to 1 and an ELC event is generated. When the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also generated.

Note 1. Addition is executed only by writing to the DODIR.

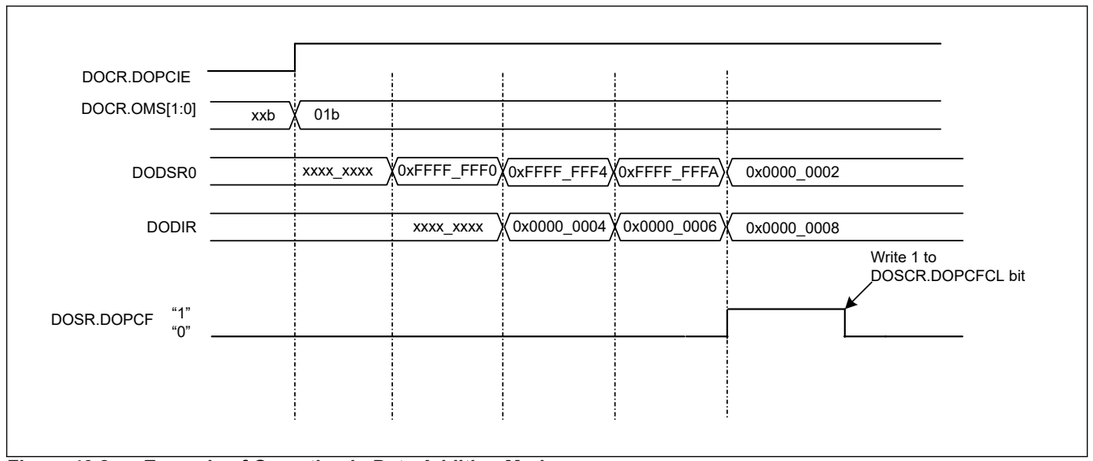


Figure 40.8 Example of Operation in Data Addition Mode

40.3.3 Data Subtraction Mode

Figure 40.9 shows an example of the steps involved in data subtraction mode *1 operation by the data operation circuit.

The following is an example of operation when the bit width of data operation is 32-bit.

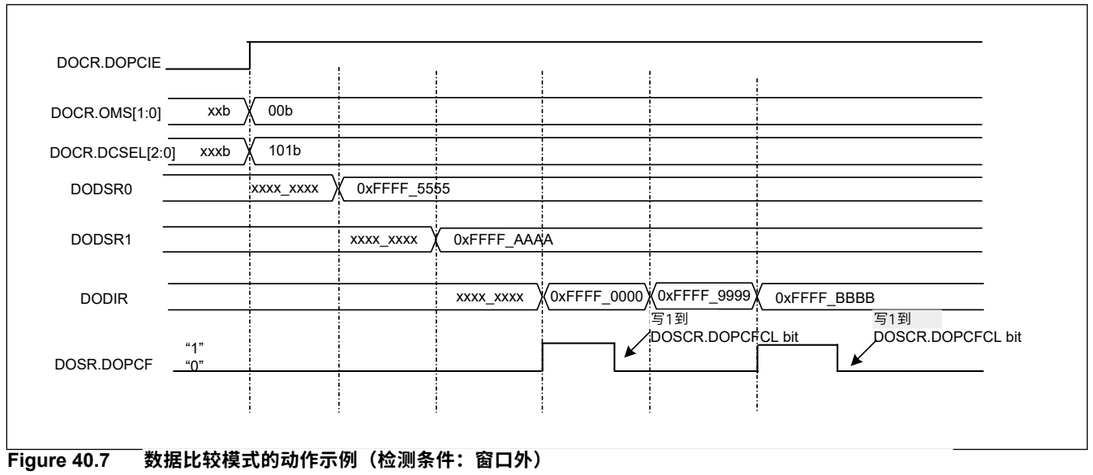


Figure 40.7 数据比较模式的动作示例（检测条件：窗口外）

40.3.2 数据加法模式

图40.8显示了数据运算电路的数据添加模式*1操作中涉及的步骤示例。

以下是数据操作的位宽为32位时的操作示例。

1.将01b写入DOCR.OMS[1:0]位选择数据添加模式。

2.在DODSR0寄存器中设置32位数据作为初始值。

3.将要添加的32位数据写入DODIR。运算结果存储在DODSR0中。

4.继续写入32位数据，直到所有要加法的数据都写入DODIR。

5.如果操作结果大于0xFFFF_FFFF，则DOSR.DOPCF标志设置为1，并生成ELC事件。当DOCR.DOPCIE位为1时，也会产生数据操作电路中断。

注1.仅通过写入DODIR来执行加法。

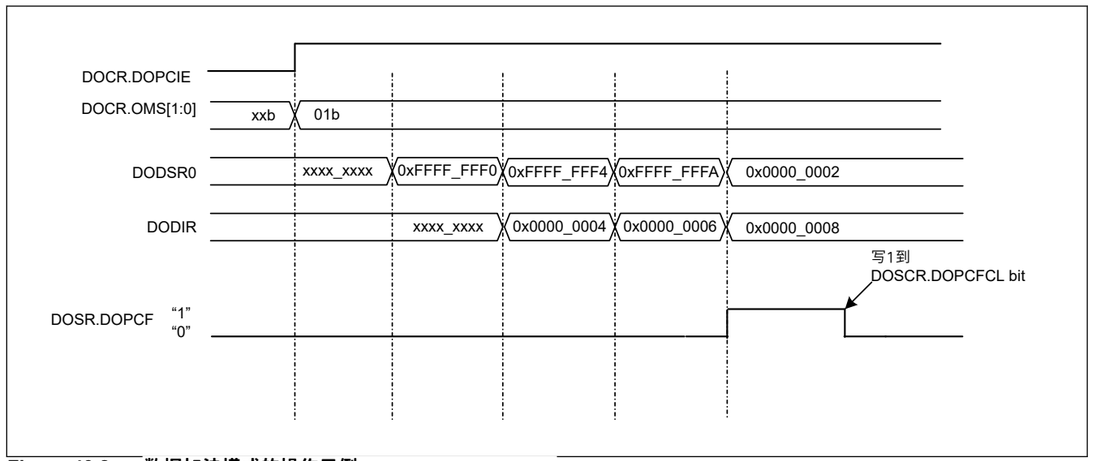


Figure 40.8 数据加法模式的操作示例

40.3.3 数据减法模式

图40.9显示了数据运算电路在数据减法模式*1操作中涉及的步骤示例。

以下是数据操作的位宽为32位时的操作示例。

1. Writing 10b to the DOCR.OMS[1:0] bits selects data subtraction mode.
2. 32-bit data is set in the DODSR0 register as the initial value.
3. 32-bit data to be subtracted is written to DODIR. The result of the operation is stored in DODSR0.
4. Writing of 32-bit data continues until all data for subtraction have been written to DODIR.
5. If the result of an operation is less than 0x0000_0000, the DOSR.DOPCF flag is set to 1 and an ELC event is generated. When the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also generated.

Note 1. Subtraction is executed only by writing to the DODIR.

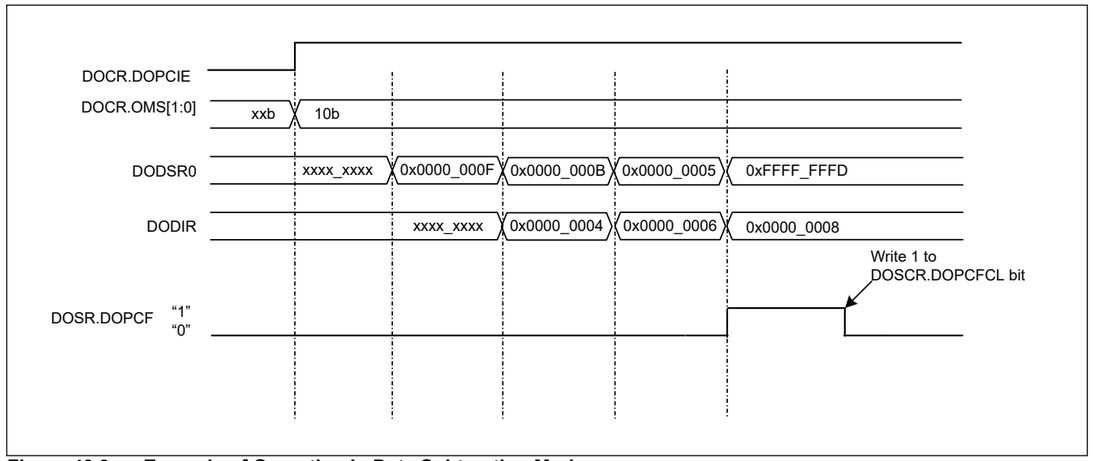


Figure 40.9 Example of Operation in Data Subtraction Mode

40.4 Interrupt Source

The data operation circuit generates the data operation circuit interrupt (DOC_DOPCI) as an interrupt request. When an interrupt source is generated, the data operation circuit flag corresponding to the interrupt is set to 1, when the data operation circuit interrupt enable bit is enabled, interrupt request signal is generated. Table 40.2 describes the interrupt request.

Table 40.2 Interrupt request from DOC

Interrupt request	Status flag	Interrupt source
DOC interrupt	DOPCF	• The compared values match the detection condition. • The result of data addition is greater than 0xFFFF (DOCR.DOBW = 0) or 0xFFFF_FFFF (DOCR.DOBW = 1). • The result of data subtraction is less than 0x0000 (DOCR.DOBW = 0) or 0x0000_0000 (DOCR.DOBW = 1).

40.5 Event Link Output

The DOC outputs event signals for the event link controller (ELC) under the following conditions, and these can be used to initiate operations by other modules selected in advance.

- The compared values match the detection condition
- The data addition result is greater than 0xFFFF (DOCR.DOBW = 0) or 0xFFFF_FFFF (DOCR.DOBW = 1)
- The data subtraction result is less than 0x0000 (DOCR.DOBW = 0) or 0x0000_0000 (DOCR.DOBW = 1)

40.6 Interrupt Handling and Event Linking

The DOC has a bit to enable or disable interrupts. An interrupt request signal is output for the CPU when an interrupt source is generated while the corresponding enable bit is enabled.

1.向DOCR.OMS[1:0]位写入10b选择数据减法模式。

2.在DODSR0寄存器中设置32位数据作为初始值。

3.将要减去的32位数据写入DODIR。运算结果存储在DODSR0中。

4.继续写入32位数据，直到所有减法数据都已写入DODIR。

5.如果操作结果小于0x0000_0000，则DOSR.DOPCF标志设置为1，并生成ELC事件。当DOCR.DOPCIE位为1时，也会产生数据操作电路中断。

注1.减法只能通过写入DODIR来执行。

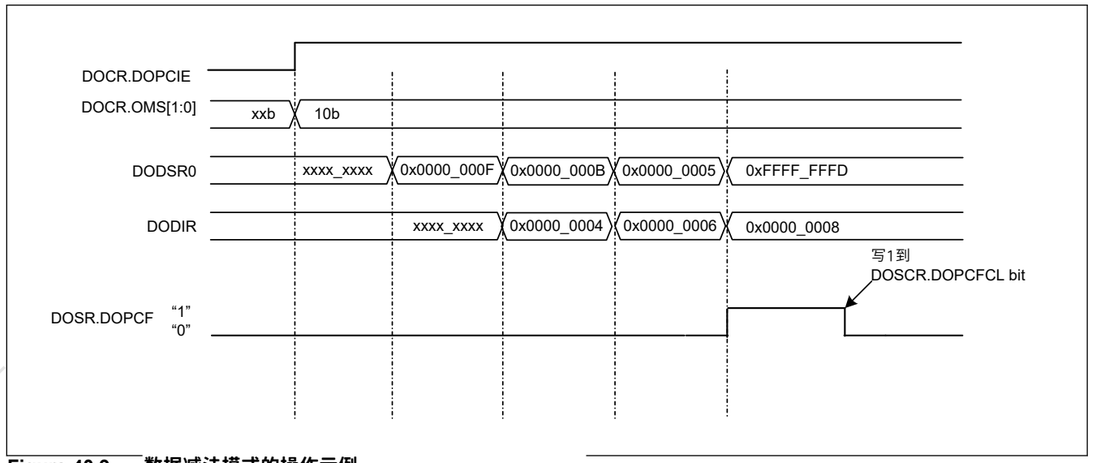


Figure 40.9 数据减法模式的操作示例

40.4 中断源

数据运算电路产生数据运算电路中断(DOC_DOPCI)作为中断请求。当产生中断源时，中断对应的数据运算电路标志置1，当数据运算电路中断使能位使能时，产生中断请求信号。表40.2描述了中断请求。

Table 40.2 来自DOC的中断请求

中断请求	状态标志	中断源
文档中断	DOPCF	• 比较值与检测条件匹配。 • 数据相加的结果大于0xFFFF(DOCR.DOBW=0)或0xFFFF_FFFF(DOCR.DOBW=1)。 • 数据减法的结果小于0x0000(DOCR.DOBW=0)或0x0000_0000(DOCR.DOBW=1)。

40.5 事件链接输出

DOC在以下条件下为事件链接控制器(ELC)输出事件信号，这些信号可用于启动预先选择的其他模块的操作。

- ●比较值符合检测条件
- ●数据相加结果大于0xFFFF（DOCR.DOBW=0）或0xFFFF_FFFF（DOCR.DOBW=1）
- ●数据减法结果小于0x0000（DOCR.DOBW=0）或0x0000_0000（DOCR.DOBW=1）

40.6 中断处理和事件链接

DOC有一个位来启用或禁用中断。当相应的使能位使能时产生中断源时，向CPU输出中断请求信号。

In contrast, an event link output signal is sent to other modules as an event signal via the ELC when an interrupt source is generated, regardless of the setting of the corresponding interrupt enable bit.

40.7 Usage Notes

40.7.1 Settings for the Module-Stop State

The module Stop Control Register C (MSTPCRC) can enable or disable DOC operation. The DOC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

相反，当产生中断源时，事件链接输出信号作为事件信号通过ELC发送到其他模块，而不管相应中断使能位的设置如何。

40.7 使用说明

40.7.1 模块停止状态的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用DOC操作。DOC在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

41. SRAM

41.1 Overview

The MCU provides an on-chip, high-density SRAM module with Error Correction Code (ECC).

Table 41.1 lists the SRAM specifications.

Table 41.1 SRAM specifications

Item	Specification
SRAM capacity	SRAM0: 64 KB
SRAM address	SRAM0: 0x2000_0000 to 0x2000_FFFF
Access	No wait states are inserted into the read cycle.
Data retention function	Not available in deep standby mode
Module-stop function	Module-stop state can be set to reduce power consumption
Error checking	SEC-DED (Single-Error Correction and Double-Error Detection Code)
Security	TrustZone Filter is integrated for memory access and SFR access. Access to the memory space is controlled by setting the memory Security Attribution (SA). And, access to I/O space (SFR) space is controlled by setting the register SA. See section 41.3.5. TrustZone Filter function.

41.2 Register Descriptions

41.2.1 SRAMSAR : SRAM Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SRAMSA2	—	SRAMSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SRAMSA0	Security attributes of registers for SRAM Protection 0: Secure 1: Non-Secure	R/W
1	—	This bit is read as 1. The write value should be 1.	R/W
2	SRAMSA2	Security attributes of registers for ECC Relation 0: Secure 1: Non-Secure	R/W
31:3	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SRAMSA0 bit (Security attributes of registers for SRAM Protection)

Security attributes of registers for Standby SRAM Protection. The target registers are as follow.

- PARIOAD
- SRAMPRCR

41. SRAM

41.1 Overview

MCU提供片上高密度SRAM模块，带有纠错码(ECC)。

表41.1列出了SRAM规格。

Table 41.1 SRAM specifications

Item	Specification
SRAM capacity	SRAM0: 64 KB
SRAM address	SRAM0: 0x2000_0000 to 0x2000_FFFF
Access	没有等待状态被插入到读取周期中。
数据保留功能	在深度待机模式下不可用
Module-stop function	可设置模块停止状态以降低功耗
错误检查	SEC-DED（单纠错双纠错码）
Security	TrustZone过滤器集成用于内存访问和SFR访问。通过设置内存安全属性（SA）来控制对内存空间的访问。并且，通过设置寄存器SA来控制对IO空间(SFR)空间的访问。请参阅第41.3.5节。TrustZone过滤功能。

41.2 注册说明

41.2.1 SRAMSAR：SRAM安全属性寄存器

Base address: CPSCU = 0x4000_8000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SRAMSA2	—	SRAMSA0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SRAMSA0	SRAM保护寄存器的安全属性 0: Secure 1: Non-Secure	R/W
1	—	该位读取为1。写入值应为1。	R/W
2	SRAMSA2	ECC关系寄存器的安全属性 0: Secure 1: Non-Secure	R/W
31:3	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

SRAMSA0位（SRAM保护寄存器的安全属性）

用于备用SRAM保护的寄存器的安全属性。目标寄存器如下。

- PARIOAD
- SRAMPRCR

SRAMSA2 bit (Security attributes of registers for ECC Relation)

Security attributes of registers for ECC Relation. The target registers are as follow.

- ECCMODE
- ECC2STS
- ECC1STSEN
- ECC1STS
- ECCPRCR
- ECCPRCR2
- ECCETST
- ECCOAD

41.2.2 PARIOAD : SRAM Parity Error Operation After Detection Register

Base address: SRAM = 0x4000_2000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation After Detection 0: Non-maskable interrupt 1: Reset	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The PARIOAD register controls the operation on detection of a parity error. The SRAM Protection Register (SRAMPRCR) protects this register against writes. Always set the SRAMPRCR bit in SRAMPRCR to enabled before writing to this bit. Do not write to the PARIOAD register while accessing the SRAM.

OAD bit (Operation After Detection)

The OAD bit specifies either a reset or non-maskable interrupt when a parity error is detected. The OAD bit is used for Standby SRAM.

41.2.3 SRAMPRCR : SRAM Protection Register

Base address: SRAM = 0x4000_2000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW[6:0]							SRAM PRCR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRAMPRCR	Register Write Control 0: Disable writes to protected registers 1: Enable writes to protected registers	R/W

SRAMSA2位（ECC关系寄存器的安全属性）

ECC关系的寄存器的安全属性。目标寄存器如下。

- ECCMODE
- ECC2STS
- ECC1STSEN
- ECC1STS
- ECCPRCR
- ECCPRCR2
- ECCETST
- ECCOAD

41.2.2 PARIOAD：检测寄存器后的SRAM奇偶校验错误操作

Base address: SRAM = 0x4000_2000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OAD
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	检测后的操作 0：不可屏蔽中断1：复位	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

PARIOAD寄存器控制检测奇偶校验错误时的操作。SRAM保护寄存器(SRAMPRCR)保护该寄存器不被写入。在写入该位之前，始终将SRAMPRCR中的SRAMPRCR位设置为启用。访问SRAM时不要写入PARIOAD寄存器。

OAD位（检测后操作）

当检测到奇偶校验错误时，OAD位指定复位或不可屏蔽中断。OAD位用于
Standby SRAM.

41.2.3 SRAMPRCR:SRAM保护寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW[6:0]							SRAM PRCR
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRAMPRCR	寄存器写控制 0：禁止写入受保护寄存器1：允许写入受保护寄存器	R/W

Bit	Symbol	Function	R/W
7:1	KW[6:0]	Write Key Code These bits enable or disable writes to the SRAMPRCR bit	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

SRAMPRCR bit (Register Write Control)

The SRAMPRCR bit controls the write mode of the PARIOAD register. Setting the bit to 1 enables writes to the PARIOAD register. When you write to this bit, always write 0x78 to KW[6:0] bits simultaneously.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the SRAMPRCR bit. When you write to the SRAMPRCR bit, always write 0x78 to these bits simultaneously. When a value other than 0x78 is written to KW[6:0], the SRAMPRCR bit is not updated. The KW[6:0] bits are always read as 0x00.

41.2.4 ECCMODE : ECC Operating Mode Control Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ECCMOD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ECCMOD[1:0]	ECC Operating Mode Select 0 0: Disable ECC function 0 1: Setting prohibited 1 0: Enable ECC function without error checking 1 1: Enable ECC function with error checking	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The ECCMODE register specifies the ECC operating mode. The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this register, set the ECCPRCR bit in the ECCPRCR register to 1 (write protection disabled). Do not write to the ECCMODE register while accessing the SRAM.

ECCMOD[1:0] bits (ECC Operating Mode Select)

The ECCMOD[1:0] bits set the SRAM0 ECC operating mode.

41.2.5 ECC2STS : ECC 2-Bit Error Status Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC1

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ECC2 ERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:1	KW[6:0]	编写关键代码 这些位启用或禁用对SRAMPRCR位的写入	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

SRAMPRCR位（寄存器写控制）

SRAMPRCR位控制PARIOAD寄存器的写模式。将该位设置为1可以写入PARIOAD寄存器。写入该位时，始终同时将0x78写入KW[6:0]位。

KW[6:0]位（写入密钥代码）

KW[6:0]位启用或禁用对SRAMPRCR位的写入。当您写入SRAMPRCR位时，请始终同时将0x78写入这些位。当向KW[6:0]写入0x78以外的值时，SRAMPRCR位不会更新。KW[6:0]位总是被读取为0x00。

41.2.4 ECCMODE:ECC操作模式控制寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0xC0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ECCMOD[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ECCMOD[1:0]	ECC操作模式选择 00：禁用ECC功能01：设置禁止10：启用ECC功能不进行错误检查11：启用ECC功能并进行错误检查	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ECCMODE寄存器指定ECC工作模式。ECC保护寄存器(ECCPRCR)保护该寄存器不被写入。在写入该寄存器之前，将ECPCRR寄存器中的ECPCRR位设置为1（禁用写保护）。访问SRAM时不要写入ECCMODE寄存器。

ECCMOD[1:0]位（ECC操作模式选择）

ECCMOD[1:0]位设置SRAM0ECC工作模式。

41.2.5 ECC2STS：ECC2位错误状态寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0xC1

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ECC2 ERR
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECC2ERR	ECC 2-Bit Error Status 0: No 2-bit ECC error occurred 1: 2-bit ECC error occurred	R/W*1
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Only 0 can be written to clear the bit.

ECC2ERR bit (ECC 2-Bit Error Status)

The ECC2ERR bit indicates whether a 2-bit ECC error occurred in SRAM0. When a 2-bit error is detected while ECC operations are enabled and error checking is selected, theECC2ERR bit is set to 1. The SRAM error signal is also asserted at this time. The 2-bit ECC error can be cleared by writing 0 to the ECC2ERR bit.

The SRAM error can be specified as a non-maskable interrupt or a reset in the ECCOAD register. Do not access the SRAM0 while writing 0 to this register.

41.2.6 ECC1STSEN : ECC 1-Bit Error Information Update Enable Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	E1STSEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	E1STSEN	ECC 1-Bit Error Information Update Enable 0: Disable updating of 1-bit ECC error information 1: Enable updating of 1-bit ECC error information	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The ECC1STSEN register enables or disables updating of the ECC 1-bit Error Status Register (ECC1STS) in response to a 1-bit error ECC error in the SRAM0.

The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this bit, set the ECCPRCR bit in the ECCPRCR register to 1 (write protection disabled).

E1STSEN bit (ECC 1-Bit Error Information Update Enable)

The E1STSEN bit enables or disables updating of the SRAM0 1-Bit Error Status Register (ECC1STS) in response to a 1-bit error in the SRAM0. This register also functions as an interrupt or a reset mask.

Bit	Symbol	Function	R/W
0	ECC2ERR	ECC2位错误状态 0：未发生2位ECC错误1：发生2位ECC错误	R/W*1
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.只能写入0来清除该位。

ECC2ERR位（ECC2位错误状态）

ECC2ERR位指示SRAM0中是否发生2位ECC错误。当启用ECC操作并选择错误检查时检测到2位错误时，ECC2ERR位设置为1。此时SRAM错误信号也被置位。将0写入ECC2ERR位可清除2位ECC错误。

SRAM错误可以指定为不可屏蔽中断或ECCOAD寄存器中的复位。不要访问SRAM0同时向该寄存器写入0。

41.2.6 ECC1STSEN：ECC1位错误信息更新使能寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0xC2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	E1STSEN
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	E1STSEN	ECC1位错误信息更新启用 0：禁止更新1位ECC错误信息1：允许更新1位ECC错误信息	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ECC1STSEN寄存器启用或禁用ECC1位错误状态寄存器(ECC1STS)的更新，以响应SRAM0中的1位错误ECC错误。

ECC保护寄存器(ECCPRCR)保护该寄存器不被写入。在写入该位之前，将ECPCRR寄存器中的ECPCRR位设置为1（禁用写保护）。

E1STSEN位（ECC1位错误信息更新使能）

E1STSEN位启用或禁用SRAM01位错误状态寄存器(ECC1STS)的更新，以响应SRAM0中的1位错误。该寄存器还用作中断或复位掩码。

41.2.7 ECC1STS : ECC 1-Bit Error Status Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC3

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ECC1ERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECC1ERR	ECC 1-Bit Error Status 0: No 1-bit ECC error occurred 1: 1-bit ECC error occurred	R/(W)*1
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Only 0 can be written to clear the bit.

ECC1ERR bit (ECC 1-Bit Error Status)

The ECC1ERR bit indicates whether a 1-bit ECC error occurred in the SRAM0. When a 1-bit error is detected while ECC operations are enabled and error checking is selected, theECC1ERR bit is set to 1. The SRAM error signal is also asserted at this time. The 1-bit ECC error can be cleared by writing 0 to the ECC1ERR bit.

The SRAM error can be specified as a non-maskable interrupt or a reset in the ECCOAD register. Do not access the SRAM0 while writing 0 to this register.

41.2.8 ECCPRCR : ECC Protection Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW[6:0]							ECCPRCR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECCPRCR	Register Write Control 0: Disable writes to the protected registers 1: Enable writes to the protected registers	R/W
7:1	KW[6:0]	Write Key Code 0x78: Enable write to the ECCPRCR bit Others: Disable write to the ECCPRCR bit	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

ECCPRCR bit (Register Write Control)

The ECCPRCR bit controls the write of the ECCMODE, ECC1STSEN, and ECCOAD registers. When this bit is set to 1, writing to the ECCMODE, ECC1STSEN, and ECCOAD registers is enabled. When writing to this bit, write 0x78 to the KW[6:0] bits at the same time.

41.2.7 ECC1STS:ECC1位错误状态寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0xC3

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ECC1ERR
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECC1ERR	ECC1位错误状态 0：未发生1位ECC错误1：发生1位ECC错误	R/(W)*1
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.只能写入0来清除该位。

ECC1ERR位（ECC1位错误状态）

ECC1ERR位指示SRAM0中是否发生1位ECC错误。如果在启用ECC操作并选择错误检查时检测到1位错误，则ECC1ERR位设置为1。此时SRAM错误信号也被置位。将0写入ECC1ERR位可清除1位ECC错误。

SRAM错误可以指定为不可屏蔽中断或ECCOAD寄存器中的复位。不要访问SRAM0同时向该寄存器写入0。

41.2.8 ECPCRR:ECC保护寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0xC4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW[6:0]							ECCPRCR
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECCPRCR	寄存器写控制 0：禁止写入受保护寄存器1：允许写入受保护寄存器	R/W
7:1	KW[6:0]	编写关键代码 0x78：允许写入ECPCRR位 其他：禁止写入ECPCRR位	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ECPCRR位（寄存器写控制）

ECPCRR位控制ECCMODE、ECC1STSEN和ECCOAD寄存器的写入。当该位设置为1时，允许写入ECCMODE、ECC1STSEN和ECCOAD寄存器。写入该位时，同时将0x78写入KW[6:0]位。

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the ECCPRCR bit. When writing toECCPRCR bit, write 0x78 to the KW[6:0] bits at the same time. When a value other than 0x78 is written to theKW[6:0] bits, the ECCPRCR bit is not updated. The KW[6:0] bits are always read as 0x00.

41.2.9 ECCPRCR2 : ECC Protection Register 2

Base address: SRAM = 0x4000_2000

Offset address: 0xD0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW2[6:0]							ECCP RCR2
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECCPRCR2	Register Write Control 0: Disable writes to the protected registers 1: Enable writes to the protected registers	R/W
7:1	KW2[6:0]	Write Key Code 0x78: Enable write to the ECCPRCR2 bit Others: Disable write to the ECCPRCR2 bit	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

ECCPRCR2 bit (Register Write Control)

The ECCPRCR2 bit controls the write mode of the ECCETST register. When the ECCPRCR2 bit is set to 1, writes to the ECCETST register is enabled. When writing to this bit, write 0x78 to the KW2[6:0] bits at the same time.

KW2[6:0] bits (Write Key Code)

The KW2[6:0] bits enable or disable writes to the ECCPRCR2 bit. When writing to ECCPRCR2 bit, write 0x78 to the KW2[6:0] bits at the same time. When a value other than 0x78 is written to the KW2[6:0] bits, the ECCPRCR2 bit is not updated. The KW2[6:0] bits are always read as 0x00.

41.2.10 ECCETST : ECC Test Control Register

Base address: SRAM = 0x4000_2000

Offset address: 0xD4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TSTB YP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSTBYP	ECC Bypass Select 0: Disable ECC bypass 1: Enable ECC bypass	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

KW[6:0]位（写入密钥代码）

KW[6:0]位启用或禁用对ECPCRR位的写入。写入ECCPRCR位时，同时向KW[6:0]位写入0x78。当向KW[6:0]位写入0x78以外的值时，不会更新ECPCRR位。KW[6:0]位总是被读取为0x00。

41.2.9 ECPCRR2:ECC保护寄存器2

Base address: SRAM = 0x4000_2000

Offset address: 0xD0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW2[6:0]							ECCP RCR2
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECCPRCR2	寄存器写控制 0：禁止写入受保护寄存器1：允许写入受保护寄存器	R/W
7:1	KW2[6:0]	编写关键代码 0x78：允许写入ECPCRR2位 其他：禁止写入ECPCRR2位	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ECPCRR2位（寄存器写控制）

ECPCRR2位控制ECCETST寄存器的写模式。当ECPCRR2位设置为1时，写入ECCETST寄存器使能。写入该位时，同时向KW2[6:0]位写入0x78。

KW2[6:0]位（写入密钥代码）

KW2[6:0]位启用或禁用对ECPCRR2位的写入。当写入ECPCRR2位时，将0x78写入KW2[6:0]位。当向KW2[6:0]位写入0x78以外的值时，不会更新ECPCRR2位。KW2[6:0]位总是读为0x00。

41.2.10 ECCETST:ECC测试控制寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0xD4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TSTB YP
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSTBYP	ECC旁路选择 0：禁用ECC旁路1：启用ECC旁路	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

The ECC Protection Register 2 (ECCPRCR2) protects this register against writes. Before writing to this bit, set the ECCPRCR2 bit in the ECCPRCR2 register to 1 (write protection disabled). Do not write to the ECCETST register while accessing the SRAM.

TSTBYP bit (ECC Bypass Select)

The TSTBYP bit enables direct access to the ECC code by bypassing the ECC function. When the ECC bypass function is used, the ECCMOD[1:0] bits in the ECCMODE register are set to 00b. The ECC must be accessed in 32 bits using the same address for 32-bit data. The ECC code is assigned to the lower 7 bits of the 32-bit data. When writing the ECC code, the upper 25 bits are ignored. When reading the ECC code, the upper 25 bits are undefined.

Note: For details of ECC test, see section 41.3.4. ECC Decoder Testing.

41.2.11 ECCOAD : SRAM ECC Error Operation After Detection Register

Base address: SRAM = 0x4000_2000

Offset address: 0xD8

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation After Detection 0: Non-maskable interrupt 1: Reset	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this bit, set the ECCPRCR bit in the ECCPRCR register to 1 (write protection disabled). Do not write to the ECCOAD register while accessing the SRAM.

OAD bit (Operation After Detection)

The OAD bit selects whether to generate a reset or a non-maskable interrupt when an ECC error is detected. The OAD bit in the ECCOAD register is used for SRAM0.

41.3 Operation

41.3.1 Module Stop Function

Power consumption can be reduced by setting module stop control register A (MSTPCRA) to stop supply of the clock signal to SRAM.

SRAM0 is controlled by SRAM0 bit in MSTPCRA register and, in the case of 1, SRAM0 becomes the clock stop state.

The SRAM is thus placed in the module-stop state by stopping supply of the clock signals. The SRAM operates after a reset.

SRAM is not accessible if it is in the module-stop state. A transition to the module-stop state should not be made while access to SRAM is in progress.

Access to the SRAM in the module-stop state is prohibited. If access is attempted, correct operation is not guaranteed.

For details on the MSTPCRA register, see section 10, Low Power Modes.

ECC保护寄存器2(ECCPRCR2)保护该寄存器不被写入。在写入该位之前，将ECPCRR2寄存器中的ECPCRR2位为1（写保护禁用）。访问SRAM时不要写入ECCETST寄存器。

TSTBYP位（ECC旁路选择）

TSTBYP位允许通过绕过ECC功能直接访问ECC代码。使用ECC旁路功能时，ECCMODE寄存器中的ECCMOD[1:0]位设置为00b。必须使用32位数据的相同地址以32位访问ECC。ECC代码分配给32位数据的低7位。写入ECC代码时，忽略高25位。读取ECC码时，高25位未定义。

Note: 有关ECC测试的详细信息，请参见第41.3.4节。ECC解码器测试。

41.2.11 ECCOAD：检测寄存器后的SRAMECC错误操作

Base address: SRAM = 0x4000_2000

Offset address: 0xD8

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OAD
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	检测后的操作 0：不可屏蔽中断1：复位	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ECC保护寄存器(ECCPRCR)保护该寄存器不被写入。在写入该位之前，将ECPCRR寄存器中的ECPCRR位设置为1（禁用写保护）。访问SRAM时不要写入ECCOAD寄存器。

OAD位（检测后操作）

OAD位选择在检测到ECC错误时是否产生复位或不可屏蔽中断。ECCOAD寄存器中的OAD位用于SRAM0。

41.3 Operation

41.3.1 模块停止功能

通过设置模块停止控制寄存器A(MSTPCRA)停止向SRAM提供时钟信号，可以降低功耗。

SRAM0由MSTPCRA寄存器中的SRAM0位控制，在为1的情况下，SRAM0变为时钟停止状态。

因此，通过停止提供时钟信号，SRAM被置于模块停止状态。SRAM在复位后运行。

如果SRAM处于模块停止状态，则无法访问。在访问SRAM的过程中，不应转换到模块停止状态。

禁止在模块停止状态下访问SRAM。如果尝试访问，则无法保证正确操作。

有关MSTPCRA寄存器的详细信息，请参见第10节，低功耗模式。

41.3.2 Correction of ECC errors

Enabling and disabling of ECC error correction can be selected through ECCMODE register setting. In the initial state, ECC error correction is disabled. The ECC check type is SEC-DED (Single-Error Correction and Double-Error Detection Code).

When ECC function is enabled, 7-bit check bits are appended to 32-bit data for writing. For reading, 39-bit (data: 32 bits, check bits: 7 bits) data is read out from the SRAM.

When ECC function is enabled and error checking is selected by setting ECCMOD[1:0] in the ECCMODE register to 00b, error correction is done if a 1-bit error occurs and the ECC1ERR bit in the ECC1STS register is set to 1 if the E1STSEN bit in the ECC1STSEN register is 1. If a 2-bit error occurs, error detection is done and the ECC2ERR bit in the ECC2STS register is set to 1, though error correction is not performed.

When ECC function is enabled and the error checking is disable, error correction is done if a 1-bit error occurs but ECC1ERR bit in the ECC1STS register is not updated although E1STSEN bit in the ECC1STSEN register is 1. If a 2-bit error occurs, this error is detected but the ECC2ERR bit in the ECC2STS register is not updated, and error correction is not performed.

When ECC function is disable, neither error correction nor error detection is done although 1-bit or 2-bit error occur.

So ECC1ERR bit and ECC2ERR bit are not updated.

There is no way to confirm the location where the error was found. Therefore, when after the occurrence of an error, update all the data.

When updating all the data after the occurrence of an error, the only support of 32 bit data writing.

Since the SRAM data is undefined after power on and release from deep software standby mode, accessing the SRAM when ECC function is enabled and error checking is selected causes an ECC error to occur. Therefore, before using ECC function, initial writing with 32bit data size to the area to be used in the SRAM should be done.

When a read access is executed in a row after a write access, read access is executed with priority. Therefore, during initialization, please do not perform the read access in a row after the write access.

41.3.3 ECC Error Interrupt Function

When ECC function is enabled and error checking is applied to the SRAM, an ECC error occurs when either the ECC2ERR bit in the ECC2STS register or the ECC1ERR bit in the ECC1STS register becomes 1 to indicate that ECC checking revealed a 2-bit error or a 1-bit error, respectively.

An ECC erroris output with a pulse width of ICLK.When the ECC 1-bit error is to be masked, set the ECC1STSEN.E1STSEN bit to 0 to disable updating of the ECC1ERR bit. An ECC error will not be generated while ECC function is disabled or when ECC function is enabled but error checking is not selected.

ECC error can choose non maskable interrupt or reset by ECCOAD register. When set 1 in the OAD bit of the ECCOAD register, ECC error is output to the Reset function. When set 0 in the OAD bit of the ECCOAD register, ECC Error interrupt is output to the ICU as non-maskable interrupt.

41.3.4 ECC Decoder Testing

Figure 41.1 shows the ECC decoder testing.

41.3.2 纠正ECC错误

可以通过ECCMODE寄存器设置来选择ECC纠错的启用和禁用。在初始状态下，ECC纠错被禁用。ECC校验类型为SEC-DED（单纠错双错误检测码）。

当ECC功能使能时，7位校验位被附加到32位数据中进行写入。读取时，从SRAM中读出39位（数据：32位，校验位：7位）数据。

当ECC功能使能并且通过将ECCMODE寄存器中的ECCMOD[1:0]设置为00b来选择错误检查时，如果发生1位错误，则进行纠错，并且ECC1STS寄存器中的ECC1ERR位设置为1，如果ECC1STSEN寄存器中的E1STSEN位为1。如果发生2位错误，则进行错误检测并将ECC2STS寄存器中的ECC2ERR位设置为1，但不执行错误纠正。

当启用ECC功能且禁用错误检查时，如果发生1位错误，则进行错误纠正，但尽管ECC1STSEN寄存器中的E1STSEN位为1，但ECC1STS寄存器中的ECC1ERR位不更新。如果发生2位错误，则会检测到该错误，但不会更新ECC2STS寄存器中的ECC2ERR位，也不执行纠错。

当ECC功能被禁用时，即使发生1位或2位错误，也不会进行纠错或错误检测。

因此ECC1ERR位和ECC2ERR位不会更新。

无法确认发现错误的位置。因此，当发生错误后，更新所有数据。

发生错误后更新所有数据时，仅支持32位数据写入。

由于上电并从深度软件待机模式释放后SRAM数据未定义，因此在启用ECC功能并选择错误检查时访问SRAM会导致发生ECC错误。因此，在使用ECC功能之前，应先将32位数据大小的数据写入SRAM中要使用的区域。

在写访问之后连续执行读访问时，优先执行读访问。因此，在初始化过程中，请不要在写访问之后连续进行读访问。

41.3.3 ECC错误中断功能

当ECC功能使能并对SRAM应用错误检查时，当ECC2STS寄存器中的ECC2ERR位或ECC1STS寄存器中的ECC1ERR位变为1时，将发生ECC错误，表示ECC检查发现2位错误或分别为1位错误。

脉冲宽度为ICLK的ECC错误输出。当要屏蔽ECC1位错误时，设置ECC1STSEN.E1STSEN位为0以禁用ECC1ERR位的更新。禁用ECC功能或启用ECC功能但未选择错误检查时，不会产生ECC错误。

ECC错误可以选择不可屏蔽中断或通过ECCOAD寄存器复位。当ECCOAD寄存器的OAD位设置为1时，ECC错误输出到复位功能。当ECCOAD寄存器的OAD位设置为0时，ECC错误中断作为不可屏蔽中断输出到ICU。

41.3.4 ECC解码器测试

图41.1显示了ECC解码器测试。

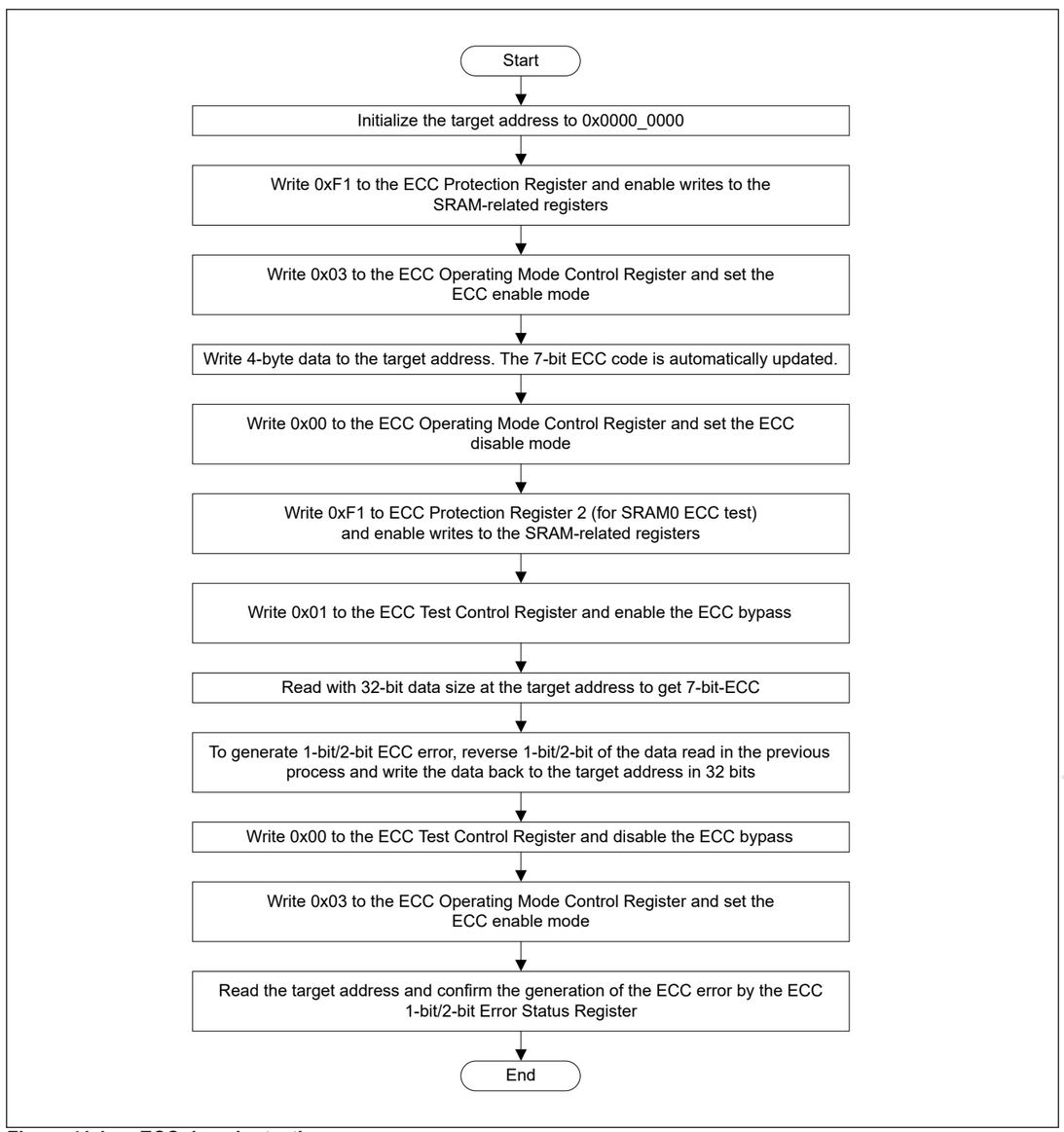


Figure 41.1 ECC decoder testing

41.3.5 TrustZone Filter function

There are two types of TrustZone Filter function for SRAM.

- TrustZone Filter for SRAM register protection
- TrustZone Filter for SRAM memory protection

41.3.5.1 TrustZone Filter for SRAM register protection

SRAM registers can be protected with a Security Attribution (SA) from Non-secure access. When SA indicates that SRAM registers are secure status, non-secure access can not overwrite them because TrustZone Filter detects finds an error and protects the write access. SA for SRAM registers is just one to be used commonly among SRAM registers.

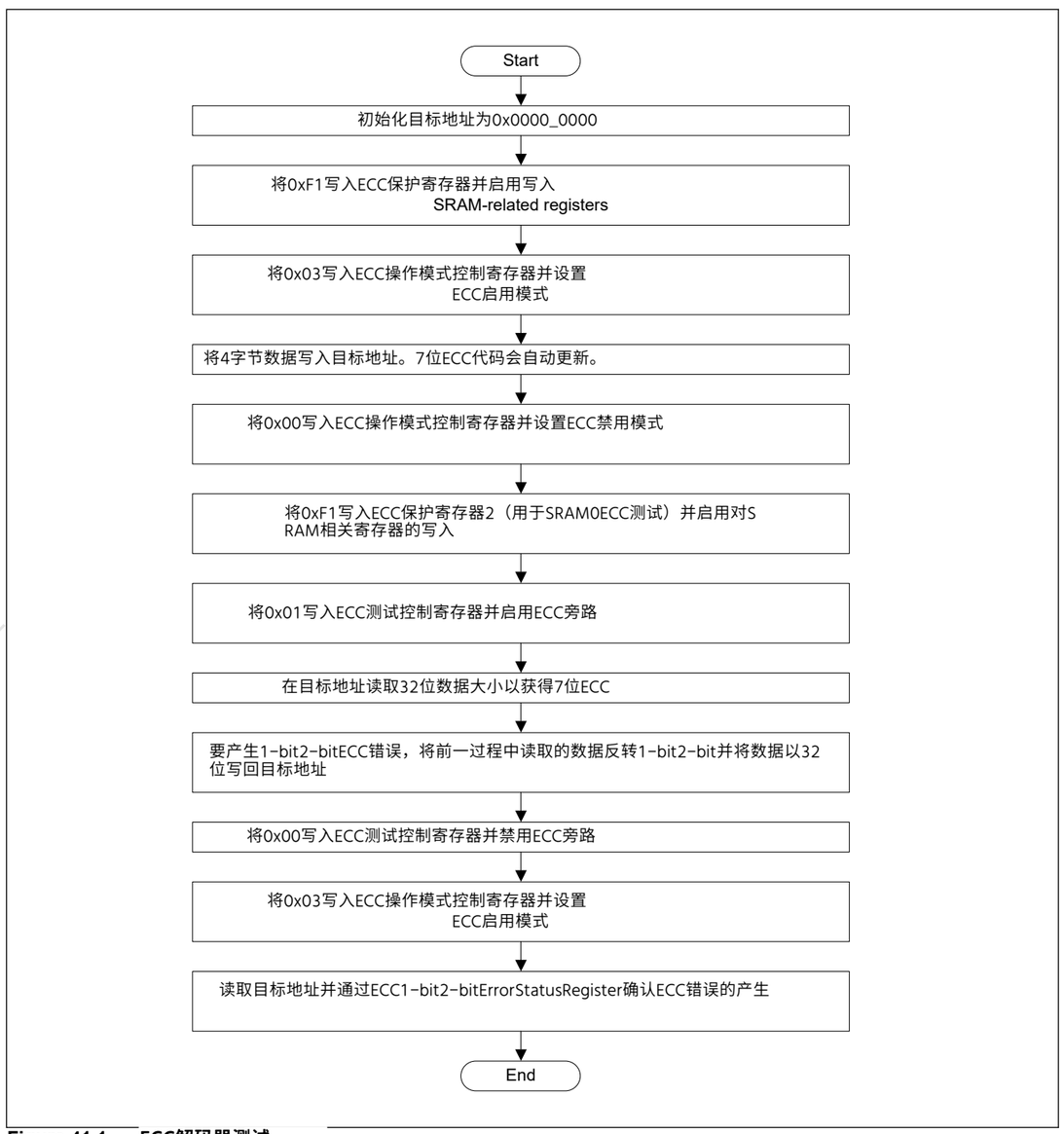


Figure 41.1 ECC解码器测试

41.3.5 TrustZone过滤器功能

SRAM有两种TrustZoneFilter功能。

●用于SRAM寄存器保护的TrustZone过滤器

●用于SRAM内存保护的TrustZone过滤器

41.3.5.1 用于SRAM寄存器保护的TrustZone过滤器

可以使用安全属性(SA)保护SRAM寄存器免受非安全访问。当SA指示SRAM寄存器处于安全状态时，非安全访问无法覆盖它们，因为TrustZoneFilter检测到发现错误并保护写访问。SRAM寄存器的SA只是SRAM寄存器中常用的一种。

Table 41.2 Register protection

SA	Access status	Write access	Read access
Secure	Secure	Permit	Permit
	Non-secure	TrustZone Filter error Protected	Permit
Non-secure	Secure	Permit	Permit
	Non-secure	Permit	Permit

When TrustZone Filter error for SRAM register access occurs, no error notification and no error response occurs.

41.3.5.2 TrustZone Filter for SRAM memory protection

SRAM memory can be divided into Secure/Non secure callable/Non secure status with Memory Security Attribution (MSA) and can be protected from Non-secure access. When MSA indicates that SRAM memory region are Secure or Non secure callable status, Non-secure access can't overwrite them.

Table 41.3 Memory protection

SA	Access status	Write access	Read access
Secure / Non secure callable	Secure	Permit	Permit
	Non-secure	TrustZone Filter error • Protected • Error response occurs	TrustZone Filter error • Read data is 0 • Error response occurs
Non-secure	Secure	Permit	Permit
	Non-secure	Permit	Permit

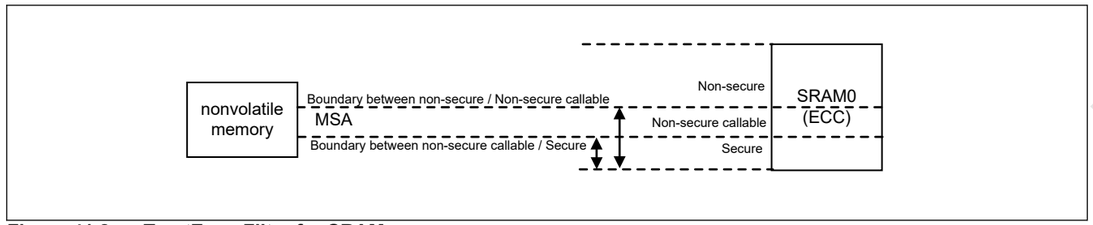


Figure 41.2 TrustZone Filter for SRAM memory

When TrustZone Filter error for SRAM memory access occurs, an error notification which become Reset request or NMI request occurs. See section 45.2. Arm TrustZone Security .

41.3.6 Interrupt Source

The SRAM interrupt source includes an ECC error and TrustZone filter error. ECC error can choose non-maskable interrupt or reset by OAD bit. When the debugger is connected, reset and non-maskable interrupt are maskable. Also, if these masks are set by the debugger, each status register is not set even if an ECC error occurs. For details on the debug mode, see section 2, CPU.

Table 41.4 SRAM Interrupt Source

Name	Interrupt Source	DTC Activation	DMAC Activation
ECCERR	ECC error	Not possible	Not possible
TZFLT	TrustZone filter error	Not possible	Not possible

41.3.7 Access Cycle

■ Number of cycles from the CPU

- When the cache is hit, access is one cycle.
- For cache off or non cacheable

Table 41.2 注册保护

SA	访问状态	写访问	读取权限
Secure	Secure	Permit	Permit
	Non-secure	TrustZone过滤器错误受保护	Permit
Non-secure	Secure	Permit	Permit
	Non-secure	Permit	Permit

当发生SRAM寄存器访问的TrustZoneFilter错误时，不会发生错误通知和错误响应。

41.3.5.2 用于SRAM内存保护的TrustZone过滤器

SRAM内存可分为SecureNonsecurecallableNonsecurestatuswithMemorySecurityAttribution(MSA)并且可以防止非安全访问。当MSA指示SRAM内存区域为安全或非安全可调用状态时，非安全访问无法覆盖它们。

Table 41.3 内存保护

SA	访问状态	写访问	读取权限
安全非安全可调用	Secure	Permit	Permit
	Non-secure	TrustZone过滤器错误● • 发生错误响应	TrustZone过滤器错误●读取数据为0 • 发生错误响应
Non-secure	Secure	Permit	Permit
	Non-secure	Permit	Permit

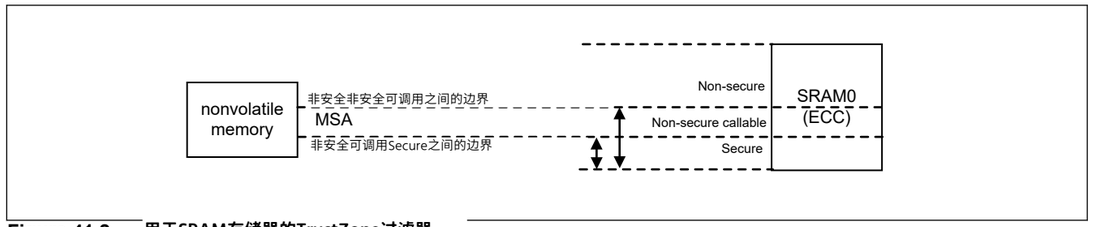


Figure 41.2 用于SRAM存储器的TrustZone过滤器

当发生SRAM内存访问的TrustZoneFilter错误时，会发生错误通知，成为Resetrequest或NMIrequest。请参见第45.2节。ArmTrustZone安全。

41.3.6 中断源

SRAM中断源包括ECC错误和TrustZone过滤器错误。ECC错误可以选择不可屏蔽中断或通过OAD位复位。当调试器连接时，复位和不可屏蔽中断都是可屏蔽的。此外，如果调试器设置了这些掩码，则即使发生ECC错误，也不会设置每个状态寄存器。有关调试模式的详细信息，请参见第2节CPU。

Table 41.4 SRAM中断源

Name	中断源	DTC Activation	DMAC Activation
ECCERR	ECC error	不可能	不可能
TZFLT	TrustZone过滤器错误	不可能	不可能

41.3.7 访问周期

■CPU的周期数

●当缓存命中时，访问为一个周期。

●对于缓存关闭或不可缓存

Table 41.5 SRAM0

Register Setting	Read (cycles)		Write (cycles)	
	Word access	Half-word/Byte access	Word access	Half-word/Byte access
ECC Off ECCMOD[1] = 0	3		2*1	
ECC On ECCMOD[1] = 1	3		2*1	4

Note 1. For efficiency of the access, when read access occurs to the same memory after write, memory write by the precedent write command delays it until for the next idle cycle or the next write access. When read continues, it is given priority to read.

- For cache on and cacheble (When the cache miss hit)

Table 41.6 SRAM0

Register Setting	Read (cycles)		Write (cycles)	
	Word access	Half-word/Byte access	Word access	Half-word/Byte access
ECC Off ECCMOD[1] = 0	3		1*1	
ECC On ECCMOD[1] = 1	3		1*1	

Note 1. For efficiency of the access, when read access occurs to the same memory after write, memory write by the precedent write command delays it until for the next idle cycle or the next write access. When read continues, it is given priority to read.

41.3.8 ECC encode specification

The following table shows ECC encoding specifications. Add the ECC cord (eout [6:0]) formed by the following calculating formula to higher 7 bits (din [38:32]) of write data and write in it at SRAM.

Table 41.7 ECC encode

ECC code	calculation formula
eout[6]	(din[13] ^ din[12] ^ din[11] ^ din[10] ^ din[9] ^ din[8] ^ din[7] ^ din[6] ^ din[5] ^ din[4] ^ din[3] ^ din[2] ^ din[1] ^ din[0])
eout[5]	(din[23] ^ din[22] ^ din[21] ^ din[20] ^ din[19] ^ din[18] ^ din[17] ^ din[16] ^ din[15] ^ din[14] ^ din[3] ^ din[2] ^ din[1] ^ din[0])
eout[4]	(din[29] ^ din[28] ^ din[27] ^ din[26] ^ din[25] ^ din[24] ^ din[17] ^ din[16] ^ din[15] ^ din[14] ^ din[7] ^ din[6] ^ din[5] ^ din[4])
eout[3]	(din[31] ^ din[30] ^ din[26] ^ din[25] ^ din[24] ^ din[20] ^ din[19] ^ din[18] ^ din[14] ^ din[10] ^ din[9] ^ din[8] ^ din[4] ^ din[0])
eout[2]	(din[31] ^ din[30] ^ din[28] ^ din[27] ^ din[24] ^ din[22] ^ din[21] ^ din[18] ^ din[15] ^ din[12] ^ din[11] ^ din[8] ^ din[5] ^ din[1])
eout[1]	~(din[30] ^ din[29] ^ din[27] ^ din[25] ^ din[23] ^ din[21] ^ din[19] ^ din[16] ^ din[13] ^ din[11] ^ din[9] ^ din[6] ^ din[2] ^ din[0])
eout[0]	~(din[31] ^ din[29] ^ din[28] ^ din[26] ^ din[23] ^ din[22] ^ din[20] ^ din[17] ^ din[13] ^ din[12] ^ din[10] ^ din[7] ^ din[3] ^ din[0])

Note: eout[6:0] = ECC code, din[31:0] = write data

Table 41.5 SRAM0

寄存器设置	Read (cycles)		Write (cycles)	
	字访问	Half-word/Byte access	字访问	Half-word/Byte access
ECC Off ECCMOD[1] = 0	3		2*1	
ECC On ECCMOD[1] = 1	3		2*1	4

注1.为提高访问效率，当写入后对同一内存进行读取访问时，先行写入命令的内存写入会将其延迟到下一个空闲周期或下一次写入访问。继续读取时，优先读取。

●forcacheonandcacheble（当缓存未命中时）

Table 41.6 SRAM0

寄存器设置	Read (cycles)		Write (cycles)	
	字访问	Half-word/Byte access	字访问	Half-word/Byte access
ECC Off ECCMOD[1] = 0	3		1*1	
ECC On ECCMOD[1] = 1	3		1*1	

注1.为提高访问效率，当写入后对同一内存进行读取访问时，先行写入命令的内存写入会将其延迟到下一个空闲周期或下一次写入访问。继续读取时，优先读取。

41.3.8 ECC编码规范

下表显示了ECC编码规范。将由以下计算公式形成的ECC线（eout[6:0]）添加到写入数据的高7位（din[38:32]）中，并写入SRAM中。

Table 41.7 ECC encode

ECC code	计算公式
eout[6]	(din[13] ^ din[12] ^ din[11] ^ din[10] ^ din[9] ^ din[8] ^ din[7] ^ din[6] ^ din[5] ^ din[4] ^ din[3] ^ din[2] ^ din[1] ^ din[0])
eout[5]	(din[23] ^ din[22] ^ din[21] ^ din[20] ^ din[19] ^ din[18] ^ din[17] ^ din[16] ^ din[15] ^ din[14] ^ din[3] ^ din[2] ^ din[1] ^ din[0])
eout[4]	(din[29] ^ din[28] ^ din[27] ^ din[26] ^ din[25] ^ din[24] ^ din[17] ^ din[16] ^ din[15] ^ din[14] ^ din[7] ^ din[6] ^ din[5] ^ din[4])
eout[3]	(din[31] ^ din[30] ^ din[26] ^ din[25] ^ din[24] ^ din[20] ^ din[19] ^ din[18] ^ din[14] ^ din[10] ^ din[9] ^ din[8] ^ din[4] ^ din[0])
eout[2]	(din[31] ^ din[30] ^ din[28] ^ din[27] ^ din[24] ^ din[22] ^ din[21] ^ din[18] ^ din[15] ^ din[12] ^ din[11] ^ din[8] ^ din[5] ^ din[1])
eout[1]	~(din[30] ^ din[29] ^ din[27] ^ din[25] ^ din[23] ^ din[21] ^ din[19] ^ din[16] ^ din[13] ^ din[11] ^ din[9] ^ din[6] ^ din[2] ^ din[0])
eout[0]	~(din[31] ^ din[29] ^ din[28] ^ din[26] ^ din[23] ^ din[22] ^ din[20] ^ din[17] ^ din[13] ^ din[12] ^ din[10] ^ din[7] ^ din[3] ^ din[0])

Note: eout[6:0]=ECC代码，din[31:0]=写入数据

42. Standby SRAM

42.1 Overview

An on-chip SRAM is provided to retain data in Deep Software Standby mode. Table 42.1 lists the Standby SRAM specifications.

Table 42.1 Standby SRAM specifications

Item	Description
SRAM capacity	1 KB
SRAM address	0x2800_0000 to 0x2800_03FF
Access	Standby SRAM clock is the same clock as the PCLKB. See section 42.3.5. Access Cycle for details.
Data retention function	Data can be retained in deep standby mode. See section 42.3.1. Data Retention for details.
parity	Even parity (data: 8 bits, parity: 1 bit)
Module-stop function	Module-stop state can be set to reduce power consumption. See section 42.3.2. Setting for the Module-stop Function for details.
Security	Permits the read and write operations to Standby RAM following TrustZone Filter function. See section 42.3.4. TrustZone Filter function for details.

42.2 Register Descriptions

42.2.1 STBRAMSAR : Standby RAM memory Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x014

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	NSBSTBR[3:0]			
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0

Bit	Symbol	Function	R/W
3:0	NSBSTBR[3:0]	Security attributes of each region for Standby RAM 0x0: Region7-0 are all Secure. 0x1: Region7 is Non-secure. Region6-0 are Secure 0x2: Region7-6 are Non-secure. Region5-0 are Secure. 0x3: Region7-5 are Non-secure. Region4-0 are Secure. 0x4: Region7-4 are Non-secure. Region 3-0 are Secure. 0x5: Region7-3 are Non-secure. Region 2-0 are Secure. 0x6: Region7-2 are Non-secure. Region 1-0 are Secure. 0x7: Region7-1 are Non-Secure. Region0 is Secure. Others: Region7-0 are all Non-Secure.	R/W
31:4	—	This bit is read as 1.	R

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

42. Standby SRAM

42.1 Overview

提供片上SRAM以在深度软件待机模式下保留数据。表42.1列出了待机SRAM规格。

Table 42.1 备用SRAM规格

Item	Description
SRAM capacity	1 KB
SRAM address	0x2800_0000 to 0x2800_03FF
Access	备用SRAM时钟与PCLKB时钟相同。请参见第42.3.5节。访问周期了解详情。
数据保留功能	数据可以在深度待机模式下保留。请参阅第42.3.1节。有关详细信息的数据保留。
parity	偶校验（数据：8位，奇偶校验：1位）
Module-stop function	可设置模块停止状态以降低功耗。请参阅第42.3.2节。设置为 模块停止功能了解详情。
Security	允许在TrustZone过滤器功能之后对备用RAM进行读取和写入操作。请参见第42.3.4节。TrustZone过滤器功能了解详情。

42.2 注册说明

42.2.1 STBRAMSAR:备用RAM内存安全属性寄存器

Base address: CPSCU = 0x4000_8000

Offset address: 0x014

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	NSBSTBR[3:0]			
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0

Bit	Symbol	Function	R/W
3:0	NSBSTBR[3:0]	StandbyRAM各区域的安全属性 0x0：Region7-0都是安全的。0x1：Region7不安全。Region6-0是安全的0x2：Region7-6是非安全的。Region5-0是安全的。0x3：Region7-5不安全。Region4-0是安全的。0x4：Region7-4不安全。区域3-0是安全的。0x5：Region7-3不安全。区域2-0是安全的。0x6：Region7-2不安全。区域1-0是安全的。0x7：Region7-1是非安全的。Region0是安全的。 其他：Region7-0都是非安全的。	R/W
31:4	—	该位读为1。	R

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

NSBSTBR[3:0] bit (Security attributes of each region for Standby RAM)

Standby RAM is divided into 8 regions. Each region can be set as Secure or Non-secure state with NSBSTBR[3:0]

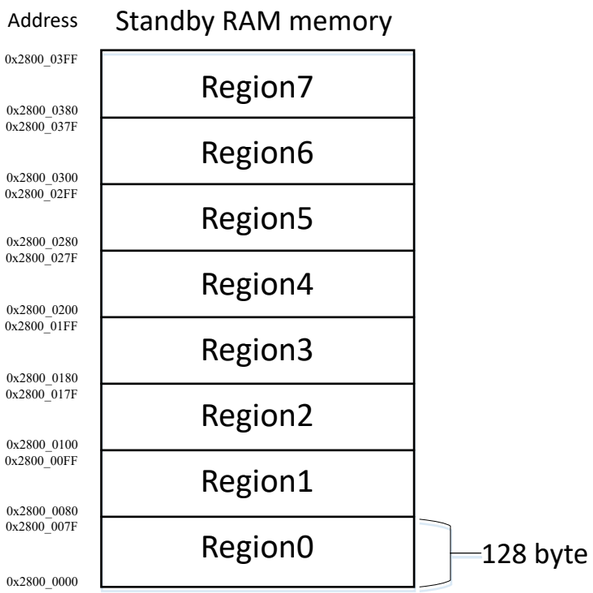


Figure 42.1 Standby RAM regions

42.3 Operation

42.3.1 Data Retention

The power supply to the Standby SRAM in Deep Software Standby mode is enabled by the DPSBYCR.DEEPCUT[1:0] bits. If the DPSBYCR.DEEPCUT[1:0] bits are set to 00b, data in the Standby SRAM is retained in Deep Software Standby mode. See section 10, Low Power Modes, for details on the DPSBYCR.DEEPCUT[1:0] bits.

42.3.2 Setting for the Module-stop Function

Power consumption can be reduced by setting module stop control register A (MSTPCRA) to stop supply of the clock signal to SRAM.

If the Standby SRAM bit in MSTPCRA is set to 1, supply of the clock signal to the Standby SRAM is stopped.

The Standby SRAM is thus placed in the module-stop state by stopping supply of the clock signals. The Standby SRAM operates after a reset.

The Standby SRAM is not accessible if it is in the module-stop state. A transition to the module-stop state should not be made while access to the standby SRAM is in progress.

For details on the MSTPCRA register, see section 10, Low Power Modes.

NSBSTBR[3:0]位（StandbyRAM每个区域的安全属性）

备用RAM分为8个区域。每个区域都可以通过NSBSTBR[3:0]设置为安全或非安全状态

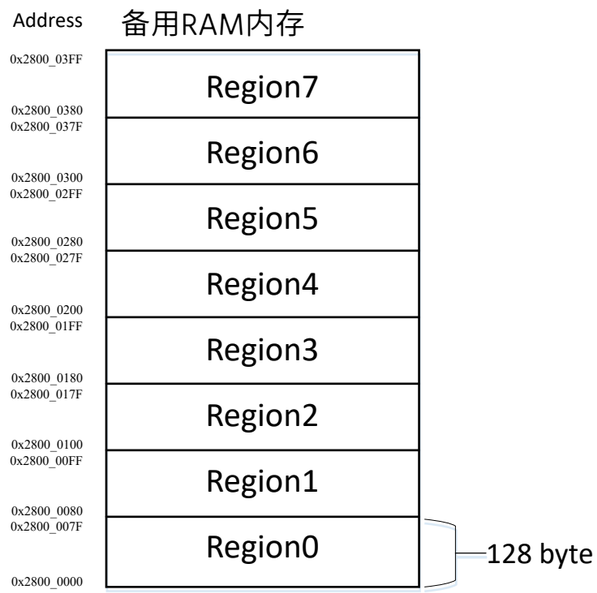


Figure 42.1 备用RAM区域

42.3 Operation

42.3.1 数据保留

深度软件待机模式下的待机SRAM电源由DPSBYCR.DEEPCUT[1:0]位启用。如果DPSBYCR.DEEPCUT[1:0]位设置为00b，则待机SRAM中的数据将保留在深度软件待机模式中。有关DPSBYCR.DEEPCUT[1:0]位的详细信息，请参见第10节，低功耗模式。

42.3.2 模块停止功能的设置

通过设置模块停止控制寄存器A(MSTPCRA)停止向SRAM提供时钟信号，可以降低功耗。

如果MSPCRA中的StandbySRAM位设置为1，则停止向StandbySRAM提供时钟信号。
因此，通过停止提供时钟信号，备用SRAM进入模块停止状态。待机SRAM在复位后运行。

如果处于模块停止状态，则无法访问备用SRAM。在访问备用SRAM的过程中，不应转换到模块停止状态。

有关MSTPCRA寄存器的详细信息，请参见第10节，低功耗模式。

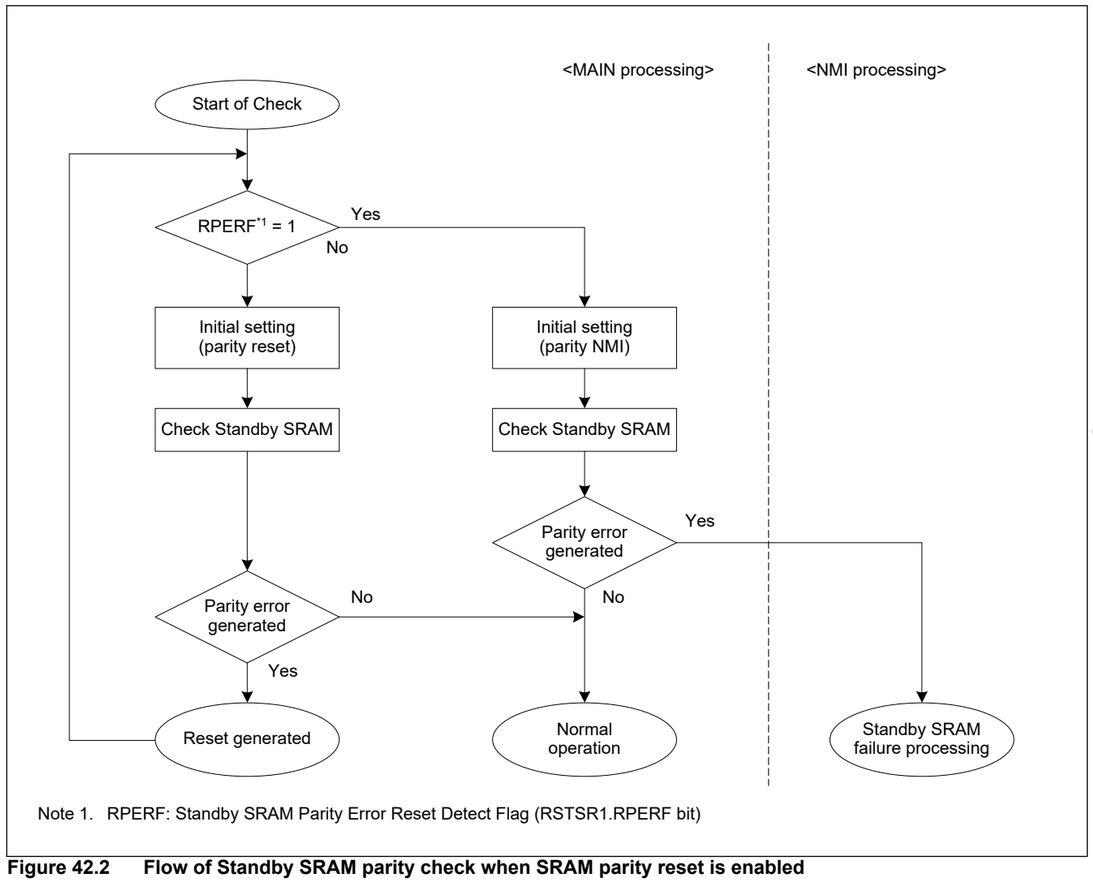
42.3.3 Parity Calculation Function

The IEC60730 standard requires the checking of SRAM data. When data is written, a parity bit is added to every 8-bit data in the Standby SRAM which has 32-bit data width, and when data is read, the parity is checked. When a parity error occurs, a parity error notification is generated. This function can also be used to trigger a reset.

The parity-error notification can be specified as a non-maskable interrupt or a reset in the OAD bit of the SRAM.PARIOAD register. When the OAD bit is set to 1, a parity error is output to the reset function. When the OAD bit is set to 0, a parity error is output to the ICU as a non-maskable interrupt.

Parity errors often occur because of noise. To confirm whether the cause of the parity error is noise or corruption, follow the parity check flows shown in Figure 42.2 and Figure 42.3.

When a read access is executed in a row after a write access, read access is executed with priority. Therefore, during initialization, do not perform the read access in a row after the write access.



Note 1. RPERF: Standby SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF bit)

Figure 42.2 Flow of Standby SRAM parity check when SRAM parity reset is enabled

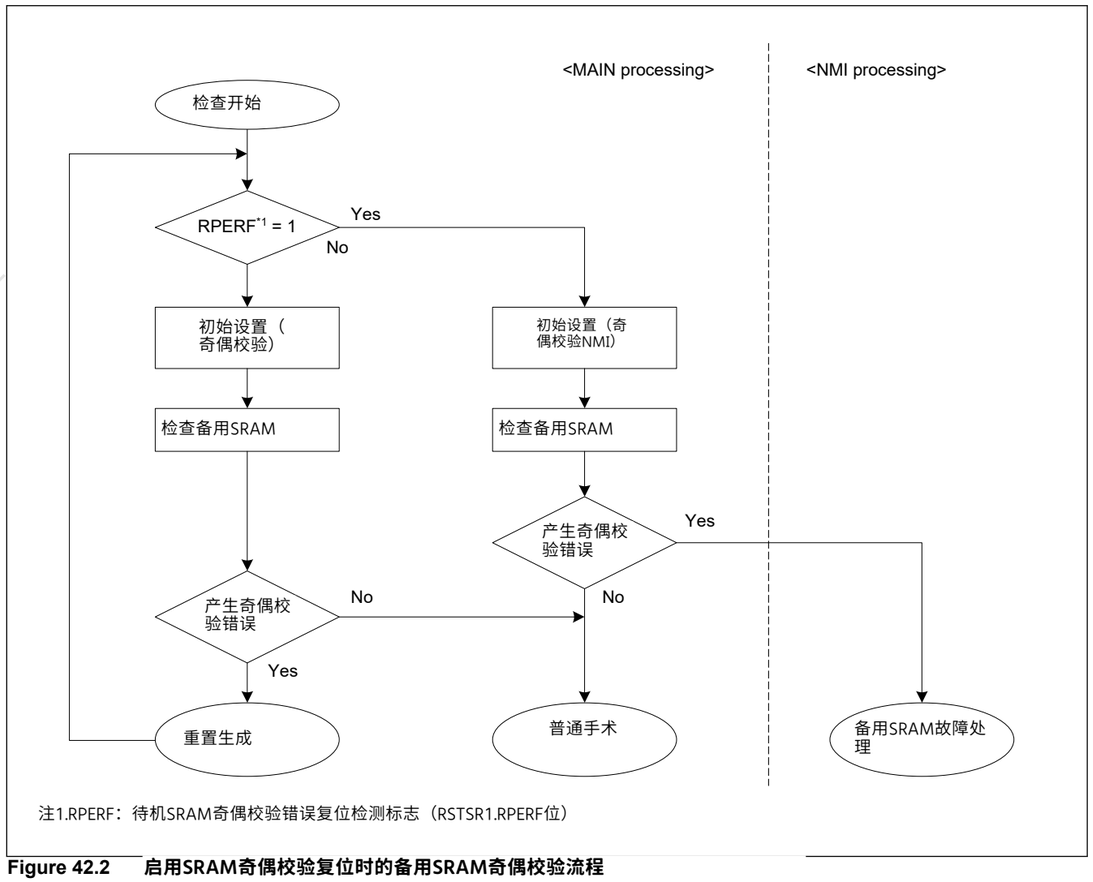
42.3.3 奇偶校验计算功能

IEC60730标准要求检查SRAM数据。写入数据时，在32位数据宽度的StandbySRAM中每8位数据添加一个奇偶校验位，读取数据时检查奇偶校验位。当发生奇偶校验错误时，会生成奇偶校验错误通知。此功能也可用于触发复位。

奇偶校验错误通知可以指定为不可屏蔽中断或SRAM.PARIOAD寄存器的OAD位中的复位。当OAD位设置为1时，奇偶校验错误输出到复位功能。当OAD位设置为0时，奇偶校验错误作为不可屏蔽中断输出到ICU。

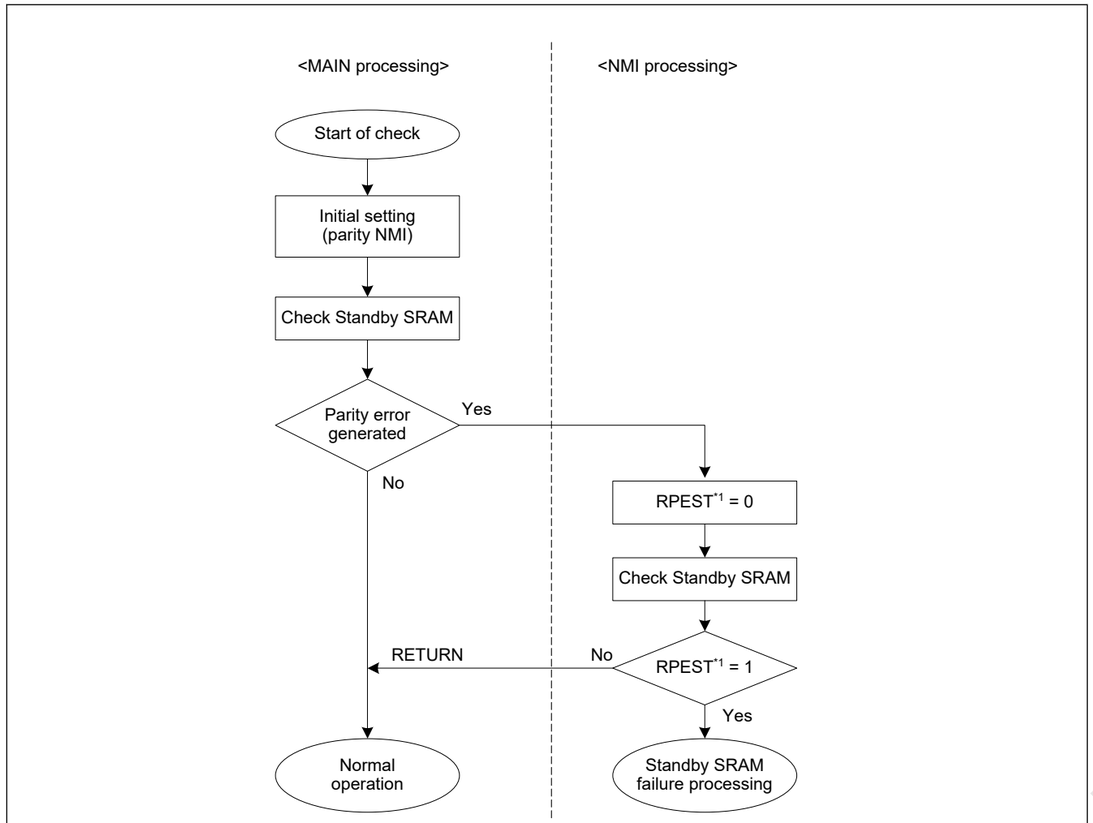
奇偶校验错误经常因噪声而发生。要确认奇偶校验错误的原因是噪声还是损坏，请遵循图42.2和图42.3所示的奇偶校验流程。

在写访问之后连续执行读访问时，优先执行读访问。因此，在初始化过程中，不要在写访问之后连续执行读访问。



注1.RPERF：待机SRAM奇偶校验错误复位检测标志（RSTSR1.RPERF位）

Figure 42.2 启用SRAM奇偶校验复位时的备用SRAM奇偶校验流程



Note 1. RPEST: SRAM Parity Error Interrupt Status Flag (NMISR.RPEST bit)

Figure 42.3 Flow of Standby SRAM parity check when SRAM parity interrupt is enabled

42.3.4 TrustZone Filter function

There is only one type of TrustZone Filter function for Standby SRAM and that is, TrustZone Filter for SRAM memory protection

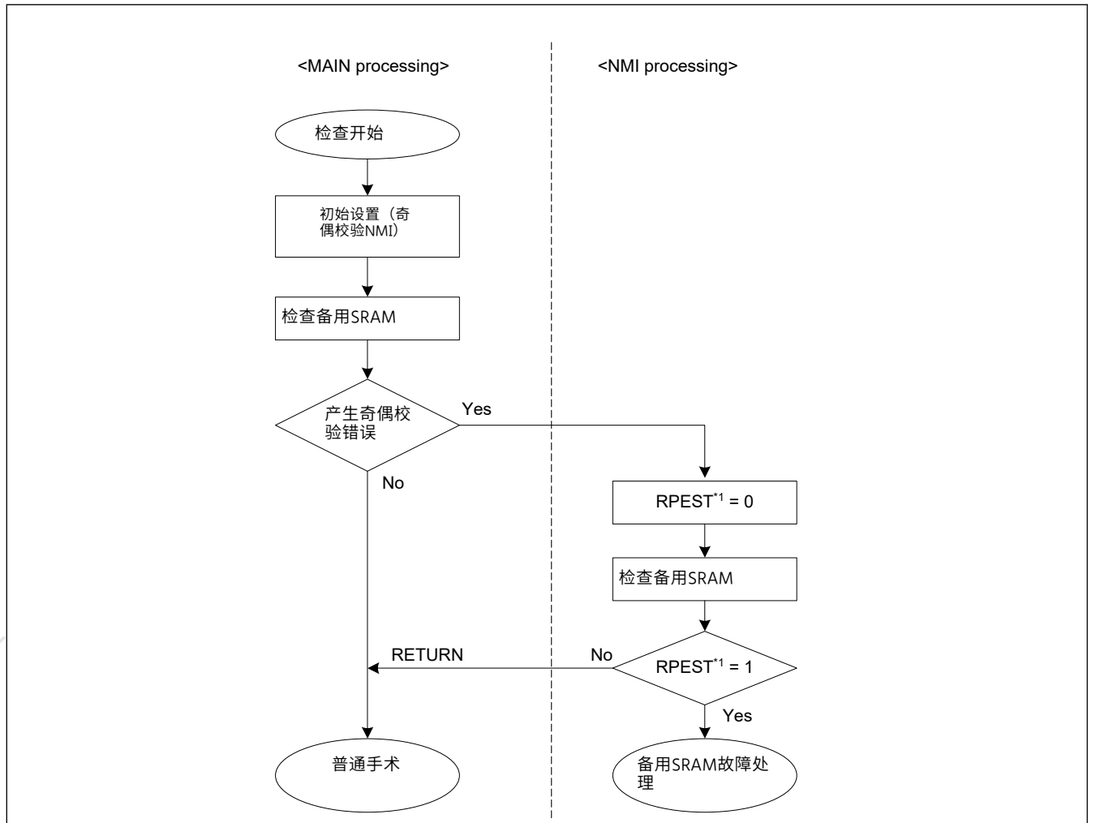
42.3.4.1 TrustZone Filter for Standby SRAM Memory Protection

Standby SRAM memory can be divided into 8 regions, 128 bytes each with a Security Attribution (SA) to be protected from Non-secure access. When SA indicates that the region in Standby SRAM is secure status, non-secure access can not overwrite them because TrustZone Filter detects finds an error and protects the write access.

Table 42.2 Security Attribution and Access status

SA	Access status	Write access	Read access
Secure	Secure	Permit	Permit
	Non-secure	TrustZone Filter error - Protected	TrustZone Filter error - Read data is 0
Non-secure	Secure	Permit	Permit
	Non-secure	Permit	Permit

When TrustZone Filter error for Standby SRAM access occurs, no error notification and no error response occurs.



注1.RPEST：SRAM奇偶校验错误中断状态标志（NMISR.RPEST位）

Figure 42.3 启用SRAM奇偶校验中断时的待机SRAM奇偶校验流程

42.3.4 TrustZone过滤器功能

StandbySRAM只有一种TrustZoneFilter功能，即用于SRAM内存保护的TrustZoneFilter

42.3.4.1 用于备用SRAM内存保护的TrustZone过滤器

备用SRAM存储器可分为8个区域，每个128字节具有安全属性(SA)
非安全访问。当SA指示StandbySRAM中的区域为安全状态时，非安全访问无法覆盖它们，因为TrustZone Filter检测发现错误并保护写访问。

Table 42.2 安全属性和访问状态

SA	访问状态	写访问	读取权限
Secure	Secure	Permit	Permit
	Non-secure	TrustZone过滤器错误受保护	TrustZone过滤器错误读取数据为0
Non-secure	Secure	Permit	Permit
	Non-secure	Permit	Permit

当StandbySRAM访问的TrustZoneFilter错误发生时，不会发生错误通知和错误响应。

42.3.5 Access Cycle

Number of cycles from the CPU.

For Standby SRAM, cache always has non-cacheable access.

Table 42.3 Standby SRAM (Parity Area 0x2800_0000 to 0x2800_03FF)

	Read cycle		Write cycle	
	Word access	Half-word/Byte access	Word access	Half-word/Byte access
ICLK ≥ PCLKB	Min.: 2 ICLK + 2 PCLKB Max.: (n + 1) ICLK + 2 PCLKB		Min.: 1 ICLK + 1 PCLKB Max.: n ICLK + 1 PCLKB	

Note: When the frequency ratio of ICLK : PCLKB is n : 1

42.4 Usage Notes

42.4.1 Instruction Fetch from the Standby SRAM Area

When using Standby SRAM to operate a program, initialize the Standby SRAM area so that the CPU can correctly prefetch data. A parity error might occur if the CPU prefetches from an area that is not initialized. Initialize the additional 12-byte area from the end address of the program with the 4-byte boundary. Renesas recommends using the NOP instruction for data initialization.

42.3.5 访问周期

CPU的周期数。

对于备用SRAM，缓存始终具有不可缓存的访问权限。

Table 42.3 备用SRAM（奇偶校验区0x2800_0000至0x2800_03FF）

	读周期		写周期	
	字访问	Half-word/Byte access	字访问	Half-word/Byte access
ICLK ≥ PCLKB	Min.: 2 ICLK + 2 PCLKB Max.: (n + 1) ICLK + 2 PCLKB		Min.: 1 ICLK + 1 PCLKB Max.: n ICLK + 1 PCLKB	

Note: 当ICLK:PCLKB的频率比为n:1时

42.4 使用说明

42.4.1 从备用SRAM区域取指令

使用StandbySRAM操作程序时，初始化StandbySRAM区域，以便CPU可以正确预取数据。如果CPU从未初始化的区域预取，则可能发生奇偶校验错误。用4字节边界从程序的结束地址初始化额外的12字节区域。瑞萨推荐使用NOP指令进行数据初始化。

43. Flash Memory

This MCU incorporates code flash memory, data flash memory, and option-setting memory. The code flash memory stores instructions and operands, and the data flash memory stores data. For option-setting memory, see section 6, Option-Setting Memory.

43.1 Overview

Table 43.1 lists the specifications of the flash memory, and Figure 43.1 is block diagrams of the flash memory related modules.

The I/O pins used in boot mode, see Table 43.27.

The FCU (flash control unit) controls programming and erasure of the flash memory. The FACI (flash application command interface) controls the FCU according to the specified FACI commands.

Regarding the configuration of the code flash memory, see Figure 43.2, and for the configuration of the data flash memory, see Figure 43.3.

Table 43.1 Specifications of flash memory (1 of 2)

Item	Code flash memory	Data flash memory
Memory capacity	User area: 512 Kbytes max	Data area: 16 Kbytes
Read cycle	See section 43.16.3. Access Cycle	See section 43.16.3. Access Cycle
Value after erasure	0xFF	Undefined
Programming/erasing method	• Programming and erasing the code flash memory and data flash memory, and programming the option-setting memory are handled by the FACI commands specified in the FACI command issuing area (0x407E_0000) (self-programming). • Programming/erasure through transfer by a serial-programmer via a serial interface (serial programming)	
Protection	Protects against erroneous rewriting of the flash memory	
Background operations (BGOs)	• The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.	
Units of programming and erasure	• Units of programming for the user area: 128 bytes • Units of erasure for the user area: Block units	• Unit of programming for the data area:4/8/16 bytes • Unit of erasure for the data area:64/128/256 bytes
Other functions	Interrupts can be accepted during self-programming. In the initial settings of this MCU, an expansion area of the option-setting memory can be set.	
On-board programming (three types)	Programming/erasure in boot mode (for the SCI interface) • The asynchronous serial interface (SCI9) is used. • The transfer rate is adjusted automatically. Programming/erasure in On-chip debug mode • JTAG or SWD interface is used Programming and erasure by self-programming • This allows code flash memory programming/erasure without resetting the system.	
Unique ID	A 16-byte ID code provided for each MCU	
FACI command	Program : 128 bytes Block erase: 1 block (8 KB or 32 KB) P/E suspend P/E resume Forced Stop Status Clear Configuration set (16 bytes)	Program: 4/8/16 bytes Block Erase: 1 block (64 bytes) Multi Block Erase: 64/128/256 bytes P/E suspend P/E resume Forced Stop Blank Check: 4 bytes to data flash memory capacity Status Clear

43. 闪存

该MCU包含代码闪存、数据闪存和选项设置存储器。代码闪存存储指令和操作数，数据闪存存储数据。有关选项设置内存，请参阅第6节，选项设置内存。

43.1 Overview

表43.1列出了闪存的规格，图43.1是闪存相关模块的框图。

引导模式下使用的IO引脚，请参见表43.27。

FCU（闪存控制单元）控制闪存的编程和擦除。FACI（闪存应用命令接口）根据指定的FACI命令控制FCU。

代码闪存的配置见图43.2，数据闪存的配置见图43.3。

Table 43.1 闪存规格(1of2)

Item	代码闪存	数据闪存
内存容量	用户区：最大512KB	Data area: 16 Kbytes
读周期	请参阅第43.16.3节。访问周期	请参阅第43.16.3节。访问周期
擦除后的值	0xFF	Undefined
Programming/erasing method	• 编程和擦除代码闪存和数据闪存以及编程选项设置存储器由FACI命令发出区域(0x407E_0000)中指定的FACI命令处理（自编程）。 • 通过串行编程器通过串行接口传输的编程擦除（串行编程）	
Protection	防止闪存的错误重写	
后台操作(BGO)	• 在对代码闪存进行编程或擦除时，可以读取数据闪存。 • 在对数据闪存进行编程或擦除时，可以读取代码闪存。	
编程和擦除单元	• 用户区编程单位：128字节 • 用户区擦除单位：块单位	• 数据区编程单位：4816字节 • 数据区擦除单位：64128256字节
其他功能	自编程期间可以接受中断。 在此MCU的初始设置中，可以设置选项设置存储器的扩展区域。	
On-board programming (three types)	引导模式下的编程擦除（用于SCI接口）● 使用异步串行接口(SCI9)。 • 传输速率会自动调整。 片上调试模式下的编程擦除● 使用JTAG或SWD接口 通过自编程进行编程和擦除● 这允许在不重置系统的情况下擦除代码闪存编程。	
唯一身份	为每个MCU提供一个16字节的ID代码	
FACI命令	程序：128字节 块擦除：1个块（8KB或32KB） PE暂停PE恢 复强制停止 状态清除 配置集（16字节）	Program: 4/8/16 bytes Block Erase: 1 block (64 bytes) 多块擦除：64128256字节 PE暂停PE恢 复强制停止 空白检查：4字节到数据闪存容量状态清除

Table 43.1 Specifications of flash memory (2 of 2)

Item	Code flash memory	Data flash memory
Security function	Protects against illicit tampering with or reading out of data in flash memory Startup area select setting protection ● BTFLG and FSUACR registers are protected by the FSPR bit. Permanent block protect setting protection ● Code flash memory is permanently protected from programming/erasure operation by the permanent block protect function. Flash memory protection for TrustZone ● Protection for flash memory area (P/E) ● Protection for flash memory area (read) ● Protection for register ● Protection during FACI command operation. ● Code flash P/E mode entry protection	
Safety function	Software protection ● FACI command protection by FENTRYR register. ● Flash memory is protected by FWEPROR register ● The user area is protected by the block protect setting Error protection ● Error is detected when unintended commands or prohibited settings occur. The FACI command is not accepted after an error detection. Boot area protection ● The start-up area select function allows customer to safely update the boot firmware. The size of the start-up area is 8 KB.	
Interrupt request	● FRDYI (flash sequencer ready (processing end)) : Enabled by FRDYIE bit. ● FIFERR (flash sequencer error) : Enabled by CFAEIE/CMDLKIE/DFAEIE bits	
Address conversion	● Start-up area select function is supported	

Figure 43.1 shows how modules related to flash memory can be configured. The flash sequencer is configured with the FCU and FACI. The FCU executes basic control for rewriting of the flash memory. The FACI receives FACI commands using peripheral bus, and controls FCU operations accordingly.

In response to a reset, the FACI transfers data from the flash memory to the option byte storage registers.

Table 43.1 闪存规格(2of2)

Item	代码闪存	数据闪存
安全功能	防止非法篡改或读取闪存中的数据 启动区选择设置保护● BTFLG和FSUACR寄存器受FSPR位保护。 永久块保护设置保护● 永久块保护功能永久保护代码闪存免受编程擦除操作的影响。TrustZone的闪存保护● 闪存区保护(PE) ● 保护闪存区域（读取） ● 注册保护 ● FACI命令操作期间的保护。 ● CodeflashPE模式进入保护	
安全功能	软件保护● FACI命令由FENTRYR寄存器保护。 ● 闪存受FWEPROR寄存器保护 ● 用户区受块保护 设置保护 错误保护● 发生意外命令或禁止设置时会检测到错误。错误检测后不接受FACI命令。引导区保护● 启动区域选择功能允许客户安全地更新启动固件。启动区的大小为8KB。	
中断请求	● FRDYI（闪存序列器就绪（处理结束））： 由FRDYIE位启用。 ● FIFERR (flash sequencer error) : 由CFAEIECMDLKIEDFAEIE位启用	
地址转换	● 支持启动区域选择功能	

图43.1显示了如何配置与闪存相关的模块。闪存定序器配置有FCU和FACI。FCU执行闪存重写的基本控制。FACI使用外围总线接收FACI命令，并相应地控制FCU操作。

响应复位，FACI将数据从闪存传输到选项字节存储寄存器。

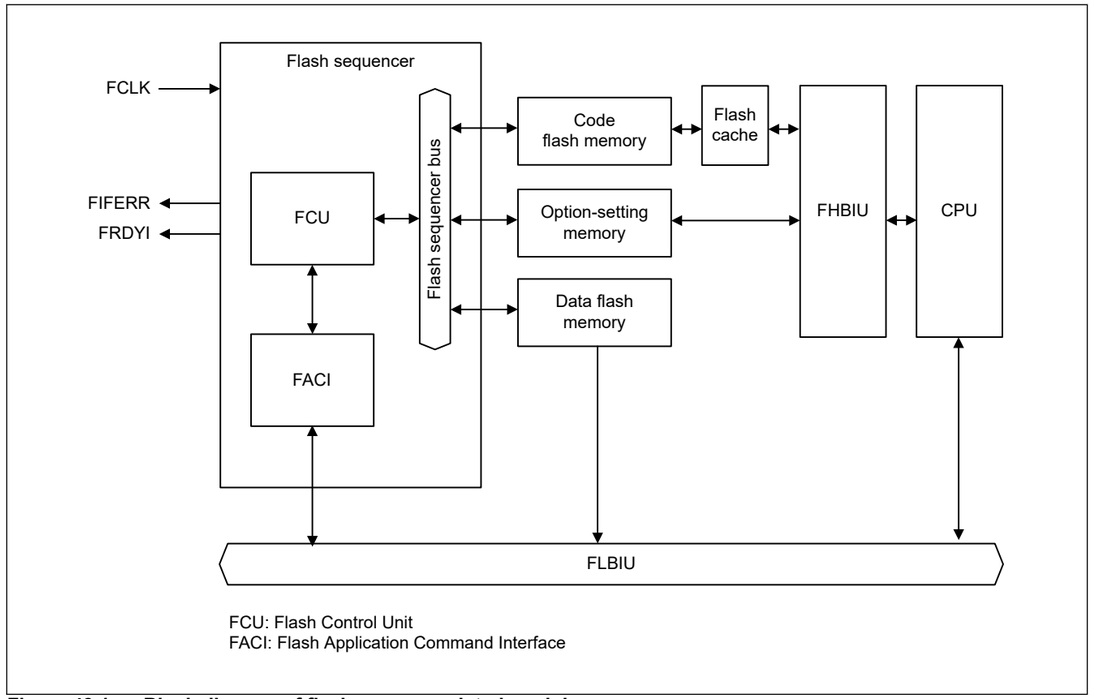


Figure 43.1 Block diagram of flash memory-related modules

43.2 Structure of Memory

Figure 43.2 shows the memory map of code flash memory.

The user area of the code flash memory in this MCU is divided into 8- and 32-Kbyte blocks, which serve as the units of erasure.

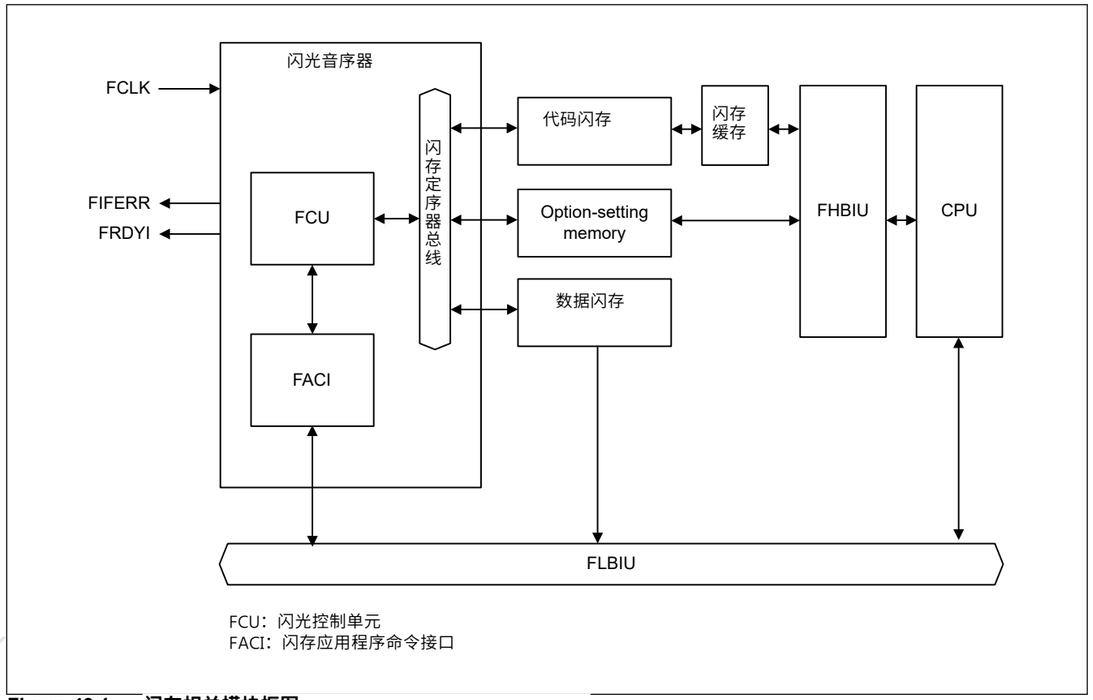


Figure 43.1 闪存相关模块框图

43.2 内存结构

图43.2显示了代码闪存的内存映射。

本MCU中代码闪存的用户区分为8和32KB块，作为擦除单位。

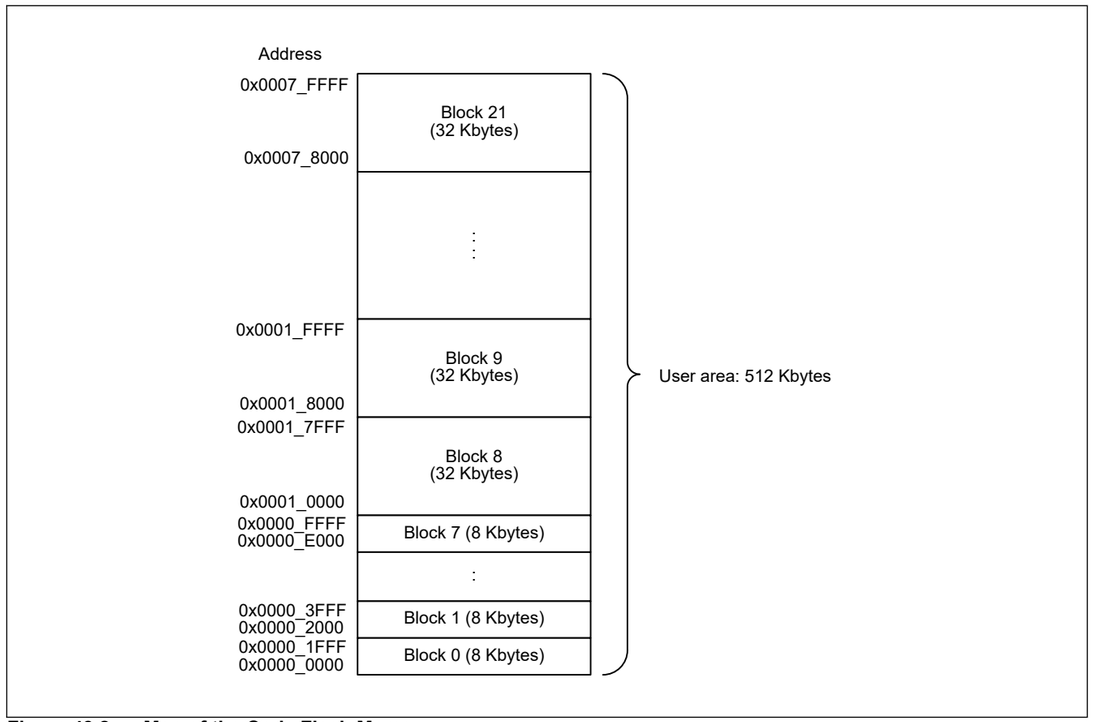


Figure 43.2 Map of the Code Flash Memory

Table 43.2 Read and programming/erasure address by product for the code flash memory

Product	Address	Number of blocks
512 Kbytes product	0x0000_0000 to 0x0007_FFFF	0 to 21
256 Kbytes product	0x0000_0000 to 0x0003_FFFF	0 to 13

The data area of the data flash memory in this MCU is divided into 64-byte blocks, with each being a unit for erasure. Figure 43.3 shows the mapping of the data flash memory.

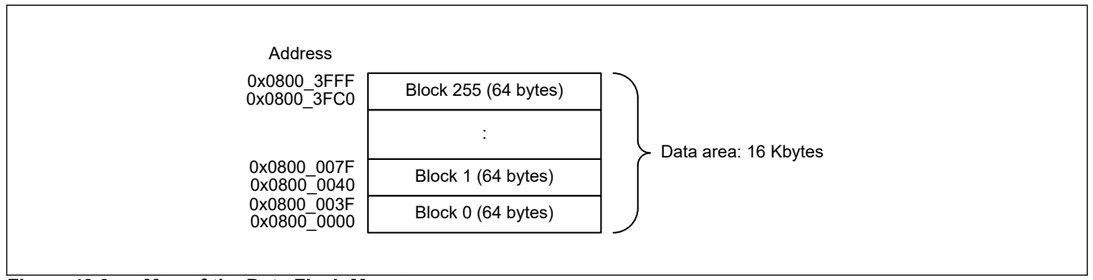


Figure 43.3 Map of the Data Flash Memory

43.3 Address Space

Using the hardware interface with flash memory requires access to all registers of the hardware, which is for issuing FACI commands. Table 43.3 provides information about the hardware interface.

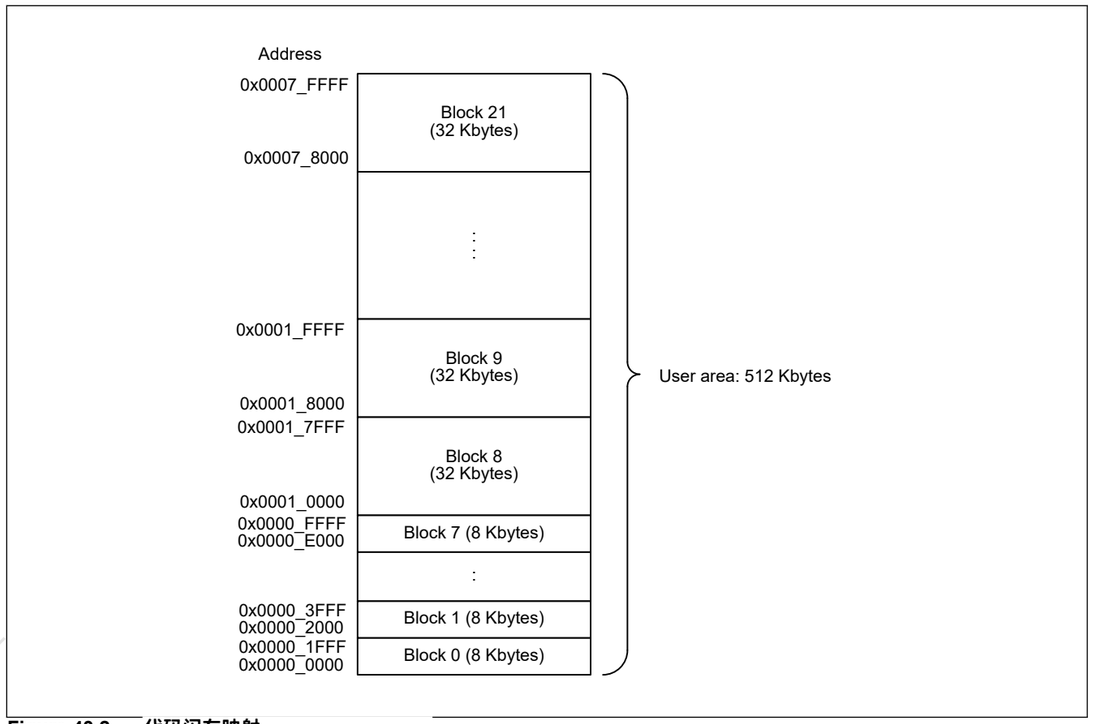


Figure 43.2 代码闪存映射

Table 43.2 按产品读取和编程代码闪存的擦除地址

Product	Address	块数
512 Kbytes product	0x0000_0000 to 0x0007_FFFF	0 to 21
256 Kbytes product	0x0000_0000 to 0x0003_FFFF	0 to 13

本单片机中数据闪存的数据区被划分为64字节块，每个块为一个擦除单元。
图43.3显示了数据闪存的映射。

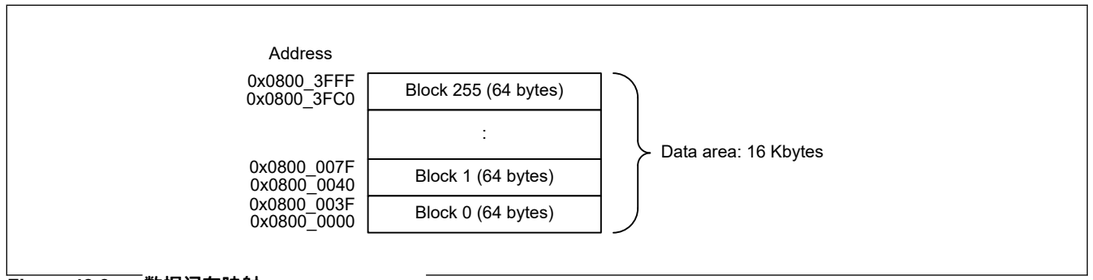


Figure 43.3 数据闪存映射

43.3 地址空间

使用带有闪存的硬件接口需要访问硬件的所有寄存器，用于发出FACI命令。表43.3提供了有关硬件接口的信息。

Table 43.3 Information on the hardware interface area

Area	Address	Capacity
Area containing various registers of the hardware	See section 43.4. Register Descriptions.	See section 43.4. Register Descriptions.
FACI command-issuing area	0x407E_0000	4 bytes

For the address information of the flash memory, see Figure 43.2.

43.4 Register Descriptions

43.4.1 FCACHEE : Flash Cache Enable Register

Base address: FCACHE = 0x4001_C100

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FCACHEEN	Flash Cache Enable 0: FCACHE is disabled 1: FCACHE is enabled	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

This register is not controlled by any security attribute register.

FCACHEEN bit (Flash Cache Enable)

FCACHEE.FCACHEEN bit enable and disables the function of Flash Cache of FCACHE1, FCACHE2 and FLPF.

FCACHEE.FCACHEEN bit dose not influence for FCACHEIV.FCACHEIV.

When FCACHE is enabled, it works for accesses marked as cacheable.

It is prohibited to disable FCACHE after enabling.

43.4.2 FCACHEIV : Flash Cache Invalidate Register

Base address: FCACHE = 0x4001_C100

Offset address: 0x004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEIV
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FCACHEIV	Flash Cache Invalidate 0: Read: Do not invalidate. Write: The setting is ignored. 1: Invalidate FCACHE is invalidated.	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

This register is not controlled by any security attribute register.

Table 43.3 硬件接口区信息

Area	Address	Capacity
包含各种硬件寄存器的区域	见第43.4节。注册说明。	见第43.4节。注册说明。
FACI指挥区	0x407E_0000	4 bytes

Flash存储器的地址信息见图43.2。

43.4 注册说明

43.4.1 FCACHEE:闪存缓存启用寄存器

Base address: FCACHE = 0x4001_C100

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FCACHEEN	闪存缓存启用 0：禁用FCACHE1：启用FCACHE	R/W
15:1	—	这些位被读取为0。写入值应为0。	R/W

该寄存器不受任何安全属性寄存器的控制。

FCACHEEN位（闪存使能）

FCACHEE.FCACHEEN位启用和禁用FCACHE1、FCACHE2和FLPF的FlashCache功能。

FCACHEE.FCACHEEN位对FCACHEIV.FCACHEIV没有影响。

启用FCACHE后，它适用于标记为可缓存的访问。

禁止启用后禁用FCACHE。

43.4.2 FCACHEIV:闪存缓存无效寄存器

Base address: FCACHE = 0x4001_C100

Offset address: 0x004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEIV
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FCACHEIV	闪存缓存失效 0：读取：不无效。 写入：忽略该设置。 1: Invalidate FCACHE无效。	R/W
15:1	—	这些位被读取为0。写入值应为0。	R/W

该寄存器不受任何安全属性寄存器的控制。

FCACHEIV bit (Flash Cache Invalidate)

When 1 is written to FCACHEIV.FCACHEIV bit, the Flash cache data of FCACHE1, FCACHE2 and FLPF is invalidated.

Invalidate FCACHE with keeping FCACHE enabled after programming or erasing the code flash or the option setting memory.

43.4.3 FLWT : Flash Wait Cycle Register

Base address: FCACHE = 0x4001_C100

Offset address: 0x01C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	FLWT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	FLWT[2:0]	Flash Wait Cycle 0 0 0: 0 wait (ICLK ≤ 120 MHz) 0 0 1: 1 wait (ICLK > 120 MHz) Others: Setting prohibited	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

FLWT[2:0] bits (Flash Wait Cycle)

The Flash Wait Cycle Register (FLWT) sets the access wait count for the flash memory.

For faster clock frequencies, set FLWT.FLWT before changing the clock frequency. For slower clock frequencies, set FLWT.FLWT after changing the clock frequency.

For information on the frequency setting, see section 8, Clock Generation Circuit.

43.4.4 FSAR : Flash Security Attribution Register

Base address: FCACHE = 0x4001_C100

Offset address: 0x040

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FCKMHZSA	—	—	—	—	—	—	—	FLWTSA
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	FLWTSA	FLWT Security Attribution Target register : FLWT 0: Secure 1: Non-Secure	R/W
7:1	—	These bits are read as 1. The write value should be 1.	R/W
8	FCKMHZSA	FCKMHZ Security Attribution Target register : FCKMHZ 0: Secure 1: Non-Secure	R/W
15:9	—	These bits are read as 1. The write value should be 1.	R/W

FCACHEIV位（FlashCache无效）

当FCACHEIV.FCACHEIV位写入1时，FCACHE1、FCACHE2和FLPF的Flash缓存数据无效。

在编程或擦除代码闪存或选项设置存储器后保持FCACHE使能，使FCACHE无效。

43.4.3 FLWT：闪存等待周期寄存器

Base address: FCACHE = 0x4001_C100

Offset address: 0x01C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	FLWT[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	FLWT[2:0]	闪存等待周期 0 0 0: 0 wait (ICLK ≤ 120 MHz) 0 0 1: 1 wait (ICLK > 120 MHz) 其他：禁止设置	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

FLWT[2:0]位（闪存等待周期）

闪存等待周期寄存器(FLWT)设置闪存的访问等待计数。

要获得更快的时钟频率，请在更改时钟频率之前设置FLWT.FLWT。对于较慢的时钟频率，设置改变时钟频率后的FLWT.FLWT。

有关频率设置的信息，请参见第8节，时钟生成电路。

43.4.4 FSAR:Flash安全属性寄存器

Base address: FCACHE = 0x4001_C100

Offset address: 0x040

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FCKMHZSA	—	—	—	—	—	—	—	FLWTSA
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	FLWTSA	FLWT安全归因 目标寄存器：FLWT 0: Secure 1: Non-Secure	R/W
7:1	—	这些位被读取为1。写入值应为1。	R/W
8	FCKMHZSA	FCKMHZ安全归属地 目标寄存器：FCKMHZ 0: Secure 1: Non-Secure	R/W
15:9	—	这些位被读取为1。写入值应为1。	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

Write access is invalid when PRCR.PRC4 bit is 0. See section 11, Register Write Protection.

FLWTSA bit (FLWT Security Attribution)

This bit sets the security attribute of FLWT.

FCKMHZSA bit (FCKMHZ Security Attribution)

This bit sets the security attribute of FCKMHZ.

43.4.5 UIDRn : Unique ID Registers n (n = 0 to 3)

Address: 0x0100_8190 + n × 4

Bit position:	31	0
Bit field:	UID	
Value after reset:	Unique value for each chip	

Bit	Symbol	Function	R/W
31:0	UID	Unique ID	R

The UIDRn is a read-only register that stores a 16-byte ID code (unique ID) for identifying the individual MCU. The UIDRn register should be read in 32-bit units. When reading by the signature request command of the serial programming interface, the data is read in order from the data with the large address. That is, the data in 0x0100_819F is read first, and in 0x0100_8190 is read last.

43.4.6 PNRn : Part Numbering Register n (n = 0 to 3)

Address: 0x0100_80F0 + n × 4

Bit position:	31	0
Bit field:	PNR	
Value after reset:	Unique value for each chip	

Bit	Symbol	Function	R/W
31:0	PNR	Part Number	R

The PNRn is a read-only register that stores a 16-byte part numbering. The PNRn register should be read in 32-bit units. Each byte corresponds to the ASCII code representation of the product part number as detailed in Table 1.13 Product list. The first character ("R", 0x52 in ASCII code) of the part number is stored in the byte with the smallest address (0x0100_80F0). When reading by the signature request command of the serial programming interface, the data is read in order from the data with the small address. That is, the data in 0x0100_80F0 is read first, and in 0x0100_80FF is read last.

43.4.7 MCUVER : MCU Version Register

Address: 0x0100_81B0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MCUVE							
Value after reset:	Value depend on the chip							

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

当PRCR.PRC4位为0时，写访问无效。参见第11节，寄存器写保护。

FLWTSA位（FLWT安全属性）

该位设置FLWT的安全属性。

FCKMHZSA位（FCKMHZ安全属性）

该位设置FCKMHZ的安全属性。

43.4.5 UIDRn：唯一ID寄存器n（n=0到3）

Address: 0x0100_8190 + n × 4

Bit position:	31	0
Bit field:	UID	
重置后的值：	每个芯片的独特价值	

Bit	Symbol	Function	R/W
31:0	UID	唯一身份	R

UIDRn是一个只读寄存器，它存储一个16字节的ID代码（唯一ID），用于识别单个MCU。这
UIDRn寄存器应以32位为单位读取。通过串口编程接口的签名请求命令读取时，从地址大的数据开始依次读取。
即先读取0x0100_819F中的数据，最后读取0x0100_8190中的数据。

43.4.6 PNRn：零件编号寄存器n（n=0到3）

Address: 0x0100_80F0 + n × 4

Bit position:	31	0
Bit field:	PNR	
重置后的值：	每个芯片的独特价值	

Bit	Symbol	Function	R/W
31:0	PNR	零件号	R

PNRn是一个只读寄存器，存储一个16字节的零件编号。PNRn寄存器应以32位为单位读取。每个字节对应于表1.13产品列表中详细说明的产品部件号的ASCII代码表示。部件号的第一个字符（“R”，ASCII码中的0x52）存储在地址最小的字节中（0x0100_80F0）。通过串行编程接口的签名请求命令读取时，从地址小的数据开始依次读取。即先读取0x0100_80F0中的数据，最后读取0x0100_80FF中的数据。

43.4.7 MCUVER:MCU版本寄存器

Address: 0x0100_81B0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MCUVE							
重置后的值：	价值取决于芯片							

Bit	Symbol	Function	R/W
7:0	MCUVE	MCU Version	R

The MCUVER is a read-only register that stores a MCU version. The MCUVER register should be read in 8-bit units.

43.4.8 FWEPROR : Flash P/E Protect Register

Base address: SYSC = 0x4001_E000

Offset address: 0x416

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	FLWE[1:0]	
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
1:0	FLWE[1:0]	Flash Programming and Erasure 0 0: Prohibits Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing. 0 1: Permits Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing. 1 0: Prohibits Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing. 1 1: Prohibits Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing.	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

It is possible that Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing are prohibited by software.

The FWEPROR register is initialized by a reset from the following:

- All reset source
- Transition to Deep Software Standby mode
- Transition to Software Standby mode.

FLWE[1:0] bits (Flash Programming and Erasure)

The FLWE[1:0] bits are used to set the flash P/E protection. The value after reset is 10b.

If these bits are set to other than 01b that does not allow programming and erasure of the flash memory, the following commands cannot be executed. Issuing any of the following commands leads to setting of the FLWEERR bit in the FSTATR register to 1.

Program / Block Erase / Multi Block Erase / Blank Check / Configuration set command

43.4.9 FASTAT : Flash Access Status Register

Base address: FACI = 0x407F_E000

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CFAE	—	—	CMDLK	DFAE	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
7:0	MCUVE	MCU Version	R

MCUVER是一个只读寄存器，用于存储MCU版本。MCUVER寄存器应以8位为单位读取。

43.4.8 FWEPROR:FlashPE保护寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x416

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	FLWE[1:0]	
重置后的值:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
1:0	FLWE[1:0]	闪存编程和擦除 00：禁止编程、块擦除、多块擦除、空白检查和配置设置命令处理。 01：允许编程、块擦除、多块擦除、空白检查和配置设置命令处理。 10：禁止编程、块擦除、多块擦除、空白检查和配置设置命令处理。 11：禁止Program、BlockErase、MultiBlockErase、BlankCheck和Configurationset命令处理。	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

程序、块擦除、多块擦除、空白检查和配置设置命令处理可能被软件禁止。

FWEPROR寄存器通过以下复位进行初始化：

●所有复位源

●转换到深度软件待机模式

●转换到软件待机模式。

FLWE[1:0]位（闪存编程和擦除）

FLWE[1:0]位用于设置flashPE保护。复位后的值为10b。

如果这些位设置为不允许对闪存进行编程和擦除的01b以外，则无法执行以下命令。发出以下任何命令都会将FSTATR寄存器中的FLWEERR位设置为1。

ProgramBlockEraseMultiBlockEraseBlankCheckConfigurationset命令

43.4.9 FASTAT：闪存访问状态寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CFAE	—	—	CMDLK	DFAE	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
3	DFAE	Data Flash Memory Access Violation Flag 0: No data flash memory access violation has occurred 1: A data flash memory access violation has occurred.	R/W*1
4	CMDLK	Command Lock Flag 0: The flash sequencer is not in the command-locked state 1: The flash sequencer is in the command-locked state.	R
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	CFAE	Code Flash Memory Access Violation Flag 0: No code flash memory access violation has occurred 1: A code flash memory access violation has occurred.	R/W*1

Note 1. Only 0 can be written to clear the flag after 1 is read.

The FASTAT register indicates whether a code flash or data flash memory access violation has occurred. If any of the CFAE, CMDLK, and DFAE bits is set to 1, the flash sequencer enters the command-locked state (see section 43.11.2. Error Protection). To release it from the command-locked state, issue a status clear command or Forced Stop command to the flash sequencer.

DFAE bit (Data Flash Memory Access Violation Flag)

The DFAE bit indicates whether a data flash memory access violation occurred. When this bit is set to 1, the ILGLERR bit in the FSTATR register is set to 1, placing the flash sequencer in the command-locked state.

[Setting conditions]

FACI commands issued in the data flash P/E mode are as follows:

- The setting of the FSADDR or FEADDR register is the reserved portion of the data area
- FACI commands of non-secure access are issued while the setting of the FSADDR or FEADDR register is the secure region address.

[Clearing conditions]

- When this bit is written as 0 after it is set to 1
- When the flash sequencer starts to process the Status Clear or Forced Stop command.

CMDLK bit (Command Lock Flag)

The CMDLK bit indicates that the flash sequencer is in the command-locked state.

[Setting conditions]

- The flash sequencer detects an error and enters the command-locked state.

[Clearing conditions]

- When the flash sequencer starts to process the Status Clear or Forced Stop command.

CFAE bit (Code Flash Memory Access Violation Flag)

The CFAE bit indicates whether a code flash memory access violation has occurred. When this bit is set to 1, the ILGLERR bit in the FSTATR register is set to 1, placing the flash sequencer in the command-locked state.

[Setting conditions]

FACI commands issued in the code flash P/E mode are as follows:

- The setting of the FSADDR register is the reserved portion of the user area
- The Configuration set command is issued while the setting of the FSADDR register is from 0x0000A100 to 0x0000A2F0 in self-programming mode
- FACI commands of non-secure access are issued while the setting of the FSADDR register is the secure region address.

[Clearing conditions]

- When this bit is written as 0 after it is set to 1

Bit	Symbol	Function	R/W
3	DFAE	数据闪存访问违规标志 0：未发生数据闪存访问违规1：发生数据闪存访问违规 。	R/W*1
4	CMDLK	命令锁定标志 0：flash定序器不处于命令锁定状态1：flash定序器处于命令锁定状态。	R
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	CFAE	代码闪存访问违规标志 0：未发生代码闪存访问违规1：发生代码闪存访问违规 。	R/W*1

注1.读取1后，只能写入0以清除标志。

FASTAT寄存器指示是否发生了代码闪存或数据闪存访问违规。如果任何一个CFAE、CMDLK和DFAE位设置为1，闪存定序器进入命令锁定状态（参见第43.11.2节。错误保护）。要将其从命令锁定状态释放，请向闪存定序器发出状态清除命令或强制停止命令。

DFAE位（数据闪存访问违规标志）

DFAE位指示是否发生数据闪存访问违规。当该位设置为1时，FSTATR寄存器中的ILGLERR位设置为1，将闪存定序器置于命令锁定状态。

[Setting conditions]

数据闪存PE模式下发出的FACI命令如下：

●FSADDR或FEADDR寄存器的设置是数据区的保留部分

●FSADDR或FEADDR寄存器的设置是安全区域地址时发出非安全访问的FACI命令。

[Clearing conditions]

●该位设置为1后写入0时

●当flashsequencer开始处理StatusClear或ForcedStop命令时。

CMDLK位（命令锁定标志）

CMDLK位指示闪存定序器处于命令锁定状态。

[Setting conditions]

●闪存定序器检测到错误并进入命令锁定状态。

[Clearing conditions]

●当flashsequencer开始处理StatusClear或ForcedStop命令时。

CFAE位（代码闪存访问违规标志）

CFAE位指示是否发生代码闪存访问违规。当该位设置为1时，FSTATR寄存器中的ILGLERR位设置为1，将闪存定序器置于命令锁定状态。

[Setting conditions]

CodeflashPE模式下发出的FACI命令如下：

●FSADDR寄存器的设置是用户区的保留部分

●自编程模式下FSADDR寄存器的设置从0x0000A100到0x0000A2F0时发出配置设置命令

●FSADDR寄存器的设置是安全区域地址时发出非安全访问的FACI命令。

[Clearing conditions]

●该位设置为1后写入0时

- When the flash sequencer starts to process the Status Clear or Forced Stop command.

43.4.10 FAEINT : Flash Access Error Interrupt Enable Register

Base address: FACI = 0x407F_E000

Offset address: 0x14

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CFAEIE	—	—	CMDLKIE	DFAEIE	—	—	—
Value after reset:	1	0	0	1	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
3	DFAEIE	Data Flash Memory Access Violation Interrupt Enable 0: Generation of an FIFERR interrupt request is disabled when FASTAT.DFAE is set to 1 1: Generation of an FIFERR interrupt request is enabled when FASTAT.DFAE is set to 1.	R/W
4	CMDLKIE	Command Lock Interrupt Enable 0: Generation of an FIFERR interrupt request is disabled when FASTAT.CMDLK is set to 1 1: Generation of an FIFERR interrupt request is enabled when FASTAT.CMDLK is set to 1.	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	CFAEIE	Code Flash Memory Access Violation Interrupt Enable 0: Generation of an FIFERR interrupt request is disabled when FASTAT.CFAE is set to 1 1: Generation of an FIFERR interrupt request is enabled when FASTAT.CFAE is set to 1.	R/W

The FAEINT register enables or disables generation of a flash access error (FIFERR) interrupt request.

DFAEIE bit (Data Flash Memory Access Violation Interrupt Enable)

The DFAEIE bit enables or disables generation of an FIFERR interrupt request when a data flash memory access violation occurs, setting the DFAE bit in the FASTAT register to 1.

CMDLKIE bit (Command Lock Interrupt Enable)

The CMDLKIE bit enables or disables generation of an FIFERR interrupt request when the flash sequencer enters the command-locked state, setting the CMDLK bit in the FASTAT register to 1.

CFAEIE bit (Code Flash Memory Access Violation Interrupt Enable)

The CFAEIE bit enables or disables generation of an FIFERR interrupt request when a code flash memory access violation occur, setting the CFAE bit in the FASTAT register to 1.

43.4.11 FRDYIE : Flash Ready Interrupt Enable Register

Base address: FACI = 0x407F_E000

Offset address: 0x18

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FRDYIE
Value after reset:	0	0	0	0	0	0	0	0

●当flashsequencer开始处理StatusClear或ForcedStop命令时。

43.4.10 FAEINT：闪存访问错误中断使能寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x14

重置后的值：	1	0	0	1	1	0	0	0
Bit field:	CFAEIE	—	—	CMDLKIE	DFAEIE	—	—	—
Bit position:	7	6	5	4	3	2	1	0

Bit	Symbol	Function	R/W
2:0	—	这些位被读取为0。写入值应为0。	R/W
3	DFAEIE	数据闪存访问冲突中断使能 0：当FASTAT.DFAE设置为1时，禁止生成FIFERR中断请求 1：当FASTAT.DFAE设置为1时，使能FIFERR中断请求的生成。	R/W
4	CMDLKIE	命令锁定中断使能 0：当FASTAT.CMDLK设置为1时，禁止生成FIFERR中断请求 1：当FASTAT.CMDLK设置为1时，使能FIFERR中断请求的生成。	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	CFAEIE	代码闪存访问冲突中断启用 0：当FASTAT.CFAE设置为1时，禁止生成FIFERR中断请求 1：当FASTAT.CFAE设置为1时，使能FIFERR中断请求的生成。	R/W

FAEINT寄存器启用或禁用闪存访问错误(FIFERR)中断请求的生成。

DFAEIE位（数据闪存访问冲突中断允许）

当发生数据闪存访问违规时，DFAEIE位启用或禁用FIFERR中断请求的生成，将FASTAT寄存器中的DFAE位设置为1。

CMDLKIE位（命令锁定中断使能）

当闪存定序器进入命令锁定状态时，CMDLKIE位启用或禁用FIFERR中断请求的生成，将FASTAT寄存器中的CMDLK位设置为1。

CFAEIE位（代码闪存访问冲突中断允许）

当发生代码闪存访问违规时，CFAEIE位启用或禁用FIFERR中断请求的生成，将FASTAT寄存器中的CFAE位设置为1。

43.4.11 FRDYIE:闪存就绪中断使能寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x18

重置后的值：	0	0	0	0	0	0	0	0
Bit field:	—	—	—	—	—	—	—	FRDYIE
Bit position:	7	6	5	4	3	2	1	0

Bit	Symbol	Function	R/W
0	FRDYIE	Flash Ready Interrupt Enable 0: Generation of an FRDY interrupt request is disabled 1: Generation of an FRDY interrupt request is enabled.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

The FRDYIE register enables or disables generation of a flash ready (FRDY) interrupt.

FRDYIE bit (Flash Ready Interrupt Enable)

The FRDYIE bit enables or disables generation of an FRDY interrupt request when the FRDY bit in the FSTATR register is changed from 0 to 1 on completion of processing by the flash sequencer of the Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command.

43.4.12 FSADDR : FACI Command Start Address Register

Base address: FACI = 0x407F_E000

Offset address: 0x30

Bit position:	31																												0
Bit field:	FSADDR[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	FSADDR[31:0]	Start Address for FACI Command Processing	R/W*1

Note 1. These bits can be written when the FRDY bit in the FSTATR register is 1. Writing to these bits are ignored when the FRDY bit is 0. Note that b0 and b1 are read-only.

Table 43.4 FACI command addres boundary

Command	Address Boundary
Program (code flash memory)	128-byte
Program (data flash memory)	4, 8, 16 -byte
Block Erase (code flash memory)	8-KB or 32-KB
Block Erase (data flash memory)	64-byte
Multi Block Erase (data flash memory)	64-byte
Blank Check (data flash memory)	4-byte
Configuration set	16-byte

The FSADDR register specifies the address where the target area for command processing starts when the FACI command for Program, Block Erase, Multi Block Erase, Blank Check, or Configuration set is issued.

The FSADDR value is initialized when the SUINIT bit in the FSUINITR register is set to 1. It is also initialized by a reset.

FSADDR[31:0] bits (Start Address for FACI Command Processing)

The FSADDR[31:0] bits specify the start address for FACI command processing. Bits [31:24] are ignored in FACI command processing for the code flash memory. Bits [31:17] are ignored in FACI command processing for the data flash memory. Bits associated with the address bits of lower order than the address boundary listed in Table 43.4 are also ignored.

For information on the addresses of the code flash memory and the data flash memory, see section 43.2. Structure of Memory.

For information on the addresses of the configuration setting, see section 43.9.3.15. Configuration Set Command.

Bit	Symbol	Function	R/W
0	FRDYIE	闪存就绪中断使能 0：禁止产生FRDY中断请求1：允许产生FRDY中断请求 。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

FRDYIE寄存器启用或禁用闪存就绪(FRDY)中断的生成。

FRDYIE位（闪存就绪中断使能）

当FSTATR寄存器中的FRDY位在程序、块擦除、多块擦除、空白检查和配置的闪存序列器的处理完成时从0变为1时，FRDYIE位启用或禁用FRDY中断请求的产生设置命令。

43.4.12 FSADDR:FACI命令起始地址寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x30

Bit position:	31																												0
Bit field:	FSADDR[31:0]																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	FSADDR[31:0]	FACI命令处理的起始地址	R/W*1

注1.当FSTATR寄存器中的FRDY位为1时可以写入这些位。当FRDY位为0时忽略写入这些位。
请注意，b0和b1是只读的。

Table 43.4 FACI命令地址边界

Command	地址边界
程序（代码闪存）	128-byte
程序（数据闪存）	4, 8, 16 -byte
块擦除（代码闪存）	8-KB or 32-KB
块擦除（数据闪存）	64-byte
多块擦除（数据闪存）	64-byte
空白检查（数据闪存）	4-byte
配置集	16-byte

FSADDR寄存器指定在发出用于编程、块擦除、多块擦除、空白检查或配置集的FACI命令时命令处理的目标区域开始的地址。

FSADDR值在FSUINITR寄存器中的SUINIT位设置为1时被初始化。它也通过复位被初始化。

FSADDR[31:0]位（FACI命令处理的起始地址）

FSADDR[31:0]位指定FACI命令处理的起始地址。在代码闪存的FACI命令处理中忽略位[31:24]。在数据闪存的FACI命令处理中忽略位[31:17]。与低于表43.4中列出的地址边界的地址位相关的位也被忽略。

有关代码闪存和数据闪存地址的信息，请参见第43.2节。结构
Memory.

有关配置设置地址的信息，请参阅第43.9.3.15节。配置集命令。

43.4.13 FEADDR : FACI Command End Address Register

Base address: FACI = 0x407F_E000

Offset address: 0x34

Bit position:	31																													0
Bit field:	FEADDR[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	FEADDR[31:0]	End Address for FACI Command Processing	R/W*1

Note 1. These bits can be written when the FRDY bit in the FSTATR register is 1. Writing to these bits are ignored when the FRDY bit is 0. Note that bit [0] and bit [1] are read-only.

The FEADDR register specifies the end address of the target area for Multi Block Erase and Blank Check command processing. When incremental mode is selected as the addressing mode for Blank Checking (when FBCCNT.BCDIR = 0), the address specified in the FSADDR register should be equal to or smaller than the address in the FEADDR register. Conversely, the address in the FSADDR register should be equal to or larger than the address in the FEADDR register when decremental mode is selected as the addressing mode for Blank Check (i.e. when FBCCNT.BCDIR = 1). If the BCDIR, FSADDR, and FEADDR bit settings are inconsistent with the specified rules, the flash sequencer enters the command-locked state (see section 43.11.2. Error Protection).

The FEADDR value is initialized when the SUINIT bit in the FSUINITR register is set to 1. It is also initialized by a reset.

FEADDR[31:0] bits (End Address for FACI Command Processing)

The FEADDR[31:0] bits specify the end address for Multi Block Erase and Blank Check command processing. In command processing, bits 31 to 17 and any bits that do not reach the address boundaries listed in the section 43.4.12. FSADDR : FACI Command Start Address Register are ignored.

For information on the addresses of the flash memory, see section 43.2. Structure of Memory.

43.4.14 FMEPROT : Flash P/E Mode Entry Protection Register

Base address: FACI = 0x407F_E000

Offset address: 0x44

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	CEPROT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	CEPROT	Code Flash P/E Mode Entry Protection 0: FENTRYC bit is not protected 1: FENTRYC bit is protected.	R/W*1 *2 *4
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code	W*3

Note 1. Writing to this bit is only possible when the FRDY bit in the FSTATR register is 1. Writing to this bit while the FRDY bit = 0 is ignored.
Note 2. Writing to this bit is only possible when 16 bits are written and the value written to the KEY bits is D9h.
Note 3. Written values are not retained by these bits (always read as 0x00).
Note 4. Only secure access can write to this register. Both secure access and non-secure read access are allowed. Non-secure write access is denied, but TrustZone access error is note generated.

CEPROT bit (Code Flash P/E Mode Entry Protection)

The CEPROT bit specifies the protection setting of the FRNTRYC bit in the FENTRYR register.

[Setting condition]

43.4.13 FEADDR:FACI命令结束地址寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x34

Bit position:	31																													0
Bit field:	FEADDR[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	FEADDR[31:0]	FACI命令处理的结束地址	R/W*1

注1.当FSTATR寄存器中的FRDY位为1时可以写入这些位。当FRDY位为0时忽略写入这些位。
请注意，位[0]和位[1]是只读的。

FEADDR寄存器指定多块擦除和空白检查命令处理的目标区域的结束地址。Whenincrementalmodeisselectedasthe addressingmodeforBlankChecking(whenFBCCNT.BCDIR=0) theaddressspecifiedintheFSADDRregistershouldbeequaltoorsmallerthantheaddressintheFEADDRregister.Conversely theaddressintheFSADDRregistershouldbeequaltoorlargerthantheaddressintheFEADDRregisterwhendecrementalmodeisselectedastheaddressingmodeforBlankCheck(i.e.whenFBCCNT.BCDIR=1).如果BCDIR、FSADDR和FEADDR位设置与指定规则不一致，则闪存定序器进入命令锁定状态（请参阅第43.11.2.错误保护部分）。

FEADDR值在FSUINITR寄存器中的SUINIT位设置为1时被初始化。它也通过复位被初始化。

FEADDR[31:0]位（FACI命令处理的结束地址）

FEADDR[31:0]位指定多块擦除和空白检查命令处理的结束地址。在命令处理中，位31到17以及任何未到达43.4.12节中列出的地址边界的位。FSADDR：FACI命令起始地址寄存器被忽略。

有关闪存地址的信息，请参阅第43.2节。内存结构。

43.4.14 FMEPROT:FlashPE模式进入保护寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x44

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	CEPROT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	CEPROT	CodeFlashPE模式进入保护 0：FENTRYC位不受保护1：FENTRYC位受保护。	R/W*1 *2 *4
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码	W*3

注1.仅当FSTATR寄存器中的FRDY位为1时才可以写入该位。当FRDY位=0时写入该位被忽略。

注2.仅当写入16位且写入KEY位的值为D9h时才能写入该位。
注3.这些位不保留写入的值（始终读取为0x00）。
注4.只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问。非安全写入访问被拒绝，但生成了TrustZone访问错误。

CEPROT位（代码闪存PE模式进入保护）

CEPROT位指定FENTRYR寄存器中FRNTRYC位的保护设置。

[Setting condition]

- 1 being written to the CEPROT bit while writing to FMEPROT is enabled.

[Clearing condition]

- 0 being written to the CEPROT bit while writing to FMEPROT is enabled.

43.4.15 FBPROT0 : Flash Block Protection Register

Base address: FACI = 0x407F_E000

Offset address: 0x78

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	BPCN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BPCN0	Block Protection for Non-secure Cancel 0: Block protection is enabled 1: Block protection is disabled.	R/W*1 *2
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code	W*3

Note 1. This bit can be written when the FRDY bit in the FSTATR register is 1. Writing to this bit is ignored when the FRDY bit is 0.
Note 2. Writing to this bit is only possible when 16 bits are written and the value written to the KEY[7:0] bits is 0x78.
Note 3. Written values are not retained by these bits (always read as 0x00).

The FBPROT0 register is used to disable the block protect function for non-secure. When the block protect setting is locked by the permanent block setting, it cannot be disabled by this register.

The FBPROT0 value is initialized when the SUINIT bit in the FSUINITR is set to 1, because the FENTRYR value is initialized to 0x0000. It is also initialized by a reset.

BPCN0 bit (Block Protection for Non-secure Cancel)

The BPCN0 bit disables the block protect setting for non-secure function.

[Setting condition]

- When the write-enabling conditions are satisfied and the FENTRYR is not 0x0000, write 1 to this bit.

[Clearing conditions]

- 8 bits being written to FBPROT0 while the FRDY bit is 1.
- A value other than 0x78 specified in the KEY bits and 16 bits are written to FBPROT0 while the FRDY bit is 1.
- 0 being written to the BPCN0 bit while writing to FBPROT0 is enabled.
- The FENTRYR register value is 0x0000.

43.4.16 FBPROT1 : Flash Block Protection for Secure Register

Base address: FACI = 0x407F_E000

Offset address: 0x7C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	BPCN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

●写入FMEPROT时将1写入CEPROT位使能。

[Clearing condition]

●使能写入FMEPROT时将0写入CEPROT位。

43.4.15 FBPROT0：闪存块保护寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x78

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	BPCN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BPCN0	非安全取消的块保护 0：启用块保护1：禁用块保护 。	R/W*1 *2
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码	W*3

注1.当FSTATR寄存器中的FRDY位为1时可以写入该位。当FRDY位为0时忽略写入该位。
注2.仅当写入16位且写入KEY[7:0]位的值为0x78时，才能写入该位。
注3.这些位不保留写入的值（始终读取为0x00）。

FBPROT0寄存器用于禁用非安全的块保护功能。当块保护设置被永久块设置锁定时，该寄存器不能将其禁用。

FBPROT0值在FSUINITR中的SUINIT位设置为1时被初始化，因为FENTRYR值被初始化为0x0000。它也由复位初始化。

BPCN0位（非安全取消的块保护）

BPCN0位禁用非安全功能的块保护设置。

[Setting condition]

●当写使能条件满足且FENTRYR不为0x0000时，向该位写1。

[Clearing conditions]

●FRDY位为1时，将8位写入FBPROT0。
●当FRDY位为1时，将KEY位中指定的0x78和16位以外的值写入FBPROT0。
●写入FBPROT0时将0写入BPCN0位使能。
●FENTRYR寄存器值为0x0000。

43.4.16 FBPROT1：安全寄存器的闪存块保护

Base address: FACI = 0x407F_E000

Offset address: 0x7C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	BPCN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	BPCN1	Block Protection for Secure Cancel 0: Block protection is enabled 1: Block protection is disabled.	R/W*1 *2
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code	W*3

Note 1. Writing to this bit is only possible when the FRDY bit in the FSTATR register is 1. Writing to this bit while FRDY bit = 0 is ignored.
Note 2. Writing to this bit is only possible when 16 bits are written and the value written to the KEY[7:0] bits is 0xB1.
Note 3. Written values are not retained by these bits (always read as 0x00).

The FBPROT1 register is used to disable the block protect function for secure developer. When the block protect setting is locked by the permanent block setting, it cannot be disabled by this register.

The FBPROT1 value is initialized when the SUINIT bit in the FSUINITR is set to 1, because the FENTRYR value is initialized to 0x0000. It is also initialized by a reset.

BPCN1 bit (Block Protection for Secure Cancel)

The BPCN1 bit disables the block protect setting for secure function.

[Setting condition]

- When the write-enabling conditions are satisfied and the FENTRYR is not 0x0000, write 1 to BPCN1.

[Clearing conditions]

- 8 bits being written to FBPROT1 while the FRDY bit is 1.
- A value other than 0xB1 specified in the KEY bits and 16 bits are written to FBPROT1 while the FRDY bit is 1.
- 0 being written to the BPCN1 bit while writing to FBPROT1 is enabled.
- The FENTRYR register value is 0x0000.

43.4.17 FSTATR : Flash Status Register

Base address: FACI = 0x407F_E000

Offset address: 0x80

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	ILGCOMERR	FESETERR	SECERR	OTERR	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	DBFULL	ERSSPD	PRGSPD	—	FLWEERR	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	FLWEERR	Flash Write/Erase Protect Error Flag 0: An error has not occurred 1: An error has occurred.	R
7	—	These bits are read as 0. The write value should be 0.	R/W
8	PRGSPD	Programming Suspend Status Flag 0: The flash sequencer is in a state other than those corresponding to the value 1 1: The flash sequencer is in the programming suspension processing state or programming suspended state.	R

Bit	Symbol	Function	R/W
0	BPCN1	安全取消的块保护 0：启用块保护1：禁用块保护 。	R/W*1 *2
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码	W*3

注1.仅当FSTATR寄存器中的FRDY位为1时才可以写入该位。当FRDY位=0时写入该位被忽略。
注2.仅当写入16位且写入KEY[7:0]位的值为0xB1时，才能写入该位。
注3.这些位不保留写入的值（始终读取为0x00）。

FBPROT1寄存器用于禁用安全开发人员的块保护功能。当块保护设置被永久块设置锁定时，该寄存器不能将其禁用。

FBPROT1值在FSUINITR中的SUINIT位设置为1时被初始化，因为FENTRYR值被初始化为0x0000。它也由复位初始化。

BPCN1位（安全取消的块保护）

BPCN1位禁用安全功能的块保护设置。

[Setting condition]

●当写使能条件满足且FENTRYR不为0x0000时，向BPCN1写1。

[Clearing conditions]

●FRDY位为1时，将8位写入FBPROT1。
●当FRDY位为1时，将KEY位中指定的0xB1和16位以外的值写入FBPROT1。
●写入FBPROT1时将0写入BPCN1位使能。
●FENTRYR寄存器值为0x0000。

43.4.17 FSTATR：闪存状态寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x80

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	ILGCOMERR	FESETERR	SECERR	OTERR	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	DBFULL	ERSSPD	PRGSPD	—	FLWEERR	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	这些位被读取为0。写入值应为0。	R/W
6	FLWEERR	闪存写擦除保护错误标志 0：未发生错误1：发生错误 。	R
7	—	这些位被读取为0。写入值应为0。	R/W
8	PRGSPD	编程挂起状态标志 0：flashsequencer处于与值1对应的状态以外的状态1：flashsequencer处于编程暂停处理状态或编程暂停状态。	R

Bit	Symbol	Function	R/W
9	ERSSPD	Erasure Suspend Status Flag 0: The flash sequencer is in a state other than those corresponding to the value 1 1: The flash sequencer is in the erasure suspension processing state or the erasure suspended state.	R
10	DBFULL	Data Buffer Full Flag 0: The data buffer is empty 1: The data buffer is full.	R
11	SUSRDY	Suspend Ready Flag 0: The flash sequencer cannot receive P/E suspend commands 1: The flash sequencer can receive P/E suspend commands.	R
12	PRGERR	Programming Error Flag 0: Programming has completed successfully 1: An error has occurred during programming.	R
13	ERSERR	Erasure Error Flag 0: Erasure has completed successfully 1: An error has occurred during erasure.	R
14	ILGLERR	Illegal Command Error Flag 0: The flash sequencer has not detected an illegal FACI command or illegal flash memory access 1: The flash sequencer has detected an illegal FACI command or illegal flash memory access.	R
15	FRDY	Flash Ready Flag 0: Program, Block Erase, Multi Block Erase, P/E suspend, P/E resume, Forced Stop, Blank Check, or Configuration set command processing is in progress 1: None of the above is in progress.	R
19:16	—	These bits are read as 0. The write value should be 0.	R/W
20	OTERR	Other Error 0: A status clear or forced stop command processing is complete 1: An error has occurred.	R
21	SECERR	Security Error 0: A status clear or forced stop command processing is complete 1: An error has occurred.	R/W
22	FESETERR	FENTRY Setting Error 0: A status clear or forced stop command processing is complete 1: An error has occurred.	R
23	ILGCOMERR	Illegal Command Error 0: A status clear or forced stop command processing is complete 1: An error has occurred.	R
31:24	—	These bits are read as 0. The write value should be 0.	R/W

The FSTATR register indicates the state of the flash sequencer.

FLWEERR flag (Flash Write/Erase Protect Error Flag)

The FLWEERR flag indicates a violation of the flash memory overwrite protection setting in the FWEPROR register. When this flag is 1, the flash sequencer is in the command-locked state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The flash sequencer starts processing the Forced Stop command.

PRGSPD flag (Programming Suspend Status Flag)

The PRGSPD flag indicates that the flash sequencer is in the programming suspension processing state or programming suspended state.

[Setting condition]

Bit	Symbol	Function	R/W
9	ERSSPD	擦除挂起状态标志 0：闪存定序器处于与值1对应的状态以外的状态1：闪存定序器处于擦除暂停处理状态或擦除暂停状态。	R
10	DBFULL	数据缓冲区满标志 0：数据缓冲区为空1：数据缓冲区已满。	R
11	SUSRDY	挂起就绪标志 0：flash定序器不能接收PE挂起命令1：flash定序器可以接收PE挂起命令。	R
12	PRGERR	编程错误标志 0：烧录成功1：烧录出错。	R
13	ERSERR	擦除错误标志 0：擦除已成功完成1：擦除过程中发生错误。	R
14	ILGLERR	非法命令错误标志 0：闪存定序器未检测到非法FACI命令或非法闪存访问 1：闪存定序器检测到非法FACI命令或非法闪存访问。	R
15	FRDY	闪存就绪标志 0：程序、块擦除、多块擦除、PE暂停、PE恢复、强制停止、空白检查或配置设置命令处理正在进行中 1：以上均未进行。	R
19:16	—	这些位被读取为0。写入值应为0。	R/W
20	OTERR	其他错误 0：状态清除或强制停止命令处理完成1：发生错误。	R
21	SECERR	安全错误 0：状态清除或强制停止命令处理完成1：发生错误。	R/W
22	FESETERR	FENTRY设置错误 0：状态清除或强制停止命令处理完成1：发生错误。	R
23	ILGCOMERR	非法命令错误 0：状态清除或强制停止命令处理完成1：发生错误。	R
31:24	—	这些位被读取为0。写入值应为0。	R/W

FSTATR寄存器指示闪存定序器的状态。

FLWEERR标志（闪存写擦除保护错误标志）

FLWEERR标志表示违反了FWEPROR寄存器中的闪存覆盖保护设置。当该标志为1时，闪存定序器处于命令锁定状态。

[Setting condition]

●发生错误。

[Clearing condition]

●闪存定序器开始处理强制停止命令。

PRGSPD标志（编程暂停状态标志）

PRGSPD标志指示闪存定序器处于编程暂停处理状态或编程暂停状态。

[Setting condition]

- The flash sequencer starts processing in response to the programming suspend command.

[Clearing conditions]

- Reception of the P/E resume command by the flash sequencer (after write access to the FACI command-issuing area is complete)
- The flash sequencer starts processing the Forced Stop command.

ERSSPD flag (Erasure Suspend Status Flag)

The ERSSPD flag indicates that the flash sequencer is in the erasure suspension processing state or erasure suspended state.

[Setting condition]

- The flash sequencer starts processing in response to an erasure suspend command.

[Clearing condition]

- Reception of the P/E resume command by the flash sequencer (after write access to the FACI command-issuing area is complete)
- The flash sequencer starts processing of the Forced Stop command.

DBFULL flag (Data Buffer Full Flag)

The DBFULL flag indicates the state of the data buffer when the program command is issued. The flash sequencer incorporates a buffer for write data (data buffer). When data for writing to the flash memory are written to the FACI command-issuing area while the data buffer is full, the flash sequencer inserts a wait cycle in the peripheral bus.

[Setting condition]

- The data buffer becomes full while program commands are issued.

[Clearing condition]

- The data buffer becomes empty.

SUSRDY flag (Suspend Ready Flag)

The SUSRDY flag indicates whether the flash sequencer can receive a P/E suspend command.

[Setting condition]

- After starting programming/erasure processing, the flash sequencer enters a state in which P/E suspend commands can be received.

[Clearing conditions]

- Reception of the P/E suspend command or Forced Stop command by the flash sequencer (after write access to the FACI command-issuing area is complete)
- During programming or erasure, the flash sequencer enters the command-locked state
- Programming or erasure has completed.

PRGERR flag (Programming Error Flag)

The PRGERR flag indicates the result of programming of the flash memory. When this flag is 1, the flash sequencer is in the command-locked state.

[Setting condition]

- An error has occurred during programming.

[Clearing condition]

- The flash sequencer starts processing of the Status Clear or Forced Stop command.

ERSERR flag (Erasure Error Flag)

The ERSERR flag indicates the result of erasure of the flash memory. When this flag is 1, the flash sequencer is in the command-locked state.

●闪存定序器响应编程暂停命令开始处理。

[Clearing conditions]

●闪存定序器接收到PEresume命令（在对FACI命令发出区域的写访问完成后）

●闪存定序器开始处理强制停止命令。

ERSSPD标志（擦除挂起状态标志）

ERSSPD标志指示闪存定序器处于擦除暂停处理状态或擦除暂停状态。

[Setting condition]

●闪存定序器响应擦除挂起命令开始处理。

[Clearing condition]

●闪存定序器接收到PEresume命令（在对FACI命令发出区域的写访问完成后）

●闪存定序器开始处理强制停止命令。

DBFULL标志（数据缓冲区满标志）

DBFULL标志指示发出程序命令时数据缓冲区的状态。闪存定序器包含一个用于写入数据的缓冲区（数据缓冲区）。当用于写入闪存的数据写入到FACI命令发布区，而数据缓冲区已满时，闪存定序器会在外围总线中插入一个等待周期。

[Setting condition]

●发出程序命令时数据缓冲区已满。

[Clearing condition]

●数据缓冲区变空。

SUSRDY标志（挂起就绪标志）

SUSRDY标志指示闪存定序器是否可以接收PE挂起命令。

[Setting condition]

●开始编程擦除处理后，flash定序器进入可以接收PE挂起命令的状态。

[Clearing conditions]

●闪存定序器接收到PE暂停命令或强制停止命令（在对FACI命令发布区域的写访问完成后）

●在编程或擦除期间，闪存定序器进入命令锁定状态

●编程或擦除已完成。

PRGERR标志（编程错误标志）

PRGERR标志指示闪存的编程结果。当该标志为1时，闪存定序器处于命令锁定状态。

[Setting condition]

●编程过程中出现错误。

[Clearing condition]

●闪存定序器开始处理状态清除或强制停止命令。

ERSERR标志（擦除错误标志）

ERSERR标志指示闪存擦除的结果。当该标志为1时，闪存定序器处于命令锁定状态。

[Setting condition]

- An error has occurred during erasure.

[Clearing condition]

- The flash sequencer starts processing of the Status Clear or Forced Stop command.

ILGLERR flag (Illegal Command Error Flag)

The ILGLERR flag indicates that the flash sequencer has detected an illegal FACI command or flash memory access. If this flag is 1, the flash sequencer is in the command-locked state.

[Setting conditions]

- See section 43.11.2. Error Protection.

[Clearing condition]

- The flash sequencer starts processing of the Status Clear or Forced Stop command.

FRDY flag (Flash Ready Flag)

The FRDY flag indicates the command processing state of the flash sequencer.

[Setting conditions]

- The flash sequencer completes command processing
- The flash sequencer receives a P/E suspend command and suspends programming of the flash memory
- The flash sequencer received the Forced Stop command and ended command processing.

[Clearing conditions]

- The flash sequencer received an FACI command
- For Program and Configuration setting, the first write access to the FACI command-issuing area
- For other commands, the last write access to the FACI command-issuing area.

OTERR flag (Other Error)

See Table 43.21. When this flag is 1, the flash sequencer is in the command-lock state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The status clear or forced stop command processing is complete.

SECERR flag (Security Error)

See Table 43.21. When this flag is 1, the flash sequencer is in the command-lock state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The status clear or forced stop command processing is complete.

FESETERR flag (FENTRY Setting Error)

See Table 43.21. When this flag is 1, the flash sequencer is in the command-lock state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The status clear or forced stop command processing is complete.

[Setting condition]

●擦除过程中发生错误。

[Clearing condition]

●闪存定序器开始处理状态清除或强制停止命令。

ILGLERR标志（非法命令错误标志）

ILGLERR标志表示闪存定序器检测到非法FACI命令或闪存访问。如果该标志为1，则闪存定序器处于命令锁定状态。

[Setting conditions]

●请参阅第43.11.2节。错误保护。

[Clearing condition]

●闪存定序器开始处理状态清除或强制停止命令。

FRDY标志（闪存就绪标志）

FRDY标志指示闪存定序器的命令处理状态。

[Setting conditions]

●flashsequencer完成命令处理

●闪存定序器收到PE暂停命令并暂停闪存的编程

●闪存定序器收到强制停止命令并结束命令处理。

[Clearing conditions]

●闪存定序器收到FACI命令

●对于ProgramandConfiguration设置，对FACI命令发布区的第一次写访问

●对于其他命令，对FACI命令发布区的最后一次写访问。

OTERR flag (Other Error)

见表43.21。当该标志为1时，闪存定序器处于命令锁定状态。

[Setting condition]

●发生错误。

[Clearing condition]

●状态清除或强制停止命令处理完成。

SECERR flag (Security Error)

见表43.21。当该标志为1时，闪存定序器处于命令锁定状态。

[Setting condition]

●发生错误。

[Clearing condition]

●状态清除或强制停止命令处理完成。

FESETERR标志（FENTRY设置错误）

见表43.21。当该标志为1时，闪存定序器处于命令锁定状态。

[Setting condition]

●发生错误。

[Clearing condition]

●状态清除或强制停止命令处理完成。

ILGCOMERR flag (Illegal Command Error)

See Table 43.21. When this flag is 1, the flash sequencer is in the command-lock state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The status clear or forced stop command processing is complete.

43.4.18 FENTRYR : Flash P/E Mode Entry Register

Base address: FACI = 0x407F_E000

Offset address: 0x84

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRYC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FENTRYC	Code Flash P/E Mode Entry 0: Code flash is in read mode 1: Code flash is in P/E mode.	R/W*1*2
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	FENTRYD	Data Flash P/E Mode Entry 0: Data flash is in read mode 1: Data flash is in P/E mode.	R/W*1*2
15:8	KEY[7:0]	Key Code	W*3

Note 1. These bits can be written when the FRDY bit in the FSTATR register is 1. Writing to these bits are ignored when the FRDY bit is 0.
Note 2. Writing to these bits is only possible when 16 bits are written and the value written to the KEY[7:0] bits is 0xAA.
Note 3. Written values are not retained by these bits (always read 0x00).

FENTRYR is used to specify code flash P/E mode or data flash P/E mode. To specify the code flash P/E mode or data flash P/E mode so that the flash sequencer can receive FACI commands, set either the FENTRYD or FENTRYC bit to 1 to place the flash sequencer in P/E mode.

FENTRYR is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

Note: Writing a value of 0XAA81 to this register causes the ILGLERR bit in the FSTATR register to be set to 1, resulting in the flash sequencer being placed in the command-locked state.

FENTRYC bit (Code Flash P/E Mode Entry)

The FENTRYC bit specifies P/E mode for the code flash memory.

[Setting condition]

- Write 1 to the FENTRYC bit while writing to FENTRYR is enabled and FENTRYR is 0x0000.

[Clearing conditions]

- Write 8 bits to FENTRYR while the FRDY bit is 1
- A value other than 0xAA is specified in the KEY[7:0] bits and 16 bits are written to FENTRYR while the FRDY bit is 1
- Write 0 to the FENTRYC bit while writing to FENTRYR is enabled
- Write to FENTRYR while writing is enabled and its value is other than 0x0000
- The protection of FMEPROT register is enabled.

FENTRYD bit (Data Flash P/E Mode Entry)

The FENTRYD bit specifies P/E mode for the data flash memory.

ILGCOMERR标志（非法命令错误）

见表43.21。当该标志为1时，闪存定序器处于命令锁定状态。

[Setting condition]

●发生错误。

[Clearing condition]

●状态清除或强制停止命令处理完成。

43.4.18 FENTRYR:FlashPE模式进入寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x84

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRYC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FENTRYC	CodeFlashPE模式进入 0：Codeflash处于读取模式1 ：Codeflash处于PE模式。	R/W*1*2
6:1	—	这些位被读取为0。写入值应为0。	R/W
7	FENTRYD	数据闪存PE模式进入 0：数据闪存处于读取模式1 ：数据闪存处于PE模式。	R/W*1*2
15:8	KEY[7:0]	关键代码	W*3

注1.当FSTATR寄存器中的FRDY位为1时可以写入这些位。当FRDY位为0时忽略写入这些位。
注2.仅当写入16位且写入KEY[7:0]位的值为0xAA时，才能写入这些位。
注3.这些位不保留写入的值（始终读取0x00）。

FENTRYR用于指定代码闪存PE模式或数据闪存PE模式。要指定代码闪存PE模式或数据闪存PE模式，以便闪存定序器可以接收FACI命令，请将FENTRYD或FENTRYC位设置为1以将闪存定序器置于PE模式。

当FSUNITR中的SUINIT位设置为1时，FENTRYR被初始化。它也被复位初始化。

Note: 将值0XAA81写入该寄存器会导致FSTATR寄存器中的ILGLERR位设置为1，从而导致闪存定序器置于命令锁定状态。

FENTRYC位（代码闪存PE模式进入）

FENTRYC位指定代码闪存的PE模式。

[Setting condition]

●写入1到FENTRYC位，同时写入FENTRYR使能并且FENTRYR为0x0000。

[Clearing conditions]

●FRDY位为1时向FENTRYR写入8位
●KEY[7:0]位中指定了0xAA以外的值，当FRDY位为1时，将16位写入FENTRYR
●使能写入FENTRYR时向FENTRYC位写入0
●启用写入时写入FENTRYR，其值不是0x0000
●FMEPROT寄存器保护使能。

FENTRYD位（数据闪存PE模式进入）

FENTRYD位指定数据闪存的PE模式。

[Setting condition]

- Write 1 to the FENTRYD bit while writing to FENTRYR is enabled and FENTRYR is 0x0000.

[Clearing conditions]

- Write 8 bits to FENTRYR while the FRDY bit is 1
- Writing of 16 bits to FENTRYR with a value other than 0xAA specified for the KEY[7:0] bits while the FRDY bit is 1
- Write 0 to the FENTRYD bit while writing to FENTRYR is enabled
- Write to FENTRYR while writing is enabled and its value is other than 0x0000.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits control writing permission to the FENTRYD or FENTRYC bits.

43.4.19 FSUINITR : Flash Sequencer Setup Initialization Register

Base address: FACI = 0x407F_E000

Offset address: 0x8C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	SUINIT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SUINIT	Set-Up Initialization 0: The FSADDR, FEADDR, FBPROT0, FBPROT1, FENTRYR, FBCCNT, and FCPSR flash sequencer setup registers keep their current values 1: The FSADDR, FEADDR, FBPROT0, FBRPOT1, FENTRYR, FBCCNT, and FCPSR flash sequencer setup registers are initialized.	R/W*1*2
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code	W*3

Note 1. This bit can be written when the FRDY bit in the FSTATR register is 1. Writing to this bit is ignored when the FRDY bit is 0.
Note 2. Writing to these bits is only possible when 16 bits are written and the value written to the KEY[7:0] bits is 0x2D.
Note 3. Written values are not retained by these bits (always read 0x00).

FSUINITR is used for initialization of the flash sequencer setup.

SUINIT bit (Set-Up Initialization)

The SUINIT bit initializes the following flash sequencer setup registers:

- FSADDR
- FEADDR
- FBPROT0
- FBPROT1
- FENTRYR
- FBCCNT
- FCPSR.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits control writing permission to the SUINIT bit.

[Setting condition]

●写入1到FENTRYD位，同时写入FENTRYR使能并且FENTRYR为0x0000。

[Clearing conditions]

●FRDY位为1时向FENTRYR写入8位
●当FRDY位为1时，将16位写入FENTRYR，其中KEY[7:0]位指定的值不是0xAA
●使能写入FENTRYR时向FENTRYD位写入0
●写入启用时写入FENTRYR，其值不是0x0000。

KEY[7:0] bits (Key Code)

KEY[7:0]位控制对FENTRYD或FENTRYC位的写入权限。

43.4.19 FSUINITR：闪存定序器设置初始化寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x8C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	SUINIT
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SUINIT	Set-Up Initialization 0：FSADDR、FEADDR、FBPROT0、FBPROT1、FENTRYR、FBCCNT和FCPSR闪存定序器设置寄存器保持其当前值 1：初始化FSADDR、FEADDR、FBPROT0、FBRPOT1、FENTRYR、FBCCNT和FCPSR闪存定序器设置寄存器。	R/W*1*2
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码	W*3

注1.当FSTATR寄存器中的FRDY位为1时可以写入该位。当FRDY位为0时忽略写入该位。
注2.仅当写入16位且写入KEY[7:0]位的值为0x2D时才能写入这些位。
注3.这些位不保留写入的值（始终读取0x00）。

FSUINITR用于初始化闪存定序器设置。

SUINIT bit (Set-Up Initialization)

SUINIT位初始化以下闪存序列器设置寄存器：

- FSADDR
- FEADDR
- FBPROT0
- FBPROT1
- FENTRYR
- FBCCNT
- FCPSR.

KEY[7:0] bits (Key Code)

KEY[7:0]位控制对SUINIT位的写入权限。

43.4.20 FCMDR : FACI Command Register

Base address: FACI = 0x407F_E000

Offset address: 0xA0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMDR[7:0]								PCMDR[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	PCMDR[7:0]	Pre-command Flag The command just before the latest command is stored.	R
15:8	CMDR[7:0]	Command Flag The latest command is stored.	R

FCMDR records the two most recent commands accepted by the flash sequencer.

PCMDR[7:0] bits (Pre-command Flag)

The PCMDR[7:0] bits indicate the command received immediately before the latest command received by the flash sequencer.

CMDR[7:0] bits (Command Flag)

The CMDR[7:0] bits indicate the latest command received by the flash sequencer.

Table 43.5 States of FCMDR after receiving commands

Command	CMDR	PCMDR
Program	0xE8	Previous command
Block erase	0xD0	0x20
Multi block erase	0xD0	0x21
P/E suspend	0xB0	Previous command
P/E resume	0xD0	Previous command
Status Clear	0x50	Previous command
Forced Stop	0xB3	Previous command
Blank Check	0xD0	0x71
Configuration set	0x40	Previous command

43.4.21 FBCCNT : Blank Check Control Register

Base address: FACI = 0x407F_E000

Offset address: 0xD0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BCDIR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BCDIR	Blank Check Direction 0: Blank checking is executed from the lower addresses to the higher addresses (incremental mode) 1: Blank checking is executed from the higher addresses to the lower addresses (decremental mode).	R/W

43.4.20 FCMDR:FACI命令寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xA0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMDR[7:0]								PCMDR[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	PCMDR[7:0]	Pre-command Flag 存储最新命令之前的命令。	R
15:8	CMDR[7:0]	命令标志 存储最新的命令。	R

FCMDR记录闪存定序器最近接受的两个命令。

PCMDR[7:0] bits (Pre-command Flag)

PCMDR[7:0]位指示在闪存定序器接收到的最新命令之前收到的命令。

CMDR[7:0] bits (Command Flag)

CMDR[7:0]位指示闪存定序器接收到的最新命令。

Table 43.5 FCMDR收到指令后的状态

Command	CMDR	PCMDR
Program	0xE8	上一条命令
块擦除	0xD0	0x20
多块擦除	0xD0	0x21
P/E suspend	0xB0	上一条命令
P/E resume	0xD0	上一条命令
状态清除	0x50	上一条命令
强制停止	0xB3	上一条命令
空白支票	0xD0	0x71
配置集	0x40	上一条命令

43.4.21 FBCCNT:空白检查控制寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xD0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BCDIR
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BCDIR	空白支票方向 0：从低地址到高地址执行空白检查（增量模式） 1：从高地址到低地址执行空白检查（递减模式）。	R/W

Bit	Symbol	Function	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

FBCCNT specifies the addressing mode in processing the Blank Check command. FBCCNT is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

BCDIR bit (Blank Check Direction)

The BCDIR bit specifies the addressing mode for Blank Check.

43.4.22 FBCSTAT : Blank Check Status Register

Base address: FACI = 0x407F_E000

Offset address: 0xD4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BCST	Blank Check Status Flag 0: The target area is in the non-programmed state, that is, the area has been erased but has not yet been reprogrammed 1: The target area has been programmed with 0s or 1s.	R
7:1	—	These bits are read as 0. The write value should be 0.	R/W

FBCSTAT stores the results of checking in response to the Blank Check command.

BCST flag (Blank Check Status Flag)

The BCST flag indicates the results of checking in response to the Blank Check command.

43.4.23 FPSADDR : Data Flash Programming Start Address Register

Base address: FACI = 0x407F_E000

Offset address: 0xD8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PSADR[16:0]																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
16:0	PSADR[16:0]	Programmed Area Start Address The address of the first programmed area	R
31:17	—	These bits are read as 0. The write value should be 0.	R/W

FPSADDR indicates the address of the first programmed area found in processing of the Blank Check command.

PSADR[16:0] bits (Programmed Area Start Address)

The PSADR[16:0] bits indicate the address of the first programmed area found in processing of the Blank Check command. The address is an offset from the address where the data flash memory starts. The setting of these bits is only valid if the BCST bit in the FBCSTAT register is 1 and while the FRDY bit in the FSTATR register is 1. When the BCST bit in the FBCSTAT register is 0, the PSADR[16:0] bits hold the address produced by the previous check.

Bit	Symbol	Function	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

FBCCNT指定处理空白检查命令的寻址模式。当FSUINITR中的SUINIT位设置为1时，FBCCNT被初始化。它也被复位初始化。

BCDIR位（空白检查方向）

BCDIR位指定空白检查的寻址模式。

43.4.22 FBCSTAT:空白检查状态寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xD4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BCST
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BCST	空白检查状态标志 0：目标区域处于非编程状态，即该区域已被擦除但尚未重新编程 1：目标区域已编程为0或1。	R
7:1	—	这些位被读取为0。写入值应为0。	R/W

FBCSTAT存储响应空白检查命令的检查结果。

BCST标志（空白检查状态标志）

BCST标志指示响应空白检查命令的检查结果。

43.4.23 FPSADDR:数据闪存编程起始地址寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xD8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PSADR[16:0]																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
16:0	PSADR[16:0]	编程区起始地址 第一个编程区域的地址	R
31:17	—	这些位被读取为0。写入值应为0。	R/W

FPSADDR指示在处理空白检查命令时发现的第一个编程区域的地址。

PSADR[16:0]位（编程区起始地址）

PSADR[16:0]位指示在处理空白检查命令时发现的第一个编程区域的地址。
该地址是数据闪存起始地址的偏移量。仅当FBCSTAT寄存器中的BCST位为1且FSTATR寄存器中的FRDY位为1时，这些位的设置才有效。当
FBCSTAT寄存器为0，PSADR[16:0]位保存上一次检查产生的地址。

43.4.24 FSUASMON : Flash Startup Area Select Monitor Register

Base address: FACI = 0x407F_E000

Offset address: 0xDC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BTFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSPR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	These bits are read as 0. The write value should be 0.	R
15	FSPR	Protection Programming Flag to set Boot Flag and Startup Area Control 0: Protected state 1: Non-protected state.	R
30:16	—	These bits are read as 0. The write value should be 0.	R
31	BTFLG	Flag of Startup Area Select for Boot Swap 0: The startup area is the alternate block (block 1) 1: The startup area is the default block (block 0).	R

FSPR bit (Protection Programming Flag to set Boot Flag and Startup Area Control)

The FSPR bit indicates the protection state against the configuration set command for the BTFLG bit, and FSUACR Register.

In response to a reset or configuration set command, the FACI transfers data from flash memory to this register.

BTFLG bit (Flag of Startup Area Select for Boot Swap)

The BTFLG bit indicates whether the address of the startup area is exchanged for the boot swap function or not.

In response to a reset or configuration set command, the FACI transfers data from flash memory to this register.

43.4.25 FCPSR : Flash Sequencer Processing Switching Register

Base address: FACI = 0x407F_E000

Offset address: 0xE0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESUSPMD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESUSPMD	Erasure Suspend Mode 0: Suspension priority mode 1: Erasure priority mode.	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

FCPSR selects the erasure suspension mode. FCPSR is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

43.4.24 FSUASMON:闪存启动区选择监控寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xDC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BTFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSPR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	这些位被读取为0。写入值应为0。	R
15	FSPR	保护编程标志设置引导标志和启动区控制 0：保护状态1：非保护状态。	R
30:16	—	这些位被读取为0。写入值应为0。	R
31	BTFLG	引导交换的启动区域选择标志 0：启动区为alternateblock（block1）1：启动区为defaultblock（block0）。	R

FSPR位（用于设置引导标志和启动区域控制的保护编程标志）

FSPR位指示针对BTFLG位的配置设置命令的保护状态，而FSUACR Register.

响应复位或配置设置命令，FACI将数据从闪存传输到该寄存器。

BTFLG位（用于引导交换的启动区域选择标志）

BTFLG位指示启动区域的地址是否被交换为引导交换功能。

响应复位或配置设置命令，FACI将数据从闪存传输到该寄存器。

43.4.25 FCPSR:闪存定序器处理切换寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xE0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESUSPMD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESUSPMD	擦除挂起模式 0：暂停优先模式1：擦除优先模式。	R/W
15:1	—	这些位被读取为0。写入值应为0。	R/W

FCPSR选择擦除暂停模式。当FSUINITR中的SUINIT位设置为1时，FCPSR被初始化。它也被复位初始化。

ESUSPMD bit (Erasure Suspend Mode)

The ESUSPMD bit selects the erasure suspension mode when a P/E suspend command is issued while the flash sequencer is executing erasure processing (see section 43.9.3.10. P/E Suspend Command). This bit should be set before issuing Block Erase or Multi Block Erase command.

43.4.26 FPCKAR : Flash Sequencer Processing Clock Notification Register

Base address: FACI = 0x407F_E000

Offset address: 0xE4

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								PCKA[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Bit	Symbol	Function	R/W
7:0	PCKA[7:0]	Flash Sequencer Operating Clock Notification These bits are used to set the operating frequency of the flash sequencer while processing FACI commands.	R/W*1*2
15:8	KEY[7:0]	Key Code	W*3

Note 1. This bit can be written when the FRDY bit in the FSTATR register is 1. Writing to this bit is ignored when the FRDY bit is 0.
Note 2. Writing to these bits is only possible when 16 bits are written and the value written to the KEY[7:0] bits is 0x1E.
Note 3. Written values are not retained by these bits (always read 0x00).

FPCKAR specifies the operating frequency of the flash sequencer while processing FACI commands. The highest operating frequency for the given product is set as the initial value.

PCKA[7:0] bits (Flash Sequencer Operating Clock Notification)

The PCKA[7:0] bits specify the operating frequency of the flash sequencer while processing FACI commands. Set the desired frequency for these bits before issuing an FACI command. Specifically, convert the frequency in MHz to a binary number and set it for these bits.

Example:

Frequency is 35.9 MHz (PCKA = 0x24)

Round up the first decimal place of 35.9 MHz to a whole number (= 36) and convert it into a binary number.

If the value set in these bits is smaller than the actual operating frequency of the flash sequencer, the flash memory programming/erasure characteristics cannot be guaranteed. If the value set in these bits is greater than the actual operating frequency of the flash sequencer, the flash memory programming/erasure characteristics can be guaranteed but the FACI command processing time such as the time programming/erasure takes will increase. The minimum FACI command processing time is obtained when the operating frequency of the flash sequencer is the same as the PCKA value.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits control writing permission to the PCKA bit.

43.4.27 FSUACR : Flash Startup Area Control Register

Base address: FACI = 0x407F_E000

Offset address: 0xE8

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	SAS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ESUSPMD位（擦除挂起模式）

当闪存定序器正在执行擦除处理时发出PE暂停命令时，ESUSPMD位选择擦除暂停模式（请参阅第43.9.3.10节。PE暂停命令）。该位应在发出块擦除或多块擦除命令之前设置。

43.4.26 FPCKAR:闪存定序器处理时钟通知寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xE4

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								PCKA[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Bit	Symbol	Function	R/W
7:0	PCKA[7:0]	闪存定序器工作时钟通知 这些位用于在处理时设置闪存定序器的工作频率 FACI命令。	R/W*1*2
15:8	KEY[7:0]	关键代码	W*3

注1.当FSTATR寄存器中的FRDY位为1时可以写入该位。当FRDY位为0时忽略写入该位。
注2.仅当写入16位且写入KEY[7:0]位的值为0x1E时，才能写入这些位。
注3.这些位不保留写入的值（始终读取0x00）。

FPCKAR在处理FACI命令时指定闪存定序器的工作频率。将给定产品的最高工作频率设置为初始值。

PCKA[7:0]位（闪存定序器工作时钟通知）

PCKA[7:0]位指定闪存定序器在处理FACI命令时的工作频率。在发出FACI命令之前为这些位设置所需的频率。具体来说，将以MHz为单位的频率转换为二进制数并为这些位设置它。

Example:

频率为35.9MHz(PCKA=0x24)

将35.9MHz的第一个小数位四舍五入为整数(=36)并将其转换为二进制数。

如果这些位中设置的值小于闪存定序器的实际工作频率，则无法保证闪存编程擦除特性。如果这些位中设置的值大于闪存定序器的实际工作频率，则可以保证闪存编程擦除特性，但FACI命令处理时间（例如编程擦除所花费的时间）会增加。当闪存定序器的工作频率与PCKA值相同时，得到最小FACI命令处理时间。

KEY[7:0] bits (Key Code)

KEY[7:0]位控制对PCKA位的写入权限。

43.4.27 FSUACR：闪存启动区控制寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xE8

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	SAS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SAS[1:0]	Startup Area Select 0 0: Startup area is selected by BTFLG bit 0 1: Startup area is selected by BTFLG bit 1 0: Startup area is temporarily switched to the default area (block 0) 1 1: Startup area is temporarily switched to the alternate area (block 1).	R/W*1 *3
7:2	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code	W*2

Note 1. Following described the write condition of thisese bits (these conditions are required at the same time).
1. Access size to this register is 16 bits
2. The value of KEY[7:0] is 0x66
3. The FSPR bit is 1.

Note 2. Written values are not retained by these bits (always read 0x00).

Note 3. Only secure access can write to this register. Both secure access and non-secure read access are allowed. Non-secure write access is denied, but TrustZone access error is note generated.

FSUACR sets the startup area for the boot swap function.

SAS[1:0] bits (Startup Area Select)

The SAS[1:0] bits select the startup area. Three methods are available for changing the startup area.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits control writing permission to the SAS [1:0] bits.

43.4.28 FCKMHZ : Data Flash Access Frequency Register

Base address: FLAD = 0x407F_C000

Offset address: 0x40

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FCKMHZ[7:0]							
Value after reset:	0	0	1	1	1	1	0	0

Bit	Symbol	Function	R/W
7:0	FCKMHZ[7:0]	Data Flash Access Frequency Register These bits optimize the speed of reading the data flash memory.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

This register optimizes the speed of reading the data flash memory.

Set the frequency of the peripheral module clock (FCLK) of internal peripheral bus which is the clock for access to the data flash memory, in MHz units. For example, 35.9 MHz should be rounded up and set the frequency to 36. Number of cycles required for access to the data flash memory are inserted according to the frequency. When changing the frequency of the FCLK, follow the procedure below to modify the value of the data flash access frequency register (FCKMHZ) in either of the following ways according to whether operation is at a lower frequency before or after the change.

- When changing the speed from low to high: Modify FCKMHZ. After confirming the change by reading FCKMHZ, change the frequency.
- When changing the speed from high to low: Change the frequency. After the frequency is changed, modify FCKMHZ.

43.5 Flash Cache

43.5.1 Feature of flash cache

Bit	Symbol	Function	R/W
1:0	SAS[1:0]	启动区域选择 00：启动区域由BTFLG位选择01：启动区域由BTFLG位选择10：启动区域暂时切换到默认区域（块0）11：启动区域暂时切换到备用区域（块1）。	R/W*1 *3
7:2	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码	W*2

注1.下面描述了这些位的写入条件（这些条件是同时需要的）。1.对该寄存器的访问大小为16位2.KEY[7:0]的值为0x663.FSPR位为1。

注2.这些位不保留写入的值（始终读取0x00）。

注3.只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问。非安全写入访问被拒绝，但生成了TrustZone访问错误。

FSUACR设置引导交换功能的启动区域。

SAS[1:0]位（启动区域选择）

SAS[1:0]位选择启动区域。三种方法可用于更改启动区域。

KEY[7:0] bits (Key Code)

KEY[7:0]位控制对SAS[1:0]位的写入权限。

43.4.28 FCKMHZ:数据闪存访问频率寄存器

Base address: FLAD = 0x407F_C000

Offset address: 0x40

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FCKMHZ[7:0]							
重置后的值：	0	0	1	1	1	1	0	0

Bit	Symbol	Function	R/W
7:0	FCKMHZ[7:0]	数据闪存访问频率寄存器 这些位优化了数据闪存的读取速度。	R/W

Note: 如果安全属性配置为安全：●
- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
- 允许安全和非安全访问。

该寄存器优化了数据闪存的读取速度。

设置内部外围总线的外围模块时钟(FCLK)的频率，它是访问数据闪存的时钟，以MHz为单位。例如，35.9MHz应向上取整，并将频率设置为36。根据频率插入访问数据闪存所需的周期数。当改变FCLK的频率时，根据改变之前或之后是在较低频率下操作，按照以下步骤，通过以下任一方式修改数据闪存访问频率寄存器(FCKMHZ)的值。

●转速由低变高时：修改FCKMHZ。通过读取FCKMHZ确认更改后，更改频率。

●速度由高变低时：改变频率。频率改变后，修改FCKMHZ。

43.5 闪存缓存

43.5.1 闪存缓存的特点

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access
- FLPF, for the prefetch access in CPU instruction fetches

Table 43.6 Flash Cache 1 (FCACHE1) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU instruction Fetch
Capacity	256 Bytes
Associativity	8WAY set associative
	128 bits/entry (128 bit aligned data), 2 entries/way
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

Table 43.7 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

Table 43.8 Prefetch Buffer (FLPF) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Capacity	32 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 2 entries
Request Address	Next address of previous CPU Instruction
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

FCACHE(FlashCache)加快了从总线主机到闪存的读取访问。FCACHE包括：

- ●FCACHE1，用于CPU取指
- ●FCACHE2，用于CPU操作数访问
- ●FLPF，用于CPU取指中的预取访问

Table 43.6 闪存1(FCACHE1)概述

缓存目标区域	0x0000_0000 - 0x007F_FFFF
目标总线主控	CPU指令取指
Capacity	256 Bytes
Associativity	8WAY集合关联
	128位入口（128位对齐数据），2入口方式
访问周期	缓存命中：0等待 CacheMiss:Flash等待周期寄存器的等待数

Table 43.7 闪存2(FCACHE2)概述

缓存目标区域	0x0000_0000 - 0x007F_FFFF
目标总线主控	CPU操作数访问
Capacity	16 Bytes
Associativity	全联想
	128位条目（128位对齐数据），1个条目
访问周期	缓存命中：0等待 CacheMiss:Flash等待周期寄存器的等待数

Table 43.8 预取缓冲区(FLPF)概述

缓存目标区域	0x0000_0000 - 0x007F_FFFF
Capacity	32 Bytes
Associativity	全联想
	128位条目（128位对齐数据），2个条目
请求地址	上一条CPU指令的下一个地址
访问周期	缓存命中：0等待 CacheMiss:Flash等待周期寄存器的等待数

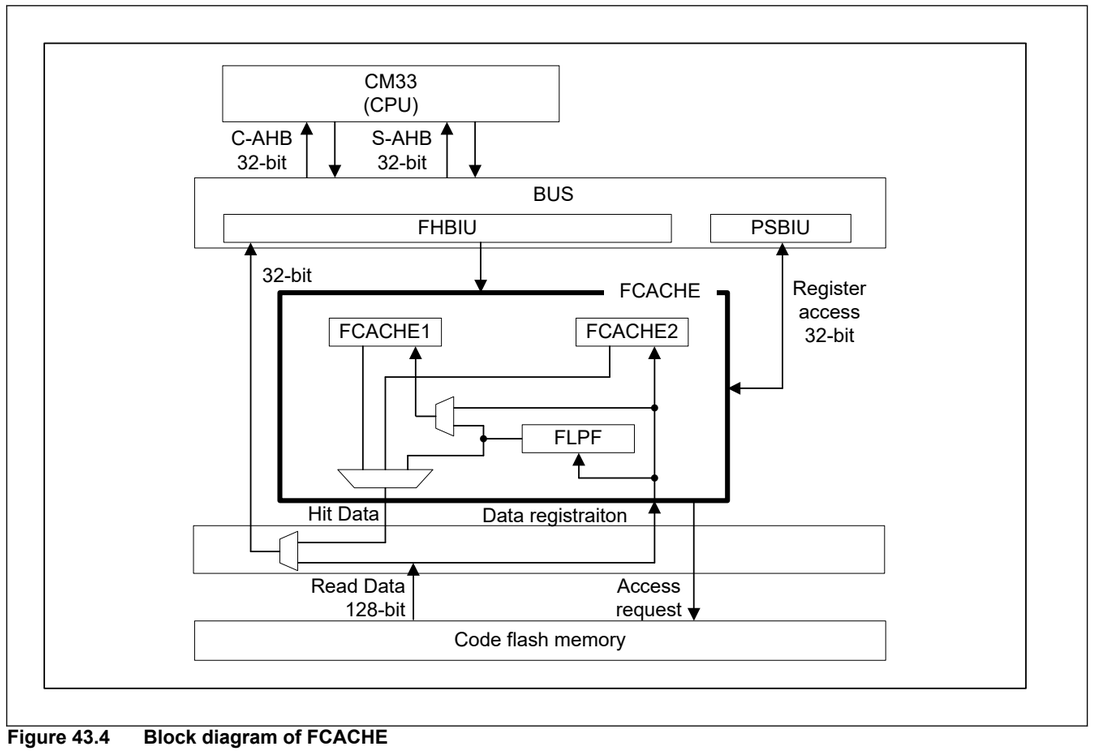


Figure 43.4 Block diagram of FCACHE

43.6 Operating Modes Associated with Flash Memory

Figure 43.5 is a diagram of the mode transitions associated with the flash memory. For the procedures for setting the modes, see section 6, Option-Setting Memory.

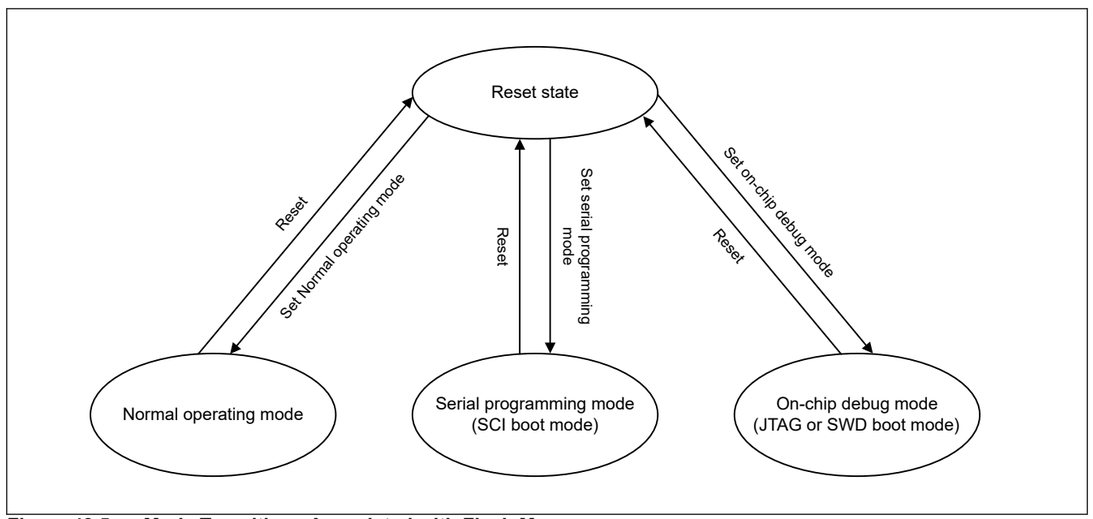


Figure 43.5 Mode Transitions Associated with Flash Memory

The flash memory area where programming and erasure are permitted and the boot program after a reset are different according to each mode. The differences between modes are listed in Table 43.9.

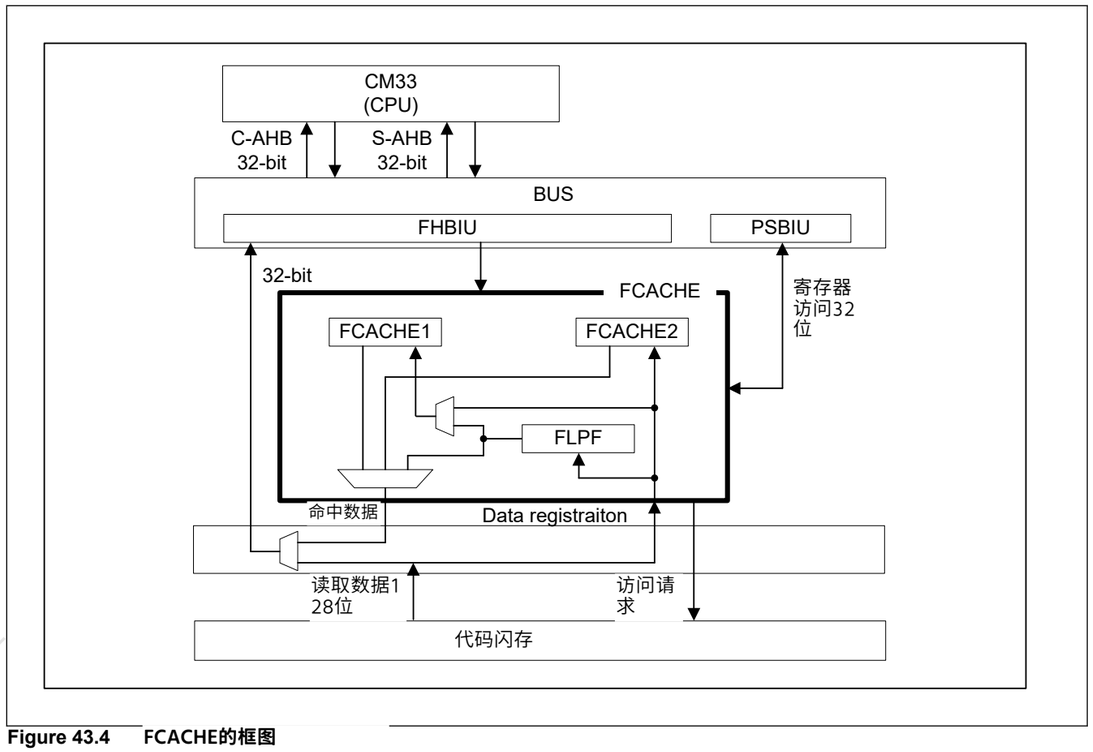


Figure 43.4 FCACHE的框图

43.6 与闪存相关的操作模式

图43.5是与闪存相关的模式转换图。有关设置模式的步骤，请参阅第6节，选项设置内存。

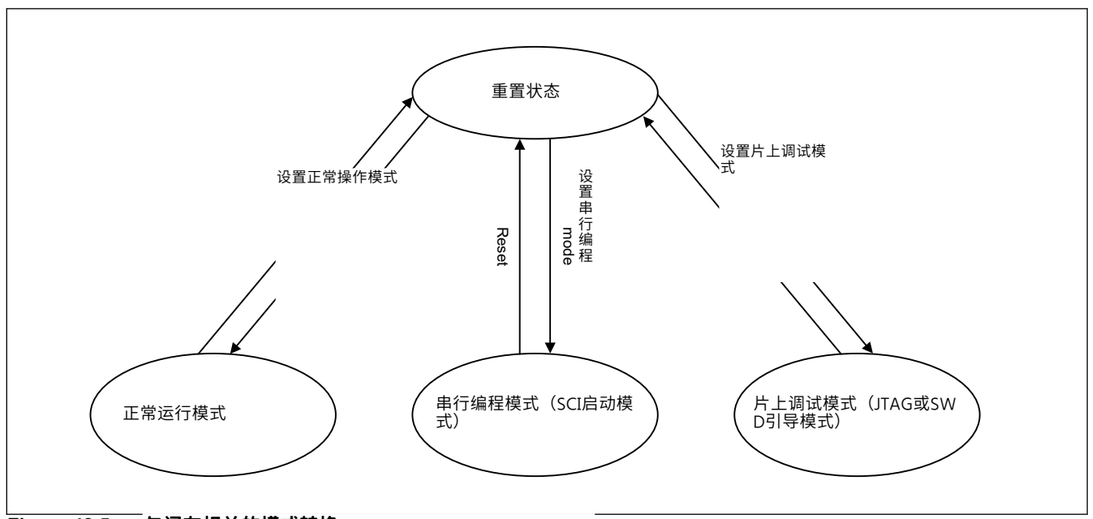


Figure 43.5 与闪存相关的模式转换

允许编程和擦除的闪存区域和复位后的引导程序根据每种模式而不同。模式之间的差异在表43.9中列出。

Table 43.9 Differences between Modes

Parameter	Normal operating mode	Serial programming mode (SCI boot mode)	On-chip debug mode (JTAG or SWD boot mode)
Programmable and erasable areas	• Code flash memory • Data flash memory • Option setting memory (programming only)	• Code flash memory • Data flash memory • Option-setting memory (programming only)	• Code flash memory • Data flash memory • Option setting memory (programming only)
Erasure in block units	Possible	Possible	Possible
Boot program at a reset	User area program	Embedded program for serial programming	Depends on debug command

43.7 Overview of Functions

By using a dedicated flash-memory programmer to program the flash memory through a serial interface (serial programming) or JTAG/SWD interface (on-chip debug mode), the device can be rewritten regardless of whether this is before or after it is mounted on the target system.

Furthermore, security functions to prohibit rewriting or reading of the user program written to the flash memory are incorporated, and this can prevent falsification and illicit reading of the programs by third parties.

Programming by the user program (self-programming) is available to suit applications where the application on the target system may require updating after manufacturing or shipment. Protection features for the safe rewriting of the flash memory are also incorporated. Furthermore, interrupt processing during self-programming is supported, so programming can proceed at the same time as processing for external communications, etc., and this is the case in various situations. Table 43.10 lists the overview of the methods of programming and the corresponding operating modes.

Table 43.10 Programming methods

Programming method	Functional overview	Operating mode
Serial programming	A dedicated flash-memory programmer through the SCI interface enables on-board programming of the flash memory after the device is mounted on the target system.	Serial programming mode
	A dedicated flash-memory programmer through the SCI interface and a dedicated programming adapter board allow off-board programming of the flash memory, for example, programming of the device before it is mounted on the target system.	
Self-programming	A user program written to memory in advance of serial programming execution can also program the flash memory. The background operation capability makes it possible to fetch instructions or otherwise read data from the code flash memory while the data flash memory is programmed. As a result, a program resident in the code flash memory is able to program the data flash memory. For background operations that are not possible, instructions in the code flash memory cannot be fetched and data cannot be accessed while the code flash memory is being programmed by self-programming. In such cases, a program for programming from the internal SRAM must be transferred in advance and executed.	Normal operating mode
JTAG or SWD programming	A dedicated flash-memory programmer or an on-chip debugger through JTAG or SWD enables on-board programming of the flash memory after the device is mounted on the target system. A dedicated flash-memory programmer or an on-chip debugger through JTAG or SWD and a dedicated programming adapter board allow off-board programming of the flash memory, for example, programming of the device before it is mounted on the target system.	On-chip debug mode

Table 43.11 lists the functions of the flash memory. Serial programmer commands realize each function of serial programming, while reading of the flash memory by an FACI command or the user program realizes each function of self-programming.

Table 43.9 模式之间的差异

Parameter	正常运行模式	串行编程模式（SCI启动模式）	片上调试模式（JTAG或SWD引导模式）
可编程和可擦除区域	• 代码闪存 • 数据闪存 • 选项设置内存（仅编程）	• 代码闪存 • 数据闪存 • Option-setting memory (programming only)	• 代码闪存 • 数据闪存 • 选项设置内存（仅编程）
以块为单位擦除	Possible	Possible	Possible
复位时的引导程序	用户区程序	用于串行编程的嵌入式程序	取决于调试命令

43.7 功能概述

通过使用专用闪存编程器通过串行接口（串行编程）或JTAGSWD接口（片上调试模式）对闪存进行编程，无论是在安装之前还是之后，都可以重写设备目标系统。

此外，内置了禁止重写或读取写入闪存的用户程序的安全功能，这可以防止第三方篡改和非法读取程序。

用户程序编程（自编程）适用于目标系统上的应用程序在制造或发货后可能需要更新的应用程序。还集成了用于安全重写闪存的保护功能。此外，支持自编程期间的中断处理，因此可以与外部通信处理等同时进行编程，这在各种情况下都是如此。表43.10列出了编程方法和相应操作模式的概述。

Table 43.10 编程方法

编程方法	功能概览	操作模式
串行编程	通过SCI接口的专用闪存编程器可在器件安装到目标系统后对闪存进行板载编程。	串行编程模式
	通过SCI接口的专用闪存编程器和专用编程适配板允许对闪存进行板外编程，例如，在器件安装到目标系统之前对其进行编程。	
Self-programming	在串行编程执行之前写入存储器的用户程序也可以对闪存进行编程。后台操作能力使得在对数据闪存进行编程时，可以从代码闪存中获取指令或以其他方式读取数据。结果，驻留在代码闪存中的程序能够对数据闪存进行编程。对于无法进行的后台操作，在自编程对代码闪存进行编程时，无法获取代码闪存中的指令并且无法访问数据。在这种情况下，必须提前传输并执行内部SRAM的编程程序。	正常运行模式
JTAG或SWD编程	专用闪存编程器或通过JTAG或SWD的片上调试器可在器件安装到目标系统后对闪存进行板载编程。专用闪存编程器或片上调试器通过 JTAG或SWD和专用编程适配器板允许对闪存进行板外编程，例如，在将器件安装到目标系统之前对其进行编程。	片上调试模式

表43.11列出了闪存的功能。串行编程器命令实现串行编程的各个功能，而通过FACI命令或用户程序读取闪存实现自编程的各个功能。

Table 43.11 Basic Functions

Function	Functional overview	Availability	
		Serial programming	Self-programming
Blank check	Checks a specified block to ensure that writing to it has not already proceeded. Results of reading from data flash memory to which nothing is written after erasure are not guaranteed, so use blank checking to confirm that writing to memory has not proceeded after erasure.	Not supported	Supported (data flash programming only)
Block erasure	Erases the memory contents in the specified block	Supported	Supported
Programming	Writes to the specified address	Supported	Supported
CRC	Calculates the CRC in the specified range of the flash memory and transfers it to the flash programmer	Supported	Non supported
Read	Reads data programmed in the flash memory	Supported	Not supported (read by user program is possible)
Start-up program protection functions	Configures the start-up program protection functions	Supported	Supported
Option function selection	Selects the option function, and modifies the initial setting of this MCU	Supported	Supported
Block protection	Setting block protection	Supported	Supported
Device lifecycle transition	Transitions the device lifecycle	Supported	Not supported
Memory security attribution	Setting the memory security attribution	Supported	Not supported
Key	Injects key	Supported	Supported (except the key related to device lifecycle transition)
All erasure	Erase the flash memory to the state after shipment	Supported	Not supported

The flash memory supports various security functions.

Table 43.12 lists the security functions supported by the flash memory.

Table 43.12 Lists of Security Functions

Function	Description
Security flag for Start-up area select	Start-up area selection can be protected by setting of security flag (FSPR).
Permanently block protection	Programming or erasure of each block of code flash memory can be protected permanently.
Protection for TrustZone	Programming or erasure area, readable area, register access, and FACI command operation are protected by ARM TrustZone security.
Programming or erasure mode protection	Only secure developer can enter the programming or erasure mode for code flash.

43.8 Operating Modes of the Flash Sequencer

The flash sequencer has three operating modes as shown in Figure 43.6. Transitions between modes are initiated by changing the value of the FENTRYR register.

When the value of the FENTRYR register is 0x0000, the flash sequencer is in read mode. In this mode, it does not receive FACI commands. The code flash memory and data flash memory are both readable.

When the value of the FENTRYR register is 0x0001, the flash sequencer is in code flash P/E mode where the code flash memory can be programmed or erased by FACI commands. In this mode, the data flash memory is readable.

When the value of the FENTRYR register is 0x0080, the flash sequencer is in data flash P/E mode where the data flash memory can be programmed or erased by FACI commands. In this mode, the data flash memory is not readable. However, the code flash memory is readable.

Table 43.11 基本功能

Function	功能概览	Availability	
		串行编程	自编程
空白支票	检查指定的块以确保尚未对其进行写入。无法保证从擦除后没有写入任何内容的数据闪存中读取的结果，因此使用空白检查来确认擦除后没有继续写入内存。	不支持	支持（仅数据闪存编程）
块擦除	擦除指定块中的内存内容	Supported	Supported
Programming	写入指定地址	Supported	Supported
CRC	计算flash存储器指定范围内的CRC，并传送给flash编程器	Supported	不支持
Read	读取闪存中编程的数据	Supported	不支持（可由用户程序读取）
启动程序保护功能	配置启动程序保护功能	Supported	Supported
选项功能选择	选择选项功能，修改本MCU的初始设置	Supported	Supported
块保护	设置块保护	Supported	Supported
设备生命周期过渡	过渡设备生命周期	Supported	不支持
内存安全归属	设置内存安全属性	Supported	不支持
Key	注入密钥	Supported	支持（设备生命周期转换相关的key除外）
全部擦除	擦除闪存到出货后的状态	Supported	不支持

闪存支持各种安全功能。

表43.12列出了闪存支持的安全功能。

Table 43.12 安全功能列表

Function	Description
启动区域选择的安全标志	启动区域选择可以通过设置安全标志(FSPR)来保护。
永久阻止保护	可以永久保护每个代码闪存块的编程或擦除。
保护TrustZone	编程或擦除区域、可读区域、寄存器访问和FACI命令操作受ARMTrustZone安全保护。
编程或擦除模式保护	只有安全的开发人员才能进入代码闪存的编程或擦除模式。

43.8 FlashSequencer的操作模式

闪存定序器具有三种操作模式，如图43.6所示。通过更改FENTRYR寄存器的值来启动模式之间的转换。

当FENTRYR寄存器的值为0x0000时，闪存定序器处于读取模式。在这种模式下，它不接收FACI命令。代码闪存和数据闪存都是可读的。

当FENTRYR寄存器的值为0x0001时，闪存定序器处于代码闪存PE模式，代码闪存可以通过FACI命令进行编程或擦除。在这种模式下，数据闪存是可读的。

当FENTRYR寄存器的值为0x0080时，闪存定序器处于数据闪存PE模式，可以通过FACI命令对数据闪存进行编程或擦除。在这种模式下，数据闪存是不可读的。但是，代码闪存是可读的。

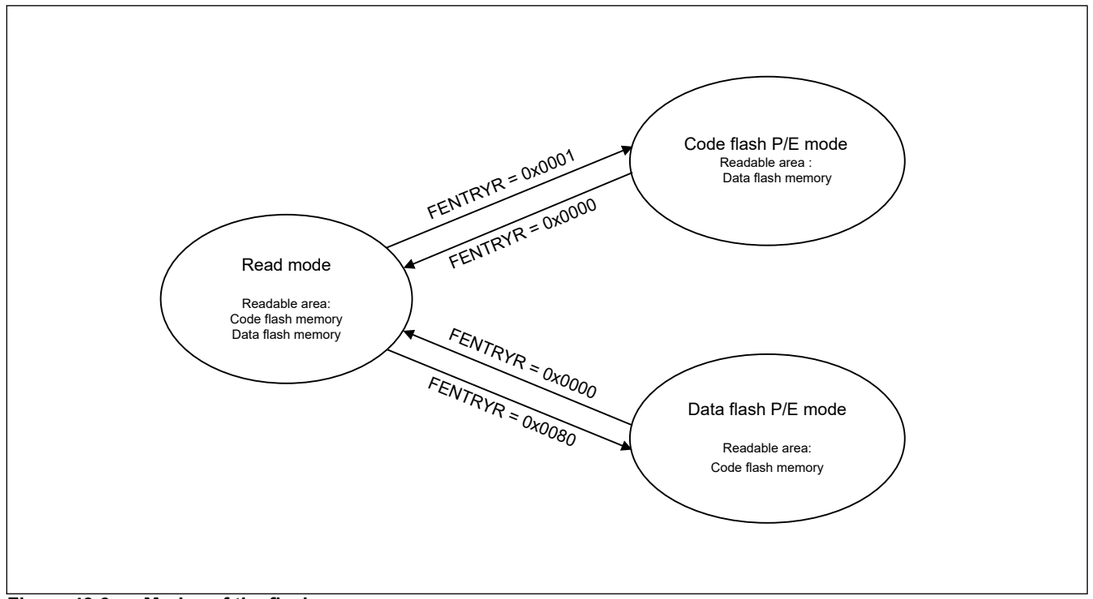


Figure 43.6 Modes of the flash sequencer

43.9 FACI Commands

43.9.1 List of FACI Commands

The FACI controls the FCU according to the specified FACI commands.

This section describes information about the FACI commands and Table 43.13 lists the FACI commands.

Table 43.13 FACI commands

FACI command	Function
Program	Programs the user area and data area. Units of programming are 128 bytes for the user area and 4, 8, or 16 bytes for the data area.
Block erase	Erases user area and data area. The erase unit is 8 KB or 32 KB for user area, and 64 bytes for data flash.
Multi block erase	Erases data area. The erase unit is 64, 128, 256 bytes for data flash.
P/E suspend	Suspends programming or erasure processing.
P/E resume	Resumes suspended programming or erasure processing.
Status clear	Initializes the ILGLERR, ERSERR, PRGERR, ILGCOMERR, FESETERR, SECERR, and OTERR bits in the FSTATR register and the CMDLK, CFAE, and DFAE bits in the FASTAT register, and the flash sequencer released from command-locked state.
Forced stop	Forcibly stops processing of FACI commands and initializes the FSTATR and FASTAT registers.
Blank check	Checks if data areas are blank. Units of Blank Check: 4 bytes to data flash memory capacity (specified in 4-byte units).
Configuration set	Sets the option-setting memory. Units of setting: 16 bytes.

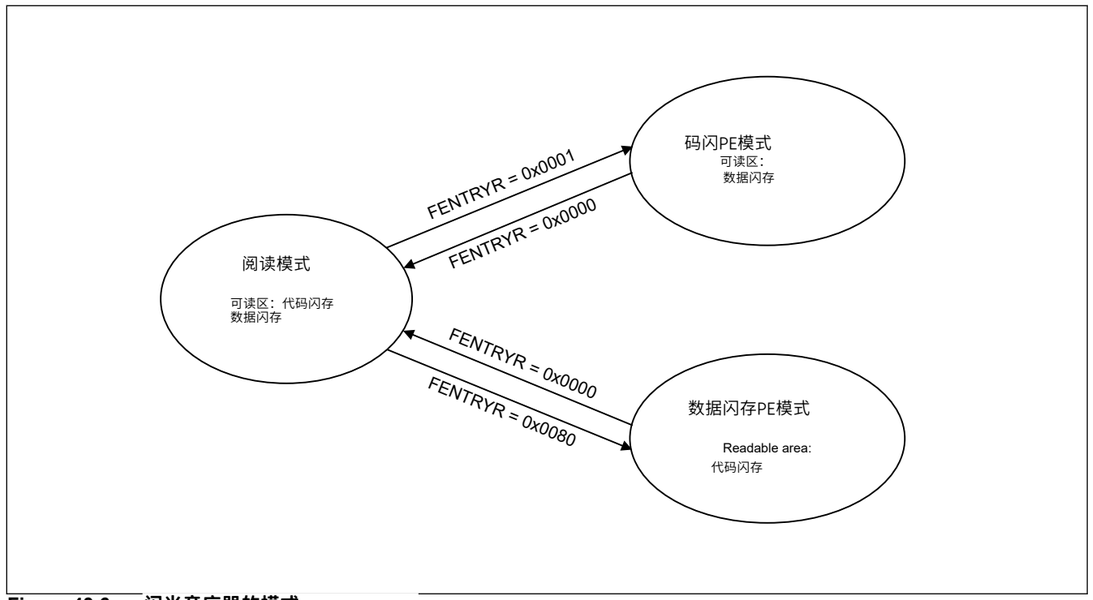


Figure 43.6 闪光音序器的模式

43.9 FACI命令

43.9.1 FACI命令列表

FACI根据指定的FACI命令控制FCU。

本节介绍有关FACI命令的信息，表43.13列出了FACI命令。

Table 43.13 FACI命令

FACI命令	Function
Program	对用户区和数据区进行编程。 用户区的编程单元为128字节，数据区为4、8或16字节。
块擦除	擦除用户区和数据区。 用户区的擦除单元为8KB或32KB，数据闪存为64字节。
多块擦除	擦除数据区。 数据闪存的擦除单元为64、128、256字节。
P/E suspend	暂停编程或擦除处理。
P/E resume	恢复暂停的编程或擦除处理。
状态清除	Initializes the ILGLERR, ERSERR, PRGERR, ILGCOMERR, FSTATR寄存器中的FESETERR、SECERR和OTERR位以及FASTAT寄存器中的CMDLK、CFAE和DFAE位，并且闪存定序器从命令锁定状态释放。
强制停止	强制停止处理FACI命令并初始化 FSTATR和FASTAT寄存器。
空白支票	检查数据区域是否为空白。 空白检查单位：4字节到数据闪存容量（以4字节为单位指定）。
配置集	设置选项设置内存。 设置单位：16字节。

The FACI commands are issued by writing to the FACI command-issuing area (see Table 43.3). When write access as shown in Table 43.14 proceeds in the specified state, the flash sequencer executes the processing associated with the given command (see section 43.9.2. Relationship between the Flash Sequencer State and FACI Commands).

Table 43.14 FACI command formats

FACI commands	Number of write access	Write data to the FACI command-issuing area			
		1st access	2nd access	3rd to (N+2)th access	(N+3)th access
Program (user area) N = 64	67	0xE8	0x40 (=N)	WD1 to WD64	0xD0
Program (data area) 4-byte programming: N = 2 8-byte programming: N = 4 16-byte programming: N = 8	N+3	0xE8	0x02 (=N) 0x04 (=N) 0x08 (=N)	WD1 to WDN	0xD0
Block Erase (user area 8K/32K Bytes)	2	0x20	0xD0	—	—
Block Erase (data area 64 bytes)	2	0x20	0xD0	—	—
Multi block erase (data area 64/128/256 bytes)	2	0x21	0xD0	—	—
P/E suspend	1	0xB0	—	—	—
P/E resume	1	0xD0	—	—	—
Status Clear	1	0x50	—	—	—
Forced Stop	1	0xB3	—	—	—
Blank Check	2	0x71	0xD0	—	—
Configuration set N = 8	11	0x40	0x08 (=N)	WD1 to WD8	0xD0

Note: WDN (N = 1, 2, …): Nth 16-bit data to be programmed.

The flash sequencer clears the FSTATR.FRDY bit to 0 at the start of a command processing other than the Status Clear command, and sets this bit to 1 on completion.

If the FRDYIE.FRDYIE bit setting is 1, a flash ready (FRDY) interrupt is generated when the FSTATR.FRDY bit is set to 1.

43.9.2 Relationship between the Flash Sequencer State and FACI Commands

The FACI commands are accepted according to the mode/state of the flash sequencer. FACI commands should be issued after transitioning of the flash sequencer to the code flash P/E mode or data flash P/E mode and after checking the state of the flash sequencer.

Use the FSTATR and FASTAT registers to check the state of the flash sequencer. In addition, the occurrence of errors in general can be checked by reading the CMDLK bit in the FASTAT register. The value of the CMDLK bit is the logical OR of the following bits in the FSTATR register:

- ILGLERR
- ILGCOMERR
- FESETERR
- SECERR
- OTERR
- ERSERR
- PRGERR
- FLWEERR.

Table 43.15 lists the available FACI commands in each operating mode.

FACI命令通过写入FACI命令发布区域来发布（参见表43.3）。当表43.14所示的写访问在指定状态下进行时，闪存定序器执行与给定命令相关的处理（请参阅第43.9.2节。闪存定序器状态和FACI命令之间的关系）。

Table 43.14 FACI命令格式

FACI命令	写访问次数	将数据写入FACI命令发布区			
		1st access	2nd access	第3次到第(N+2)次访问	(N+3)th access
Program (user area) N = 64	67	0xE8	0x40 (=N)	WD1 to WD64	0xD0
Program (data area) 4-byte programming: N = 2 8-byte programming: N = 4 16-byte programming: N = 8	N+3	0xE8	0x02 (=N) 0x04 (=N) 0x08 (=N)	WD1 to WDN	0xD0
块擦除（用户区8K32K字节）	2	0x20	0xD0	—	—
块擦除（数据区64字节）	2	0x20	0xD0	—	—
多块擦除（数据区64128256字节）	2	0x21	0xD0	—	—
P/E suspend	1	0xB0	—	—	—
P/E resume	1	0xD0	—	—	—
状态清除	1	0x50	—	—	—
强制停止	1	0xB3	—	—	—
空白支票	2	0x71	0xD0	—	—
配置集 N = 8	11	0x40	0x08 (=N)	WD1 to WD8	0xD0

Note: WDN(N=1 2 …)：要编程的第N个16位数据。

闪存定序器在除状态清除命令之外的命令处理开始时将FSTATR.FRDY位清除为0，并在完成时将此位设置为1。

如果FRDYIE.FRDYIE位设置为1，则当FSTATR.FRDY位设置为1时会产生闪存就绪(FRDY)中断。

43.9.2 FlashSequencerState和FACI命令之间的关系

根据闪存定序器的模式状态接受FACI命令。FACI命令应在闪存定序器转换到代码闪存PE模式或数据闪存PE模式并检查闪存定序器的状态之后发出。

使用FSTATR和FASTAT寄存器检查闪存序列器的状态。此外，一般可以通过读取FASTAT寄存器中的CMDLK位来检查错误的发生。CMDLK位的值是FSTATR寄存器中以下位的逻辑或：

- ILGLERR
- ILGCOMERR
- FESETERR
- SECERR
- OTERR
- ERSERR
- PRGERR
- FLWEERR.

表43.15列出了每种操作模式下可用的FACI命令。

Table 43.15 Operating mode and available FACI commands

Operating mode	FENTRYR	Available FACI commands
Read mode	0x0000	None
Code flash P/E mode	0x0001	Program Block erase P/E suspend P/E resume Status Clear Forced Stop Configuration set
Data flash P/E mode	0x0080	Program Block erase Multi block erase P/E suspend P/E resume Status Clear Forced Stop Blank Check

Table 43.16 shows the state of the flash sequencer and acceptable FACI commands. An appropriate mode is assumed to have been set before the commands are executed.

Table 43.16 Acceptable FACI commands and state of the flash sequencer

	Program, block erase or multi block erase command processing	Configuration set command processing	Program, block erase or multi block erase command suspension processing	Blank check command processing	Programming suspended	Erasure suspended	Programming while erasure is suspended	Command-locked state (FRDY = 1)	Command-locked state (FRDY = 0)	Processing of forced stop command	Other state
FRDY bit	0	0	0	0	1	1	0	1	0	0	1
SUSRDY bit	1	0	0	0	0	0	0	0	0	0	0
ERSSPD bit	0	0	0/1	0/1	0	1	1	0/1	0/1	0	0
PRGSPD bit	0	0	0/1	0/1	1	0	0	0/1	0/1	0	0
CMDLK bit	0	0	0	0	0	0	0	1	1	0	0
Program	X	X*4	X	X	X	O*3	X	X	X	X	O
Block erase or multi block erase	X	X*4	X	X	X	X	X	X	X	X	O
P/E suspend	O	X*4	X	X	X	X	X	—	X	X	—
P/E resume	X	X*4	X	X	O	O	X	X	X	X	X
Status clear	X	X*4	X	X	O	O	X	O	X	X	O
Forced stop	O	O*4	O	O	O	O	O	O	O	O	O
Blank check	X	X*4	X	X	O*1	O*1	X	X	X	X	O*1
Configuration set	X	X*4	X	X	X	X	X	X	X	X	O*2

Note: O: Acceptable
X: Not acceptable (places the sequencer in the command-locked state)

Table 43.15 操作模式和可用的FACI命令

操作模式	FENTRYR	可用的FACI命令
阅读模式	0x0000	None
码闪PE模式	0x0001	Program 块擦除PE暂 停PE恢复状 态清除强制 停止 配置集
数据闪存PE模式	0x0080	Program 块擦除多块擦除 PE暂停PE恢 复状态清除 强制停止空 白检查

表43.16显示了闪存定序器的状态和可接受的FACI命令。假设在执行命令之前已经设置了适当的模式。

Table 43.16 可接受的FACI命令和闪存定序器的状态

	编程、块擦除或多块擦除命令处理	配置集命令处理	编程、块擦除或多块擦除命令暂停处理	空白检查命令处理	编程暂停	擦除暂停	擦除暂停时编程	Command-locked state (FRDY = 1)	Command-locked state (FRDY = 0)	强制停止指令的处理	其他状态
FRDY bit	0	0	0	0	1	1	0	1	0	0	1
SUSRDY bit	1	0	0	0	0	0	0	0	0	0	0
ERSSPD bit	0	0	0/1	0/1	0	1	1	0/1	0/1	0	0
PRGSPD bit	0	0	0/1	0/1	1	0	0	0/1	0/1	0	0
CMDLK bit	0	0	0	0	0	0	0	1	1	0	0
Program	X	X*4	X	X	X	O*3	X	X	X	X	O
块擦除或多块擦除	X	X*4	X	X	X	X	X	X	X	X	O
P/E suspend	O	X*4	X	X	X	X	X	—	X	X	—
P/E resume	X	X*4	X	X	O	O	X	X	X	X	X
状态清除	X	X*4	X	X	O	O	X	O	X	X	O
强制停止	O	O*4	O	O	O	O	O	O	O	O	O
空白支票	X	X*4	X	X	O*1	O*1	X	X	X	X	O*1
配置集	X	X*4	X	X	X	X	X	X	X	X	O*2

Note: O: Acceptable
X：不可接受（将定序器置于命令锁定状态）

—: Ignored
Note 1. Only acceptable in data flash P/E mode.
Note 2. Only acceptable in code flash P/E mode
Note 3. Acceptable when programming area is other than erase suspending block.
Note 4. When configuration set is processing and when FSTATR.DBFULL bit is 1, do not issue this command.

43.9.3 Usage of FACI Commands

43.9.3.1 Overview of Command Usage in Code Flash P/E Mode

Figure 43.7 show an overview of FACI command usage in code flash P/E mode. For the available commands in code flash P/E mode, see Table 43.15.

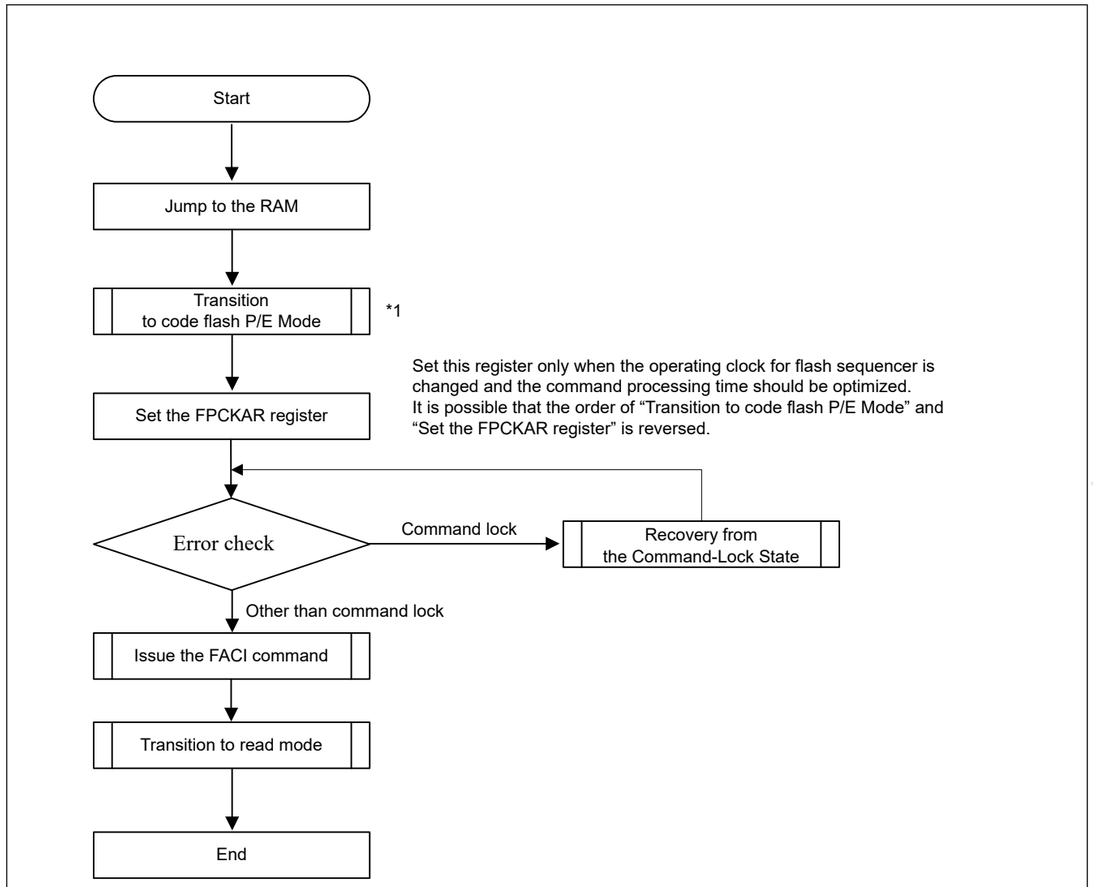


Figure 43.7 Overview of command usage in code flash P/E mode

43.9.3.2 Overview of Command Usage in Data Flash P/E Mode

Figure 43.8 shows an overview of FACI command usage in data flash P/E and Table 43.15 lists the available commands in data flash P/E mode.

—: Ignored
注1.仅在数据闪存PE模式下可接受。注2.仅在代码闪存PE模式下可接受
注3.当编程区域不是擦除暂停块时可接受。
注4.当配置集正在处理并且FSTATR.DBFULL位为1时，不要发出此命令。

43.9.3 FACI命令的使用

43.9.3.1 CodeFlashPE模式中的命令使用概述

图43.7显示了代码闪存PE模式下的FACI命令使用概览。对于代码闪存中的可用命令PE模式，见表43.15。

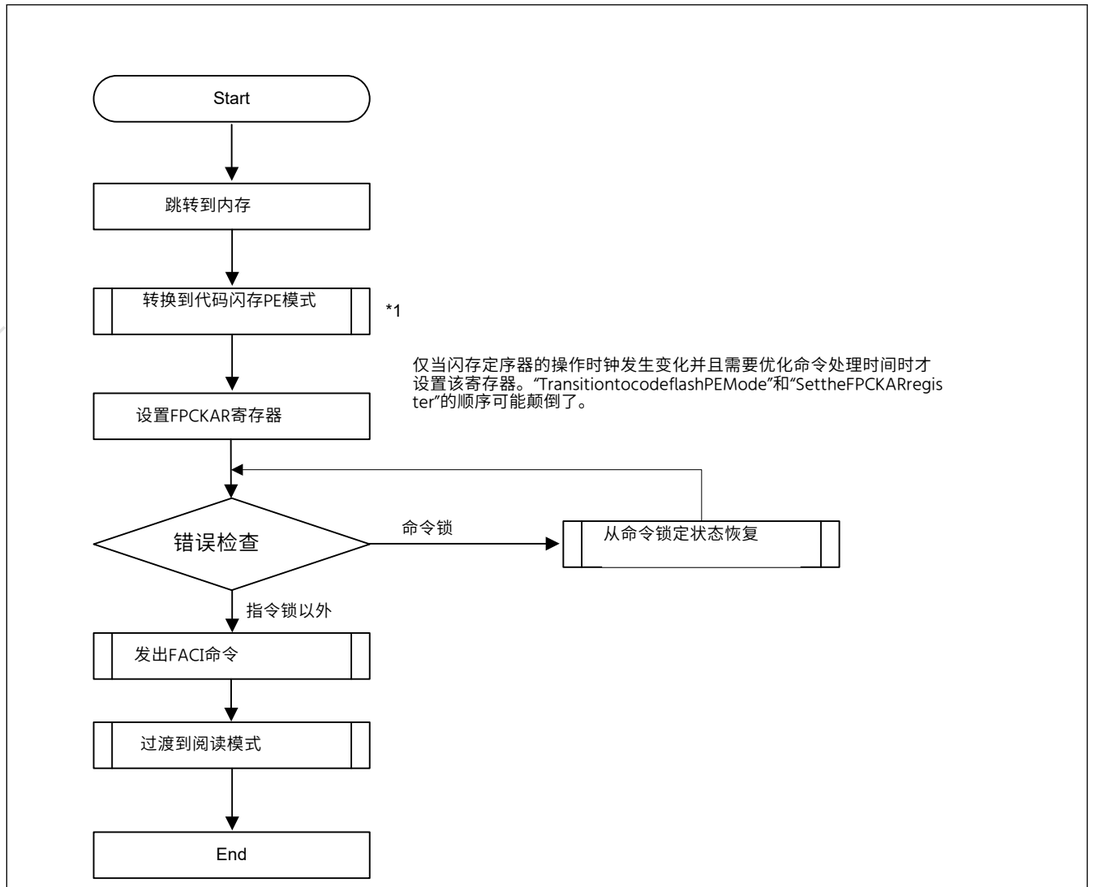


Figure 43.7 CodeflashPE模式下的命令使用概述

43.9.3.2 DataFlashPE模式下的命令使用概述

图43.8显示了数据闪存PE中FACI命令使用的概述，表43.15列出了数据闪存PE模式下的可用命令。

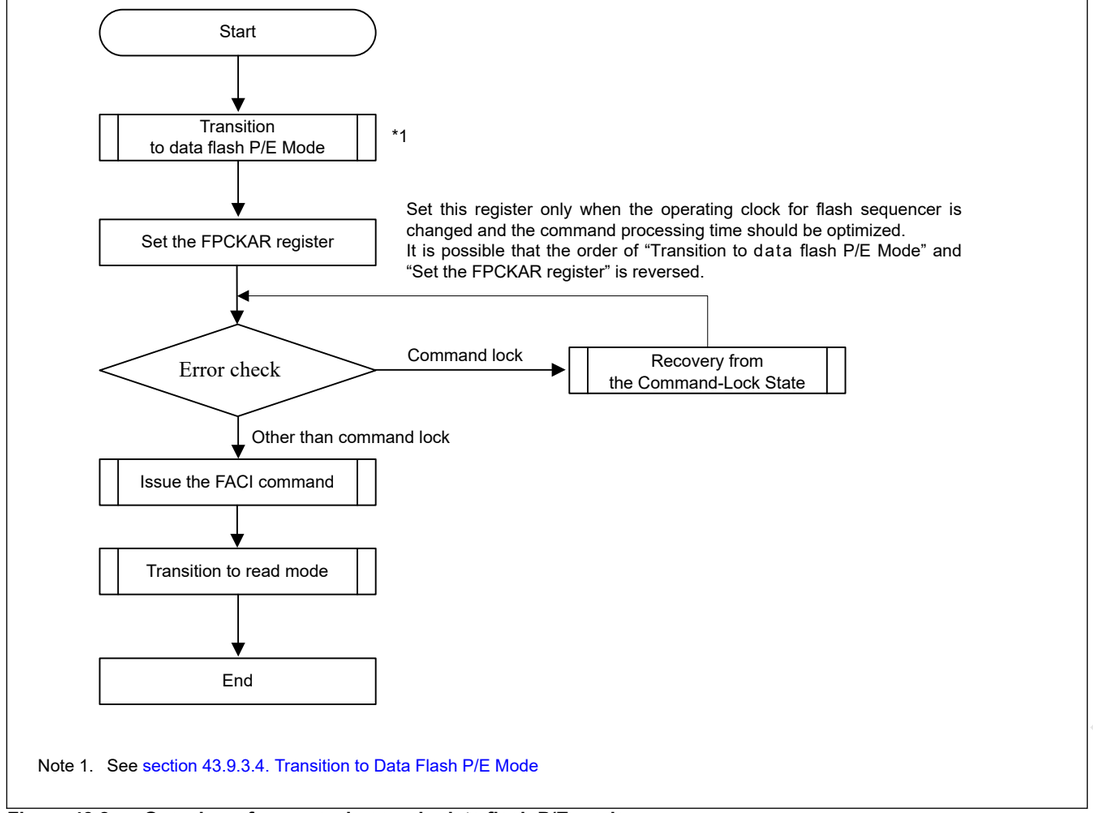


Figure 43.8 Overview of command usage in data flash P/E mode

43.9.3.3 Transition to Code Flash P/E Mode

To issue FACI commands for the code flash memory, a transition to code flash P/E mode is required by setting the FENTRYC bit in the FENTRYR register to 1.

Figure 43.9 shows the procedure to transition to code flash P/E mode.

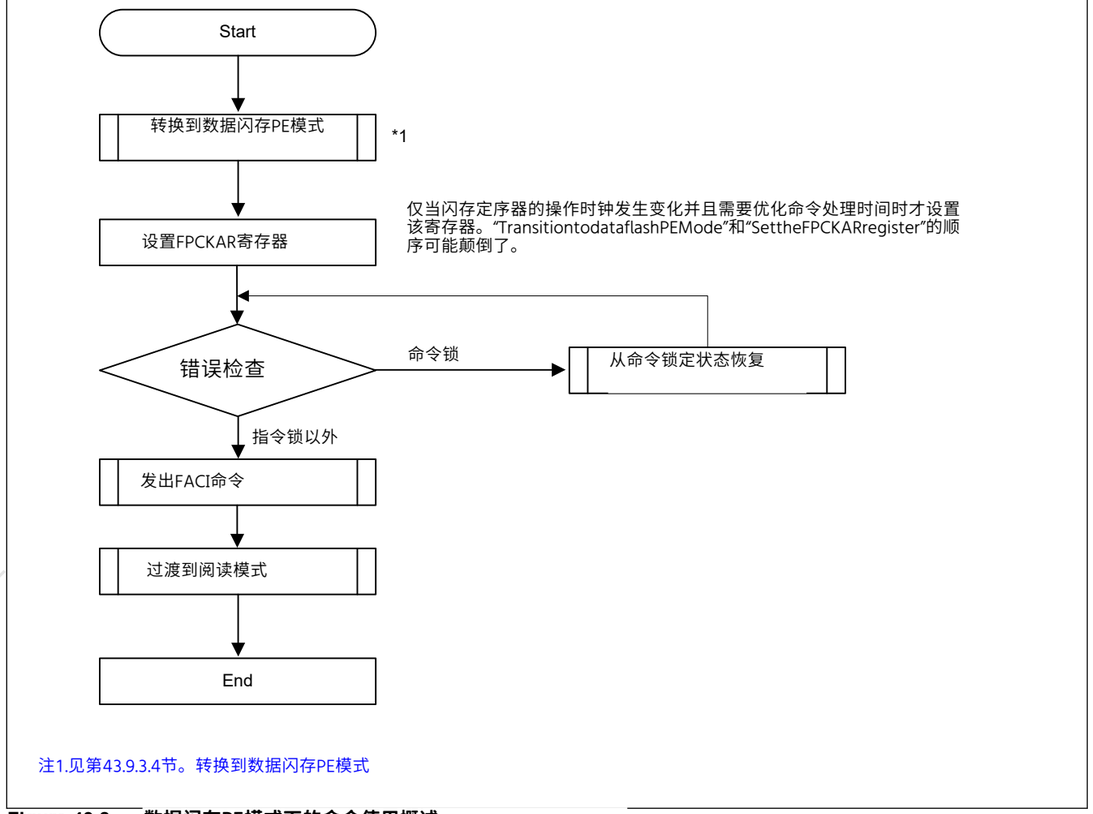


Figure 43.8 数据闪存PE模式下的命令使用概述

43.9.3.3 转换到CodeFlashPE模式

要为代码闪存发出FACI命令，需要通过设置FENTRYR寄存器中的FENTRYC位为1。

图43.9显示了转换到代码闪存PE模式的过程。

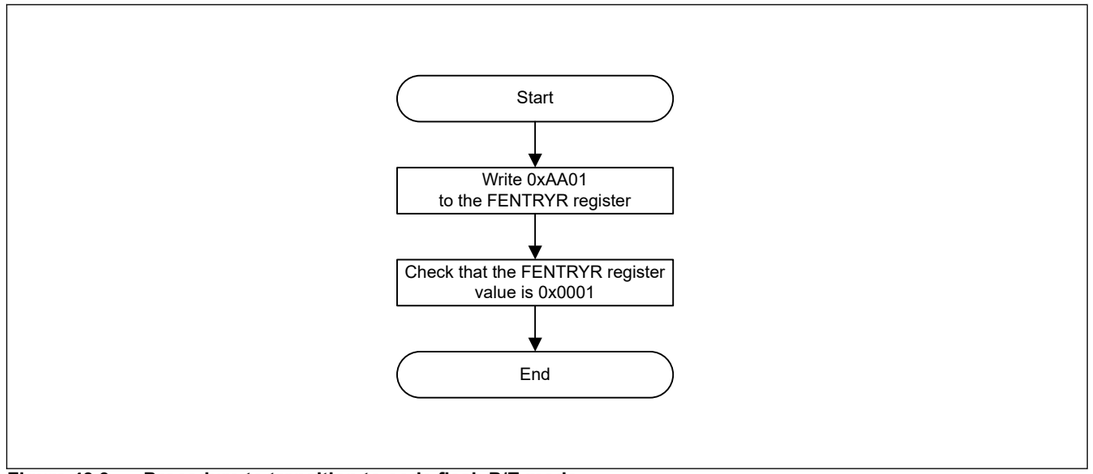


Figure 43.9 Procedure to transition to code flash P/E mode

43.9.3.4 Transition to Data Flash P/E Mode

To issue FACI commands for the data flash memory, a transition to data flash P/E mode is required by setting the FENTRYD bit in the FENTRYR register to 1.

Figure 43.10 shows the procedure to transition to data flash P/E mode.

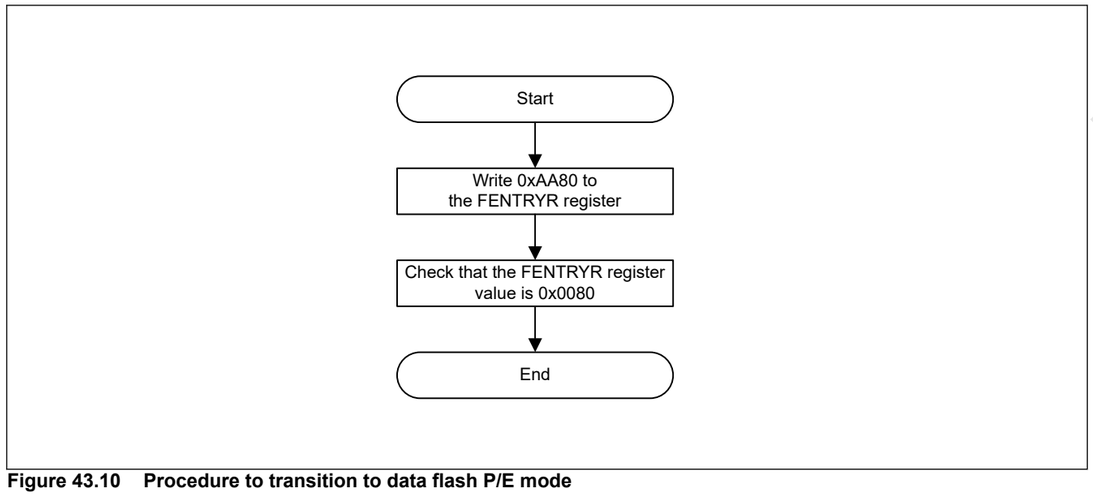


Figure 43.10 Procedure to transition to data flash P/E mode

43.9.3.5 Transition to Read Mode

To read the flash memory, a transition to read mode is required by setting the FENTRYR register to 0x0000. The transition to read mode should be made after the flash sequencer completes the processing and while operation is not in the command-locked state.

Figure 43.11 shows the procedure to transition to read mode.

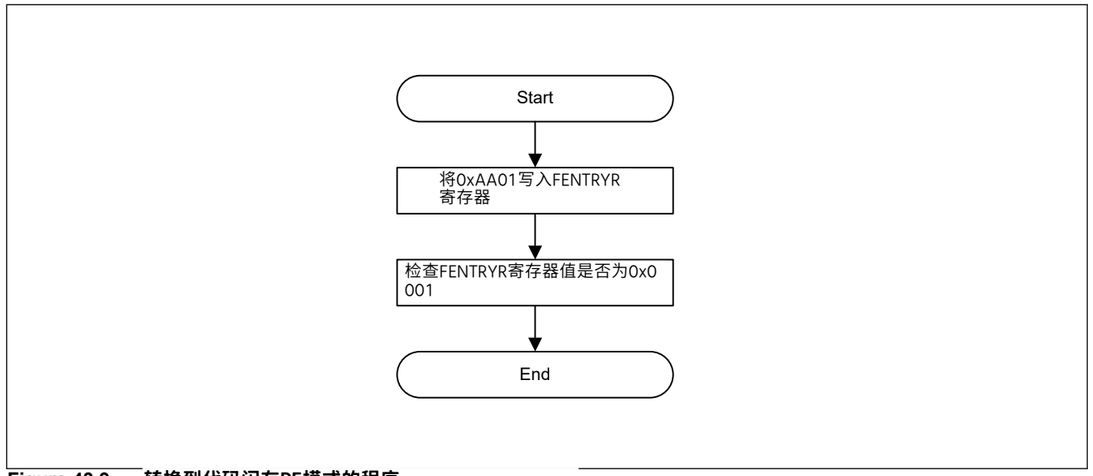


Figure 43.9 转换到代码闪存PE模式的程序

43.9.3.4 转换到数据闪存PE模式

要为数据闪存发出FACI命令，需要通过设置FENTRYR寄存器中的FENTRYD位为1。

图43.10显示了转换到数据闪存PE模式的过程。

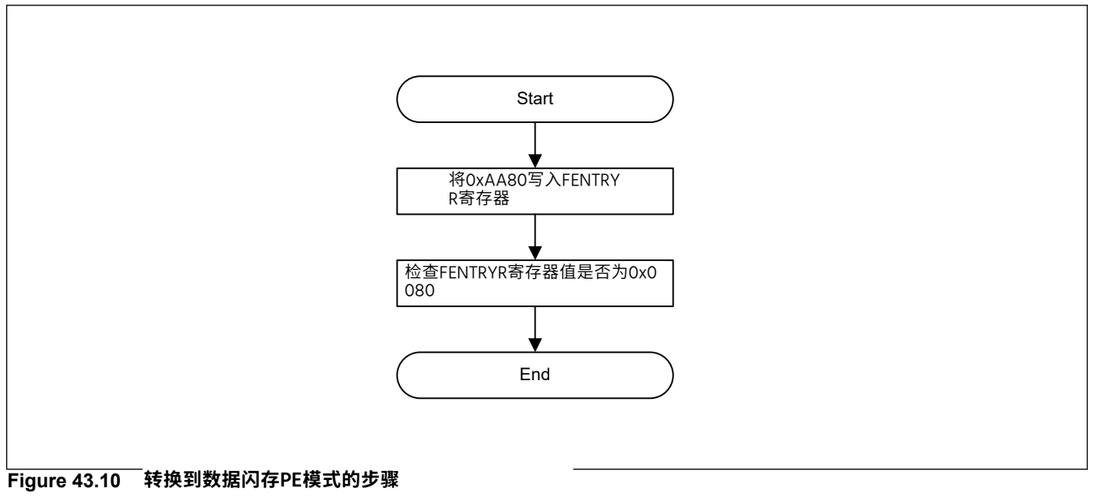
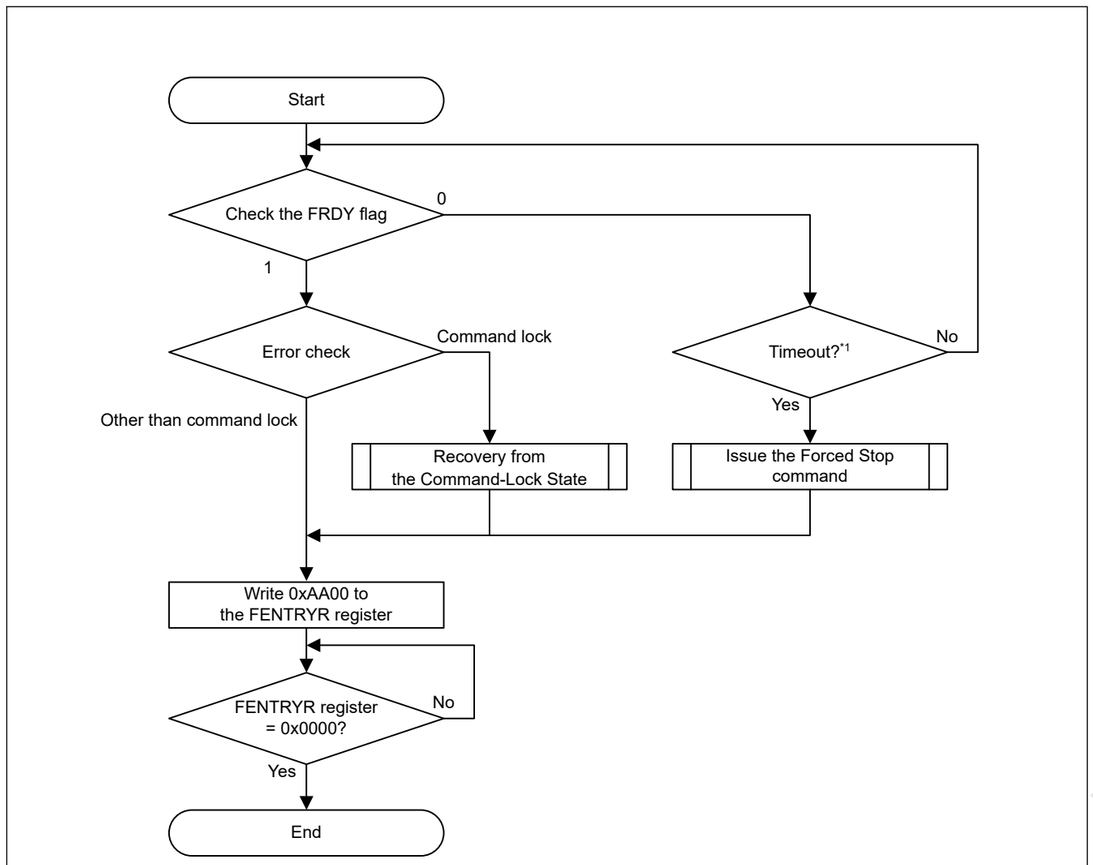


Figure 43.10 转换到数据闪存PE模式的步骤

43.9.3.5 过渡到阅读模式

要读取闪存，需要通过将FENTRYR寄存器设置为0x0000转换到读取模式。闪存定序器完成处理后且操作未处于命令锁定状态时，应转换到读取模式。

图43.11显示了转换到读取模式的过程。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for processing of the FACI command that is in progress (see section 46, Electrical Characteristics)

Figure 43.11 Procedure to transition to read mode

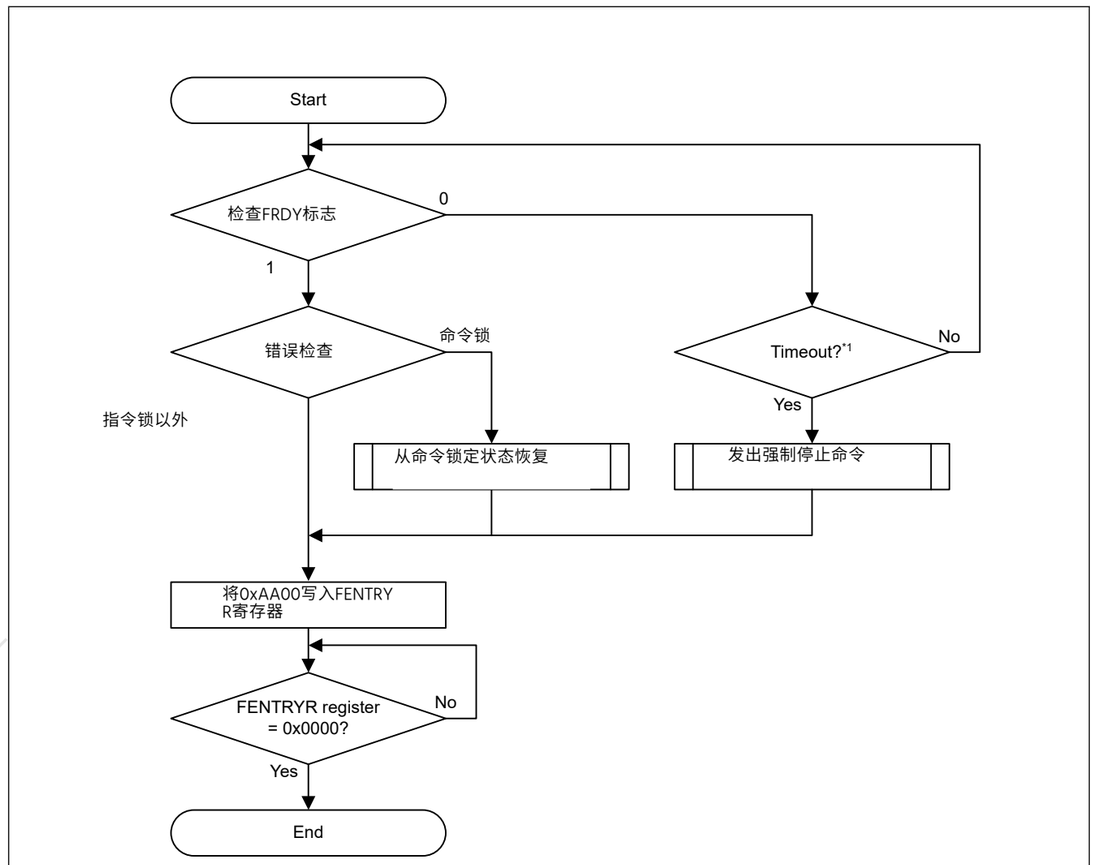
43.9.3.6 Recovery from the Command-Locked State

When the flash sequencer enters the command-locked state, FACI commands cannot be accepted. To release the sequencer from the command-locked state, use the status clear command, forced stop command, or FASTAT register.

When the command-locked state is detected by checking for an error before issuing the P/E suspend command, the FRDY bit in the FSTATR register might be 0 even though command processing has not completed. If processing is not complete by the maximum programming/erasure time specified in the electrical characteristics, this is a timeout and the flash sequencer must be stopped with the forced stop command.

The FLWEERR bit in the FSTATR register does not change from 1 to 0 with the status clear command. When these bits are set to 1, use the forced stop command to release from the command-locked state. Bits other than FRDY and FLWEERR in FSTATR register that indicate the command-locked state can be changed from 1 to 0 with the status clear or forced stop command.

Figure 43.12 shows the recovery flow from the command-locked state.



注1.超时的判断是基于1.1倍的FACI命令处理正在进行的最长时间（见第46节，电气特性）

Figure 43.11 转换到阅读模式的过程

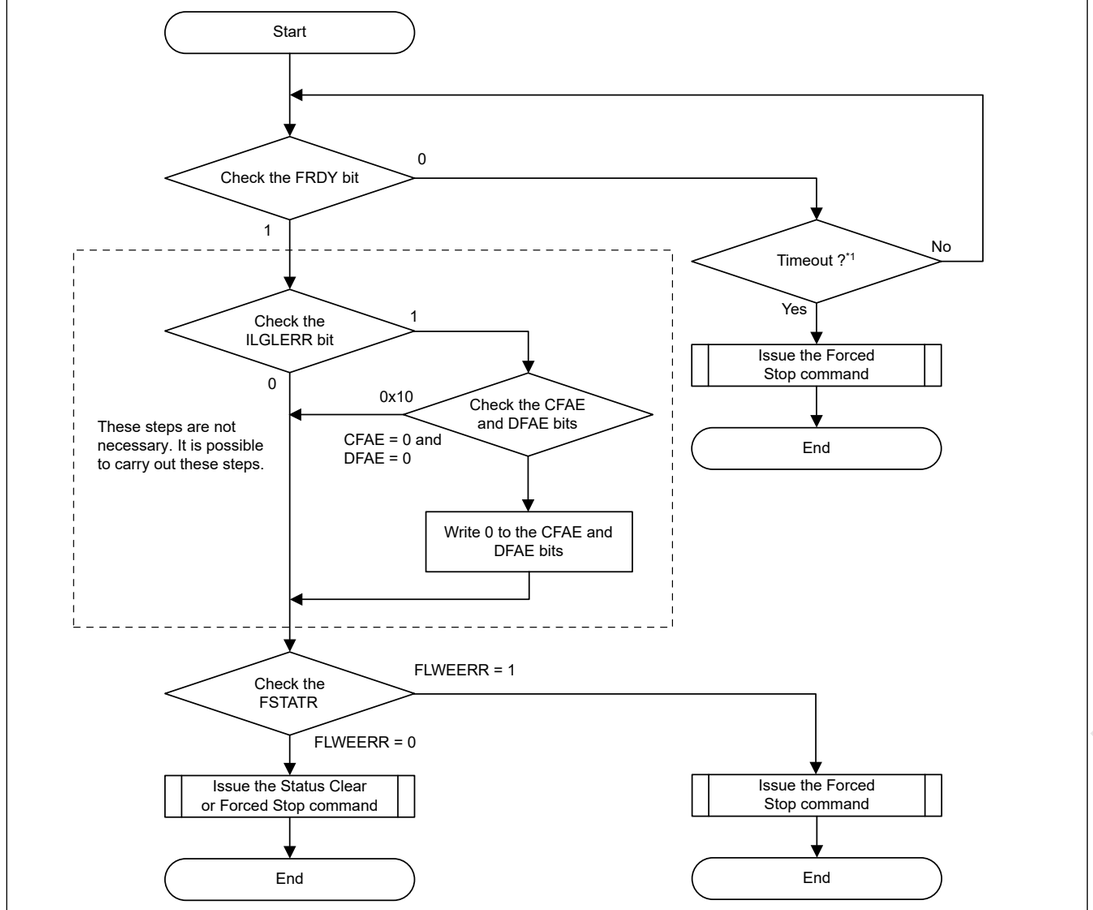
43.9.3.6 从命令锁定状态恢复

当闪存定序器进入命令锁定状态时，无法接受FACI命令。要从命令锁定状态释放定序器，请使用状态清除命令、强制停止命令或FASTAT寄存器。

当通过在发出PE挂起命令之前检查错误来检测命令锁定状态时，即使命令处理尚未完成，FSTATR寄存器中的FRDY位也可能为0。如果在电气特性中指定的最大编程擦除时间未完成处理，则这是一个超时，并且必须使用强制停止命令停止闪存定序器。

FSTATR寄存器中的FLWEERR位不会随着状态清除命令从1变为0。当这些位设置为1时，使用强制停止命令从命令锁定状态中释放。FSTATR寄存器中除FRDY和FLWEERR以外的位指示命令锁定状态可以通过状态清除或强制停止命令从1更改为0。

图43.12显示了从命令锁定状态的恢复流程。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for processing of the FACI command that is in progress (see section 46, Electrical Characteristics)

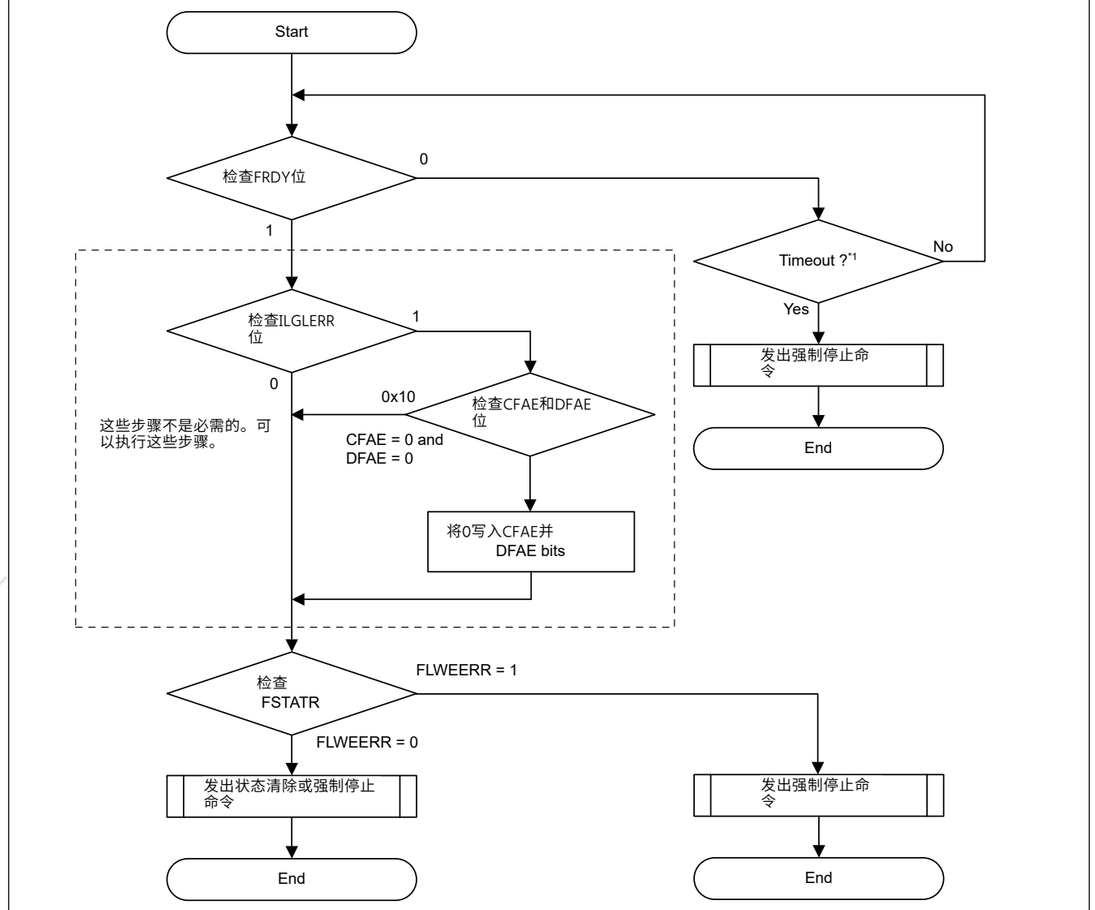
Figure 43.12 Recovery flow from the command-locked state

43.9.3.7 Program Command

The program command is used for writing to the user area and data area. Before issuing the FACI program command, set the first address of the target block in the FSADDR register. Writing 0xD0 at the final access of the FACI command-issuing area starts the program command processing. If the target area of program command processing contains area that are not for writing, write 0xFFFF to the corresponding area.

Issuing the program command while the FACI internal data buffer is full leads to a wait on the peripheral bus that might affect communications performance of other peripheral modules. To avoid a wait, set the DBFULL bit in the FSTATR register to 0 when issuing the FACI command. Writing to the data area does not lead to the data buffer becoming full.

Figure 43.13 shows the usage of the program command.



注1.超时的判断是基于1.1倍的FACI命令处理正在进行的最长时间（见第46节，电气特性）

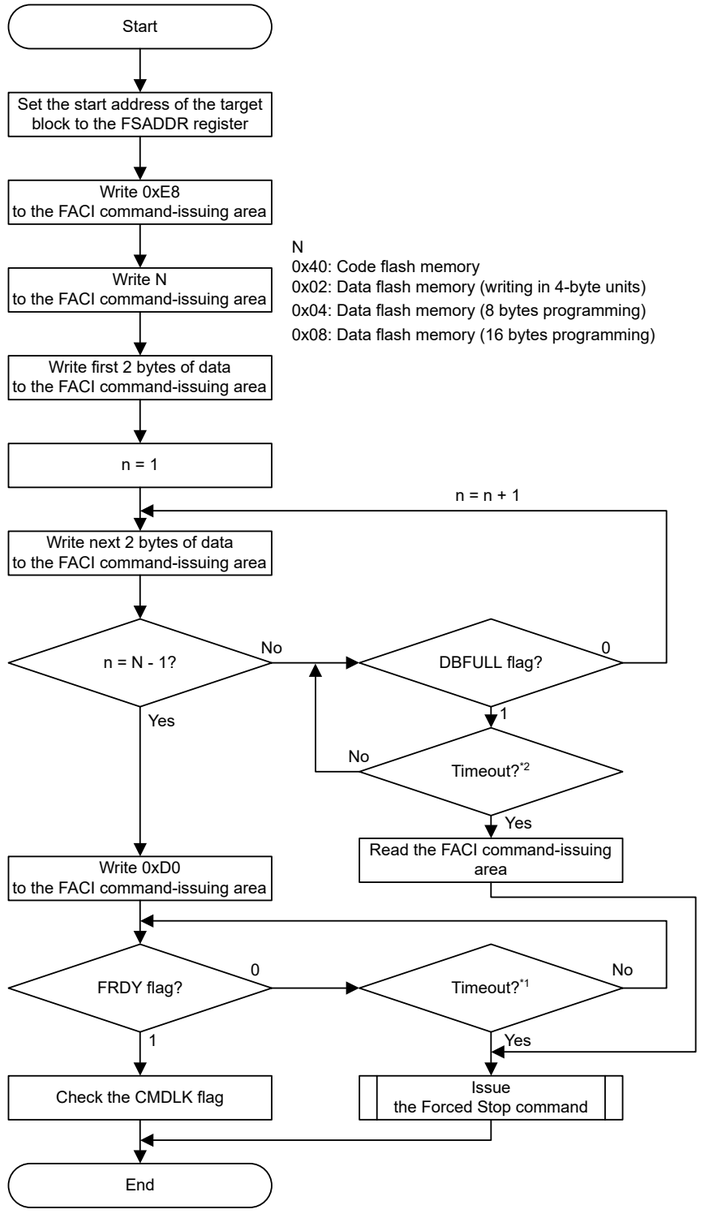
Figure 43.12 从命令锁定状态恢复流程

43.9.3.7 程序命令

程序命令用于写入用户区和数据区。在发出FACI程序命令之前，在FSADDR寄存器中设置目标块的首地址。在最终访问FACI命令发布区域时写入0xD0开始程序命令处理。如果程序命令处理的目标区域包含非写入区域，则将0xFFFF写入相应区域。

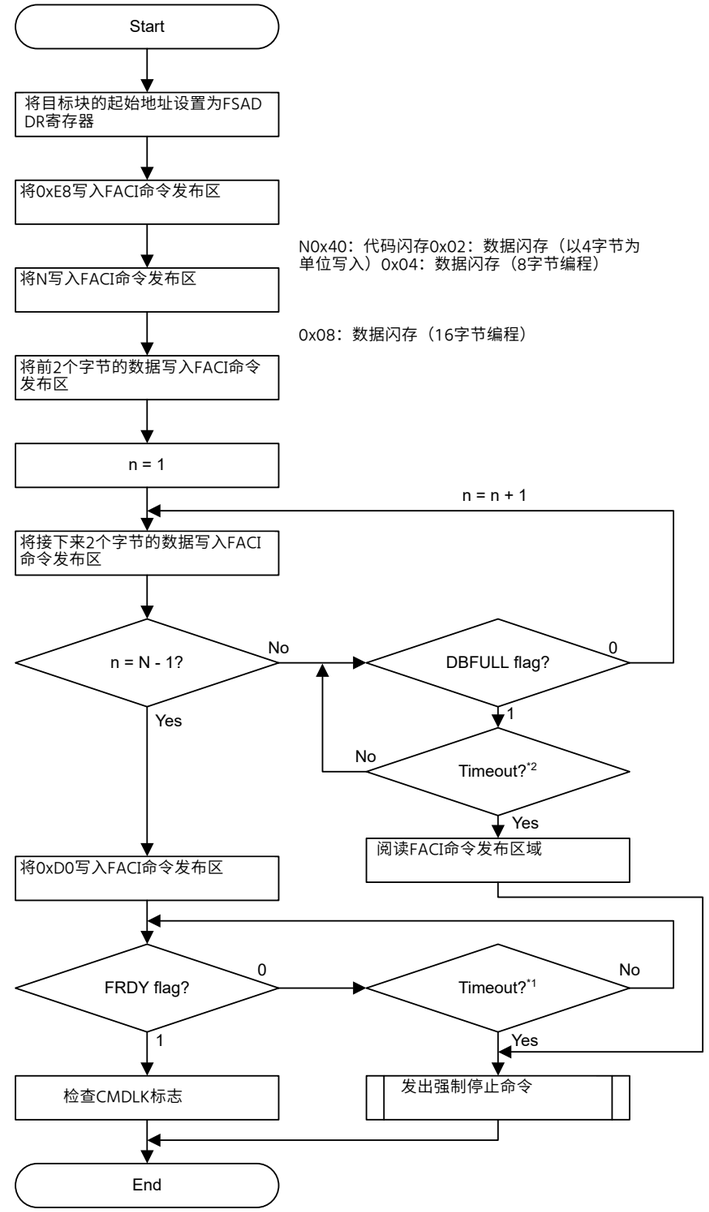
在FACI内部数据缓冲区已满时发出程序命令会导致外围总线等待，这可能会影响其他外围模块的通信性能。为避免等待，请在发出FACI命令时将FSTATR寄存器中的DBFULL位设置为0。写入数据区不会导致数据缓冲区变满。

图43.13显示了程序命令的用法。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of programming. See section 46, Electrical Characteristics about those time
Note 2. 1.4 µs (f_{FCLK} ≥ 20 MHz)

Figure 43.13 Usage flow of the program command



注1.超时的判断是基于最大编程时间的1.1倍。见第46节，电气那个时代的特征
Note 2. 1.4 µs (f_{FCLK} ≥ 20 MHz)

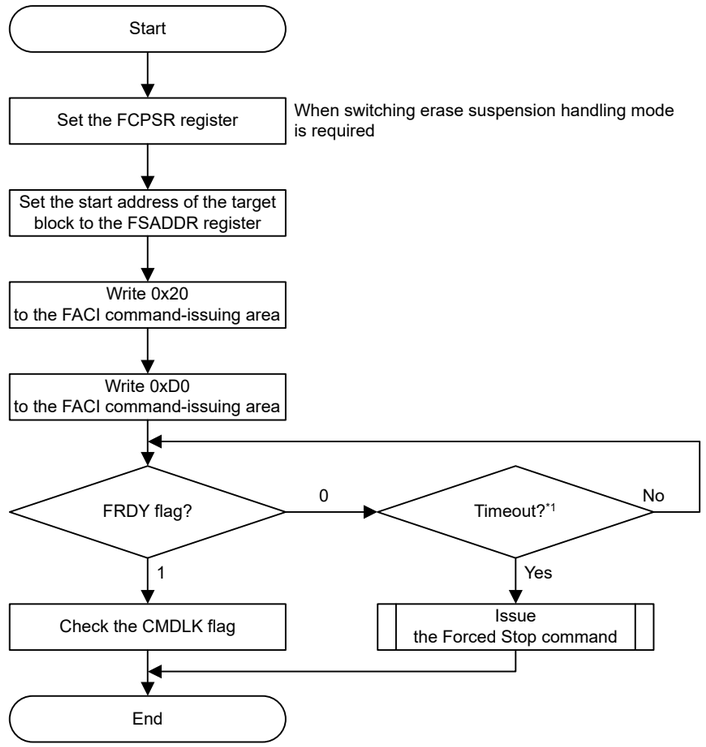
Figure 43.13 程序指令的使用流程

43.9.3.8 Block Erase Command

The block erase command is used for erasing user area or data area. The erase unit is one block. Before issuing a block erase command, set the first address of the target block to FSADRR register. Writing 0xD0 at the second write access of the FACI command triggers the FACI to start the block erase command processing. Completion of command processing can be confirmed with the FRDY bit of FSTATR register.

Set the FCPSR registers before issuing the block erase command. Additionally, FCPSR must be set when the erasure-suspended mode is to be switched.

Figure 43.14 shows the usage of the block erase command.



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of erasure. See section 46, Electrical Characteristics.

Figure 43.14 Usage flow of the block erase command

43.9.3.9 Multi Block Erase Command

The multi block erase command is used for erasing data area. The erase unit is 64, 128, or 256 bytes. Before issuing the multi block erase command, set the start address to FSADRR register and the end address to FEADDR register. Writing 0xD0 at the second write access of the FACI command triggers FACI to start the multi block erase command processing. Completion of command processing can be confirmed with the FRDY bit of FSTATR register.

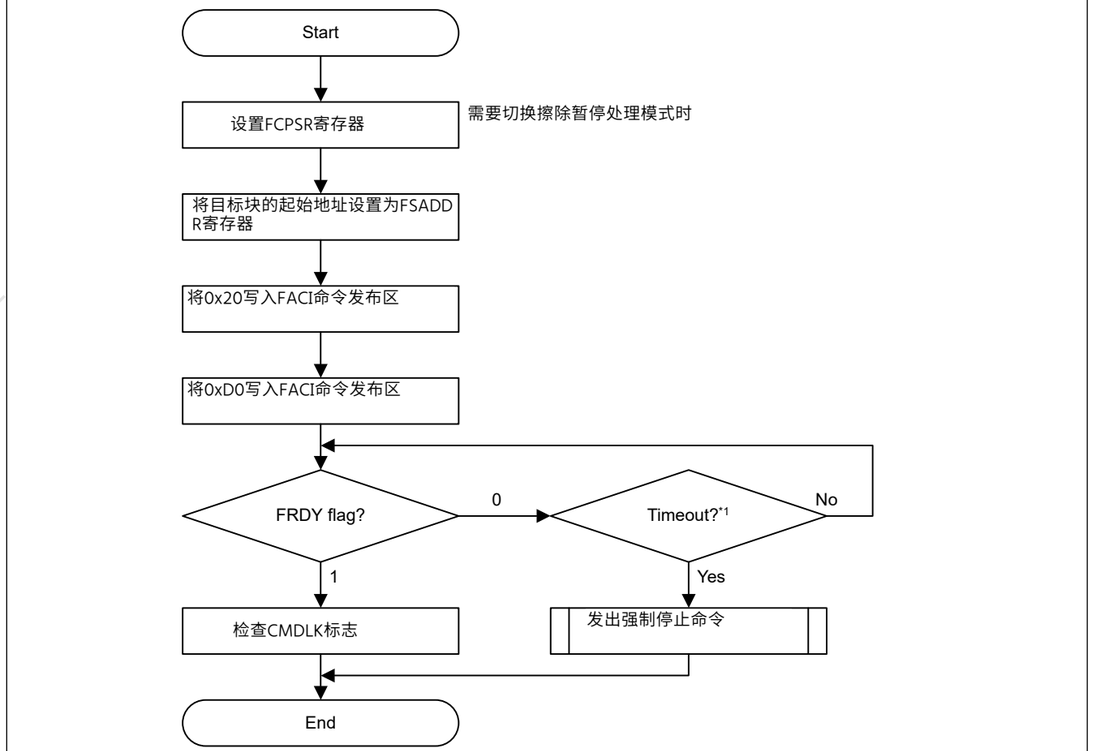
Set the FCPSR registers before issuing the multi block erase command. Additionally, FCPSR must be set when the erasure-suspended mode is to be switched.

43.9.3.8 块擦除命令

块擦除命令用于擦除用户区或数据区。擦除单位是一个块。在发出块擦除命令之前，将目标块的首地址设置为FSADRR寄存器。在FACI命令的第二次写访问时写入0xD0会触发FACI开始块擦除命令处理。命令处理的完成可以通过FSTATR寄存器的FRDY位来确认。

在发出块擦除命令之前设置FCPSR寄存器。此外，当要切换擦除暂停模式时，必须设置FCPSR。

图43.14显示了块擦除命令的用法。



注1.超时的判断是基于最大擦除时间的1.1倍。
参见第46节，电气特性。

Figure 43.14 块擦除命令的使用流程

43.9.3.9 多块擦除命令

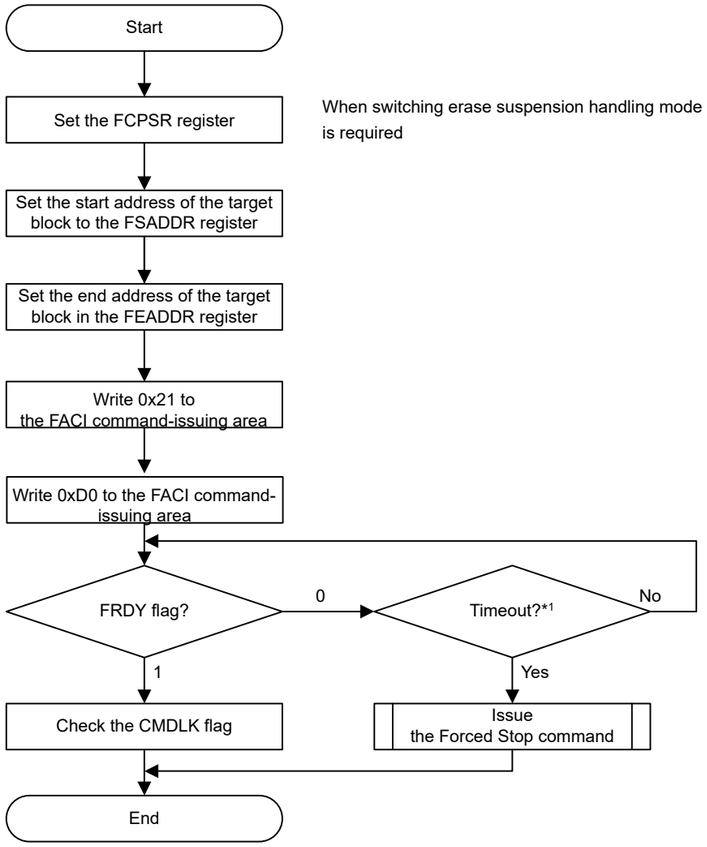
多块擦除命令用于擦除数据区域。擦除单元为64、128或256字节。在发出多块擦除命令之前，将起始地址设置为FSADRR寄存器，将结束地址设置为FEADDR寄存器。在FACI命令的第二次写访问时写入0xD0会触发FACI开始多块擦除命令处理。命令处理的完成可以通过FSTATR寄存器的FRDY位来确认。

在发出多块擦除命令之前设置FCPSR寄存器。此外，当要切换擦除暂停模式时，必须设置FCPSR。

The erase size is specified by both the FSADDR and FEADDR settings. Table 43.17 describes how to set the FSADDR and FEADDR.

Table 43.17 Settings for the erase size

Erase size	FSADDR	FEADDR
64 bytes	FSA0 to FSA5 = 0 (64 byte-boundary)	FSADDR + 0x3C
128 bytes	FSA0 to FSA6 = 0 (128 byte-boundary)	FSADDR + 0x7C
256 bytes	FSA0 to FSA7 = 0 (256 byte-boundary)	FSADDR + 0xFC



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of erasure. See section 46, Electrical Characteristics.

Figure 43.15 Usage flow of the multi block command

43.9.3.10 P/E Suspend Command

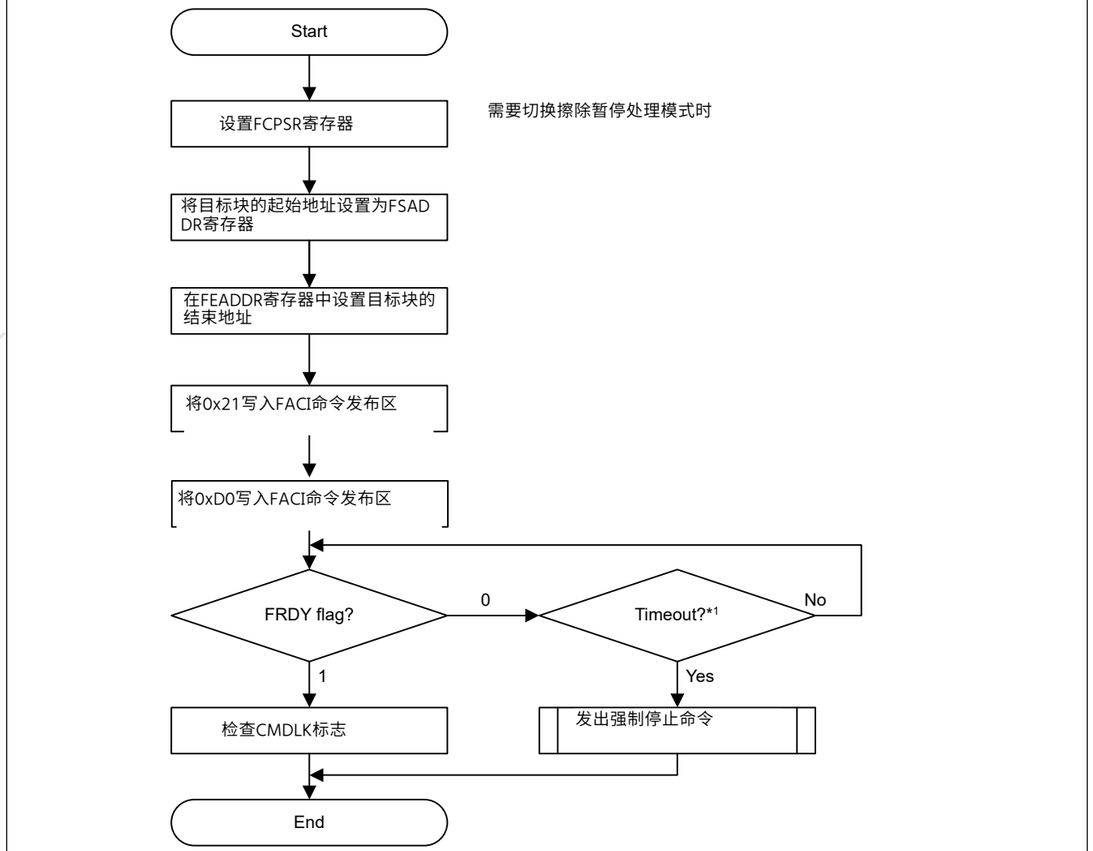
The P/E suspend command is used to suspend programming/erasure. Before issuing a P/E suspend command, check that the CMDLK bit in the FASTAT register is 0, and that the execution of programming/erasure is performed normally. To confirm that the P/E suspend command can be received, check that the SUSRDY bit in the FSTATR register is 1. After issuing a P/E suspend command, read the CMDLK bit to confirm that no error occurs.

If an error occurs during programming/erasure, the CMDLK bit is set to 1. When programming/erasure processing has finished from the time when the SUSRDY bit is 1 to when the P/E suspend command is received, no error occurs and the

擦除大小由FSADDR和FEADDR设置指定。表43.17描述了如何设置FSADDR和FEADDR.

Table 43.17 擦除大小的设置

擦除大小	FSADDR	FEADDR
64 bytes	FSA0 to FSA5 = 0 (64 byte-boundary)	FSADDR + 0x3C
128 bytes	FSA0 to FSA6 = 0 (128 byte-boundary)	FSADDR + 0x7C
256 bytes	FSA0 to FSA7 = 0 (256 byte-boundary)	FSADDR + 0xFC



注1.超时的判断是基于最大擦除时间的1.1倍。
参见第46节，电气特性。

Figure 43.15 多块命令的使用流程

43.9.3.10 PE挂起命令

PE暂停命令用于暂停编程擦除。在发出PE挂起命令之前，请检查FASTAT寄存器中的CMDLK位是否为0，并且编程擦除的执行是否正常执行。要确认可以接收到PE挂起命令，请检查FSTATR寄存器中的SUSRDY位是否为1。发出PE挂起命令后，读取CMDLK位以确认没有错误发生。

如果在编程擦除过程中发生错误，则将CMDLK位设置为1。从SUSRDY位为1到接收到PE暂停命令时，当编程擦除处理完成时，不会发生错误，并且

suspended state is not entered (the FRDY bit in the FSTATR register is 1 and the ERSSPD and PRGSPD bits in FSTATR are 0).

When a P/E suspend command is received and the programming/erasure suspend processing finishes normally, the flash sequencer enters the suspended state, the FRDY bit is set to 1, and the ERSSPD or PRGSPD bit is 1. After issuing a P/E suspend command, check that the ERSSPD or PRGSPD bit is 1 and the suspended state is entered, then proceed with the subsequent flow. If a P/E resume command is issued in the subsequent flow even when the suspended state is not entered, an illegal command error occurs and the flash sequencer shifts to the command-locked state (see section 43.11.2. Error Protection).

If the erasure suspended state is entered, programming to blocks other than an erasure target block can be performed. Additionally, the programming and erasure suspended states can shift to read mode by clearing the FENTRYR register.

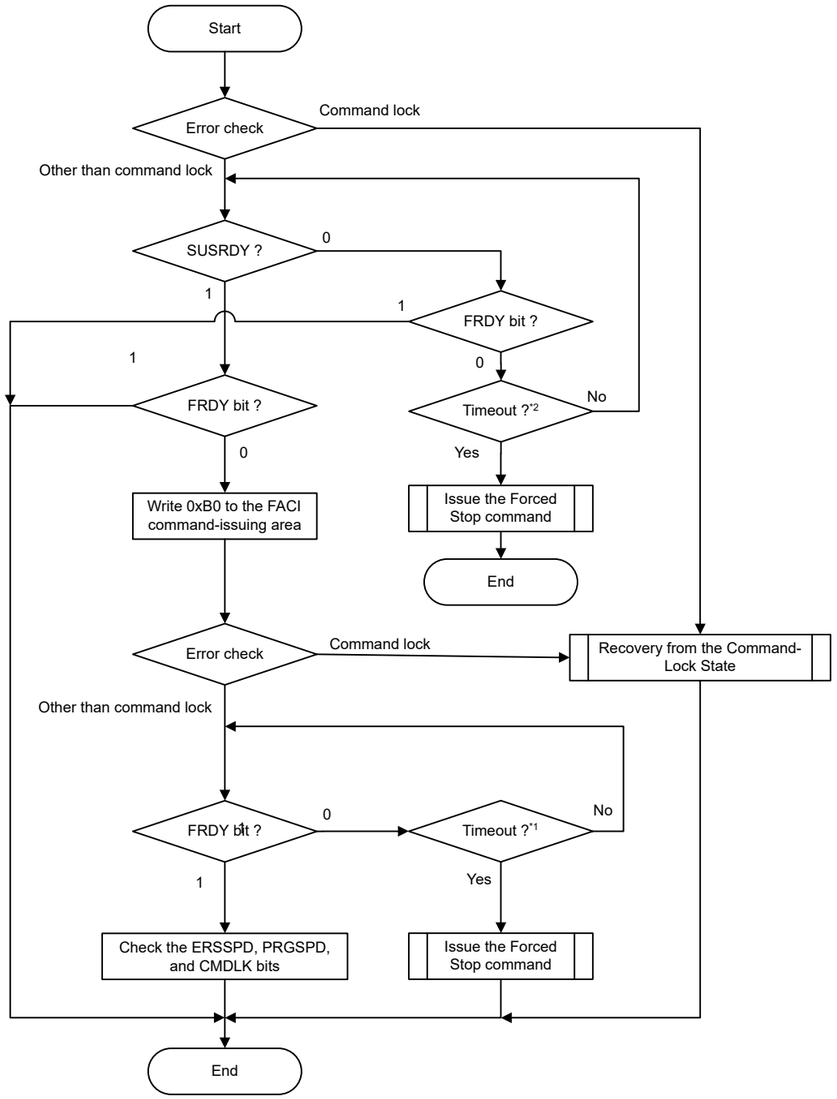
Figure 43.16 shows the usage of the P/E suspend command.

未进入挂起状态（FSTATR寄存器中的FRDY位为1，FSTATR中的ERSSPD和PRGSPD位为0）。

当接收到PE挂起命令并且编程擦除挂起处理正常完成时，闪存定序器进入挂起状态，FRDY位设置为1，ERSSPD或PRGSPD位为1。发出PE挂起命令后，检查是否ERSSPD或PRGSPD位为1，进入挂起状态，然后进行后续流程。如果在后续流程中发出PEresume命令，即使没有进入挂起状态，也会发生非法命令错误，并且闪存定序器会切换到命令锁定状态（请参阅第43.11.2节。错误保护）。

如果进入擦除暂停状态，则可以执行对擦除目标块以外的块的编程。
此外，通过清除FENTRYR寄存器，编程和擦除暂停状态可以转换为读取模式。

图43.16显示了PE挂起命令的用法。

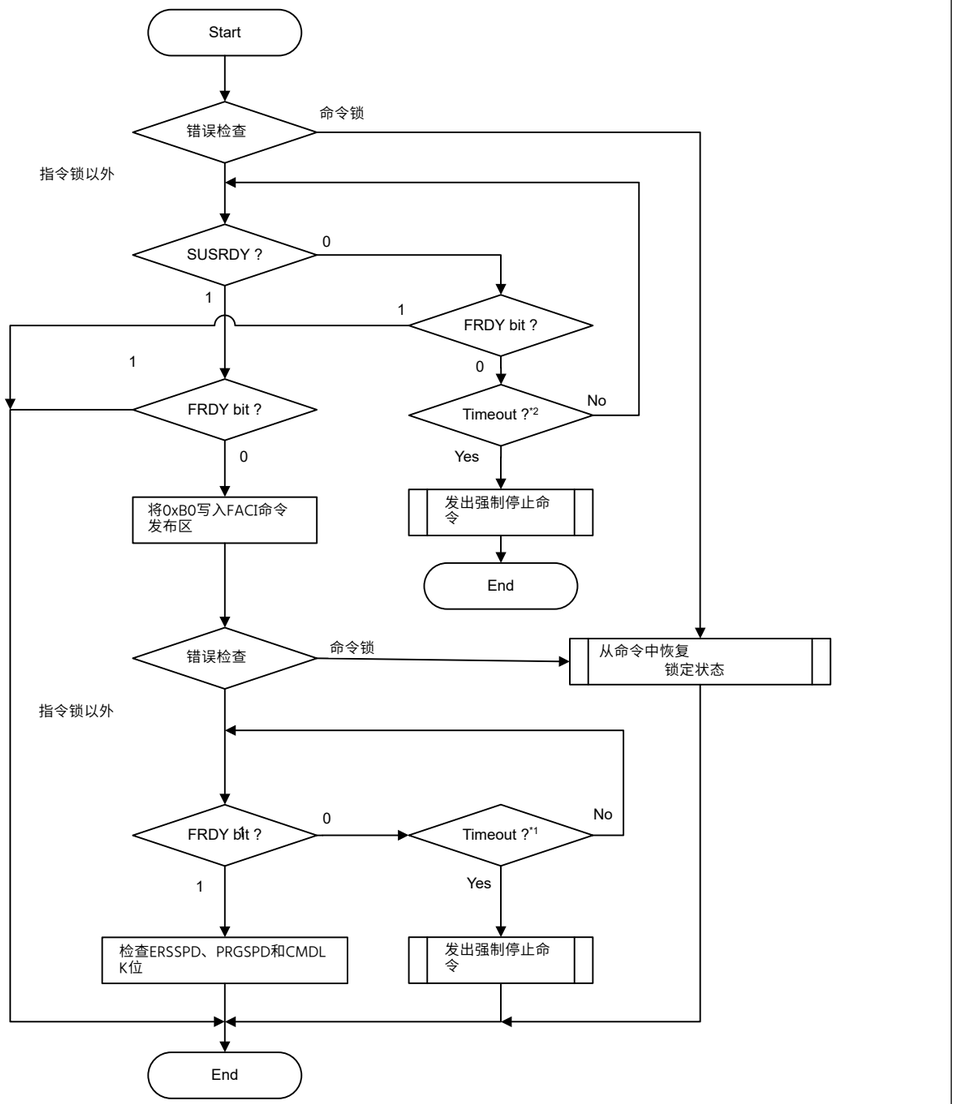


Note 1. Judgment of the timeout is based on 1.1 times the maximum time of suspend delay during erasure for both code flash and data flash.
See section 46, Electrical Characteristics.
Note 2. 4.4µs (f_{FCLK} >= 20MHz)

Figure 43.16 Usage flow of the P/E suspend command

(1) Suspension during Programming

When issuing a P/E suspend command during flash memory programming, the flash sequencer suspends programming processing. Figure 43.17 shows the suspend programming operation. When receiving programming-related command, the flash sequencer clears the FRDY bit in the FSTATR register to 0 to start programming. If the flash sequencer enters the state



注1.超时的判断是基于1.1倍的擦除期间挂起延迟最大时间的代码闪存和数据闪存。参见第46节，电气特性。

Note 2. 4.4µs (f_{FCLK} >= 20MHz)

Figure 43.16 PE挂起命令的使用流程

(1) 编程期间暂停

在闪存编程期间发出PE暂停命令时，闪存定序器暂停编程处理。图43.17显示了挂起编程操作。当接收到编程相关命令时，flashsequencer将FSTATR寄存器中的FRDY位清0以开始编程。如果闪存定序器进入状态

in which the P/E suspend command can be received after programming starts, it sets the SUSRDY bit in the FSTATR register to 1.

When a P/E suspend command is issued, the flash sequencer receives the command and clears the SUSRDY bit to 0. If the flash sequencer receives a P/E suspend command while a programming pulse is applied, the flash sequencer continues with the pulse. After the specified pulse application time, the flash sequencer finishes pulse application, starts the programming suspend processing, and sets the PRGSPD bit in the FSTATR register to 1.

When a suspended processing finishes, the flash sequencer sets the FRDY bit to 1 to enter the programming suspended state. When receiving a P/E resume command in the programming suspended state, the flash sequencer clears the FRDY and PRGSPD bits to 0 and resumes programming.

Figure 43.17 shows the timing for suspension during programming.

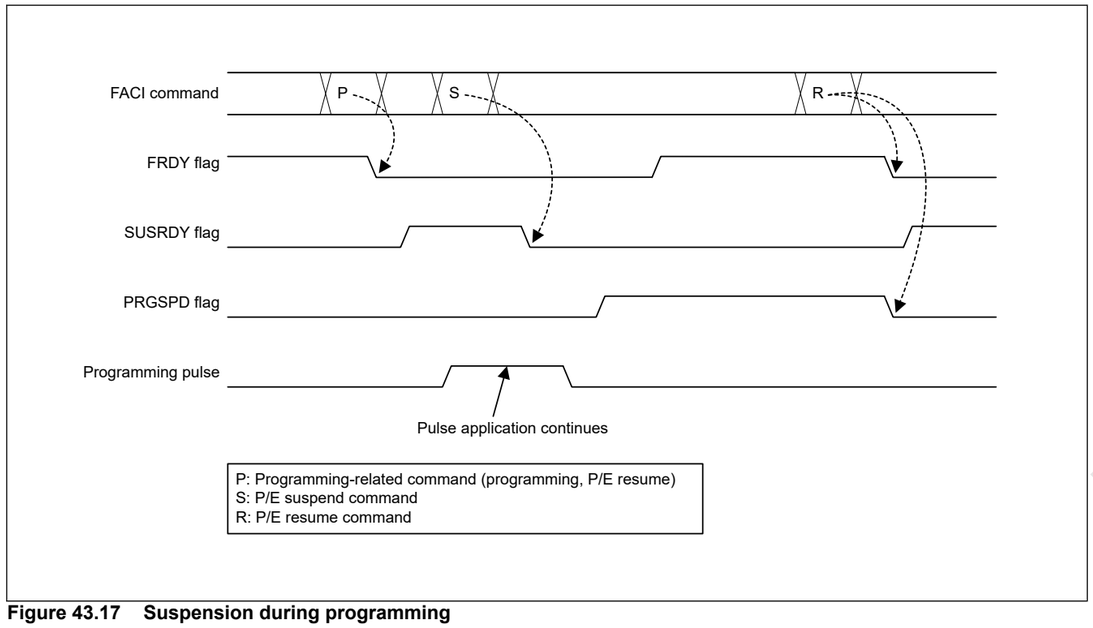


Figure 43.17 Suspension during programming

(2) Suspension during Erasure (Suspension Priority Mode)

The flash sequencer has a suspension priority mode for the suspension of erasure. Figure 43.18 shows the suspend operation of erasure when the erasure suspend mode is set to the suspension priority mode (the ESUSPMD bit in the FCPSR register is 0).

When receiving an erasure-related command, the flash sequencer clears the FRDY bit in the FSTATR register to 0 to start erasure. If the flash sequencer enters the state in which the P/E suspend command can be received after erasure starts, it sets the SUSRDY bit in the FSTATR register to 1.

When a P/E suspend command is issued, the flash sequencer receives the command and clears the SUSRDY bit to 0.

When receiving a suspend command during erasure, the flash sequencer starts the suspend processing and sets the ERSSPD bit in the FSTATR register to 1 even when it is applying an erasure pulse. When the suspended processing finishes, the flash sequencer sets the FRDY bit to 1 to enter the erasure suspended state. When receiving a P/E resume command in the erasure suspended state, the flash sequencer clears the FRDY and ERSSPD bits to 0 and resumes erasure. Operations of the FRDY, SUSRDY, and ERSSPD bits at the suspension and resumption of erasure are the same, regardless of the erasure suspend mode.

The setting of the erasure suspend mode affects the control method of erasure pulses. In suspension priority mode, when receiving a P/E suspend command while erasure pulse A that has not been previously suspended is being applied, the flash sequencer suspends the application of erasure pulse A and enters the erasure suspended state. When receiving a P/E suspend command while reapplying erasure pulse A after erasure is resumed with a P/E resume command, the flash sequencer

在编程开始后可以接收PE挂起命令的情况下，它将FSTATR寄存器中的SUSRDY位设置为1。

当发出PE暂停命令时，闪存定序器接收该命令并将SUSRDY位清除为0。如果在施加编程脉冲时闪存定序器接收到PE暂停命令，则闪存定序器继续执行该脉冲。在指定的脉冲施加时间之后，闪存序列器完成脉冲施加，开始编程暂停处理，并将FSTATR寄存器中的PRGSPD位设置为1。

当暂停处理完成时，闪存定序器将FRDY位设置为1以进入编程暂停状态。当在编程暂停状态下接收到PEresume命令时，闪存定序器将FRDY和PRGSPD位清除为0并恢复编程。

图43.17显示了编程期间暂停的时序。

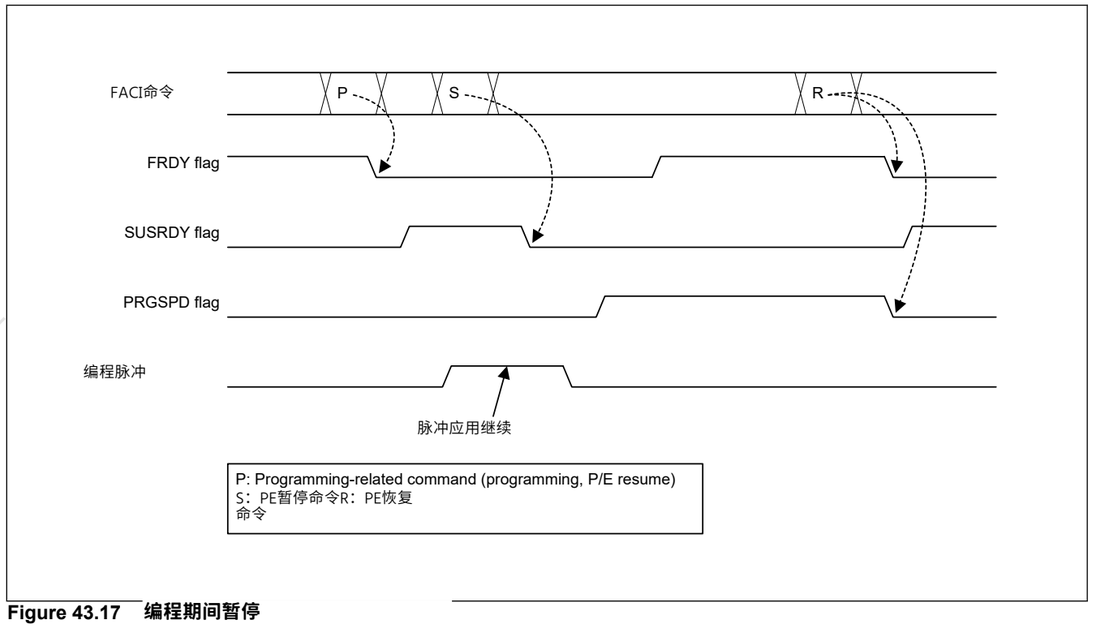


Figure 43.17 编程期间暂停

(2) 擦除期间暂停（暂停优先模式）

闪存定序器具有用于暂停擦除的暂停优先模式。图43.18显示了擦除挂起模式设置为挂起优先模式（FCPSR寄存器中的ESUSPMD位为0）时的擦除挂起操作。

当接收到擦除相关命令时，闪存定序器将FSTATR寄存器中的FRDY位清零以开始擦除。如果闪存序列器在擦除开始后进入可以接收PE挂起命令的状态，它会将FSTATR寄存器中的SUSRDY位设置为1。

当发出PE挂起命令时，闪存定序器接收该命令并将SUSRDY位清除为0。

在擦除期间接收到挂起命令时，闪存定序器启动挂起处理并将FSTATR寄存器中的ERSSPD位设置为1，即使它正在施加擦除脉冲。当挂起处理完成时，闪存定序器将FRDY位设置为1以进入擦除挂起状态。当在擦除暂停状态下接收到PE恢复命令时，闪存定序器将FRDY和ERSSPD位清除为0并恢复擦除。无论擦除暂停模式如何，FRDY、SUSRDY和ERSSPD位在擦除暂停和恢复时的操作都是相同的。

擦除暂停模式的设置会影响擦除脉冲的控制方法。在挂起优先模式下，当在施加先前未被挂起的擦除脉冲A的同时接收到PE挂起命令时，闪存定序器挂起擦除脉冲A的施加并进入擦除挂起状态。在使用PE恢复命令恢复擦除后，在重新应用擦除脉冲A的同时接收到PE暂停命令时，闪存定序器

continues to apply erasure pulse A. After the specified pulse application time, the flash sequencer finishes erasure pulse application and enters the erasure suspended state.

When the flash sequencer receives a P/E resume command next and erasure pulse B is being applied, the flash sequencer receives a P/E suspend command again, and the application of erasure pulse B is then suspended. In suspension priority mode, delays due to suspension can be minimized because the application of an erasure pulse is suspended once per pulse, and priority is given to the suspend processing.

If the interval of suspension after resume is longer than t_{REST1} (Resume time: priority on suspension, resume after the 1st suspend for the same pulse), suspend delay will be always t_{SESD1} (Suspend delay: priority on suspension, the 1st suspend for the same pulse).

If the interval of suspension after resume is shorter than t_{REST1}, suspend delay becomes either t_{SESD1} or t_{SESD2} (Suspend delay: priority on suspension, the 2nd suspend for the same pulse).

(The value of t_{REST1} / t_{SESD1} / t_{SESD2}, see section 46, Electrical Characteristics.)

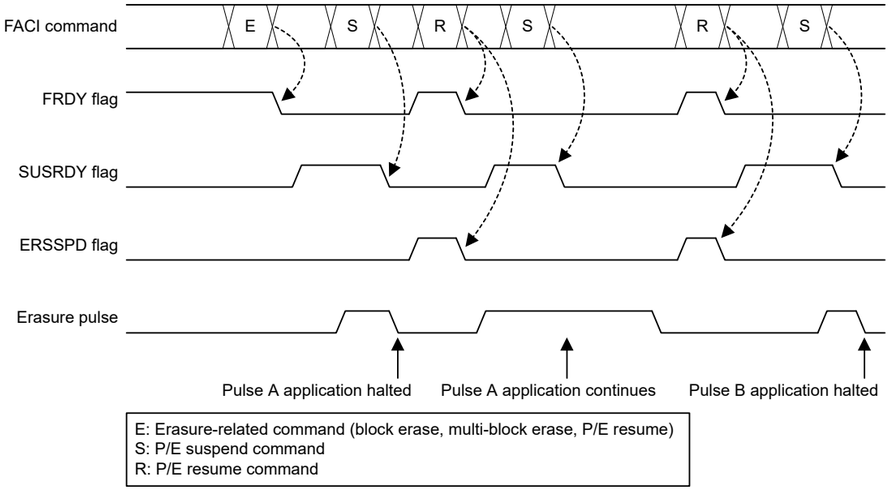


Figure 43.18 Suspension during erasure (suspension priority mode)

(3) Suspension during Erasure (Erasure Priority Mode)

The flash sequencer has an erasure priority mode for the suspension of erasure. Figure 43.19 shows the suspend operation of erasure when the erasure suspend mode is set to the erasure priority mode (the ESUSPMD bit in the FCPSR register is 1). The control method of erasure pulses in erasure priority mode is the same as that of programming pulses for the programming suspend processing.

If the flash sequencer receives a P/E suspend command while an erasure pulse is applied, the flash sequencer continues to apply the pulse. In this mode, the required time for the erasure processing can be reduced compared to the suspension priority mode because the re-application of erasure pulses does not occur when a P/E resume command is issued.

继续施加擦除脉冲A。在指定的脉冲施加时间之后，闪存定序器完成擦除脉冲施加并进入擦除暂停状态。

当闪存定序器接下来接收到PE恢复命令并且正在施加擦除脉冲B时，闪存定序器再次接收到PE暂停命令，然后暂停擦除脉冲B的施加。在挂起优先模式中，由于擦除脉冲的施加在每个脉冲中挂起一次，因此挂起引起的延迟可以被最小化，并且挂起处理具有优先权。

如果恢复后挂起的时间间隔大于tREST1（恢复时间：挂起优先，相同脉冲第一次挂起后恢复），挂起延迟将始终为tSESD1（挂起延迟：挂起优先，第一次挂起相同的脉冲）。

如果恢复后的暂停间隔小于tREST1，则暂停延迟变为tSESD1或tSESD2（暂停延迟：暂停优先，相同脉冲的第2次暂停）。

（tREST1tSESD1tSESD2的值，请参见第46节，电气特性。）

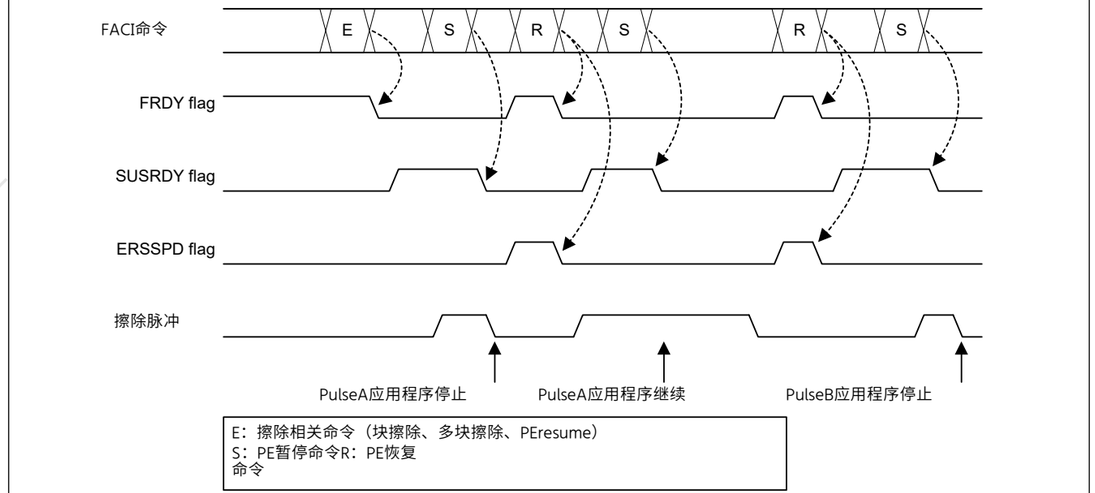


Figure 43.18 擦除期间暂停（暂停优先模式）

(3) 擦除期间暂停（擦除优先模式）

闪存定序器具有用于暂停擦除的擦除优先模式。图43.19显示了擦除挂起模式设置为擦除优先模式时的擦除挂起操作（FCPSR寄存器中的ESUSPMD位为1）。擦除优先模式中擦除脉冲的控制方法与用于编程暂停处理的编程脉冲的控制方法相同。

如果在施加擦除脉冲时闪存定序器接收到PE暂停命令，则闪存定序器继续施加脉冲。在这种模式下，与暂停优先模式相比，擦除处理所需的时间可以减少，因为当发出PE恢复命令时不会发生擦除脉冲的重新施加。

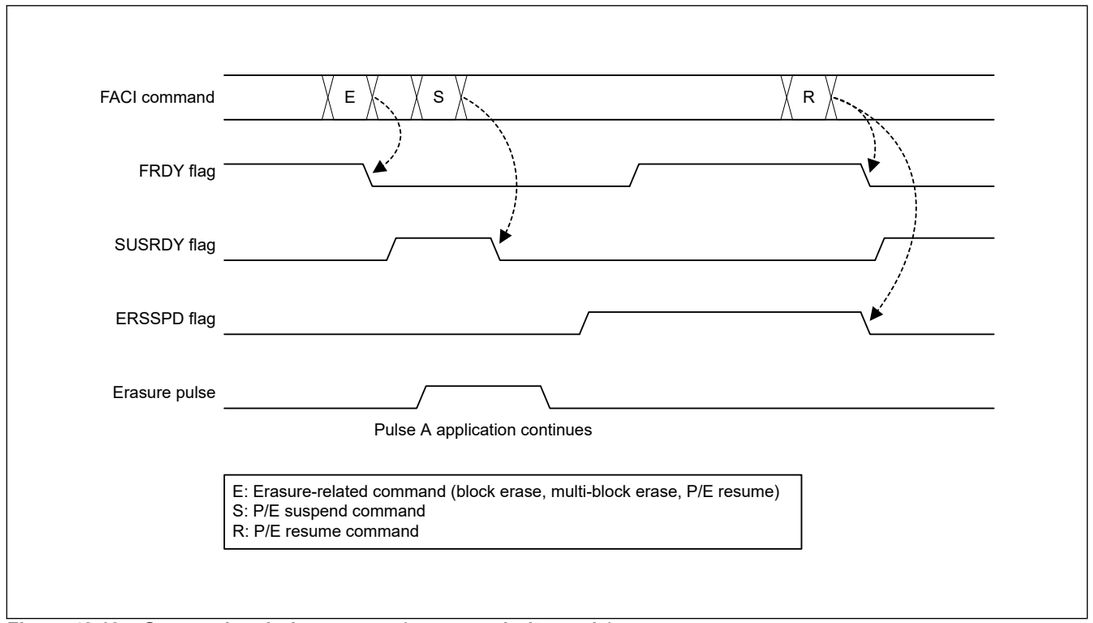
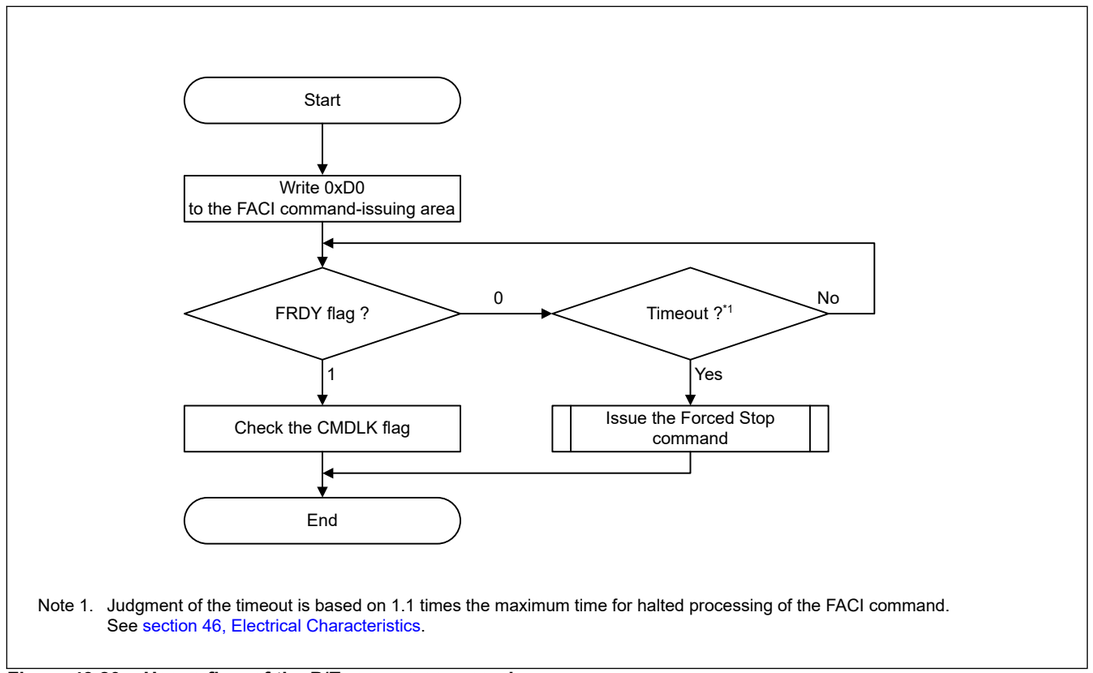


Figure 43.19 Suspension during erasure (erasure priority mode)

43.9.3.11 P/E Resume Command

The P/E resume command is used to resume suspended programming or erasure. If the FENTRYR setting has been modified during suspension, issue a P/E resume command only after resetting FENTRYR to the previous value that was held before the P/E suspend command was issued. Figure 43.20 shows usage of the P/E resume command.



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for halted processing of the FACI command. See section 46, Electrical Characteristics.

Figure 43.20 Usage flow of the P/E resume command

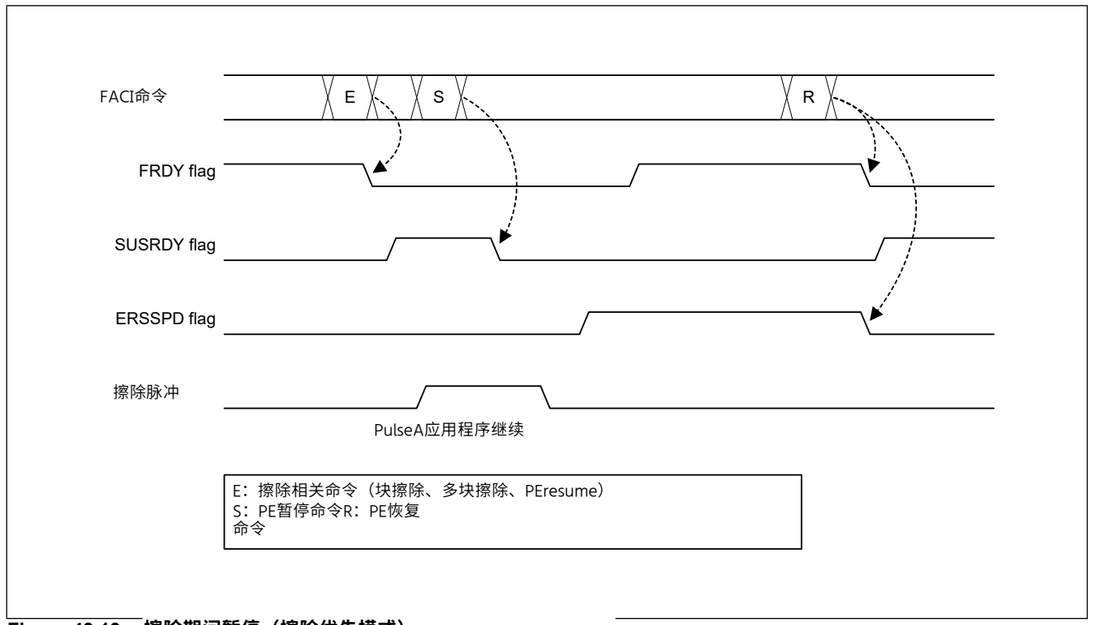
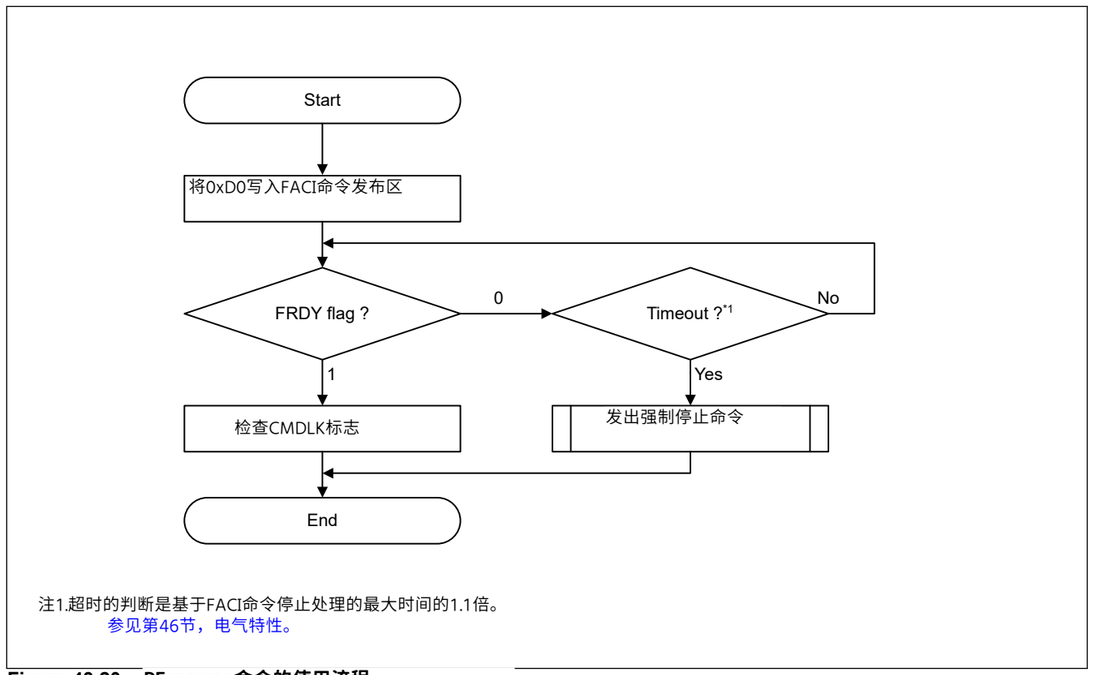


Figure 43.19 擦除期间暂停（擦除优先模式）

43.9.3.11 PE恢复命令

PEresume命令用于恢复暂停的编程或擦除。如果在挂起期间修改了FENTRYR设置，则仅在将FENTRYR重置为发出PE挂起命令之前保持的先前值之后才发出PEresume命令。图43.20显示了PEresume命令的用法。



注1.超时的判断是基于FACI命令停止处理的最大时间的1.1倍。
参见第46节，电气特性。

Figure 43.20 PEresume命令的使用流程

43.9.3.12 Status Clear Command

The status clear command is used to clear the command-locked state (see section 43.9.3.6. Recovery from the Command-Locked State).

You can use the status clear command to clear the following bits in the FSTATR register in the command-locked state:

- ILGLERR
- ILGCOMERR
- FESETERR
- SECERR
- OTERR
- ERSERR
- PRGERR

Figure 43.21 shows usage of the status clear command.

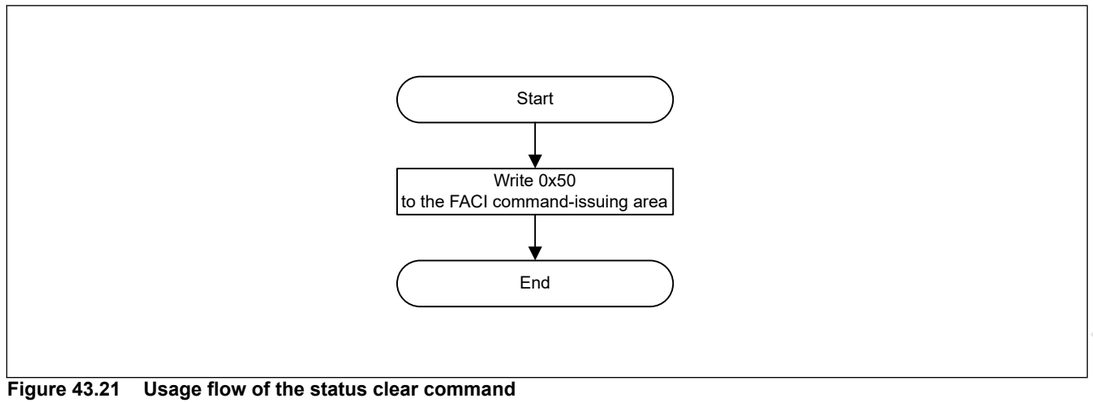


Figure 43.21 Usage flow of the status clear command

43.9.3.13 Forced Stop Command

The forced stop command is used to forcibly end command processing by the flash sequencer. Although this command halts command processing more quickly than the P/E suspension command, values from the programming or erasure that are in progress are not guaranteed. Additionally, resumption of processing is not possible. Processing of programming or erasure that is halted by the forced stop command is also defined as one programming round.

Executing the forced stop command also initializes part of the FACI, the whole FCU, the FSTATR and FASTAT registers. This command can be used in the procedure for recovery from the command-locked state and for processing in response to a timeout of the flash sequencer (see section 43.9.3.6. Recovery from the Command-Locked State).

Figure 43.22 shows usage of the forced stop command.

43.9.3.12 状态清除命令

statusclear命令用于清除命令锁定状态（参见第43.9.3.6节。从命令中恢复锁定状态）。

在命令锁定状态下，您可以使用statusclear命令清除FSTATR寄存器中的以下位：

- ILGLERR
- ILGCOMERR
- FESETERR
- SECERR
- OTERR
- ERSERR
- PRGERR

图43.21显示了statusclear命令的用法。

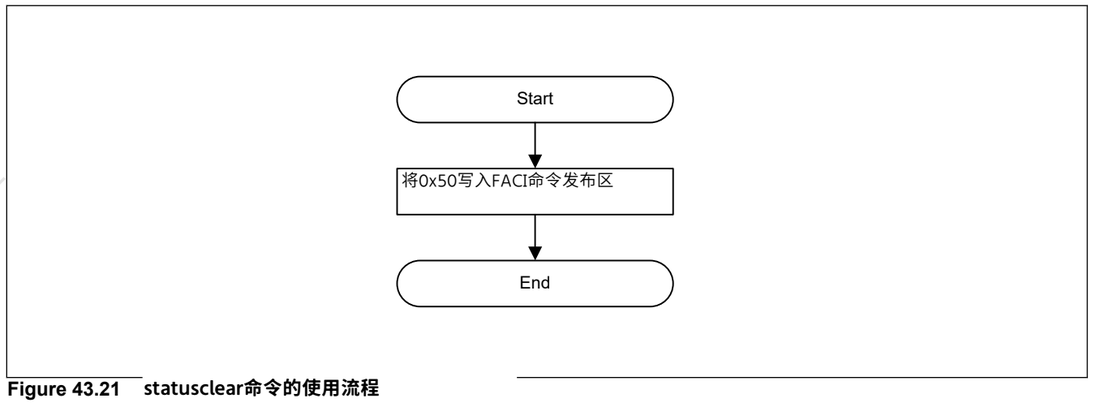


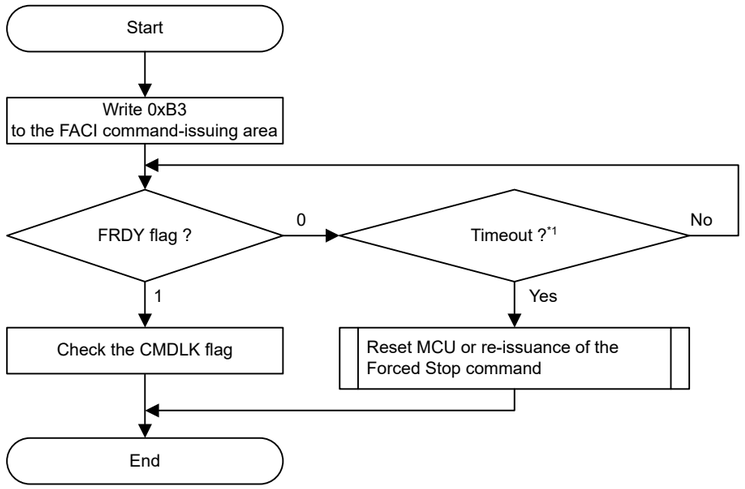
Figure 43.21 statusclear命令的使用流程

43.9.3.13 强制停止命令

强制停止命令用于强制结束闪存定序器的命令处理。尽管此命令比PE暂停命令更快地停止命令处理，但不能保证正在进行的编程或擦除的值。此外，无法恢复处理。由强制停止命令停止的编程或擦除的处理也被定义为一轮编程。

执行强制停止命令还会初始化部分FACI、整个FCU、FSTATR和FASTAT寄存器。
此命令可用于从命令锁定状态恢复的过程以及用于响应闪存定序器超时的处理（请参阅第43.9.3.6节。从命令锁定状态恢复）。

图43.22显示了强制停止命令的用法。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of the Forced Stop command latency.
See section 46, Electrical Characteristics.

Figure 43.22 Usage flow of the forced stop command

(1) Notes on Using the Forced Stop Command during Command Issue

When using the forced stop command at the timeout occurrence by DBFULL bit of the program command, writing in the FACI command-issuing area is sometimes processed as writing in data of the program command. See Table 43.3 in section 43.3. Address Space for information on the FACI command-issuing area to force a command lock. Then issue a forced stop command with return method from the command lock status (see Figure 43.13). Locking commands is possible in any case where the unit for reading the FACI command issuing area is 8, 16, or 32 bits.

43.9.3.14 Blank Check Command

The blank check command is used to confirm that an area is in the non-programmed state. Values read from the data flash memory that have been erased but not yet programmed again that is in the non-programmed state, are undefined.

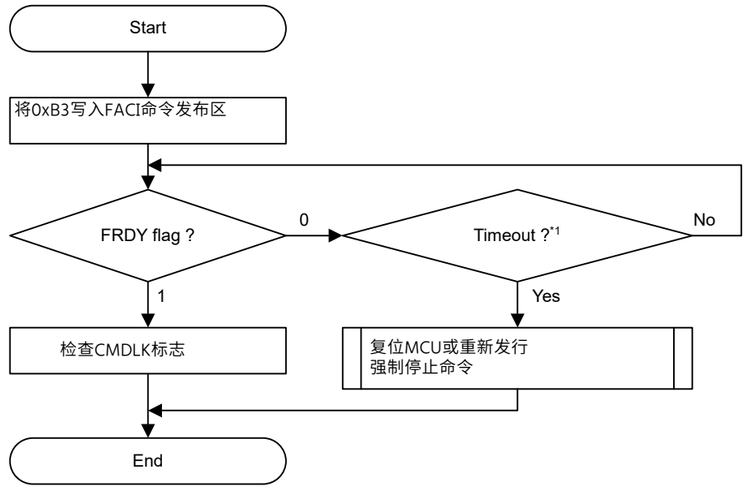
Before issuing the Blank Check command, set addressing mode, start address, and end address of the target area for Blank Check to the FBCCNT, FSADDR, and FEADDR registers. When Blank Check addressing mode is set to decremental mode (i.e. FBCCNT.BCDIR = 1), address specified in FSADDR should be equal to or larger than address in FEADDR.

On the other hand, the address in FSADDR should be equal to or smaller than address in FEADDR when Blank Check addressing mode is set to incremental mode (i.e. FBCCNT.BCDIR = 0).

If the settings of the BCDIR bit, FSADDR, and FEADDR are inconsistent, the flash sequencer enters the command-locked state. The size of the target area for Blank Check is in the range from 4 bytes to the data flash memory capacity and is set in units of 4 bytes.

Write 0x71 and 0xD0 to the FACI command-issuing area to start Blank Check. Completion of processing can be confirmed by the FRDY bit of the FSTATR register. At the end of processing, the result of Blank Check is stored in the BCST bit in the FBCSTAT register. If non-programmed data exists within the target area for Blank Check, flash sequencer stops Blank Check command operation. In this case, address of non-programmed data is indicated to FPSADDR register.

Figure 43.23 shows usage of the blank check command.



注1.超时的判断基于强制停止命令延迟的最大时间的1.1倍。
参见第46节，电气特性。

Figure 43.22 强制停止命令的使用流程

(1) 命令发出期间使用强制停止命令的注意事项

通过程序命令的DBFULL位在超时发生时使用强制停止命令时，写入
FACI命令发布区域有时被处理为写入程序命令的数据。请参见第43.3节中的表43.3。FACI命令发布区域信息的地址空间以强制命令锁定。然后从命令锁定状态发出带返回方法的强制停止命令（见图43.13）。在读取FACI命令发布区域的单位为8、16或32位的任何情况下，锁定命令都是可能的。

43.9.3.14 空白检查命令

空白检查命令用于确认某个区域处于非编程状态。从处于未编程状态的已擦除但尚未再次编程的数据闪存读取的值未定义。

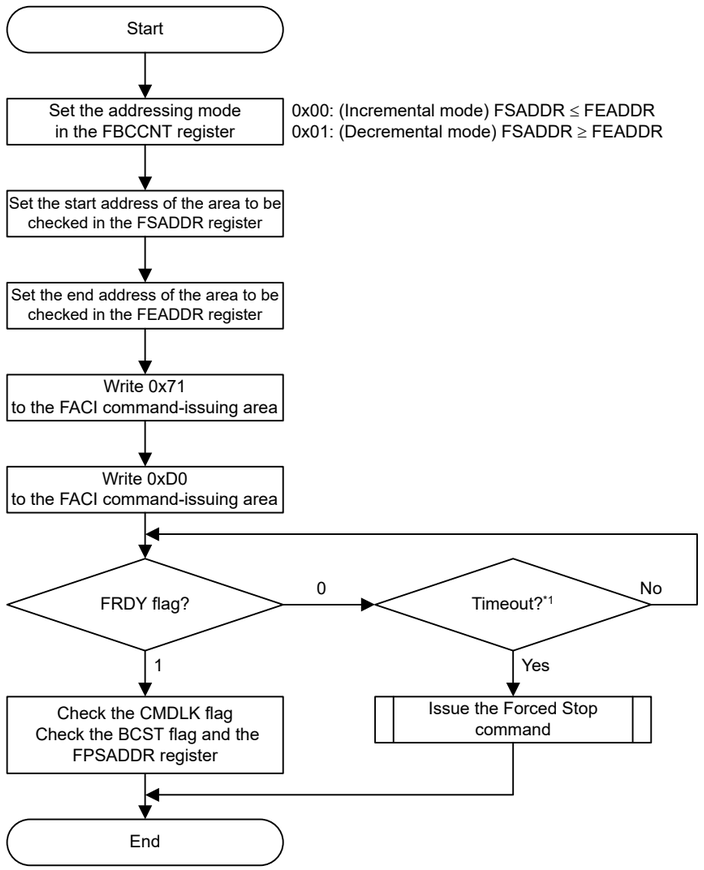
在发出空白检查命令之前，设置空白目标区域的寻址方式、起始地址和结束地址
检查FBCCNT、FSADDR和FEADDR寄存器。当空白检查寻址模式设置为递减模式（即FBCCNT.BCDIR=1）时，FSADDR中指定的地址应等于或大于FEADDR中的地址。

另一方面，当空白检查寻址模式设置为增量模式（即FBCCNT.BCDIR=0）时，FSADDR中的地址应等于或小于FEADDR中的地址。

如果BCDIR位、FSADDR和FEADDR的设置不一致，则flashsequencer进入command-locked状态。BlankCheck的目标区域大小在4字节到数据闪存容量的范围内，以4字节为单位设置。

将0x71和0xD0写入FACI命令发出区域以启动空白检查。可通过FSTATR寄存器的FRDY位确认处理完成。处理结束时，空白检查的结果存储在FBCSTAT寄存器的BCST位中。如果空白检查的目标区域内存在未编程的数据，闪存定序器将停止空白
检查命令操作。在这种情况下，非编程数据的地址被指示到FPSADDR寄存器。

图43.23显示了空白检查命令的用法。



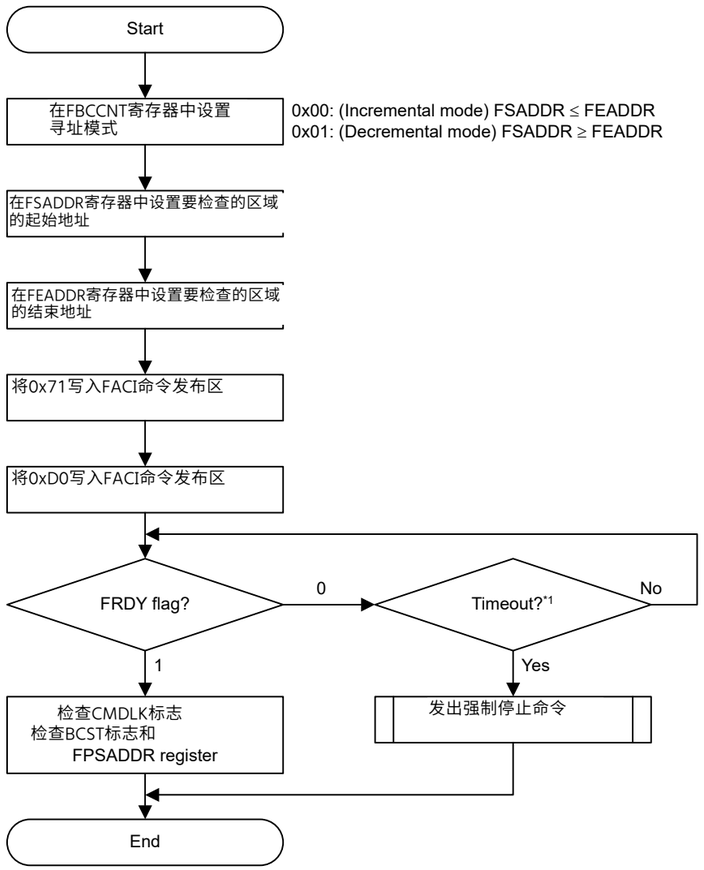
Note 1. Judgment of the timeout is based on 1.1 times the maximum time of Blank Checking for the whole target range. See section 46, Electrical Characteristics.

Figure 43.23 Usage flow of the blank check command

43.9.3.15 Configuration Set Command

The Configuration set command is used to set option-setting memory. Before issuing the Configuration set command, set the specified address (shown in Table 43.18) in the FSADDR register. Writing 0xD0 to the FACI command-issuing area in the final access for issuing the FACI command starts FACI processing of the Configuration set command.

Figure 43.24 shows usage of the configuration set command.



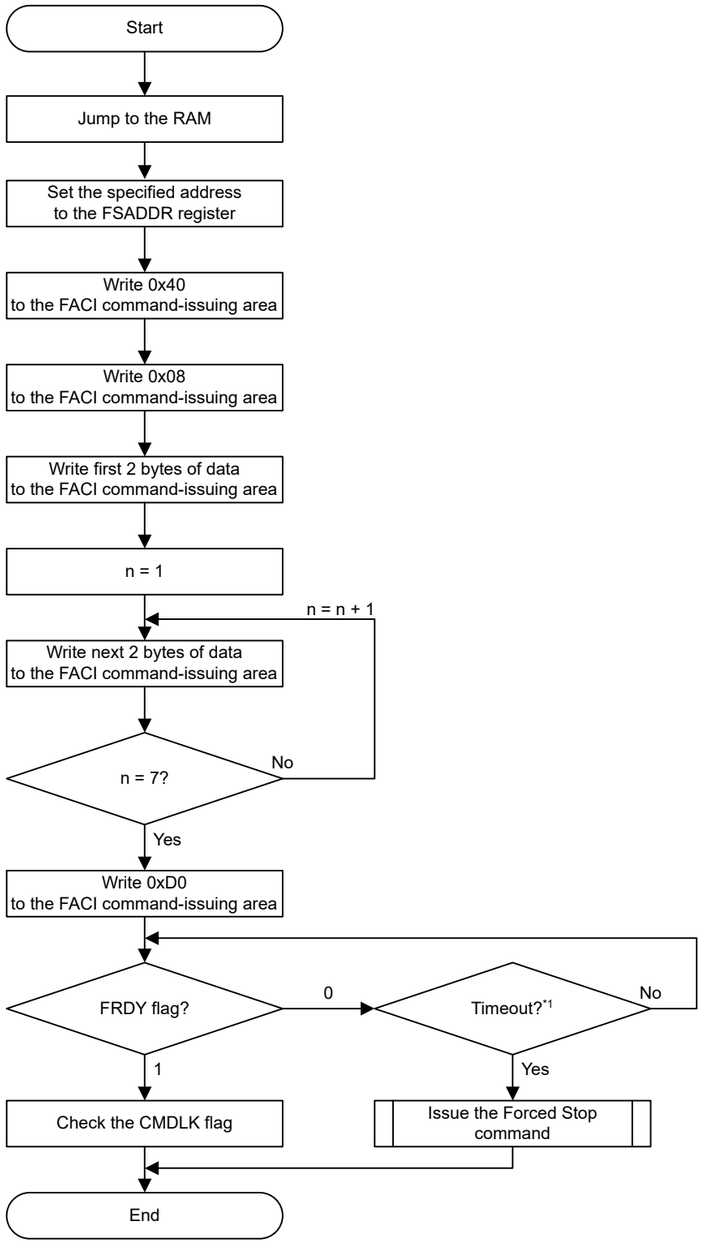
注1.超时的判断是基于1.1倍的整个目标范围的BlankChecking最大时间。看第46节，电气特性。

Figure 43.23 空白检查命令的使用流程

43.9.3.15 配置集命令

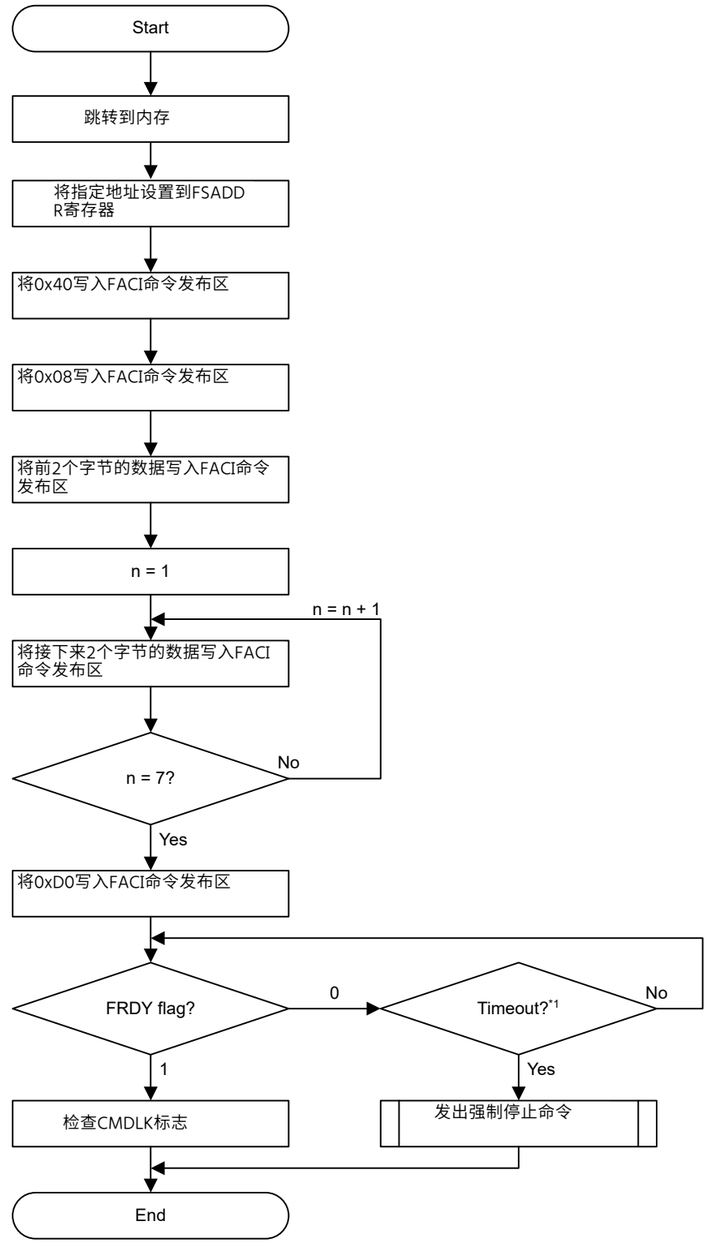
Configurationset命令用于设置选项设置内存。在发出配置设置命令之前，在FSADDR寄存器中设置指定的地址（如表43.18所示）。在发出FACI命令的最终访问中将0xD0写入FACI命令发出区域，开始配置设置命令的FACI处理。

图43.24显示了配置集命令的用法。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of programing in option-setting memory. See section 46, Electrical Characteristics.

Figure 43.24 Usage flow of the configuration set command



注1.超时的判断是基于选项设置内存中最大编程时间的1.1倍。参见第46节，电气特性。

Figure 43.24 配置集命令使用流程

The correspondence between the possible target data for configuration setting and the address value set in the FSADDR register is shown in Table 43.18. For details, see section 43.4.12. FSADDR : FACI Command Start Address Register.

Table 43.18 Address Used by Configuration Set Command

Address	FSADDR Register Value	Setting Data	Operation of additional writing		Timing when the Setting is Enabled
			SAS.FSPR bit is 1	SAS.FSPR bit is 0	
0x0100_A100	0x0100_A100	Option Function Select Register 0 (OFS0)	Writable	Writable	At a reset
0x0100_A134	0x0100_A130	Start-up Area Setting Register (SAS)	Writable	Not writable*1	When a reset or command is executed
0x0100_A180	0x0100_A180	Option Function Select Register 1 (OFS1)	Writable	Writable	At a reset
0x0100_A1C0	0x0100_A1C0	Block Protect Setting Register (BPS)	Writable*2	Writable*2	When a reset or command is executed
0x0100_A1E0	0x0100_A1E0	Permanent Block Protect Setting Register (PBPS)	Writable*3 (from 1 to 0 only)	Writable*3 (from 1 to 0 only)	When a reset or command is executed
0x0100_A200	0x0100_A200	Option Function Select Register 1 Secure (OFS1_SEC)	Writable	Writable	At a reset
0x0100_A240	0x0100_A240	Block Protect Setting Register Secure (BPS_SEC)	Writable*4	Writable*4	When a reset or command is executed
0x0100_A260	0x0100_A260	Permanent Block Protect Setting Register Secure (PBPS_SEC)	Writable*5 (from 1 to 0 only)	Writable*5 (from 1 to 0 only)	When a reset or command is executed
0x0100_A280	0x0100_A280	Option Function Select Register 1 Select (OFS1_SEL)	Writable	Writable	At a reset
0x0100_A2C0	0x0100_A2C0	Block Protect Setting Register Select (BPS_SEL)	Writable	Writable	At a reset

Note 1. The SAS.FSPR bit cannot be restored to 1 by using the Configuration set command once it is set to 0. Therefore, setting the start-up area select flags again becomes impossible. (when the Configuration set command is issued to the address of 0x0100A134, the command is locked.) Exercise extra caution when handling the SAS.FSPRbit.
Note 2. Once PBPS[n] bit is set to 0, the BPS[n] bit cannot be restored to 1 by using the Configuration set command.
Note 3. Once these bits are set to 0, the bits cannot be restored to 1 by using the Configuration set command. The PBPS[n] bit can not be set to 0 by using the Configuration set command when the BPS[n] bit is 1.
Note 4. Once PBPS_SEC[n] bit is set to 0, the BPS_SEC[n] bit cannot be restored to 1 by using the Configuration set command.
Note 5. Once these bits are set to 0, the bits cannot be restored to 1 by using the Configuration set command. The PBPS_SEC[n] bit cannot be set to 0 by using the Configuration set command when the BPS_SEC[n] bit is 1.

43.10 Suspend Operation

Reading from the flash memory is not possible during programming or erasure if the conditions for background operation given in Table 43.29 are not satisfied. When a P/E suspend command is issued to suspend the programming or erasure of the flash memory, reading from the flash memory is enabled. Regarding P/E suspend commands, there are one suspend command mode for programming and two suspend command modes for erasure (suspension priority mode and erasure priority mode). To resume suspended programming or erasure, the P/E resume command is available. See details on the suspend operation, refer to Figure 43.16.

43.11 Protection Function

43.11.1 Software Protection

Software protection disables programming and erasure of the code flash memory through the settings of control registers and block protect setting in the user area. If an attempt is made to issue an FACI command against software protection, the flash sequencer enters the command-locked state.

43.11.1.1 Protection through FWEPROR

Unless the FWEPROR.FLWE[1:0] bits are set to 01b, programming cannot proceed in any mode.

配置设置的可能目标数据与FSADDR寄存器中设置的地址值的对应关系如表43.18所示。详见43.4.12节。FSADDR：FACI命令起始地址寄存器。

Table 43.18 配置设置命令使用的地址

Address	FSADDR 寄存器值设置数据		追加写入的操作		设置为的时间 Enabled
			SAS.FSPR位为1	SAS.FSPR位为0	
0x0100_A100	0x0100_A100	选项功能选择寄存器0(OFS0)	Writable	Writable	复位时
0x0100_A134	0x0100_A130	启动区设置寄存器(SAS)	Writable	Not writable*1	执行复位或命令时
0x0100_A180	0x0100_A180	选项功能选择寄存器1(OFS1)	Writable	Writable	复位时
0x0100_A1C0	0x0100_A1C0	块保护设置寄存器(BPS)	Writable*2	Writable*2	执行复位或命令时
0x0100_A1E0	0x0100_A1E0	永久块保护设置 Register (PBPS)	Writable*3 (from 1 to 0 only)	Writable*3 (from 1 to 0 only)	执行复位或命令时
0x0100_A200	0x0100_A200	选项功能选择寄存器1安全(OFS1_SEC)	Writable	Writable	复位时
0x0100_A240	0x0100_A240	块保护设置寄存器 Secure (BPS_SEC)	Writable*4	Writable*4	执行复位或命令时
0x0100_A260	0x0100_A260	永久块保护设置 注册安全(PBPS_SEC)	Writable*5 (from 1 to 0 only)	Writable*5 (from 1 to 0 only)	执行复位或命令时
0x0100_A280	0x0100_A280	选项功能选择寄存器1选择(OFS1_SEL)	Writable	Writable	复位时
0x0100_A2C0	0x0100_A2C0	块保护设置寄存器 Select (BPS_SEL)	Writable	Writable	复位时

注1.SAS.FSPR位一旦设置为0，就无法通过Configurationset命令恢复为1。因此，再次设置启动区域选择标志变得不可能。（当向0x0100A134地址发出Configurationset命令时，该命令被锁定。）处理SAS.FSPRbit时要格外小心。

注2.一旦PBPS[n]位设置为0，BPS[n]位不能通过使用配置设置命令恢复为1。
注3.一旦这些位设置为0，就不能使用配置设置命令将这些位恢复为1。当BPS[n]位为1时，不能使用配置设置命令将PBPS[n]位设置为0。

注4.一旦PBPS_SEC[n]位设置为0，则BPS_SEC[n]位无法通过使用配置设置命令恢复为1。
注5.一旦这些位设置为0，就不能使用配置设置命令将这些位恢复为1。当BPS_SEC[n]位为1时，无法使用配置设置命令将PBPS_SEC[n]位设置为0。

43.10 暂停操作

如果不满足表43.29中给出的后台操作条件，则在编程或擦除期间无法从闪存读取。当发出PE暂停命令以暂停闪存的编程或擦除时，将启用从闪存读取。关于PE挂起命令，有一种用于编程的挂起命令模式和两种用于擦除的挂起命令模式（挂起优先模式和擦除优先模式）。要恢复暂停的编程或擦除，可以使用PEresume命令。参见挂起操作的详细信息，参见图43.16。

43.11 保护功能

43.11.1 软件保护

软件保护通过控制寄存器的设置和用户区的块保护设置禁用代码闪存的编程和擦除。如果尝试针对软件保护发出FACI命令，则闪存定序器进入命令锁定状态。

43.11.1.1 通过FWEPROR进行保护

除非FWEPROR.FLWE[1:0]位设置为01b，否则无法在任何模式下进行编程。

43.11.1.2 Protection by FENTRYR

When the FENTRYR register is set to 0x0000, the flash sequencer enters read mode. In read mode, FACI commands cannot be accepted. If an attempt is made to issue an FACI command in read mode, the flash sequencer enters the command-locked state.

43.11.1.3 Protection by Block Protect Setting

Each block in user area has the block protect setting (BPS or BPS_SEC). When the FBPROT0 or FBPROT1 register is 0x0000 and the block protect bit is 0, issuing the Program or Block Erase command to user area of the code flash causes the command-locked state. To program or erase the block whose block protect bit is 0, set the FBPROT0 or FBPROT1 register to 0x0001.

The block protect setting can be locked by the permanent block protect setting (PBPS or PBPS_SEC). When the permanent block protect setting and the block protect setting are 0, issuing a Program or Block erase command to user area of the code flash causes the flash sequencer to enter the command-locked state regardless of the FBPROT0 and FBPROT1 register settings.

Valid block protect setting (BPS or BPS_SEC) depends on the Block Protect Select bit (BPS_SEL).

See section 43.12.2. Permanent Block Protect Setting for details of the block protect setting and permanent block protect setting. See section 43.4.15. FBPROT0 : Flash Block Protection Register and section 43.4.16. FBPROT1 : Flash Block Protection for Secure Register for more information.

For details of block protect setting (BPS or BPS_SEC) and block protect select (BPS_SEL), see section 6, Option-Setting Memory.

The protected area by the block protect setting is always determined by the address of the FSADDR register setting regardless of the address swapping function setting (the startup area select). Table 43.19 to Table 43.20 show the relation of user area and the block protect setting in each function setting.

- BPS[0] to BPS[n] or BPS_SEC[0] to BPS_SEC[n] are assigned to the block of user area (for example, address is 0x00_0000 to the last block address).
- BPS[0]/BPS_SEC[0] and BPS[1]/BPS_SEC[1] are assigned to the block of user area depending on the startup area select setting (SAS.BTFLG bit). (See section 43.11.3. Start-Up Program Protection).

Table 43.19 shows the block protect setting when the startup area select is disabled (not swapping).

Table 43.20 show example of the block protect setting when the address conversion function is used.

Table 43.19 Example of Block Protect setting when SAS.BTFLG is 1

FSADDR[23:0]	Block size	Block protect setting	User area block number	Notes
The last block address	32 KB	BPS[n] or BPS_SEC[n]	Block n	—
⋮	⋮	⋮	⋮	—
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 9	—
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 8	—
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 7	—
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 6	—
⋮	⋮	⋮	⋮	—
0x00_2000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 1	Not swap block 0 and block 1 in this startup area select setting
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 0	Not swap block 0 and block 1 in this startup area select setting

43.11.1.2 FENTRYR的保护

当FENTRYR寄存器设置为0x0000时，闪存定序器进入读取模式。在读取模式下，无法接受FACI命令。如果尝试在读取模式下发出FACI命令，则闪存定序器进入命令锁定状态。

43.11.1.3 通过块保护设置进行保护

用户区的每个块都有块保护设置（BPS或BPS_SEC）。当FBPROT0或FBPROT1寄存器为0x0000且块保护位为0时，向代码闪存的用户区发出Program或BlockErase命令会导致命令锁定状态。要编程或擦除块保护位为0的块，请将FBPROT0或FBPROT1寄存器设置为0x0001。

块保护设置可以通过永久块保护设置（PBPS或PBPS_SEC）锁定。当永久块保护设置和块保护设置为0时，无论FBPROT0和FBPROT1寄存器设置如何，向代码闪存的用户区发出程序或块擦除命令都会使闪存定序器进入命令锁定状态。

有效的块保护设置（BPS或BPS_SEC）取决于块保护选择位（BPS_SEL）。

请参见第43.12.2节。永久块保护设置有关块保护设置和永久块保护设置的详细信息。请参见第43.4.15节。FBPROT0：闪存块保护寄存器和第43.4.16节。FBPROT1：安全寄存器的闪存块保护了解更多信息。

有关块保护设置（BPS或BPS_SEC）和块保护选择（BPS_SEL）的详细信息，请参阅第6节，选项设置Memory.

块保护设置的保护区域始终由FSADDR寄存器设置的地址决定，与地址交换功能设置（启动区域选择）无关。表43.19至表43.20显示了每个功能设置中用户区和块保护设置的关系。

●BPS[0]到BPS[n]或BPS_SEC[0]到BPS_SEC[n]分配给用户区的块（例如，地址是0x00_0000到最后一个块地址）。

●BPS[0]BPS_SEC[0]和BPS[1]BPS_SEC[1]根据启动区选择设置（SAS.BTFLG位）分配给用户区块。（参见第43.11.3节。启动程序保护）。

表43.19显示了禁用启动区域选择（不交换）时的块保护设置。

表43.20显示了使用地址转换功能时的块保护设置示例。

Table 43.19 SAS.BTFLG为1时的块保护设置示例

FSADDR[23:0]	块大小	块保护设置	用户区块号	Notes
最后一个区块地址	32 KB	BPS[n] or BPS_SEC[n]	Block n	—
⋮	⋮	⋮	⋮	—
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 9	—
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 8	—
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 7	—
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 6	—
⋮	⋮	⋮	⋮	—
0x00_2000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 1	不交换此启动区域中的块0和块1选择设置
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 0	不交换此启动区域中的块0和块1选择设置

Table 43.20 Example of Block Protect setting when SAS.BTFLG is 0

FSADDR[23:0]	Block size	Block protect setting	User area block number	Notes
The last block address	32 KB	BPS[n] or BPS_SEC[n]	Block n	—
⋮	⋮	⋮	⋮	—
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 9	—
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 8	—
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 7	—
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 6	—
⋮	⋮	⋮	⋮	—
0x00_2000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 0	Swap block 0 and block 1 in this startup area select setting
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 1	Swap block 0 and block 1 in this startup area select setting

43.11.2 Error Protection

Error protection detects the issuing of illegal FACI commands, illegal access, and flash sequencer malfunction. FACI command acceptance is disabled (command-locked state) in response to the detection of these errors. The flash memory cannot be programmed or erased while the flash sequencer is in the command-locked state. For release from the command-locked state, issue the Status Clear or Forced Stop command. The Status Clear command can only be used while the FRDY bit in the FSTATR register is 1. The Forced Stop command can be used regardless of the value of the FRDY bit. While the CMDLKIE bit in the FAEINT register is 1, a flash access error (FIFERR) interrupt is generated if the flash sequencer enters the command-locked state (the CMDLK bit in the FASTAT register is set to 1).

If the flash sequencer enters the command-locked state in response to a command other than the P/E suspend command during programming or erasure processing, the flash sequencer continues the processing for programming or erasure. In this state, the P/E suspend command cannot be used to suspend the processing for programming or erasure. If a command is issued in the command-locked state, the ILGLERR bit becomes 1 and the other bits retain the values set from previous error detection.

Table 43.21 shows the error protection types and status bit values after error detections.

Table 43.21 Error protection type (1 of 3)

Error type	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
FENTRYR setting error	The value set in FENTRYR is not 0x0000, 0x0001, or 0x0080	0	1	0	0	1	0	0	0	0	0
	The FENTRYR setting at suspension is different from that at resumption	0	1	0	0	1	0	0	0	0	0

Table 43.20 SAS.BTFLG为0时的块保护设置示例

FSADDR[23:0]	块大小	块保护设置	用户区块号	Notes
最后一个区块地址	32 KB	BPS[n] or BPS_SEC[n]	Block n	—
⋮	⋮	⋮	⋮	—
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 9	—
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 8	—
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 7	—
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 6	—
⋮	⋮	⋮	⋮	—
0x00_2000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 0	在此启动区域选择设置中交换块0和块1
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 1	在此启动区域选择设置中交换块0和块1

43.11.2 错误保护

错误保护检测非法FACI命令的发出、非法访问和闪存定序器故障。FACI命令接受被禁用（命令锁定状态）以响应检测到这些错误。闪存定序器处于命令锁定状态时，无法对闪存进行编程或擦除。要从命令锁定状态释放，请发出状态清除或强制停止命令。状态清除命令只能在FSTATR寄存器中的FRDY位为1时使用。无论FRDY位的值如何，都可以使用强制停止命令。当FAEINT寄存器中的CMDLKIE位为1时，如果闪存定序器进入命令锁定状态（FASTAT寄存器中的CMDLK位设置为1），则会产生闪存访问错误(FIFERR)中断。

如果闪存定序器在编程或擦除处理期间响应于除了PE暂停命令之外的命令而进入命令锁定状态，则闪存定序器继续进行编程或擦除处理。在这种状态下，PE挂起命令不能用于挂起编程或擦除处理。如果在命令锁定状态下发出命令，则ILGLERR位变为1，其他位保留先前错误检测设置的值。

表43.21显示了错误检测后的错误保护类型和状态位值。

Table 43.21 错误保护类型(1of3)

错误类型	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
FENTRYR设置错误	FENTRYR中设置的值不是0x0000、0x0001或0x0080	0	1	0	0	1	0	0	0	0	0
	暂停时的FENTRYR设置与恢复时的设置不同	0	1	0	0	1	0	0	0	0	0

Table 43.21 Error protection type (2 of 3)

Error type	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
Illegal command error	An undefined size is specified in the first cycle of the command. (not byte-write)	1	0	0	0	1	0	0	0	0	0
	An undefined code is written in the first access of the FACI command	1	0	0	0	1	0	0	0	0	0
	The value specified in the last access of the multiple-access FACI command is not 0xD0	1	0	0	0	1	0	0	0	0	0
	The value (N) specified in the second write access of the FACI command in the program or configuration set command is wrong	1	0	0	0	1	0	0	0	0	0
	Blank Check command is issued with inconsistent BCDIR, FSADDR, and FEADDR settings (see section 43.4.13. FEADDR : FACI Command End Address Register)	1	0	0	0	1	0	0	0	0	0/1 *1
	A multi block erase command is issued with inconsistent FSADDR and FEADDR settings. ● FSADDR > FEADDR ● FEADDR is set to reserved area.	1	0	0	0	1	0	0	0	0	0/1 *1
	An FACI command not acceptable in each mode is issued (see Table 43.15)	1	0	0	0	1	0	0	0	0	0
	An FACI command is issued when command acceptance conditions are not satisfied (see Table 43.16)	0/1	0/1	0/1	0/1	1	0/1	0/1	0/1	0/1	0/1
	A program or block erase command is issued against the area protected by the block protect setting (see section 43.11.1.3. Protection by Block Protect Setting)	1	0	0	0	1	0	0	0	0	0
	A program command is issued against the erase area in erase suspend	1	0	0	0	1	0	0	0	0	0
Erasure error	An error occurs during erasure	0	0	0	0	0	1	0	0	0	0
Programming error	An error occurs during programming	0	0	0	0	0	0	1	0	0	0
Code flash memory access violation	An FACI command is issued to the reserved portion of the user area in code flash P/E mode	0	0	0	0	1	0	0	0	1	0
	Configuration set command is issued to the reserved option-setting memory	0	0	0	0	1	0	0	0	1	0
	Configuration set command of non-secure access is issued to the secure region of TrustZone in the code flash	0	0	0	0	1	0	0	0	1	0
	Program or block erase command of non-secure access is issued to the secure region of user area.	0	0	0	0	1	0	0	0	1	0

Table 43.21 错误保护类型（2个，共3个）

错误类型	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
非法命令错误	在命令的第一个循环中指定了未定义的大小。（不是字节写入）	1	0	0	0	1	0	0	0	0	0
	在FACI命令的第一次访问中写入了未定义的代码	1	0	0	0	1	0	0	0	0	0
	多路访问FACI命令的最后一次访问指定的值不是0xD0	1	0	0	0	1	0	0	0	0	0
	程序或配置集命令中FACI命令的第二次写访问指定的值（N）错误	1	0	0	0	1	0	0	0	0	0
	使用不一致的BCDIR、FSADDR和FEADDR设置发出空白检查命令（请参阅第43.4.13节。 FEADDR:FACI命令结束地址 Register)	1	0	0	0	1	0	0	0	0	0/1 *1
	使用不一致的FSADDR和FEADDR设置发出多块擦除命令。● ● FEADDR设置为保留区域。	1	0	0	0	1	0	0	0	0	0/1 *1
	发出了在每种模式下都不可接受的FACI命令（参见表43.15）	1	0	0	0	1	0	0	0	0	0
	不满足命令接受条件时发出FACI命令（见表43.16）	0/1	0/1	0/1	0/1	1	0/1	0/1	0/1	0/1	0/1
	针对受块保护设置保护的区域发出编程或块擦除命令（参见第43.11.1.3节。块保护设置保护）	1	0	0	0	1	0	0	0	0	0
	在擦除挂起中针对擦除区域发出编程命令	1	0	0	0	1	0	0	0	0	0
擦除错误	擦除过程中发生错误	0	0	0	0	0	1	0	0	0	0
编程错误	编程过程中出现错误	0	0	0	0	0	0	1	0	0	0
代码闪存访问冲突	在代码闪存PE模式下，向用户区的保留部分发出FACI命令	0	0	0	0	1	0	0	0	1	0
	向保留的选项设置内存发出配置设置命令	0	0	0	0	1	0	0	0	1	0
	向代码闪存中的TrustZone的安全区域发出非安全访问的配置集命令	0	0	0	0	1	0	0	0	1	0
	对用户区的安全区域发出非安全访问的程序或块擦除命令。	0	0	0	0	1	0	0	0	1	0

Table 43.21 Error protection type (3 of 3)

Error type	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
Data flash memory access violation	A program or block erase command is issued to the reserved data area in data flash P/E mode	0	0	0	0	1	0	0	0	0	1
	A multi block erase command is issued to the reserved data area in data flash P/E mode. (FSADDR is set to reserved data area).	1	0	0	0	1	0	0	0	0	1
	Blank Check command is issued to reserved data area in data flash P/E mode. (FSADDR is set to reserved data area).	1	0	0	0	1	0	0	0	0	1
	A program, block erase, multi block erase, or blank check command of non-secure access is issued to the secure region of data area.	0	0	0	0	1	0	0	0	0	1
Security error	Configuration set command for the SAS.BTFLG bit setting is issued when the SAS.FSPR bit is 0 (see section 43.9.3.15. Configuration Set Command)	0	0	1	0	1	0	0	0	0	0
Others	An FACI command-issuing area is accessed in read mode	0	0	0	1	1	0	0	0	0	0
	An FACI command-issuing area is read in code flash P/E mode or data flash P/E mode	0	0	0	1	1	0	0	0	0	0
Flash write erase protection error	A flash memory write protection error is detected by the FWEPROR register setting*2 during command processing by the flash sequencer	0	0	0	0	0	0/1	0/1	1	0	0

Note 1. DFAE value depends on the FSADDR setting.
Note 2. For details on the FWEPROR register, see section 43.4.8. FWEPROR : Flash P/E Protect Register.

43.11.3 Start-Up Program Protection

Protection of the startup program is for protection of the program to be started after a reset (the startup program). This function provides a way to safely update the startup program when rewriting is suspended during a reset.

The startup area is 8 Kbytes in size and is assigned to the user area in the code flash memory. This function uses the values of the SAS.BTFLG bit and the FSUACR.SAS[1:0] bits to change the area where the startup program is stored in block units (see Figure 43.25 to Figure 43.28).

In protection of the startup program, the state of the selection of the startup area can be fixed by the FSPR bit. However, the SAS.FSPR bit never be restored to 1 once the flag is set to 0. Exercise extra caution when handling the SAS.FSPR bit.

Table 43.21 错误保护类型（3之3）

错误类型	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
数据闪存访问违规	在数据闪存PE模式下，向保留数据区域发出程序或块擦除命令	0	0	0	0	1	0	0	0	0	1
	在数据闪存PE模式下，向保留数据区域发出多块擦除命令。（FSADDR设置为保留数据区）。	1	0	0	0	1	0	0	0	0	1
	在数据闪存PE模式下，向保留数据区域发出空白检查命令。（FSADDR设置为保留数据区）。	1	0	0	0	1	0	0	0	0	1
	向数据区域的安全区域发出非安全访问的编程、块擦除、多块擦除或空白检查命令。	0	0	0	0	1	0	0	0	0	1
安全错误	当SAS.FSPR位为0时，发出SAS.BTFLG位设置的配置设置命令（请参阅第43.9.3.15节。配置设置命令）	0	0	1	0	1	0	0	0	0	0
Others	以读取模式访问FACI命令发布区域	0	0	0	1	1	0	0	0	0	0
	在代码闪存PE模式或数据闪存PE模式下读取FACI命令发布区域	0	0	0	1	1	0	0	0	0	0
Flash写擦除保护错误	在闪存定序器的命令处理期间，通过FWEPROR寄存器设置*2检测到闪存写保护错误	0	0	0	0	0	0/1	0/1	1	0	0

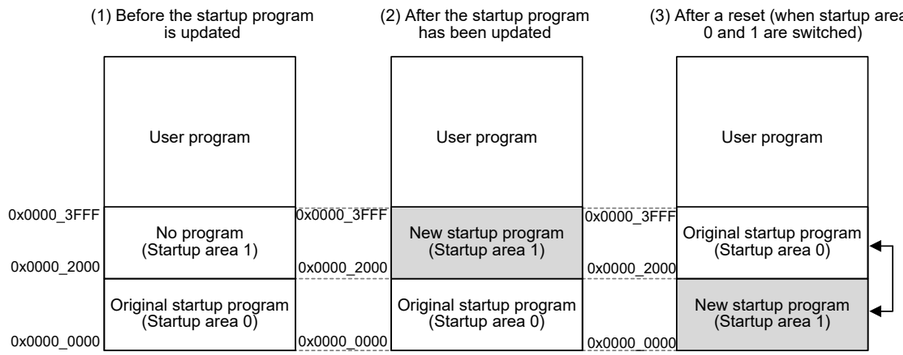
注1.DFAE值取决于FSADDR设置。
注2.关于FWEPROR寄存器的详细信息，请参阅第43.4.8节。FWEPROR：闪存PE保护寄存器。

43.11.3 启动程序保护

启动程序的保护是为了保护复位后要启动的程序（启动程序）。此功能提供了一种在复位期间暂停重写时安全更新启动程序的方法。

启动区大小为8KB，分配给代码闪存中的用户区。该函数使用SAS.BTFLG位和FSUACR.SAS[1:0]位的值来改变以块为单位存储启动程序的区域（见图43.25至图43.28）。

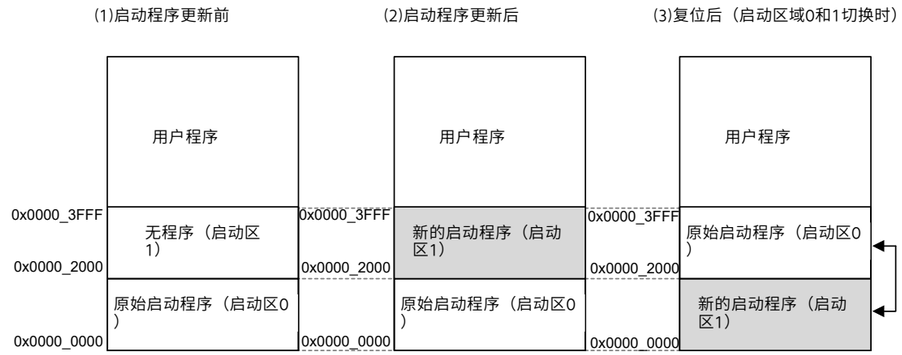
在启动程序的保护中，启动区域的选择状态可以通过FSPR位来固定。但是，那一旦标志设置为0，SAS.FSPR位永远不会恢复为1。处理SAS.FSPR位时要格外小心。



Note: The addresses are used for reading, programming, and erasure. Startup area 0 is erased when Block Erase command is issued for the address 0x00000000 with allocation shown under 3.

1. Before the startup program is updated
   When the SAS.BTFLG bit is 1 and the FSUACR.SAS[1:0] bits are 0xb, the address range from 0x00002000 to 0x00003FFF is selected as startup area 1 and the address range from 0x00000000 to 0x00001FFF is selected as startup area 0.
2. After the startup program has been updated
   A new startup program can be written to startup area 1. At this time, startup area 0 will still contain the previous startup program, so rewriting by starting up from startup area 0 remains possible if rewriting to the startup area 1 fails.
3. After a reset (when startup areas 0 and 1 are switched)
   When rewriting startup area 1 is successfully completed, switch the assignment of startup areas 0 and 1 by rewriting the startup area selection bit (the SAS.BTFLG bit) with Configuration set command. Afterwards, the program is started up from startup area 1 after a reset.

Figure 43.25 Concept of Protection of the Startup Program



Note: 这些地址用于读取、编程和擦除。当对地址0x00000000发出块擦除命令时，启动区域0被擦除，分配如下3所示。1.更新启动程序之前

当SAS.BTFLG位为1且FSUACR.SAS[1:0]位为0xb时，选择0x00002000到0x00003FFF的地址范围作为启动区1，选择从0x00000000到0x00001FFF的地址范围作为启动区0。2.启动程序更新后

可以将新的启动程序写入启动区1。此时启动区0仍会包含之前的启动程序，因此如果对启动区1的重写失败，仍然可以从启动区0启动进行重写。3.复位后（启动区域0和1切换时）

当重写启动区1成功完成时，通过使用Configurationset命令重写启动区选择位（SAS.BTFLG位）来切换启动区0和1的分配。之后，程序在复位后从启动区1启动。

Figure 43.25 保护启动程序的概念

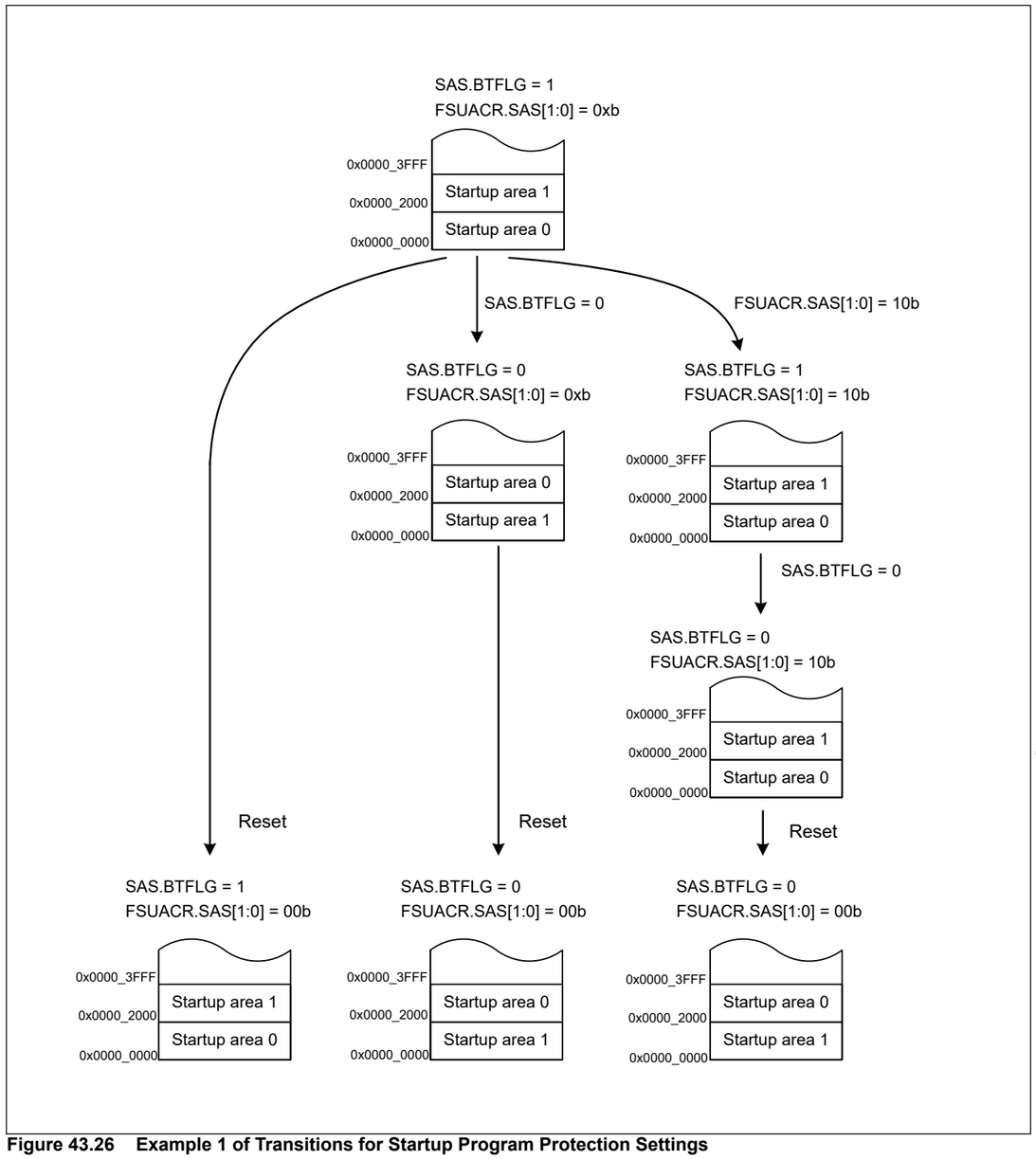


Figure 43.26 Example 1 of Transitions for Startup Program Protection Settings

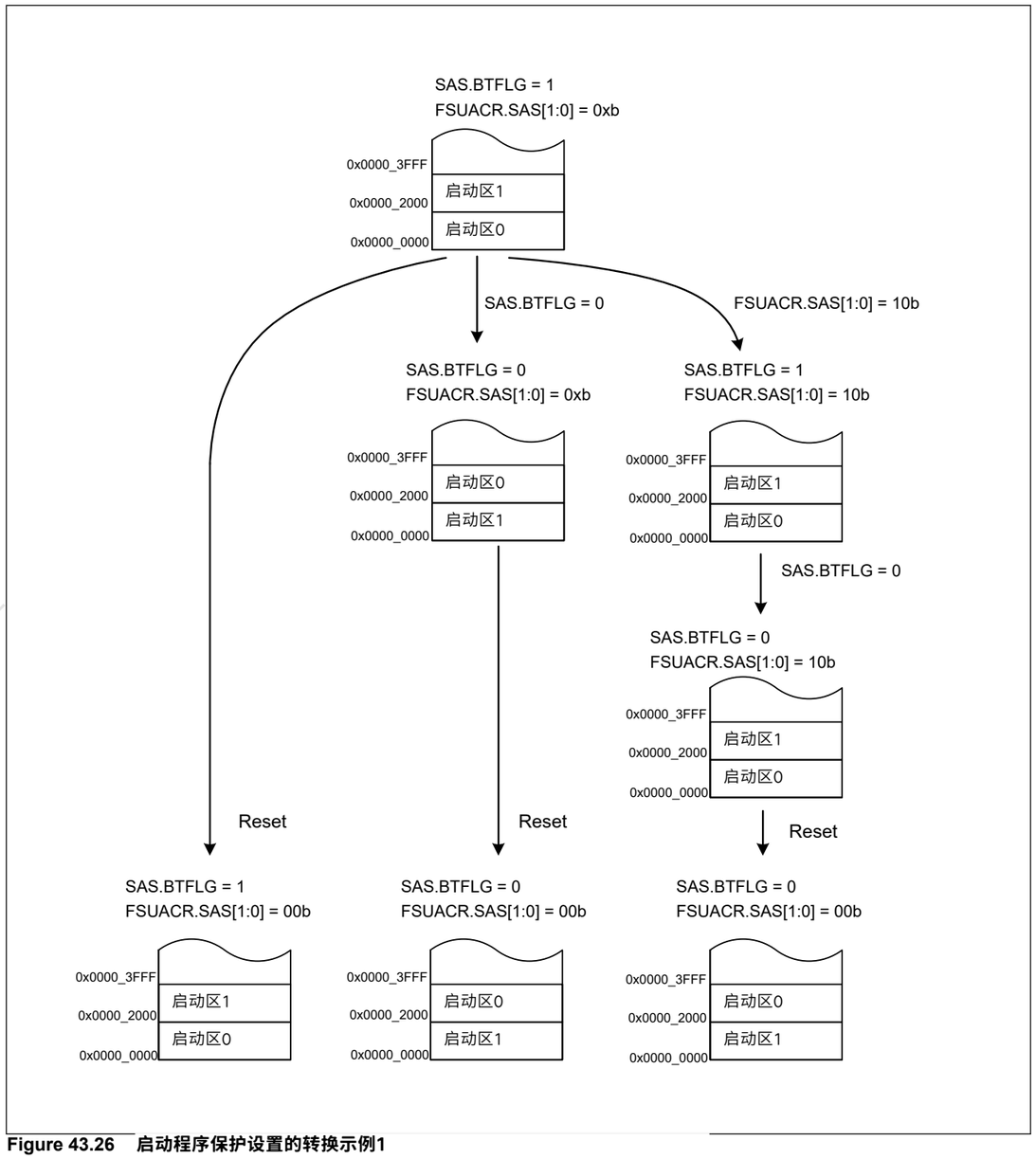


Figure 43.26 启动程序保护设置的转换示例1

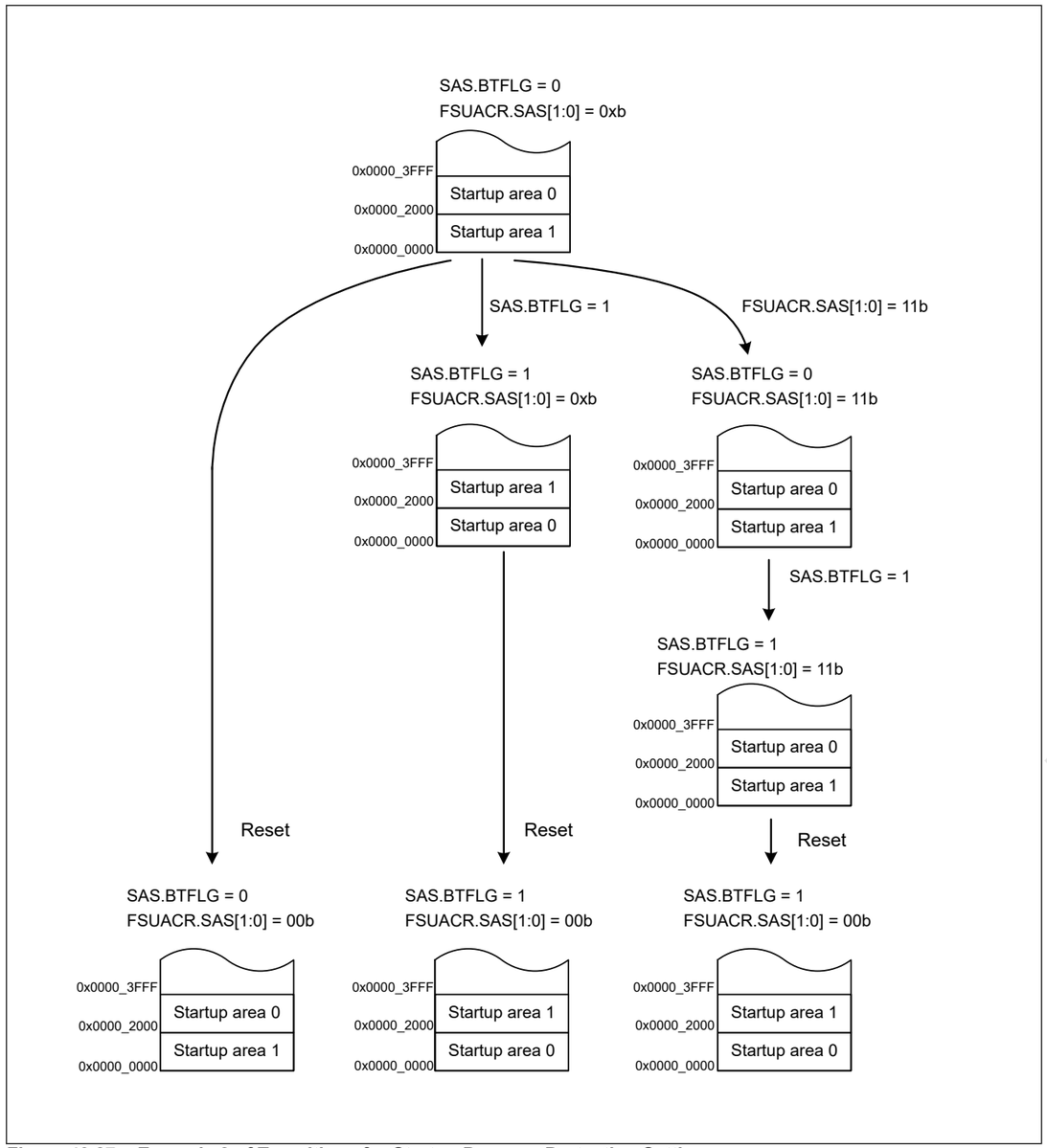


Figure 43.27 Example 2 of Transitions for Startup Program Protection Settings

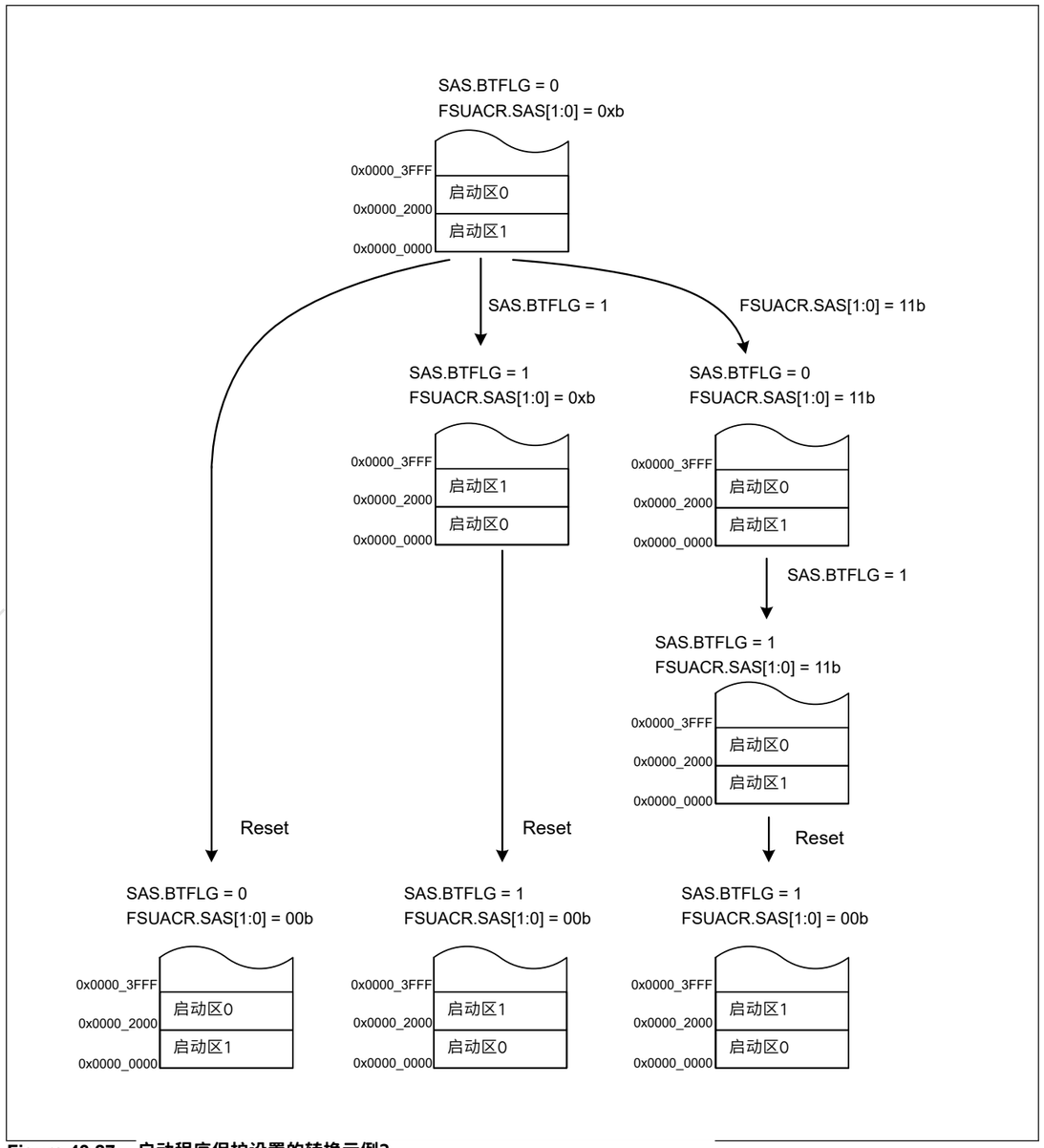
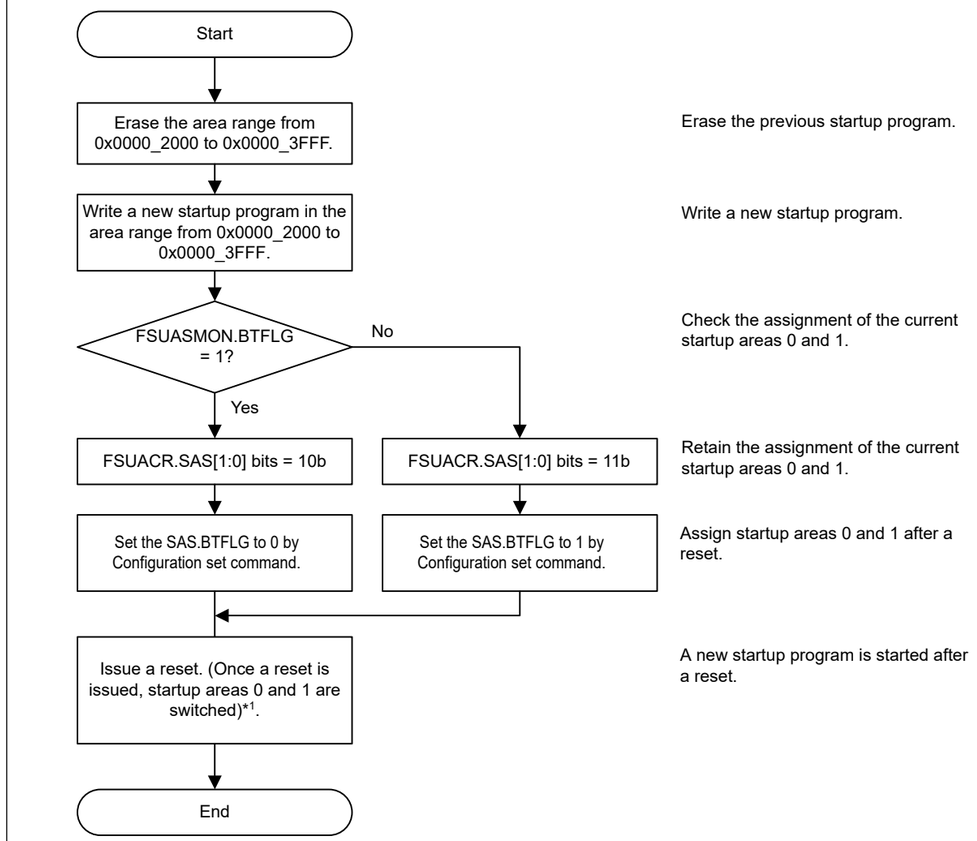


Figure 43.27 启动程序保护设置的转换示例2



Note 1. For details, see Figure 43.26 and Figure 43.27.

Figure 43.28 Concept of Protection of the Startup Program

43.12 Security Function

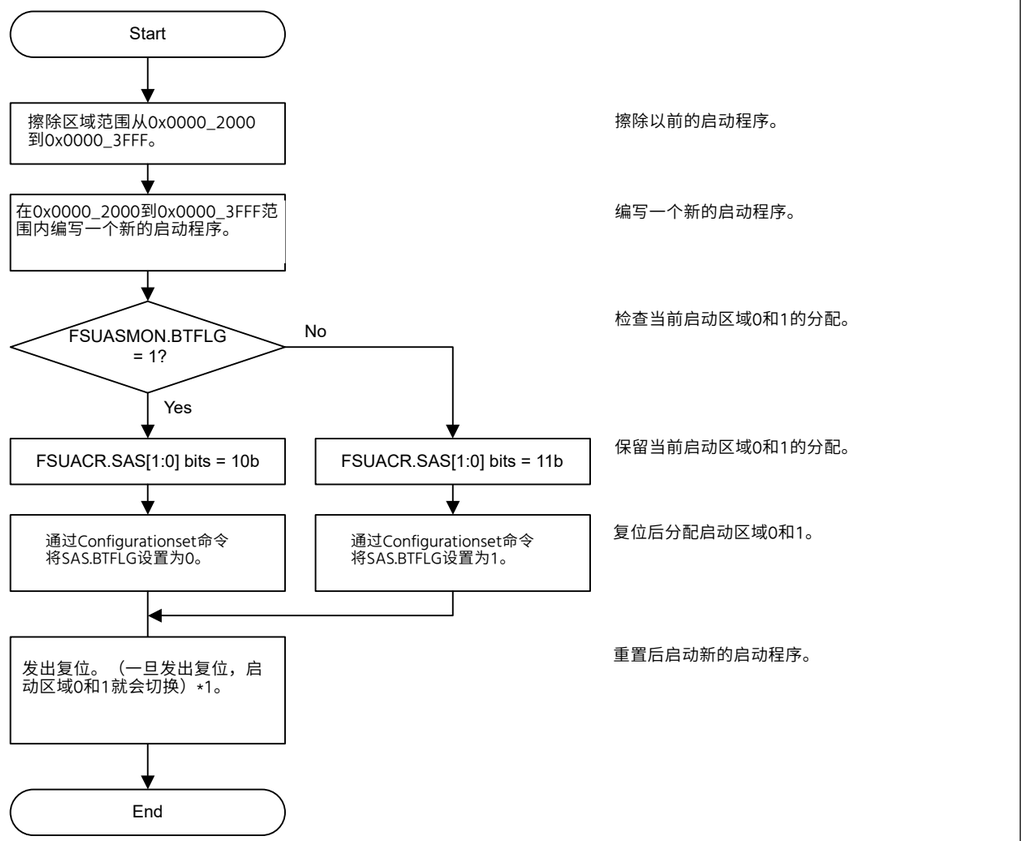
The flash sequencer supports the following security functions:

- Security flag for startup area
- Permanent block protect setting
- Flash memory protection for TrustZone

43.12.1 Security Flag for Startup Area Select

The security flag (SAS.FSPR) for the startup area is located in the option-setting memory.

When the SAS.FSPR bit is 0, issuing the configuration set command to change the SAS.BTFLG bit causes the flash sequencer to be in the command-locked state. Also, when the SAS.FSPR bit is 0, it is invalid to write to the Startup Area Select bits SAS[1:0] in the FSUACR register. The SAS.FSPR bit enables protection.



注1.详见图43.26和图43.27。

Figure 43.28 保护启动程序的概念

43.12 安全功能

闪存定序器支持以下安全功能：

●启动区安全标志

●永久封锁保护设置

●TrustZone的闪存保护

43.12.1 启动区域选择的安全标志

启动区域的安全标志(SAS.FSPR)位于选项设置内存中。

当SAS.FSPR位为0时，发出配置设置命令来更改SAS.BTFLG位会导致闪存定序器处于命令锁定状态。此外，当SAS.FSPR位为0时，写入FSUACR寄存器中的启动区域选择位SAS[1:0]无效。SAS.FSPR位启用保护。

43.12.2 Permanent Block Protect Setting

The permanent block protect setting is the clear protection for the block protection setting. User area cannot be permanently updated by the FACI command when the permanent block protect setting is enabled. See section 43.11.1.3. Protection by Block Protect Setting for more details.

The block protect setting and the permanent block protect setting have the write/clear protection against the configuration set command. The flash sequencer does not detect an error when the configuration set command is issued to the write/clear protected settings.

Figure 43.29 and Table 43.22 show the write/clear protection against the block protect setting (BPS[n]) and the permanent protect setting (PBPS[n]). Figure 43.30 and Table 43.23 show the write/clear protection against the block protect setting for secure (BPS_SEC[n]) and permanent protect setting for secure (PBPS_SEC[n]).

Effective permanent block protect setting (PBPS or PBPS_SEC) depends on block protect select (BPS_SEL). For details of permanent block protect setting (PBPS or PBPS_SEC) and block protect select (BPS_SEL), see section 6, Option-Setting Memory.

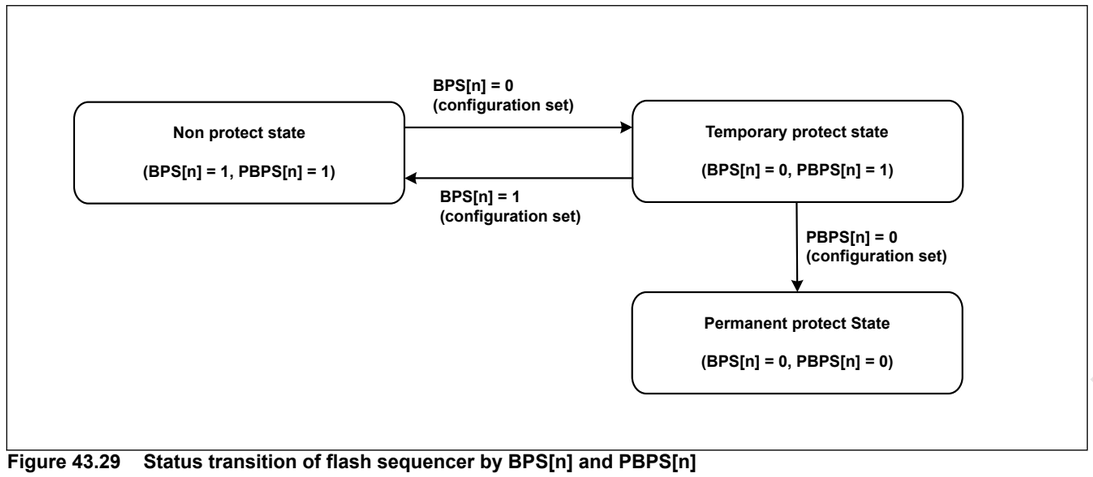


Figure 43.29 Status transition of flash sequencer by BPS[n] and PBPS[n]

Table 43.22 Write/clear protection of BPS[n] and PBPS[n]

Current state		Updatable state by configuration set command			
BPS[n]	PBPS[n]	BPS[n] = 1	BPS[n] = 0	PBPS[n] = 1	PBPS[n] = 0
1	1	✓	✓	✓	X
1	0	—	—	—	—
0	1	✓	✓	✓	✓
0	0	X	✓	X	✓

Note:
- ✓ indicates updatable by configuration set command.
- X indicates not updatable by configuration set command (error does not occur).
- — indicates not reaching to this state.

43.12.2 永久块保护设置

永久块保护设置是对块保护设置的明确保护。启用永久块保护设置后，FACI命令无法永久更新用户区域。请参阅第43.11.1.3节。通过块保护设置进行保护以获取更多详细信息。

块保护设置和永久块保护设置具有针对配置集命令的写清除保护。向写清除保护设置发出配置设置命令时，闪存定序器不会检测到错误。

图43.29和表43.22显示了针对块保护设置(BPS[n])和永久保护设置(PBPS[n])的写清除保护。图43.30和表43.23显示了针对安全的块保护设置(BPS_SEC[n])和安全的永久保护设置(PBPS_SEC[n])的写清除保护。

有效的永久块保护设置（PBPS或PBPS_SEC）取决于块保护选择（BPS_SEL）。有关永久块保护设置（PBPS或PBPS_SEC）和块保护选择（BPS_SEL）的详细信息，请参见第6节，选项设置存储器。

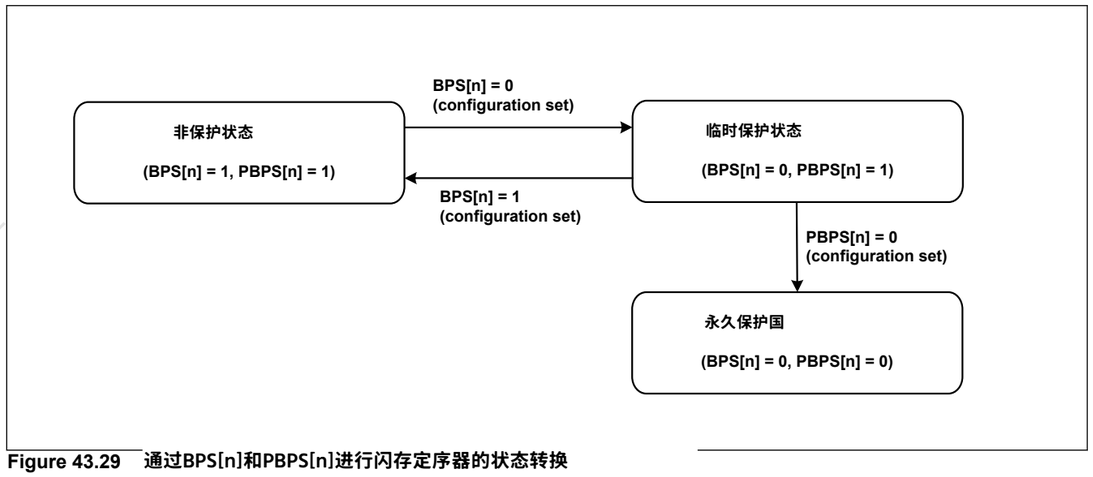


Figure 43.29 通过BPS[n]和PBPS[n]进行闪存定序器的状态转换

Table 43.22 BPS[n]和PBPS[n]的写清除保护

当前状态		可通过配置设置命令更新状态			
BPS[n]	PBPS[n]	BPS[n] = 1	BPS[n] = 0	PBPS[n] = 1	PBPS[n] = 0
1	1	✓	✓	✓	X
1	0	—	—	—	—
0	1	✓	✓	✓	✓
0	0	X	✓	X	✓

Note:
- 表示可通过配置设置命令更新。
- X表示不能通过配置设置命令更新（不发生错误）。
- —表示未达到此状态。

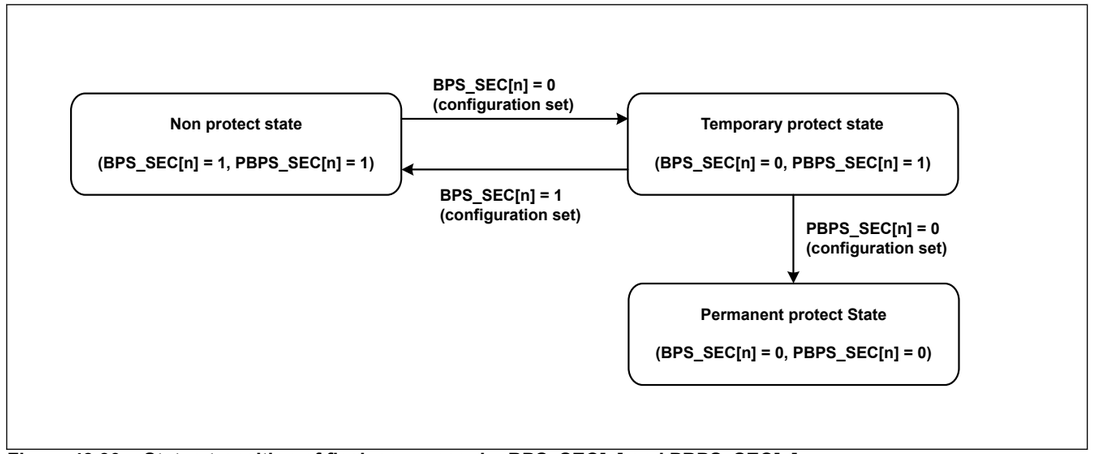


Figure 43.30 Status transition of flash sequencer by BPS_SEC[n] and PBPS_SEC[n]

Table 43.23 Write/clear protection of BPS_SEC[n] and PBPS_SEC[n]

Current state		Updatable state by configuration set command			
BPS_SEC[n]	PBPS_SEC[n]	BPS_SEC[n] = 1	BPS_SEC[n] = 0	PBPS_SEC[n] = 1	PBPS_SEC[n] = 0
1	1	✓	✓	✓	X
1	0	—	—	—	—
0	1	✓	✓	✓	✓
0	0	X	✓	X	✓

Note:
- ✓ indicates updatable by configuration set command.
- X indicates not updatable by configuration set command (error does not occur).
- — indicates not reaching to this state.

43.12.3 Flash Memory Protection for TrustZone

Information in this section focuses on the flash sequencer operation.

The flash memory provides the following types of protect function against non-secure access:

- Protection for flash memory area (P/E)
- Protection for flash memory area (read)
- Protection for registers
- Protection during FACI command operation
- Code flash P/E mode entry protection

43.12.3.1 Protection for Flash Memory Area (P/E)

This function protects the secure region of the code flash and data flash from FACI commands of non-secure access. The condition of protection depends on the FACI command, the access attribution, and the memory boundary setting.

For details of secure region, see section 45, Security Features .

See Table 43.24 for information on protection of the flash memory area (P/E).

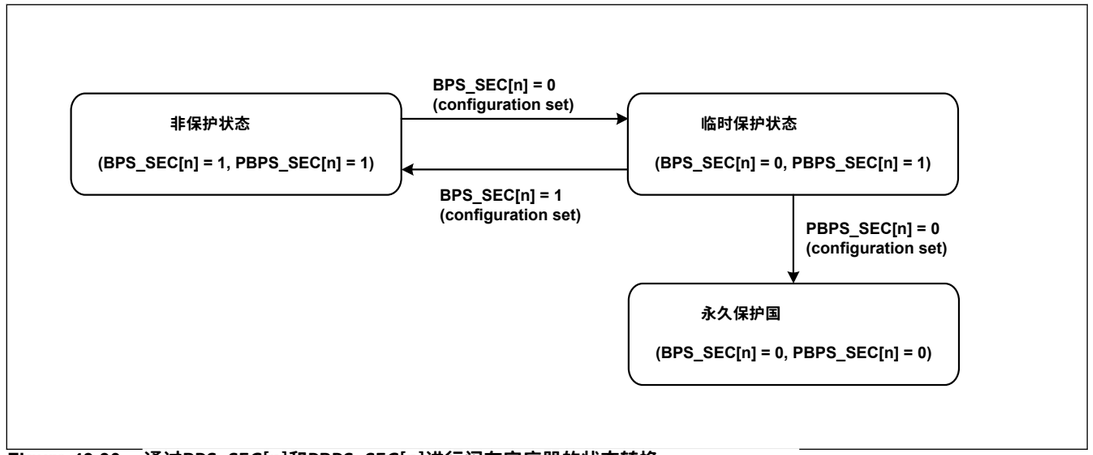


Figure 43.30 通过BPS_SEC[n]和PBPS_SEC[n]进行闪存定序器的状态转换

Table 43.23 BPS_SEC[n]和PBPS_SEC[n]的写清除保护

当前状态		可通过配置设置命令更新状态			
BPS_SEC[n]	PBPS_SEC[n]	BPS_SEC[n] = 1	BPS_SEC[n] = 0	PBPS_SEC[n] = 1	PBPS_SEC[n] = 0
1	1	✓	✓	✓	X
1	0	—	—	—	—
0	1	✓	✓	✓	✓
0	0	X	✓	X	✓

Note:
- 表示可通过配置设置命令更新。
- X表示不能通过配置设置命令更新（不发生错误）。
- 一表示未达到此状态。

43.12.3 TrustZone的闪存保护

本节中的信息侧重于闪存定序器的操作。

闪存提供以下类型的保护功能以防止非安全访问：

- ●保护闪存区（PE）
- ●保护闪存区域（读取）
- ●寄存器保护
- ●FACI命令操作期间的保护
- ●CodeflashPE模式进入保护

43.12.3.1 对闪存区域(PE)的保护

此功能保护代码闪存和数据闪存的安全区域免受非安全访问的FACI命令的影响。保护条件取决于FACI命令、访问属性和内存边界设置。

有关安全区域的详细信息，请参阅第45节，安全功能。

有关保护闪存区域(PE)的信息，请参见表43.24。

Table 43.24 Protection for the flash memory area (P/E)

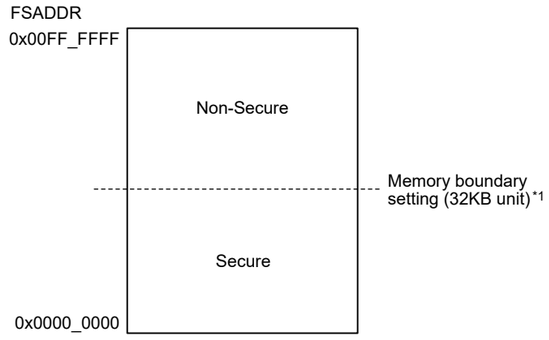
FACI command	Target area		Issuing of FACI command by non-secure access	Issuing of FACI command by secure access
Program Block erase	Code flash memory	User area (non-secure area)	✓	✓
		User area (secure area)	X	✓
	Data flash memory	Data area (non-secure area)	✓	✓
		Data area (secure area)	X	✓
Multi block erase Blank check	Data flash memory	Data area (non-secure area)	✓	✓
		Data area (secure area)	X	✓
Configuration set	Code flash memory	option-setting memory (non-secure area)	✓	✓
		option-setting memory (secure area)	X	✓

Note:
- ✓ indicates FACI command operation is not prohibited.
- X indicates FACI command operation is prohibited. Error occurs when the area is selected, and the FACI command is executed.

When the target area of FACI command is the user area of code flash, the flash sequencer compares the FSADDR register setting with the memory boundary setting of the code flash and determines whether the target area is in the secure region.

The memory boundary can be set to 0x0000_0000 to 0x00FF_8000 in 32 KB unit.

Figure 43.31 shows details of the non-secure/secure attribute of user area in the code flash.



Note 1. Comparing FSADDR with memory boundary setting of user area and judges whether the target area is in secure area.

Figure 43.31 Secure/non-secure region in user area

When the target area of the issuing FACI command is the data area of data flash, the flash sequencer compares the FSADDR/FEADDR register setting with the memory boundary setting of the data flash and determines whether the target area is in secure region. The memory boundary can be set to 0x0800_0000 to 0x0800_FC00 in 1 KB unit. Figure 43.32 shows details of the non-secure/secure attribute of data area in the data flash.

Table 43.24 对闪存区域(PE)的保护

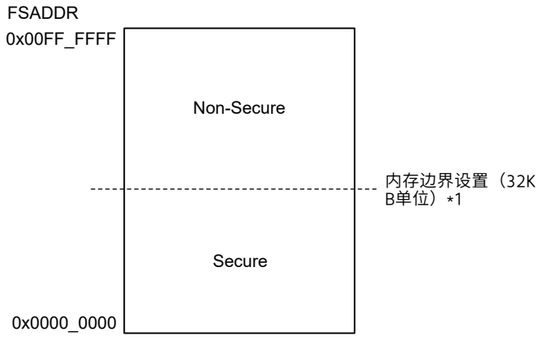
FACI命令	目标区域		通过非安全访问发出FACI命令	通过安全访问发出FACI命令
Program 块擦除	代码闪存	用户区（非安全区）	✓	✓
		用户区（安全区）	X	✓
	数据闪存	数据区（非安全区）	✓	✓
		数据区（安全区）	X	✓
多块擦除 空白支票	数据闪存	数据区（非安全区）	✓	✓
		数据区（安全区）	X	✓
配置集	代码闪存	option-setting memory (non-secure area)	✓	✓
		option-setting memory (secure area)	X	✓

Note:
- 表示不禁止FACI命令操作。
- X表示禁止FACI命令操作。选择区域时发生错误，执行FACI命令。

当FACI命令的目标区域是代码闪存的用户区域时，闪存定序器将FSADDR寄存器设置与代码闪存的内存边界设置进行比较，并确定目标区域是否在安全区域中。

内存边界可以以32KB为单位设置为0x0000_0000到0x00FF_8000。

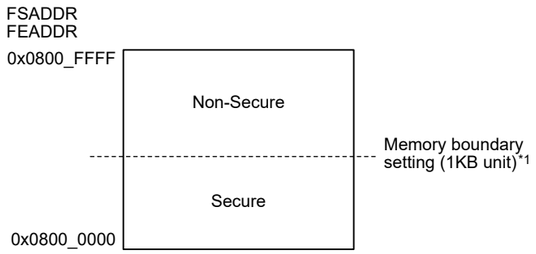
图43.31显示了代码flash中用户区的non-secure安全属性的详细信息。



注1.将FSADDR与用户区的内存边界设置进行比较，判断目标区是否在安全区。

Figure 43.31 用户区域中的安全非安全区域

当发出FACI命令的目标区域是数据flash的数据区域时，flashsequencer比较FSADDRFEADDR寄存器设置与数据闪存的内存边界设置并确定目标区域是否在安全区域中。内存边界可以以1KB为单位设置为0x0800_0000到0x0800_FC00。图43.32显示了数据闪存中数据区域的非安全安全属性的详细信息。



Note 1. Comparing FSADDR/FEADDR with memory boundary setting of data area and judges whether the target area is in secure area.

Figure 43.32 Secure/non-secure region in data area

See Figure 43.33 in the details of non-secure/secure region of option-setting memory. The flash sequencer judges that target area is secure region from the FSADDR register setting.

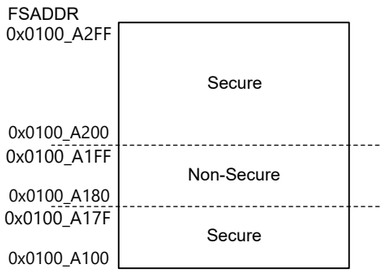


Figure 43.33 Secure/non-secure region in option-setting memory

43.12.3.2 Protection for Flash Memory Area (Read)

This function protects the secure region of code flash and data flash from non-secure bus access.

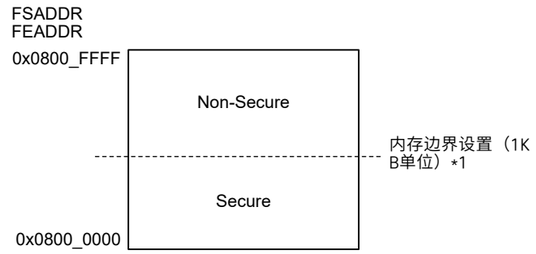
For details of secure region, see section 45, Security Features .

43.12.3.3 Protection for Register

The flash sequencer registers have write-access protection against non-secure access. Table 43.25 shows details of the protected registers of the flash sequencer.

Table 43.25 Protected registers of the flash sequencer for TrustZone (1 of 2)

Protection target register	Security attribute setting	Notes
FCKMHZ	Security attribution register setting (FSAR.FCKMHZSA)	See section 43.4.4. FSAR : Flash Security Attribution Register
FMEPROT	Always secure	See section 43.4.14. FMEPROT : Flash P/E Mode Entry Protection Register



注1.将FSADDRFEADDR与数据区域的内存边界设置进行比较，判断目标区域是否在安全区域。

Figure 43.32 数据区域中的安全非安全区域

有关选项设置内存的非安全安全区域的详细信息，请参见图43.33。闪存定序器根据FSADDR寄存器设置判断目标区域是安全区域。

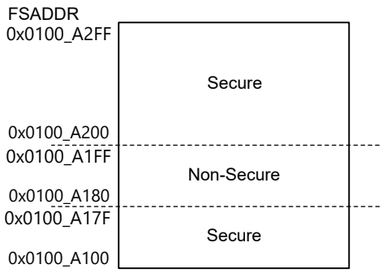


Figure 43.33 选项设置内存中的安全非安全区域

43.12.3.2 保护闪存区域（读取）

该功能保护代码闪存和数据闪存的安全区域免受非安全总线访问。

有关安全区域的详细信息，请参阅第45节，安全功能。

43.12.3.3 注册保护

闪存定序器寄存器具有针对非安全访问的写访问保护。表43.25显示了闪存定序器的受保护寄存器的详细信息。

Table 43.25 TrustZone的闪存定序器的受保护寄存器（1of2）

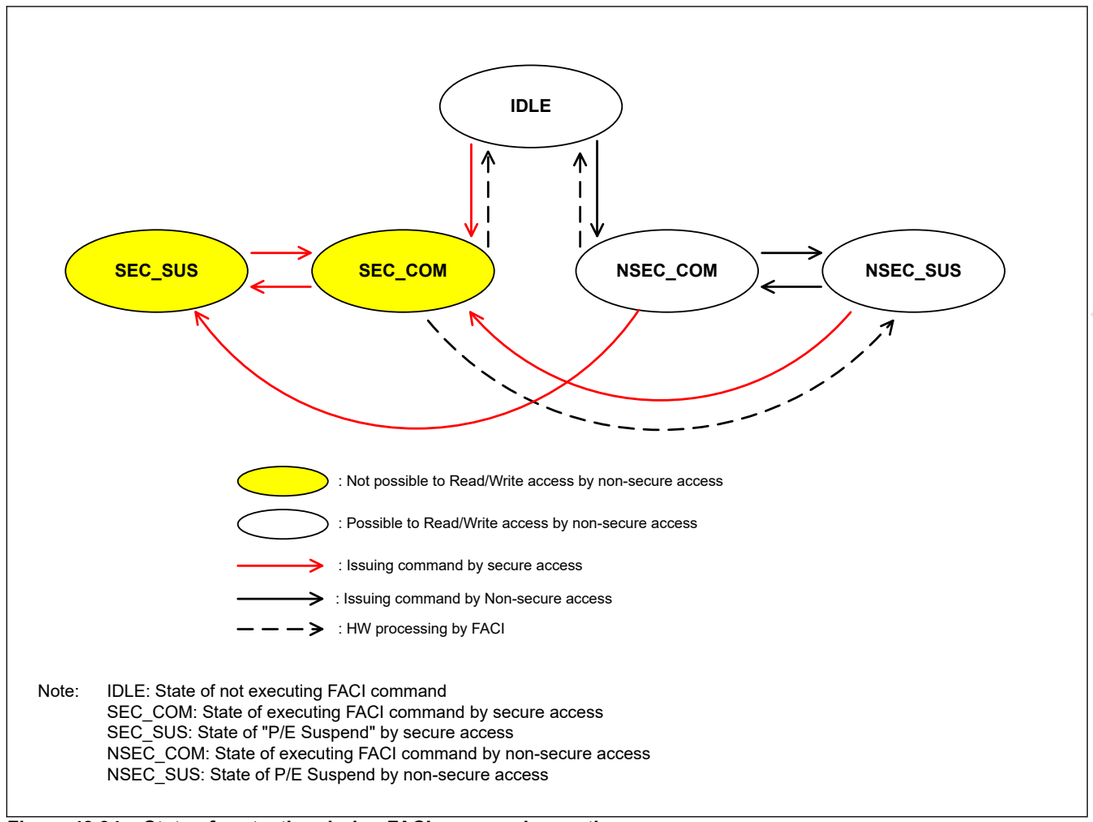
保护对象寄存器	安全属性设置	Notes
FCKMHZ	安全属性寄存器设置(FSAR.FCKMHZSA)	请参见第43.4.4节。FSAR：闪存安全归属登记
FMEPROT	始终安全	请参阅第43.4.14节。FMEPROT:闪存PE模式进入保护寄存器

Table 43.25 Protected registers of the flash sequencer for TrustZone (2 of 2)

Protection target register	Security attribute setting	Notes
FBPROT1	Always secure	See section 43.4.16. FBPROT1 : Flash Block Protection for Secure Register
FSUACR	Always secure	See section 43.4.27. FSUACR : Flash Startup Area Control Register
FACI command-issuing area and all registers of FACI (Base address is FACI) and FWEPROR register	During FACI command processing by secure access	See section 43.12.3.4. Protection during FACI Command Operation

43.12.3.4 Protection during FACI Command Operation

This function protects read/write access to the FACI command-issuing area, including all registers of FACI (Base address is FACI) and FWEPROR register by the non-secure access during the FACI command processing of the secure access. The protect condition includes the suspending period of the program, block erase, or multi block erase command by the P/E suspend command of the secure access. See Figure 43.34 and Table 43.26 for details of the protection during the FACI command operation.



Note: IDLE: State of not executing FACI command
SEC_COM: State of executing FACI command by secure access
SEC_SUS: State of "P/E Suspend" by secure access
NSEC_COM: State of executing FACI command by non-secure access
NSEC_SUS: State of P/E Suspend by non-secure access

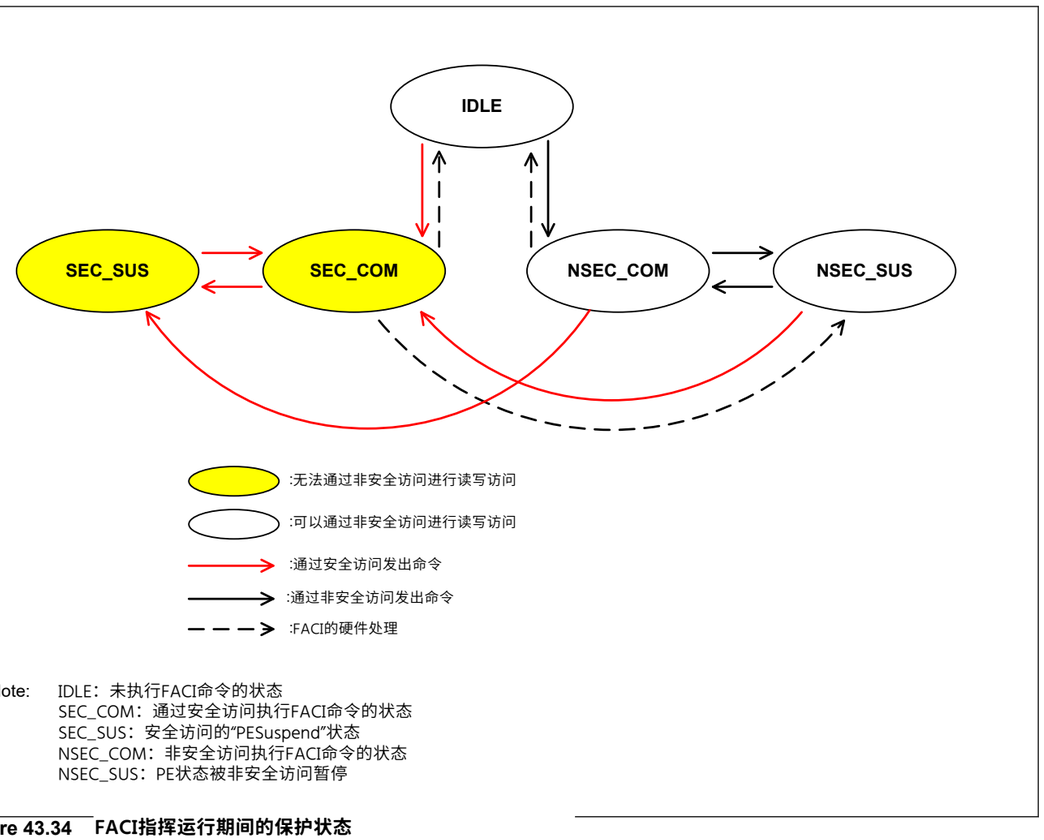
Figure 43.34 State of protection during FACI command operation

Table 43.25 TrustZone的闪存定序器的受保护寄存器（2个中的2个）

保护对象寄存器	安全属性设置	Notes
FBPROT1	始终安全	请参见第43.4.16节。FBPROT1：闪存安全寄存器的块保护
FSUACR	始终安全	请参阅第43.4.27节。FSUACR:闪光启动区控制寄存器
FACI命令发布区和FACI的所有寄存器（基地址为FACI）和FWEPROR寄存器	通过安全访问处理FACI命令期间	请参阅第43.12.3.4节。保护期间FACI命令操作

43.12.3.4 FACI指挥行动期间的保护

此功能保护对FACI命令发布区域的读写访问，包括FACI的所有寄存器（基地址为FACI)和FWEPROR在安全访问的FACI命令处理期间由非安全访问注册。保护条件包括程序的暂停周期、块擦除或由安全访问的PE暂停命令执行的多块擦除命令。FACI命令操作期间的保护细节见图43.34和表43.26。



Note: IDLE：未执行FACI命令的状态
SEC_COM：通过安全访问执行FACI命令的状态
SEC_SUS：安全访问的“PESuspend”状态
NSEC_COM：非安全访问执行FACI命令的状态
NSEC_SUS：PE状态被非安全访问暂停

Figure 43.34 FACI指挥运行期间的保护状态

Table 43.26 Protection during FACI command operation

	Flash sequencer is not operating			Program, Block erase, Multi block erase, Blank check, or Configuration set command processing		Command lock state		Forced stop command processing		While suspend Program, Block erase, or Multi block erase command		Program command processing while suspend Block erase or Multi block erase command by secure access		Program command processing while suspend Block erase or Multi block erase command by non-secure access		P/E resume command processing while suspend Program, Block erase, or Multi block erase command by secure access		P/E Resume command processing while suspend Program, Block erase, or Multi block erase command by non-secure access	
FACI command attribute	—	S	NS	S	NS	S	NS	S	NS	S	NS *1	S	NS	S	NS *1	S	NS	S	NS
FRDY bit	1	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0		
PRGSPD or ERSSPD bit	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0		
CMDLK bit	0	0	0	1	1	1/0	1/0	1/0	1/0	0	0	0	0	0	0	0	0		
Non-secure access	✓	X	✓	✓	✓	X	✓	X	✓	X	✓	X	✓	X	✓	X	✓		

Note:
- S indicates the FACI command by the secure access.
- NS indicates the FACI command by the non-secure access.
- ✓ indicates read/write access is possible by the non-secure access.
- X indicates read/write access is not possible by the non-secure access. Write data is ignored and read data is always 0.

Note 1. The FACI command issued by the non-secure access is not allowed.

Code flash programming/erasure can be protected by the FMEPROT register of secure function. Therefore, it does not assume that secure function issues P/E suspend command during code flash programming/erasure of non-secure function.

Data flash programming/erasure of non-secure can be suspended by secure function. If secure function issues P/E suspend command during data flash programming/erasure of non-secure function, secure function should issue P/E resume command. When secure function issues P/E resume command, secure function should notify non-secure function that data flash programming/erasure is complete and return to non-secure function. See Figure 43.35 and Figure 43.36 in example of issuing P/E suspend of secure function during programming/erasure of non-secure function.

Table 43.26 FACI命令操作期间的保护

	闪存定序器未运行		检查或配置设置命令编程、块擦除、多块擦除、空白processing		命令锁定状态		强制停止指令处理		块擦除命令暂停编程、块擦除或多		安全访问块擦除或多块擦除命令由暂停时的程序命令处理		non-secure access块擦除或多块擦除命令由暂停时的程序命令处理		通过安全访问擦除命令暂停编程、块擦除或多块PE恢复命令处理while		通过非安全访问擦除命令暂停编程、块擦除或多块PE恢复命令处理while	
FACI命令属性	—	S	NS	S	NS	S	NS	S	NS	S	NS *1	S	NS	S	NS *1	S	NS		
FRDY bit	1	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0		
PRGSPD或ERSSPD位	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0		
CMDLK bit	0	0	0	1	1	1/0	1/0	1/0	1/0	0	0	0	0	0	0	0	0		
Non-secure access	✓	X	✓	✓	✓	X	✓	X	✓	X	✓	X	✓	X	✓	X	✓		

Note:
- S表示通过安全访问的FACI命令。
- NS通过非安全访问指示FACI命令。
- 表示非安全访问可以进行读写访问。
- X表示非安全访问无法进行读写访问。写入数据被忽略，读取数据始终为0。

注1.非安全访问发出的FACI命令是不允许的。

代码闪存编程擦除可以通过安全功能的FMEPROT寄存器进行保护。因此，不假设安全功能在非安全功能的代码闪存编程擦除期间发出PE挂起命令。

非安全的数据闪存编程擦除可以通过安全功能暂停。如果在非安全功能的数据闪存编程擦除期间安全功能发出PE暂停命令，安全功能应发出PE恢复命令。当安全功能发出PEresume命令时，安全功能应通知非安全功能数据闪存编程擦除完成并返回到非安全功能。在对非安全功能进行编程擦除时发出PE暂停安全功能的示例请参见图43.35和图43.36。

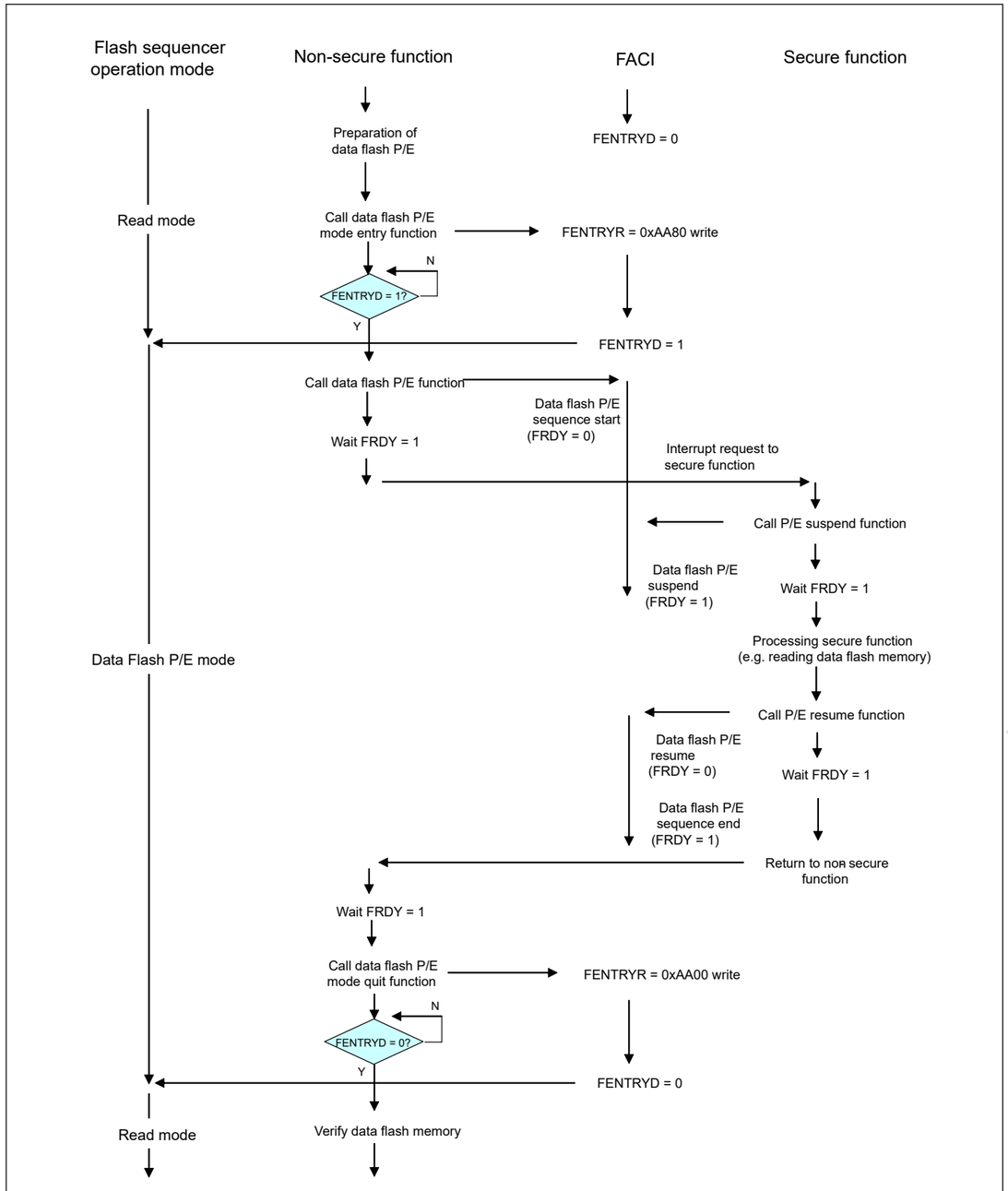


Figure 43.35 Data Flash P/E suspend of secure function Example (Check FRDY bit to detect P/E end)

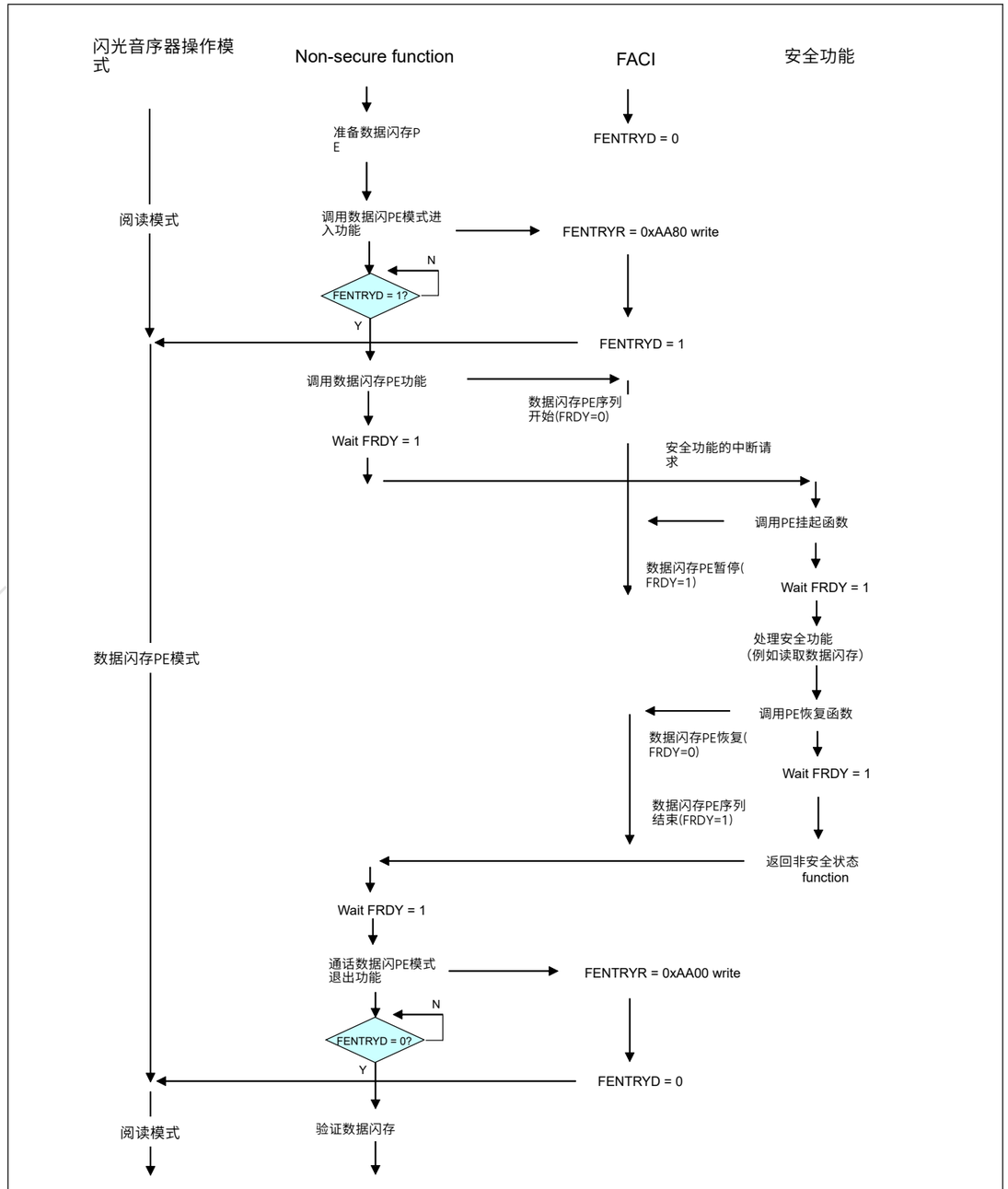


Figure 43.35 数据闪存PE安全功能暂停示例（检查FRDY位以检测PE结束）

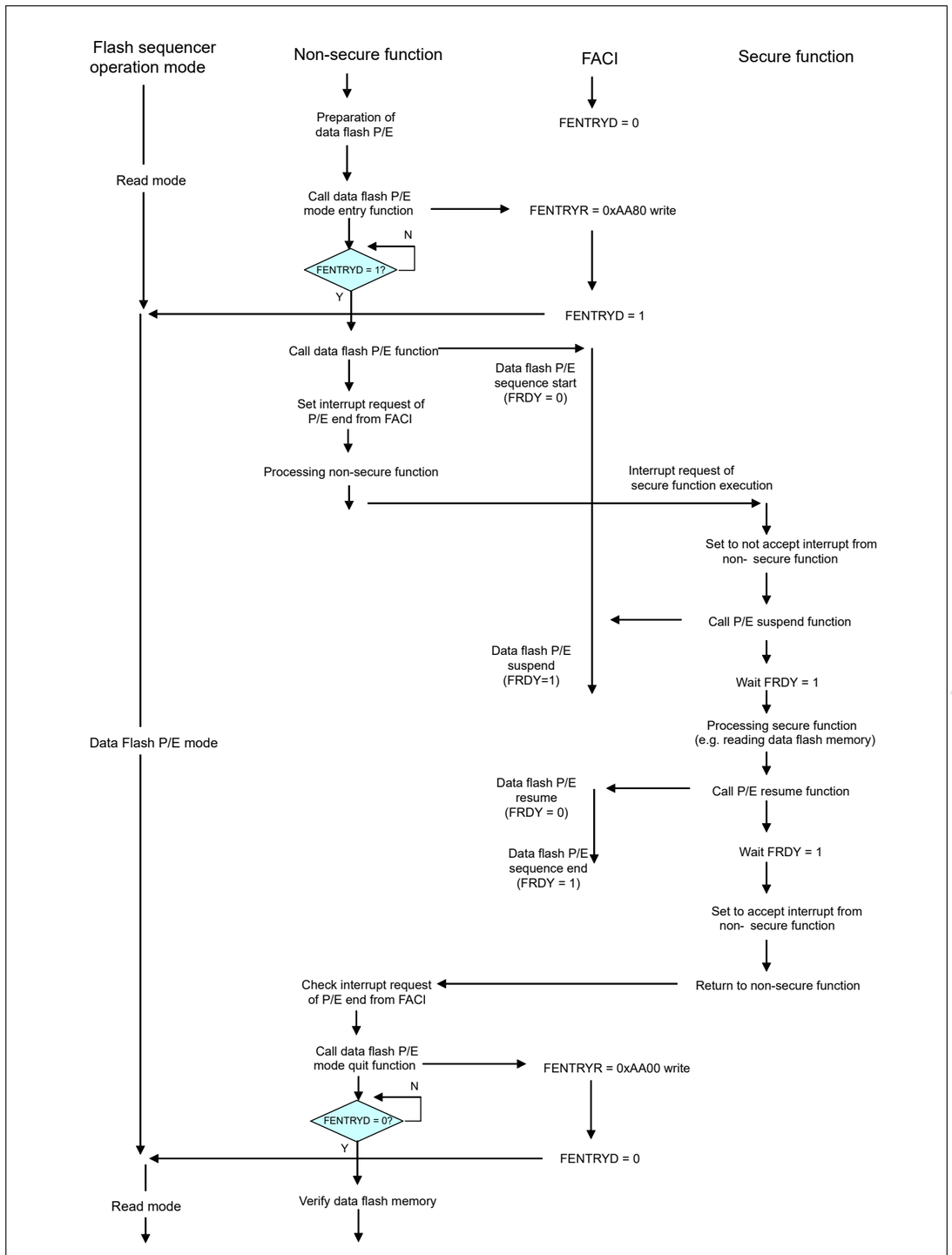


Figure 43.36 Data Flash P/E suspend of secure function Example (Check interrupt request to detect P/E end)

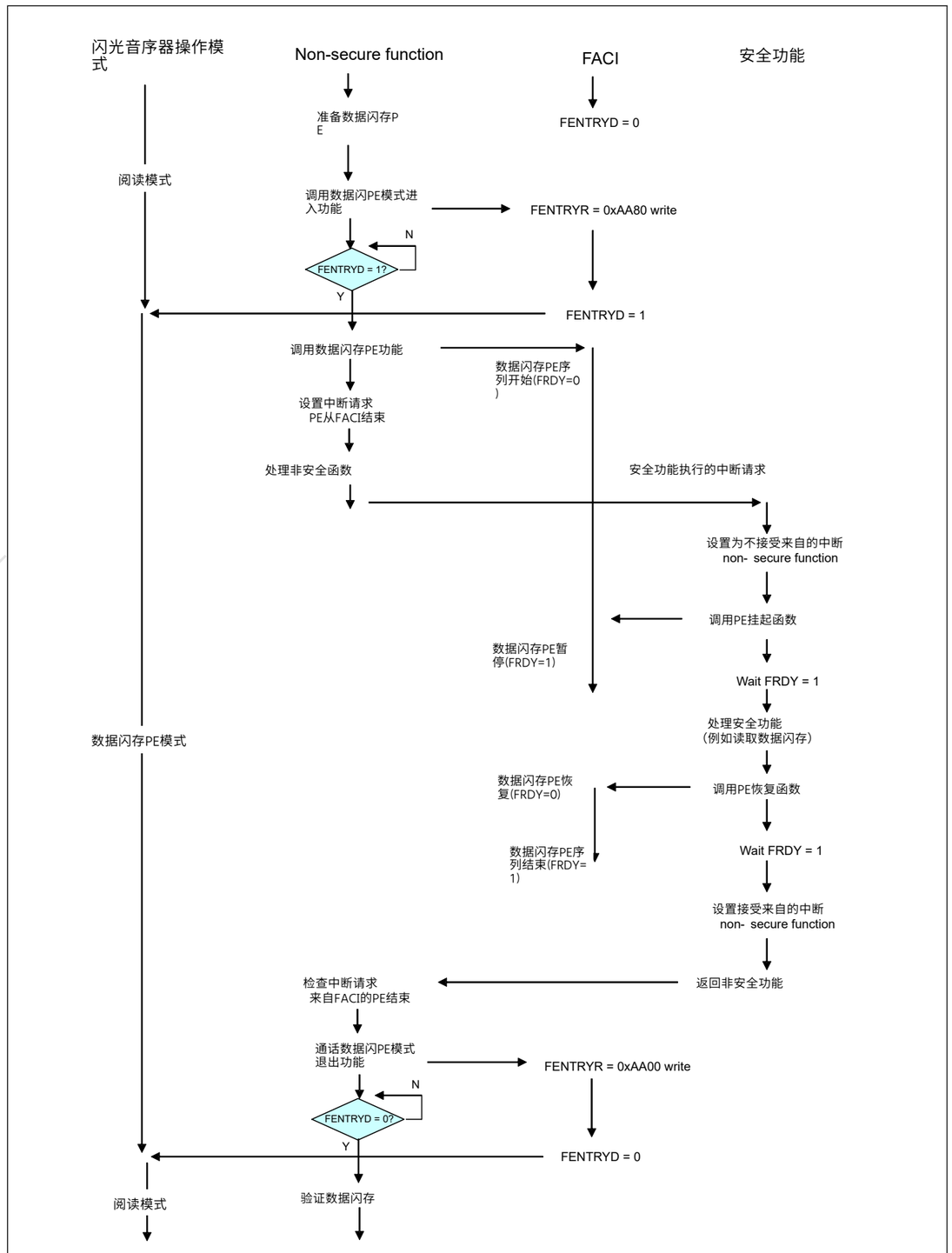


Figure 43.36 数据闪存PE安全功能暂停示例（检查中断请求以检测PE结束）

43.12.3.5 Code Flash P/E Mode Entry Protection

The flash sequencer has protection function of code flash P/E by the FMEPROT register for the secure developer. Secure function can prevent disturbance of reading code flash memory by this protection function. See section 43.4.14. FMEPROT : Flash P/E Mode Entry Protection Register.

For applications that do not require non-secure region programming/erasure other than from secure function, it is recommended to always disable non-secure function of code flash programming/erasure by enabling the protection function of FMEPROT register.

See Figure 43.37 in details of the code flash P/E sequence example by non-secure function.

43.12.3.5 CodeFlashPE模式进入保护

闪存定序器通过FMEPROT寄存器为安全开发人员提供代码闪存PE的保护功能。安全功能可以通过此保护功能防止读取代码闪存的干扰。请参阅第43.4.14节。FMEPROT：FlashPE模式进入保护寄存器。

对于除安全功能外不需要非安全区域编程擦除的应用，建议始终通过启用FMEPROT寄存器的保护功能来禁用代码闪存编程擦除的非安全功能。

有关非安全功能的代码闪存PE序列示例的详细信息，请参见图43.37。

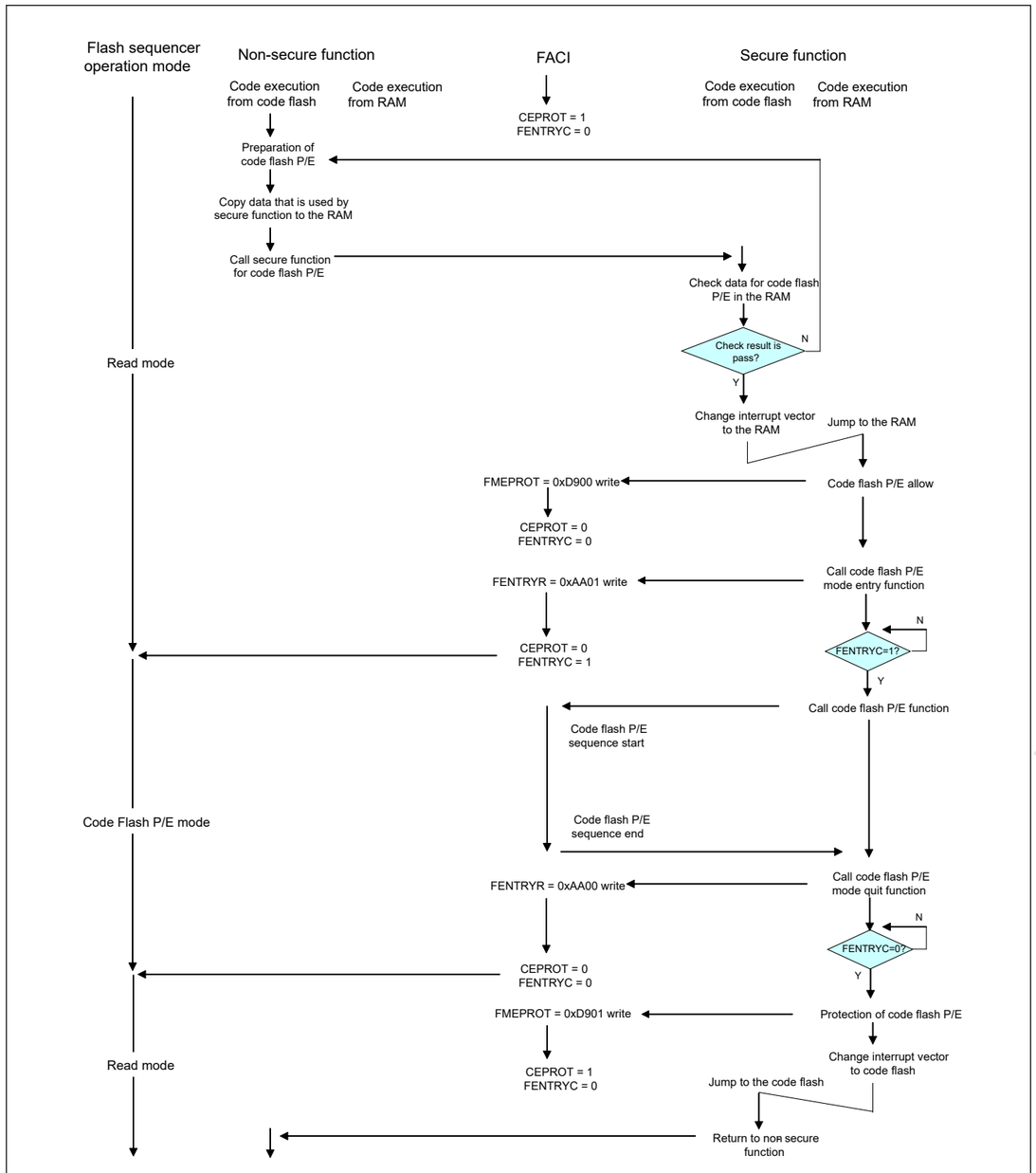


Figure 43.37 Code Flash P/E Sequence Example by non-secure function (Using secure function for code flash P/E)

43.13 Boot Mode

There are two serial programming modes; the boot mode (for the SCI interface) with SCI9. Table 43.27 lists the I/O pins used in boot mode. Table 43.28 lists the available communication interface used in the boot mode.

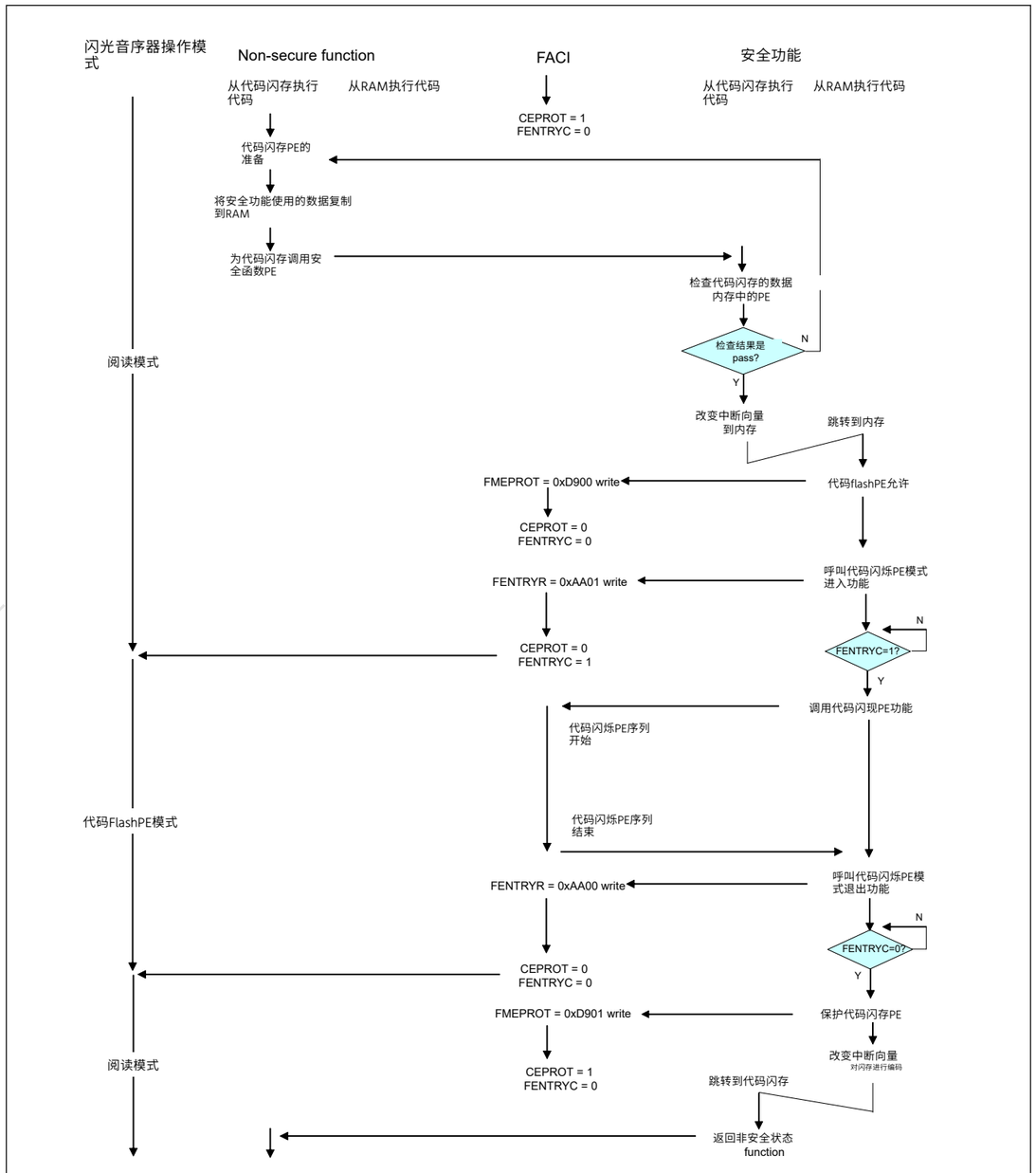


Figure 43.37 CodeFlashPESequenceExamplebynon−securefunction(Usingsecurefunctionforcodeflash PE)

43.13 引导模式

有两种串行编程模式；启动模式（用于SCI接口）与SCI9。表43.27列出了引导模式中使用的IO引脚。表43.28列出了启动模式中使用的可用通信接口。

Table 43.27 I/O Pins Used in Boot Mode

Pin Name	I/O	Mode to be Used	Use
MD	Input	Boot mode (for the SCI interface)	Selection of operating mode
PA15/RXD9	Input	Boot mode (for the SCI interface)	For host communication (to receive data through SCI)
PB03/TXD9	Output		For host communication (to transmit data through SCI)

Table 43.28 Available Communication Interface Used in Boot Mode

Main clock oscillator or external clock is connected	Yes	No	No
Tool connection time*1	Up to 1 second	Up to 2 seconds	Up to 3 seconds

Note 1. See the boot firmware manual for the detail connection time.

43.13.1 Boot Mode (for the SCI Interface)

In boot mode (for the SCI interface), the host sends control commands and data for programming, and the flash memory is programmed or erased accordingly. An on-chip SCI handles transfer between the host and this MCU in asynchronous mode. Tools for transmission of control commands and the data for programming must be prepared in the host.

When this MCU is activated in boot mode (for the SCI interface), the program on the dedicated area the MCU is executed. The boot program automatically adjusts the bit rate of the SCI and controls programming/erasure by receiving control commands from the host.

Figure 43.38 shows the system configuration for operations in boot mode (for the SCI interface).

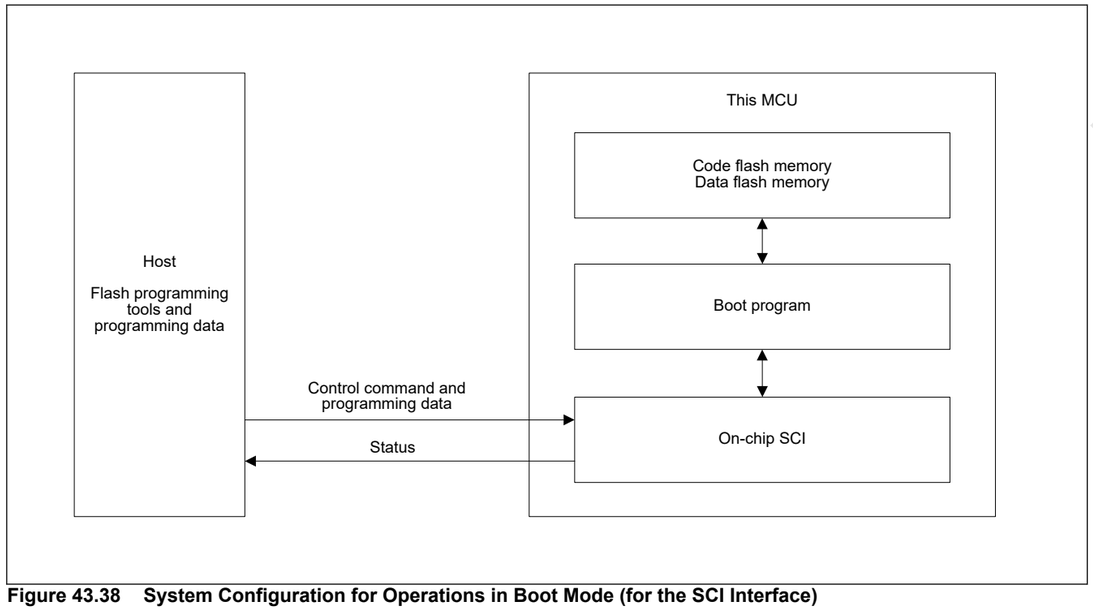


Figure 43.38 System Configuration for Operations in Boot Mode (for the SCI Interface)

43.14 Using the Serial Programmer for Rewriting

A serial programmer can be used to rewrite flash memory in boot mode.

(1) Serial Programming

This MCU is mounted on the system board at the time of serial programming. Providing a connector to the board enables rewriting of this MCU by the serial programmer to proceed.

Table 43.27 引导模式下使用的IO引脚

引脚名称	I/O	使用模式	Use
MD	Input	引导模式（用于SCI接口）	操作模式的选择
PA15/RXD9	Input	引导模式（用于SCI接口）	用于主机通信（通过SCI接收数据）
PB03/TXD9	Output		用于主机通信（通过SCI传输数据）

Table 43.28 引导模式中使用的可用通信接口

连接主时钟振荡器或外部时钟	Yes	No	No
工具连接时间*1	最多1秒	最多2秒	最多3秒

注1.详细连接时间请参见启动固件手册。

43.13.1 引导模式（用于SCI接口）

在引导模式下（针对SCI接口），主机发送控制命令和数据进行编程，相应地对闪存进行编程或擦除。片上SCI以异步模式处理主机和该MCU之间的传输。主机中必须准备好用于传输控制命令和编程数据的工具。

当这个MCU在启动模式下被激活时（对于SCI接口），在MCU的专用区域上的程序被执行。
引导程序通过接收来自主机的控制命令自动调整SCI的比特率并控制编程擦除。

图43.38显示了引导模式下操作的系统配置（对于SCI接口）。

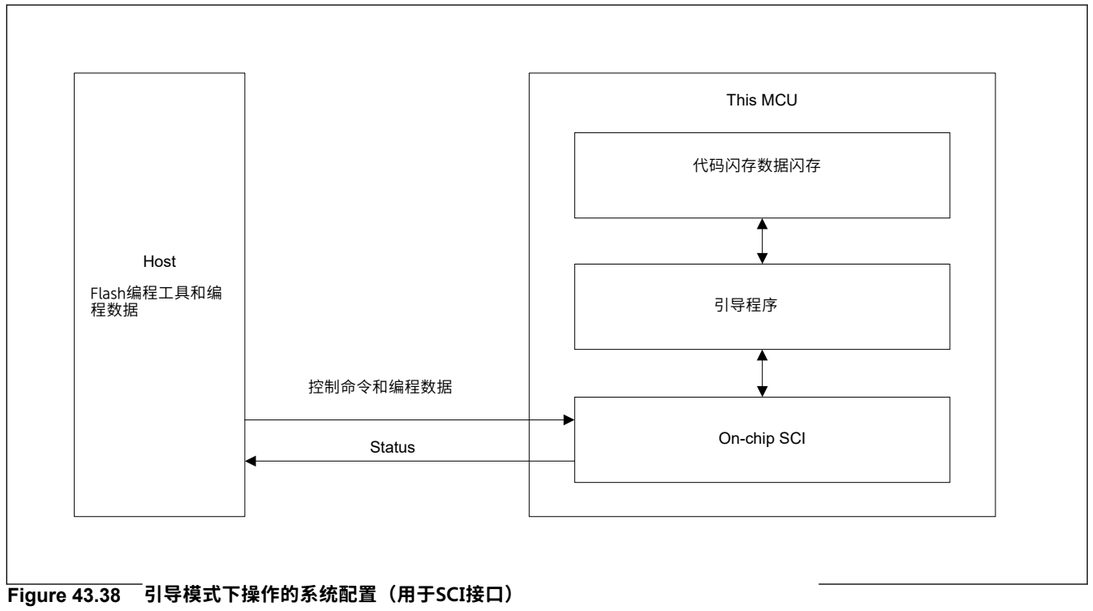


Figure 43.38 引导模式下操作的系统配置（用于SCI接口）

43.14 使用串行编程器进行重写

串行编程器可用于在引导模式下重写闪存。

(1) 串行编程

该MCU在串行编程时安装在系统板上。为电路板提供连接器可以让串行编程器重写该MCU以继续进行。

43.14.1 Environments for Serial Programming

The recommended environments for rewriting the flash memory of the MCU with data are described below.

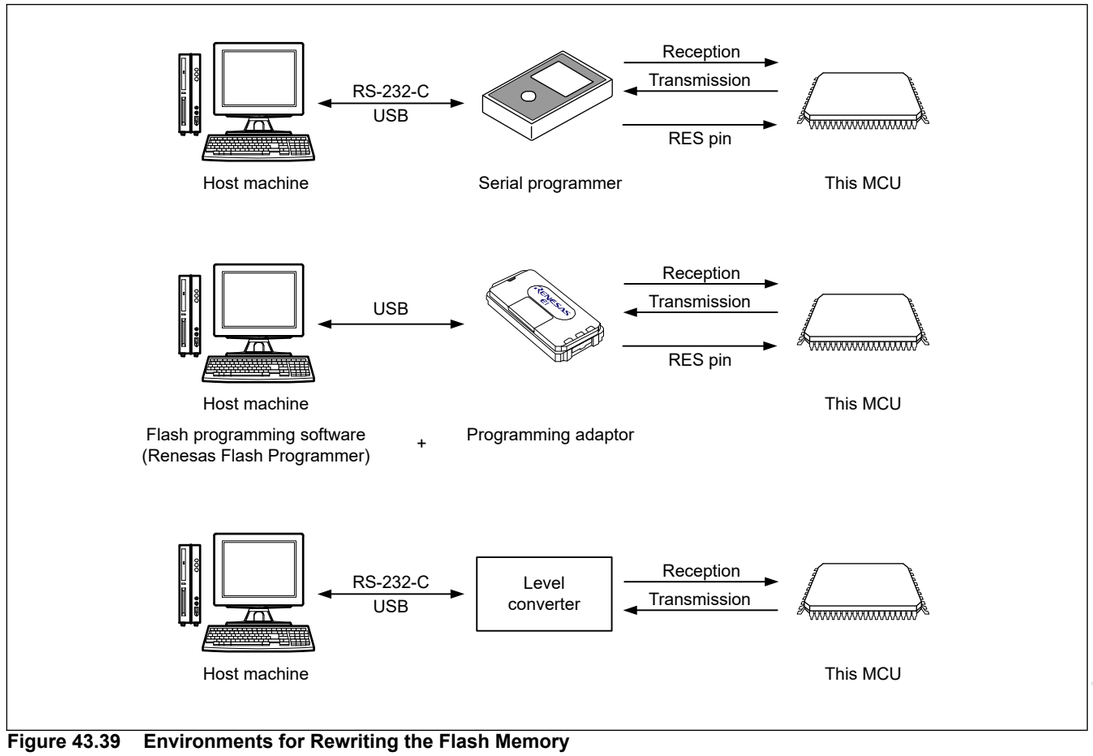


Figure 43.39 Environments for Rewriting the Flash Memory

43.15 Programming through Self-Programming

43.15.1 Overview

This MCU supports programming of the flash memory by the user program itself. The FACI commands can be used with user programs for writing to the flash memory. This allows upgrading of user programs and rewriting of constant data fields.

The program for rewriting must be transferred to the internal RAM in advance when the BGO is not available or when rewriting the option-setting memory.

43.14.1 串行编程环境

使用数据重写MCU的闪存的推荐环境如下所述。

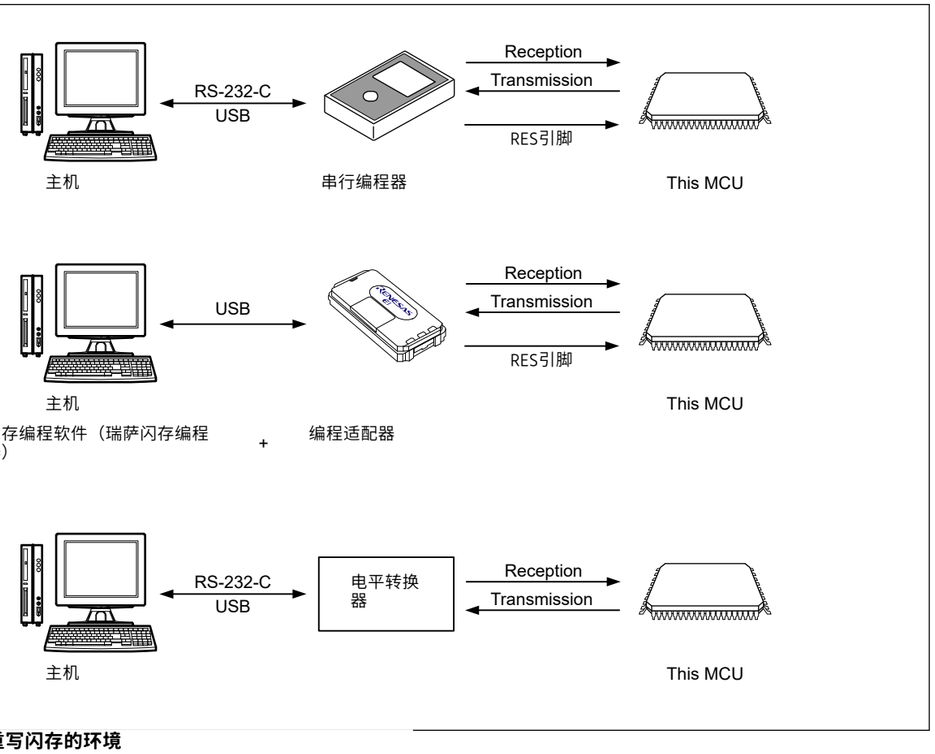


Figure 43.39 重写闪存的环境

43.15 通过自编程进行编程

43.15.1 Overview

该MCU支持用户程序本身对闪存进行编程。FACI命令可与用户程序一起用于写入闪存。这允许升级用户程序和重写常量数据字段。

当BGO不可用或重写选项设置存储器时，必须提前将重写程序传送到内部RAM。

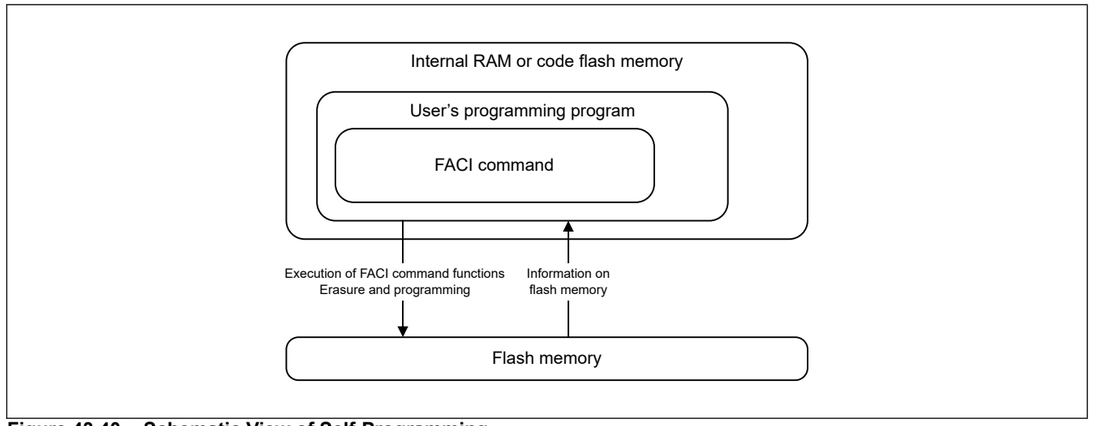


Figure 43.40 Schematic View of Self-Programming

For comprehensive information on the self-programming, refer to section 43.9. FACI Commands

43.15.2 Background Operation

The background operation (BGO) can be used to execute the flash rewrite routine on the code flash memory when the data flash memory is rewritten.

Background operations can be used when the combination of the flash memory for rewriting and the flash memory for reading is any of those listed below.

Table 43.29 Conditions under which Background Operation is Usable

	Range for rewriting	Range for reading
Common	Code flash memory	Data flash memory
	Data flash memory	Code flash memory

43.16 Reading Flash Memory

43.16.1 Reading Code Flash Memory

Special settings are not required to read code flash memory after release from the reset state. Data can simply be read out through access to addresses in the code flash memory.

When reading code flash memory that has been erased but not yet been programming again (i.e. that is in the non-programmed state), all bits are read as 1.

43.16.2 Reading Data Flash Memory

Special settings are not required to read data flash memory after release from the reset state. Data can simply be read out through access to addresses in the data flash memory.

Values read from data flash memory that has been erased but not yet been programming again (i.e. that is in the non-programmed state) are undefined. Use blank checking when you need to confirm that an area is in the non-programmed state.

43.16.3 Access Cycle

When the CPU cache is hit, access is one cycle.

For the CPU cache is missed while CPU cache operation is enabled, or CPU cache is disabled. (This operation only guarantees the first read access of a wrapping burst in AHB protocol. Otherwise, access wait occurs until the CPU cache is filled.)

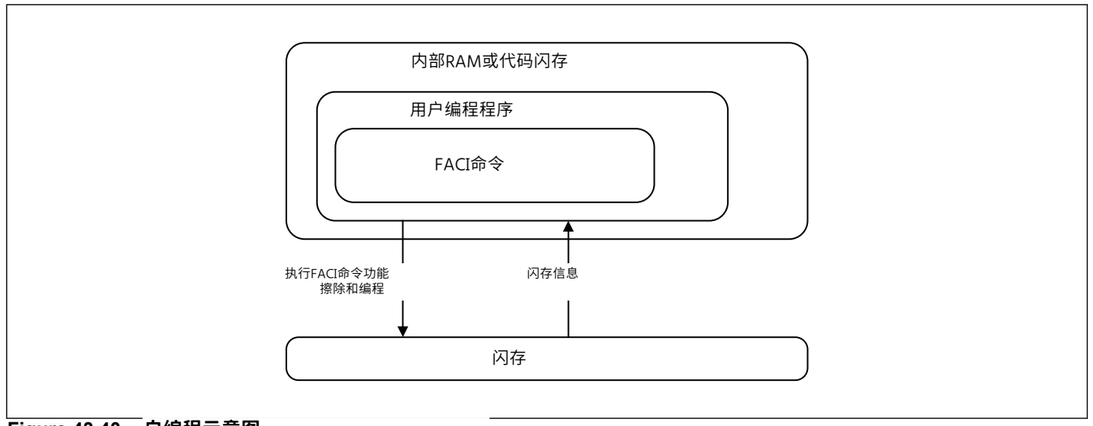


Figure 43.40 自编程示意图

有关自编程的全面信息，请参阅第43.9节。FACI命令

43.15.2 后台操作

当数据闪存被重写时，后台操作（BGO）可用于在代码闪存上执行闪存重写例程。

当用于重写的闪存和用于读取的闪存的组合为下列任何一种时，可以使用后台操作。

Table 43.29 后台操作可用的条件

	重写范围	读取范围
Common	代码闪存	数据闪存
	数据闪存	代码闪存

43.16 读取闪存

43.16.1 读码闪存

从复位状态释放后，读取代码闪存不需要特殊设置。可以通过访问代码闪存中的地址来简单地读取数据。

当读取已擦除但尚未再次编程的代码闪存时（即处于未编程状态），所有位都被读取为1。

43.16.2 读取数据闪存

从复位状态释放后读取数据闪存不需要特殊设置。通过访问数据闪存中的地址可以简单地读取数据。

从已擦除但尚未再次编程（即处于未编程状态）的数据闪存中读取的值未定义。当您需要确认某个区域处于非编程状态时，请使用空白检查。

43.16.3 访问周期

当CPU缓存被命中时，访问为一个周期。

启用CPU缓存操作或禁用CPU缓存时CPU缓存丢失。（此操作仅保证AHB协议中包装突发的第一次读取访问。否则，将等待访问，直到CPU缓存被填满。）

Table 43.30 Code Flash Memory

Flash Cache Operation	FLWT Register Setting	Read cycle (ICLK)
enable and hit	—	3
disable or miss	0x00	3
	0x01	4

Table 43.31 Data Flash Memory

FCKMHZ Register Setting	Read (cycle)
0x00 to 0x09	Min: 2 ICLK + 3 FCLK Max: (n + 1) ICLK + 3 FCLK
0x0A to 0x13	Min: 2 ICLK + 4 FCLK Max: (n + 1) ICLK + 4 FCLK
0x14 to 0x1D	Min: 2 ICLK + 5 FCLK Max: (n + 1) ICLK + 5 FCLK
0x1E to 0x27	Min: 2 ICLK + 6 FCLK Max: (n + 1) ICLK + 6 FCLK
0x28 to 0x31	Min: 2 ICLK + 7 FCLK Max: (n + 1) ICLK + 7 FCLK
0x32 to 0x3B	Min: 2 ICLK + 8 FCLK Max: (n + 1) ICLK + 8 FCLK
0x3C	Min: 2 ICLK + 9 FCLK Max: (n + 1) ICLK + 9 FCLK

Note: When the frequency ratio of ICLK : FCLK is n : 1

43.17 Usage Notes

(1) Reading Area Where Programming/Erasure was Interrupted and Area Targeted for Suspension

The data stored in the area where programming or erasure has been suspended or the area where programming or erasure has been suspended by using the suspend command are undefined. To avoid faulty operation caused by reading undefined data, take care not to fetch instructions or read data from areas where programming or erasure was suspended and where programming or erasure was suspended by using the suspend command.

(2) Suspension During Programming/Erasure

When processing of programming/erasure is stopped by issuing the P/E suspend command, the programming/erasure processing can be resumed by issuing the P/E resume command. If the flash sequencer enters the command-locked state for any reason and issues the forced stop command after the suspended processing is normally completed and the ERSSPD flag or PRGSPD flag is set to 1, the suspended processing cannot be resumed. In addition, the values in the area where the processing was suspended are not guaranteed. Erase that area

(3) Prohibition of Additional Programming

Programming a given area of the code flash memory or data flash memory twice is not possible. To program the code flash memory or data flash memory where has been programed, erase the target area. Programming can be added to the option-setting memory.

(4) Resets During Programming/Erasure, or Blank Checking

In the case of a reset due to the signal on the RES pin during programming/erasure, or blank checking of the flash memory, wait for at least t_{RESW} (see section 46, Electrical Characteristics) of the reset input period once the operating voltage is within the range stipulated in the electrical characteristics, then release the device from the reset state.

(5) Allocation of Vectors for Interrupts and Other Exceptions During Programming/Erasure

Generation of an interrupt or other exception during programming/erasure may lead to fetching of the vector from the code flash memory. Under conditions where BGO cannot be used, set the address of the vector to an address that is not in the

Table 43.30 代码闪存

闪存缓存操作	FLWT寄存器设置	读周期(ICLK)
启用并点击	—	3
禁用或错过	0x00	3
	0x01	4

Table 43.31 数据闪存

FCKMHZ寄存器设置	Read (cycle)
0x00 to 0x09	Min: 2 ICLK + 3 FCLK Max: (n + 1) ICLK + 3 FCLK
0x0A to 0x13	Min: 2 ICLK + 4 FCLK Max: (n + 1) ICLK + 4 FCLK
0x14 to 0x1D	Min: 2 ICLK + 5 FCLK Max: (n + 1) ICLK + 5 FCLK
0x1E to 0x27	Min: 2 ICLK + 6 FCLK Max: (n + 1) ICLK + 6 FCLK
0x28 to 0x31	Min: 2 ICLK + 7 FCLK Max: (n + 1) ICLK + 7 FCLK
0x32 to 0x3B	Min: 2 ICLK + 8 FCLK Max: (n + 1) ICLK + 8 FCLK
0x3C	Min: 2 ICLK + 9 FCLK Max: (n + 1) ICLK + 9 FCLK

Note: 当ICLK:FCLK的频率比为n:1时

43.17 使用说明

(1) 编程擦除被中断的阅读区域和暂停的目标区域

存储在已暂停编程或擦除的区域或已使用suspend命令暂停编程或擦除的区域中的数据是未定义的。为避免因读取未定义数据而导致错误操作，请注意不要从暂停编程或擦除的区域以及使用暂停命令暂停编程或擦除的区域获取指令或读取数据。

(2) 编程擦除期间的暂停

当通过发出PE暂停命令停止编程擦除处理时，可以通过发出PE恢复命令来恢复编程擦除处理。如果闪存定序器由于任何原因进入命令锁定状态并在挂起处理正常完成并且ERSSPD标志或PRGSPD标志设置为1后发出强制停止命令，则无法恢复挂起的处理。此外，不能保证处理暂停的区域中的值。擦除该区域

(3) 禁止额外编程

不能对代码闪存或数据闪存的给定区域进行两次编程。要对已编程的代码闪存或数据闪存进行编程，请擦除目标区域。可以将编程添加到选项设置存储器中。

(4) 在编程擦除或空白检查期间复位

如果在编程擦除期间由于RES引脚上的信号而导致复位，或者闪存的空白检查，一旦工作电压为在电气特性规定的范围内，然后将设备从复位状态释放。

(5) 在编程擦除期间为中断和其他异常分配向量

在编程擦除期间产生中断或其他异常可能会导致从代码闪存中获取向量。在无法使用BGO的情况下，将向量的地址设置为不在

code flash memory. Alternatively, make sure that no handling of interrupts or exceptions proceeds during programming/erasure.

(6) Items Prohibited During Programming/Erasure, or Blank Checking

High voltage is applied to the flash memory during programming/erasure, or blank checking. To prevent damage to the flash memory, do not perform the following operations.

- Have the operating voltage from the power supply go beyond the permitted range.
- Change the FWEPROR.FLWE[1:0]bits.
- Change the OPCCR.OPCM[2:0] bits.
- Change the SCKDIVCR.FCK[2:0]bits.
- Change the SCKSCR.CKSEL[2:0]bits.
- Transition to the software standby mode, or deep software standby mode.

(7) Programming/Erasure in Low-Speed Modes

Do not programming/erasure the flash memory when low-speed mode is selected with the operating power control register (OPCCR).

(8) Emulator Connection

Renesas provides the emulator which supports both debugging using SWD or JTAG communication and serial programming using SCI communication. This emulator makes it easy to switch between debugging and serial programming.

Table 43.32 shows the pinout of 10 pin or 20 pin socket pinouts when using this emulator. The pinout of SWD and JTAG is ARM standard, and MD, TXD, RXD pins are added for the serial programming using SCI communication.

The serial programming interface must be used to program the TrustZone IDAU boundary register settings.

It is recommended to connect PA14/SWCLK/TCK and P201/MD pins using wired OR circuit on the board to use both debugging and serial programming

Table 43.32 Pin assign for emulator

Pin No.	SWD	JTAG	Serial Programming using SCI
1	VCC	VCC	VCC
2	PA13/SWDIO	PA13/TMS	NC
4	PA14/SWCLK	PA14/TCK	P201/MD
	Wired OR with P201/MD	Wired OR with P201/MD	
6	PB03/SWO/TXD9	PB03/TDO/TXD9	PB03/TXD9
8	PA15/RXD9	PA15/TDI/RXD9	PA15/RXD9
9	GNDdetect	GNDdetect	GNDdetect
10	nRESET	nRESET	nRESET
12	PE02/TCLK	PE02/TCLK	NC
14	PE03/TDATA[0]	PE03/TDATA[0]	NC
16	PE04/TDATA[1]	PE04/TDATA[1]	NC
18	PE05/TDATA[2]	PE05/TDATA[2]	NC
20	PE06/TDATA[3]	PE06/TDATA[3]	NC
3, 5, 15, 17, 19	GND	GND	GND
7	NC	NC	NC
11, 13	NC	NC	NC

代码闪存。或者，确保在编程擦除期间不处理中断或异常。

(6) 编程擦除或空白检查期间禁止的项目

在编程擦除或空白检查期间向闪存施加高电压。为防止损坏闪存，请勿执行以下操作。

- 电源的工作电压是否超出允许范围。
- 改变FWEPROR.FLWE[1:0]位。
- 更改OPCCR.OPCM[2:0]位。
- 更改SCKDIVCR.FCK[2:0]位。
- 更改SCKSCR.CKSEL[2:0]位。
- 转换到软件待机模式或深度软件待机模式。

(7) 低速模式下的编程擦除

当使用操作电源控制寄存器(OPCCR)选择低速模式时，不要对闪存进行编程擦除。

(8) 仿真器连接

瑞萨电子提供的仿真器支持使用SWD或JTAG通信进行调试和使用SCI通信进行串行编程。该仿真器可以轻松地在调试和串行编程之间切换。

表43.32显示了使用该仿真器时10针或20针插座的引脚排列。SWD和JTAG的管脚是ARM标准，并增加了MD、TXD、RXD引脚用于使用SCI通信的串行编程。

必须使用串行编程接口对TrustZoneIDAU边界寄存器设置进行编程。

建议使用板上的有线或电路连接PA14SWCLKTCK和P201MD引脚，以同时使用调试和串行编程

Table 43.32 为模拟器分配引脚

针号	SWD	JTAG	使用SCI进行串行编程
1	VCC	VCC	VCC
2	PA13/SWDIO	PA13/TMS	NC
4	PA14/SWCLK	PA14/TCK	P201/MD
	有线或带P201MD	有线或带P201MD	
6	PB03/SWO/TXD9	PB03/TDO/TXD9	PB03/TXD9
8	PA15/RXD9	PA15/TDI/RXD9	PA15/RXD9
9	GNDdetect	GNDdetect	GNDdetect
10	nRESET	nRESET	nRESET
12	PE02/TCLK	PE02/TCLK	NC
14	PE03/TDATA[0]	PE03/TDATA[0]	NC
16	PE04/TDATA[1]	PE04/TDATA[1]	NC
18	PE05/TDATA[2]	PE05/TDATA[2]	NC
20	PE06/TDATA[3]	PE06/TDATA[3]	NC
3, 5, 15, 17, 19	GND	GND	GND
7	NC	NC	NC
11, 13	NC	NC	NC

44. Internal Voltage Regulator

44.1 Overview

The MCU includes one internal voltage regulator:

- Linear regulator (LDO)

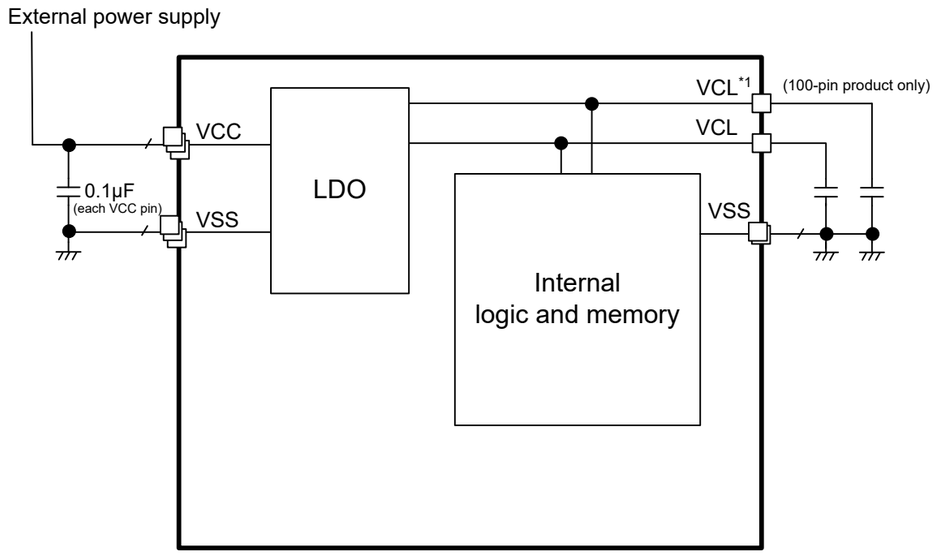
This regulator supplies voltage to all internal circuits and memory except for I/O and analog power domains.

44.2 Operation

Table 44.1 lists the LDO mode pin settings, and Figure 44.1 shows the LDO mode settings. In LDO mode, the internal voltage is generated from VCC.

Table 44.1 LDO mode pin

Pins	Setting descriptions
All VCC	• Connect each pin to the system power supply. • Connect each pin to VSS through a 0.1-μF multilayer ceramic capacitor. Place the capacitor close to the pin.
All VCL (100-pin product)	Connect the each pin to VSS through a 0.1-μF multilayer ceramic capacitor. Place the capacitor close to the pin.
VCL (64, 48-pin products)	Connect the each pin to VSS through a 0.22-μF multilayer ceramic capacitor. Place the capacitor close to the pin.



Note 1. Only 100-pin product has two VCL pins.

Figure 44.1 LDO mode settings

44. 内部稳压器

44.1 Overview

MCU包含一个内部稳压器：

●线性稳压器（LDO）

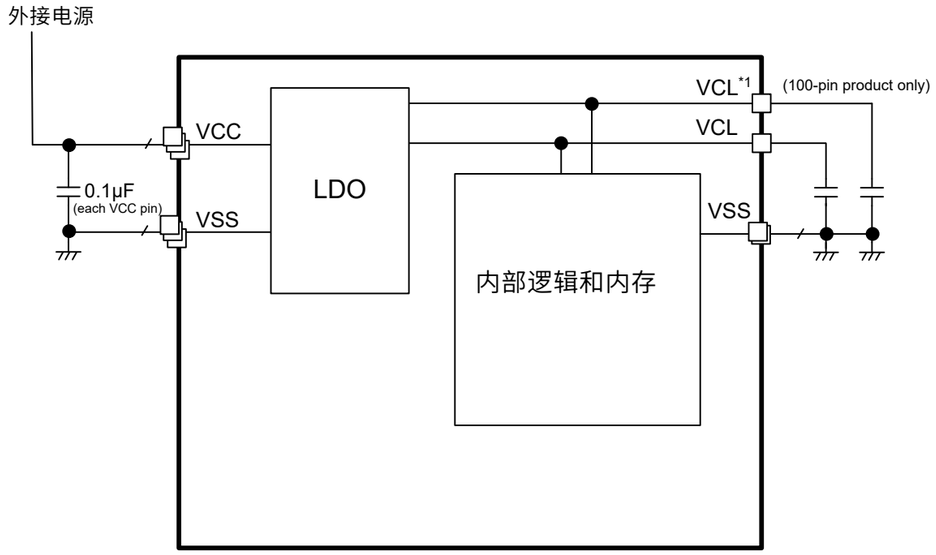
该稳压器为除IO和模拟电源域之外的所有内部电路和存储器提供电压。

44.2 Operation

表44.1列出了LDO模式引脚设置，图44.1显示了LDO模式设置。在LDO模式下，内部电压由VCC产生。

Table 44.1 LDO模式引脚

Pins	设置说明
All VCC	• 将每个引脚连接到系统电源。 • 通过一个0.1μF多层陶瓷电容器将每个引脚连接到VSS。将电容器靠近引脚放置。
All VCL (100-pin product)	通过一个0.1μF多层陶瓷电容器将每个引脚连接到VSS。将电容器靠近引脚放置。
VCL (64, 48-pin products)	通过一个0.22μF多层陶瓷电容器将每个引脚连接到VSS。将电容器靠近引脚放置。



注1.只有100-pin产品有两个VCL引脚。

Figure 44.1 LDO模式设置

45. Security Features

45.1 Features

- ARMv8-M TrustZone security
  - Eight regions IDAU for memory space
    - Up to three regions for the code flash
    - Up to two regions for the data flash
    - Up to three regions for the SRAM
    - IDAU setting is common for the CPU, DMAC, and DTC
  - SAU is not implemented
  - Secure or Non-secure region for the Standby SRAM
  - Individual Secure or Non-secure security attribution for each peripheral
  - Some peripherals support both Secure and Non-secure security attributions
- Device lifecycle management
- Three debug access levels
  - DBG2: The debugger connection is allowed, and no restriction to access memories and peripherals
  - DBG1: The debugger connection is allowed, and restricted to access only non-secure memory regions and peripherals
  - DBG0: The debugger connection is not allowed
- Key injection
- Cryptographic accelerator
  - See section 35, Secure Cryptographic Engine (SCE5)

45.2 Arm TrustZone Security

45.2.1 Arm TrustZone Technology

Arm TrustZone technology divides the system and the application into Secure and Non-secure domains. Secure application can access both Secure and Non-secure memory and resources. Non-secure application can only access Non-secure memory and resources.

The system starts up in Secure state by default. The security state of CPU can be either Secure or Non-secure.

45.2.2 Memory Security Attribution

The code flash, the data flash, and the SRAM are divided into Secure (S), Non-secure (NS) and Non-secure callable (NSC) regions. These memory security attributions are set into the nonvolatile memory by the serial programming command when the device lifecycle is SSD state. These memory security attributions are loaded into the IDAU and the memory controller before application execution. These memory security attributions cannot be updated by application but can be through the dedicated registers.

The code flash can be divided in up to three regions. The data flash can be divided in up to two regions. The SRAM can be divided in up to three regions. Figure 45.1 shows the memory mapping. Table 45.1 shows the size of memory region.

45. 安全功能

45.1 Features

- ARMv8-M TrustZone security

  八个区域IDAU用于存储空间
  - 代码闪存最多三个区域
  - 最多两个区域用于数据闪存
  - SRAM最多三个区域
  - IDAU设置对于CPU、DMAC和DTC是通用的

  SAU未实施

  备用SRAM的安全或非安全区域

  每个外围设备的单独安全或非安全安全属性

  一些外围设备同时支持安全和非安全安全属性

●设备生命周期管理

●三个调试访问级别

DBG2：允许调试器连接，并且对访问内存和外设没有限制

DBG1：允许调试器连接，但仅限于访问非安全内存区域和外围设备

DBG0：不允许调试器连接

●密钥注入

●密码加速器

参见第35节，安全加密引擎(SCE5)

45.2 ArmTrustZone安全

45.2.1 ArmTrustZone技术

ArmTrustZone技术将系统和应用程序划分为安全和非安全域。安全应用程序可以访问安全和非安全内存和资源。非安全应用程序只能访问非安全内存和资源。

系统默认以安全状态启动。CPU的安全状态可以是Secure或Non-secure。

45.2.2 内存安全归属

代码闪存、数据闪存和SRAM分为安全(S)、非安全(NS)和非安全可调用(NSC)区域。当设备生命周期为SSD状态时，这些内存安全属性由串行编程命令设置到非易失性内存中。这些内存安全属性在应用程序执行之前被加载到IDAU和内存控制器中。这些内存安全属性不能由应用程序更新，但可以通过专用寄存器来更新。

代码闪存最多可分为三个区域。数据闪存最多可分为两个区域。SRAM最多可分为三个区域。图45.1显示了内存映射。表45.1显示了内存区域的大小。

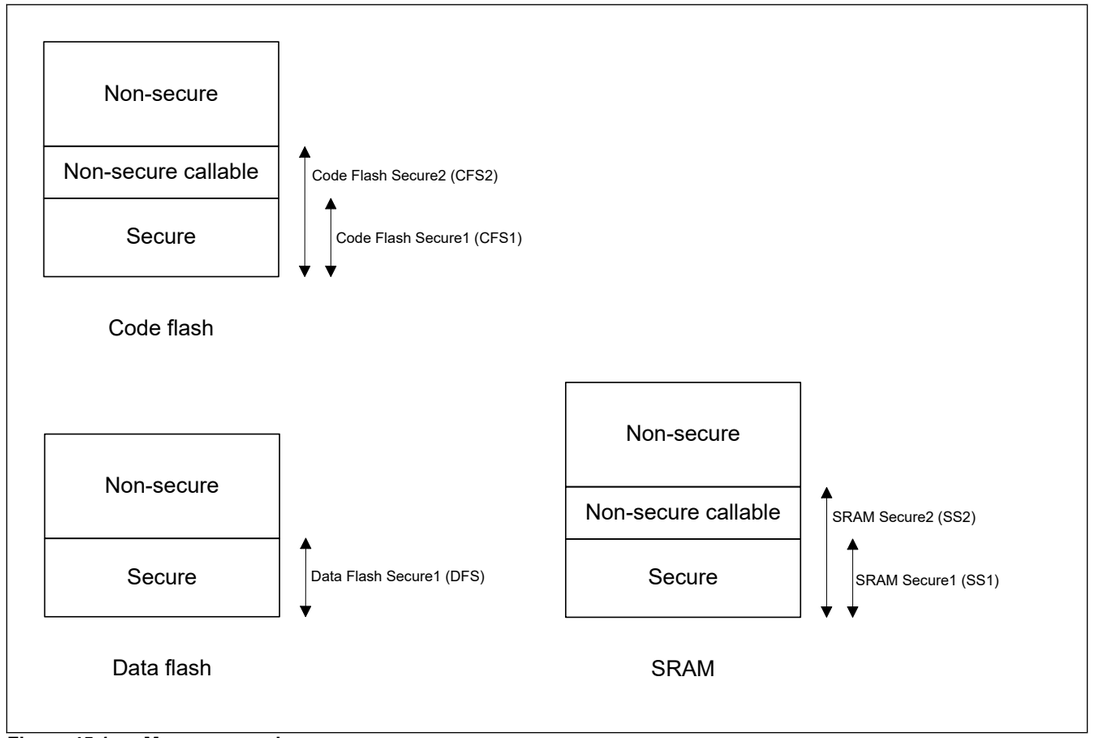


Figure 45.1 Memory mapping

Table 45.1 Memory Region Size

Memory Region	Start Address	Size
Code flash secure	0x0000_0000	CFS1 × 1 KB
Code flash non-secure callable	CFS1 × 1 KB	CFS2 × 32 KB - CFS1 × 1 KB
Code flash non-secure	CFS2 × 32 KB	Code flash size - CFS2 × 32 KB
Data flash secure	0x0800_0000	DFS × 1 KB
Data flash non-secure	0x0800_0000 + DFS × 1 KB	Data flash size - DFS × 1 KB
SRAM secure	0x2000_0000	SS1 × 1 KB
SRAM non-secure callable	0x2000_0000 + SS1 × 1 KB	SS2 × 8 KB - SS1 × 1 KB
SRAM non-secure	0x2000_0000 + SS2 × 8 KB	SRAM size - SS2 × 8 KB

The Standby SRAM is divided 8 regions. Security attribution can be set for each region, but both secure region and non-secure region must be contiguous. In other words, the Standby SRAM can have one contiguous secure region and one contiguous non-secure region. The Standby SRAM security attribution is set to the dedicated register by the secure application. See section 42, Standby SRAM for the details.

Table 45.2 shows the access permission of the memory.

Table 45.2 Access Permission of Memory (1 of 2)

Memory	Secure access	Non-secure access
Code flash, Data flash, SRAM configured as Secure or Non-secure callable	allowed	Write ignored / Read ignored TrustZone Access error is generated
Code flash, Data flash, SRAM configured as non-secure	allowed	allowed

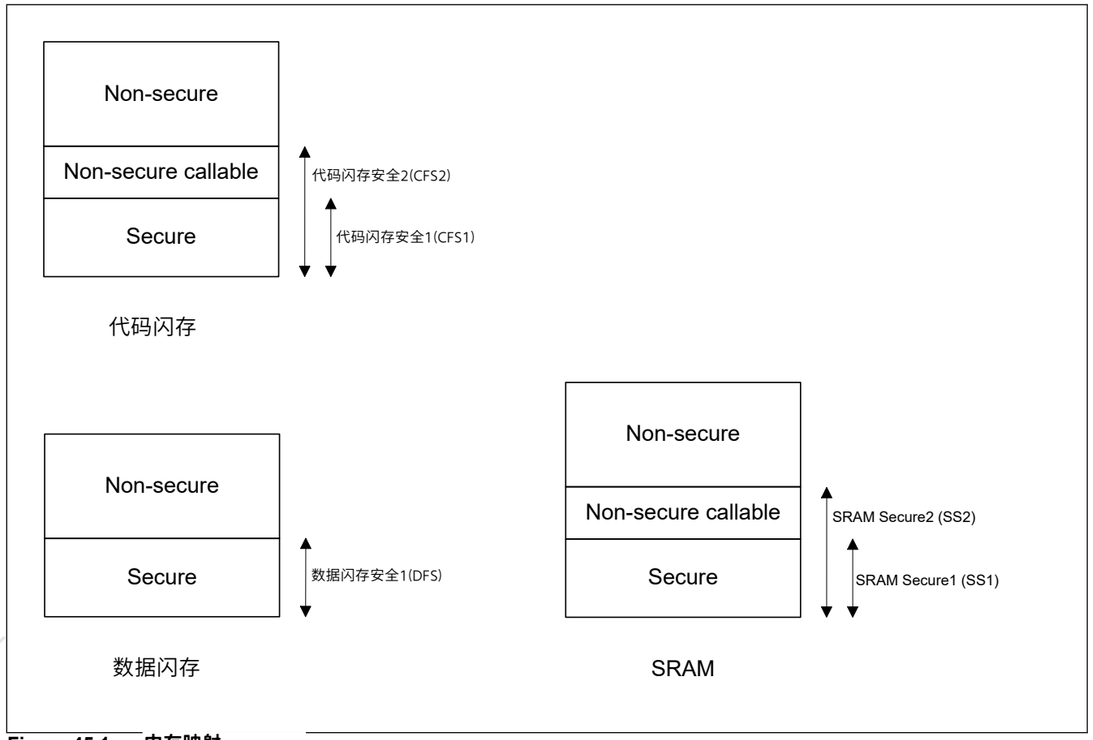


Figure 45.1 内存映射

Table 45.1 内存区域大小

记忆区	起始地址	Size
代码闪存安全	0x0000_0000	CFS1 × 1 KB
代码闪存非安全可调用	CFS1 × 1 KB	CFS2 × 32 KB - CFS1 × 1 KB
代码闪存不安全	CFS2 × 32 KB	代码闪存大小CFS2×32KB
数据闪存安全	0x0800_0000	DFS × 1 KB
数据闪存不安全	0x0800_0000 + DFS × 1 KB	数据闪存大小DFS×1KB
SRAM secure	0x2000_0000	SS1 × 1 KB
SRAM non-secure callable	0x2000_0000 + SS1 × 1 KB	SS2 × 8 KB - SS1 × 1 KB
SRAM non-secure	0x2000_0000 + SS2 × 8 KB	SRAM size - SS2 × 8 KB

备用SRAM分为8个区域。可以为每个区域设置安全属性，但安全区域和非安全区域必须是连续的。换言之，StandbySRAM可以有一个连续的安全区域和一个连续的非安全区域。备用SRAM安全属性由安全应用程序设置到专用寄存器。有关详细信息，请参见第42节，备用SRAM。

表45.2显示了内存的访问权限。

Table 45.2 内存访问权限(1of2)

Memory	安全访问	Non-secure access
代码闪存、数据闪存、SRAM配置为安全或非安全可调用	allowed	写被忽略读被忽略 生成TrustZone访问错误
代码闪存、数据闪存、配置为非安全的SRAM	allowed	allowed

Table 45.2 Access Permission of Memory (2 of 2)

Memory	Secure access	Non-secure access
Standby SRAM configured as Secure	allowed	Write ignored / Read 0x00 TrustZone Access error is not generated
Standby SRAM configured as Non-secure	allowed	allowed

45.2.3 Peripheral Security Attribution

Each peripheral can be configured to be Secure or Non-secure.

Peripherals are divided into two types.

Type-1 peripherals has the one security attribution. Access to all registers is controlled by one security attribution. Type-1 peripheral security attribution is set to the PSARx (x = B to E) register by the secure application.

Type-2 peripherals has the security attribution for each register or for each bit. Access to each register or bit field is controlled according to these security attributions. Type-2 peripheral security attribution is set to the Security Attribution register in each module by the secure application. For the Security Attribution register, see sections in the user manual for each peripheral.

Table 45.3 shows the classification of peripheral type.

Table 45.3 Peripheral Type Classification

Type	Peripheral
Type-1	SCI, SPI, CANFD, IIC, SCE5, DOC, CRC, CAC, TSN, ADC, DAC12, POEG, AGT, IWDT, WDT, IIRFA, TFU, ACMPHS, KINT
Type-2	System control (Resets, LVD, Clock Generation Circuit, Low Power Modes), FLASH CACHE, SRAM controller, CPU CACHE, DMAC, DTC, ICU, MPU, BUS, Security setting, ELC, I/O ports
Always Non-secure	GPT, PDG

Table 45.4 shows the access permission of type-1 peripherals. The access permission of type-2 peripherals is different by peripherals. See section Register Description of each peripherals.

Table 45.4 The access permission of type-1 peripherals

Permission	Secure access	Non-secure access
Peripheral configured as secure	allowed	Write ignored / Read ignored TrustZone Access error is generated
Peripheral configured as non-secure	allowed	allowed

45.2.4 Flash Sequencer Security Attribution

The flash sequencer is used to program or erase the flash.

The flash sequencer has the special security attribution. Table 45.5 shows the access permission of flash sequencer.

Table 45.5 Access Permissions of Flash Sequencer (1 of 2)

	Secure access	Non-secure access
FACI command issuing area	allowed	When the FACI command is issued to the secure region of code flash, data flash and option-setting memory ● Issued FACI command is invalid ● Flash sequencer error is generated When the FACI command is issued to the non-secure region of code flash, data flash and option-setting memory ● Issued FACI command is valid
FBPROT1, FSUACR, FMEPROT registers	allowed	Write ignored / Readable TrustZone Access error is not generated

Table 45.2 内存访问权限(2of2)

Memory	安全访问	Non-secure access
备用SRAM配置为安全	allowed	写入忽略读取0x00 未生成TrustZone访问错误
备用SRAM配置为非安全	allowed	allowed

45.2.3 外围安全属性

每个外围设备都可以配置为安全或非安全。

外设分为两种。

Type-1外围设备具有唯一的安全属性。对所有寄存器的访问由一个安全属性控制。类型1外设安全属性由安全应用程序设置到PSARx（x=B到E）寄存器。

Type-2外设对每个寄存器或每个位都有安全属性。根据这些安全属性控制对每个寄存器或位字段的访问。类型2外围安全属性由安全应用程序设置到每个模块中的安全属性寄存器。对于安全属性寄存器，请参阅每个外设的用户手册中的部分。

表45.3显示了外围类型的分类。

Table 45.3 外设类型分类

Type	Peripheral
Type-1	SCI、SPI、CANFD、IIC、SCE5、DOC、CRC、CAC、TSN、ADC、DAC12、POEG、AGT、IWDT、WDT、IIRFA、TFU、ACMPHS, KINT
Type-2	系统控制（复位、LVD、时钟生成电路、低功耗模式）、闪存缓存、SRAM控制器、CPUCACHE DMAC DTC ICU MPU BUS Securitysetting ELC IOports
Always Non-secure	GPT, PDG

表45.4显示了type-1外设的访问权限。type-2外设的访问权限因外设而异。请参阅每个外设的寄存器描述部分。

Table 45.4 type-1外设的访问权限

Permission	安全访问	Non-secure access
外设配置为安全	allowed	写被忽略读被忽略 生成TrustZone访问错误
外设配置为非安全	allowed	allowed

45.2.4 FlashSequencer安全属性

闪存定序器用于对闪存进行编程或擦除。

闪存定序器具有特殊的安全属性。表45.5显示了flashsequencer的访问权限。

Table 45.5 FlashSequencer的访问权限(1of2)

	安全访问	Non-secure access
FACI指令发布区	allowed	当FACI命令被发送到代码闪存、数据闪存和选项设置存储器的安全区域时● 发出的FACI命令无效 ● 产生闪存定序器错误 当FACI命令被发送到代码闪存、数据闪存和选项设置存储器的非安全区域时● 发出的FACI命令有效
FBPROT1, FSUACR, FMEPROT registers	allowed	写忽略可读 未生成TrustZone访问错误

Table 45.5 Access Permissions of Flash Sequencer (2 of 2)

	Secure access	Non-secure access
FCKMHZ register	allowed	Configured by Flash Security Attribution register When configured as Secure, ● Write ignored / Readable ● TrustZone Access error is not generated. When configured as Non-secure ● allowed
Other registers	allowed	During programming/erasure or during suspend programming/erasure by secure application ● Write ignored / Read 0x00 ● TrustZone Access error is not generated In other state ● allowed

45.2.5 Address Space Security Attribution

Table 45.6 shows the security attribution of the address space.

Table 45.6 Address Space Security Attribution

Region	Attribution
Code flash secure	Secure
Code flash non-secure callable	Non-secure callable
Code flash non-secure	Non-secure
Data flash secure	Secure
Data flash non-secure	Non-Secure
SRAM secure	Secure
SRAM non-secure callable	Non-secure callable
SRAM non-secure	Non-secure
Peripherals	Exempt
Other area	Exempt

Note: Exempt: No check will be done. All bus transactions are propagated.

45.2.6 TrustZone Access Error

Table 45.7 shows the behavior when TrustZone access error. The behavior varies depending on the master or slave area to be accessed.

Table 45.7 The Behavior When TrustZone Access Error

Area	CPU	DMAC/DTC
Code flash, Data flash, SRAM	Detect SecureFault exception*2	● Transfer does not start ● Occur NMI or reset*1 ● Occur interrupt (DMA_TRANSERR)
Other area	● Detect BusFault exception*2 *3 ● Occur NMI or reset*1*2 *3	● Stop transfer ● Occur NMI or reset *1 ● Occur interrupt (DMA_TRANSERR)

Note 1. NMI or reset is selected with TZFOAD.OAD bit.
Note 2. When TrustZone access error occurs by the debugger access, exception, NMI, or reset does not occurs.Only the error response is returned.
Note 3. These error behaviors does not occur for write access to the PHBIU or PLBIU address space which memory attribute is set to "Early Write Acknowledgment" by the ARM MPU.

45.3 Device Lifecycle Management

Device lifecycle identifies the current phase of the device and controls the capabilities of the debug interface, the serial programming interface and Renesas test mode. Figure 45.2 is the illustration of the device lifecycle. Table 45.8 shows the lifecycle definition and capability in each lifecycle.

Table 45.5 FlashSequencer的访问权限(2of2)

	安全访问	Non-secure access
FCKMHZ register	allowed	由Flash安全属性寄存器配置 当配置为安全时，● 写忽略可读 ● 未生成TrustZone访问错误。 当配置为非安全时●
其他寄存器	allowed	在编程擦除期间或在安全应用程序的暂停编程擦除期间● 写入忽略读取0x00 ● 未生成TrustZone访问错误 在其他状态 ●

45.2.5 地址空间安全属性

表45.6显示了地址空间的安全属性。

Table 45.6 地址空间安全属性

Region	Attribution
代码闪存安全	Secure
代码闪存非安全可调用	Non-secure callable
代码闪存不安全	Non-secure
数据闪存安全	Secure
数据闪存不安全	Non-Secure
SRAM secure	Secure
SRAM non-secure callable	Non-secure callable
SRAM non-secure	Non-secure
Peripherals	Exempt
其他区域	Exempt

Note: 豁免：不会进行任何检查。传播所有总线事务。

45.2.6 TrustZone访问错误

表45.7显示了TrustZone访问错误时的行为。行为因要访问的主区域或从区域而异。

Table 45.7 TrustZone访问错误时的行为

Area	CPU	DMAC/DTC
代码闪存、数据闪存、SRAM	检测SecureFault异常*2	● 传输未开始 ● 发生NMI或复位*1 ● 发生中断(DMA_TRANSERR)
其他区域	● 检测BusFault异常*2*3 ● 发生NMI或复位*1*2*3	● 停止转移 ● 发生NMI或复位*1 ● 发生中断(DMA_TRANSERR)

注1.通过TZFOAD.OAD位选择NMI或复位。
注2.当调试器访问发生TrustZone访问错误时，不会发生异常、NMI或复位。仅返回错误响应。
注3.对内存属性设置为"Early"的PHBIU或PLBIU地址空间的写访问不会发生这些错误行为
ARMMPU的"写确认"。

45.3 设备生命周期管理

设备生命周期识别设备的当前阶段并控制调试接口、串行编程接口和瑞萨测试模式的功能。图45.2是设备生命周期的图示。表45.8显示了每个生命周期中的生命周期定义和能力。

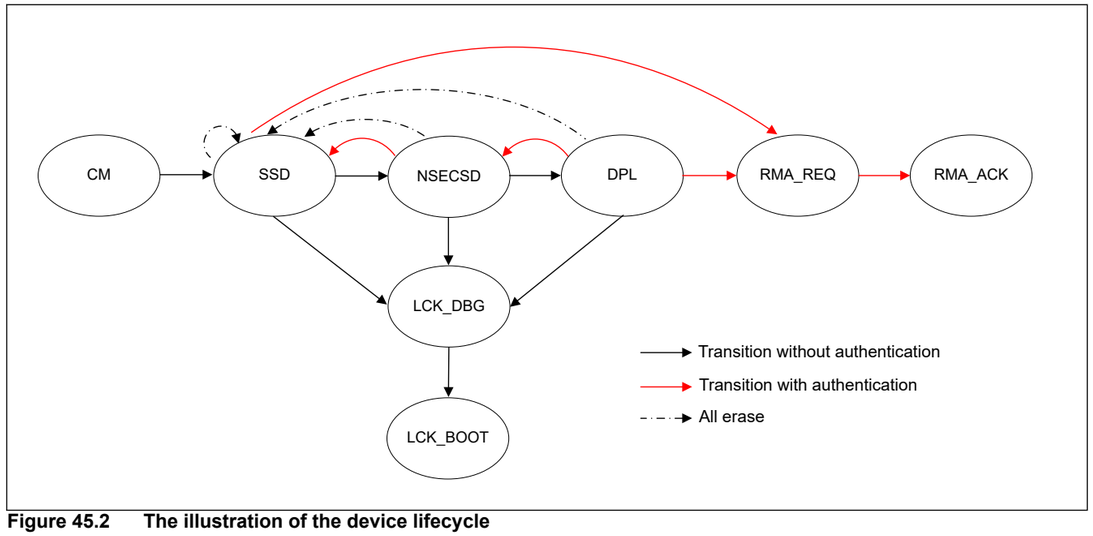


Figure 45.2 The illustration of the device lifecycle

Table 45.8 The lifecycle definition and the capability can be used in each lifecycle

Lifecycle	Definition	Debug level	Serial programming	Renesas test mode
CM	“Chip Manufacturing” The device is in Renesas factory. The state when the customer received the device.	DBG2	Available cannot access code/data flash area	Not available
SSD	“Secure Software Development” The secure part of application is being developed.	DBG2	Available can program/erase/read all code/data flash area	Not available
NSECSD	“Non-SECure Software Development” The non-secure part of application is being developed.	DBG1	Available can program/erase/read only non-secure code/data flash area	Not available
DPL	“DePLoyed” The device is in-field.	DBG0	Available cannot access code/data flash area	Not available
LCK_DBG	“LoCKed DeBuG” The debug interface is permanently disabled.	DBG0	Available cannot access code/data flash area	Not available
LCK_BOOT	“LoCKed BOOT interface” The debug interface and the serial programming interface are permanently disabled.	DBG0	Not available	Not available
RMA_REQ	“Return Material Authorization REQuest” Request for RMA. The customer must send the device to Renesas in this state.	DBG0	Available cannot access code/data flash area	Not available
RMA_ACK	“Return Material Authorization ACKnowledged” Failure analysis in Renesas	DBG2	Available cannot access code/data flash area	Available

45.3.1 Changing the Lifecycle State

Use the serial programming commands to change the device lifecycle state. See the boot firmware application note for the detail of command. The lifecycle cannot be updated by application but can read through the dedicated registers.

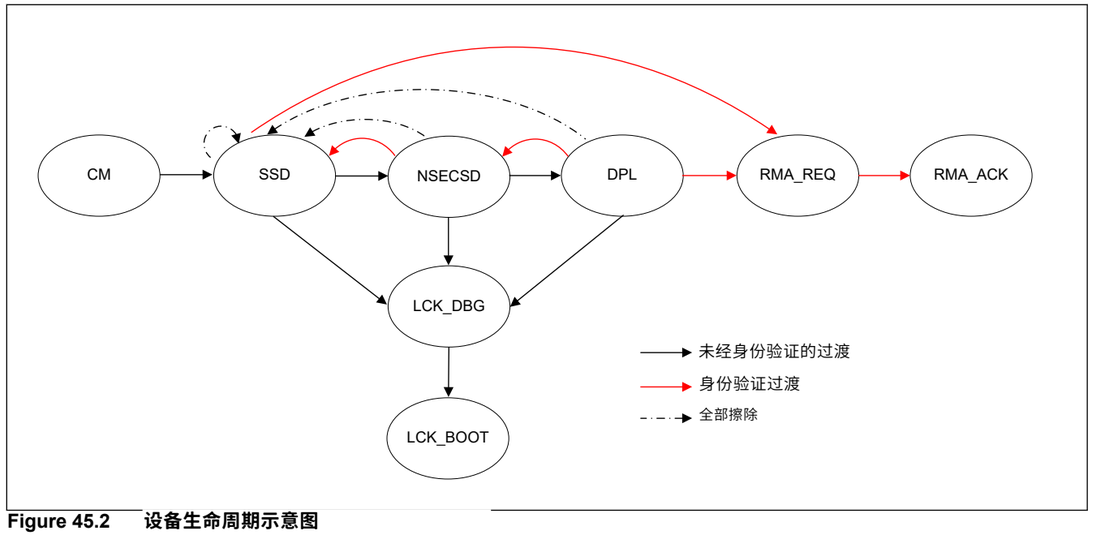


Figure 45.2 设备生命周期示意图

Table 45.8 生命周期定义和能力可以在每个生命周期中使用

Lifecycle	Definition	调试级别	串行编程	瑞萨测试模式
CM	“Chip Manufacturing” 该设备在瑞萨电子工厂。客户收到设备时的状态。	DBG2	Available 无法访问代码数据闪存区	无法使用
SSD	“Secure Software Development” 应用程序的安全部分正在开发中。	DBG2	Available 可以编程擦除读取所有代码数据闪存区域	无法使用
NSECSD	“Non-SECure Software Development” 应用程序的非安全部分正在开发中。	DBG1	Available 可以编程擦除只读非安全代码数据闪存区域	无法使用
DPL	“DePLoyed” 该设备在现场。	DBG0	Available 无法访问代码数据闪存区	无法使用
LCK_DBG	“LoCKed DeBuG” 调试接口被永久禁用。	DBG0	Available 无法访问代码数据闪存区	无法使用
LCK_BOOT	“LoCKed BOOT interface” 调试接口和串行编程接口被永久禁用。	DBG0	无法使用	无法使用
RMA_REQ	“退货授权请求” 请求RMA。客户必须在此状态下将设备发送给瑞萨电子。	DBG0	Available 无法访问代码数据闪存区	无法使用
RMA_ACK	“已确认退货授权” 瑞萨电子的故障分析	DBG2	Available 无法访问代码数据闪存区	Available

45.3.1 更改生命周期状态

使用串行编程命令更改设备生命周期状态。有关命令的详细信息，请参见启动固件应用说明。生命周期不能由应用程序更新，但可以通过专用寄存器读取。

As shown in Figure 45.2, there are three types lifecycle transition.

The first one is to change to lower debug access level or restrict the serial programming mode. This change can be done with no restriction.

Note: The debug interface is permanently disabled in LCK_DBG. After changed to LCK_DBG, the debug interface cannot be used forever.

Note: The debug interface and serial programming interface are permanently disabled in LCK_BOOT. After changed to LCK_BOOT, the debug interface and the serial programming interface cannot be used forever.

The second one is to change to higher debug access level or request for RMA. This change needs key authentication. The key length is 128 bits. The secure developer needs to inject two keys when the lifecycle is SSD state. One is "SECDBG_KEY" which is used to authentication to change the lifecycle from NSECSD to SSD. Other one is "RMA_KEY" which is used to authentication to change the lifecycle from SSD or DPL to RMA_REQ. The non-secure developer needs to inject one key when the lifecycle is NSECSD state. This is "NONSECDBG_KEY" which is used to authentication to change the lifecycle from DPL to NSECSD. See section 45.4. Key Injection for the detail of how to inject the key. The key authentication uses a challenge and response authentication or authentication using the unique ID. The authentication using the unique ID is available only transition to RMA_REQ. The following is the process of how to calculate the response, challenge and response authentication, or the authentication code using unique ID.

Response = AES128-CMAC (KEY, 128bits challenge)

Authentication code = AES128-CMAC (KEY, 128bits unique ID)

Note: In case the key is not injected, these lifecycle changes cannot be done.

Note: In the lifecycle transition from NSECSD to SSD or form DPL to NSECSD, the contents on the flash memory are not erased.

Note: MCU does not respond after changing to higher debug access level or RMA_REQ. If you continue to use the serial programming commands, need to re-enter the boot mode after a reset. See the boot firmware application note for the detail.

Note: In the lifecycle transition to RMA_REQ, the contents on the flash memory except permanently locked block or setting or BPS_SEL register are erased. The contents in the permanently locked block or register can be read by Renesas at failure analysis. Permanently locked block means the block which programming and erasure is disabled permanently by PBPS, PBPS_SEC and BPS_SEL register. Permanently locked register means SAS register which programming and erasure is disabled permanently by FSPR bit.

The third one is all erase. This is done by an initialize command unless an initialize command itself is disabled. The lifecycle is back to SSD and the contents on the flash memory is erased. If there is permanently locked block or register, an initialize command does not execute. In case of the all bits of PBPS and PBPS_SEC register are 1 and FSPR bit is1, an initialize command is executable.

Note: The initialize command can be issued by everyone, so contents on the flash memory are easily erased. Developers who do not want this can invalidate the initialize command permanently by parameter setting command.

Note: MCU does not respond after executing the initialize command. If you continue to use the serial programming commands, need to re-enter the boot mode after a reset. See the boot firmware application note for the detail.

45.3.2 Debug access level

There are three debug access levels, and the debug access level changes according to the lifecycle state.

- DBG2: The debugger connection is allowed, and no restriction to access memories and peripherals
- DBG1: The debugger connection is allowed, and restricted to access only non-secure memory regions and peripherals
- DBG0: The debugger connection is not allowed

45.3.3 Serial Programming

Whether a serial programmer can be connected and the range of flash memory that can be accessed depends on the lifecycle state as shown in Table 45.8. And the accepted serial programming command differs depending on the lifecycle state. See the boot firmware application note for the detail of command.

如图45.2所示，生命周期转换分为三种。

第一个是更改为降低调试访问级别或限制串行编程模式。这种改变可以不受限制地进行。

Note: 调试接口在LCK_DBG中被永久禁用。改成LCK_DBG后，调试接口就不能一直使用了。

Note: 调试接口和串行编程接口在LCK_BOOT中永久禁用。改成之后
LCK_BOOT、调试接口和串行编程接口不能永远使用。

第二个是更改为更高的调试访问级别或请求RMA。此更改需要密钥身份验证。密钥长度为128位。当生命周期为SSD状态时，安全开发人员需要注入两个密钥。一种是"SECDBG_KEY"，用于身份验证以将生命周期从NSECSD更改为SSD。另一种是"RMA_KEY"，用于身份验证以将生命周期从SSD或DPL更改为RMA_REQ。当生命周期为NSECSD状态时，非安全开发者需要注入一个密钥。这是"NONSECDBG_KEY"，用于身份验证以将生命周期从DPL更改为NSECSD。见第45.4节。KeyInjection有关如何注入密钥的详细信息。密钥身份验证使用质询和响应身份验证或使用唯一ID的身份验证。使用唯一ID的身份验证只能转换到RMA_REQ。以下是如何计算响应、挑战和响应身份验证或使用唯一ID的身份验证码的过程。

Response = AES128-CMAC (KEY, 128bits challenge)

认证码=AES128-CMAC(KEY 128bitsuniqueID)

Note: 如果未注入密钥，则无法完成这些生命周期更改。

Note: 在从NSECSD到SSD或从DPL到NSECSD的生命周期转换中，闪存上的内容不会被擦除。

Note: 更改为更高的调试访问级别或RMA_REQ后，MCU没有响应。如果继续使用串口编程命令，需要复位后重新进入开机模式。有关详细信息，请参阅启动固件应用说明。

Note: 在到RMA_REQ的生命周期转换中，闪存上的内容除了永久锁定的块或设置或BPS_SEL寄存器外被擦除。瑞萨在故障分析时可以读取永久锁定的块或寄存器中的内容。永久锁定块是指被PBPS、PBPS_SEC和BPS_SEL寄存器永久禁用编程和擦除的块。永久锁定寄存器是指通过FSPR位永久禁用编程和擦除的SAS寄存器。

第三个是全部擦除。这由初始化命令完成，除非初始化命令本身被禁用。生命周期回到SSD，闪存上的内容被擦除。如果存在永久锁定的块或寄存器，则不会执行初始化命令。如果PBPS和PBPS_SEC寄存器的所有位为1，FSPR位为1，则可执行初始化命令。

Note: 每个人都可以发出初始化命令，因此闪存上的内容很容易被擦除。不希望这样的开发者可以通过参数设置命令使初始化命令永久无效。

Note: 执行初始化命令后MCU没有响应。如果继续使用串口编程命令，需要复位后重新进入开机模式。有关详细信息，请参阅启动固件应用说明。

45.3.2 调试访问级别

共有三个调试访问级别，调试访问级别根据生命周期状态而变化。

- DBG2：允许调试器连接，不限制访问内存和外设
- DBG1：允许调试器连接，但仅限于访问非安全内存区域和外围设备
- DBG0：不允许调试器连接

45.3.3 串行编程

是否可以连接串行编程器以及可以访问的闪存范围取决于生命周期状态，如表45.8所示。并且接受的串行编程命令根据生命周期状态而有所不同。有关命令的详细信息，请参见启动固件应用说明。

45.3.4 Lifecycle changing example

The following is a typical lifecycle changing example.

Secure developer

- Change the lifecycle from CM to SSD by using the serial programming command.
- Set the memory security attribution of the code flash, data flash and SRAM by using the serial programming command.
- Program the secure application by using the serial programming interface and debug the secure application. Debug is possible if the lifecycle is CM, but it is impossible to set the memory security attribution in CM state. If the memory security attribution is not set, all area of the code flash, data flash and SRAM is Secure.

Note: Need to configure the registers listed in Table 45.10 as Non-secure only in NSECSD state. See section 45.6.1. Restrictions on setting the security attribution for details.

- Inject SECDBG_KEY and RMA_KEY by using the serial programming command (if need).
- Disable the all erase by using the serial programming command (if need).
- Change the lifecycle from SSD to NSECSD by using the serial programming command.

Non-secure developer

- Program the Non-secure application by using the serial programming interface and debug the Non-secure application.
- Inject NONSECDBG_KEY by using the serial programming command (if need).
- Disable the all erase by using the serial programming command (if need).
- Change the lifecycle to DPL by using the serial programming command.

45.3.5 Failure analysis

If the customer requests the failure analysis to Renesas, it is necessary to send the device after changing the lifecycle to RMA_REQ. If the lifecycle is not RMA_REQ, Renesas can not do the failure analysis. Because RMA_REQ is permanent state, it can not back to the another state after changing to RMA_REQ. It is assumed to change to SSD or NSECSD and analyze before changing to RMA_REQ.

Devices sent to Renesas will not be returned to customers. The device will be discarded.

Note: As described in the section 45.3.1. Changing the Lifecycle State, RMA_KEY is needed to change the lifecycle to RMA_REQ. If the customer forgets the RMA_KEY, Renesas can not do the failure analysis.

45.4 Key Injection

There are three steps required to inject a user key into the MCU.

First, the customer needs to create the 128 bits installation key. This key is called User Factory Programming Key (UFPK) and used to encrypt a user key. The customer gets the key of the wrapped version (W-UFPK) through the Renesas Key Wrapping Service.

Second the customer encrypts the user key using UFPK as the AES key.

Last the customer sends W-UFPK and the encrypted user key to the MCU by using serial programming interface. The sent user key is decrypted, wrapped with the hardware unique key, and then stored in the nonvolatile memory.

Figure 45.3 is the illustration of key injection. Table 45.9 shows the keys that can be injected by serial programming interface.

User Key is used for authentication during the life cycle transition.

45.3.4 生命周期更改示例

以下是一个典型的生命周期更改示例。

安全开发人员

●使用串行编程命令将生命周期从CM更改为SSD。

●使用串行编程命令设置codeflash、dataflash和SRAM的内存安全属性。

●使用串行编程接口对安全应用程序进行编程并调试安全应用程序。如果生命周期是CM，则可以调试，但无法在CM状态下设置内存安全属性。如果未设置内存安全属性，则代码闪存、数据闪存和SRAM的所有区域都是安全的。

Note: 仅在NSECSD状态下需要将表45.10中列出的寄存器配置为非安全。请参见第45.6.1节。设置安全属性的限制以获取详细信息。

●使用串行编程命令（如果需要）注入SECDBG_KEY和RMA_KEY。

●使用串行编程命令禁用全部擦除（如果需要）。

●使用串行编程命令将生命周期从SSD更改为NSECSD。

Non-secure developer

●使用串行编程接口对非安全应用程序进行编程并调试非安全应用程序。

●使用串行编程命令（如果需要）注入NONSECDBG_KEY。

●使用串行编程命令禁用全部擦除（如果需要）。

●使用串行编程命令将生命周期更改为DPL。

45.3.5 故障分析

如果客户要求对瑞萨进行故障分析，则需要在将生命周期更改为RMA_REQ后发送设备。如果生命周期不是RMA_REQ，瑞萨将无法进行故障分析。因为RMA_REQ是永久状态，所以在更改为RMA_REQ后不能回到另一个状态。假设更改为SSD或NSECSD并在更改为RMA_REQ之前进行分析。

发送给瑞萨的设备将不会退还给客户。该设备将被丢弃。

Note: 如第45.3.1节所述。更改LifecycleState，需要RMA_KEY才能将生命周期更改为RMA_REQ。如果客户忘记了RMA_KEY，瑞萨将无法进行故障分析。

45.4 密钥注入

将用户密钥注入MCU需要三个步骤。

首先，客户需要创建128位安装密钥。此密钥称为用户工厂编程密钥(UFPK)，用于加密用户密钥。客户通过RenesasKeyWrappingService获得打包版本(W-UFPK)的密钥。

其次，客户使用UFPK作为AES密钥对用户密钥进行加密。

最后客户通过串行编程接口将W-UFPK和加密的用户密钥发送给MCU。发送的用户密钥被解密，用硬件唯一密钥包装，然后存储在非易失性存储器中。

图45.3是密钥注入的示意图。表45.9显示了可以通过串行编程接口注入的密钥。

用户密钥用于生命周期过渡期间的身份验证。

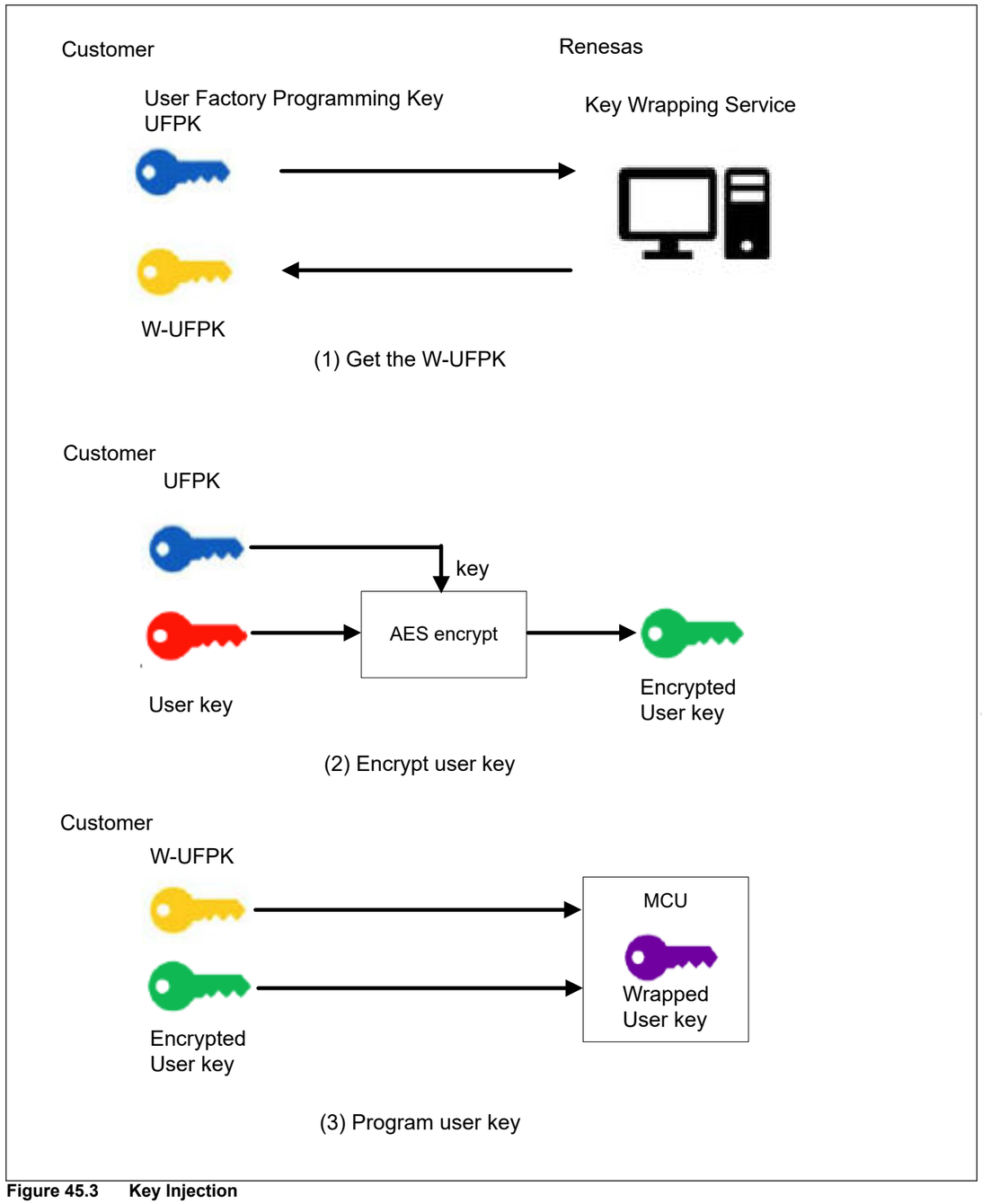


Figure 45.3 Key Injection

Table 45.9 The keys that can be injected by serial programming

Lifecycle transition	SECDBG_KEY, NONSECDBG_KEY, RMA_KEY

45.5 Register Description

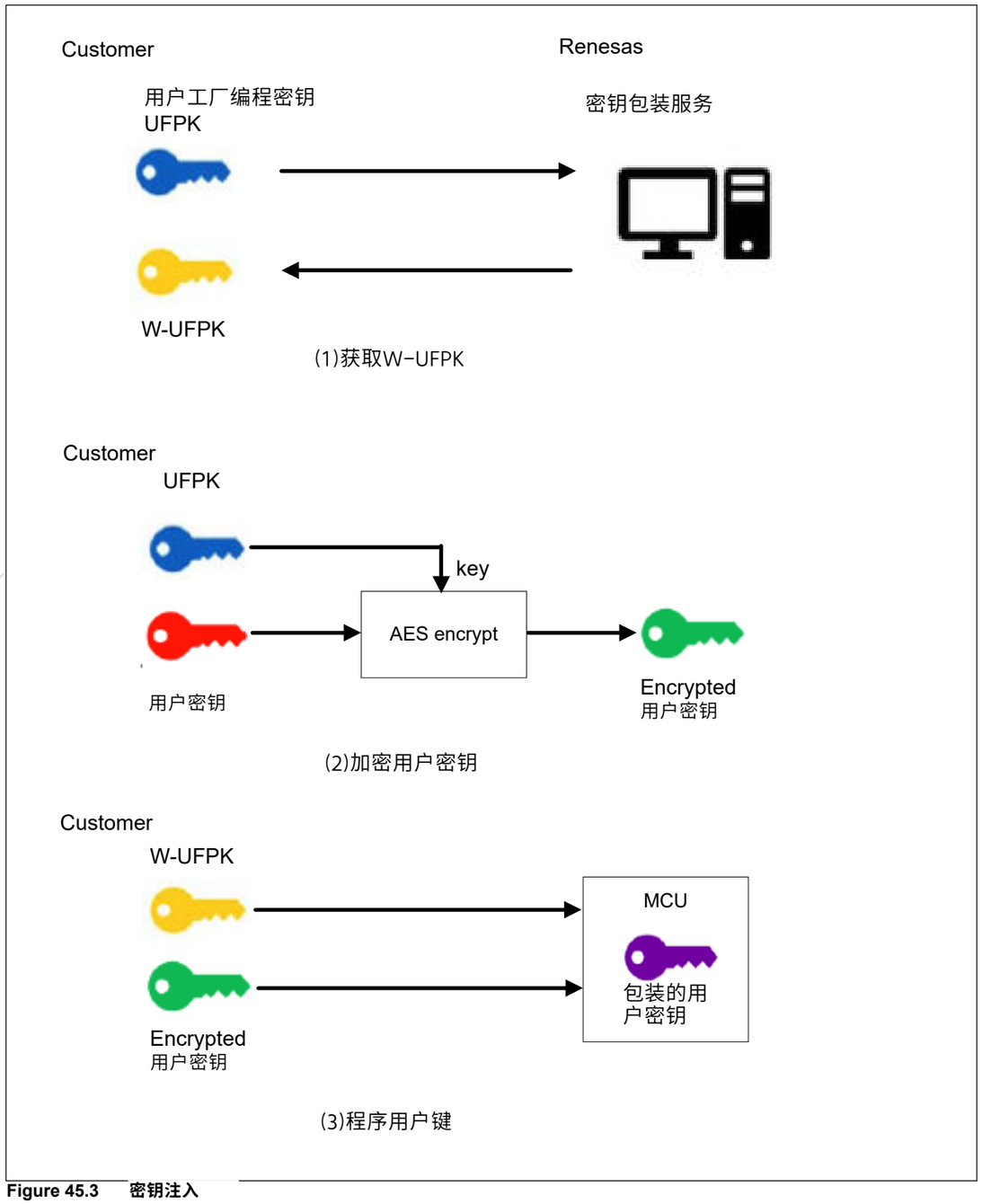


Figure 45.3 密钥注入

Table 45.9 串行编程可以注入的密钥

生命周期过渡	SECDBG_KEY, NONSECDBG_KEY, RMA_KEY

45.5 注册说明

45.5.1 PSARB : Peripheral Security Attribution Register B

Base address: PSCU = 0x400E_0000

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PSARB31	PSARB30	PSARB29	PSARB28	PSARB27	—	—	—	—	PSARB22	—	—	PSARB19	PSARB18	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PSARB9	PSARB8	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	—	This bit is read as 1. The write value should be 1.	R/W
1	—	This bit is read as 1. The write value should be 1.	R/W
2	—	This bit is read as 1. The write value should be 1.	R/W
3	—	This bit is read as 1. The write value should be 1.	R/W
5:4	—	These bits are read as 1. The write value should be 1.	R/W
6	—	This bit is read as 1. The write value should be 1.	R/W
7	—	This bit is read as 1. The write value should be 1.	R/W
8	PSARB8	IIC1 and the MSTPCRB.MSTPB8 bit security attribution 0: Secure 1: Non-secure	R/W
9	PSARB9	IIC0 and the MSTPCRB.MSTPB9 bit security attribution 0: Secure 1: Non-secure	R/W
10	—	This bit is read as 1. The write value should be 1.	R/W
11	—	This bit is read as 1. The write value should be 1.	R/W
12	—	This bit is read as 1. The write value should be 1.	R/W
14:13	—	These bits are read as 1. The write value should be 1.	R/W
15	—	This bit is read as 1. The write value should be 1.	R/W
16	—	This bit is read as 1. The write value should be 1.	R/W
17	—	This bit is read as 1. The write value should be 1.	R/W
18	PSARB18	SPI1 and the MSTPCRB.MSTPB18 bit security attribution 0: Secure 1: Non-secure	R/W
19	PSARB19	SPI0 and the MSTPCRB.MSTPB19 bit security attribution 0: Secure 1: Non-secure	R/W
21:20	—	These bits are read as 1. The write value should be 1.	R/W
22	PSARB22	SCI9 and the MSTPCRB.MSTPB22 bit security attribution 0: Secure 1: Non-secure	R/W
23	—	This bit is read as 1. The write value should be 1.	R/W
24	—	This bit is read as 1. The write value should be 1.	R/W
25	—	This bit is read as 1. The write value should be 1.	R/W

45.5.1 PSARB:外设安全属性寄存器B

Base address: PSCU = 0x400E_0000

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PSARB31	PSARB30	PSARB29	PSARB28	PSARB27	—	—	—	—	PSARB22	—	—	PSARB19	PSARB18	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PSARB9	PSARB8	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	—	该位读取为1。写入值应为1。	R/W
1	—	该位读取为1。写入值应为1。	R/W
2	—	该位读取为1。写入值应为1。	R/W
3	—	该位读取为1。写入值应为1。	R/W
5:4	—	这些位被读取为1。写入值应为1。	R/W
6	—	该位读取为1。写入值应为1。	R/W
7	—	该位读取为1。写入值应为1。	R/W
8	PSARB8	IIC1和MSTPCRB.MSTPB8位安全归属 0: Secure 1: Non-secure	R/W
9	PSARB9	IIC0和MSTPCRB.MSTPB9位安全归属 0: Secure 1: Non-secure	R/W
10	—	该位读取为1。写入值应为1。	R/W
11	—	该位读取为1。写入值应为1。	R/W
12	—	该位读取为1。写入值应为1。	R/W
14:13	—	这些位被读取为1。写入值应为1。	R/W
15	—	该位读取为1。写入值应为1。	R/W
16	—	该位读取为1。写入值应为1。	R/W
17	—	该位读取为1。写入值应为1。	R/W
18	PSARB18	SPI1和MSTPCRB.MSTPB18位安全归属 0: Secure 1: Non-secure	R/W
19	PSARB19	SPI0和MSTPCRB.MSTPB19位安全归属 0: Secure 1: Non-secure	R/W
21:20	—	这些位被读取为1。写入值应为1。	R/W
22	PSARB22	SCI9和MSTPCRB.MSTPB22位安全归属 0: Secure 1: Non-secure	R/W
23	—	该位读取为1。写入值应为1。	R/W
24	—	该位读取为1。写入值应为1。	R/W
25	—	该位读取为1。写入值应为1。	R/W

Bit	Symbol	Function	R/W
26	—	This bit is read as 1. The write value should be 1.	R/W
27	PSARB27	SCI4 and the MSTPCRB.MSTPB27 bit security attribution 0: Secure 1: Non-secure	R/W
28	PSARB28	SCI3 and the MSTPCRB.MSTPB28 bit security attribution 0: Secure 1: Non-secure	R/W
29	PSARB29	SCI2 and the MSTPCRB.MSTPB29 bit security attribution 0: Secure 1: Non-secure	R/W
30	PSARB30	SCI1 and the MSTPCRB.MSTPB30 bit security attribution 0: Secure 1: Non-secure	R/W
31	PSARB31	SCI0 and the MSTPCRB.MSTPB31 bit security attribution 0: Secure 1: Non-secure	R/W

Note: A bit undefined in this table is reserved bit. The reserved bit should be kept the initial value.
Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The PSARB specifies the security attribution for each module and the corresponding bit in Module Stop Control Register.

45.5.2 PSARC : Peripheral Security Attribution Register C

Base address: PSCU = 0x400E_0000
Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PSARC31	—	—	—	PSARC27	—	—	—	—	—	PSARC21	PSARC20	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PSARC13	—	—	—	—	—	—	—	—	—	—	—	PSARC1	PSARC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	PSARC0	CAC and the MSTPCRC.MSTPC0 bit security attribution 0: Secure 1: Non-secure	R/W
1	PSARC1	CRC and the MSTPCRC.MSTPC1 bit security attribution 0: Secure 1: Non-secure	R/W
2	—	This bit is read as 1. The write value should be 1.	R/W
3	—	This bit is read as 1. The write value should be 1.	R/W
7:4	—	These bits are read as 1. The write value should be 1.	R/W
8	—	This bit is read as 1. The write value should be 1.	R/W
11:9	—	These bits are read as 1. The write value should be 1.	R/W
12	—	This bit is read as 1. The write value should be 1.	R/W
13	PSARC13	DOC and the MSTPCRC.MSTPC13 bit security attribution 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
26	—	该位读取为1。写入值应为1。	R/W
27	PSARB27	SCI4和MSTPCRB.MSTPB27位安全归属 0: Secure 1: Non-secure	R/W
28	PSARB28	SCI3和MSTPCRB.MSTPB28位安全归属 0: Secure 1: Non-secure	R/W
29	PSARB29	SCI2和MSTPCRB.MSTPB29位安全归属 0: Secure 1: Non-secure	R/W
30	PSARB30	SCI1和MSTPCRB.MSTPB30位安全归属 0: Secure 1: Non-secure	R/W
31	PSARB31	SCI0和MSTPCRB.MSTPB31位安全归属 0: Secure 1: Non-secure	R/W

Note: 该表中未定义的位是保留位。保留位应保持初始值。
Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

PSARB指定每个模块的安全属性以及模块停止控制寄存器中的相应位。

45.5.2 PSARC:外设安全属性寄存器C

Base address: PSCU = 0x400E_0000
Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PSARC31	—	—	—	PSARC27	—	—	—	—	—	PSARC21	PSARC20	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PSARC13	—	—	—	—	—	—	—	—	—	—	—	PSARC1	PSARC0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	PSARC0	CAC和MSTPCRC.MSTPC0位安全属性 0: Secure 1: Non-secure	R/W
1	PSARC1	CRC和MSTPCRC.MSTPC1位安全属性 0: Secure 1: Non-secure	R/W
2	—	该位读取为1。写入值应为1。	R/W
3	—	该位读取为1。写入值应为1。	R/W
7:4	—	这些位被读取为1。写入值应为1。	R/W
8	—	该位读取为1。写入值应为1。	R/W
11:9	—	这些位被读取为1。写入值应为1。	R/W
12	—	该位读取为1。写入值应为1。	R/W
13	PSARC13	DOC和MSTPCRC.MSTPC13位安全属性 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
19:14	—	These bits are read as 1. The write value should be 1.	R/W
20	PSARC20	TFU and the MSTPCRC.MSTPC20 bit security attribution 0: Secure 1: Non-secure	R/W
21	PSARC21	IIRFA and the MSTPCRC.MSTPC21 bit security attribution 0: Secure 1: Non-secure	R/W
26:22	—	These bits are read as 1. The write value should be 1.	R/W
27	PSARC27	CANFD and the MSTPCRC.MSTPC27 bit security attribution 0: Secure 1: Non-secure	R/W
30:28	—	These bits are read as 1. The write value should be 1.	R/W
31	PSARC31	SCE5 and the MSTPCRC.MSTPC31 bit security attribution 0: Secure 1: Non-secure	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The PSARC specifies the security attribution for each module and the corresponding bit in Module Stop Control Register.

45.5.3 PSARD : Peripheral Security Attribution Register D

Base address: PSCU = 0x400E_0000

Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	PSARD28	PSARD27	PSARD26	PSARD25	—	—	PSARD22	—	PSARD20	PSARD19	—	—	PSARD16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	PSARD14	PSARD13	PSARD12	PSARD11	—	—	—	—	—	—	—	PSARD3	PSARD2	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 1. The write value should be 1.	R/W
2	PSARD2	AGT1 and the MSTPCRD.MSTPD2 bit security attribution 0: Secure 1: Non-secure	R/W
3	PSARD3	AGT0 and the MSTPCRD.MSTPD3 bit security attribution 0: Secure 1: Non-secure	R/W
10:4	—	These bits are read as 1. The write value should be 1.	R/W
11	PSARD11	POEG Group D and the MSTPCRD.MSTPD11 bit security attribution 0: Secure 1: Non-secure	R/W
12	PSARD12	POEG Group C and the MSTPCRD.MSTPD12 bit security attribution 0: Secure 1: Non-secure	R/W
13	PSARD13	POEG Group B and the MSTPCRD.MSTPD13 bit security attribution 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
19:14	—	这些位被读取为1。写入值应为1。	R/W
20	PSARC20	TFU和MSTPCRC.MSTPC20位安全属性 0: Secure 1: Non-secure	R/W
21	PSARC21	IIRFA和MSTPCRC.MSTPC21位安全属性 0: Secure 1: Non-secure	R/W
26:22	—	这些位被读取为1。写入值应为1。	R/W
27	PSARC27	CANFD和MSTPCRC.MSTPC27位安全属性 0: Secure 1: Non-secure	R/W
30:28	—	这些位被读取为1。写入值应为1。	R/W
31	PSARC31	SCE5和MSTPCRC.MSTPC31位安全归属 0: Secure 1: Non-secure	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

PSARC指定每个模块的安全属性以及模块停止控制寄存器中的相应位。

45.5.3 PSARD:外围安全属性寄存器D

Base address: PSCU = 0x400E_0000

Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	PSARD28	PSARD27	PSARD26	PSARD25	—	—	PSARD22	—	PSARD20	PSARD19	—	—	PSARD16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	PSARD14	PSARD13	PSARD12	PSARD11	—	—	—	—	—	—	—	PSARD3	PSARD2	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
1:0	—	这些位被读取为1。写入值应为1。	R/W
2	PSARD2	AGT1和MSTPCRD.MSTPD2位安全归属 0: Secure 1: Non-secure	R/W
3	PSARD3	AGT0和MSTPCRD.MSTPD3位安全属性 0: Secure 1: Non-secure	R/W
10:4	—	这些位被读取为1。写入值应为1。	R/W
11	PSARD11	POEGGroupD和MSTPCRD.MSTPD11位安全归属 0: Secure 1: Non-secure	R/W
12	PSARD12	POEGGroupC和MSTPCRD.MSTPD12位安全归属 0: Secure 1: Non-secure	R/W
13	PSARD13	POEGGroupB和MSTPCRD.MSTPD13位安全归属 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
14	PSARD14	POEG Group A and the MSTPCRD.MSTPD14 bit security attribution 0: Secure 1: Non-secure	R/W
15	—	This bit is read as 1. The write value should be 1.	R/W
16	PSARD16	ADC and the MSTPCRD.MSTPD16 bit security attribution 0: Secure 1: Non-secure	R/W
18:17	—	These bits are read as 1. The write value should be 1.	R/W
19	PSARD19	DAC12 unit1 and the MSTPCRD.MSTPD19 bit security attribution 0: Secure 1: Non-secure	R/W
20	PSARD20	DAC12 unit0 and the MSTPCRD.MSTPD20 bit security attribution 0: Secure 1: Non-secure	R/W
21	—	This bit is read as 1. The write value should be 1.	R/W
22	PSARD22	TSN and the MSTPCRD.MSTPD22 bit security attribution 0: Secure 1: Non-secure	R/W
24:23	—	These bits are read as 1. The write value should be 1.	R/W
25	PSARD25	ACMPHS3 and the MSTPCRD.MSTPD25 bit security attribution 0: Secure 1: Non-secure	R/W
26	PSARD26	ACMPHS2 and the MSTPCRD.MSTPD26 bit security attribution 0: Secure 1: Non-secure	R/W
27	PSARD27	ACMPHS1 and the MSTPCRD.MSTPD27 bit security attribution 0: Secure 1: Non-secure	R/W
28	PSARD28	ACMPHS0 and the MSTPCRD.MSTPD28 bit security attribution 0: Secure 1: Non-secure	R/W
31:29	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The PSARD specifies the security attribution for each module and the corresponding bit in Module Stop Control Register.

45.5.4 PSARE : Peripheral Security Attribution Register E

Base address: PSCU = 0x400E_0000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	PSARE4	—	—	PSARE1	PSARE0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
14	PSARD14	POEGGroupA和MSTPCRD.MSTPD14位安全归属 0: Secure 1: Non-secure	R/W
15	—	该位读取为1。写入值应为1。	R/W
16	PSARD16	ADC和MSTPCRD.MSTPD16位安全属性 0: Secure 1: Non-secure	R/W
18:17	—	这些位被读取为1。写入值应为1。	R/W
19	PSARD19	DAC12unit1和MSTPRD.MSTPD19位安全属性 0: Secure 1: Non-secure	R/W
20	PSARD20	DAC12unit0和MSTPRD.MSTPD20位安全归属 0: Secure 1: Non-secure	R/W
21	—	该位读取为1。写入值应为1。	R/W
22	PSARD22	TSN和MSTPCRD.MSTPD22位安全属性 0: Secure 1: Non-secure	R/W
24:23	—	这些位被读取为1。写入值应为1。	R/W
25	PSARD25	ACMPHS3和MSTPCRD.MSTPD25位安全归属 0: Secure 1: Non-secure	R/W
26	PSARD26	ACMPHS2和MSTPCRD.MSTPD26位安全属性 0: Secure 1: Non-secure	R/W
27	PSARD27	ACMPHS1和MSTPCRD.MSTPD27位安全属性 0: Secure 1: Non-secure	R/W
28	PSARD28	ACMPHS0和MSTPCRD.MSTPD28位安全属性 0: Secure 1: Non-secure	R/W
31:29	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

PSARD指定每个模块的安全属性以及模块停止控制寄存器中的相应位。

45.5.4 PSARE:外设安全属性寄存器E

Base address: PSCU = 0x400E_0000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	PSARE4	—	—	PSARE1	PSARE0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	PSARE0	WDT security attribution 0: Secure 1: Non-secure	R/W
1	PSARE1	IWDT security attribution 0: Secure 1: Non-secure	R/W
3:2	—	These bits are read as 1. The write value should be 1.	R/W
4	PSARE4	KINT and the MSTPCRE.MSTPE4 bit security attribution 0: Secure 1: Non-secure	R/W
31:5	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The PSARE specifies the security attribution for each module and the corresponding bit in Module Stop Control Register.

45.5.5 MSSAR : Module Stop Security Attribution Register

Base address: PSCU = 0x400E_0000

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	MSSAR3	MSSAR2	MSSAR1	MSSAR0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MSSAR0	The MSTPCRC.MSTPC14 bit security attribution 0: Secure 1: Non-secure	R/W
1	MSSAR1	The MSTPCRA.MSTPA22 bit security attribution 0: Secure 1: Non-secure	R/W
2	MSSAR2	The MSTPCRA.MSTPA7 bit security attribution 0: Secure 1: Non-secure	R/W
3	MSSAR3	The MSTPCRA.MSTPA0 bit security attribution 0: Secure 1: Non-secure	R/W
31:4	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The MSSAR specifies the security attribution for the corresponding bit in Module Stop Control Register.

Bit	Symbol	Function	R/W
0	PSARE0	WDT安全归属 0: Secure 1: Non-secure	R/W
1	PSARE1	IWDT安全归属 0: Secure 1: Non-secure	R/W
3:2	—	这些位被读取为1。写入值应为1。	R/W
4	PSARE4	KINT和MSTPCRE.MSTPE4位安全属性 0: Secure 1: Non-secure	R/W
31:5	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

PSARE指定每个模块的安全属性以及模块停止控制寄存器中的相应位。

45.5.5 MSSAR：模块停止安全属性寄存器

Base address: PSCU = 0x400E_0000

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	MSSAR3	MSSAR2	MSSAR1	MSSAR0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MSSAR0	MSTPCRC.MSTPC14位安全属性 0: Secure 1: Non-secure	R/W
1	MSSAR1	MSTPCRA.MSTPA22位安全属性 0: Secure 1: Non-secure	R/W
2	MSSAR2	MSTPCRA.MSTPA7位安全属性 0: Secure 1: Non-secure	R/W
3	MSSAR3	MSTPCRA.MSTPA0位安全属性 0: Secure 1: Non-secure	R/W
31:4	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

MSSAR指定模块停止控制寄存器中相应位的安全属性。

45.5.6 CFSAMONA : Code Flash Security Attribution Monitor Register A

Base address: PSCU = 0x400E_0000

Offset address: 0x18

Bit position:	31								23								15								0
Bit field:	—	—	—	—	—	—	—	—	CFS2[8:0]								—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	The value set by user								0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	These bits are read as 0.	R
23:15	CFS2[8:0]	Code Flash Secure area 2 Indicate the total area of secure region and non-secure callable region for code flash.	R
31:24	—	These bits are read as 0.	R

Note: The CFSAMONA does not have security attribution.

45.5.7 CFSAMONB : Code Flash Security Attribution Monitor Register B

Base address: PSCU = 0x400E_0000

Offset address: 0x1C

Bit position:	31								23								10								0
Bit field:	—	—	—	—	—	—	—	—	CFS1[13:0]								—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	The value set by user								0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	These bits are read as 0.	R
23:10	CFS1[13:0]	Code Flash Secure area 1 Indicate the area of secure region for code flash.	R
31:24	—	These bits are read as 0.	R

Note: The CFSAMONB does not have security attribution.

45.5.8 DFSAMON : Data Flash Security Attribution Monitor Register

Base address: PSCU = 0x400E_0000

Offset address: 0x20

Bit position:	31																15					10									0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DFS[5:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	The value set by user														

Bit	Symbol	Function	R/W
9:0	—	These bits are read as 0.	R
15:10	DFS[5:0]	Data flash Secure area Indicate the area of Secure region for data flash.	R
31:16	—	These bits are read as 0.	R

Note: The DFSAMON does not have security attribution.

45.5.6 CFSAMONA：代码闪存安全属性监控寄存器A

Base address: PSCU = 0x400E_0000

Offset address: 0x18

Bit position:	31								23								15								0
Bit field:	—	—	—	—	—	—	—	—	CFS2[8:0]								—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	用户设置的值								0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	这些位读为0。	R
23:15	CFS2[8:0]	CodeFlash安全区2 指示代码闪存的安全区域和非安全可调用区域的总面积。	R
31:24	—	这些位读为0。	R

Note: CFSAMONA没有安全属性。

45.5.7 CFSAMONB:代码闪存安全属性监控寄存器B

Base address: PSCU = 0x400E_0000

Offset address: 0x1C

Bit position:	31								23								10								0
Bit field:	—	—	—	—	—	—	—	—	CFS1[13:0]								—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	用户设置的值								0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	这些位读为0。	R
23:10	CFS1[13:0]	CodeFlash安全区1 指示代码闪存的安全区域区域。	R
31:24	—	这些位读为0。	R

Note: CFSAMONB没有安全属性。

45.5.8 DFSAMON:数据闪存安全属性监控寄存器

Base address: PSCU = 0x400E_0000

Offset address: 0x20

Bit position:	31																15					10									0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DFS[5:0]														
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	用户设置的值														

Bit	Symbol	Function	R/W
9:0	—	这些位读为0。	R
15:10	DFS[5:0]	数据闪存安全区 指示数据闪存的安全区域区域。	R
31:16	—	这些位读为0。	R

Note: DFSAMON没有安全属性。

45.5.9 SSAMONA : SRAM Security Attribution Monitor Register A

Base address: PSCU = 0x400E_0000

Offset address: 0x24

Bit position:	31										20												13												0
Bit field:	—	—	—	—	—	—	—	—	—	—	SS2[7:0]												—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	The value set by user												0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
12:0	—	These bits are read as 0.	R
20:13	SS2[7:0]	SRAM Secure area 2 Indicate the total area of Secure region and non-secure callable region for SRAM.	R
31:21	—	These bits are read as 0.	R

Note: The SSAMONA does not have security attribution.

45.5.10 SSAMONB : SRAM Security Attribution Monitor Register B

Base address: PSCU = 0x400E_0000

Offset address: 0x28

Bit position:	31										20										10										0
Bit field:	—	—	—	—	—	—	—	—	—	—	SS1[10:0]										—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	The value set by user										0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	These bits are read as 0.	R
20:10	SS1[10:0]	SRAM secure area 1 Indicate the area of secure region for SRAM.	R
31:21	—	These bits are read as 0.	R

Note: The SSAMONB does not have security attribution.

45.5.11 DLMMON : Device Lifecycle Management State Monitor Register

Base address: PSCU = 0x400E_0000

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	DLMMON[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	DLM status value			

45.5.9 SSAMONA:SRAM安全属性监控寄存器A

Base address: PSCU = 0x400E_0000

Offset address: 0x24

Bit position:	31										20												13												0
Bit field:	—	—	—	—	—	—	—	—	—	—	SS2[7:0]												—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	用户设置的值												0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
12:0	—	这些位读为0。	R
20:13	SS2[7:0]	SRAM安全区域2 指示SRAM的安全区域和非安全可调用区域的总面积。	R
31:21	—	这些位读为0。	R

Note: SSAMONA没有安全属性。

45.5.10 SSAMONB:SRAM安全属性监控寄存器B

Base address: PSCU = 0x400E_0000

Offset address: 0x28

Bit position:	31										20										10										0
Bit field:	—	—	—	—	—	—	—	—	—	—	SS1[10:0]										—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	用户设置的值										0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	这些位读为0。	R
20:10	SS1[10:0]	SRAM安全区1 指示SRAM的安全区域区域。	R
31:21	—	这些位读为0。	R

Note: SSAMONB没有安全属性。

45.5.11 DLMMON:设备生命周期管理状态监视器寄存器

Base address: PSCU = 0x400E_0000

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	DLMMON[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	DLM状态值			

Bit	Symbol	Function	R/W
3:0	DLMMON[3:0]	Device Lifecycle Management State Monitor 0x1: CM 0x2: SSD 0x3: NSECSD 0x4: DPL 0x5: LCK_DBG 0x6: LCK_BOOT 0x7: RMA_REQ 0x8: RMA_ACK Others: Reserved	R
31:4	—	These bits are read as 0. The write value should be 0.	R

Note: The DLMMON does not have security attribution.

45.5.12 TZFSAR : TrustZone Filter Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x180

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TZFSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	TZFSA0	Security attributes of registers for TrustZone Filter 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1.	R

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

TZFSA0 bit (Security attributes of registers for TrustZone Filter)

Security attributes of register for TZFOAD and TZFPT registers.

45.5.13 TZFOAD : TrustZone Filter Operation After Detection Register

Base address: TZF = 0x4000_0E00

Offset address: 0x00

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation after detection 0: Non-maskable interrupt 1: Reset	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
3:0	DLMMON[3:0]	设备生命周期管理状态监视器 0x1: CM 0x2: SSD 0x3: NSECSD 0x4: DPL 0x5: LCK_DBG 0x6: LCK_BOOT 0x7: RMA_REQ 0x8: RMA_ACK Others: Reserved	R
31:4	—	这些位被读取为0。写入值应为0。	R

Note: DLMMON没有安全属性。

45.5.12 TZFSAR:TrustZone过滤器安全属性寄存器

Base address: CPSCU = 0x4000_8000

Offset address: 0x180

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TZFSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	TZFSA0	TrustZone过滤器寄存器的安全属性 0: Secure 1: Non-secure	R/W
31:1	—	这些位读为1。	R

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

TZFSA0位（TrustZone过滤器寄存器的安全属性）

TZFOAD和TZFPT寄存器的寄存器安全属性。

45.5.13 TZFOAD：检测寄存器后的TrustZone过滤器操作

Base address: TZF = 0x4000_0E00

Offset address: 0x00

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	OAD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	检测后操作 0：不可屏蔽中断1：复位	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
15:8	KEY[7:0]	KeyCode This bit is used to enable or disable writing of the OAD bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

OAD bit (Operation after detection)

The OAD bit is specified to generate either reset or non-maskable interrupt when the access to the protect region is detected by the TrustZone Filter.

When the OAD bit is set, write 0xA5 in the KEY[7:0] bits at the same time.

KEY[7:0] bits (KeyCode)

The KEY[7:0] bits are used to enable or disable writing of the OAD bit. When writing the OAD bit, write 0xA5 in the KEY[7:0] bits at the same time.

When the KEY[7:0] bits value except 0xA5 is written in, the OAD bit is not updated.

The KEY[7:0] bits are read always as 0x00.

45.5.14 TZFPT : TrustZone Filter Protect Register

Base address: TZF = 0x4000_0E00

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: All Bus TrustZone Filter register writing is protected. Read is possible. 1: All Bus TrustZone Filter register writing is possible.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	KeyCode This bit is used to enable or disable writing of the PROTECT bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

PROTECT bit (Protection of register)

The PROTECT bit controls enable or disable writing to the corresponding registers to be protected. TZFOAD register is protected by PROTECT.

When the PROTECT bit is set, write 0xA5 in the KEY[7:0] bits at the same time.

KEY[7:0] bits (KeyCode)

The KEY[7:0] bits are used to enable or disable writing of the PROTECT bit. When writing the PROTECT bit, write 0xA5 in the KEY[7:0] bits at the same time.

When the KEY[7:0] bits value except 0xA5 is written in, the PROTECT bit is not updated.

The KEY[7:0] bits are read always as 0x00.

45.6 Usage Notes

Bit	Symbol	Function	R/W
15:8	KEY[7:0]	KeyCode 该位用于启用或禁用OAD位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

OAD位（检测后的操作）

当TrustZone过滤器检测到对保护区域的访问时，OAD位被指定为产生复位或不可屏蔽中断。

当OAD位置位时，同时向KEY[7:0]位写入0xA5。

KEY[7:0] bits (KeyCode)

KEY[7:0]位用于启用或禁用OAD位的写入。写入OAD位时，将0xA5写入KEY[7:0]位。

当KEY[7:0]位值除0xA5被写入时，OAD位不会更新。

KEY[7:0]位总是被读取为0x00。

45.5.14 TZFPT:TrustZone过滤器保护寄存器

Base address: TZF = 0x4000_0E00

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	保护
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	注册保护 0：所有总线TrustZone过滤器寄存器写入受到保护。读取是可能的。1：所有总线TrustZone过滤器寄存器写入都是可能的。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	KeyCode 该位用于启用或禁用PROTECT位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

PROTECT位（寄存器保护）

PROTECT位控制启用或禁用对受保护的相应寄存器的写入。TZFOAD寄存器受PROTECT保护。

当PROTECT位置位时，同时向KEY[7:0]位写入0xA5。

KEY[7:0] bits (KeyCode)

KEY[7:0]位用于启用或禁用PROTECT位的写入。写入PROTECT位时，同时向KEY[7:0]位写入0xA5。

写入除0xA5以外的KEY[7:0]位值时，PROTECT位不更新。

KEY[7:0]位总是被读取为0x00。

45.6 使用说明

45.6.1 Restrictions on setting the security attribution

To set the software breakpoint, the debugger need to re-program the flash. Table 45.10 shows the registers that the debugger sets to re-program the flash. If the security attribution of the register listed in Table 45.10 is configured as secure, the debugger can not set the software breakpoint in NSECSD state because the debugger can not change the register setting. Secure developper need to configure the registers listed in Table 45.10 as non-secure only in NSECSD state.

Table 45.10 The registers that the debugger sets to re-program the flash

Function name	Register name
Clock Generation Circuit	SCKDIVCR, SCKCR, PLLCCR, PLLCR, HOCOCR, MOCOCR
Low-Power modes	OPCCR

45.6.2 SAU setting

After reset, all of address space is marked as Secure by SAU default setting. SAU_CTRL register should be set to 0x2 to enable the IDAU security attribution. That is, after setting SAU_CTRL register to 0x2, the address space security attribution becomes as shown in Table 45.6.

45.6.3 Non-secure exception during the setting of FACI registers

As shown in Table 45.5, the registers related to FACI are protected from non-secure access only during programming/erasure or during suspend programming/erasure. Outside of this state, the access from non-secure region is not protected. For example, when programming by the secure user, the non-secure user can rewrite the FSADDR if a non-secure exception occurs immediately after “Set the start address of the target block to the FSADDR register” flow in Figure 43.13. If the FACI command is issued after the non-secure exception processing is completed and the CPU state returns to the secure state, data will be programmed to an address not intended by the secure user.

To prevent such a things, secure user needs to set not to accept the non-secure exception during the following period.

- Set not to accept the non-secure exeption before setting FWEPROR to 01h or setting FENTRYR to other than 0000h, that is before lereasing the protection of FWEPROR or FENTRYR.
- Set to accept the non-secure exception after all write access to the FACI command-issuing area is completed.

45.6.4 FCU interrupt usage

It is recommended that secure users do not use the FCU interrupts, but rather use the register polling. Because non-secure users can program/erase the data flash without calling the secure gateway, if secure user uses FCU interrupts, the unintentional exception handliing may be exeuted when data flash is programmed/erased by a non-secure user.

45.6.1 设置安全属性的限制

要设置软件断点，调试器需要重新编程闪存。表45.10显示了调试器为重新编程闪存而设置的寄存器。如果表45.10中列出的寄存器的安全属性配置为安全，则调试器无法在NSECSD状态下设置软件断点，因为调试器无法更改寄存器设置。仅在NSECSD状态下，安全开发人员需要将表45.10中列出的寄存器配置为非安全。

Table 45.10 调试器设置的用于重新编程闪存的寄存器

函数名称	注册名称
时钟产生电路	SCKDIVCR, SCKCR, PLLCCR, PLLCR, HOCOCR, MOCOCR
Low-Power modes	OPCCR

45.6.2 SAU设置

复位后，SAU默认设置将所有地址空间标记为安全。SAU_CTRL寄存器应设置为0x2以启用IDAU安全属性。即设置SAU_CTRL寄存器为0x2后，地址空间安全属性变为如表45.6所示。

45.6.3 FACI寄存器设置期间的非安全异常

如表45.5所示，与FACI相关的寄存器仅在编程擦除或挂起编程擦除期间受到保护，不会受到非安全访问。在此状态之外，来自非安全区域的访问不受保护。例如，当由安全用户编程时，如果在图43.13中的“将目标块的起始地址设置为FSADDR寄存器”流程之后立即发生非安全异常，则非安全用户可以重写FSADDR。如果在非安全异常处理完成后发出FACI命令并且CPU状态返回到安全状态，则数据将被编程到安全用户不打算使用的地址。

为了防止这样的事情发生，安全用户需要在接下来的时间段内设置不接受非安全异常。

- ●在将FWEPROR设置为01h或将FENTRYR设置为0000h以外的值之前，即在解除对FWEPROR或FENTRYR的保护之前，设置不接受非安全例外。
- ●设置为在对FACI命令发布区域的所有写访问完成后接受非安全异常。

45.6.4 FCU中断使用

建议安全用户不要使用FCU中断，而是使用寄存器轮询。由于非安全用户可以在不调用安全网关的情况下对数据闪存进行编程擦除，因此如果安全用户使用FCU中断，则在数据闪存被非安全用户编程擦除时可能会执行意外异常处理。

46. Electrical Characteristics

Unless otherwise specified, minimum and maximum values are guaranteed by either design simulation, characterization results or test in production.

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = AVCC0 = 2.7 to 3.6 V
- 2.7 ≤ VREFH0 ≤ AVCC0
- VSS = AVSS0 = VREFL0 = 0 V
- $T_a = T_{opr}$

Figure 46.1 shows the timing conditions.

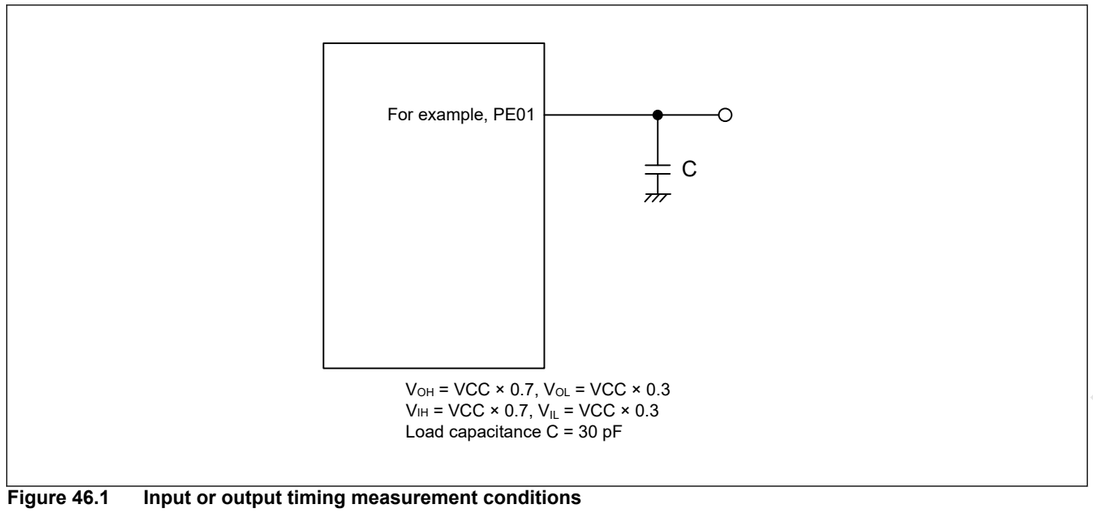


Figure 46.1 Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

46.1 Absolute Maximum Ratings

Table 46.1 Absolute maximum ratings (1 of 2)

Parameter	Symbol	Value	Unit
Power supply voltage	VCC	–0.3 to +4.0	V
Input voltage (except for 5 V-tolerant ports*1)	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (5 V-tolerant ports*1)	V_{in}	–0.3 to + VCC + 4.0 (max. 5.8)	V
Reference power supply voltage	VREFH0	–0.3 to VCC + 0.3	V
Analog power supply voltage	AVCC0*2	–0.3 to +4.0	V
Analog input voltage (except for PA00 to PA05, PB02, P002)	V_{AN}	–0.3 to AVCC0 + 0.3	V
Analog input voltage (PA00 to PA05, PB02, P002) when PGA differential input is disabled	V_{AN}	–0.3 to AVCC0 + 0.3	V
Analog input voltage (PA00, PA02, PA04, PB02) when PGA differential input is enabled	V_{AN}	–1.3 to AVCC0 + 0.3	V
Analog input voltage (PA01, PA03, PA05, P002) when PGA differential input is enabled	V_{AN}	–0.8 to AVCC0 + 0.3	V

46. 电气特性

除非另有说明，否则最小值和最大值由设计模拟、表征结果或生产测试来保证。

支持的外围功能和引脚因产品名称而异。

除非另有规定，MCU的电气特性在以下条件下定义：

- VCC = AVCC0 = 2.7 to 3.6 V
- 2.7 ≤ VREFH0 ≤ AVCC0
- VSS = AVSS0 = VREFL0 = 0 V
- $T_a = T_{opr}$

图46.1显示了时序条件。

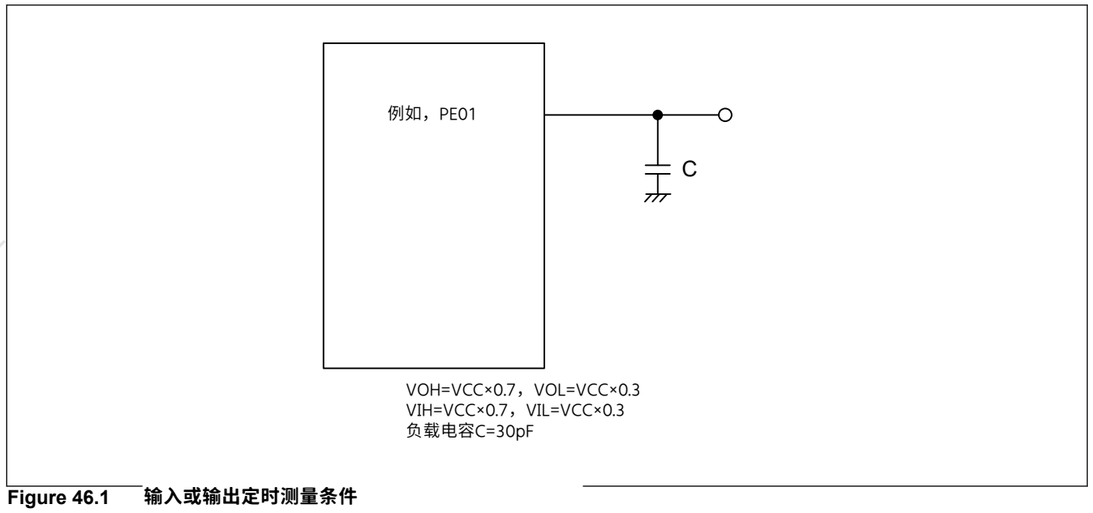


Figure 46.1 输入或输出定时测量条件

所提供的每个外设时序规范的推荐测量条件是为了实现最佳外设操作。确保调整每个引脚的驱动能力以满足您的条件。

46.1 绝对最大额定值

Table 46.1 绝对最大额定值(1of2)

Parameter	Symbol	Value	Unit
电源电压	VCC	–0.3 to +4.0	V
输入电压（5V容限端口*1除外）	V_{in}	–0.3 to VCC + 0.3	V
输入电压（5V耐压端口*1）	V_{in}	–0.3 to + VCC + 4.0 (max. 5.8)	V
参考电源电压	VREFH0	–0.3 to VCC + 0.3	V
模拟电源电压	AVCC0*2	–0.3 to +4.0	V
模拟输入电压（除了PA00到PA05、PB02、P002)	V_{AN}	–0.3 to AVCC0 + 0.3	V
模拟输入电压（PA00至PA05、PB02、P002）时PGA差分输入被禁用	V_{AN}	–0.3 to AVCC0 + 0.3	V
PGA差分输入使能时的模拟输入电压（PA00、PA02、PA04、PB02）	V_{AN}	–1.3 to AVCC0 + 0.3	V
PGA差分输入使能时的模拟输入电压（PA01、PA03、PA05、P002）	V_{AN}	–0.8 to AVCC0 + 0.3	V

Table 46.1 Absolute maximum ratings (2 of 2)

Parameter	Symbol	Value	Unit
Operating temperature*3 *4	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note 1. Ports PA12 to PA15, PB03 to PB09, PC10 to PC12, PC14, PC15, PD00 to PD07, PE00, and PE01 are 5 V tolerant.
Note 2. Connect AVCC0 to VCC.
Note 3. See section 46.2.1. Tj/Ta Definition.
Note 4. Contact a Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Table 46.2 Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltages	VCC	2.7	—	3.6	V
	VSS	—	0	—	V
Analog power supply voltages	AVCC0*1	—	VCC	—	V
	AVSS0	—	0	—	V

Note 1. Connect AVCC0 to VCC. When the A/D converter and the D/A converter are not in use, do not leave the AVCC0, VREFH0, AVSS0, and VREFL0 pins open. Connect the AVCC0 and VREFH0 pins to VCC, and the AVSS0 and VREFL0 pins to VSS, respectively.

46.2 DC Characteristics

46.2.1 Tj/Ta Definition

Table 46.3 DC characteristics

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	T_j	—	125	°C	High-speed mode Low-speed mode

Note: Make sure that $T_j = T_a + \theta ja \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.

Table 46.1 绝对最大额定值(2of2)

Parameter	Symbol	Value	Unit
工作温度*3*4	T_{opr}	–40 to +105	°C
贮存温度	T_{stg}	–55 to +125	°C

注1.端口PA12至PA15、PB03至PB09、PC10至PC12、PC14、PC15、PD00至PD07、PE00和PE01可承受5V。
注2.将AVCC0连接到VCC。
注3：见第46.2.1节。TjTa定义。
注4.有关在Ta=+85°C至+105°C时降额运行的信息，请联系瑞萨电子销售办事处。降额是系统地减少负载以提高可靠性。

Caution: 如果超过绝对最大额定值，可能会对MCU造成永久性损坏。

Table 46.2 推荐工作条件

Parameter	Symbol	Min	Typ	Max	Unit
电源电压	VCC	2.7	—	3.6	V
	VSS	—	0	—	V
模拟电源电压	AVCC0*1	—	VCC	—	V
	AVSS0	—	0	—	V

注1.将AVCC0连接到VCC。不使用AD转换器和DA转换器时，请勿将AVCC0、VREFH0、AVSS0和VREFL0引脚悬空。将AVCC0和VREFH0引脚连接到VCC，将AVSS0和VREFL0引脚分别连接到VSS。

46.2 DC Characteristics

46.2.1 Tj/Ta Definition

Table 46.3 DC characteristics

Parameter	Symbol	Typ	Max	Unit	测试条件
允许结温	T_j	—	125	°C	High-speed mode Low-speed mode

Note: 确保Tj=Ta+θja×总功耗(W)，其中总功耗=(VCCVOH)×ΣIOH+VOL×ΣIOL+ $I_{CC}max \times VCC$.

46.2.2 I/O V_{IH}, V_{IL}

Table 46.4 I/O V_{IH}, V_{IL}

Parameter			Symbol	Min	Typ	Max	Unit
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL (external clock input), SPI (except RSPCK)	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
		IIC (SMBus)*1	V_{IH}	2.1	—	—	
			V_{IL}	—	—	0.8	
		IIC (SMBus)*2	V_{IH}	2.1	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	0.8	
Schmitt trigger input voltage	Peripheral function pin	IIC (Except for SMBus)*1	V_{IH}	VCC × 0.7	—	—	
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.05	—	—	
		IIC (Except for SMBus)*2	V_{IH}	VCC × 0.7	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.05	—	—	
		5 V-tolerant ports*3 *7	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
		Other input pins*4	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
	Ports	5 V-tolerant ports*5 *7	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
		Other input pins*6	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	

Note 1. SCL0_C, SDA0_C, SCL0_D, SDA0_D, SCL0_E, SDA0_E, SCL0_F, SDA0_F, SCL1_C, SDA1_C, SCL1_D, SDA1_D, SCL1_E, SDA1_E (total 14 pins). This is the value when IIC function is selected.
Note 2. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL1_A, SDA1_A, SCL1_B, SDA1_B (total 8 pins). This is the value when IIC function is selected.
Note 3. RES and peripheral function pins associated with PA12 to PA15, PB03, PB05 to PB09, PC10 to PC12, PC14, PC15, PD00 to PD07, PE00, and PE01 (total 26 pins).
Note 4. All input pins except for the peripheral function pins already described in the table.
Note 5. PA12 to PA15, PB03, PB05 to PB09, PC10 to PC12, PC14, PC15, PD00 to PD07, PE00, and PE01 (total 25 pins).
Note 6. All input pins except for the ports already described in the table.
Note 7. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

46.2.2 IOVIH

Table 46.4 IOVIH

Parameter			象征	Min	Typ	Max	Unit
输入电压（施密特触发器输入引脚除外）	外设功能引脚	EXTAL（外部时钟输入）、SPI（除RSPCK)	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
		IIC (SMBus)*1	V_{IH}	2.1	—	—	
			V_{IL}	—	—	0.8	
		IIC (SMBus)*2	V_{IH}	2.1	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	0.8	
施密特触发器输入电压	外设功能引脚	IIC (Except for SMBus)*1	V_{IH}	VCC × 0.7	—	—	
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.05	—	—	
		IIC (Except for SMBus)*2	V_{IH}	VCC × 0.7	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.05	—	—	
		5 V-tolerant ports*3 *7	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
		其他输入引脚*4	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
	Ports	5 V-tolerant ports*5 *7	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
		其他输入引脚*6	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	

Note 1. SCL0_C, SDA0_C, SCL0_D, SDA0_D, SCL0_E, SDA0_E, SCL0_F, SDA0_F, SCL1_C, SDA1_C, SCL1_D, SDA1_D, SCL1_E, SDA1_E（共14个引脚）。这是选择IIC功能时的值。
注2.SCL0_A、SDA0_A、SCL0_B、SDA0_B、SCL1_A、SDA1_A、SCL1_B、SDA1_B（共8个引脚）。这是选择IIC功能时的值。

注3.与PA12至PA15、PB03、PB05至PB09、PC10至PC12、PC14、PC15、PD00至PD07相关的RES和外围功能引脚，
PE00, and PE01 (total 26 pins).
注4.除表中已描述的外围功能引脚外的所有输入引脚。
注5.PA12～PA15、PB03、PB05～PB09、PC10～PC12、PC14、PC15、PD00～PD07、PE00、PE01（共25个引脚）。
注6.除表中已描述的端口外的所有输入引脚。
注7.当VCC小于2.7V时，5V容限端口的输入电压应小于3.6V，否则可能发生击穿，因为5V容限端口是电气控制的，以免违反击穿电压。

46.2.3 I/O I_{OH}, I_{OL}

Table 46.5 I/O I_{OH}, I_{OL}

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	IIC pins	Standard mode*1	I_{OL}	—	—	3.0	mA
		Fast mode*1	I_{OL}	—	—	6.0	mA
		Fast mode plus*2	I_{OL}	—	—	20	mA
		High speed mode*2	I_{OL}	—	—	3.0	mA
	Other output pins*3	Low drive*4	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*5	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*6	I_{OH}	—	—	–10	mA
			I_{OL}	—	—	10	mA
		High speed high drive*7	I_{OH}	—	—	–10	mA
			I_{OL}	—	—	10	mA
		High current drive*8	I_{OH}	—	—	–10	mA
			I_{OL}	—	—	20	mA
Permissible output current (max value per pin)	IIC pins	Standard mode*1	I_{OL}	—	—	3.0	mA
		Fast mode*1	I_{OL}	—	—	6.0	mA
		Fast mode plus*2	I_{OL}	—	—	20	mA
		High speed mode*2	I_{OL}	—	—	3.0	mA
	Other output pins*3	Low drive*4	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*5	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*6	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
		High speed high drive*7	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
		High current drive*8	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	20	mA
Permissible output current (max value of total of all pins)	Maximum of all output pins		ΣI_{OH} (max)	—	—	–80	mA
			ΣI_{OL} (max)	—	—	80	mA

Note 1. SCL0_A, SDA0_A, SCL1_A, SDA1_A (total 4 pins). This is the value when IIC function is selected.
Note 2. SCL0_A, SDA0_A (total 2 pins). This is the value when IIC function is selected.
Note 3. Except for P000 to P002, PA00 to PA07, PB00 to PB02, PC00 to PC05, PC13, which are input ports.
Note 4. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 5. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 6. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

46.2.3 我爱我哦

Table 46.5 我爱我哦

Parameter			Symbol	Min	Typ	Max	Unit
允许输出电流（每个引脚的平均值）	IIC pins	标准模式*1	I_{OL}	—	—	3.0	mA
		快速模式*1	I_{OL}	—	—	6.0	mA
		快速模式加*2	I_{OL}	—	—	20	mA
		高速模式*2	I_{OL}	—	—	3.0	mA
	其他输出引脚*3	低驱动*4	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		中间驱动器*5	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		高速驱动*6	I_{OH}	—	—	–10	mA
			I_{OL}	—	—	10	mA
		高速高速*7	I_{OH}	—	—	–10	mA
			I_{OL}	—	—	10	mA
		大电流驱动*8	I_{OH}	—	—	–10	mA
			I_{OL}	—	—	20	mA
允许输出电流（每个引脚的最大值）	IIC pins	标准模式*1	I_{OL}	—	—	3.0	mA
		快速模式*1	I_{OL}	—	—	6.0	mA
		快速模式加*2	I_{OL}	—	—	20	mA
		高速模式*2	I_{OL}	—	—	3.0	mA
	其他输出引脚*3	低驱动*4	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		中间驱动器*5	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		高速驱动*6	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
		高速高速*7	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
		大电流驱动*8	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	20	mA
允许输出电流（所有引脚总和的最大值）	所有输出引脚的最大值		ΣI_{OH} (max)	—	—	–80	mA
			ΣI_{OL} (max)	—	—	80	mA

注1.SCL0_A、SDA0_A、SCL1_A、SDA1_A（共4个引脚）。这是选择IIC功能时的值。
注2.SCL0_A、SDA0_A（共2个引脚）。这是选择IIC功能时的值。
注3.P000～P002、PA00～PA07、PB00～PB02、PC00～PC05、PC13为输入端口除外。
注4.这是在PmnPFS寄存器的端口驱动能力位中选择低驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

注5.这是在PmnPFS寄存器的端口驱动能力位中选择中等驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

注6.这是在PmnPFS寄存器的端口驱动能力位中选择高驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

Note 7. This is the value when high speed high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 8. This is the value when high current driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

46.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 46.6 I/O V_{OH}, V_{OL}, and other characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1	V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA
		V_{OL}	—	—	0.6		I_{OL} = 6.0 mA
	IIC*2	V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (BFCTL.FMPE = 1)
		V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (BFCTL.FMPE = 1)
		V_{OL}	—	—	0.4		I_{OL} = 3.0 mA (BFCTL.HSME = 1)
	Ports PA08 to PA11, PB12 to PB15, PC06 to PC09, PD08 to PD15, PE10 to PE15*3	V_{OH}	VCC – 0.5	—	—		I_{OH} = –1.0 mA
		V_{OL}	—	—	0.6		I_{OL} = 20 mA
	Other output pins	V_{OH}	VCC – 0.5	—	—		I_{OH} = –1.0 mA
		V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
Input leakage current	RES	$\|I_{in}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Port P000, P001, PA06, PA07, PB00, PB01, PC00 to PC05, PC13		—	—	1.0		V_{in} = 0 V V_{in} = VCC
	Port PA00, PA02, PA04, PB02 (PGA input pins)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
	Port PA01, PA03, PA05, P002 (PGAVSS pins)*4		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5 V-tolerant ports	$\|I_{TSI}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for input ports)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up MOS current	Ports P0, P2, PA to PE (except for ports P002, PA00 to PA05, PB02)	I_p	–300	—	–10	µA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Pull-up current serving as the SCL current source	IIC*5	I_{CS}	3	—	12	mA	VCC = 3.0 to 3.6 V V_{in} = 0.3 × VCC to 0.7 × VCC
Input capacitance	All input pins	C_{in}	—	—	8	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz Ta = 25°C

Note 1. SCL0_A, SDA0_A, SCL1_A, SDA1_A (total 4 pins). This is the value when IIC function is selected.
Note 2. SCL0_A, SDA0_A (total 2 pins). This is the value when IIC function is selected.
Note 3. This is the value when high current driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. This is the value when the pseudo-differential input on the PGAn pin is disabled (single-ended input).
Note 5. SCL0_A (1 pin). This is the value when IIC high speed mode is selected.

注7.这是在PmnPFS寄存器的端口驱动能力位中选择高速高速驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

注8.这是在PmnPFS寄存器的端口驱动能力位中选择高电流驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

Caution: 为保护单片机的可靠性，输出电流值不应超过此表中的值。平均输出电流表示在100µs期间测量的电流平均值。

46.2.4 IOVOH VOL和其他特性

Table 46.6 IOVOH、VOL和其他特性

Parameter		符号	最小值	典型	最大	单位	测试条件
输出电压	IIC*1	V_{OL}	—	—	0.4	V	我OL=3.0毫安
		V_{OL}	—	—	0.6		我OL=6.0毫安
	IIC*2	V_{OL}	—	—	0.4		IOL=15.0mA(BFCTL.FMPE=1)
		V_{OL}	—	0.4	—		IOL=20.0mA(BFCTL.FMPE=1)
		V_{OL}	—	—	0.4		IOL=3.0mA(BFCTL.HSME=1)
	端口PA08至PA11、PB12至PB15、PC06 to PC09, PD08 to PD15, PE10 to PE15*3	V_{OH}	VCC – 0.5	—	—		IOH= 1.0毫安
		V_{OL}	—	—	0.6		我OL=20毫安
	其他输出引脚	V_{OH}	VCC – 0.5	—	—		IOH= 1.0毫安
		V_{OL}	—	—	0.5		我OL=1.0毫安
输入漏电流	RES	$\|I_{in}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Port P000, P001, PA06, PA07, PB00, PB01, PC00 to PC05, PC13		—	—	1.0		V_{in} = 0 V V_{in} = VCC
	端口PA00、PA02、PA04、PB02（PGA输入引脚）		—	—	1.0		V_{in} = 0 V V_{in} = VCC
	Port PA01, PA03, PA05, P002 (PGAVSS pins)*4		—	—	1.0		V_{in} = 0 V V_{in} = VCC
三态漏电流（关闭状态）	5 V-tolerant ports	$\|I_{TSI}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	其他端口（输入端口除外）		—	—	1.0		V_{in} = 0 V V_{in} = VCC
输入上拉MOS电流	端口P0、P2、PA到PE（端口除外P002, PA00 to PA05, PB02)	I_p	–300	—	–10	µA	VCC = 2.7 to 3.6 V V_{in} = 0 V
上拉电流作为SCL电流源	IIC*5	I_{CS}	3	—	12	mA	VCC = 3.0 to 3.6 V Vin=0.3×VCC至0.7×VCC
输入电容	所有输入引脚	C_{in}	—	—	8	pF	Vbias = 0 V Vamp=20mVf=1MHzTa=25°C

注1.SCL0_A、SDA0_A、SCL1_A、SDA1_A（共4个引脚）。这是选择IIC功能时的值。
注2.SCL0_A、SDA0_A（共2个引脚）。这是选择IIC功能时的值。
注3.这是在PmnPFS寄存器的端口驱动能力位中选择高电流驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

注4.这是禁用PGAn引脚上的伪差分输入（单端输入）时的值。
注5.SCL0_A（1个引脚）。这是选择IIC高速模式时的值。

46.2.5 Operating and Standby Current

Table 46.7 Operating and standby current

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Supply current*1	High-speed mode	Maximum*2		I_{CC}*3	—	—	150	mA	ICLK = 240 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz
		CoreMark®*5 *6			—	34	—		
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash*4		—	44	—		
			All peripheral clocks disabled, while (1) code executing from flash*5 *6		—	28	—		
		Sleep mode*5 *6			—	13	78		
		Increase during BGO operation	Data flash P/E		—	6	—		
			Code flash P/E		—	8	—		
	Low-speed mode*5 *10				—	5	—		ICLK = 1 MHz
	Software Standby mode		SNZCR.RXDREQEN = 1		—	—	63		ICLK = 32.768 kHz
			SNZCR.RXDREQEN = 0		—	5.1	—		—
	Deep Software Standby mode	Power supplied to Standby SRAM			—	22.7	60	μA	—
		Power not supplied to SRAM	Power-on reset circuit low power function disabled		—	11.3	30		—
			Power-on reset circuit low power function enabled		—	4.4	20		—
	Inrush current on returning from deep software standby mode		Inrush current*7	I_{RUSH}	—	160	—	mA	
			Energy of inrush current*7	E_{RUSH}	—	1.0	—	μC	
Analog power supply current	During ADC conversion (1unit)		Without SH	AI_{CC}	—	4.8	6.0	mA	
			With SH		—	7.3	11.5	mA	
	PGA (1channel)				—	1	3	mA	
	ACMPHS (1unit)				—	0.1	0.2	mA	
	Temperature sensor				—	0.1	0.2	mA	
	During D/A conversion (1channel)*8		Without AMP output		—	0.2	0.3	mA	
			With AMP output		—	0.8	1.3	mA	
	Waiting for ADC, DAC12 conversion (all units)				—	3.8	4.5	mA	
	ADC, DAC12 in standby modes (all units)*9				—	0.7	10	μA	
Reference power supply current (VREFH0)	During ADC conversion (1unit)			AI_{REFH0}	—	21	50	μA	
	Waiting for ADC, DAC12 conversion (all units)				—	18	50	μA	
	ADC, DAC12 in standby modes (all units)*9				—	0.03	1	μA	

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows.
I_{CC} Max. = 0.34 × f + 67 (max. operation in high-speed mode)
I_{CC} Typ. = 0.095 × f + 4.7 (normal operation in high-speed mode, all peripheral clocks disabled)
I_{CC} Typ. = 0.9 × f + 4.1 (low-speed mode)
I_{CC} Max. = 0.045 × f + 67 (sleep mode)
Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.75 MHz).
Note 7. Reference value
Note 8. The DAC12 includes the Reference current in the analog power supply current.

46.2.5 工作和待机电流

Table 46.7 工作和待机电流

Parameter				符号	最小值	典型值	最大	单元	测试条件
供电电流*1	High-speed mode	Maximum*2		I_{CC}*3	—	—	150	mA	ICLK = 240 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz
		CoreMark®*5 *6			—	34	—		
		正常模式	启用所有外设时钟，同时(1) 代码从闪存执行*4		—	44	—		
			禁用所有外设时钟，同时(1) 代码从闪存执行*5*6		—	28	—		
		睡眠模式*5*6			—	13	78		
		BGO运行期间增加	数据闪存PE		—	6	—		
			代码闪存PE		—	8	—		
	Low-speed mode*5 *10				—	5	—		ICLK = 1 MHz
	软件待机模式		SNZCR.RXDREQEN = 1		—	—	63		ICLK = 32.768 kHz
			SNZCR.RXDREQEN = 0		—	5.1	—		—
	Deep Software 待机模式	为备用SRAM供电			—	22.7	60	μA	—
		未向SRAM供电	上电复位电路低功耗功能禁用		—	11.3	30		—
			上电复位电路低功耗功能启用		—	4.4	20		—
	从深度软件待机模式返回时的浪涌电流		Inrush current*7	I_{RUSH}	—	160	—	mA	
			浪涌电流能量*7	E_{RUSH}	—	1.0	—	μC	
模拟电源电流	ADC转换期间（1个单位）		Without SH	AI_{CC}	—	4.8	6.0	mA	
			With SH		—	7.3	11.5	mA	
	PGA (1channel)				—	1	3	mA	
	ACMPHS (1unit)				—	0.1	0.2	mA	
	温度感应器				—	0.1	0.2	mA	
	DA转换期间（1通道）*8		无AMP输出		—	0.2	0.3	mA	
			带AMP输出		—	0.8	1.3	mA	
	等待ADC、DAC12转换（所有单元）				—	3.8	4.5	mA	
	待机模式下的ADC、DAC12（所有单元）*9				—	0.7	10	μA	
参考电源电流(VREFH0)	ADC转换期间（1个单位）			AI_{REFH0}	—	21	50	μA	
	等待ADC、DAC12转换（所有单元）				—	18	50	μA	
	待机模式下的ADC、DAC12（所有单元）*9				—	0.03	1	μA	

注1.电源电流值是在所有输出引脚空载且所有输入上拉MOS处于关闭状态时的值。
注2.使用提供给外设功能的时钟测量。这不包括BGO操作。
注3.ICC取决于f(ICLK)，如下所示。
我CC最大。=0.34×f+67（高速模式下的最大操作）
我CC典型。=0.095×f+4.7（高速模式下正常运行，所有外设时钟禁用）
I_{CC} Typ. = 0.9 × f + 4.1 (low-speed mode)
I_{CC} Max. = 0.045 × f + 67 (sleep mode)
注4.这不包括BGO操作。
注5.在此状态下停止向外围设备提供时钟信号。这不包括BGO操作。
注6.FCLK、PCLKA、PCLKB、PCLKC和PCLKD设置为64分频（3.75MHz）。
注7.参考值
注8.DAC12在模拟电源电流中包含参考电流。

Note 9. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-Bit A/D Converter Module Stop bit) is in the module-stop state.
Note 10. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (15.6 kHz).

Table 46.8 Coremark and normal mode current

Parameter			Symbol	Typ	Unit	Test conditions
Supply Current*1	Coremark		I_{CC}	139	µA/MHz	ICLK = 240 MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 3.75 MHz
	Normal mode	All peripheral clocks disabled, cache on, while (1) code executing from flash*2		139		
		All peripheral clocks disabled, cache off, while (1) code executing from flash*2		115		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

46.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 46.9 Rise and fall gradient characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	—	20	ms/V	—
	Voltage monitor 0 reset enabled at startup		0.0084	—	—		—
	SCI boot mode*1		0.0084	—	20		—
VCC falling gradient		SfVCC	0.0084	—	—	ms/V	—

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Table 46.10 Rising and falling gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	—	—	10	kHz	Figure 46.2 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 46.2 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 46.2 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

注9.当MCU处于软件待机模式或MSTPCRD.MSTPD16（12位AD转换器模块停止位）处于模块停止状态时。

注10.FCLK、PCLKA、PCLKB、PCLKC和PCLKD设置为64分频（15.6kHz）。

Table 46.8 Coremark和正常模式电流

Parameter			Symbol	Typ	Unit	测试条件
电源电流*1	Coremark		I_{CC}	139	µA/MHz	ICLK = 240 MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 3.75 MHz
	正常模式	禁用所有外设时钟，开启缓存，同时(1)从闪存执行代码*2		139		
		所有外设时钟禁用，缓存关闭，同时(1)代码从闪存执行*2		115		

注1.电源电流值是在所有输出引脚空载且所有输入上拉MOS处于关闭状态时的值。
注2.在此状态下停止向外围设备提供时钟信号。这不包括BGO操作。

46.2.6 VCC上升和下降梯度和纹波频率

Table 46.9 上升和下降梯度特性

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
VCC上升梯度	启动时禁用电压监视器0复位	SrVCC	0.0084	—	20	ms/V	—
	启动时启用电压监视器0复位		0.0084	—	—		—
	SCI开机模式*1		0.0084	—	20		—
VCC下降梯度		SfVCC	0.0084	—	—	ms/V	—

注1.在引导模式下，无论OFS1.LVDAS位的值如何，都禁止从电压监视器0进行的复位。

Table 46.10 上升下降梯度和纹波频率特性

纹波电压必须在VCC上限(3.6V)和下限(2.7
五）。当VCC变化超过VCC±10%时，必须满足允许的电压变化上升和下降梯度dtdVCC。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
允许纹波频率	$f_{r\ (VCC)}$	—	—	10	kHz	Figure 46.2 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 46.2 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 46.2 $V_{r\ (VCC)} \leq VCC \times 0.06$
允许电压变化上升下降梯度	dt/dVCC	1.0	—	—	ms/V	当VCC变化超过VCC ±10%

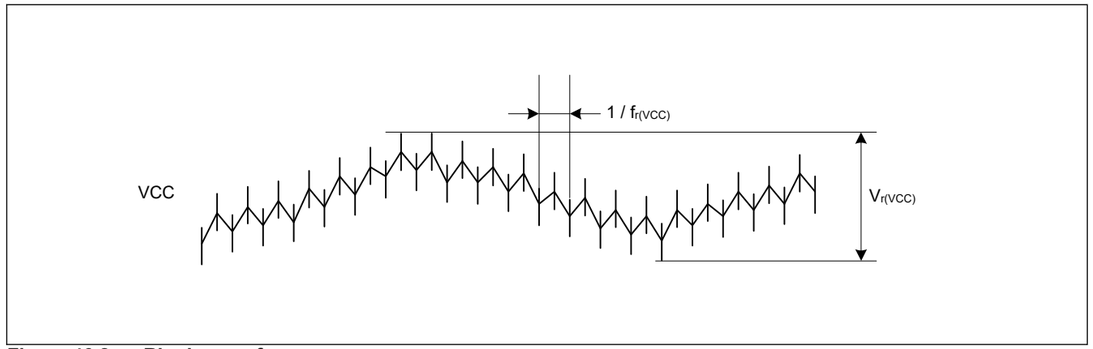


Figure 46.2 Ripple waveform

46.2.7 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of section 46.2.1. Tj/Ta Definition.

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption
  - Tj : Junction Temperature (°C)
  - Ta : Ambient Temperature (°C)
  - Tt : Top Center Case Temperature (°C)
  - θja : Thermal Resistance of "Junction"-to-"Ambient" (°C/W)
  - Ψjt : Thermal Resistance of "Junction"-to-"Top Center Case" (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (I_{OL} × V_{OL}) /Voltage + Σ (|I_{OH}| × |VCC – V_{OH}|) /Voltage
- Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
  - C_{in}: Input capacitance
  - C_{load}: Output capacitance

Regarding θja and Ψjt, refer to Table 46.11.

Table 46.11 Thermal Resistance

Parameter	Package	Symbol	Value*1	Unit	Test conditions
Thermal Resistance	100-pin LQFP (PLQP0100KB-B)	θja	36	°C/W	JESD 51-2 and 51-7 compliant
	64-pin LQFP (PLQP0064KB-C)		39		
	64-pin QFN (PWQN0064LA-A)		26		
	48-pin LQFP (PLQP0048KB-B)		60		
	48-pin QFN (PWQN0048KB-A)		28		
	100-pin LQFP (PLQP0100KB-B)	Ψjt	0.65	°C/W	JESD 51-2 and 51-7 compliant
	64-pin LQFP (PLQP0064KB-C)		0.69		
	64-pin QFN (PWQN0064LA-A)		0.15		
	48-pin LQFP (PLQP0048KB-B)		2.01		
	48-pin QFN (PWQN0048KB-A)		0.17		

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

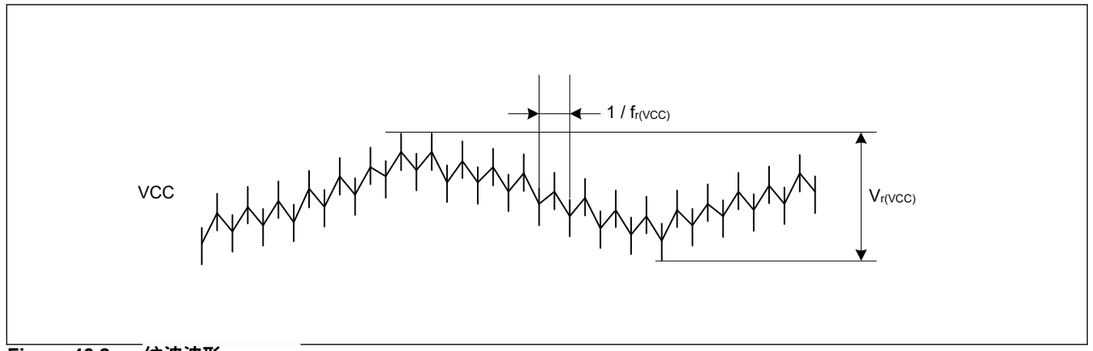


Figure 46.2 纹波波形

46.2.7 热特性

结温最大值(Tj)不得超过第46.2.1节的值。TjTa定义。

Tj通过以下任一公式计算。

●Tj=Ta+θja×总功耗

●Tj=Tt+Ψjt×总功耗

Tj：结温(°C)

Ta：环境温度 (°C)

Tt：顶部中心外壳温度(°C)

θja："结"到"环境"的热阻(°CW)

Ψjt："结"到"顶部中心外壳"的热阻(°CW)

●总功耗=电压×（漏电流+动态电流）

●IO漏电流=Σ(IOL×VOL)电压+Σ(IOH×VCC VOH)电压

●IO的动态电流=ΣIO(Cin+Cload)×IO开关频率×电压

Cin:输入电容

C负载：输出电容

关于θja和Ψjt，请参阅表46.11。

Table 46.11 热阻

Parameter	Package	Symbol	Value*1	Unit	测试条件
热阻	100-pin LQFP (PLQP0100KB-B)	θja	36	°C/W	符合JESD51-2和51-7
	64-pin LQFP (PLQP0064KB-C)		39		
	64-pin QFN (PWQN0064LA-A)		26		
	48-pin LQFP (PLQP0048KB-B)		60		
	48-pin QFN (PWQN0048KB-A)		28		
	100-pin LQFP (PLQP0100KB-B)	Ψjt	0.65	°C/W	符合JESD51-2和51-7
	64-pin LQFP (PLQP0064KB-C)		0.69		
	64-pin QFN (PWQN0064LA-A)		0.15		
	48-pin LQFP (PLQP0048KB-B)		2.01		
	48-pin QFN (PWQN0048KB-A)		0.17		

注1.数值为使用4层板时的参考值。热阻取决于板的层数或尺寸。有关详细信息，请参阅JEDEC标准。

46.2.7.1 Calculation guide of ICCmax

Table 46.12 shows the power consumption of each unit.

Table 46.12 Power consumption of each unit

Dynamic current/Leakage current	MCU Domain	Category	Item	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]
Leakage current	Analog	LDO and Leak*2	Ta = 75 °C*3	—	—	37.8
			Ta = 85 °C*3	—	—	46.4
			Ta = 95 °C*3	—	—	56.1
			Ta = 105 °C*3	—	—	68.0
Dynamic current	CPU	Operation with Flash and SRAM	Coremark	240	105.324	25.28
	Peripheral Unit	Timer	GPT32 (10ch)*4	120	29.697	3.56
			POEG (4 Groups)*4	60	1.483	0.09
			AGT (2ch)*4	60	3.09	0.19
			WDT	60	0.641	0.04
			IWDT	60	0.225	0.01
		Communication interfaces	SCI (6ch)*4	120	27.683	3.32
			IIC (2ch)*4	120	5.304	0.64
			CANFD	60	5.763	0.35
			SPI (2ch)*4	120	5.738	0.69
		Data processing accelerator	TFU	240	1.188	0.03
			IIRFA	240	34.252	8.22
		Data processing	DOC	120	0.221	0.03
			CRC	120	0.508	0.06
		Analog	ADC (2 Units)*4	60	172.958	10.38
			DAC12 (4ch)*4	120	1.097	0.13
			ACMPHS (4ch)*4	60	0.641	0.04
			TSN	60	0.111	0.01
		Event link	ELC	60	1.852	0.11
		Security	SCE5	120	68.404	8.21
		System	CAC	60	0.63	0.04
			KINT	60	0.072	0.004
		DMA	DMAC	240	5.073	1.22
			DTC	240	4.18	1

Note 1. The values are guaranteed by design.
Note 2. LDO and Leak are internal voltage regulator's current and MCU's leakage current.
It is selected according to the temperature of Ta.
Note 3. Δ(Tj-Ta) = 20 °C is considered to measure the current.
Note 4. To determine the current consumption per channel or unit, divide Current [mA] by the number of channels, groups or units.

Table 46.13 Outline of operation for each unit (1 of 2)

Peripheral	Outline of operation
GPT	Operating modes is set to saw-wave PWM mode. GPT is operating with PCLKD.

46.2.7.1 ICCmax的计算指南

表46.12显示了每个单元的功耗。

Table 46.12 各单元耗电量

动态电流漏电流	MCU Domain	Category	Item	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]
漏电流	Analog	LDO和泄漏*2	Ta = 75 °C*3	—	—	37.8
			Ta = 85 °C*3	—	—	46.4
			Ta = 95 °C*3	—	—	56.1
			Ta = 105 °C*3	—	—	68.0
动态电流	CPU	操作与闪存和SRAM	Coremark	240	105.324	25.28
	外围单元	Timer	GPT32 (10ch)*4	120	29.697	3.56
			POEG (4 Groups)*4	60	1.483	0.09
			AGT (2ch)*4	60	3.09	0.19
			WDT	60	0.641	0.04
			IWDT	60	0.225	0.01
		通讯接口	SCI (6ch)*4	120	27.683	3.32
			IIC (2ch)*4	120	5.304	0.64
			CANFD	60	5.763	0.35
			SPI (2ch)*4	120	5.738	0.69
		数据处理加速器	TFU	240	1.188	0.03
			IIRFA	240	34.252	8.22
		数据处理	DOC	120	0.221	0.03
			CRC	120	0.508	0.06
		Analog	ADC (2 Units)*4	60	172.958	10.38
			DAC12 (4ch)*4	120	1.097	0.13
			ACMPHS (4ch)*4	60	0.641	0.04
			TSN	60	0.111	0.01
		活动链接	ELC	60	1.852	0.11
		Security	SCE5	120	68.404	8.21
		System	CAC	60	0.63	0.04
			KINT	60	0.072	0.004
		DMA	DMAC	240	5.073	1.22
			DTC	240	4.18	1

注1.数值由设计保证。
注2.LDO和Leak是内部稳压器的电流和MCU的漏电流。
根据Ta的温度选择。
注3.测量电流时考虑Δ(Tj-Ta)=20°C。
注4.要确定每个通道或单元的电流消耗，请将电流[mA]除以通道 、组或单元的数量。

Table 46.13 每个单元的操作概要（2个中的1个）

Peripheral	操作概要
GPT	操作模式设置为锯齿波PWM模式。 GPT使用PCLKD运行。

Table 46.13 Outline of operation for each unit (2 of 2)

Peripheral	Outline of operation
POEG	Only clear module stop bit.
AGT	AGT is operating with PCLKB.
WDT	WDT is operating with PCLKB.
IWDT	IWDT is operating with IWDTCLK.
SCI	SCI is transmitting data in clock synchronous mode.
IIC	Communication format is set to I2C-bus format. IIC is transmitting data in master mode.
CANFD	CANFD is transmitting and receiving data in self-test mode 1.
SPI	SPI mode is set to SPI operation (4-wire method). SPI master/slave mode is set to master mode. SPI is transmitting 8-bit width data.
TFU	Performs sincos operations.
IIRFA	Channel 0 perfoms 32 stages of channel processing.
DOC	DOC is operating in data addition mode.
CRC	CRC is generating CRC code using 32-bit CRC32-C polynomial.
ADC	Resolution is set to 12-bit accuracy. Conversion Data Operation Control B Register is set to 16 times average mode. ADC is converting the analog input in continuous scan mode. ADC is operating with PCLKC.
DAC12	DAC12 is outputting the conversion result while updating the value of data register.
ACMPHS	Compare between IVCMP2 and IVREF0 and enable compare output.
TSN	TSN is operating.
ELC	Only clear module stop bit.
SCE5	SCE5 is executing built-in self test.
DMAC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DMAC is transferring data from SRAM0 to SRAM0.
DTC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DTC is transferring data from SRAM0 to SRAM0.
CAC	Measurement target clocks is set to PCLKB. Measurement reference clocks is set to PCLKB. CAC is measuring the clock frequency accuracy.
KINT	Only clear module stop bit.

46.2.7.2 Example of Tj calculation

Assumption:

- Package 100-pin LQFP: θja = 36.0 °C/W
- Ta = 100 °C
- I_{CC}max = 80 mA
- VCC = 3.5 V (VCC = AVCC0)
- I_{OH} = 1 mA, V_{OH} = VCC – 0.5 V, 12 Outputs
- I_{OL} = 20 mA, V_{OL} = 1.0 V, 8 Outputs
- I_{OL} = 1 mA, V_{OL} = 0.5 V, 12 Outputs
- C_{in} = 8 pF, 16 pins, Input frequency = 10 MHz

Table 46.13 每个单元的操作概要（2个中的2个）

Peripheral	操作概要
POEG	只清除模块停止位。
AGT	AGT使用PCLKB运行。
WDT	WDT使用PCLKB运行。
IWDT	IWDT使用IWDTCLK运行。
SCI	SCI在时钟同步模式下传输数据。
IIC	通信格式设置为I2C总线格式。 IIC在主机模式下传输数据。
CANFD	CANFD在自检模式1下发送和接收数据。
SPI	SPI模式设置为SPI操作（4线方法）。 SPI主从模式设置为主模式。 SPI正在传输8位宽度的数据。
TFU	执行sincos操作。
IIRFA	通道0执行32个通道处理阶段。
DOC	DOC在数据添加模式下运行。
CRC	CRC使用32位CRC32-C多项式生成CRC码。
ADC	分辨率设置为12位精度。 转换数据操作控制B寄存器设置为16次平均模式。 ADC在连续扫描模式下转换模拟输入。 ADC使用PCLKC运行。
DAC12	DAC12在更新数据寄存器值的同时输出转换结果。
ACMPHS	比较IVCMP2和IVREF0并启用比较输出。
TSN	TSN正在运行。
ELC	只清除模块停止位。
SCE5	SCE5正在执行内置自检。
DMAC	传输数据的位长设置为32位。 传输模式设置为块传输模式。 DMAC正在将数据从SRAM0传输到SRAM0。
DTC	传输数据的位长设置为32位。 传输模式设置为块传输模式。 DTC正在将数据从SRAM0传输到SRAM0。
CAC	测量目标时钟设置为PCLKB。 测量参考时钟设置为PCLKB。CAC正在测量时钟 频率精度。
KINT	只清除模块停止位。

46.2.7.2 Tj计算示例

Assumption:

- Package 100-pin LQFP: θja = 36.0 °C/W
- Ta = 100 °C

●ICC最大值=80mA

- VCC = 3.5 V (VCC = AVCC0)

●IOH=1mA，VOH=VCC 0.5V，12个输出

●IOL=20mA，VOL=1.0V，8个输出

●IOL=1mA，VOL=0.5V，12路输出

●Cin=8pF，16个引脚，输入频率=10MHz

- C_{load} = 30 pF, 16 pins, Output frequency = 10 MHz

Leakage current of IO = Σ (V_{OL} × I_{OL}) / Voltage + Σ ((VCC - V_{OH}) × I_{OH}) / Voltage
= (20 mA × 1 V) × 8 / 3.5 V + (1 mA × 0.5 V) × 12 / 3.5 V + ((VCC - (VCC - 0.5 V)) × 1 mA) × 12 / 3.5 V
= 45.7 mA + 1.71 mA + 1.71 mA
= 49.1 mA

Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
= ((8 pF × 16) × 10 MHz + (30 pF × 16) × 10 MHz) × 3.5 V
= 21.3 mA

Total power consumption = Voltage × (Leakage current + Dynamic current)
= (80 mA × 3.5 V) + (49.1 mA + 21.3 mA) × 3.5 V
= 526 mW (0.526 W)

Tj = Ta + θja × Total power consumption
= 100 °C + 36.0 °C/W × 0.526W
= 118.9 °C

46.3 AC Characteristics

46.3.1 Frequency

Table 46.14 Operation frequency value in high-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK*2)	f	—	—	240	MHz
	Peripheral module clock (PCLKA)*2		—	—	120	
	Peripheral module clock (PCLKB)*2		—	—	60	
	Peripheral module clock (PCLKC)*2		—*3	—	60	
	Peripheral module clock (PCLKD)*2		—	—	120	
	Flash interface clock (FCLK)*2		—*1	—	60	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. See section 8, Clock Generation Circuit for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK frequencies.
Note 3. When the ADC is used, the PCLKC frequency must be at least 1 MHz.

Table 46.15 Operation frequency value in low-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	—	—	1	MHz
	Peripheral module clock (PCLKA)*2		—	—	1	
	Peripheral module clock (PCLKB)*2		—	—	1	
	Peripheral module clock (PCLKC)*2 *3		—*3	—	1	
	Peripheral module clock (PCLKD)*2		—	—	1	
	Flash interface clock (FCLK)*1 *2		—	—	1	

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.
Note 2. See section 8, Clock Generation Circuit for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK frequencies.
Note 3. When the ADC is used, the PCLKC frequency must be set to at least 1 MHz.

●C负载=30pF，16引脚，输出频率=10MHz

IO漏电流 =Σ(VOL×IOL)电压+Σ((VCCVOH)×IOH)电压
= (20 mA × 1 V) × 8 / 3.5 V + (1 mA × 0.5 V) × 12 / 3.5 V + ((VCC - (VCC - 0.5 V)) × 1 mA) × 12 / 3.5 V
= 45.7 mA + 1.71 mA + 1.71 mA
= 49.1 mA

IO的动态电流 =ΣIO(Cin+Cload)×IO开关频率×电压
= ((8 pF × 16) × 10 MHz + (30 pF × 16) × 10 MHz) × 3.5 V
= 21.3 mA

总功耗 =电压×(漏电流+动态电流)
= (80 mA × 3.5 V) + (49.1 mA + 21.3 mA) × 3.5 V
= 526 mW (0.526 W)

Tj =Ta+θja×总功耗
= 100 °C + 36.0 °C/W × 0.526W
= 118.9 °C

46.3 交流特性

46.3.1 Frequency

Table 46.14 高速模式下的运行频率值

Parameter		Symbol	Min	Typ	Max	Unit
运行频率	系统时钟（ICLK*2）	f	—	—	240	MHz
	外围模块时钟(PCLKA)*2		—	—	120	
	外围模块时钟(PCLKB)*2		—	—	60	
	外围模块时钟(PCLKC)*2		—*3	—	60	
	外围模块时钟(PCLKD)*2		—	—	120	
	闪存接口时钟(FCLK)*2		—*1	—	60	

注1.在对闪存进行编程或擦除时，FCLK必须以至少4MHz的频率运行。
注2.有关ICLK、PCLKA、PCLKB、PCLKC、PCLKD和FCLK频率之间的关系，请参见第8节，时钟生成电路。

注3.使用ADC时，PCLKC频率必须至少为1MHz。

Table 46.15 低速模式下的运行频率值

Parameter		Symbol	Min	Typ	Max	Unit
运行频率	系统时钟(ICLK)*2	f	—	—	1	MHz
	外围模块时钟(PCLKA)*2		—	—	1	
	外围模块时钟(PCLKB)*2		—	—	1	
	外围模块时钟(PCLKC)*2*3		—*3	—	1	
	外围模块时钟(PCLKD)*2		—	—	1	
	Flash接口时钟(FCLK)*1*2		—	—	1	

注1.在低速模式下禁止对闪存进行编程或擦除。
注2.有关ICLK、PCLKA、PCLKB、PCLKC、PCLKD和FCLK频率之间的关系，请参见第8节，时钟生成电路。

注3.使用ADC时，PCLKC频率必须设置为至少1MHz。

46.3.2 Clock Timing

Table 46.16 Clock timing

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 46.3
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rise time	t_{EXr}	—	—	5.0	ns	
EXTAL external clock fall time	t_{EXf}	—	—	5.0	ns	
Main clock oscillator frequency	f_{MAIN}	8	—	24	MHz	—
Main clock oscillation stabilization wait time (crystal)*1	$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 46.4
LOCO clock oscillation frequency	f_{LOCO}	29.4912	32.768	36.0448	kHz	—
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	60.4	µs	Figure 46.5
ILOCO clock oscillation frequency	f_{ILOCO}	13.5	15	16.5	kHz	—
MOCO clock oscillation frequency	F_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization wait time	t_{MOCOWT}	—	—	15.0	µs	—
HOCO clock oscillator oscillation frequency	f_{HOCO16}	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
	f_{HOCO18}	17.75	18	18.25		
	f_{HOCO20}	19.72	20	20.28		
	f_{HOCO16}	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
	f_{HOCO18}	17.68	18	18.32		
	f_{HOCO20}	19.64	20	20.36		
HOCO clock oscillation stabilization wait time*2	t_{HOCOWT}	—	—	64.7	µs	—
HOCO period jitter	—	—	±85	—	ps	—
PLL clock frequency	f_{PLL}	120	—	240	MHz	—
PLL2 clock frequency	f_{PLL2}	120	—	240	MHz	—
PLL/PLL2 clock oscillation stabilization wait time	t_{PLLWT}	—	—	174.9	µs	Figure 46.6
PLL/PLL2 period jitter	—	—	±100	—	ps	—
PLL/PLL2 long term jitter	—	—	±300	—	ps	Term: 1µs, 10µs

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

46.3.2 时钟时序

Table 46.16 时钟计时

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
EXTAL外部时钟输入周期时间	t_{EXcyc}	41.66	—	—	ns	Figure 46.3
EXTAL外部时钟输入高脉冲宽度	t_{EXH}	15.83	—	—	ns	
EXTAL外部时钟输入低脉冲宽度	t_{EXL}	15.83	—	—	ns	
EXTAL外部时钟上升时间	t_{EXr}	—	—	5.0	ns	
EXTAL外部时钟下降时间	t_{EXf}	—	—	5.0	ns	
主时钟振荡器频率	f_{MAIN}	8	—	24	MHz	—
主时钟振荡稳定等待时间（晶体）*1tMANOSCWT—			—	—*1	ms	Figure 46.4
LOCO时钟振荡频率	f_{LOCO}	29.4912	32.768	36.0448	kHz	—
LOCO时钟振荡稳定等待时间	t_{LOCOWT}	—	—	60.4	µs	Figure 46.5
ILOCO时钟振荡频率	f_{ILOCO}	13.5	15	16.5	kHz	—
MOCO时钟振荡频率	F_{MOCO}	6.8	8	9.2	MHz	—
MOCO时钟振荡稳定等待时间	t_{MOCOWT}	—	—	15.0	µs	—
HOCO时钟振荡器振荡频率	f_{HOCO16}	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
	f_{HOCO18}	17.75	18	18.25		
	f_{HOCO20}	19.72	20	20.28		
	f_{HOCO16}	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
	f_{HOCO18}	17.68	18	18.32		
	f_{HOCO20}	19.64	20	20.36		
HOCO时钟振荡稳定等待时间*2	t_{HOCOWT}	—	—	64.7	µs	—
HOCO周期抖动	—	—	±85	—	ps	—
锁相环时钟频率	f_{PLL}	120	—	240	MHz	—
PLL2时钟频率	f_{PLL2}	120	—	240	MHz	—
PLLPLL2时钟振荡稳定等待时间	t_{PLLWT}	—	—	174.9	µs	Figure 46.6
PLLPLL2周期抖动	—	—	±100	—	ps	—
PLLPLL2长期抖动	—	—	±300	—	ps	Term: 1µs, 10µs

注1.设置主时钟振荡器时，请向振荡器制造商索取振荡评估，并将结果作为推荐的振荡稳定时间。将MOSCWTCR寄存器设置为等于或大于推荐值的值。更改MOSCCR.MOSTP位的设置以启动主时钟操作后，读取OSCSF.MOSCSF标志以确认其为1，然后开始使用主时钟振荡器。

注2.这是从复位状态释放到HOCO振荡频率(fHOCO)达到保证工作范围的时间。

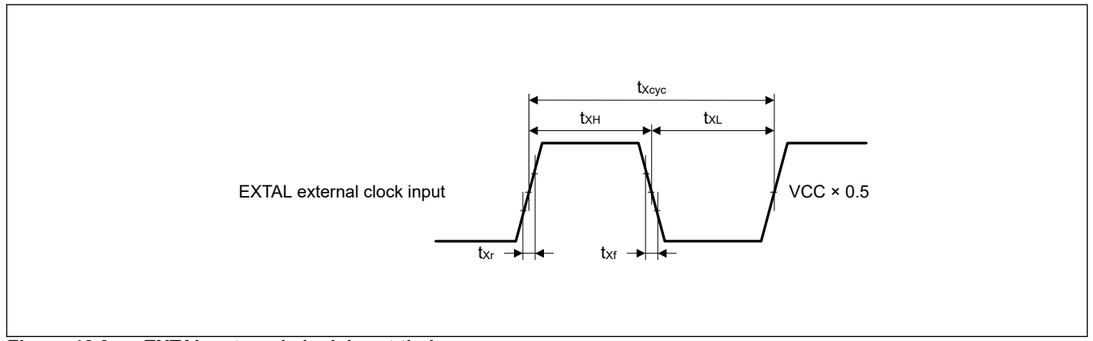


Figure 46.3 EXTAL external clock input timing

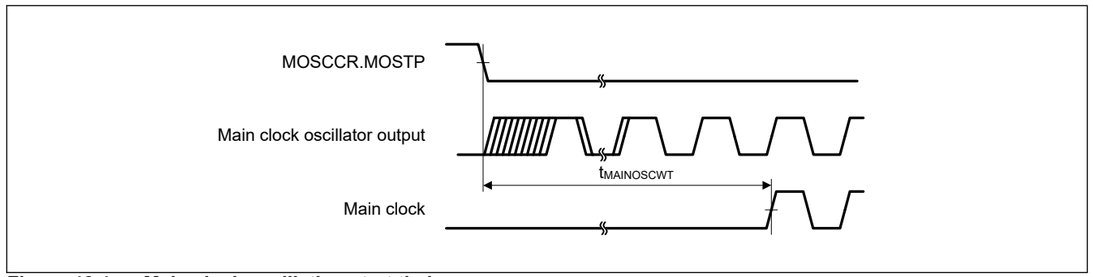


Figure 46.4 Main clock oscillation start timing

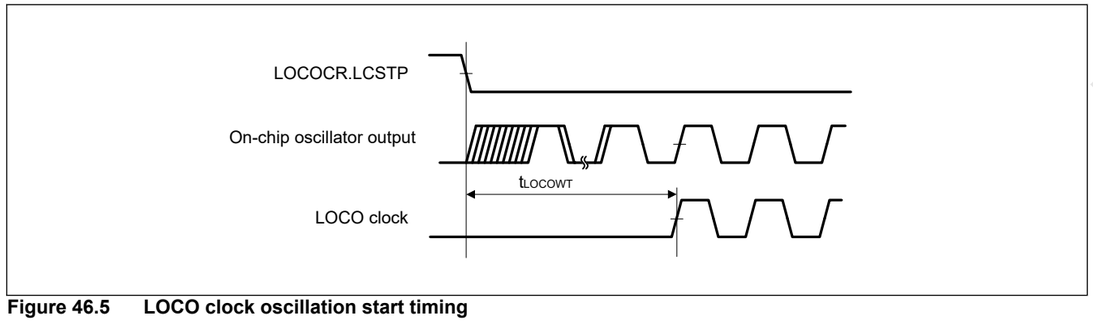


Figure 46.5 LOCO clock oscillation start timing

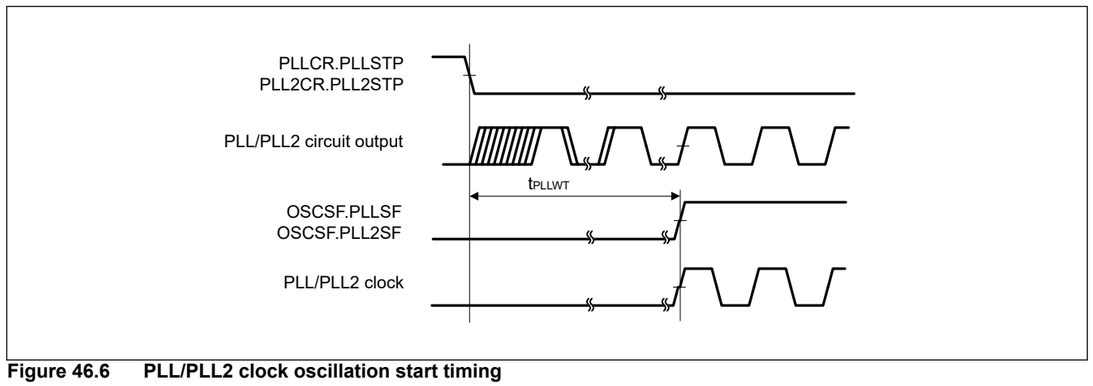


Figure 46.6 PLL/PLL2 clock oscillation start timing

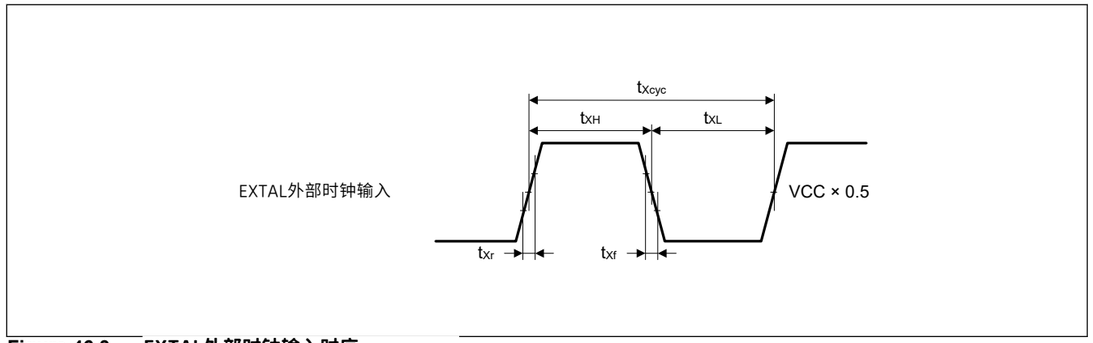


Figure 46.3 EXTAL外部时钟输入时序

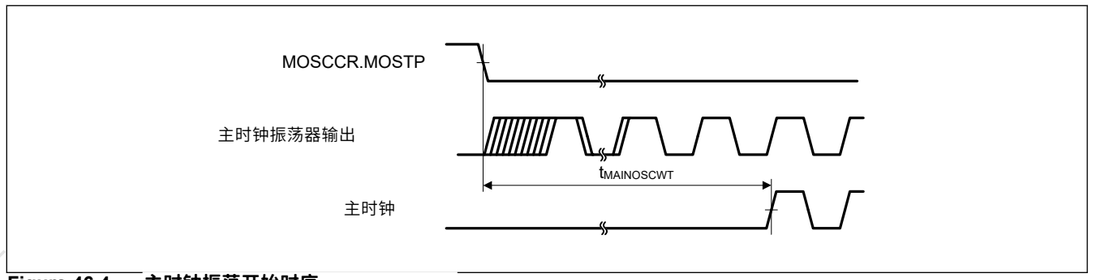


Figure 46.4 主时钟振荡开始时序

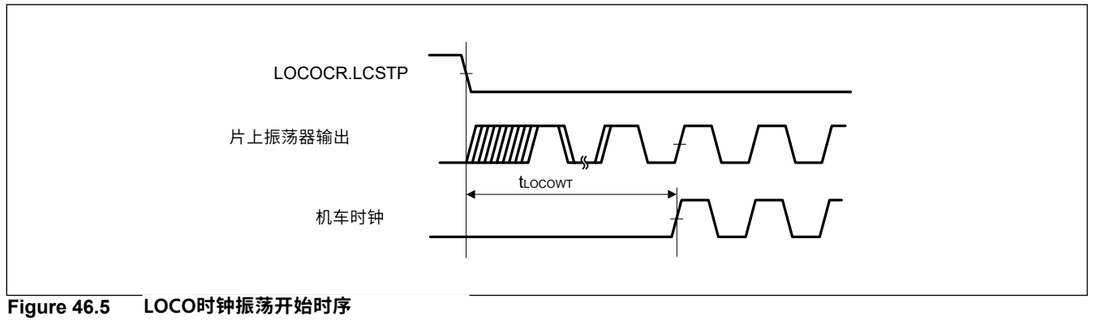


Figure 46.5 LOCO时钟振荡开始时序

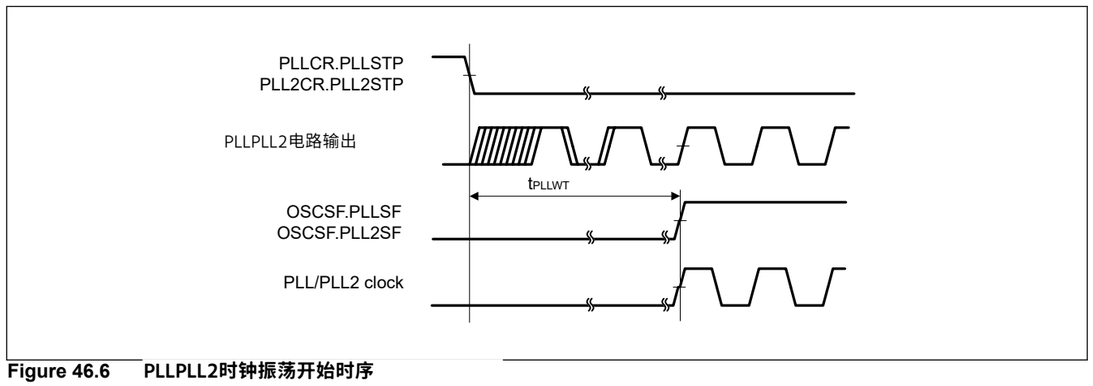


Figure 46.6 PLLPLL2时钟振荡开始时序

46.3.3 Reset Timing

Table 46.17 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	0.7	—	—	ms	Figure 46.7
	Deep Software Standby mode	t_{RESWD}	0.6	—	—	ms	Figure 46.8
	Software Standby mode	t_{RESWS}	0.3	—	—	ms	
	All other	t_{RESW}	200	—	—	µs	
Wait time after RES cancellation		t_{RESWT}	—	37.3	41.2	µs	Figure 46.7
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, bus master MPU error reset, TrustZone error reset, Cache parity error reset)		t_{RESW2}	—	324	397.7	µs	—

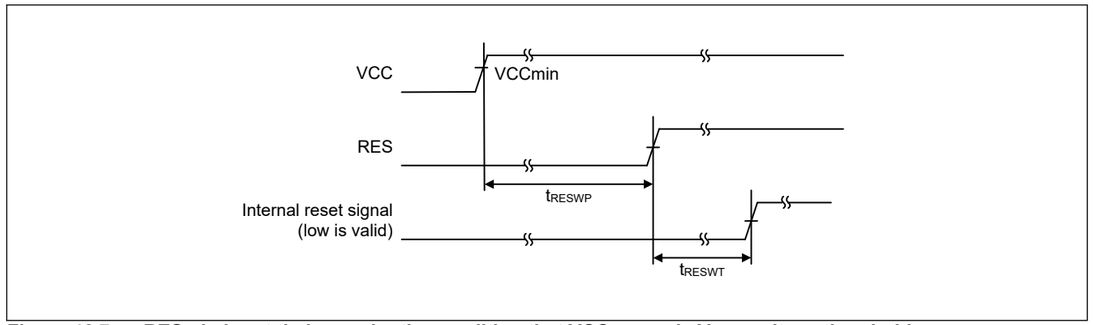


Figure 46.7 RES pin input timing under the condition that VCC exceeds V_{POR} voltage threshold

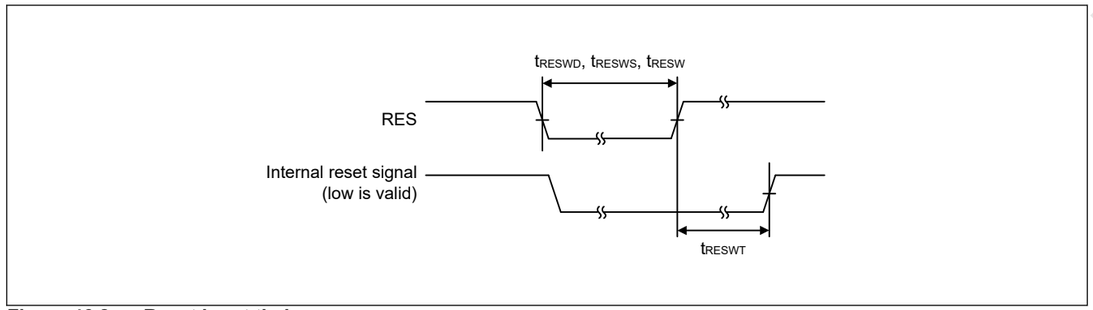


Figure 46.8 Reset input timing

46.3.3 重置时间

Table 46.17 重置时间

Parameter		符号	最小值	典型值	Max	单元	测试条件
RES脉冲宽度	Power-on	t_{RESWP}	0.7	—	—	ms	Figure 46.7
	深度软件待机模式	t_{RESWD}	0.6	—	—	ms	Figure 46.8
	软件待机模式	t_{RESWS}	0.3	—	—	ms	
	所有其他	t_{RESW}	200	—	—	µs	
RES取消后的等待时间		t_{RESWT}	—	37.3	41.2	µs	Figure 46.7
内部复位取消后的等待时间（IWDT复位、WDT复位、软件复位、SRAM奇偶校验错误复位、总线主控MPU错误复位、TrustZone错误复位、缓存奇偶校验错误复位）		t_{RESW2}	—	324	397.7	µs	—

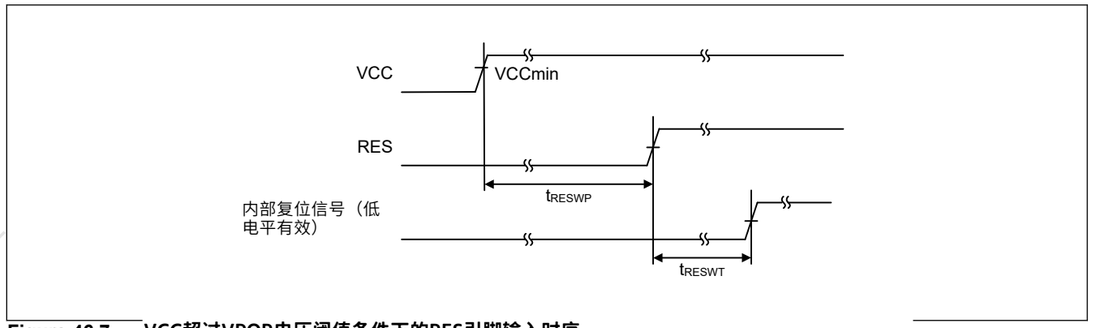


Figure 46.7 VCC超过VPOR电压阈值条件下的RES引脚输入时序

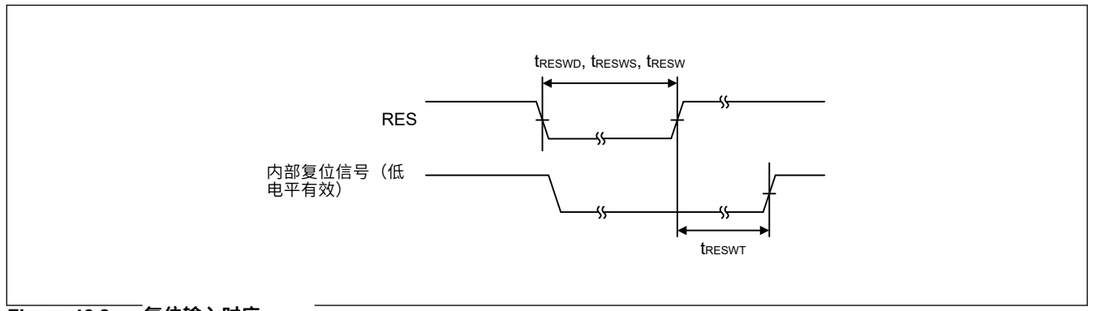


Figure 46.8 复位输入时序

46.3.4 Wakeup Timing

Table 46.18 Timing of recovery from low power modes

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}*11	—	2.1	2.4	ms	Figure 46.9 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	t_{SBYPC}*11	—	2.2	2.6	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}*11	—	45	125	µs	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}*11	—	170	255	µs	
	System clock source is LOCO*6		t_{SBYLO}*11	—	0.7	0.9	ms	
	System clock source is HOCO clock oscillator*7		t_{SBYHO}*11	—	55	130	µs	
	System clock source is PLL with HOCO*8		t_{SBYPH}*11	—	175	265	µs	
	System clock source is MOCO clock oscillator*9		t_{SBYMO}*11	—	35	65	µs	
Recovery time from Deep Software Standby mode	DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E		t_{DSBY}	—	0.38	0.54	ms	Figure 46.10
	DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19		t_{DSBY}	—	0.55	0.73	ms	
Wait time after cancellation of Deep Software Standby mode			t_{DSBYWT}	56	—	57	t_{cyc}	
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)		t_{SNZ}	—	35*10	70*10	µs	Figure 46.11
	High-speed mode when system clock source is MOCO (8 MHz)		t_{SNZ}	—	11*10	14*10	µs	

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest tSBYOSCWT in the active oscillators - tSBYOSCWT for the system clock + 2 LOCO cycles (when LOCO is operating)
Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 1.
Note 3. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 4.
Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 1.
Note 5. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 4.
Note 6. The LOCO frequency is 32.768 kHz and the greatest value of the internal clock division setting is 1.
Note 7. The HOCO frequency is 20 MHz and the greatest value of the internal clock division setting is 1.
Note 8. The PLL frequency is 240 MHz and the greatest value of the internal clock division setting is 4.
Note 9. The MOCO frequency is 8 MHz and the greatest value of the internal clock division setting is 1.
Note 10. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time: 16 µs (typical), 48 µs (maximum).
Note 11. The recovery time can be calculated with the equation of tSBYOSCWT + tSBYSEQ. And they can be determined with the following value and equation. For n, the greatest value is selected from among the internal clock division settings.

Wakeup time	TYP		MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYMC	(MSTS[7:0]*32 + 3) / 0.262	35 + 18 / fICLK + 4n / fMAIN	(MSTS[7:0]*32 + 14 / 0.236	62 + 18 / fICLK + 4n / fMAIN	µs
tSBYPC	(MSTS[7:0]*32 + 34) / 0.262	35 + 18 / fICLK + 4n / fPLL	(MSTS[7:0]*32 + 45) / 0.236	62 + 18 / fICLK + 4n / fPLL	µs

46.3.4 唤醒时间

Table 46.18 从低功耗模式恢复的时间

Parameter			Symbol	Min	Typ	Max	单元测试条件	
恢复时间从软件待机模式*1	连接到主时钟振荡器的晶体谐振器	系统时钟源为主时钟振荡器*2	t_{SBYMC}*11	—	2.1	2.4	ms	Figure 46.9 所有振荡器的分频比为1。
		系统时钟源为带主时钟振荡器的PLL*3	t_{SBYPC}*11	—	2.2	2.6	ms	
	主时钟振荡器的外部时钟输入	系统时钟源为主时钟振荡器*4	t_{SBYEX}*11	—	45	125	µs	
		系统时钟源为带主时钟振荡器的PLL*5	t_{SBYPE}*11	—	170	255	µs	
	系统时钟源为LOCO*6		t_{SBYLO}*11	—	0.7	0.9	ms	
	系统时钟源为HOCO时钟振荡器*7		t_{SBYHO}*11	—	55	130	µs	
	系统时钟源是带有HOCO*8的PLL		t_{SBYPH}*11	—	175	265	µs	
	系统时钟源为MOCO时钟振荡器*9		t_{SBYMO}*11	—	35	65	µs	
恢复时间从深度软件待机模式	DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E		t_{DSBY}	—	0.38	0.54	ms	Figure 46.10
	DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19		t_{DSBY}	—	0.55	0.73	ms	
取消深度软件待机模式后的等待时间			t_{DSBYWT}	56	—	57	t_{cyc}	
恢复时间从软件待机模式到贪睡模式	系统时钟源为高速模式 HOCO (20 MHz)		t_{SNZ}	—	35*10	70*10	µs	Figure 46.11
	系统时钟源为高速模式 MOCO (8 MHz)		t_{SNZ}	—	11*10	14*10	µs	

注1.恢复时间由系统时钟源决定。当多个振荡器处于活动状态时，恢复时间可以通过以下公式确定：总恢复时间=一个振荡器作为系统时钟源的恢复时间+系统时钟有效振荡器中的最长tSBYOSCWTtSBYOSCWT+2个LOCO周期（当LOCO正在运行）

注2.当晶振频率为24MHz（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x05）且内部时钟分频设置的最大值为1时。

注3.当PLL的频率为240MHz（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x05）且内部时钟分频设置的最大值为4时。

注4.当外部时钟频率为24MHz（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x00）且内部时钟分频设置的最大值为1时。

注5.当PLL的频率为240MHz（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x00）且内部时钟分频设置的最大值为4时。

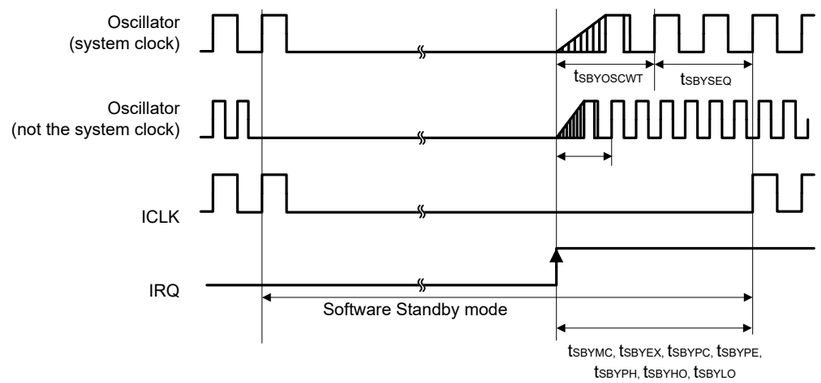
注6.LOCO频率为32.768kHz，内部时钟分频设置的最大值为1。
注7.HOCO频率为20MHz，内部时钟分频设置最大值为1。注8.PLL频率为240MHz，内部时钟分频设置最大值为4。注9.MOCO频率为8MHz，内部时钟分频设置的最大值为1。

注10.当SNZCR.RXDREQEN位设置为0时，添加以下时间作为电源恢复时间：16µs（典型值）、48µs（最大值）。

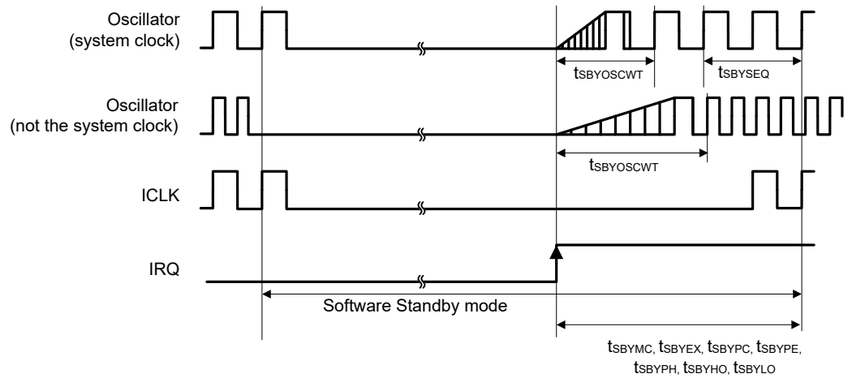
注11.恢复时间可以用tSBYOSCWT+tSBYSEQ等式计算。并且它们可以通过以下值和等式确定。对于n，从内部时钟分频设置中选择最大值。

唤醒时间典型值			MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYMC	(MSTS[7:0]*32 + 3) / 0.262	35 + 18 / fICLK + 4n / fMAIN	(MSTS[7:0]*32 + 14 / 0.236	62 + 18 / fICLK + 4n / fMAIN	µs
tSBYPC	(MSTS[7:0]*32 + 34) / 0.262	35 + 18 / fICLK + 4n / fPLL	(MSTS[7:0]*32 + 45) / 0.236	62 + 18 / fICLK + 4n / fPLL	µs

Wakeup time	TYP		MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYEX	10	35 + 18 / fICLK + 4n / fEXMAIN	62	62 + 18 / fICLK + 4n / fEXMAIN	µs
tSBYPE	135	35 + 18 / fICLK + 4n / fPLL	192	62 + 18 / fICLK + 4n / fPLL	µs
tSBYLO	0	35 + 18 / fICLK + 4n / fLOCO	0	62 + 18 / fICLK + 4n / fLOCO	µs
tSBYHO	20	35 + 18 / fICLK + 4n / fHOCO	67	62 + 18 / fICLK + 4n / fHOCO	µs
tSBYPH	140	35 + 18 / fICLK + 4n / fPLL	202	62 + 18 / fICLK + 4n / fPLL	µs
tSBYMO	0	35 + 18 / fICLK + 4n / fMOCO	0	62 + 18 / fICLK + 4n / fMOCO	µs



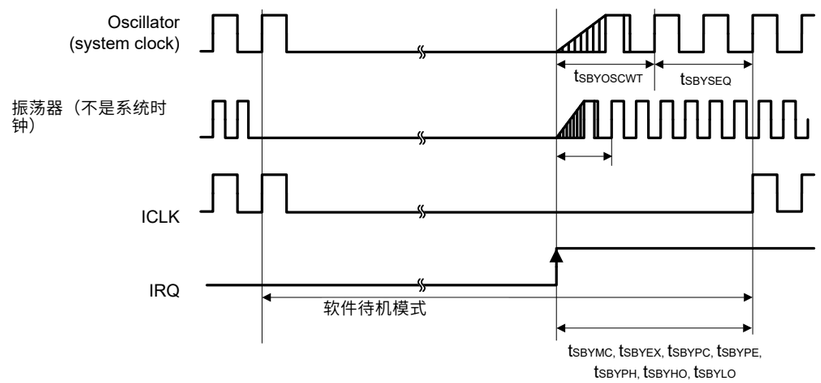
When stabilization of the system clock oscillator is slower



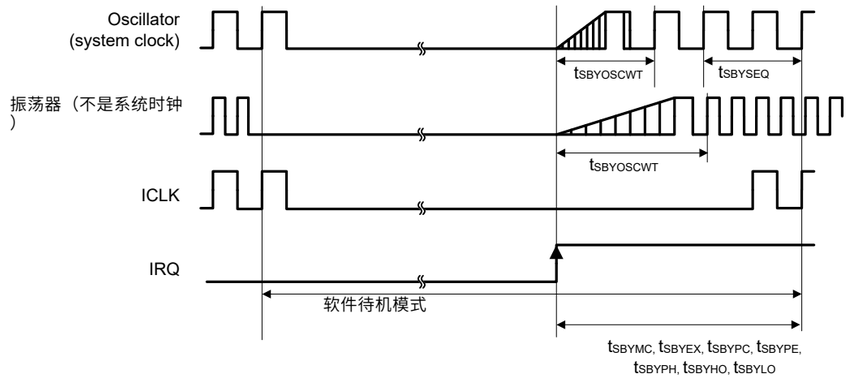
When stabilization of an oscillator other than the system clock is slower

Figure 46.9 Software Standby mode cancellation timing

唤醒时间典型值			MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYEX	10	35 + 18 / fICLK + 4n / fEXMAIN	62	62 + 18 / fICLK + 4n / fEXMAIN	µs
tSBYPE	135	35 + 18 / fICLK + 4n / fPLL	192	62 + 18 / fICLK + 4n / fPLL	µs
tSBYLO	0	35 + 18 / fICLK + 4n / fLOCO	0	62 + 18 / fICLK + 4n / fLOCO	µs
tSBYHO	20	35 + 18 / fICLK + 4n / fHOCO	67	62 + 18 / fICLK + 4n / fHOCO	µs
tSBYPH	140	35 + 18 / fICLK + 4n / fPLL	202	62 + 18 / fICLK + 4n / fPLL	µs
tSBYMO	0	35 + 18 / fICLK + 4n / fMOCO	0	62 + 18 / fICLK + 4n / fMOCO	µs



当系统时钟振荡器的稳定速度较慢时



当系统时钟以外的振荡器稳定较慢时

Figure 46.9 软件待机模式取消时序

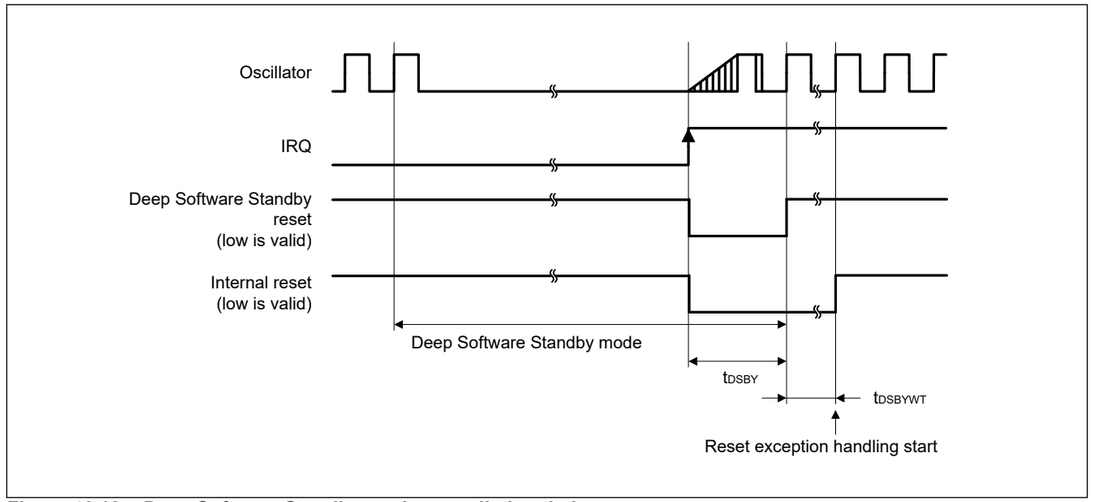
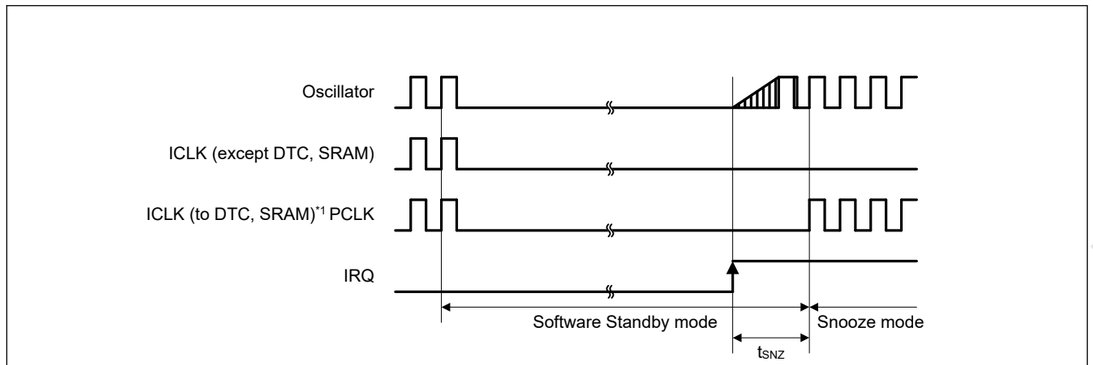


Figure 46.10 Deep Software Standby mode cancellation timing



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 46.11 Recovery timing from Software Standby mode to Snooze mode

46.3.5 NMI and IRQ Noise Filter

Table 46.19 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

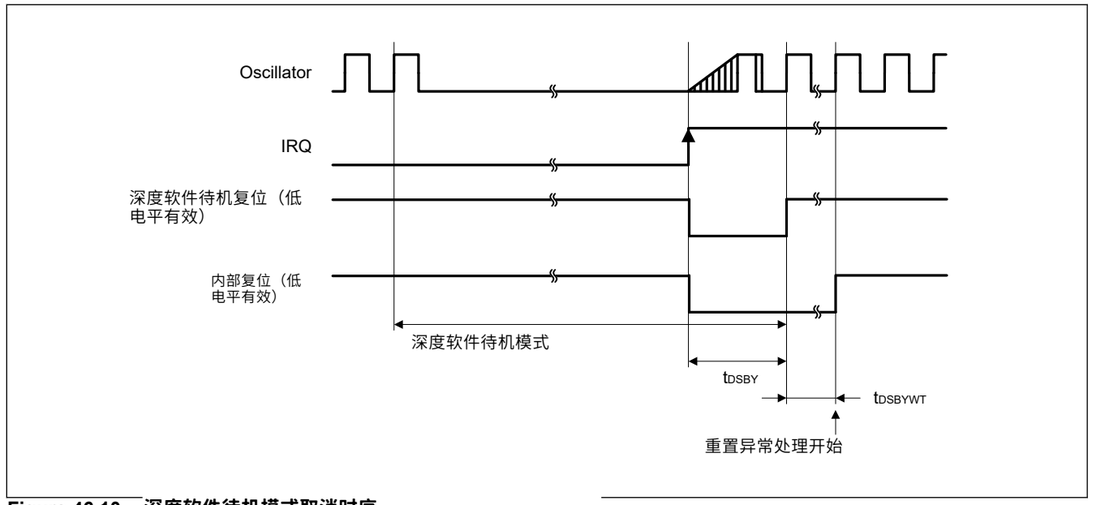
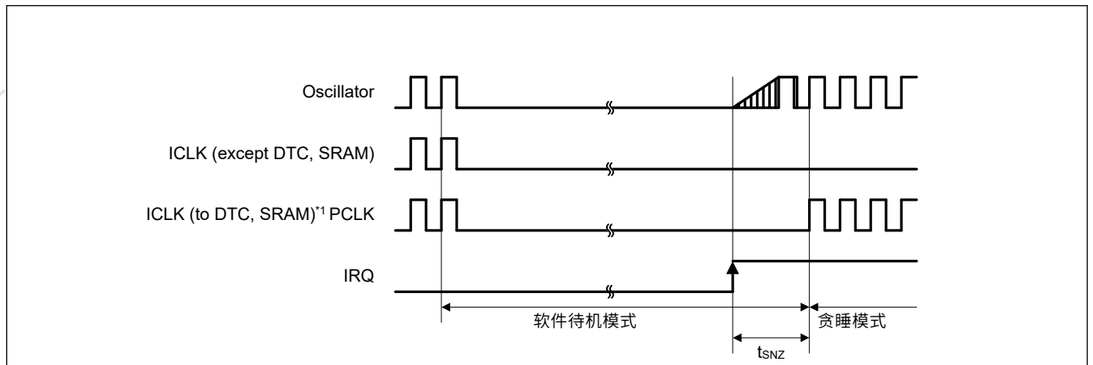


Figure 46.10 深度软件待机模式取消时序



注1.当SNZCR.SNZDTCEN位设置为1时，ICLK提供给DTC和SRAM。

Figure 46.11 从软件待机模式到贪睡模式的恢复时间

46.3.5 NMI和IRQ噪声滤波器

Table 46.19 NMI和IRQ噪声滤波器

Parameter	Symbol	Min	Typ	Max	Unit	测试条件	
NMI脉冲宽度	t_{NMIW}	200	—	—	ns	NMI数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		启用NMI数字滤波器	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ脉冲宽度	t_{IRQW}	200	—	—	ns	IRQ数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		启用IRQ数字滤波器	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

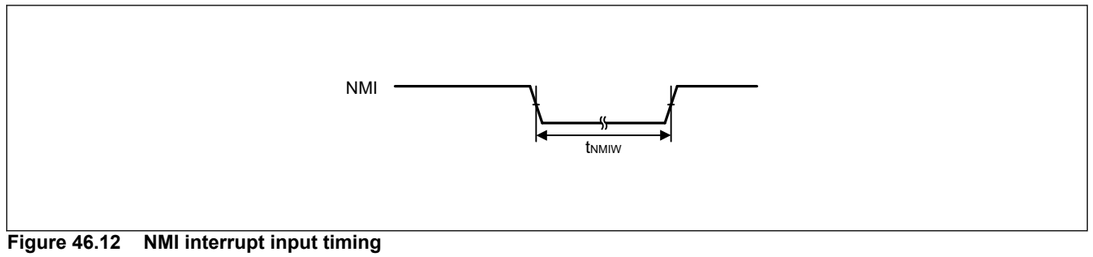


Figure 46.12 NMI interrupt input timing

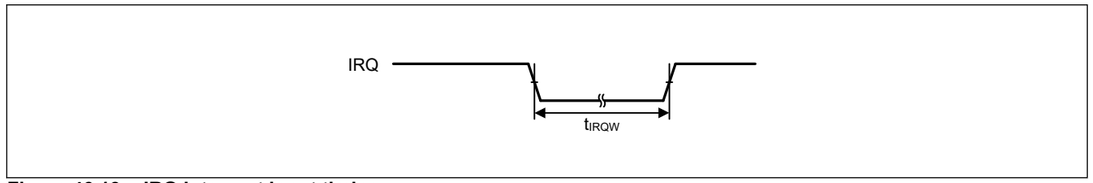


Figure 46.13 IRQ interrupt input timing

46.3.6 I/O Ports, POEG, GPT, AGT, KINT and ADC Trigger Timing

Table 46.20 I/O ports, POEG, GPT, AGT, KINT and ADC trigger timing (1 of 4)

GPT Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	—	t_{Icyc}	Figure 46.14

Note: 软件待机模式下最少200ns。
Note: 如果时钟源切换，则增加切换源的4个时钟周期。
注1.tPcyc表示PCLKB周期。
注2.tNMICK表示NMI数字滤波器采样时钟的周期。注3.tIRQCK表示IRQi数字滤波器采样时钟的周期。

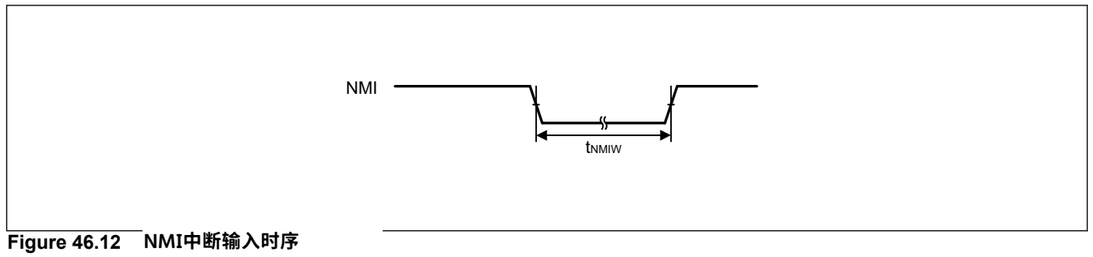


Figure 46.12 NMI中断输入时序

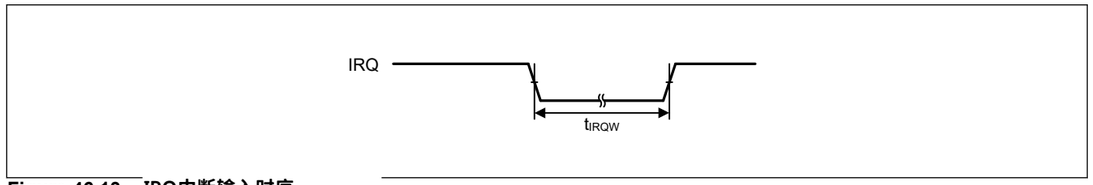


Figure 46.13 IRQ中断输入时序

46.3.6 IO端口、POEG、GPT、AGT、KINT和ADC触发时序

Table 46.20 IO端口、POEG、GPT、AGT、KINT和ADC触发时序（4个中的1个）

GPT条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

AGT Conditions:
在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
I/O ports	输入数据脉冲宽度	t_{PRW}	1.5	—	—	t_{Icyc}	Figure 46.14

Table 46.20 I/O ports, POEG, GPT, AGT, KINT and ADC trigger timing (2 of 4)

GPT Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
POEG	GTETRGn input pulse width		t_{POEW}	1.5	—	—	t_{Pcyc}	Figure 46.15
	Output disable time	Input level detection of the GTETRGn pin (via flag)	t_{POEGDI}	—	—	3 PCLKB + 0.34	µs	Figure 46.16 When the digital noise filter is not in use (POEGGn.NFEN = 0 (n = A to D))
		Detection of the output stopping signal from GPT (deadtime error, simultaneous high output, or simultaneous low output)	t_{POEGDE}	—	—	0.5	µs	Figure 46.17
		Edge detection signal from a comparator	t_{POEGDC}	—	—	4 PCLKB + 0.5	µs	Figure 46.18 The time is that when the noise filter for ACMPHS is not in use (CMPCTL.CDFS[1:0] = 00) and excludes the time for detection by ACMPHS.
		Register setting	t_{POEGDS}	—	—	1 PCLKB + 0.3	µs	Figure 46.19 Time for access to the register is not included.
		Oscillation stop detection*3	$t_{POEGDOS}$	—	≤ 1	—	µs	Figure 46.20
		Input level detection of the GTETRGn pin (direct path)	$t_{POEGDDI}$	—	—	2 PCLKB + 1 PCLKD + 0.34	µs	Figure 46.21
		Level detection signal from a comparator	$t_{POEGDDC}$	—	—	3 PCLKD + 0.3	µs	Figure 46.22 The time is that when the noise filter for ACMPHS is not in use (CMPCTL.CDFS[1:0] = 00) and excludes the time for detection by ACMPHS.

Table 46.20 IO端口、POEG、GPT、AGT、KINT和ADC触发时序（4个中的2个）

GPT条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

AGT Conditions:
在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
POEG	GTETRn输入脉冲宽度		t_{POEW}	1.5	—	—	t_{Pcyc}	Figure 46.15
	输出禁用时间	的输入电平检测 GTETRGn pin (via flag)	t_{POEGDI}	—	—	3 PCLKB + 0.34	µs	Figure 46.16 当不使用数字噪声滤波器时（POEGGn.NFEN=0（n=A到 D))
		检测来自GPT的输出停止信号（死区错误、同时高输出或同时低输出）	t_{POEGDE}	—	—	0.5	µs	Figure 46.17
		来自比较器的边缘检测信号	t_{POEGDC}	—	—	4 PCLKB + 0.5	µs	Figure 46.18 时间是不使用ACMPHS的噪声滤波器时（CMPCTL.CDFS[1:0]=00），不包括ACMPHS检测的时间。
		注册设置	t_{POEGDS}	—	—	1 PCLKB + 0.3	µs	Figure 46.19 不包括访问寄存器的时间。
		振荡停止检测*3	$t_{POEGDOS}$	—	≤ 1	—	µs	Figure 46.20
		GTETRn引脚的输入电平检测（直接路径）	$t_{POEGDDI}$	—	—	2 PCLKB + 1 PCLKD + 0.34	µs	Figure 46.21
		来自比较器的电平检测信号	$t_{POEGDDC}$	—	—	3 PCLKD + 0.3	µs	Figure 46.22 时间是不使用ACMPHS的噪声滤波器时（CMPCTL.CDFS[1:0]=00），不包括ACMPHS检测的时间。

Table 46.20 I/O ports, POEG, GPT, AGT, KINT and ADC trigger timing (3 of 4)

GPT Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
GPT	Input capture pulse width	Single edge		t_{GTICW}	1.5	—	—	t_{PDcyc}	Figure 46.23
		Dual edge			2.5	—	—		
	GTIOCxY output skew (x = 0 to 3, Y = A or B)	Middle drive buffer		t_{GTISK}*1	—	—	4	ns	Figure 46.24
		High drive buffer			—	—	4		
		High current output buffer			—	—	4		
	GTIOCxY output skew (x = 4 to 6, Y = A or B)	Middle drive buffer			—	—	4		
		High drive buffer			—	—	4		
		High current output buffer			—	—	4		
	GTIOCxY output skew (x = 7 to 9, Y = A or B)	Middle drive buffer			—	—	4		
		High drive buffer			—	—	4		
		High current output buffer			—	—	4		
	GTIOCxY output skew (x = 0 to 9, Y = A or B)	Middle drive buffer			—	—	6		
		High drive buffer			—	—	6		
		High current output buffer			—	—	6		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO			t_{GTOSK}	—	—	5	ns	Figure 46.25
	External trigger input pulse width	Synchronous clock	Single-edge setting	t_{GTEW}	1.5	—	—	t_{Pcyc}	Figure 46.26
			Both-edge setting		2.5	—	—		
		Asynchronous clock	Single-edge setting		2.5	—	—		
			Both-edge setting		3.5	—	—		
	Timer clock pulse width	Synchronous clock	Single-edge setting	t_{GTCKWH}, t_{GTCKWL}	1.5	—	—	t_{Pcyc}	Figure 46.27
			Both-edge setting		2.5	—	—		
		Asynchronous clock	Single-edge setting		2.5	—	—		
			Both-edge setting		3.5	—	—		
GPT (PWM Delay Generation Circuit)	GTIOCxY_Z skew (x = 0 to 3, Y = A or B, Z = A to D)			t_{HRSK}*2	—	—	4.0	ns	Figure 46.28
AGT	AGTIO, AGTEE input cycle			t_{ACYC}*2	50	—	—	ns	Figure 46.29
	AGTIO, AGTEE input high width, low width			t_{ACKWH}, t_{ACKWL}	20	—	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle			t_{ACYC2}	33.3	—	—	ns	
KINT	KRn (n = 00 to 07) pulse width			t_{KR}	250	—	—	ns	Figure 46.30

Table 46.20 IO端口、POEG、GPT、AGT、KINT和ADC触发时序（3of4）

GPT条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

AGT Conditions:
在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
GPT	输入捕捉脉冲宽度	单边		t_{GTICW}	1.5	—	—	t_{PDcyc}	Figure 46.23
		双刃			2.5	—	—		
	GTIOCxY输出偏差（x=0到3，Y=A或B）	中间驱动缓冲器		t_{GTISK}*1	—	—	4	ns	Figure 46.24
		高驱动缓冲器			—	—	4		
		大电流输出缓冲器			—	—	4		
	GTIOCxY输出偏移（x=4到6，Y=A或B）	中间驱动缓冲器			—	—	4		
		高驱动缓冲器			—	—	4		
		大电流输出缓冲器			—	—	4		
	GTIOCxY输出偏移（x=7到9，Y=A或B）	中间驱动缓冲器			—	—	4		
		高驱动缓冲器			—	—	4		
		大电流输出缓冲器			—	—	4		
	GTIOCxY输出偏移（x=0到9，Y=A或B）	中间驱动缓冲器			—	—	6		
		高驱动缓冲器			—	—	6		
		大电流输出缓冲器			—	—	6		
	OPS输出偏差GTOUUP、GTOULO、GTOVUP, GTOVLO, GTOWUP, GTOWLO			t_{GTOSK}	—	—	5	ns	Figure 46.25
	外部触发输入脉冲宽度	Synchronous clock	Single-edge setting	t_{GTEW}	1.5	—	—	t_{Pcyc}	Figure 46.26
			Both-edge setting		2.5	—	—		
		Asynchronous clock	Single-edge setting		2.5	—	—		
			Both-edge setting		3.5	—	—		
	定时器时钟脉冲宽度	Synchronous clock	Single-edge setting	t_{GTCKWH}, t_{GTCKWL}	1.5	—	—	t_{Pcyc}	Figure 46.27
			Both-edge setting		2.5	—	—		
		Asynchronous clock	Single-edge setting		2.5	—	—		
			Both-edge setting		3.5	—	—		
GPT（PWM延迟生成 Circuit)	GTIOCxY_Z偏斜（x=0到3，Y=A或B，Z=A到D）			t_{HRSK}*2	—	—	4.0	ns	Figure 46.28
AGT	AGTIO、AGTEE输入周期			t_{ACYC}*2	50	—	—	ns	Figure 46.29
	AGTIO、AGTEE输入高宽、低宽			t_{ACKWH}, t_{ACKWL}	20	—	—	ns	
	AGTIO、AGTO、AGTOA、AGTOB输出周期			t_{ACYC2}	33.3	—	—	ns	
KINT	KRn(n=00to07)脉冲宽度			t_{KR}	250	—	—	ns	Figure 46.30

Table 46.20 I/O ports, POEG, GPT, AGT, KINT and ADC trigger timing (4 of 4)

GPT Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
ADC	ADC trigger input pulse width	t_{TRGW}	1.5	—	—	t_{ADcyc}	Figure 46.31

Note: t_{Icyc}: ICLK cycle, t_{Pcyc}: PCLKB cycle, t_{PDcyc}: GTCLK cycle, t_{ADcyc}: ADCLK cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.
Note 3. Reference value.

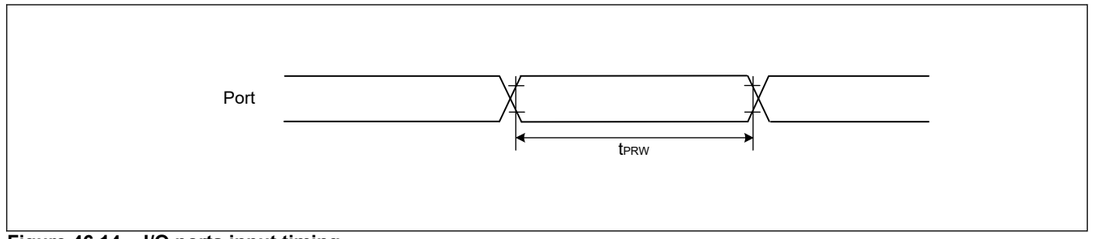


Figure 46.14 I/O ports input timing

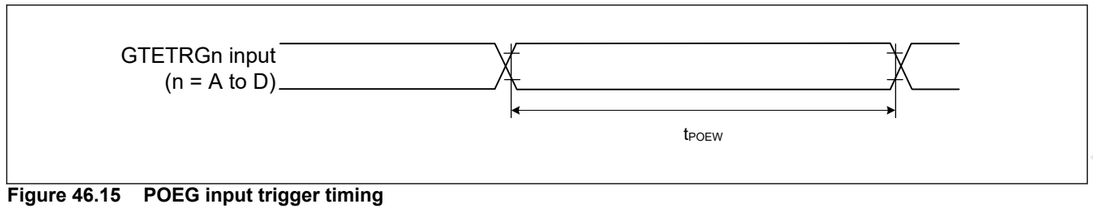


Figure 46.15 POEG input trigger timing

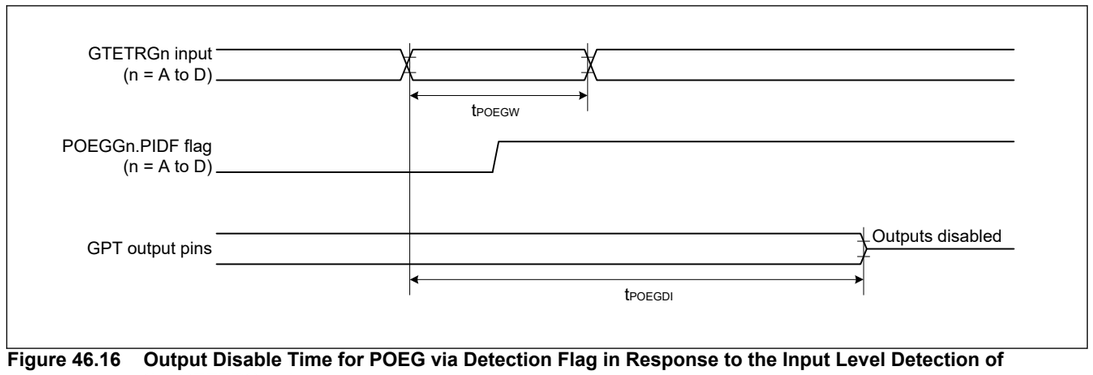


Figure 46.16 Output Disable Time for POEG via Detection Flag in Response to the Input Level Detection of the GTETRGn pin

Table 46.20 IO端口、POEG、GPT、AGT、KINT和ADC触发时序（4个中的4个）

GPT条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

AGT Conditions:
在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
ADC	ADC触发输入脉冲宽度	t_{TRGW}	1.5	—	—	t_{ADcyc}	Figure 46.31

Note: t_{Icyc}: ICLK cycle, t_{Pcyc}: PCLKB cycle, t_{PDcyc}: GTCLK cycle, t_{ADcyc}: ADCLK cycle.
注1.当使用相同的驱动器IO时，此偏差适用。如果中高驱动器的IO混合使用，则无法保证运行。
注2.输入周期的限制：
不切换源时钟时：tPcyc×2<tACYC应满足。
切换源时钟时：tPcyc×6<tACYC应满足。
注3.参考值。

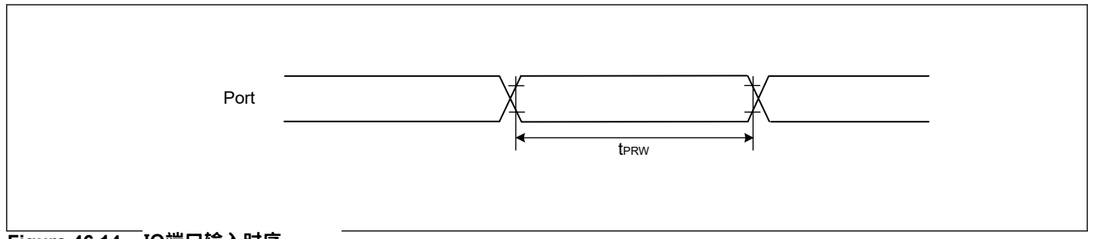


Figure 46.14 IO端口输入时序

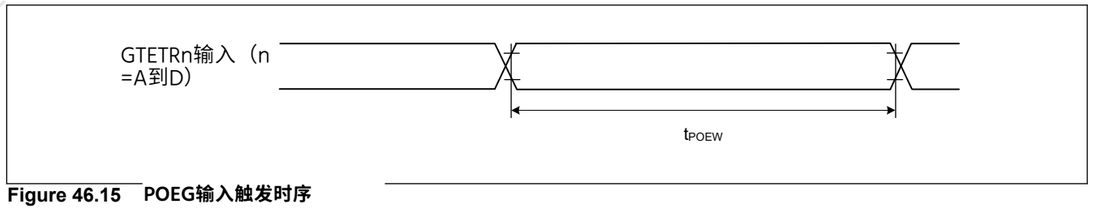


Figure 46.15 POEG输入触发时序

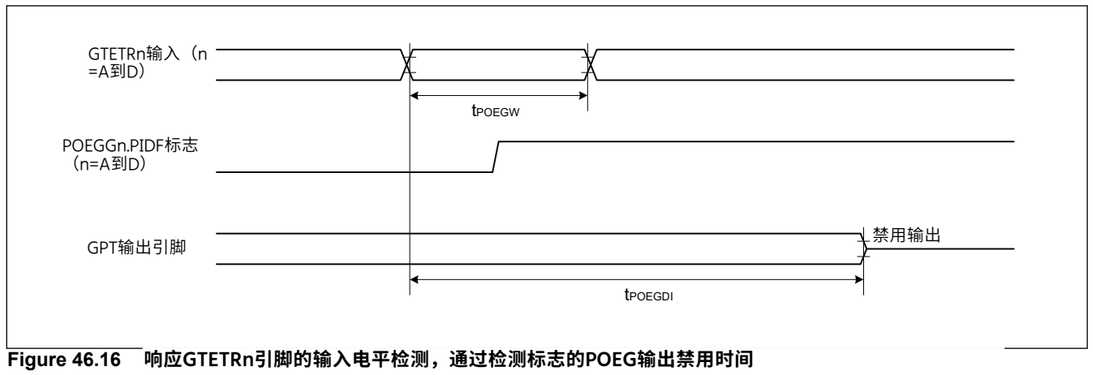
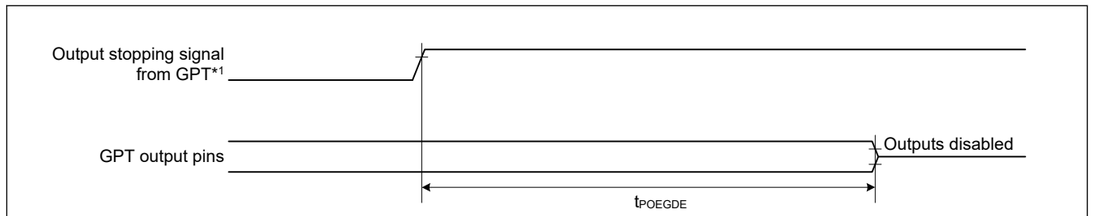


Figure 46.16 响应GTETRn引脚的输入电平检测，通过检测标志的POEG输出禁用时间



Note 1. GPT32n.GTST.DTEF (dead time error flag), GPT32n.GTST.OABLF (simultaneous low output flag), or GPT32n.GTST.OABHF (simultaneous high output flag)

Figure 46.17 Output Disable Time for POEG in Response to Detection of the Output Stopping Signal from GPT

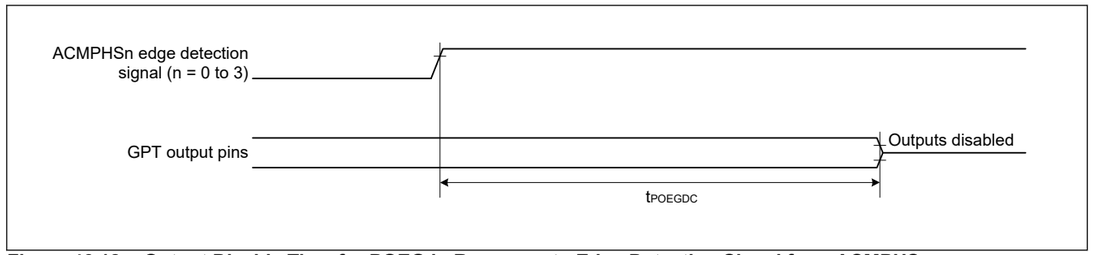


Figure 46.18 Output Disable Time for POEG in Response to Edge Detection Signal from ACMPHS

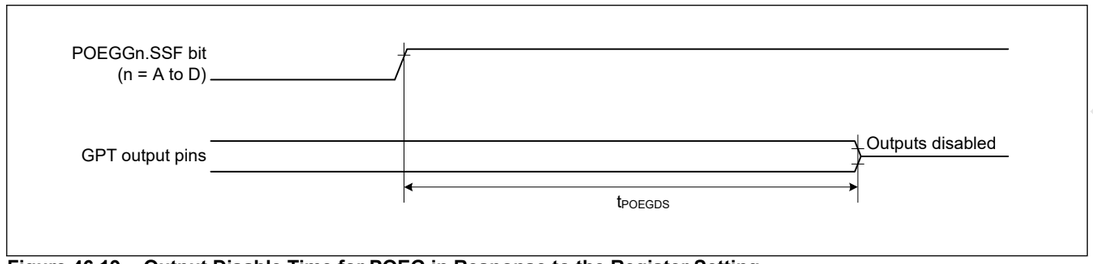


Figure 46.19 Output Disable Time for POEG in Response to the Register Setting

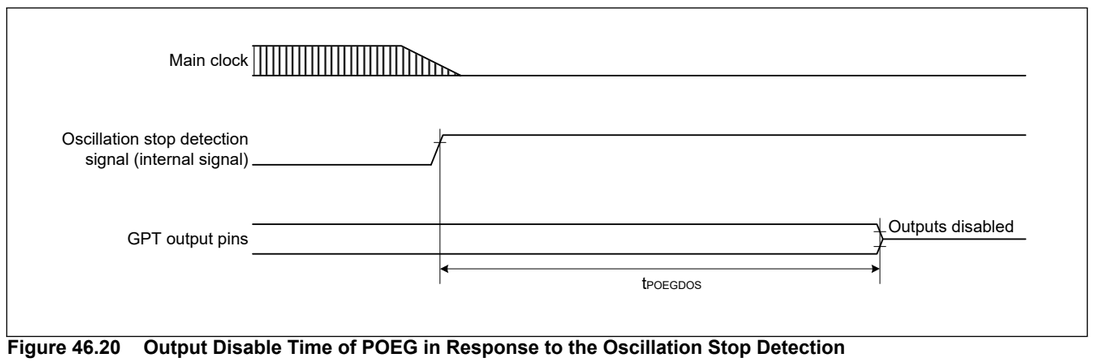
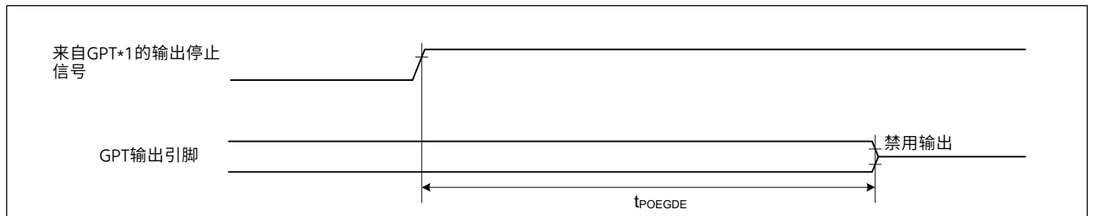


Figure 46.20 Output Disable Time of POEG in Response to the Oscillation Stop Detection



注1.GPT32n.GTST.DTEF（死区时间错误标志），GPT32n.GTST.OABLF（同时低输出标志），或GPT32n.GTST.OABHF（同时高电平输出标志）

Figure 46.17 POEG响应检测到输出停止信号的输出禁用时间

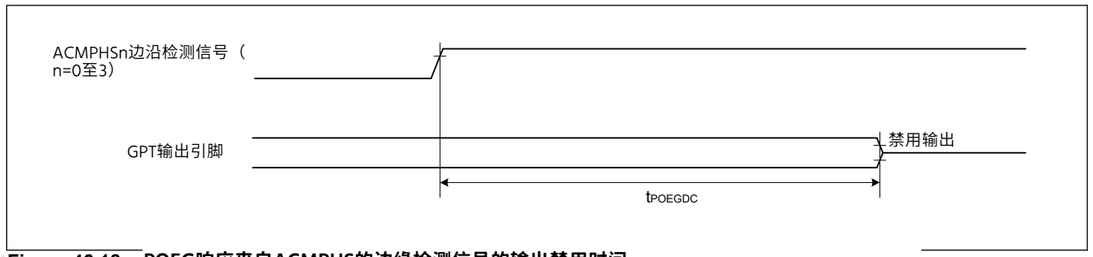


Figure 46.18 POEG响应来自ACMPHS的边缘检测信号的输出禁用时间

Figure 46.19 POEG响应寄存器设置的输出禁用时间

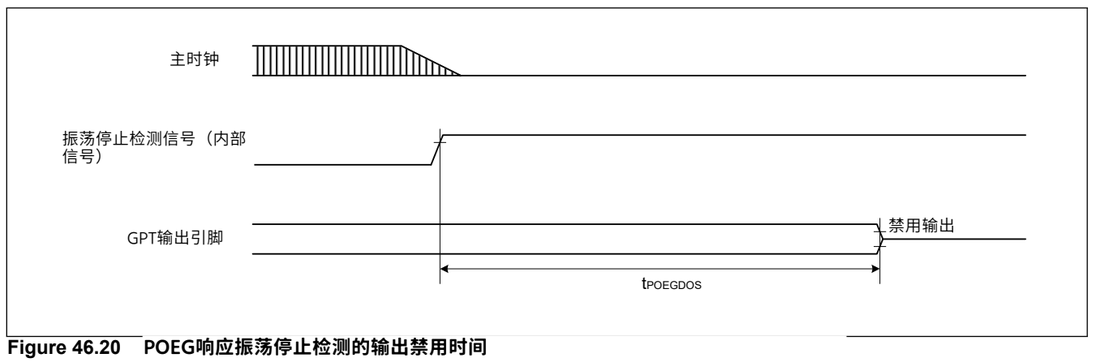


Figure 46.20 POEG响应振荡停止检测的输出禁用时间

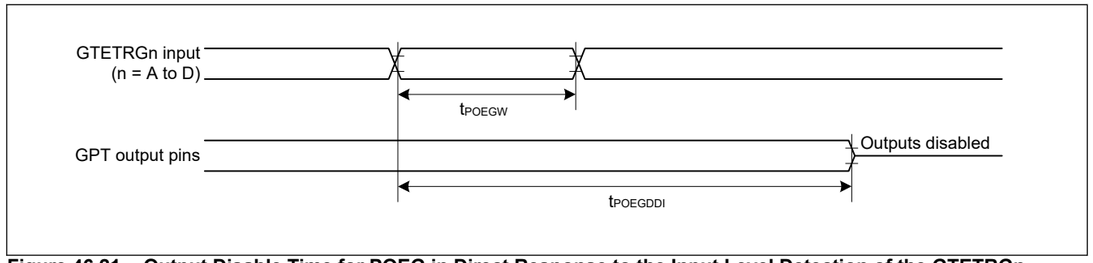


Figure 46.21 Output Disable Time for POEG in Direct Response to the Input Level Detection of the GTETRGn pin

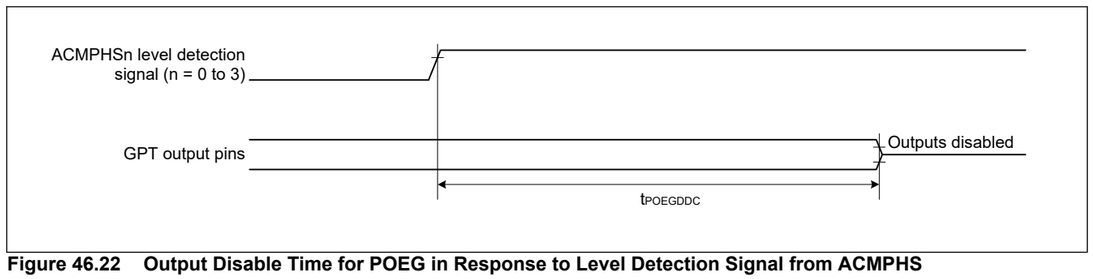


Figure 46.22 Output Disable Time for POEG in Response to Level Detection Signal from ACMPHS

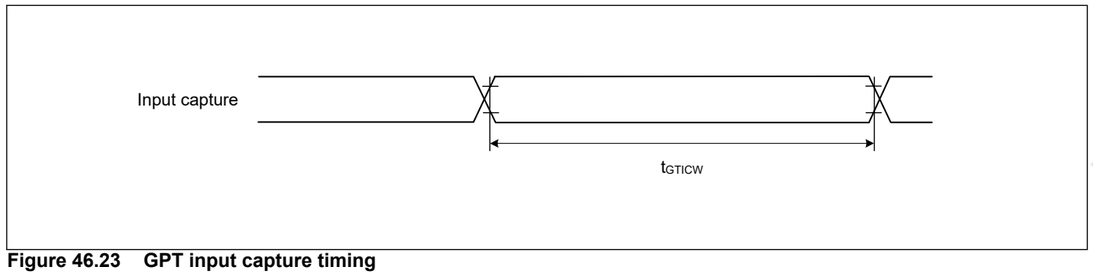


Figure 46.23 GPT input capture timing

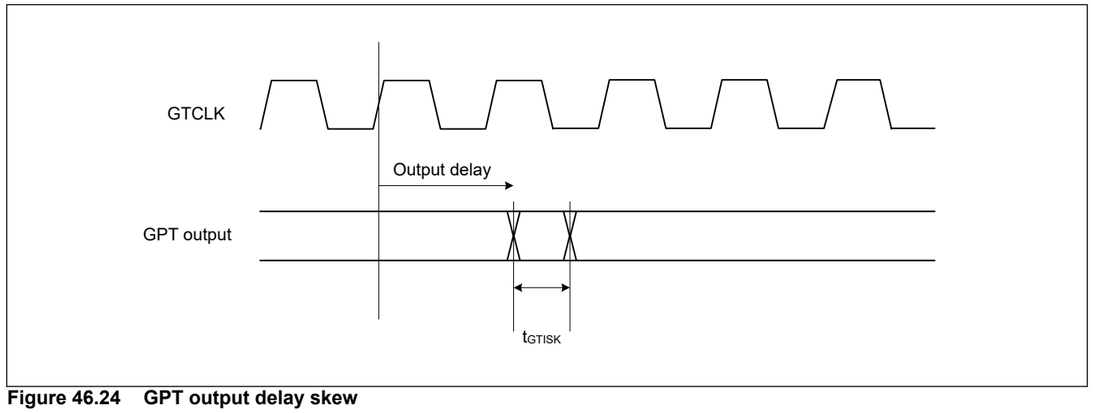


Figure 46.24 GPT output delay skew

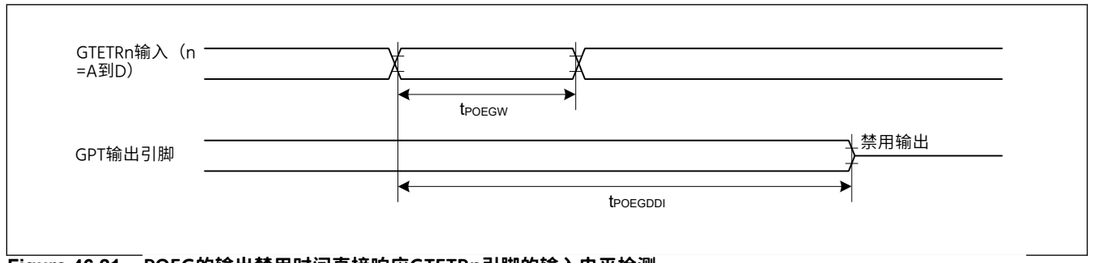


Figure 46.21 POEG的输出禁用时间直接响应GTETRn引脚的输入电平检测

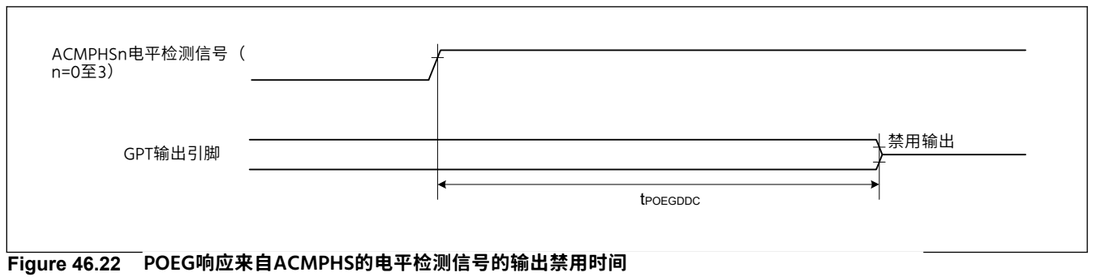


Figure 46.22 POEG响应来自ACMPHS的电平检测信号的输出禁用时间

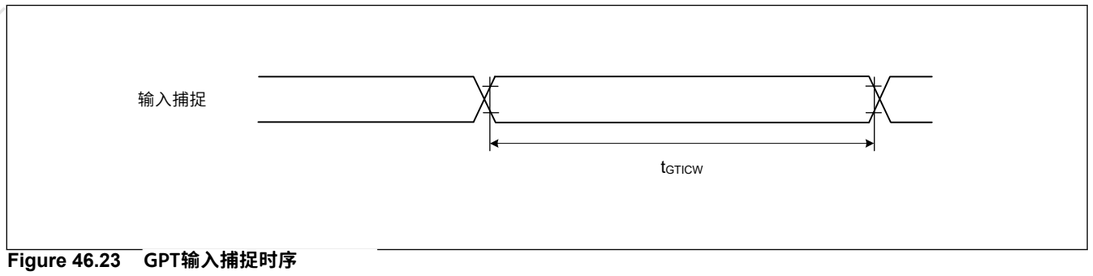


Figure 46.23 GPT输入捕捉时序

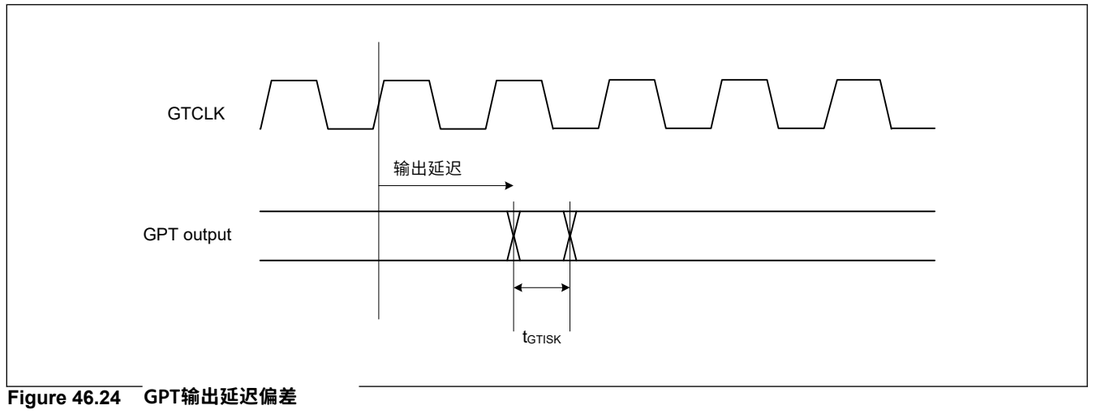


Figure 46.24 GPT输出延迟偏差

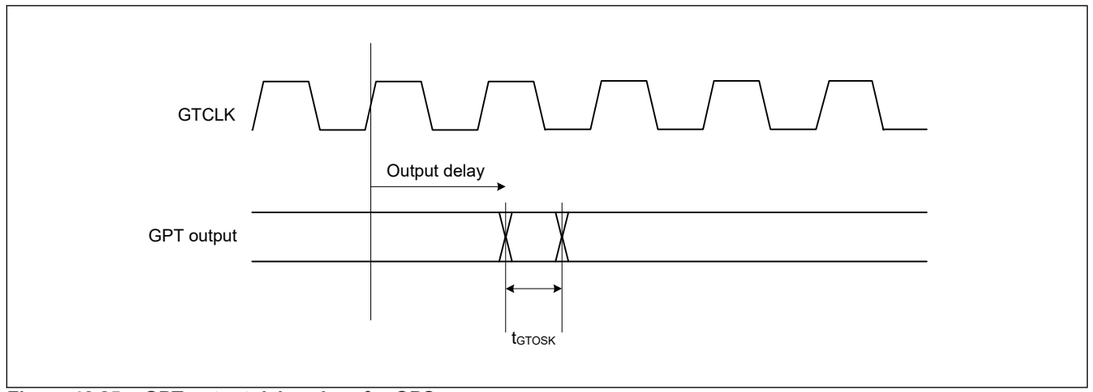


Figure 46.25 GPT output delay skew for OPS

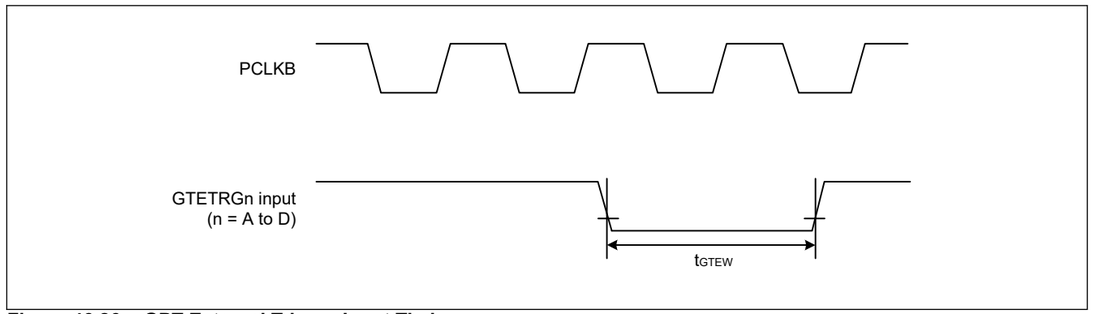


Figure 46.26 GPT External Trigger Input Timing

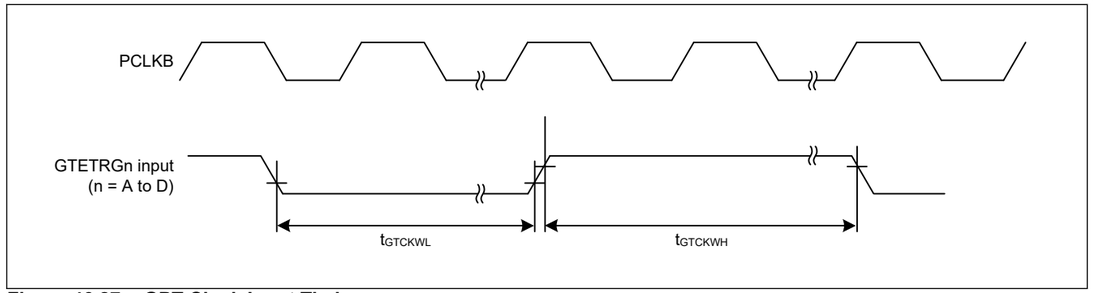


Figure 46.27 GPT Clock Input Timing

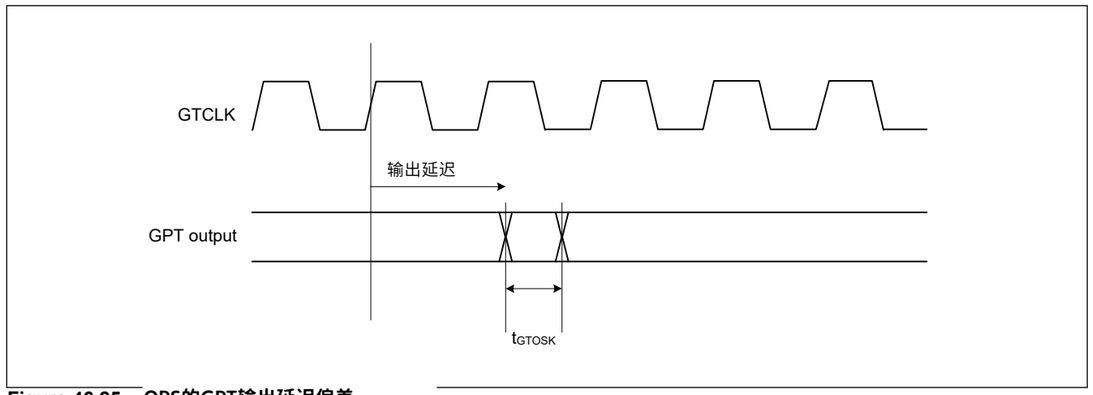


Figure 46.25 OPS的GPT输出延迟偏差

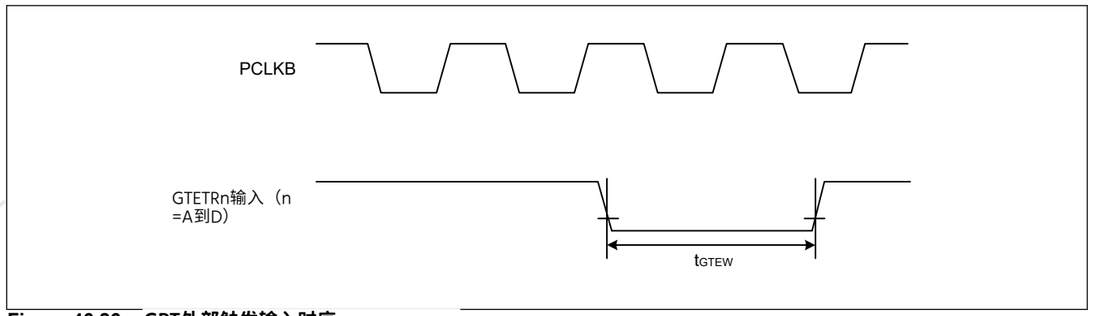


Figure 46.26 GPT外部触发输入时序

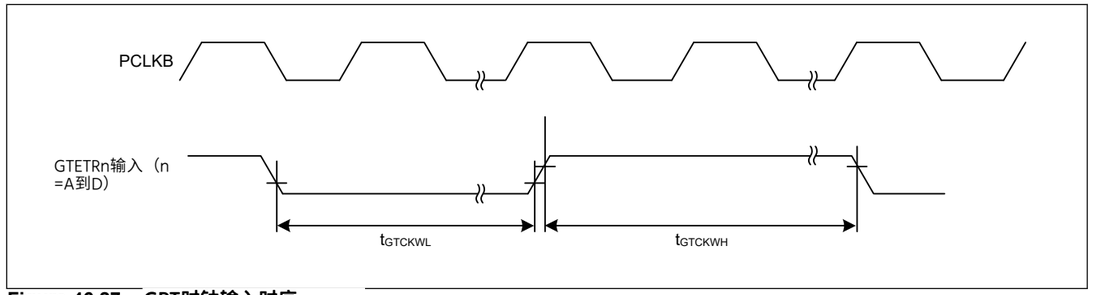


Figure 46.27 GPT时钟输入时序

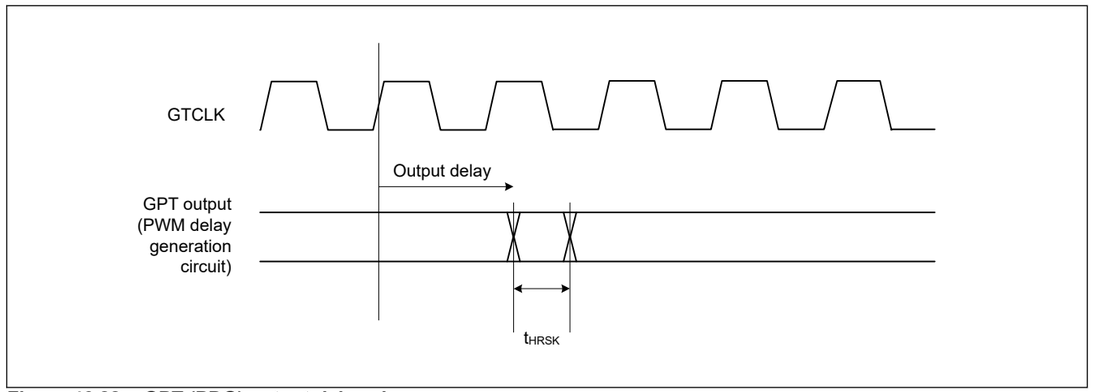


Figure 46.28 GPT (PDG) output delay skew

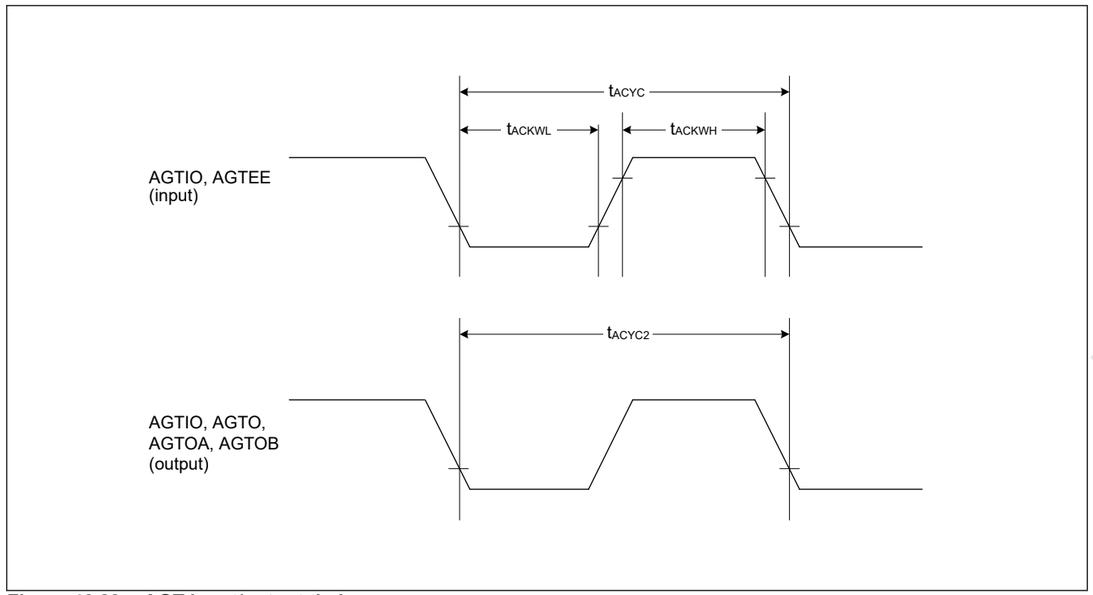


Figure 46.29 AGT input/output timing

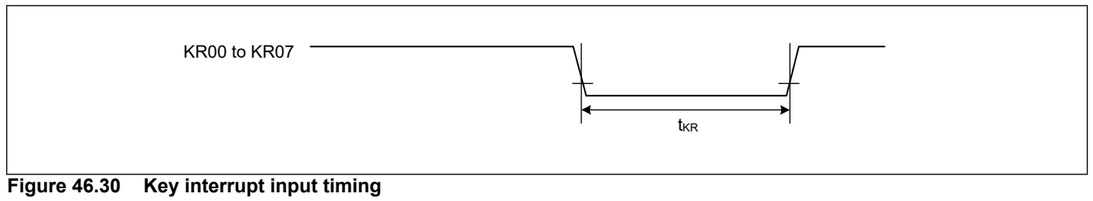


Figure 46.30 Key interrupt input timing

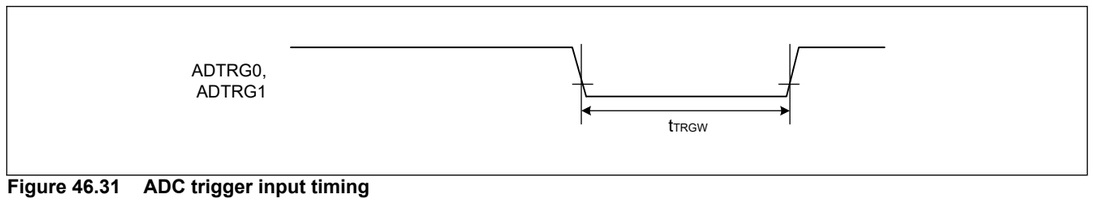


Figure 46.31 ADC trigger input timing

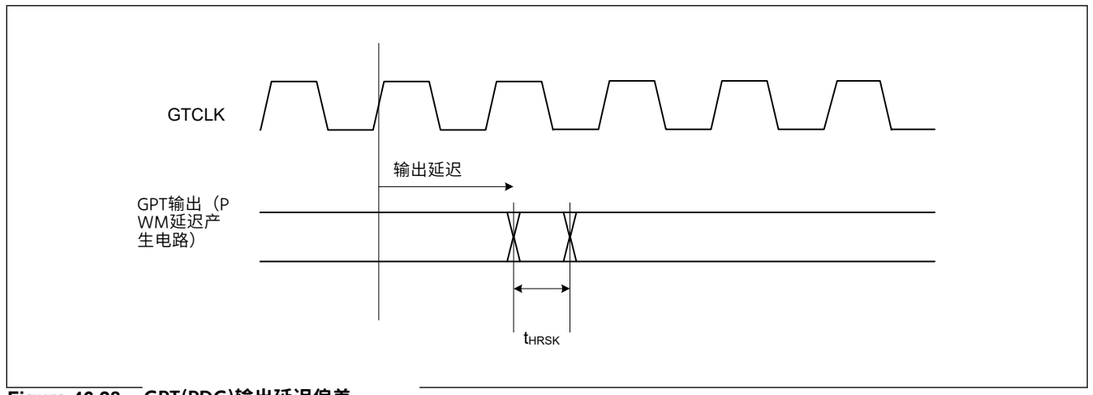


Figure 46.28 GPT(PDG)输出延迟偏差

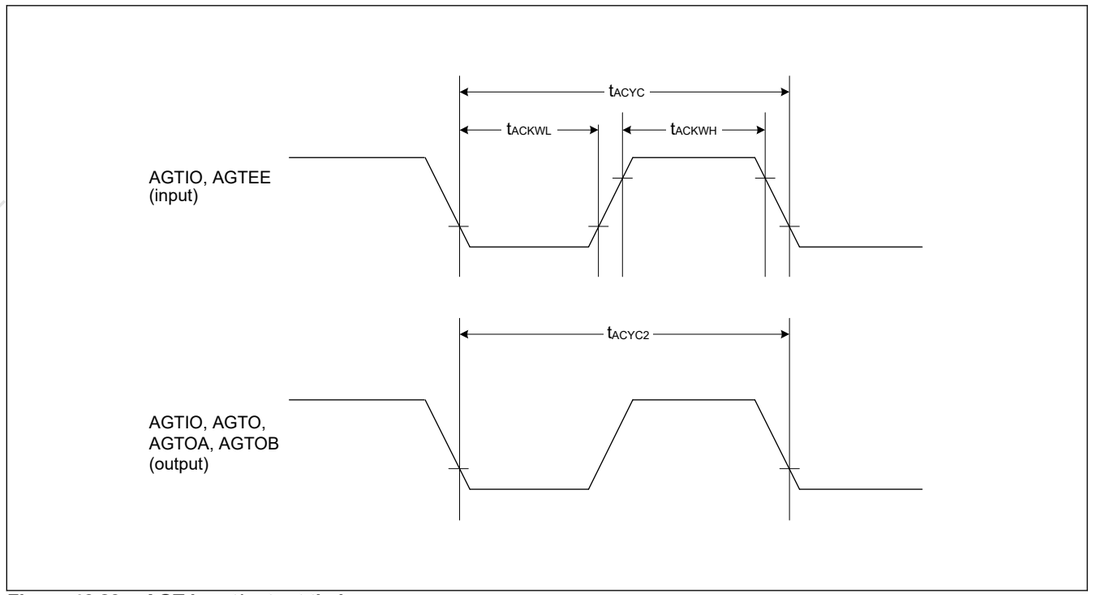


Figure 46.29 AGT input/output timing

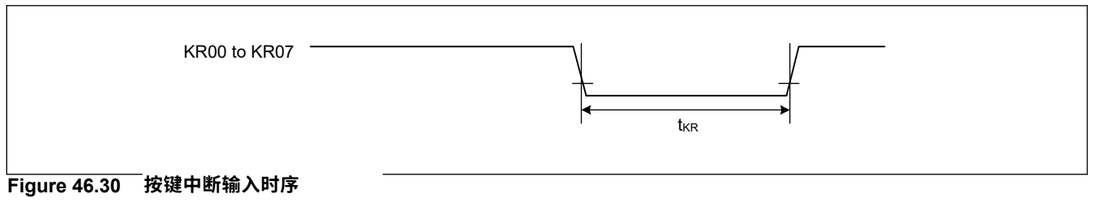


Figure 46.30 按键中断输入时序

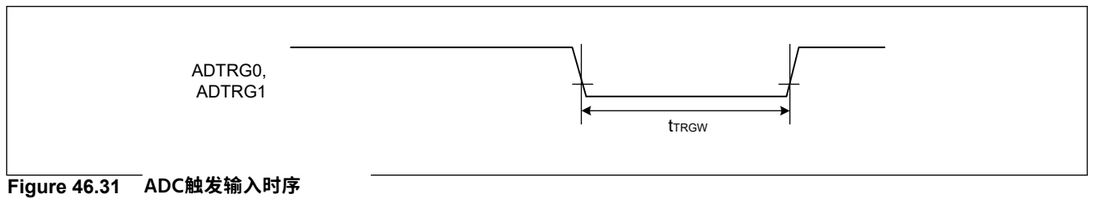


Figure 46.31 ADC触发输入时序

46.3.7 PDG Timing

Table 46.21 PDG timing

Parameter	Min	Typ	Max	Unit	Test conditions
Operation frequency	80	—	200	MHz	—
Resolution	—	156	—	ps	GPTCLK = 200 MHz
DNL*1	—	±2.0	—	LSB	—

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

46.3.8 CAC Timing

Table 46.22 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \le t_{cac}$*1	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	—	—	ns	—
		$t_{PBcyc} > t_{cac}$*1		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	—	—	ns	

Note: t_{PBcyc}: PCLKB cycle.
Note 1. t_{cac}: CAC count clock source cycle.

46.3.9 SCI Timing

Table 46.23 SCI timing (Asynchronous mode)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Note
Input clock cycle	t_{Scyc}	4	—	t_{Tcyc}	
Input clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}	
Input clock rise time	t_{SCKr}	—	5	ns	
Input clock fall time	t_{SCKf}	—	5	ns	
Output clock cycle	t_{Scyc}	6	—	t_{Tcyc}	
Output clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}	
Output clock rise time	t_{SCKr}	—	5	ns	
Output clock fall time	t_{SCKf}	—	5	ns	

Note: t_{Tcyc}: SCITCLK cycle.

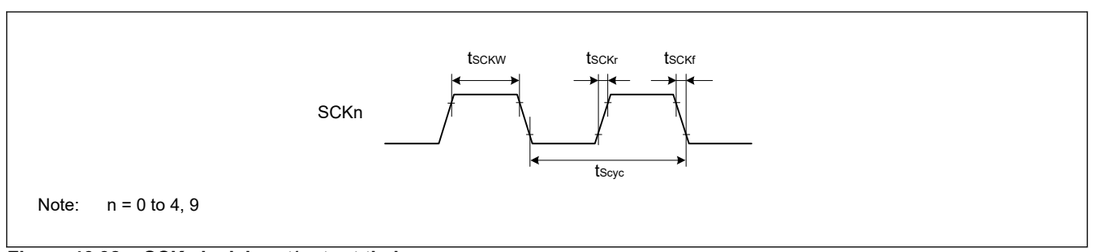


Figure 46.32 SCK clock input/output timing

Table 46.24 SCI timing (Simple SPI) (1 of 2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		High Speed/ Default	Symbol	Min	Max	Unit	Note
SCK clock cycle output	Master		t_{SPcyc}	2	65536	t_{Tcyc}	
SCK clock cycle input	Slave			2	—		

46.3.7 PDG Timing

Table 46.21 PDG timing

Parameter	Min	Typ	Max	Unit	测试条件
运行频率	80	—	200	MHz	—
Resolution	—	156	—	ps	GPTCLK = 200 MHz
DNL*1	—	±2.0	—	LSB	—

注1.该值将1-LSB分辨率中的行之间的差异归一化。

46.3.8 CAC时序

Table 46.22 CAC计时

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
CAC	CACREF输入脉冲宽度	$t_{PBcyc} \le t_{cac}$*1	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	—	—	ns	—
		$t_{PBcyc} > t_{cac}$*1		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	—	—	ns	

Note: t_{PBcyc}: PCLKB cycle.
注1.tcac：CAC计数时钟源周期。

46.3.9 SCI时序

Table 46.23 SCI时序（异步模式）

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter	Symbol	Min	Max	Unit	Note
输入时钟周期	t_{Scyc}	4	—	t_{Tcyc}	
输入时钟脉冲宽度	t_{SCKW}	0.4	0.6	t_{Scyc}	
输入时钟上升时间	t_{SCKr}	—	5	ns	
输入时钟下降时间	t_{SCKf}	—	5	ns	
输出时钟周期	t_{Scyc}	6	—	t_{Tcyc}	
输出时钟脉冲宽度	t_{SCKW}	0.4	0.6	t_{Scyc}	
输出时钟上升时间	t_{SCKr}	—	5	ns	
输出时钟下降时间	t_{SCKf}	—	5	ns	

Note: t_{Tcyc}: SCITCLK cycle.

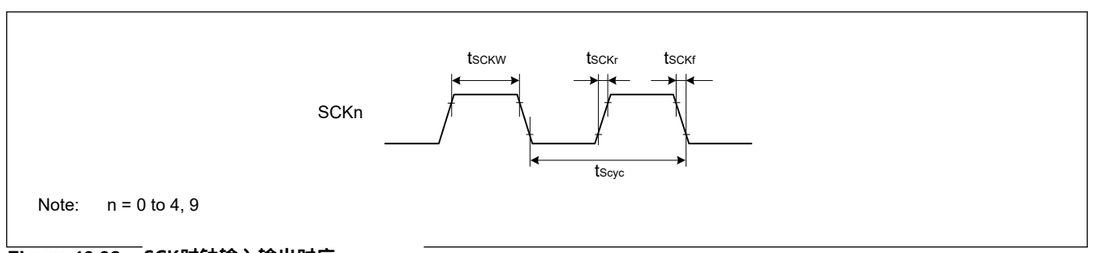


Figure 46.32 SCK时钟输入输出时序

Table 46.24 SCI时序(SimpleSPI)(1of2)

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter		High Speed/ Default	Symbol	Min	Max	Unit	Note
SCK时钟周期输出	Master		t_{SPcyc}	2	65536	t_{Tcyc}	
SCK时钟周期输入	Slave			2	—		

Table 46.24 SCI timing (Simple SPI) (2 of 2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		High Speed/ Default	Symbol	Min	Max	Unit	Note
SCK clock high pulse width	Master		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	Slave						
SCK clock low pulse width	Master		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	Slave						
SCK clock rise and fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns	
	Input			—	1	us	
Data input setup time	Master	High Speed*1	t_{SU}	1.7	—	ns	
		Default*2		3	—	ns	
	Slave			3.3	—	ns	
Data input hold time	Master	High Speed*1	t_H	12	—	ns	
		Default*2		14	—	ns	
	Slave			3	—	ns	
Data output delay	Master	High Speed*1	t_{OD}	—	5	ns	
		Default*2		—	7.3	ns	
	Slave	High Speed*1		—	15	ns	
		Default*2		—	21	ns	
Data output hold time	Master		t_{OH}	0	—	ns	
	Slave			0	—	ns	
Data rise and fall time	Output		t_{Dr}, t_{Df}	—	5	ns	
	Input			—	1	ns	
Slave access time			t_{SA}	—	5	t_{Tcyc}	
Slave output release time			t_{REL}	—	5	t_{Tcyc}	

Note: t_{Tcyc}: SCITCLK cycle.
Note 1. Must use pins that have a letter appended to their name, for instance _A, _B, _C, to indicate group membership. SCI0 is instance _A, SCI2 and SCI3 are instance _B, SCI1 and SCI9 are instance _C, SCI4 is instance _C and RXD is only PD14.
Note 2. All pins of group membership can be used.

Table 46.25 SCI timing (Simple SPI mode)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Note
SS input setup time	t_{LEAD}	1	—	t_{SPcyc}	
SS input hold time	t_{LAG}	1	—	t_{SPcyc}	
SS input rise and fall time	t_{SSLr}, t_{SSLf}	—	1	us	

Table 46.26 SCI timing (Clock synchronous mode) (1 of 2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		High Speed/ Default	Symbol	Min	Max	Unit	Note
SCK clock cycle output	Master		t_{SPcyc}	2	—	t_{Tcyc}	
SCK clock cycle input	Slave			2	—		
SCK clock high pulse width	Master		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	Slave						

Table 46.24 SCI时序(SimpleSPI)(2of2)

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter		High Speed/ Default	Symbol	Min	Max	Unit	Note
SCK时钟高脉冲宽度	Master		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	Slave						
SCK时钟低脉冲宽度	Master		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	Slave						
SCK时钟上升和下降时间	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns	
	Input			—	1	us	
数据输入建立时间	Master	高速*1	t_{SU}	1.7	—	ns	
		Default*2		3	—	ns	
	Slave			3.3	—	ns	
数据输入保持时间	Master	高速*1	t_H	12	—	ns	
		Default*2		14	—	ns	
	Slave			3	—	ns	
数据输出延迟	Master	高速*1	t_{OD}	—	5	ns	
		Default*2		—	7.3	ns	
	Slave	高速*1		—	15	ns	
		Default*2		—	21	ns	
数据输出保持时间	Master		t_{OH}	0	—	ns	
	Slave			0	—	ns	
数据上升和下降时间	Output		t_{Dr}, t_{Df}	—	5	ns	
	Input			—	1	ns	
从站访问时间			t_{SA}	—	5	t_{Tcyc}	
从机输出释放时间			t_{REL}	—	5	t_{Tcyc}	

Note: t_{Tcyc}: SCITCLK cycle.
注1.必须使用名称后附有字母的引脚，例如_A、_B、_C，以表示组成员身份。SCI0是实例_A，SCI2和SCI3是实例_B，SCI1和SCI9是实例_C，SCI4是实例_C，RXD只有PD14。
注2.可以使用组成员的所有引脚。

Table 46.25 SCI时序（简单SPI模式）

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter	Symbol	Min	Max	Unit	Note
SS输入建立时间	t_{LEAD}	1	—	t_{SPcyc}	
SS输入保持时间	t_{LAG}	1	—	t_{SPcyc}	
SS输入上升和下降时间	t_{SSLr}, t_{SSLf}	—	1	us	

Table 46.26 SCI时序（时钟同步模式）（1of2）

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter		High Speed/ Default	Symbol	Min	Max	Unit	Note
SCK时钟周期输出	Master		t_{SPcyc}	2	—	t_{Tcyc}	
SCK时钟周期输入	Slave			2	—		
SCK时钟高脉冲宽度	Master		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	Slave						

Table 46.26 SCI timing (Clock synchronous mode) (2 of 2)

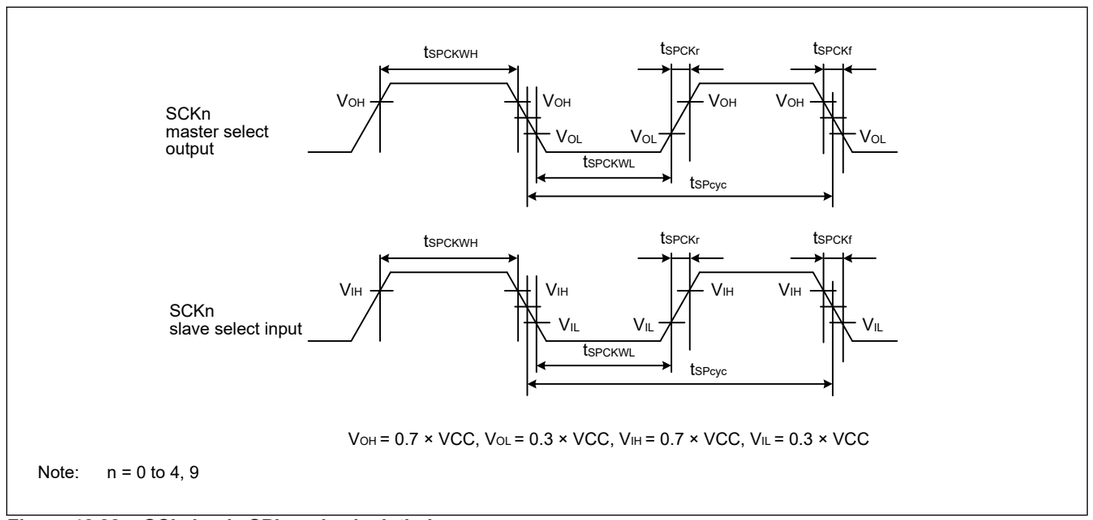
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		High Speed/ Default	Symbol	Min	Max	Unit	Note
SCK clock low pulse width	Master		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	Slave						
SCK clock rise and fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns	
	Input						
Data input setup time	Master	High Speed*1	t_{SU}	2.6	—	ns	
		Default*2		2.8	—	ns	
	Slave			3.3		ns	
Data input hold time	Master	High Speed*1	t_H	12	—	ns	
		Default*2		14	—	ns	
	Slave			3		ns	
Data output delay	Master	High Speed*1	t_{OD}	—	5	ns	
		Default*2		—	7.3	ns	
	Slave	High Speed*1		—	15	ns	
		Default*2		—	21	ns	
Data output hold time	Master		t_{OH}	0	—	ns	
	Slave			0	—	ns	
Data rise and fall time	Output		t_{Dr}, t_{Df}	—	5	ns	
	Input			—	5	ns	

Note: t_{Tcyc}: SCITCLK cycle.

Note 1. Must use pins that have a letter appended to their name, for instance _A, _B, _C, to indicate group membership. SCI0 is instance _A, SCI2 and SCI3 are instance _B, SCI1 and SCI9 are instance _C, SCI4 is instance _C and RXD is only PD14.

Note 2. All pins of group membership can be used.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Note: n = 0 to 4, 9

Figure 46.33 SCI simple SPI mode clock timing

Table 46.26 SCI时序（时钟同步模式）(2of2)

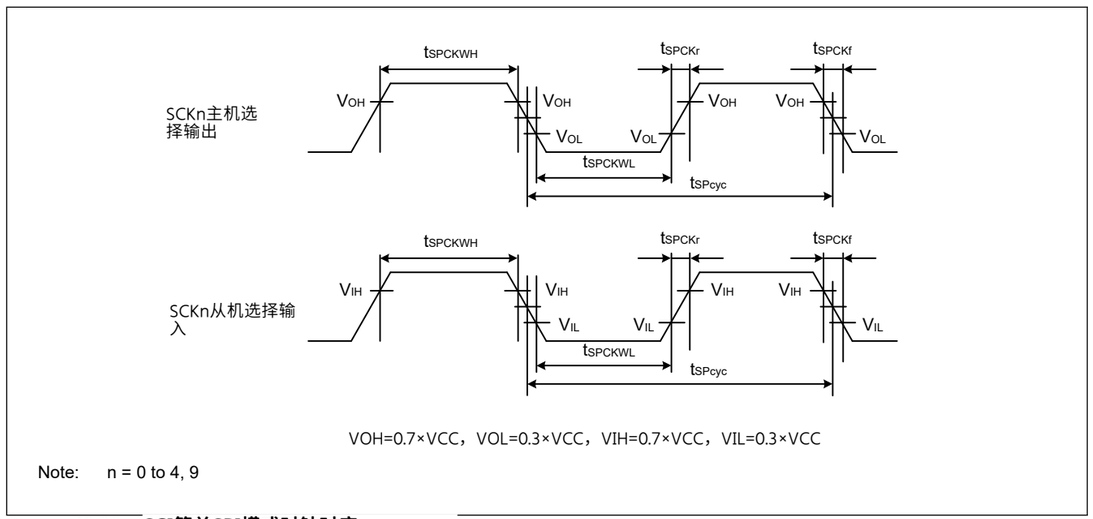
条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter		High Speed/ Default	Symbol	Min	Max	Unit	Note
SCK时钟低脉冲宽度	Master		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	Slave						
SCK时钟上升和下降时间	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns	
	Input						
数据输入建立时间	Master	高速*1	t_{SU}	2.6	—	ns	
		Default*2		2.8	—	ns	
	Slave			3.3		ns	
数据输入保持时间	Master	高速*1	t_H	12	—	ns	
		Default*2		14	—	ns	
	Slave			3		ns	
数据输出延迟	Master	高速*1	t_{OD}	—	5	ns	
		Default*2		—	7.3	ns	
	Slave	高速*1		—	15	ns	
		Default*2		—	21	ns	
数据输出保持时间	Master		t_{OH}	0	—	ns	
	Slave			0	—	ns	
数据上升和下降时间	Output		t_{Dr}, t_{Df}	—	5	ns	
	Input			—	5	ns	

Note: t_{Tcyc}: SCITCLK cycle.

注1.必须使用名称后附有字母的引脚，例如_A、_B、_C，以表示组成员身份。SCI0是实例_A，SCI2和SCI3是实例_B，SCI1和SCI9是实例_C，SCI4是实例_C，RXD只有PD14。

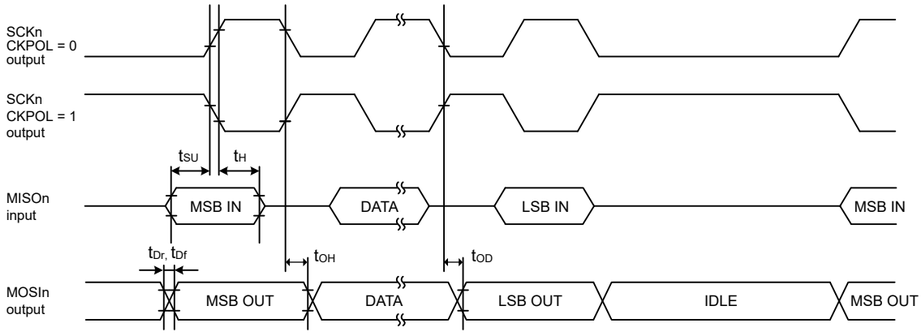
注2.可以使用组成员的所有引脚。



VOH=0.7×VCC，VOL=0.3×VCC，VIH=0.7×VCC，VIL=0.3×VCC

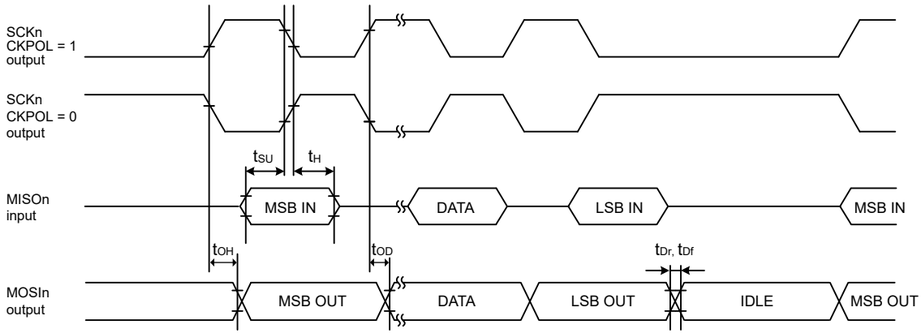
Note: n = 0 to 4, 9

Figure 46.33 SCI简单SPI模式时钟时序



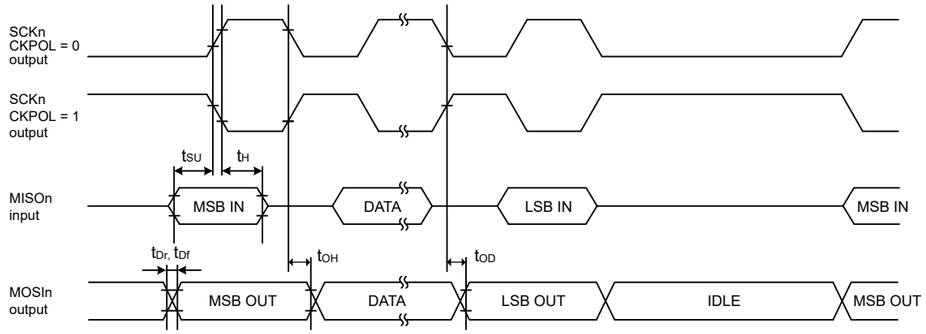
Note: n = 0 to 4, 9

Figure 46.34 SCI simple SPI mode timing for master when CKPH = 1



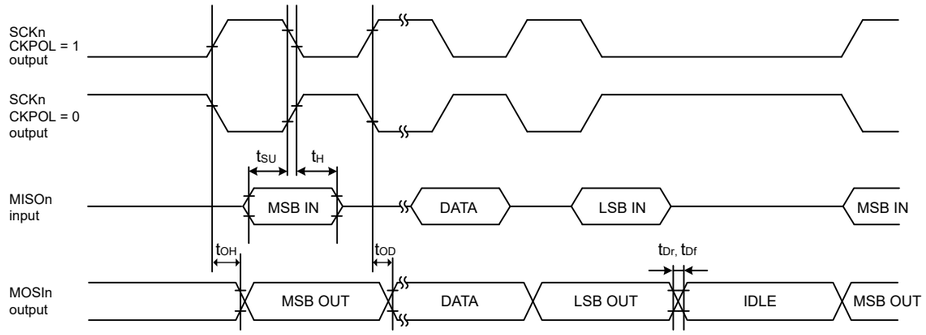
Note: n = 0 to 4, 9

Figure 46.35 SCI simple SPI mode timing for master when CKPH = 0



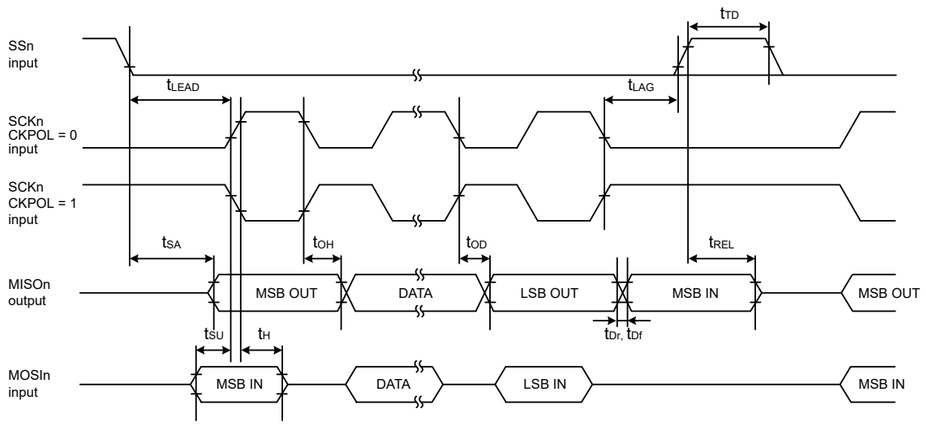
Note: n = 0 to 4, 9

Figure 46.34 CKPH=1时主机的SCI简单SPI模式时序



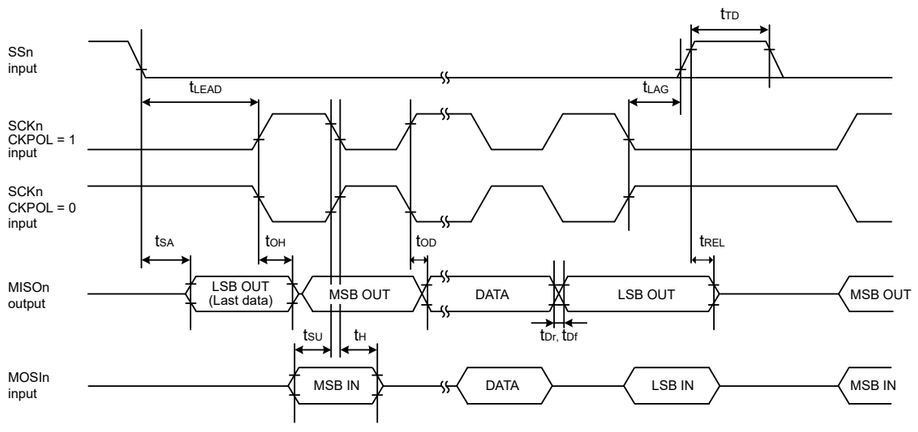
Note: n = 0 to 4, 9

Figure 46.35 CKPH=0时主机的SCI简单SPI模式时序



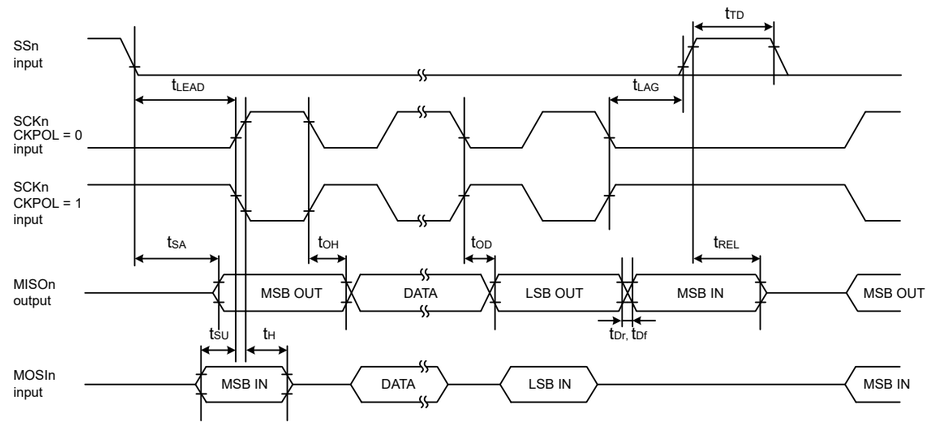
Note: n = 0 to 4, 9

Figure 46.36 SCI simple SPI mode timing for slave when CKPH = 1



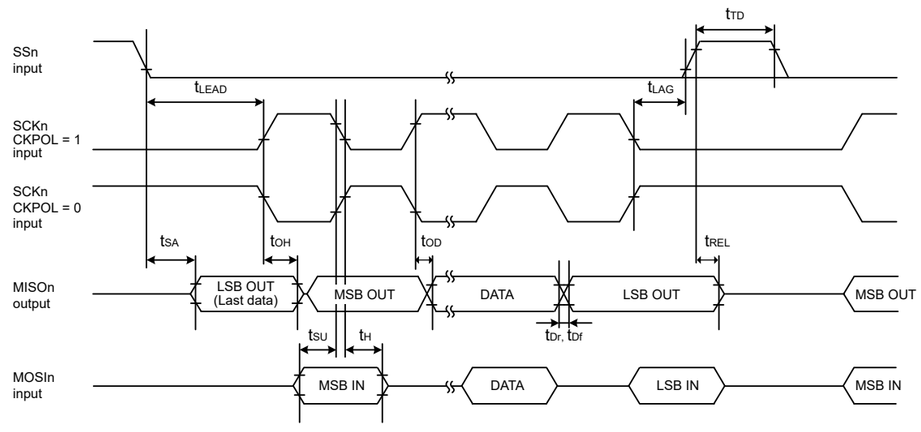
Note: n = 0 to 4, 9

Figure 46.37 SCI simple SPI mode timing for slave when CKPH = 0



Note: n = 0 to 4, 9

Figure 46.36 CKPH=1时从机的SCI简单SPI模式时序



Note: n = 0 to 4, 9

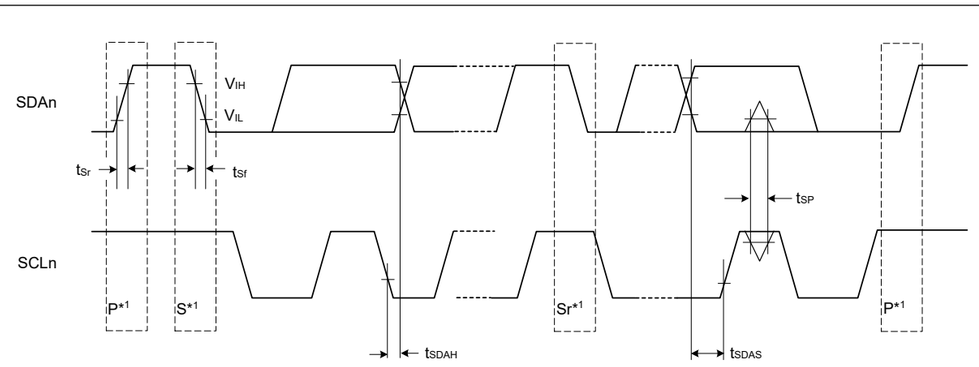
Figure 46.37 CKPH=0时从机的SCI简单SPI模式时序

Table 46.27 SCI timing (Simple IIC mode)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Note
Simple IIC (Standard mode)	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{Tcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast mode)	SCL, SDA input rise time	t_{Sr}	—	300	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{Tcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: t_{Tcyc}: SCITCLK cycle.
Note 1. Cb indicates the total capacity of the bus line.



Test conditions:
$V_{IH} = V_{CC} \times 0.7$, $V_{IL} = V_{CC} \times 0.3$
$V_{OL} = 0.6$ V, $I_{OL} = 6$ mA (ICFER.FMPE = 0)
$V_{OL} = 0.4$ V, $I_{OL} = 20$ mA (ICFER.FMPE = 1)

Note: n = 0 to 4, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

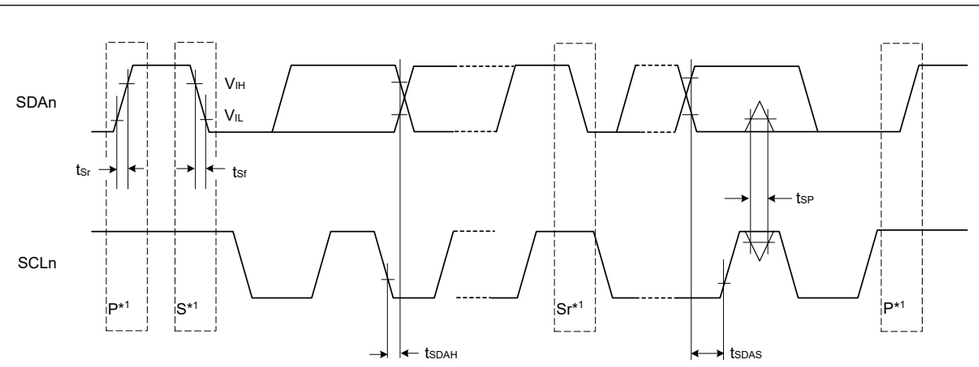
Figure 46.38 SCI simple IIC mode timing

Table 46.27 SCI时序（简单IIC模式）

条件：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	Note
Simple IIC (Standard mode)	SCL、SDA输入上升时间	t_{Sr}	—	1000	ns	
	SCL、SDA输入下降时间	t_{Sf}	—	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{Tcyc}	ns	
	数据输入建立时间	t_{SDAS}	250	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast mode)	SCL、SDA输入上升时间	t_{Sr}	—	300	ns	
	SCL、SDA输入下降时间	t_{Sf}	—	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{Tcyc}	ns	
	数据输入建立时间	t_{SDAS}	100	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: t_{Tcyc}: SCITCLK cycle.
注1.Cb表示总线的总容量。



Test conditions:
VIH=VCC×0.7，VIL=VCC×0.3
VOL=0.6V，IOL=6mA(ICFER.FMPE=0)VOL=0
.4V，IOL=20mA(ICFER.FMPE=1)

Note: n = 0 to 4, 9
注1.S、P和Sr表示以下条件：
S：开始条件P：
停止条件
Sr：重启条件

Figure 46.38 SCI简单IIC模式时序

46.3.10 SPI Timing

Table 46.28 SPI timing (1 of 2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		High Speed/ Default	Symbol	VCC = 3.0 to 3.6 V, C = 15 pF		VCC = 2.7 to 3.6 V, C = 30 pF		Unit	Note
				Min	Max	Min	Max		
RSPCK clock cycle	Master		t_{SPcyc}	2	4096	2	4096	t_{Tcyc}	
	Slave			2	—	2	—		
RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
	Slave			0.4	0.6	0.4	0.6	t_{SPcyc}	
RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
	Slave			0.4	0.6	0.4	0.6	t_{SPcyc}	
RSPCK clock rise and fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	—	5	ns	
	Input			—	1	—	1	µs	
Data input setup time	Master	High Speed*1	t_{SU}	0	—	—	—	ns	
		Default*2		—	—	1.3	—	ns	
	Slave			2.5	—	2.7	—	ns	
Data input hold time	Master	High Speed*1	t_H	6.2	—	—	—	ns	
		Default*2		—	—	8	—	ns	
	Slave			2.5	—	2.5	—	ns	
SSL setup time	Master		t_{LEAD}	1	8	1	8	t_{SPcyc}	
	Slave			6	—	6	—	t_{Tcyc}	
SSL hold time	Master		t_{LAG}	1	8	1	8	t_{SPcyc}	
	Slave			6	—	6	—	t_{Tcyc}	
TI SSP SS input setup time	Slave		t_{TISS}	2.5	—	2.8	—	ns	
TI SSP SS input hold time	Slave		t_{TISH}	2.5	—	2.5	—	ns	
TI SSP next-access time	Slave		t_{TIND}	$2 \times t_{Tcyc} + SLNDL \times t_{Tcyc}$	—	$2 \times t_{Tcyc} + SLNDL \times t_{Tcyc}$	—	ns	
TI SSP master SS output delay	Master		t_{TISSOD}	—	8.9	—	8.9	ns	

46.3.10 SPI时序

Table 46.28 SPI时序（1of2）

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter		High Speed/ Default	Symbol	VCC = 3.0 to 3.6 V, C = 15 pF		VCC = 2.7 to 3.6 V, C = 30 pF		Unit	Note
				Min	Max	Min	Max		
RSPCK时钟周期	Master		t_{SPcyc}	2	4096	2	4096	t_{Tcyc}	
	Slave			2	—	2	—		
RSPCK时钟高脉冲宽度	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
	Slave			0.4	0.6	0.4	0.6	t_{SPcyc}	
RSPCK时钟低脉冲宽度	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
	Slave			0.4	0.6	0.4	0.6	t_{SPcyc}	
RSPCK时钟上升和下降时间	Output		t_{SPCKr}, t_{SPCKf}	—	5	—	5	ns	
	Input			—	1	—	1	µs	
数据输入建立时间	Master	High Speed*1	t_{SU}	0	—	—	—	ns	
		Default*2		—	—	1.3	—	ns	
	Slave			2.5	—	2.7	—	ns	
数据输入保持时间	Master	High Speed*1	t_H	6.2	—	—	—	ns	
		Default*2		—	—	8	—	ns	
	Slave			2.5	—	2.5	—	ns	
SSL设置时间	Master		t_{LEAD}	1	8	1	8	t_{SPcyc}	
	Slave			6	—	6	—	t_{Tcyc}	
SSL保持时间	Master		t_{LAG}	1	8	1	8	t_{SPcyc}	
	Slave			6	—	6	—	t_{Tcyc}	
TISSPSS输入建立时间	Slave		t_{TISS}	2.5	—	2.8	—	ns	
TISSPSS输入保持时间	Slave		t_{TISH}	2.5	—	2.5	—	ns	
TISSP下次访问时间	Slave		t_{TIND}	$2 \times t_{Tcyc} + SLNDL \times t_{Tcyc}$	—	$2 \times t_{Tcyc} + SLNDL \times t_{Tcyc}$	—	ns	
TISSP主控SS输出延迟	Master		t_{TISSOD}	—	8.9	—	8.9	ns	

Table 46.28 SPI timing (2 of 2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		High Speed/ Default	Symbol	VCC = 3.0 to 3.6 V, C = 15 pF		VCC = 2.7 to 3.6 V, C = 30 pF		Unit	Note
				Min	Max	Min	Max		
Data output delay time	Master	High Speed*1	t_{OD}	—	4.6	—	—	ns	
		Default*2		—	—	—	7	ns	
	Slave	High Speed*1		—	14	—	—	ns	
		Default*2		—	—	—	21	ns	
Data output hold time	Master		t_{OH}	0	—	0	—	ns	
	Slave			0	—	0	—	ns	
Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Tcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	$t_{SPcyc} + 2 \times t_{Tcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
	Slave			t_{Tcyc}	—	t_{Tcyc}	—	ns	
MOSI and MISO rise and fall time	Output		t_{Dr}	—	5	—	5	ns	
	Input		t_{Df}	—	1	—	1	µs	
SSL rise and fall time	Output		t_{SSLr}	—	5	—	5	ns	
	Input		t_{SSLf}	—	1	—	1	µs	
Slave access time	Slave		t_{SA}	—	20	—	20	ns	
Slave output release time	Slave		t_{REL}	—	20	—	20	ns	

Note: t_{Tcyc}: PCLKA or SCISPICLK cycle.

Note 1. Must use pins that have a letter appended to their name, for instance _A, _B, _C, to indicate group membership. SPIA is instance _B, SPIB is instance _A.

Note 2. All pins of group membership can be used.

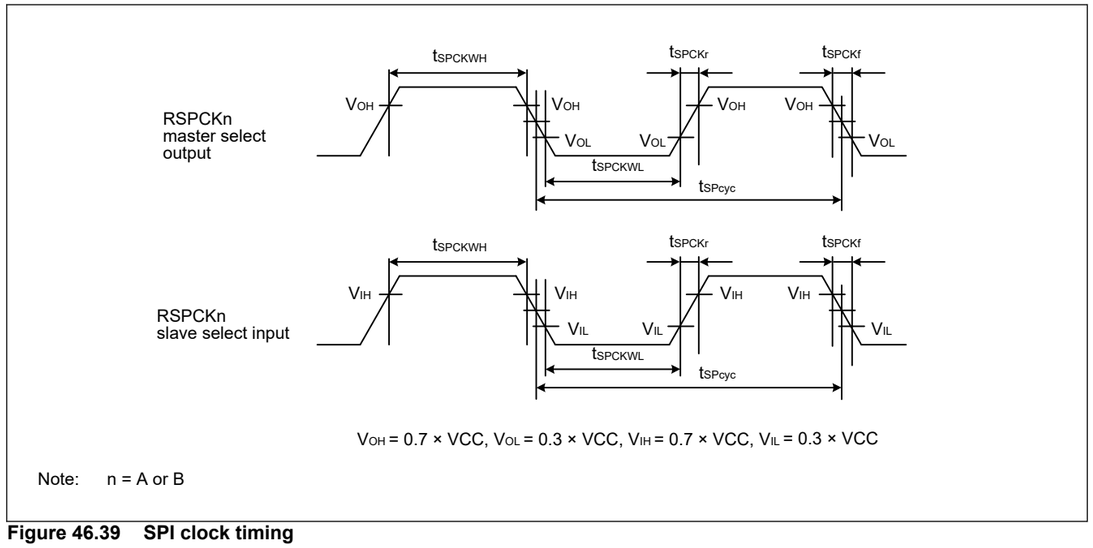


Figure 46.39 SPI clock timing

Table 46.28 SPI时序（2之2）

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter		High Speed/ Default	Symbol	VCC = 3.0 to 3.6 V, C = 15 pF		VCC = 2.7 to 3.6 V, C = 30 pF		Unit	Note
				Min	Max	Min	Max		
数据输出延迟时间	Master	High Speed*1	t_{OD}	—	4.6	—	—	ns	
		Default*2		—	—	—	7	ns	
	Slave	High Speed*1		—	14	—	—	ns	
		Default*2		—	—	—	21	ns	
数据输出保持时间	Master		t_{OH}	0	—	0	—	ns	
	Slave			0	—	0	—	ns	
连续传输延迟时间	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Tcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	$t_{SPcyc} + 2 \times t_{Tcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
	Slave			t_{Tcyc}	—	t_{Tcyc}	—	ns	
MOSI和MISO上升和下降时间	Output		t_{Dr}	—	5	—	5	ns	
	Input		t_{Df}	—	1	—	1	µs	
SSL上升和下降时间	Output		t_{SSLr}	—	5	—	5	ns	
	Input		t_{SSLf}	—	1	—	1	µs	
从站访问时间	Slave		t_{SA}	—	20	—	20	ns	
从机输出释放时间	Slave		t_{REL}	—	20	—	20	ns	

Note: tTcyc：PCLKA或SCISPICLK周期。

注1.必须使用名称后附有字母的引脚，例如_A、_B、_C，以表示组成员身份。SPIA是实例_B，SPIB是实例_A。

注2.可以使用组成员的所有引脚。

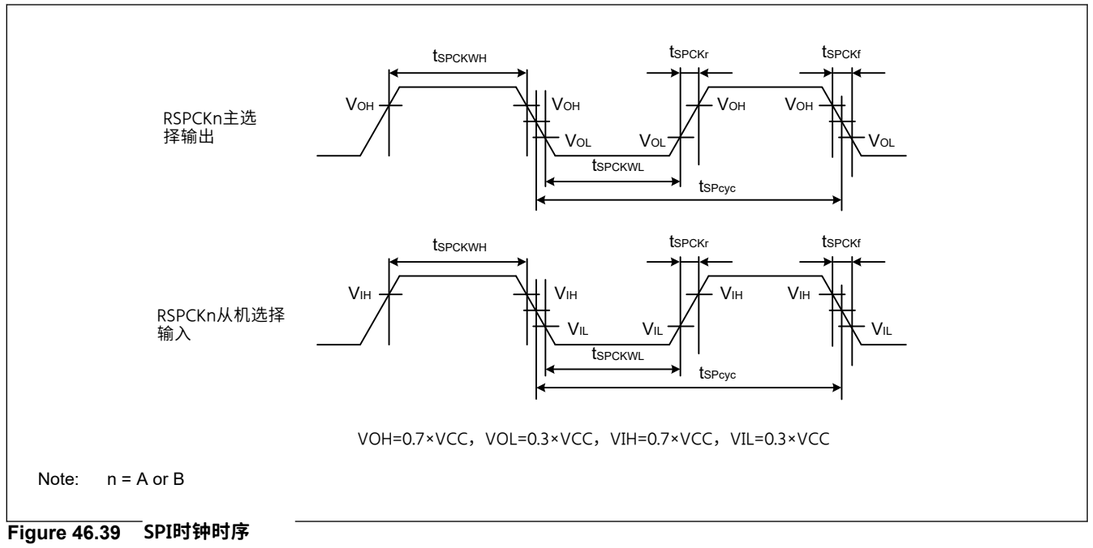


Figure 46.39 SPI时钟时序

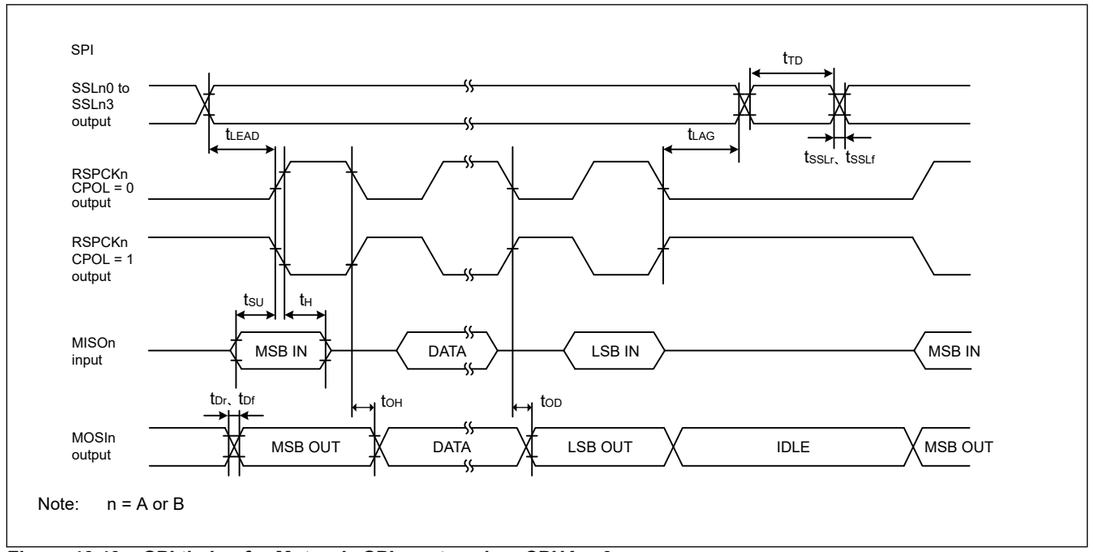


Figure 46.40 SPI timing for Motorola SPI master when CPHA = 0

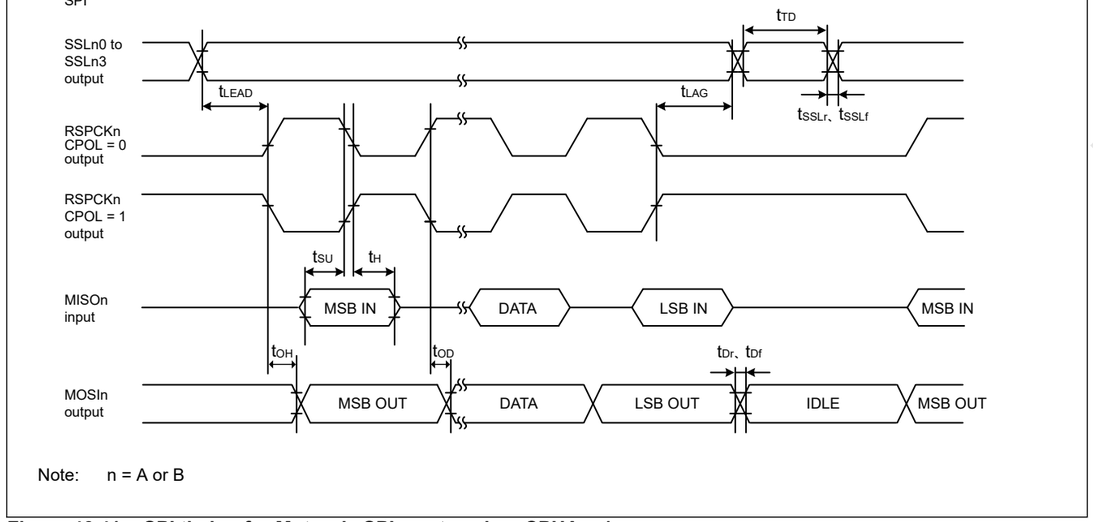


Figure 46.41 SPI timing for Motorola SPI master when CPHA = 1

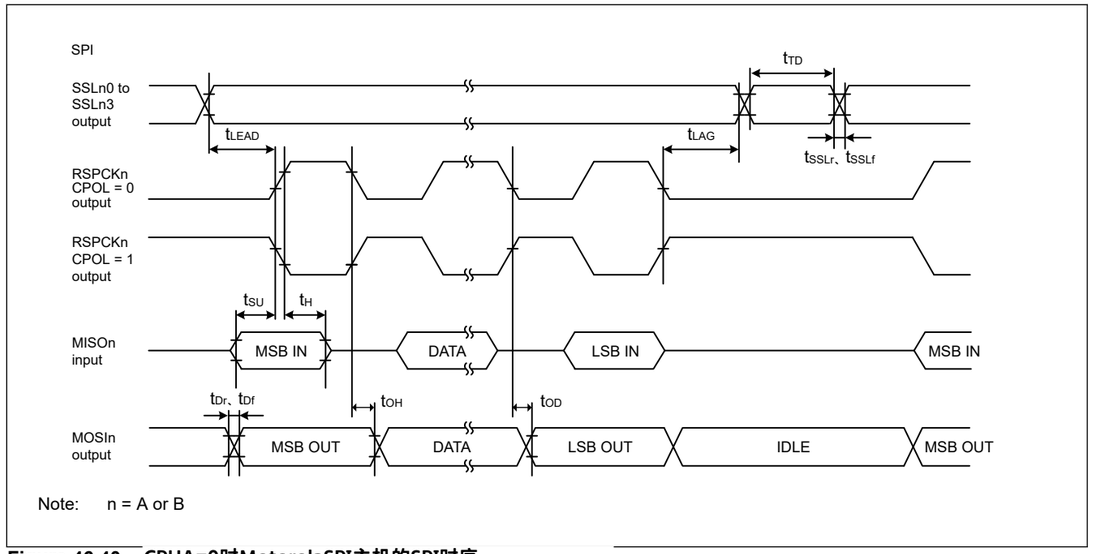


Figure 46.40 CPHA=0时MotorolaSPI主机的SPI时序

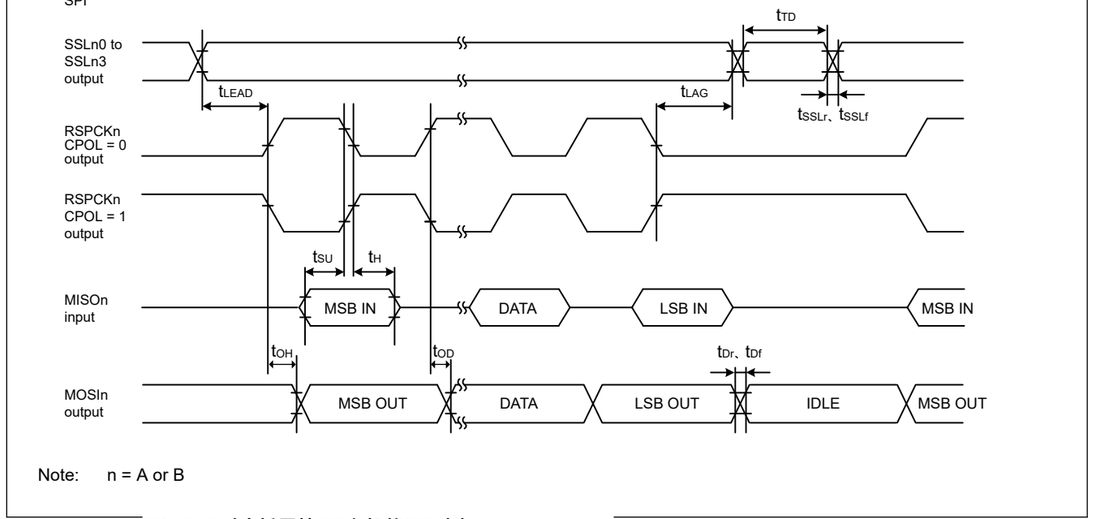


Figure 46.41 CPHA=1时摩托罗拉SPI主机的SPI时序

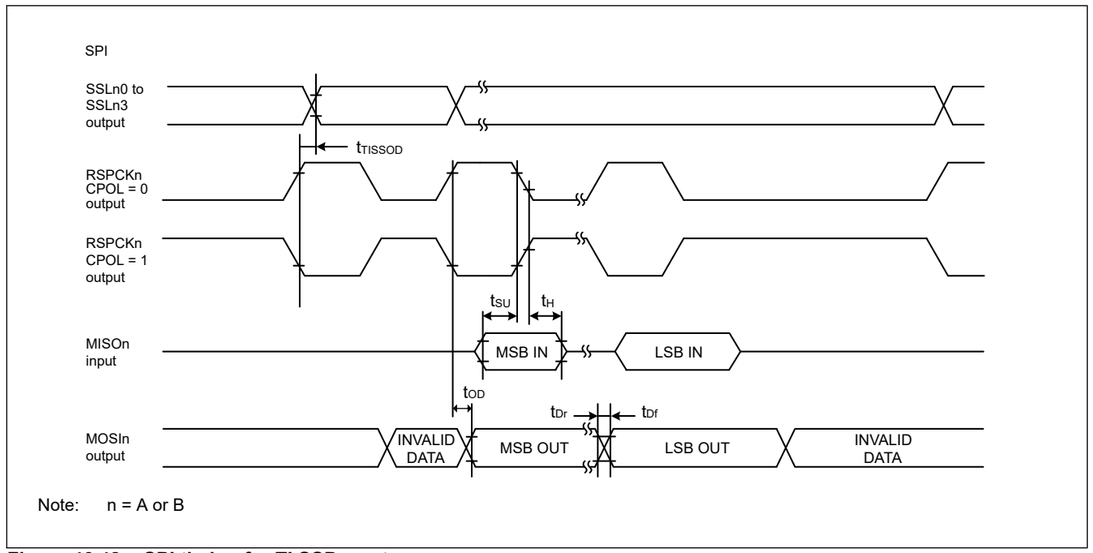


Figure 46.42 SPI timing for TI SSP master

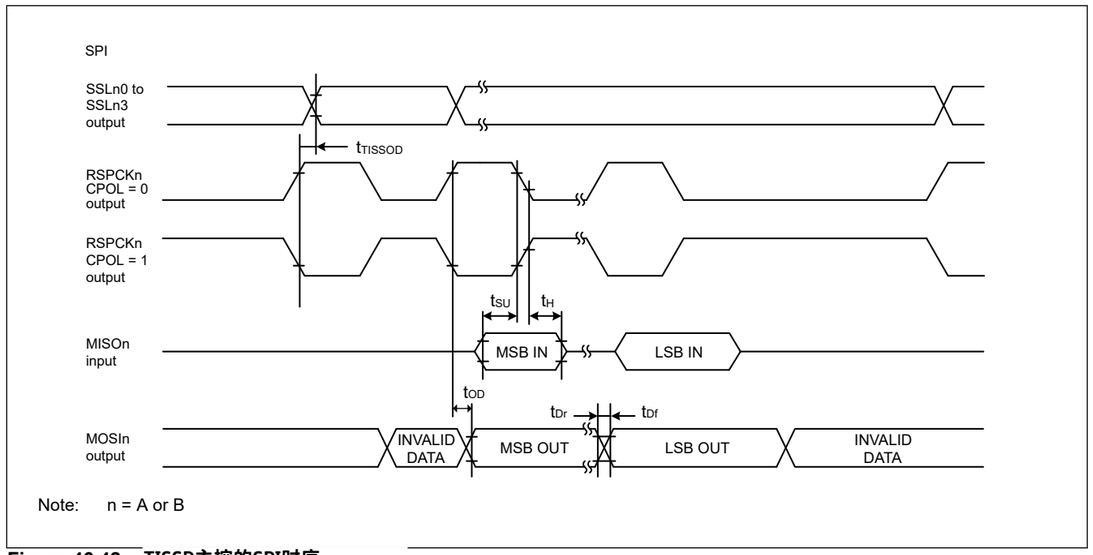


Figure 46.42 TISSP主控的SPI时序

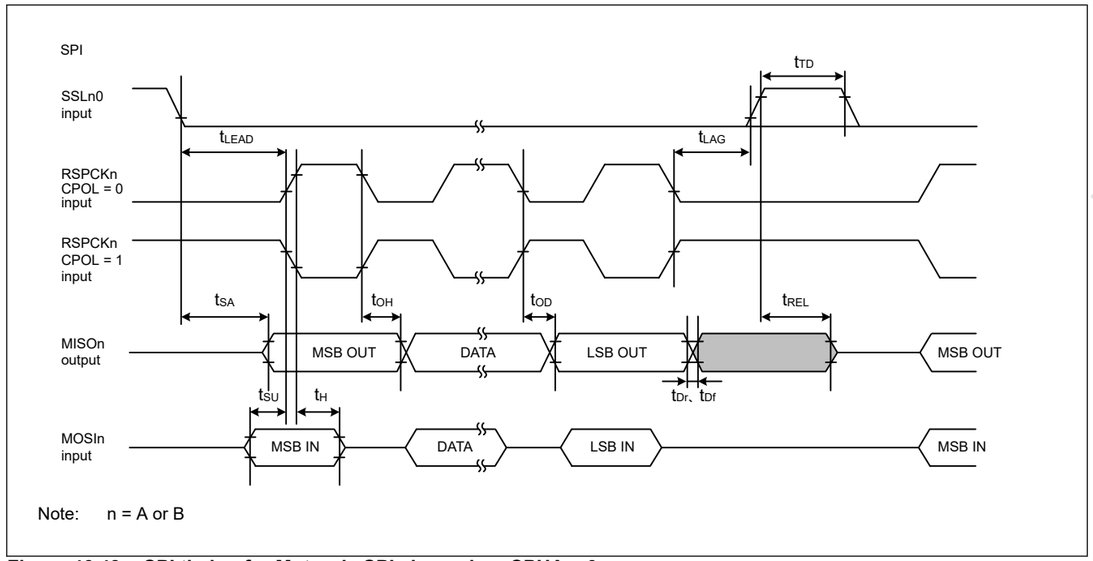


Figure 46.43 SPI timing for Motorola SPI slave when CPHA = 0

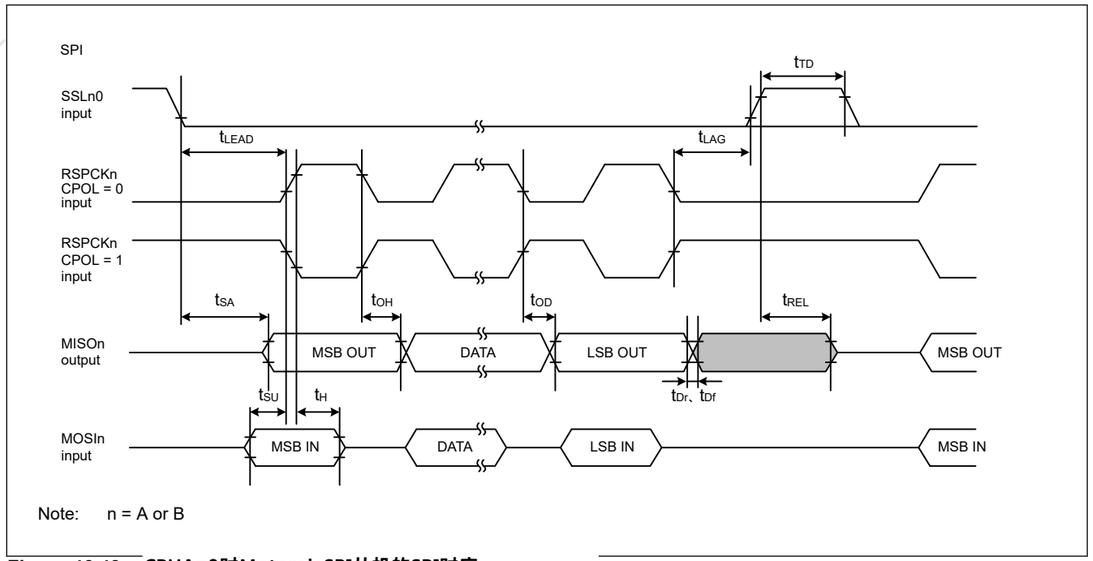
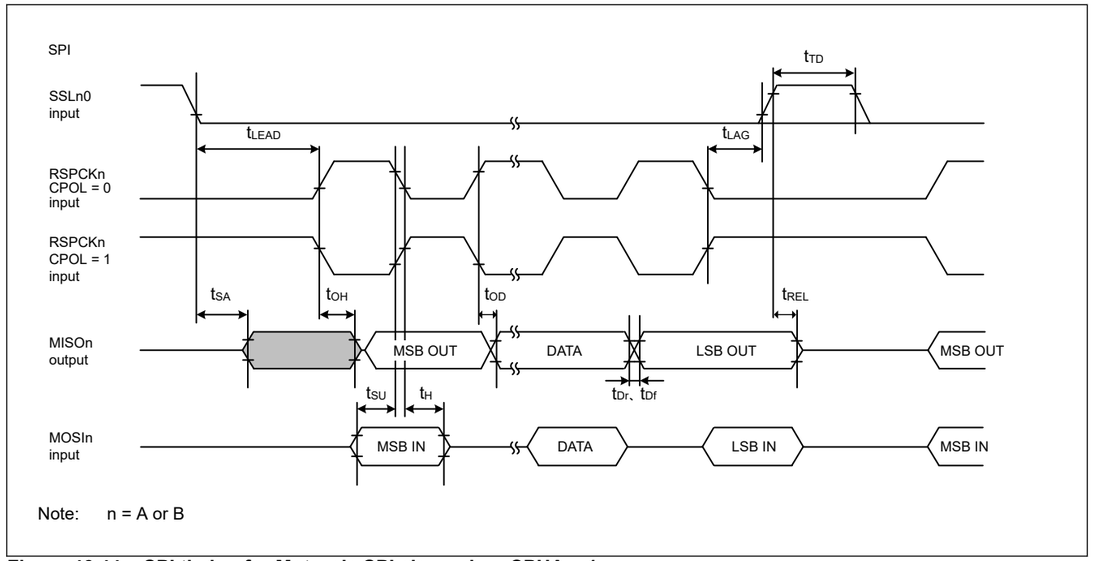


Figure 46.43 CPHA=0时MotorolaSPI从机的SPI时序



Note: n = A or B

Figure 46.44 SPI timing for Motorola SPI slave when CPHA = 1

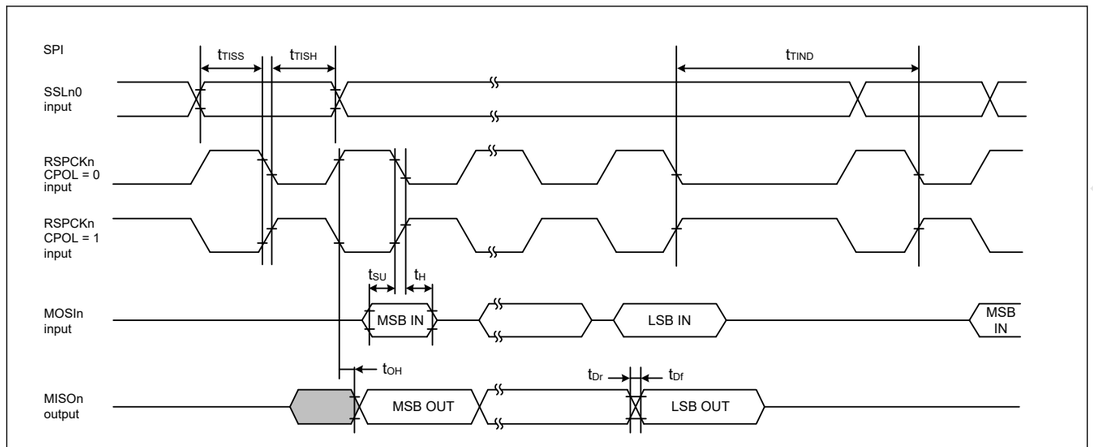
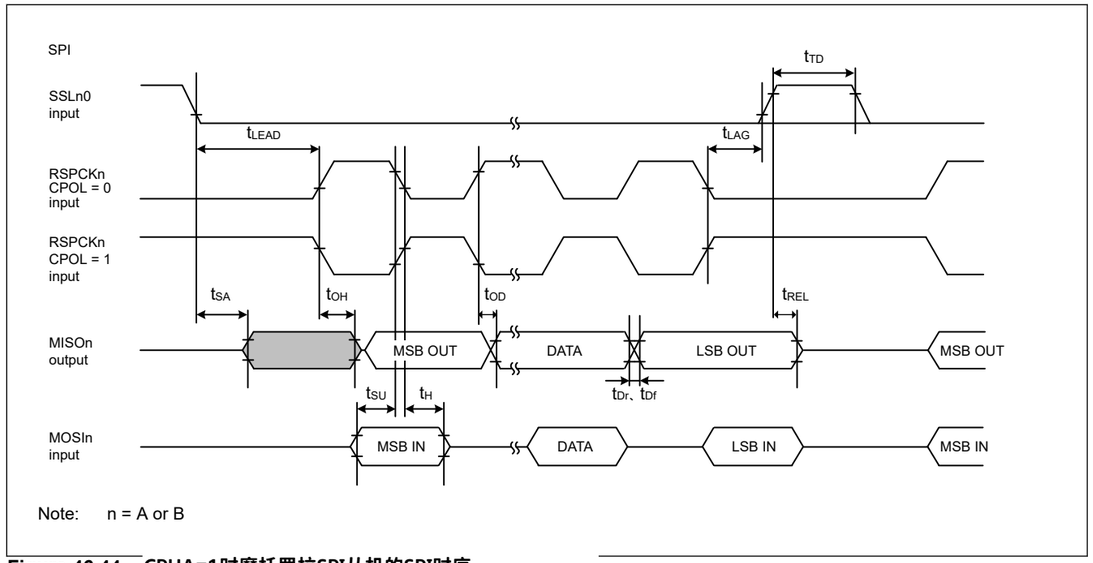


Figure 46.45 SPI timing for TI SSP slave when transmit with delay between frames



Note: n = A or B

Figure 46.44 CPHA=1时摩托罗拉SPI从机的SPI时序

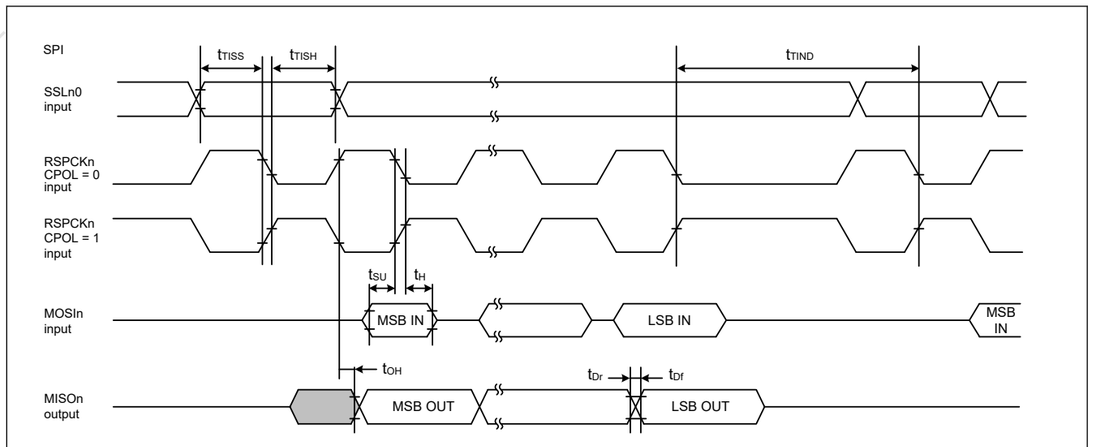


Figure 46.45 TISSP从机在帧间延迟传输时的SPI时序

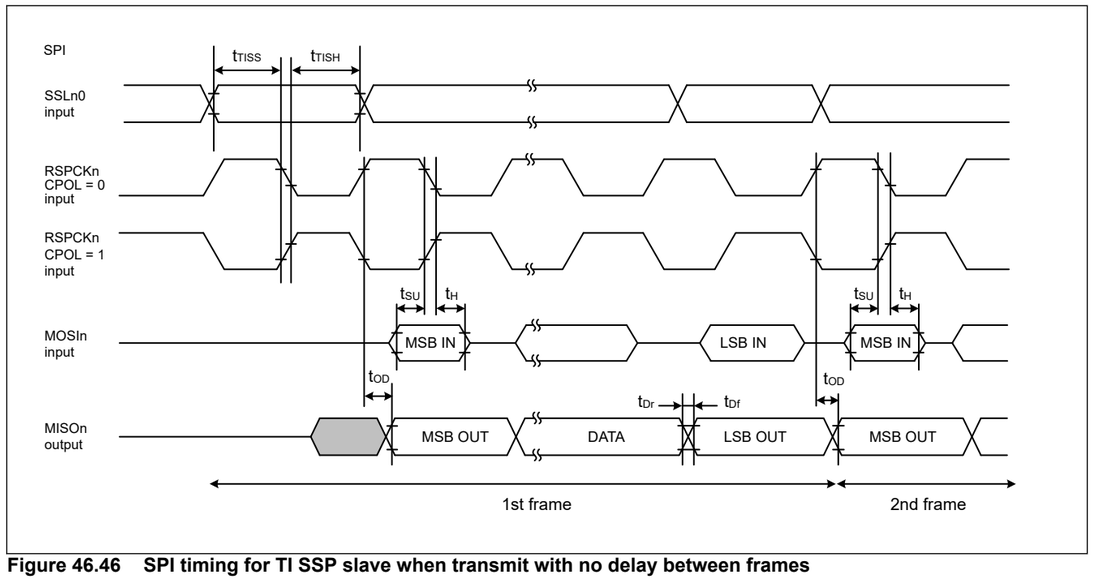


Figure 46.46 SPI timing for TI SSP slave when transmit with no delay between frames

46.3.11 IIC Timing

Table 46.29 IIC timing (1)-1

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_B, SCL1_B, SCL0_C, SDA0_C, SCL0_D, SDA0_D, SCL0_E, SDA0_E, SCL0_F, SDA0_F, SCL1_C, SDA1_C, SCL1_D, SDA1_D, SCL1_E, SDA1_E.
(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL1_A, SDA1_A.
(3) Use pins that have a letter appended to their names, for instance _A or _B or _C or _D or _E or _F, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit	Test conditions
IIC (Standard mode, SMBus) BFCTL.FMPE = 0	SCL input cycle time	t_{SCL}	10 (18) × t_{IICcyc} + 1300	—	ns	Figure 46.47
	SCL input high pulse width	t_{SCLH}	5 (9) × t_{IICcyc}	—	ns	
	SCL input low pulse width	t_{SCLL}	5 (9) × t_{IICcyc}	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	5 (9) × t_{IICcyc} + 300	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *1	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.

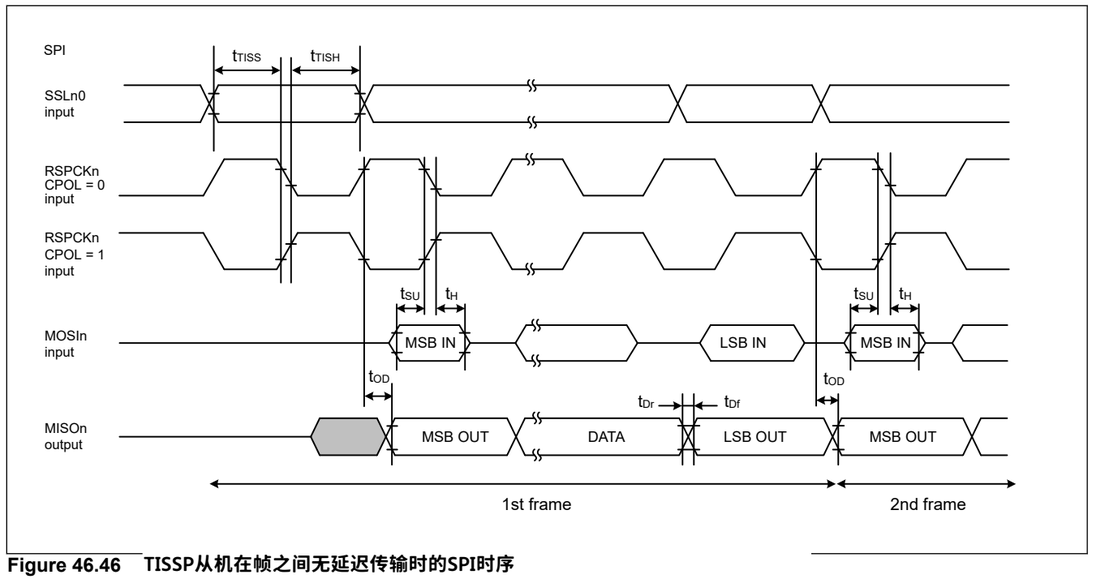


Figure 46.46 TISSP从机在帧之间无延迟传输时的SPI时序

46.3.11 IIC Timing

Table 46.29 IIC timing (1)-1

(1)条件：在PmnPFS寄存器的PortDriveCapability位为以下引脚选择中间驱动输出：SDA0_B、SCL0_B、SDA1_B、SCL1_B、SCL0_C、SDA0_C、SCL0_D、SDA0_D、SCL0_E、SDA0_E、SCL0_F、SDA0_F、SCL1_C SDA1_C SCL1_D SDA1_D、SCL1_E、SDA1_E。(2)以下引脚不需要设置：SCL0_A、SDA0_A、SCL1_A、SDA1_A。(3)使用名称后附有字母的引脚，例如_A或_B或_C或_D或_E或_F，以表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

Parameter		Symbol	Min	Max	Unit	测试条件
IIC (Standard mode, SMBus) BFCTL.FMPE = 0	SCL输入周期时间	t_{SCL}	10 (18) × t_{IICcyc} + 1300	—	ns	Figure 46.47
	SCL输入高脉冲宽度	t_{SCLH}	5 (9) × t_{IICcyc}	—	ns	
	SCL输入低脉冲宽度	t_{SCLL}	5 (9) × t_{IICcyc}	—	ns	
	SCL、SDA上升时间	t_{Sr}	—	1000	ns	
	SCL、SDA下降时间	t_{Sf}	—	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA输入总线空闲时间	t_{BUF}	5 (9) × t_{IICcyc} + 300	—	ns	
	START条件输入保持时间	t_{STAH}	t_{IICcyc} + 300	—	ns	
	重复启动条件输入建立时间	t_{STAS}	1000	—	ns	
	STOP条件输入建立时间	t_{STOS}	1000	—	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *1	—	400	pF	

Note: tIICcyc:IIC内部参考时钟(IICφ)周期。
Note: 括号中的值适用于INCTL.DNFS[3:0]设置为0011b且数字滤波器启用且INCTL.DNFE设置为1的情况。
注1.Cb表示公交线路的总容量。

Table 46.30 IIC timing (1)-2

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_B, SCL1_B, SCL0_C, SDA0_C, SCL0_D, SDA0_D, SCL0_E, SDA0_E, SCL0_F, SDA0_F, SCL1_C, SDA1_C, SCL1_D, SDA1_D, SCL1_E, SDA1_E.
(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL1_A, SDA1_A.
(3) Use pins that have a letter appended to their names, for instance _A or _B or _C or _D or _E or _F, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit	Test conditions
IIC (Fast-mode)	SCL input cycle time	t_{SCL}	10 (18) × t_{IICcyc} + 600	—	ns	Figure 46.47
	SCL input high pulse width	t_{SCLH}	5 (9) × t_{IICcyc}	—	ns	
	SCL input low pulse width	t_{SCLL}	5 (9) × t_{IICcyc}	—	ns	
	SCL, SDA rise time	t_{Sr}	20 × (external pullup voltage/ 5.5V)*1	300	ns	
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/ 5.5V)*1	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	5 (9) × t_{IICcyc} + 300	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.
Note: Must use pins that have a letter appended to their name, for instance _A, _B, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. Only supported for SCL0_A, SDA0_A, SCL1_A, and SDA1_A. Other ports are depend on DC characteristics.
Note 2. C_b indicates the total capacity of the bus line.

Table 46.30 IIC timing (1)-2

(1)条件：在PmnPFS寄存器的PortDriveCapability位为以下引脚选择中间驱动输出：SDA0_B、SCL0_B、SDA1_B、SCL1_B、SCL0_C、SDA0_C、SCL0_D、SDA0_D、SCL0_E、SDA0_E、SCL0_F、SDA0_F、SCL1_C SDA1_C SCL1_D SDA1_D、SCL1_E、SDA1_E。(2)以下引脚不需要设置：SCL0_A、SDA0_A、SCL1_A、SDA1_A。(3)使用名称后附有字母的引脚，例如_A或_B或_C或_D或_E或_F，以表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

Parameter		Symbol	Min	Max	Unit	测试条件
IIC (Fast-mode)	SCL输入周期时间	t_{SCL}	10 (18) × t_{IICcyc} + 600	—	ns	Figure 46.47
	SCL输入高脉冲宽度	t_{SCLH}	5 (9) × t_{IICcyc}	—	ns	
	SCL输入低脉冲宽度	t_{SCLL}	5 (9) × t_{IICcyc}	—	ns	
	SCL、SDA上升时间	t_{Sr}	20 × (external pullup voltage/ 5.5V)*1	300	ns	
	SCL、SDA下降时间	t_{Sf}	20 × (external pullup voltage/ 5.5V)*1	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA输入总线空闲时间	t_{BUF}	5 (9) × t_{IICcyc} + 300	—	ns	
	START条件输入保持时间	t_{STAH}	t_{IICcyc} + 300	—	ns	
	重复启动条件输入建立时间	t_{STAS}	300	—	ns	
	STOP条件输入建立时间	t_{STOS}	300	—	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Note: tIICcyc:IIC内部参考时钟(IICφ)周期。
Note: 括号中的值适用于INCTL.DNFS[3:0]设置为0011b且数字滤波器启用且INCTL.DNFE设置为1的情况。
Note: 必须使用名称后附有字母的引脚，例如_A、_B，以表明组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

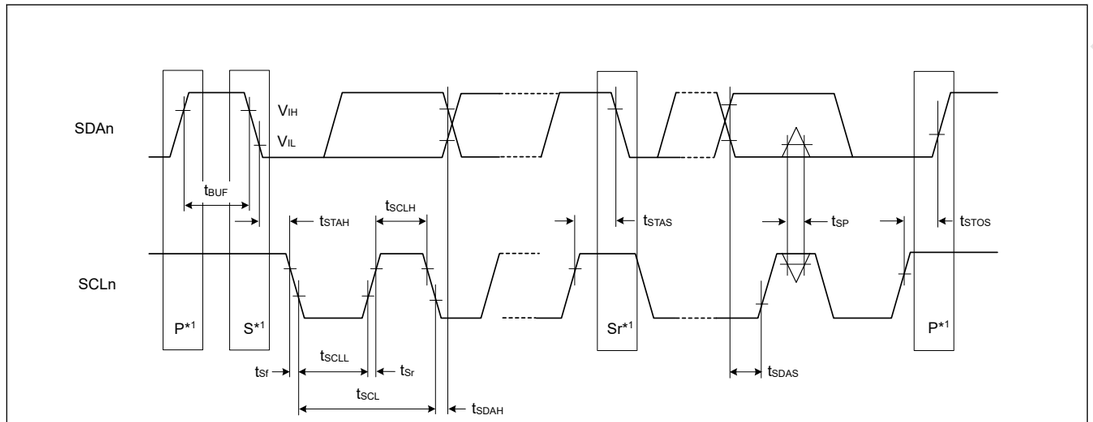
注1.仅支持SCL0_A、SDA0_A、SCL1_A和SDA1_A。其他端口取决于直流特性。
注2.Cb表示公交线路的总容量。

Table 46.31 IIC timing (1)-3

Setting of the SCL0_A, SDA0_A pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
IIC (Fast-mode+) BFCTL.FMPE = 1	SCL input cycle time	t_{SCL}	10 (18) × t_{IICcyc} + 240	—	ns	Figure 46.47
	SCL input high pulse width	t_{SCLH}	5 (9) × t_{IICcyc}	—	ns	
	SCL input low pulse width	t_{SCLL}	5 (9) × t_{IICcyc}	—	ns	
	SCL, SDA rise time	t_{Sr}	—	120	ns	
	SCL, SDA fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	5 (9) × t_{IICcyc} + 120	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 120	—	ns	
	Repeated START condition input setup time	t_{STAS}	120	—	ns	
	STOP condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 30	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.
Note: Targets are SCL0_A and SDA0_A.
Note 1. C_b indicates the total capacity of the bus line.



Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

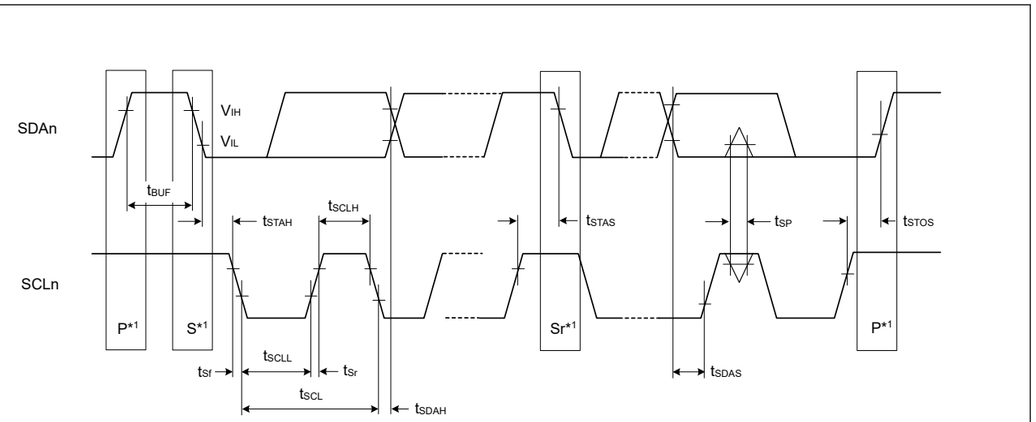
Figure 46.47 I^2C bus interface input/output timing

Table 46.31 IIC timing (1)-3

PmnPFS寄存器中的端口驱动能力位不需要设置SCL0_A、SDA0_A引脚。

Parameter		Symbol	Min	Max	Unit	测试条件
IIC (Fast-mode+) BFCTL.FMPE = 1	SCL输入周期时间	t_{SCL}	10 (18) × t_{IICcyc} + 240	—	ns	Figure 46.47
	SCL输入高脉冲宽度	t_{SCLH}	5 (9) × t_{IICcyc}	—	ns	
	SCL输入低脉冲宽度	t_{SCLL}	5 (9) × t_{IICcyc}	—	ns	
	SCL、SDA上升时间	t_{Sr}	—	120	ns	
	SCL、SDA下降时间	t_{Sf}	—	120	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA输入总线空闲时间	t_{BUF}	5 (9) × t_{IICcyc} + 120	—	ns	
	START条件输入保持时间	t_{STAH}	t_{IICcyc} + 120	—	ns	
	重复启动条件输入建立时间	t_{STAS}	120	—	ns	
	STOP条件输入建立时间	t_{STOS}	120	—	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 30	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	550	pF	

Note: tIICcyc:IIC内部参考时钟(IICφ)周期。
Note: 括号中的值适用于INCTL.DNFS[3:0]设置为0011b且数字滤波器启用且INCTL.DNFE设置为1的情况。
Note: 目标是SCL0_A和SDA0_A。
注1.Cb表示公交线路的总容量。



注1.S、P和Sr表示以下条件：
S：开始条件P：
停止条件
Sr：重启条件

Figure 46.47 I2C总线接口输入输出时序

Table 46.32 IIC timing (2)

Setting of the SCL0_A, SDA0_A pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
IIC (Hs-mode) BFCTL.HSME = 1	SCL input cycle time		t_{SCL}	10 (12) × t_{IICcyc} + 80	—	ns	Figure 46.48
	SCL input high pulse width		t_{SCLH}	5 (6) × t_{IICcyc}	—	ns	
	SCL input low pulse width		t_{SCLL}	5 (6) × t_{IICcyc}	—	ns	
	SCL rise time	C_b = 400pF	t_{SrCL}	—	80	ns	
		C_b = 100pF		—	40	ns	
	SDA rise time	C_b = 400pF	t_{SrDA}	—	160	ns	
		C_b = 100pF		—	80	ns	
	SCL fall time	C_b = 400pF	t_{SfCL}	—	80	ns	
		C_b = 100pF		—	40	ns	
	SDA fall time	C_b = 400pF	t_{SfDA}	—	160	ns	
		C_b = 100pF		—	80	ns	
	SCL, SDA input spike pulse removal time		t_{SP}	0	1 (1) × t_{IICcyc}	ns	
	Repeated START condition input setup time		t_{STAS}	40	—	ns	
	STOP condition input setup time		t_{STOS}	40	—	ns	
	Data input setup time		t_{SDAS}	10	—	ns	
	Data input hold time	C_b = 400pF	t_{SDAH}	0	150	ns	
		C_b = 100pF		0	70	ns	
	SCL, SDA capacitive load		C_b*1	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.
Note: Targets are SCL0_A and SDA0_A.
Note 1. C_b indicates the total capacity of the bus line.

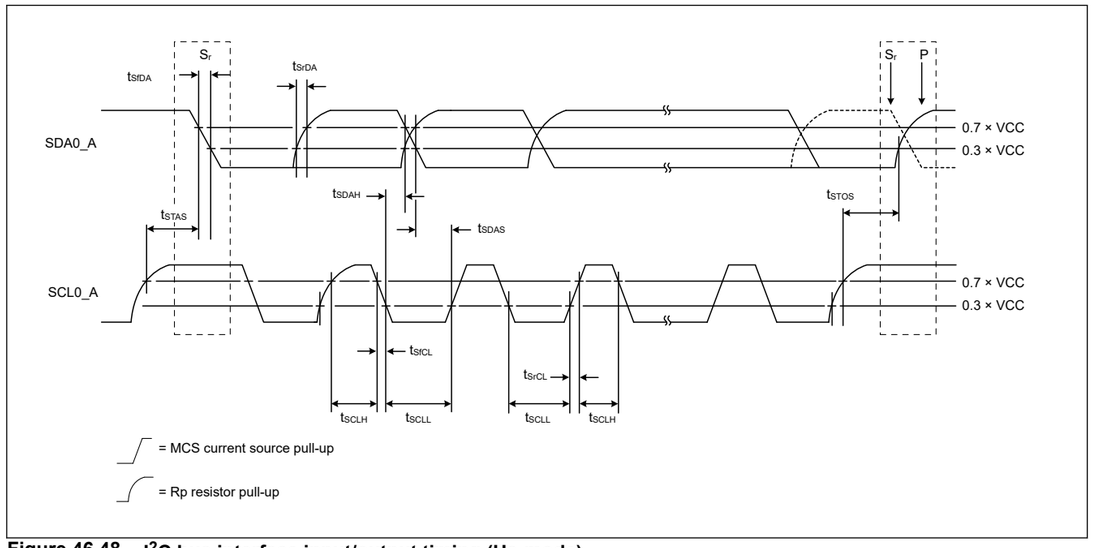


Figure 46.48 I²C bus interface input/output timing (Hs-mode)

Table 46.32 IIC timing (2)

PmnPFS寄存器中的端口驱动能力位不需要设置SCL0_A、SDA0_A引脚。

Parameter			Symbol	Min	Max	Unit	测试条件
IIC (Hs-mode) BFCTL.HSME = 1	SCL输入周期时间		t_{SCL}	10 (12) × t_{IICcyc} + 80	—	ns	Figure 46.48
	SCL输入高脉冲宽度		t_{SCLH}	5 (6) × t_{IICcyc}	—	ns	
	SCL输入低脉冲宽度		t_{SCLL}	5 (6) × t_{IICcyc}	—	ns	
	SCL上升时间	C_b = 400pF	t_{SrCL}	—	80	ns	
		C_b = 100pF		—	40	ns	
	SDA上升时间	C_b = 400pF	t_{SrDA}	—	160	ns	
		C_b = 100pF		—	80	ns	
	SCL下降时间	C_b = 400pF	t_{SfCL}	—	80	ns	
		C_b = 100pF		—	40	ns	
	SDA下降时间	C_b = 400pF	t_{SfDA}	—	160	ns	
		C_b = 100pF		—	80	ns	
	SCL、SDA输入尖峰脉冲去除时间		t_{SP}	0	1 (1) × t_{IICcyc}	ns	
	重复启动条件输入建立时间		t_{STAS}	40	—	ns	
	STOP条件输入建立时间		t_{STOS}	40	—	ns	
	数据输入建立时间		t_{SDAS}	10	—	ns	
	数据输入保持时间	C_b = 400pF	t_{SDAH}	0	150	ns	
		C_b = 100pF		0	70	ns	
	SCL, SDA capacitive load		C_b*1	—	400	pF	

Note: tIICcyc:IIC内部参考时钟(IICφ)周期。
Note: 括号中的值适用于INCTL.DNFS[3:0]设置为0011b且数字滤波器启用且INCTL.DNFE设置为1的情况。
Note: 目标是SCL0_A和SDA0_A。
注1.Cb表示公交线路的总容量。

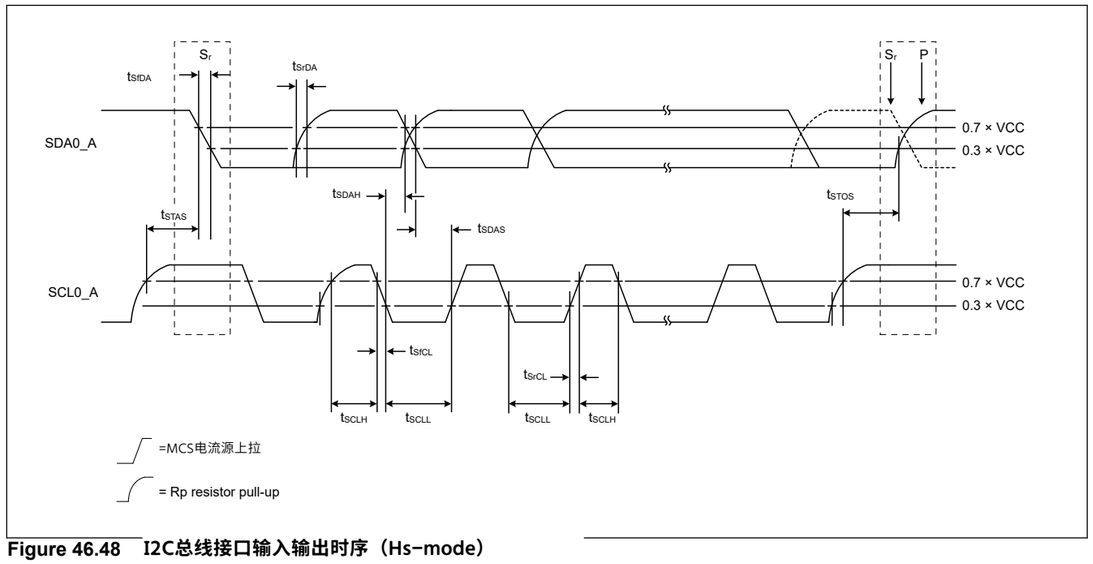


Figure 46.48 I2C总线接口输入输出时序（Hs-mode）

46.3.12 CANFD Timing

Table 46.33 CANFD interface timing

Parameter	Symbol	CAN		CAN-FD		Unit	Test conditions
		Min	Max	Min	Max		
Internal delay time	t_{node}	—	100	—	75	ns	Figure 46.49
Transmission rate		—	1	—	5	Mbps	

Note: $t_{node} = t_{output} + t_{input}$

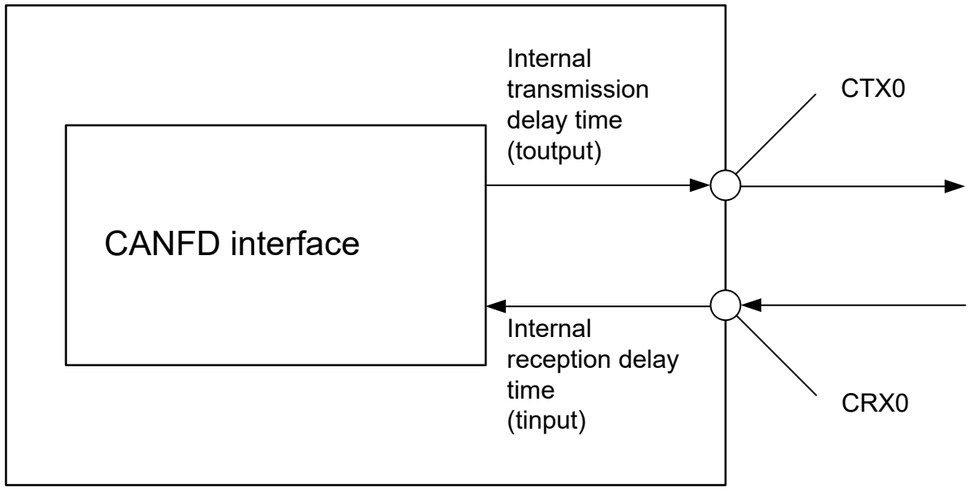


Figure 46.49 CANFD interface condition

46.4 ADC Characteristics

Table 46.34 A/D conversion characteristics (Common) (1 of 2)

Parameter				Min	Typ	Max	Unit	Test conditions
A/D conversion clock frequency(ADCLK)				25	50	60	MHz	
Quantization error				—	±0.5	—	LSB	
Successive approximation time				100	—	140	ns	
A/D sampling time	During calibration			400	—	—	ns	
	In self-diagnosis mode			1 × t_{ADcyc} + 40	—	—	ns	
	During A/D conversion	Channel-dedicated sample-and-hold circuits in use	(AN000 to AN005) (AN006 to AN011)	1 × t_{ADcyc} + 160	—	—	ns	
		High-speed channels	(AN000 to AN005) (AN006 to AN011) (AN018 to AN019)	1 × t_{ADcyc} + 40	—	—	ns	
		High-precision channels	(AN012 to AN017)	180	—	—	ns	
		Normal-precision channels	(AN020 to AN028)	400	—	—	ns	

46.3.12 CANFD Timing

Table 46.33 CANFD接口时序

Parameter	Symbol	CAN		CAN-FD		Unit	测试条件
		Min	Max	Min	Max		
内部延迟时间	t_{node}	—	100	—	75	ns	Figure 46.49
传输速率		—	1	—	5	Mbps	

Note: t节点=t输出+t输入

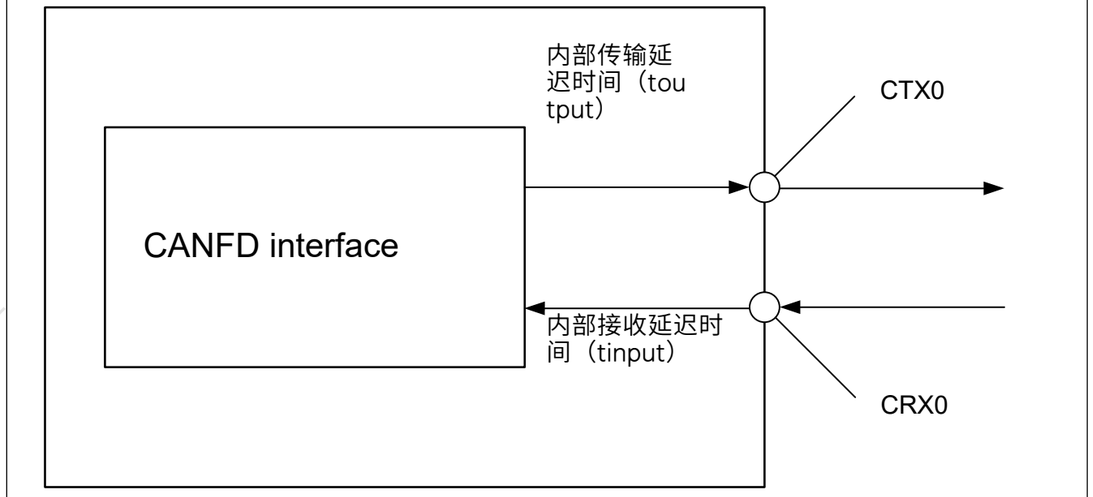


Figure 46.49 CANFD接口情况

46.4 ADC Characteristics

Table 46.34 AD转换特性(Common)(1of2)

Parameter				Min	Typ	Max	Unit	测试条件
AD转换时钟频率(ADCLK)				25	50	60	MHz	
量化误差				—	±0.5	—	LSB	
逐次逼近时间				100	—	140	ns	
AD采样时间	校准期间			400	—	—	ns	
	处于自诊断模式			1 × t_{ADcyc} + 40	—	—	ns	
	在AD转换期间	使用中的通道专用采样保持电路	(AN000 to AN005) (AN006 to AN011)	1 × t_{ADcyc} + 160	—	—	ns	
		High-speed channels	(AN000 to AN005) (AN006 to AN011) (AN018 to AN019)	1 × t_{ADcyc} + 40	—	—	ns	
		High-precision channels	(AN012 to AN017)	180	—	—	ns	
		Normal-precision channels	(AN020 to AN028)	400	—	—	ns	

Table 46.34 A/D conversion characteristics (Common) (2 of 2)

Parameter		Min	Typ	Max	Unit	Test conditions
Channel-dedicated sample-and-hold circuits	Sampling time during calibration	400	—	—	ns	
	Sampling time during A/D conversion	400	—	—	ns	
	Hold mode switching time	40	—	—	ns	
	Hold time	—	—	5	µs	
Operation stabilization time	A/D start-up time	2.0	—	—	us	
	Channel-dedicated sample-and-hold circuits start-up time	2.0	—	—	us	
	A/D shut-down time	1.0	—	—	us	
Analog input voltage range		VREFL0	—	VREFH0	V	

Note: t_{ADcyc} : ADCLK cycle

Table 46.35 A/D conversion characteristics (1 of 2)

Parameter			Min	Typ	Max	Unit	Test conditions
Resolution			—	—	12	bit	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN005) (AN006 to AN011)	Conversion time*1 (operation at ADCLK = 50 MHz)	Permissible signal source impedance Max. = 50Ω	0.70	—	—	µs	• Sampling time of channel-dedicated sample-and-hold circuits: 20 ADCLK • Hold mode switching time of channel-dedicated sample-and-hold circuits: 2 ADCLK • Sampling time: 8 ADCLK • Successive approximation time: 5 ADCLK
	Offset error		—	±0.5	±1.0	LSB	
	Full-scale error		—	±1.0	±1.5	LSB	
	Absolute accuracy		—	±5.0	±7.0	LSB	
	DNL pseudo-differential nonlinearity error		—	-1 to +1.5	-1 to +2.5	LSB	
	INL integral nonlinearity error		—	±2.0	±3.0	LSB	
High-speed channels (AN000 to AN005) (AN006 to AN011) (AN018 to AN019)*2	Conversion time*1 (operation at ADCLK = 50 MHz)	Permissible signal source impedance Max. = 50Ω	0.16	—	—	µs	• Sampling time: 3 ADCLK • Successive approximation time: 5 ADCLK
	Offset error		—	±1.0	±3.0	LSB	
	Full-scale error		—	±1.5	±2.5	LSB	
	Absolute accuracy		—	±5.5	±7.0	LSB	
	DNL pseudo-differential nonlinearity error		—	-1 to +1.5	-1 to +2.5	LSB	
	INL integral nonlinearity error		—	±2.0	±3.0	LSB	
High-precision channels (AN012 to AN017)	Conversion time*1 (operation at ADCLK = 50 MHz)	Permissible signal source impedance Max. = 50Ω	0.28	—	—	µs	• Sampling time: 9 ADCLK • Successive approximation time: 5 ADCLK
	Offset error		—	±1.0	±1.5	LSB	
	Full-scale error		—	±1.0	±2.5	LSB	
	Absolute accuracy		—	±4.0	±7.0	LSB	
	DNL pseudo-differential nonlinearity error		—	-1 to +1.5	-1 to +2.5	LSB	
	INL integral nonlinearity error		—	±2.0	±3.0	LSB	

Table 46.34 AD转换特性(Common)(2of2)

Parameter		Min	Typ	Max	Unit	测试条件
Channel-dedicated sample-and-hold circuits	校准期间的采样时间	400	—	—	ns	
	AD转换期间的采样时间	400	—	—	ns	
	保持模式切换时间	40	—	—	ns	
	保持时间	—	—	5	µs	
运行稳定时间	A/D start-up time	2.0	—	—	us	
	通道专用采样保持电路的启动时间	2.0	—	—	us	
	A/D shut-down time	1.0	—	—	us	
模拟输入电压范围		VREFL0	—	VREFH0	V	

Note: t_{ADcyc} : ADCLK cycle

Table 46.35 AD转换特性(1of2)

Parameter			Min	Typ	Max	Unit	测试条件
Resolution			—	—	12	bit	
使用中的通道专用采样保持电路（AN000至AN005）（AN006至AN011）	转换时间*1 (operation at ADCLK = 50 MHz)	允许的信号源阻抗 Max.=50Ω	0.70	—	—	µs	• 通道专用采样保持电路的采样时间：20ADCLK • 通道专用采样保持电路的保持模式切换时间：2ADCLK • Sampling time: 8 ADCLK • 逐次逼近时间：5 ADCLK
	偏移误差		—	±0.5	±1.0	LSB	
	Full-scale error		—	±1.0	±1.5	LSB	
	绝对精度		—	±5.0	±7.0	LSB	
	DNL pseudo-differential nonlinearity error		—	-1 to +1.5	-1 to +2.5	LSB	
	INL积分非线性误差		—	±2.0	±3.0	LSB	
高速通道(AN000至AN005)(AN006至AN011)(AN018至AN019)*2	转换时间*1 (operation at ADCLK = 50 MHz)	允许的信号源阻抗 Max.=50Ω	0.16	—	—	µs	• Sampling time: 3 ADCLK • 逐次逼近时间：5 ADCLK
	偏移误差		—	±1.0	±3.0	LSB	
	Full-scale error		—	±1.5	±2.5	LSB	
	绝对精度		—	±5.5	±7.0	LSB	
	DNL pseudo-differential nonlinearity error		—	-1 to +1.5	-1 to +2.5	LSB	
	INL积分非线性误差		—	±2.0	±3.0	LSB	
高精度通道（AN012至AN017）	转换时间*1 (operation at ADCLK = 50 MHz)	允许的信号源阻抗 Max.=50Ω	0.28	—	—	µs	• Sampling time: 9 ADCLK • 逐次逼近时间：5 ADCLK
	偏移误差		—	±1.0	±1.5	LSB	
	Full-scale error		—	±1.0	±2.5	LSB	
	绝对精度		—	±4.0	±7.0	LSB	
	DNL pseudo-differential nonlinearity error		—	-1 to +1.5	-1 to +2.5	LSB	
	INL积分非线性误差		—	±2.0	±3.0	LSB	

Table 46.35 A/D conversion characteristics (2 of 2)

Parameter			Min	Typ	Max	Unit	Test conditions
Normal-precision channels (AN020 to AN028)	Conversion time*1 (operation at ADCLK = 50 MHz)	Permissible signal source impedance Max. = 50Ω	0.50	—	—	µs	• Sampling time: 20 ADCLK • Successive approximation time: 5 ADCLK
	Offset error		—	±1.0	±2.5	LSB	
	Full-scale error		—	±1.5	±2.5	LSB	
	Absolute accuracy		—	±5.5	±8.0	LSB	
	DNL pseudo-differential nonlinearity error		—	-1 to +1.5	-1 to +2.5	LSB	
	INL integral nonlinearity error		—	±2.0	±4.0	LSB	

Note 1. Channel-dedicated sample-and-hold circuits in use; The conversion time is the sum of the sampling time of channel-dedicated sample-and-hold circuits, the hold mode switching time, the sampling time and the successive approximation time. Each of the above state is indicated for the test conditions.
Channel-dedicated sample-and-hold circuits not in use; The conversion time is the sum of the sampling time and the successive approximation time. Each of the above state is indicated for the test conditions.
Note 2. These channels cannot be used with Channel-dedicated sample-and-hold circuits.

Table 46.36 A/D internal reference voltage characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	
Sampling time	4.15	—	—	µs	

Table 46.37 A/D with D/A conversion characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
Sampling time	1	—	—	µs	

46.5 DAC12 Characteristics

Table 46.38 D/A conversion characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bits	—
Without output amplifier					
Absolute accuracy	—	—	±24	LSB	Resistive load 2 MΩ
INL	—	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	—	±1.0	±2.0	LSB	—
Output impedance	—	8.5	—	kΩ	—
Conversion time	—	—	3	µs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	—	AVCC0	V	—
With output amplifier					
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
Conversion time	—	—	4.0	µs	—
Resistive load	5	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
Output voltage range	0.2	—	AVCC0 – 0.2	V	—

Table 46.35 AD转换特性(2of2)

Parameter			Min	Typ	Max	Unit	测试条件
普通精度通道（AN020至AN028）	转换时间*1 (operation at ADCLK = 50 MHz)	允许的信号源阻抗 Max.=50Ω	0.50	—	—	µs	• Sampling time: 20 ADCLK • 逐次逼近时间：5 ADCLK
	偏移误差		—	±1.0	±2.5	LSB	
	Full-scale error		—	±1.5	±2.5	LSB	
	绝对精度		—	±5.5	±8.0	LSB	
	DNL pseudo-differential nonlinearity error		—	-1 to +1.5	-1 to +2.5	LSB	
	INL积分非线性误差		—	±2.0	±4.0	LSB	

注1.使用中的通道专用采样保持电路；转换时间是通道专用采样保持电路的采样时间、保持模式切换时间、采样时间和逐次逼近时间之和。上述每种状态均针对测试条件进行指示。未使用通道专用的采样保持电路；转换时间是采样时间和逐次逼近时间之和。上述每种状态均针对测试条件进行指示。

注2.这些通道不能与通道专用的采样保持电路一起使用。

Table 46.36 AD内部参考电压特性

Parameter	Min	Typ	Max	Unit	测试条件
AD内部参考电压	1.13	1.18	1.23	V	
采样时间	4.15	—	—	µs	

Table 46.37 AD具有DA转换特性

Parameter	Min	Typ	Max	Unit	测试条件
采样时间	1	—	—	µs	

46.5 DAC12 Characteristics

Table 46.38 DA转换特性

Parameter	Min	Typ	Max	Unit	测试条件
Resolution	—	—	12	Bits	—
无输出放大器					
绝对精度	—	—	±24	LSB	阻性负载2MΩ
INL	—	±2.0	±8.0	LSB	阻性负载2MΩ
DNL	—	±1.0	±2.0	LSB	—
输出阻抗	—	8.5	—	kΩ	—
转换时间	—	—	3	µs	电阻负载2MΩ，电容负载20pF
输出电压范围	0	—	AVCC0	V	—
带输出放大器					
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
转换时间	—	—	4.0	µs	—
阻性负载	5	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
输出电压范围	0.2	—	AVCC0 – 0.2	V	—

46.6 TSN Characteristics

Table 46.39 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.0	—	°C	—
Temperature slope	—	—	4.0	—	mV/°C	—
Output voltage (at 25 °C)	—	—	1.24	—	V	—
Temperature sensor start time	t_{START}	—	—	30	µs	—
Sampling time	—	4.15	—	—	µs	—

46.7 ACMPHS Characteristics

Table 46.40 ACMPHS characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input offset voltage	V_{IO}	—	—	40	mV	
Reference voltage range	V_{REF}	0	—	AVCC0	V	
Input voltage range	V_I	0	—	AVCC0	V	
Output delay	$t_{tot(r)}$	—	—	200	ns	VOD = 100 mV CMPCTL.CDFS = 0
	$t_{tot(f)}$	—	—	200	ns	
Waiting time for stabilization following switching of the input	t_{cwait}	300	—	—	ns	
Operation stabilization time	t_{cmp}	—	—	1	us	

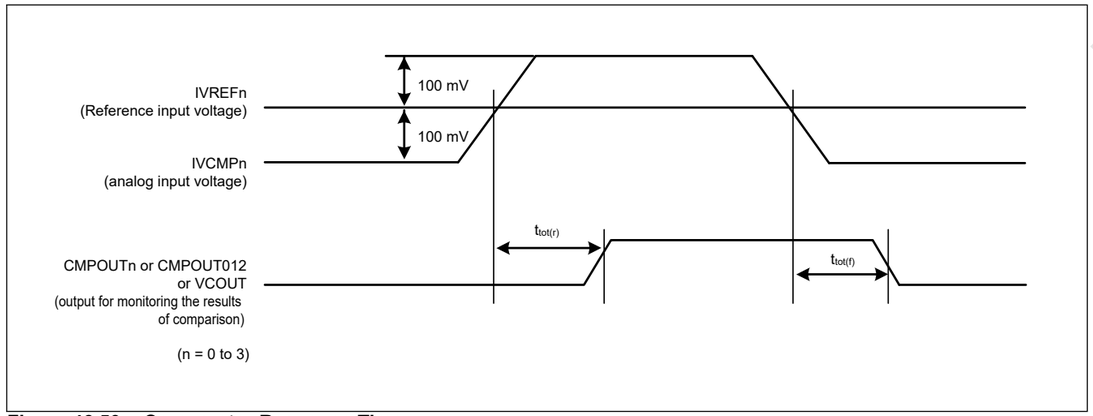


Figure 46.50 Comparator Response Time

46.8 PGA Characteristics

Table 46.41 PGA characteristics in single mode (1 of 3)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Offset error	Voff	-8	—	8	mV	

46.6 TSN Characteristics

Table 46.39 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
相对精度	—	—	± 1.0	—	°C	—
温度斜率	—	—	4.0	—	mV/°C	—
输出电压（25°C时）	—	—	1.24	—	V	—
温度传感器启动时间	t_{START}	—	—	30	µs	—
采样时间	—	4.15	—	—	µs	—

46.7 ACMPHS Characteristics

Table 46.40 ACMPHS characteristics

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
输入失调电压	V_{IO}	—	—	40	mV	
参考电压范围	V_{REF}	0	—	AVCC0	V	
输入电压范围	V_I	0	—	AVCC0	V	
输出延迟	$t_{tot(r)}$	—	—	200	ns	VOD = 100 mV CMPCTL.CDFS = 0
	$t_{tot(f)}$	—	—	200	ns	
输入切换后的稳定等待时间	t_{cwait}	300	—	—	ns	
运行稳定时间	t_{cmp}	—	—	1	us	

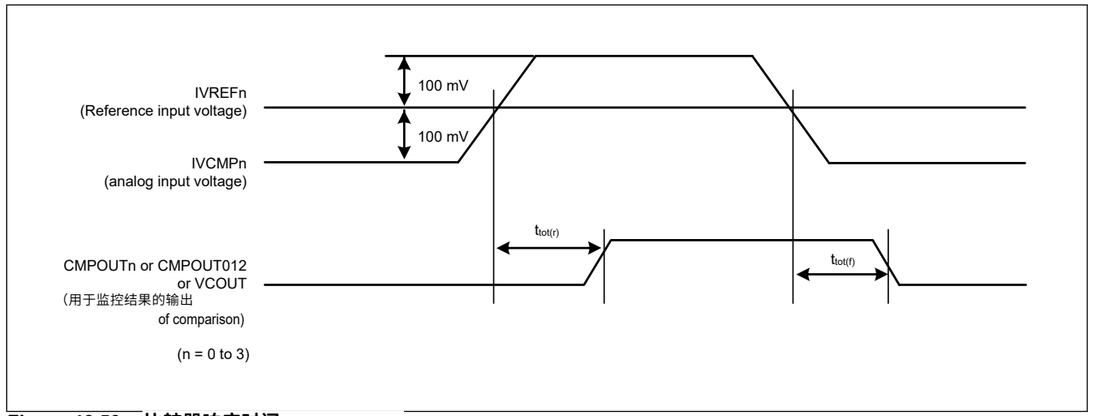


Figure 46.50 比较器响应时间

46.8 PGA特性

Table 46.41 单模PGA特性（3个中的1个）

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
偏移误差	Voff	-8	—	8	mV	

Table 46.41 PGA characteristics in single mode (2 of 3)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
PGAVSS input voltage range	PGAVSS	0	—	0	V	
	AIN0 (G = 2.000)	0.05 × AVCC0	—	0.45 × AVCC0	V	
	AIN1 (G = 2.500)	0.047 × AVCC0	—	0.36 × AVCC0	V	
	AIN2 (G = 2.667)	0.046 × AVCC0	—	0.337 × AVCC0	V	
	AIN3 (G = 2.857)	0.046 × AVCC0	—	0.32 × AVCC0	V	
	AIN4 (G = 3.077)	0.045 × AVCC0	—	0.292 × AVCC0	V	
	AIN5 (G = 3.333)	0.044 × AVCC0	—	0.265 × AVCC0	V	
	AIN6 (G = 3.636)	0.042 × AVCC0	—	0.247 × AVCC0	V	
	AIN7 (G = 4.000)	0.04 × AVCC0	—	0.212 × AVCC0	V	
	AIN8 (G = 4.444)	0.036 × AVCC0	—	0.191 × AVCC0	V	
	AIN9 (G = 5.000)	0.033 × AVCC0	—	0.17 × AVCC0	V	
	AIN10 (G = 5.714)	0.031 × AVCC0	—	0.148 × AVCC0	V	
	AIN11 (G = 6.667)	0.029 × AVCC0	—	0.127 × AVCC0	V	
	AIN12 (G = 8.000)	0.027 × AVCC0	—	0.09 × AVCC0	V	
	AIN13 (G = 10.000)	0.025 × AVCC0	—	0.08 × AVCC0	V	
	AIN14 (G = 13.333)	0.023 × AVCC0	—	0.06 × AVCC0	V	
Output voltage range*1	PGAOUT0 (G = 2.000)	0.100 × AVCC0	—	0.900 × AVCC0	V	
	PGAOUT1 (G = 2.500)	0.118 × AVCC0	—	0.900 × AVCC0	V	
	PGAOUT2 (G = 2.667)	0.123 × AVCC0	—	0.899 × AVCC0	V	
	PGAOUT3 (G = 2.857)	0.131 × AVCC0	—	0.914 × AVCC0	V	
	PGAOUT4 (G = 3.077)	0.138 × AVCC0	—	0.898 × AVCC0	V	
	PGAOUT5 (G = 3.333)	0.147 × AVCC0	—	0.883 × AVCC0	V	
	PGAOUT6 (G = 3.636)	0.153 × AVCC0	—	0.898 × AVCC0	V	
	PGAOUT7 (G = 4.000)	0.160 × AVCC0	—	0.848 × AVCC0	V	
	PGAOUT8 (G = 4.444)	0.160 × AVCC0	—	0.849 × AVCC0	V	
	PGAOUT9 (G = 5.000)	0.165 × AVCC0	—	0.850 × AVCC0	V	
	PGAOUT10 (G = 5.714)	0.177 × AVCC0	—	0.846 × AVCC0	V	
	PGAOUT11 (G = 6.667)	0.193 × AVCC0	—	0.847 × AVCC0	V	
	PGAOUT12 (G = 8.000)	0.216 × AVCC0	—	0.720 × AVCC0	V	
	PGAOUT13 (G = 10.000)	0.250 × AVCC0	—	0.800 × AVCC0	V	
	PGAOUT14 (G = 13.333)	0.307 × AVCC0	—	0.800 × AVCC0	V	

Table 46.41 单模PGA特性(2of3)

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
PGAVSS输入电压范围	PGAVSS	0	—	0	V	
	AIN0 (G = 2.000)	0.05 × AVCC0	—	0.45 × AVCC0	V	
	AIN1 (G = 2.500)	0.047 × AVCC0	—	0.36 × AVCC0	V	
	AIN2 (G = 2.667)	0.046 × AVCC0	—	0.337 × AVCC0	V	
	AIN3 (G = 2.857)	0.046 × AVCC0	—	0.32 × AVCC0	V	
	AIN4 (G = 3.077)	0.045 × AVCC0	—	0.292 × AVCC0	V	
	AIN5 (G = 3.333)	0.044 × AVCC0	—	0.265 × AVCC0	V	
	AIN6 (G = 3.636)	0.042 × AVCC0	—	0.247 × AVCC0	V	
	AIN7 (G = 4.000)	0.04 × AVCC0	—	0.212 × AVCC0	V	
	AIN8 (G = 4.444)	0.036 × AVCC0	—	0.191 × AVCC0	V	
	AIN9 (G = 5.000)	0.033 × AVCC0	—	0.17 × AVCC0	V	
	AIN10 (G = 5.714)	0.031 × AVCC0	—	0.148 × AVCC0	V	
	AIN11 (G = 6.667)	0.029 × AVCC0	—	0.127 × AVCC0	V	
	AIN12 (G = 8.000)	0.027 × AVCC0	—	0.09 × AVCC0	V	
	AIN13 (G = 10.000)	0.025 × AVCC0	—	0.08 × AVCC0	V	
	AIN14 (G = 13.333)	0.023 × AVCC0	—	0.06 × AVCC0	V	
输出电压范围*1	PGAOUT0 (G = 2.000)	0.100 × AVCC0	—	0.900 × AVCC0	V	
	PGAOUT1 (G = 2.500)	0.118 × AVCC0	—	0.900 × AVCC0	V	
	PGAOUT2 (G = 2.667)	0.123 × AVCC0	—	0.899 × AVCC0	V	
	PGAOUT3 (G = 2.857)	0.131 × AVCC0	—	0.914 × AVCC0	V	
	PGAOUT4 (G = 3.077)	0.138 × AVCC0	—	0.898 × AVCC0	V	
	PGAOUT5 (G = 3.333)	0.147 × AVCC0	—	0.883 × AVCC0	V	
	PGAOUT6 (G = 3.636)	0.153 × AVCC0	—	0.898 × AVCC0	V	
	PGAOUT7 (G = 4.000)	0.160 × AVCC0	—	0.848 × AVCC0	V	
	PGAOUT8 (G = 4.444)	0.160 × AVCC0	—	0.849 × AVCC0	V	
	PGAOUT9 (G = 5.000)	0.165 × AVCC0	—	0.850 × AVCC0	V	
	PGAOUT10 (G = 5.714)	0.177 × AVCC0	—	0.846 × AVCC0	V	
	PGAOUT11 (G = 6.667)	0.193 × AVCC0	—	0.847 × AVCC0	V	
	PGAOUT12 (G = 8.000)	0.216 × AVCC0	—	0.720 × AVCC0	V	
	PGAOUT13 (G = 10.000)	0.250 × AVCC0	—	0.800 × AVCC0	V	
	PGAOUT14 (G = 13.333)	0.307 × AVCC0	—	0.800 × AVCC0	V	

Table 46.41 PGA characteristics in single mode (3 of 3)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Gain error	Gerr0 (G = 2.000)	-1.0	—	1.0	%	
	Gerr1 (G = 2.500)	-1.0	—	1.0	%	
	Gerr2 (G = 2.667)	-1.0	—	1.0	%	
	Gerr3 (G = 2.857)	-1.0	—	1.0	%	
	Gerr4 (G = 3.007)	-1.0	—	1.0	%	
	Gerr5 (G = 3.333)	-1.5	—	1.5	%	
	Gerr6 (G = 3.636)	-1.5	—	1.5	%	
	Gerr7 (G = 4.000)	-1.5	—	1.5	%	
	Gerr8 (G = 4.444)	-2.0	—	2.0	%	
	Gerr9 (G = 5.000)	-2.0	—	2.0	%	
	Gerr10 (G = 5.714)	-2.0	—	2.0	%	
	Gerr11 (G = 6.667)	-2.0	—	2.0	%	
	Gerr12 (G = 8.000)	-2.0	—	2.0	%	
	Gerr13 (G = 10.000)	-2.0	—	2.0	%	
	Gerr14 (G = 13.333)	-2.0	—	2.0	%	
Operation stabilization time	t_{start}	—	—	5	µs	

Note 1. Calculate with the following formula. (n = 0 to 14)
PGAOUTn = AINn × G
Actual output range includes gain error.
PGAOUTn = (AINn × G) × (Gerr + 100%)

Table 46.42 PGA characteristics in differential mode

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Offset error		Voff	-20	—	20	mV	
PGAVSS input voltage range		PGAVSS	-0.5	—	0.3	V	
Differential input voltage range	G = 1.500	AIN-PGAVSS	-0.5	—	0.5	V	
	G = 2.333		-0.4	—	0.4	V	
	G = 4.000		-0.2	—	0.2	V	
	G = 5.667		-0.15	—	0.15	V	
Output voltage range*1	G = 1.500	V_{OR}	0.600	—	2.550	V	
	G = 2.333		0.417	—	2.733	V	
	G = 4.000		0.550	—	2.600	V	
	G = 5.667		0.500	—	2.650	V	
Gain error	G = 1.500	Gerr	-1.0	—	1.0	%	
	G = 2.333		-1.0	—	1.0	%	
	G = 4.000		-1.0	—	1.0	%	
	G = 5.667		-1.0	—	1.0	%	
Operation stabilization time		t_{start}	—	—	5	µs	

Note 1. Calculate with the following formula.
V_{OR} = (AIN-PGAVSS) × G + (0.5 × AVCC0)
Actual output range includes gain error.
V_{OR} = (AIN-PGAVSS) × G × (Gerr +100%) + (0.5 × AVCC0)

Table 46.41 单模PGA特性（3个中的3个）

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
增益误差	Gerr0 (G = 2.000)	-1.0	—	1.0	%	
	Gerr1 (G = 2.500)	-1.0	—	1.0	%	
	Gerr2 (G = 2.667)	-1.0	—	1.0	%	
	Gerr3 (G = 2.857)	-1.0	—	1.0	%	
	Gerr4 (G = 3.007)	-1.0	—	1.0	%	
	Gerr5 (G = 3.333)	-1.5	—	1.5	%	
	Gerr6 (G = 3.636)	-1.5	—	1.5	%	
	Gerr7 (G = 4.000)	-1.5	—	1.5	%	
	Gerr8 (G = 4.444)	-2.0	—	2.0	%	
	Gerr9 (G = 5.000)	-2.0	—	2.0	%	
	Gerr10 (G = 5.714)	-2.0	—	2.0	%	
	Gerr11 (G = 6.667)	-2.0	—	2.0	%	
	Gerr12 (G = 8.000)	-2.0	—	2.0	%	
	Gerr13 (G = 10.000)	-2.0	—	2.0	%	
	Gerr14 (G = 13.333)	-2.0	—	2.0	%	
运行稳定时间	t_{start}	—	—	5	µs	

注1.用下列公式计算。（n=0到14）
PGAOUTn = AINn × G
实际输出范围包括增益误差。
PGAOUTn = (AINn × G) × (Gerr + 100%)

Table 46.42 差模下的PGA特性

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
偏移误差		Voff	-20	—	20	mV	
PGAVSS输入电压范围		PGAVSS	-0.5	—	0.3	V	
差分输入电压范围	G = 1.500	AIN-PGAVSS	-0.5	—	0.5	V	
	G = 2.333		-0.4	—	0.4	V	
	G = 4.000		-0.2	—	0.2	V	
	G = 5.667		-0.15	—	0.15	V	
输出电压范围*1	G = 1.500	V_{OR}	0.600	—	2.550	V	
	G = 2.333		0.417	—	2.733	V	
	G = 4.000		0.550	—	2.600	V	
	G = 5.667		0.500	—	2.650	V	
增益误差	G = 1.500	Gerr	-1.0	—	1.0	%	
	G = 2.333		-1.0	—	1.0	%	
	G = 4.000		-1.0	—	1.0	%	
	G = 5.667		-1.0	—	1.0	%	
运行稳定时间		t_{start}	—	—	5	µs	

注1.用下列公式计算。
V_{OR} = (AIN-PGAVSS) × G + (0.5 × AVCC0)
实际输出范围包括增益误差。
V_{OR} = (AIN-PGAVSS) × G × (Gerr +100%) + (0.5 × AVCC0)

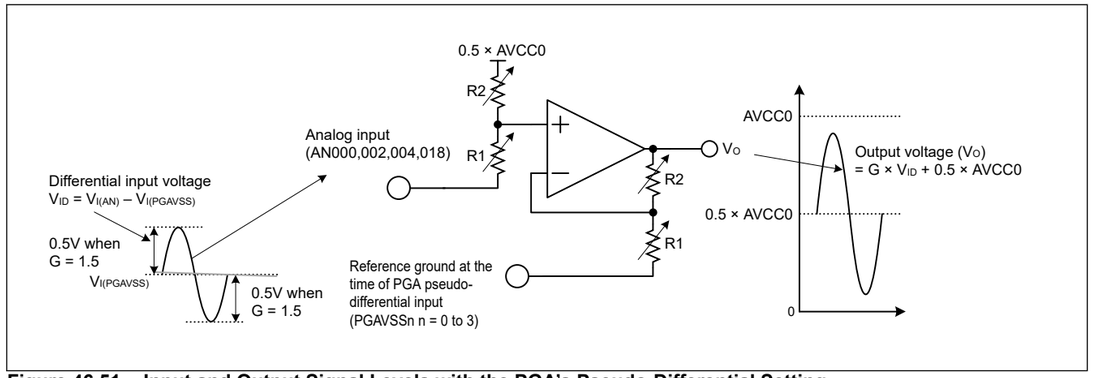


Figure 46.51 Input and Output Signal Levels with the PGA's Pseudo-Differential Setting

46.9 OSC Stop Detect Characteristics

Table 46.43 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 46.52

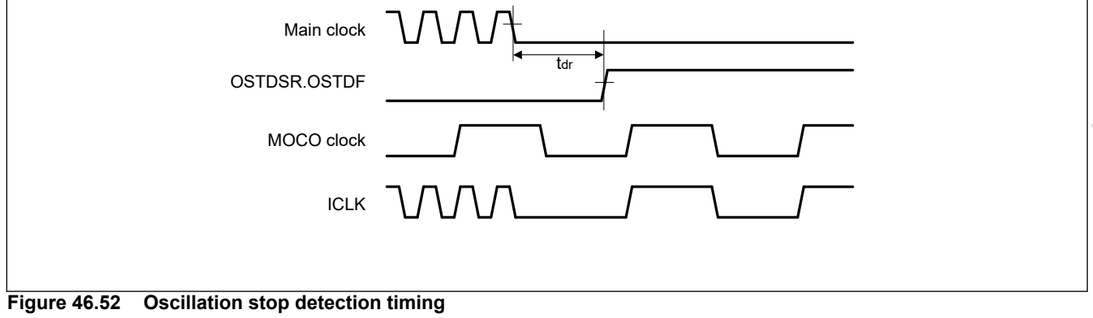


Figure 46.52 Oscillation stop detection timing

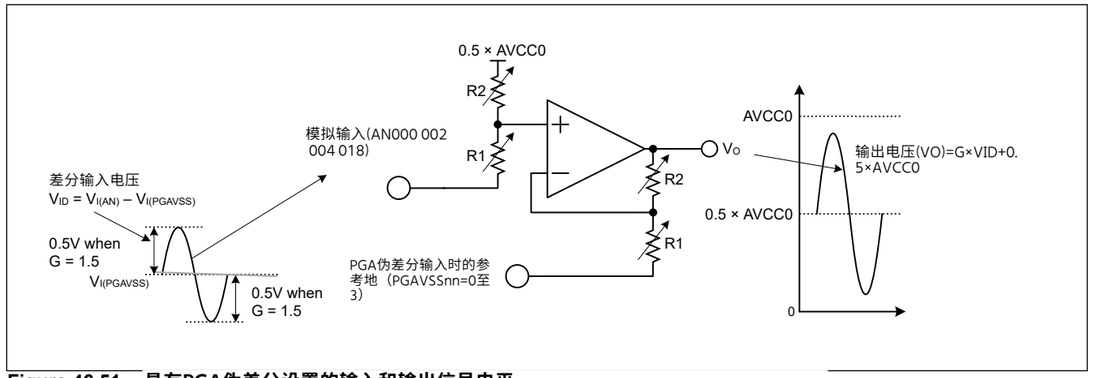


Figure 46.51 具有PGA伪差分设置的输入和输出信号电平

46.9 OSC停止检测特性

Table 46.43 振荡停止检测电路特性

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
检测时间	t_{dr}	—	—	1	ms	Figure 46.52

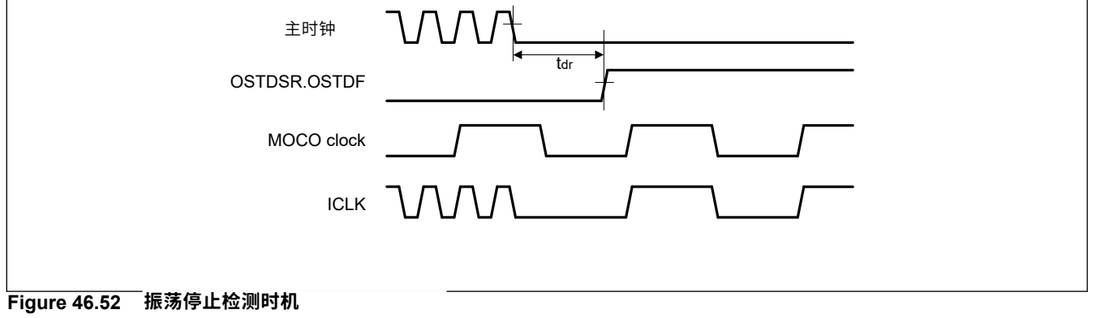


Figure 46.52 振荡停止检测时机

46.10 POR and LVD Characteristics

Table 46.44 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b.	V_{POR}	2.5	2.6	2.7	V	Figure 46.53
		DPSBYCR.DEEPCUT[1:0] = 11b.		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 46.54
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 46.55
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 46.56
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	—	4.5	—	ms	Figure 46.53
	LVD0 reset time		t_{LVD0}	—	0.51	—		Figure 46.54
	LVD1 reset time		t_{LVD1}	—	0.38	—		Figure 46.55
	LVD2 reset time		t_{LVD2}	—	0.38	—		Figure 46.56
Minimum VCC down time*1			t_{VOFF}	200	—	—	μs	Figure 46.53, Figure 46.54
Response delay			t_{det}	—	—	200	μs	Figure 46.54 to Figure 46.56
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	—	—	10	μs	Figure 46.55, Figure 46.56
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	70	—	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for POR and LVD.

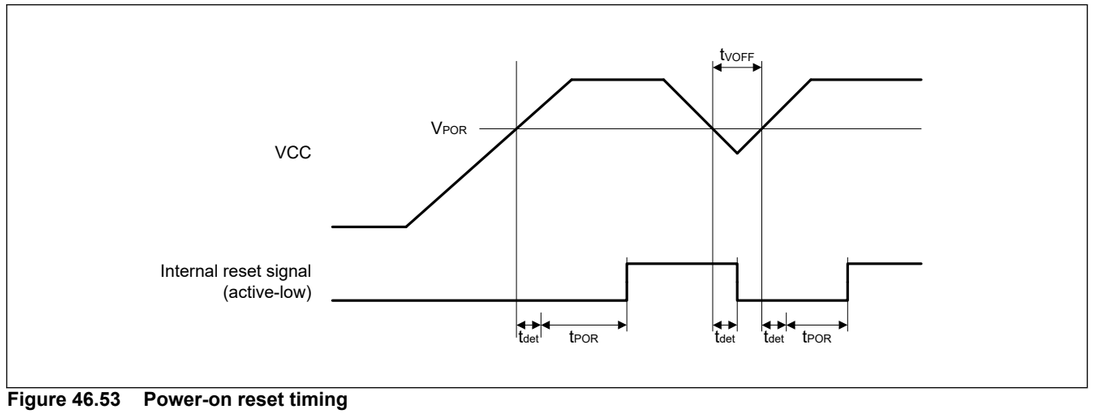


Figure 46.53 Power-on reset timing

46.10 POR和LVD特性

Table 46.44 上电复位电路及电压检测电路特性（一）

Parameter			Symbol	Min	Typ	Max	单元	测试条件
电压检测电平	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b.	V_{POR}	2.5	2.6	2.7	V	Figure 46.53
		DPSBYCR.DEEPCUT[1:0] = 11b.		1.8	2.25	2.7		
	电压检测电路（LVD0）		V_{det0_1}	2.84	2.94	3.04		Figure 46.54
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	电压检测电路（LVD1）		V_{det1_1}	2.89	2.99	3.09		Figure 46.55
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	电压检测电路（LVD2）		V_{det2_1}	2.89	2.99	3.09		Figure 46.56
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
内部复位时间	上电复位时间		t_{POR}	—	4.5	—	ms	Figure 46.53
	LVD0复位时间		t_{LVD0}	—	0.51	—		Figure 46.54
	LVD1复位时间		t_{LVD1}	—	0.38	—		Figure 46.55
	LVD2复位时间		t_{LVD2}	—	0.38	—		Figure 46.56
最小VCC停机时间*1			t_{VOFF}	200	—	—	μs	Figure 46.53, Figure 46.54
响应延迟			t_{det}	—	—	200	μs	图46.54至 Figure 46.56
LVD操作稳定时间（启用LVD后）			$t_{d(E-A)}$	—	—	10	μs	Figure 46.55, Figure 46.56
迟滞宽度（LVD1和LVD2）			V_{LVH}	—	70	—	mV	

注1.最小VCC停机时间是指VCC低于电压检测电平VPOR、Vdet0、Vdet1和Vdet2用于POR和LVD。

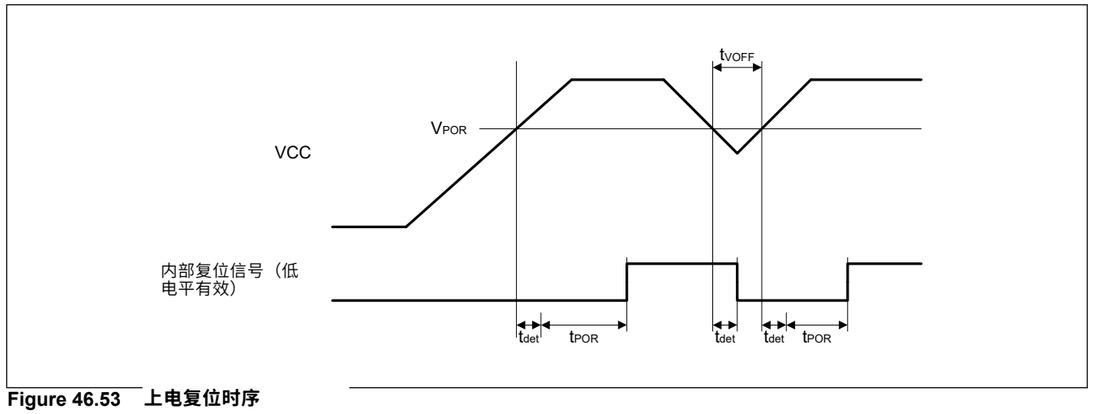


Figure 46.53 上电复位时序

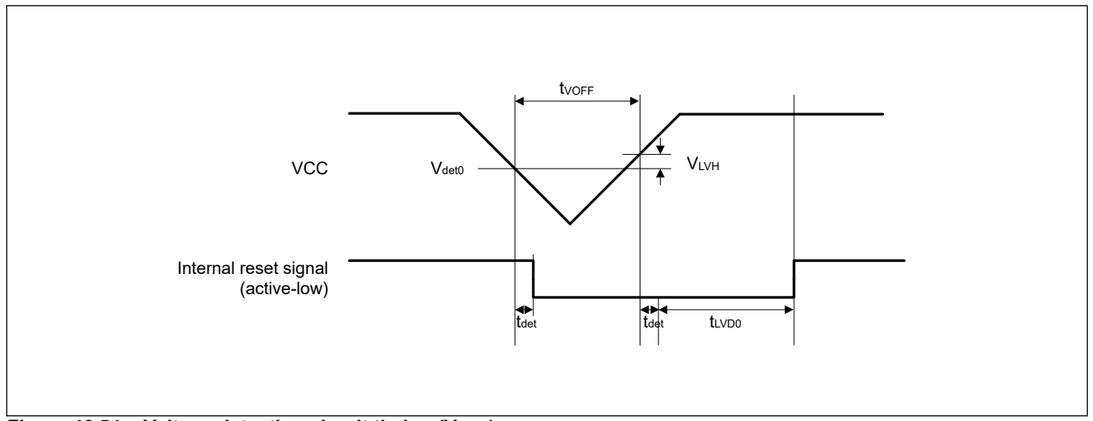


Figure 46.54 Voltage detection circuit timing (V_{det0})

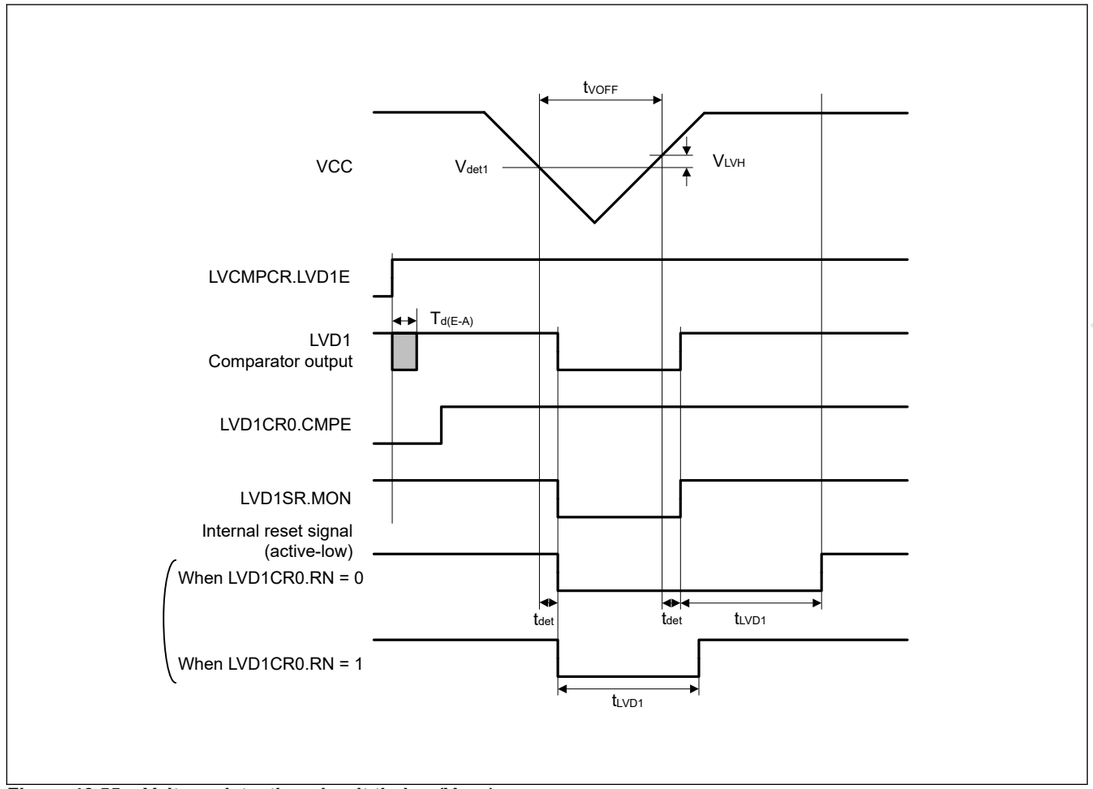


Figure 46.55 Voltage detection circuit timing (V_{det1})

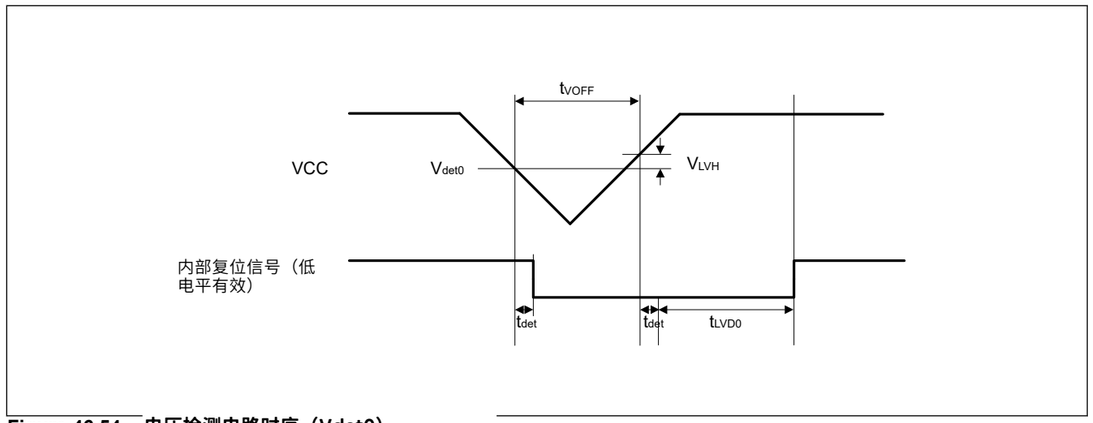


Figure 46.54 电压检测电路时序（Vdet0）

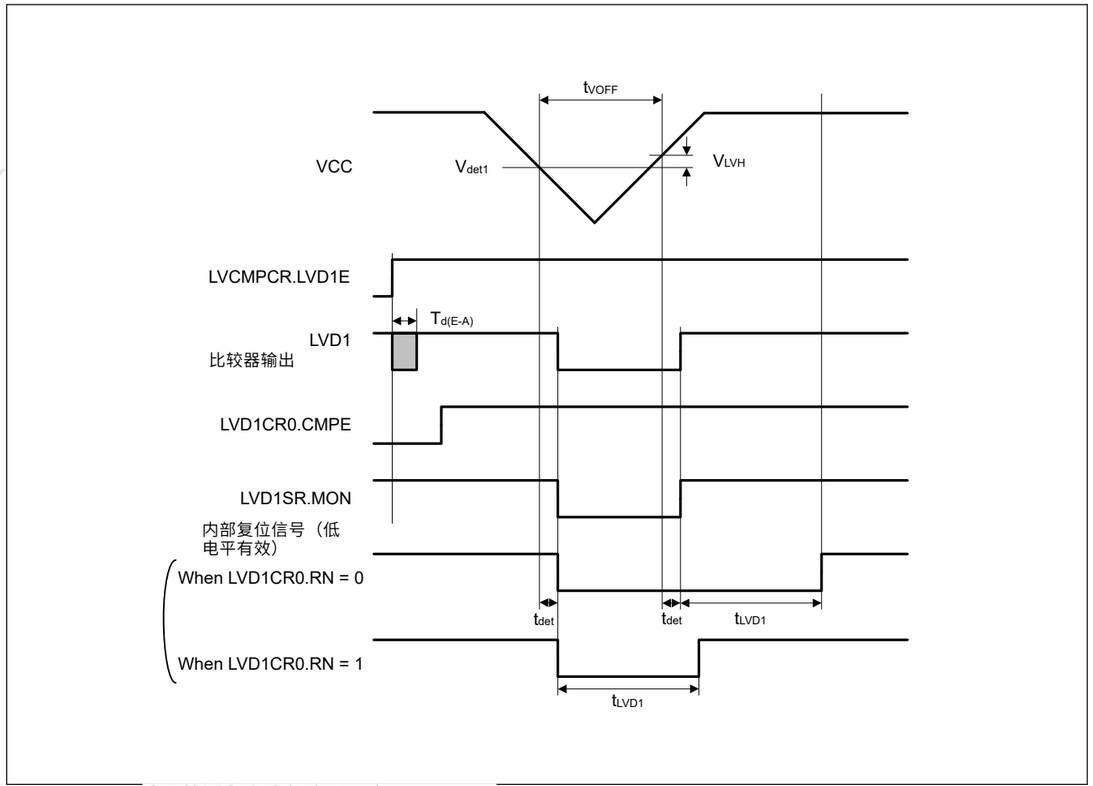


Figure 46.55 电压检测电路时序（Vdet1）

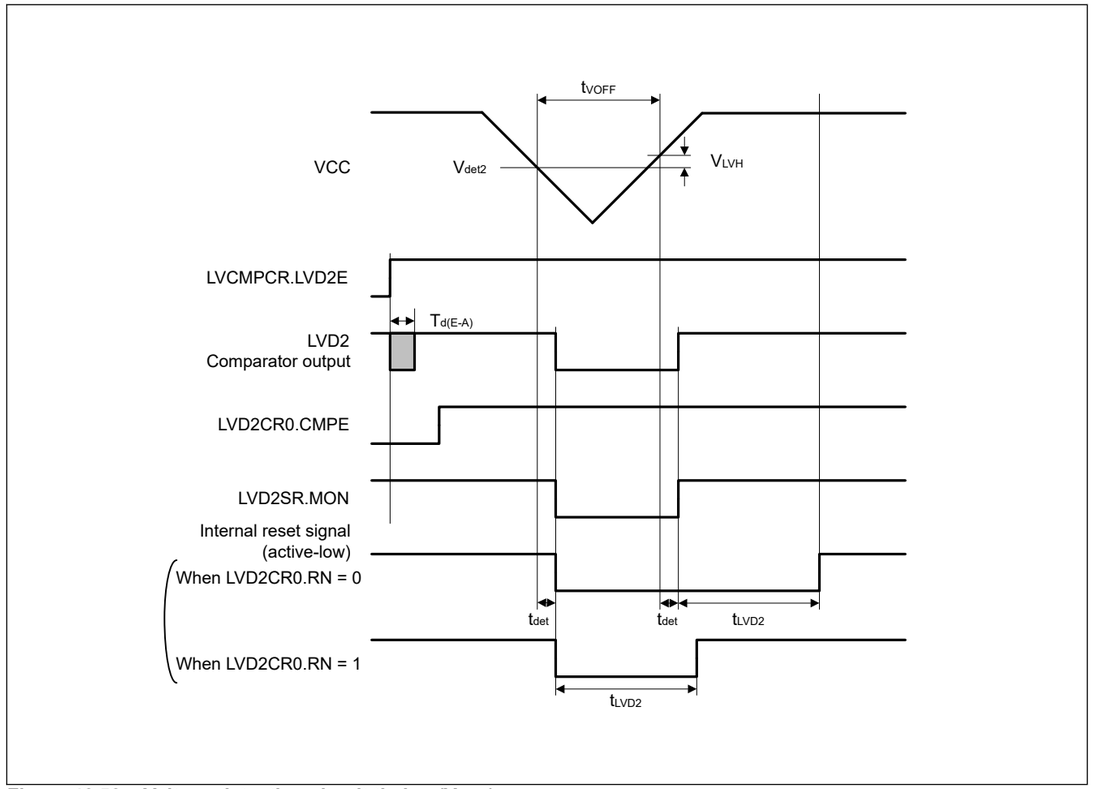


Figure 46.56 Voltage detection circuit timing (V_{det2})

46.11 Flash Memory Characteristics

46.11.1 Code Flash Memory Characteristics

Table 46.45 Code flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time N_{PEC} ≤ 100 times	128-byte	t_{P128}	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t_{P8K}	—	49	176	—	22	80	ms	
	32-KB	t_{P32K}	—	194	704	—	88	320	ms	
Programming time N_{PEC} > 100 times	128-byte	t_{P128}	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t_{P8K}	—	60	212	—	27	96	ms	
	32-KB	t_{P32K}	—	234	848	—	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8-KB	t_{E8K}	—	78	216	—	43	120	ms	
	32-KB	t_{E32K}	—	283	864	—	157	480	ms	
Erasure time N_{PEC} > 100 times	8-KB	t_{E8K}	—	94	260	—	52	144	ms	
	32-KB	t_{E32K}	—	341	1040	—	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	—	—	10000*1	—	—	Times	

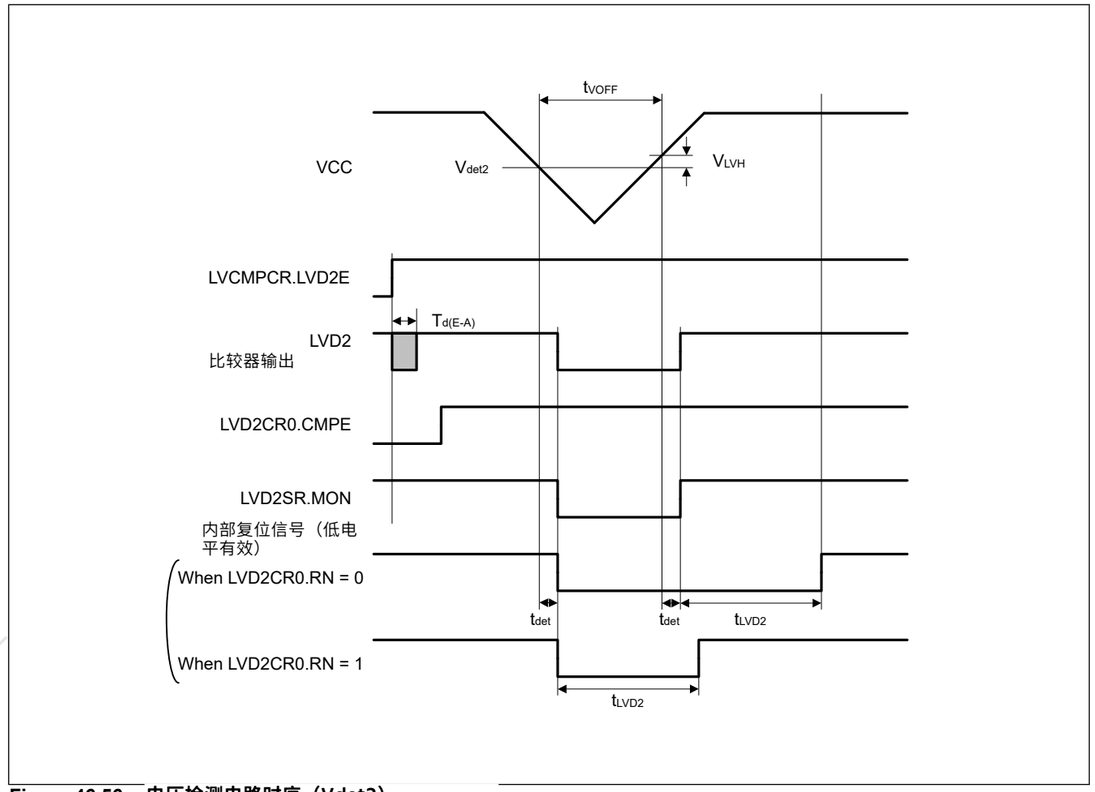


Figure 46.56 电压检测电路时序（Vdet2）

46.11 闪存特性

46.11.1 代码闪存特性

Table 46.45 代码闪存特性(1of2)

条件：编程或擦除：FCLK=4至60MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	测试条件
			Min	Typ*6	Max	Min	Typ*6	Max		
编程时间NPEC≤100次	128-byte	t_{P128}	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t_{P8K}	—	49	176	—	22	80	ms	
	32-KB	t_{P32K}	—	194	704	—	88	320	ms	
编程时间NPEC>100次	128-byte	t_{P128}	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t_{P8K}	—	60	212	—	27	96	ms	
	32-KB	t_{P32K}	—	234	848	—	106	384	ms	
擦除时间 NPEC≤100次	8-KB	t_{E8K}	—	78	216	—	43	120	ms	
	32-KB	t_{E32K}	—	283	864	—	157	480	ms	
擦除时间 NPEC>100次	8-KB	t_{E8K}	—	94	260	—	52	144	ms	
	32-KB	t_{E32K}	—	341	1040	—	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	—	—	10000*1	—	—	Times	

Table 46.45 Code flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
		Min	Typ*6	Max	Min	Typ*6	Max		
Suspend delay during programming	t_{SPD}	—	—	264	—	—	120	µs	
Programming resume time	t_{PRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode	t_{SESD1}	—	—	216	—	—	120	µs	
Second suspend delay during erasure in suspend priority mode	t_{SESD2}	—	—	1.7	—	—	1.7	ms	
Suspend delay during erasure in erasure priority mode	t_{SEED}	—	—	1.7	—	—	1.7	ms	
First erasing resume time during erasure in suspend priority mode*5	t_{REST1}	—	—	1.7	—	—	1.7	ms	
Second erasing resume time during erasure in suspend priority mode	t_{REST2}	—	—	144	—	—	80	µs	
Erasing resume time during erasure in erasure priority mode	t_{REET}	—	—	144	—	—	80	µs	
Forced stop command	t_{FD}	—	—	32	—	—	20	µs	
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3V and room temperature.

Table 46.45 代码闪存特性(2of2)

条件：编程或擦除：FCLK=4至60MHz
Read: FCLK ≤ 60 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	测试条件
		Min	Typ*6	Max	Min	Typ*6	Max		
编程期间暂停延迟	t_{SPD}	—	—	264	—	—	120	µs	
编程恢复时间	t_{PRT}	—	—	110	—	—	50	µs	
挂起优先模式下擦除期间的第一个挂起延迟	t_{SESD1}	—	—	216	—	—	120	µs	
挂起优先模式下擦除期间的第二挂起延迟	t_{SESD2}	—	—	1.7	—	—	1.7	ms	
擦除优先模式下擦除期间的挂起延迟	t_{SEED}	—	—	1.7	—	—	1.7	ms	
挂起优先模式擦除期间的第一次擦除恢复时间*5	t_{REST1}	—	—	1.7	—	—	1.7	ms	
挂起优先模式下擦除期间的第二次擦除恢复时间	t_{REST2}	—	—	144	—	—	80	µs	
在擦除优先模式下擦除期间擦除恢复时间	t_{REET}	—	—	144	—	—	80	µs	
强制停止命令	t_{FD}	—	—	32	—	—	20	µs	
数据保持时间*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

注1.这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。
注2.这表示在指定范围内执行重新编程时特性的最小值。
注3：此结果来自可靠性测试。
注4.重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=10 000）时，可以对每个块执行n次擦除。例如，当对8KB块中的不同地址执行64次128字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。禁止覆盖。

注5.恢复时间包括重新应用暂停时切断的擦除脉冲（最多1个完整脉冲）的时间。
注6.VCC=3.3V和室温下的参考值。

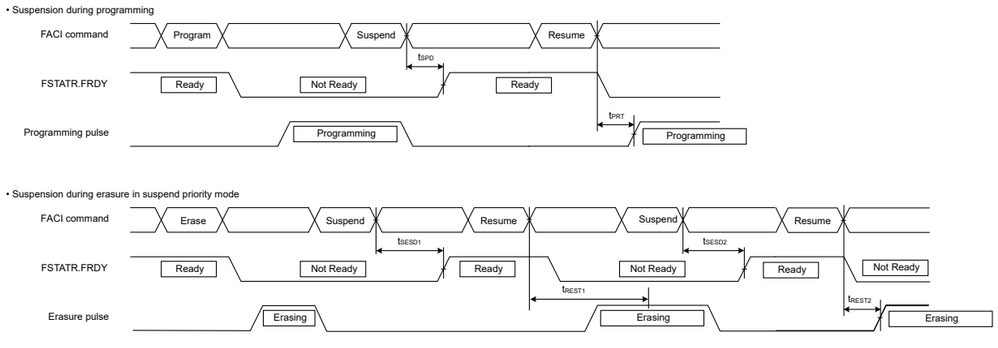


Figure 46.57 Suspension and forced stop timing for flash memory programming and erasure

46.11.2 Data Flash Memory Characteristics

Table 46.46 Data flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time	4-byte	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
	8-byte	t_{DP8}	—	0.38	4.0	—	0.17	1.8		
	16-byte	t_{DP16}	—	0.42	4.5	—	0.19	2.0		
Erasure time	64-byte	t_{DE64}	—	3.1	18	—	1.7	10	ms	
	128-byte	t_{DE128}	—	4.7	27	—	2.6	15		
	256-byte	t_{DE256}	—	8.9	50	—	4.9	28		
Blank check time	4-byte	t_{DBC4}	—	—	84	—	—	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	—	—	125000*2	—	—	—	
Suspend delay during programming	4-byte	t_{DSPD}	—	—	264	—	—	120	µs	
	8-byte		—	—	264	—	—	120		
	16-byte		—	—	264	—	—	120		
Programming resume time		t_{DPRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	—	—	216	—	—	120	µs	
	128-byte		—	—	216	—	—	120		
	256-byte		—	—	216	—	—	120		

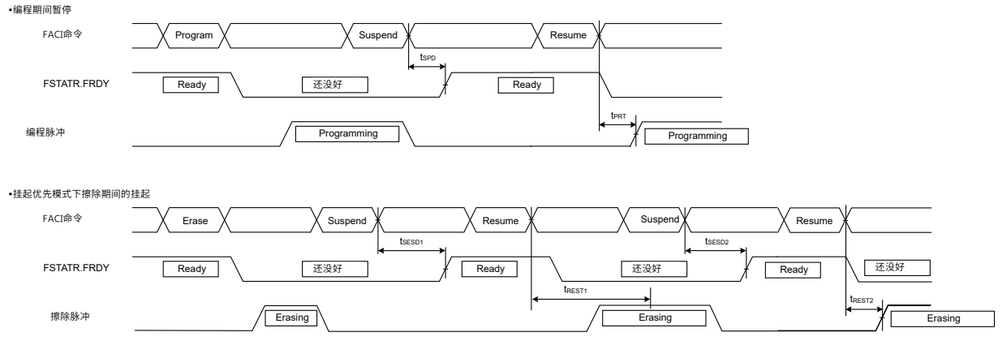


Figure 46.57 闪存编程和擦除的暂停和强制停止时序

46.11.2 数据闪存特性

Table 46.46 数据闪存特性(1of2)

条件：编程或擦除：FCLK=4至60MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	测试条件
			Min	典型*6最大值最小值			Typ*6	Max		
编程时间	4-byte	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
	8-byte	t_{DP8}	—	0.38	4.0	—	0.17	1.8		
	16-byte	t_{DP16}	—	0.42	4.5	—	0.19	2.0		
擦除时间	64-byte	t_{DE64}	—	3.1	18	—	1.7	10	ms	
	128-byte	t_{DE128}	—	4.7	27	—	2.6	15		
	256-byte	t_{DE256}	—	8.9	50	—	4.9	28		
空白检查时间	4-byte	t_{DBC4}	—	—	84	—	—	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	—	—	125000*2	—	—	—	
编程期间暂停延迟	4-byte	t_{DSPD}	—	—	264	—	—	120	µs	
	8-byte		—	—	264	—	—	120		
	16-byte		—	—	264	—	—	120		
编程恢复时间		t_{DPRT}	—	—	110	—	—	50	µs	
挂起优先模式下擦除期间的第一个挂起延迟	64-byte	t_{DSESD1}	—	—	216	—	—	120	µs	
	128-byte		—	—	216	—	—	120		
	256-byte		—	—	216	—	—	120		

Table 46.46 Data flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	—	—	300	—	—	300	µs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	—	—	300	—	—	300	µs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
First erasing resume time during erasure in suspend priority mode*5		t_{DREST1}	—	—	300	—	—	300	µs	
Second erasing resume time during erasure in suspend priority modeFirst erasing resume time during erasure in suspend priority mode		t_{DREST2}	—	—	126	—	—	70	µs	
Erasing resume time during erasure in erasure priority mode		t_{DREET}	—	—	126	—	—	70	µs	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*3		t_{DRP}	10*3 *4	—	—	10*3 *4	—	—	Year	
			30*3 *4	—	—	30*3 *4	—	—		Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3 V and room temperature.

46.11.3 Option Setting Memory Characteristics

Table 46.47 Option setting memory characteristics

Conditions: Program: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Programming time N_{OPC} ≤ 100 times	t_{OP}	—	83	309	—	45	162	ms	
Programming time N_{OPC} > 100 times	t_{OP}	—	100	371	—	55	195	ms	
Reprogramming cycle	N_{OPC}	20000*1	—	—	20000*1	—	—	Times	
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reference value at VCC = 3.3 V and room temperature.

46.12 Boundary Scan

Table 46.46 数据闪存特性(2of2)

条件：编程或擦除：FCLK=4至60MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	测试条件
			Min	典型*6最大值最小值			Typ*6	Max		
挂起优先模式下擦除期间的第二挂起延迟	64-byte	t_{DSESD2}	—	—	300	—	—	300	µs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
在擦除优先模式下擦除期间暂停延迟	64-byte	t_{DSEED}	—	—	300	—	—	300	µs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
挂起优先模式擦除期间的第一次擦除恢复时间*5		t_{DREST1}	—	—	300	—	—	300	µs	
挂起优先模式下擦除期间的第二次擦除恢复时间挂起优先模式下擦除期间的第二次擦除恢复时间		t_{DREST2}	—	—	126	—	—	70	µs	
在擦除优先模式下擦除期间擦除恢复时间		t_{DREET}	—	—	126	—	—	70	µs	
强制停止命令		t_{FD}	—	—	32	—	—	20	µs	
数据保持时间*3		t_{DRP}	10*3 *4	—	—	10*3 *4	—	—	Year	
			30*3 *4	—	—	30*3 *4	—	—		Ta = +85°C

注1.重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=125 000）时，可以对每个块执行n次擦除。例如，当对64字节块中的不同地址执行16次4字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。禁止覆盖。
注2.这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。
注3.这表示在指定范围内执行重新编程时特性的最小值。
注4：此结果来自可靠性测试。
注5.恢复时间包括重新应用暂停时切断的擦除脉冲（最多1个完整脉冲）的时间。
注6.VCC=3.3V和室温下的参考值。

46.11.3 选项设置内存特性

Table 46.47 选项设置内存特性

Conditions: Program: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	测试条件
		Min	Typ*4	Max	Min	Typ*4	Max		
编程时间NOPC≤100次	t_{OP}	—	83	309	—	45	162	ms	
编程时间NOPC>100次	t_{OP}	—	100	371	—	55	195	ms	
重编程周期	N_{OPC}	20000*1	—	—	20000*1	—	—	Times	
数据保持时间*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

注1.这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。
注2.这表示在指定范围内执行重新编程时特性的最小值。
注3：此结果来自可靠性测试。
注4.VCC=3.3V和室温下的参考值。

46.12 边界扫描

Table 46.48 Boundary scan characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 46.58
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 46.59
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay	t_{TDOD}	—	—	40	ns	
Boundary scan circuit startup time*1	T_{BSSTUP}	t_{RESWP}	—	—	—	Figure 46.60

Note 1. Boundary scan does not function until the power-on reset becomes negative.

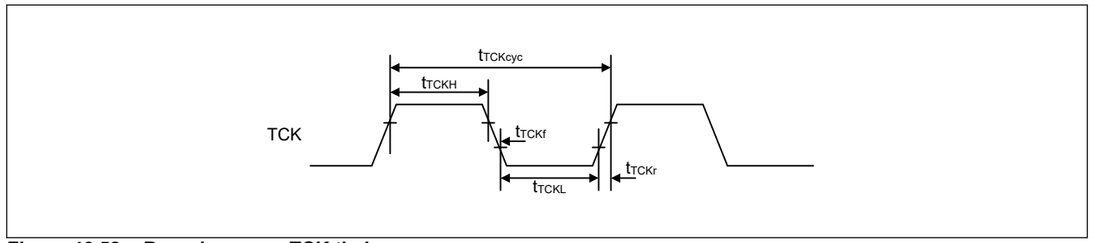


Figure 46.58 Boundary scan TCK timing

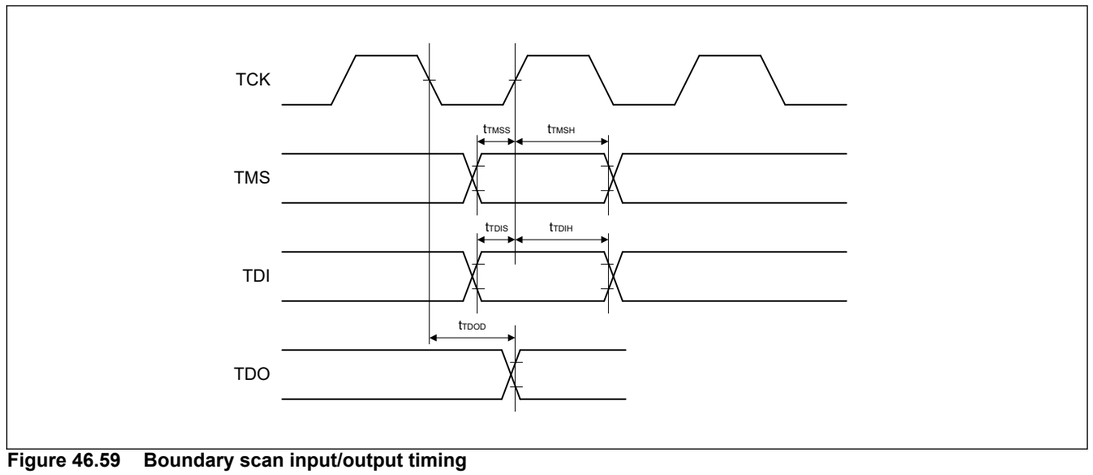


Figure 46.59 Boundary scan input/output timing

Table 46.48 边界扫描特性

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCK时钟周期时间	t_{TCKcyc}	100	—	—	ns	Figure 46.58
TCK时钟高脉冲宽度	t_{TCKH}	45	—	—	ns	
TCK时钟低脉冲宽度	t_{TCKL}	45	—	—	ns	
TCK时钟上升时间	t_{TCKr}	—	—	5	ns	
TCK时钟下降时间	t_{TCKf}	—	—	5	ns	
TMS设置时间	t_{TMSS}	20	—	—	ns	Figure 46.59
TMS保持时间	t_{TMSH}	20	—	—	ns	
TDI建立时间	t_{TDIS}	20	—	—	ns	
TDI保持时间	t_{TDIH}	20	—	—	ns	
TDO数据延迟	t_{TDOD}	—	—	40	ns	
边界扫描电路启动时间*1	T_{BSSTUP}	t_{RESWP}	—	—	—	Figure 46.60

注1.在上电复位变为负值之前，边界扫描不起作用。

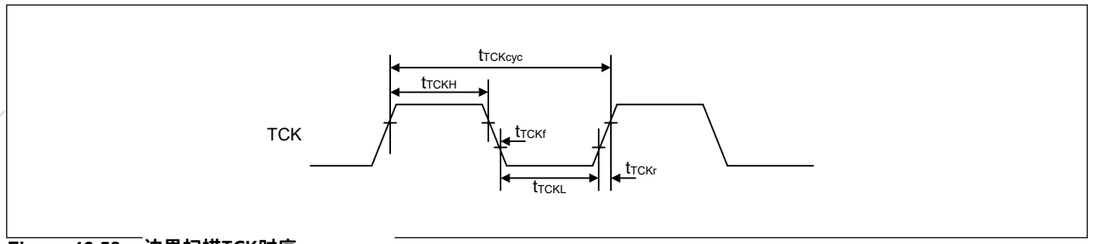


Figure 46.58 边界扫描TCK时序

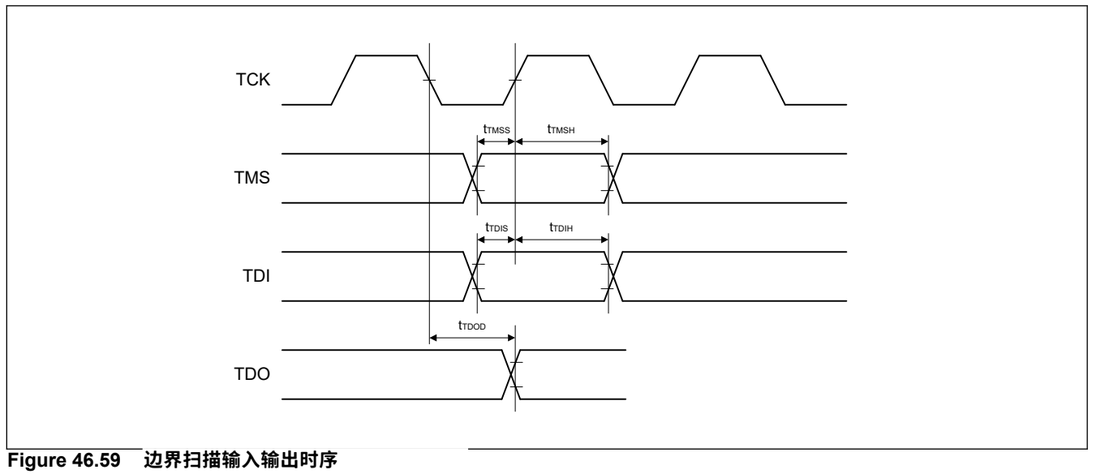


Figure 46.59 边界扫描输入输出时序

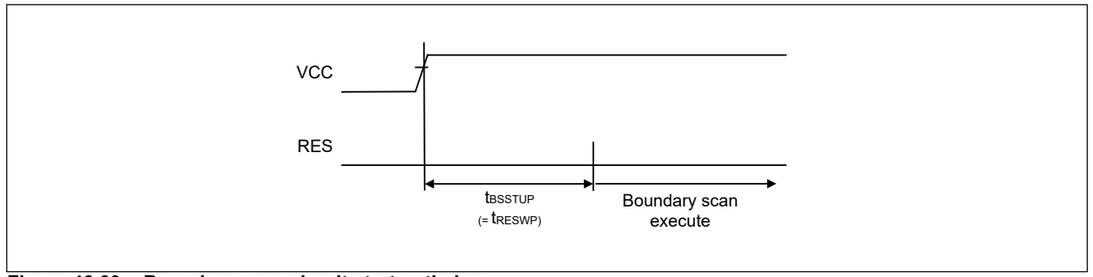


Figure 46.60 Boundary scan circuit startup timing

46.13 Joint Test Action Group (JTAG)

Table 46.49 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	40	—	—	ns	Figure 46.61
TCK clock high pulse width	t_{TCKH}	15	—	—	ns	
TCK clock low pulse width	t_{TCKL}	15	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TMS setup time	t_{TMSS}	8	—	—	ns	Figure 46.62
TMS hold time	t_{TMSH}	8	—	—	ns	
TDI setup time	t_{TDIS}	8	—	—	ns	
TDI hold time	t_{TDIH}	8	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	20	ns	

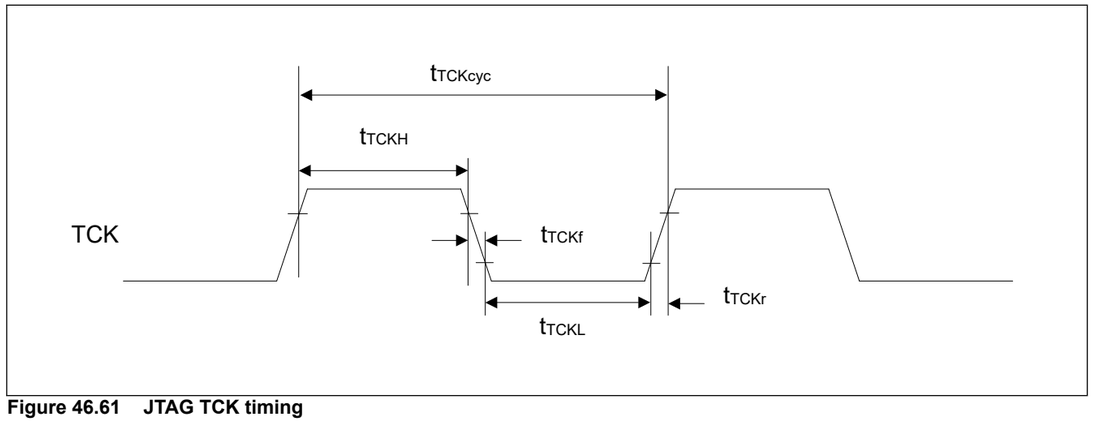


Figure 46.61 JTAG TCK timing

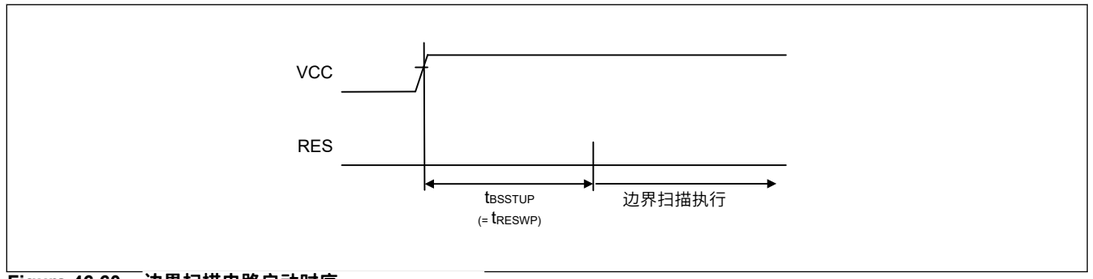


Figure 46.60 边界扫描电路启动时序

46.13 联合测试行动组(JTAG)

Table 46.49 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCK时钟周期时间	t_{TCKcyc}	40	—	—	ns	Figure 46.61
TCK时钟高脉冲宽度	t_{TCKH}	15	—	—	ns	
TCK时钟低脉冲宽度	t_{TCKL}	15	—	—	ns	
TCK时钟上升时间	t_{TCKr}	—	—	5	ns	
TCK时钟下降时间	t_{TCKf}	—	—	5	ns	
TMS设置时间	t_{TMSS}	8	—	—	ns	Figure 46.62
TMS保持时间	t_{TMSH}	8	—	—	ns	
TDI建立时间	t_{TDIS}	8	—	—	ns	
TDI保持时间	t_{TDIH}	8	—	—	ns	
TDO数据延迟时间	t_{TDOD}	—	—	20	ns	

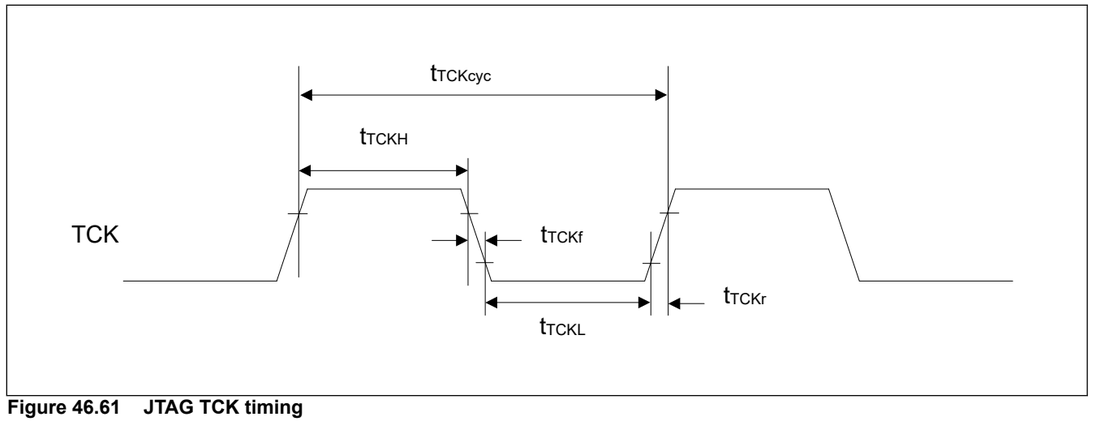


Figure 46.61 JTAG TCK timing

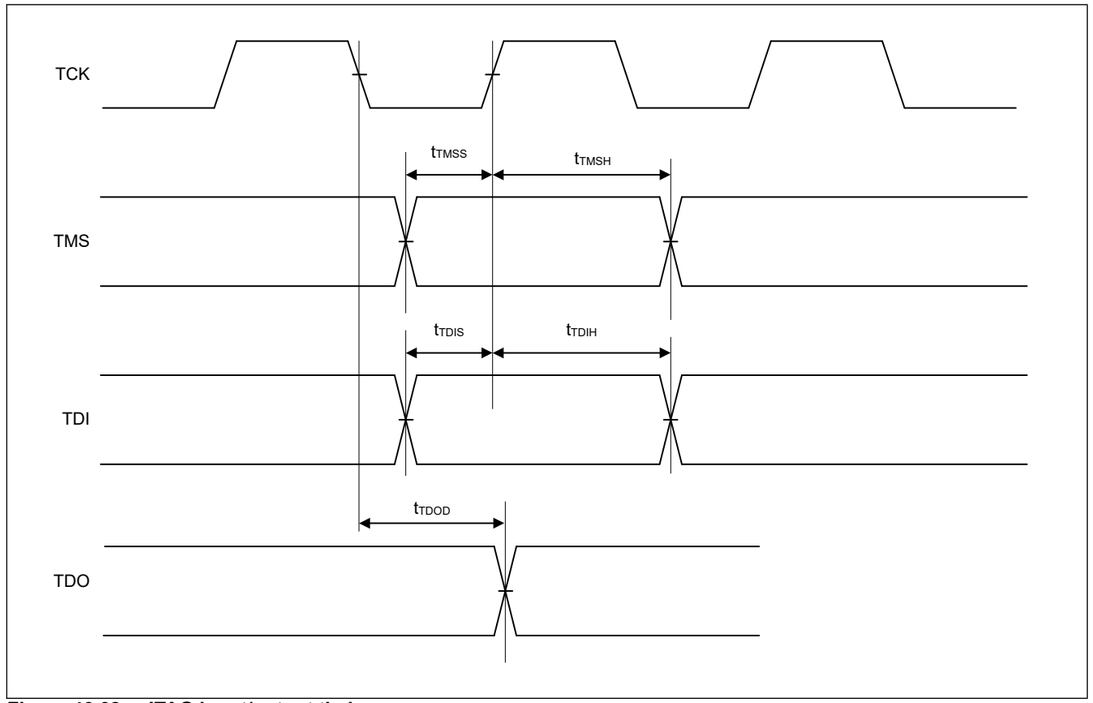


Figure 46.62 JTAG input/output timing

46.14 Serial Wire Debug (SWD)

Table 46.50 SWD

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	40	—	—	ns	Figure 46.63
SWCLK clock high pulse width	t_{SWCKH}	15	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	8	—	—	ns	Figure 46.64
SWDIO hold time	t_{SWDH}	8	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	28	ns	

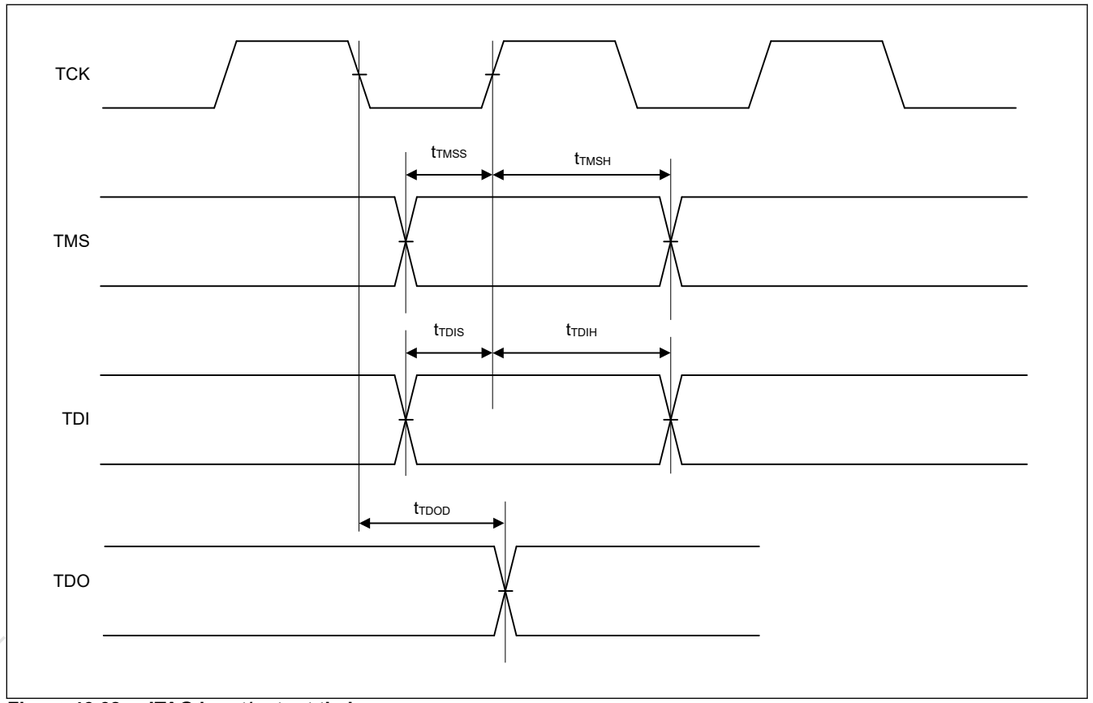


Figure 46.62 JTAG input/output timing

46.14 串行线调试(SWD)

Table 46.50 SWD

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWCLK时钟周期时间	$t_{SWCKcyc}$	40	—	—	ns	Figure 46.63
SWCLK时钟高脉冲宽度	t_{SWCKH}	15	—	—	ns	
SWCLK时钟低脉冲宽度	t_{SWCKL}	15	—	—	ns	
SWCLK时钟上升时间	t_{SWCKr}	—	—	5	ns	
SWCLK时钟下降时间	t_{SWCKf}	—	—	5	ns	
SWDIO设置时间	t_{SWDS}	8	—	—	ns	Figure 46.64
SWDIO保持时间	t_{SWDH}	8	—	—	ns	
SWDIO数据延迟时间	t_{SWDD}	2	—	28	ns	

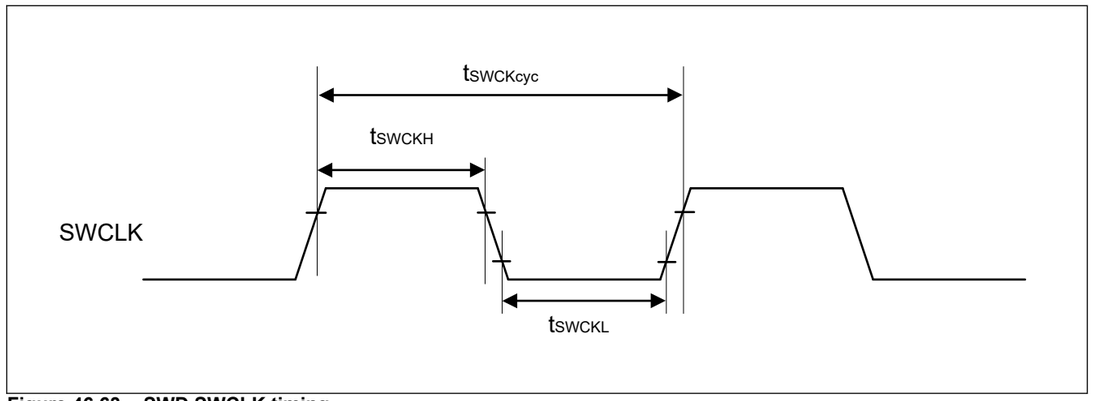


Figure 46.63 SWD SWCLK timing

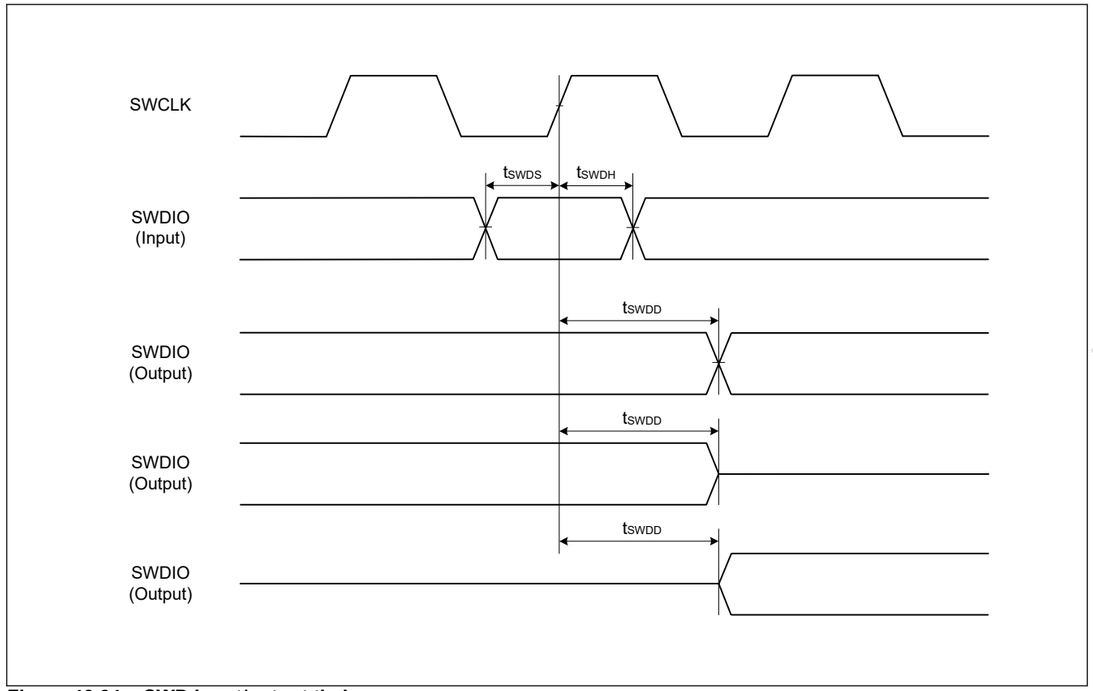


Figure 46.64 SWD input/output timing

46.15 Embedded Trace Macro Interface (ETM)

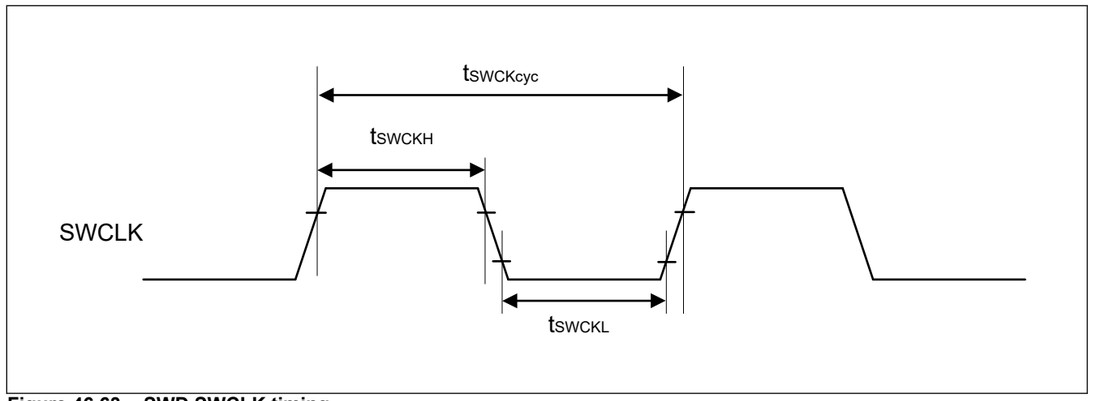


Figure 46.63 SWD SWCLK timing

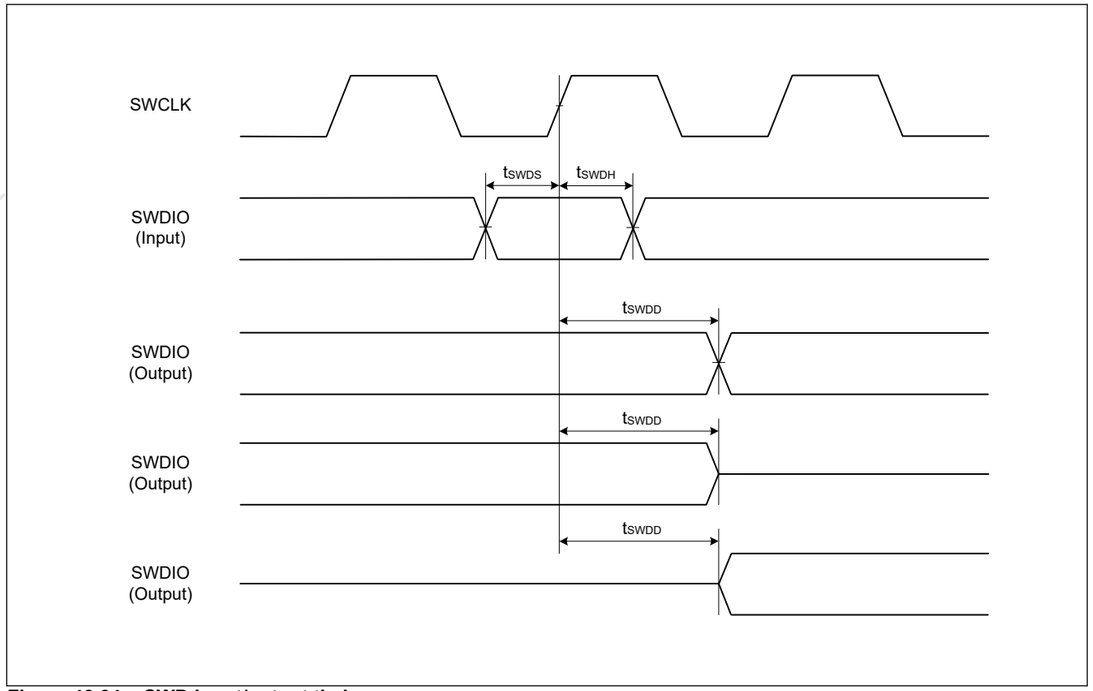


Figure 46.64 SWD input/output timing

46.15 嵌入式跟踪宏接口(ETM)

Table 46.51 ETM

Conditions: High speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCLK clock cycle time	$t_{TCLKcyc}$	16.7	—	—	ns	Figure 46.65
TCLK clock high pulse width	t_{TCLKH}	7.35	—	—	ns	
TCLK clock low pulse width	t_{TCLKL}	7.35	—	—	ns	
TCLK clock rise time	t_{TCLKr}	—	—	1	ns	
TCLK clock fall time	t_{TCLKf}	—	—	1	ns	
TDATA[3:0] output setup time	t_{TRDS}	2.5	—	—	ns	Figure 46.66
TDATA[3:0] output hold time	t_{TRDH}	1.5	—	—	ns	

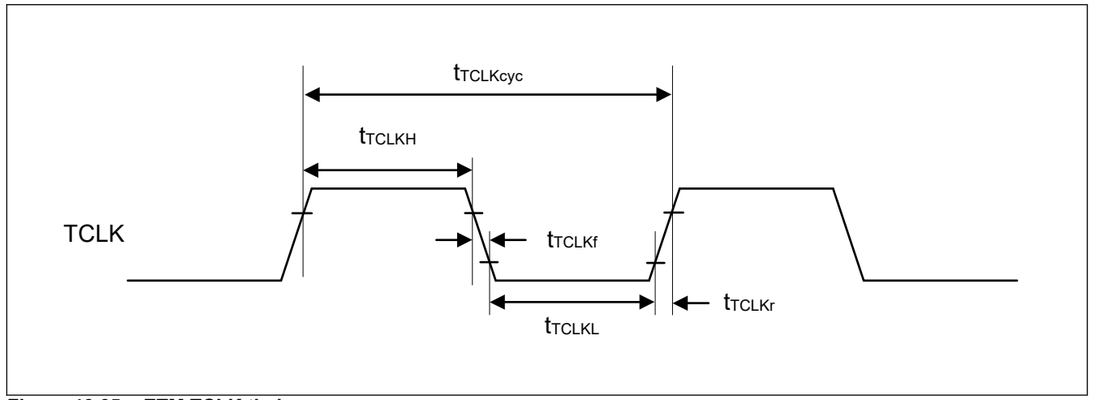


Figure 46.65 ETM TCLK timing

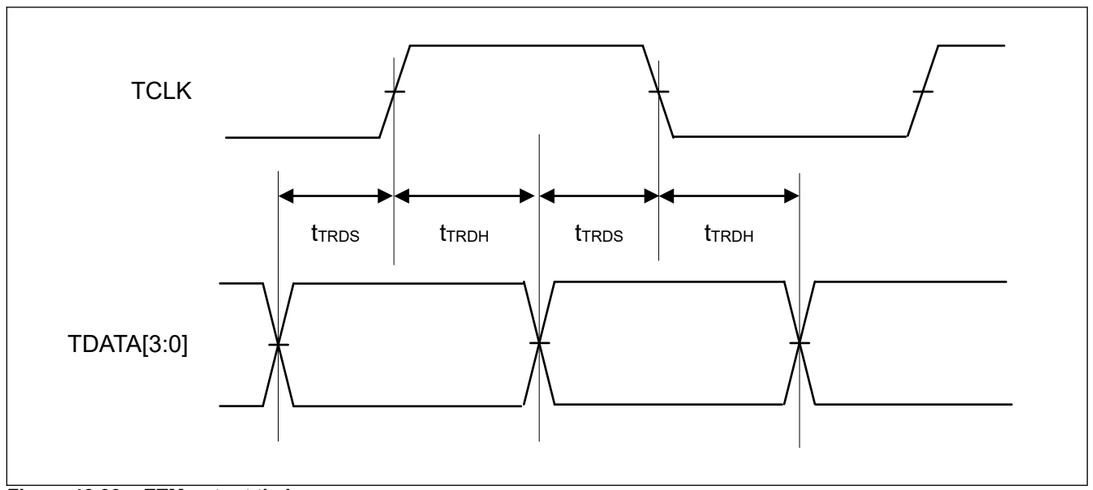


Figure 46.66 ETM output timing

Table 46.51 ETM

条件：在PmnPFS寄存器的端口驱动能力位中选择高速高驱动输出。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCLK时钟周期时间	$t_{TCLKcyc}$	16.7	—	—	ns	Figure 46.65
TCLK时钟高脉冲宽度	t_{TCLKH}	7.35	—	—	ns	
TCLK时钟低脉冲宽度	t_{TCLKL}	7.35	—	—	ns	
TCLK时钟上升时间	t_{TCLKr}	—	—	1	ns	
TCLK时钟下降时间	t_{TCLKf}	—	—	1	ns	
TDATA[3:0]输出建立时间	t_{TRDS}	2.5	—	—	ns	Figure 46.66
TDATA[3:0]输出保持时间	t_{TRDH}	1.5	—	—	ns	

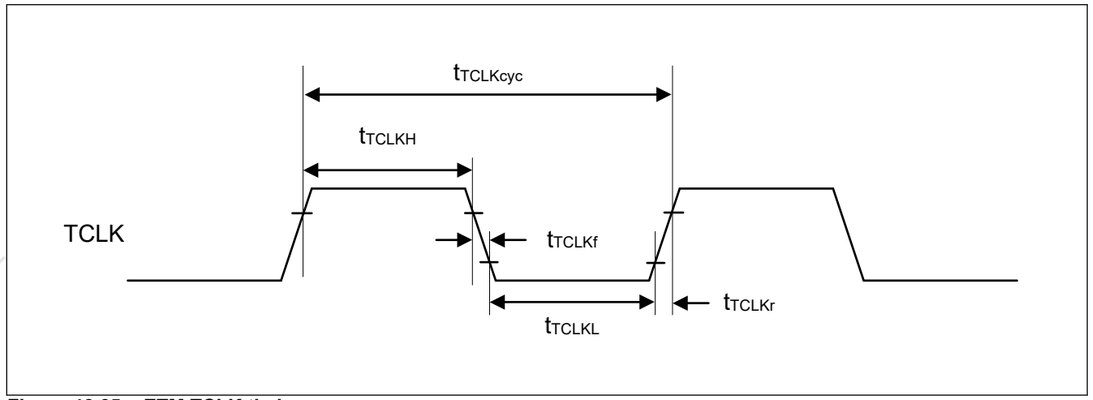


Figure 46.65 ETM TCLK timing

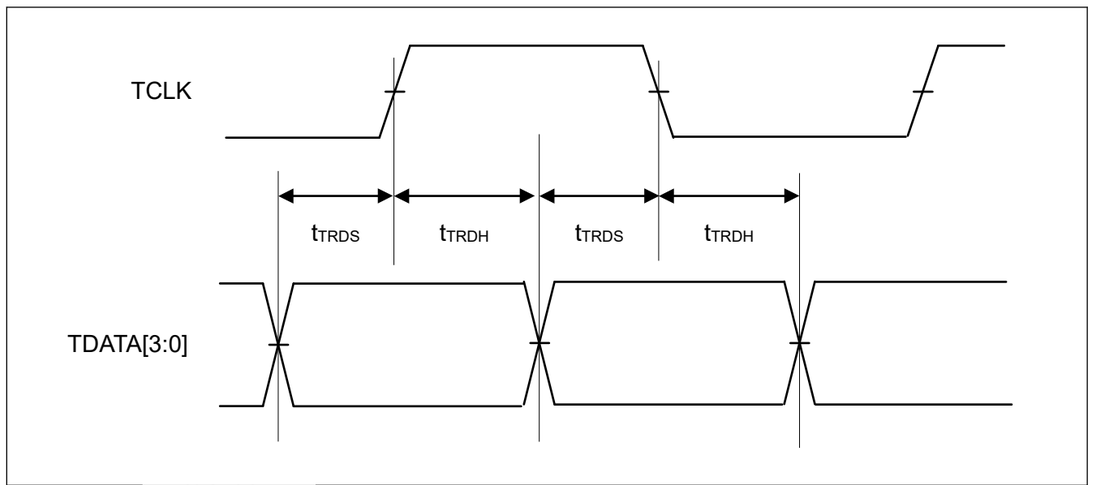


Figure 46.66 ETM输出时序

Appendix 1. Port States in Each Processing Mode

Function	Pin function	Reset	Software Standby mode	Deep Software Standby mode	After Deep Software Standby mode is canceled (return to startup mode)	
					IOKEEP = 0	IOKEEP = 1*1
Mode	MD	Pull-up	Keep-O	Keep	Hi-Z	Keep
JTAG	TCK/TMS/TDI	Pull-up	Keep-O	Keep	Hi-Z	Keep
	TDO	TDO output	Keep-O	Keep	TDO output	Keep
Trace	TCLK/TDATAx	Hi-Z	Keep-O	Keep	Hi-Z	Keep
IRQ	IRQx	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
	IRQx-DS	Hi-Z	Keep-O*2	Keep*3	Hi-Z	Keep
KINT	KRxx	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
AGT	AGTIOn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
IIC	SCLn/SDAn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
CLKOUT	CLKOUT	Hi-Z	[CLKOUT selected] CLKOUT output	Keep	Hi-Z	Keep
ACMPHS	VCOUT, CMPOUTm, CMPOUT012	Hi-Z	Hi-Z (Keep-O)	Hi-Z (Keep-O)	Hi-Z	Keep
	IVREFn	Hi-Z	Hi-Z (Keep-O)	Hi-Z (Keep-O)	Hi-Z	Hi-Z
	IVCMPmn	Hi-Z	Hi-Z (Keep-O)	Hi-Z (Keep-O)	Hi-Z	Hi-Z
DAC12	DAn	Hi-Z	[DAn output (DAOE = 1)] D/A output retained	Keep	Hi-Z	Keep
ADC	ANxxx	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	PGAINn	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	PGAVSSn	Pull-up*4	Pull-up*5 / Keep	Pull-up*5 / Keep	Pull-up*5 / Keep	Pull-up*5 / Keep
	PGAOUTn	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Others	—	Hi-Z	Keep-O	Keep	Hi-Z	Keep

Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Keep: Pin states are retained during periods in Software Standby mode.

Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.
Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.
Note 4. The built-in pull-up is turned on to protect the circuit from negative potential inputs.
Note 5. Regardless of whether the PGA is enabled or disabled, when the PGA is set to pseudo-differential mode, the built in pull-up is turned on to protect the circuit from negative potential inputs. To turn off the built-in pull-up, turn off the PGA's pseudo-differential mode and set it to single mode.

Appendix 1. 每种处理模式下的端口状态

Function	引脚功能	Reset	软件待机模式	深度软件待机模式	取消深度软件待机模式后（返回启动模式）	
					IOKEEP = 0	IOKEEP = 1*1
Mode	MD	Pull-up	Keep-O	Keep	Hi-Z	Keep
JTAG	TCK/TMS/TDI	Pull-up	Keep-O	Keep	Hi-Z	Keep
	TDO	TDO输出	Keep-O	Keep	TDO输出	Keep
Trace	TCLK/TDATAx	Hi-Z	Keep-O	Keep	Hi-Z	Keep
IRQ	IRQx	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
	IRQx-DS	Hi-Z	Keep-O*2	Keep*3	Hi-Z	Keep
KINT	KRxx	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
AGT	AGTIOn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
IIC	SCLn/SDAn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
CLKOUT	CLKOUT	Hi-Z	[CLKOUT selected] CLKOUT output	Keep	Hi-Z	Keep
ACMPHS	VCOUT, CMPOUTm, CMPOUT012	Hi-Z	Hi-Z (Keep-O)	Hi-Z (Keep-O)	Hi-Z	Keep
	IVREFn	Hi-Z	Hi-Z (Keep-O)	Hi-Z (Keep-O)	Hi-Z	Hi-Z
	IVCMPmn	Hi-Z	Hi-Z (Keep-O)	Hi-Z (Keep-O)	Hi-Z	Hi-Z
DAC12	DAn	Hi-Z	[DAn输出(DAOE=1)]DA 输出保留	Keep	Hi-Z	Keep
ADC	ANxxx	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	PGAINn	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	PGAVSSn	Pull-up*4	Pull-up*5 / Keep	Pull-up*5 / Keep	Pull-up*5 / Keep	Pull-up*5 / Keep
	PGAOUTn	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Others	—	Hi-Z	Keep-O	Keep	Hi-Z	Keep

Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O：输出引脚保留其先前的值。输入引脚变为高阻抗。
保持：在软件待机模式期间保持引脚状态。

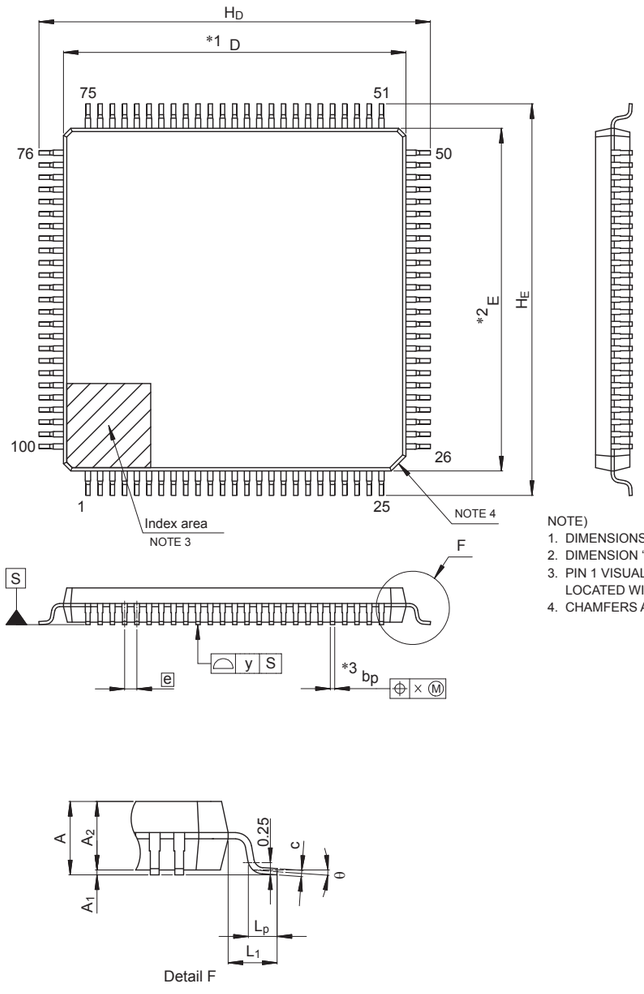
注1.保持IO端口状态直到DPSBYCR.IOKEEP位被清除为0。
注2.如果引脚被指定为软件待机取消源，同时它被用作外部中断引脚，则输入被启用。
注3.如果引脚被指定为深度软件待机取消源，则启用输入。
注4.内置上拉电阻打开以保护电路免受负电位输入的影响。
注5.无论PGA启用还是禁用，当PGA设置为伪差分模式时，内置上拉电阻会打开以保护电路免受负电位输入的影响。要关闭内置上拉，关闭PGA的伪差分模式并将其设置为单模式。

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in Packages on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

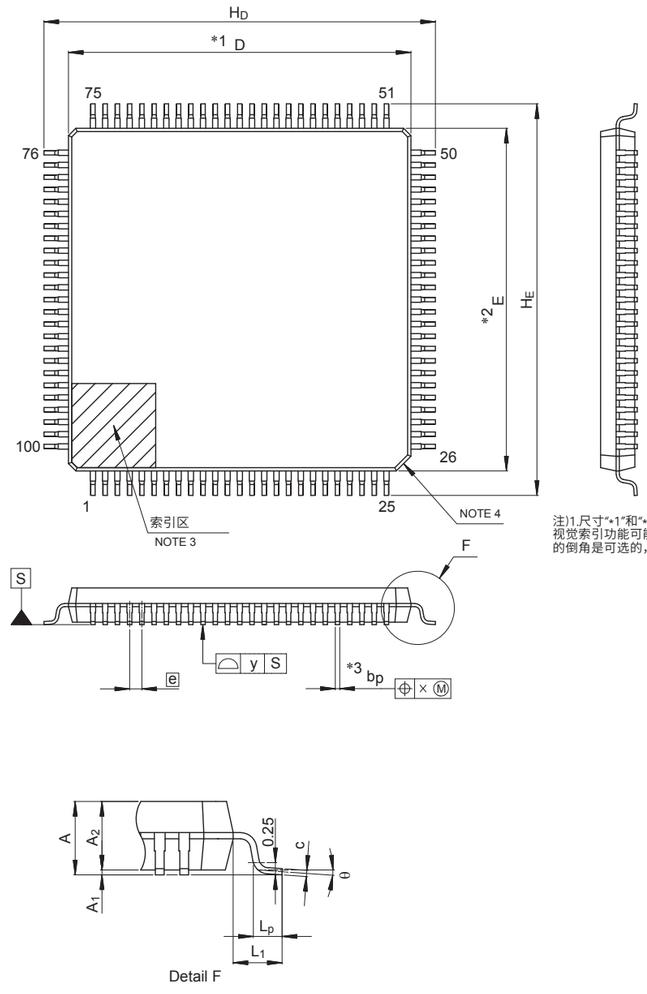
Figure 2.1 LQFP 100-pin

Appendix 2. 包装尺寸

最新版本的封装尺寸或安装信息显示在瑞萨的封装中
电子公司网站。

JEITA包装代码	RENESAS Code	以前的代码	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



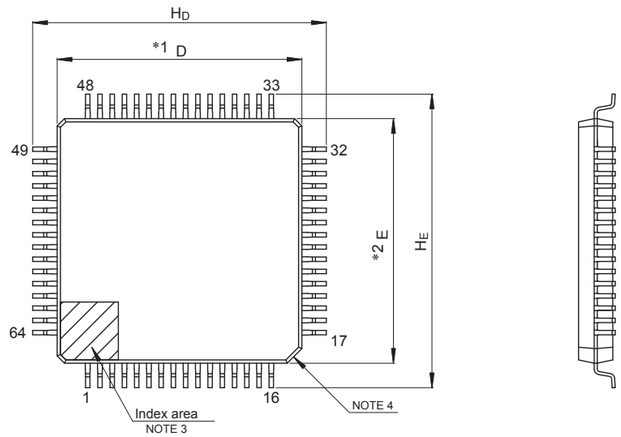
注)1.尺寸"*1"和"*2"不包括毛边。2.尺寸"*3"不包括微调偏移。3.PIN1视觉索引功能可能会有所不同，但必须位于阴影区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。

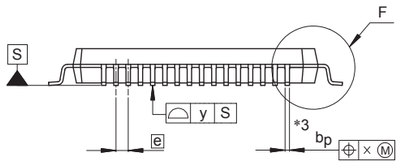
参考符号	尺寸以毫米为单位		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

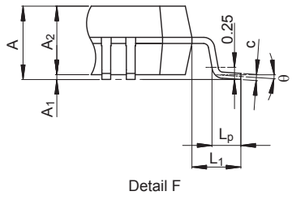
Figure 2.1 LQFP 100-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm







Detail F

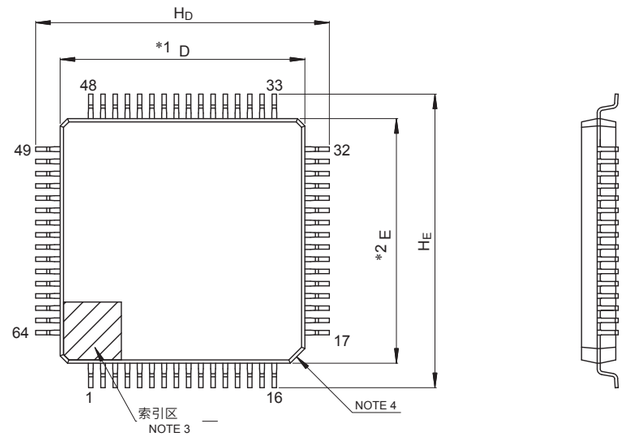
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

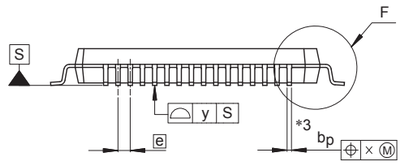
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

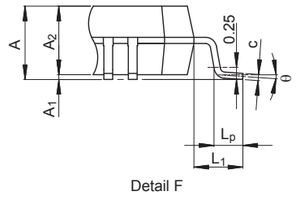
Figure 2.2 LQFP 64-pin

JEITA包装代码	RENESAS Code	以前的代码	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm







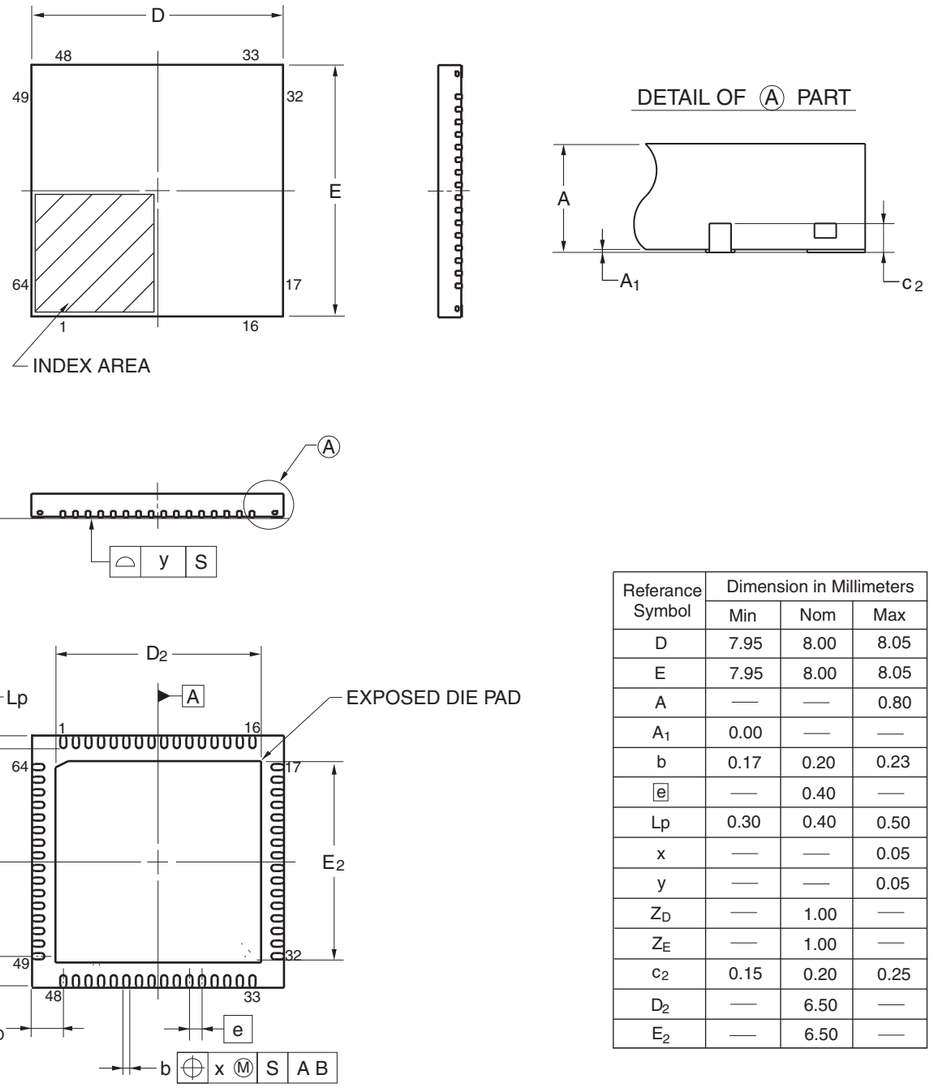
Detail F

注)1.尺寸"*1"和"*2"不包括毛边。2.尺寸"*3"不包括微调偏移。3.PIN1视觉索引功能可能会有所不同，但必须位于阴影区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。

参考符号	尺寸以毫米为单位		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 2.2 LQFP 64-pin

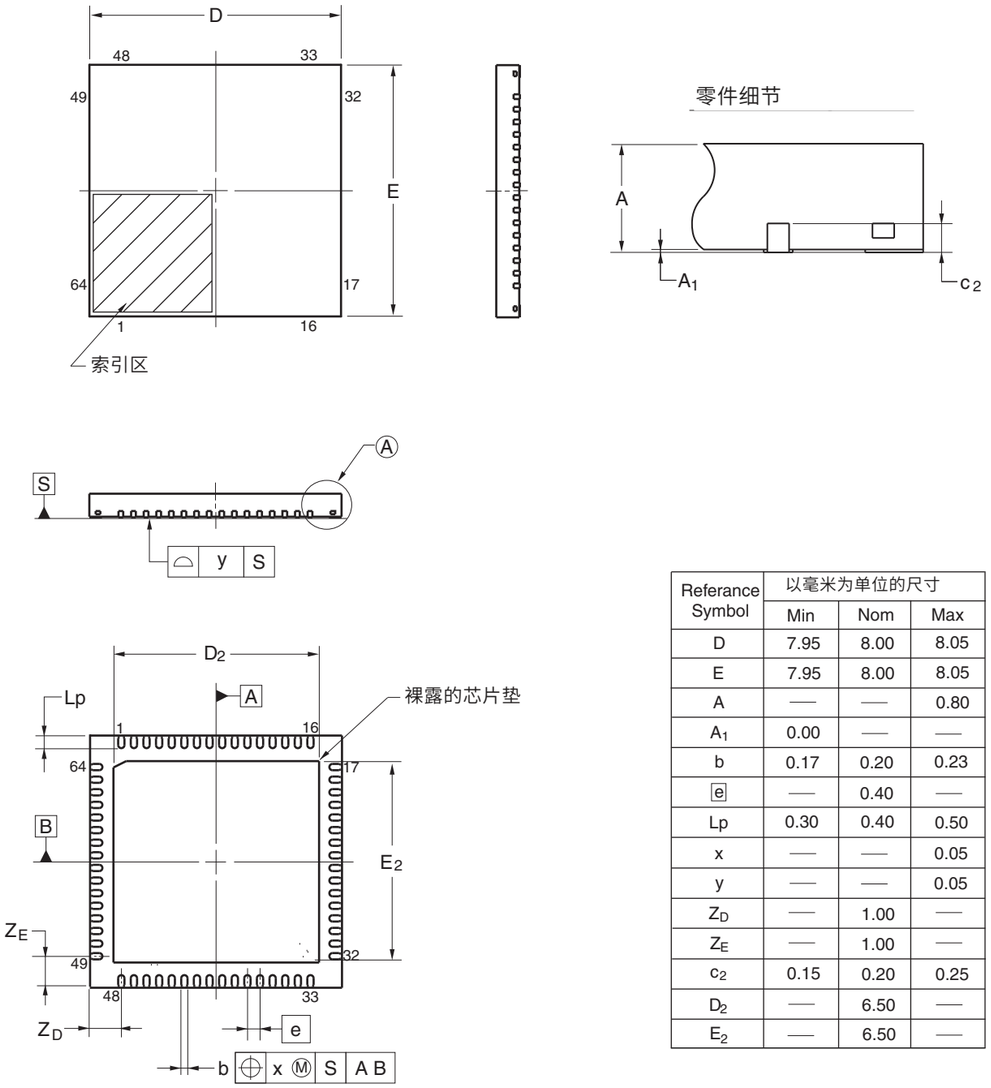
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN64-8x8-0.40	PWQN0064LA-A	P64K8-40-9B5-3	0.16



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	7.95	8.00	8.05
E	7.95	8.00	8.05
A	—	—	0.80
A_1	0.00	—	—
b	0.17	0.20	0.23
e	—	0.40	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	1.00	—
Z_E	—	1.00	—
c_2	0.15	0.20	0.25
D_2	—	6.50	—
E_2	—	6.50	—

Figure 2.3 QFN 64-pin

JEITA包装代码	RENESAS code	以前的代码	MASS(TYP.)[g]
P-HWQFN64-8x8-0.40	PWQN0064LA-A	P64K8-40-9B5-3	0.16

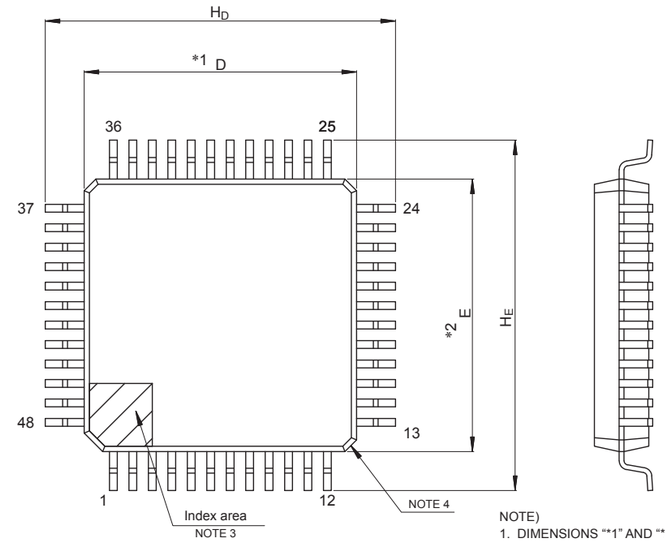


Referance Symbol	以毫米为单位的尺寸		
	Min	Nom	Max
D	7.95	8.00	8.05
E	7.95	8.00	8.05
A	—	—	0.80
A_1	0.00	—	—
b	0.17	0.20	0.23
e	—	0.40	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	1.00	—
Z_E	—	1.00	—
c_2	0.15	0.20	0.25
D_2	—	6.50	—
E_2	—	6.50	—

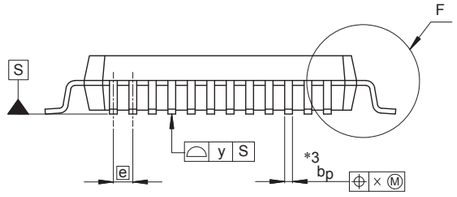
Figure 2.3 QFN 64-pin

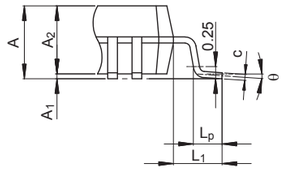
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.





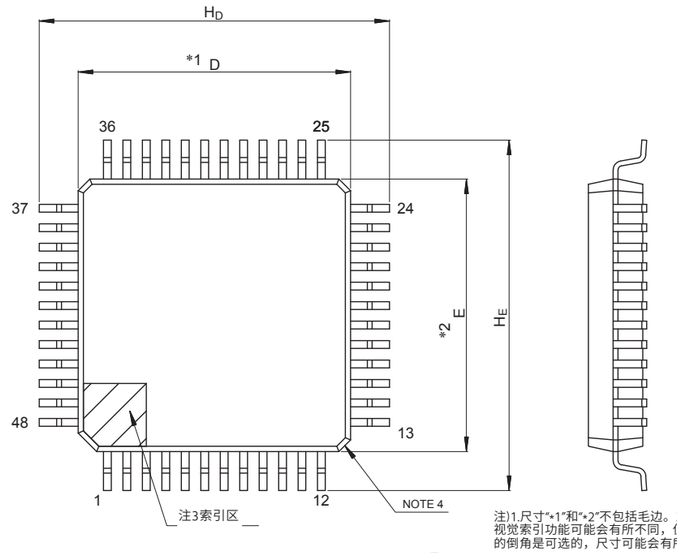
Detail F

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

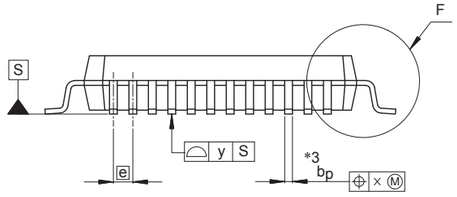
Figure 2.4 LQFP 48-pin

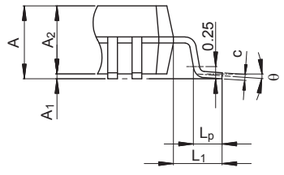
JEITA包装代码	RENESAS Code	以前的代码	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm



注)1.尺寸"*1"和"*2"不包括毛边。2.尺寸"*3"不包括微调偏移。3.PIN1视觉索引功能可能会有所不同，但必须位于阴影区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。



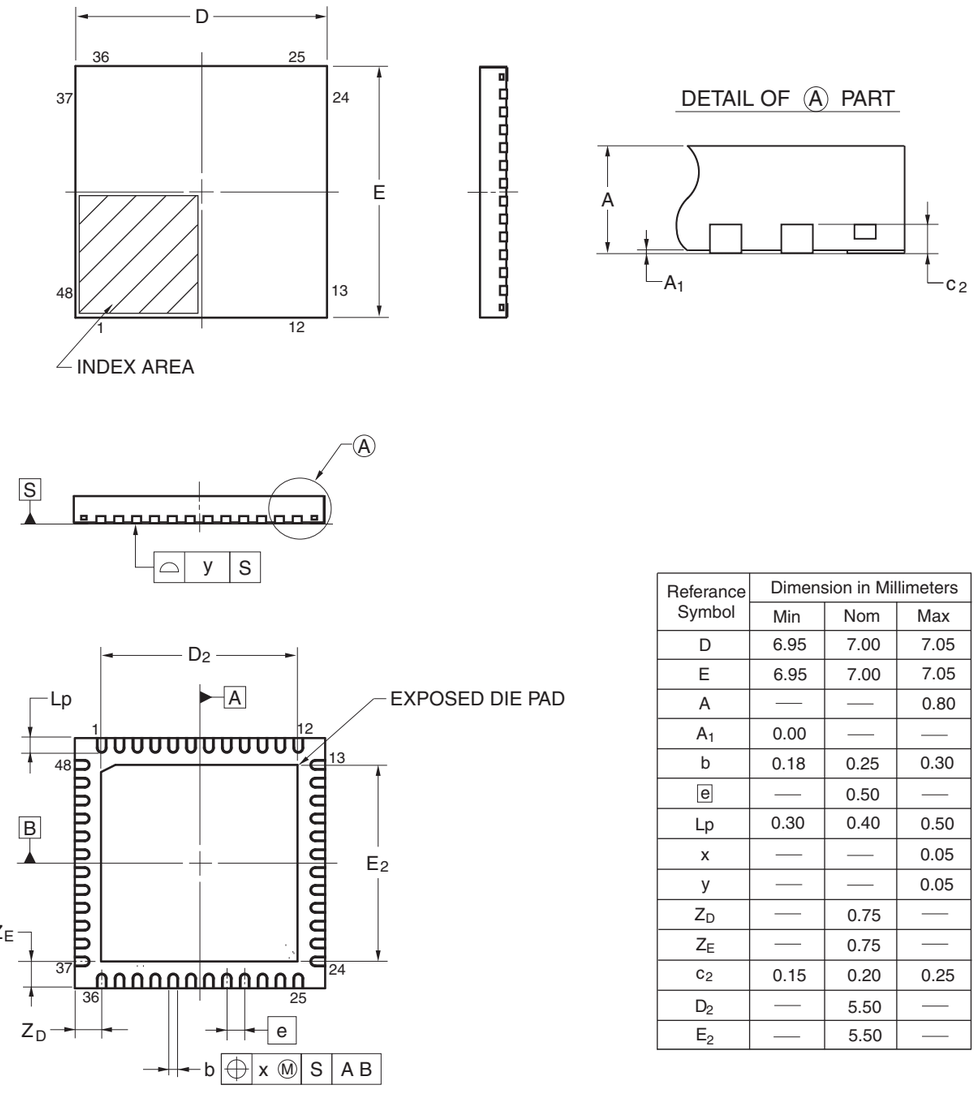


Detail F

参考符号	尺寸以毫米为单位		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 2.4 LQFP 48-pin

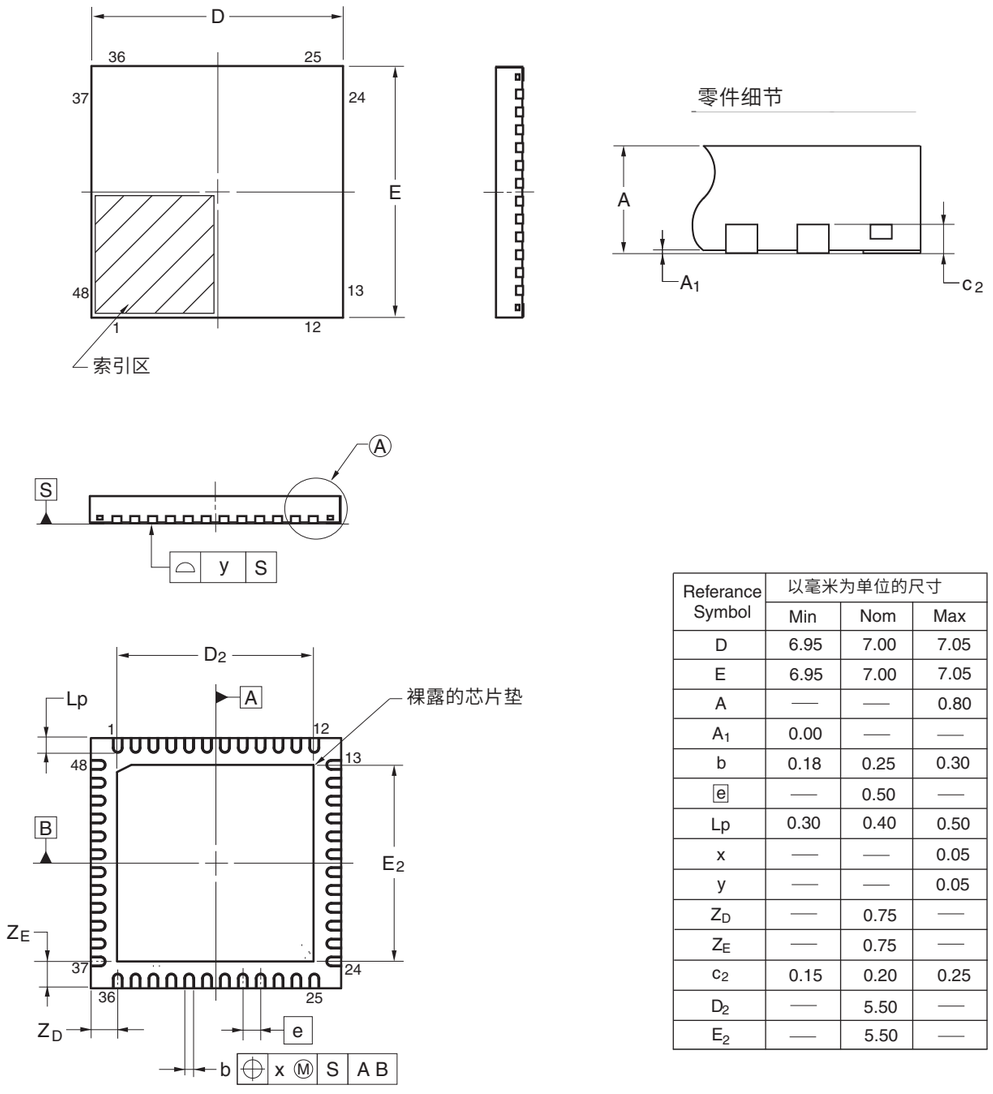
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	5.50	—
E_2	—	5.50	—

Figure 2.5 QFN 48-pin

JEITA包装代码	RENESAS code	以前的代码	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13



Referance Symbol	以毫米为单位的尺寸		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	5.50	—
E_2	—	5.50	—

Figure 2.5 QFN 48-pin

Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 3)

Name	Description	Base address
RMPU	Renesas Memory Protection Unit	0x4000_0000
TZF	TrustZone Filter	0x4000_0E00
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DMAC0	Direct memory access controller 0	0x4000_5000
DMAC1	Direct memory access controller 1	0x4000_5040
DMAC2	Direct memory access controller 2	0x4000_5080
DMAC3	Direct memory access controller 3	0x4000_50C0
DMAC4	Direct memory access controller 4	0x4000_5100
DMAC5	Direct memory access controller 5	0x4000_5140
DMAC6	Direct memory access controller 6	0x4000_5180
DMAC7	Direct memory access controller 7	0x4000_51C0
DMA	DMAC Module Activation	0x4000_5200
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
CACHE	CACHE	0x4000_7000
CPSCU	CPU System Security Control Unit	0x4000_8000
DBG	Debug Function	0x4001_B000
FCACHE	Flash Cache	0x4001_C100
SYSC	System Control	0x4001_E000
PORT0	Port 0 Control Registers	0x4001_F000
PORT2	Port 2 Control Registers	0x4001_F040
PORTA	Port A Control Registers	0x4001_F140
PORTB	Port B Control Registers	0x4001_F160
PORTC	Port C Control Registers	0x4001_F180
PORTD	Port D Control Registers	0x4001_F1A0
PORTE	Port E Control Registers	0x4001_F1C0
PFS_B	Pmn Pin Function Control Register	0x4001_F800
IIRFA	IIR Filter Accelerator	0x4002_0000
TFU	Trigonometric Function Unit	0x4002_1000
ELC_B	Event Link Controller	0x4008_2000
IWDT	Independent Watchdog Timer	0x4008_3200
WDT	Watchdog Timer	0x4008_3400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4008_3600
MSTP	Module Stop Control A, B, C, D, E	0x4008_4000

Appendix 3. I/O Registers

本附录按功能描述了IO寄存器地址和访问周期。

3.1 外设基地址

本节提供本手册中描述的外设的基地址。表3.1显示了每个外设的名称、描述和基地址。

Table 3.1 外设基地址(1of3)

Name	Description	基址
RMPU	瑞萨内存保护单元	0x4000_0000
TZF	TrustZone Filter	0x4000_0E00
SRAM	SRAM Control	0x4000_2000
BUS	总线控制	0x4000_3000
DMAC0	直接内存访问控制器0	0x4000_5000
DMAC1	直接内存访问控制器1	0x4000_5040
DMAC2	直接内存访问控制器2	0x4000_5080
DMAC3	直接内存访问控制器3	0x4000_50C0
DMAC4	直接内存访问控制器4	0x4000_5100
DMAC5	直接内存访问控制器5	0x4000_5140
DMAC6	直接内存访问控制器6	0x4000_5180
DMAC7	直接内存访问控制器7	0x4000_51C0
DMA	DMAC模块激活	0x4000_5200
DTC	数据传输控制器	0x4000_5400
ICU	中断控制器	0x4000_6000
CACHE	CACHE	0x4000_7000
CPSCU	CPU系统安全控制单元	0x4000_8000
DBG	调试功能	0x4001_B000
FCACHE	闪存缓存	0x4001_C100
SYSC	系统控制	0x4001_E000
PORT0	端口0控制寄存器	0x4001_F000
PORT2	端口2控制寄存器	0x4001_F040
PORTA	端口A控制寄存器	0x4001_F140
PORTB	端口B控制寄存器	0x4001_F160
PORTC	端口C控制寄存器	0x4001_F180
PORTD	端口D控制寄存器	0x4001_F1A0
PORTE	端口E控制寄存器	0x4001_F1C0
PFS_B	Pmn引脚功能控制寄存器	0x4001_F800
IIRFA	IIR滤波器加速器	0x4002_0000
TFU	三角函数单元	0x4002_1000
ELC_B	事件链接控制器	0x4008_2000
IWDT	独立看门狗定时器	0x4008_3200
WDT	看门狗定时器	0x4008_3400
CAC	时钟频率精度测量电路	0x4008_3600
MSTP	模块停止控制A、B、C、D、E	0x4008_4000

Table 3.1 Peripheral base address (2 of 3)

Name	Description	Base address
KINT	Key Interrupt Function	0x4008_5000
POEG	Port Output Enable for GPT	0x4008_A000
IIC0WU_B	Inter-Integrated Circuit 0 Wake-up Unit	0x4009_F098
CANFD_B	CANFD Module Control	0x400B_0000
PSCU	Peripheral Security Control Unit	0x400E_0000
AGTW_B0	Low Power Asynchronous General purpose Timer 0	0x400E_8000
AGTW_B1	Low Power Asynchronous General purpose Timer 1	0x400E_8100
TSN	Temperature Sensor	0x400F_3000
ACMPHS0	High-Speed Analog Comparator	0x400F_4000
ACMPHS1	High-Speed Analog Comparator	0x400F_4100
ACMPHS2	High-Speed Analog Comparator	0x400F_4200
ACMPHS3	High-Speed Analog Comparator	0x400F_4300
CRC	Cyclic Redundancy Check	0x4010_8000
DOC_B	Data Operation Circuit	0x4010_9000
SCI_B0	Serial Communication Interface 0	0x4011_8000
SCI_B1	Serial Communication Interface 1	0x4011_8100
SCI_B2	Serial Communication Interface 2	0x4011_8200
SCI_B3	Serial Communication Interface 3	0x4011_8300
SCI_B4	Serial Communication Interface 4	0x4011_8400
SCI_B9	Serial Communication Interface 9	0x4011_8900
SPI_B0	Serial Peripheral Interface 0	0x4011_A000
SPI_B1	Serial Peripheral Interface 1	0x4011_A100
IIC_B0	Inter-Integrated Circuit 0	0x4011_F000
IIC_B1	Inter-Integrated Circuit 1	0x4011_F400
ECCMB	CANFD ECC Module	0x4012_F200
SCE5_B	Secure Cryptographic Engine	0x4016_1000
GPT0	General PWM Timer 0	0x4016_9000
GPT1	General PWM Timer 1	0x4016_9100
GPT2	General PWM Timer 2	0x4016_9200
GPT3	General PWM Timer 3	0x4016_9300
GPT4	General PWM Timer 4	0x4016_9400
GPT5	General PWM Timer 5	0x4016_9500
GPT6	General PWM Timer 6	0x4016_9600
GPT7	General PWM Timer 7	0x4016_9700
GPT8	General PWM Timer 8	0x4016_9800
GPT9	General PWM Timer 9	0x4016_9900
GPT_OPS	Output Phase Switching Controller	0x4016_9A00
GPT_GTCLK	General PWM Timer	0x4016_9B00
PDG	PWM Delay Generation	0x4016_A000
ADC_B	12-Bit A/D Converter	0x4017_0000
DAC120	12-bit D/A converter	0x4017_2000
DAC121	12-bit D/A converter	0x4017_2100

Table 3.1 外设基地址（2个，共3个）

Name	Description	基址
KINT	按键中断功能	0x4008_5000
POEG	GPT的端口输出使能	0x4008_A000
IIC0WU_B	内部集成电路0唤醒单元	0x4009_F098
CANFD_B	CANFD模块控制	0x400B_0000
PSCU	外围安全控制单元	0x400E_0000
AGTW_B0	低功耗异步通用定时器0	0x400E_8000
AGTW_B1	低功耗异步通用定时器1	0x400E_8100
TSN	温度感应器	0x400F_3000
ACMPHS0	高速模拟比较器	0x400F_4000
ACMPHS1	高速模拟比较器	0x400F_4100
ACMPHS2	高速模拟比较器	0x400F_4200
ACMPHS3	高速模拟比较器	0x400F_4300
CRC	循环冗余校验	0x4010_8000
DOC_B	数据运算电路	0x4010_9000
SCI_B0	串行通讯接口0	0x4011_8000
SCI_B1	串行通讯接口1	0x4011_8100
SCI_B2	串行通讯接口2	0x4011_8200
SCI_B3	串行通讯接口3	0x4011_8300
SCI_B4	串行通讯接口4	0x4011_8400
SCI_B9	串行通讯接口9	0x4011_8900
SPI_B0	串行外设接口0	0x4011_A000
SPI_B1	串行外设接口1	0x4011_A100
IIC_B0	Inter-Integrated Circuit 0	0x4011_F000
IIC_B1	Inter-Integrated Circuit 1	0x4011_F400
ECCMB	CANFD ECC Module	0x4012_F200
SCE5_B	安全加密引擎	0x4016_1000
GPT0	通用PWM定时器0	0x4016_9000
GPT1	通用PWM定时器1	0x4016_9100
GPT2	通用PWM定时器2	0x4016_9200
GPT3	通用PWM定时器3	0x4016_9300
GPT4	通用PWM定时器4	0x4016_9400
GPT5	通用PWM定时器5	0x4016_9500
GPT6	通用PWM定时器6	0x4016_9600
GPT7	通用PWM定时器7	0x4016_9700
GPT8	通用PWM定时器8	0x4016_9800
GPT9	通用PWM定时器9	0x4016_9900
GPT_OPS	输出相位切换控制器	0x4016_9A00
GPT_GTCLK	通用PWM定时器	0x4016_9B00
PDG	PWM延迟生成	0x4016_A000
ADC_B	12-Bit A/D Converter	0x4017_0000
DAC120	12-bit D/A converter	0x4017_2000
DAC121	12-bit D/A converter	0x4017_2100

Table 3.1 Peripheral base address (3 of 3)

Name	Description	Base address
FLAD	Data Flash	0x407F_C000
FACI	Flash Application Command Interface	0x407F_E000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.
- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with bus access from other bus masters such as DTC or DMAC.

Table 3.2 Access cycles (1 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU	0x4000_0000	0x4000_6FFF	4	3	4	3	ICLK	Renesas Memory Protection Unit, TrustZone Filter, SRAM Control, BUS Control, Direct memory access controller n, DMAC Module Activation, DTC Control Register, Interrupt Controller
CACHE	0x4000_7000	0x4000_7FFF	4	5	4	5	ICLK	CACHE
CPSCU, DBG, FCACHE	0x4000_8000	0x4001_CFFF	4	3	4	3	ICLK	CPU System Security Control Unit, Debug Function, Flash Cache
SYSC	0x4001_E000	0x4001_E3FF	5	4	5	4	ICLK	System Control
SYSC	0x4001_E400	0x4001_E5FF	9	8	5 to 8	5 to 8	PCLKB	System Control
PORTn	0x4001_F000	0x4001_F7FF	5	3	5	3	ICLK	PORTn Control Register 1/3/4
PORTn (PCNTR2)	0x4001_F000	0x4001_F7FF	8	3	8	3	ICLK	PORTn Control Register 2
PFS	0x4001_F800	0x4001_FFFF	8	3	8	3	ICLK	Pmn Pin Function Control Register
IIRFA	0x4002_0000	0x4002_03FF	4	3	4	3	ICLK	IIR Filter Accelerator
IIRFA	0x4002_0400	0x4002_0FFF	6	3	6	3	ICLK	IIR Filter Accelerator

Table 3.1 外设基地址(3of3)

Name	Description	基址
FLAD	数据闪存	0x407F_C000
FACI	Flash应用命令接口	0x407F_E000

Note: 名称=外设名称
描述=外围功能
基地址=外设使用的最低保留地址或地址

3.2 访问周期

本节提供本手册中描述的IO寄存器的访问周期信息。

●寄存器按相关模块分组。

●访问周期数是指基于指定参考时钟的周期数。

●在内部IO区，不能访问未分配给寄存器的保留地址，否则无法保证操作。

●IO访问周期数取决于内部外设总线的总线周期、分频时钟同步周期和每个模块的等待周期。分频时钟同步周期取决于ICLK和PCLK之间的频率比。

●当ICLK的频率等于PCLK的频率时，分频的时钟同步周期数始终是恒定的。

●当ICLK频率大于PCLK频率时，分频时钟同步周期数至少增加1个PCLK周期。

●写访问周期数是指非缓冲写访问所获得的周期数。

Note: 这适用于当来自CPU的访问与来自其他总线主控器（例如DTC或DMAC）的总线访问不冲突时的周期数。

Table 3.2 访问周期(1of3)

Peripherals	Address		访问周期数				Cycle Unit	相关功能
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU	0x4000_0000	0x4000_6FFF	4	3	4	3	ICLK	瑞萨内存保护单元、TrustZone过滤器、SRAM控制，总线控制、直接内存访问控制器n、DMAC模块激活、DTC控制寄存器、中断控制器
CACHE	0x4000_7000	0x4000_7FFF	4	5	4	5	ICLK	CACHE
CPSCU, DBG, FCACHE	0x4000_8000	0x4001_CFFF	4	3	4	3	ICLK	CPU系统安全控制单元，调试功能，闪存
SYSC	0x4001_E000	0x4001_E3FF	5	4	5	4	ICLK	系统控制
SYSC	0x4001_E400	0x4001_E5FF	9	8	5 to 8	5 to 8	PCLKB	系统控制
PORTn	0x4001_F000	0x4001_F7FF	5	3	5	3	ICLK	PORTn控制寄存器134
PORTn (PCNTR2)	0x4001_F000	0x4001_F7FF	8	3	8	3	ICLK	PORTn Control Register 2
PFS	0x4001_F800	0x4001_FFFF	8	3	8	3	ICLK	Pmn引脚功能控制寄存器
IIRFA	0x4002_0000	0x4002_03FF	4	3	4	3	ICLK	IIR滤波器加速器
IIRFA	0x4002_0400	0x4002_0FFF	6	3	6	3	ICLK	IIR滤波器加速器

Table 3.2 Access cycles (2 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
TFU	0x4002_1000	0x4002_1FFF	4	3	4	3	ICLK	Trigonometric Function Unit
ELC	0x4008_2000	0x4008_2FFF	5	4	3 to 5	2 to 4	PCLKB	Event Link Controller
IWDT, WDT, CAC	0x4008_3000	0x4008_3FFF	5	4	3 to 5	2 to 4	PCLKB	Independent Watchdog Timer, Watchdog Timer, Clock Frequency Accuracy Measurement Circuit
MSTP	0x4008_4000	0x4008_4FFF	5	4	2 to 4	2 to 4	PCLKB	Module Stop Control
KINT	0x4008_5000	0x4008_5FFF	4	3	1 to 4	1 to 3	PCLKB	Key Interrupt Function
POEG	0x4008_A000	0x4008_AFFF	5	4	3 to 5	2 to 4	PCLKB	Port Output Enable for GPT
CANFD	0x400B_0000	0x400C_1FFF	5	4	2 to 5	2 to 4	PCLKB	CANFD Module
PSCU	0x400E_0000	0x400E_0FFF	5	4	2 to 5	2 to 4	PCLKB	Peripheral Security Control Unit
AGTn	0x400E_8000	0x400E_8FFF	7	4	4 to 7	2 to 4	PCLKB	Low Power Asynchronous General Purpose Timer n
TSN	0x400F_3000	0x400F_3FFF	5	4	2 to 5	2 to 4	PCLKB	Temperature Sensor
ACMPHSn	0x400F_4000	0x400F_4FFF	4	3	1 to 3	1 to 3	PCLKB	High-Speed Analog Comparator
CRC, DOC	0x4010_8000	0x4010_9FFF	5	4	2 to 5	2 to 4	PCLKA	Cyclic Redundancy Check, Data Operation Circuit
SCIn	0x4011_8000	0x4011_8FFF	5	4	2 to 4	2 to 4	PCLKA	Serial Communication Interface n
SPIn	0x4011_A000	0x4011_AFFF	5	4	2 to 5	2 to 4	PCLKA	Serial Peripheral Interface n
IICn	0x4011_F000	0x4011_FFFF	5	4	2 to 4	2 to 4	PCLKA	Inter-Integrated Circuit n
CANFD ECC	0x4012_F200	0x4012_FFFF	5	4	2 to 5	2 to 4	PCLKA	CANFD ECC Module
SCE5	0x4016_1000	0x4016_1FFF	6	4	3 to 6	2 to 4	PCLKA	Secure Cryptographic Engine
GPTn, GPT_OPS (core clock = PCLKD)	0x4016_9000	0x4016_9FFF	8	5	5 to 8	3 to 5	PCLKA	General PWM Timer n, Output Phase Switching Controller
GPTn, GPT_OPS (core clock = GPTCLK)	0x4016_9000	0x4016_9FFF	10	7	7 to 10	5 to 7	PCLKA	General PWM Timer n, Output Phase Switching Controller
GPT (GTCKCR)	0x4016_9B00	0x4016_9B00	5	4	2 to 4	2 to 4	PCLKA	GPT Clock Control Register
PDG	0x4016_A000	0x4016_AFFF	4	3	1 to 3	1 to 3	PCLKA	PWM Delay Generation
ADC	0x4017_0000	0x4017_0FFF	5	4	2 to 5	2 to 4	PCLKA	12-bit A/D Converter
ADC	0x4017_1000	0x4017_1FFF	4	3	1 to 3	1 to 3	PCLKA	12-bit A/D Converter
DAC12n	0x4017_2000	0x4017_2FFF	5	4	2 to 4	2 to 4	PCLKA	12-bit D/A Converter

Table 3.2 访问周期（2个，共3个）

Peripherals	Address		访问周期数				Cycle Unit	相关功能
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
TFU	0x4002_1000	0x4002_1FFF	4	3	4	3	ICLK	三角函数单元
ELC	0x4008_2000	0x4008_2FFF	5	4	3 to 5	2 to 4	PCLKB	事件链接控制器
IWDT, WDT, CAC	0x4008_3000	0x4008_3FFF	5	4	3 to 5	2 to 4	PCLKB	Independent 看门狗定时器，看门狗定时器，时钟频率 Accuracy 测量电路
MSTP	0x4008_4000	0x4008_4FFF	5	4	2 to 4	2 to 4	PCLKB	模块停止控制
KINT	0x4008_5000	0x4008_5FFF	4	3	1 to 4	1 to 3	PCLKB	按键中断功能
POEG	0x4008_A000	0x4008_AFFF	5	4	3 to 5	2 to 4	PCLKB	端口输出使能 GPT
CANFD	0x400B_0000	0x400C_1FFF	5	4	2 to 5	2 to 4	PCLKB	CANFD Module
PSCU	0x400E_0000	0x400E_0FFF	5	4	2 to 5	2 to 4	PCLKB	外围安全 控制单元
AGTn	0x400E_8000	0x400E_8FFF	7	4	4 to 7	2 to 4	PCLKB	低电量 Asynchronous 一般用途 Timer n
TSN	0x400F_3000	0x400F_3FFF	5	4	2 to 5	2 to 4	PCLKB	温度感应器
ACMPHSn	0x400F_4000	0x400F_4FFF	4	3	1 to 3	1 to 3	PCLKB	High-Speed Analog Comparator
CRC, DOC	0x4010_8000	0x4010_9FFF	5	4	2 to 5	2 to 4	PCLKA	循环冗余 检查，数据 运算电路
SCIn	0x4011_8000	0x4011_8FFF	5	4	2 to 4	2 to 4	PCLKA	串行通信 Interface n
SPIn	0x4011_A000	0x4011_AFFF	5	4	2 to 5	2 to 4	PCLKA	串行外设 Interface n
IICn	0x4011_F000	0x4011_FFFF	5	4	2 to 4	2 to 4	PCLKA	Inter-Integrated Circuit n
CANFD ECC	0x4012_F200	0x4012_FFFF	5	4	2 to 5	2 to 4	PCLKA	CANFD ECC Module
SCE5	0x4016_1000	0x4016_1FFF	6	4	3 to 6	2 to 4	PCLKA	安全密码学 Engine
GPTn, GPT_OPS (core clock = PCLKD)	0x4016_9000	0x4016_9FFF	8	5	5 to 8	3 to 5	PCLKA	通用PWM定时器n，输出相位切换控制器
GPTn, GPT_OPS (core clock = GPTCLK)	0x4016_9000	0x4016_9FFF	10	7	7 to 10	5 to 7	PCLKA	通用PWM定时器n，输出相位切换控制器
GPT (GTCKCR)	0x4016_9B00	0x4016_9B00	5	4	2 to 4	2 to 4	PCLKA	GPT时钟控制 Register
PDG	0x4016_A000	0x4016_AFFF	4	3	1 to 3	1 to 3	PCLKA	PWM延迟 生成
ADC	0x4017_0000	0x4017_0FFF	5	4	2 to 5	2 to 4	PCLKA	12-bit A/D Converter
ADC	0x4017_1000	0x4017_1FFF	4	3	1 to 3	1 to 3	PCLKA	12-bit A/D Converter
DAC12n	0x4017_2000	0x4017_2FFF	5	4	2 to 4	2 to 4	PCLKA	12-bit D/A Converter

Table 3.2 Access cycles (3 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = FCLK		ICLK > FCLK*1			
	From	To	Read	Write	Read	Write		
FLAD, FACI	0x407F_C000	0x407F_EFFF	5	4	2 to 5	2 to 4	FCLK	Data Flash, Flash Application Command Interface

Note 1. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.

Table 3.2 访问周期（3个，共3个）

Peripherals	Address		访问周期数				Cycle Unit	相关功能
			ICLK = FCLK		ICLK > FCLK*1			
	From	To	Read	Write	Read	Write		
FLAD, FACI	0x407F_C000	0x407F_EFFF	5	4	2 to 5	2 to 4	FCLK	数据闪存、闪存应用命令 Interface

注1.如果PCLK或FCLK周期数为非整数（例如1.5），则最小值不带小数点，最大值四舍五入到小数点。例如，1.5到2。5是1到3。

Appendix 4. Peripheral Variant

Table 4.1 shows the correspondence between the module neme used in this manual and the Peripheral Variant.

Table 4.1 Module name vs Peripheral Variant

Module name	Peripheral Variant
ELC	ELC_B
AGTW	AGTW_B
SCI	SCI_B
IIC	IIC_B
CANFD	CANFD_B
SPI	SPI_B
SCE5	SCE5_B
ADC	ADC_B
DOC	DOC_B

Appendix 4. 外设变体

表4.1显示了本手册中使用的模块名称与PeripheralVariant之间的对应关系。

Table 4.1 模块名称与外设变体

模块名称	外设变体
ELC	ELC_B
AGTW	AGTW_B
SCI	SCI_B
IIC	IIC_B
CANFD	CANFD_B
SPI	SPI_B
SCE5	SCE5_B
ADC	ADC_B
DOC	DOC_B

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