Datasheet

RA0E3 Group

Renesas Microcontrollers

R01DS0500EJ0100
Rev.1.00
Oct 29, 2025

Ultra low power 32 MHz Arm® Cortex®-M23 core, 16-KB code flash memory, 2-KB SRAM, 10-bit A/D Converter, Serial interfaces and Safety features.

Features

■ Arm Cortex-M23 Core
- Armv8-M architecture
- Maximum operating frequency: 32 MHz
- Debug and Trace: DWT, FPB, CoreSight™ MTB-M23
- CoreSight Debug Port: SW-DP

■ Memory
- 16-KB code flash memory
- 2-KB SRAM
- Flash read protection (FRP)
- 128-bit unique ID

■ Connectivity
- Serial Array Unit (SAU)
  - Simplified SPI × 2
  - Simplified IIC × 2
  - UART × 1
  - UART (LIN-bus supported) × 1
- I^{2}C Bus interface (IICA) × 1

■ Analog
- 10-bit A/D Converter (ADC10)
- Temperature Sensor (TSN)

■ Timers
- 16-bit Timer Array Unit (TAU) × 8
- 32-bit interval timer (TML32) × 1
  - 1 channel in 32-bit counter mode
  - 2 channels in 16-bit counter mode
  - 4 channels in 8-bit counter mode

■ Safety
- Flash area protection
- ADC self-diagnosis function
- Cyclic Redundancy Check (CRC)
- Independent Watchdog Timer (IWDT)
- GPIO read-back level detection
- Register write protection
- Illegal memory access detection

■ System and Power Management
- Low power modes
- Data Transfer Controller (DTC)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Multiple Clock Sources
- High-speed on-chip oscillator (HOCO) (32 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Clock trim function for HOCO/LOCO
- Clock out support

■ Up to 17 pins for general I/O ports
- 5-V tolerance, open drain, input pull-up

■ Operating Voltage
- VCC: 1.6 to 5.5 V

■ Operating Temperature and Packages
- Ta = -40°C to +125°C
  - 20-pin TSSOP (4.4 mm × 6.5 mm, 0.65 mm pitch)

数据表

RA0E3组

瑞萨微控制器

R01DS0500EJ0100
Rev.1.00
2025年10月29日

超低功耗 32 MHzArm®Cortex®-M23 内核，16 KB 代码闪存，2 KB SRAM，10 位 A/D 转换器，串行接口和安全功能。

特征

■Arm Cortex-M23核心
- Armv8-M架构
- 最大工作频率：32 MHz
- 调试和跟踪：DWT、FPB、CoreSight™ MTB-M23
- CoreSight调试端口：SW-DP

■记忆
- 16KB 代码闪存
- 2-KB SRAM
- 闪存读取保护（FRP）
- 128 位唯一标识符

■连接性
- 串行阵列单元（SAU）
  - 简化版SPI × 2
  - 简化的 IIC× 2
  - UART × 1
  - UART（支持 LIN 总线）× 1
- I^{2}C 总线接口(IICA) × 1

■模拟
- 10位模数转换器（ADC10）
- 温度传感器（TSN）

■定时器
- 16 位定时器阵列单元(TAU) × 8
- 32位间隔定时器(TML32) × 1
  - 1 个通道，32 位计数器模式
  - 2 个通道，16 位计数器模式
  - 4 个通道，8 位计数器模式

■安全
- 闪光区域保护
- ADC自诊断功能
- 循环冗余校验（CRC）
- 独立看门狗定时器（IWDT）
- GPIO 读取回读电平检测
- 寄存器写保护
- 非法内存访问检测

■系统和电源管理
- 低功耗模式
- 数据传输控制器（DTC）
- 上电重置
- 低电压检测 (LVD) 及电压设置

■多个时钟源
- 高速片上振荡器（HOCO）（32 MHz）
- 低速片上振荡器（LOCO）（32.768 kHz）
- HOCO/LOCO 的时钟微调功能
- 下班支持

■最多可使用17个引脚的通用I/O端口
- 5V容差，开漏，输入上拉

■工作电压
- VCC：1.6 至5.5 V

■工作温度和封装
- Ta = -40°C 至+125°C
  - 20引脚 TSSOP(4.4 mm × 6.5 mm,0.65 mm 间距)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability.

The MCU in this series incorporates an energy-efficient Arm Cortex®-M23 32-bit core, that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- 16-KB code flash memory
- 2-KB SRAM
- Serial Interface (SAU, IICA)
- General Purpose Timer (TAU, TML32)
- 10-bit A/D Converter (ADC10)

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M23 core	● Maximum operating frequency: up to 32 MHz ● Arm Cortex-M23 core: – Revision: r1p0-00rel0 – Armv8-M architecture profile – Single-cycle integer multiplier – 19-cycle integer divider ● SysTick timer: – Driven by SYSTICCLK (LOCO) or ICLK

Table 1.2 Memory

Feature	Functional description
Code flash memory	16-KB of code flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip SRAM

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Operating mode: ● Single-chip mode
Resets	The MCU provides 6 resets (RES pin reset, power-on reset, independent watchdog timer reset, voltage monitor 0/1 resets, software reset).
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of two separate voltage level detectors (LVD0, LVD1). LVD0 and LVD1 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.
Clocks	● High-speed on-chip oscillator (HOCO) ● Low-speed on-chip oscillator (LOCO) ● Clock output / Buzzer output support
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).

1. 概述

MCU 集成了多个系列的软件和引脚兼容的Arm®32 位内核，这些内核共享一组通用的瑞萨外设，以方便设计的可扩展性。

该系列MCU采用节能型Arm Cortex®-M23 32位内核，特别适用于对成本敏感和低功耗的应用，具有以下特点：

- 16KB 代码闪存
- 2-KB SRAM
- 串行接口（SAU、IICA）
- 通用定时器（TAU、TML32）
- 10位模数转换器（ADC10）

1.1 功能概述

表 1.1 臂核心

特征	功能描述
Arm Cortex-M23 核心	●最高工作频率：高达 32 MHz ●Arm Cortex-M23 核心： −修订版：r1p0-00rel0 −Armv8-M架构配置文件 单周期整数乘法器 -19周期整数除法器 ●系统滴答定时器： −由 SYSTICCLK (LOCO) 或 ICLK 驱动

表 1.2 内存

特征	功能描述
代码闪存	16KB 代码闪存。
选项设置内存	选项设置存储器决定MCU复位后的状态。
SRAM	片上SRAM

表 1.3 系统（1/2）

特征	功能描述
操作模式	操作模式： ●单芯片模式
重置	MCU 提供 6 种复位方式（RES 引脚复位、上电复位、独立看门狗定时器复位、电压监视器0/1复位、软件复位）。
低电压检测（LVD）	低电压检测 (LVD) 模块监控输入到 VCC 引脚的电压电平。检测电平可通过寄存器设置进行选择。LVD 模块包含两个独立的电压电平检测器 (LVD0 和 LVD1)。LVD0 和 LVD1 测量输入到 VCC 引脚的电压电平。LVD 寄存器允许您的应用程序配置在不同的电压阈值下检测 VCC 变化。
时钟	●高速片上振荡器（HOCO） ●低速片上振荡器（LOCO） ●时钟输出/蜂鸣器输出支持
中断控制器单元（ICU）	中断控制器单元 (ICU) 控制哪些事件信号链接到嵌套向量中断控制器 (NVIC) 和数据传输控制器 (DTC) 模块。ICU 还控制不可屏蔽中断。
低功耗模式	可以通过多种方式降低功耗，包括设置时钟分频器、停止模块、在正常运行中选择电源控制模式以及过渡到低功耗模式。
寄存器写保护	寄存器写保护功能可防止重要寄存器因软件错误而被写入。需要保护的寄存器通过保护寄存器（PRCR）进行设置。

Table 1.3 System (2 of 2)

Feature	Functional description
Flash Read Protection	The MCU incorporates the flash read protection with one secure regions that include the code flash. The secure region can be protected from non-secure program accesses. A non-secure program cannot access a protected region.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with the LOCO, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.4 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 1.5 Timers

Feature	Functional description
Timer Array Unit (TAU)	The timer array unit has eight 16-bit timers. Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more channels can be used to create a High functional timer.
32-bit Interval Timer (TML32)	The 32-bit interval timer is made up of four 8-bit interval timers (referred to as channels 0 to 3). Each is capable of operating independently and in that case they all have the same functions. Two 8-bit interval timer channels can be connected to operate as a 16-bit interval timer. Four 8-bit interval timer channels can be connected to operate as a 32-bit interval timer.

Table 1.6 Communication interfaces

Feature	Functional description
Serial Array Unit (SAU)	A Serial Array Unit (SAU) has one unit. Unit0 has four channels. Each channel can achieve simplified SPI, UART, or simplified IIC.
I^2C Bus Interface (IICA)	The I^2C Bus Interface (IICA) has 1 channel. The IICA module conforms I^2C (Inter-Integrated Circuit) Bus Interface functions.

Table 1.7 Analog

Feature	Functional description
10-bit A/D Converter (ADC10)	A 10-bit successive approximation A/D converter is provided. Up to 6 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC10 for conversion and can be further used by the end application.

Table 1.8 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. Two CRC-generation polynomials (CRC-CCITT, CRC-32) are available.

表 1.3 系统（2/2）

特征	功能描述
闪存读取保护	该MCU集成了闪存读取保护功能，并包含一个安全区域，该安全区域存储着代码闪存。安全区域可防止非安全程序访问。非安全程序无法访问受保护的区域。
独立看门狗定时器（IWDT）	独立看门狗定时器 (IWDT) 由一个 14 位递减计数器组成，必须定期进行维护以防止计数器下溢。IWDT 提供复位 MCU、生成不可屏蔽中断或下溢中断的功能。由于该定时器与 LOCO 协同工作，因此在系统失控时，它作为一种故障保护机制，能够有效地将 MCU 恢复到已知状态。IWDT 可以由复位、下溢、刷新错误或寄存器中计数值的刷新自动触发。

表 1.4 直接内存访问

特征	功能描述
数据传输控制器（DTC）	提供数据传输控制器（DTC）模块，用于在中断请求激活时传输数据。

表 1.5 计时器

特征	功能描述
定时器阵列单元（TAU）	定时器阵列单元包含八个 16 位定时器。每个 16 位定时器称为一个通道，可以作为独立的定时器使用。此外，两个或多个通道可以组合成一个高电平功能定时器。
32 位间隔定时器 (TML32)	32 位间隔定时器由四个 8 位间隔定时器（称为通道 0 到 3）组成。每个定时器都可以独立运行，此时它们的功能相同。两个 8 位间隔定时器通道可以连接起来，组成一个 16 位间隔定时器。四个 8 位间隔定时器通道可以连接起来，组成一个 32 位间隔定时器。

表 1.6 通信接口

特征	功能描述
串行阵列单元（SAU）	串行阵列单元（SAU）包含一个单元。单元0有四个通道。每个通道可以实现简化的SPI、UART或简化的IIC。
I2C总线接口（IICA）	I^2C总线接口 (IICA) 有 1 个通道。IICA 模块符合I^2C(集成电路间) 总线接口功能。

表 1.7 模拟

特征	功能描述
10 位模数转换器 (ADC10)	本产品配备一个10位逐次逼近型模数转换器。最多可选择6个模拟输入通道。温度传感器输出和内部参考电压均可用于转换。
温度传感器（TSN）	片上温度传感器 (TSN) 用于检测和监控芯片温度，以确保器件可靠运行。该传感器输出的电压与芯片温度成正比，且芯片温度与输出电压之间的关系基本呈线性。输出电压被送至 ADC10 进行转换，转换后的信号可供最终应用使用。

表 1.8 数据处理

特征	功能描述
循环冗余校验 (CRC) 计算器	循环冗余校验（CRC）生成CRC码以检测数据中的错误。目前有两种CRC生成多项式（CRC-CCITT和CRC-32）可用。

Table 1.9 I/O ports

Feature	Functional description
I/O ports	● I/O ports for the 20-pin TSSOP – I/O pins: 16 – Input pins: 1 – Pull-up resistors: 12 – N-ch open-drain outputs: 11

表 1.9 I/O 端口

特征	功能描述
I/O端口	●20引脚TSSOP封装的I/O端口 −I/O引脚：16个 输入引脚：1 上拉电阻：12 −N沟道开漏输出：11

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

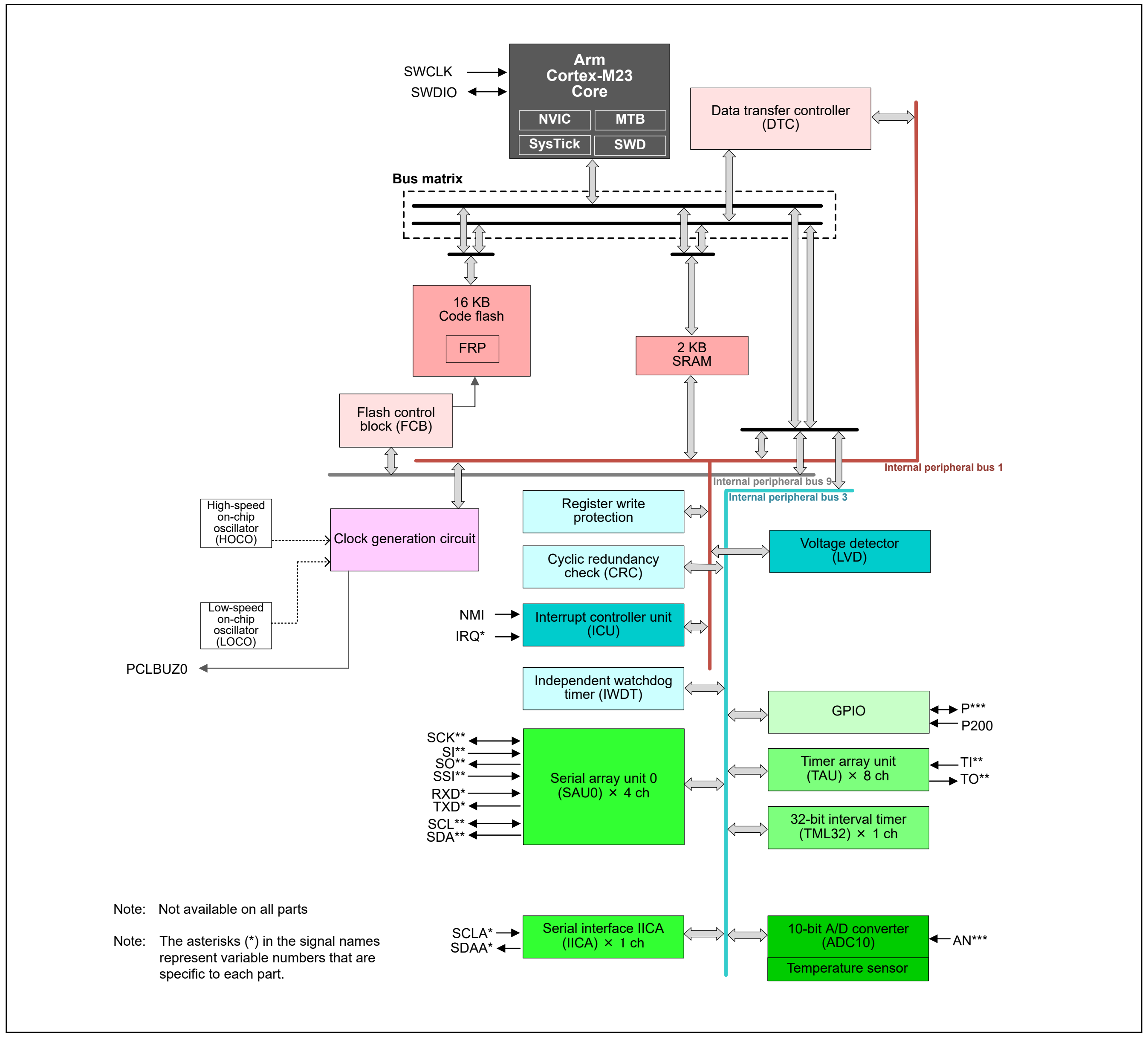


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.10 shows a list of products.

1.2框图

图 1.1 显示了 MCU 超集的框图。该组内的一些单个器件具有部分功能。

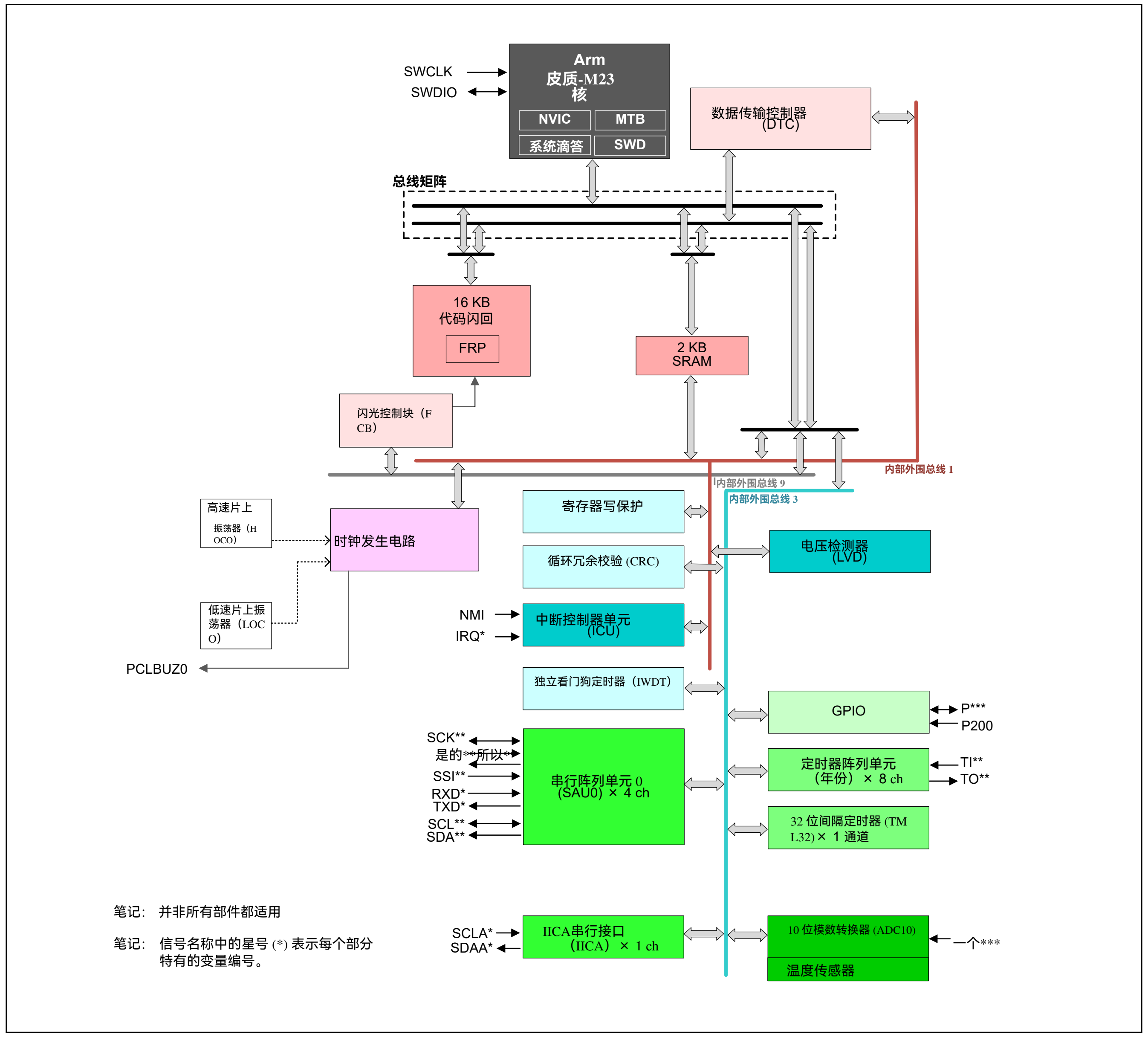
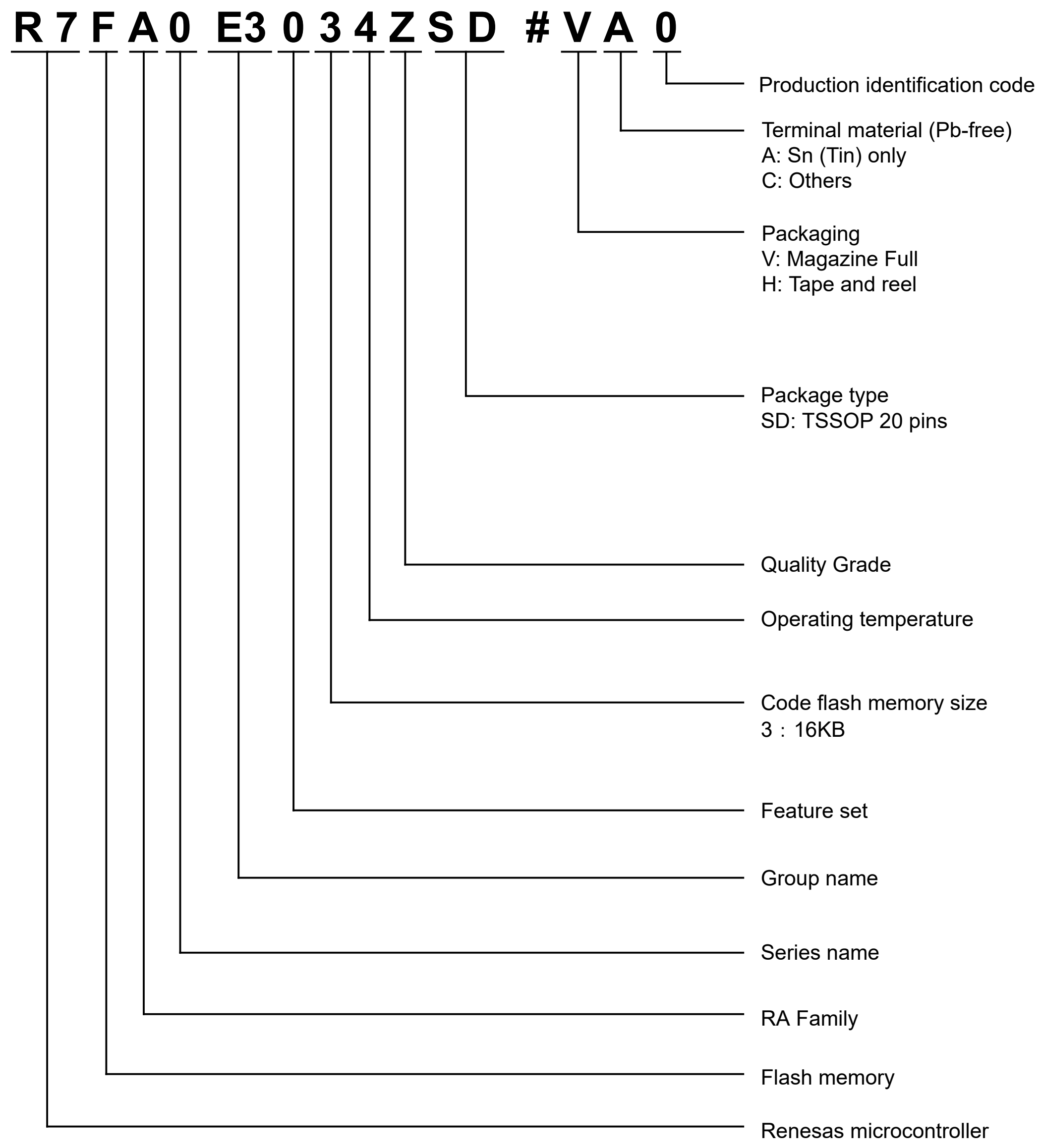


图 1.1 方框图

1.3零件编号

图 1.2 显示了产品部件号信息，包括内存容量和封装类型。表 1.10 列出了产品清单。

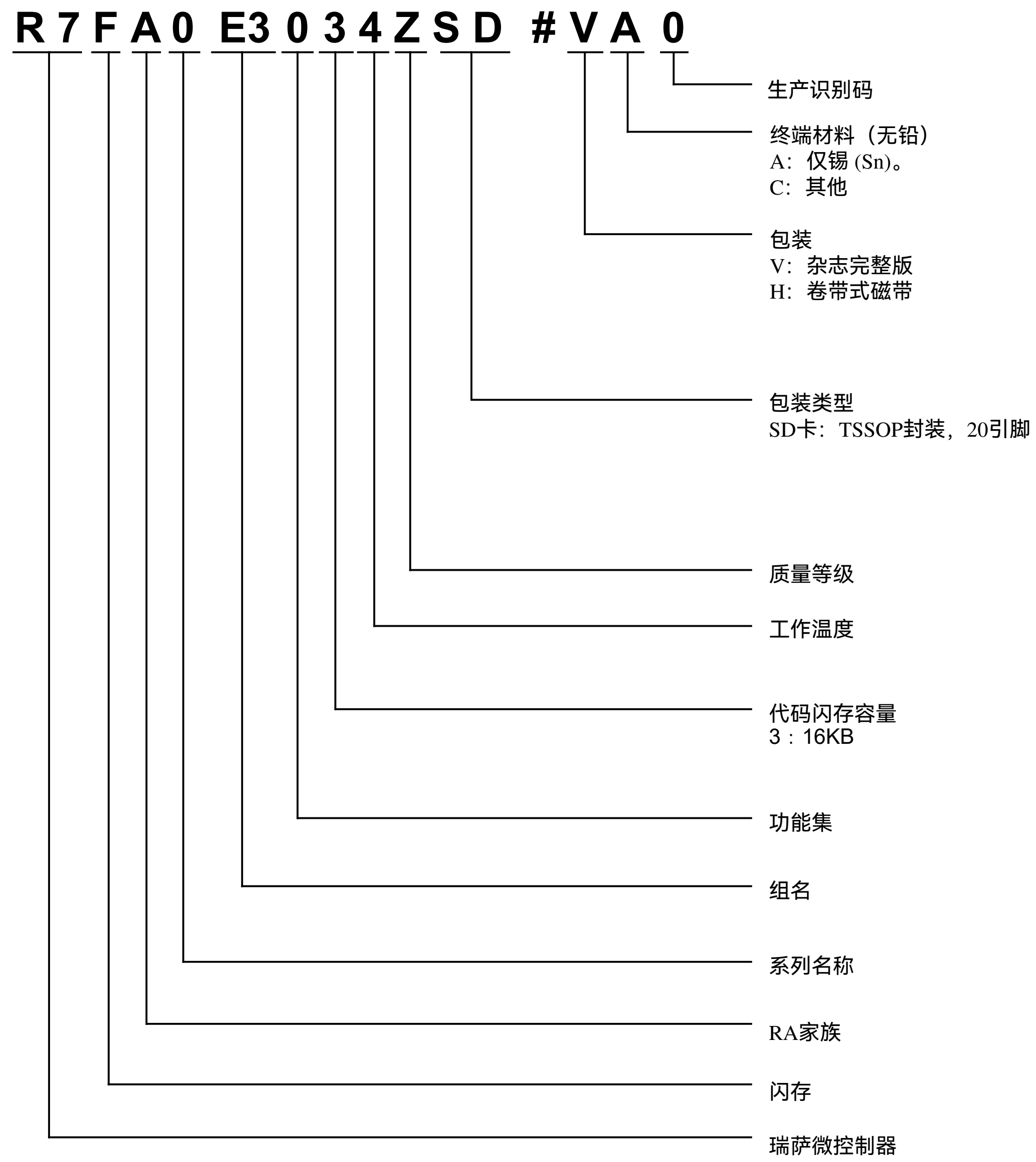


Note: Check the order screen for each product on the Renesas website for valid symbols after the #.

Figure 1.2 Part numbering scheme

Table 1.10 Product list

Product part number	Package code	Code flash	SRAM	Operating temperature
R7FA0E3034ZSD	PTSP0020JI-A	16 KB	2 KB	-40 to +125°C



注意：请在瑞萨电子网站上查看每个产品的订购页面，确认 # 后面是否有有效符号。

图 1.2 零件编号方案

表 1.10 产品清单

产品零件编号	包装代码	代码闪回	SRAM	工作温度
R7FA0E3034ZSD	PTSP0020JI-A	16 KB	2 KB	-40 to +125°C

1.4 Function Comparison

Table 1.11 Function comparison

Parts number		R7FA0E3034ZSD
Pin count		20
Package		TSSOP
Code flash memory		16 KB
SRAM		2 KB
System	CPU clock	32 MHz
	ICU	Yes
DMA	DTC	Yes
Timers	TAU	8 (PWM outputs: 7)
	TML32	1 (32-bit counter mode), 2 (16-bit counter mode), 4 (8-bit counter mode)
	IWDT	Yes
Communication	SAU	2 (simplified SPI)*1, 2 (simplified IIC)*1, 1 (UART)*1, 1 (UART supporting LIN-bus)*1
	IICA	1
Analog	ADC10	6
	TSN	Yes
Data processing	CRC	Yes
I/O ports	I/O pins	16
	Input pins	1
	Pull-up resistors	12
	N-ch open-drain outputs	11
	5-V tolerance	—

Note 1. SAU consists of several channels. Each channel can be assigned only one function at a time.

1.4 功能比较

表 1.11 功能比较

零件编号		R7FA0E3034ZSD
保龄球		20
包裹		TSSOP
代码闪存		16 KB
SRAM		2 KB
系统	CPU时钟	32 MHz
	ICU	Yes
DMA	DTC	Yes
定时器	TAU	8（PWM 输出：7）
	TML32	1（32 位计数器模式），2（ 16 位计数器模式），4（8 位计数器模式）
	IWDT	Yes
沟通	SAU	2 个（简化 SPI）*1、2 个（ 简化 IIC）*1、1 个（UART）* 1、1 个（支持 LIN 总线的 UA RT）*1
	IICA	1
模拟	ADC10	6
	TSN	Yes
数据处理	CRC	Yes
I/O端口	I/O引脚	16
	输入引脚	1
	上拉电阻	12
	N沟道开漏输出	11
	5V容差	—

注1：SAU由多个通道组成。每个通道一次只能分配一个功能。

1.5 Pin Functions

Table 1.12 Pin functions

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-µF capacitor. Place the capacitor close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	PCLBUZ0	Output	Clock output / Buzzer output
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
On-chip debug	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ5	Input	Maskable interrupt request pins
TAU	TI00 to TI07	Input	Pins for inputting an external counting clock/capture trigger to 16-bit timers 00 to 07
	TO00 to TO07	I/O	Timer output pins for 16-bit timers 00 to 07
IICA	SCLAn (n = 0)	I/O	Input/output pins for the clock
	SDAAn (n = 0)	I/O	Input/output pins for data
SAU	SCK00, SCK11	I/O	Serial clock I/O pins for serial interfaces SPI00, SPI11
	SI00, SI11	Input	Serial data input pins for serial interfaces SPI00, SPI11
	SO00, SO11	Output	Serial data output pins for serial interfaces SPI00, SPI11
	SSI00	Input	Chip select pin for serial interfaces SPI00
	SCL00, SCL11	Output	Serial clock output pins for serial interfaces IIC00, IIC11
	SDA00, SDA11	I/O	Serial data I/O pins for serial interfaces IIC00, IIC11
	RXD0, RXD1	Input	Serial data input pins for serial interfaces UART0, UART1
	TXD0, TXD1	Output	Serial data output pins for serial interfaces UART0, UART1
Analog power supply	VREFH0	Input	Analog reference voltage supply pin for the ADC10. Connect this pin to external reference voltage or VCC.
	VREFL0	Input	Analog reference ground pin for the ADC10. Connect this pin to external reference voltage or VSS.
ADC10	AN000, AN001, AN004, AN005, AN021 to AN022	Input	Input pins for the analog signals to be processed by the A/D converter.
I/O ports	P010 to P013	I/O	General-purpose input/output pins
	P100 to P102, P108 to P110, P112	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P206, P212, P213	I/O	General-purpose input/output pins
	P300	I/O	General-purpose input/output pins

1.5针脚功能

表 1.12 引脚功能

功能	信号	I/O	描述
电源	VCC	输入	电源引脚。将其连接到系统电源。使用一个0.1-µF 电容将此引脚连接到VSS。将电容靠近引脚放置。
	VCL	I/O	将此引脚通过用于稳定内部电源的滤波电容连接到 VSS 引脚。将电容靠近引脚放置。
	VSS	输入	接地引脚。将其连接到系统电源(0 V)。
钟	PCLBUZ0	输出	时钟输出/蜂鸣器输出
系统控制	RES	输入	复位信号输入引脚。当此信号为低电平时，MCU 进入复位状态。
片上调试	SWDIO	I/O	串行线调试数据输入/输出引脚
	SWCLK	输入	串行线时钟引脚
打断	NMI	输入	不可屏蔽中断请求引脚
	IRQ0 至 IRQ5	输入	可屏蔽中断请求引脚
TAU	TI00 至 TI07	输入	用于向 16 位定时器 00 至 07 输入外部计数时钟/捕获触发信号的引脚
	TO00 至 TO07	I/O	16 位定时器的定时器输出引脚 00 至 07
IICA	SCLAn (n = 0)	I/O	时钟的输入/输出引脚
	SDAAn (n = 0)	I/O	数据输入/输出引脚
SAU	SCK00, SCK11	I/O	串行接口 SPI00、SPI11 的串行时钟 I/O 引脚
	SI00, SI11	输入	串行接口 SPI00、SPI11 的串行数据输入引脚
	SO00, SO11	输出	串行接口 SPI00、SPI11 的串行数据输出引脚
	SSI00	输入	串行接口 SPI00 的片选引脚
	SCL00、SCL11	输出	串行接口 IIC00、IIC11 的串行时钟输出引脚
	SDA00, SDA11	I/O	串行接口 IIC00、IIC11 的串行数据 I/O 引脚
	RXD0，RXD1	输入	串行接口 UART0、UART1 的串行数据输入引脚
	TXD0，TXD1	输出	串行接口 UART0、UART1 的串行数据输出引脚
模拟电源	VREFH0	输入	ADC10 的模拟参考电压供电引脚。将此引脚连接到外部参考电压或 VCC。
	VREFL0	输入	ADC10 的模拟参考接地引脚。将此引脚连接到外部参考电压或 VSS。
ADC10	AN000、AN001、AN004、AN005、AN021 至 AN022	输入	用于输入模拟信号的引脚，这些信号将由 A/D 转换器处理。
I/O端口	P010 至 P013	I/O	通用输入/输出引脚
	P100 至 P102，P108 至 P110、P112	I/O	通用输入/输出引脚
	P200	输入	通用输入引脚
	P201, P206, P212, P213	I/O	通用输入/输出引脚
	P300	I/O	通用输入/输出引脚

1.6 Pin Assignments

Figure 1.3 shows the pin assignment from the top view.

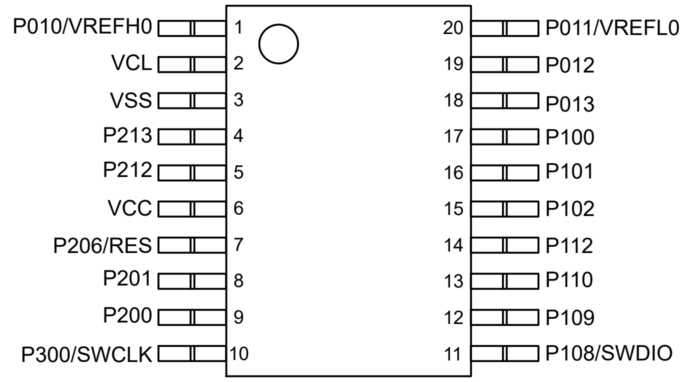


Figure 1.3 Pin assignment for TSSOP 20-pin (top view)

1.6引脚分配

图 1.3 显示了从俯视图看到的引脚分配情况。

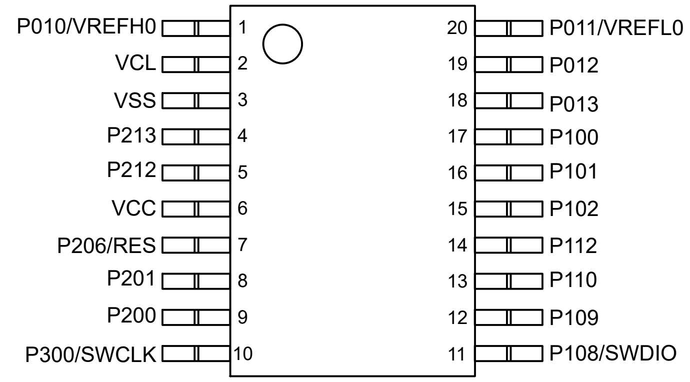


图 1.3 TSSOP 20 引脚封装的引脚分配（俯视图）

1.7 Pin Lists

Table 1.13 Pin list

Pin number				Timers	Communication interfaces		Analogs
TSSOP 20-pin	Power, System, Clock, Debug	I/O ports	Interrupt	TAU	SAU	IICA	ADC
1	VREFH0	P010	—	—	—	—	AN000
2	VCL	—	—	—	—	—	—
3	VSS	—	—	—	—	—	—
4	—	P213	IRQ0_B	TI00_A/TI02_B/TO02_B	TXD1_A/SO11_A	SDAA0_B	—
5	—	P212	IRQ1_B	TO00_A/TI03_C/TO03_C	RXD1_A/SDA11_A/SI11_A	SCLA0_B	—
6	VCC	—	—	—	—	—	—
7	RES	P206	IRQ1_C	—	—	—	—
8	PCLBUZ0_A	P201	IRQ5_B	TI05_B/TO05_B	SCL11_B/SSI00_B/SCK11_B	—	—
9	—	P200	IRQ0_A/NMI	TI06_B	RXD1_B/SSI00_D	—	—
10	SWCLK	P300	—	TI04_B/TO04_B	TXD1_B	SDAA0_E	—
11	SWDIO/PCLBUZ0_D	P108	—	TI03_B/TO03_B	SCK00_C	SCLA0_E	—
12	—	P109	IRQ4_B	TI02_A/TO02_A	TXD0_B/SO00_B	SDAA0_C	—
13	—	P110	IRQ3_B	TI01_A/TO01_A	RXD0_B/SDA00_B/SI00_B	SCLA0_C	—
14	—	P112	IRQ2_B	TI03_A/TO03_A	SCL00_B/SCK00_B/SSI00_C	—	—
15	PCLBUZ0_B	P102	IRQ4_A	TI06_A/TO06_A/TO00_C	SCL00_A/SCK00_A	—	—
16	—	P101	IRQ3_A	TI07_A/TO07_A/TI00_C	TXD0_A/SO00_A	SDAA0_D	AN021
17	—	P100	IRQ2_A	TI04_A/TO04_A/TI01_B/TO01_B	RXD0_A/SDA00_A/SI00_A	SCLA0_D	AN022
18	—	P013	—	—	—	—	AN005
19	—	P012	—	—	—	—	AN004
20	VREFL0	P011	—	—	—	—	AN001

Note: Some signal names have _A, _B, _C, _D, or _E suffixes, but these suffixes can be ignored when assigning functionality, except for SAU and IICA. For SAU and IICA, only signals, except for SCL11, SCK11, SCK00, and SSI00, bearing the same suffix can be selected. Assigning the same function to two or more pins simultaneously is prohibited.

1.7引脚列表

表 1.13 引脚列表

Pin number				定时器	通信接口		类似物
TSSOP 20-pin	力量，系统，钟，调试	I/O ports	打断	TAU	SAU	IICA	ADC
1	VREFH0	P010	—	—	—	—	AN000
2	VCL	—	—	—	—	—	—
3	VSS	—	—	—	—	—	—
4	—	P213	IRQ0_B	TI00_A/TI02_B/TO02_B	TXD1_A/SO11_A	SDAA0_B	—
5	—	P212	IRQ1_B	TO00_A/TI03_C/TO03_C	RXD1_A/SDA11_A/SI11_A	SCLA0_B	—
6	VCC	—	—	—	—	—	—
7	RES	P206	IRQ1_C	—	—	—	—
8	PCLBUZ0_A	P201	IRQ5_B	TI05_B/TO05_B	SCL11_B/SSI00_B/SCK11_B	—	—
9	—	P200	IRQ0_A/NMI	TI06_B	RXD1_B/SSI00_D	—	—
10	SWCLK	P300	—	TI04_B/TO04_B	TXD1_B	SDAA0_E	—
11	SWDIO/PCLBUZ0_D	P108	—	TI03_B/TO03_B	SCK00_C	SCLA0_E	—
12	—	P109	IRQ4_B	TI02_A/TO02_A	TXD0_B/SO00_B	SDAA0_C	—
13	—	P110	IRQ3_B	TI01_A/TO01_A	RXD0_B/SDA00_B/SI00_B	SCLA0_C	—
14	—	P112	IRQ2_B	TI03_A/TO03_A	SCL00_B/SCK00_B/SSI00_C	—	—
15	PCLBUZ0_B	P102	IRQ4_A	TI06_A/TO06_A/TO00_C	SCL00_A/SCK00_A	—	—
16	—	P101	IRQ3_A	TI07_A/TO07_A/TI00_C	TXD0_A/SO00_A	SDAA0_D	AN021
17	—	P100	IRQ2_A	TI04_A/TO04_A/TI01_B/TO01_B	RXD0_A/SDA00_A/SI00_A	SCLA0_D	AN022
18	—	P013	—	—	—	—	AN005
19	—	P012	—	—	—	—	AN004
20	VREFL0	P011	—	—	—	—	AN001

注意：部分信号名称带有 _A、_B、_C、_D 或 _E 后缀，但在分配功能时可以忽略这些后缀，SAU 和 IICA 除外。对于 SAU 和 IICA，只能选择具有相同后缀的信号（SCL11、SCK11、SCK00 和 SSI00 除外）。禁止同时为两个或多个引脚分配相同的功能。

2. Electrical Characteristics

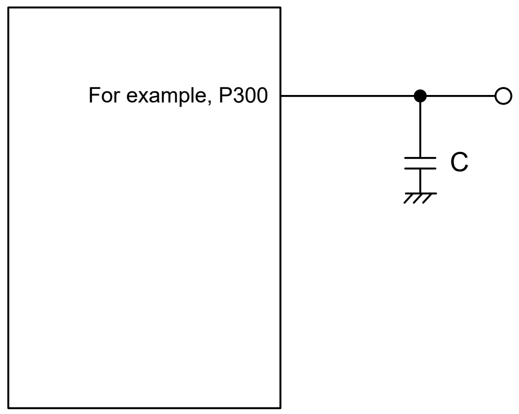
Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC*1 = VREFH0 = 1.6 to 5.5 V

VSS = VREFL0 = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3 V.

Figure 2.1 shows the timing conditions.



V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
Load capacitance C = 30 pF

Figure 2.1 Input or output timing measurement conditions

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings (1 of 2)

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +6.5	V
VCL pin input voltage		V_{IVCL}	-0.3 to +2.1 and -0.3 to VCC + 0.3*1	V
Input voltage	P100 to P102, P108 to P110, P112, P200, P201, P206, P300	V_{I1}	-0.3 to VCC + 0.3*2	V
	P010 to P013, P212, P213	V_{I2}	-0.3 to VCC + 0.3*2	V
Output voltage	P100 to P102, P108 to P110, P112, P201, P206, P300	V_{O1}	-0.3 to VCC + 0.3*2	V
	P010 to P013, P212, P213	V_{O2}	-0.3 to VCC + 0.3*2	V
Analog input voltage	AN000 to AN001, AN004 to AN005	V_{AI1}	-0.3 to VCC + 0.3 and -0.3 to VREFH0 + 0.3*2 *3	V
	AN021 to AN022	V_{AI2}	-0.3 to VCC + 0.3 and -0.3 to VREFH0 + 0.3*2 *3	V

2.电气特性

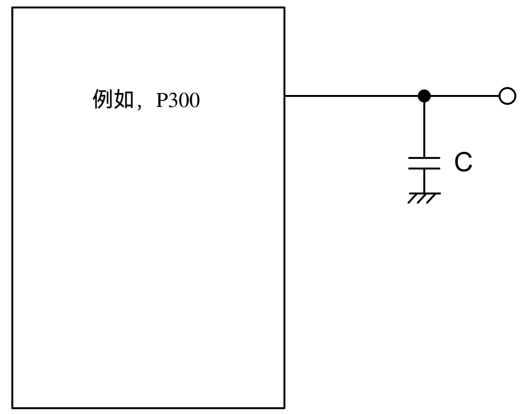
除非另有规定，MCU的电气特性在以下条件下定义：

VCC*1 = VREFH0 = 1.6 to 5.5 V

VSS = VREFL0 = 0 V, Ta = T_{opr}

注1. 典型条件设置为VCC = 3.3 V.

图 2.1 显示了时序条件。



V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
负载电容C = 30 pF

图 2.1 输入或输出时序测量条件

2.1 绝对最大额定值

表 2.1 绝对最大评级（1/2）

范围		象征	价值	单元
电源电压		VCC	-0.5 to +6.5	V
VCL引脚输入电压		V_{IVCL}	-0.3 至+2.1和 -0.3 至VCC + 0.3*1	V
输入电压	P100 至 P102、P108 至 P110、P112、P200、P201、P206, P300	V_{I1}	-0.3 to VCC + 0.3*2	V
	P010 至 P013、P212、P213	V_{I2}	-0.3 to VCC + 0.3*2	V
输出电压	P100 至 P102、P108 至 P110、P112、P201、P206 P300	V_{O1}	-0.3 to VCC + 0.3*2	V
	P010 至 P013、P212、P213	V_{O2}	-0.3 to VCC + 0.3*2	V
模拟输入电压	AN000 至 AN001，AN004 至 AN005	V_{AI1}	-0.3 至VCC + 0.3和 -0.3 至 VR EFH0 + 0.3*2 *3	V
	AN021 to AN022	V_{AI2}	-0.3 至VCC + 0.3和 -0.3 至 VR EFH0 + 0.3*2 *3	V

Table 2.1 Absolute maximum ratings (2 of 2)

Parameter			Symbol	Value	Unit
High-level output current	P100 to P102, P108 to P110, P112, P201, P206, P300	Per pin	I_{OH1}	-40	mA
		Total of all pins		-100	mA
	P010 to P013, P212, P213	Per pin	I_{OH2}	-5	mA
		Total of all pins		-20	mA
Low-level output current	P100 to P102, P108 to P110, P112, P201, P206, P300	Per pin	I_{OL1}	40	mA
		Total of all pins		100	mA
	P010 to P013, P212, P213	Per pin	I_{OL2}	10	mA
		Total of all pins		20	mA
Ambient operating temperature	In normal operation mode		Ta	-40 to +125	°C
	In flash memory programming mode			-40 to +125	°C
Storage temperature			Tstg	-65 to +150	°C

Note 1. Connect the VCL pin to VSS via a capacitor (0.47 to 1 μF). The listed value is the absolute maximum rating of the VCL pins. Only use the capacitor connection. Do not apply a specific voltage to this pin.
Note 2. This voltage must be no higher than 6.5 V.
Note 3. The voltage on a pin in use for A/D conversion must not exceed VREFH0 + 0.3.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Note: VREFH0 refers to the positive reference voltage of the A/D converter.

Note: The reference voltage is VSS.

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Table 2.2 Recommended operating conditions

Parameter	Symbol		Min.	Typ.	Max.	Unit
Power supply voltages	VCC		1.6	—	5.5	V
	VSS		—	0	—	V
Analog power supply voltages	VREFH0	When used as ADC10 Reference	1.6	—	VCC	V
	VREFL0		—	0	—	V

2.1.1 Tj/Ta Definition

Table 2.3 Tj/Ta definition

Conditions: Products with operating temperature Ta = -40 to +125°C

Parameter	Symbol	Typ.	Max.	Unit	Test conditions
Permissible junction temperature	Tj	—	140[*1]	°C	High-speed mode Middle-speed mode Low-speed mode Subosc-speed mode

Note 1. The upper limit of operating temperature is 125°C.

Note: Make sure that $Tj = T_a + \theta ja \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.

表 2.1 绝对最大评级（2/2）

范围			象征	价值	单元
高输出电流	P100 至 P102、P108 至 P110、P112、P201、P206、P300	别针	I_{OH1}	-40	mA
		所有引脚总数		-100	mA
	P010 至 P013、P212、P213	别针	I_{OH2}	-5	mA
		所有引脚总数		-20	mA
低电平输出电流	P100 至 P102、P108 至 P110、P112、P201、P206、P300	别针	I_{OL1}	40	mA
		所有引脚总数		100	mA
	P010 至 P013、P212、P213	别针	I_{OL2}	10	mA
		所有引脚总数		20	mA
环境工作温度	正常运行模式		Ta	-40 to +125	°C
	闪存编程模式			-40 to +125	°C
储存温度			测试	-65 to +150	°C

注1：使用电容（0.47至1 μF）将VCL引脚连接至VSS。所列数值为VCL引脚的绝对最大额定值。仅使用电容连接，切勿向该引脚施加任何电压。

注2. 此电压不得高于6.5 V.
注 3. 用于 A/D 转换的引脚上的电压不得超过 VREFH0+ 0.3。

注意：除非另有规定，否则在给定引脚上复用的功能的特性与端口引脚的特性相同。

注：VREFH0 指的是 A/D 转换器的正参考电压。

注：参考电压为VSS。

注意：即使任何参数的绝对最大额定值被瞬间超过，产品质量也可能受到影响。也就是说，绝对最大额定值是指产品即将遭受物理损坏时的额定值，因此必须在确保不超过绝对最大额定值的条件下使用产品。

表 2.2 推荐运行条件

范围	象征		最小。	类型。	最大限度。	单元
电源电压	VCC		1.6	—	5.5	V
	VSS		—	0	—	V
模拟电源电压	VREFH0	当用作 ADC10 时参考	1.6	—	VCC	V
	VREFL0		—	0	—	V

2.1.1Tj/Ta 定义

表 2.3 Tj/Ta 定义

条件：工作温度在Ta = -40至+125°C范围内的产品

范围	象征	类型。	最大限度。	单元	测试条件
允许的结温	Tj	—	140[*1]	°C	高速模式 中速模式 低速模式 子振荡器速度模式

注1. 工作温度的上限为125°C。

注意：确保$Tj = T_a + \theta ja \times$总功耗(W)，其中总功耗= $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$。

2.2 Oscillators Characteristics

2.2.1 On-chip Oscillators Characteristics

Table 2.4 On-chip oscillators characteristics

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
High-speed on-chip oscillator clock frequency		f_{HOCO}	1	—	32	MHz	—
High-speed on-chip oscillator clock frequency accuracy	OSCSF.HOCOSF = 1	—	-1.0	—	+1.0	%	Ta = -40 to +125°C, 1.6 V ≤ VCC ≤ 5.5 V
High-speed on-chip oscillator clock frequency trimming resolution		—	—	0.05	—	%	—
High-speed on-chip oscillator clock oscillation stabilization time[*3]		t_{HOCO}	—	—	4.4	μs	—
Low-speed on-chip oscillator clock frequency[*1]		f_{LOCO}	—	32.768	—	kHz	—
Low-speed on-chip oscillator clock frequency accuracy		—	-15	—	15	%	—
Low-speed on-chip oscillator clock frequency trimming resolution		—	—	0.3	—	%	—
Low-speed on-chip oscillator clock oscillation stabilization time		t_{LOCO}	—	—	100	μs	—
Low-speed on-chip oscillator frequency temperature coefficient		—	—	—	±0.21[*2]	%/°C	—

Note 1. The listed values only indicate the characteristics of the oscillators. Refer to AC Characteristics for instruction execution time.
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
Note 3. Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.

2.3 DC Characteristics

2.3.1 Pin Characteristics

Table 2.5 I/O I_{OH}

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Allowable high-level output current[*1]	Per pin for P100 to P102, P108 to P110, P112, P201, P206, P300	I_{OH1}	—	—	-10[*2]	mA	1.6 V ≤ VCC ≤ 5.5 V
	Total of all pins (when duty ≤ 70%[*3])		—	—	-80[*4]	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	-19	mA	2.7 V ≤ VCC < 4.0 V
			—	—	-10	mA	1.8 V ≤ VCC < 2.7 V
			—	—	-5	mA	1.6 V ≤ VCC < 1.8 V
	Per pin for P010 to P013, P212, P213	I_{OH2}	—	—	-3[*2]	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	-1[*2]	mA	2.7 V ≤ VCC < 4.0 V
			—	—	-1[*2]	mA	1.8 V ≤ VCC < 2.7 V
			—	—	-0.5[*2]	mA	1.6 V ≤ VCC < 1.8 V
	Total of all pins (when duty ≤ 70%[*3])		—	—	-20	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	-10	mA	2.7 V ≤ VCC < 4.0 V
			—	—	-5	mA	1.8 V ≤ VCC < 2.7 V
			—	—	-5	mA	1.6 V ≤ VCC < 1.8 V

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from the VCC pin to an output pin.

2.2 振荡器特性

2.2.1 片上振荡器特性

表 2.4 片上振荡器特性

条件：VCC = 1.6至5.5 V, VSS = 0 V，Ta = -40 至+125°C

范围		象征	最小。	类型。	最大限度。	单元	测试条件
高速片上振荡器时钟频率		f_{HOCO}	1	—	32	MHz	—
高速片上振荡器时钟频率精度	OSCSF.HOCOSF = 1	—	-1.0	—	+1.0	%	Ta = -40至+125°C, 1.6 V ≤ VCC ≤ 5.5 V
高速片上振荡器时钟频率微调分辨率		—	—	0.05	—	%	—
高速片上振荡器时钟振荡稳定时间[*3]		t_{HOCO}	—	—	4.4	μs	—
低速片上振荡器时钟频率[*1]		薄片	—	32.768	—	kHz	—
低速片上振荡器时钟频率精度		—	-15	—	15	%	—
低速片上振荡器时钟频率微调分辨率		—	—	0.3	—	%	—
低速片上振荡器时钟振荡稳定时间		疯狂	—	—	100	μs	—
低速片上振荡器频率温度系数		—	—	—	±0.21[*2]	%/°C	—

注1：所列数值仅表示振荡器的特性。有关指令执行时间，请参阅交流特性。
注2. 这些数值是特性评估的结果，并非出货时的检查值。
注 3. 检查 OSCSF.HOCOSF 以确认稳定时间是否已过。

2.3直流特性

2.3.1引脚特性

表 2.5 I/O IOH

条件：VCC = 1.6至5.5 V, VSS= 0 V，Ta= -40 至+125°C

范围		象征	最小。	类型。	最大限度。	单元	测试条件
允许的高电平输出电流[*1]	P100 至 P102 的每个引脚，P108 至 P110、P112、P201, P206, P300	I_{OH1}	—	—	-10[*2]	mA	1.6 V ≤ VCC ≤ 5.5 V
	所有引脚总数（当占空比为≤ 70%[*3]）		—	—	-80[*4]	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	-19	mA	2.7 V ≤ VCC < 4.0 V
			—	—	-10	mA	1.8 V ≤ VCC < 2.7 V
			—	—	-5	mA	1.6 V ≤ VCC < 1.8 V
	P010 至 P013 的每个引脚，P212, P213	I_{OH2}	—	—	-3[*2]	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	-1[*2]	mA	2.7 V ≤ VCC < 4.0 V
			—	—	-1[*2]	mA	1.8 V ≤ VCC < 2.7 V
			—	—	-0.5[*2]	mA	1.6 V ≤ VCC < 1.8 V
	所有引脚总数（当职责≤ 70%[*3]）		—	—	-20	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	-10	mA	2.7 V ≤ VCC < 4.0 V
			—	—	-5	mA	1.8 V ≤ VCC < 2.7 V
			—	—	-5	mA	1.6 V ≤ VCC < 1.8 V

注 1. 即使电流从 VCC 引脚流向输出引脚，也能保证器件在所列电流下正常工作。

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.
Note 3. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

- Total output current from the listed pins = (I_{OH} × 0.7)/(n × 0.01)
  Example when n = 80% and I_{OH} = -10.0 mA
  Total output current from the listed pins = (-10.0 × 0.7)/(80 × 0.01) = -8.75 mA
  Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. The maximum value is -50 mA with an ambient operating temperature range of 85°C to 125°C.

Note: The following pins are not capable of the output of high-level signals in the N-ch open-drain mode.
P100 to P102, P108 to P110, P112, P201, P212, P213, P300

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Table 2.6 I/O I_{OL}

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Allowable low-level output current*1	Per pin for P100 to P102, P108 to P110, P112, P201, P206, P300	I_{OL1}	—	—	20*2	mA	—
	Total of all pins (when duty ≤ 70%*3)		—	—	80*4	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	35	mA	2.7 V ≤ VCC < 4.0 V
			—	—	20	mA	1.8 V ≤ VCC < 2.7 V
			—	—	10	mA	1.6 V ≤ VCC < 1.8 V
	Per pin for P010 to P013, P212, P213	I_{OL2}	—	—	8.5*2	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	1.5*2	mA	2.7 V ≤ VCC < 4.0 V
			—	—	0.6*2	mA	1.8 V ≤ VCC < 2.7 V
			—	—	0.4*2	mA	1.6 V ≤ VCC < 1.8 V
	Total of all pins (when duty ≤ 70%*3)		—	—	20	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	20	mA	2.7 V ≤ VCC < 4.0 V
			—	—	15	mA	1.8 V ≤ VCC < 2.7 V
			—	—	10	mA	1.6 V ≤ VCC < 1.8 V

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from an output pin to VSS pin.
Note 2. The combination of these and other pins must also not exceed the value for maximum total current.
Note 3. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

- Total output current from the listed pins = (I_{OL} × 0.7)/(n × 0.01)
  Example when n = 80% and I_{OL} = 10.0 mA
  Total output current from the listed pins = (10.0 × 0.7)/(80 × 0.01) = 8.75 mA
  Note that the duty cycle has no effect on the current that is allowed to flow into a single pin.
  A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. The maximum value is 40 mA with an ambient operating temperature range of 85°C to 125°C.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

注2：这些引脚和其他引脚的组合电流不得超过最大总电流值。
注3. 所列电流适用于占空比不大于70%的情况。当占空比大于70%, 时，使用以下公式计算输出电流，其中n为占空比。

- 所列引脚的总输出电流= (I_{OH} × 0.7)/(n × 0.01)
  例如，当n = 80%和I = -10.0 mA时
  所列引脚的总输出电流= (-10.0 × 0.7)/(80 × 0.01) = -8.75 mA
  请注意，占空比对允许流入单个引脚的电流没有影响。流入单个引脚的电流不得超过绝对最大额定值。

注4. 最大值为-50 mA，环境工作温度范围为85°C 至125°C。

注意：在 N 沟道开漏模式下，以下引脚不能输出高电平信号。
P100至 P102、P108 至 P110、P112、P201、P212、P213、P300

注意：除非另有规定，否则在给定引脚上复用的功能的特性与端口引脚的特性相同。

表 2.6 I/O 人工晶状体

条件：VCC = 1.6至5.5 V, VSS = 0 V, Ta = -40 至+125°C

范围		象征	最小。	类型。	最大限度。	单元	测试条件
允许的低电平输出电流*1	P100 至 P102 的每个引脚，P108 至 P110、P112、P201, P206, P300	I_{OL1}	—	—	20*2	mA	—
	所有引脚总数（当占空比为≤ 70%*3）		—	—	80*4	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	35	mA	2.7 V ≤ VCC < 4.0 V
			—	—	20	mA	1.8 V ≤ VCC < 2.7 V
			—	—	10	mA	1.6 V ≤ VCC < 1.8 V
	P010 至 P013 的每个引脚，P212, P213	I_{OL2}	—	—	8.5*2	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	1.5*2	mA	2.7 V ≤ VCC < 4.0 V
			—	—	0.6*2	mA	1.8 V ≤ VCC < 2.7 V
			—	—	0.4*2	mA	1.6 V ≤ VCC < 1.8 V
	所有引脚总数（当职责≤ 70%*3）		—	—	20	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	20	mA	2.7 V ≤ VCC < 4.0 V
			—	—	15	mA	1.8 V ≤ VCC < 2.7 V
			—	—	10	mA	1.6 V ≤ VCC < 1.8 V

注 1. 即使电流从输出引脚流向 VSS 引脚，也能保证器件在所列电流下正常工作。
注2：这些引脚和其他引脚的组合电流也不得超过最大总电流值。
注3. 所列电流适用于占空比不大于70%的情况。当占空比大于70%, 时，使用以下公式计算输出电流，其中n为占空比。

- 所列引脚的总输出电流= (I_{OL} × 0.7)/(n × 0.01)
  例如，当n = 80% 和I_{OL} = 10.0mA
  所列引脚的总输出电流= (10.0 × 0.7)/(80 × 0.01) = 8.75 mA
  请注意，占空比对允许流入单个引脚的电流没有影响。
  单个引脚的电流不得超过其绝对最大额定值。

注4：最大值为40 mA，环境工作温度范围为85°C至125°C。

注意：除非另有规定，否则在给定引脚上复用的功能的特性与端口引脚的特性相同。

Table 2.7 I/O V_{IH}, V_{IL}

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter			Symbol	Min.	Typ.	Max.	Unit	Test conditions
Input voltage, high	P100 to P102, P108 to P110, P112, P200, P201, P206, P300	Normal input buffer	V_{IH1}	VCC × 0.8	—	VCC	V	—
	P100 to P102, P108 to P110, P112, P201, P300	TTL input buffer	V_{IH2}	2.2	—	VCC	V	4.0 V ≤ VCC ≤ 5.5 V
				2.0	—	VCC	V	3.3 V ≤ VCC < 4.0 V
				1.5	—	VCC	V	1.6 V ≤ VCC < 3.3 V
	P010 to P013		V_{IH3}	VCC × 0.7	—	VCC	V	—
	P212 to P213		V_{IH4}	VCC × 0.8	—	VCC	V	—
Input voltage, low	P100 to P102, P108 to P110, P112, P200, P201, P206, P300	Normal input buffer	V_{IL1}	0	—	VCC × 0.2	V	—
	P100 to P102, P108 to P110, P112, P201, P300	TTL input buffer	V_{IL2}	0	—	0.8	V	4.0 V ≤ VCC ≤ 5.5 V
				0	—	0.5	V	3.3 V ≤ VCC < 4.0 V
				0	—	0.32	V	1.6 V ≤ VCC < 3.3 V
	P010 to P013		V_{IL3}	0	—	VCC × 0.3	V	—
	P212 to P213		V_{IL4}	0	—	VCC × 0.2	V	—

Note: The maximum value of V_{IH} of pins P100 to P102, P108 to P110, P112, P201, P212, P213, P300 is VCC, even in the N-ch open-drain mode.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Table 2.8 I/O V_{OH}, V_{OL} (1 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Output voltage, high	P100 to P102, P108 to P110, P112, P201, P206, P300	V_{OH1}	VCC - 1.5	—	—	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -10 mA
			VCC - 0.7	—	—	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -3 mA
			VCC - 0.6	—	—	V	2.7 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -2 mA
			VCC - 0.5	—	—	V	1.8 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -1.5 mA
			VCC - 0.5	—	—	V	1.6 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -1 mA
	P010 to P013, P212, P213	V_{OH2}	VCC - 0.7	—	—	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OH}2$ = -3 mA
			VCC - 0.5	—	—	V	2.7 V ≤ VCC < 4.0 V $I_{OH}2$ = -1 mA
			VCC - 0.5	—	—	V	1.8 V ≤ VCC < 2.7 V $I_{OH}2$ = -1 mA
			VCC - 0.5	—	—	V	1.6 V ≤ VCC < 1.8 V $I_{OH}2$ = -0.5 mA

表 2.7I/O V_{IH}, V_{IL}

条件：VCC = 1.6至5.5 V, VSS= 0 V，Ta = -40 至+125°C

范围			象征	最小。	类型。	最大限度。	单元	测试条件
输入电压高	P100 至 P102, P108 至 P110, P112, P200, P201, P206, P300	普通输入缓冲区	V_{IH1}	VCC × 0.8	—	VCC	V	—
	P100 至 P102, P108 至 P110, P112, P201, P300	TTL输入缓冲器	V_{IH2}	2.2	—	VCC	V	4.0 V ≤ VCC ≤ 5.5 V
				2.0	—	VCC	V	3.3 V ≤ VCC < 4.0 V
				1.5	—	VCC	V	1.6 V ≤ VCC < 3.3 V
	P010 至 P013		V_{IH3}	VCC × 0.7	—	VCC	V	—
	P212 至 P213		V_{IH4}	VCC × 0.8	—	VCC	V	—
输入电压低	P100 至 P102, P108 至 P110, P112, P200, P201, P206, P300	普通输入缓冲区	V_{IL1}	0	—	VCC × 0.2	V	—
	P100 至 P102, P108 至 P110, P112, P201, P300	TTL输入缓冲器	V_{IL2}	0	—	0.8	V	4.0 V ≤ VCC ≤ 5.5 V
				0	—	0.5	V	3.3 V ≤ VCC < 4.0 V
				0	—	0.32	V	1.6 V ≤ VCC < 3.3 V
	P010 至 P013		V_{IL3}	0	—	VCC × 0.3	V	—
	P212 至 P213		V_{IL4}	0	—	VCC × 0.2	V	—

注意：引脚P100至P102, P108 至 P110、P112、P201、P212、P213、P300 的V_{IH}的最大值为 VCC，即使在 N 沟道开漏模式下也是如此。

注意：除非另有规定，否则在给定引脚上复用的功能的特性与端口引脚的特性相同。

表 2.8I/OV_{OH}，VOL（1/2）

条件：VCC = 1.6至5.5 V, VSS = 0 V，Ta = -40 至+125°C

范围		象征	最小。	类型。	最大限度。	单元	测试条件
输出电压高	P100 至 P102，P108 至 P110、P112、P201、P206 P300	V_{OH1}	VCC - 1.5	—		V	4.0 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -10 mA
			VCC - 0.7	—	—	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -3 mA
			VCC - 0.6	—	—	V	2.7 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -2 mA
			VCC - 0.5	—	—	V	1.8 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -1.5 mA
			VCC - 0.5	—	—	V	1.6 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -1 mA
	P010 至 P013、P212、P213	V_{OH2}	VCC - 0.7	—	—	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OH}2$ = -3 mA
			VCC - 0.5	—	—	V	2.7 V ≤ VCC < 4.0 V $I_{OH}2$ = -1 mA
			VCC - 0.5	—	—	V	1.8 V ≤ VCC < 2.7 V $I_{OH}2$ = -1 mA
			VCC - 0.5	—	—	V	1.6 V ≤ VCC < 1.8 V $I_{OH}2$ = -0.5 mA

Table 2.8 I/O V_{OH}, V_{OL} (2 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Output voltage, low	P100 to P102, P108 to P110, P112, P201, P206, P300	V_{OL1}	—	—	1.3	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 20 mA
			—	—	0.7	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 8.5 mA
			—	—	0.6	V	2.7 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 3 mA
			—	—	0.4	V	2.7 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 1.5 mA
			—	—	0.4	V	1.8 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 0.6 mA
			—	—	0.4	V	1.6 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 0.3 mA
	P010 to P013, P212, P213	V_{OL2}	—	—	0.7	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OL}2$ = 8.5 mA
			—	—	0.5	V	2.7 V ≤ VCC < 4.0 V $I_{OL}2$ = 1.5 mA
			—	—	0.4	V	1.8 V ≤ VCC < 2.7 V $I_{OL}2$ = 0.6 mA
			—	—	0.4	V	1.6 V ≤ VCC < 1.8 V $I_{OL}2$ = 0.4 mA

Note: P100 to P102, P108 to P110, P112, P201, P212, P213, P300 do not output high-level signals in the N-ch open-drain mode.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Table 2.9 I/O other characteristics

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Input leakage current, high	P100 to P102, P108 to P110, P112, P200, P201, P206, P300	I_{LIH1}	—	—	1	μA	V_I = VCC
	P010 to P013	I_{LIH2}	—	—	1	μA	V_I = VCC
	P212 to P213	I_{LIH3}	—	—	1	μA	V_I = VCC
Input leakage current, low	P100 to P102, P108 to P110, P112, P200, P201, P206, P300	I_{LIL1}	—	—	-1	μA	V_I = VSS
	P010 to P013	I_{LIL2}	—	—	-1	μA	V_I = VSS
	P212 to P213	I_{LIL3}	—	—	-1	μA	V_I = VSS
On-chip pull-up resistance	P100 to P102, P108 to P110, P112, P201, P206, P300	R_U	10	20	100	kΩ	V_I = VSS In input port
Input capacitance	P200	Cin	—	—	30	pF	Vin = 0 V, f = 1 MHz, Ta = 25°C
	Other input pins		—	—	15		

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

表 2.8I/O VOH，VOL（2/2）

条件：VCC = 1.6至5.5 V, VSS= 0 V，Ta = -40 至+125°C

范围		象征	最小。	类型。	最大限	单元	测试条件
输出电压低	P100 至 P102，P108 至 P110、P112、P201、P206 P300	V_{OL1}	—	—	度3	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 20 mA
			—	—	0.7	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 8.5 mA
			—	—	0.6	V	2.7 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 3 mA
			—	—	0.4	V	2.7 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 1.5 mA
			—	—	0.4	V	1.8 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 0.6 mA
			—	—	0.4	V	1.6 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 0.3 mA
	P010 至 P013、P212、P213	V_{OL2}	—	—	0.7	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OL}2$ = 8.5 mA
			—	—	0.5	V	2.7 V ≤ VCC < 4.0 V $I_{OL}2$ = 1.5 mA
			—	—	0.4	V	1.8 V ≤ VCC < 2.7 V $I_{OL}2$ = 0.6 mA
			—	—	0.4	V	1.6 V ≤ VCC < 1.8 V $I_{OL}2$ = 0.4 mA

注意：P100 至P102, P108 至 P110、P112、P201、P212、P213、P300 在 N 沟道开漏模式下不输出高电平信号。

注意：除非另有规定，否则在给定引脚上复用的功能的特性与端口引脚的特性相同。

表 2.9 I/O 其他特性

条件：VCC = 1.6至5.5 V, VSS= 0V，Ta= -40 至+125°C

范围		象征	最小。	类型。	最大限度。	单元	测试条件
输入漏电流高	P100 至 P102，P108 至 P110、P112、P200、P201、P206, P300	I_{LIH1}	—	—	1	μA	V_I = VCC
	P010 至 P013	I_{LIH2}	—	—	1	μA	V_I = VCC
	P212 至 P213	I_{LIH3}	—	—	1	μA	V_I = VCC
输入漏电流低	P100 至 P102，P108 至 P110、P112、P200、P201、P206, P300	I_{LIL1}	—	—	-1	μA	V_I = VSS
	P010 至 P013	I_{LIL2}	—	—	-1	μA	V_I = VSS
	P212 至 P213	I_{LIL3}	—	—	-1	μA	V_I = VSS
片上上拉电阻	P100 至 P102，P108 至 P110、P112、P201、P206 P300	R_U	10	20	100	kΩ	V_I = VSS 输入端口
输入电容	P200	吃	—	—	30	pF	Vin = 0 V, f = 1 MHz, Ta = 25°C
	其他输入引脚		—	—	15		

注意：除非另有规定，否则在给定引脚上复用的功能的特性与端口引脚的特性相同。

2.3.2 Operating and Standby Current

Table 2.10 Operating and standby current (1) (1 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter					Symbol	Typ.*4	Max.	Unit	Test Conditions
Supply current*1	High-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash	ICLK = 32 MHz	Icc	2.6	—	mA	—
			All peripheral clocks enabled, CoreMark code executing from flash*5	ICLK = 32 MHz		—	3.5		—
		Sleep mode	All peripheral clocks disabled	ICLK = 32 MHz		0.82	—		—
			All peripheral clocks enabled*5	ICLK = 32 MHz		—	1.4		—
	Middle-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash	ICLK = 16 MHz		1.5	—		—
				ICLK = 8 MHz		0.9	—		—
				ICLK = 4 MHz		0.70	—		—
			All peripheral clocks enabled, CoreMark code executing from flash*5	ICLK = 16 MHz		—	2.0		—
				ICLK = 8 MHz		—	1.3		—
				ICLK = 4 MHz		—	0.9		—
		Sleep mode	All peripheral clocks disabled	ICLK = 16 MHz		0.61	—		—
				ICLK = 8 MHz		0.50	—		—
				ICLK = 4 MHz		0.44	—		—
			All peripheral clocks enabled*5	ICLK = 16 MHz		—	0.9		—
				ICLK = 8 MHz		—	0.7		—
				ICLK = 4 MHz		—	0.6		—
	Low-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash	ICLK = 2 MHz		450	—	μA	—
			All peripheral clocks enabled, CoreMark code executing from flash*5	ICLK = 2 MHz		—	600		—
		Sleep mode	All peripheral clocks disabled	ICLK = 2 MHz		324	—		—
			All peripheral clocks enabled*5	ICLK = 2 MHz		—	448		—

2.3.2 工作电流和待机电流

表 2.10 工作电流和待机电流 (1) (1/2)

条件：VCC = 1.6至5.5 V

范围					象征	4型	最大	单元	测试状况
供电电流*1	高速模式*2	正常模式	所有外设时钟均已禁用，CoreMark 代码从闪存执行	ICLK = 32 MHz	国际商会	2.6	限度。	mA	—
			所有外设时钟均已启用，CoreMark 代码从闪存*5 执行	ICLK = 32 MHz		—	3.5		—
		睡眠模式	所有外设时钟均已禁用	ICLK = 32 MHz		0.82	—		—
			所有外设时钟均已启用*5	ICLK = 32 MHz		—	1.4		—
	中速模式*2	正常模式	所有外设时钟均已禁用，CoreMark 代码从闪存执行	ICLK = 16 MHz		1.5	—		—
				ICLK = 8 MHz		0.9	—		—
				ICLK = 4 MHz		0.70	—		—
			所有外设时钟已启用，CoreMark 代码正在执行 来自闪光灯*5	ICLK = 16 MHz		—	2.0		—
				ICLK = 8 MHz		—	1.3		—
				ICLK = 4 MHz		—	0.9		—
		睡眠模式	所有外设时钟均已禁用	ICLK = 16 MHz		0.61	—		—
				ICLK = 8 MHz		0.50	—		—
				ICLK = 4 MHz		0.44	—		—
			所有外设时钟均已启用*5	ICLK = 16 MHz		—	0.9		—
				ICLK = 8 MHz		—	0.7		—
				ICLK = 4 MHz		—	0.6		—
	低速模式*2	正常模式	所有外设时钟均已禁用，CoreMark 代码从闪存执行	ICLK = 2 MHz		450	—	μA	—
			所有外设时钟均已启用，CoreMark 代码从闪存*5 执行	ICLK = 2 MHz		—	600		—
		睡眠模式	所有外设时钟均已禁用	ICLK = 2 MHz		324	—		—
			所有外设时钟均已启用*5	ICLK = 2 MHz		—	448		—

Table 2.10 Operating and standby current (1) (2 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter						Symbol	Typ.*4	Max.	Unit	Test Conditions
Supply current*1	Subosc-speed mode*3	Normal mode	Peripheral clocks disabled	ICLK = 32.768 kHz	Ta = -40°C	Icc	2.8	—	μA	—
					Ta = 25°C		3.0	—		
					Ta = 50°C		3.2	—		
					Ta = 70°C		3.3	—		
					Ta = 85°C		3.6	—		
					Ta = 105°C		4.2	—		
					Ta = 125℃		5.5	—		
			Peripheral clocks enabled*6	ICLK = 32.768 kHz	Ta = -40°C		—	6.0		
					Ta = 25°C		—	6.2		
					Ta = 50°C		—	9.2		
					Ta = 70°C		—	12.6		
					Ta = 85°C		—	15.9		
					Ta = 105°C		—	21.7		
					Ta = 125℃		—	42.0		
		Sleep mode	Peripheral clocks disabled	ICLK = 32.768 kHz	Ta = -40°C		0.8	—		—
					Ta = 25°C		0.9	—		
					Ta = 50°C		1.0	—		
					Ta = 70°C		1.1	—		
					Ta = 85°C		1.3	—		
					Ta = 105°C		1.7	—		
					Ta = 125℃		2.9	—		
			Peripheral clocks enabled*6	ICLK = 32.768 kHz	Ta = -40°C		—	3.6		
					Ta = 25°C		—	3.8		
					Ta = 50°C		—	6.2		
					Ta = 70°C		—	9.3		
					Ta = 85°C		—	12.6		
					Ta = 105°C		—	18.7		
					Ta = 125℃		—	38.5		

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The clock source is high-speed on-chip oscillator (HOCO).
Note 3. The clock source is LOCO.
Note 4. VCC = 3.3 V.
Note 5. Includes operating current for PCLBUZ, TAU, SAU, and IICA functions only. For other peripheral operating currents, please add the current in Peripheral Functions Supply current in Table 2.12.
Note 6. Includes operating current for PCLBUZ, TAU and SAU functions only. For other peripheral operating currents, please add the current in Peripheral Functions Supply current in Table 2.12.

表 2.10 工作电流和待机电流 (1) (2/2)

条件：VCC = 1.6至5.5 V

范围						象征	4型	最大限度。	单元	测试状况
供电电流*1	次振荡模式*3	正常模式	外围时钟已禁用	ICLK = 32.768 kHz	Ta = -40°C	国际商会	2.8	—	μA	—
					Ta = 25°C		3.0	—		
					Ta = 50°C		3.2	—		
					Ta = 70°C		3.3	—		
					Ta = 85°C		3.6	—		
					Ta = 105°C		4.2	—		
					Ta = 125℃		5.5	—		
			外围时钟已启用*6	ICLK = 32.768 kHz	Ta = -40°C		—	6.0		
					Ta = 25°C		—	6.2		
					Ta = 50°C		—	9.2		
					Ta = 70°C		—	12.6		
					Ta = 85°C		—	15.9		
					Ta = 105°C		—	21.7		
					Ta = 125℃		—	42.0		
		睡眠模式	外围时钟已禁用	ICLK = 32.768 kHz	Ta = -40°C		0.8	—		—
					Ta = 25°C		0.9	—		
					Ta = 50°C		1.0	—		
					Ta = 70°C		1.1	—		
					Ta = 85°C		1.3	—		
					Ta = 105°C		1.7	—		
					Ta = 125℃		2.9	—		
			外围时钟已启用*6	ICLK = 32.768 kHz	Ta = -40°C		—	3.6		
					Ta = 25°C		—	3.8		
					Ta = 50°C		—	6.2		
					Ta = 70°C		—	9.3		
					Ta = 85°C		—	12.6		
					Ta = 105°C		—	18.7		
					Ta = 125℃		—	38.5		

注1：电源电流是指流入VCC的总电流。电源电流值适用于内部上拉MOS管处于截止状态的情况，并且这些值不包括任何引脚的输出充放电电流。

注2：时钟源为高速片上振荡器（HOCO）。
注3.时钟源为LOCO。
Note 4. VCC = 3.3 V.
注5：仅包含PCLBUZ、TAU、SAU和IICA功能的运行电流。其他外围设备的运行电流，请参考表2.12中的“外围设备供电电流”部分。

注6：仅包含PCLBUZ、TAU和SAU功能的运行电流。其他外设的运行电流，请参考表2.12中的“外设功能供电电流”部分。

Table 2.11 Operating and standby current (2)

Conditions: VCC = 1.6 to 5.5 V

Parameter				Symbol	Typ.*3	Max.	Unit	Test conditions
Supply current*1	Software Standby mode*2	Peripheral modules stop	Ta = -40°C	Icc	0.2	0.9	μA	—
			Ta = 25°C		0.2	0.9		
			Ta = 50°C		0.3	2.2		
			Ta = 70°C		0.4	4.7		
			Ta = 85°C		0.5	8.1		
			Ta = 105°C		1.1	17		
			Ta = 125℃		2.3	35		

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The IWDT and LVD are not operating.
Note 3. VCC = 3.3 V.

Table 2.12 Peripheral Functions Supply current

Conditions: VCC = 1.6 to 5.5 V

Parameter				Symbol	Typ.*10	Max.	Unit	Test conditions
Peripheral Functions Supply current*1	High-speed on chip oscillator operating current*1		OFS1.HOCOFRQ1[2:0] are 010b	I_{HOCO}	320	—	μA	—
	Low-speed on chip oscillator operating current*1			I_{LOCO}	0.24	—	μA	—
	32-bit interval timer operating current*1*2*3			I_{IT}	0.06	—	μA	—
	Independent watchdog timer operating current*1*2*4		f_{LOCO} = 32.768 kHz (typ.)	I_{IWDT}	0.03	—	μA	—
	A/D converter operating current*1*5	When conversion at maximum speed	Normal mode, VREFH0 = VCC = 5.0 V	I_{ADC}	1.3	1.7	mA	—
			Low voltage mode, VREFH0 = VCC = 3.0 V		0.5	0.7	mA	—
	A/D converter internal reference voltage current*1			I_{ADREF}	100	—	μA	—
	Temperature sensor operating current*1			I_{TMPS}	100	—	μA	—
	LVD operating current*1		LVD0 is enabled*7	I_{LVD0}	0.03	—	μA	—
			LVD1 is enabled*8	I_{LVD1}	0.03	—	μA	—
	Self-programming operating current*1*9			I_{FSP}	—	12.2	mA	—
	DTC		Data transfer to RAM	I_{DTC}	1.82	—	mA	—

Note 1. This current flows into V_{CC}.
Note 2. The listed currents apply when the high-speed on-chip oscillator (HOCO) is stopped.
Note 3. This current only flows to the 32-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator (LOCO).
The supply current of the RA0 microcontrollers is the sum of either Icc and I_{IT}.
When the low-speed on-chip oscillator (LOCO) is selected, I_{LOCO} should be included in the supply current.
Note 4. This current only flows to the independent watchdog timer. It does not include the operating current of the low-speed on-chip oscillator (LOCO) .
The supply current of the RA0 microcontrollers is the sum of either Icc, I_{IWDT} and I_{LOCO}.
Note 5. This current only flows to the A/D converter. The supply current of the RA0 microcontrollers is the sum of Icc and I_{ADC} when the A/D converter is operating or in the SLEEP mode.
Note 6. This current flows into VREFH0.
Note 7. This current only flows to the LVD0 circuit. The supply current of the RA0 microcontrollers is the sum of Icc and I_{LVD0} when the LVD0 circuit is in operation.
Note 8. This current only flows to the LVD1 circuit. The supply current of the RA0 microcontrollers is the sum of Icc and I_{LVD1} when the LVD1 circuit is in operation.
Note 9. This current only flows during self programming.
Note 10. VCC = 3.3 V.

表 2.11 工作电流和待机电流 (2)

条件：VCC = 1.6至5.5 V

范围				象征	类型.*3	最大限度。	单元	测试条件
供电电流*1	软件待机模式*2	外围模块停止	Ta = -40°C	国际商会	0.2	0.9	μA	—
			Ta = 25°C		0.2	0.9		
			Ta = 50°C		0.3	2.2		
			Ta = 70°C		0.4	4.7		
			Ta = 85°C		0.5	8.1		
			Ta = 105°C		1.1	17		
			Ta = 125℃		2.3	35		

注1：电源电流是指流入VCC的总电流。电源电流值适用于内部上拉MOS管处于截止状态的情况，并且这些值不包括任何引脚的输出充放电电流。

注2. IWDT和LVD未运行。
Note 3. VCC = 3.3 V.

表 2.12 外围功能供电电流

条件：VCC = 1.6到 5.5 V

范围				象征	类型*10	最大限度。	单元	测试条件
外围功能供电电流*1	高速片上振荡器工作电流*1		OFS1.HOCOFRQ1[2:0] are 010b	I_{HOCO}	320	—	μA	—
	低速片上振荡器工作电流*1			I_{LOCO}	0.24	—	μA	—
	32 位间隔定时器工作电流*1*2*3			I_{IT}	0.06	—	μA	—
	独立看门狗定时器工作电流*1*2*4		fLOCO= 32.768 kHz（典型值）	I_{IWDT}	0.03	—	μA	—
	A/D转换器工作电流*1*5	转换时最高速度	正常模式，VREFH0= VCC = 5.0 V	I_{ADC}	1.3	1.7	mA	—
			低电压模式，VREFH0= VCC = 3.0 V		0.5	0.7	mA	—
	A/D转换器内部参考电压电流*1			I_{ADREF}	100	—	μA	—
	温度传感器工作电流*1			I_{TMPS}	100	—	μA	—
	低压差线性稳压器工作电流*1		LVD0 已启用*7	I_{LVD0}	0.03	—	μA	—
			LVD1 已启用*8	I_{LVD1}	0.03	—	μA	—
	自编程工作电流*1*9			I_{FSP}	—	12.2	mA	—
	DTC		数据传输到内存	I_{DTC}	1.82	—	mA	—

注1. 此电流流入V_{CC}.
注 2. 所列电流适用于高速片上振荡器 (HOCO) 停止工作的情况。
注3. 此电流仅流向32位间隔定时器。它不包括低速片上振荡器（LOCO）的工作电流。

RA0 微控制器的供电电流是 Icc 和I_{IT}之和。
选择低速片上振荡器 (LOCO) 时，应将 ILOCO 包含在电源电流中。
注 4. 此电流仅流向独立看门狗定时器。它不包括低速片上振荡器 (LOCO) 的工作电流。

RA0 微控制器的供电电流是 Icc、IIWDT 和 ILOCO 之和。
注5. 此电流仅流向A/D转换器。当A/D转换器工作或处于睡眠模式时，RA0微控制器的供电电流为Icc和I_{ADC}之和。

注 6. 此电流流入 VREFH0。
注7：该电流仅流向LVD0电路。当LVD0电路工作时，RA0微控制器的供电电流为Icc和ILVD0之和。

注8. 此电流仅流向LVD1电路。当LVD1电路工作时，RA0微控制器的供电电流是Icc和I_{LVD1}之和。

注9：此电流仅在自编程期间流动。
Note 10. VCC = 3.3 V.

2.3.3 Thermal Characteristics

The maximum value of junction temperature (Tj) must not exceed the value specified in the section 2.1.1. Tj/Ta Definition.

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption
  Tj : Junction Temperature (°C)
  Ta : Ambient Temperature (°C)
  Tt : Top Center Case Temperature (°C)
  θja : Thermal Resistance of "Junction"-to-"Ambient" (°C/W)
  Ψjt : Thermal Resistance of "Junction"-to-"Top Center Case" (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (I_{OL} × V_{OL}) / Voltage + Σ (|I_{OH}| × |VCC – V_{OH}|) / Voltage
- Dynamic current of IO = Σ IO (Cin + Cload) × IO switching frequency × Voltage
  Cin: Input capacitance
  Cload: Output capacitance

Regarding θja and Ψjt, see Table 2.13.

Table 2.13 Thermal resistance

Parameter	Package	Symbol	Value[*1]	Unit	Test condition
Thermal resistance	20-pin TSSOP	θja	76.0	°C/W	JESD 51-2 and 51-7 compliant
	20-pin TSSOP	Ψjt	2.95	°C/W	JESD 51-2 and 51-7 compliant

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

2.4 AC Characteristics

Table 2.14 AC characteristics (1 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter			Symbol	Min.	Typ.	Max.	Unit	Test conditions
Instruction cycle (minimum instruction execution time)	Main system clock (FMAIN) operation	High-speed mode	T_{CY}	0.03125	—	1	μs	1.8 V ≤ VCC ≤ 5.5 V
				0.25	—	1	μs	1.6 V ≤ VCC < 1.8 V
		Middle-speed mode		0.0625	—	1	μs	1.8 V ≤ VCC ≤ 5.5 V
				0.25	—	1	μs	1.6 V ≤ VCC < 1.8 V
		Low-speed mode		0.5	—	1	μs	1.6 V ≤ VCC ≤ 5.5 V
	Subsystem clock (FSUB) operation			26.041	30.5	31.3	μs	1.6 V ≤ VCC ≤ 5.5 V
	In the self-programming mode	High-speed mode		0.03125	—	1	μs	1.8 V ≤ VCC ≤ 5.5 V
		Middle-speed mode		0.0625	—	1	μs	1.8 V ≤ VCC ≤ 5.5 V
TI00 to TI07 input high-level width, low-level width			t_{TIH} t_{TIL}	$1/f_{MCK}$ +10[*1]	—	—	ns	

2.3.3 热特性

The maximum value of junction temperature (Tj) must not exceed the value specified in the section 2.1.1. Tj/Ta Definition.

Tj 可通过以下任一公式计算。

- Tj = Ta + θja ×总功耗
- Tj = Tt + Ψjt ×总功耗
  Tj:结温(°C)
  Ta：环境温度(°C)
  Tt：顶部中心外壳温度(°C)
  θja:结到环境的热阻(°C/W)
  Ψjt：结到"顶部中心外壳"的热阻(°C/W)
- 总功耗= 电压×（漏电流+ 动态电流）
- IO = Σ 的漏电流 (I_{OL} × V_{OL}) / Voltage + Σ (|I_{OH}| × |VCC – V_{OH}|) / Voltage
- 动态电流IO = Σ IO(Cin + Cload) × IO开关频率×电压
  Cin：输入电容
  Cload：输出电容

关于θja 和Ψjt，请参见表 2.13。

表 2.13 热阻

范围	包裹	象征	值*1	单元	测试条件
热阻	20引脚TSSOP封装	θja	76.0	°C/W	符合 JESD 51-2 和 51-7 标准
	20引脚TSSOP封装	Ψjt	2.95	°C/W	符合 JESD 51-2 和 51-7 标准

注1：这些数值是使用四层板时的参考值。热阻取决于层数或电路板尺寸。详情请参阅JEDEC标准。

2.4AC特性

表 2.14 交流特性（1/2）

条件：VCC = 1.6至5.5 V, VSS= 0 V, Ta = -40 至+125°C

范围			象征	最小。	类型。	最大限度。	单元	测试条件
指令周期（最短指令执行时间）	主系统时钟（FMAIN）操作	高速模式	T_{CY}	0.03125	—	1	μs	1.8 V ≤ VCC ≤ 5.5 V
				0.25	—	1	μs	1.6 V ≤ VCC < 1.8 V
		中速模式		0.0625	—	1	μs	1.8 V ≤ VCC ≤ 5.5 V
				0.25	—	1	μs	1.6 V ≤ VCC < 1.8 V
		低速模式		0.5	—	1	μs	1.6 V ≤ VCC ≤ 5.5 V
	子系统时钟（FSUB） 手术			26.041	30.5	31.3	μs	1.6 V ≤ VCC ≤ 5.5 V
	在自编程模式下	高速模式		0.03125	—	1	μs	1.8 V ≤ VCC ≤ 5.5 V
		中速模式		0.0625	—	1	μs	1.8 V ≤ VCC ≤ 5.5 V
TI00 至 TI07 输入高电平宽度、低电平宽度			t_{TIH} t_{TIL}	$1/f_{MCK}$ +10[*1]	—	—	ns	

Table 2.14 AC characteristics (2 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
TO00 to TO07 output frequency	High-speed mode Middle-speed mode	f_{TO}	—	—	16*2	MHz	4.0 V ≤ VCC ≤ 5.5 V
			—	—	8	MHz	2.7 V ≤ VCC < 4.0 V
			—	—	4	MHz	1.8 V ≤ VCC < 2.7 V
			—	—	2	MHz	1.6 V ≤ VCC < 1.8 V
	Low-speed mode		—	—	2	MHz	1.6 V ≤ VCC ≤ 5.5 V
PCLBUZ0 output frequency	High-speed mode Middle-speed mode	f_{PCL}	—	—	16*2	MHz	4.0 V ≤ VCC ≤ 5.5 V
			—	—	8	MHz	2.7 V ≤ VCC < 4.0 V
			—	—	4	MHz	1.8 V ≤ VCC < 2.7 V
			—	—	2	MHz	1.6 V ≤ VCC < 1.8 V
	Low-speed mode		—	—	2	MHz	1.6 V ≤ VCC ≤ 5.5 V
Interrupt input high-level width, low-level width	NMI/IRQ0, IRQ1 to IRQ5	f_{IRQH} f_{IRQL}	1	—	—	μs	1.6 V ≤ VCC ≤ 5.5 V

Note 1. f_{MCK}: Timer array unit operating clock frequency
To set this operating clock, use the CKS[1:0] bits of the timer mode register 0n (TMR0n).
m: Unit number (m = 0), n: Channel number (n = 0 to 7)
Note 2. The maximum value is 12MHz with an ambient operating temperature range of 105°C to 125°C.

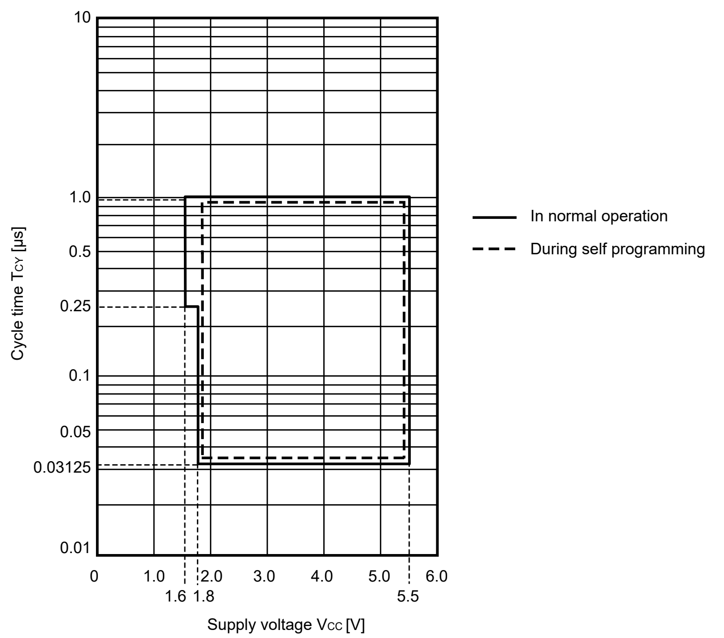


Figure 2.2 T_{CY} vs V_{CC} in High-speed mode

表 2.14 交流特性（2/2）

条件：VCC = 1.6至5.5 V, VSS= 0V，Ta = -40 至+125°C

范围		象征	最小。	类型。	最大限	单元	测试条件
TO00至TO07输出频率	高速模式中速模式	f_{TO}	—	—	16*2	MHz	4.0 V ≤ VCC ≤ 5.5 V
			—	—	8	MHz	2.7 V ≤ VCC < 4.0 V
			—	—	4	MHz	1.8 V ≤ VCC < 2.7 V
			—	—	2	MHz	1.6 V ≤ VCC < 1.8 V
	低速模式		—	—	2	MHz	1.6 V ≤ VCC ≤ 5.5 V
PCLBUZ0 输出频率	高速模式中速模式	f_{PCL}	—	—	16*2	MHz	4.0 V ≤ VCC ≤ 5.5 V
			—	—	8	MHz	2.7 V ≤ VCC < 4.0 V
			—	—	4	MHz	1.8 V ≤ VCC < 2.7 V
			—	—	2	MHz	1.6 V ≤ VCC < 1.8 V
	低速模式		—	—	2	MHz	1.6 V ≤ VCC ≤ 5.5 V
中断输入高电平宽度，低电平宽度	NMI/IRQ0, IRQ1 到 IRQ5	f_{IRQH} f_{IRQL}	1	—	—	μs	1.6 V ≤ VCC ≤ 5.5 V

注1. fMCK：定时器阵列单元工作时钟频率
要设置此工作时钟，请使用定时器模式寄存器 0n (TMR0n) 的 CKS[1:0] 位。
m：单元编号(m = 0)，n：通道编号(n = 0 至7)
注2. 最大值为12MHz，环境工作温度范围为105°C 至125°C。

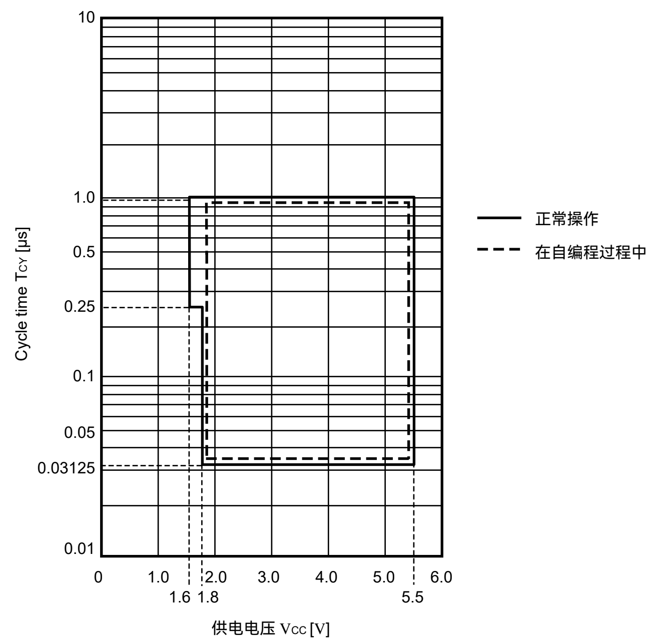


图 2.2 高速模式下 TCY 与Vcc的关系

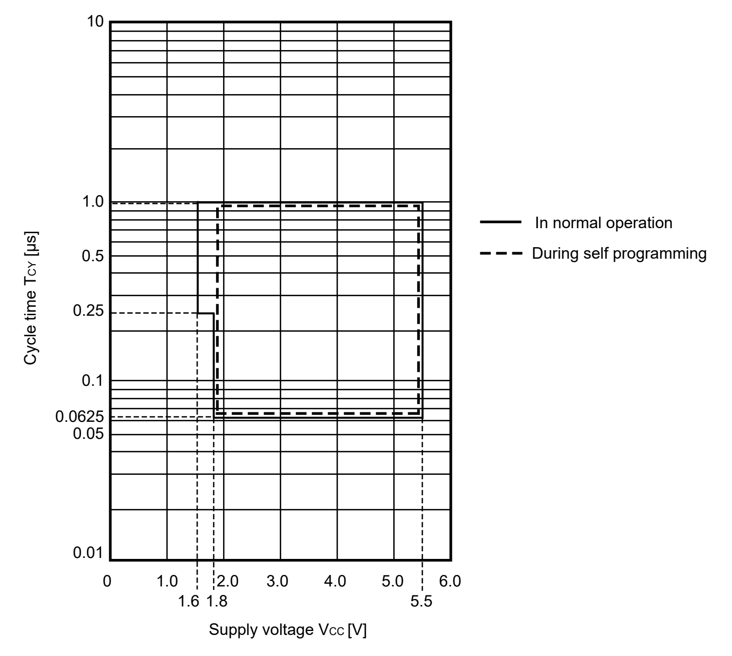


Figure 2.3 T_{CY} vs V_{CC} in Middle-speed mode

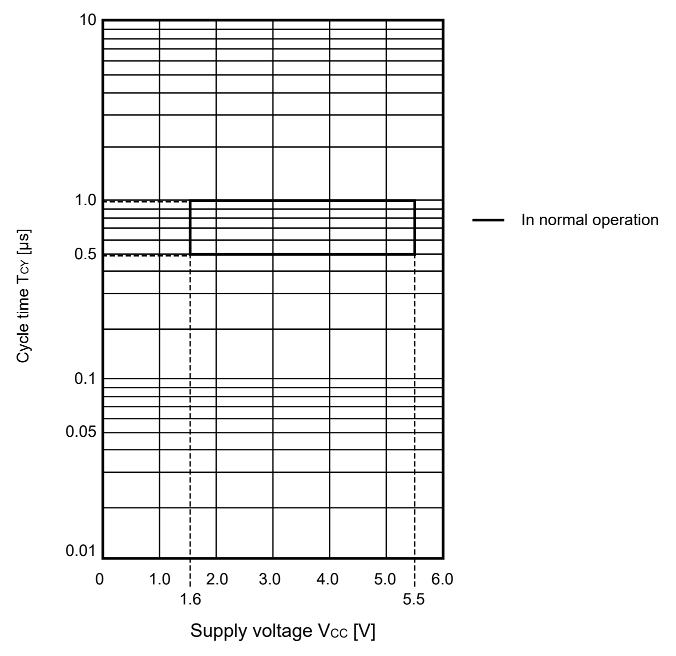


Figure 2.4 T_{CY} vs V_{CC} in Low-speed mode

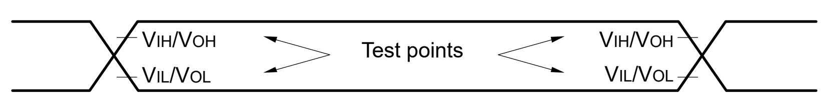


Figure 2.5 AC timing test points

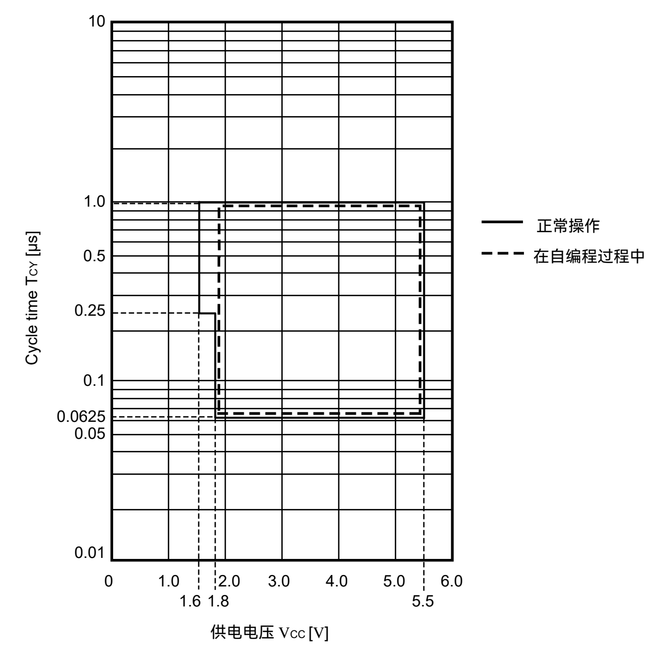


图 2.3 中速模式下 TCY 与VCC的关系

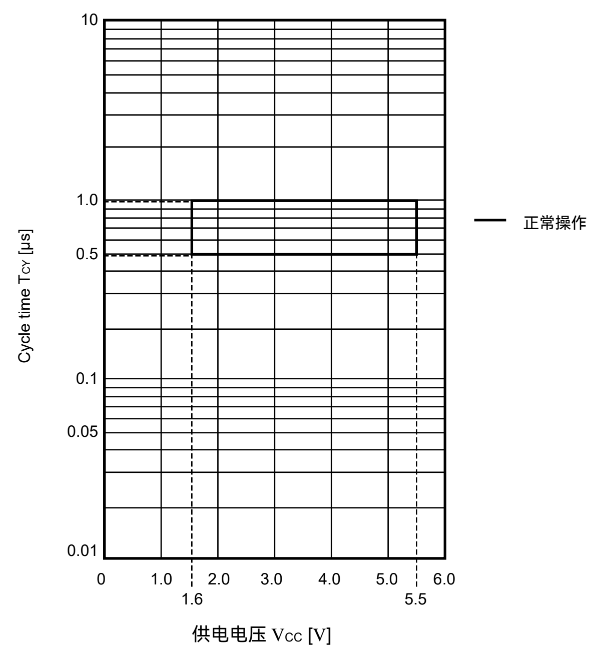


图 2.4 低速模式下 TCY 与VCC的关系

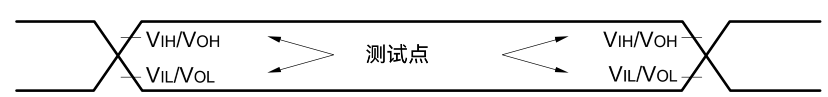


图 2.5AC 时序测试点

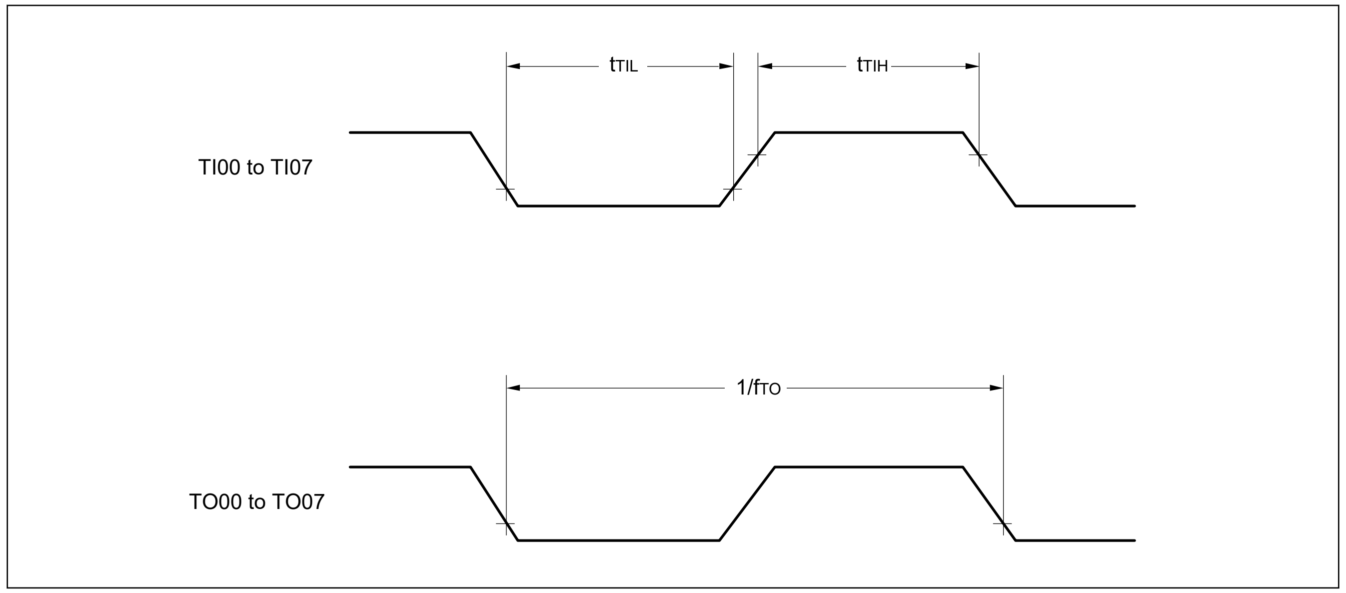


Figure 2.6 TI/TO timing

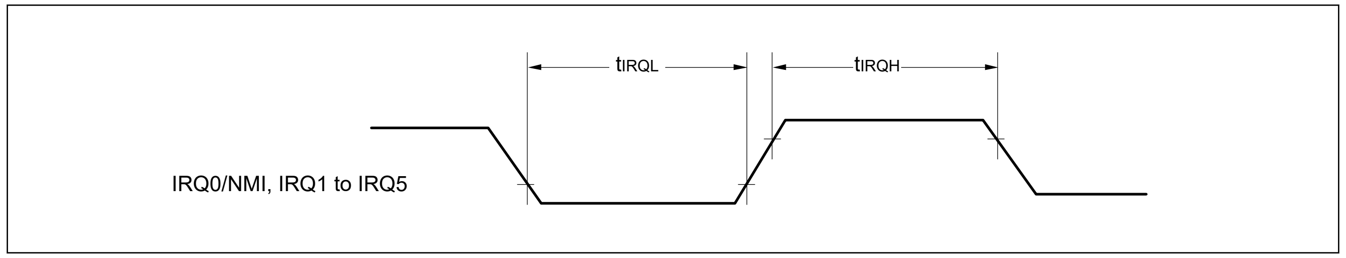


Figure 2.7 IRQ interrupt input timing

2.4.1 Reset Timing

Table 2.15 Reset timing

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
RES pulse width	At power-on*3	t_{RESWP}	9.9	—	—	ms	—
	Not at power-on	t_{RESW}	10	—	—	μs	—
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	t_{RESWT}	—	0.506	0.694	ms	—
	LVD0 disabled*2		—	0.201	0.335	ms	—
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	t_{RESWT2}	—	0.476	0.616	ms	—
	LVD0 disabled*2		—	0.170	0.257	ms	—
Internal reset by Independent watch dog timer reset, software reset		t_{RESW2}	—	0.04	0.041	ms	—

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. When RES pin is not used as the external reset input, this specification can be ignored.

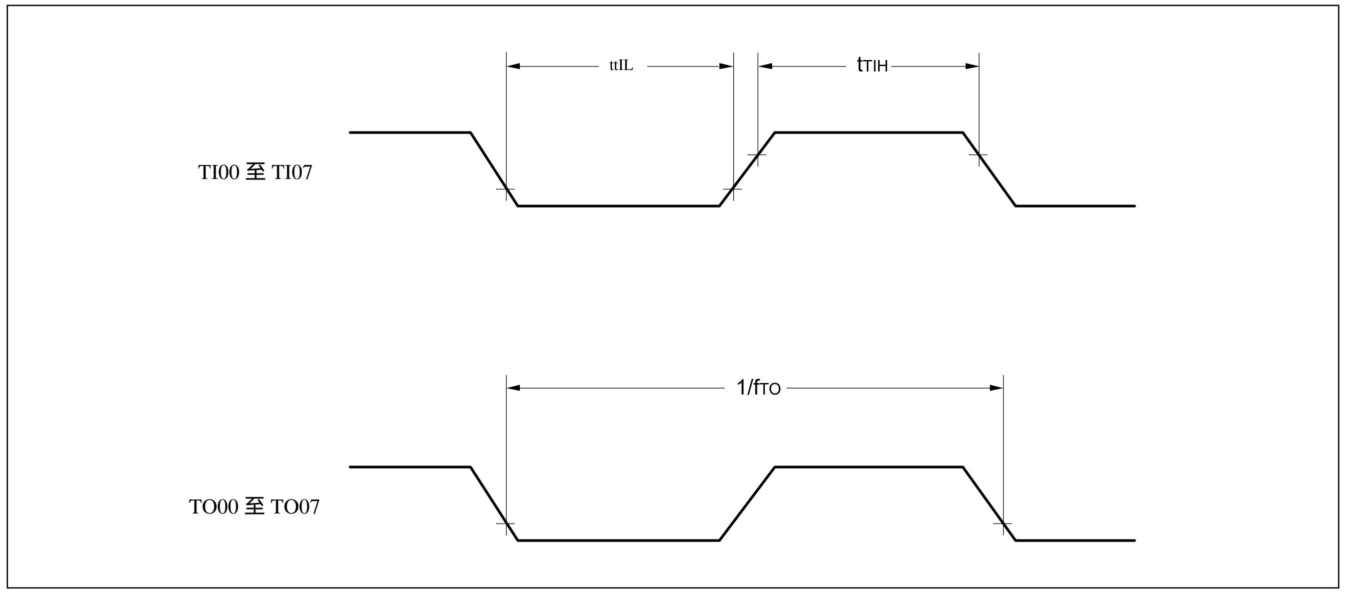


图 2.6TI/TO 时序

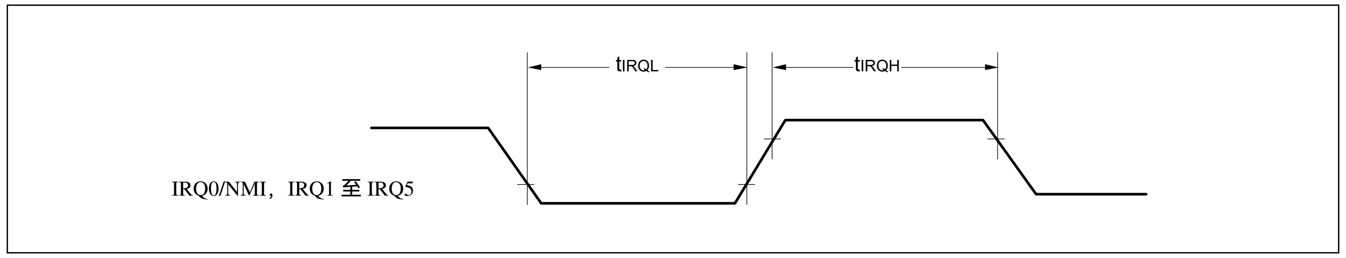


图 2.7 IRQ 中断输入时序

2.4.1 复位时序

表 2.15 复位时序

范围		象征	最小。	类型。	最大限度。	单元	测试条件
RES脉冲宽度	开机时*3	t_{RESWP}	9.9	—	—	ms	—
	未通电	t_{RESW}	10	—	—	μs	—
取消预订后的等待时间（开机时）	LVD0 已启用*1	t_{RESWT}	—	0.506	0.694	ms	—
	LVD0 已禁用*2		—	0.201	0.335	ms	—
取消预订后的等待时间（通电状态下）	LVD0 已启用*1	t_{RESWT2}	—	0.476	0.616	ms	—
	LVD0 已禁用*2		—	0.170	0.257	ms	—
内部复位方式包括独立看门狗定时器复位和软件复位		t_{RESW2}	—	0.04	0.041	ms	—

注1. 当 OFS1.LVDAS= 0时。
注2. 当 OFS1.LVDAS= 1时。
注 3. 当 RES 引脚未用作外部复位输入时，可以忽略此规范。

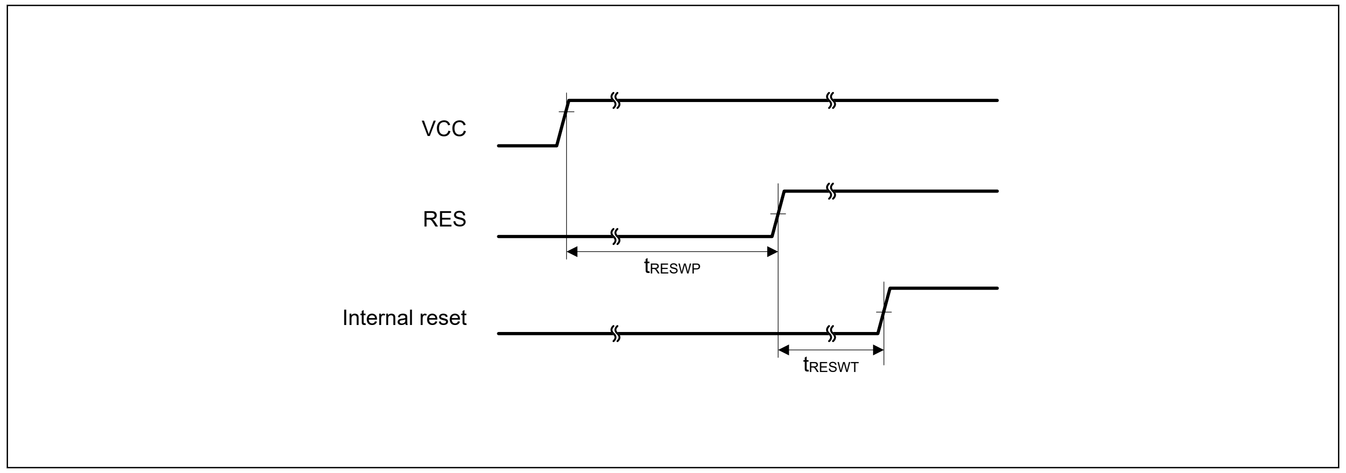


Figure 2.8 Reset input timing at power-on

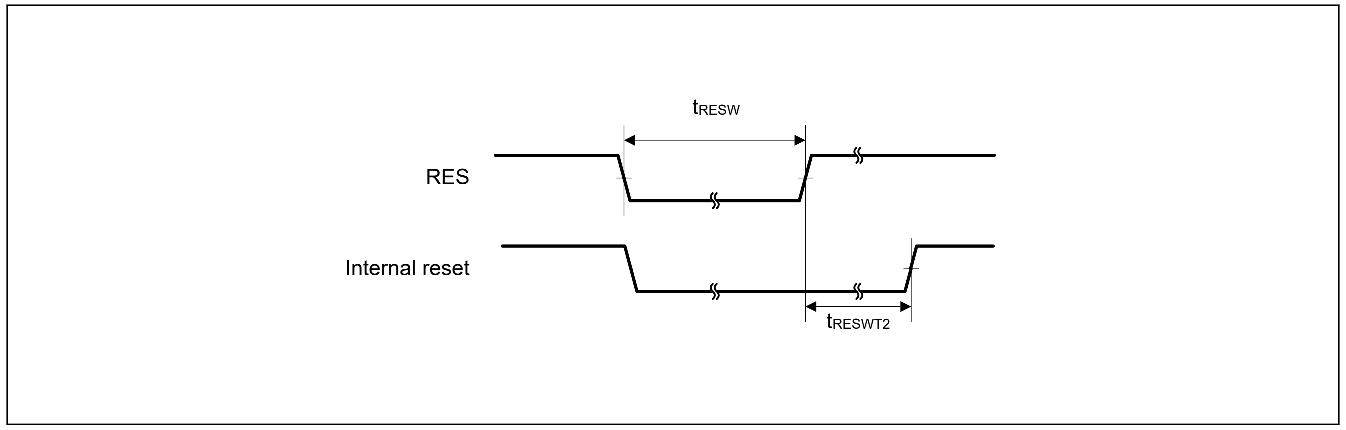


Figure 2.9 Reset input timing (1)

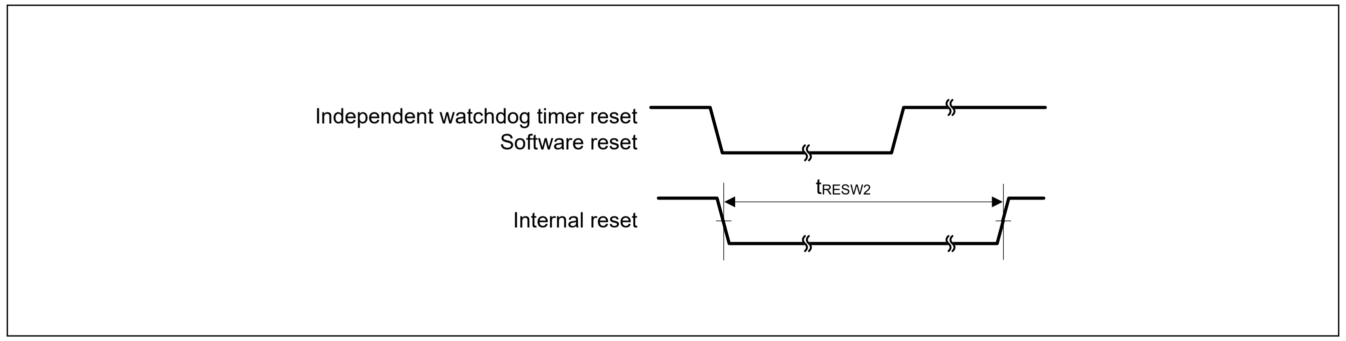


Figure 2.10 Reset input timing (2)

2.4.2 Wakeup Time

Table 2.16 Timing of recovery from low power modes (1)

Parameter				Symbol	Min.	Typ.	Max.	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	System clock source is HOCO	System clock source is HOCO (32 MHz) VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	5.3	5.7	μs	Figure 2.11
			System clock source is HOCO (4 MHz) VCC = 1.6 V to 1.8 V		—	7.3	7.7	μs	

Note 1. The division ratio of ICLK is the minimum division ratio within the allowable frequency range.
The recovery time is determined by the system clock source.

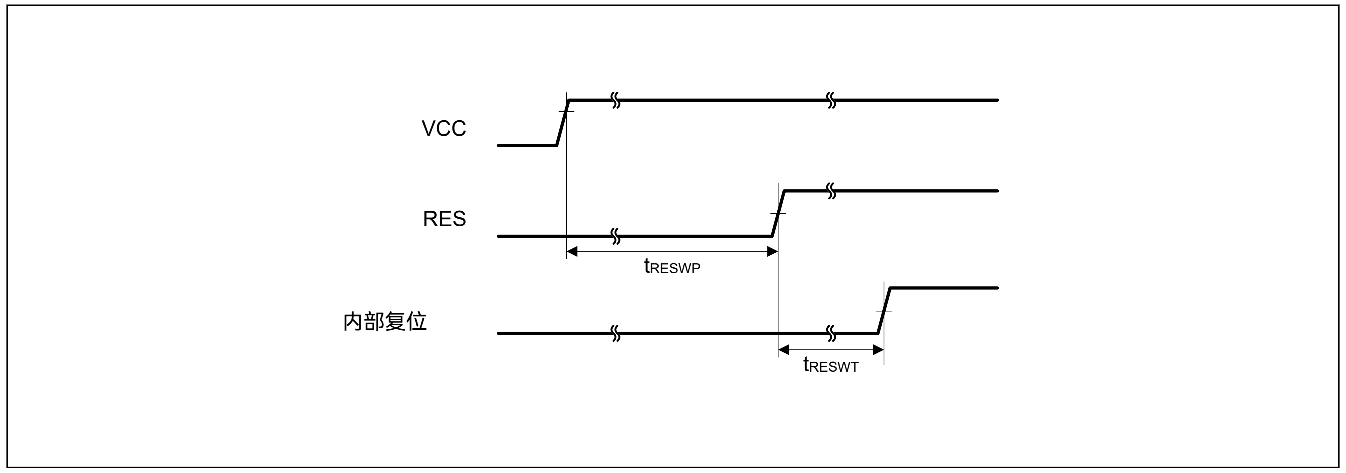


图 2.8 上电时的复位输入时序

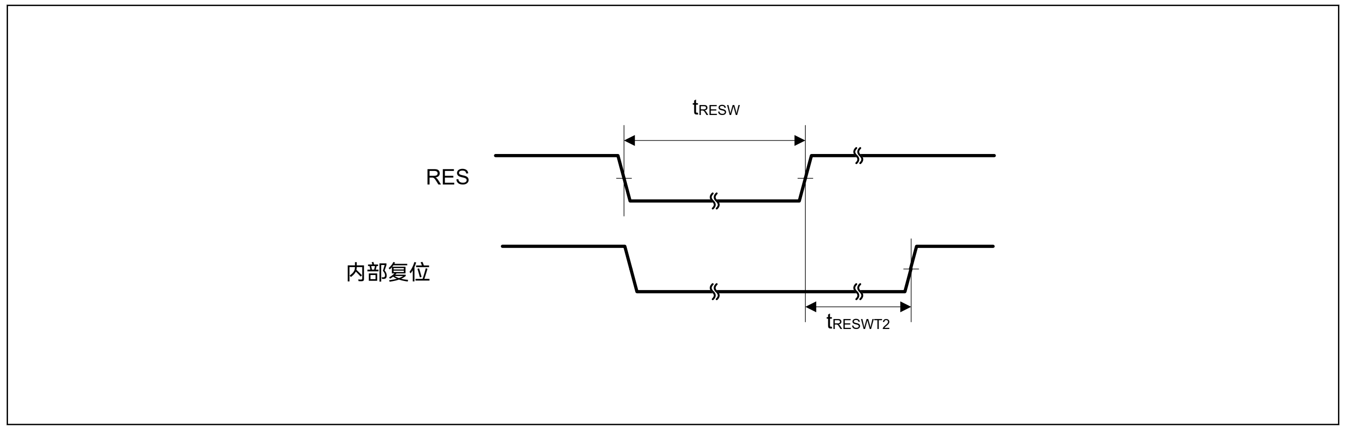


图 2.9 复位输入时序 (1)

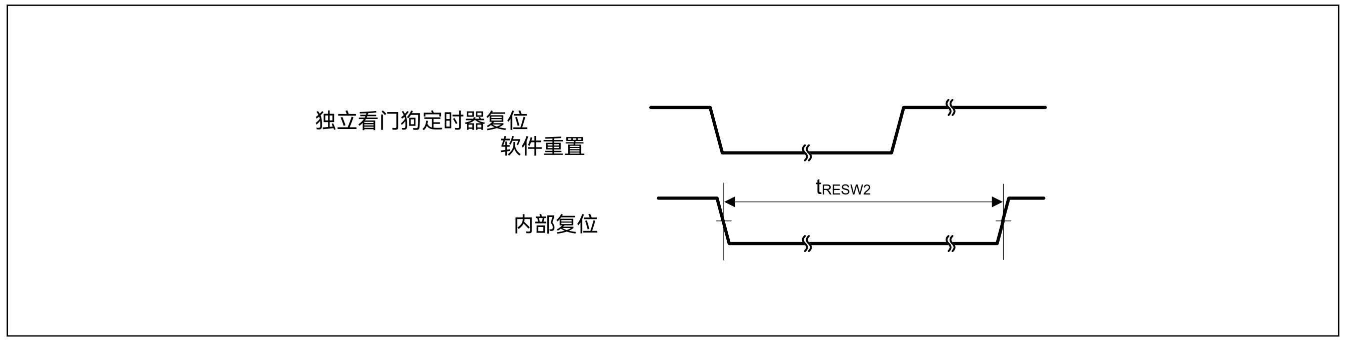


图 2.10 复位输入时序 (2)

2.4.2 起床时间

表 2.16 低功耗模式恢复时间 (1)

范围				象征	最小。	类型。	最大	单元	测试条件
软件待机模式恢复时间*1	高速模式	系统时钟源是 HOCO	系统时钟源为 HOCO (32 MHz) VCC= 10.8 V 至 5.5 V	t_{SBYHO}	—	5.3	限度。	μs	图 2.11
			系统时钟源为 HOCO (4 MHz)VCC = 1.6 V 至 1.8 V		—	7.3	7.7	μs	

注1. ICLK的分频比是允许频率范围内的最小分频比。
恢复时间由系统时钟源决定。

Table 2.17 Timing of recovery from low power modes (2)

Parameter				Symbol	Min.	Typ.	Max.	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	System clock source is HOCO	System clock source is HOCO (16 MHz) VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	5.5	5.8	μs	Figure 2.11
			System clock source is HOCO (4 MHz) VCC = 1.6 V to 1.8 V		—	7.3	7.7	μs	

Note 1. The division ratio of ICLK is the minimum division ratio within the allowable frequency range.
The recovery time is determined by the system clock source.

Table 2.18 Timing of recovery from low power modes (3)

Parameter			Symbol	Min.	Typ.	Max.	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	System clock source is HOCO (2 MHz)	t_{SBYHO}	—	10.0	10.5	μs	Figure 2.11

Note 1. The division ratio of ICLK is the minimum division ratio within the allowable frequency range.
The recovery time is determined by the system clock source.

Table 2.19 Timing of recovery from low power modes (4)

Parameter			Symbol	Min.	Typ.	Max.	Unit	Test conditions
Recovery time from Software Standby mode*1	Subosc-speed mode	System clock source is LOCO (32.768 kHz)	t_{SBYLO}	—	0.29	0.36	ms	Figure 2.11

Note 1. The LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

表 2.17 低功耗模式恢复时间 (2)

范围				象征	最小。	类型。	最大限度。	单元	测试条件
软件待机模式恢复时间*1	中速模式	系统时钟源为 HOCO	系统时钟源为 HOCO (16 MHz)VCC = 1.8 V至 5.5 V	t_{SBYHO}	—	5.5	5.8	μs	图 2.11
			系统时钟源为 HOCO (4 MHz)VCC = 1.6 V至 1.8 V		—	7.3	7.7	μs	

注1. ICLK的分频比是允许频率范围内的最小分频比。
恢复时间由系统时钟源决定。

表 2.18 低功耗模式恢复时间 (3)

范围			象征	最小。	类型。	最大限度。	单元	测试条件
软件待机模式恢复时间*1	低速模式	系统时钟源为 HOCO（2 MHz）	t_{SBYHO}	—	10.0	10.5	μs	图 2.11

注1. ICLK的分频比是允许频率范围内的最小分频比。
恢复时间由系统时钟源决定。

表 2.19 低功耗模式恢复时间 (4)

范围			象征	最小。	类型。	最大限度。	单元	测试条件
软件待机模式恢复时间*1	子振荡器速度模式	系统时钟源为 LOCO (32.768 kHz)	t_{SBYLO}	—	0.29	0.36	ms	图 2.11

注 1. 在 Subosc 速度模式下，LOCO 本身在软件待机模式下继续振荡。

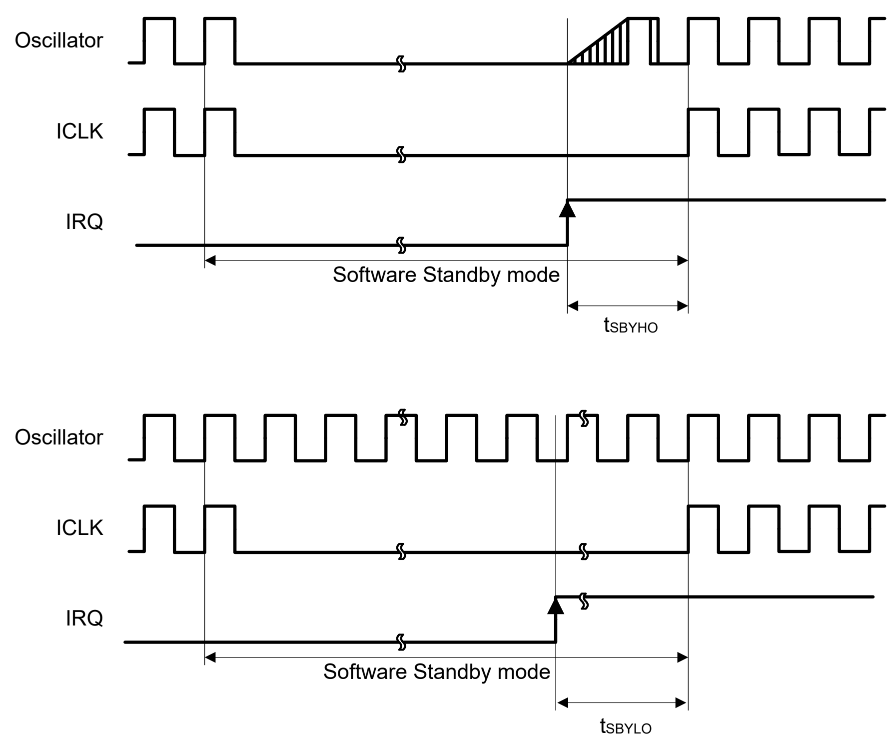


Figure 2.11 Software Standby mode cancellation timing

Table 2.20 Timing of recovery from low power modes (5)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	t_{SNZ}	—	5.3	5.7	μs	Figure 2.12
	Middle-speed mode System clock source is HOCO (16 MHz) VCC = 1.8 V to 5.5 V	t_{SNZ}	—	5.5	5.8	μs	
	Middle-speed mode System clock source is HOCO (4 MHz) VCC = 1.6 V to 1.8 V	t_{SNZ}	—	6.3	6.7	μs	
	Low-speed mode System clock source is HOCO (2 MHz)	t_{SNZ}	—	8.0	8.4	μs	

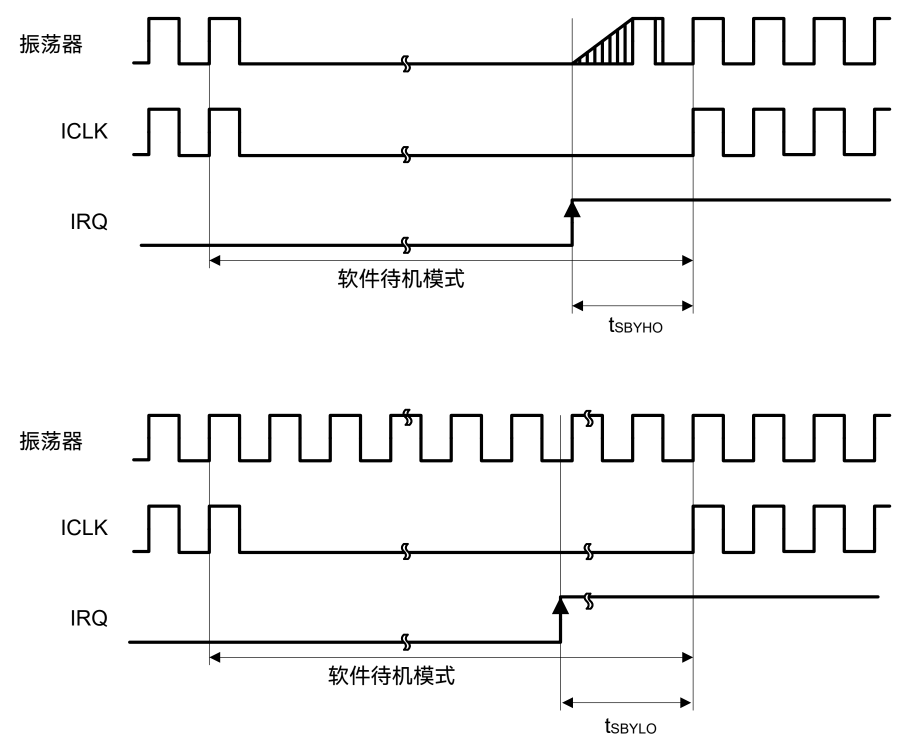
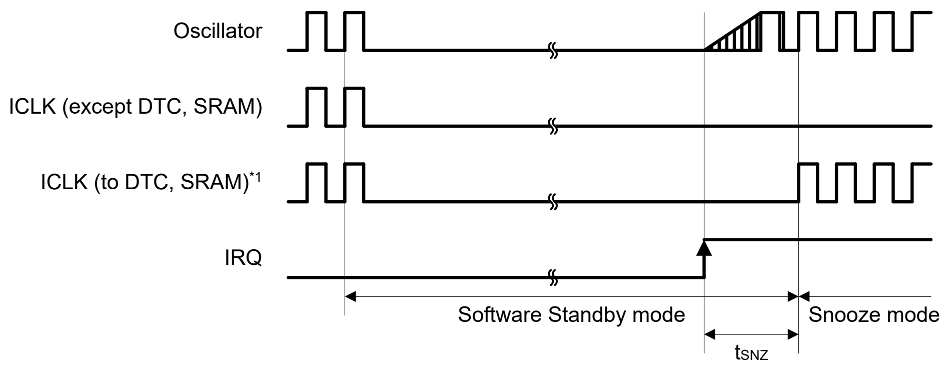


图 2.11 软件待机模式取消时序

表 2.20 低功耗模式恢复时间 (5)

范围		象征	最小。	类型。	最大限度。	单元	测试条件
恢复时间 软件待机模式 贪睡模式	高速模式系统时钟源为 HO CO	t_{SNZ}	—	5.3	5.7	μs	图 2.12
	中速模式 系统时钟源是 HOCO（16 MHz） VCC = 1.8 V to 5.5 V	t_{SNZ}	—	5.5	5.8	μs	
	中速模式 系统时钟源是 HOCO（4 MHz） VCC = 1.6 V to 1.8 V	t_{SNZ}	—	6.3	6.7	μs	
	低速模式 系统时钟源是 HOCO（2 MHz）	t_{SNZ}	—	8.0	8.4	μs	



Note 1. When SBYEDCR0.DTCED bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.12 Recovery timing from Software Standby mode to Snooze mode

2.5 Peripheral Function Characteristics

2.5.1 Serial Array Unit (SAU)

Table 2.21 In UART communications with devices operating at the same voltage levels

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter			Symbol	High-speed mode Min.	High-speed mode Max.	Middle-speed mode Min.	Middle-speed mode Max.	Low-speed mode Min.	Low-speed mode Max.	Unit	Test Conditions
Transfer rate*1	1.6 V ≤ VCC ≤ 5.5 V		—	—	f_{MCK}/6	—	f_{MCK}/6	—	f_{MCK}/6	bps	Figure 2.14
		Theoretical value of the maximum transfer rate f_{MCK} = PCLKB*2		—	5.3	—	4	—	0.33	Mbps	

Note 1. The transfer rate in SNOOZE mode is within the range from 4800 to 9600 bps when SBYCR.FWKUP = 0, and within the range from 4800 to 115200 bps when SBYCR.FWKUP = 1.

Note 2. The maximum operating frequencies of the peripheral module clock (PCLKB) are as follows.
High-speed mode: 32 MHz (1.8 V ≤ VCC ≤ 5.5 V), 4 MHz (1.6 V ≤ VCC ≤ 5.5 V)
Middle-speed mode: 16 MHz (1.8 V ≤ VCC ≤ 5.5 V), 4 MHz (1.6 V ≤ VCC ≤ 5.5 V)
Low-speed mode: 2 MHz (1.6 V ≤ VCC ≤ 5.5 V)

Note: Select the normal input buffer for the RXDq pin and the normal output mode for the TXDq pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

gh: Port number (gh = 100, 101, 109, 110, 200, 212, 213, 300)

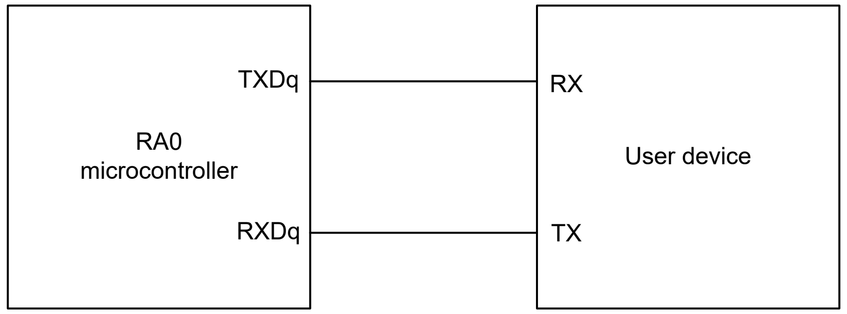
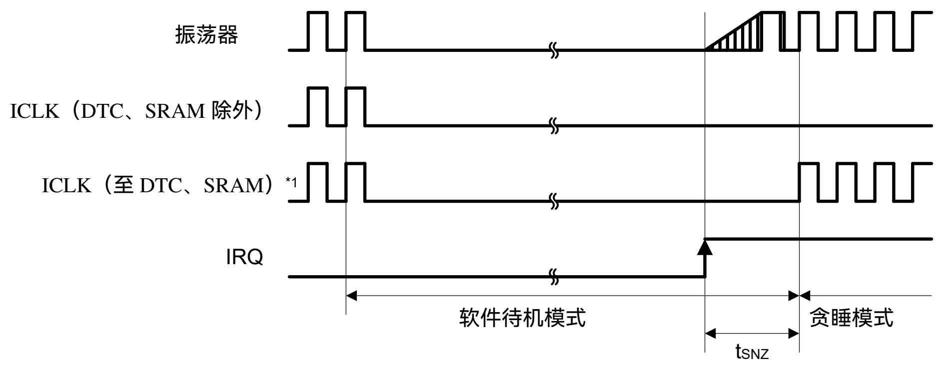


Figure 2.13 Connection in the UART communications with devices operating at the same voltage levels



注 1. 当 SBYEDCR0.DTCED 位设置为 1 时，ICLK 会提供给 DTC 和 SRAM。

图 2.12 从软件待机模式恢复到休眠模式的时序

2.5 外周功能特征

2.5.1串行阵列单元（SAU）

表 2.21 在与工作电压相同的设备进行 UART 通信时

条件：VCC = 1.6至5.5 V, VSS= 0 V,Ta= -40 至+125°C

范围			象征	高速模式 最小。	高速模式 最大限度。	中速模式 最小。	中速模式 最大限度。	低速模式 最小。	低速模式 最大限度。	单元	测试状况
转账费率*1	1.6 V ≤ VCC ≤ 5.5 V		—	—	f_{MCK}/6	—	f_{MCK}/6	—	f_{MCK}/6	bps	图 2.14
		最大传输速率的理论值 f MCK= PCLKB*2		—	5.3	—	4	—	0.33	兆比特	

注1. 当SBYCR.FWKUP= 0，时，SNOOZE模式下的传输速率在4800到9600 bps范围内；当SBYCR.FWKUP= 1时，SNOOZE模式下的传输速率在4800到115200 bps范围内。

注2. 外设模块时钟（PCLKB）的最大工作频率如下。
高速模式：32 MHz (1.8 V ≤ VCC ≤ 5.5 V)，4 MHz (1.6 V ≤ VCC ≤ 5.5 V) 中速模式：16MHz (1.8 V ≤ VCC ≤ 5.5 V)，4 MHz（1.6 V ≤ VCC ≤ 5.5 V）低速模式：2 MHz (1.6 V ≤ VCC ≤ 5.5 V)

注意：使用端口 gh 引脚功能选择寄存器（PghPFS_A.PIM 和 PghPFS_A.NCODR）为 RXDq 引脚选择正常输入缓冲器，为 TXDq 引脚选择正常输出模式。

gh：端口号(gh = 100, 101，109、110、200、212、213、300）

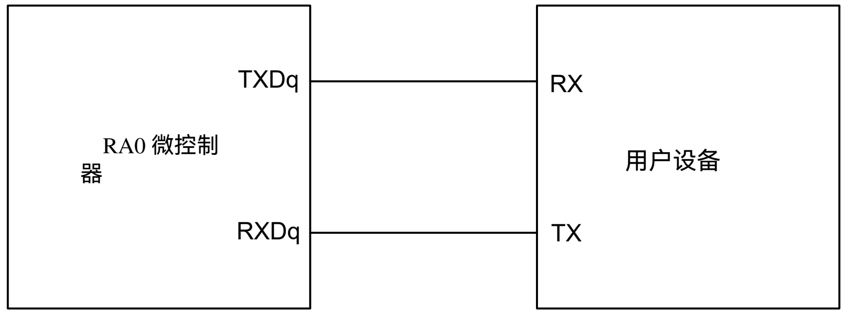


图 2.13 UART 通信中与工作电压相同的设备的连接

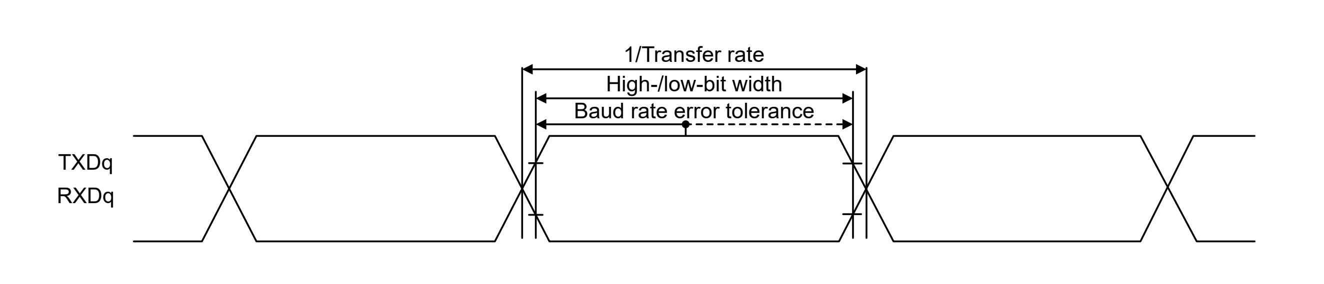


Figure 2.14 Bit width in the UART communications when interfacing devices operate at the same voltage level (reference)

Note:
- q: UART number (q = 0, 1), gh: Port number (gh = 100, 101, 109, 110, 200, 212, 213, 300)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, set the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 01, 02, 03)

Table 2.22 In simplified SPI communications in the master mode with devices operating at the same voltage levels with the internal SCKp clock (the ratings below are only applicable to SPI00)

Conditions: VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = -40 to +85℃

Parameter			Symbol	High-speed mode Min.	High-speed mode Max.	Middle-speed mode Min.	Middle-speed mode Max.	Low-speed mode Min.	Low-speed mode Max.	Unit	Test Conditions
SCKp cycle time	t_{KCY1} ≥ 2/ PCLKB	4.0 V ≤ VCC ≤ 5.5 V	t_{KCY1}	62.5	—	125	—	1000	—	ns	Figure 2.16 Figure 2.17
		2.7 V ≤ VCC ≤ 5.5 V		125	—	125	—	1000	—	ns	
SCKp high-/low-level width	4.0 V ≤ VCC ≤ 5.5 V		t_{KH1}, t_{KL1}	t_{KCY1}/2 - 7	—	t_{KCY1}/2 - 10	—	t_{KCY1}/2 - 50	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			t_{KCY1}/2 - 10	—	t_{KCY1}/2 - 15	—	t_{KCY1}/2 - 50	—	ns	
SIp setup time (to SCKp↑)*1	4.0 V ≤ VCC ≤ 5.5 V		t_{SIK1}	23	—	33	—	110	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			33	—	50	—	110	—	ns	
SIp hold time (from SCKp↑)*1	2.7 V ≤ VCC ≤ 5.5 V		t_{KSI1}	10	—	10	—	10	—	ns	
Delay time from SCKp↓ to SOp output*2	C = 20 pF*3		t_{KSO1}	—	10	—	10	—	10	ns	

Note 1. The setting applies when SCRmn.DCP0[1:0] = 00b or 11b. The setting for the SIp setup time becomes to SCKp↓ and that for the SIp hold time becomes from SCKp↓ when SCRmn.DCP0[1:0] = 01b or 10b.
Note 2. This setting applies when SCRmn.DCP0[1:0] = 00b or 11b. The setting for the delay time to SOp output becomes from SCKp↑ when SCRmn.DCP0[1:0] = 01b or 10b.
Note 3. C is the load capacitance of the SCKp and SOp output lines.

Note: Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

Note:
- The listed times are only valid when the peripheral I/O redirect function of SPI00 is not in use.
- p: Simplified SPI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), gh: Port number (gh = 100 to 102, 108 to 110, 112, 200)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00)

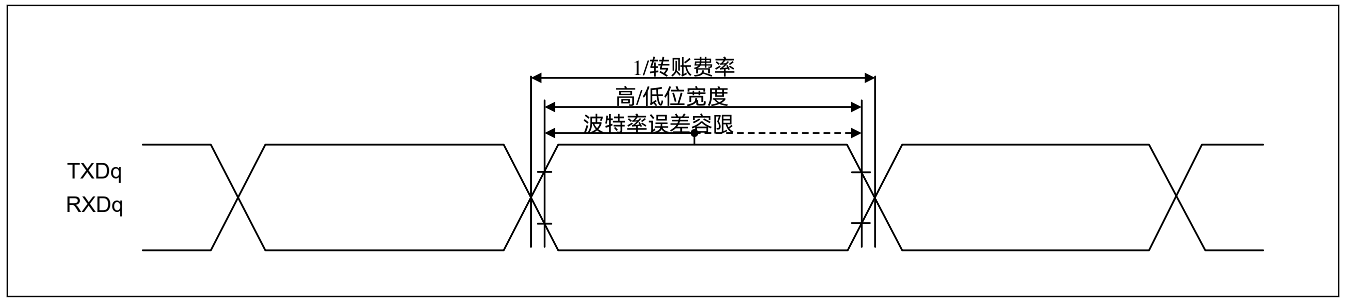


图 2.14 当接口设备工作在相同电压电平（参考）时，UART 通信中的位宽

注：●q：UART 号(q = 0, 1)，gh：端口号(gh = 100, 101，109、110、200、212、213、300)
●fMCK：串行阵列单元操作时钟频率
要设置此工作时钟，请设置串行模式寄存器 mn (SMRmn) 中的 CKS 位。
m：单元编号，n：通道编号(mn = 00, 01, 02, 03)

表 2.22 在主模式下，简化的 SPI 通信中，设备在与内部 SCKp 时钟相同的电压电平下工作（以下额定值仅适用于 SPI00）

条件：VCC = 2.7至 5.5 V，VSS= 0 V，Ta= -40 至+85℃

范围			象征	高速模式 最小。	高速模式 最大限度。	中速模式 最小。	中速模式 最大限度。	低速模式 最小。	低速模式 最大限度。	单元	测试状况
SCKp 循环时间	t_{KCY1} ≥ 2/ PCLKB	4.0 V ≤ VCC ≤ 5.5 V	t_{KCY1}	62.5	—	125	—	1000	—	ns	图 2.16 图 2.17
		2.7 V ≤ VCC ≤ 5.5 V		125	—	125	—	1000	—	ns	
SCKp 高/低电平宽度	4.0 V ≤ VCC ≤ 5.5 V		t_{KH1}, t_{KL1}	t_{KCY1}/2 - 7	—	t_{KCY1}/2 - 10	—	t_{KCY1}/2 - 50	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			t_{KCY1}/2 - 10	—	t_{KCY1}/2 - 15	—	t_{KCY1}/2 - 50	—	ns	
SIp 建立时间（到 SCKp↑）*1	4.0 V ≤ VCC ≤ 5.5 V		t_{SIK1}	23	—	33	—	110	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			33	—	50	—	110	—	ns	
SIp 保持时间（来自SCKp↑)*1	2.7 V ≤ VCC ≤ 5.5 V		t_{KSI1}	10	—	10	—	10	—	ns	
从 SCKp↓ 到SOp输出的延迟时间*2	C = 20 pF*3		t_{KSO1}	—	10	—	10	—	10	ns	

注 1. 当SCRmn.DCP0[1:0] = 00b 或 11b 时，此设置适用。SIp 建立时间的设置变为SCKp↓，SIp 保持时间的设置变为当 SCRmn.DCP0[1:0] = 01b 或 10b 时，SCKp↓ 。
注 2. 此设置适用于 SCRmn.DCP0[1:0] = 00b或 11b。当SCRmn.DCP0[1:0] = 01b 或 10b 时，延迟时间到SOp输出的设置将变为SCKp↑ 。

注3. C 是SCKp和SOp输出线的负载电容。

注意：使用端口 gh 引脚功能选择寄存器（PghPFS_A.PIM 和 PghPFS_A.NCODR）为SIp引脚选择正常输入缓冲模式，为SOp引脚和 SCKp 引脚选择正常输出模式。

注意：●所列时间仅在未使用外设SPI00重定向功能时有效。
●p：简化的 SPI 编号(p = 00)，m：单元编号(m = 0)，n：通道编号(n = 0)，gh：端口编号(gh =（100 至 102、108 至 110、112、200)
●fMCK：串行阵列单元操作时钟频率
要设置此工作时钟，请使用串行模式寄存器 mn (SMRmn) 中的 CKS 位。
m：单元编号，n：通道编号(mn = 00)

Table 2.23 In simplified SPI communications in the master mode with devices operating at the same voltage levels with the internal SCKp clock

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	t_{KCY1} ≥ 4/ PCLKB	2.7 V ≤ VCC ≤ 5.5 V	t_{KCY1}	125	—	166	—	2000	—	ns	Figure 2.16 Figure 2.17
		2.4 V ≤ VCC ≤ 5.5 V		250	—	250	—	2000	—	ns	
		1.8 V ≤ VCC ≤ 5.5 V		500	—	500	—	2000	—	ns	
		1.6 V ≤ VCC ≤ 5.5 V		1000	—	1000	—	2000	—	ns	
SCKp high-/low-level width	4.0 V ≤ VCC ≤ 5.5 V		t_{KH1}, t_{KL1}	t_{KCY1}/2 - 12	—	t_{KCY1}/2 - 21	—	t_{KCY1}/2 - 50	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			t_{KCY1}/2 - 18	—	t_{KCY1}/2 - 25	—	t_{KCY1}/2 - 50	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			t_{KCY1}/2 - 38	—	t_{KCY1}/2 - 38	—	t_{KCY1}/2 - 50	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			t_{KCY1}/2 - 50	—	t_{KCY1}/2 - 50	—	t_{KCY1}/2 - 50	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			t_{KCY1}/2 - 100	—	t_{KCY1}/2 - 100	—	t_{KCY1}/2 - 100	—	ns	
SIp setup time (to SCKp↑)*1	4.0 V ≤ VCC ≤ 5.5 V		t_{SIK1}	44	—	54	—	110	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			44	—	54	—	110	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			75	—	75	—	110	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			110	—	110	—	110	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			220	—	220	—	220	—	ns	
SIp hold time (from SCKp↑)*1	1.6 V ≤ VCC ≤ 5.5 V		t_{KSI1}	19	—	19	—	19	—	ns	
Delay time from SCKp↓ to SOp output*2	1.6 V ≤ VCC ≤ 5.5 V C = 30 pF*3		t_{KSO1}	—	25	—	25	—	25	ns	

Note 1. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the SIp setup time becomes to SCKp↓ and that for the SIp hold time becomes from SCKp↓ when SCRmn.DCP[1:0] = 01b or 10b.

Note 2. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the delay time to SOp output becomes from SCKp↑ when SCRmn.DCP[1:0] = 01b or 10b.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Note: Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

Note:
- p: Simplified SPI number (p = 00, 11), m: Unit number (m = 0), n: Channel number (n = 0, 3), gh: Port number (gh = 100 to 102, 108 to 110, 112, 200, 201, 212, 213)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03)

表 2.23 简化的主模式下 SPI 通信，设备工作电压电平相同，并使用内部 SCKp 时钟。

条件：VCC= 1.6至 5.5 V，VSS= 0 V,Ta= -40至+125°C

范围			象征	高速模式		中速模式		低速模式		单元	测试状况
				最小。	最大限度。	最小。	最大限度。	最小。	最大限度。		
SCKp 循环时间	t_{KCY1} ≥ 4/ PCLKB	2.7 V ≤ VCC ≤ 5.5 V	t_{KCY1}	125	—	166	—	2000	—	ns	图 2.16 图 2.17
		2.4 V ≤ VCC ≤ 5.5 V		250	—	250	—	2000	—	ns	
		1.8 V ≤ VCC ≤ 5.5 V		500	—	500	—	2000	—	ns	
		1.6 V ≤ VCC ≤ 5.5 V		1000	—	1000	—	2000	—	ns	
SCKp 高/低水平宽度	4.0 V ≤ VCC ≤ 5.5 V		t_{KH1}, t_{KL1}	t_{KCY1}/2 - 12	—	t_{KCY1}/2 - 21	—	t_{KCY1}/2 - 50	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			t_{KCY1}/2 - 18	—	t_{KCY1}/2 - 25	—	t_{KCY1}/2 - 50	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			t_{KCY1}/2 - 38	—	t_{KCY1}/2 - 38	—	t_{KCY1}/2 - 50	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			t_{KCY1}/2 - 50	—	t_{KCY1}/2 - 50	—	t_{KCY1}/2 - 50	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			t_{KCY1}/2 - 100	—	t_{KCY1}/2 - 100	—	t_{KCY1}/2 - 100	—	ns	
SIP 设置时间（至 SCKp↑）*1	4.0 V ≤ VCC ≤ 5.5 V		t_{SIK1}	44	—	54	—	110	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			44	—	54	—	110	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			75	—	75	—	110	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			110	—	110	—	110	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			220	—	220	—	220	—	ns	
SIp 保持时间（来自 SCKp↑）*1	1.6 V ≤ VCC ≤ 5.5 V		t_{KSI1}	19	—	19	—	19	—	ns	
从SCKp↓到 SOp 输出的延迟时间*2	1.6 V ≤ VCC ≤ 5.5 V C = 30 pF*3		t_{KSO1}	—	25	—	25	—	25	ns	

注 1. 此设置适用于 SCRmn.DCP[1:0] = 00b 或 11b。当 SCRmn.DCP[1:0] = 01b 或 10b 时，SIp设置时间变为SCKp↓，SIp 保持时间变为SCKp↓ 。

注 2. 此设置适用于 SCRmn.DCP[1:0] = 00b 或 11b。当SCRmn.DCP[1:0] = 01b 或10b时，延迟到SOp输出的设置将变为SCKp↑。

注3. C 是SCKp和SOp输出线的负载电容。

注意：使用端口 gh 引脚功能选择寄存器（PghPFS_A.PIM 和 PghPFS_A.NCODR）为SIp引脚选择正常输入缓冲模式，为SOp引脚和 SCKp 引脚选择正常输出模式。

注：●p：简化的 SPI 编号(p = 00，11），m：单元编号(m = 0)，n：通道编号(n = 0, 3)，gh：端口编号(gh = 100至 102、108 至 110、112、200、201、212、213）

●fMCK：串行阵列单元操作时钟频率
要设置此工作时钟，请使用串行模式寄存器 mn (SMRmn) 中的 CKS 位。
m：单元号，n：通道号(mn = 00，03) ●fMCK：

Table 2.24　In simplified SPI communications in the slave mode with devices operating at the same voltage levels with the SCKp external clock

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Item	Conditions		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time[*4]	4.0 V ≤ VCC ≤ 5.5 V	20 MHz < f_{MCK}	t_{KCY2}	$8/f_{MCK}$	—	$8/f_{MCK}$	—	—	—	ns	Figure 2.16 Figure 2.17
		f_{MCK} ≤ 20 MHz		$6/f_{MCK}$	—	$6/f_{MCK}$	—	$6/f_{MCK}$	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V	16 MHz < f_{MCK}		$8/f_{MCK}$	—	$8/f_{MCK}$	—	—	—	ns	
		f_{MCK} ≤ 16 MHz		$6/f_{MCK}$	—	$6/f_{MCK}$	—	$6/f_{MCK}$	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			Greater of: $6/f_{MCK}$ or 500	—	Greater of: $6/f_{MCK}$ or 500	—	Greater of: $6/f_{MCK}$ or 500	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			Greater of: $6/f_{MCK}$ or 750	—	Greater of: $6/f_{MCK}$ or 750	—	Greater of: $6/f_{MCK}$ or 750	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			Greater of: $6/f_{MCK}$ or 1500	—	Greater of: $6/f_{MCK}$ or 1500	—	Greater of: $6/f_{MCK}$ or 1500	—	ns	
SCKp high-/low-level width	4.0 V ≤ VCC ≤ 5.5 V		t_{KH2}, t_{KL2}	$t_{KCY2}/2 - 7$	—	$t_{KCY2}/2 - 7$	—	$t_{KCY2}/2 - 7$	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			$t_{KCY2}/2 - 8$	—	$t_{KCY2}/2 - 8$	—	$t_{KCY2}/2 - 8$	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			$t_{KCY2}/2 - 18$	—	$t_{KCY2}/2 - 18$	—	$t_{KCY2}/2 - 18$	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$t_{KCY2}/2 - 66$	—	$t_{KCY2}/2 - 66$	—	$t_{KCY2}/2 - 66$	—	ns	
SIp setup time (to SCKp↑)[*1]	2.7 V ≤ VCC ≤ 5.5 V		t_{SIK2}	$1/f_{MCK} + 20$	—	$1/f_{MCK} + 30$	—	$1/f_{MCK} + 30$	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			$1/f_{MCK} + 30$	—	$1/f_{MCK} + 30$	—	$1/f_{MCK} + 30$	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$1/f_{MCK} + 40$	—	$1/f_{MCK} + 40$	—	$1/f_{MCK} + 40$	—	ns	
SIp hold time (from SCKp↑)[*1]	1.8 V ≤ VCC ≤ 5.5 V		t_{KSI2}	$1/f_{MCK} + 31$	—	$1/f_{MCK} + 31$	—	$1/f_{MCK} + 31$	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$1/f_{MCK} + 250$	—	$1/f_{MCK} + 250$	—	$1/f_{MCK} + 250$	—	ns	
Delay time from SCKp↓ to SOp output[*2]	C = 30 pF[*3]	2.7 V ≤ VCC ≤ 5.5 V	t_{KSO2}	—	$2/f_{MCK} + 44$	—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	ns	
		2.4 V ≤ VCC ≤ 5.5 V		—	$2/f_{MCK} + 75$	—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	ns	
		1.8 V ≤ VCC ≤ 5.5 V		—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	ns	
		1.6 V ≤ VCC ≤ 5.5 V		—	$2/f_{MCK} + 220$	—	$2/f_{MCK} + 220$	—	$2/f_{MCK} + 220$	ns	

Note 1. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the SIp setup time becomes to SCKp↓ and that for the SIp hold time becomes from SCKp↓ when SCRmn.DCP[1:0] = 01b or 10b.
Note 2. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the delay time to SOp output becomes from SCKp↑ when SCRmn.DCP[1:0] = 01b or 10b.
Note 3. C is the load capacitance of the SOp output line.
Note 4. Transfer rate in the Snooze mode is 1 Mbps at the maximum.

Note: Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

Note:
- p: Simplified SPI number (p = 00, 11), m: Unit number (m = 0, 1), n: Channel number (n = 0, 3), gh: Port number (gh = 100 to 102, 108 to 110, 112, 200, 201, 212, 213)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03)

表 2.24 简化了从模式下的 SPI 通信，其中设备在与外部时钟 SCKp 相同的电压电平下工作。

条件：VCC= 1.6至 5.5 V，VSS= 0 V,Ta= -40至+125°C

物品	状况		象征	高速模式		中速模式		低速模式		单元	测试状况
				最小。	最大限度。	最小。	最大限度。	最小。	最大限度。		
SCKp 循环时间*4	4.0 V ≤ VCC ≤ 5.5 V	20 MHz < f_{MCK}	t_{KCY2}	$8/f_{MCK}$	—	$8/f_{MCK}$	—	—	—	ns	图 2.16 图 2.17
		f_{MCK} ≤ 20 MHz		$6/f_{MCK}$	—	$6/f_{MCK}$	—	$6/f_{MCK}$	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V	16 MHz < f_{MCK}		$8/f_{MCK}$	—	$8/f_{MCK}$	—	—	—	ns	
		f_{MCK} ≤ 16 MHz		$6/f_{MCK}$	—	$6/f_{MCK}$	—	$6/f_{MCK}$	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			以下两者中的较大值：$6/f_{MCK}$ or 500		取较大值：6/ fMCK 或 500	—	取较大值：6/ f_{MCK} or 500	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			以下两者中的较大值：6/fMCK 或 750		以下两者中的较大值：6/ fMCK 或 750		以下两者中的较大值：6/ fMCK 或 750		ns	
	1.6 V ≤ VCC ≤ 5.5 V			以下两者中的较大值：6/fMCK 或 1500		以下两者中的较大值：6/ fMCK 或 1500		以下两者中的较大值：6/ fMCK 或 1500		ns	
SCKp 高/低电平宽度	4.0 V ≤ VCC ≤ 5.5 V		tKH2, t_{KL2}	$t_{KCY2}/2 - 7$	—	$t_{KCY2}/2 - 7$	—	$t_{KCY2}/2 - 7$	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			$t_{KCY2}/2 - 8$	—	$t_{KCY2}/2 - 8$	—	$t_{KCY2}/2 - 8$	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			$t_{KCY2}/2 - 18$	—	$t_{KCY2}/2 - 18$	—	$t_{KCY2}/2 - 18$	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$t_{KCY2}/2 - 66$	—	$t_{KCY2}/2 - 66$	—	$t_{KCY2}/2 - 66$	—	ns	
SIP 设置时间（至 SCKp↑）*1	2.7 V ≤ VCC ≤ 5.5 V		t_{SIK2}	$1/f_{MCK} + 20$	—	$1/f_{MCK} + 30$	—	$1/f_{MCK} + 30$	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			$1/f_{MCK} + 30$	—	$1/f_{MCK} + 30$	—	$1/f_{MCK} + 30$	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$1/f_{MCK} + 40$	—	$1/f_{MCK} + 40$	—	$1/f_{MCK} + 40$	—	ns	
啜饮保持时间（来自SCKp↑)[*1]	1.8 V ≤ VCC ≤ 5.5 V		t_{KSI2}	$1/f_{MCK} + 31$	—	$1/f_{MCK} + 31$	—	$1/f_{MCK} + 31$	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$1/f_{MCK} + 250$	—	$1/f_{MCK} + 250$	—	$1/f_{MCK} + 250$	—	ns	
从 SCKp↓ 到 SOp 输出的延迟时间*2	C = 30 pF[*3]	2.7 V ≤ VCC ≤ 5.5 V	t_{KSO2}	—	$2/f_{MCK} + 44$	—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	ns	
		2.4 V ≤ VCC ≤ 5.5 V		—	$2/f_{MCK} + 75$	—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	ns	
		1.8 V ≤ VCC ≤ 5.5 V		—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	ns	
		1.6 V ≤ VCC ≤ 5.5 V		—	$2/f_{MCK} + 220$	—	$2/f_{MCK} + 220$	—	$2/f_{MCK} + 220$	ns	

注 1. 此设置适用于 SCRmn.DCP[1:0] = 00b 或 11b。当 SCRmn.DCP[1:0] = 01b 或 10b 时，SIp设置时间变为SCKp↓，SIp 保持时间变为SCKp↓。

注 2. 此设置适用于 SCRmn.DCP[1:0] = 00b 或 11b。当SCRmn.DCP[1:0] = 01b 或 10b 时，延迟到SOp输出的设置将来自 SCKp↑。

注3. C是SOp 输出线的负载电容。
注 4. 休眠模式下的最大传输速率为 1 Mbps。

注意：使用端口 gh 引脚功能选择寄存器（PghPFS_A.PIM 和 PghPFS_A.NCODR）为 SIp 引脚和SCKp引脚选择正常输入缓冲模式，为 Sop 引脚选择正常输出模式。

注：●p：简化的SPI编号(p = 00，11），m：单元编号(m = 0，1），n：通道编号(n = 0, 3）gh：端口编号(gh = 100至102、108至110、112、200、201、212、213）

串行阵列单元操作时钟频率
要设置此工作时钟，请使用串行模式寄存器 mn (SMRmn) 中的 CKS 位。
m：单元编号，n：通道编号(mn = 00，03）

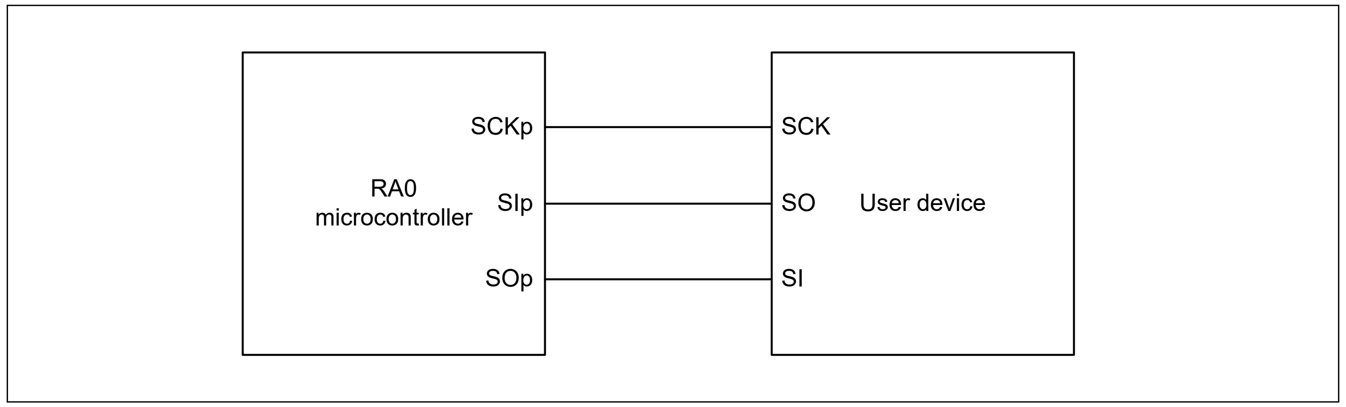


Figure 2.15 Connection in the simplified SPI communications with devices operating at the same voltage levels

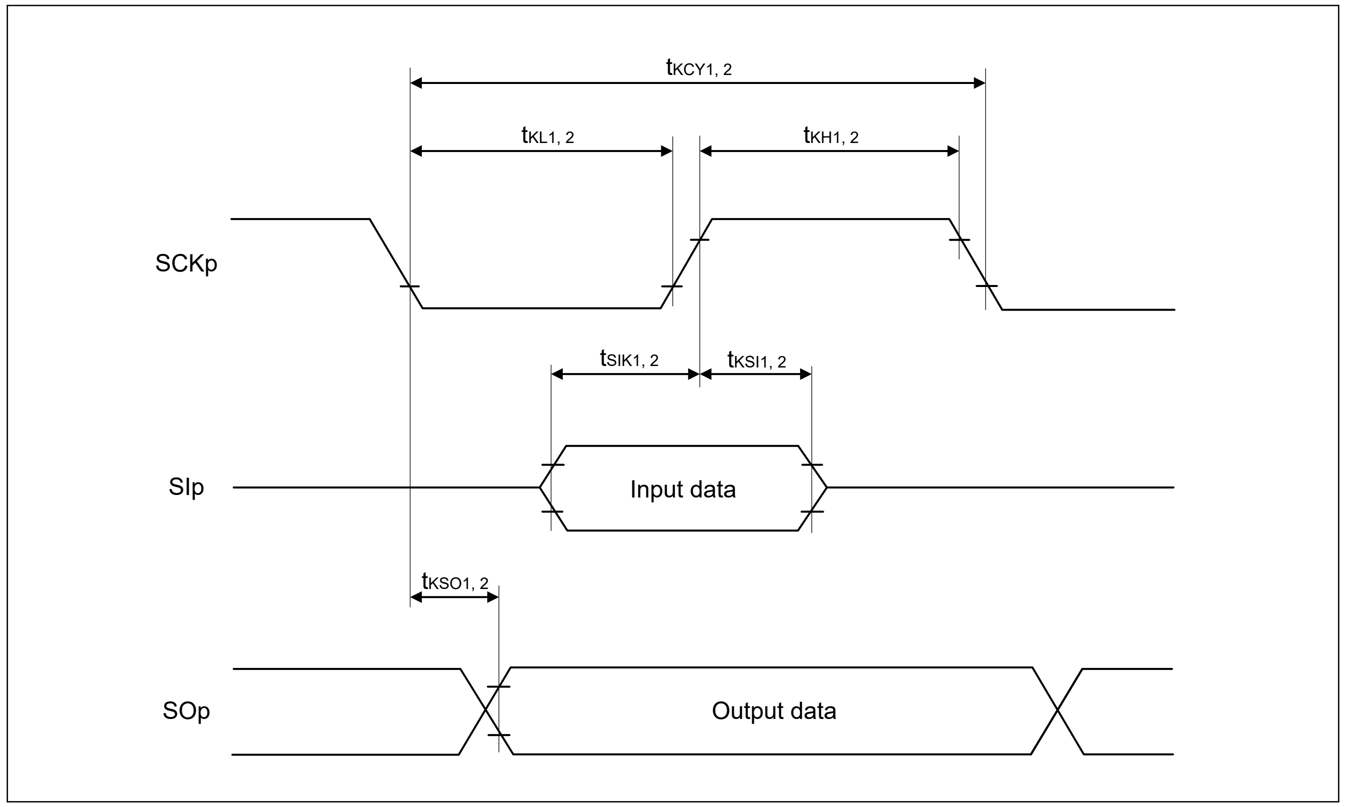


Figure 2.16 Timing of serial transfer in the simplified SPI communications with devices operating at the same voltage levels when SCRmn.DCP[1:0] = 00b or 11b

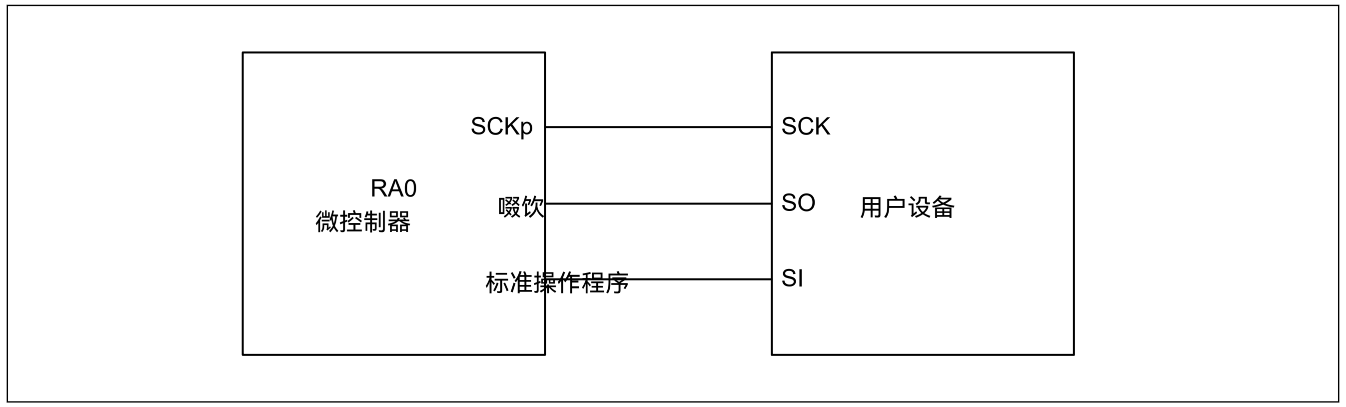


Figure 2.15 简化的SPI通信连接，适用于工作电压相同的设备。

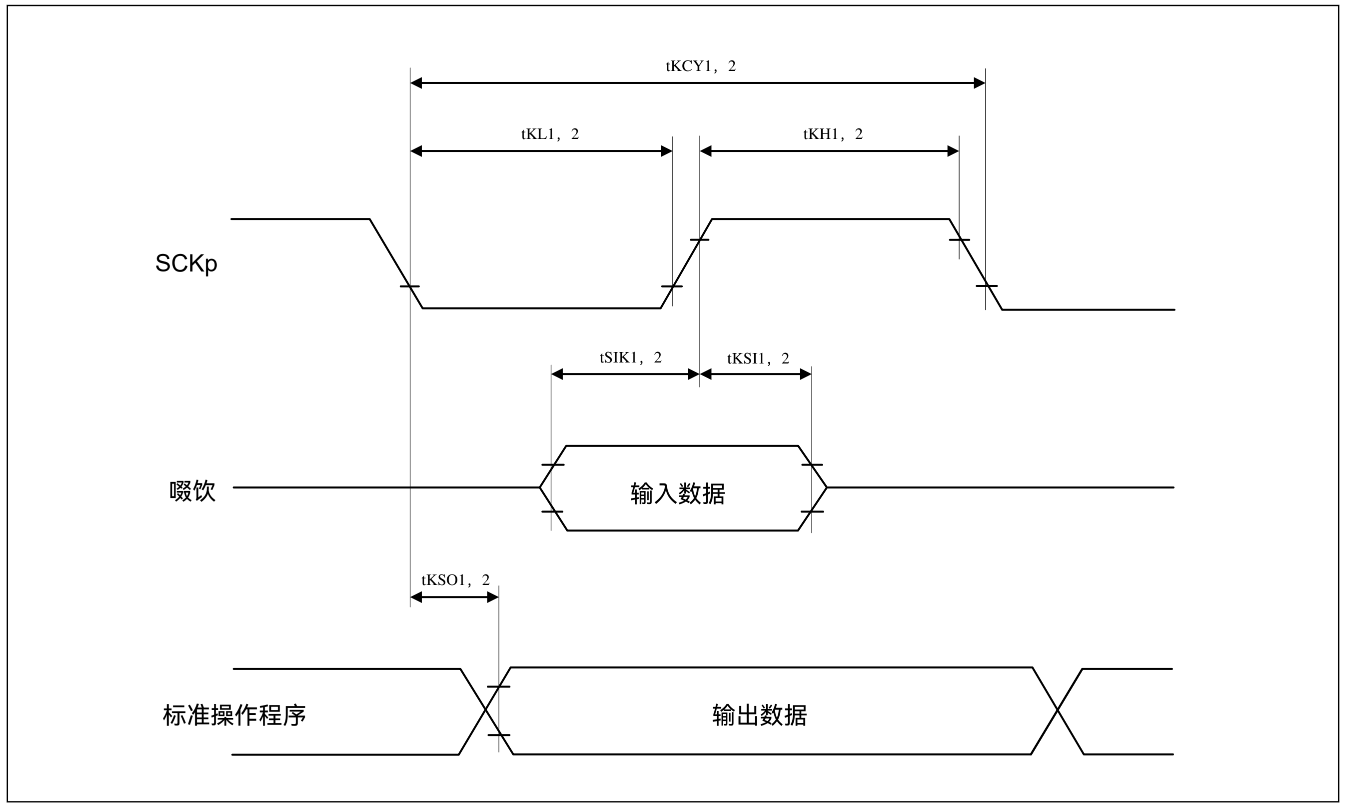


图 2.16 简化 SPI 通信中串行传输的时序，当 SCRmn.DCP[1:0] = 00b 或 11b 时，工作电压相同的设备。

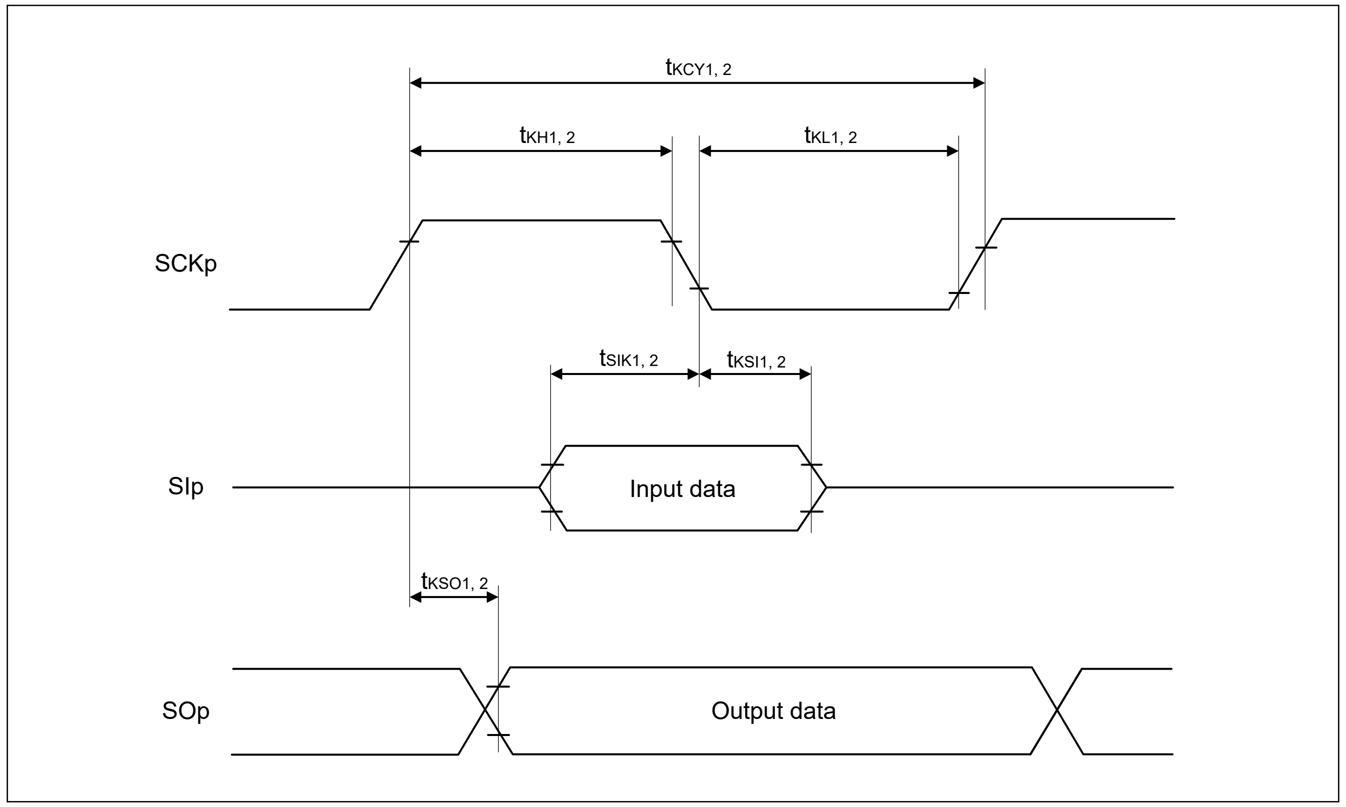


Figure 2.17 Timing of serial transfer in the simplified SPI communications with devices operating at the same voltage levels when SCRmn.DCP[1:0] = 01b or 10b

Note:
- p: Simplified SPI number (p = 00, 11)
- m: Unit number, n: Channel number (mn = 00, 03)

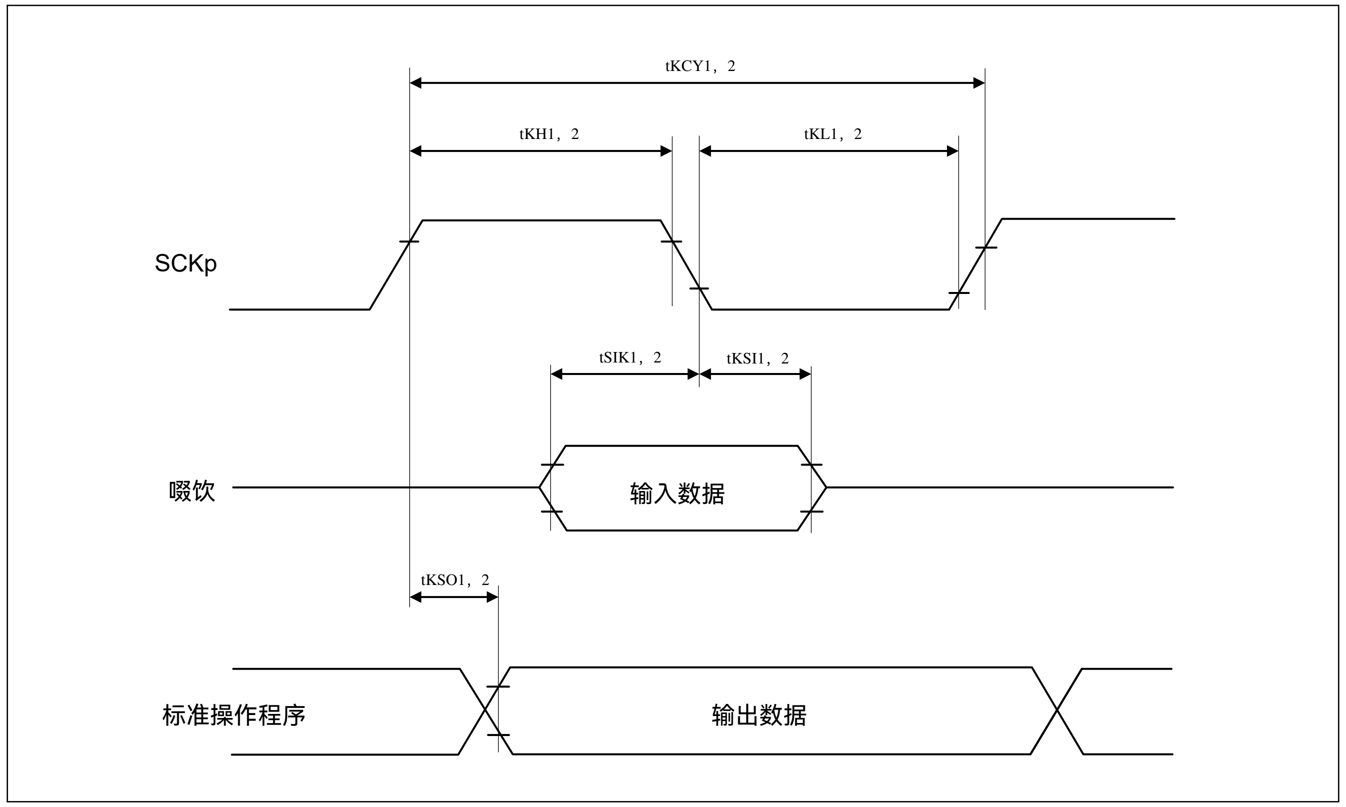


图 2.17 简化 SPI 通信中串行传输的时序，当 SCRmn.DCP[1:0] = 01b 或 10b 时，工作电压相同的设备。

注：●p：简化的 SPI 编号(p = 00，11)
●m：单元编号，n：通道编号(mn = 00，03)

Table 2.25 In simplified IIC communications with devices operating at the same voltage levels (1 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
SCLr clock frequency	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	f_{SCL}	—	1000*1	—	1000*1	—	400*1	kHz	Figure 2.19
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		—	400*1	—	400*1	—	400*1	kHz	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		—	300*1	—	300*1	—	300*1	kHz	
	1.6 V ≤ VCC < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		—	250*1	—	250*1	—	250*1	kHz	
Hold time when SCLr is low	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	t_{LOW}	475	—	475	—	1150	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		1150	—	1150	—	1150	—	ns	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		1550	—	1550	—	1550	—	ns	
	1.6 V ≤ VCC < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		1850	—	1850	—	1850	—	ns	
Hold time when SCLr is high	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	t_{HIGH}	475	—	475	—	1150	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		1150	—	1150	—	1150	—	ns	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		1550	—	1550	—	1550	—	ns	
	1.6 V ≤ VCC < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		1850	—	1850	—	1850	—	ns	

表 2.25 简化的 IIC 通信，适用于工作电压相同的设备（1/2）

条件：VCC = 1.6至5.5 V, VSS= 0 V, Ta= -40 至+125°C

范围		象征	高速模式		中速模式		低速模式		单元	测试状况
			最小。	最大限度	最小。	最大限度	最小。	最大限度		
SCLr 时钟频率	2.7 V ≤ VCC ≤ 5.5 V, Cb= 50 pF, Rb= 2.7 kΩ	f_{SCL}	—	1000*1	—	1000*1	—	400*1	kHz	图 2.19
	1.8 V ≤ VCC ≤ 5.5 V, Cb= 100 pF, Rb= 3 kΩ		—	400*1	—	400*1	—	400*1	kHz	
	1.8 V ≤ VCC < 2.7 V, C_b = 100pF, R_b = 5 kΩ		—	300*1	—	300*1	—	300*1	kHz	
	1.6 V ≤ VCC < 1.8 V, Cb= 100 pF, Rb= 5 kΩ		—	250*1	—	250*1	—	250*1	kHz	
保持时间 SCLr 低	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50pF, R_b = 2.7 kΩ	低	475	—	475	—	1150	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100pF, R_b = 3 kΩ		1150	—	1150	—	1150	—	ns	
	1.8 V ≤ VCC < 2.7 V, Cb= 100 pF, Rb= 5 kΩ		1550	—	1550	—	1550	—	ns	
	1.6 V ≤ VCC < 1.8 V, Cb= 100 pF, Rb= 5 kΩ		1850	—	1850	—	1850	—	ns	
保持时间 SCLr 值高	2.7 V ≤ VCC ≤ 5.5 V, Cb= 50 pF, R_b = 2.7 kΩ	大腿	475	—	475	—	1150	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V, Cb= 100 pF, Rb= 3 kΩ		1150	—	1150	—	1150	—	ns	
	1.8 V ≤ VCC < 2.7 V, Cb= 100 pF, Rb= 5 kΩ		1550	—	1550	—	1550	—	ns	
	1.6 V ≤ VCC < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		1850	—	1850	—	1850	—	ns	

Table 2.25 In simplified IIC communications with devices operating at the same voltage levels (2 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
Data setup time (reception)	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	$t_{SU:DAT}$	$1/f_{MCK}$ + 85*2	—	$1/f_{MCK}$ + 85*2	—	$1/f_{MCK}$ + 145*2	—	ns	Figure 2.19
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		$1/f_{MCK}$ + 145*2	—	$1/f_{MCK}$ + 145*2	—	$1/f_{MCK}$ + 145*2	—	ns	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		$1/f_{MCK}$ + 230*2	—	$1/f_{MCK}$ + 230*2	—	$1/f_{MCK}$ + 230*2	—	ns	
	1.6 V ≤ VCC < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		$1/f_{MCK}$ + 290*2	—	$1/f_{MCK}$ + 290*2	—	$1/f_{MCK}$ + 290*2	—	ns	
Data hold time (transmission)	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	$t_{HD:DAT}$	0	305	0	305	0	305	ns	
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		0	355	0	355	0	355	ns	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		0	405	0	405	0	405	ns	
	1.6 V ≤ VCC < 1.8 V, C_b= 100 pF, R_b = 5 kΩ		0	405	0	405	0	405	ns	

Note 1. The listed times must be no greater than $f_{MCK}/4$.

Note 2. Set f_{MCK} so that it does not exceed the hold time when SCLr is low or high.

Note: Select the normal input buffer and the N-ch open drain output [withstand voltage of VCC] mode for the SDAr pin and the normal output mode for the SCLr pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

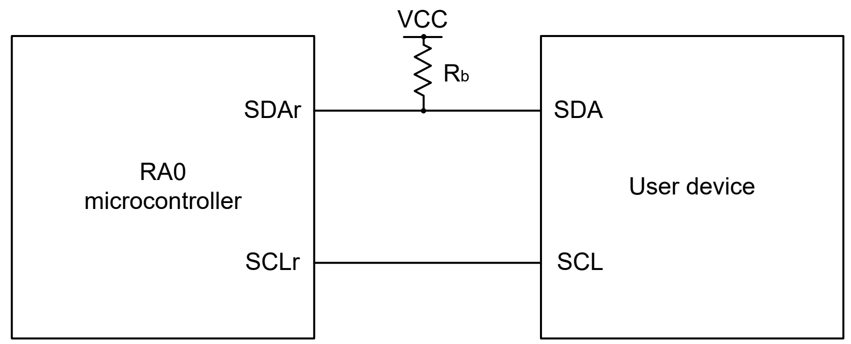


Figure 2.18 Connection in the simplified IIC communications with devices operating at the same voltage levels

表 2.25 简化的 IIC 通信，适用于工作电压相同的设备（2/2）

条件：VCC = 1.6至5.5 V, VSS= 0 V, Ta= -40 至+125°C

范围		象征	高速模式		中速模式		低速模式		单元	测试状况
			最小。	最大限	最小。	最大限	最小。	最大限		
数据建立时间（接收）	2.7 V ≤ VCC ≤ 5.5 V, Cb= 50 pF, Rb= 2.7 kΩ	TSU:DAT	$1/f_{MCK}$ + 85*2	度。	$1/f_{MCK}$ + 85*2	度。	$1/f_{MCK}$ + 145*2	度。	ns	图 2.19
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		$1/f_{MCK}$ + 145*2	—	$1/f_{MCK}$ + 145*2	—	$1/f_{MCK}$ + 145*2	—	ns	
	1.8 V ≤ VCC < 2.7 V, C_b = 100pF, R_b = 5 kΩ		$1/f_{MCK}$ + 230*2	—	$1/f_{MCK}$ + 230*2	—	$1/f_{MCK}$ + 230*2	—	ns	
	1.6 V ≤ VCC < 1.8 V, Cb= 100 pF, Rb= 5 kΩ		$1/f_{MCK}$ + 290*2	—	$1/f_{MCK}$ + 290*2	—	$1/f_{MCK}$ + 290*2	—	ns	
数据保持时间（传输）	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50pF, R_b = 2.7 kΩ	$t_{HD:DAT}$	0	305	0	305	0	305	ns	
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100pF, R_b = 3 kΩ		0	355	0	355	0	355	ns	
	1.8 V ≤ VCC < 2.7 V, Cb= 100 pF, Rb= 5 kΩ		0	405	0	405	0	405	ns	
	1.6 V ≤ VCC < 1.8 V, C_b= 100 pF, Rb= 5 kΩ		0	405	0	405	0	405	ns	

注1. 所列时间不得大于$f_{MCK}/4$.

注 2. 设置f_{MCK}，使其在 SCLr 为低或高时不超过保持时间。

注意：使用端口 gh 引脚功能选择寄存器（PghPFS_A.PIM 和 PghPFS_A.NCODR）为 SDAr 引脚选择正常输入缓冲器和 N 通道开漏输出[耐压 VCC] 模式，为 SCLr 引脚选择正常输出模式。

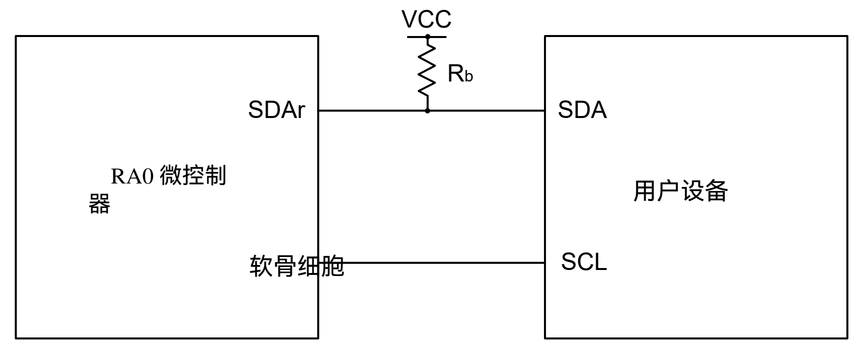


图 2.18 简化的 IIC 通信中与工作电压相同的设备的连接

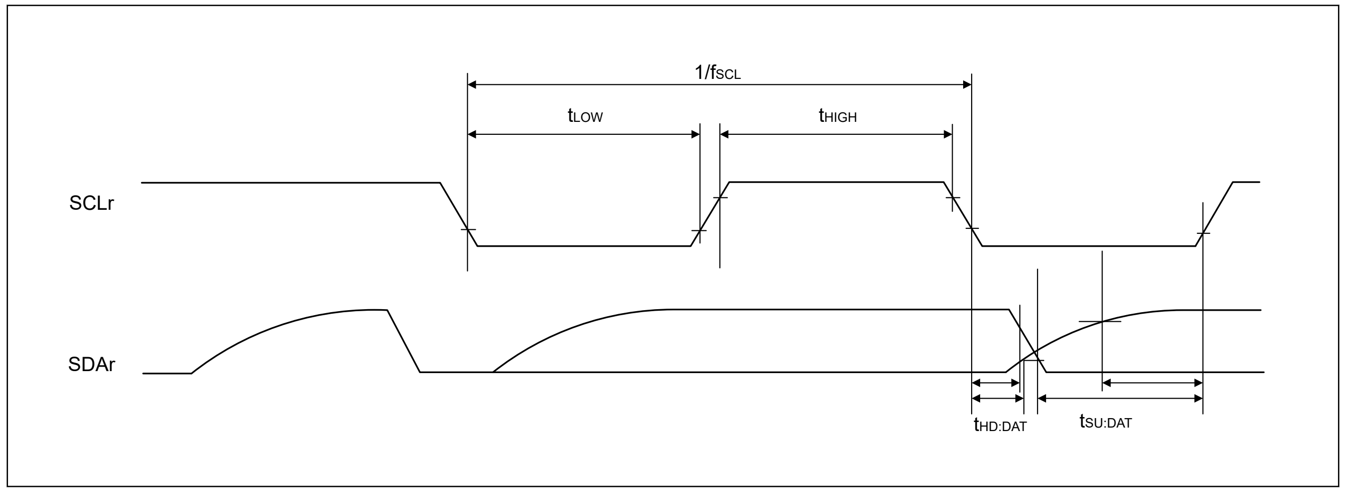


Figure 2.19 Timing of serial transfer in the simplified IIC communications with devices operating at the same voltage levels

Note:
- R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance
- r: IIC number (r = 00, 11), gh: Port number (gh = 100, 102, 110, 112, 201, 212)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03)

Table 2.26 In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V) (1)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter				Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
					Min.	Max.	Min.	Max.	Min.	Max.		
Transfer rate	Reception	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		—	—	$f_{MCK}/6^{*1}$	—	$f_{MCK}/6^{*1}$	—	$f_{MCK}/6^{*1}$	bps	Figure 2.21
			Theoretical value of the maximum transfer rate f_{MCK} = PCLKB*3		—	5.3	—	4	—	0.33	Mbps	
		2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			—	$f_{MCK}/6^{*1}$	—	$f_{MCK}/6^{*1}$	—	$f_{MCK}/6^{*1}$	bps	
			Theoretical value of the maximum transfer rate f_{MCK}*3 = PCLKB*3		—	5.3	—	4	—	0.33	Mbps	
		1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			—	$f_{MCK}/6^{*1}$ *2	—	$f_{MCK}/6^{*1\ *2}$	—	$f_{MCK}/6^{*1}$ *2	bps	
			Theoretical value of the maximum transfer rate f_{MCK} = PCLKB*3		—	5.3	—	4	—	0.33	Mbps	

Note 1. Transfer rate in the Snooze mode is within the range from 4800 to 9600 bps.
Note 2. Use this rate with VCC ≥ V_b.
Note 3. The maximum operating frequencies of the system clock (PCLKB) are:
High-speed mode: 32 MHz (1.8 V ≤ VCC ≤ 5.5 V), 4 MHz (1.6 V ≤ VCC ≤ 5.5 V)
Middle-speed mode: 16 MHz (1.8 V ≤ VCC ≤ 5.5 V), 4 MHz (1.6 V ≤ VCC ≤ 5.5 V)
Low-speed mode: 2 MHz (1.6 V ≤ VCC ≤ 5.5 V)

Note: Select the TTL input buffer for the RXDq pin and the N-ch open drain output [withstand voltage of VCC] mode for the TXDq pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

Note:
- V_b[V]: Communication line voltage
- q: UART number (q = 0, 1), gh: Port number (gh = 100, 101, 109, 110, 212, 213, 300)
- f_{MCK}: Serial array unit operation clock frequency

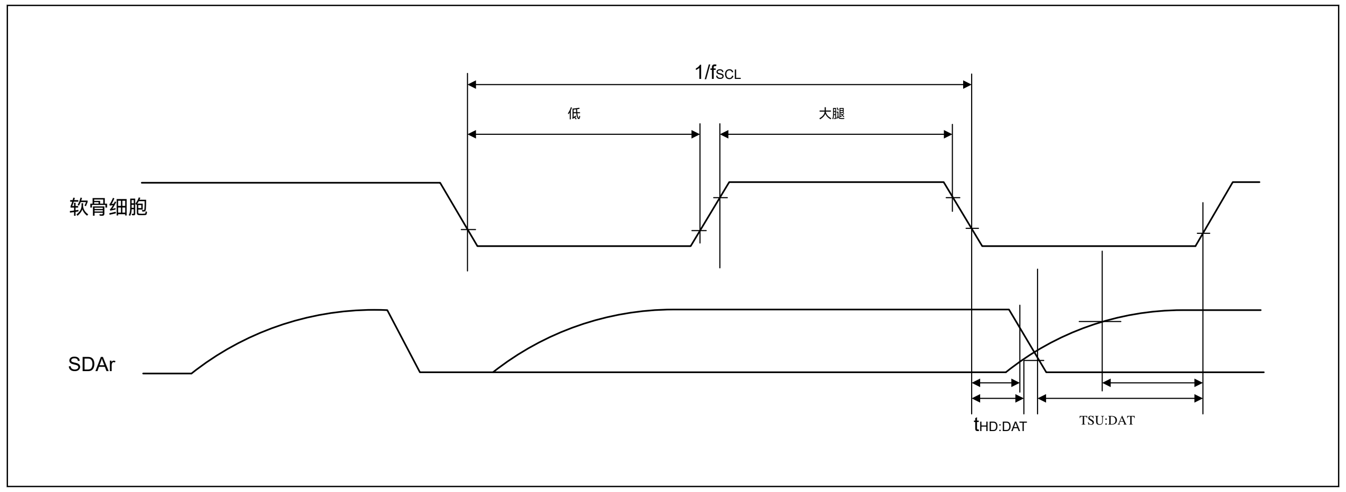


图 2.19 简化的 IIC 通信中，工作电压相同的设备串行传输的时序

注：●R_b[Ω]: 通信线 (SDAr) 上拉电阻，C_b[F]: 通信线 (SDAr, SCLr) 负载电容

●r：IIC 号码(r = 00, 11），gh：端口号(gh = 100，102、110、112、201、212）

●fMCK：串行阵列单元操作时钟频率
要设置此工作时钟，请使用串行模式寄存器 mn (SMRmn) 中的 CKSmn 位。
m：单元编号，n：通道编号(mn = 00，03）

表 2.26 与工作电压等级不同的设备（1.8 V、2.5 V、3 V）进行 UART 通信 (1)

条件：VCC = 1.8至5.5 V, VSS= 0 V,Ta= -40 至+125°C

范围				象征	高速模式		中速模式		低速模式		单元	测试状况
					最小。	最大限度。	最小。	最大限度。	最小。	最大限度。		
Transfer rate	Reception	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V		—	—	$f_{MCK}/6^{*1}$	—	$f_{MCK}/6^{*1}$	—	$f_{MCK}/6^{*1}$	bps	图 2.21
			最大转移率的理论值 f_{MCK} = PCLKB*3		—	5.3	—	4	—	0.33	兆比特	
		2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V			—	$f_{MCK}/6^{*1}$	—	$f_{MCK}/6^{*1}$	—	$f_{MCK}/6^{*1}$	bps	
			最大转移率的理论值 f_{MCK}*3 = PCLKB*3		—	5.3	—	4	—	0.33	兆比特	
		1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V			—	$f_{MCK}/6^{*1}$ *2	—	$f_{MCK}/6^{*1\ *2}$	—	$f_{MCK}/6^{*1}$ *2	bps	
			最大转移率的理论值 f_{MCK} = PCLKB*3		—	5.3	—	4	—	0.33	兆比特	

注1：睡眠模式下的传输速率在4800到9600 bps范围内。
注2. 将此利率与VCC ≥ V_b.一起使用
注3. 系统时钟（PCLKB）的最大工作频率为：
高速模式：32 MHz (1.8 V ≤ VCC ≤ 5.5 V)，4 MHz(1.6 V ≤ VCC ≤ 5.5 V)
中速模式：16 MHz(1.8 V ≤ VCC ≤ 5.5 V)，4MHz (1.6 V ≤ VCC ≤ 5.5 V)
低速模式：2 MHz(1.6 V ≤ VCC ≤ 5.5 V)

注意：使用端口gh引脚功能选择寄存器（PghPFS_A.PIM和PghPFS_A.NCODR）为RXDq引脚选择TTL输入缓冲器，并为TXDq引脚选择N沟道开漏输出模式（[VCC耐压模式，]）。对于V_{IH}和V_{IL}，请参阅选择TTL输入缓冲器后的直流特性。

注：●V_b[V]: 通信线路电压

●q：UART 号(q = 0, 1)，gh：端口号(gh = 100, 101，109、110、212、213、300）

● f_{MCK}: 串行阵列单元操作时钟频率

To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 03)

- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Table 2.27 In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V) (2)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter			Symbol	High-speed mode Min.	High-speed mode Max.	Middle-speed mode Min.	Middle-speed mode Max.	Low-speed mode Min.	Low-speed mode Max.	Unit	Test Conditions
Transfer rate, Transmission	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		—	—	*1	—	*1	—	*1	bps	Figure 2.21
		Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		—	2.8*2	—	2.8*2	—	2.8*2	Mbps	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			—	*3	—	*3	—	*3	bps	
		Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		—	1.2*4	—	1.2*4	—	1.2*4	Mbps	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			—	*5 *6	—	*5 *6	—	*5 *6	bps	
		Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		—	0.43*7	—	0.43*7	—	0.43*7	Mbps	

Note 1. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\left\{-C_b \times R_b \times \ln\left(1-\frac{2.2}{V_b}\right)\right\} \times 3}[\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate}\times 2} - \left\{-C_b \times R_b \times \ln\left(1-\frac{2.2}{V_b}\right)\right\}}{\left(\frac{1}{\text{Transfer rate}}\right)\times \text{Number of transferred bits}} \times 100[\%]$$

This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This rate is calculated as an example when the conditions described in the Conditions column are met. See *1 above to calculate the maximum transfer rate under the conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\left\{-C_b \times R_b \times \ln\left(1-\frac{2.0}{V_b}\right)\right\} \times 3}[\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate}\times 2} - \left\{-C_b \times R_b \times \ln\left(1-\frac{2.0}{V_b}\right)\right\}}{\left(\frac{1}{\text{Transfer rate}}\right)\times \text{Number of transferred bits}} \times 100[\%]$$

This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4. This rate is calculated as an example when the conditions described in the Conditions column are met. See *3 above to calculate the maximum transfer rate under the conditions of the customer.

Note 5. Use this rate with VCC ≥ V_b.

Note 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\left\{-C_b \times R_b \times \ln\left(1-\frac{1.5}{V_b}\right)\right\} \times 3}[\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate}\times 2} - \left\{-C_b \times R_b \times \ln\left(1-\frac{1.5}{V_b}\right)\right\}}{\left(\frac{1}{\text{Transfer rate}}\right)\times \text{Number of transferred bits}} \times 100[\%]$$

要设置此工作时钟，请使用串行模式寄存器 mn (SMRmn) 中的 CKS 位。
m：单元编号，n：通道编号(mn = 00, 01, 02, 03)

●由于 P212PFS_A 和 P213PFS_A 寄存器没有 PIM 位，因此无法使用 P212 和 P213 与工作电压不同的设备进行通信。

表 2.27 与工作电压等级不同的设备（1.8 V、2.5 V、3 V）进行 UART 通信 (2)

条件：VCC = 1.8到5.5 V, VSS = 0 V,然后= -40 到+125°C

范围			象征	高速模式 最小。	高速模式 最大限度。	中速模式 最小。	中速模式 最大限度。	低速模式 最小。	低速模式 最大限度。	单元	测试状况
Transfer rate, Transmission	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V		—	—	*1	—	*1	—	*1	bps	图 2.21
		理论最大传输速率值：C b = 50pF，Rb= 10.4 kΩ，Vb= 20.7 V		—	2.8*2	—	2.8*2	—	2.8*2	兆比特	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V			—	*3	—	*3	—	*3	bps	
		最大转移率的理论值C_b = 50pF, R_b = 2.7 kΩ, V_b = 2.3 V		—	1.2*4	—	1.2*4	—	1.2*4	兆比特	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V			—	*5 *6	—	*5 *6	—	*5 *6	bps	
		最大转移率的理论值C_b = 50pF, R_b = 5.5 kΩ, V_b = 1.6 V		—	0.43*7	—	0.43*7	—	0.43*7	兆比特	

注 1. 使用$f_{MCK}/6$ 或以下表达式得出的较小最大转移率是有效的最大转移率。
当4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V时，计算转移率的表达式

$$\text{最大转账速率} = \frac{1}{-C_b \times R_b \times \ln\ 1-\frac{2.2}{V_b} \times 3}[\text{bps}]$$

$$\text{波特率误差（oretical value)} = \frac{\frac{1}{\text{Transfer rate}\times 2} - -C_b \times R_b \times \ln\ 1-\frac{2.2}{V_b}}{\frac{1}{\text{Transfer rate}}\times \text{Number of transferred bits}} \times 100[\%]$$

该值是发射端和接收端之间相对差异的理论值。

注2：此费率是在满足“条件”列中所述条件时计算的示例费率。See *1 用于计算客户条件下的最大转账费率。

注 3. 使用$f_{MCK}/6$ 或以下表达式得出的较小最大转移率是有效的最大转移率。
Expression for calculating the transfer rate when 2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V

$$\text{格言 m transfer rate} = \frac{1}{\left\{-C_b \times R_b \times \ln\left(1-\frac{2.0}{V_b}\right)\right\} \times 3}[\text{bps}]$$

$$\text{波德拉te error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate}\times 2} - \left\{-C_b \times R_b \times \ln\left(1-\frac{2.0}{V_b}\right)\right\}}{\left(\frac{1}{\text{Transfer rate}}\right)\times \text{Number of transferred bits}} \times 100[\%]$$

该值是发射端和接收端之间相对差异的理论值。

注4：此费率是在满足“条件”列中所述条件时计算的示例。See *3用于计算客户条件下的最大转账费率。

注5. 将此利率与VCC ≥ V_b一起使用

注 6. 使用$f_{MCK}/6$ 或以下表达式得出的较小最大转移率是有效的最大转移率。
当1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V时，计算转移率的表达式

$$\text{Maximum transfer rate} = \frac{1}{\left\{-C_b \times R_b \times \ln\left(1-\frac{1.5}{V_b}\right)\right\} \times 3}[\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate}\times 2} - \left\{-C_b \times R_b \times \ln\left(1-\frac{1.5}{V_b}\right)\right\}}{\left(\frac{1}{\text{Transfer rate}}\right)\times \text{Number of transferred bits}} \times 100[\%]$$

This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 7. This rate is calculated as an example when the conditions described in the Conditions column are met. See *6 above to calculate the maximum transfer rate under the conditions of the customer.

Note: Select the TTL input buffer for the RXDq pin and the N-ch open drain output [withstand voltage of VCC] mode for the TXDq pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

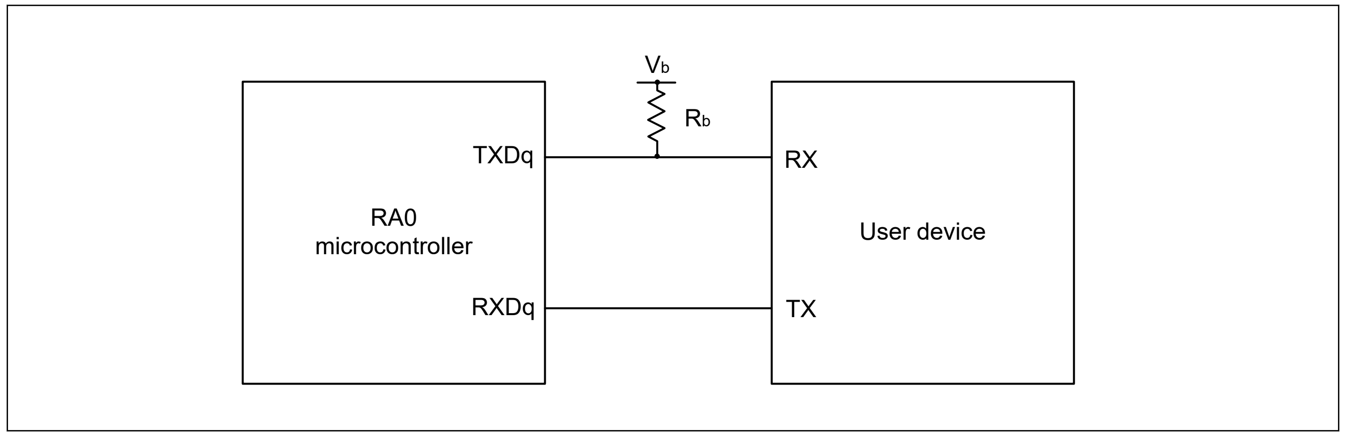


Figure 2.20 In UART communications with devices operating at different voltage levels

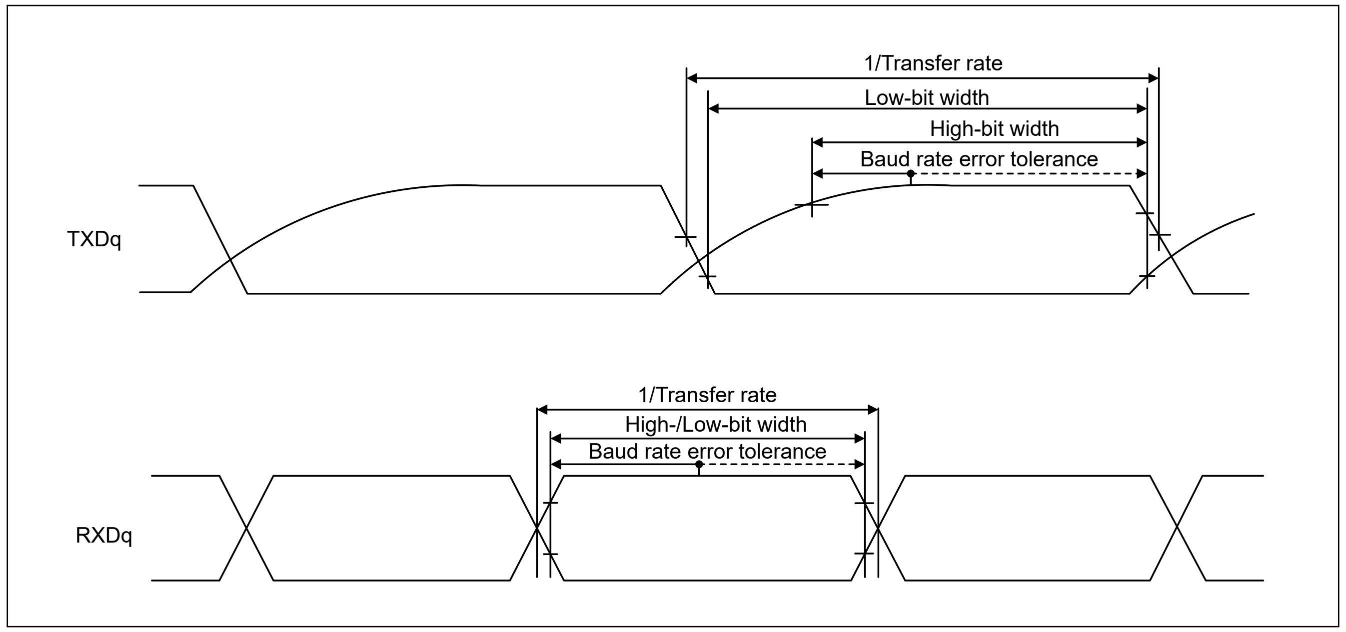


Figure 2.21 Bit width in the UART communications with devices operating at different voltage levels (reference)

Note:
- R_b[Ω]: Communication line (TXDq) pull-up resistance, C_b[F]: Communication line (TXDq) load capacitance, V_b[V]: Communication line voltage
- q: UART number (q = 0, 1), gh: Port number (gh = 100, 101, 109, 110, 212, 213, 300)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 01, 02, 03)
- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

该值是发射端和接收端之间相对差异的理论值。

注7：此费率仅为示例，计算时需满足“条件”栏中所述的条件。有关客户具体条件下的最高转账费率，请参见上文*6。

注意：使用端口 gh 引脚功能选择寄存器（PghPFS_A.PIM 和 PghPFS_A.NCODR）为 RXDq 引脚选择 TTL 输入缓冲器，并为 TXDq 引脚选择 N 沟道开漏输出模式（[耐压 VCC]）。对于V_{IH}和V_{IL}，请参阅选择 TTL 输入缓冲器后的直流特性。

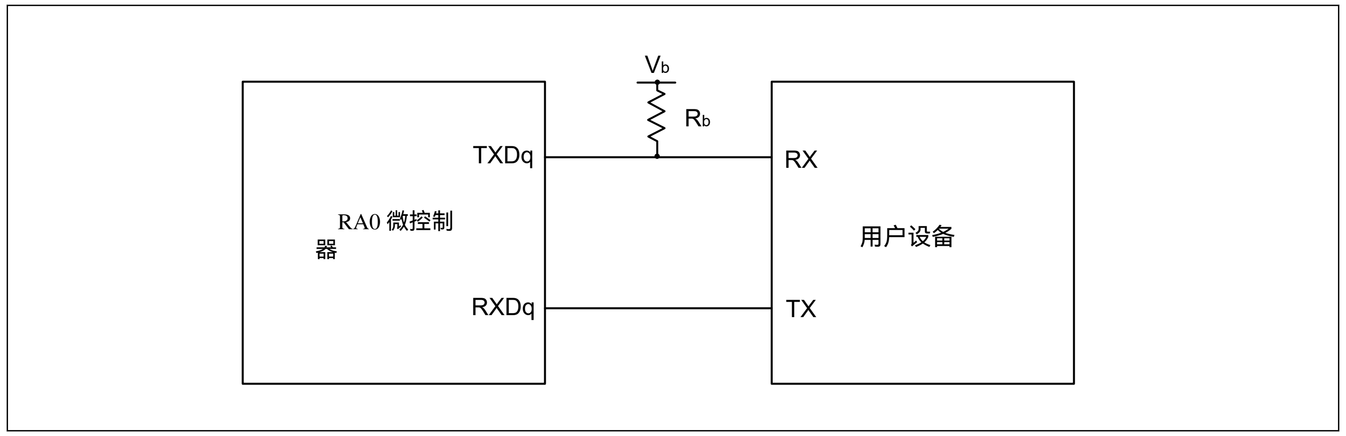


图 2.20 UART 与工作电压不同的设备进行通信

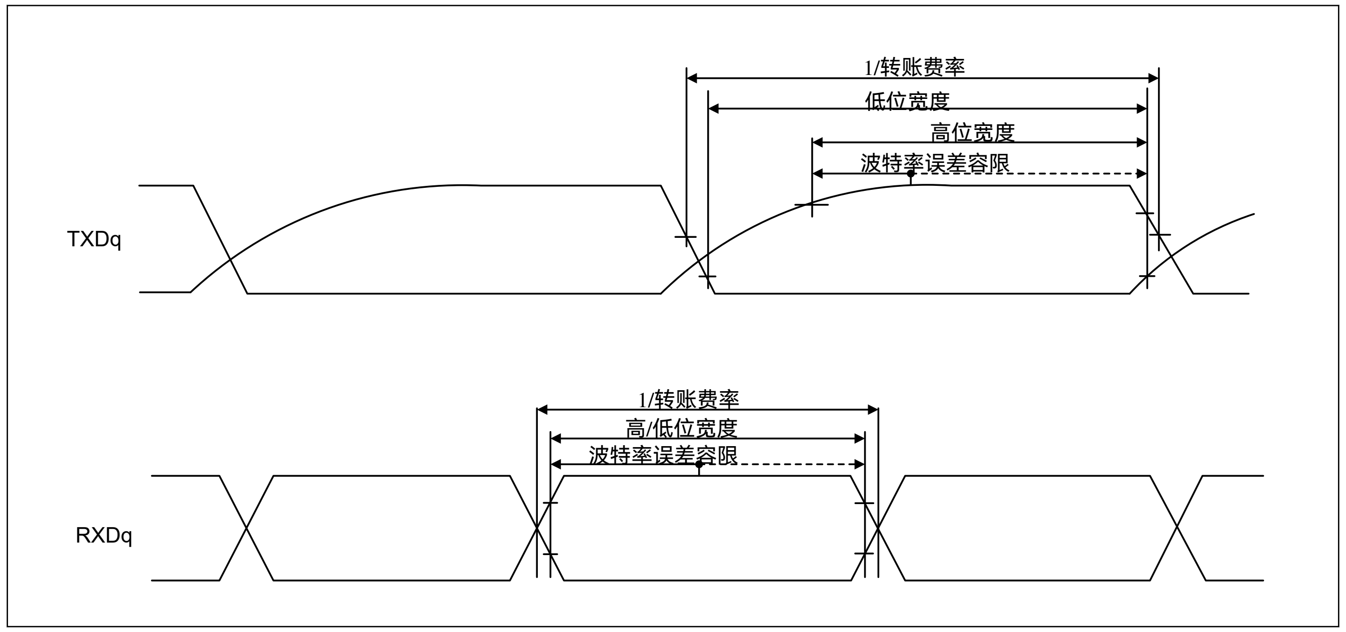


图 2.21 不同电压电平设备 UART 通信中的位宽（参考）

注：
- R_b[Ω]: 通信线 (TXDq) 上拉电阻，C_b[F]: 通信线 (TXDq) 负载电容，
  V_b[V]: 通信线路电压
- q：UART 号(q = 0, 1)，gh：端口号(gh = 100, 101，109、110、212、213、300)
- f_{MCK}：串行阵列单元操作时钟频率
  要设置此工作时钟，请使用串行模式寄存器 mn (SMRmn) 中的 CKS 位。
  m：单元编号，n：通道编号(mn = 00, 01, 02, 03)
- 由于 P212PFS_A 和 P213PFS_A 寄存器没有 PIM 位，因此无法使用 P212 和 P213 与工作电压不同的设备进行通信。

Table 2.28 In simplified SPI communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to SPI00)

Conditions: VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = -40 to +105℃

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	t_{KCY1} ≥ 2/PCLKB	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	t_{KCY1}	200	—	200	—	2300	—	ns	Figure 2.23 Figure 2.24
		2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		300	—	300	—	2300	—	ns	
SCKp high-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KH1}	t_{KCY1}/2 - 50	—	t_{KCY1}/2 - 50	—	t_{KCY1}/2 - 50	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			t_{KCY1}/2 - 120	—	t_{KCY1}/2 - 120	—	t_{KCY1}/2 - 120	—	ns	
SCKp low-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KL1}	t_{KCY1}/2 -7	—	t_{KCY1}/2 -7	—	t_{KCY1}/2 - 50	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			t_{KCY1}/2 - 10	—	t_{KCY1}/2 - 10	—	t_{KCY1}/2 - 50	—	ns	
SIp setup time (to SCKp↑)*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{SIK1}	58	—	58	—	479	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			121	—	121	—	479	—	ns	
SIp hold time (from SCKp↑)*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KSI1}	10	—	10	—	10	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			10	—	10	—	10	—	ns	
Delay time from SCKp↓ to SOp output*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KSO1}	—	60	—	60	—	60	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			—	130	—	130	—	130	ns	
SIp setup time (to SCKp↓)*2	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{SIK1}	23	—	23	—	110	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			33	—	33	—	110	—	ns	
SIp hold time (from SCKp↓)*2	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KSI1}	10	—	10	—	10	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			10	—	10	—	10	—	ns	
Delay time from SCKp↑ to SOp output*2	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KSO1}	—	10	—	10	—	10	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			—	10	—	10	—	10	ns	

Note 1. This setting applies when SCRmn.DCP[1:0] = 00b or 11b.
Note 2. This setting applies when SCRmn.DCP[1:0] = 01b or 10b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

Note:
- R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage
- p: Simplified SPI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), gh: Port number (gh = 100 to 102, 108 to 110, 112)
- f_{MCK}: Serial array unit operation clock frequency

表 2.28 在主模式下，简化的 SPI 通信，设备工作电压电平为(2.5 V或3 V，使用内部 SCKp 时钟（以下额定值仅适用于 SPI00）。

条件：VCC = 2.7至5.5 V, VSS= 0 V, Ta= -40 至+105℃

范围			象征	高速模式		中速模式		低速模式		单元	测试状况
				最小。	最大限度。	最小。	最大限度。	最小。	最大限度。		
SCKp 周期	t_{KCY1} ≥ 2/PCLKB	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V, Cb= 20 pF, Rb= 1.4 kΩ	t_{KCY1}	200	—	200	—	2300	—	ns	图 2.23 图 2.24
		2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V, Cb= 20 pF, Rb= 2.7 kΩ		300	—	300	—	2300	—	ns	
SCKp 高电平宽度	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF，R_b = 1.4 kΩ		t_{KH1}	t_{KCY1}/2 - 50	—	t_{KCY1}/2 - 50	—	t_{KCY1}/2 - 50	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V，C_b = 20 pF，R_b = 2.7 kΩ			t_{KCY1}/2 - 120	—	t_{KCY1}/2 - 120	—	t_{KCY1}/2 - 120	—	ns	
SCKp 低层宽度	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V，C_b = 20pF，R_b = 1.4 kΩ		t_{KL1}	t_{KCY1}/2 -7	—	t_{KCY1}/2 -7	—	t_{KCY1}/2 - 50	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V，C_b = 20 pF，R_b = 2.7 kΩ			t_{KCY1}/2 - 10	—	t_{KCY1}/2 - 10	—	t_{KCY1}/2 - 50	—	ns	
SIP 设置时间（至SCKp↑)*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF，R_b = 1.4 kΩ		t_{SIK1}	58	—	58	—	479	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V C_b = 20pF、R_b = 2.7 kΩ			121	—	121	—	479	—	ns	
啜饮保持时间（来自SCKp↑)*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF，R_b = 1.4 kΩ		t_{KSI1}	10	—	10	—	10	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V，C_b = 20pF，R_b = 2.7 kΩ			10	—	10	—	10	—	ns	
从SCKp↓ 到 SOp 输出的延迟时间*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF，R_b = 1.4 kΩ		t_{KSO1}	—	60	—	60	—	60	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF，R_b = 2.7 kΩ			—	130	—	130	—	130	ns	
SIp 设置时间（至SCKp↓)*2	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF，R_b = 1.4 kΩ		t_{SIK1}	23	—	23	—	110	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V C_b = 20pF、R_b = 2.7 kΩ			33	—	33	—	110	—	ns	
啜饮保持时间（从SCKp↓)*2	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF，R_b = 1.4 kΩ		t_{KSI1}	10	—	10	—	10	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V、C_b = 20pF、R_b = 2.7 kΩ			10	—	10	—	10	—	ns	
从SCKp↑ 到 SOp 输出的延迟时间*2	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF，R_b = 1.4 kΩ		t_{KSO1}	—	10	—	10	—	10	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF，R_b = 2.7 kΩ			—	10	—	10	—	10	ns	

注 1. 此设置适用于 SCRmn.DCP[1:0] = 00b 或 11b。
注 2. 此设置适用于 SCRmn.DCP[1:0] = 01b 或 10b。

注意：使用端口gh引脚功能选择寄存器（PghPFS_A.PIM和PghPFS_A.NCODR）为SIp引脚选择TTL输入缓冲器，并为[引脚选择N沟道开漏输出耐压模式（VCC为]），为SOp引脚和SCKp引脚选择N沟道开漏输出模式。对于V_{IH}和V_{IL}，引脚，请参阅选择TTL输入缓冲器后的直流特性。

注：
- R_b[Ω]: 通信线路(SCKp, SOp) 上拉电阻，C_b[F]: 通信线路（SCKp、SOp）负载电容，V_b[V]: 通信线路电压
- p：简化的 SPI 编号(p = 00），m：单元编号(m = 0) n：通道编号(n = 0)，gh：端口编号(gh =（100 至 102，108 至 110，112）
- fMCK：串行阵列单元操作时钟频率

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00)

Table 2.29 In simplified SPI communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock (1)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	t_{KCY1} ≥ 4/ PCLKB	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}	300	—	300	—	2300	—	ns	Figure 2.23 Figure 2.24
		2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		500	—	500	—	2300	—	ns	
		1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*1, C_b = 30 pF, R_b = 5.5 kΩ		1150	—	1150	—	2300	—	ns	
SCKp high-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KH1}	$t_{KCY1}/2 - 75$	—	$t_{KCY1}/2 - 75$	—	$t_{KCY1}/2 - 75$	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			$t_{KCY1}/2 - 170$	—	$t_{KCY1}/2 - 170$	—	$t_{KCY1}/2 - 170$	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*1, C_b = 30 pF, R_b = 5.5 kΩ			$t_{KCY1}/2 - 458$	—	$t_{KCY1}/2 - 458$	—	$t_{KCY1}/2 - 458$	—	ns	
SCKp low-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KL1}	$t_{KCY1}/2 - 12$	—	$t_{KCY1}/2 - 12$	—	$t_{KCY1}/2 - 50$	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			$t_{KCY1}/2 - 18$	—	$t_{KCY1}/2 - 18$	—	$t_{KCY1}/2 - 50$	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*1, C_b = 30 pF, R_b = 5.5 kΩ			$t_{KCY1}/2 - 50$	—	$t_{KCY1}/2 - 50$	—	$t_{KCY1}/2 - 50$	—	ns	

Note 1. Use this setting with VCC ≥ V_b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

要设置此工作时钟，请使用串行模式寄存器 mn (SMRmn) 中的 CKSmn 位。
m：单元编号，n：通道编号(mn = 00)

表 2.29 在主模式下，简化的 SPI 通信中，设备以不同的电压电平（1.8 V、2.5 V, 或3 V)，内部 SCKp 时钟 (1)）运行。

条件：VCC = 1.8至5.5 V, VSS = 0 V, Ta = -40 to +125°C

范围			象征	高速模式		中速模式		低速模式		单元	测试状况
				最小。	最大限度。	最小。	最大限度。	最小。	最大限度。		
SCKp 循环时间	t_{KCY1} ≥ 4/ PCLKB	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V, Cb= 30 pF, Rb= 1.4 kΩ	t_{KCY1}	300	—	300	—	2300	—	ns	图 2.23 图 2.24
		2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V, Cb= 30 pF, Rb= 2.7 kΩ		500	—	500	—	2300	—	ns	
		1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*1, Cb= 30 pF, Rb= 5.5 kΩ		1150	—	1150	—	2300	—	ns	
SCKp高级别宽度	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V, C_b = 30pF, R_b = 1.4 kΩ		t_{KH1}	$t_{KCY1}/2 - 75$	—	$t_{KCY1}/2 - 75$	—	$t_{KCY1}/2 - 75$	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V, C_b = 30pF, R_b = 2.7 kΩ			$t_{KCY1}/2 - 170$	—	$t_{KCY1}/2 - 170$	—	$t_{KCY1}/2 - 170$	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*1, Cb= 30 pF, R_b = 5.5 kΩ			$t_{KCY1}/2 - 458$	—	$t_{KCY1}/2 - 458$	—	$t_{KCY1}/2 - 458$	—	ns	
SCKp 低水平宽度	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V, Cb= 30 pF, R_b = 1.4 kΩ		t_{KL1}	$t_{KCY1}/2 - 12$	—	$t_{KCY1}/2 - 12$	—	$t_{KCY1}/2 - 50$	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V, C_b = 30pF, R_b = 2.7 kΩ			$t_{KCY1}/2 - 18$	—	$t_{KCY1}/2 - 18$	—	$t_{KCY1}/2 - 50$	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*1, C_b = 30pF, R_b = 5.5 kΩ			$t_{KCY1}/2 - 50$	—	$t_{KCY1}/2 - 50$	—	$t_{KCY1}/2 - 50$	—	ns	

注1. 将此设置与VCC ≥ V_b一起使用。

注意：使用端口gh引脚功能选择寄存器（PghPFS_A.PIM和PghPFS_A.NCODR）为SIp 引脚选择TTL输入缓冲器，为N引脚选择VCC耐压模式，为[引脚和] 引脚选择VCC耐压模式。对于V_{IH}和V_{IL}引脚，请参阅选择TTL输入缓冲器后的直流特性。

Table 2.30 In simplified SPI communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock (2)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
SIp setup time (to SCKp↑)*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{SIK1}	81	—	81	—	479	—	ns	Figure 2.23 Figure 2.24
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		177	—	177	—	479	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*2, C_b = 30 pF, R_b = 5.5 kΩ		479	—	479	—	479	—	ns	
SIp hold time (from SCKp↑)*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KSI1}	19	—	19	—	19	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		19	—	19	—	19	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*2, C_b = 30 pF, R_b = 5.5 kΩ		19	—	19	—	19	—	ns	
Delay time from SCKp↓ to SOp output*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KSO1}	—	100	—	100	—	100	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		—	195	—	195	—	195	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*2, C_b = 30 pF, R_b = 5.5 kΩ		—	483	—	483	—	483	ns	

Note 1. This setting applies when SCRmn.DCP[1:0] = 00b or 11b.
Note 2. Use this setting with VCC ≥ V_b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

表 2.30 在主模式下，简化的 SPI 通信，设备工作电压电平不同（1.8 V、2.5 V 或3 V），内部 SCKp 时钟 (2)）

条件：VCC = 1.8至5.5 V, VSS = 0 V, Ta = -40 至+125°C

范围		象征	高速模式		中速模式		低速模式		单元	测试状况
			最小。	最大限度。	最小。	最大限度。	最小。	最大限度。		
SIp 建立时间（到 SCKp↑）*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V, Cb= 30 pF, Rb= 1.4 kΩ	t_{SIK1}	81	—	81	—	479	—	ns	图 2.23 图 2.24
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V, Cb= 30 pF, Rb= 2.7 kΩ		177	—	177	—	479	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*2, Cb= 30 pF, Rb= 5.5 kΩ		479	—	479	—	479	—	ns	
SIp 保持时间（来自SCKp↑)*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30pF，R_b = 1.4 kΩ	t_{KSI1}	19	—	19	—	19	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V, Cb= 30 pF，R_b = 2.7 kΩ		19	—	19	—	19	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*2, C_b = 30pF，R_b = 5.5 kΩ		19	—	19	—	19	—	ns	
从SCKp↓ 到 SOp 输出的延迟时间*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V, C_b = 30pF，R_b = 1.4 kΩ	t_{KSO1}	—	100	—	100	—	100	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V, Cb= 30 pF，R_b = 2.7 kΩ		—	195	—	195	—	195	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*2, C_b = 30pF，R_b = 5.5 kΩ		—	483	—	483	—	483	ns	

注 1. 此设置适用于 SCRmn.DCP[1:0] = 00b 或 11b。
注2. 将此设置与VCC ≥ V_b一起使用。

注意：使用端口gh引脚功能选择寄存器（PghPFS_A.PIM和PghPFS_A.NCODR）为SIp 引脚选择TTL输入缓冲器，为N引脚选择VCC耐压模式，为[引脚和] 引脚选择VCC耐压模式。对于V_{IH}和V_{IL}引脚，请参阅选择TTL输入缓冲器后的直流特性。

Table 2.31 In simplified SPI communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock (3)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
SIp setup time (to SCKp↓)*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{SIK1}	44	—	44	—	110	—	ns	Figure 2.23 Figure 2.24
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		44	—	44	—	110	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*2, C_b = 30 pF, R_b = 5.5 kΩ		110	—	110	—	110	—	ns	
SIp hold time (from SCKp↓)*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KSI1}	19	—	19	—	19	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		19	—	19	—	19	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*2, C_b = 30 pF, R_b = 5.5 kΩ		19	—	19	—	19	—	ns	
Delay time from SCKp↑ to SOp output*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KSO1}	—	25	—	25	—	25	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		—	25	—	25	—	25	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*2, C_b = 30 pF, R_b = 5.5 kΩ		—	25	—	25	—	25	ns	

Note 1. This setting applies when SCRmn.DCP[1:0] = 01b or 10b.
Note 2. Use this setting with VCC ≥ V_b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

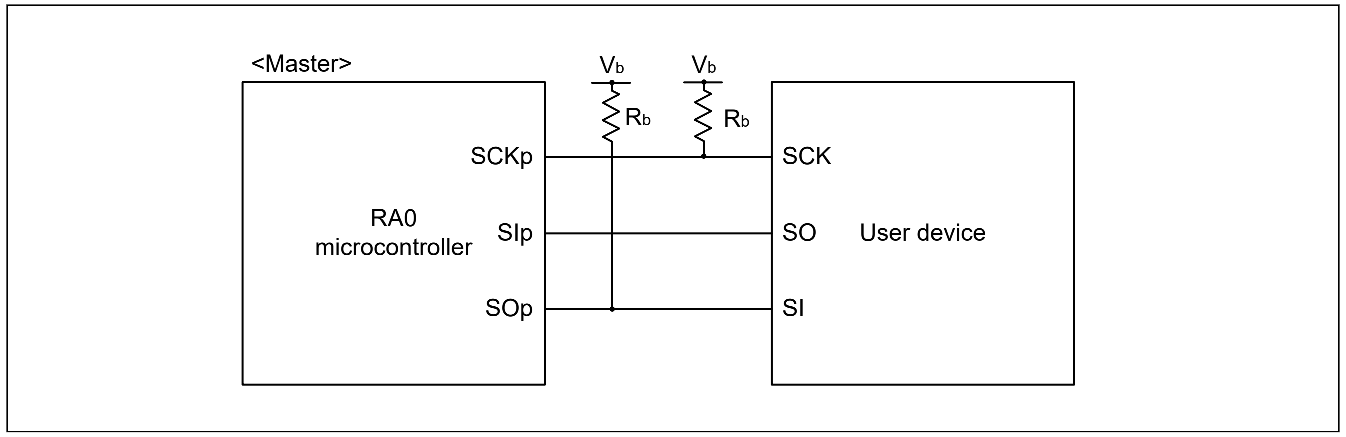


Figure 2.22 Connection in the simplified SPI communications with devices operating at different voltage levels

Note: • R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

表 2.31 在主模式下，简化的 SPI 通信，设备工作电压电平不同（1.8 V、2.5 V 或3 V），内部 SCKp 时钟 (3)）

条件：VCC = 1.8至5.5 V, VSS = 0 V, Ta = -40 至+125°C

范围		象征	高速模式		中速模式		低速模式		单元	测试状况
			最小。	最大限度。	最小。	最大限度。	最小。	最大限度。		
SIp 设置时间（至 SCKp↓)*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V, Cb= 30 pF, Rb= 1.4 kΩ	t_{SIK1}	44	—	44	—	110	—	ns	图 2.23 图 2.24
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V, Cb= 30 pF, Rb= 2.7 kΩ		44	—	44	—	110	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*2, Cb= 30 pF, Rb= 5.5 kΩ		110	—	110	—	110	—	ns	
SIp 保持时间（来自 SCKp↓ ）*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30pF, R_b = 1.4 kΩ	t_{KSI1}	19	—	19	—	19	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V, Cb= 30 pF, R_b = 2.7 kΩ		19	—	19	—	19	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*2, Cb= 30 pF, R_b = 5.5 kΩ		19	—	19	—	19	—	ns	
从SCKp↑ 到SOp输出的延迟时间*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V, C_b = 30pF, R_b = 1.4 kΩ	t_{KSO1}	—	25	—	25	—	25	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V, Cb= 30 pF, R_b = 2.7 kΩ		—	25	—	25	—	25	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*2, Cb= 30 pF, R_b = 5.5 kΩ		—	25	—	25	—	25	ns	

注 1. 此设置适用于 SCRmn.DCP[1:0] = 01b 或 10b。
注2. 将此设置与VCC ≥ V_b一起使用。

注意：使用端口gh引脚功能选择寄存器（PghPFS_A.PIM和PghPFS_A.NCODR）为SIp 引脚选择TTL输入缓冲器，为N引脚选择VCC耐压模式，为[引脚和] 引脚选择VCC耐压模式。对于V_{IH}和V_{IL}引脚，请参阅选择TTL输入缓冲器后的直流特性。

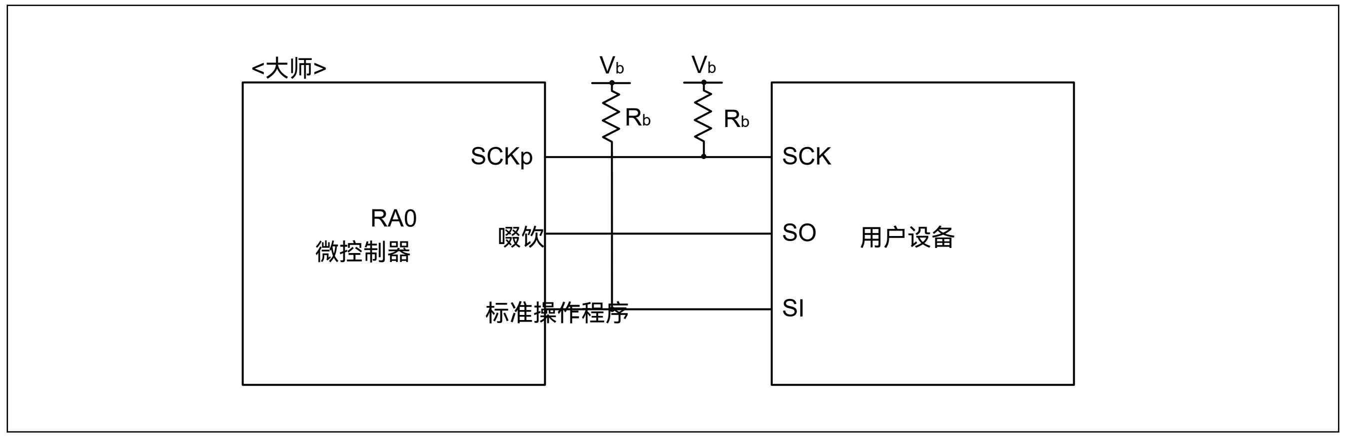


图 2.22 简化的 SPI 通信中与不同电压等级设备的连接

注：●R_b[Ω]: 通信线（SCKp、SOP）上拉电阻，C_b[F]: 通信线（SCKp、SOP）负载电容，V_b[V]: 通信线电压●p:

- p: Simplified SPI number (p = 00, 11), m: Unit number, n: Channel number (mn = 00, 03), gh: Port number (gh = 100 to 102, 108 to 110, 112, 201, 212, 213)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03)
- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

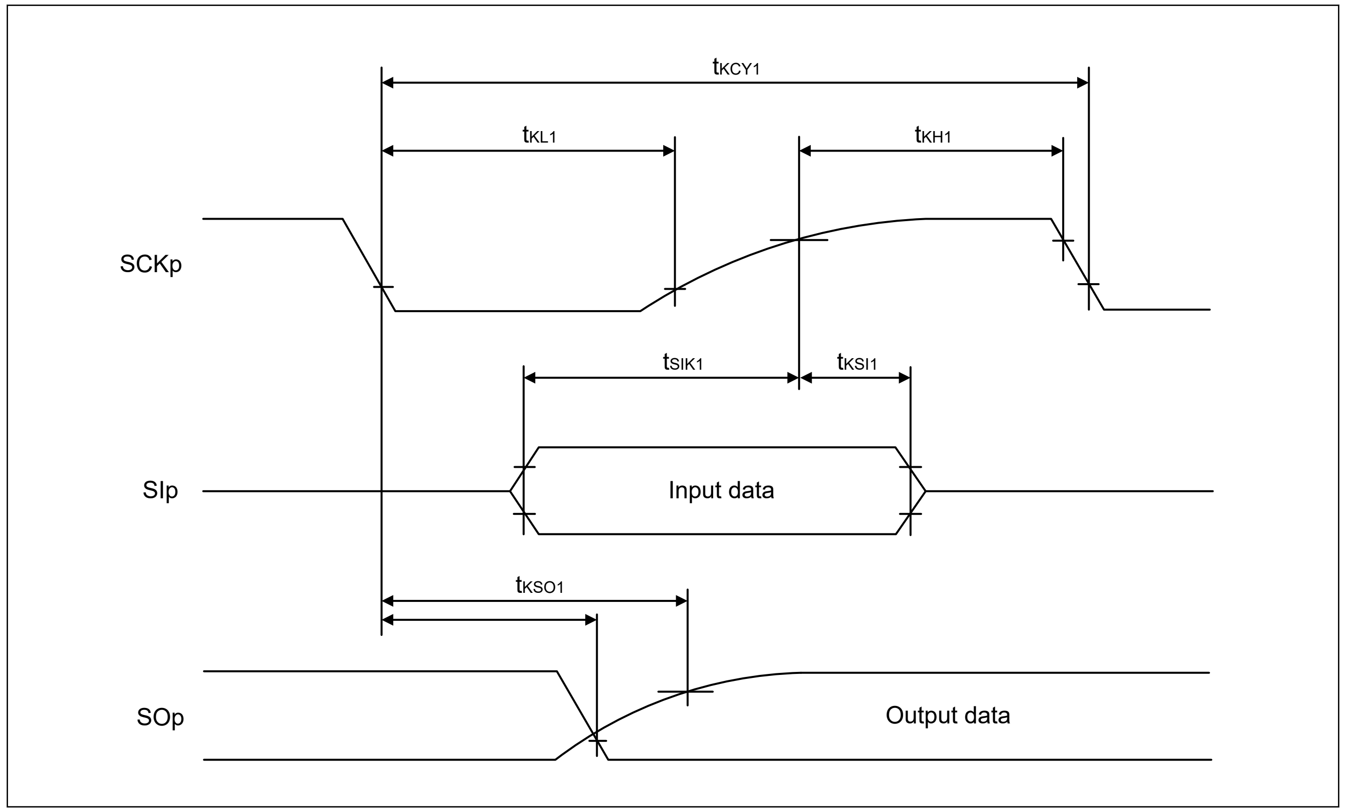


Figure 2.23 Timing of serial transfer in the simplified SPI communications in the master mode with devices operating at different voltage levels when SCRmn.DCP[1:0] = 00b or 11b

简化的 SPI 编号(p = 00, 11), m: 单元号, n: 通道号(mn = 00, 03), gh: 端口号(gh =100 至 102, 108 至 110, 112, 201, 212, 213)

●fMCK：串行阵列单元操作时钟频率
要设置此工作时钟，请使用串行模式寄存器 mn (SMRmn) 中的 CKS 位。
m：单元编号，n：通道编号(mn = 00，03)
●由于 P212PFS_A 和 P213PFS_A 寄存器没有 PIM 位，因此无法使用 P212 和 P213 与工作电压不同的设备进行通信。

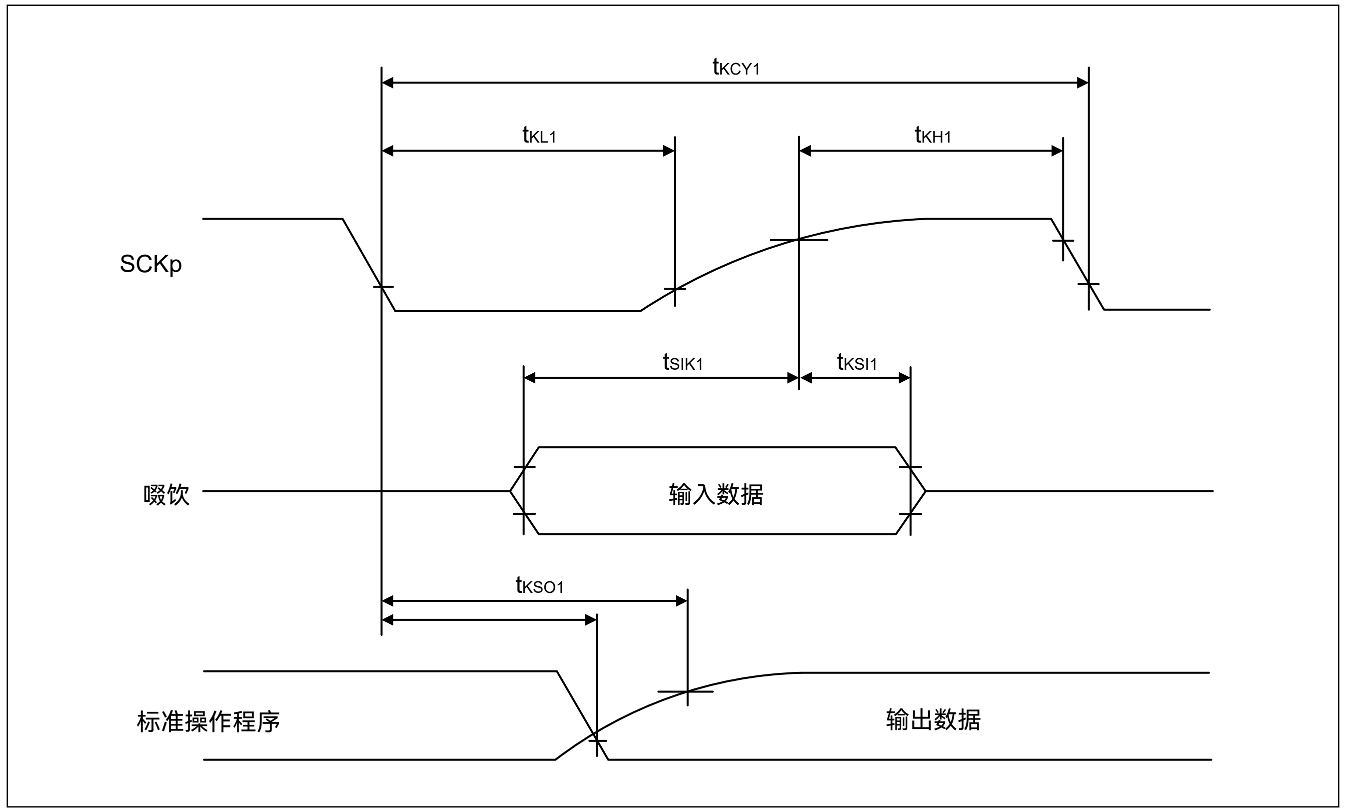


图 2.23 简化 SPI 通信中，主模式下，当 SCRmn.DCP[1:0] = 00b或 11b 时，器件工作在不同电压电平下的串行传输时序

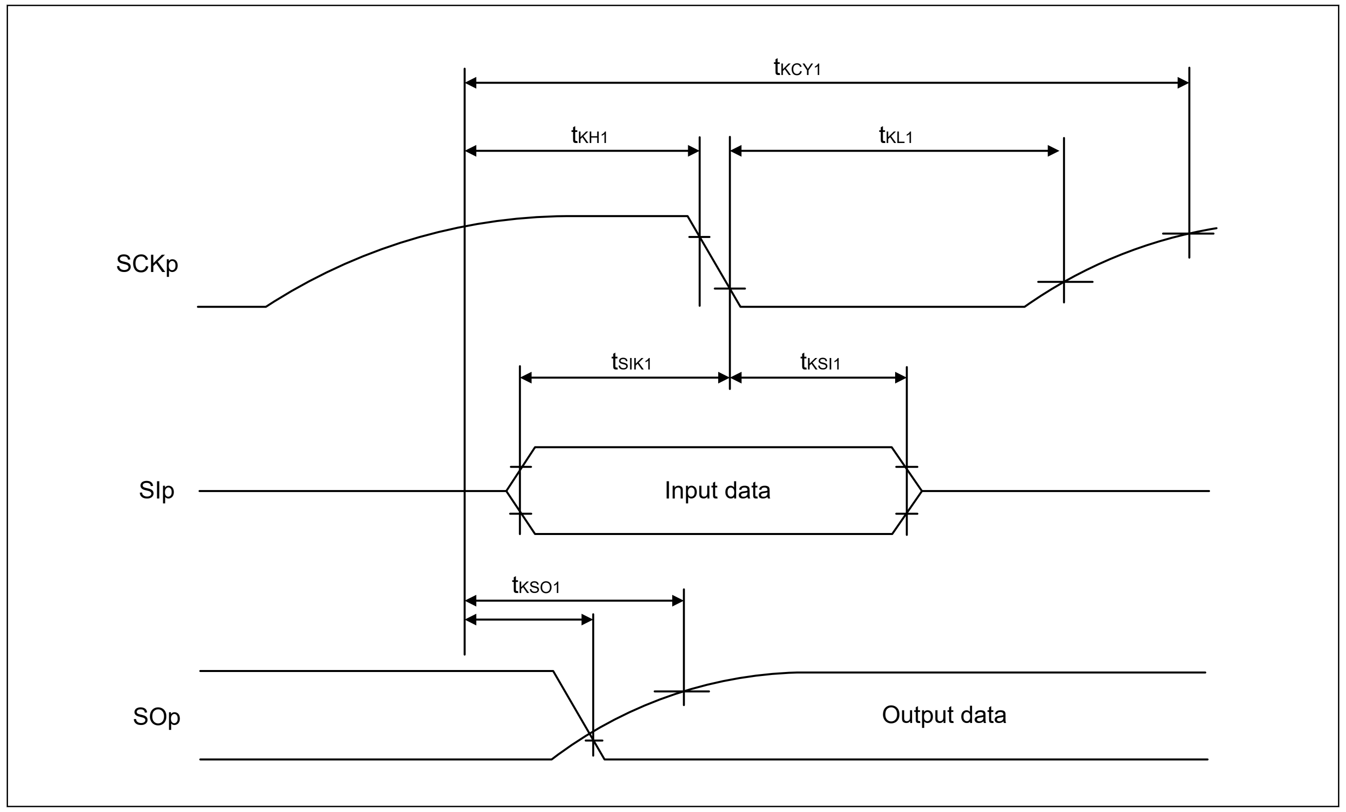


Figure 2.24 Timing of serial transfer in the simplified SPI communications in the master mode with devices operating at different voltage levels when SCRmn.DCP[1:0] = 01b or 10b

Note:
- p: Simplified SPI number (p = 00, 11), m: Unit number, n: Channel number (mn = 00, 03), gh: Port number (gh = 100 to 102, 108 to 110, 112, 201, 212, 213)
- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

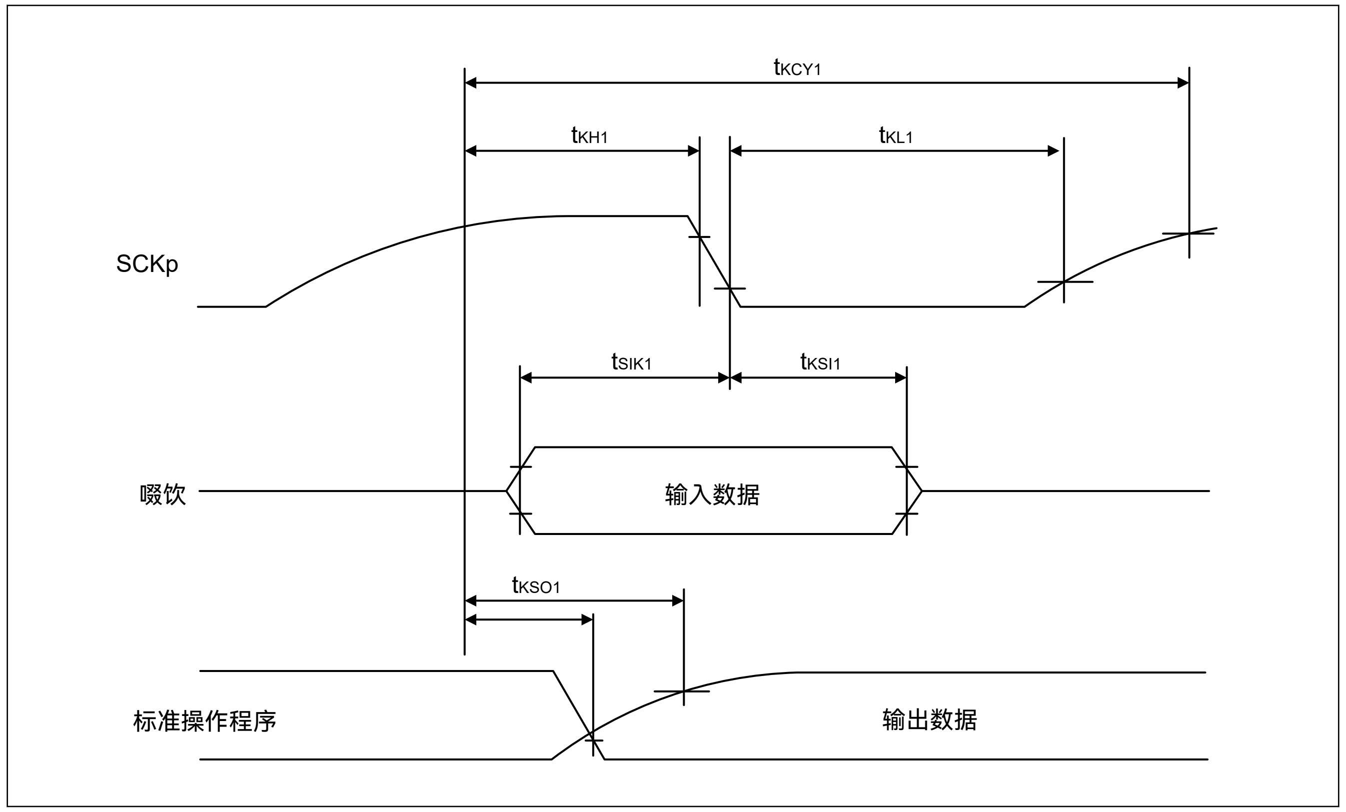


图 2.24 简化 SPI 通信中，主模式下，当 SCRmn.DCP[1:0] = 01b或 10b 时，器件工作在不同电压电平下的串行传输时序

注：●p：简化的 SPI 编号（(p = 00，11），m：单元编号，n：通道编号（(mn = 00, 03)），gh：端口编号（(gh =，100 至 102，108 至 110，112，201，212，213）

●由于 P212PFS_A 和 P213PFS_A 寄存器没有 PIM 位，因此无法使用 P212 和 P213 与工作电压不同的设备进行通信。

Table 2.32 In simplified SPI communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	f_{MCK} = 32 MHz	t_{KCY2}	14/f_{MCK}	—	—	—	—	—	ns	Figure 2.26 Figure 2.27
		8 MHz < f_{MCK} ≤ 16 MHz		10/f_{MCK}	—	10/f_{MCK}	—	—	—	ns	
		4 MHz < f_{MCK} ≤ 8 MHz		8/f_{MCK}	—	8/f_{MCK}	—	—	—	ns	
		f_{MCK} ≤ 4 MHz		6/f_{MCK}	—	6/f_{MCK}	—	10/f_{MCK}	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	f_{MCK} = 32 MHz		20/f_{MCK}	—	—	—	—	—	ns	
		8 MHz < f_{MCK} ≤ 16 MHz		12/f_{MCK}	—	12/f_{MCK}	—	—	—	ns	
		4 MHz < f_{MCK} ≤ 8 MHz		8/f_{MCK}	—	8/f_{MCK}	—	—	—	ns	
		f_{MCK} ≤ 4 MHz		6/f_{MCK}	—	6/f_{MCK}	—	10/f_{MCK}	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*2	f_{MCK} = 32 MHz		48/f_{MCK}	—	—	—	—	—	ns	
		8 MHz < f_{MCK} ≤ 16 MHz		26/f_{MCK}	—	26/f_{MCK}	—	—	—	ns	
		4 MHz < f_{MCK} ≤ 8 MHz		16/f_{MCK}	—	16/f_{MCK}	—	—	—	ns	
		f_{MCK} ≤ 4 MHz		10/f_{MCK}	—	10/f_{MCK}	—	10/f_{MCK}	—	ns	
SCKp high-/low-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KH2}, t_{KL2}	t_{KCY2}/2 - 12	—	t_{KCY2}/2 - 12	—	t_{KCY2}/2 - 50	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			t_{KCY2}/2 - 18	—	t_{KCY2}/2 - 18	—	t_{KCY2}/2 - 50	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*2			t_{KCY2}/2 - 50	—	t_{KCY2}/2 - 50	—	t_{KCY2}/2 - 50	—	ns	
SIp setup time (to SCKp↑)*3	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{SIK2}	1/f_{MCK} + 20	—	1/f_{MCK} + 20	—	1/f_{MCK} + 30	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			1/f_{MCK} + 20	—	1/f_{MCK} + 20	—	1/f_{MCK} + 30	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*2			1/f_{MCK} + 30	—	1/f_{MCK} + 30	—	1/f_{MCK} + 30	—	ns	
SIp hold time (from SCKp↑)*3			t_{KSI2}	1/f_{MCK} + 31	—	1/f_{MCK} + 31	—	1/f_{MCK} + 31	—	ns	
Delay time from SCKp↓ to SOp output*4	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KSO2}	—	2/f_{MCK} + 120	—	2/f_{MCK} + 120	—	2/f_{MCK} + 573	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			—	2/f_{MCK} + 214	—	2/f_{MCK} + 214	—	2/f_{MCK} + 573	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*2, C_b = 30 pF, R_b = 5.5 kΩ			—	2/f_{MCK} + 573	—	2/f_{MCK} + 573	—	2/f_{MCK} + 573	ns	

Note 1. Transfer rate in the Snooze mode: 1 Mbps (max.)
Note 2. Use this setting with VCC ≥ V_b.
Note 3. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The SIp setup time becomes to SCKp↓ and SIp hold time becomes from SCKp↓ when SCRmn.DCP[1:0] = 01b or 10b.
Note 4. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The delay time to SOp output becomes from SCKp↑ when SCRmn.DCP[1:0] = 01b or 10b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

表 2.32 简化的 SPI 从机模式下不同电压电平设备的通信（1.8 V，2.5 V, 或3 V），使用外部 SCKp 时钟）

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

范围			象征	高速模式		中速模式		低速模式		单元	测试状况
				最小。	最大限度。	最小。	最大限度。	最小。	最大限度。		
SCKp 循环时间*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V	f_{MCK} = 32 MHz	t_{KCY2}	14/f_{MCK}	—	—	—	—	—	ns	图 2.26 图 2.27
		8 MHz < f_{MCK} ≤ 16 MHz		10/f_{MCK}	—	10/f_{MCK}	—	—	—	ns	
		4 MHz < f_{MCK} ≤ 8 MHz		8/f_{MCK}	—	8/f_{MCK}	—	—	—	ns	
		f_{MCK} ≤ 4 MHz		6/f_{MCK}	—	6/f_{MCK}	—	10/f_{MCK}	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	f_{MCK} = 32 MHz		20/f_{MCK}	—	—	—	—	—	ns	
		8 MHz < f_{MCK} ≤ 16 MHz		12/f_{MCK}	—	12/f_{MCK}	—	—	—	ns	
		4 MHz < f_{MCK} ≤ 8 MHz		8/f_{MCK}	—	8/f_{MCK}	—	—	—	ns	
		f_{MCK} ≤ 4 MHz		6/f_{MCK}	—	6/f_{MCK}	—	10/f_{MCK}	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*2	f_{MCK} = 32 MHz		48/f_{MCK}	—	—	—	—	—	ns	
		8 MHz < f_{MCK} ≤ 16 MHz		26/f_{MCK}	—	26/f_{MCK}	—	—	—	ns	
		4 MHz < f_{MCK} ≤ 8 MHz		16/f_{MCK}	—	16/f_{MCK}	—	—	—	ns	
		f_{MCK} ≤ 4 MHz		10/f_{MCK}	—	10/f_{MCK}	—	10/f_{MCK}	—	ns	
SCKp 高/低电平宽度	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KH2}, t_{KL2}	t_{KCY2}/2 - 12	—	t_{KCY2}/2 - 12	—	t_{KCY2}/2 - 50	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V			t_{KCY2}/2 - 18	—	t_{KCY2}/2 - 18	—	t_{KCY2}/2 - 50	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*2			t_{KCY2}/2 - 50	—	t_{KCY2}/2 - 50	—	t_{KCY2}/2 - 50	—	ns	
SIp 设置时间（至SCKp↑）*3	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{SIK2}	1/f_{MCK} + 20	—	1/f_{MCK} + 20	—	1/f_{MCK} + 30	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V			1/f_{MCK} + 20	—	1/f_{MCK} + 20	—	1/f_{MCK} + 30	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*2			1/f_{MCK} + 30	—	1/f_{MCK} + 30	—	1/f_{MCK} + 30	—	ns	
啜饮保持时间（来自SCKp↑）*3			t_{KSI2}	1/f_{MCK} + 31	—	1/f_{MCK} + 31	—	1/f_{MCK} + 31	—	ns	
从SCKp↓到SOp输出的延迟时间*4	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V, Cb= 30 pF, R_b = 1.4 kΩ		t_{KSO2}	—	2/f_{MCK} + 120	—	2/f_{MCK} + 120	—	2/f_{MCK} + 573	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V, Cb= 30 pF, R_b = 2.7 kΩ			—	2/f_{MCK} + 214	—	2/f_{MCK} + 214	—	2/f_{MCK} + 573	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*2, C_b = 30pF, R_b = 5.5 kΩ			—	2/f_{MCK} + 573	—	2/f_{MCK} + 573	—	2/f_{MCK} + 573	ns	

注1：休眠模式下的传输速率：1 Mbps（最大值）
注2. 将此设置与VCC ≥ V_b一起使用。
注 3. 此设置适用于 SCRmn.DCP[1:0] = 00b 或 11b。当 SCRmn.DCP[1:0] = 01b 或 10b 时，SIp的建立时间变为SCKp↓，SIp的保持时间变为SCKp↓ 。

注 4. 此设置适用于 SCRmn.DCP[1:0] = 00b 或 11b。当 SCRmn.DCP[1:0] = 01b 或 10b 时，SOp输出的延迟时间将变为SCKp↑ 。

注意：使用端口gh引脚功能选择寄存器（PghPFS_A.PIM和PghPFS_A.NCODR）为SIp 引脚选择TTL输入缓冲器，并为[引脚选择N沟道开漏输出耐压模式（VCC），为SOp引脚和SCKp引脚选择N沟道开漏输出模式。对于V_{IH}和V_{IL}引脚，请参阅选择TTL输入缓冲器后的直流特性。

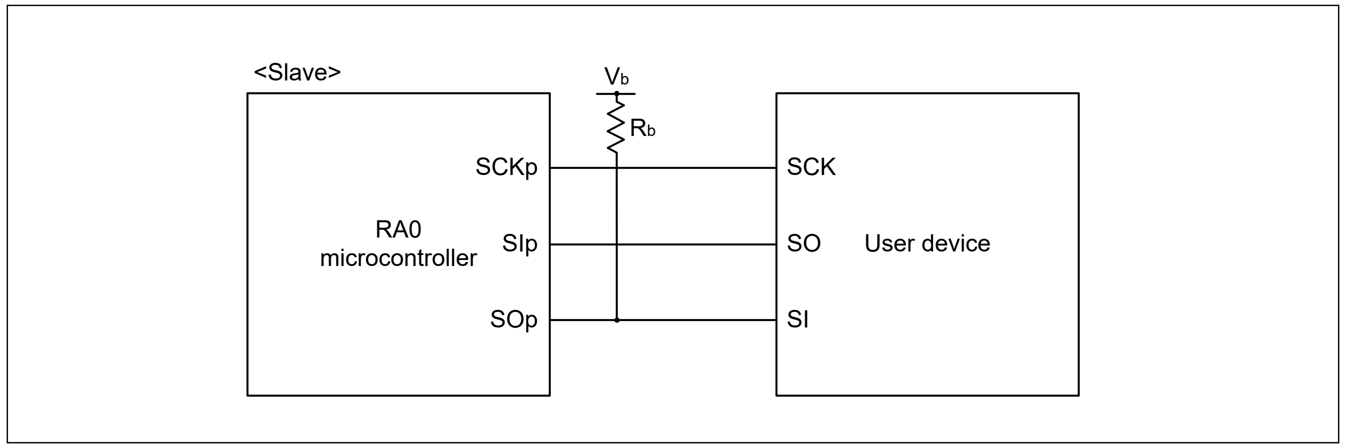


Figure 2.25 Connection in the simplified SPI communications with devices operating at different voltage levels

Note:
- R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage
- p: Simplified SPI number (p = 00, 11), m: Unit number, n: Channel number (mn = 00, 03), gh: Port number (gh = 100 to 102, 108 to 110, 112, 201, 212, 213)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03, 10, 11)
- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

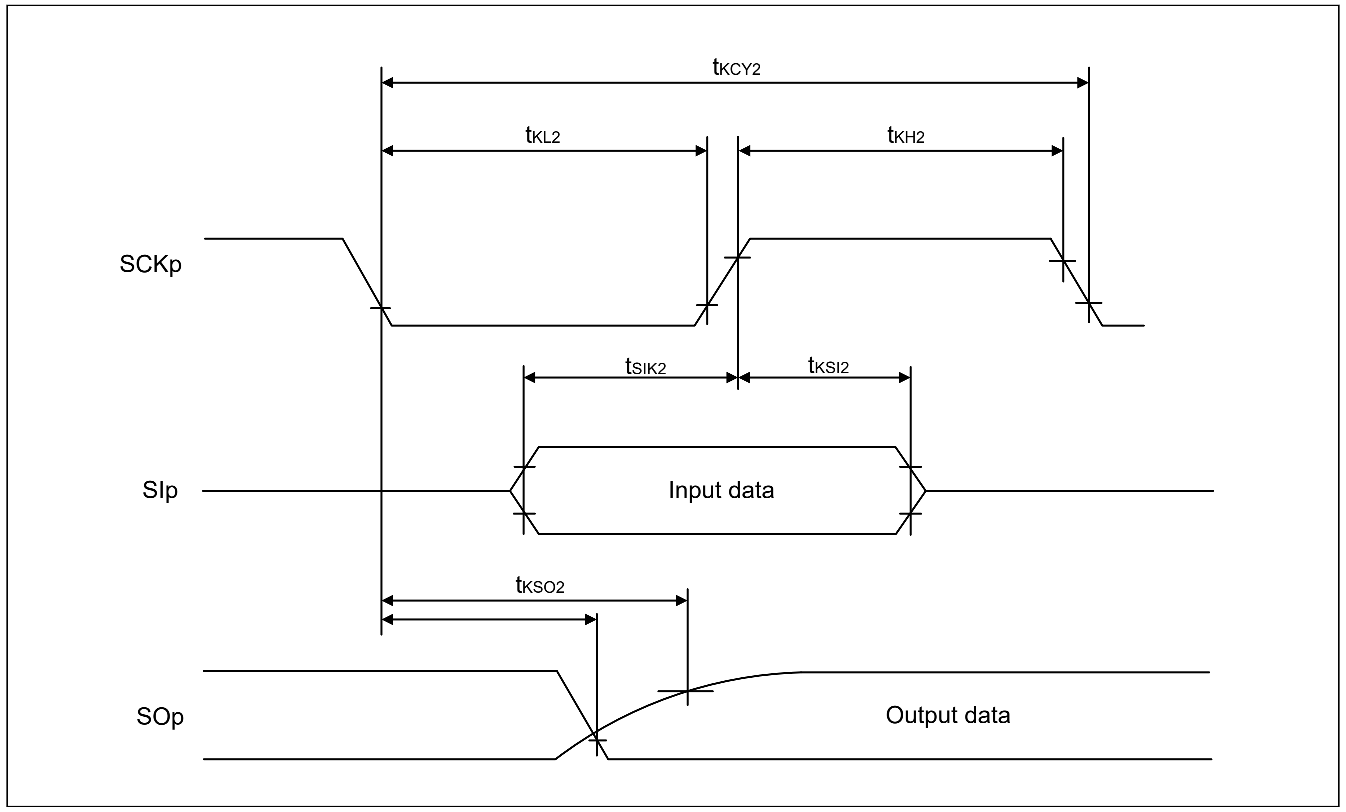


Figure 2.26 Timing of serial transfer in the simplified SPI communications in the slave mode with devices operating at different voltage levels when SCRmn.DCP[1:0] = 00b or 11b

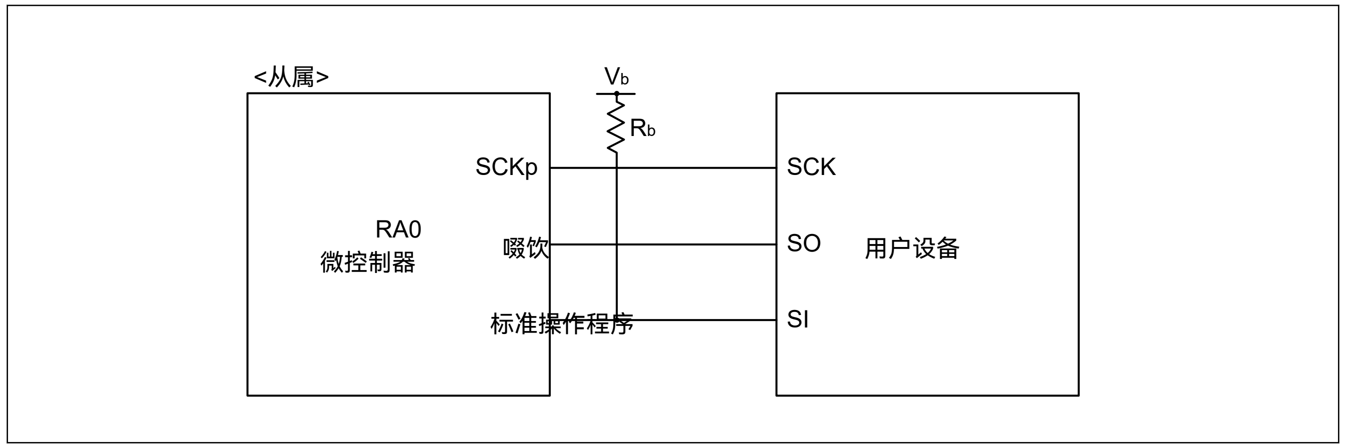


图 2.25 简化的 SPI 通信中与不同电压等级设备的连接

注：●R_b[Ω]: 通信线（SOp）上拉电阻，C_b[F]: 通信线，(SOp) 负载电容，V_b[V]:
通信线路电压

●p：简化的 SPI 编号（(p = 00，11），m：单元编号，n：通道编号（(mn = 00，03），gh：端口编号（(gh =，100 至 102、108 至 110、112、201、212、213）

●fMCK：串行阵列单元操作时钟频率
要设置此工作时钟，请使用串行模式寄存器 mn (SMRmn) 中的 CKS 位。
m：单元编号，n：通道编号(mn = 00, 03, 10, 11)

●由于 P212PFS_A 和 P213PFS_A 寄存器没有 PIM 位，因此无法使用 P212 和 P213 与工作电压不同的设备进行通信。

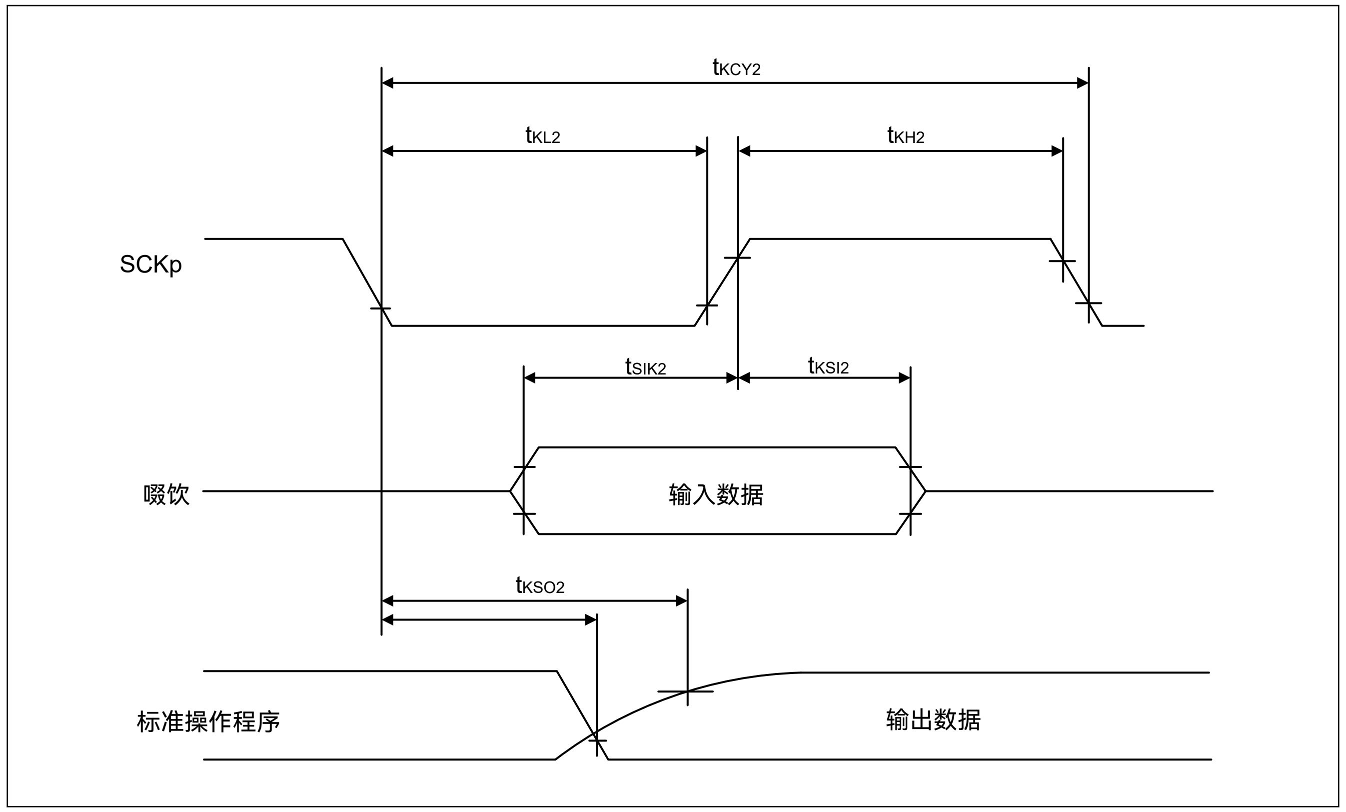


图 2.26 简化 SPI 通信中从模式下串行传输的时序，其中器件工作在不同电压电平，当 SCRmn.DCP[1:0] = 00b 或 11b

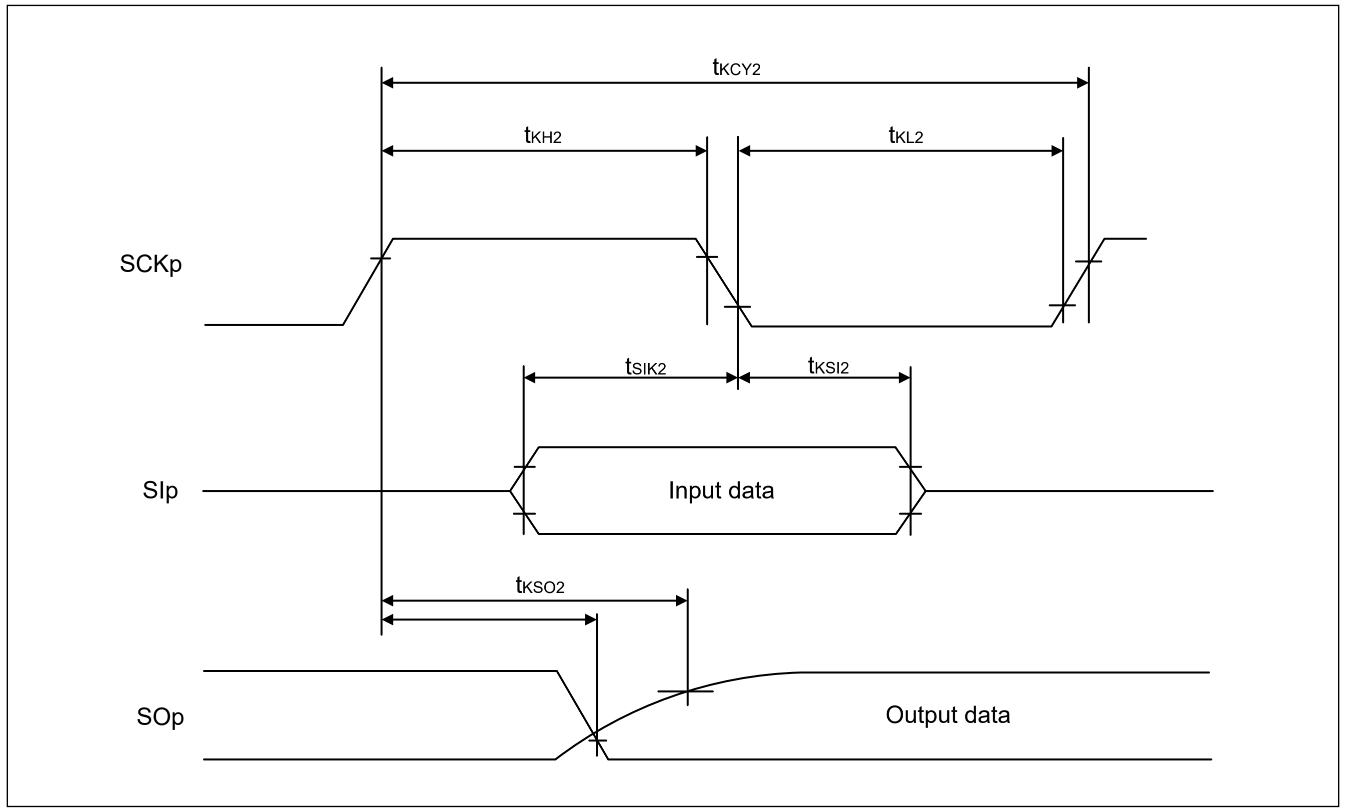


Figure 2.27 Timing of serial transfer in the simplified SPI communications in the slave mode with devices operating at different voltage levels when SCRmn.DCP[1:0] = 01b or 10b

Note:
- p: Simplified SPI number (p = 00, 11), m: Unit number, n: Channel number (mn = 00, 03), gh: Port number (gh = 100 to 102, 108 to 110, 112, 201, 212, 213)
- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

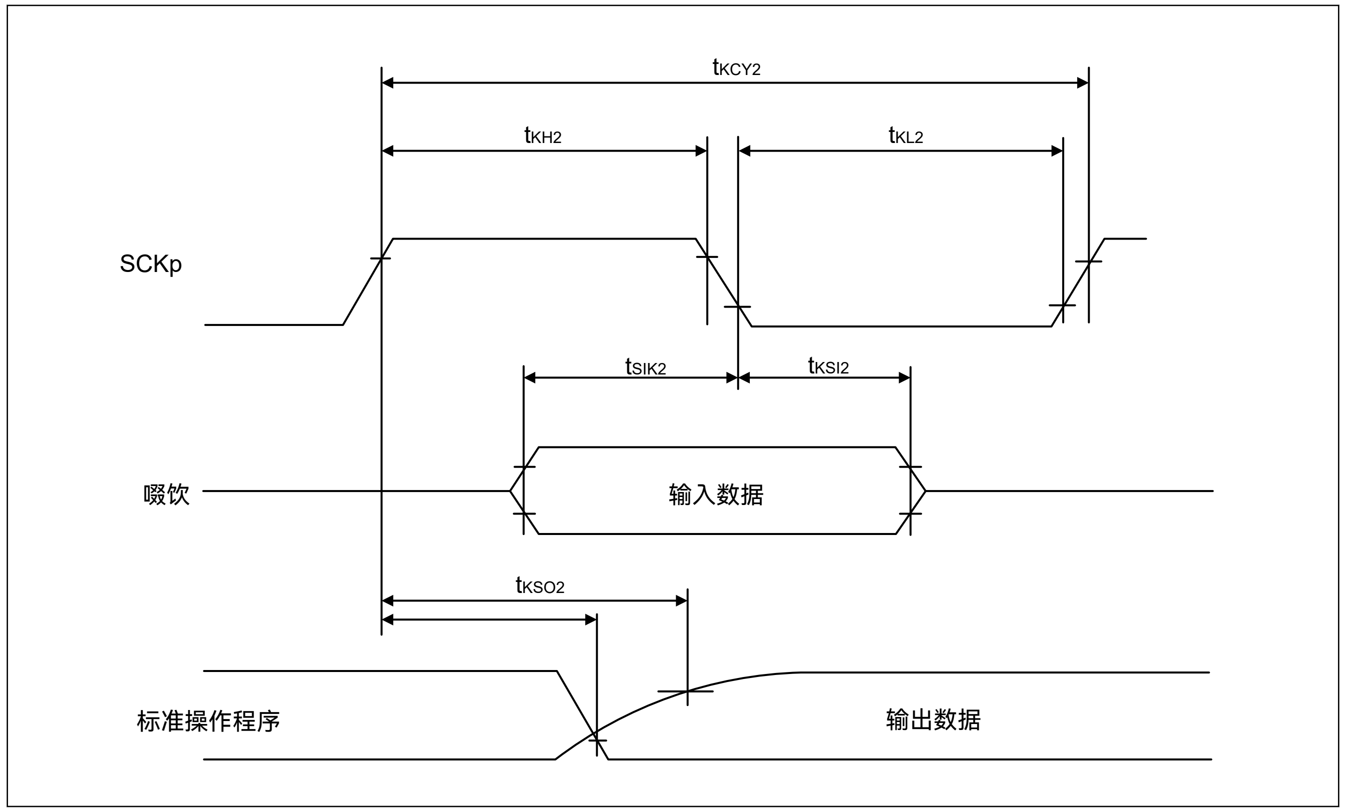


图 2.27 简化 SPI 通信中从模式下串行传输的时序，其中器件工作在不同电压电平，当 SCRmn.DCP[1:0] = 01b 或 10b

注：●p：简化的SPI编号(p = 00，11），m：单元编号，n：通道编号(mn = 00, 03），gh：端口编号(gh =（100至102，108至110，112，201，212，213）

●由于 P212PFS_A 和 P213PFS_A 寄存器没有 PIM 位，因此无法使用 P212 和 P213 与工作电压不同的设备进行通信。

Table 2.33 Simplified IIC communications with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) (1 of 2)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
SCLr clock frequency	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	f_{SCL}	—	1000[*1]	—	1000[*1]	—	300[*1]	kHz	Figure 2.29
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		—	1000[*1]	—	1000[*1]	—	300[*1]	kHz	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		—	400[*1]	—	400[*1]	—	300[*1]	kHz	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		—	400[*1]	—	400[*1]	—	300[*1]	kHz	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 100 pF, R_b = 5.5 kΩ		—	300[*1]	—	300[*1]	—	300[*1]	kHz	
Hold time when SCLr is low	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	t_{LOW}	475	—	475	—	1550	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		475	—	475	—	1550	—	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		1150	—	1550	—	1550	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		1150	—	1550	—	1550	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 100 pF, R_b = 5.5 kΩ		1550	—	1550	—	1550	—	ns	
Hold time when SCLr is high	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	t_{HIGH}	245	—	245	—	610	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		200	—	200	—	610	—	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		675	—	675	—	610	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		600	—	600	—	610	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 100 pF, R_b = 5.5 kΩ		610	—	610	—	610	—	ns	

表 2.33 简化的 IIC 通信，适用于工作电压不同的设备（1.8 V、2.5 V 或 3V）。V）（1/2）

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

范围		象征	高速模式		中速模式		低速模式		单元	测试条件
			最小。	最大限度。	最小。	最大限度。	最小。	最大限度。		
SCLr 时钟频率	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V， Cb= 50 pF，Rb= 20.7 kΩ	f_{SCL}	—	1000[*1]	—	1000[*1]	—	300[*1]	kHz	图 2.29
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V， Cb= 50 pF， R_b = 2.7 kΩ		—	1000[*1]	—	1000[*1]	—	300[*1]	kHz	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V， Cb= 100 pF， R_b = 2.8 kΩ		—	400[*1]	—	400[*1]	—	300[*1]	kHz	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V， Cb= 100 pF， R_b = 2.7 kΩ		—	400[*1]	—	400[*1]	—	300[*1]	kHz	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*2, Cb= 100 pF， R_b = 5.5 kΩ		—	300[*1]	—	300[*1]	—	300[*1]	kHz	
保持时间 SCLr 低	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50pF， R_b = 2.7 kΩ	低	475	—	475	—	1550	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50pF， R_b = 2.7 kΩ		475	—	475	—	1550	—	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF， R_b = 2.8 kΩ		1150	—	1550	—	1550	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V， Cb= 100 pF， R_b = 2.7 kΩ		1150	—	1550	—	1550	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*2, C_b = 100 pF， R_b = 5.5 kΩ		1550	—	1550	—	1550	—	ns	
保持时间 SCLr 值高	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50pF， R_b = 2.7 kΩ	大腿	245	—	245	—	610	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V， C_b = 50pF， R_b = 2.7 kΩ		200	—	200	—	610	—	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF， R_b = 2.8 kΩ		675	—	675	—	610	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V， Cb= 100 pF， R_b = 2.7 kΩ		600	—	600	—	610	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*2, Cb= 100 pF， R_b = 5.5 kΩ		610	—	610	—	610	—	ns	

Table 2.33 Simplified IIC communications with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) (2 of 2)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
Data setup time (reception)	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	$t_{SU:DAT}$	$1/f_{MCK}$ + 135*3	—	$1/f_{MCK}$ + 135*3	—	$1/f_{MCK}$ + 190*3	—	ns	Figure 2.29
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		$1/f_{MCK}$ + 135*3	—	$1/f_{MCK}$ + 135*3	—	$1/f_{MCK}$ + 190*3	—	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		$1/f_{MCK}$ + 190*3	—	$1/f_{MCK}$ + 190*3	—	$1/f_{MCK}$ + 190*3	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		$1/f_{MCK}$ + 190*3	—	$1/f_{MCK}$ + 190*3	—	$1/f_{MCK}$ + 190*3	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*2, C_b = 100 pF, R_b = 5.5 kΩ		$1/f_{MCK}$ + 190*3	—	$1/f_{MCK}$ + 190*3	—	$1/f_{MCK}$ + 190*3	—	ns	
Data hold time (transmission)	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	$t_{HD:DAT}$	0	305	0	305	0	305	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		0	305	0	305	0	305	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		0	355	0	355	0	355	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		0	355	0	355	0	355	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V*2, C_b = 100 pF, R_b = 5.5 kΩ		0	405	0	405	0	405	ns	

Note 1. The listed times must be no greater than $f_{MCK}/4$.
Note 2. Use this setting with VCC ≥ V_b.
Note 3. Set f_{MCK} so that it does not exceed the hold time when SCLr is low or high.

Note: Select the TTL input buffer and the N-ch open drain output [withstand voltage of VCC] mode for the SDAr pin and the N-ch open drain output [withstand voltage of VCC] mode for the SCLr pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

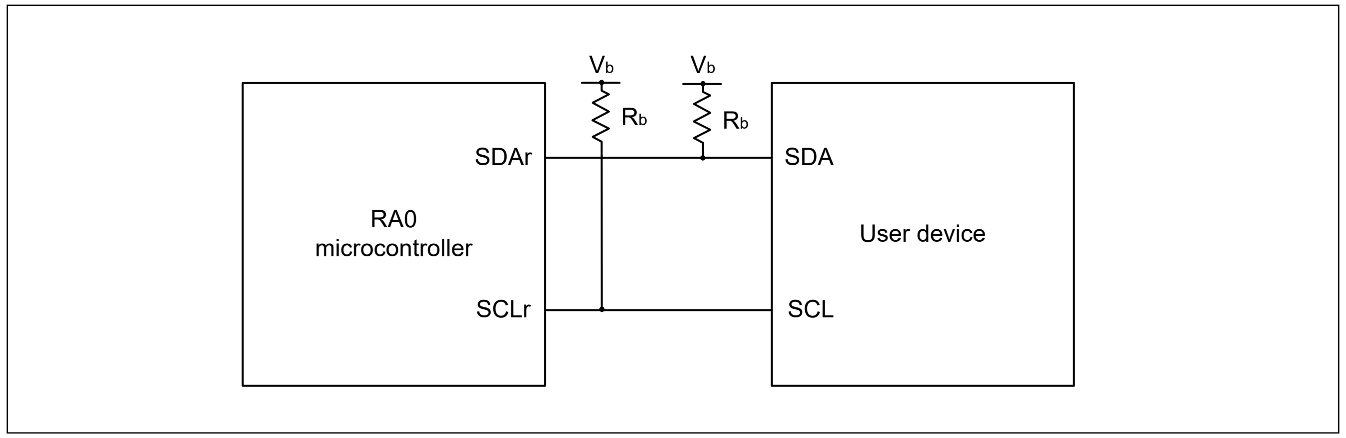


Figure 2.28 Connection in the IIC communications with devices operating at different voltage levels

表 2.33 简化的 IIC 通信，适用于工作电压不同的设备(1.8 V, 2.5 V, 或 3 V) (2/2)

条件：VCC = 1.8至 5.5 V，VSS= 0 V，Ta= -40 至+125°C

范围		象征	高速模式		中速模式		低速模式		单元	测试条件
			最小。	最大限	最小。	最大限	最小。	最大限		
数据建立时间（接收）	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V, Cb= 50 pF, R_b = 2.7 kΩ	TSU:DAT	$1/f_{MCK}$ + 135*3	度。	$1/f_{MCK}$ + 135*3	度。	$1/f_{MCK}$ + 190*3	度。	ns	图 2.29
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V, Cb= 50 pF, R_b = 2.7 kΩ		$1/f_{MCK}$ + 135*3	—	$1/f_{MCK}$ + 135*3	—	$1/f_{MCK}$ + 190*3	—	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7V≤ Vb≤ 4.0V, Cb= 100 pF, R_b = 2.8 kΩ		$1/f_{MCK}$ + 190*3	—	$1/f_{MCK}$ + 190*3	—	$1/f_{MCK}$ + 190*3	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V, Cb= 100 pF, R_b = 2.7 kΩ		$1/f_{MCK}$ + 190*3	—	$1/f_{MCK}$ + 190*3	—	$1/f_{MCK}$ + 190*3	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*2, Cb= 100 pF, R_b = 5.5 kΩ		$1/f_{MCK}$ + 190*3	—	$1/f_{MCK}$ + 190*3	—	$1/f_{MCK}$ + 190*3	—	ns	
数据保持时间（传输）	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50pF, R_b = 2.7 kΩ	$t_{HD:DAT}$	0	305	0	305	0	305	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50pF, R_b = 2.7 kΩ		0	305	0	305	0	305	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		0	355	0	355	0	355	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3V≤ Vb≤ 2.7V, Cb= 100 pF, R_b = 2.7 kΩ		0	355	0	355	0	355	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6V≤ Vb≤ 2.0V*2, C_b = 100 pF, R_b = 5.5 kΩ		0	405	0	405	0	405	ns	

注1.所列时间不得大于$f_{MCK}/4$。
注2. 将此设置与VCC ≥ V_b一起使用。
注 3. 设置 fMCK，使其在 SCLr 低或高时不超过保持时间。

注意：使用端口gh引脚功能选择寄存器（PghPFS_A.PIM和PghPFS_A.NCODR）为SDAr引脚选择TTL输入缓冲器和N沟道开漏输出[耐压] 模式，为SCLr引脚选择N沟道开漏输出[耐压] 模式。对于V_{IH}和V_{IL}，请参阅选择TTL输入缓冲器时的直流特性。

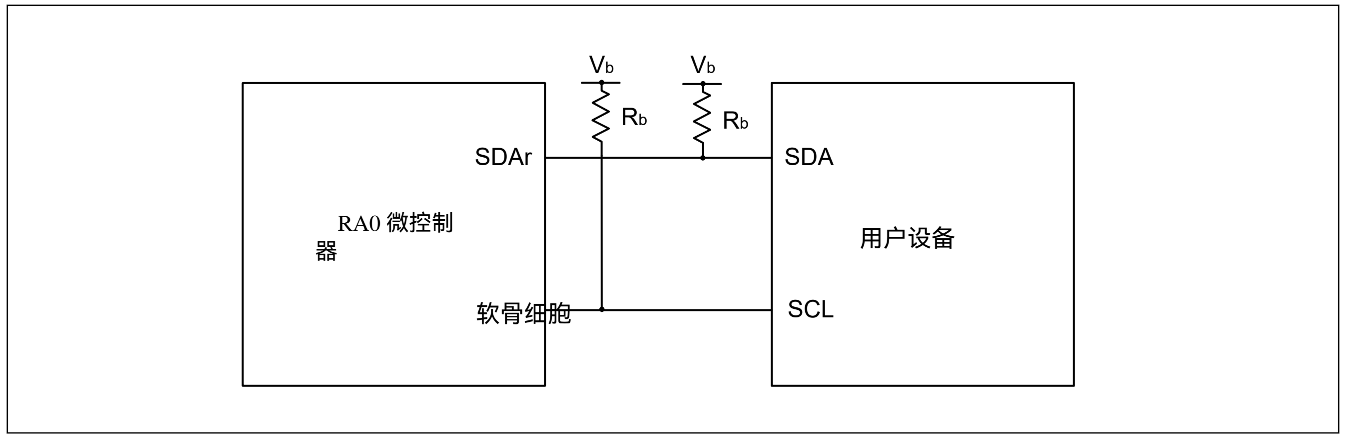


图 2.28 IIC 通信中与不同电压等级设备的连接

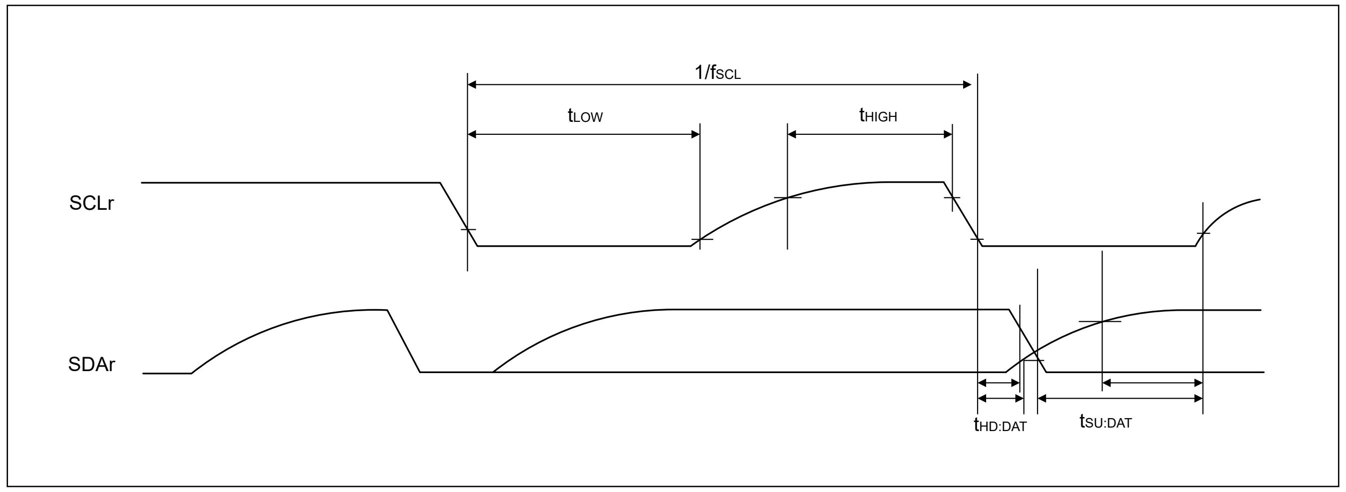


Figure 2.29 Timing of serial transfer in simplified IIC communications with devices operating at different voltage levels

Note:
- R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage
- r: Simplified IIC number (r = 00, 11), gh: Port number (gh = 100, 102, 110, 112, 201, 212)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03)

2.5.2 I^{2}C Bus Interface (IICA)

Table 2.34 I^{2}C standard mode

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
SCLAn clock frequency	Standard mode: PCLKB ≥ 1 MHz	f_{SCL}	0	—	100	kHz	Figure 2.30
Setup time of restart condition	—	$t_{SU:STA}$	4.7	—	—	μs	
Hold time[*1]	—	$t_{HD:STA}$	4	—	—	μs	
Hold time when SCLAn is low	—	t_{LOW}	4.7	—	—	μs	
Hold time when SCLAn is high	—	t_{HIGH}	4	—	—	μs	
Data setup time (reception)	—	$t_{SU:DAT}$	250	—	—	ns	
Data hold time (transmission)[*2]	—	$t_{HD:DAT}$	0	—	3.45	μs	
Setup time of stop condition	—	$t_{SU:STO}$	4	—	—	μs	
Bus-free time	—	t_{BUF}	4.7	—	—	μs	

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.
Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Note: n: Unit number (0)

Note: Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Note: The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.

C_b = 400 pF, R_b = 2.7 kΩ

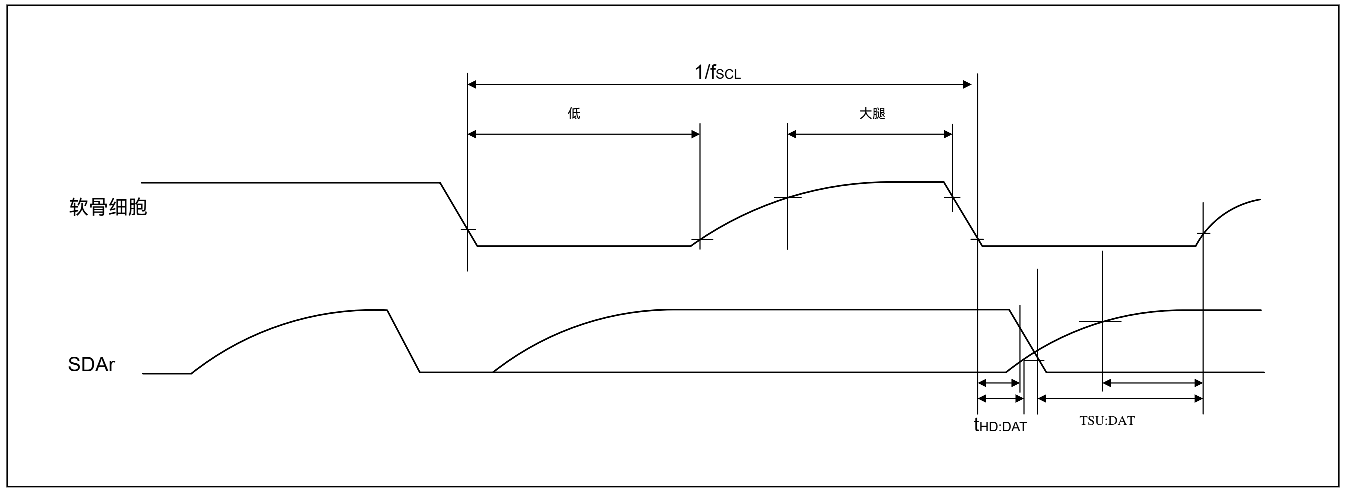


图 2.29 简化 IIC 通信中，不同电压电平器件的串行传输时序

注：●R_b[Ω]: 通信线路（SDAr、SCLr）上拉电阻，C_b[F]: 通信线路（SDAr、SCLr）负载电容，V_b[V]: 通信线路电压

●r：简化的 IIC 号码(r = 00，11），gh：端口号(gh = 100, 102，110、112、201、212）
●fMCK：串行阵列单元操作时钟频率
要设置此工作时钟，请使用串行模式寄存器 mn (SMRmn) 中的 CKS 位。
m：单元编号，n：通道编号(mn = 00，03）

2.5.2I^{2}C总线接口（IICA）

表 2.34I^{2}C 标准模式

条件：VCC = 1.6至5.5 V, VSS= 0 V，Ta = -40 至+125°C

范围		象征	最小。	类型。	最大限度	单元	测试条件
SCLAn 时钟频率	标准模式：PCLKB≥ 1 MHz	f_{SCL}	0	—	100	kHz	图 2.30
重启条件的设置时间	—	津苏:STA	4.7	—	—	μs	
保持时间*1	—	$t_{HD:STA}$	4	—	—	μs	
SCLAn 低时的保持时间	—	低	4.7	—	—	μs	
SCLAn 高的保持时间	—	大腿	4	—	—	μs	
数据建立时间（接收）	—	TSU:DAT	250	—	—	ns	
数据保持时间（传输）*2	—	$t_{HD:DAT}$	0	—	3.45	μs	
停止条件的设置时间	—	津：STO	4	—	—	μs	
无公交时间	—	t_{BUF}	4.7	—	—	μs	

注1. 第一个时钟脉冲是在此周期之后，当检测到启动或重启条件时产生的。
注2：$t_{HD:DAT}$的最大值适用于正常传输。时钟拉伸将在收到确认 (ACK) 信号时插入。

注：n：单元编号（0）

注意：由于 P212PFS_A 和 P213PFS_A 寄存器没有 PIM 位，因此无法使用 P212 和 P213 与工作电压不同的设备进行通信。

注意：通信线路电容(C_b) 和通信线路上拉电阻(R_b)的最大值如下。

C_b = 400 pF, R_b = 2.7 kΩ

Table 2.35 I²C fast mode

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
SCLAn clock frequency	Fast mode: PCLKB ≥ 3.5 MHz 1.8 V ≤ VCC ≤ 5.5 V	f_{SCL}	0	—	400	kHz	Figure 2.30
Setup time of restart condition	1.8 V ≤ VCC ≤ 5.5 V	$t_{SU:STA}$	0.6	—	—	μs	
Hold time*1	1.8 V ≤ VCC ≤ 5.5 V	$t_{HD:STA}$	0.6	—	—	μs	
Hold time when SCLAn is low	1.8 V ≤ VCC ≤ 5.5 V	t_{LOW}	1.3	—	—	μs	
Hold time when SCLAn is high	1.8 V ≤ VCC ≤ 5.5 V	t_{HIGH}	0.6	—	—	μs	
Data setup time (reception)	1.8 V ≤ VCC ≤ 5.5 V	$t_{SU:DAT}$	100	—	—	ns	
Data hold time (transmission)*2	1.8 V ≤ VCC ≤ 5.5 V	$t_{HD:DAT}$	0	—	0.9	μs	
Setup time of stop condition	1.8 V ≤ VCC ≤ 5.5 V	$t_{SU:STO}$	0.6	—	—	μs	
Bus-free time	1.8 V ≤ VCC ≤ 5.5 V	t_{BUF}	1.3	—	—	μs	

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.
Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Note: Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Note: The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.

C_b = 320 pF, R_b = 1.1 kΩ

Table 2.36 I²C fast mode plus

Conditions: VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
SCLAn clock frequency	Fast mode plus: PCLKB ≥ 10 MHz 2.7 V ≤ VCC ≤ 5.5 V	f_{SCL}	0	—	1000	kHz	Figure 2.30
Setup time of restart condition	2.7 V ≤ VCC ≤ 5.5 V	$t_{SU:STA}$	0.26	—	—	μs	
Hold time*1	2.7 V ≤ VCC ≤ 5.5 V	$t_{HD:STA}$	0.26	—	—	μs	
Hold time when SCLAn is low	2.7 V ≤ VCC ≤ 5.5 V	t_{LOW}	0.5	—	—	μs	
Hold time when SCLAn is high	2.7 V ≤ VCC ≤ 5.5 V	t_{HIGH}	0.26	—	—	μs	
Data setup time (reception)	2.7 V ≤ VCC ≤ 5.5 V	$t_{SU:DAT}$	50	—	—	ns	
Data hold time (transmission)*2	2.7 V ≤ VCC ≤ 5.5 V	$t_{HD:DAT}$	0	—	0.45	μs	
Setup time of stop condition	2.7 V ≤ VCC ≤ 5.5 V	$t_{SU:STO}$	0.26	—	—	μs	
Bus-free time	2.7 V ≤ VCC ≤ 5.5 V	t_{BUF}	0.5	—	—	μs	

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.
Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Note: Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Note: The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.

C_b = 120 pF, R_b = 1.1 kΩ

表 2.35I²C 快速模式

条件：VCC = 1.8至5.5 V, VSS= 0V，Ta= -40 至+125°C

范围		象征	最小。	类型。	最大限度。	单元	测试条件
SCLAn 时钟频率	快速模式：PCLKB≥ 3.5 MHz 1.8 V ≤ VCC ≤ 5.5 V	f_{SCL}	0	—	400	kHz	图 2.30
重启条件的设置时间	1.8 V ≤ VCC ≤ 5.5 V	津苏:STA	0.6	—	—	μs	
保持时间*1	1.8 V ≤ VCC ≤ 5.5 V	$t_{HD:STA}$	0.6	—	—	μs	
SCLAn 低时的保持时间	1.8 V ≤ VCC ≤ 5.5 V	低	1.3	—	—	μs	
SCLAn 高的保持时间	1.8 V ≤ VCC ≤ 5.5 V	t_{HIGH}	0.6	—	—	μs	
数据建立时间（接收）	1.8 V ≤ VCC ≤ 5.5 V	TSU:DAT	100	—	—	ns	
数据保持时间（传输）*2	1.8 V ≤ VCC ≤ 5.5 V	$t_{HD:DAT}$	0	—	0.9	μs	
停止条件的设置时间	1.8 V ≤ VCC ≤ 5.5 V	津：STO	0.6	—	—	μs	
无公交时间	1.8 V ≤ VCC ≤ 5.5 V	t_{BUF}	1.3	—	—	μs	

注1. 第一个时钟脉冲是在此周期之后，当检测到启动或重启条件时产生的。
注2：$t_{HD:DAT}$的最大值适用于正常传输。时钟拉伸将在收到确认 (ACK) 信号时插入。

注意：由于 P212PFS_A 和 P213PFS_A 寄存器没有 PIM 位，因此无法使用 P212 和 P213 与工作电压不同的设备进行通信。

注意：通信线路电容(C_b) 和通信线路上拉电阻(R_b)的最大值如下。

C_b = 320 pF, R_b = 1.1 kΩ

表 2.36I²C 快速模式加

条件：VCC = 2.7至5.5 V, VSS = 0 V，Ta = -40 至+125°C

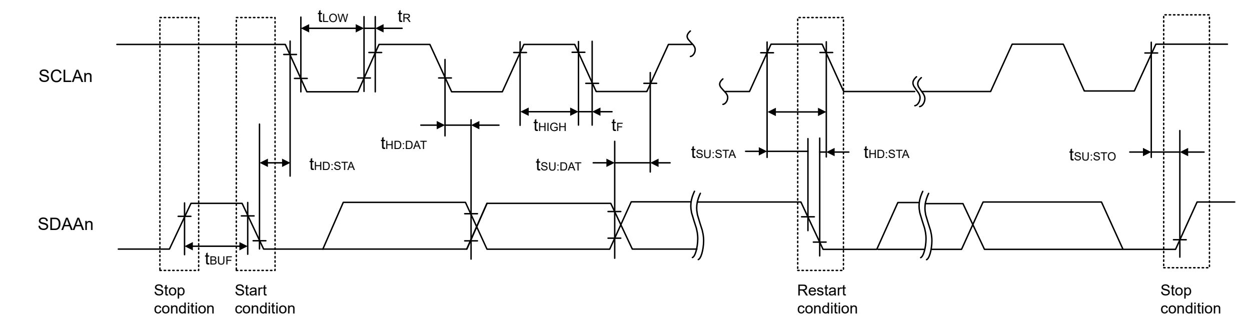
范围		象征	最小。	类型。	最大限度。	单元	测试条件
SCLAn 时钟频率	快速模式增强：PCLKB≥ 10 MHz 2.7 V ≤ VCC ≤ 5.5 V	f_{SCL}	0	—	1000	kHz	图 2.30
重启条件的设置时间	2.7 V ≤ VCC ≤ 5.5 V	津苏:STA	0.26	—	—	μs	
保持时间*1	2.7 V ≤ VCC ≤ 5.5 V	$t_{HD:STA}$	0.26	—	—	μs	
SCLAn 低时的保持时间	2.7 V ≤ VCC ≤ 5.5 V	低	0.5	—	—	μs	
SCLAn 高的保持时间	2.7 V ≤ VCC ≤ 5.5 V	大腿	0.26	—	—	μs	
数据建立时间（接收）	2.7 V ≤ VCC ≤ 5.5 V	TSU:DAT	50	—	—	ns	
数据保持时间（传输）*2	2.7 V ≤ VCC ≤ 5.5 V	$t_{HD:DAT}$	0	—	0.45	μs	
停止条件的设置时间	2.7 V ≤ VCC ≤ 5.5 V	津：STO	0.26	—	—	μs	
无公交时间	2.7 V ≤ VCC ≤ 5.5 V	t_{BUF}	0.5	—	—	μs	

注1. 第一个时钟脉冲是在此周期之后，当检测到启动或重启条件时产生的。
注2：tHD:DAT的最大值适用于正常传输。时钟拉伸将在收到确认（ACK）信号时插入。

注意：由于 P212PFS_A 和 P213PFS_A 寄存器没有 PIM 位，因此无法使用 P212 和 P213 与工作电压不同的设备进行通信。

注意：通信线路电容(C_b) 和通信线路上拉电阻(R_b)的最大值如下。

C_b = 120 pF, R_b = 1.1 kΩ



Note: n = 0

Figure 2.30 IICA serial transfer timing

2.6 Analog Characteristics

2.6.1 A/D Converter Characteristics for T_A = -40 to +85°C

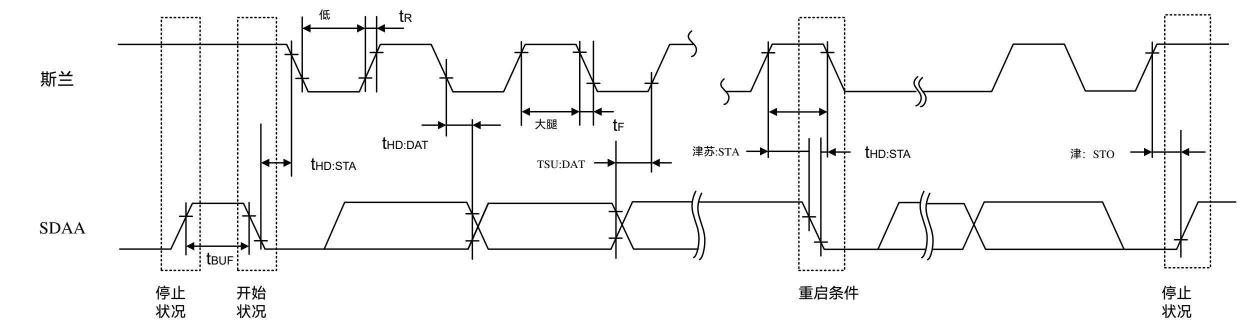
Table 2.37 Reference for the characteristics of the A/D converter

Input channel	Reference Voltage		
	Reference voltage (+) = VREFH0 Reference voltage (–) = VREFL0	Reference voltage (+) = VCC Reference voltage (–) = VSS	Reference voltage (+) = V_{BGR} Reference voltage (–) = VREFL0
AN000, AN001, AN004, AN005	Refer to Table 2.38.	Refer to Table 2.40.	Refer to Table 2.41.
AN021, AN022	Refer to Table 2.39.		
Internal reference voltage Temperature sensor output voltage	Refer to Table 2.38.		—

Table 2.38 A/D conversion characteristics (AN004, AN005, internal reference voltage, and temperature sensor output voltage) (1 of 2)

Conditions: 1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).
Target pins: AN004, AN005, internal reference voltage, and temperature sensor output voltage
(Reference voltage (+) = VREFH0, Reference voltage (–) = VREFL0 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Resolution	RES	8	—	10	bit	—	
Overall error*1*2*3	AINL	—	1.2	±3.5	LSB	10-bit resolution VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	1.2	±7.0	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V*6



笔记: n = 0

图 2.30 IICA 串行传输时序

2.6 Analog Characteristics

2.6.1 T_A = -40 至+85°C的 A/D 转换器特性

表 2.37 A/D 转换器特性参考

输入通道	参考电压		
	参考电压(+) = VREFH0 参考电压(–) = VREFL0	参考电压(+) = VCC 参考电压(–) = VSS	参考电压(+) = V_{BGR} 参考电压(–) = VREFL0
AN000、AN001、AN004、AN005	请参阅表 2.38。	请参阅表 2.40。	请参阅表 2.41。
AN021, AN022	请参阅表 2.39。		
内部参考电压温度传感器输出电压	请参阅表 2.38。		—

表 2.38 A/D 转换特性（AN004、AN005、内部参考电压和温度传感器输出电压）（1/2）

条件：1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
参考电压范围应用于 VREFH0 (ADREFP[1:0] = 01b) 和 VREFL0 (ADREFM= 1b)。
目标引脚：AN004、AN005、内部参考电压和温度传感器输出电压
（参考电压(+) = VREFH0, 参考电压(–) = VREFL0 = 0 V）

范围	象征	最小。	类型。	最大限度。	单元	状况	
解决	RES	8	—	10	少量	—	
全面的错误*1*2*3	AINL	—	1.2	±3.5	LSB	10 位分辨率 VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	1.2	±7.0	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V*6

Table 2.38 A/D conversion characteristics (AN004, AN005, internal reference voltage, and temperature sensor output voltage) (2 of 2)

Conditions: 1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).
Target pins: AN004, AN005, internal reference voltage, and temperature sensor output voltage
(Reference voltage (+) = VREFH0, Reference voltage (–) = VREFL0 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Conversion time	tCONV	2.125	—	39	µs	10-bit resolution Target pin: AN004, AN005	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	µs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	µs		1.8 V ≤ VCC ≤ 5.5 V
		57	—	95	µs		1.6 V ≤ VCC ≤ 5.5 V
		2.375	—	39	µs	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage	3.6 V ≤ VCC ≤ 5.5 V
		3.5625	—	39	µs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	µs		1.8 V ≤ VCC ≤ 5.5 V
Zero-scale error*1*2*3*4	E_{ZS}	—	—	±0.25	%FSR	10-bit resolution VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±0.50	%FSR		1.6 V ≤ VREFH0 ≤ 5.5 V*6
Full-scale error*1*2*3*4	E_{FS}	—	—	±0.25	%FSR	10-bit resolution VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±0.50	%FSR		1.6 V ≤ VREFH0 ≤ 5.5 V*6
Integral linearity error*1*2*3	ILE	—	—	±2.5	LSB	10-bit resolution VREFH0 = VCC*5	1.8 V ≤ VREFH0≤ 5.5 V
		—	—	±5.0	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V*6
Differential linearity error*1*2*3	DLE	—	—	±1.5	LSB	10-bit resolution VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±2.0	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V*6
Analog input voltage	V_{AIN}	0	—	VREFH0	V	AN004, AN005	
		V_{BGR}*7			V	Internal reference voltage (1.8 V ≤ VCC ≤ 5.5 V)	
		V_{TMPS25}*7			V	Temperature sensor output voltage (1.8 V ≤ VCC ≤ 5.5 V)	

Note 1. The Typ. value is an average value at TA = 25°C. The Max. value is an average value ±3σ at normal distribution.
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
Note 3. This value does not include the quantization error (±1/2 LSB).
Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 5. When VREFH0 < VCC, the maximum values are as follows.

表 2.38 A/D 转换特性（AN004、AN005、内部参考电压和温度传感器输出电压）（2/2）

条件：1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).
目标引脚：AN004、AN005、内部参考电压和温度传感器输出电压
（参考电压(+) = VREFH0, 参考电压(–) = VREFL0 = 0 V）

范围	象征	最小。	类型。	最大限度。	单元	状况	
转换时间	tCONV	2.125	—	39	µs	10 位分辨率 目标引脚：AN004, AN005	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	µs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	µs		1.8 V ≤ VCC ≤ 5.5 V
		57	—	95	µs		1.6 V ≤ VCC ≤ 5.5 V
		2.375	—	39	µs	10 位分辨率 目标引脚：内部参考 电压和温度传感器输出电压	3.6 V ≤ VCC ≤ 5.5 V
		3.5625	—	39	µs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	µs		1.8 V ≤ VCC ≤ 5.5 V
零尺度错误*1*2*3*4	E_{ZS}	—	—	±0.25	%FSR	10 位分辨率 VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±0.50	%FSR		1.6 V ≤ VREFH0 ≤ 5.5 V*6
全面错误*1*2*3*4	E_{FS}	—	—	±0.25	%FSR	10 位分辨率 VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±0.50	%FSR		1.6 V ≤ VREFH0 ≤ 5.5 V*6
积分线性错误*1*2*3	ILE	—	—	±2.5	LSB	10 位分辨率 VREFH0 = VCC*5	1.8 V ≤ VREFH0≤ 5.5 V
		—	—	±5.0	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V*6
微分线性错误*1*2*3	DLE	—	—	±1.5	LSB	10 位分辨率 VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±2.0	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V*6
模拟输入电压	V_{AIN}	0	—	VREFH0	V	AN004, AN005	
		V_{BGR}*7			V	内部参考电压 (1.8 V ≤ VCC ≤ 5.5 V)	
		V_{TMPS25}*7			V	温度传感器输出电压 (1.8 V ≤ VCC ≤ 5.5 V)	

注 1. 典型值是TA = 25°C. 处的平均值，最大值是±3σ处的平均值。
注2. 这些数值是特性评估的结果，并非出货时的检查值。
注3.此值不包括量化误差(±1/2 LSB)。
注 4. 此值表示为(%FSR) 与满量程值的比率。
注5. 当VREFH0 < VCC, 时，最大值如下。

- Overall error: Add ± 1.0 LSB to the maximum value when VCC = VREFH0.
- Zero-scale/full-scale error: Add ±0.05%FSR to the maximum value when VCC = VREFH0.
- Integral linearity error and differential linearity error: Add ±0.5 LSB to the maximum value when VCC = VREFH0.

Note 6. The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57 μs and 95 μs.
Note 7. See section 2.6.3. Temperature Sensor/Internal Reference Voltage Characteristics.

Table 2.39 A/D conversion characteristics (AN021 to AN022)

Conditions: 1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).
Target pins: AN021 to AN022
(Reference voltage (+) = VREFH0, Reference voltage (–) = VREFL0 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Resolution	RES	8	—	10	bit	—	
Overall error*1*2*3	AINL	—	1.2	±5.0	LSB	10-bit resolution VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	1.2	±8.5	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V*6
Conversion time	tCONV	2.125	—	39	μs	10-bit resolution Target pin: AN021, AN022	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		1.8 V ≤ VCC ≤ 5.5 V
		57	—	95	μs		1.6 V ≤ VCC ≤ 5.5 V
Zero-scale error*1*2*3*4	E_{ZS}	—	—	±0.35	%FSR	10-bit resolution VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±0.60	%FSR		1.6 V ≤ VREFH0 ≤ 5.5 V*6
Full-scale error*1*2*3*4	E_{FS}	—	—	±0.35	%FSR	10-bit resolution VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±0.60	%FSR		1.6 V ≤ VREFH0 ≤ 5.5 V*6
Integral linearity error*1*2*3	ILE	—	—	±3.5	LSB	10-bit resolution VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±6.0	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V*6
Differential linearity error*1*2*3	DLE	—	—	±2.0	LSB	10-bit resolution VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±2.5	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V*6
Analog input voltage	V_{AIN}	0	—	VREFH0	V	AN021, AN022	

Note 1. The Typ. value is an average value at TA = 25°C. The Max. value is an average value ±3σ at normal distribution.
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
Note 3. This value does not include the quantization error (±1/2 LSB).
Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 5. When VREFH0 < VCC, the maximum values are as follows.

- Overall error: Add ± 1.0 LSB to the maximum value when VCC = VREFH0.

- 总体误差：当VCC = VREFH0时，将± 1.0 LSB添加到最大值。
- 零刻度/满刻度误差：当VCC = VREFH0时，将±0.05%FSR加到最大值。
- 积分线性误差和微分线性误差：当 VCC= VREFH0 时，将±0.5LSB 加到最大值。

注6：所列值适用于最大和最小转换时间值分别设置为57 μs和95 μs的情况。
注7.参见2.6.3节。温度传感器/内部参考电压特性。

表 2.39 A/D 转换特性（AN021 至 AN022）

条件：1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V，Ta = -40至+85°C
Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).
Target pins: AN021 to AN022
（参考电压(+) = VREFH0, 参考电压(–) = VREFL0 = 0 V)

范围	象征	最小。	类型。	最大限度。	单元	状况	
解决	RES	8	—	10	少量	—	
全面的 错误*1*2*3	AINL	—	1.2	±5.0	LSB	10 位分辨率 VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	1.2	±8.5	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V*6
转换时间	tCONV	2.125	—	39	μs	10 位分辨率 目标引脚：AN021, AN022	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		1.8 V ≤ VCC ≤ 5.5 V
		57	—	95	μs		1.6 V ≤ VCC ≤ 5.5 V
零尺度 错误*1*2*3*4	E_{ZS}	—	—	±0.35	%FSR	10 位分辨率 VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±0.60	%FSR		1.6 V ≤ VREFH0 ≤ 5.5 V*6
全面 错误*1*2*3*4	E_{FS}	—	—	±0.35	%FSR	10 位分辨率 VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±0.60	%FSR		1.6 V ≤ VREFH0 ≤ 5.5 V*6
积分线性 错误*1*2*3	ILE	—	—	±3.5	LSB	10 位分辨率 VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±6.0	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V*6
微分线性 错误*1*2*3	DLE	—	—	±2.0	LSB	10 位分辨率 VREFH0 = VCC*5	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±2.5	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V*6
模拟输入电压	V_{AIN}	0	—	VREFH0	V	AN021, AN022	

注 1. 典型值是TA = 25°C. 处的平均值，最大值是±3σ处的平均值。
注2. 这些数值是特性评估的结果，并非出货时的检查值。
注3.此值不包括量化误差(±1/2 LSB)。
注 4. 此值表示为(%FSR)与满量程值的比率。
注5. 当VREFH0 < VCC时，最大值如下。

- 总体误差：当VCC = VREFH0时，将± 1.0 LSB添加到最大值。

- Zero-scale/full-scale error: Add ±0.05% FSR to the maximum value when VCC = VREFH0.
- Integral linearity error/differential linearity error: Add ±0.5 LSB to the maximum value when VCC = VREFH0.

Note 6. The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57 μs and 95 μs.

Table 2.40 A/D conversion characteristics (AN000, AN001, AN004, AN005, AN021, AN022, internal reference voltage, and temperature sensor output voltage) (1 of 2)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
Reference voltage range applied to the VCC (ADREFP[1:0] = 00b) and VSS (ADREFM = 0b).
Target pins: AN000, AN001, AN004, AN005, AN021, AN022, internal reference voltage[*7], and temperature sensor output voltage[*7]
(Reference voltage (+) = VCC, Reference voltage (–) = VSS)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Resolution	RES	8	—	10	bit	—	
Overall error[*1*2*3]	AINL	—	1.2	±7.0	LSB	10-bit resolution	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	1.2	±10.5	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V[*5]
Conversion time	tCONV	2.125	—	39	μs	10-bit resolution Target pin: AN000, AN001, AN004, AN005, AN021, AN022	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		1.8 V ≤ VCC ≤ 5.5 V
		57	—	95	μs		1.6 V ≤ VCC ≤ 5.5 V
		2.375	—	39	μs	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage	3.6 V ≤ VCC ≤ 5.5 V
		3.5625	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		1.8 V ≤ VCC ≤ 5.5 V
Zero-scale error[*1*2*3*4]	E_{ZS}	—	—	±0.60	%FSR	10-bit resolution	1.8 V ≤ VCC ≤ 5.5 V
		—	—	±0.85	%FSR		1.6 V ≤ VCC ≤ 5.5 V[*5]
Full-scale error[*1*2*3*4]	E_{FS}	—	—	±0.60	%FSR	10-bit resolution	1.8 V ≤ VCC ≤ 5.5 V
		—	—	±0.85	%FSR		1.6 V ≤ VCC ≤ 5.5 V[*5]
Integral linearity error[*1*2*3]	ILE	—	—	±4.0	LSB	10-bit resolution	1.8 V ≤ VCC ≤ 5.5 V
		—	—	±6.0	LSB		1.6 V ≤ VCC ≤ 5.5 V[*5]
Differential linearity error[*1*2*3]	DLE	—	—	±2.0	LSB	10-bit resolution	1.8 V ≤ VCC ≤ 5.5 V
		—	—	±2.5	LSB		1.6 V ≤ VCC ≤ 5.5 V[*5]

●零刻度/满刻度误差：当VCC = VREFH0时，将±0.05%FSR 加到最大值上

●积分线性误差/微分线性误差：当 VCC=VREFH0 时，将±0.5 LSB 加到最大值。

注6：所列值适用于最大和最小转换时间值分别设置为57 μs和95 μs的情况。

表 2.40 A/D 转换特性（AN000、AN001、AN004、AN005、AN021、AN022、内部参考电压和温度传感器输出电压）（1/2）

条件：1.6 V ≤ VCC ≤ 5.5 V VSS = 0 V Ta = -40 至+85°C
应用于 VCC (ADREFP[1:0] = 00b)) 和 VSS (ADREFM= 0b) 的参考电压范围。
目标引脚：AN000、AN001、AN004、AN005、AN021、AN022、内部参考电压*7 和温度传感器输出电压*7
（参考电压(+) = VCC，参考电压(–) = VSS)）

范围	象征	最小。	类型。	最大限度。	单元	状况	
解决	RES	8	—	10	少量	—	
全面的 错误*1*2*3	AINL	—	1.2	±7.0	LSB	10 位分辨率	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	1.2	±10.5	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V[*5]
转换时间	tCONV	2.125	—	39	μs	10 位分辨率 目标引脚：AN000, AN001, AN004, AN005, AN021, AN022	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		1.8 V ≤ VCC ≤ 5.5 V
		57	—	95	μs		1.6 V ≤ VCC ≤ 5.5 V
		2.375	—	39	μs	10 位分辨率 目标引脚：内部参考 电压和温度传感器输出电压	3.6 V ≤ VCC ≤ 5.5 V
		3.5625	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		1.8 V ≤ VCC ≤ 5.5 V
零尺度 错误*1*2*3*4	E_{ZS}	—	—	±0.60	%FSR	10 位分辨率	1.8 V ≤ VCC ≤ 5.5 V
		—	—	±0.85	%FSR		1.6 V ≤ VCC ≤ 5.5 V[*5]
全面 错误*1*2*3*4	E_{FS}	—	—	±0.60	%FSR	10 位分辨率	1.8 V ≤ VCC ≤ 5.5 V
		—	—	±0.85	%FSR		1.6 V ≤ VCC ≤ 5.5 V[*5]
积分线性 错误*1*2*3	ILE	—	—	±4.0	LSB	10 位分辨率	1.8 V ≤ VCC ≤ 5.5 V
		—	—	±6.0	LSB		1.6 V ≤ VCC ≤ 5.5 V[*5]
微分线性 错误*1*2*3	DLE	—	—	±2.0	LSB	10 位分辨率	1.8 V ≤ VCC ≤ 5.5 V
		—	—	±2.5	LSB		1.6 V ≤ VCC ≤ 5.5 V[*5]

Table 2.40 A/D conversion characteristics (AN000, AN001, AN004, AN005, AN021, AN022, internal reference voltage, and temperature sensor output voltage) (2 of 2)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
Reference voltage range applied to the VCC (ADREFP[1:0] = 00b) and VSS (ADREFM = 0b).
Target pins: AN000, AN001, AN004, AN005, AN021, AN022, internal reference voltage*7, and temperature sensor output voltage*7
(Reference voltage (+) = VCC, Reference voltage (–) = VSS)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Analog input voltage	V_{AIN}	0	—	VCC	V	AN000, AN001, AN004, AN005, AN021, AN022
		V_{BGR}*6			V	Internal reference voltage (1.8 V ≤ VCC ≤ 5.5 V)
		V_{TMPS25}*6			V	Temperature sensor output voltage (1.8 V ≤ VCC ≤ 5.5 V)

Note 1. The Typ. value is an average value at TA = 25°C. The Max. value is an average value ±3σ at normal distribution.
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
Note 3. This value does not include the quantization error (±1/2 LSB).
Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 5. The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57 µs and 95 µs.
Note 6. See section 2.6.3. Temperature Sensor/Internal Reference Voltage Characteristics.
Note 7. If the internal reference voltage or temperature sensor output voltage is to be A/D converted, VCC must be at least 1.8 V.

Table 2.41 A/D conversion characteristics (AN000, AN004, AN005, AN021, AN022)

Conditions: 1.8 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
Reference voltage range applied to the VBGR (ADREFP[1:0] = 10b) and VREFL0 (ADREFM = 1b).
Target pins: AN000, AN004, AN005, AN021, AN022
(Reference voltage (+) = V_{BGR}*5, Reference voltage (–) = VREFL0*6 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Resolution	RES	8			bit	—
Conversion time	tCONV	17	—	39	µs	—
Zero-scale error*1*2*3*4	E_{ZS}	—	—	±0.60	%FSR	—
Integral linearity error*1*2*3	ILE	—	—	±2.0	LSB	—
Differential linearity error*1*2*3	DLE	—	—	±1.0	LSB	—
Analog input voltage	V_{AIN}	0	—	V_{BGR}*5	V	—

Note 1. The Typ. value is an average value at TA = 25°C. The MAX. value is an average value ±3σ at normal distribution.
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
Note 3. This value does not include the quantization error (±1/2 LSB).
Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 5. See section 2.6.3. Temperature Sensor/Internal Reference Voltage Characteristics.
Note 6.
- Zero-scale error: Add ±0.35%FSR to the maximum value when reference voltage (–) = VREFL0.
- Integral linearity error: Add ±0.5 LSB to the maximum value when reference voltage (–) = VREFL0.
- Differential linearity error: Add ±0.2 LSB to the maximum value when reference voltage (–) = VREFL0.

2.6.2 A/D Converter Characteristics for T_A = -40 to +125°C

Table 2.42 Reference for the characteristics of the A/D converter

Input channel	Reference Voltage		
	Reference voltage (+) = VREFH0 Reference voltage (–) = VREFL0	Reference voltage (+) = VCC Reference voltage (–) = VSS	Reference voltage (+) = V_{BGR} Reference voltage (–) = VREFL0
AN000, AN001, AN004, AN005	Refer to Table 2.43.	Refer to Table 2.45.	Refer to Table 2.46.
AN021, AN022	Refer to Table 2.44.		
Internal reference voltage Temperature sensor output voltage	Refer to Table 2.43.		—

表 2.40 A/D 转换特性（AN000、AN001、AN004、AN005、AN021、AN022、内部参考电压和温度传感器输出电压）（2/2）

条件：1.6 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
Reference voltage range applied to the VCC (ADREFP[1:0] = 00b) and VSS (ADREFM = 0b).
Target pins: AN000, AN001, AN004, AN005, AN021, AN022, internal reference voltage*7, and temperature sensor output voltage*7
（参考电压(+) = VCC、参考电压(–) = VSS）

范围	象征	最小。	类型。	最大限度。	单元	状况
模拟输入电压	V_{AIN}	0	—	VCC	V	AN000、AN001、AN004、AN005、AN021, AN022
		V_{BGR}*6			V	内部参考电压 (1.8 V ≤ VCC ≤ 5.5 V)
		V_{TMPS25}*6			V	温度传感器输出电压 (1.8 V ≤ VCC ≤ 5.5 V)

注 1. 典型值是TA = 25°C. 处的平均值，最大值是±3σ处的平均值。
注2. 这些数值是特性评估的结果，并非出货时的检查值。
注3.此值不包括量化误差(±1/2 LSB)。
注 4. 此值表示为(%FSR) 与满量程值的比率。
注5：所列值适用于最大和最小转换时间值分别设置为57 µs和95 µs的情况。
注 6. 请参阅第 2.6.3 节。温度传感器/内部参考电压特性。
注7. 如果内部参考电压或温度传感器输出电压需要进行A/D转换，则VCC必须至少为1.8 V.

表 2.41A/D 转换特性（AN000、AN004、AN005、AN021、AN022）

条件：1.8 V ≤ VREFH0 ≤ VCC ≤ 5.5 V、VSS = 0 V、Ta = -40至+85°C
应用于 VBGR (ADREFP[1:0] = 10b) 和 VREFL0 (ADREFM= 1b) 的参考电压范围。
目标引脚：AN000、AN004、AN005、AN021、AN022
（参考电压(+) = V_{BGR}*5, 参考电压(–) = VREFL0*6 = 0 V)

范围	象征	最小。	类型。	最大限度。	单元	状况
解决	RES	8			少量	—
转换时间	tCONV	17	—	39	µs	—
零刻度误差*1*2*3*4	E_{ZS}	—	—	±0.60	%FSR	—
积分线性误差*1*2*3	ILE	—	—	±2.0	LSB	—
微分线性误差*1*2*3	DLE	—	—	±1.0	LSB	—
模拟输入电压	V_{AIN}	0	—	V_{BGR}*5	V	—

注 1. 典型值是TA = 25°C. 处的平均值，最大值是±3σ处的平均值。
注2. 这些数值是特性评估的结果，并非出货时的检查值。
注3.此值不包括量化误差(±1/2 LSB)。
注 4. 此值表示为(%FSR)与满量程值的比率。
注5.参见第2.6.3节。温度传感器/内部参考电压特性。
注6.●零刻度误差：当参考电压(–) = VREFL0时，将±0.35%FSR加到最大值。
●积分线性误差：当参考电压(–) = VREFL0时，将±0.5 LSB加到最大值。
●差分线性误差：当参考电压(–) = VREFL0 时，将±0.2LSB 加到最大值。

2.6.2 T_A = -40 to +125°C的 A/D 转换器特性

表 2.42 A/D 转换器特性参考

输入通道	参考电压		
	参考电压(+) = VREFH0 参考电压(–) = VREFL0	参考电压(+) = VCC 参考电压(–) = VSS	参考电压(+) = V_{BGR} 参考电压(–) = VREFL0
AN000、AN001、AN004、AN005	请参阅表 2.43。	请参阅表 2.45。	请参阅表 2.46。
AN021, AN022	请参阅表 2.44。		
内部参考电压温度传感器输出电压	请参阅表 2.43。		—

Table 2.43 A/D conversion characteristics

Conditions: 2.4 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C
Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).
Target pins: AN004, AN005, internal reference voltage, and temperature sensor output voltage
(Reference voltage (+) = VREFH0, Reference voltage (–) = VREFL0 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Resolution	RES	8	—	10	bit	—	
Overall error*1*2*3	AINL	—	1.2	±3.5	LSB	10-bit resolution VREFH0 = VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
Conversion time	tCONV	2.125	—	39	μs	10-bit resolution Target pin: AN004, AN005	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		2.4 V ≤ VCC ≤ 5.5 V
		2.375	—	39	μs	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage	3.6 V ≤ VCC ≤ 5.5 V
		3.5625	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		2.4 V ≤ VCC ≤ 5.5 V
Zero-scale error*1*2*3*4	E_{ZS}	—	—	±0.25	%FSR	10-bit resolution VREFH0 = VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
Full-scale error*1*2*3*4	E_{FS}	—	—	±0.25	%FSR	10-bit resolution VREFH0 = VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
Integral linearity error*1*2*3	ILE	—	—	±2.5	LSB	10-bit resolution VREFH0 = VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
Differential linearity error*1*2*3	DLE	—	—	±1.5	LSB	10-bit resolution VREFH0 = VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
Analog input voltage	V_{AIN}	0	—	VREFH0	V	AN004, AN005	
		V_{BGR}*6			V	Internal reference voltage	
		V_{TMPS25}*6			V	Temperature sensor output voltage	

Note 1. The Typ. value is an average value at TA = 25°C. The Max. value is an average value ±3σ at normal distribution.
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
Note 3. This value does not include the quantization error (±1/2 LSB).
Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 5. When VREFH0 < VCC, the maximum values are as follows.

- Overall error: Add ±1.0 LSB to the maximum value when VCC = VREFH0.
- Zero-scale/full-scale error: Add ±0.05%FSR to the maximum value when VCC = VREFH0.
- Integral linearity error and differential linearity error: Add ±0.5 LSB to the maximum value when VCC = VREFH0.

Note 6. See section 2.6.3. Temperature Sensor/Internal Reference Voltage Characteristics.

表 2.43 A/D 转换特性

条件：2.4 V ≤ VREFH0 ≤ VCC ≤ 5.5 V、VSS = 0 V、Ta = -40至+125°C参考电压范围应用于 VREFH0 (A DREFP[1:0] = 01b) 和 VREFL0 (ADREFM= 1b)。
目标引脚：AN004、AN005、内部参考电压和温度传感器输出电压（参考电压(+) = VREFH0, 参考电压(–) = VREFL0 = 0 V)

范围	象征	最小。	类型。	最大限度。	单元	状况	
解决	RES	8	—	10	少量	—	
全面的 错误*1*2*3	AINL	—	1.2	±3.5	LSB	10 位分辨率 VREFH0=VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
转换时间	tCONV	2.125	—	39	μs	10 位分辨率 目标引脚：AN004, AN005	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		2.4 V ≤ VCC ≤ 5.5 V
		2.375	—	39	μs	10 位分辨率 目标引脚：内部参考电压和温度传感器输出电压	3.6 V ≤ VCC ≤ 5.5 V
		3.5625	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		2.4 V ≤ VCC ≤ 5.5 V
零尺度 错误*1*2*3*4	E_{ZS}	—	—	±0.25	%FSR	10 位分辨率 VREFH0=VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
全面 错误*1*2*3*4	E_{FS}	—	—	±0.25	%FSR	10 位分辨率 VREFH0 = VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
积分线性 错误*1*2*3	ILE	—	—	±2.5	LSB	10 位分辨率 VREFH0 = VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
微分线性 错误*1*2*3	DLE	—	—	±1.5	LSB	10 位分辨率 VREFH0=VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
模拟输入电压	V_{AIN}	0	—	VREFH0	V	AN004, AN005	
		V_{BGR}*6			V	内部参考电压	
		V_{TMPS25}*6			V	温度传感器输出电压	

注 1. 典型值是TA = 25°C. 处的平均值，最大值是±3σ处的平均值。
注2. 这些数值是特性评估的结果，并非出货时的检查值。
注3.此值不包括量化误差(±1/2 LSB)。
注 4. 此值表示为(%FSR)与满量程值的比率。
注5. 当VREFH0 < VCC时，最大值如下。

- 总体误差：当 VCC=VREFH0 时，将±1.0 LSB添加到最大值。
- 零刻度/满刻度误差：当VCC = VREFH0时，将±0.05%FSR加到最大值。
- 积分线性误差和微分线性误差：当 VCC= VREFH0 时，将±0.5 LSB加到最大值。

注 6. 请参阅第 2.6.3 节。温度传感器/内部参考电压特性。

Table 2.44 A/D conversion characteristics (AN021 to AN022)

Conditions: 2.4 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C
Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).
Target pins: AN021 to AN022
(Reference voltage (+) = VREFH0, Reference voltage (–) = VREFL0 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Resolution	RES	8	—	10	bit	—	
Overall error*1*2*3	AINL	—	1.2	±5.0	LSB	10-bit resolution VREFH0 = VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
Conversion time	tCONV	2.125	—	39	μs	10-bit resolution Target pin: AN021, AN022	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		2.4 V ≤ VCC ≤ 5.5 V
Zero-scale error*1*2*3*4	E_{ZS}	—	—	±0.35	%FSR	10-bit resolution VREFH0 = VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
Full-scale error*1*2*3*4	E_{FS}	—	—	±0.35	%FSR	10-bit resolution VREFH0 = VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
Integral linearity error*1*2*3	ILE	—	—	±3.5	LSB	10-bit resolution VREFH0 = VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
Differential linearity error*1*2*3	DLE	—	—	±2.0	LSB	10-bit resolution VREFH0 = VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
Analog input voltage	V_{AIN}	0	—	VREFH0	V	AN021, AN022	

Note 1. The Typ. value is an average value at TA = 25°C. The Max. value is an average value ±3σ at normal distribution.
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
Note 3. This value does not include the quantization error (±1/2 LSB).
Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 5. When VREFH0 < VCC, the maximum values are as follows.

- Overall error: Add ±1.0 LSB to the maximum value when VCC = VREFH0.
- Zero-scale/full-scale error: Add ±0.05%FSR to the maximum value when VCC = VREFH0.
- Integral linearity error and differential linearity error: Add ±0.5 LSB to the maximum value when VCC = VREFH0.

Table 2.45 A/D conversion characteristics (1 of 2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C
Reference voltage range applied to the VCC (ADREFP[1:0] = 00b) and VSS (ADREFM = 0b).
Target pins: AN000, AN001, AN004, AN005, AN021, AN022, internal reference voltage, and temperature sensor output voltage
(Reference voltage (+) = VCC, Reference voltage (–) = VSS)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Resolution	RES	8	—	10	bit	—	
Overall error*1*2*3	AINL	—	1.2	±7.0	LSB	10-bit resolution	2.4 V ≤ VREFH0 ≤ 5.5 V

表 2.44A/D 转换特性（AN021 至 AN022）

条件：2.4 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V，Ta= -40至+125°C
参考电压范围应用于 VREFH0 (ADREFP[1:0] = 01b) 和 VREFL0 (ADREFM= 1b)。
目标引脚：AN021 至 AN022
(Reference voltage (+) = VREFH0, Reference voltage (–) = VREFL0 = 0 V)

范围	象征	最小。	类型。	最大限度。	单元	状况	
解决	RES	8	—	10	少量	—	
全面的错误*1*2*3	AINL	—	1.2	±5.0	LSB	10 位分辨率 VREFH0=VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
转换时间	tCONV	2.125	—	39	μs	10 位分辨率 目标引脚：AN021, AN022	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		2.4 V ≤ VCC ≤ 5.5 V
零尺度错误*1*2*3*4	E_{ZS}	—	—	±0.35	%FSR	10 位分辨率 VREFH0=VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
全面错误*1*2*3*4	E_{FS}	—	—	±0.35	%FSR	10 位分辨率 VREFH0=VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
积分线性误差*1*2*3	ILE	—	—	±3.5	LSB	10 位分辨率 VREFH0=VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
微分线性错误*1*2*3	DLE	—	—	±2.0	LSB	10 位分辨率 VREFH0=VCC*5	2.4 V ≤ VREFH0 ≤ 5.5 V
模拟输入电压	V_{AIN}	0	—	VREFH0	V	AN021, AN022	

注 1. 典型值是TA = 25°C. 处的平均值，最大值是±3σ处的平均值。
注2. 这些数值是特性评估的结果，并非出货时的检查值。
注3.此值不包括量化误差(±1/2 LSB)。
注 4. 此值表示为(%FSR)与满量程值的比率。
注5. 当VREFH0 < VCC, 时，最大值如下。

- 总体误差：当VCC = VREFH0时，将±1.0LSB 加到最大值。
- 零刻度/满刻度误差：当VCC = VREFH0时，将±0.05%FSR加到最大值。
- 积分线性误差和微分线性误差：当 VCC= VREFH0 时，将±0.5LSB 加到最大值。

表 2.45 A/D 转换特性（1/2）

条件：2.4 V ≤ VCC ≤ 5.5 V、VSS = 0 V、Ta = -40 至+125°C
应用于 VCC 的参考电压范围（ADREFP[1:0] = 00b) 和 VSS(ADREFM = 0b)）。
目标引脚：AN000、AN001、AN004、AN005、AN021、AN022、内部参考电压和温度传感器输出电压
（参考电压(+) = VCC，参考电压(–) = VSS)）

范围	象征	最小。	类型。	最大限度。	单元	状况	
解决	RES	8	—	10	少量	—	
全面的错误*1*2*3	AINL	—	1.2	±7.0	LSB	10 位分辨率	2.4 V ≤ VREFH0 ≤ 5.5 V

Table 2.45 A/D conversion characteristics (2 of 2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C
Reference voltage range applied to the VCC (ADREFP[1:0] = 00b) and VSS (ADREFM = 0b).
Target pins: AN000, AN001, AN004, AN005, AN021, AN022, internal reference voltage, and temperature sensor output voltage
(Reference voltage (+) = VCC, Reference voltage (–) = VSS)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Conversion time	tCONV	2.125	—	39	μs	10-bit resolution Target pin: AN000, AN001, AN004, AN005, AN021, AN022	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		2.4 V ≤ VCC ≤ 5.5 V
		2.375	—	39	μs	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage	3.6 V ≤ VCC ≤ 5.5 V
		3.5625	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		2.4 V ≤ VCC ≤ 5.5 V
Zero-scale error*1*2*3*4	E_{ZS}	—	—	±0.60	%FSR	10-bit resolution	2.4 V ≤ VCC ≤ 5.5 V
Full-scale error*1*2*3*4	E_{FS}	—	—	±0.60	%FSR	10-bit resolution	2.4 V ≤ VCC ≤ 5.5 V
Integral linearity error*1*2*3	ILE	—	—	±4.0	LSB	10-bit resolution	2.4 V ≤ VREFH0 ≤ 5.5 V
Differential linearity error*1*2*3	DLE	—	—	±2.0	LSB	10-bit resolution	2.4 V ≤ VREFH0 ≤ 5.5 V
Analog input voltage	V_{AIN}	0	—	VCC	V	AN000, AN001, AN004, AN005, AN021, AN022	
		V_{BGR}*5			V	Internal reference voltage	
		V_{TMPS25}*5			V	Temperature sensor output voltage	

Note 1. The Typ. value is an average value at TA = 25°C. The Max. value is an average value ±3σ at normal distribution.
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
Note 3. This value does not include the quantization error (±1/2 LSB).
Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 5. See section 2.6.3. Temperature Sensor/Internal Reference Voltage Characteristics.

Table 2.46 A/D conversion characteristics (AN000, AN004, AN005, AN021, AN022)

Conditions: 2.4 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C
Reference voltage range applied to the VBGR (ADREFP[1:0] = 10b) and VREFL0 (ADREFM = 1b).
Target pins: AN000, AN004, AN005, AN021, AN022
(Reference voltage (+) = V_{BGR}*5, Reference voltage (–) = VREFL0*6 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Resolution	RES	8			bit	—
Conversion time	tCONV	17	—	39	μs	—
Zero-scale error*1*2*3*4	E_{ZS}	—	—	±0.60	%FSR	—
Integral linearity error*1*2*3	ILE	—	—	±2.0	LSB	—
Differential linearity error*1*2*3	DLE	—	—	±1.0	LSB	—
Analog input voltage	V_{AIN}	0	—	V_{BGR}*5	V	—

Note 1. The Typ. value is an average value at TA = 25°C. The Max. value is an average value ±3σ at normal distribution.
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
Note 3. This value does not include the quantization error (±1/2 LSB).

表 2.45 A/D 转换特性（2/2）

条件：2.4 V ≤ VCC ≤ 5.5 V、VSS = 0 V、Ta = -40 至+125°C
应用于 VCC 的参考电压范围（ADREFP[1:0] = 00b) 和 VSS(ADREFM = 0b)）。
目标引脚：AN000、AN001、AN004、AN005、AN021、AN022、内部参考电压和温度传感器输出电压（参考电压(+) = VCC，参考电压(
–) = VSS)）。

范围	象征	最小。	类型。	最大限度。	单元	状况	
转换时间	tCONV	2.125	—	39	μs	10 位分辨率 目标引脚：AN000, AN001, AN004, AN005, AN021, AN022	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		2.4 V ≤ VCC ≤ 5.5 V
		2.375	—	39	μs	10 位分辨率 目标引脚：内部参考 电压和温度传感器输出电压	3.6 V ≤ VCC ≤ 5.5 V
		3.5625	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		2.4 V ≤ VCC ≤ 5.5 V
零尺度错误*1*2*3*4	E_{ZS}	—	—	±0.60	%FSR	10 位分辨率	2.4 V ≤ VCC ≤ 5.5 V
满量程误差*1*2*3*4	E_{FS}	—	—	±0.60	%FSR	10 位分辨率	2.4 V ≤ VCC ≤ 5.5 V
积分线性错误*1*2*3	ILE	—	—	±4.0	LSB	10 位分辨率	2.4 V ≤ VREFH0 ≤ 5.5 V
微分线性错误*1*2*3	DLE	—	—	±2.0	LSB	10 位分辨率	2.4 V ≤ VREFH0 ≤ 5.5 V
模拟输入电压	V_{AIN}	0	—	VCC	V	AN000、AN001、AN004、AN005、AN021, AN022	
		V_{BGR}*5			V	内部参考电压	
		V_{TMPS25}*5			V	温度传感器输出电压	

注 1. 典型值是TA = 25°C. 处的平均值，最大值是±3σ处的平均值。
注2. 这些数值是特性评估的结果，并非出货时的检查值。
注3.此值不包括量化误差(±1/2 LSB)。
注 4. 此值以与满量程值的比率 (%FSR) 表示。
注5.参见第2.6.3节。温度传感器/内部参考电压特性。

表 2.46A/D 转换特性（AN000、AN004、AN005、AN021、AN022）

条件：2.4 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V，Ta = -40至+125°C
应用于 VBGR (ADREFP[1:0] = 10b) 和 VREFL0 (ADREFM = 1b) 的参考电压范围
目标引脚：AN000、AN004、AN005、AN021、AN022
（参考电压(+) = V_{BGR}*5，参考电压(–) = VREFL0*6 = 0 V)）

范围	象征	最小。	类型。	最大限度。	单元	状况
解决	RES	8			少量	—
转换时间	tCONV	17	—	39	μs	—
零尺度误差*1*2*3*4	E_{ZS}	—	—	±0.60	%FSR	—
积分线性误差*1*2*3	ILE	—	—	±2.0	LSB	—
微分线性误差*1*2*3	DLE	—	—	±1.0	LSB	—
模拟输入电压	V_{AIN}	0	—	V_{BGR}*5	V	—

注 1. 典型值是TA = 25°C. 处的平均值，最大值是±3σ处的平均值。
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
注3.此值不包括量化误差(±1/2 LSB)。

Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 5. See section 2.6.3. Temperature Sensor/Internal Reference Voltage Characteristics.
Note 6.
- Zero-scale error: Add ±0.35%FSR to the maximum value when reference voltage (–) = VREFL0.
- Integral linearity error: Add ±0.5 LSB to the maximum value when reference voltage (–) = VREFL0.
- Differential linearity error: Add ±0.2 LSB to the maximum value when reference voltage (–) = VREFL0.

2.6.3 Temperature Sensor/Internal Reference Voltage Characteristics

Table 2.47 Temperature sensor/internal reference voltage characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Temperature sensor output voltage	V_{TMPS25}	—	1.05	—	V	at = 25°C
Internal reference voltage	V_{BGR}	1.40	1.48	1.56	V	—
Temperature coefficient	F_{VTMPS}	—	-3.3	—	mV/°C	—
Operation stabilization wait time	t_{AMP}	5	—	—	μs	—

2.6.4 POR Characteristics

Table 2.48 POR characteristics

Conditions: VSS = 0 V, Ta = -40 to +125°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection voltage	VPOR VPDR	1.43	1.50	1.57	V	—
Minimum pulse width[*1]	TPW	300	—	—	μs	—

Note 1. This width is the minimum time required for a POR reset when VCC falls below VPDR. This width is also the minimum time required for a POR reset from when VCC falls below 0.7 V to when VCC exceeds VPOR in the Software standby mode or while the main system clock is stopped through setting HOCOCR.HCSTOP bit.

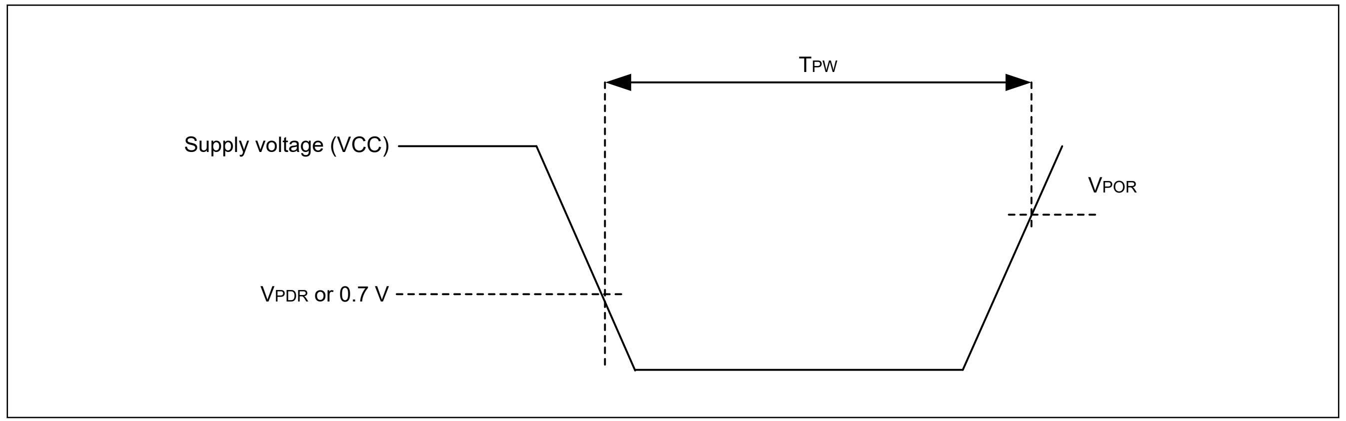


Figure 2.31 Minimum VCC pulse width

注 4. 此值以与满量程值的比率 (%FSR) 表示。
注5.参见第2.6.3节。温度传感器/内部参考电压特性。
注6.●零刻度误差：当参考电压(–) = VREFL0时，将±0.35%FSR加到最大值。
●积分线性误差：当参考电压(–) =VREFL0 时，将±0.5LSB 加到最大值。
●差分线性误差：当参考电压(–) =VREFL0 时，将±0.2LSB 加到最大值。

2.6.3 温度传感器/内部参考电压特性

表 2.47 温度传感器/内部参考电压特性

条件：1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 至+125°C

范围	象征	最小。	类型。	最大限度。	单元	测试条件
温度传感器输出电压	V_{TMPS25}	—	1.05	—	V	at = 25°C
内部参考电压	V_{BGR}	1.40	1.48	1.56	V	—
温度系数	F_{VTMPS}	—	-3.3	—	mV/°C	—
运行稳定等待时间	夯	5	—	—	μs	—

2.6.4 POR特性

表 2.48 POR 特征

条件：VSS = 0 V，Ta = -40至+125°C

范围	象征	最小。	类型。	最大限度。	单元	测试条件
检测电压	VPOR VPDR	1.43	1.50	1.57	V	—
最小脉冲宽度*1	TPW	300	—	—	μs	—

注1：此宽度为VCC低于VPDR时POR复位所需的最小时间。此宽度也是在软件待机模式下，或通过设置HOCOCR.HCSTOP位停止主系统时钟时，从VCC低于0.7 V到VCC超过VPOR之间POR复位所需的最小时间。

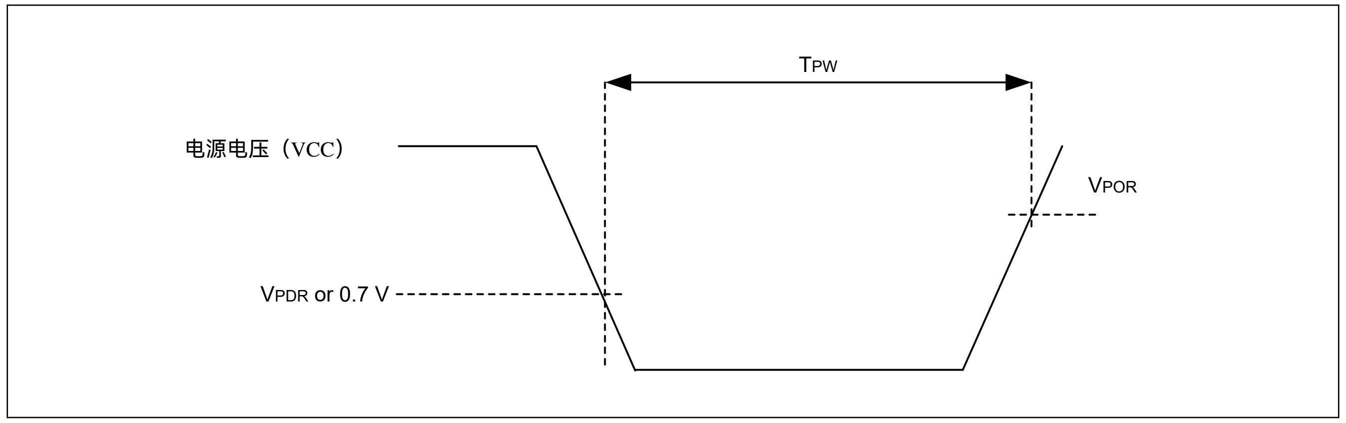


图 2.31 最小 VCC 脉冲宽度

2.6.5 LVD Characteristics

Table 2.49 LVD0 characteristics

Conditions: VPDR ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection voltage	Supply voltage level	V_{det0_0}	3.84	3.96	4.08	V	The power supply voltage is rising.
			3.76	3.88	4.00	V	The power supply voltage is falling.
		V_{det0_1}	2.88	2.97	3.06	V	The power supply voltage is rising.
			2.82	2.91	3.00	V	The power supply voltage is falling.
		V_{det0_2}	2.59	2.67	2.75	V	The power supply voltage is rising.
			2.54	2.62	2.70	V	The power supply voltage is falling.
		V_{det0_3}	2.31	2.38	2.45	V	The power supply voltage is rising.
			2.26	2.33	2.40	V	The power supply voltage is falling.
		V_{det0_4}	1.84	1.90	1.95	V	The power supply voltage is rising.
			1.80	1.86	1.91	V	The power supply voltage is falling.
		V_{det0_5}	1.64	1.69	1.74	V	The power supply voltage is rising.
			1.60	1.65	1.70	V	The power supply voltage is falling.
Minimum pulse width		t_{LW0}	500	—	—	μs	—
Detection delay time		t_{det0}	—	—	500	μs	—

Table 2.50 LVD1 characteristics (1 of 2)

Conditions: VPDR ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection voltage	Supply voltage level	V_{det1_0}	4.08	4.16	4.24	V	The power supply voltage is rising.
			4.00	4.08	4.16	V	The power supply voltage is falling.
		V_{det1_1}	3.88	3.96	4.04	V	The power supply voltage is rising.
			3.80	3.88	3.96	V	The power supply voltage is falling.
		V_{det1_2}	3.68	3.75	3.82	V	The power supply voltage is rising.
			3.60	3.67	3.74	V	The power supply voltage is falling.
		V_{det1_3}	3.48	3.55	3.62	V	The power supply voltage is rising.
			3.40	3.47	3.54	V	The power supply voltage is falling.
		V_{det1_4}	3.28	3.35	3.42	V	The power supply voltage is rising.
			3.20	3.27	3.34	V	The power supply voltage is falling.
		V_{det1_5}	3.07	3.13	3.19	V	The power supply voltage is rising.
			3.00	3.06	3.12	V	The power supply voltage is falling.
		V_{det1_6}	2.91	2.97	3.03	V	The power supply voltage is rising.
			2.85	2.91	2.97	V	The power supply voltage is falling.
		V_{det1_7}	2.76	2.82	2.87	V	The power supply voltage is rising.
			2.70	2.76	2.81	V	The power supply voltage is falling.
		V_{det1_8}	2.61	2.66	2.71	V	The power supply voltage is rising.
			2.55	2.60	2.65	V	The power supply voltage is falling.
		V_{det1_9}	2.45	2.50	2.55	V	The power supply voltage is rising.
			2.40	2.45	2.50	V	The power supply voltage is falling.
		V_{det1_A}	2.35	2.40	2.45	V	The power supply voltage is rising.
			2.30	2.35	2.40	V	The power supply voltage is falling.

2.6.5LVD特性

表 2.49LVD0 特征

条件：VPDR≤VCC≤ 5.5 V、VSS = 0 V、Ta= -40至+125°C

范围		象征	最小。	类型。	最大限度	单元	测试条件
检测电压	供电电压等级	V_{det0_0}	3.84	3.96	4.08	V	电源电压正在上升。
			3.76	3.88	4.00	V	电源电压正在下降。
		V_{det0_1}	2.88	2.97	3.06	V	电源电压正在上升。
			2.82	2.91	3.00	V	电源电压正在下降。
		V_{det0_2}	2.59	2.67	2.75	V	电源电压正在上升。
			2.54	2.62	2.70	V	电源电压正在下降。
		V_{det0_3}	2.31	2.38	2.45	V	电源电压正在上升。
			2.26	2.33	2.40	V	电源电压正在下降。
		V_{det0_4}	1.84	1.90	1.95	V	电源电压正在上升。
			1.80	1.86	1.91	V	电源电压正在下降。
		V_{det0_5}	1.64	1.69	1.74	V	电源电压正在上升。
			1.60	1.65	1.70	V	电源电压正在下降。
最小脉冲宽度		t_{LW0}	500	—	—	μs	—
检测延迟时间		t_{det0}	—	—	500	μs	—

表 2.50LVD1 特征（1/2）

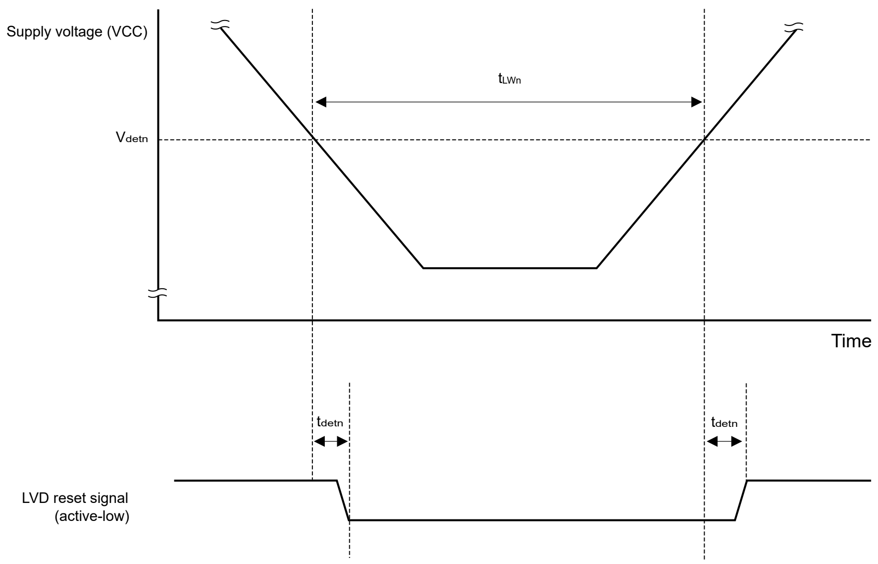
条件：VPDR≤VCC≤ 5.5V、VSS= 0 V、Ta= -40至+125°C

范围		象征	最小。	类型。	最大限度	单元	测试条件
检测电压	供电电压等级	V_{det1_0}	4.08	4.16	4.24	V	电源电压正在上升。
			4.00	4.08	4.16	V	电源电压正在下降。
		V_{det1_1}	3.88	3.96	4.04	V	电源电压正在上升。
			3.80	3.88	3.96	V	电源电压正在下降。
		V_{det1_2}	3.68	3.75	3.82	V	电源电压正在上升。
			3.60	3.67	3.74	V	电源电压正在下降。
		V_{det1_3}	3.48	3.55	3.62	V	电源电压正在上升。
			3.40	3.47	3.54	V	电源电压正在下降。
		V_{det1_4}	3.28	3.35	3.42	V	电源电压正在上升。
			3.20	3.27	3.34	V	电源电压正在下降。
		V_{det1_5}	3.07	3.13	3.19	V	电源电压正在上升。
			3.00	3.06	3.12	V	电源电压正在下降。
		V_{det1_6}	2.91	2.97	3.03	V	电源电压正在上升。
			2.85	2.91	2.97	V	电源电压正在下降。
		V_{det1_7}	2.76	2.82	2.87	V	电源电压正在上升。
			2.70	2.76	2.81	V	电源电压正在下降。
		V_{det1_8}	2.61	2.66	2.71	V	电源电压正在上升。
			2.55	2.60	2.65	V	电源电压正在下降。
		V_{det1_9}	2.45	2.50	2.55	V	电源电压正在上升。
			2.40	2.45	2.50	V	电源电压正在下降。
		V_{det1_A}	2.35	2.40	2.45	V	电源电压正在上升。
			2.30	2.35	2.40	V	电源电压正在下降。

Table 2.50 LVD1 characteristics (2 of 2)

Conditions: VPDR ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection voltage	Supply voltage level	V_{det1_B}	2.25	2.30	2.34	V	The power supply voltage is rising.
			2.20	2.25	2.29	V	The power supply voltage is falling.
		V_{det1_C}	2.15	2.20	2.24	V	The power supply voltage is rising.
			2.10	2.15	2.19	V	The power supply voltage is falling.
		V_{det1_D}	2.05	2.09	2.13	V	The power supply voltage is rising.
			2.00	2.04	2.08	V	The power supply voltage is falling.
		V_{det1_E}	1.94	1.98	2.02	V	The power supply voltage is rising.
			1.90	1.94	1.98	V	The power supply voltage is falling.
		V_{det1_F}	1.84	1.88	1.91	V	The power supply voltage is rising.
			1.80	1.84	1.87	V	The power supply voltage is falling.
		V_{det1_10}	1.74	1.78	1.81	V	The power supply voltage is rising.
			1.70	1.74	1.77	V	The power supply voltage is falling.
		V_{det1_11}	1.64	1.67	1.70	V	The power supply voltage is rising.
			1.60	1.63	1.66	V	The power supply voltage is falling.
Minimum pulse width		t_{LW1}	500	—	—	μs	—
Detection delay time		t_{det1}	—	—	500	μs	—
LVD1 detection voltage stabilization time (after changing the LVD1 detection voltage)		$t_{d(E-A)}$	—	—	1500	μs	—



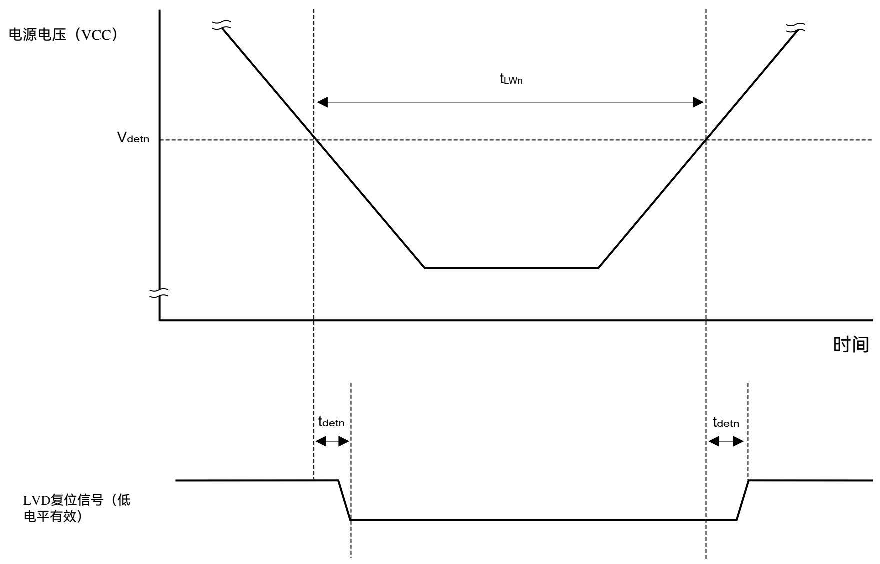
Note: n = 0, 1

Figure 2.32 Voltage detection circuit timing

表 2.50LVD1 特征（2/2）

条件：VPDR ≤ VCC ≤ 5.5 VVSS= 0 V,Ta = -40至+125°C

范围		象征	最小。	类型。	最大限度	单元	测试条件
检测电压	供电电压等级	V_{det1_B}	2.25	2.30	2.34	V	电源电压正在上升。
			2.20	2.25	2.29	V	电源电压正在下降。
		V_{det1_C}	2.15	2.20	2.24	V	电源电压正在上升。
			2.10	2.15	2.19	V	电源电压正在下降。
		V_{det1_D}	2.05	2.09	2.13	V	电源电压正在上升。
			2.00	2.04	2.08	V	电源电压正在下降。
		V_{det1_E}	1.94	1.98	2.02	V	电源电压正在上升。
			1.90	1.94	1.98	V	电源电压正在下降。
		V_{det1_F}	1.84	1.88	1.91	V	电源电压正在上升。
			1.80	1.84	1.87	V	电源电压正在下降。
		V_{det1_10}	1.74	1.78	1.81	V	电源电压正在上升。
			1.70	1.74	1.77	V	电源电压正在下降。
		V_{det1_11}	1.64	1.67	1.70	V	电源电压正在上升。
			1.60	1.63	1.66	V	电源电压正在下降。
最小脉冲宽度		t_{LW1}	500	—	—	μs	—
检测延迟时间		t_{det1}	—	—	500	μs	—
LVD1检测电压稳定时间（改变LVD1检测电压后）		$t_{d(E-A)}$	—	—	1500	μs	—



Note: n = 0, 1

图 2.32 电压检测电路时序

2.6.6 Power Supply Voltage Rising Slope Characteristics

Table 2.51 Power supply voltage rising slope characteristics

Conditions: VSS = 0 V, Ta = -40 to +125°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power supply voltage rising slope	S_{VCC}	—	—	54	V/ms	—

Note: Make sure to keep the internal reset state by the LVD0 circuit or an external reset until VCC reaches the operating voltage range shown in AC characteristics.

2.7 RAM Data Retention Characteristics

Table 2.52 RAM data retention characteristics

Conditions: VSS = 0 V, Ta = -40 to +125°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	1.43[*1]	—	5.5	V	—

Note 1. This voltage depends on the POR detection voltage. When the voltage drops, the data in RAM are retained until a POR is applied, but are not retained following a POR.

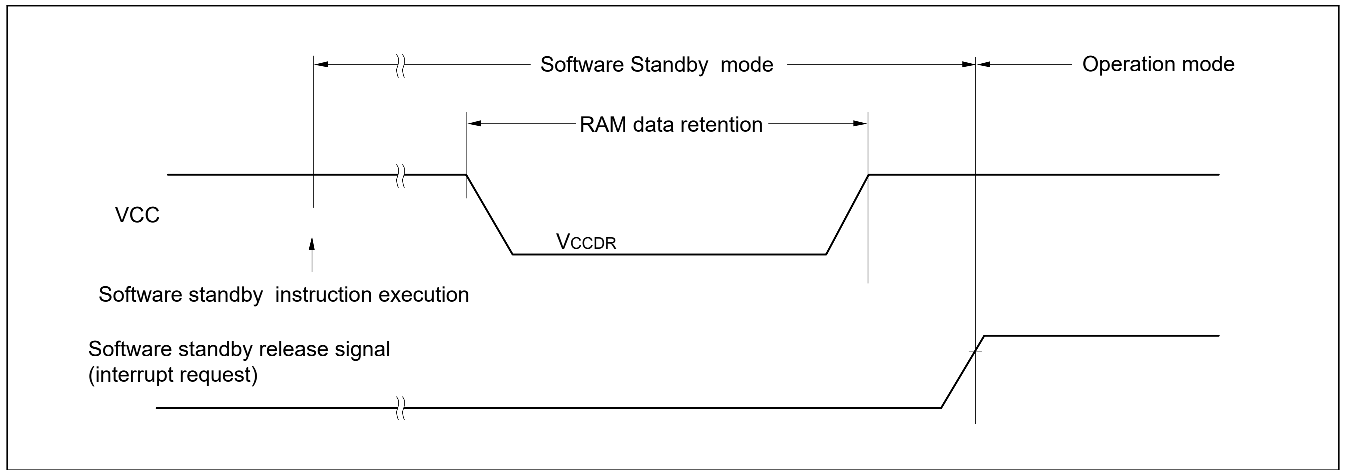


Figure 2.33 RAM data retention

2.8 Flash Memory Programming Characteristics

Table 2.53 Flash memory programming characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CPU/peripheral hardware clock frequency	I_{CLK}	1	—	32	MHz	—
Number of code flash rewrites[*1 *2 *3]	Cerwr	10000	—	—	Times	Retained for 10 years Ta = 85°C
		1000	—	—		Retained for 20 years Ta = 85°C

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
Note 2. The listed numbers of times apply when using the flash memory programmer and self-programming.
Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

Table 2.54 Code flash memory characteristics (1 of 2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz, 3 MHz			4 MHz ≤ ICLK < 8 MHz			8 MHz ≤ ICLK < 32 MHz			ICLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	μs

2.6.6 电源电压上升斜率特性

表 2.51 电源电压上升斜率特性

条件：VSS = 0 V，Ta = -40至+125°C

范围	象征	最小。	类型。	最大限度。	单元	测试条件
电源电压上升斜率	S_{VCC}	—	—	54	伏/毫秒	—

注意：务必通过 LVD0 电路或外部复位保持内部复位状态，直到 VCC 达到交流特性中所示的工作电压范围。

2.7 RAM 数据保持特性

表 2.52 RAM 数据保持特性

条件：VSS = 0 V，Ta= -40至+125°C

范围	象征	最小。	类型。	最大限度。	单元	测试条件
数据保持供电电压	V_{CCDR}	1.43[*1]	—	5.5	V	—

注1：此电压取决于POR检测电压。当电压下降时，RAM中的数据会保留，直到施加POR操作，但POR操作后数据不会被保留。

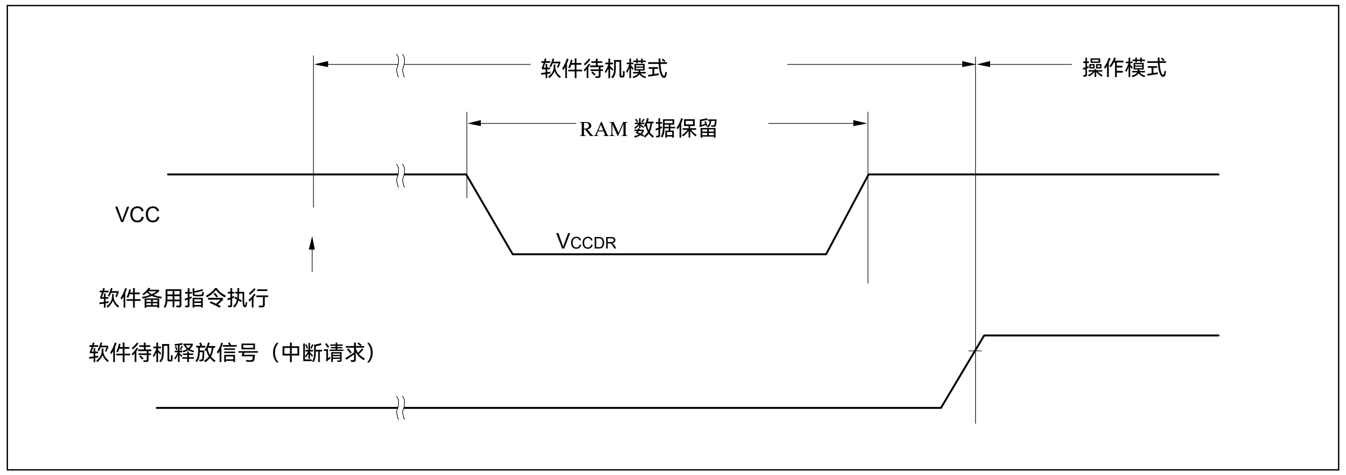


图 2.33 RAM 数据保持

2.8 闪存编程特性

表 2.53 闪存编程特性

条件：1.8 V ≤ VCC ≤ 5.5 V，VSS = 0 V Ta = -40 至+125°C

范围	象征	最小。	类型。	最大限度。	单元	测试条件
CPU/外围硬件时钟频率	I_{CLK}	1	—	32	MHz	—
代码闪存重写次数*1 *2 *3	卡弗	10000	—	—	《时代周刊》	保留10年 Ta = 85°C
		1000	—	—		保留了20年 Ta = 85°C

注1. 擦除后写入操作视为1次重写。保留期限至下次重写为止。
注 2. 所列次数适用于使用闪存编程器和自行编程的情况。
注3. 这些是闪存的特性以及瑞萨电子株式会社通过可靠性测试获得的结果。

表 2.54 代码闪存特性（1/2）

条件：1.8V≤ VCC≤ 5.5V，VSS= 0V，Ta= -40 至+125°C

范围		象征	ICLK = 1 MHz			ICLK = 2 MHz, 3 MHz			4 MHz ≤ ICLK < 8 MHz			8 MHz ≤ ICLK < 32 MHz			ICLK = 32 MHz			单元
			最小。	类型。	最大限度。	最小。	类型。	最大限度。	最小。	类型。	最大限度。	最小。	类型。	最大限度。	最小。	类型。	最大限度。	
编程时间	4 字节	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	μs

Table 2.54 Code flash memory characteristics (2 of 2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz, 3 MHz			4 MHz ≤ ICLK < 8 MHz			8 MHz ≤ ICLK < 32 MHz			ICLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Erasure time	2 Kbytes	t_{E2K}	—	10.4	312.2	—	7.7	258.5	—	6.4	231.8	—	5.8	218.4	—	5.6	214.4	ms
Blank checking time	4 bytes	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	μs
	2 Kbytes	t_{BC2K}	—	—	2618.9	—	—	1309.5	—	—	658.3	—	—	332.8	—	—	234.1	μs
Time taken to forcibly stop the erasure		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	μs
Security setting time		t_{AWSSAS}	—	18.0	525.5	—	14.3	468.7	—	12.5	440.7	—	11.6	426.7	—	11.3	422.3	ms
Time until programming starts following cancellation of the Software standby instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	μs
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	2	—	—	2	—	—	2	—	—	μs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	15	—	—	15	—	—	15	—	—	μs

Note: The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

2.9 Serial Wire Debug (SWD)

Table 2.55 SWD characteristics (1)

Conditions: VCC = 2.4 to 5.5 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	80	—	—	ns	Figure 2.34
SWCLK clock high pulse width	t_{SWCKH}	35	—	—	ns	
SWCLK clock low pulse width	t_{SECKL}	35	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	16	—	—	ns	Figure 2.35
SWDIO hold time	t_{SWDH}	16	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	70	ns	

Table 2.56 SWD characteristics (2)

Conditions: VCC = 1.6 to 2.4 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	—	—	ns	Figure 2.34
SWCLK clock high pulse width	t_{SWCKH}	120	—	—	ns	
SWCLK clock low pulse width	t_{SECKL}	120	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	50	—	—	ns	Figure 2.35
SWDIO hold time	t_{SWDH}	50	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	170	ns	

表 2.54 代码闪存特性（2/2）

条件：1.8V≤ VCC≤ 5.5 V、VSS= 0 V、Ta= -40 至+125°C

范围		象征	ICLK = 1 MHz			ICLK = 2 MHz, 3 MHz			4 MHz ≤ ICLK < 8 MHz			8 MHz ≤ ICLK < 32 MHz			ICLK = 32 MHz			单元
			最小。	类型。	最大限度。	最小。	类型。	最大限度。	最小。	类型。	最大限度。	最小。	类型。	最大限度。	最小。	类型。	最大限度。	
抹除时间	2 千字节	t_{E2K}	—	10.4	312.2	—	7.7	258.5	—	6.4	231.8	—	5.8	218.4	—	5.6	214.4	ms
空白支票时间	4 字节	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	μs
	2 千字节	t_{BC2K}	—	—	2618.9	—	—	1309.5	—	—	658.3	—	—	332.8	—	—	234.1	μs
强制阻止抹除所花费的时间		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	μs
安全设置时间		t_{AWSSAS}	—	18.0	525.5	—	14.3	468.7	—	12.5	440.7	—	11.6	426.7	—	11.3	422.3	ms
取消软件待机指令后，编程开始所需的时间		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	μs
闪存模式转换等待时间 1		t_{DIS}	2	—	—	2	—	—	2	—	—	2	—	—	2	—	—	μs
闪存模式转换等待时间 2		t_{MS}	15	—	—	15	—	—	15	—	—	15	—	—	15	—	—	μs

注意：所列数值不包括软件执行指令后闪存开始运行所需的时间。

2.9串行线调试（SWD）

表 2.55SWD 特征 (1)

条件：VCC = 2.4至5.5 V

范围	象征	最小。	类型。	最大限度。	单元	测试条件
SWCLK 时钟周期时间	$t_{SWCKcyc}$	80	—	—	ns	图 2.34
SWCLK时钟高脉冲宽度	t_{SWCKH}	35	—	—	ns	
SWCLK时钟低脉冲宽度	t_{SECKL}	35	—	—	ns	
SWCLK 时钟上升时间	t_{SWCKr}	—	—	5	ns	
SWCLK 时钟下降时间	t_{SWCKf}	—	—	5	ns	
SWDIO 设置时间	t_{SWDS}	16	—	—	ns	图 2.35
SWDIO保持时间	t_{SWDH}	16	—	—	ns	
SWDIO 数据延迟时间	t_{SWDD}	2	—	70	ns	

表 2.56SWD 特征 (2)

条件：VCC = 1.6至2.4 V

范围	象征	最小。	类型。	最大限度。	单元	测试条件
SWCLK 时钟周期时间	$t_{SWCKcyc}$	250	—	—	ns	图 2.34
SWCLK时钟高脉冲宽度	t_{SWCKH}	120	—	—	ns	
SWCLK时钟低脉冲宽度	t_{SECKL}	120	—	—	ns	
SWCLK 时钟上升时间	t_{SWCKr}	—	—	5	ns	
SWCLK 时钟下降时间	t_{SWCKf}	—	—	5	ns	
SWDIO 设置时间	t_{SWDS}	50	—	—	ns	图 2.35
SWDIO保持时间	t_{SWDH}	50	—	—	ns	
SWDIO 数据延迟时间	t_{SWDD}	2	—	170	ns	

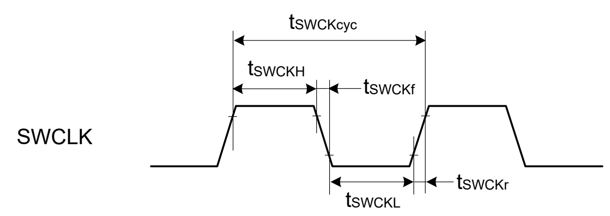


Figure 2.34 SWD SWCLK timing

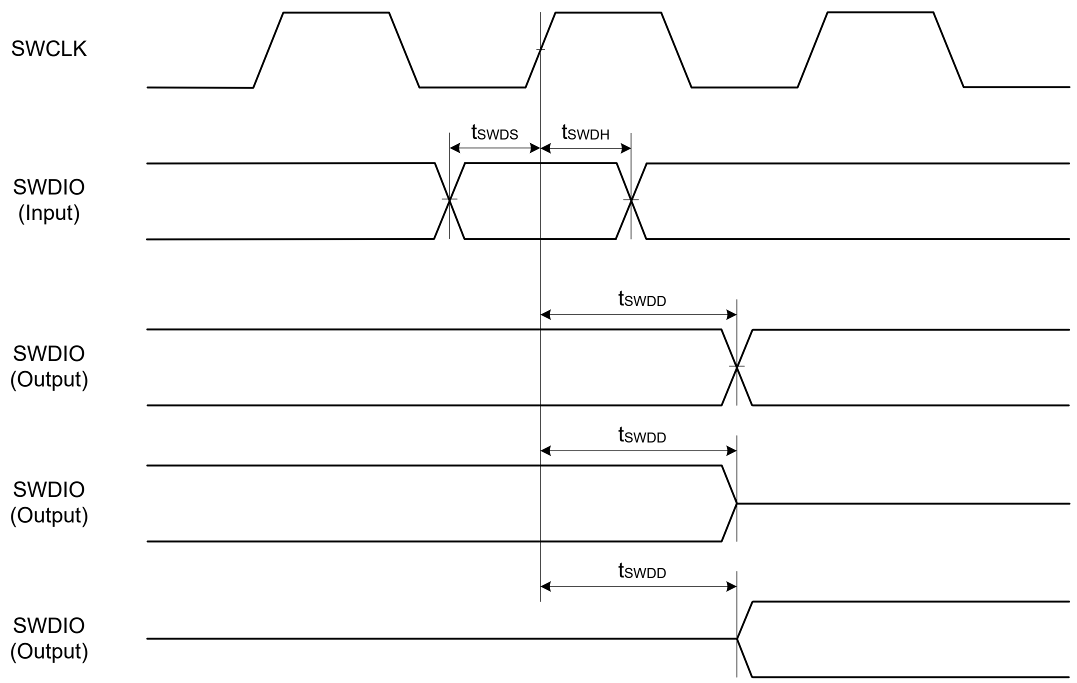


Figure 2.35 SWD input/output timing

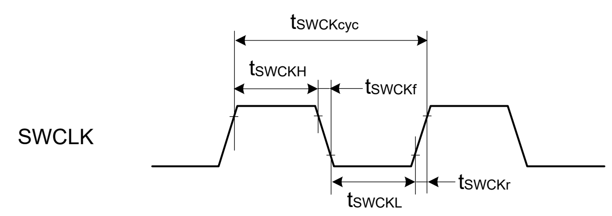


图 2.34SWD SWCLK 时序

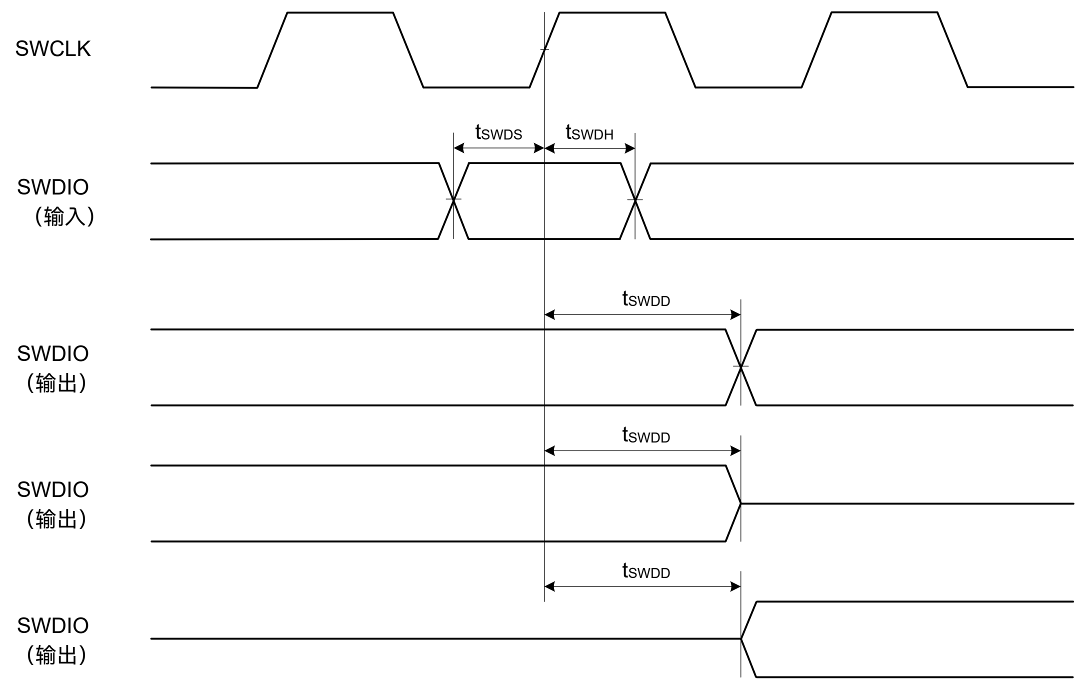


图 2.35SWD 输入/输出时序

Appendix 1. Port States in each Processing Mode

Table A1.1 Port states in each processing mode (1 of 2)

Port name	Reset	Software Standby Mode
P010/VREFH0/AN000	Hi-Z	Keep-O
P011/VREFL0/AN001	Hi-Z	Keep-O
P012/AN004	Hi-Z	Keep-O
P013/AN005	Hi-Z	Keep-O
P100/AN022/IRQ2_A/TI04_A/TO04_A/TI01_B/TO01_B/RXD0_A/SI00_A/SDA00_A/SCLA0_D	Hi-Z	[IRQ2_A selected] IRQ2_A input [SCLA0_D selected] SCLA0_D inout [Other than the above] Keep-O
P101/AN021/IRQ3_A/TI07_A/TO07_A/TI00_C/TXD0_A/SO00_A/SDAA0_D	Hi-Z	[IRQ3_A selected] IRQ3_A input [SDAA0_D selected] SDAA0_D inout [Other than the above] Keep-O
P102/IRQ4_A/TI06_A/TO06_A/TO00_C/PCLBUZ0_B/SCK00_A/SCL00_A	Hi-Z	[IRQ4_A selected] IRQ4_A input [PCLBUZ0_B selected] PCLBUZ0_B output [Other than the above] Keep-O
P108/SWDIO/TI03_B/TO03_B/PCLBUZ0_D/SCLA0_E/SCK00_C	Pull-up	[SCLA0_E selected] SCLA0_E inout [PCLBUZ0_D selected] PCLBUZ0_D output Keep-O
P109/IRQ4_B/TI02_A/TO02_A/TXD0_B/SO00_B/SDAA0_C	Hi-Z	[IRQ4_B selected] IRQ4_B input [SDAA0_C selected] SDAA0_C inout [Other than the above] Keep-O
P110/IRQ3_B/TI01_A/TO01_A/RXD0_B/SI00_B/SDA00_B/SCLA0_C	Hi-Z	[IRQ3_B selected] IRQ3_B input [SCLA0_C selected] SCLA0_C inout [Other than the above] Keep-O
P112/IRQ2_B/TI03_A/TO03_A/SCK00_B/SCL00_B/SSI00_C	Hi-Z	[IRQ2_B selected] IRQ2_B input [Other than the above] Keep-O
P200/NMI/IRQ0_A/TI06_B/SSI00_D/RXD1_B	Hi-Z	[NMI/IRQ0_A selected] NMI/IRQ0_A input [Other than the above] Hi-Z
P201/IRQ5_B/TI05_B/TO05_B/PCLBUZ0_A/SSI00_B/SCK11_B/SCL11_B	Hi-Z	[IRQ5_B selected] IRQ5_B input [PCLBUZ0_A selected] PCLBUZ0_A output [Other than the above] Keep-O

附录 1. 各处理模式下的端口状态

表 A1.1 各处理模式下的端口状态（1/2）

端口名称	重置	软件待机模式
P010/VREFH0/AN000	高阻抗	Keep-O
P011/VREFL0/AN001	高阻抗	Keep-O
P012/AN004	高阻抗	Keep-O
P013/AN005	高阻抗	Keep-O
P100/AN022/IRQ2_A/TI04_A/TO04_A/TI01_B/TO01_B/RXD0_A/SI00_A/SDA00_A/SCLA0_D	高阻抗	[IRQ2_A 已选择] IRQ2_A 输入 [SCLA0_D 已选择] SCLA0_D 输入/输出 [除上述内容外] Keep-O
P101/AN021/IRQ3_A/TI07_A/TO07_A/TI00_C/TXD0_A/SO00_A/SDAA0_D	高阻抗	[IRQ3_A 已选择] IRQ3_A 输入 [SDAA0_D 已选择] SDAA0_D 输入/输出 [除上述内容外] Keep-O
P102/IRQ4_A/TI06_A/TO06_A/TO00_C/PCLBUZ0_B/SCK00_A/SCL00_A	高阻抗	[IRQ4_A 已选择] IRQ4_A 输入 [PCLBUZ0_B 已选择] PCLBUZ0_B 输出 [除上述内容外] Keep-O
P108/SWDIO/TI03_B/TO03_B/PCLBUZ0_D/SCLA0_E/SCK00_C	引体向上	[SCLA0_E 已选择] SCLA0_E 输入/输出 [PCLBUZ0_D 已选择] PCLBUZ0_D 输出 Keep-O
P109/IRQ4_B/TI02_A/TO02_A/TXD0_B/SO00_B/SDAA0_C	高阻抗	[IRQ4_B 已选择] IRQ4_B 输入 [SDAA0_C 已选择] SDAA0_C 输入/输出 [除上述内容外] Keep-O
P110/IRQ3_B/TI01_A/TO01_A/RXD0_B/SI00_B/SDA00_B/SCLA0_C	高阻抗	[IRQ3_B 已选择] IRQ3_B 输入 [SCLA0_C 已选择] SCLA0_C 输入输出 [除上述内容外] Keep-O
P112/IRQ2_B/TI03_A/TO03_A/SCK00_B/SCL00_B/SSI00_C	高阻抗	[IRQ2_B 已选择] IRQ2_B 输入 [除上述内容外] Keep-O
P200/NMI/IRQ0_A/TI06_B/SSI00_D/RXD1_B	高阻抗	[已选择 NMI/IRQ0_A] NMI/IRQ0_A 输入 [除上述内容外] 高阻抗
P201/IRQ5_B/TI05_B/TO05_B/PCLBUZ0_A/SSI00_B/SCK11_B/SCL11_B	高阻抗	[IRQ5_B 已选择] IRQ5_B 输入 [PCLBUZ0_A 已选择] PCLBUZ0_A 输出 [除上述内容外] Keep-O

Table A1.1 Port states in each processing mode (2 of 2)

Port name	Reset	Software Standby Mode
P206/RES/IRQ1_C	Pull-up	[IRQ1_C selected] IRQ1_C input [RES (OFS1.PORTSELB = 1) selected] RES input [P206 (OFS1.PORTSELB = 0) selected] Keep-O
P212/IRQ1_B/TO00_A/TI03_C/TO03_C/RXD1_A/SI11_A/SDA11_A/SCLA0_B	Hi-Z	[IRQ1_B selected] IRQ1_B input [SCLA0_B selected] SCLA0_B inout [Other than the above] Keep-O
P213/IRQ0_B/TI00_A/TI02_B/TO02_B/TXD1_A/SO11_A/SDAA0_B	Hi-Z	[IRQ0_B selected] IRQ0_B input [SDAA0_B selected] SDAA0_B inout [Other than the above] Keep-O
P300/SWCLK/TI04_B/TO04_B/SDAA0_E/TXD1_B	Pull-up	[SDAA0_E selected] SDAA0_E inout [Other than the above] Keep-O

Note: Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins become high-impedance.

表 A1.1 各处理模式下的端口状态（2/2）

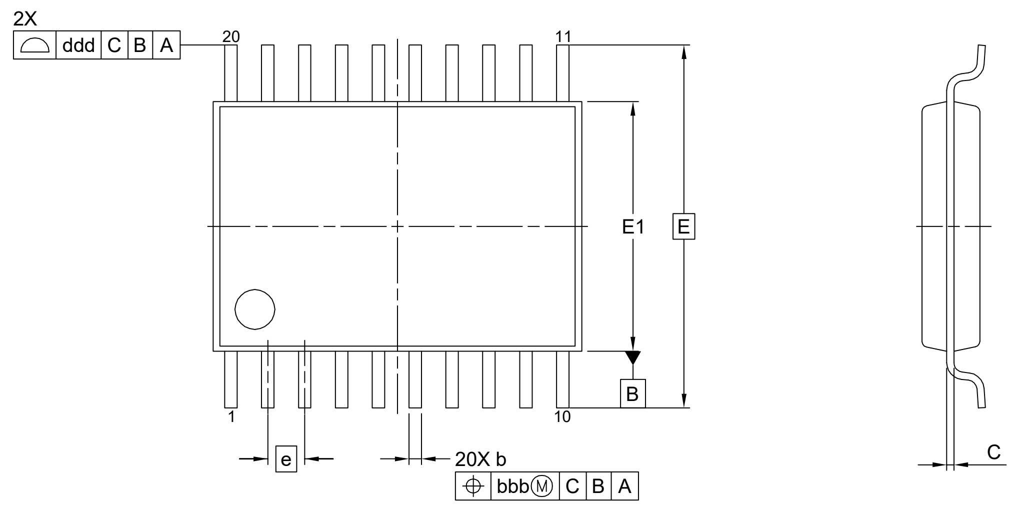
端口名称	重置	软件待机模式
P206/RES/IRQ1_C	引体向上	[IRQ1_C 已选择]IRQ1_C 输入[RES (OFS1.PORTSELB= 1) 已选择]RES 输入[P206 (OFS1.PORTSELB= 0) 已选择]保持 O
P212/IRQ1_B/TO00_A/TI03_C/TO03_C/RXD1_A/SI11_A/SDA11_A/SCLA0_B	高阻抗	[IRQ1_B 已选择] IRQ1_B 输入 [SCLA0_B 已选择] SCLA0_B 输入/输出 [除上述内容外] Keep-O
P213/IRQ0_B/TI00_A/TI02_B/TO02_B/TXD1_A/SO11_A/SDAA0_B	高阻抗	[IRQ0_B 已选择] IRQ0_B 输入 [SDAA0_B 已选择] SDAA0_B 输入/输出 [除上述内容外] Keep-O
P300/SWCLK/TI04_B/TO04_B/SDAA0_E/TXD1_B	引体向上	[SDAA0_E 已选择] SDAA0_E 输入/输出 [除上述内容外] Keep-O

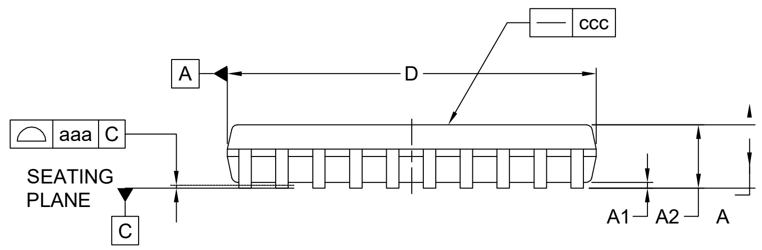
注：Hi-Z：高阻抗
Keep-O：输出引脚保持其先前的值。输入引脚变为高阻抗。

Appendix 2. Package Dimensions

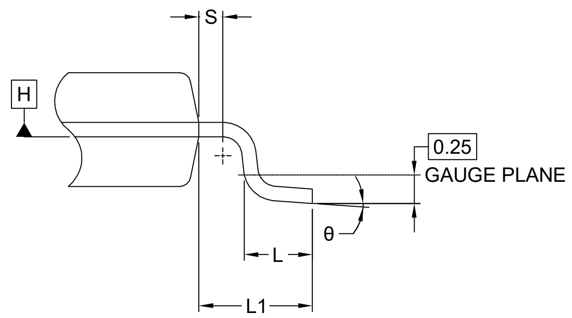
Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-TSSOP20-4.40x6.50-0.65	PTSP0020JI-A	0.08





Detail of Lead End



NOTES:
1.DIMENSION 'D' AND 'E1' DOES NOT INCLUDE MOLD FLASH.
2.DIMENSION 'b' DOES NOT INCLUDE TRIM OFFSET.
3.DIMENSION 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H.

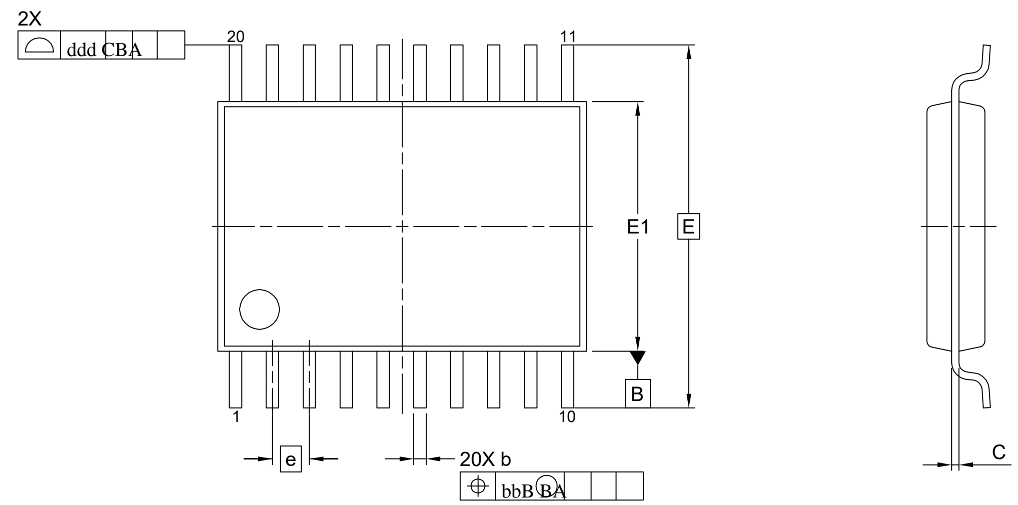
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
C	0.09	0.127	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.50	0.60	0.75
S	0.20	—	—
θ	0°	—	8°
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		

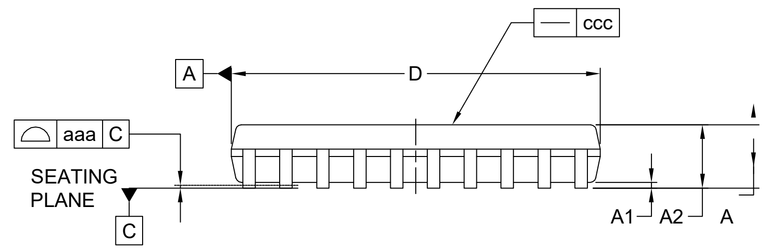
Figure A2.1 TSSOP 20-pin

附录 2.包装尺寸

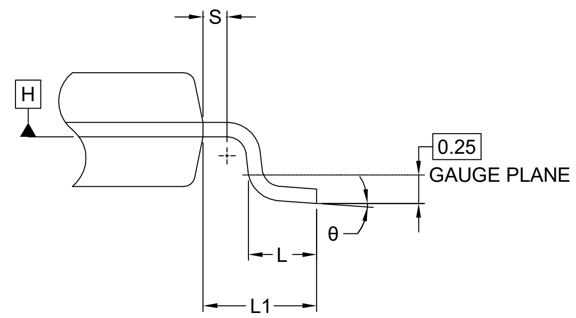
有关最新版本封装尺寸或安装方式的信息，请参阅瑞萨电子株式会社网站上的“封装”部分。

JEITA 包装代码	瑞萨斯代码	质量（典型值）[克]
P-TSSOP20-4.40x6.50-0.65	PTSP0020JI-A	0.08





引线端细节



NOTES:
1.尺寸“D”和“E1”不包括模具飞边。
2.尺寸“b”不包括修剪偏移量。
3.尺寸“D”和“E1”在基准面H处确定。

参考象征	尺寸单位为毫米		
	最小。	Nom.	最大限度。
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
C	0.09	0.127	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.50	0.60	0.75
S	0.20	—	—
θ	0°	—	8°
啊啊	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		

图 A2.1TSSOP 20引脚封装

Appendix 3. I/O Registers

This appendix describes I/O register addresses, access cycles, and reset values by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual.

Table A3.1 shows the name, description, and the base address of each peripheral.

Table A3.1 Peripheral base address

Name	Description	Base address
BUS	BUS Control	0x4000_3000
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
DBG	Debug Function	0x4001_B000
SYSC	System Control	0x4001_E000
IWDT	Independent Watchdog Timer	0x4004_4400
MSTP	Module Stop Control	0x4004_7000
CRC	CRC Calculator	0x4007_4000
PORT0	Port 0 Control	0x400A_0000
PORT1	Port 1 Control	0x400A_0020
PORT2	Port 2 Control	0x400A_0040
PORT3	Port 3 Control	0x400A_0060
PFS_A	Pmn Pin Function Select	0x400A_0200
PORGA	Product Organize	0x400A_1000
ADC_D	10-bit A/D Converter	0x400A_1800
SAU0	Serial Array Unit 0	0x400A_2000
TAU	Timer Array Unit	0x400A_2600
IICA	I^2C Bus Interface	0x400A_3000
TML32	32-bit Interval Timer	0x400A_3800
PCLBUZ	Clock Output/Buzzer Output Controller	0x400A_3B00
FLCN	Flash I/O Registers	0x407E_C000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

The following information applies to Table A3.2:

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus master such as DTC.

附录 3. I/O 寄存器

本附录按功能描述 I/O 寄存器地址、访问周期和复位值。

3.1 外围设备基地址

本节提供本手册中所述外围设备的基地址。

表 A3.1 显示了每个外围设备的名称、描述和基地址。

表 A3.1 外围设备基址

Name	描述	基地址
BUS	总线控制	0x4000_3000
DTC	数据传输控制器	0x4000_5400
ICU	中断控制器	0x4000_6000
DBG	调试功能	0x4001_B000
SYSC	系统控制	0x4001_E000
IWDT	独立看门狗定时器	0x4004_4400
MSTP	模块停止控制	0x4004_7000
CRC	CRC计算器	0x4007_4000
PORT0	端口 0 控制	0x400A_0000
PORT1	端口 1 控制	0x400A_0020
PORT2	端口 2 控制	0x400A_0040
PORT3	端口 3 控制	0x400A_0060
PFS_A	PMN引脚功能选择	0x400A_0200
PORGA	产品组织	0x400A_1000
ADC_D	10位模数转换器	0x400A_1800
SAU0	串行阵列单元 0	0x400A_2000
TAU	定时器阵列单元	0x400A_2600
IICA	I2C总线接口	0x400A_3000
TML32	32 位间隔定时器	0x400A_3800
PCLBUZ	时钟输出/蜂鸣器输出控制器	0x400A_3B00
FLCN	闪存 I/O 寄存器	0x407E_C000

注意：名称= 外围设备名称
描述=外围功能
基地址=最低保留地址或外围设备使用的地址

3.2 访问周期

本节提供本手册中描述的I/O寄存器的访问周期信息。

以下信息适用于表 A3.2：

- 寄存器按关联模块分组。
- 访问周期数表示基于指定参考时钟的周期数。
- 在内部I/O 区域中，未分配给寄存器的保留地址不得访问，否则无法保证操作。
- I/O访问周期数取决于内部外设总线的总线周期、分频时钟同步周期以及每个模块的等待周期。

注意：这适用于 CPU 访问与从外部存储器获取指令或从其他总线主控器（如 DTC）访问总线不冲突时的周期数。

Table A3.2 shows the register access cycles.

Table A3.2 Access cycles

Peripherals	Address		Number of access cycles			
	From	To	Read	Write	Cycle unit	Related function
BUS, DTC, ICU, DBG	0x4000_3000	0x4001_BFFF	3		ICLK	Buses, Data Transfer Controller, Interrupt Controller, CPU, Flash Memory
SYSC	0x4001_E000	0x4001_E6FF	2		ICLK	Low Power Modes, Resets, Low Voltage Detection, Clock Generation Circuit, Register Write Protection
IWDT, MSTP	0x4004_0000	0x4004_7FFF	3		PCLKB	Watchdog Timer, Module Stop Control
CRC	0x4007_4000	0x4007_4FFF	3		PCLKB	CRC Calculator
PORT, PFS_A, PORGA, ADC10, SAU0, TAU, IICA, TML32, PCLBUZ	0x400A_0000	0x400A_3FFF	2		PCLKB	I/O Ports, 10-bit A/D Converter, Serial Array Unit 0, Timer Array Unit, I^2C Bus Interface, 32-bit Interval Timer, Clock/Buzzer Output Controller
FLCN	0x407E_C000	0x407E_FFFF	7		ICLK	Flash Control

表 A3.2 显示了寄存器访问周期。

表 A3.2 访问周期

外围设备	地址		访问周期数			
	从	To	读	写	循环单元	相关功能
BUS、DTC、ICU、DBG	0x4000_3000	0x4001_BFFF	3		ICLK	总线、数据传输控制器 中断控制器、CPU、闪存 记忆
SYSC	0x4001_E000	0x4001_E6FF	2		ICLK	低功耗模式、重置、低 电压检测，时钟生成 电路寄存器写保护
IWDT，MSTP	0x4004_0000	0x4004_7FFF	3		PCLKB	看门狗定时器，模块停止控制
CRC	0x4007_4000	0x4007_4FFF	3		PCLKB	CRC计算器
端口、PFS_A、PORGA、ADC10、SAU0、TAU、IICA、TML32、PCLBUZ	0x400A_0000	0x400A_3FFF	2		PCLKB	输入/输出端口、10 位模数转换器、串行接口 数组单元 0，定时器数组单元，I^2C总线 接口，32 位间隔定时器，时钟/ 蜂鸣器输出控制器
FLCN	0x407E_C000	0x407E_FFFF	7		ICLK	闪光控制

Appendix 4. Peripheral Variant

Table A4.1 shows the correspondence between the module name used in this manual and the peripheral variant.

Table A4.1 Module name vs peripheral variant

Module name	Peripheral variant
ADC10	ADC_D

附录 4.外周变异

表 A4.1 显示了本手册中使用的模块名称与外围设备型号之间的对应关系。

表 A4.1 模块名称与外围设备变体

模块名称	外周变异
ADC10	ADC_D

Revision History

Revision 1.00 — Oct 29, 2025

Initial release

修订历史

版本 1.00 — 2025 年 10 月 29 日

初始版本

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

微处理器和微控制器产品处理的一般注意事项

以下使用说明适用于瑞萨电子的所有微处理器和微控制器产品。有关本文档所涵盖产品的详细使用说明，请参阅本文档的相关章节以及针对这些产品发布的任何技术更新。

1. 防止静电放电 (ESD)

强电场作用于CMOS器件时，会破坏栅极氧化层，最终导致器件性能下降。必须采取措施尽可能防止静电产生，并在静电产生时迅速将其消散。环境控制必须到位。干燥时，应使用加湿器。建议避免使用容易积聚静电的绝缘材料。

半导体器件必须存放在防静电容器、防静电屏蔽袋或导电材料中，并进行运输。所有测试和测量工具，包括工作台和地面，都必须接地。操作人员也必须佩戴接地腕带。半导体
devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. 开机处理

通电时，产品的状态未定义。LSI内部电路的状态不确定，寄存器设置和引脚的状态在通电时也未定义。在成品中，如果复位信号施加到外部复位引脚，则从通电到复位过程完成期间，引脚的状态无法保证。同样，对于通过片上上电复位功能复位的产品，从通电到电源达到复位所需的电平期间，引脚的状态也无法保证。

3. 断电状态下的信号输入

设备断电时，请勿输入信号或 I/O 上拉电源。输入此类信号或 I/O 上拉电源产生的电流注入可能导致设备故障，此时流经设备的异常电流可能会损坏内部元件。请遵循产品文档中关于断电状态下输入信号的指导原则。

4. 未使用引脚的处理

请按照手册中“未使用引脚的处理”部分所述步骤处理未使用的引脚。CMOS 产品的输入引脚通常处于高阻抗状态。如果将未使用的引脚置于开路状态，则会在 LSI 附近感应出额外的电磁噪声，导致内部产生直通电流，并且由于引脚状态被错误识别为输入信号，可能会引发故障。

5. 时钟信号

复位后，只有在工作时钟信号稳定后才能释放复位线。在程序执行期间切换时钟信号时，请等待目标时钟信号稳定后再进行操作。如果在复位期间时钟信号由外部谐振器或外部振荡器产生，请确保仅在时钟信号完全稳定后才释放复位线。此外，在程序执行过程中切换到由外部谐振器或外部振荡器产生的时钟信号时，也请等待目标时钟信号稳定后再进行操作。

6. 输入引脚上的电压施加波形

输入噪声或反射波引起的波形失真可能导致故障。例如，如果由于噪声导致CMOS器件的输入电压停留在V_{IL}（最大值）和V_{IH} (Min.) 之间的区域，则器件可能会发生故障。当输入电平固定时，以及输入电平在V_{IL}（最大值）和V_{IH}（最小值）之间的过渡期间，应注意防止抖动噪声进入器件。

7. 禁止访问保留地址

禁止访问保留地址。保留地址仅供未来功能扩展之用。请勿访问这些地址，否则无法保证LSI的正常运行。

8. 产品之间的差异

在更换产品之前，例如更换为不同部件号的产品，请务必确认更换不会导致任何问题。即使是同一组但部件号不同的微处理器或微控制器单元产品，其内部存储容量、布局模式和其他因素也可能存在差异，这些差异会影响电气特性范围，例如特性值、工作裕度、抗噪声能力和辐射噪声量。更换为不同部件号的产品时，请对该产品进行系统评估测试。

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